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Sub Sea Power Electronics

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Problem Description

Fully submerged sub sea compression units in the several megawatt range are important to maintain reservoir pressure as the gas is extracted from a gas field. Electric motor drives are suitable for this kind of application, and existing solutions are available where the power electronics are encapsulated in thick walled tanks holding 1 atmosphere. As new gas fields are discovered at continually deeper waters, this tank is becoming costly and the interest for a new solution is increasing. A suggested solution is to encapsulate the power electronics in a tank with thin flexible walls and completely fill it with insulating oil allowing the pressure on the inside to be the same as on the outside. For this solution to work, the power electronic components must be compatible with oil and function under high hydrostatic pressure.

Some suitable electrical drive systems should be investigated for a high voltage sub sea compression application. The most likely to be used power semiconductor, the IGBT, is to be investigated in detail with suggested state of the art modules available from manufacturers. Description on how these modules are made and how the characteristics are improved is included in the theory along with packaging and discussion around if it is possible to apply hydrostatic pressure on the housings.

A description of the most important components in an experiment set up must be done. This for investigating compatibility of an IGBT module with silicon oil follows with test results by comparing characteristic waveforms obtained when operated in room environment and fully submerged.

The candidate should:

- Investigate suitable electric drives systems for the compression application.
- Include theory around the IGBT and available modules on the marked.
- Discuss whether or not some of these modules are suitable for high hydrostatic pressure applications.
- Construct a lab setup for testing compatibility of an IGBT module with silicon oil and document the results.

Assignment given: 22. January 2007
Supervisor: Tore Marvin Undeland, ELKRAFT

Preface

This master thesis is a continuance of the project report “Sub Sea Power Electronics”, and consists of a literature study and documentation from an experiment performed at the power electronics test laboratory at NTNU.

The thesis was initiated and financed by Norsk Hydro represented by Dr.ing. Snorre Frydenlund, and executed by graduate student Andreas H. W. Kristoffersen.

The report suggests solutions for power electronic drives at deep waters for a compression application, and theory around some of the semiconductor switches that may be used. The practical experiment investigates how a transistor behaves when fully submerged in oil and operated in a converter bridge configuration.

I would like to take this opportunity to thank people that have influenced my work.

Professor Dr.ing. Tore M. Undeland has been my advisor and supported me during my work.

Dr.ing. Snorre Frydenlund works for Norsk Hydro and has been my contact person with the initiators of the project. He has provided me with useful information and has also made sure that the finances were taken care of.

Magnar Hernes works for SINTEF Energy Research and is the project leader for the experimental set up.

Kjell Ljøkelsøy works for SINTEF Energy Research and was my laboratory partner through the whole project. With his knowledge and experience in practical work, a lot of time was saved during fail seeking and set up of the system.

All these people did not hesitate to help me whenever I stopped by or contacted them, and have been very supportive and helpful with my work.

Trondheim, June 12 2007

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Andreas H. W. Kristoffersen

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Abbreviations

$\%THD_v$	:	Total harmonic voltage distortion
A	:	Ampere
AC	:	Alternating current
AFE	:	Active front end
BJT	:	Bipolar junction transistor
DBC	:	Direct bonded copper
DC	:	Direct current
EP-IGBT	:	Enhanced planar insulated gate bipolar transistor
ESR	:	Equivalent series resistance
IEGT	:	Injection Enhanced Gate Transistor
IGBT	:	Insulated gate bipolar transistor
JFET	:	Junction gate field effect transistor
MLC	:	Monolithic capacitor
MOSFET	:	Metal oxide semiconductor field effect transistor
NPC	:	Neutral point clamped
NPT	:	Non punch through
PCB	:	Printed circuit board
PWM	:	Pulse width modulation
Rms	:	Root mean square
SOA	:	Safe operating area
SPT	:	Soft punch through
V	:	Volts
VSC	:	Voltage source converter
VSI	:	Voltage source inverter

Abstract

Sub sea compression for maintaining reservoir pressure in a gas field is important to have a steady production of gas as it is extracted from the field. Electrical drives in the several megawatt range are suitable to control the compressor motor since it is not desirable to have gears which need maintenance. Problems related to the location on the sea bed have so far been overcome by using massive pressure tanks which hold 1 atmosphere. A new approach would be to allow the pressure on the sea bed to be applied on the electrical components. This will reduce and simplify the system only needing a thin walled casing filled with oil to contain the electronics, but the electronic components then need to be compatible with the oil and function at high hydrostatic pressure. This report include suitable electrical power systems for a compression application, theory around the most likely to be used switch, some available modules and an experimental set up for testing IGBT compatibility with oil.

Converters consisting of rectifiers and inverters are widely used in industrial motor drives and it is assumed that such a converter will be used consisting of a diode bridge rectifier and a neutral point clamped inverter. High voltage applications often operate with voltages above the rated value of many semiconductor components which means that switches must be series connected. A neutral point clamped inverter with series connected switches will be able to handle the high voltages and produce a good spectral output to the motor terminals.

The switches used in the inverter will probably be IGBTs. The IGBT evolved as the most successful device for high power, high switching frequency applications blending MOSFET switching capabilities with BJT on-state conduction properties. Development has produced a lot of versions of this kind of switch, and by modifying doping profiles and geometrical properties a set of devices with improved characteristics has been made. Packaging techniques make it possible to integrate the switches in different environments. Examples are the press pack modules which can be hermetically sealed and the standard DBC solutions.

To test compatibility with insulating oil, an experiment was set up. An IGBT inverter leg module was placed inside a tank which was filled with oil. The module was operated in an H-bridge configuration with another bridge leg on the outside of the tank. Thorough testing before submerging it was performed to ensure and document normal behaviour. When fully submerged the module was tested and the results compared with those from the initial testing. Short duration of continuous switching was also performed followed by intermittent operation with current pulses and long term continuous switching. None of the captured scope pictures or temperature measurements showed deviation from normal IGBT behaviour or change of characteristics. It can then be concluded that when submerging an IGBT module in insulating oil, no instant failure or change of electrical behaviour occurs.

1 Introduction

Oil and gas installations on the sea bed saves a lot of money compared to traditional platforms on the surface. Both environmentally and economically, there are a lot of benefits by putting components on the sea bed, but it also arises some challenges that need to be solved to get a reliable and efficient system. One of these challenges related to natural gas production is the need for a compressor unit in the several MW range on the sea bed to maintain production pressure in the reservoir as the gas is extracted from the field. Since access to the unit for maintenance is limited, the system should be as reliable as possible.

A compressor unit with electrical drives to control the performance is suggested as a good solution, but when placed on the sea bed, there is major difference in the working environment for the electronic components which are designed for surface conditions. A way to cope with this problem is to encapsulate the components in a tank holding one atmosphere and fill it with a fluid. This solution is used today, but as the depths increase along with larger physical size of the drives, the tank and penetration for wiring will become expensive. As an alternative, the tank could be completely filled with insulating oil with walls allowing the pressure on the inside to be the same as on the outside. The work in this report is based on that alternative and some aspects around it are investigated.

It will be briefly discussed different electrical drive configurations that may be suitable. Thorough investigation of the most likely to be used semiconductor switch, the IGBT will be given and available modules will also be presented with some of the theory leading to these state of the art devices. Switches and configurations involving power electronic components are the main focus and signal level devices will not be investigated. Description and documentation from the experimental set up where an IGBT power module is tested when fully submerged in oil will be given along with suggestion for further work.

The initial plan was to investigate the behaviour of the transistor under high hydrostatic pressure with an available pressure tank used for similar tests previously, but because of new rules and regulations along with lack of necessary documentation of the available pressure tank, the tank could not be used. Since this was a late discovery within the time frame of this project a compromise had to be made to get some results. The module was only tested submerged in silicon oil instead to test and verify that it will function when completely covered. This was a step back from the initial goal, but still an important step on the way.

2 System description

The work throughout this report will be narrowed down to closely investigate one type of power semiconductor. The initial chapters will however introduce the systems where these kinds of semiconductors can be used and that are most likely to be chosen in the final decision.

As described in [1] there are several possibilities when deciding what kind of converter topology which will suit the sub sea compression application best. The final decision will have to take into account all the technical details as well as economical and environmental issues. However, the industry has some solutions that are commonly used and perhaps more likely to be chosen than others. The VSI is well known and has proven to be both robust and reliable. NPC inverters also features these qualities and especially for high voltage applications. Since the choice is not made yet, it will be assumed that the converter topology will be a diode bridge based rectifier and a NPC inverter with IGBTs. This assumption corresponds with the assumptions of the initiators of the project [2]. A simplified drawing of the assumed system with diode rectifier and NPC inverter is presented in Fig 2.1. The figure only shows the power modules. Signal level devices in the control logic are left out since these are not the main scope of interest.

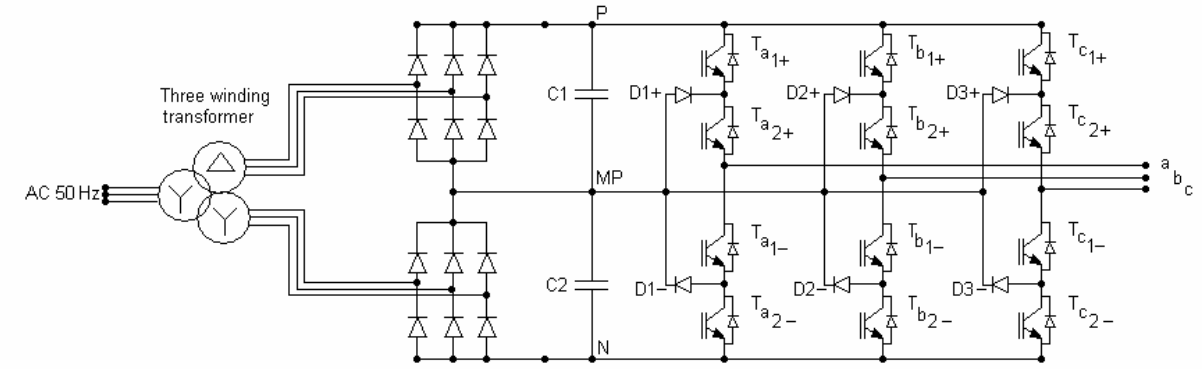

Fig 2.1 System description

Other possible solutions can be found in [1] where a short description of NPC and some other multilevel inverters are presented. Detailed information on other multilevel configurations can be found in [3].

2.1 Diode bridge rectifier

The diode rectifier bridge rectifies the sinusoidal voltages from the secondary and tertiary side of the three winding transformer to a DC-voltage with some ripple. In a 12 pulse configuration the output from the rectifier bridges will be as shown in Fig 2.2. Voltage from the supply is transformed through the three winding transformer where one of the secondary outputs is phase shifted 30 degrees. Each diode bridge produces a 6 pulse output phase shifted 30 degrees with respect to each other. When combined on the DC-link, a 12 pulse output is obtained. To further improve the DC-voltage supply for the inverter, a capacitor bank is installed between the positive- and the negative DC-bus.

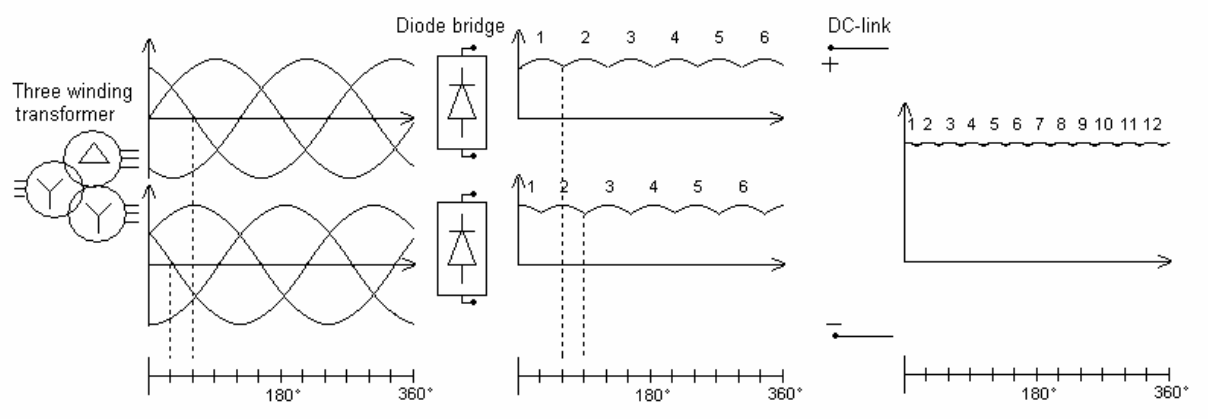

Fig 2.2 Waveforms through rectification

Because of the 12 pulse configuration, the harmonic currents drawn from the main bus is significantly reduced. The dominant harmonics will be around the multiples of 12 i.e. 11^{th} and 13^{th}, 23^{rd} and 25^{th} and so on. The other harmonics will be cancelled out to a negligible degree. This is in most applications enough to fulfil the %THDv requirements stated by the Bureau Veritas in Norway or the American Bureau of Shipping in USA or other official authorities for classifications of offshore and maritime installations. A typical %THDv limit can be 5% on the main bus with no single harmonic larger than 3% up to the 100^{th} [4].

If the 12 pulse configuration does not meet the requirements, a 24 pulse configuration can be used. With 24 pulse output on the DC-link, the dominant harmonics will be around the multiples of 24 with the first ones at 23^{rd} and 25^{th}. This will significantly reduce the total harmonic content in a typical installation and in most cases be more than sufficient to fulfil the requirements.

One way to obtain 24 pulse output is to use four diode bridge rectifiers and two three winding transformers. The three winding transformers primary sides then have to be phase shifted with respect to each other. A zigzag configuration on the primary side makes this possible as shown in Fig 2.3.

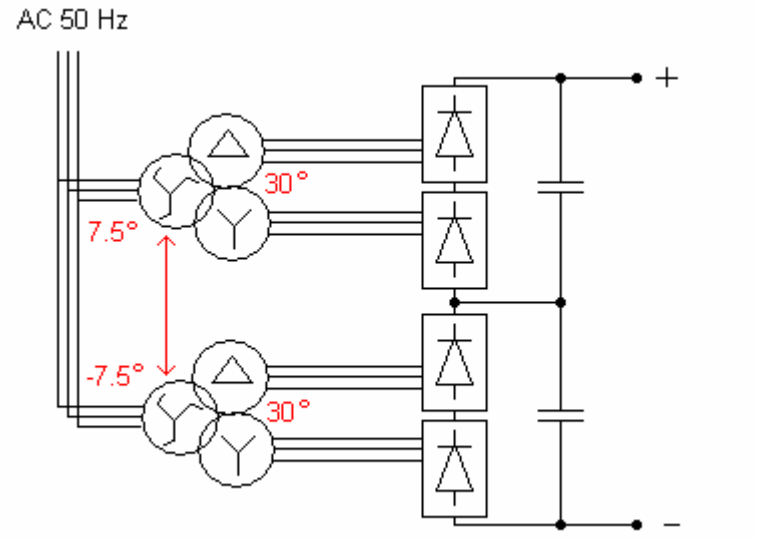

Fig 2.3 Configuration with 24 pulse output

The reason for wanting to reduce the harmonic distortion is to protect other sensitive equipment connected to the same network. If all other components connected are tolerant to higher levels of harmonic distortion, the %THDv can be allowed higher than previously stated. This is in fact the case for the planned sub sea compression application where the other consumers connected to the same isolated network all consist of components with a higher tolerance for harmonic distortion.

2.2 NPC inverter

The rectified output from the diode bridges serves as input to the inverter where the frequency and amplitude of the output can be controlled. The three-level, so called neutral point clamped, inverter has the advantage of dividing the maximum amplitude of the output voltage into two steps. This reduces the harmonic content and the line to line output achieves a very high content of the fundamental component. It also reduces iron losses in the motor. Other advantages are the ease of control where the gating electronics is very simple, no snubber circuit is necessary and that each switch is protected from the large DC-link voltage by the clamping diodes [3].

Line to line output in a NPC-inverter has five different voltage levels. These levels are obtained by the degree of freedom of switch statuses which allows the output to be switched via the neutral point. Compared to a two level inverter the NPC has 25 possible switching conditions whereas the two-level has 7 [5]. The output waveforms from a two-level inverter and a three-level inverter are plotted along with the fundamental component in Fig 2.4. It is clearly evident that the three-level output has a higher content of the fundamental component.

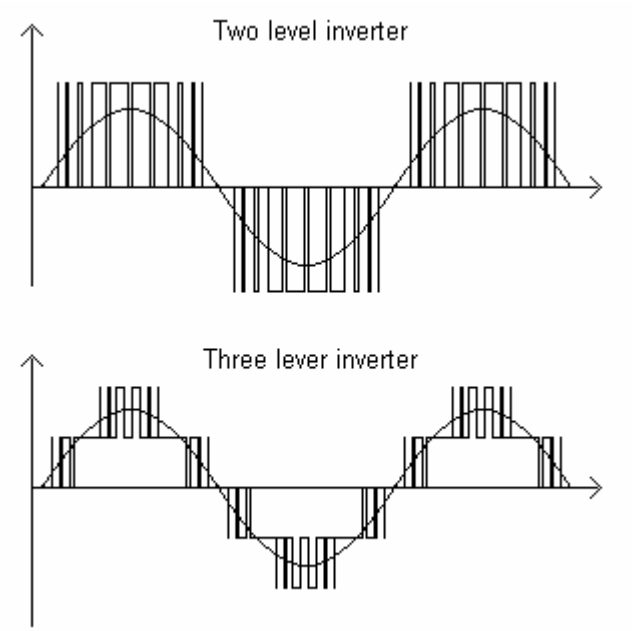

Fig 2.4 Voltage waveforms of two- and three-level inverter

There are a number of switching schemes available for a three-level inverter. One example is asynchronous sinusoidal PWM where the frequency of the triangular signal is kept constant. Other forms of PWM with vector control are also developed and are commonly used.

2.3 Active front end

Although it has previously been stated that the %THDv level can be allowed higher in the isolated network which the compressor unit is to be connected, the possibility of further lowering the harmonics is present by using an active front end.

The current fed to the motor from a three level inverter is near perfect and this feature is exploited for improving supply side current wave-shape. Using an identical converter configuration for the line-side rectifier a four-quadrant drive-converter configuration is created, that not only draws near perfect sinusoidal current from supply line, but also allows smooth reversal of power flow to provide motoring and regenerative braking. AFE uses fast internal switching together with an input choke. The AFE is commutation fault proof, which means no blown fuses with brown or black outs. A stable DC-link voltage is maintained even on very weak power supplies and at severe voltage dips. The configuration is illustrated in Fig 2.5 [5].

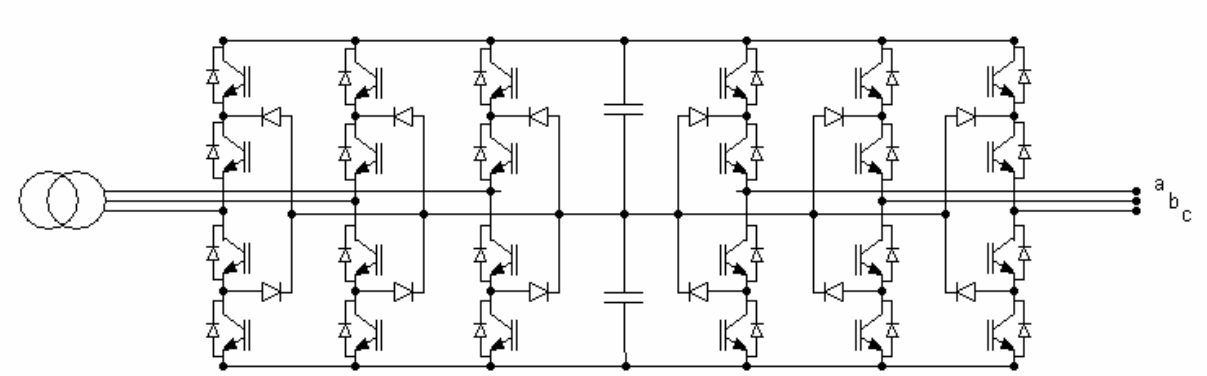

Fig 2.5 IGBT inverter with active front end

Should the mains dip during regeneration, the energy returned to the supply is maintained because the current increases proportional to the voltage decrease. This allows maintaining full capacity and speed even during phases of fluctuating supply voltage. The AFE is dimensioned so that even voltage increases associated with regeneration into weak supplies are trouble-free. Safe current limiting is also possible if the AFE regenerates into a short circuit [5].

Another feature of the AFE is power factor control in both motoring and regenerative mode. As standard, the AFE can compensate for system power factor in two power factor correction modes. It can either ensure constant VAr or constant power factor. In the constant VAr mode a percentage, 0% to 100%, of the AFE current capacity is utilized as a reactive current, leading or lagging, and the reactive current is independent of the motor load. However, in the constant power factor mode the power factor is set in the range 1.0 to 0.8 leading or lagging and the reactive current is dependent of the motor load. The power factor or VAr requirement is set as a fixed value on a parameter or a variable value changed via a communication bus or analogue input. This feature can be taken advantage of for compensation of other inductive or capacitive loads connected to the same line [5].

Whenever the drive is running at an output below its design rating the remaining reactive power can be used for compensation. This can also be designed by adequate selection of the respective converter size. Only the AFE rectifier and the DC-link capacitors have to be matched to the expected reactive power demand. This is of essential importance for networks,

which due to weight and size of the electrical equipment have do be optimized most carefully with respect to the ratio of real power versus reactive power load. Ship propulsion and auxiliary drives or equipment on platforms are typical examples [5].

2.4 High voltage applications

With high voltage applications, the three-level configuration with the clamping diodes effectively protects the IGBTs from getting all the DC-link voltage across the collector and emitter. Some applications might require even higher voltage levels above the rating of what is available of IGBTs. A solution is to series connect two IGBTs and operate the pair as one switch. The three-level configuration can still be used, but with some extra control that ensures that the switches switch simultaneously. The three level inverter with two series connected IGBTs operated as one switch is shown in Fig 2.6.

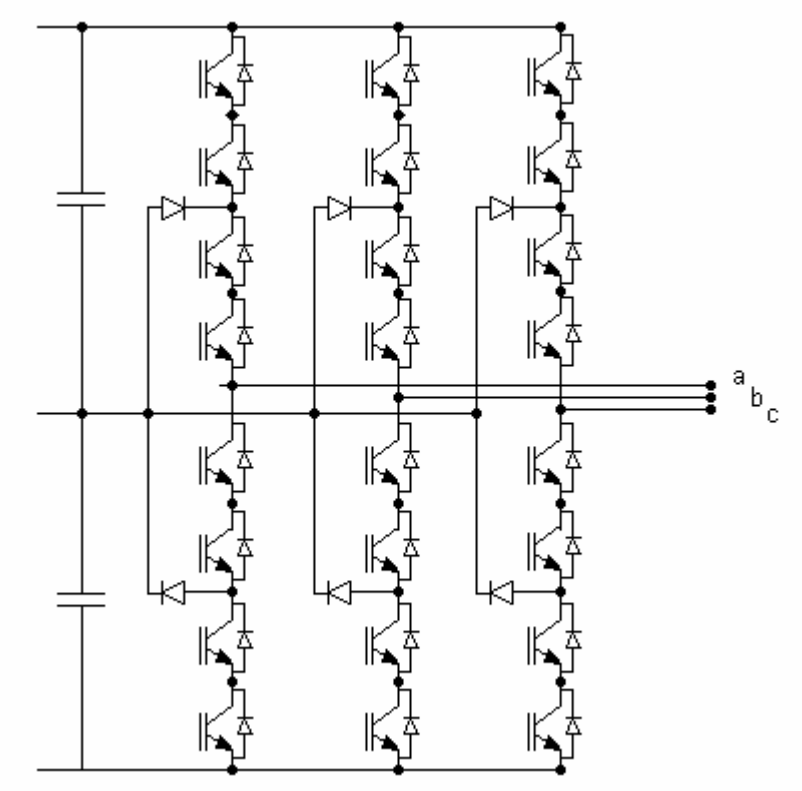

Fig 2.6 Three level inverter with series connection of IGBTs

There have been developed several different approaches to ensure even voltage dividing between the switches operating in series. A first approach is based on the use of turn-off snubbers in parallel to each device in order to force the slope of the voltage variation across them to be dominated by the charge of the capacitance and hence to become independent on the devices switching times. Dynamic voltage sharing can also be achieved with capacitors in parallel with the switches.

2.4.1 Voltage sharing between IGBTs in series

Test results from experiments with switches in series shows that the faster device will have all the supply voltage applied over its terminals for a short duration. This may bring the device out of its safe operating area. Although the switches are equal and the driving circuits are the same, the switching will not happen exactly at the same time. Parameter deviations within a

population of devices are inevitable, and when the number of components increases it is almost definite that the switching will not be exactly at the same time. The concept of voltage sharing with capacitors in parallel with the switches is investigated in [6], and the topology is reproduced in Fig 2.7.

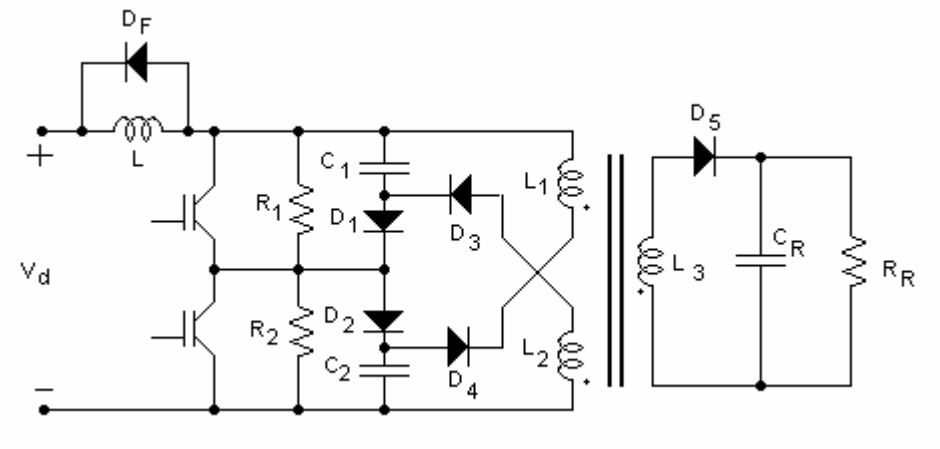

Fig 2.7 Schematics of the circuit used for the series connection of two IGBTs

In the figure, the load inductance and the freewheeling diode are L and D_F, respectively. The resistances R_1 and R_2 provide for a uniform steady state voltage distribution, whereas the remaining part of the circuit is used to evenly share the voltage among the devices during switching operations.

If the upper switch is slightly faster than the lower switch, the load current is forced to charge the capacitance C_2. If the duration of the period of which the upper switch is on and the lower switch is off is small enough combined with a large capacitance of C_2, the voltage over the lower switch will be kept at about ½ V_d. When the lower switch turns on each capacitor is in parallel with one of the primary windings of the transformer through the diodes D_3 and D_4. C_2, which has accumulated more energy than C_1, will transfer this energy to the inductor, L_1, and the voltage over C_2 will decrease while the current through L_1 increase linearly. When the faster upper switch turns off, the load current is forced to charge C_1, holding a voltage of approximately ½ V_d over the slower lower switch. When this switch turns off, the energy stored in the transformer will be transferred to the secondary side through R_R [6].

Another interesting approach makes use of active driving circuits which sense the voltage across each device and are able to affect their switching times in order to avoid unbalance of the voltage among them. More detailed information about this approach can be found in [7]

3 Semiconductors and switches

For an industrial electrical motor drive, there are many switches that are available on the marked today ranging from low power single units to high power modules.

Ideally, a semiconductor switch should possess all the characteristic features listed in Table 3.1 [8]. Although advances in power devices have revolutionized power electronics, there is by today still not a single switch which possesses all these characteristics. However, there is a wide spectrum of devices intended for different applications where a fair degree of similarity with some of the characteristics in Table 3.1 is obtained. An example is the thyristor, which can carry large currents in the forward direction, in the area of several kA, with less than 2 V voltage drop. It is also capable of blocking very large voltages in the reverse direction, in the area of more than 6 kV. A major drawback with the thyristor is that the turn-off is obtained by collector-emitter voltage reversal.

In applications where the load current is turned on and off by the input signal, power bipolar junction transistors (BJT) have been extensively used. A drawback with this device is the need of a high base current drive both in on-state and during turn-off, but the on state losses are very small.

The gate turn off thyristor (GTO) is another device that is able to turn on and off the load current, but with higher forward current capabilities. The drawback of this device is the excessively higher drive current along with limitations in switching frequency.

Table 3.1 Characteristics of a perfect switch

Very low or zero driving losses	Obtained with high input impedance so that the drive current is infinitesimally small. Furthermore, the drive circuit should be simple an inexpensive.
Insignificant on-state or forward conduction losses	The forward voltage drop should be zero at the operating current. Additionally the operational current density large, making the chip small in size and cost effective for a given current-carrying capability
Minimal off-state or reverse blocking losses	The reverse blocking capability should be infinitely large even when exposed to elevated temperatures.
Extremely low switching losses	Both the turn-on and turn-off times should approach zero.

Other devices with gate turn-off capabilities evolved from the progressive development of the existing devices and include the integrated gate commutated thyristor (IGCT) and different types of metal oxide semiconductor field effect transistors (MOSFET). MOSFETs have high switching frequency capabilities along with ease of drive and capability to withstand high rates of rise in the on-state voltage. A major drawback is larger on-state losses and the limitations in voltage ratings because the device operates by unipolar conduction. With increasing voltage ratings, the inherent reverse diode shows increasing reverse recovery time causing more switching losses [8].

To obtain features closer to those listed for a perfect switch; it was worthwhile blending the properties of MOSFETs and bipolar devices. After some development, the insulated gate bipolar transistor (IGBT) evolved as the most successful device combining the best from each type. Another semiconductor worth mentioning is the injection enhanced gate transistor, the IEGT which is closely related to the IGBT, and shows excellent forward conduction capabilities.

The switches in the inverters discussed so far are illustrated as IGBTs, but could be one of the other types as well. IGCT is an alternative that could be argued is the best and it is hard to say if that is the case. A limitation with this device is that the gate driver must be as close as possible to the gate since en extremely large current is drawn out to turn it off. With large physical distance, the inductance in the wires would cause high voltage that could destroy the device. This means that it is hard to physically separate the control logic from the power semiconductor which limits the degree of freedom when placing components in the system. Because of the large power and switching requirements the switches will most probably be power IGBTs in the final solution. Simple gate control and low on state losses are other arguments for using the IGBT. Because the IGBT is the most likely to be used switch, the theory presented will focus on features and characteristics around this kind of transistor.

4 Insulated gate bipolar transistor

As a reference for subsequent experiments and to fully understand the mechanisms and processes leading to the results, theory around the IGBT is presented in this chapter.

Fig 4.1 [8] shows, schematically, the cross section of the basic IGBT structure. This is one of the several structures possible for this device. In practice, the power IGBT essentially comprises a repetitive array of millions of unit cells, where one cell labelled red in the figure can be seen.

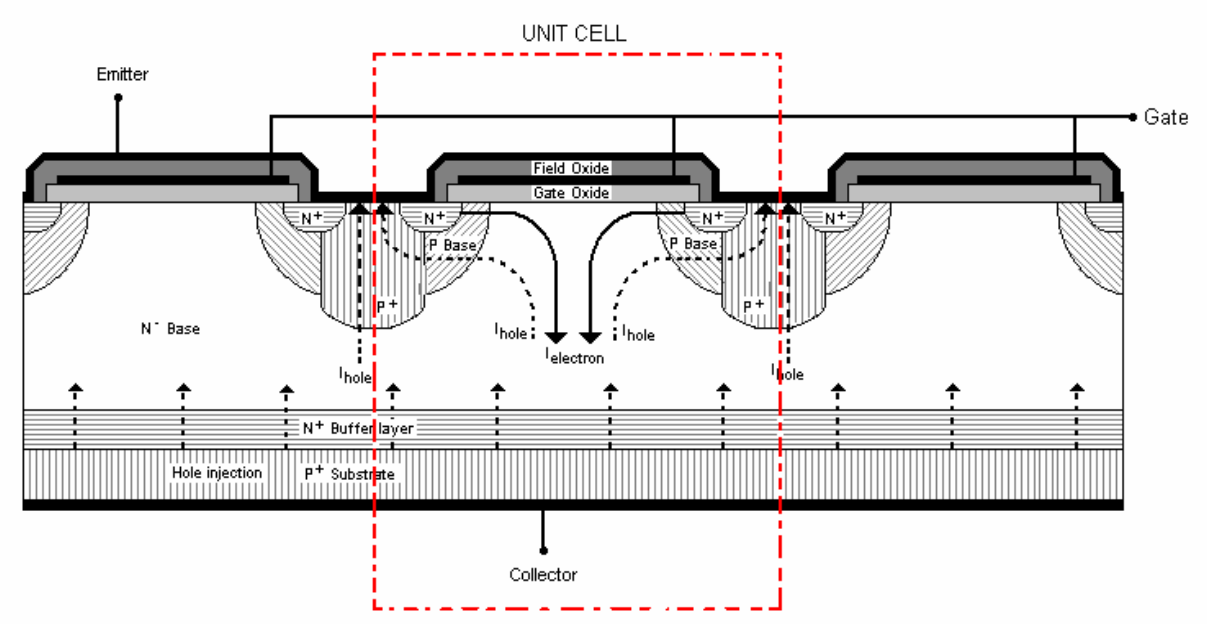

Fig 4.1 Cross section of the basic IGBT structure

As illustrated in Fig 4.1, the IGBT is made up of several different layers. The top N^+ layer is the emitter, and the bottom P^+ layer is the collector. Between the emitter and the collector there are two base regions known as the P-base and the N-base. In the illustrated figure the P-base also includes P^+ wells that penetrate deeper into the N-base. The N-base is often referred to as the N^- drift region, and the thickness and resistance of the N-type material between the P wells control the voltage rating. In addition, there is an N^+ buffer layer on top of the P^+ collector layer. This layer is not essential, but including this layer introduces a feature that is well suited in some applications. This will be further discussed in a subsequent chapter.

Current paths are also included in Fig 4.1, where the dotted lines represent movement of holes while the continuous lines indicate electron movement.

4.1 Equivalent circuit representations

A clear perception of IGBT operation can be obtained by examining its equivalent circuit. A close investigation of the cross sectional illustration in Fig 4.1 reveals a pair of NPN and PNP transistors forming a parasitic thyristor. The collector of the NPN transistor is connected to the base of the PNP transistor, and likewise the collector of the PNP transistor supplies the

base current for the NPN transistor through a JFET which represents the constriction of current between any two neighbouring IGBT cells. The equivalent circuit can be drawn as shown in Fig 4.2, where the resistance R_s represents the shorting resistance between the base of the NPN transistor and the emitter. Emitter-base shorting is essential to ensure that the sum total gain of the NPN and PNP transistors does not exceed unity which will cause latch up of the parasitic thyristor. Furthermore, the MOSFET channel is formed in the P base below the gate oxide. This channel joins the N^+ emitter and N^- collector of the NPN transistor, so this transistor is shunted by a MOSFET in the equivalent circuit [8].

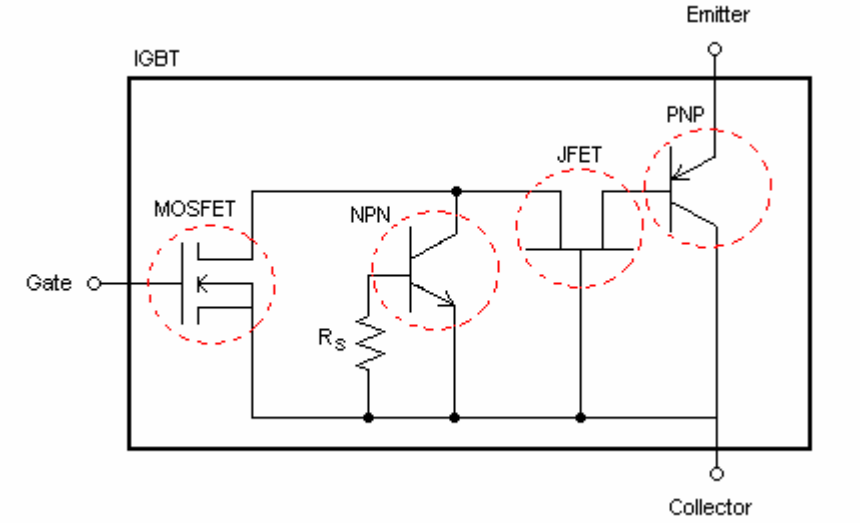

Fig 4.2 Equivalent circuit models of IGBT

Simplifications in the equivalent circuit can be obtained by looking at the emitter-base shorting. For normal operation, it is absolutely necessary that the NPN-transistor does not turn on, and this is avoided by shorting the base of the NPN transistor and the emitter. This will effectively reduce the probability of the NPN transistor to turn on to a negligible degree, and thus the equivalent circuit can be simplified to that shown in Fig 4.3 [8].

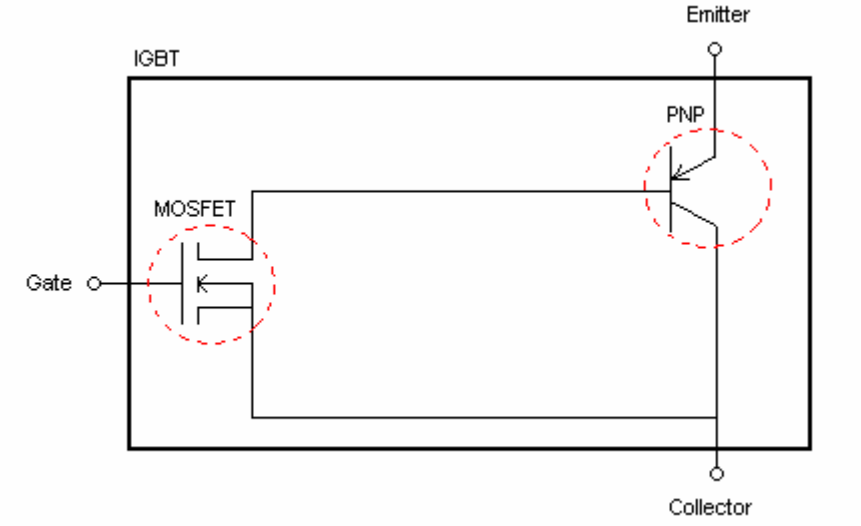

Fig 4.3 Simplified equivalent circuit model of IGBT

The configuration in Fig 4.3 can be viewed as an N-channel enhancement mode MOSFET driving a PNP bipolar transistor.

4.2 Principal of operation

With zero gate bias applied, the IGBT structure shown in Fig 4.4, is equivalent to a PNPN break-over diode having an emitter short. The IGBT remains off when the collector is at a higher potential than the emitter. This is because the junction, J_2, between the P-base and N^- drift region is reversed biased. Similarly, the IGBT remains in the off state when the collector-emitter voltage is less than zero, due to reverse bias across the junction, J_1, between P^+ substrate and N^- drift region layer.

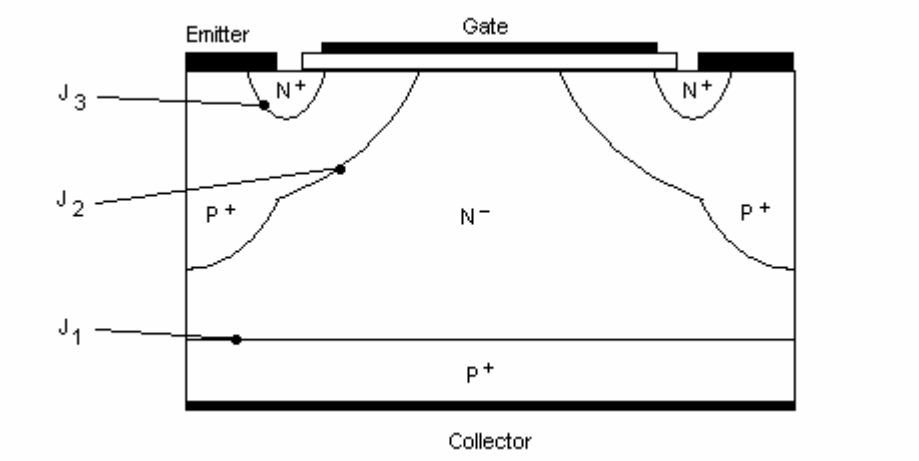

Fig 4.4 IGBT structure

With positive collector-emitter voltage, the IGBT can be turned on by applying a positive gate-emitter voltage. The positive gate-emitter voltage induces an N-channel in the underlying P region, thereby connecting the N^+ emitter with the N^- base. The junction, J_1, is then forward biased and hole-injection from the P^+ collector substrate into the N^- base starts. Consequently, conductivity modulation of this layer takes place, reducing its resistance and bringing about a large flow if collector emitter current

To turn off the IGBT, the gate-emitter voltage is made zero so that the channel in the P region is removed. Depending on the value of the collector-emitter voltage, V_{ce}, three different regions of operation are observed in the IGBT. In the first regime, at a small value of V_{ce}~0.7 V, the IGBT is a vertical diffused MOSFET in parallel with a PNP transistor. Current transport takes place by recombination of excess electrons and holes in the N^- region. The second regime commences from V_{ce} >0.7 V where the characteristics portray MOSFET behaviour. At high V_{ce} values, the excess holes injected from the emitter of the PNP transistor are not absorbed by recombination in the N^- base and spill over to the P base contributing to PNP bipolar current. The MOSFET current I_{mos} is the base current of the bipolar transistor, and the collector emitter current of the IGBT duplicates the general shape of MOSFET characteristics except that it is the amplified version of I_{mos}. In the third regime, when the current exceeds a critical level, the device latches up like the ON state of a thyristor. Consequently, gate control is lost [8].

4.2.1 Reverse blocking mode

With the gate terminal shorted to the emitter terminal, a positive bias is applied to the N^+ emitter while a negative bias is applied to the P^+ collector. In this condition, with reference to Fig 4.4, junctions J_1 and J_3 are reverse biased while the junction J_2 is forward biased. The reversed biased junctions J_1 and J_3 inhibit the current flow through the device, imparting to it

the reverse blocking capability. The voltage is supported mainly across the junction J_1. A large fraction of the depletion region extends across the low doped N^- base and slightly across the P^+ collector due to its heavy doping. The reverse blocking voltage is determined by an open base transistor comprising P^+ collector, N^- base and P-base regions. This transistor may suffer breakdown by reach-through for the thin N^- base, or light doping of this region. The resistance and the thickness of the N^- base must therefore be optimized for the required breakdown voltage. A rule of thumb is to choose the N^- base thickness equal to the depletion layer width at the maximum operating voltage, plus one minority carrier diffusion length [8].

4.2.2 Forward blocking mode

The forward blocking mode is obtained when the collector has a positive potential and the emitter negative while the emitter is shorted to the gate. In this condition, with reference to Fig 4.4, the junctions J_1 and J_3 are forward biased. The blocking occurs across junction J_2 which is reversed biased. The depletion region stretches partly into the P-base, but most of it into the N^- drift region. In Fig 4.5 a) the electric field is shown for a non punch through IGBT. As it can be seen, the field does not reach all the way to the P^+ substrate, and hence the name non punch through. The forward voltage blocking capabilities can be found as the shaded red area under the electric field curve.

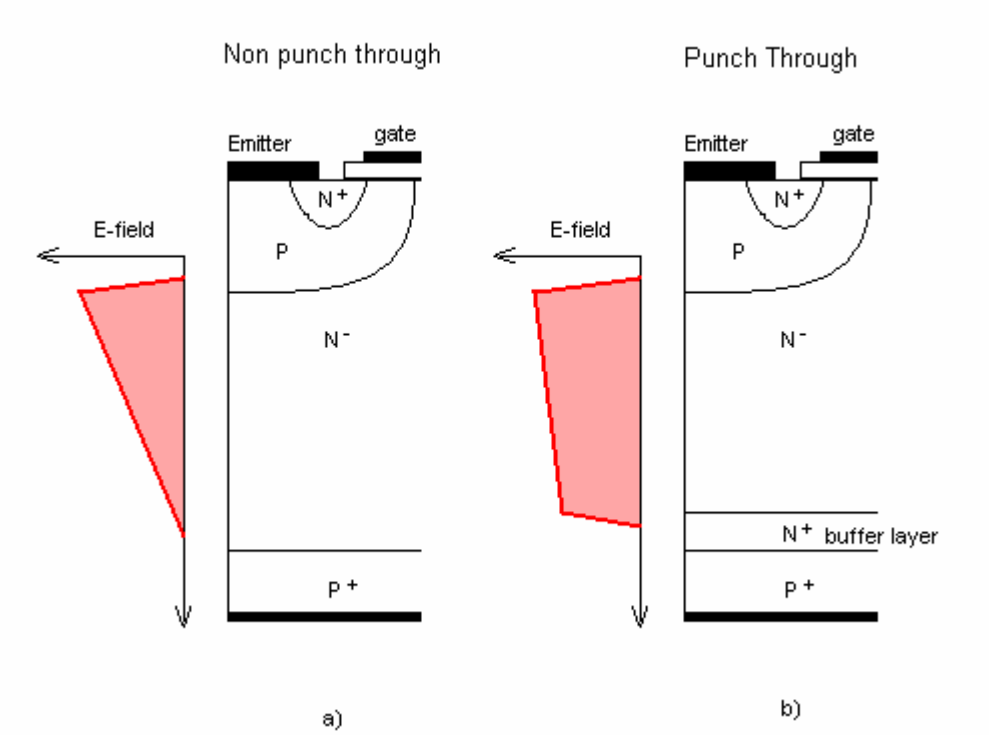

Fig 4.5 a) Forward electric field in Non Punch through IGBT b) Forward electric field in Punch through IGBT

As mentioned previously and indicated in Fig 4.1, there is sometimes added an extra layer in the IGBT structure, the N^+ buffer layer. This layer is added to improve the forward voltage blocking capabilities. As the forward voltage increases, the depletion layer will extend all the way through the N^- drift region and come in contact with the N^+ buffer layer. When this occurs, further increases in voltage will not cause the depletion region to widen any further because the large doping density in the N^+ layer effectively blocks further growth of the depletion layer. Instead the electric field profile begins to flatten out, as shown in Fig 4.5 b),

becoming less triangular and more rectangular. The area under the electric field curve is larger than for the non punch through, indicating a larger voltage blocking capability. If the forward voltage blocking capability is kept equal to the non punch through, the effect of the added N^+ buffer layer will be lower on-state resistance. This is obtained because the length of the N^- drift region can be reduced. However, the increase in forward blocking capabilities or lowering of on-state resistance does not come without a cost. As illustrated in Fig 4.6 b), the reverse voltage blocking capability is severely reduced compared to the non punch through IGBT in Fig 4.6 a). This is caused by the junction between the highly doped P^+ substrate and the highly doped N^+ buffer layer, which is unable to block any voltage of significant degree [9]. This can be seen from the small shaded area under the electric field curve. A non punch through IGBT can be fabricated with reverse blocking voltage equal to forward blocking voltage because the highly doped P^+ substrate is in contact with the lightly doped N^- drift region allowing growth of the depletion layer into it.

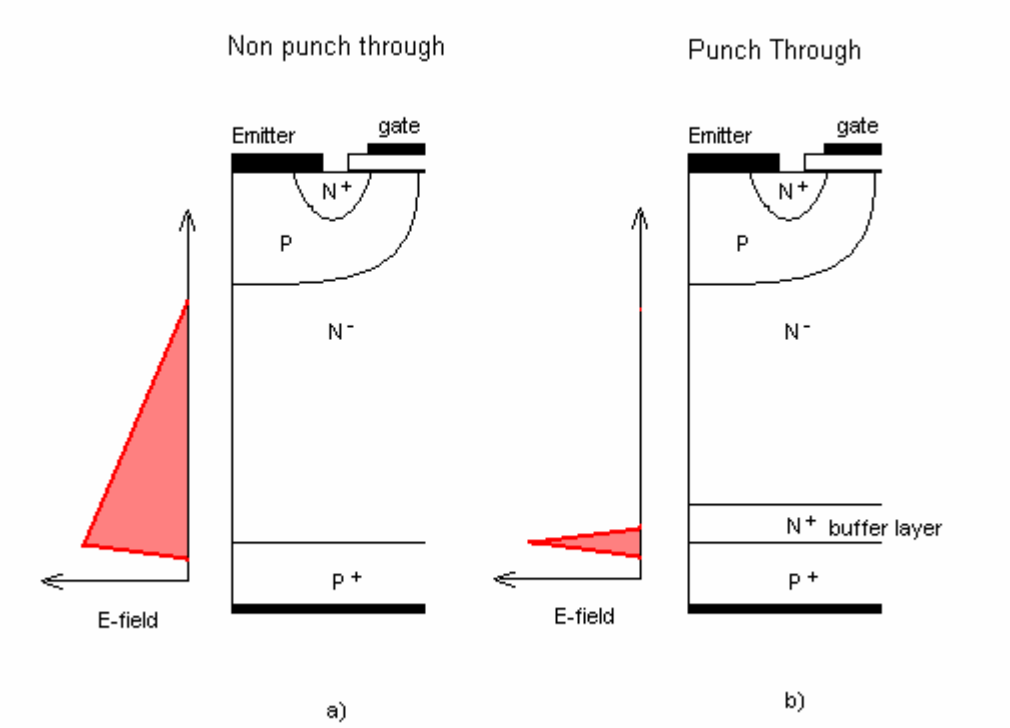

Fig 4.6 a) Reverse electric field in Non punch through IGBT b) Reverse electric field in Punch through IGBT

The disadvantage of having insignificant reverse blocking capabilities is in some applications not a problem. In inverter applications where the inverter is fed by a rectifier, the switches will never have to block any reverse voltages, so in high voltage, high power inverter applications the punch through IGBT will be very well suited.

4.2.3 Conduction modes and conductivity modulation

An IGBT in forward blocking state can be transferred to the forward conducting state by removing the gate-emitter shorting and applying a positive voltage of sufficient level to invert the Si below in the P base. Under this condition the voltages at the terminals must be positive collector, negative emitter and positive gate. With these requirements satisfied, an n-channel develops in the underlying P-base connecting the N^+ emitter to the N^- drift region. Through this channel electrons are transported from the emitter to the drift region. This flow of

electrons lowers the potential in the N^- region, and the junction between the P^+ collector substrate and the drift region becomes forward biased. Under these forward bias conditions, a high density of minority carrier holes is injected into the N^- layer. When the injected carrier concentration is much larger than the background concentration, a condition of high-level injection is said to prevail in the N^- region of the IGBT. A hole injected by the P^+ collector from a point directly below the emitter-base short traverses a rectilinear path through the N^- region/P-base and reaches the N^- base/P-base space charge region. Finally it arrives at the emitter contact after crossing the P^+ region. Another hole, which is ejected from a point directly below the gate region, travels vertically upwards and reaches under the gate. Here it is repelled by the positively charged accumulation layer below the gate and diverted toward the P-base/N^- base space charge region. Moving underneath the N^+ emitter and through the P^+ region, it is captured by the emitter contact. Thus at high collector supply voltage, a plasma of holes builds up in the N^- drift region. This plasma of holes attracts electrons from the emitter contact to maintain local charge neutrality. In this manner, approximately equal excess concentrations of holes and electrons are gathered in the N^- base. These excess electron concentrations drastically enhance the conductivity of N^- base. The mechanism of rise in conductivity is referred to as conductivity modulation of the N^- drift region. The ON state resistance and thereby the forward voltage drop is then significantly reduced [8].

4.2.4 i-v characteristics

The i-v characteristics of IGBTs are shown in Fig 4.7, and consist of two operating regions, reverse and forward. The steady state forward characteristic show several lines plotted, each of which corresponds to a different gate-emitter voltage. Keeping the gate-emitter voltage fixed, the collector-emitter current is measured as a function of collector-emitter voltage.

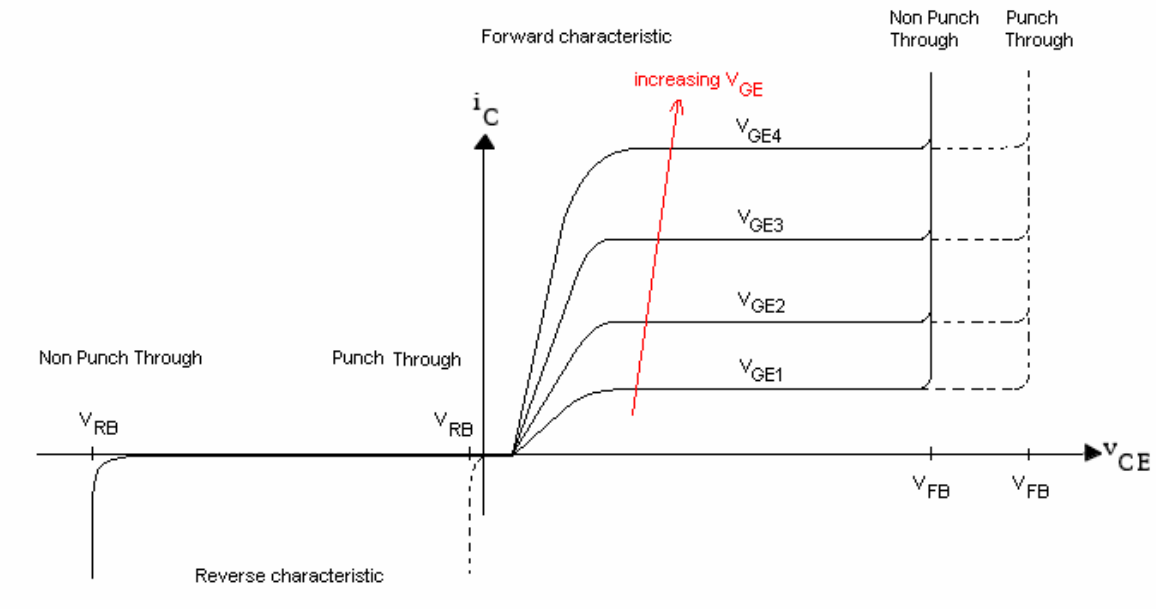

Fig 4.7 i-v characteristics of IGBT

The reverse blocking capability for both punch through and non punch through IGBTs are indicated with V_{RB}. As it can be seen, the reverse blocking voltage of a non punch through IGBT can be as large as the forward voltage, V_{FB}, while the reverse blocking voltage of a punch through will be close to zero. If the N^- drift region is kept equal in length in the punch

through and non punch through IGBTs, the forward blocking voltage will be larger for the punch through, as indicated in the figure.

The transfer characteristics of an IGBT will be equal to that of a MOSFET. The transfer characteristic is shown in Fig 4.8. The IGBT will start conducting as soon as the gate-emitter voltage exceeds the threshold voltage $V_{GE(th)}$, and the N-channel is formed in the P-base.

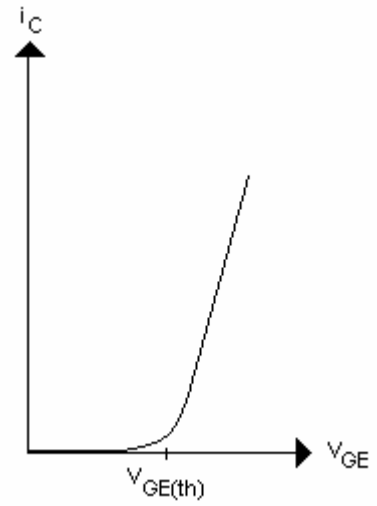

Fig 4.8 Transfer characeteristic of IGBT

4.3 Switching behavior of IGBT

The IGBT is switched by applying gate pulses. When a pulse is applied, the IGBT turns on, while it turns off when the pulse ceases. The switching behaviour can be thoroughly described by looking at an IGBT in a power circuit.

4.3.1 Turn-on transient

The switching waveforms of an IGBT in a clamped inductive circuit are shown in Fig 4.9. The time constant (L/R) of the load is assumed to be large compared to the switching frequency so the load current can be considered to be constant. The IGBT turn-on switching performance is dominated by its MOS structure. During $t_{d(on)}$ the gate current charges the constant input capacitance with a constant slope until the gate-emitter voltage reaches the threshold voltage $V_{GE(th)}$ of the device. During t_{ri}, load current is transferred from the diode into the device and increases to its steady state value. The gate voltage rise time and IGBT transconductance determine the current slope and as a result the length of the interval t_{ri}. When the gate-emitter voltage reaches $V_{GE(on)}$ that will support the steady state collector current, collector-emitter voltages starts to decrease. After this there are two distinct intervals during IGBT turn on. In the first interval the collector-emitter voltage drops rapidly as the gate-drain capacitance of the MOSFET portion of IGBT discharges. At low collector-emitter voltage the capacitance increases. A finite time is required for high level injection conditions to set in the drift region. The pnp transistor portion of the IGBT has a slower transition to its on state than the MOSFET. The gate voltage starts rising again only after the transistor comes out of its saturation region into the linear region, when complete conductivity modulation occurs and the collector-emitter voltage reaches its final on-state value [10].

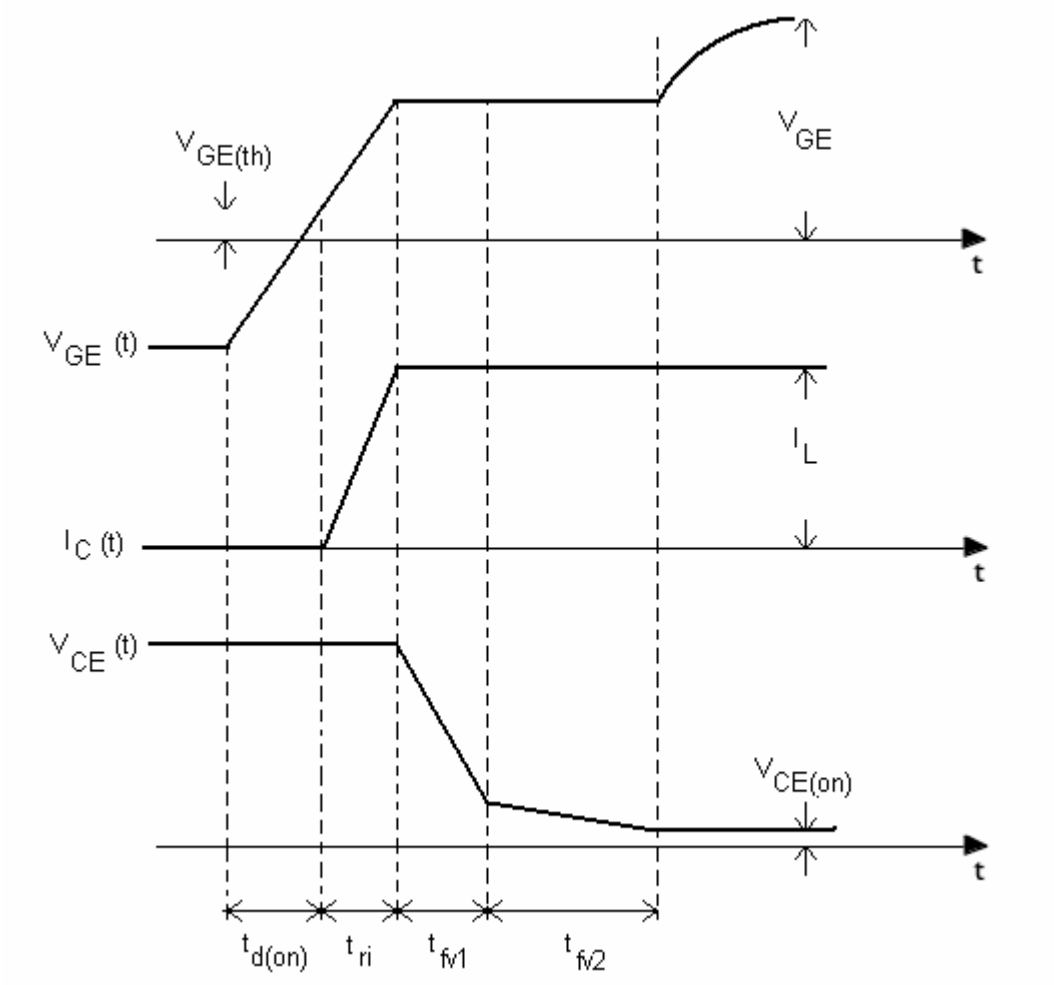

Fig 4.9 IGBT turn on waveforms in a clamped inductive load circuit

4.3.2 Turn-off transient

Turn off begins by removing the gate-emitter voltage. Voltage and current remain constant until the gate voltage reaches $V_{GE(on)}$ required to maintain the collector steady state current as shown in Fig 4.10. After this delay time, the collector voltage rises, while the current is held constant. The gate resistance determines the rate of collector voltage rise. As the MOS channel turns off, collector current decreases sharply during t_{fi1}. The MOSFET portion of the IGBT determines the turn off delay time and the voltage rise time. When the collector voltage reaches the bus voltage, the freewheeling diode starts to conduct. However, the excess stored charge in the N^- drift region during on state conduction must be removed for the device to turn off. Recombination of the minority carriers in the base region gradually decreases the collector current and results in a current tail. Because there is no access to the base of the PNP-transistor, the excess minority carriers can not be removed by reverse biasing the gate. The t_{fi2} interval is long because the excess carrier lifetime in this region is kept high to reduce on-state voltage drop. Because the collector-emitter voltage has reached the bus voltage in this interval a significant power loss occur that increases with frequency. Therefore the current tail limits the IGBT operating frequency and there is a trade off between the on-state losses and faster switching times. For an on-state current of I_{on}, the magnitude of current tail, and time required for the collector current to decrease to 10% of its on-state value, turn-off (t_{off}) time, are approximated as,

$$I_C(t) = \alpha_{pnp} I_{on} e^{-(t/\tau_{HL})} \tag{1}$$

$$t_{off} = \tau_{HL} \ln(10\alpha_{pnp}) \tag{2}$$

$$\alpha_{pnp} = \frac{1}{\cosh\left(\frac{l}{L_a}\right)} = \operatorname{sech}\left(\frac{l}{L_a}\right) \tag{3}$$

I_c = magnitude of collector current
t_{off} = turn-off time
α_{pnp} = gain of PNP-transistor
τ_{HL} = high level lifetime
l = undepleted basewidth
L_a = ambipolar diffusion length

By reducing the life time and the gain of the PNP-transistor, τ_{HL} and α_{pnp} respectively, the magnitude of the current tail can be reduced. However, the conductivity modulation decreases, which increase the on-state voltage drop in the drift region. Therefore, higher speed IGBTs have lower current rating.

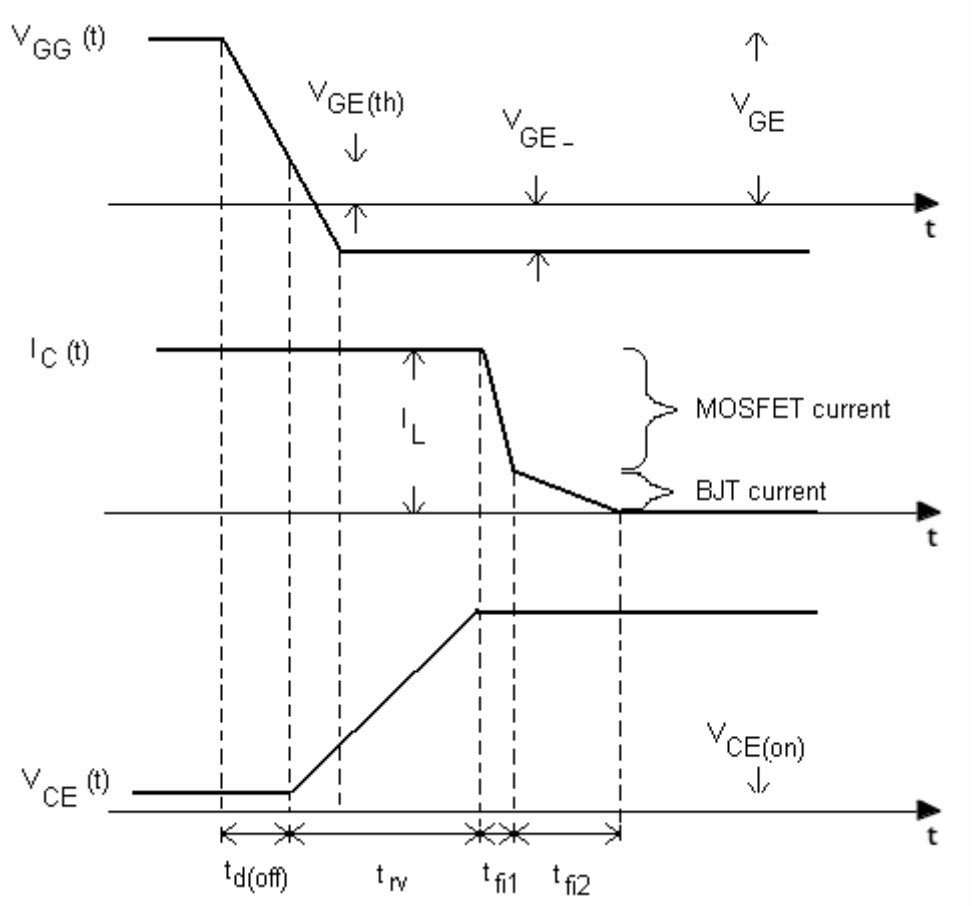

Fig 4.10 IGBT turn off waveforms in a clamped inductive load circuit

5 IGBT power modules

The compression application will have to use power modules with high ratings to ensure safe and reliable operating of the system.

The most suitable power semiconductor package for a high power sub sea compression application will probably be an IGBT power module with several paralleled chips or an IGBT press pack module. IGBT modules with paralleled chips have high current carrying capabilities and are well known and documented by numerous manufactures. The press pack is designed to have a very robust structure and can also handle large currents and voltages. Other types are also available and include the so called hockey puck package and discrete packages. The discrete package contains only one die and is constructed for medium voltage applications. The hockey puck package contains one large die and is used for very high power applications.

IGBT power modules with paralleled dice have current carrying capabilities depending on the size and the number of dice along with the current carrying capabilities of the wires paralleling the dice. The dice are mounted on a substrate or a lead frame which in turn is mounted on a copper baseplate or a thick film baseplate, forming a stacked formation. Stacking techniques such as direct bond copper (DBC), insulated metal substrate (IMS) and thick film stacking are common. Connection to gate, emitter and collector are provided and the paralleling of chips is carried out using aluminium bond wires. For protection from partial discharge and impurities, silicon gel is provided to cover all components and on top of that, hard plastic encapsulation with connection to external terminals.

One power module can consist of an inverter leg or a full inverter module with all the phase legs in one package. The heat sink will then be common for all legs. Electrical isolation of the baseplate from the semiconductor is necessary in order to contain multiple phases on the same heat sink. Another important reason for electrical isolation of the baseplate is safety where the heat sink can be held at ground potential [11].

Flat- or press-pack encapsulation offers several advantages over the traditional module package. In a press-pack IGBT, electrical contact is established by pressing the IGBT chips between two high-planarity disks. An adequate stress relief layer is included to forebear the compression. The outermost poles are the emitter and collector pads, both made of nickel plated copper. On the emitter side, a molybdenum washer and a nickel-plated copper foil are inserted between the emitter pole and the IGBT chip. Because the copper is a soft material, it ensures proper electrical contact and also enhances uniformity of pressure distribution.

5.1 DBC solutions

In Fig 5.1 a cross section of a DBC solution is illustrated where the copper baseplate, solder layers, ceramic layers, dice, silicon gel, bond wires and housing can be seen. In DBC solutions it is the ceramic layer that isolates the semiconductors from the baseplate.

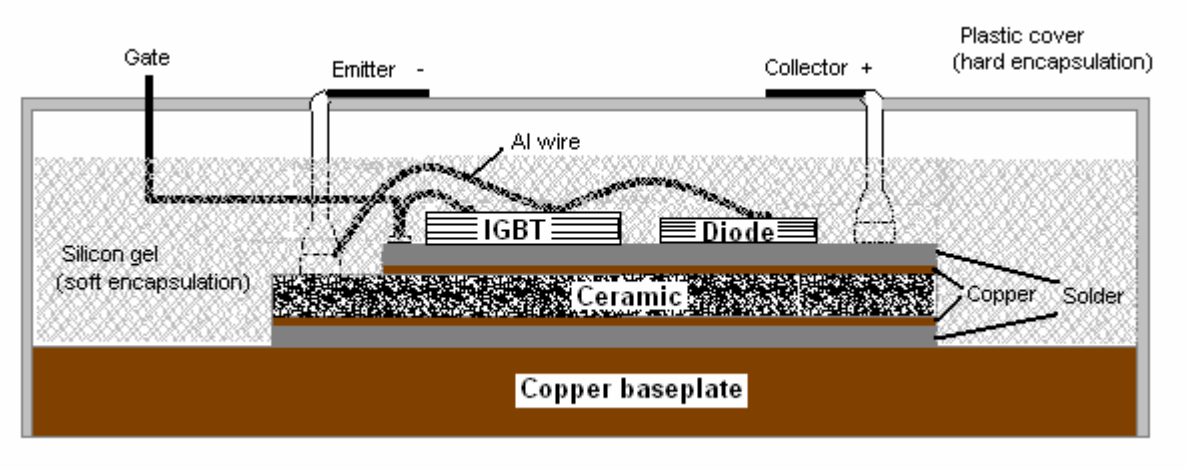

Fig 5.1 Direct bonded copper packaging of IGBT power module

DBC substrates are composed of a ceramic insulator, typically aluminium oxide, Al_2O_3, or aluminium nitride, AlN, onto which pure copper metal is attached by a high temperature eutectic melting process and thus tightly and firmly joined to the ceramic. The process is carried out by forming a thin film of oxide on the copper and then bringing the copper into intimate contact with the ceramic at an elevated temperature. The thin oxide layer on the copper then chemically bonds to the substrate. The assembly is cooled back to room temperature which imparts additional strength to the stacked structure because the ceramic is under compression due to the higher thermal expansion coefficient (CTE) of the copper. The total thermal expansion coefficient of the stack is much closer to that of the silicon in the dice than pure copper if the thickness of the ceramic and copper are in proper proportion [11]. This can be seen from Table 5.1 [12], where some material properties are listed.

Table 5.1 Material properties

Material	Thermal conductivity [W/mK]	CTE [µm/K]
Al_2O_3	30	7.4
AlN	170	4.2
Cu	385	18.5
Si	124	3.6

The unique usefulness of DBC substrates in power electronics include properties such as [13]:

- High thermal conductivity
- High insulating voltage (in the area of approximately 5-10 kV/mm)
- High heat dissipation
- Similarity of thermal expansion coefficient enables chip-on-board applications

5.2 Press pack modules

Press-pack IGBT has been developed in recent years as a superior high power IGBT device to conventional IGBT module in reliability and performance. This type of IGBT is replacing GTOs or thyristors in such applications as traction, power transmission and industrial motor drive because of its excellent advantages such as high performance, high reliability, compactness due to the both-sided cooling and rupture free feature [14]. The press packs comes in round or square packages. The square package has a beneficial geometry due to the geometry of the chips inside which also has a square form. The module is hermetically sealed

and compressed to ensure electrical contact which principle is illustrated in Fig 5.2. Because the module is subjected to great forces, the mechanical ruggedness is design to be superior to the traditional modules [15].

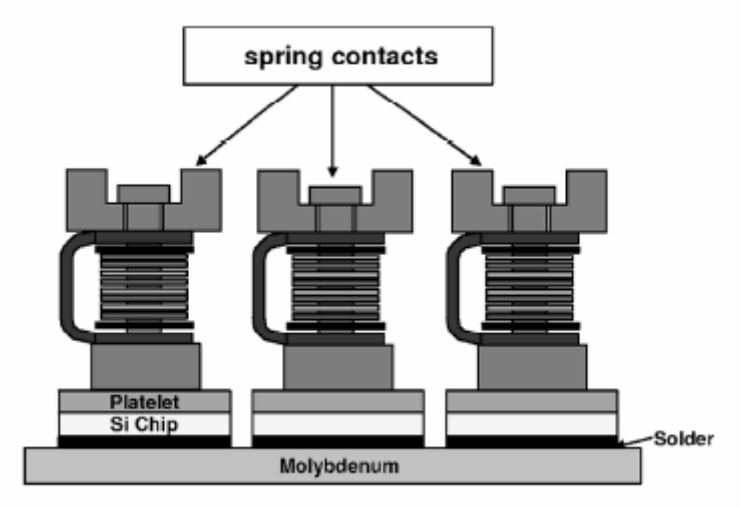

Fig 5.2 Press pack principle

6 Suitable semiconductor modules for the final solution

A lot of high power semiconductor modules are developed by various manufacturers. A few selected is presented in this chapter that may be applicable in a high power application under high hydrostatic pressure.

Manufacturers continuously improve the characteristics of the IGBTs as the demand for higher power and reliability grows. Some state of the art IGBT modules include a new soft punch through device, ABB's HiPak Module with the next generation soft punch through IGBTs, and a new press pack IGBT module manufactured by Toshiba. Since a suggested solution is to have the modules at high hydrostatic pressure on the sea bed, the housing of the modules must either be strong enough to withstand the pressure, or be penetrated so that the insulating oil can completely fill it without any air pockets.

6.1 ABB's HiPak modules with next generation SPT$^+$ IGBTs

ABB Switzerland Ltd, semiconductor manufacturer has developed a high voltage soft punch through IGBT. The SPT concept is based on using a low doped N-buffer profile at the anode side of the IGBT. At a normal DC-link operating voltage, the space charge region does not reach the boundary of this buffer region with the high resistance N-base layer. Therefore, despite the much thinner base region, the dynamical electrical properties of the SPT-IGBT are almost comparable with those of a thicker non punch through IGBT. The soft punch through feature is especially applied with respect to the softness of the current and voltage curves during switching transients. Hence, the term "Soft" in SPT originates from this fact. In addition, the buffer acts as a field stopper for voltages higher than the DC-link voltage up to the nominal blocking voltage as shown in Fig 6.1 [16]. As mentioned above, the major benefits of the SPT-IGBT are resulting from a substantially (30%) thinner wafer thickness compared to a NPT-IGBT of the same nominal blocking voltage. As a consequence, both on-state voltage and turn-off losses are reduced simultaneously. However, the main advantages of the NPT structure are also maintained with regard to extreme ruggedness, low temperature dependence during IGBT turnoff transient and finally, a positive temperature coefficient for $V_{ce(sat)}$ during on-state [16].

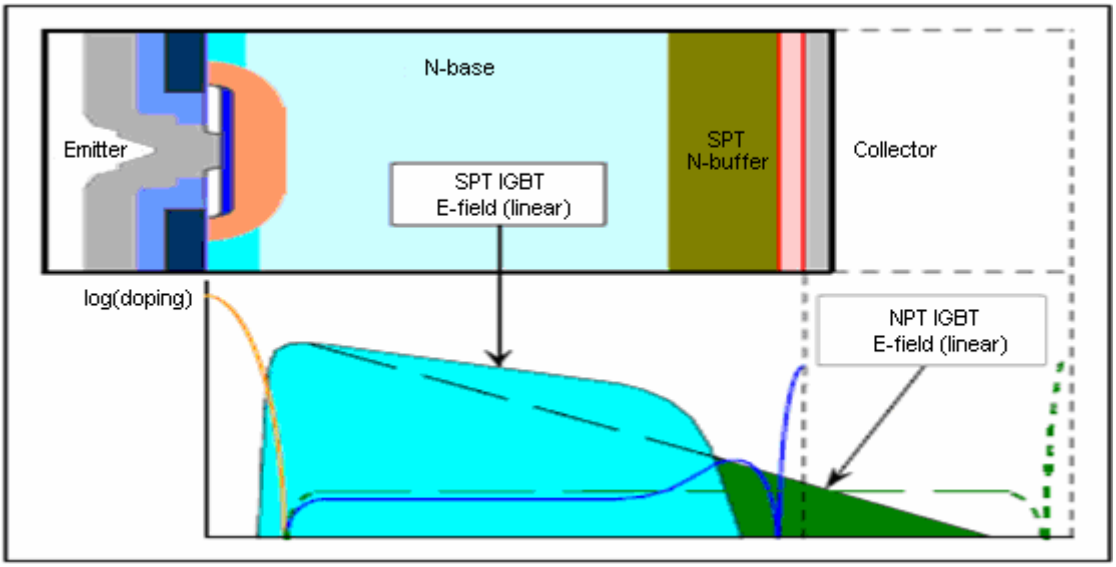

Fig 6.1 SPT IGB doping profile and electric field distribution with respect to an NPT IGBT structure

The new HiPak modules with the next generation SPT$^+$ take advantage of the existing SPT technology, shown in Fig 6.1, with modifications to improve the performance and voltage levels. One of the new achievements is the planar technology which exploits an enhanced carrier profile through planar cell optimisation. This leads to a significant increase in plasma concentration at the emitter and thus a lower on state voltage is obtained for the same turn-off loss. In addition an optimised base region combined with soft punch through buffer allows the collector current to smoothly decrease during the turn off transient thanks to the progressive and controlled manner in which the depletion layer is established. To illustrate the improvement in performance, a comparison of the SPT$^+$ with the SPT is made in Fig 6.2 [17] for the voltage range 1200V to 4500V. The values for $V_{ce(sat)}$ are obtained at the same current densities and for similar turn-off losses, for each voltage class [17].

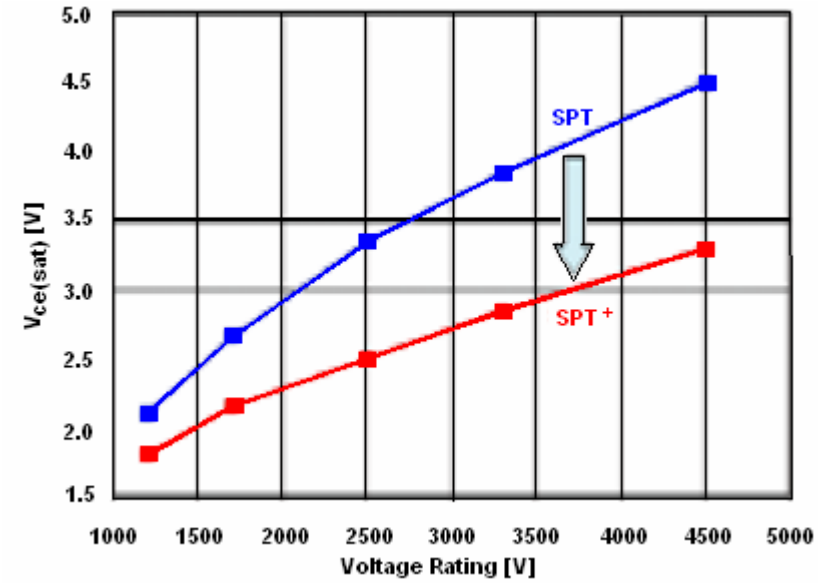

Fig 6.2 SPT and SPT$^+$ IGBT on-state voltage vs. rated blocking voltage at 125°C

On-state losses in the SPT$^+$ are significantly reduced as can be seen from the above figure. The reduction in $V_{ce(sat)}$ due to SPT$^+$ cell enhancement ranges from 15% for a 1200V IGBT up to 30% for a 4500V device, allowing corresponding increases in current ratings. ABB has also

reported testing of IGBTs with voltage ratings up to 6.5kV with approximately 30% in $V_{ce(sat)}$ reduction. Switching waveforms and other electrical characteristics for the HiPak modules from ABB can be found in [17] where the module with the new SPT$^+$ technology is presented as a device which will give system designers greater freedom in achieving higher power and better efficiency for their applications.

6.1.1 Enhanced Planar IGBT

As mention briefly in the previous chapter, one of the new achievements is the planar technology with planar cell enhancement. The Enhanced-Planar technology is integrated with the soft punch through buffer concept for ensuring controllable and soft switching behaviour. The improvements in the on state losses shown in Fig 6.2 were achieved through enhancement of the carrier profile near the emitter while maintaining the same drift region thickness as for the standard SPT design.

In order to design the enhancement N-layer for an optimum trade-off between low losses, high safe operating area and maximum blocking capability, the positioning and doping profile of the N-layer was investigated experimentally by ABB Switzerland Ltd, Semiconductors. Results were also confirmed through simulations carried out on the different structures. In addition to an n-layer fully surrounding the cell's P-well, prototype samples were fabricated where an N-layer was only placed laterally near the edge of the P-well, and in a third version it was centralised underneath the P-well as shown in Fig 6.3 [18]. The peak concentration for the N -layer was the same for all three versions. Major improvements in on-state losses were observed for the lateral version, similar to those achieved for the fully encompassed P-well structure. This was attributed to three main interacting effects;

1. Improved spreading of electrons from the MOS channel
2. Shorter channel length
3. Improved PiN effect between the cells due to the enhanced hole accumulation at the periphery of the cell

Due to the fact that the lateral n-layer does not extend beyond the maximum P-well depth, a favourable trade-off with blocking capability was achieved, thus allowing a higher doping for the enhancement N-layer to obtain even lower losses. These effects were all absent in the second centralised version, which only provided a hole barrier under the cell with a negligible contribution to plasma enhancement. However, the centralised N -layer design demonstrated a higher RBSOA capability compared to the other structures due to the positioning of the peak field directly below the contact. This was achieved at the expense of reduced blocking voltage capability. The final EP-IGBT design utilised an optimum doping profile for both the lateral and centralized regions for achieving the lowest on-state losses, maximum blocking capability and highest SOA limits. Cosmic ray measurements also showed that the EP-IGBT dose not result in a higher failure rate at the required DC voltage-levels when compared to the equivalent standard IGBT [18].

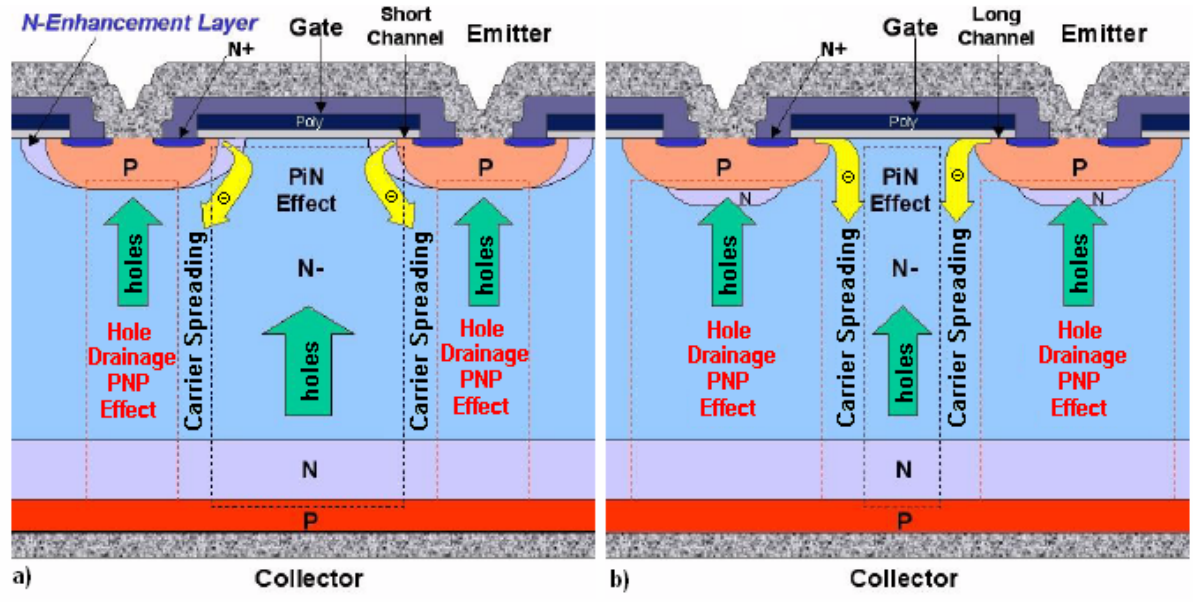

Fig 6.3 a) Conduction with lateral n-layer and b) centralised n-layer

6.1.2 Packaging

Five different HiPak modules are shown in Fig 6.4, and as it can be seen, the packaging follows conventional standards. From various datasheets for different HiPak modules it can not be determined if the housing is hermetically sealed or not. However, assuming that it is sealed, the housing will probably not withstand any significant hydrostatic pressure in a sub sea application where the module is submerged in oil. A way to solve this problem is to penetrate the housing so that the insulating oil can completely fill it. Any soft encapsulation of the chips then has to be removed, because it may dissolve when in contact with the oil. This is easy to test in the lab, but any new module has to undergo several tests and verifications before hitting the marked, and if modified the warranties will no longer apply.

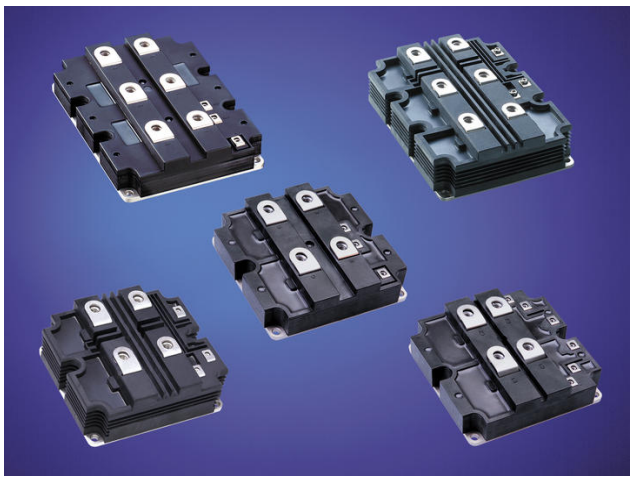

Fig 6.4 HiPak module packaging

The HiPak module can be suitable for high pressure applications if it can be delivered with minor modifications, or guarantees that it is hermetically sealed and will withstand high hydrostatic pressure.

6.1.3 ABB's Press packs

Another way of making the module pressure resistant is to integrate known packaging technology with the new SPT$^+$ technology. Press pack modules are developed which shows excellent mechanical strength. ABB developed new pressure-contact technology which decouples the external clamping force from the direct pressure on the chip. This was achieved by the use of a flexible emitter contact (individual press-pin) in combination with a stiff housing as shown schematically in Fig 6.5 [19].

To further reduce the stress coming from mechanical unevenness, each chip is contacted by an individual flexible pin. During mounting, a certain amount of the applied pressure is transferred onto the chip by compression of the individual press-pin contacts whereas the excess pressure is taken over by the robust housing. At the same time, the robust housing limits the compression of the flexible contacts. With this design, the pressure on the chip can be adjusted by the stress-strain characteristic of the individual pressure contact. The significant advantage of this concept is that it is much less sensitive to pressure inhomogeneities compared to traditional hockey-puck designs with stiff copper pole-pieces and that it allows very high mounting force as well as much wider mechanical tolerances. The result is a gain in mechanical reliability at reduced costs [19].

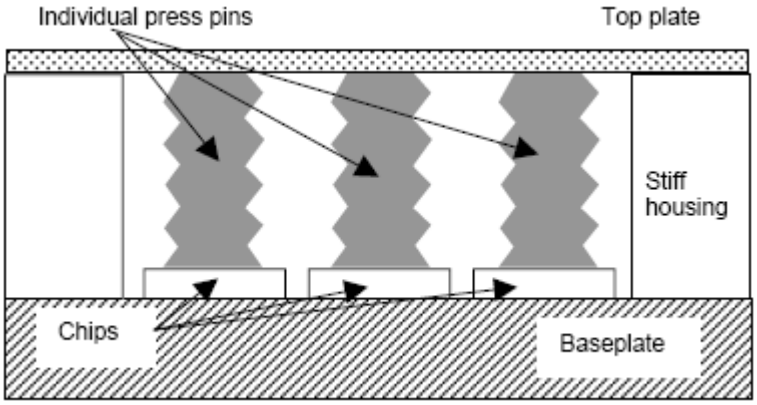

Fig 6.5 Schematic view of the pressure scheme

An interesting test of the press pack is reported in [19]. The test is a so called explosion test, where the module is subjected to several hundred kA for several hundred microseconds. The test determines if the housing explodes when high vapour pressure builds up inside. Peak power of the test was 110MW and the housing was still intact after the test with no ejected parts. This implies that the housing is extremely robust, and that it very well may be suited for high hydrostatic pressure applications like a sub sea compressor unit with no pressure chamber holding 1 atmosphere.

Existing press pack units can also be used without the SPT$^+$ technology. Data from the module used in the explosion test can be found in Table 6.1 and it shows high power capability. It should also be noted that the press pack has a square form and not a round hockey puck shape.

Table 6.1 Press pack module data

Mechanical properties	
Dimensions of press pack	260x220x26 mm^3
Mounting force	75±10 kN
Surface creepage distance	52 mm
Weight	3.5 kg
Electrical properties	
Max collector-emitter voltage	5200 V
Nominal collector current	2000 V
Switching safe operating SOA	3000 V, 4000 A

6.2 Planar gate press pack Injection Enhanced Gate Transistor

Toshiba developed a planar press pack injection enhanced gate transistor for high power applications. The vertical cross section of an IEGT cell is presented in Fig 6.6 [20]. It is similar to the standard IGBT cell but it has wider cell width, indicated with L_g, in the figure. In the presented cell, there has been added a highly doped N^+ buffer layer to form a punch through structure.

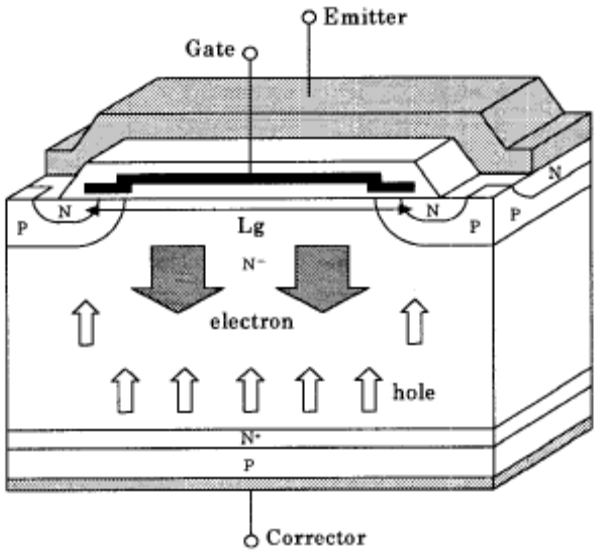

Fig 6.6 Cross section of planar IEGT

The wide L_g structure induces the injection enhancement effect of electrons on the emitter side of the N^- high resistance layer. The high density of carrier is accumulated in the N^- high resistance layer during on-state. By this effect, it makes possible that the IEGT achieves low on-state voltage drop close GTO thyristors with easy gate drivability and wide SOA of MOS transistors. Fig 6.7 shows the on-state voltage as function of L_g. In Fig 6.7, L_g = 88um is the gate-width design of P-IEGT and L_g = 68.48um is design of conventional IGBT. The figure shows that the gate width increases and the on-stage voltage decreases. This means that the conductance of the electron accumulation layer under the gate oxide is one of the major factors for a high voltage planar device design [20].

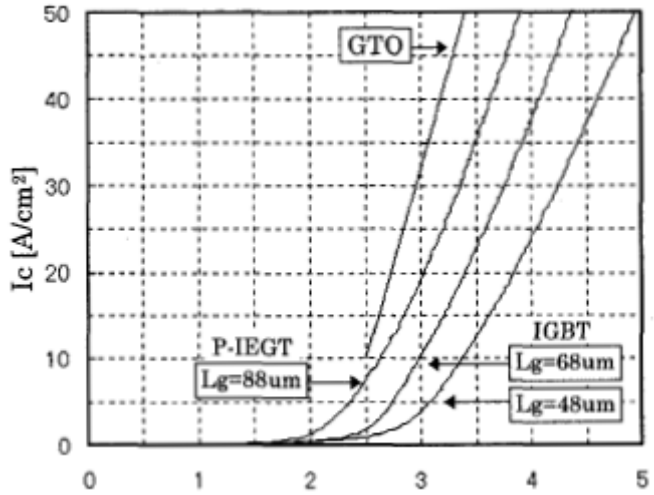

Fig 6.7 On state voltage with various cell widths

6.2.1 Packaging

The Toshiba module is press packed with a hockey puck shape. A picture of one module is shown in Fig 6.8.

Fig 6.8 Toshiba IEGT press pack module

The module seems compact and solid by visual inspection and it would be assumed that the explosion test previously described also has been done on this module. The packaging class SF6 indicates that the module is evacuated and then filled with a gas with slightly overpressure. A small sealed penetration pin on the side, not shown in the picture, has been used for evacuation and filling purposes. Perpendicular pressure on the planar surfaces would not be a problem since it is how the module is design to be installed, but hydrostatic pressure may compress the sides and either part the metal surfaces from the plastic sides or destroy the chip alignment on the inside causing destruction of device.

For hydrostatic pressure applications, the housing could be delivered filled with a fluid. This will probably be the best solutions causing the least modifications on the device.

6.3 Semikron's SEMIX IGBT module

The module from Semikron, SEMIX 202GB128D, will not be suitable for the sub sea compression application. However, to test IGBT switching operation when the chips are submerged in oil, this unit was available with the necessary modifications to execute the experiment that follows.

The SEMIX module is a DBC solution previously described with paralleled chips connected with bond wires inside the housing to improve current carrying capabilities. The casing is modified to allow fluid to fill the housing. The module was delivered without the silicon gel normally covering the chips. This was custom ordered for the testing purpose of this experiment. From the data sheet in appendix A, the equivalent circuit in Fig 6.9 shows that the module is one converter bridge leg.

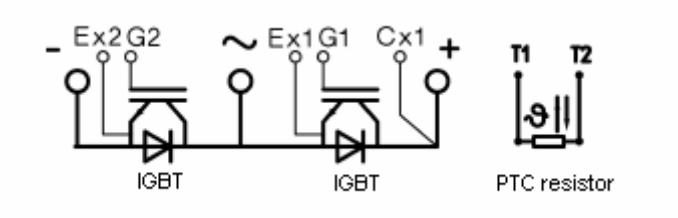

Fig 6.9 Equivalent circuit of SEMIX module

The ohmic value of the PTC resistor indicated in Fig 6.9 will change as the temperature changes according to the formula,

$$R_2 = R_1 e^{\left[B\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right]} \tag{4}$$

R_1	= Initial resistor value	[Ohm]
R_2	= Current resistor value	[Ohm]
B	= Constant	[-]
T_1	= Initial temperature	[K]
T_2	= Current temperature	[K]

From the data sheet in appendix A, the constant, B, is given to be 3420. However, after temperature tests in the laboratory, a new value was calculated to be a little bit lower, but it was close enough to conclude that the tests done by the manufacturer probably is correct.

7 Experimental setup, components

The experiment is set up to test operating capabilities of an IGBT module under high hydrostatic pressure, and consists of an electrical system and a pressurising system. As previously mentioned and explained no pressure was applied. However, the system will still be described as if pressure was applied as basis for further work.

In Fig 7.1, a sketch of the test object is shown. It consists of an IGBT module mounted on a heat spreader and three capacitors forming a part of the total capacitor bank. The remaining part of the capacitor bank is located on the outside of the tank. Capacitors used in this experiment are manufactured by Evox Rifa with standard metallised film technology. Metallised film technology is further described in [1], and more information about the IGBT module can be found in the data sheet in appendix A.

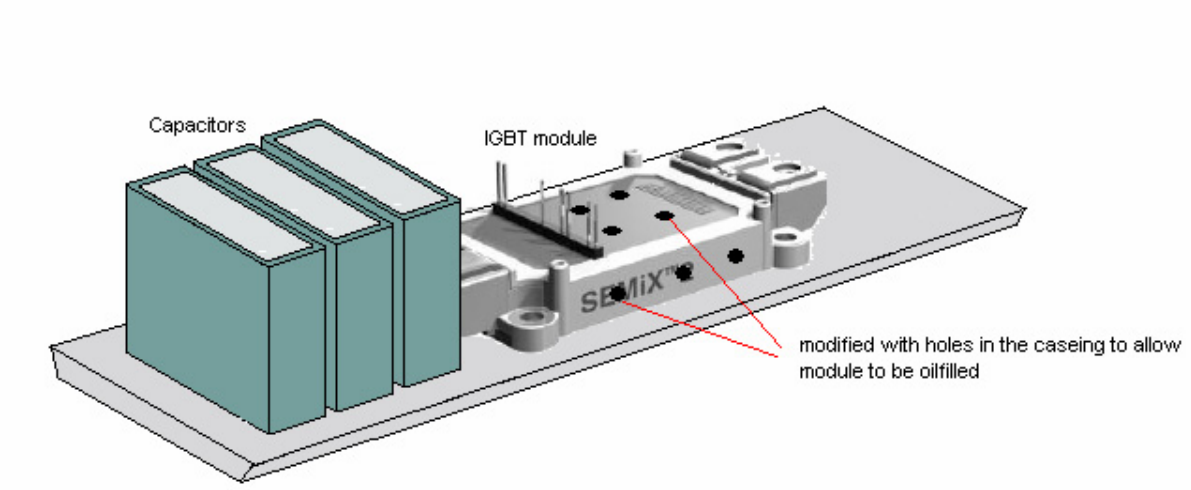

Fig 7.1 Test object

The heat spreader with the IGBT and capacitors is placed inside a pressure tank which is illustrated in Fig 7.2. The tank is then filled with silicon oil and the IGBT is operated with continuous switching. Thermal management is obtained by convective cooling caused by circulation of the oil inside the tank.

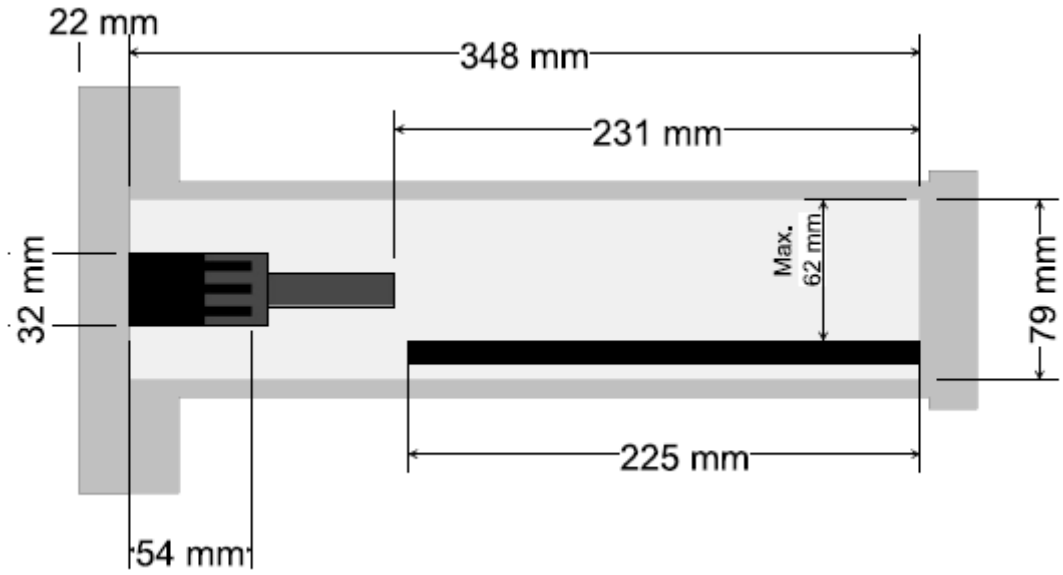

Fig 7.2 Pressure tank

Physical measurements of the heat spreader can be found appendix H.

7.1 Electrical system

The electrical system is shown in Fig 7.3, where the encapsulated bridge leg can be seen inside the tank. The IGBT module is mounted on a heat spreader for thermal management reasons. Also on the heat spreader, three capacitors are mounted as a part of the capacitor bank. The current is circulated through an inductor to another bridge leg on the outside of the tank, forming an H-bridge connection. The power circuit is fed through a 300V DC-current supply, but the performance of the system is restricted by the current carrying capabilities of the wires in the bushing. Their current carrying capability is approximately 15 A. The bridge leg on the outside of the tank is controlled with a current controller, while the pressurised is controlled by setting a voltage reference.

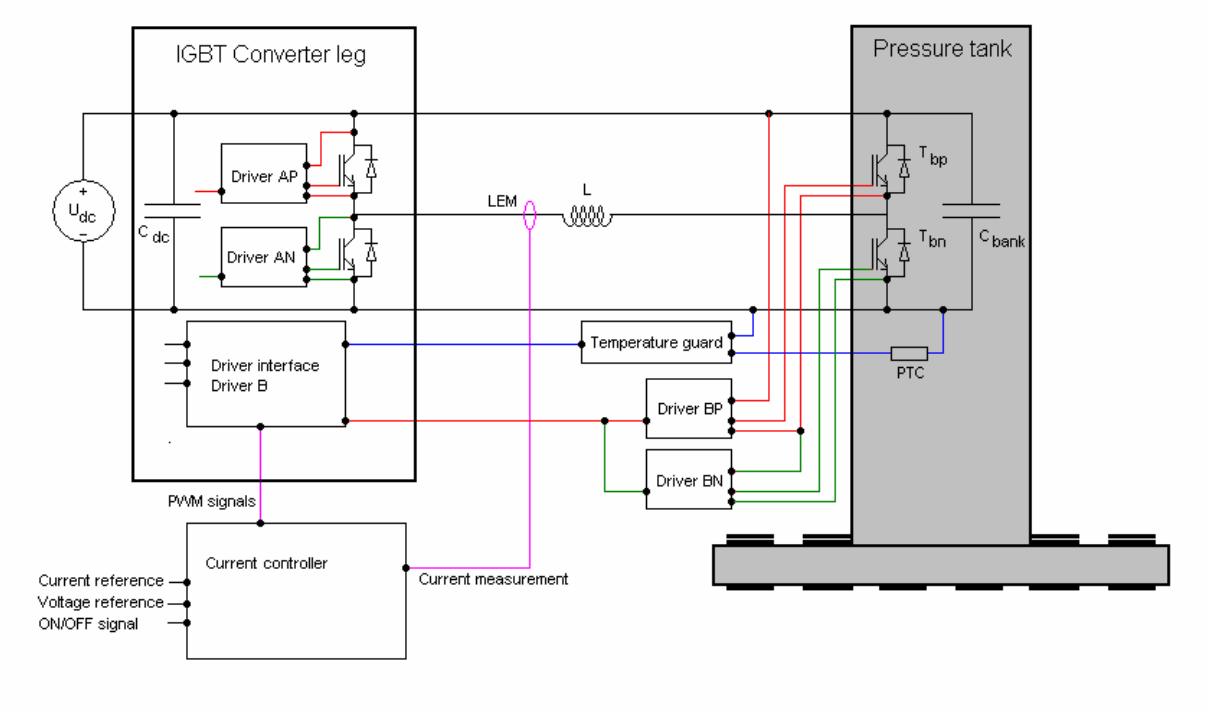

Fig 7.3 Electrical system

Some measuring equipment is set up to constantly monitor the condition of the experiment. If the drivers fail, or the temperature gets too high, the switching will stop. Switching will also stop if the pressure inside the tank gets too high. This is illustrated in Fig 7.4.

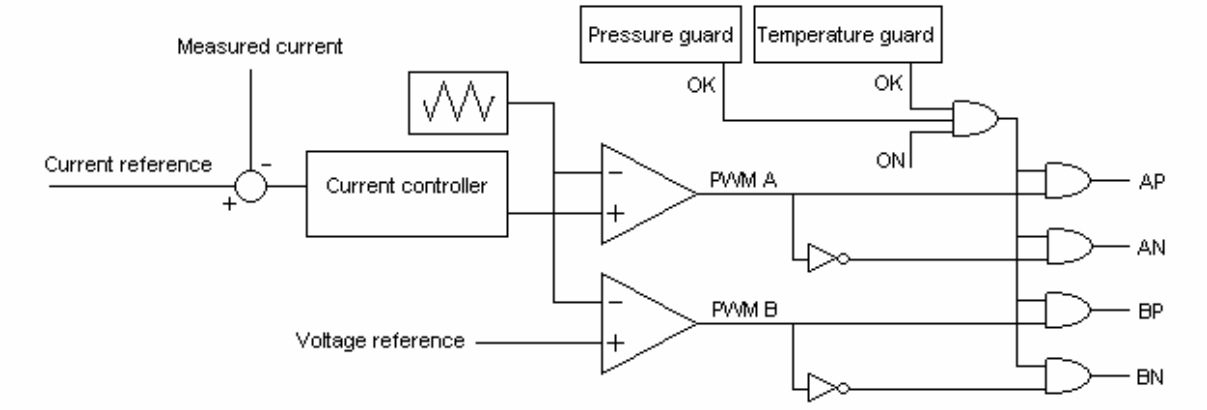

Fig 7.4 Control system

All parts of the electrical system were available and nothing had to be made from scratch or redesigned. Small modifications were made on some of the devices which will be described later.

In the next subchapters a brief description of the most important components follows.

7.1.1 IGBT converter leg

The converter leg on the outside of the tank was available from previous experiments, and is one leg of an IGBT converter designed for DC/DC and AC/DC conversion. It can also be used for motor control. The converter consists of IGBT transistors, capacitor bank, brake chopper with control circuitry, heat spreader and fan, drivers with short circuit protection and power supply and over voltage protection. The circuit diagram is shown in Fig 7.5 [21].

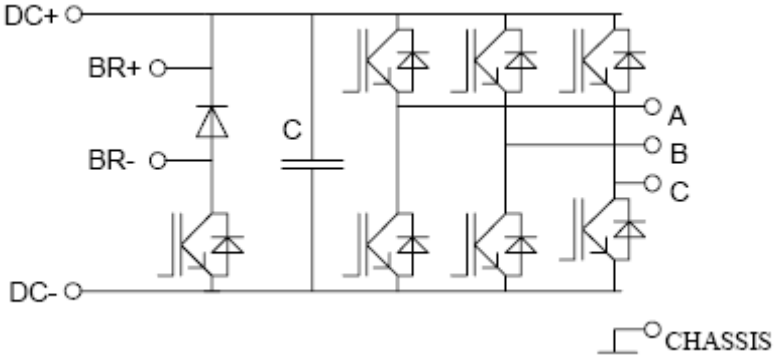

Fig 7.5 20 kW IGBT converter

Other technical data are listed in Table 7.1 [21]. The full converter is not used in this experiment. As mentioned previously, only one leg will be active together with another leg located inside the pressure tank. Control of the active leg is maintained by a current control card.

Table 7.1 Technical data 20 kW IGBT converter

V_{DC}	0-640 V
C_{bank}	3300 uF
Short circuit protection	Shut down at 400-600A
Switching frequency	0-25 kHz
Modulation	0-100%
I_{max} steady state	45A at 300V DC, 20 kHz switching 70A at 300V DC, 10 kHz switching 95A at 300V DC, 5 kHz switching 110A at 300V DC, 2 kHz switching 25A at 500V DC, 20 kHz switching 50A at 500V DC, 10 kHz switching 80A at 500V DC, 5 kHz switching 105A at 500V DC, 2 kHz switching
Thermal management	Air cooled heat spreader with fan. Fan starts at 50 degrees celcius.
Heat spreader	Fischer LA V 10-300
Heat capacity	560 W
IGBT transistors	Semikron SKM400GB123D. 2x400A 1200V bridge leg modules

7.1.2 Brake chopper control board

This board contains control electronics for an IGBT-based brake resistor chopper. It operates as an autonomous unit, monitoring the DC link voltage. When the voltage ruses above a threshold level, the brake chopper power transistor is switched on. The transistor is switched off when the voltage sinks below the threshold level again. Some amount of hysteresis limits the switching frequency of the brake chopper.

If the voltage rises even further, above a second level, this is detected and signalled as an overvoltage condition, prompting an external control unit to take action. The overvoltage trip setpoint is fixed, and is determined by the main voltage divider and a 5V reference voltage. The default overvoltage trip setpoint is 640V. This setpoint can be altered by changing values of the resistors in the divider chain and it can range from 0-100% of the default value by using a potmeter.

The power transistor is protected against short circuit conditions by a circuit monitoring the collector-emitter voltage drop. A complete circuit diagram of the brake chopper control board can be found in appendix B.

7.1.3 Current control card

A simplified Diagram for the current control card is presented in Fig 7.6. The card is designed for current control with three controllers and three pulse width modulators and can be set up as either a P- or a PI-controller. The card monitors its voltage supply and if failure occurs the OK-signal to the drivers is blocked. The control parameters can be altered by switching between prestructured values on the card [22].

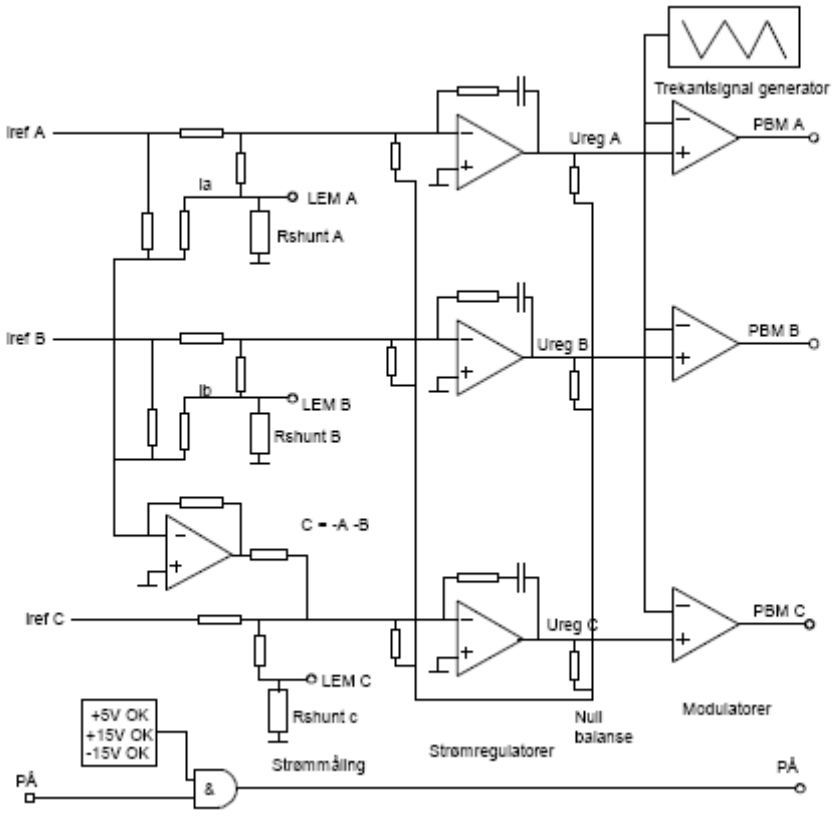

Fig 7.6 Current control card circuitry

Other features of the current control card and examples are listed below [22].

- The three controllers operate independent of each other. Each with its own reference values and current measurements.
- C phase controller works as a slave with output signals dictated by the references and measurements in phase A and B.
- An H bridge configuration can be controlled with the A-phase controller and double PWM by using the B-phase controller as an amplifier which inverts the output signal from A.
- Another way of controlling an H bridge is using the A-phase controller and single PWM by letting the B-phase controller work in opposite phase of the A-phase modulator.

7.1.4 Gate driver

In Fig 7.7 [23] one of the gate drive card used in the experiment is shown. There are two independent, isolated gate drivers which are controlled from isolated logic. Galvanic isolation between the drivers is provided by a DC-DC converter. The voltage signal to gate is in the area of 12V-15V and it can provide a frequency of the gate signal of at least 20 kHz of 400A/1200V IGBTs. Other features of the gate driver card are listed below, and a complete circuit diagram for one driver can be found in appendix C [23].

- 0-100% duty cycle (not included blanking time and delays).
- Blanking time can be adjusted by changing components on the card.
- Independent gate resistors for turn-on and turn-off. Maximum 15A peak gate current.
- 2.5kV$_{RMS}$ isolation spec. between gate drivers and control logic (8.3 mm creepage distance).
- 5 mm creepage distance between the 2 gate drivers.
- Short circuit surveillance between collector and emitter.
- Local turn off when fault with adjustable blocking time (default 0.1 sec)
- Local surveillance of gate driver supplies.
- LED and optocoupler giving active feedback when OK.

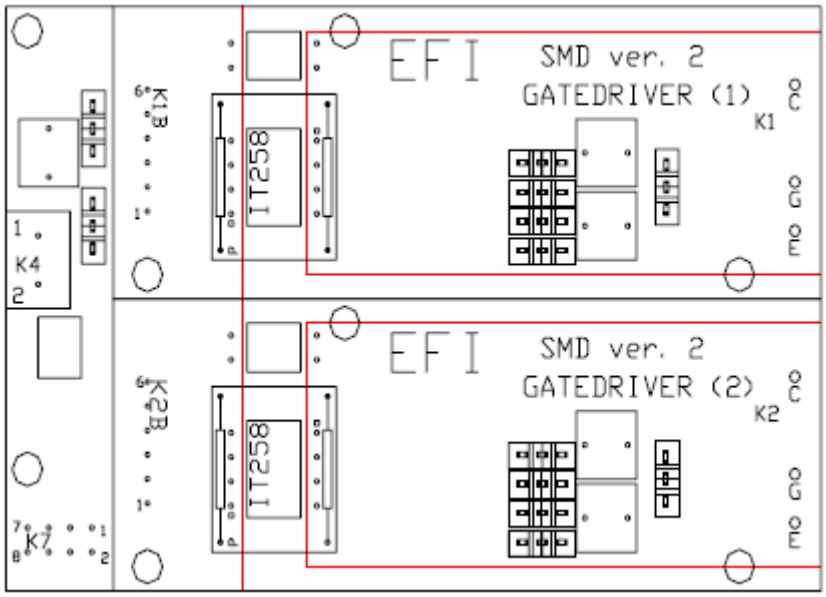

Fig 7.7 Gate driver card

A general purpose, logic level interface card between the control system and the power circuit switches are also available.

7.1.5 Driver interface board

The driver interface board is made for use with the gate driver previously described, and is shown schematically in Fig 7.8 [24].

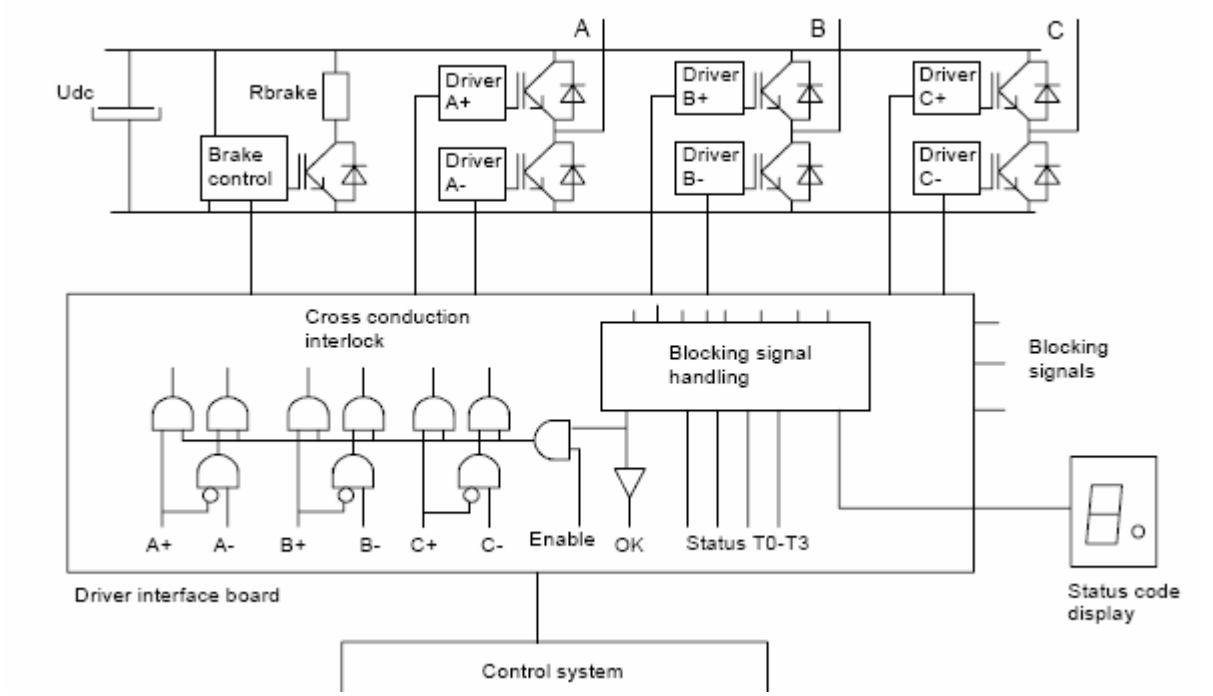

Fig 7.8 Driver interface

Features of this card are listed below [24], and the complete circuit diagram can be found in appendix D.

- Turn-on signal delay for blanking time purpose is provided by circuitry on the board.
- Cross conduction interlock logic gives defined behaviour when both switches in a bridge leg get simultaneous on-signals. The on-signal for the positive switch suppresses the on-signal for the negative switch.
- Both switches in a half bridge can be controlled by the on-signal for the positive switch. The control signal input for the negative switch is set permanently on, and indirectly controlled by the interlock logic.
- A global enable signal is used as an off-signal to block all the on-signals to the drivers.
- All control signals in the driver interface are designed as active signals, with pulldown resistors at the inputs. The control system must give active high signals to initiate switching. This ensures that the power stage is in a safe, passive state if the control system is switched off or disconnected.
- If not all monitoring signals are OK, on-signals will be blocked.

7.1.6 Temperature surveillance

If the junction temperature, T_j, in the IGBT module gets to high, the switching is stopped to prevent destruction of the device. The IGBT module is fabricated with a PTC-resistor which changes its ohmic value as the temperature is increased according to equation (4). This PTC-resistor works as the input to a temperature surveillance card where it is compared to an adjustable reference resistor. When the value of the PTC-resistor becomes lower than the reference value, the OK-signal will be blocked and the output from the card will go low which in turn stops the switching of the module. A simplified sketch of the card of the card is illustrated in Fig 7.9, while the complete circuit diagram can be found in appendix E.

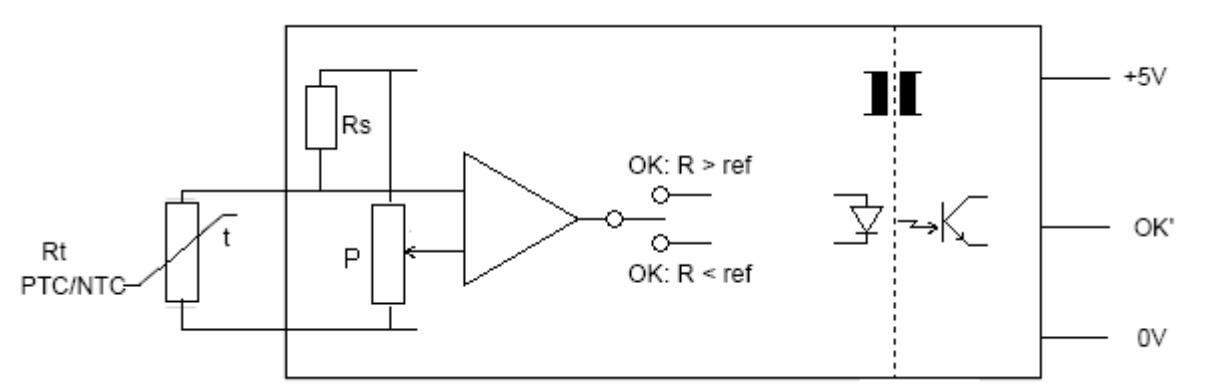

Fig 7.9 Temperature surveillance card

7.2 Pressurising system

Since the pressurising system was not set up, a very brief introduction to one way of setting the experiment up for pressure tests will be described. A suggestion for how to set up a pressurising system is schematically illustrated in Fig 7.10.

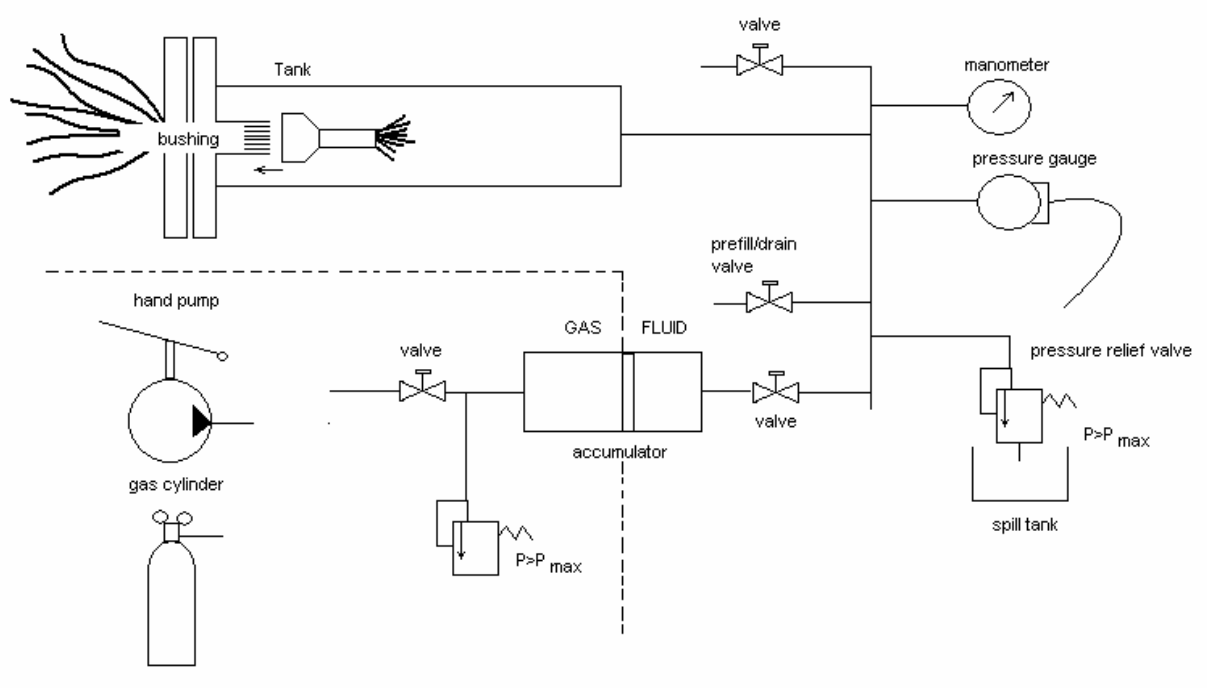

Fig 7.10 Pressurising system

The basic idea is to fill the tank with silicon oil, seal it, and then apply pressure through an accumulator with a piston. The other components are suggestions of safety valves and spill tanks that should be included in the system to ensure a safe working environment. Pressure measurements with logic should also be installed which trips the experiment and opens a pressure relief valve if build up of pressure should occur. To minimize explosion hazard, the pressure should be applied through a hand pump, but gas could also be used.

8 Experimental set up, complete system

Fig 8.1 is a picture of the complete experimental set up with some important components marked with yellow arrows. The test object in this picture is inside the tank which in turn is filled with oil. All the other equipment is set up to operate the IGBT module in the tank together with one bridge leg on the outside as an H-bridge. The inductor is not labelled, but can be seen just above the supply label. Documentation was saved using the scope and the data logger. The data logger was set up to measure temperatures on five different places which are listed in Table 8.1, while the scope captured pictures of the current through the inductor and selected voltages of interest.

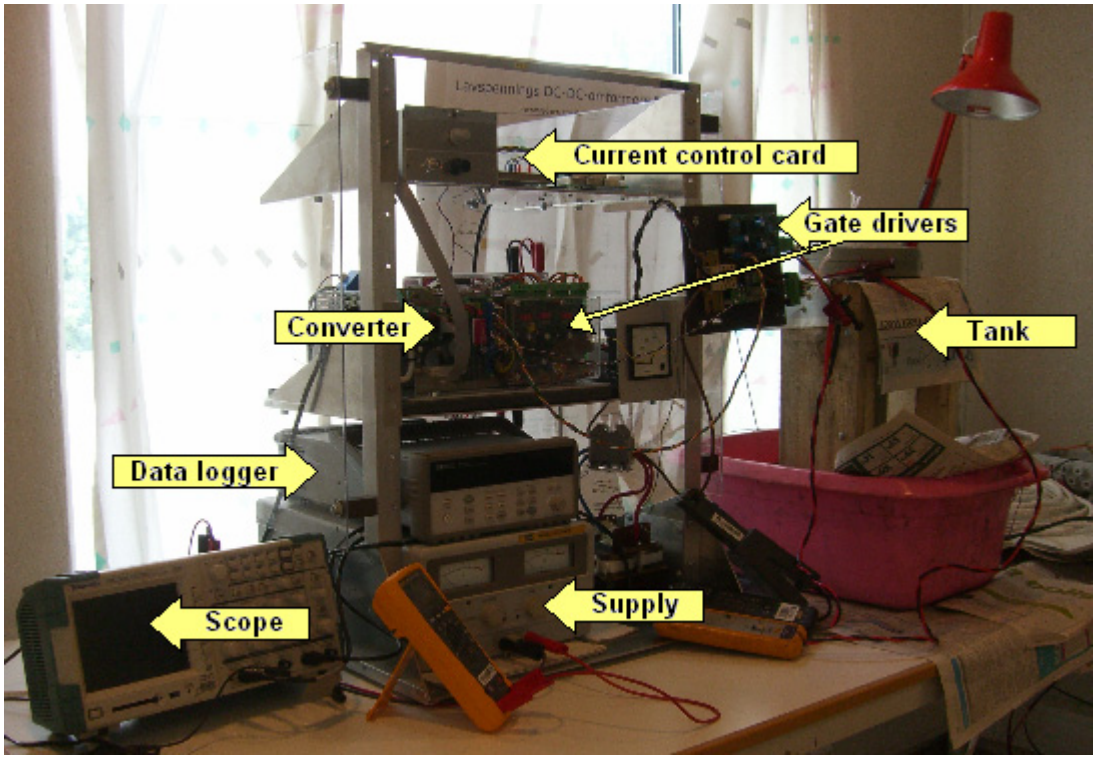

Fig 8.1 Complete experemental set up

Table 8.1 Data logger channels

Ch 1	Temperature on heat spreader
Ch 2	Temperature inside tank at the bottom
Ch 3	Temperature inside the tank at the top
Ch 4	Temperature outside tank wall
Ch 5	Room temperature

The test object inside the tank is shown in Fig 8.2. After this picture was taken, a few modifications were made to ensure electrical isolation from the inside of the tank wall. A plastic casing was put over the capacitors to fully cover the conducting wires, and collector and emitter connections were inspected to see if contact could occur.

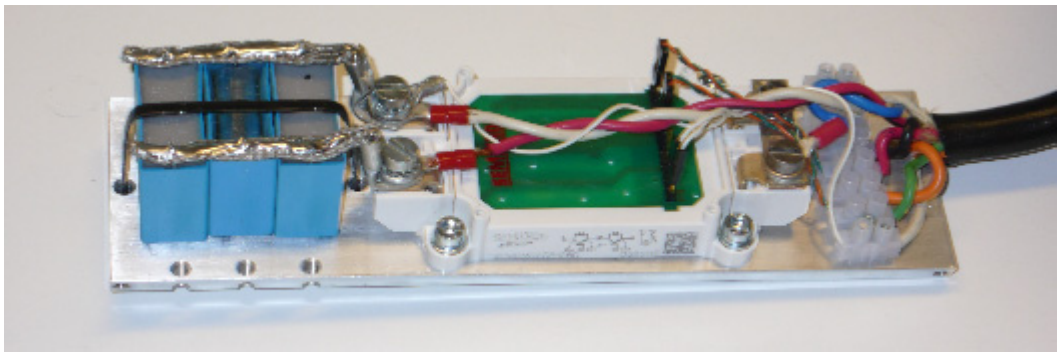

Fig 8.2 Test object

Temperature measurements were assembled on the module using one of the spare screw holes seen in front of the capacitors.

9 Experimental set up, test results

Thorough testing was preformed by first testing the module on the lab bench, then in the tank with air, and finally submerged in oil. The testing procedure was carefully chosen to obtain comparable plots of selected waveforms for room environment and submerged in oil and see if there were any changes of behaviour. Since the waveforms are dependent on the gate driver, it was assured that the same gate driver was used throughout the whole experiment along with all the other components as well.

Documentation was saved using oscilloscope of the Tektronix TPS 2000 family and data logger from Hewlett Packard.

To calculate on state losses and switching losses, the voltage over one transistor was measured along with the current when it was set to always be on. The temperature development in the tank was logged with the data logger with known losses and proportionality was assumed when calculating new losses based on corresponding temperature developments. During constant temperature rise, the slope was calculated for the known effect test. Same procedure was repeated for other temperature development curves, and the ratio between the slopes was assumed to reflect the ratio between the losses.

During intermittent operation the RMS current was calculated using the formula

$$i_{RMS} = \sqrt{\frac{1}{T}\int_0^T I^2 dt} \tag{5}$$

T = Period
I = Current

9.1 Initial testing of behaviour

The test object was first tested outside the tank in room environment. A test card with different settings made it possible to set the transistors to be permanently on, off or switched. The first test was to check if measuring on the transistor altered the behaviour in any way. An oscilloscope picture of the gate emitter voltage measured on one of the gate drivers was the basis for the test. During measurements directly on the transistor, another scope picture of the gate emitter voltage measured on the gate driver was taken and compared with the initial one. There was no visible difference in the two pictures, so it could be concluded that measuring directly on the transistor would not alter the behaviour in any significant way.

9.1.1 Pulse tests with no voltage on DC-link

The gate resistances were not modified and gate turn on resistance, R29, (appendix C) was 4x12 ohm in parallel which combined is 3 ohm, while gate turn off resistance, R28, (appendix C) was 4x39 ohm in parallel which combined is 9.75 ohm.

As an initial test of behaviour, single pulse tests of the some of the transistors were made. The transistor states for the initial pulse test are listed in Table 9.1.

Table 9.1 Transistor status during test

Transistor A+	Always on
Transistor A-	Always off
Transistor B+	Always off
Transistor B-	Switched

The measurements were made directly on the transistor module with no voltage on the power circuit. Oscilloscope channels were as listed in Table 9.2.

Table 9.2 Channel output

Channel 1	Gate-emitter voltage
Channel 2	NA (not available)
Channel 3	NA
Channel 4	NA

Fig 9.1 shows that the driver works as intended and the rise time is fast. This can also be deduced from the IGBT data sheet in appendix where the gate resistance curve is plotted in an I_{RR} vs. di/dt axis system and also reproduced in chapter 9.2. With 3 ohm gate turn on resistance, the current peak is high and hence the injection of carriers happens quickly. Since the gate turn off resistance is larger than the turn on resistance, the fall time is longer as shown in Fig 9.2

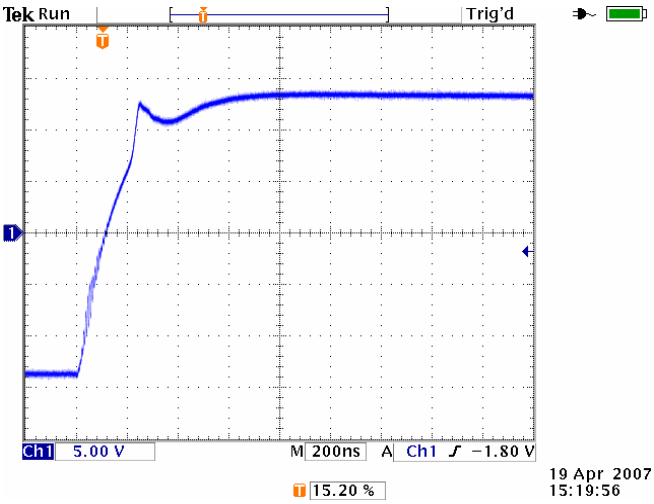

Fig 9.1 Gate-emitter voltage rise, transistor B-

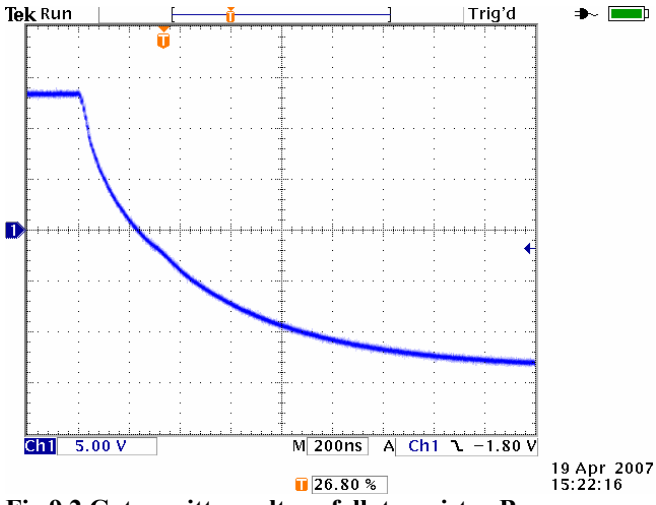

Fig 9.2 Gate-emitter voltage fall, transistor B-

The same test was made on transistor B+, and the results are shown in Fig 9.3 and Fig 9.4 for rise and fall of gate emitter voltage, respectively. This transistor also worked as intended with a fast response.

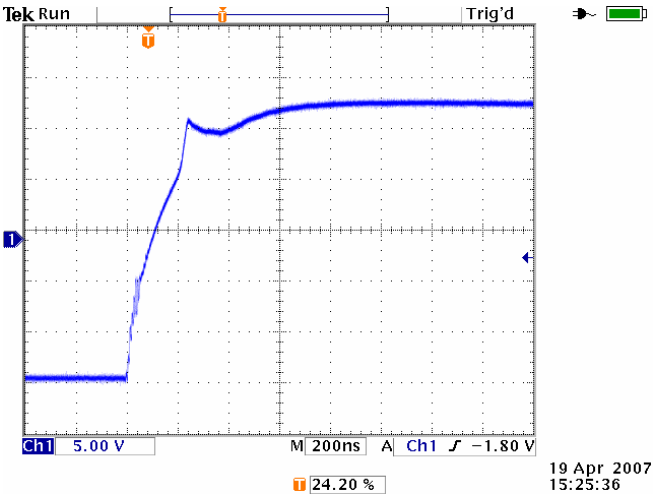

Fig 9.3 Gate-emitter voltage rise, transistor B+

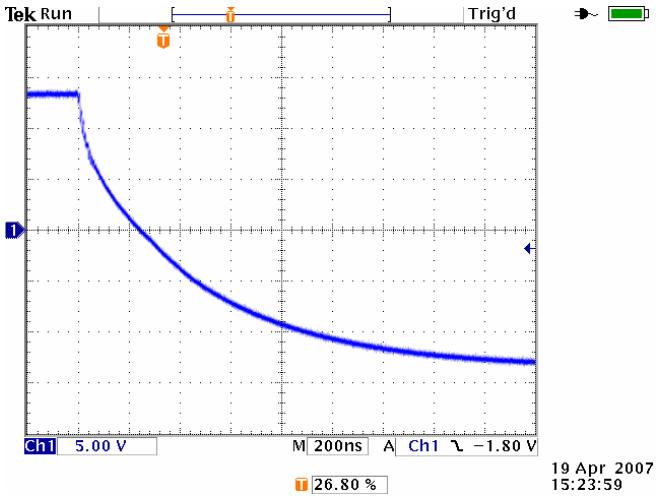

Fig 9.4 Gate-emitter voltage fall, transistor B+

Still with no voltage on the DC-link, the same measurements made in Fig 9.1 and Fig 9.2 were repeated only now measured on the gate driver card. The results can be found in Fig 9.5 and Fig 9.6 for rise and fall, respectively. Oscilloscope channels were as listed in Table 9.3

Table 9.3 Channel output

Channel 1	NA
Channel 2	Gate-emitter voltage measured on gate driver
Channel 3	NA
Channel 4	NA

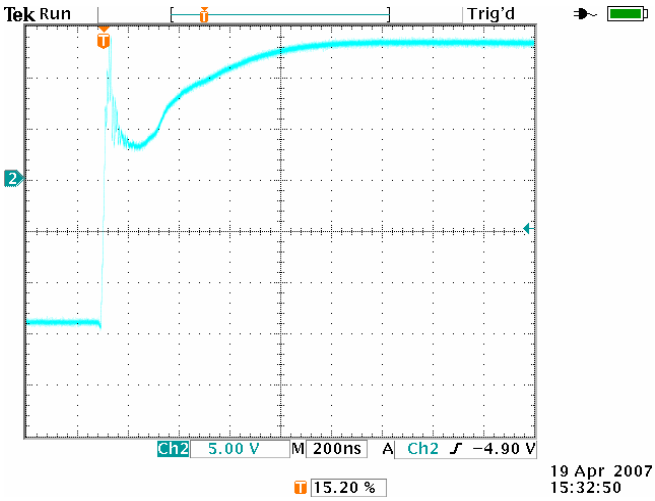

Fig 9.5 Gate-emitter voltage rise measured on gate driver card, transistor B-

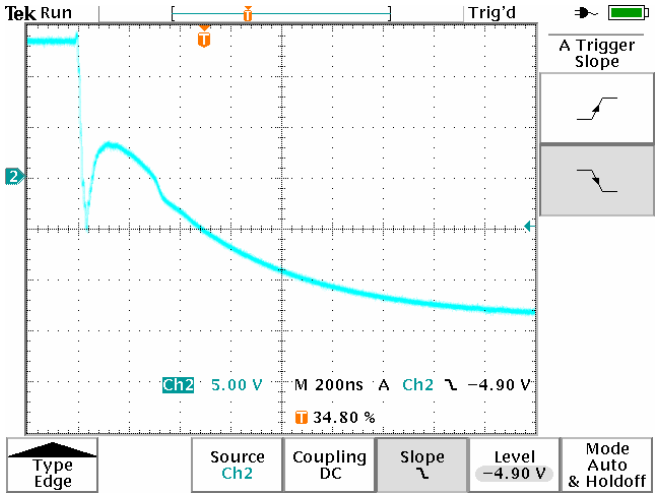

Fig 9.6 Gate-emitter voltage fall measured on gate driver card, transistor B-

In Fig 9.7 and Fig 9.8, the B- transistor gate-emitter voltages from both measurements are shown, i.e. directly on the transistor on channel 1 and on the gate driver on channel 2. As it can be seen, there is some difference in the measurements. This is caused by the inductance in the gate wire. The gate wire length in this experiment is approximately 30cm, which is close to the limit of what is acceptable.

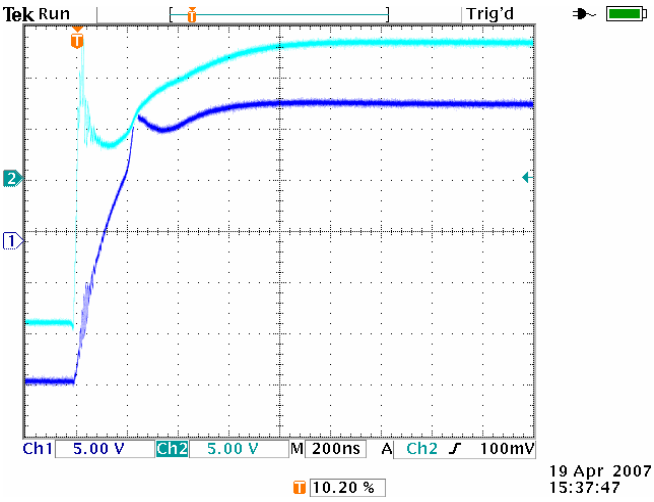

Fig 9.7 Gate-emitter voltage rise measured on transistor (Ch1) and on gate card (Ch2), transistor B-

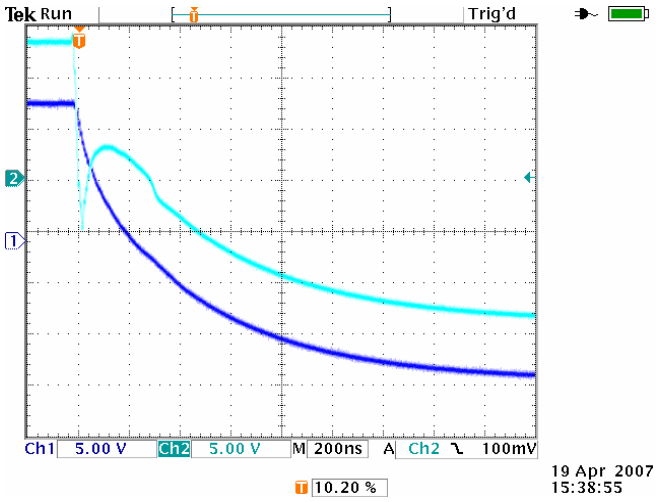

Fig 9.8 Gate-emitter voltage fall measured on transistor (Ch1) and on gate card (Ch2) transistor B-

9.1.2 Pulse tests with voltage on the DC-link

The next step in the testing procedure was measurements with voltage on the DC link when a double pulse was applied on the gate. Double pulse tests were done to check the transistor for both turn on and off and with turn on with leading freewheeling diode. The object under test was transistor B- and no modification was done on the gate driver card. Table 9.4 shows the channel description for the measurements made directly on the transistor.

Table 9.4 Channel output

Channel 1	Gate-emitter voltage on transistor
Channel 2	Collector-emitter voltage on transistor B-
Channel 3	Emitter-collector voltage on transistor B +
Channel 4	Current measurement 10 mV / Ampere

Fig 9.9 shows an overview picture of a double pulse test on the transistor under test with 200V on the DC-link. There are no deviations from what was expected. In Fig 9.10 the first turn off transient is shown with time scale 200 ns/div.

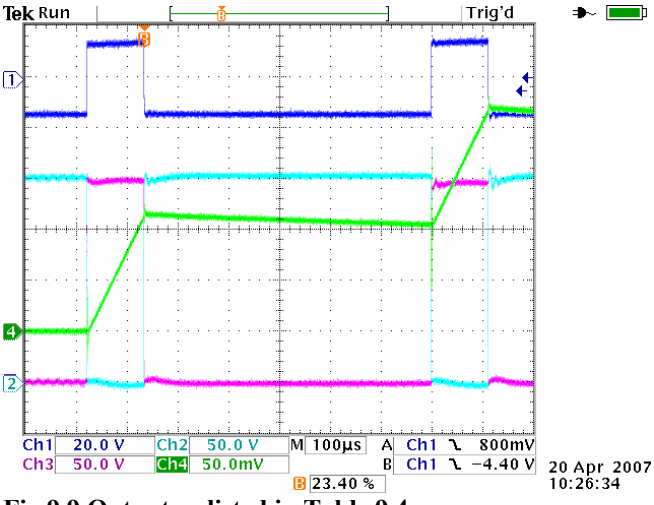

Fig 9.9 Output as listed in Table 9.4

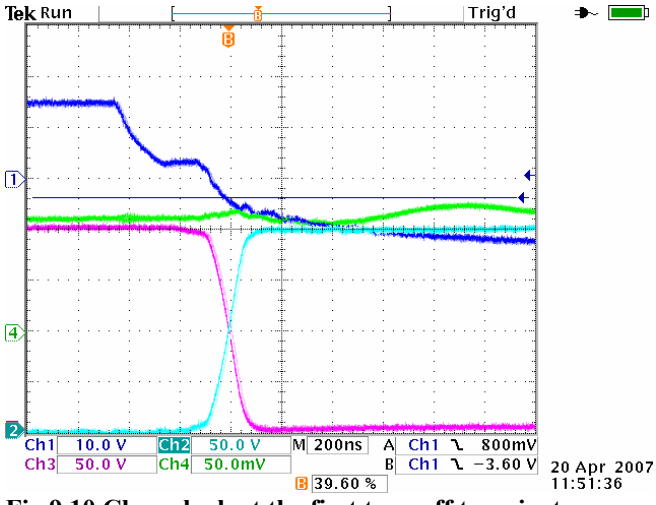

Fig 9.10 Closer look at the first turn off transients

To further check switching characteristics, scope pictures of second turn on and overview of first turn off and second turn on were taken and can be found in Fig 9.11 and Fig 9.12, respectively.

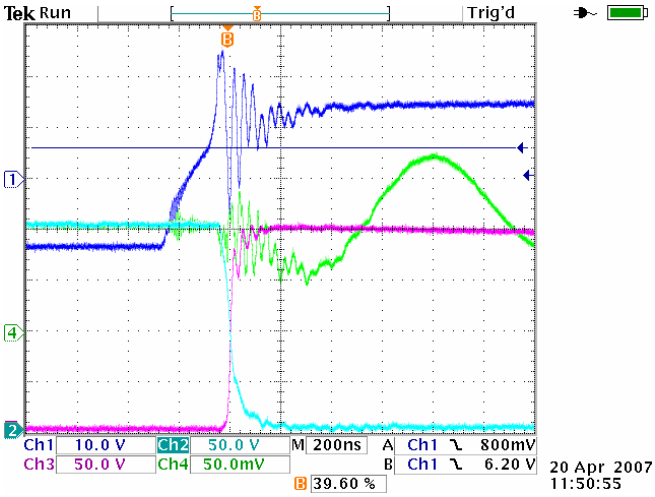

Fig 9.11 Second turn on transients

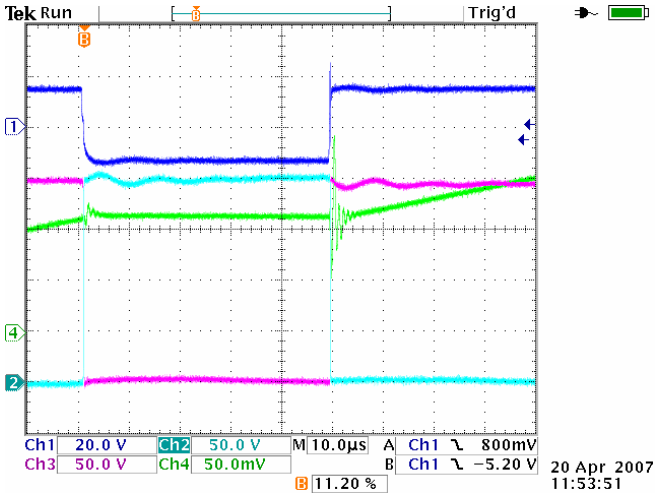

Fig 9.12 Overview of first turn off

With reference to Fig 9.9 to Fig 9.12, it can be concluded that the set up works as intended and no deviations from expected behaviour can be seen. To further investigate the switching transients, 300V was applied to the DC-link with 30 A current flowing through the inductor. This test was done as over voltage detection, and the scope picture is presented in Fig 9.13. The scope picture in Fig 9.14 was taken for oscillation detection to see if the voltage oscillated more than expected. The current were tuned up to 40 A during this test. Nothing wrong was found during the tests.

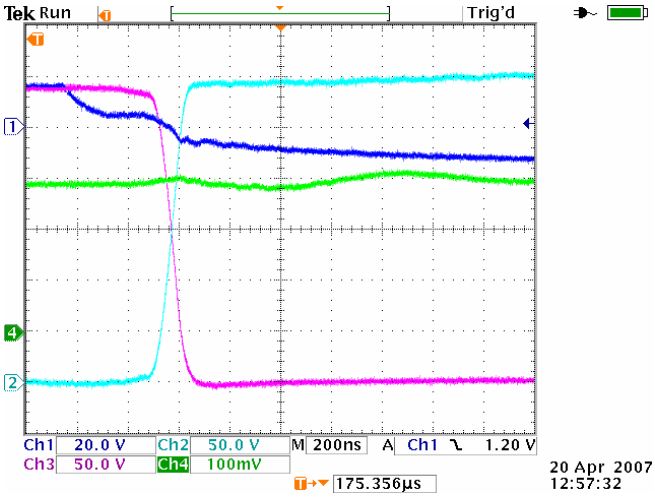

Fig 9.13 Over voltage detection test

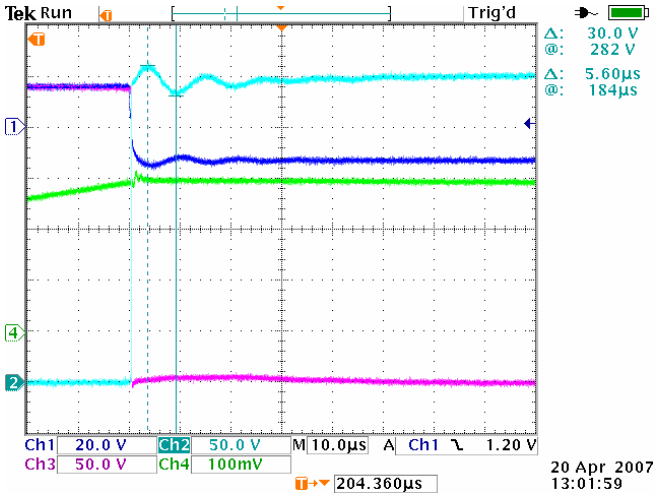

Fig 9.14 Oscillation detection test

As a last measurement before modifying the gate resistances the rise time transients were captured in a scope picture shown in Fig 9.15.

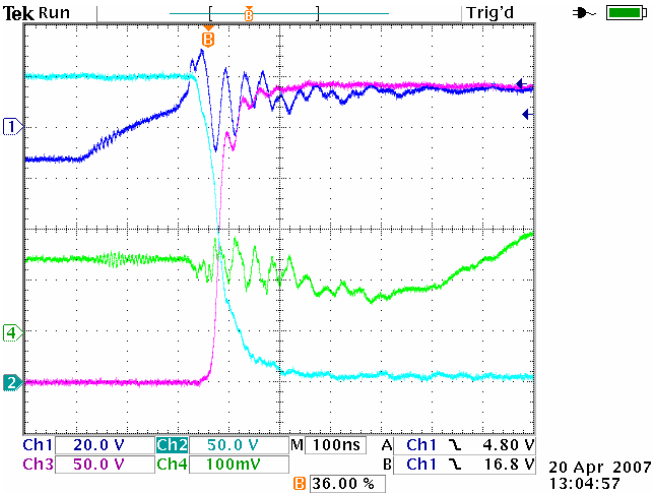

Fig 9.15 Rise time and transients, second turn on

Short circuit protection on the gate driver was not tested. The short circuit protection is assumed to function because of the part of the capacitor bank which is mounted on the heat spreader which has large capacity. Short circuit protection is handled by the gate driver card by measuring on state voltage. If the voltage during on state suddenly increases this is an indication of large currents flowing through the device and the gate driver will turn off the transistor.

9.1.3 Pulse tests; no voltage on DC-link and modified gate driver card

Because the rise time was so fast with the gate turn on resistance previously mentioned, the gate driver card was modified. This was done to limit the large current peak that injects carriers into the base of the transistor as a precaution to avoid destruction of device. Two of the four 12 ohms gate turn on resistances in parallel were removed from the card so that total gate turn on resistance became 6 ohm instead of 3 ohm.

With the new gate turn on resistance, the gate-emitter voltage of the B- transistor was measured during a single pulse test. Both turn on and turn off curve is shown in Fig 9.16, where channel 1 is the turn on and the black curve is turn off.

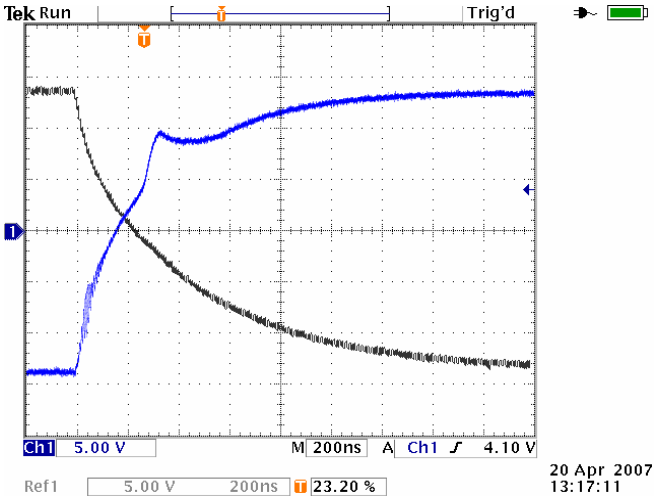

Fig 9.16 Gate-emitter voltage, transistor B- with modified gate resistance

9.1.4 Pulse tests; voltage on DC-link and modified gate driver card

Same tests as for the non modified gate card was done with 300V on DC-link and 12A in a double pulse test. The tests shows the first turn off and turn on with leading freewheeling diode. Measurements were made directly on the transistor with oscilloscope output as listed in Table 9.5.

Table 9.5 Channel output

Channel 1	Gate emitter voltage on transistor
Channel 2	Collector-emitter voltage measured on transistor
Channel 3	Voltage over freewheeling diode (emitter-collector)
Channel 4	Current measurement 10 mV / Ampere

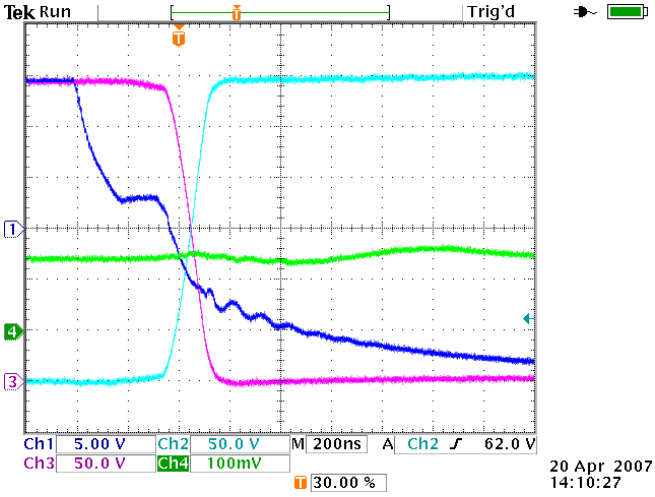

Fig 9.17 First turn off transients with modified gate driver, 300V 12A transistor B-

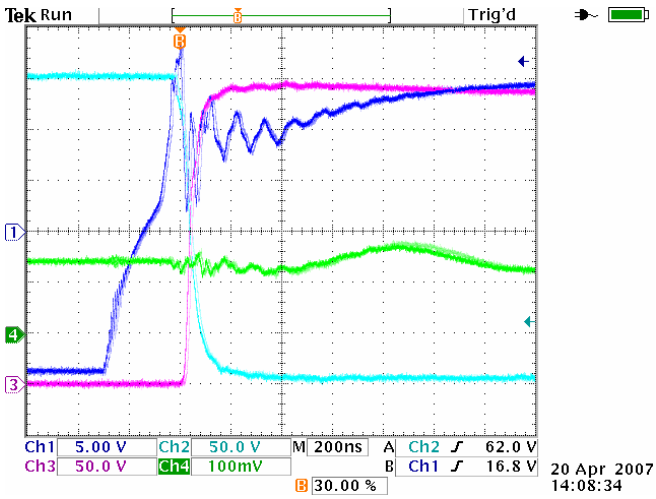

Fig 9.18 Turn on transient with leading freewheeling diode and modified gate driver, 300V 12A transistor B-

The same measurements shown in Fig 9.17 and Fig 9.18 were repeated when measuring on the measure points on the gate driver. As previously mentioned these are the only accessible points when the module is inside the tank submerged in oil. The 300V 12A double pulse test was repeated with curves plotted in Fig 9.19 and Fig 9.20 and channel output as listed in Table 9.5.

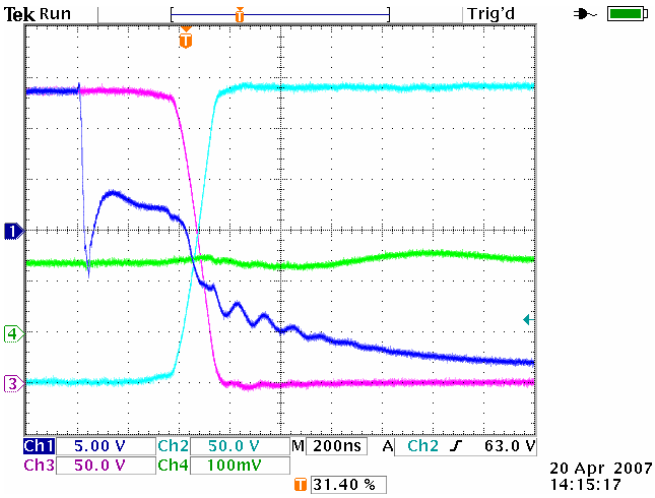

Fig 9.19 First turn off transients measured on gate driver with modified gate resistance, 300V 12A transistor B-

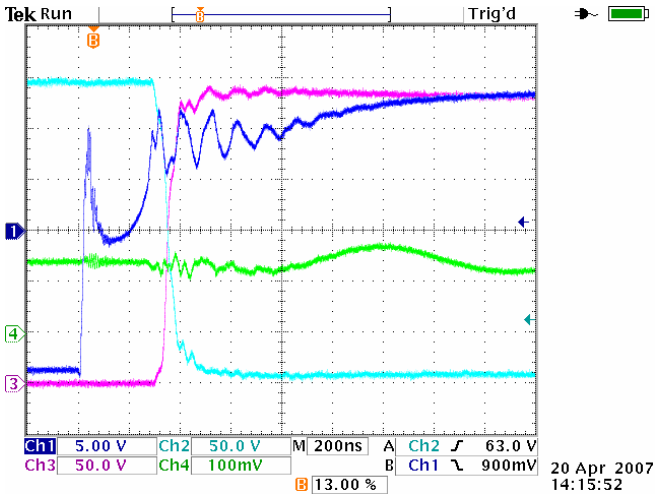

Fig 9.20 Turn on transient with leading freewheeling diode measured on gate driver with modified gate resistance, 300V 12A transistor B-

The effect of the length of the gate wires clearly shows when comparing the curves from the measurements directly on the transistor with the ones made on the gate driver card.

Another observation worth mentioning was that during pulse tests, the temperature guard card was not affected by any noise from the circuitry or measurements.

9.2 Impact of modifying the gate resistance

By comparison of the figures in chapter 9.1.1 with the figures in 9.1.3 it can be seen by the slope of the gate-emitter voltage rise that modifying the gate turn on resistance has direct impact on the rise time. This phenomenon can be described by looking at the curve plotted in Fig 9.21. The initial 3 ohm gate turn on resistance indicates a large di/dt, approximately 4800 A/us, which will quickly charge the Miller capacitance and hence turn on the transistor very fast. To minimize the stress on the chips, the gate resistance was modified to 6 ohm. The di/dt decrease to about 3300 A/us and the steepness of the gate-emitter voltage rise decreases.

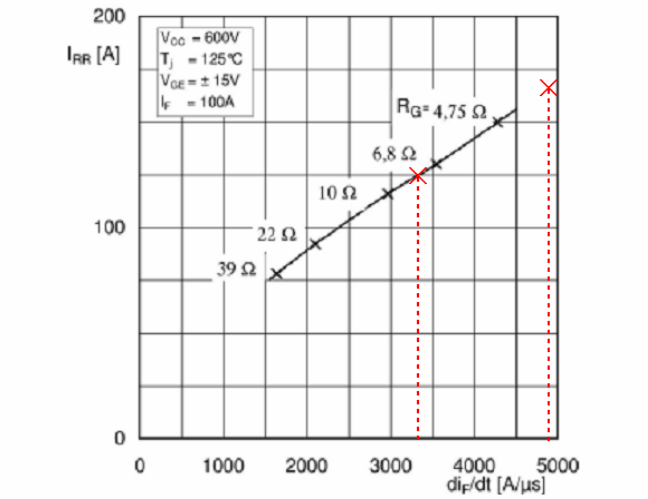

Fig 9.21 Diode peak reverse recovery current

9.3 Continuous switching tests

In the continuous switching test the two bridge legs were switched as an H-bridge configuration with double pulse modulation. This test was similar to the final testing when the module was submerged in oil. Channel output was as listed in Table 9.6.

Table 9.6 Channel output

Channel 1	Gate emitter voltage on transistor
Channel 2	Collector-emitter voltage
Channel 3	NA
Channel 4	Current measurement 10 mV / Ampere

Fig 9.22 and Fig 9.23 shows the results from the continuous switching test for 100V with current 10A and 200V with current 10A, respectively.

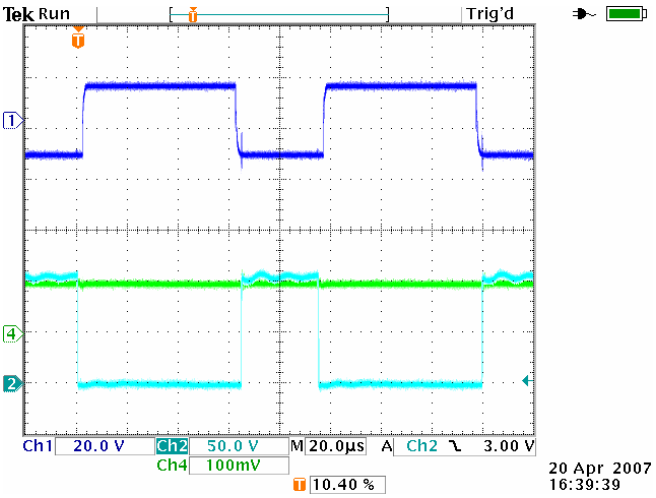

Fig 9.22 Continuous switching test, 100V 10A

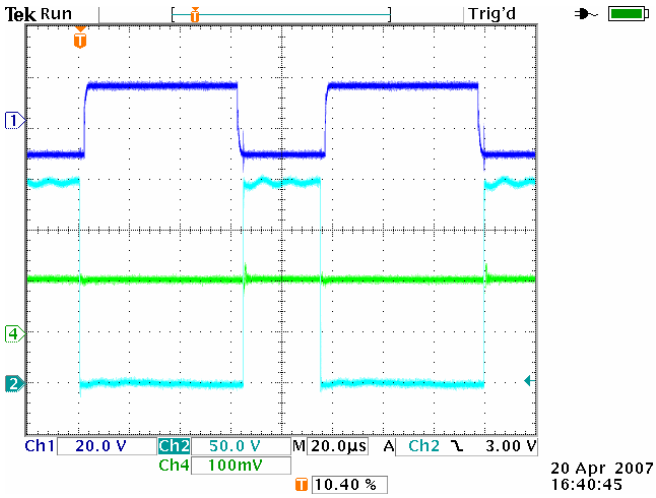

Fig 9.23 Continuous switching test, 200V 10A

9.3.1 Thermal testing

To test the thermal behaviour, the module was run with continuous switching at 300V, 10 kHz and 10A while logging the temperature every 10th second. The temperature measurements were assembled right next to the capacitors. This was done because these are the components which are least temperature resistant. Temperature rise curve is shown in Fig 9.24, where it can be seen that the test were terminated at approximately 85 degrees.

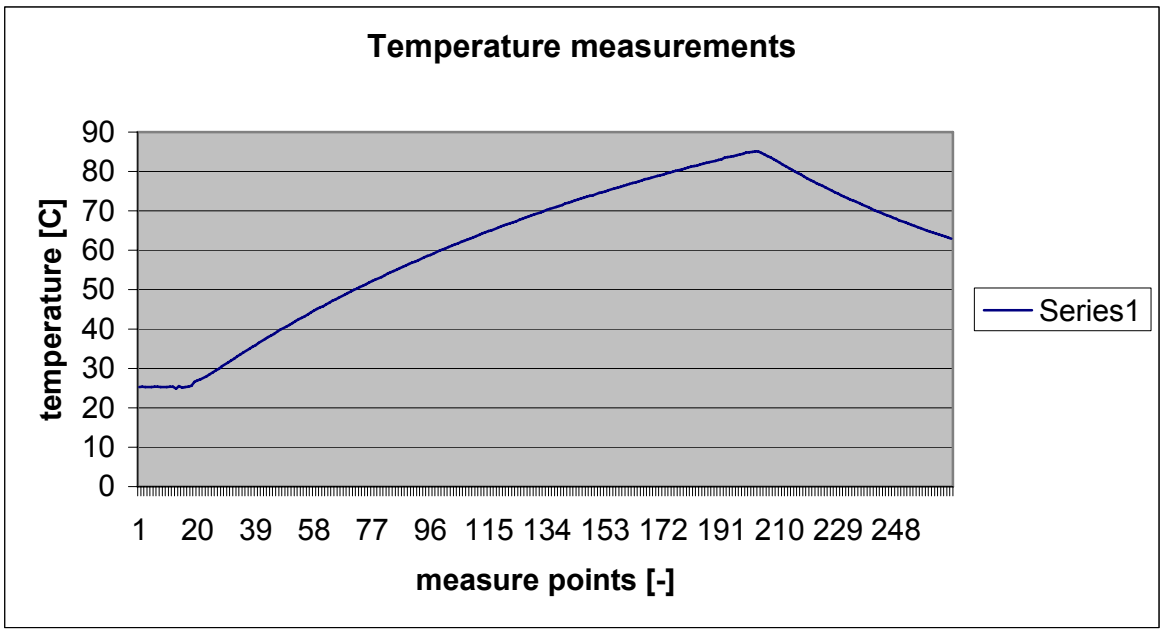

Fig 9.24 Temperature testing of module, 300V, 10A and 10 kHz

The same test was done at 300V and 5A with 10 kHz switching frequency and Fig 9.25 shows the result. The logging was preformed every 10th second. Termination of the test happened at approximately 73 °C when the temperature surveillance card tripped the test.

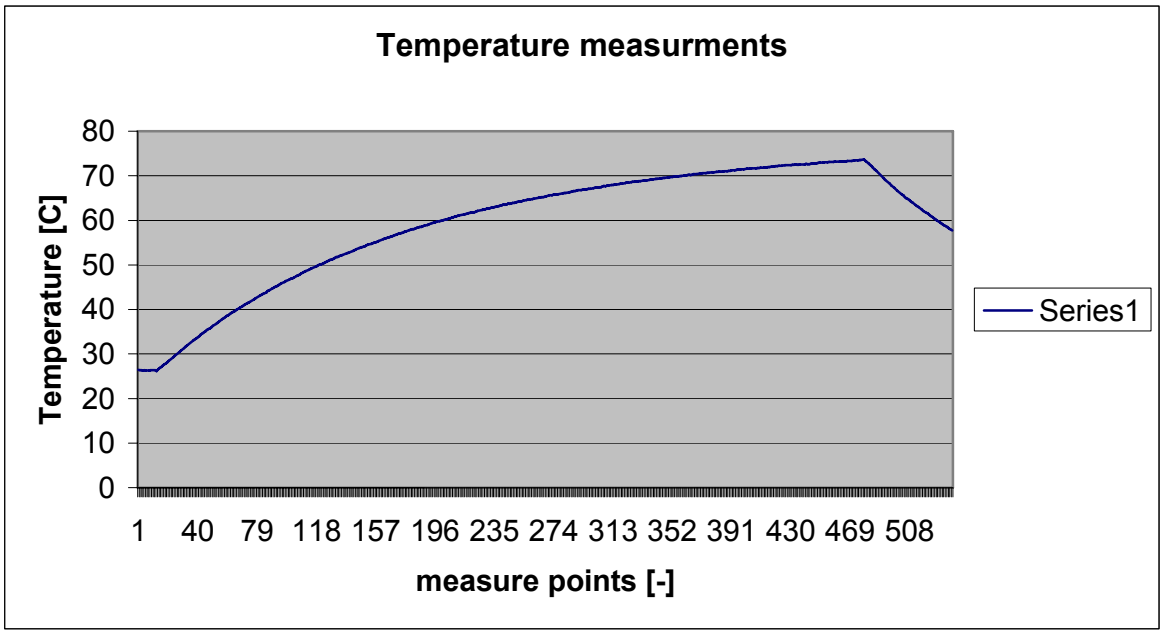

Fig 9.25 Temperature testing of module, 300V, 5A and 10 kHz

9.3.2 Loss measurements

To measure the total losses when all the transistors were operating, the voltage was set to specified values with known switching speeds while the current from the source was read. The results from the tests are listed in Table 9.7 and Table 9.8.

Table 9.7 Loss measurements 10 kHz switching frequency

Voltage [V]	Collector-emitter current [A]	Switching frequency [kHz]	Current from source [A]	Power loss [W]
100	10	10	0.380	38.0
200	10	|10	0.294	58.8
300	10	10	0.284	85.2

Table 9.8 Loss measurements 21 kHz switching frequency

Voltage [V]	Collector-emitter current [A]	Switching frequency [kHz]	Current from source [A]	Power loss [W]
100	10	21	0.516	51.6
200	10	2|1	0.449	89.8
300	10	21	0.461	138.3

With 21 kHz switching frequency, the snubber cards mounted on the frequency converter were heated significantly. The capacitors on the snubber cards may not withstand the heat generated, so the switching frequency was set back to 10 kHz.

To measure the on state losses the transistor H-bridge configuration was set so that transistor A- and B+ where permanently on while A+ and B- where off. The current was fed by a

current source and set to 10 A. The voltage and current of transistor B+ was measured and logged with a data logger. Also logged was the temperature on the heat spreader. To ensure constant effect, a series resistance with approximately 2 V voltage drop was included in the circuit along with a shunt resistor for current measurements. The shunt resistor's conversion ratio was 50 mV equals 15 A.

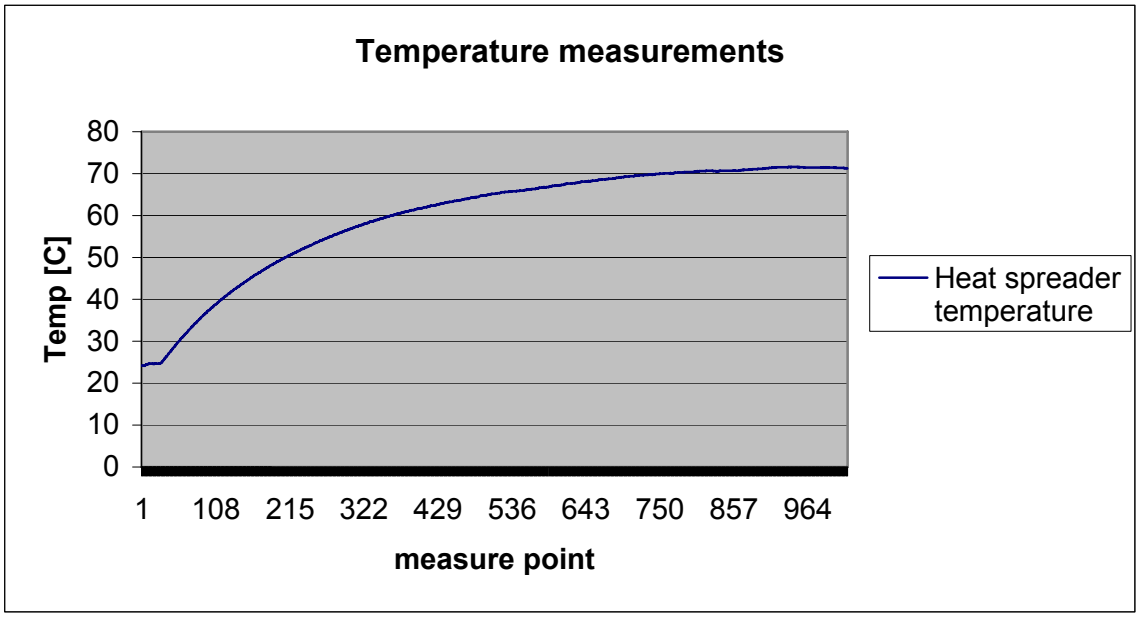

Fig 9.26 Temperature rise with known effect

On state voltage drop over transistor B+ and the current are plotted in Fig 9.27

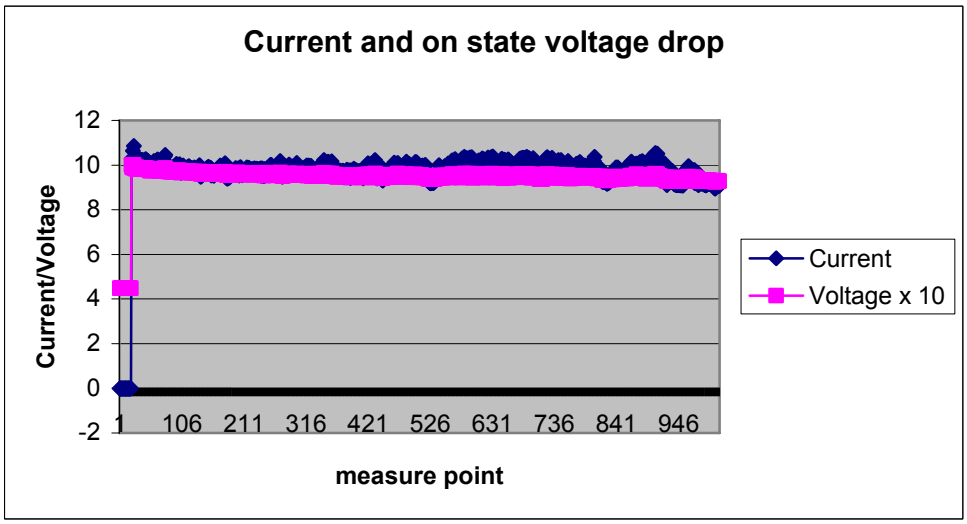

Fig 9.27 Current and voltage of transistor B+

With decreasing on state voltage over the transistor, the current was slightly increased. This was due to the resistance connected in series with approximately the same voltage drop as the two leading transistors. As the voltage decreases, the current increases to maintain the same power. This can be detected in Fig 9.27 where the trend of increasing current with decreasing voltage can be seen and further in Fig 9.28 where the power tends to stay fairly constant. The averaged value of the losses, indicated with the pink graph, is 9.13 W for the transistor B+.

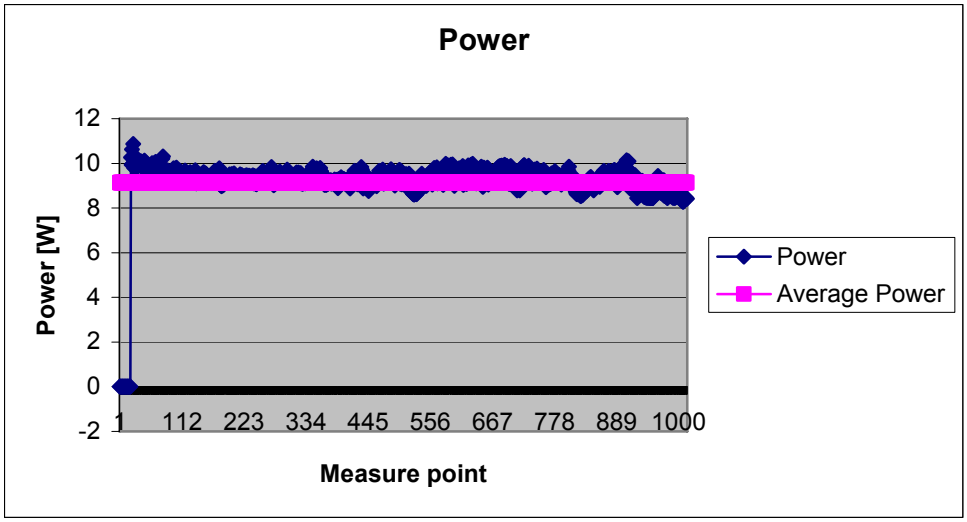

Fig 9.28 Power measurments and calculated average value

9.4 Testing with the module submerged in silicon oil

The same on-state loss test was repeated right after the tank was filled with silicon oil. This was done to investigate the cooling effect of submerging the module in a fluid, and to get a reference for loss calculations. The fluid circulates as it gets heated up and transports the heat to the periphery of the tank more efficient than when air filled. The temperature development is shown in Fig 9.29.

As a reference for subsequent loss measurements, the slope of the constant temperature rise for the test with known effect is calculated to be 0.439 °C/min. The slope is calculated from measure point 167 at 27.026 °C to measure point 191 at 28.782 °C, with 10 seconds between every measure point.

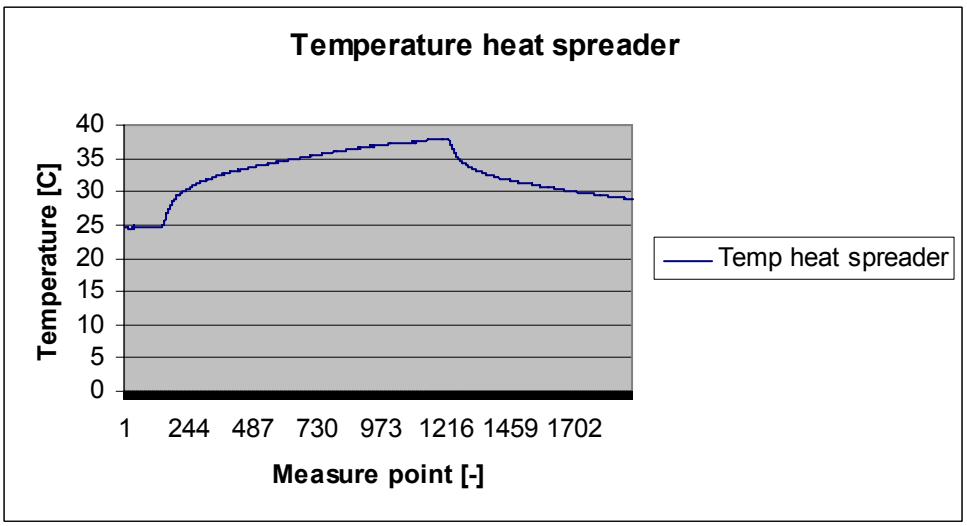

Fig 9.29 Temperature development with known losses

In the subsequent chapters, short term continuous switching test, intermittent operations tests and long term continuous switching tests follows.

9.4.1 Short term continuous switching test

A continuous switching test was performed with the module submerged in oil. The first testing was to ensure that the oil did not affect the switching in any way, and that the material is compatible with the silicon oil without any instant catastrophic failures. Scope pictures from the switching of transistor B- was captured with the channel output as listed in Table 9.9. The channel output was identical for all subsequent tests, if not otherwise is specified.

Table 9.9 Channel output

Channel 1	Collector-emitter voltage. Ratio 1/200
Channel 2	Gate-emitter voltage. Ratio 1/50
Channel 3	NA
Channel 4	Current measurement 10 mV / Ampere

The voltage reference was set to 50% on the current control card, and the DC-link voltage was set to 300V. With switching frequency of 10 kHz, the current from the source showed 0.310A.

Fig 9.30 and Fig 9.31 are two scope pictured captured at the start and the end of test, respectively. The temperature in the first picture is at approximately 33 °C while it was 56 °C at the end of the test.

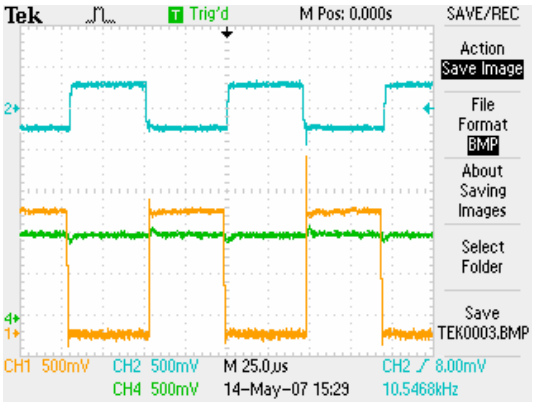

Fig 9.30 Scope picture at start of test

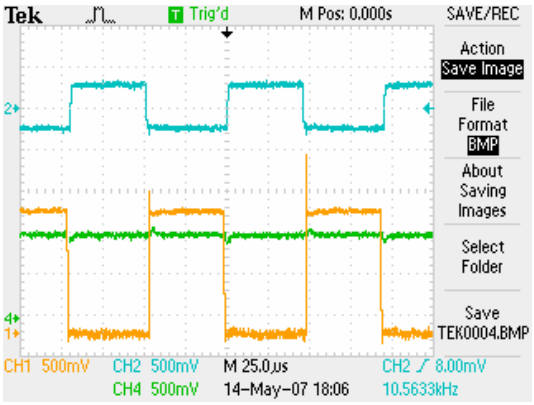

Fig 9.31 Scope picture at end of test

Two conclusions can be made when comparing the scope pictures in Fig 9.30 and Fig 9.31 with the ones where the transistor is operated in room environment. The first is that no instant catastrophic failure occurred when operating the module in the new environment, and the other that the new environment did not change the behaviour of the transistor.

To further investigate that in fact the oil does not alter the behaviour, a closer look at one of the turn off transient is presented in Fig 9.32.

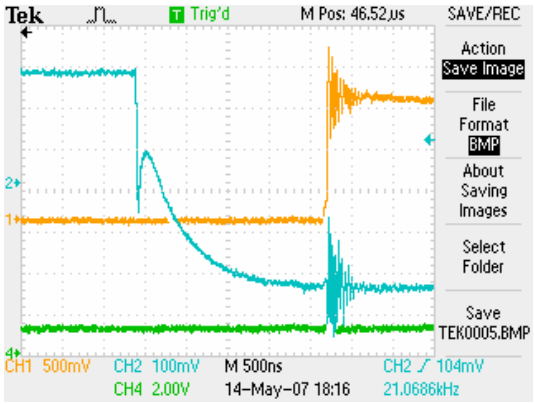

Fig 9.32 Turn off transient when submerged

The waveforms captured are similar to the ones without oil and Fig 9.30 to Fig 9.32 shows that the short term effect of the IGBT module submerged in silicon oil is negligible.

Temperature development inside the tank during the test is shown in Fig 9.33. The slope of the temperature rise during constant rise is calculated to be 1.503 °C/min based on values from measure point 291 at 27.882 °C to measure point 315 at 33.895 °C. When assuming proportionality with the known losses case, the losses in this test is approximately 3.42 times higher i.e. 31.2 W. With on state losses little over 9 W, the switching losses adds up to be about 22 W.

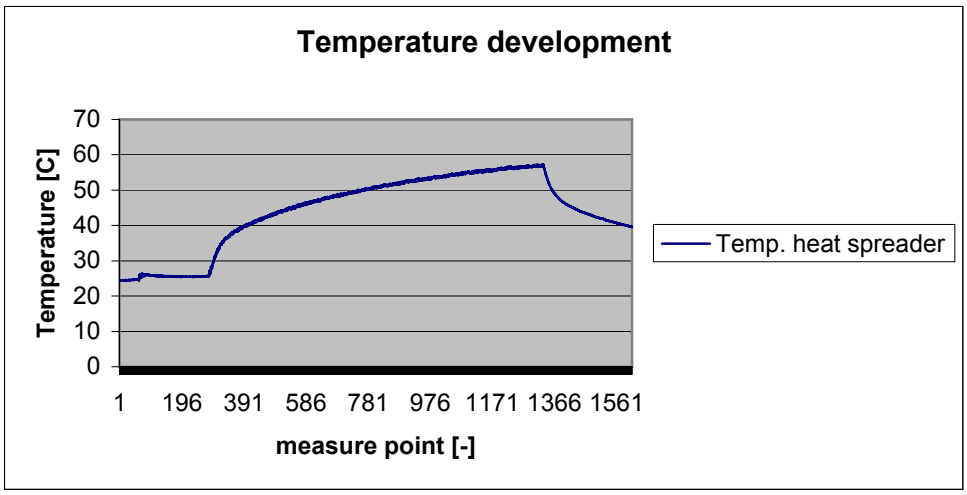

Fig 9.33 Temperature development, 300V 10A submerged continuous switching test

9.4.2 Intermittent operation with 20 A pulses

Because of the limitations in current carrying capabilities of the wires penetrating the tank, intermittent operation test was initiated with current pulses of 20 A. This was done by connecting a pulse generator on the current reference on the current control card. The pulses were calculated according to (5) and set to be ¼ of a period so that the rms value of the current equalled 10A. The frequency of the pulses was 2 Hz, so the duration of the current pulses was 125 ms.

Fig 9.34 is a scope picture of channel 4, and shows the current pulses at the start of the test at approximately 30 °C. The ratio between the voltage measured and the actual current is as listed in Table 9.9.

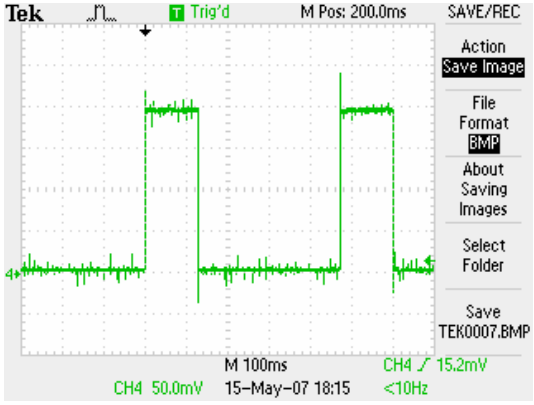

Fig 9.34 Current pulses 20A intermittent operation

The switching pulses and a closer look at a turn off transient are shown in Fig 9.35 and Fig 9.36. No deviations from expected behaviour are detected in the waveforms.

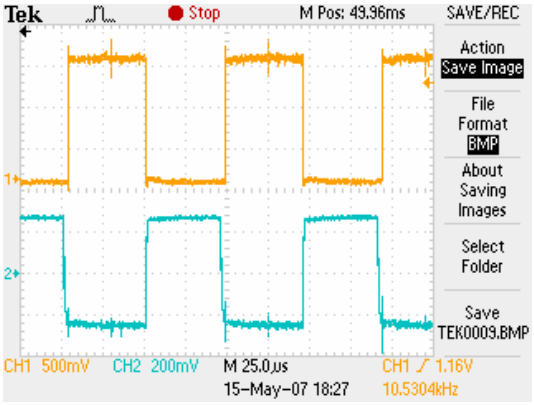

Fig 9.35 Switdhing pulses

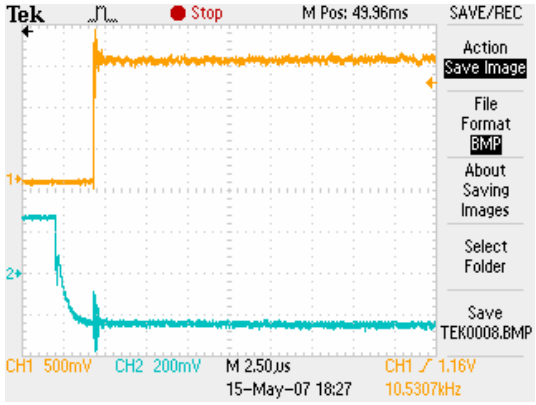

Fig 9.36 Turn off transient

At the end of the test at 42 °C, current- and switching pulse pictures were captured and shown in Fig 9.37 and Fig 9.38.

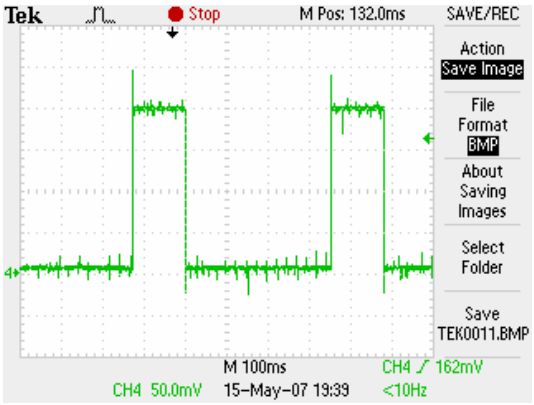

Fig 9.37 Current pulses 20A intermittent operation at end of test

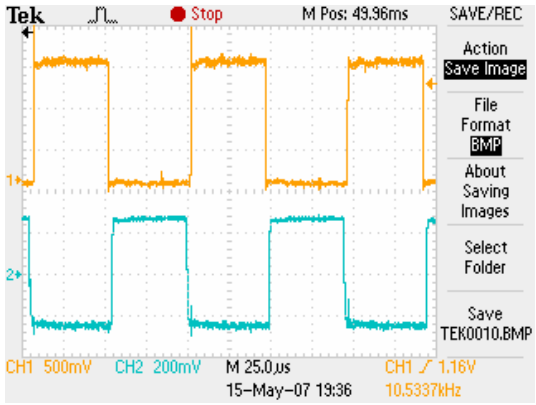

Fig 9.38 Switching pulses at end of test

The temperature development is shown in the figure below. The star indicates when the scope pictures were taken.

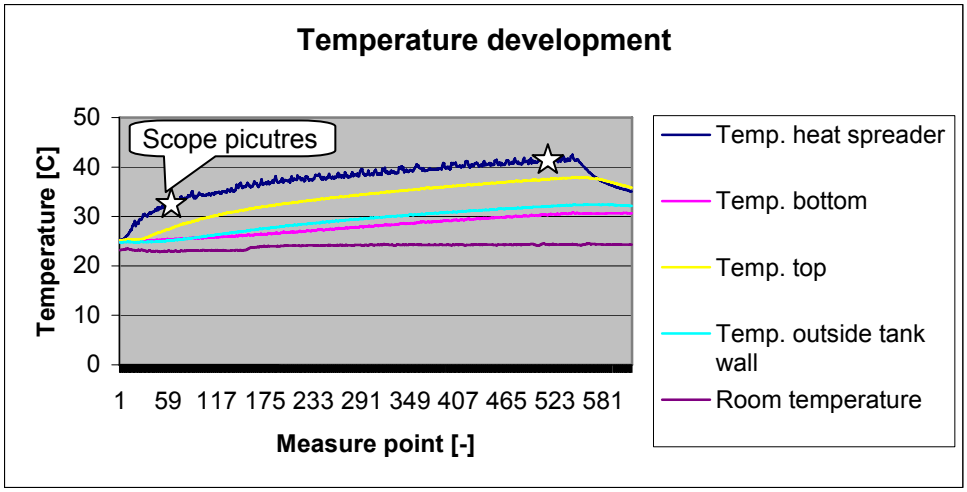

Fig 9.39 Temperature development during 20A intermittent operation test

All the figures from the intermittent operation test with 20A pulses show no sign of malfunction of device.

9.4.3 Intermittent operation with 30A pulses

Due to limitations in the wires, the rms value of the current was still held at 10A. With the frequency of the pulses at 2 Hz, the width of the pulse was calculated according to (5) to be 1/9 of a period. To avoid over voltage on the current control card, the shunt resistance for current measurements was modified by adding another resistance in parallel.

The scope pictures below shows the current pulses, switching pulses and turn off transient, respectively. These first scope pictures were taken at approximately 28 °C at the start of test.

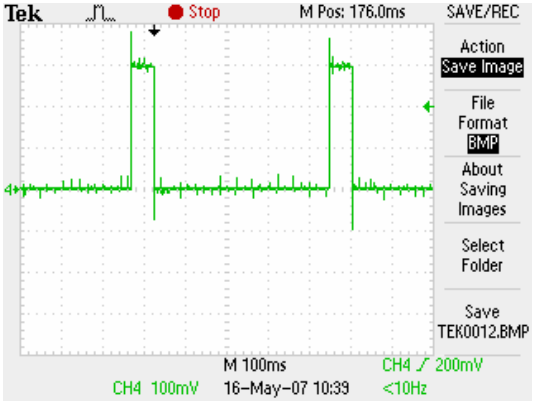

Fig 9.40 Current pulses 30A intermittent operation

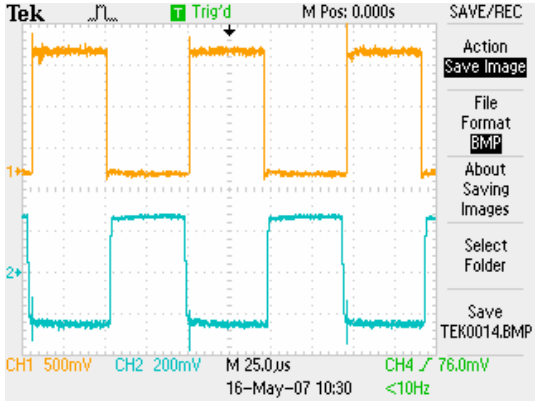

Fig 9.41 Switching pulses start of test

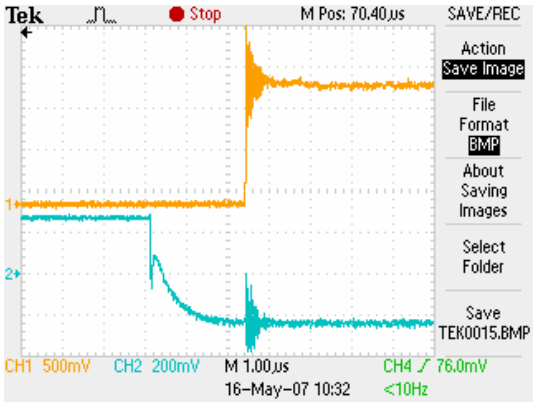

Fig 9.42 Turn off transient

As for the 20A intermittent operation, no deviations from normal behaviour can be detected. The same graphs were captured at the end of test at approximately 40 °C, and shown in Fig 9.43, Fig 9.44 and Fig 9.45.

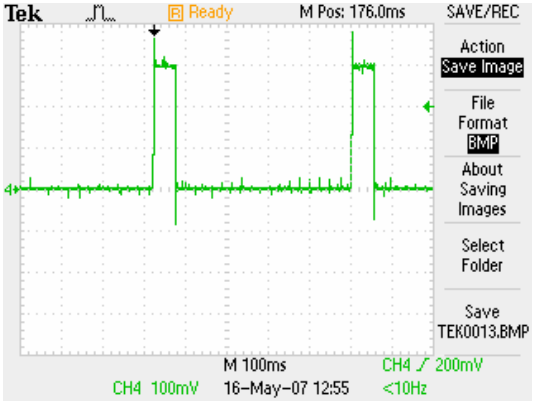

Fig 9.43 Current pulses 30A intermittent operation at end of test

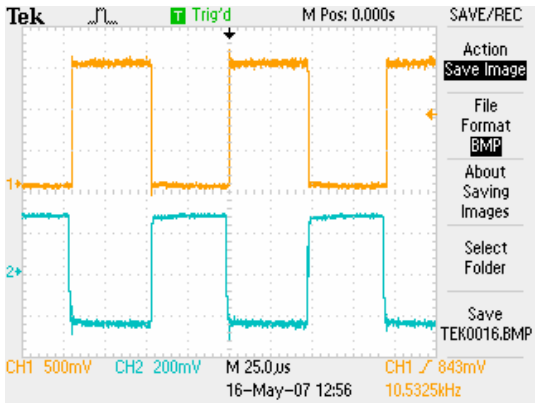

Fig 9.44 Switching pulses at end of test

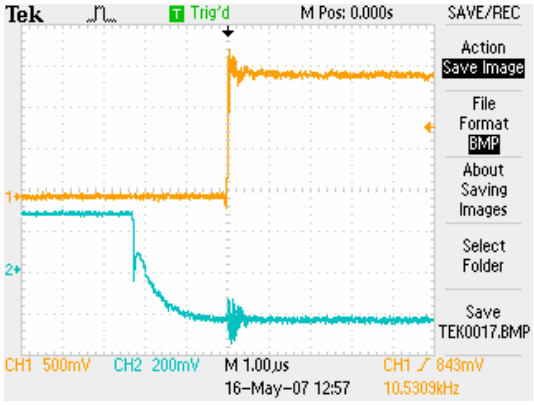

Fig 9.45 Turn off transient at end of test

The temperature development during the 30A intermittent operation test is shown in Fig 9.46.

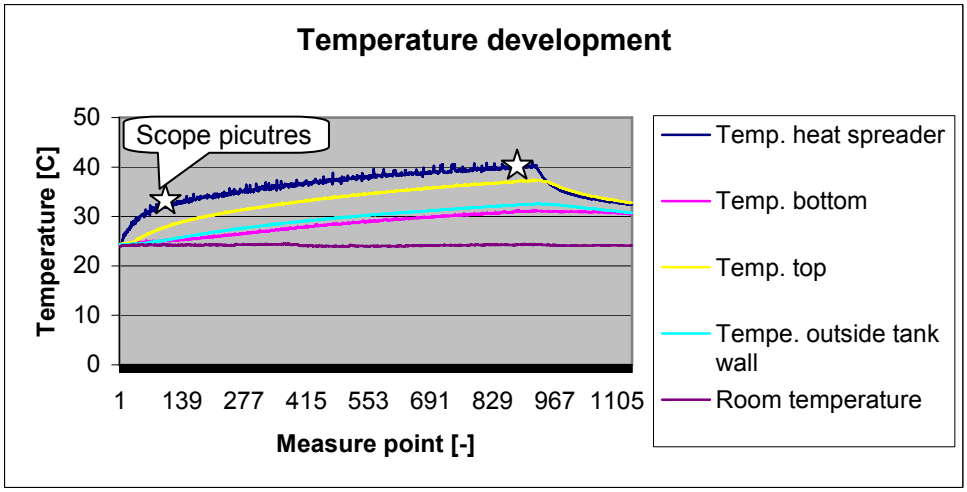

Fig 9.46 Temperature development 30A intermittent operation test

As for the 20A current pulse test, the figures for the 30A intermittent operation test show no sign of malfunction.

9.4.4 Intermittent operation with 40A pulses

The same procedure was repeated with calculating the pulse width according to (5), and capturing scope pictures which are shown in Fig 9.47 to Fig 9.49 at the start of test with temperature of about 28 °C

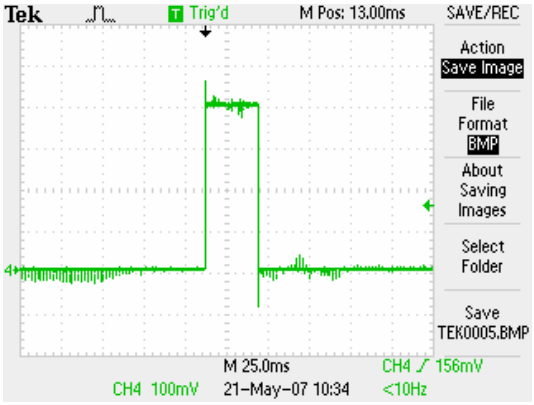

Fig 9.47 Current pulse 40A intermittent operation at start of test

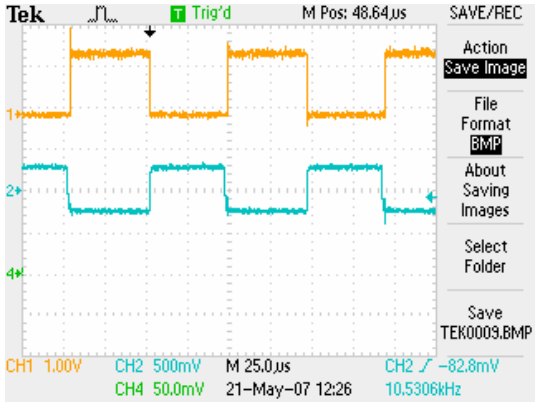

Fig 9.48 Switching pulses at start of test

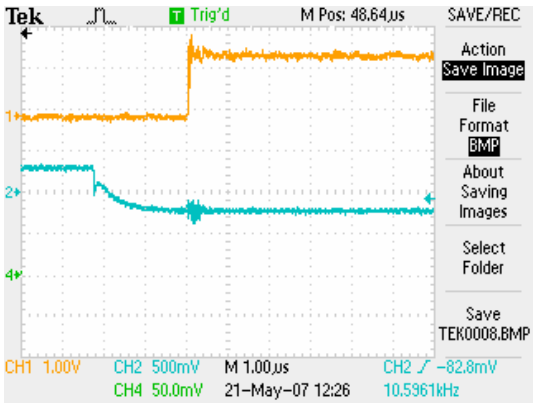

Fig 9.49 Turn off transient at start of test

The same pictures were taken at the end of test at about 38 °C and shown in Fig 9.50 to Fig 9.52.

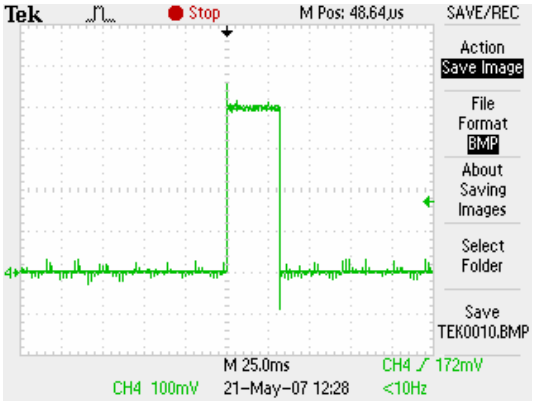

Fig 9.50 Current pulse 40A intermittent operation at end of test

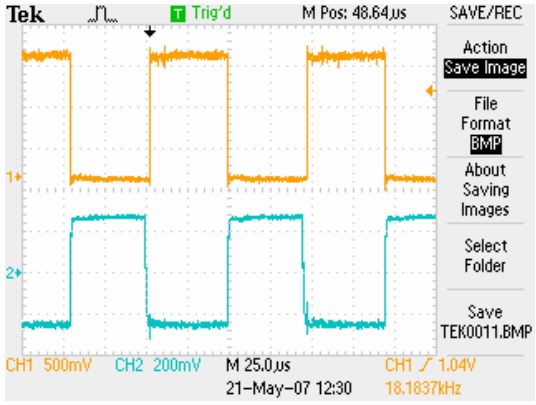

Fig 9.51 Switching pulses at end of test

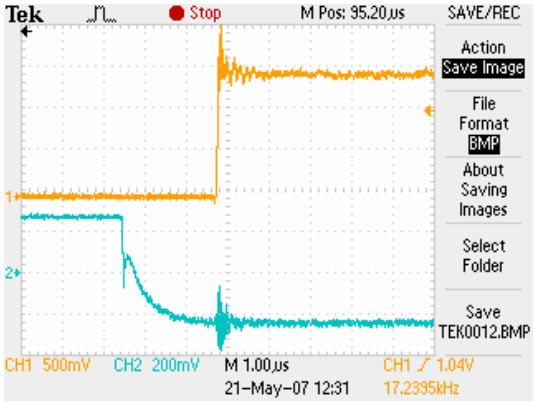

Fig 9.52 Turn off transient

Temperature development for the 40A intermittent operation test is plotted in Fig 9.53.

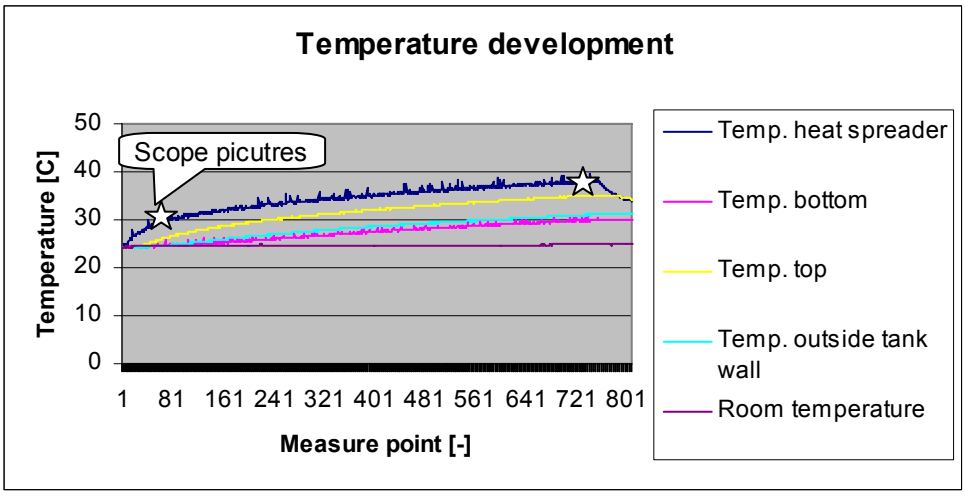

Fig 9.53 Temperature development 40A intermittent operation test

The selection of graphs from the 40A intermittent operation test shown in the previous figures shows no sign of deviation from normal behaviour.

9.4.5 Continuous switching 10 hour durations

After intermittent operation tests, the system was set to run at fixed current reference and continuous switching for longer durations. As a first long term test, the system was set on for two 10 hour periods. As the graphs show, the current reference was 10A with 10 kHz switching frequency, and the voltage on the DC-link was 300V. The channel output was as listed in Table 9.10.

Table 9.10 Channel output

Channel 1	Collector-emitter voltage. Ratio 1/200
Channel 2	Gate-emitter voltage. Ratio 1/50
Channel 3	NA
Channel 4	Current measurement 10 mV / Ampere

The scope pictures below shows the waveforms and a turn off transient for the first and second long term test at the end of test.

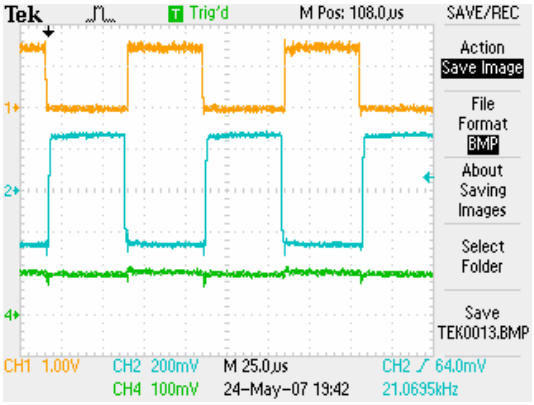

Fig 9.54 Waveforms at end of first long term test

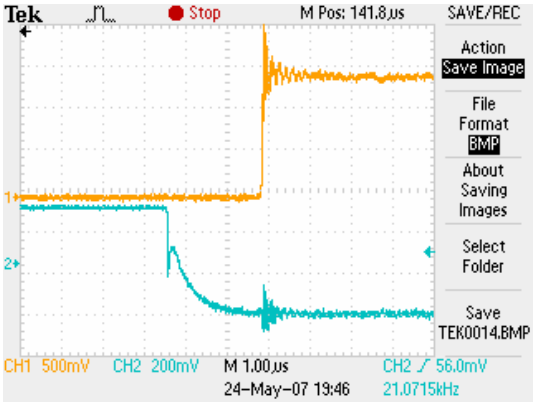

Fig 9.55 Turn off transient at end of first long term test

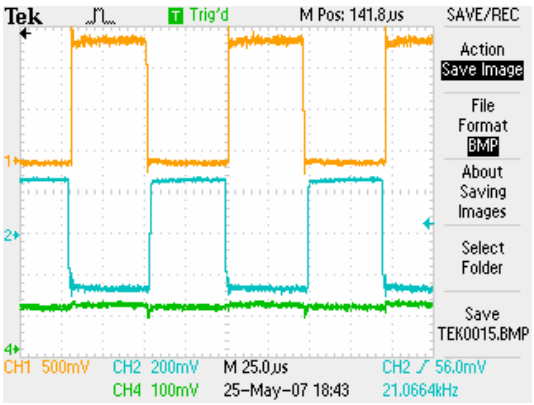

Fig 9.56 Waveforms at end of the second long term test

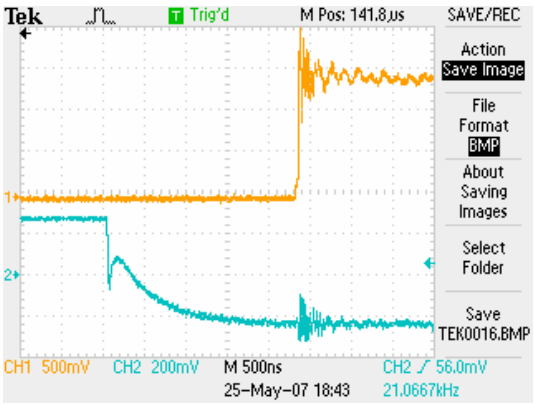

Fig 9.57 Turn off transient at end of second long term test

As it can be seen, there are no indications of change of behaviour after 10 hours continuous switching submerged in oil. The temperature development during the last of the 10 hour periods is shown in Fig 9.58. Slope of the temperature curve during constant rise is calculated to be 1.577 °C/min which is about the same as for the short term continuous switching test since the test criteria in both cases were similar except for the duration. The switching losses and on state losses are then 22 W and 9 W, respectively.

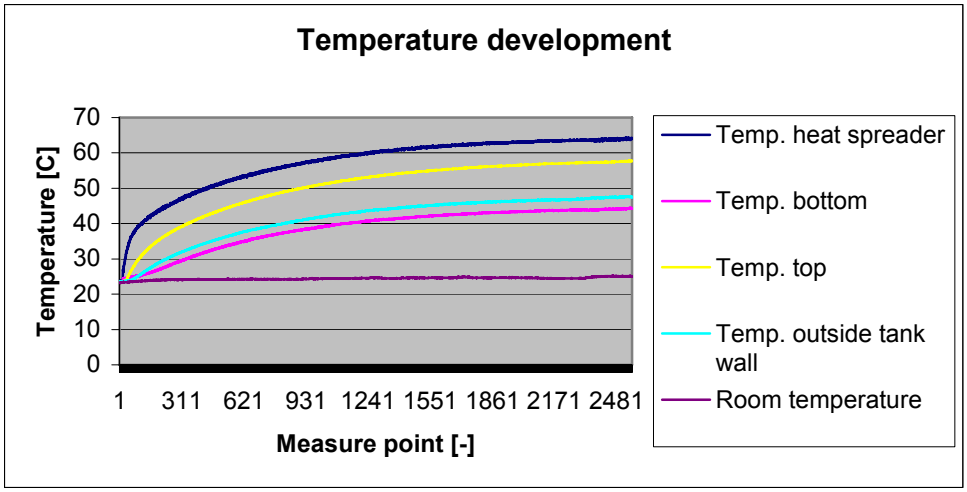

Fig 9.58 Temperature development during 10 hour continuous switching test

The temperature stabilised at approximately 64 °C which is considerably lower than the limit set on the temperature guard.

9.4.6 Long term continuous switching submerged in oil

After thorough testing, both intermittent and with fixed current reference for longer periods of time, the system could be considered safe for testing with out human presence. The long term test was started June 5th and terminated June 11th after six days of continuous switching submerged in oil. Table 9.11 shows the channel output.

Table 9.11 Channel output

Channel 1	Collector-emitter voltage. Ratio 1/200
Channel 2	Gate-emitter voltage. Ratio 1/50
Channel 3	NA
Channel 4	Current measurement 10 mV / Ampere

Fig 9.59 and Fig 9.60 are the same waveforms captured at the start of test and end of test, respectively. There are no visible differences between the two pictures and the temperature was approximately 66 °C.

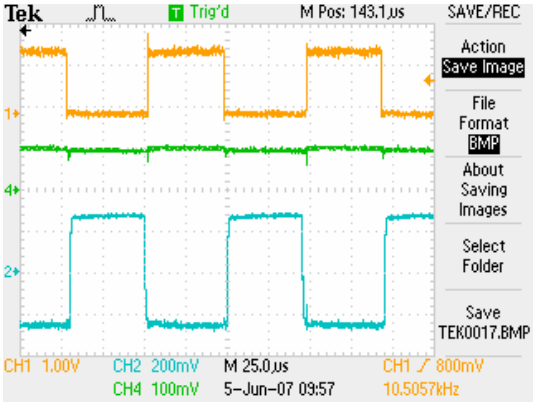

Fig 9.59 Waveforms at start of test

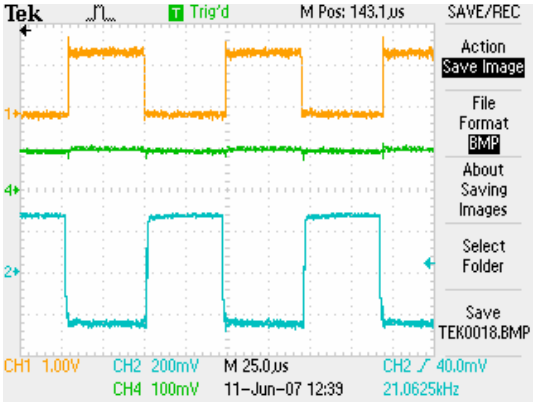

Fig 9.60 Waveforms at end of test

One turn-off transient is captured in Fig 9.61 where it can be seen that the turn off is similar to all the other measurements both submerged and in air.

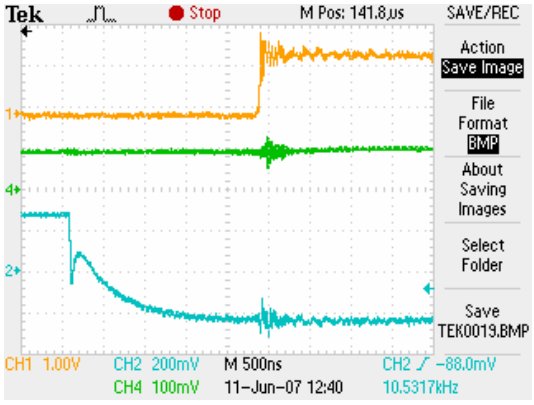

Fig 9.61 Turn off transient

10 Discussion

The NPC inverter presented in chapter 2.2 is the simplest form of a multilevel inverter. Although the spectral output can be considerably better for higher level inverters, the gain is suppressed by other factors that complicate the utilisation of such a converter. It is a combination of fabrication, control, performance and part count that makes the NPC converter favourable over other types.

Aside from these outstanding advantages the NPC inverter has some drawbacks. The neutral point potential has to be controlled actively. For most modulation schemes and under ideal conditions the DC-link capacitor voltages naturally balance over one fundamental cycle. However, semiconductors with slightly varying characteristics, different gate unit delay times, dynamic load changes, or unbalanced loads can cause a steady drift of the neutral point potential. These problems have been investigated in numerous papers, and by use of redundant switch states in developed space vector diagrams, a long term stability of the neutral point potential with no additional circuitry or switching transitions is obtained [25].

In chapter 2.4.1 some existing solutions of series connection of IGBTs are presented. It should be mentioned that manufacturers can deliver systems with these features integrated in modules ready for use. ABB has developed a solution where they series connect their press pack IGBTs and reports that switch modules are available for 10s of thousands of volts.

In Fig 4.1, a cross section of one IGBT cell is presented. It is important to notice that this representation is only one of many possible cell structures. By altering the doping profiles, P-wells and N-base region, the IGBT characteristics can be altered to fit applications where some qualities are more important than others. This point becomes evident when in chapter 6.1 and 6.2, other cell structures are presented with improved on state characteristics.

Fig 5.1 shows a standard DBC solution with soft encapsulation covering the chips. It was mentioned that one way of making the module suitable for hydrostatic pressure was to remove the gel and penetrate the housing so that the oil could cover the chips. Another possibility, not yet discussed, is to completely fill the housing with gel. To do so, it must be ensured that the housing is completely sealed so that no oil can come in contact with the gel, since the gel most likely is soluble with the oil. These modifications are less dramatic than completely removing the gel and penetrate the housing since it consists only of adding extra gel in an existing air gap with no practical function.

The test results in chapter 9 shows a number of captured scope pictures which show various graphs. By inspection of these graphs and by comparison with the theoretical waveforms in Fig 4.9 and Fig 4.10, the different sections can be recognised. The fact that the theoretical waveforms correspond with the measured ones is a good indication that the IGBT works as intended even after submerged in silicon oil. This fact is further proven by measurements in chapter 9.3, 9.4.5 and 9.4.6. When comparing the graphs from testing in air, with the ones where the module is submerged, the characteristic waveforms are the same. It should be noted that the scope had to be replaced, so close investigation of the graph must be done to see the similarity.

The temperature surveillance card was set to trip at 80 degrees in the thermal testing reported in chapter 9.3.1, but failed to do so because of lack of electrical connection with the PTC

resistor, so the test had to be manually terminated. The temperature surveillance was set to compare the PTC-resistor on the IGBT module with the adjustable reference resistance on the card, and showed ok-signal because the measured resistance was always larger. This is a weakness that should be noted and avoided by so called “fail to safe” practice.

During continuous switching test in room environment a failure occurred. After thorough inspection of the circuit and set up, it was discovered that the failure was caused by mix up of two cables. Because the initial testing was single- and double pulse tests, the failure was not detected. A signal wire had been mixed up with the power wire. With reference to the data sheet in appendix A, the Ex2 signal output had been connected to the negative DC-link output. This resulted in melting of the Ex2 output connection and the IGBT-module had to be replaced. The melted spot on the module are shown in Fig 10.1. Another IGBT-module was assembled on the heat spreader and some of the initial pulse tests were repeated. The new module worked as intended and a selection of the curves can be found in appendix F.

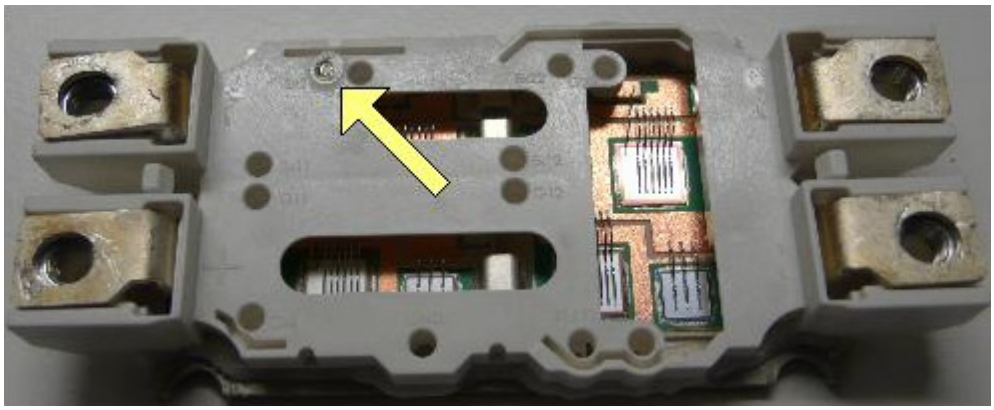

Fig 10.1 Melted spot on transistor

Losses for the test object were calculated using a reference temperature development with known effect. In chapter 9.4.1 the losses in the tank are calculated to be about 31 W, while the whole system shows a total loss of approximately 93 W. If it is assumed that the losses are equal in the two bridge legs, the total losses should add up to be about 62 W. The additional losses in the system come from voltage drops in the wires and equivalent series resistances in the capacitors which have been neglected in the calculations.

In the temperature development for intermittent operation tests it can be seen that the temperature stabilises at a lower temperature as the current pulses increase in magnitude and decrease in width to hold the same rms value of the current. Explanation for this lies in the duration of the pulses which are shorter with higher amplitude, combined with effective cooling. With longer off-periods the convective cooling effectively removes the heat to the periphery of the tank where it is accumulated by the room environment.

Loss calculations for the intermittent operation tests are not made because the temperature curve shows that the measure points is not synchronised with the current pulses. That is one of the reasons for the irregularities in the graph. Another is the induced circulation of the oil for each pulse which causes a disturbed flow pattern and locally fluctuating temperatures. From the curves it can be seen that despite these disturbing elements the development trend is fully captured. Losses could be calculated, but since it is not the essential part of the experiment it is skipped in this section.

When initiating 40A intermittent operation, the short circuit protection was trigged to stop the switching. The short circuit protection is set to monitor the voltage drop over the transistor. If the voltage drop is above a pre adjusted level, the OK signal will go low to protect destruction of device. The reason for short circuit detection was found when closely investigating the behaviour during double pulse tests. The graphs are shown in appendix G, and it became evident that the high current caused a voltage drop in the thin wires for the upper transistor, B+, which shares power and signal wire. To cope with the problem, the gate driver card was modified to trip at a higher voltage level by putting another resistance in parallel with the existing one. A 3.3 kohm resistor was used in parallel with the existing 1.8 kohm. This altered the level from about 2.8 V to about 3.5 V.

The last continuous switching test in chapter 9.4.6 is referred to as a long term test. In a sub sea application, long term would probably be at least longer than 5 years, and maybe up to 10 or 20, but obviously this can not be investigated within the time frame of this thesis. Long term in this manner means more than a few days.

The practical experiment does not include any advanced and accurate calculations but rather estimates and sometimes even rough estimates. It was not the goal to finely investigate certain details and aspects around the components. The components and set up are well known and tested many times before for performance and reported in numerous papers. The interesting aspect of the experimental set up is the compatibility with the new environment.

11 Concluding remarks

A suitable converter topology for a sub sea compression application will be a diode bridge based rectifier and a neutral point clamped inverter. Such a system will ensure good spectral input to the compressor's motor terminals with good control and acceptable disturbances in the rest of the electrical network. For high voltage applications, a neutral point clamped inverter with series connection of switches can be used since the switches then share the voltage. To obtain simultaneous switching, or to protect the devices from overvoltages, special measures must be taken. Paralleled capacitors or intelligent control can achieve safe and reliable operation.

Semiconductor switches in the converter will most probably be the insulated gate bipolar transistor. This device has proven to be both reliable with good performance and suitable for high switching frequency with low losses. A number of elements in the cell structure of the IGBT can be altered to change operating characteristics. The device can be optimised to fit certain applications and working environments. Examples would be the enhanced planar technology and the soft punch through features that can be obtained by modifying the doping profiles in the cell structure. Other examples are the packaging technology with different forms of press pack and the traditional DBC solution. Manufacturers constantly improve both performance and packaging technology through the introduction of new devices to meet the new demands that constantly arises.

One of these demands is operation related to the oil and gas industry in new environments like on the seabed where the pressure is high and availability is low. A suggested solution is to encapsulate the power electronics in a tank with flexible walls and fill it with insulating oil. The flexible walls will allow the pressure to be the same on the inside as on the outside. The components will then be under high hydrostatic pressure, which is not one of the normal design criteria when developing devices.

The experiments in this report shows that the materials used in a standard DBC IGBT module is compatible with silicon oil with no change of characteristics from air environment to fully submerged in silicon oil when operated with continuously switching.. The module was left submerged in the oil for approximately 1 month with varying temperatures from 25 °C to 65 °C. By a brief visual inspection, it looks like the module survived without any noticeable changes.

The tests show that no instant change will occur when submerging the Semix transistor in oil. The conclusion is that it looks promising for further testing, and that the initial obstacle of compatibility is solved. It is still a lot of work left to fully conclude that IGBT modules can be operated submerged in insulating oil, but all in all the work presented in this report shows promising results.

12 Further work

Before deciding the final solution it would be necessary to investigate other aspects as well. Economically it is of great importance if the need for a complete new solution with pressurised electronics is necessary. It could be that it is not beneficial to develop such a system with regards to saved costs versus reliability.

Technically, it should be investigated more on what kinds of modules are available at this point, and what is expected to become available within the nearest future. To do this, a close cooperation with some of the leading manufacturers of power electronic components must be started.

Since the scope of the experiment was a little bit amputated and no pressure was applied, a natural step would be to get the pressure system up and running, and then apply pressure on the IGBT module. A suggested pressure system is briefly introduced for this purpose, and could be used as a basis.

With the pressure system it would be natural to pressure test other components as well. If the control circuitry is to be submerged and pressurised, it must be investigated that signal level components also are able to function under high hydrostatic pressure. Designing new gate drivers and surveillance cards with this in mind would be an important step on the way to a final system.

Capacitors are extremely important in electrical drive systems, and must also be tested for high hydrostatic pressure. The manufacturing techniques and design of these components must be thoroughly investigated to reveal if there are any possibilities for instant failures.

A long term test with continuous switching for several months must also be carried out along with power cycling and thermal cycling. The wiring in the experimental set up should be changed so that components can be operated with rated values.

The pressure tank available is not certified for pressure and when ordering a new tank it should be taken into consideration that larger modules and components must be tested as well. A new module ready for testing is the injection enhanced gate transistor shown in Fig 6.8. Large capacitors in the capacitor bank must fit inside the tank and finally a complete converter configuration with control electronics and thermal management system must be pressurised.

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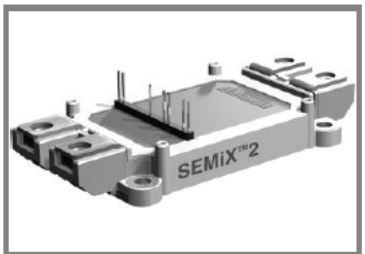
Appendix

Appendix A

SEMiX 202GB128D



SEMiX® 2

SPT IGBT Modules

SEMiX 202GB128D

Preliminary Data

Features

- Homogeneous Si
- SPT = Soft-Punch-Through technology
- $V_{CE(sat)}$ with positive temperature coefficient
- High short circuit capability

Typical Applications

- AC inverter drives
- UPS
- Electronic welders up to 20 kHz

Remarks

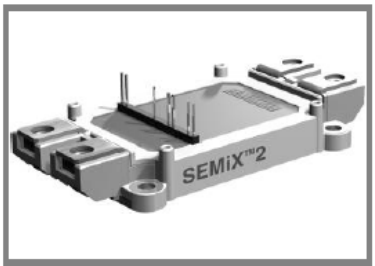
- Not for new design

Absolute Maximum Ratings			T_{case} = 25°C, unless otherwise specified	
Symbol	**Conditions**		**Values**	**Units**
IGBT				
V_{CES}	T_j = 25 °C		1200	V
I_C	T_j = 150 °C	T_{case} = 25 °C	190	A
		T_{case} = 80 °C	135	A
I_{CRM}	I_{CRM}=2xI_{Cnom}		200	A
V_{GES}			±20	V
t_{psc}	V_{CC} = 600 V; $V_{GE} \leq$ 20 V; V_{CES} < 1200 V	T_j = 125 °C	10	µs
Inverse Diode				
I_F	T_j = 150 °C	T_{case} = 25 °C	150	A
		T_{case} = 80 °C	100	A
I_{FRM}	I_{FRM}=2xI_{Fnom}		200	A
I_{FSM}	t_p = 10 ms; sin.	T_j = 25 °C	1000	A
Module				
$I_{t(RMS)}$			600	A
T_{vj}			-40 ... + 150	°C
T_{stg}			-40 ... + 125	°C
V_{isol}	AC, 1 min.		4000	V

Characteristics			T_{case} = 25°C, unless otherwise specified			
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Units**
IGBT						
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 4 mA		4,5	5	6,5	V
I_{CES}	V_{GE} = 0 V, V_{CE} = V_{CES}	T_j = 25 °C			0,3	mA
V_{CE0}		T_j = 25 °C		1	1,15	V
		T_j = 125 °C		0,9	1,05	V
r_{CE}	V_{GE} = 15 V	T_j = 25°C		9	12	mΩ
		T_j = 125°C		12	15	mΩ
$V_{CE(sat)}$	I_{Cnom} = 100 A, V_{GE} = 15 V	T_j = 25°C$_{chiplev.}$		1,9	2,35	V
		T_j = 125°C$_{chiplev.}$		2,1	2,55	V
C_{ies}	V_{CE} = 25, V_{GE} = 0 V	f = 1 MHz		8		nF
C_{oes}				1,5		nF
C_{res}				1		nF
Q_G	V_{GE} = -8 V ... +15 V			960		nC
$t_{d(on)}$	R_{Gon} = 6,8 Ω	V_{CC} = 600V		85		ns
t_r		I_{Cnom} = 100A		50		ns
E_{on}		T_j = 125 °C		11		mJ
$t_{d(off)}$	R_{Goff} = 6,8 Ω			430		ns
t_f				55		ns
E_{ff}				8		mJ
$R_{th(j-c)}$	per IGBT				0,165	K/W

GB

SEMiX 202GB128D



SEMiX® 2

SPT IGBT Modules

SEMiX 202GB128D

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- Homogeneous Si
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- UPS
- Electronic welders up to 20 kHz

Remarks

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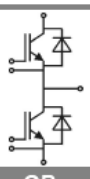

GB

Characteristics

Symbol	Conditions		min.	typ.	max.	Units
Inverse Diode						
$V_F = V_{EC}$	I_{Fnom} = 100 A; V_{GE} = 0 V	T_j = 25 °C$_{chiplev.}$		2	2,5	V
		T_j = 125 °C$_{chiplev.}$		1,8	2,3	V
V_{F0}		T_j = 25 °C		1,1	1,2	V
		T_j = 125 °C				V
r_F		T_j = 25 °C		9	13	mΩ
		T_j = 125 °C				mΩ
I_{RRM}	I_{Fnom} = 100 A	T_j = 125 °C		130		A
Q_{rr}	di/dt = 3550 A/µs			16		µC
E_{rr}	V_{GE} = -15 V; V_{CC} = 600 V			6		mJ
$R_{th(j-c)D}$	per diode				0,3	K/W
Module						
L_{CE}				18		nH
$R_{CC'+EE'}$	res., terminal-chip	T_{case}= 25 °C		0,7		mΩ
		T_{case}= 125 °C		1		mΩ
$R_{th(c-s)}$	per module			0,045		K/W
M_s	to heat sink (M5)		3		5	Nm
M_t	to terminals (M6)		2,5		5	Nm
w				289	250	g
Temperature sensor						
R_{100}	T_c=100°C (R_{25}=5 kΩ)			0,493±5%		kΩ
$B_{100/125}$	$R(T)=R_{100}\exp[B_{100/125}(1/T-1/T_{100})]$; T[K]; B			3550±2%		K

This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.

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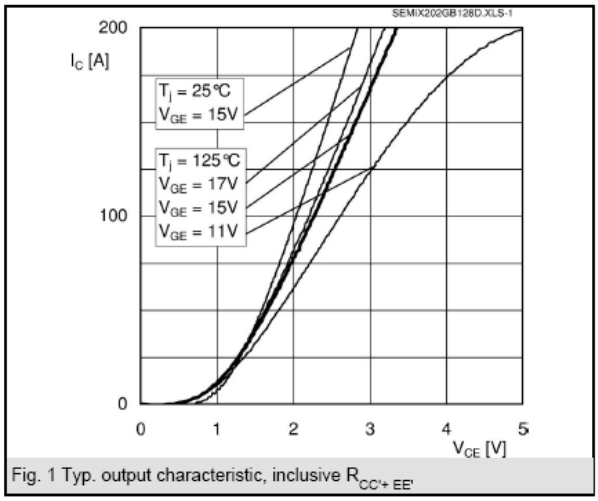

Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

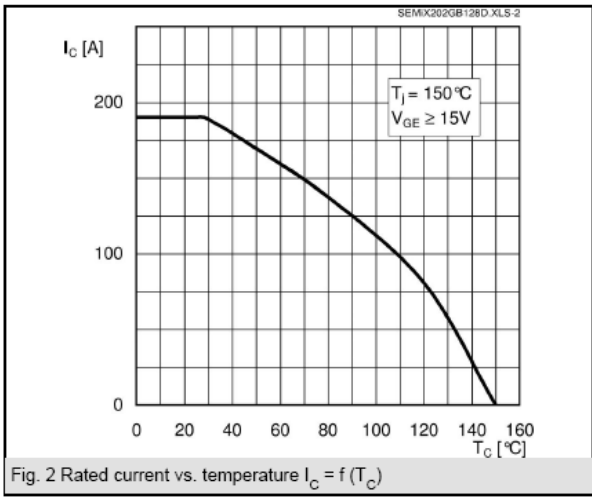

Fig. 2 Rated current vs. temperature $I_C = f(T_C)$

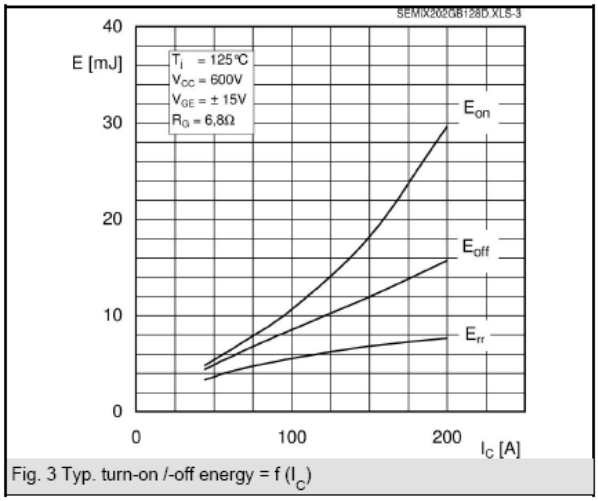

Fig. 3 Typ. turn-on /-off energy = f (I_C)

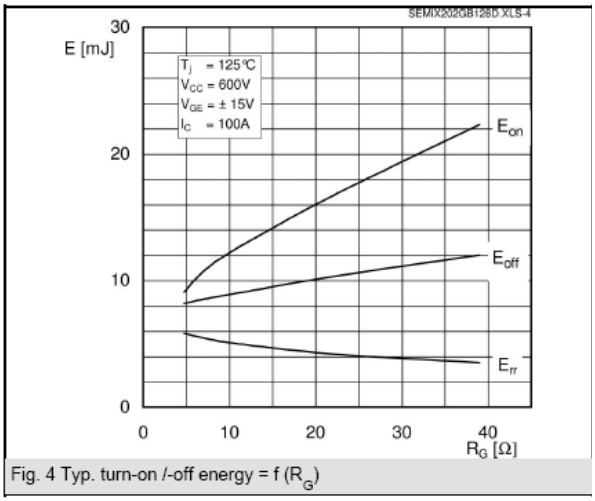

Fig. 4 Typ. turn-on /-off energy = f (R_G)

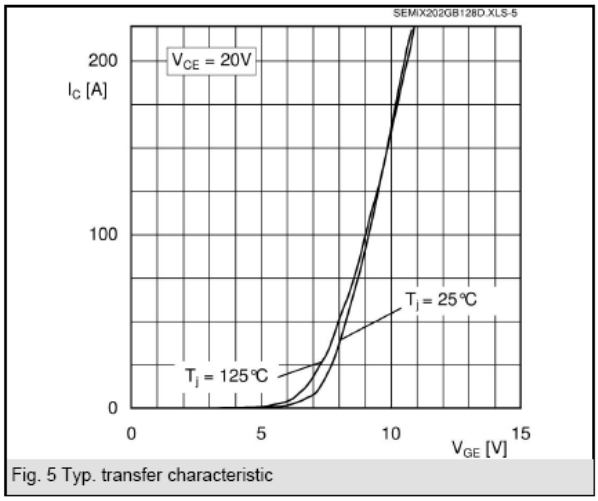

Fig. 5 Typ. transfer characteristic

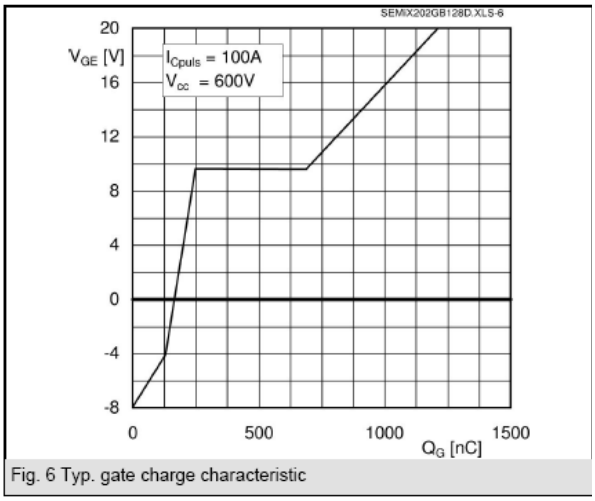

Fig. 6 Typ. gate charge characteristic

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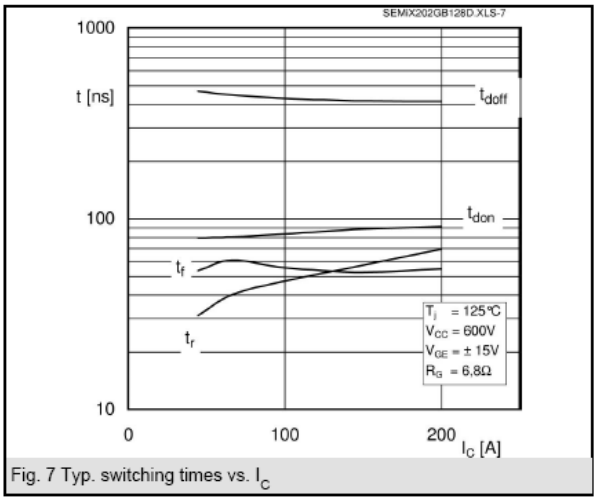

Fig. 7 Typ. switching times vs. I_C

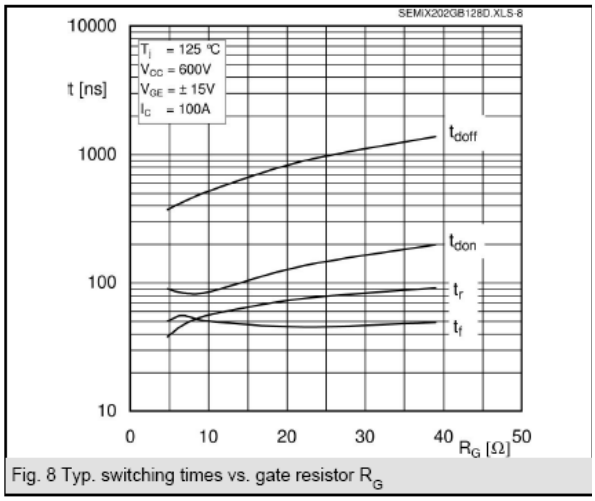

Fig. 8 Typ. switching times vs. gate resistor R_G

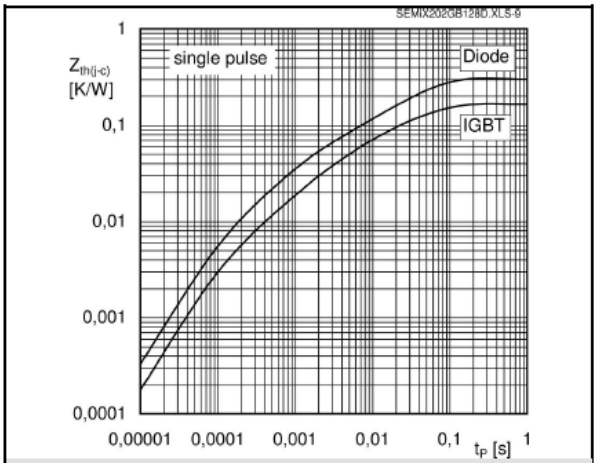

Fig. 9 Typ. transient thermal impedance

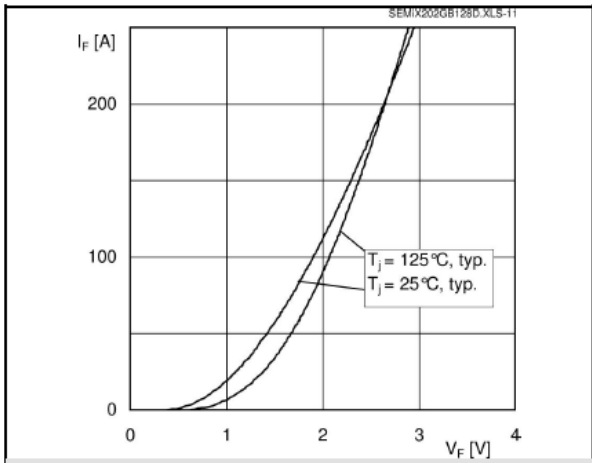

Fig. 10 Typ. CAL diode forward charact., incl. $R_{CC'+EE'}$

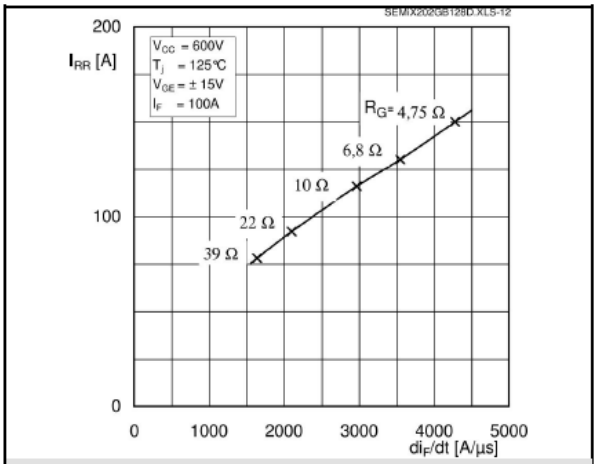

Fig. 11 Typ. CAL diode peak reverse recovery current

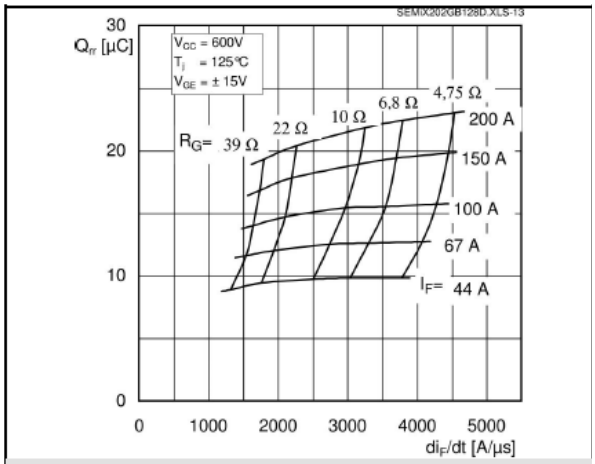

Fig. 12 Typ. CAL diode recovery charge

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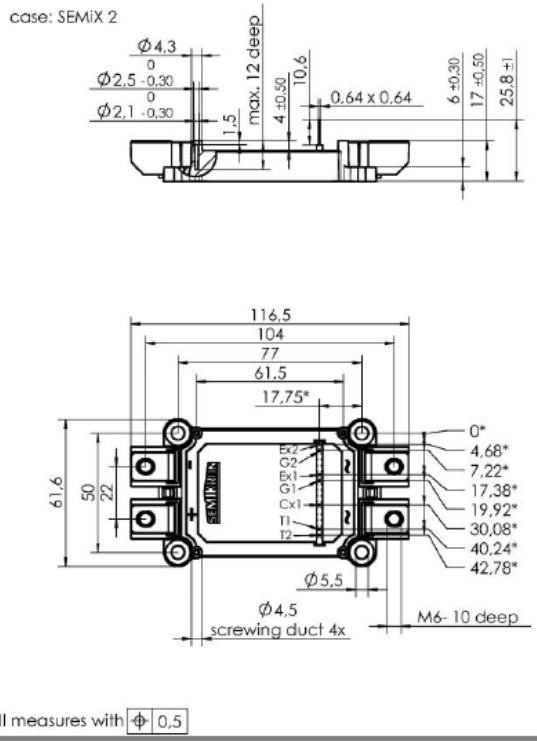
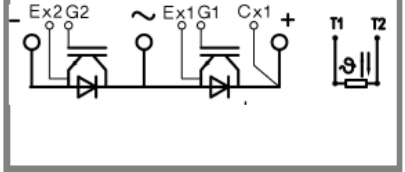
UL Recognized
File no. E 63 532

Dimensions in mm

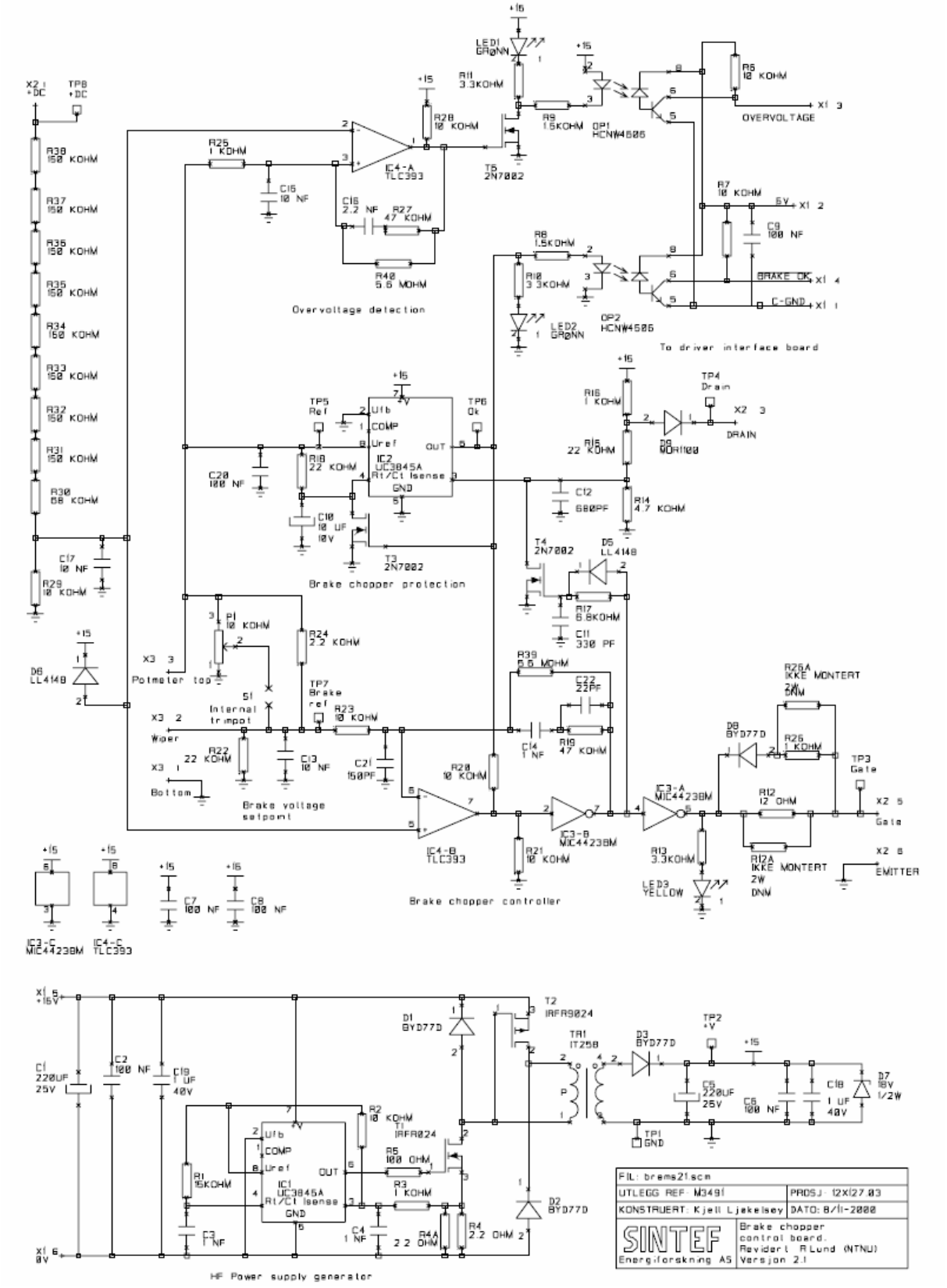


Case SEMiX 2s



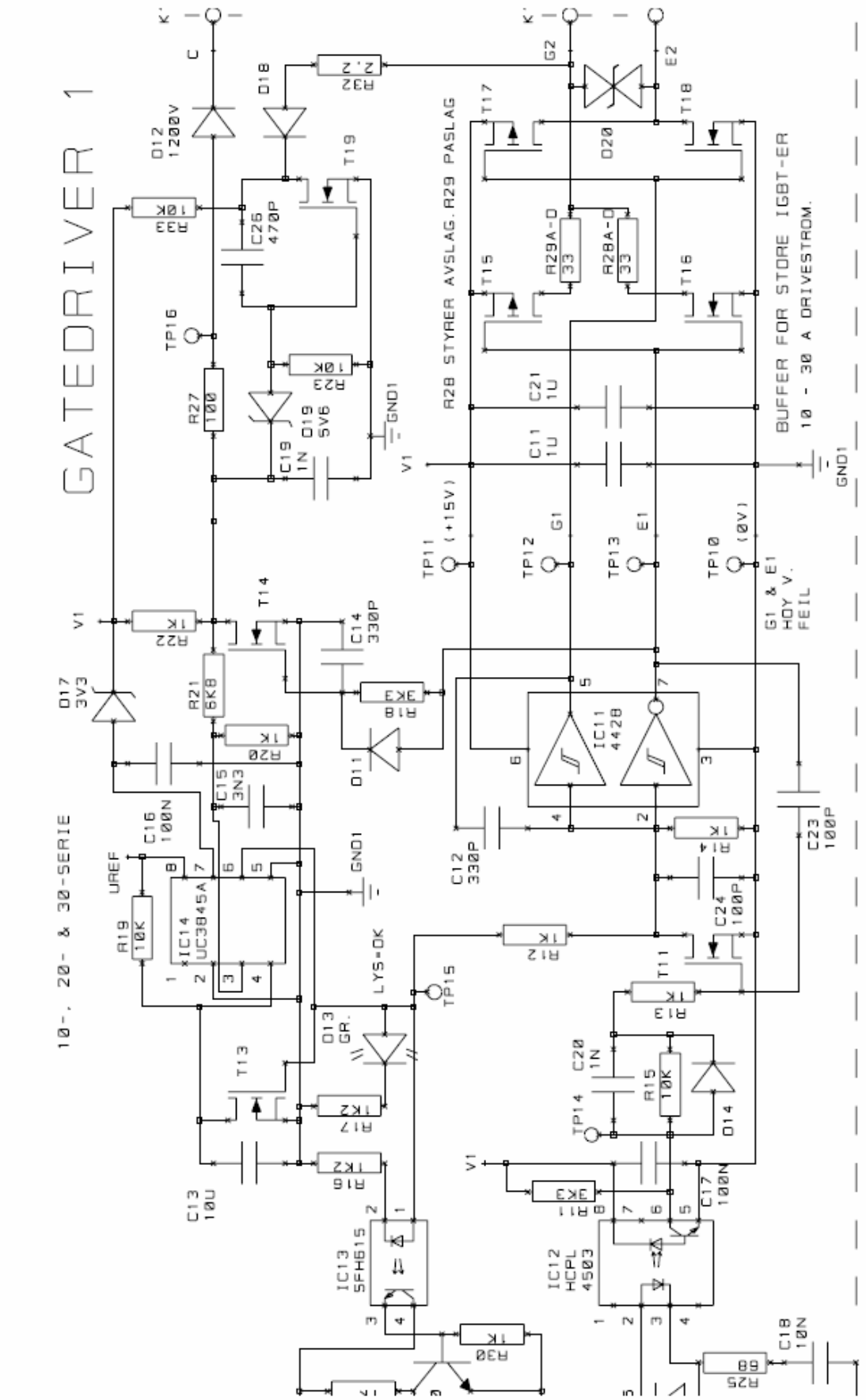
Pinout GD

Appendix B



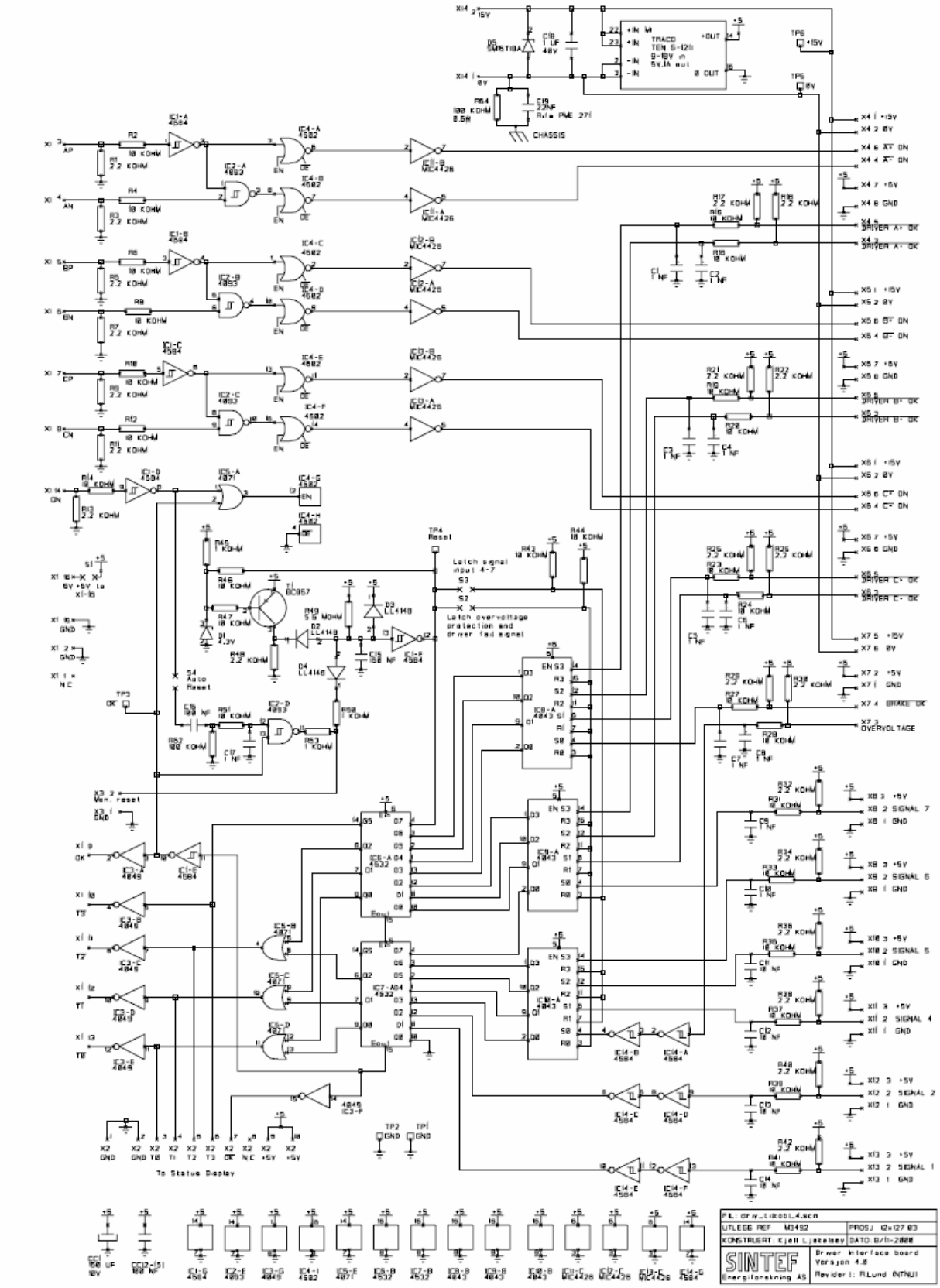
Appendix fig 1 Brake chopper control board

Appendix C



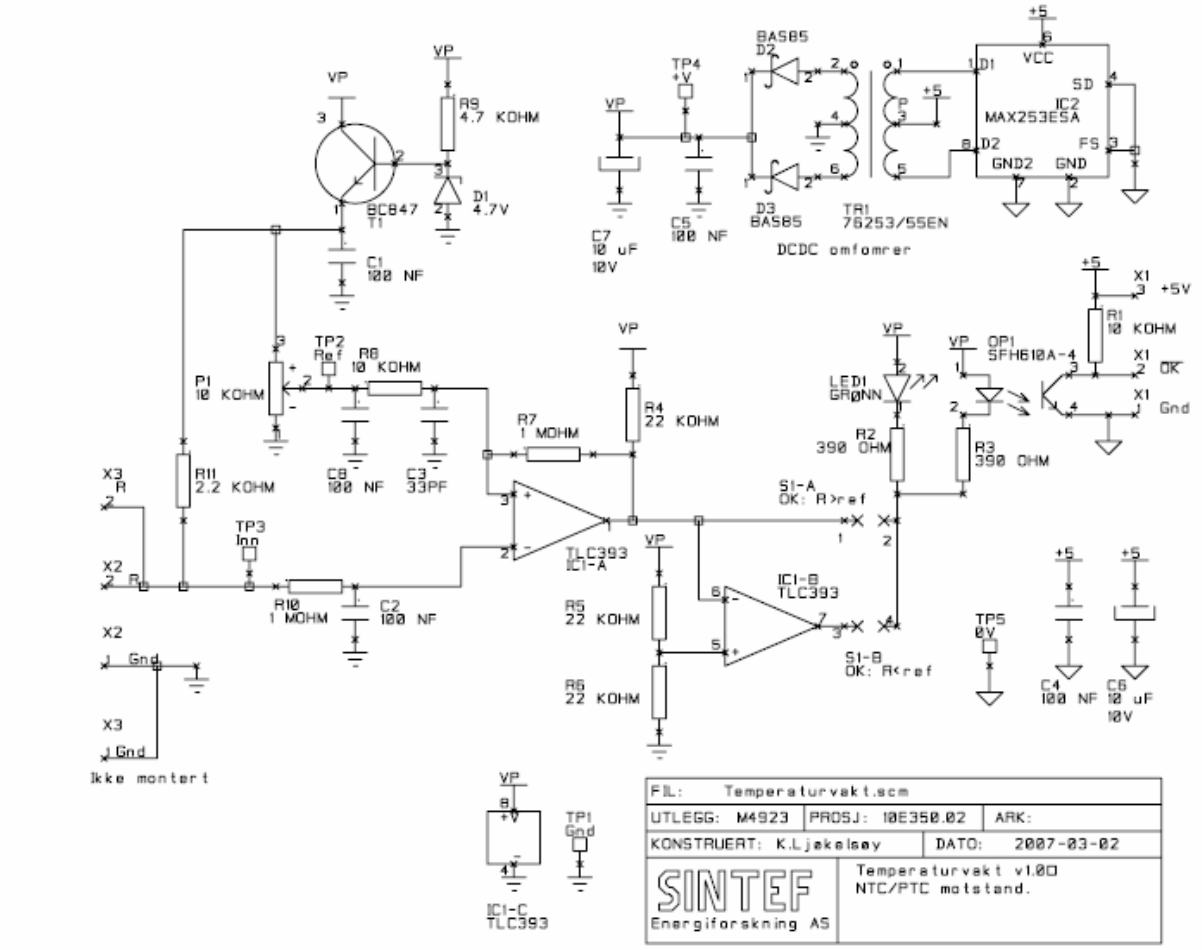
Appendix fig 2 Gate driver

Appendix D



Appendix fig 3 Gate driver interface board

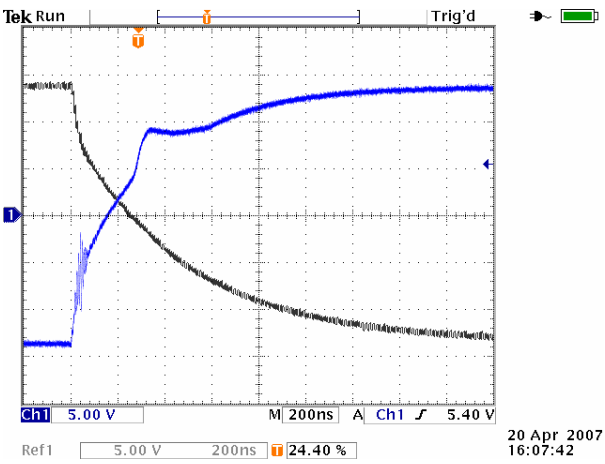
Appendix E

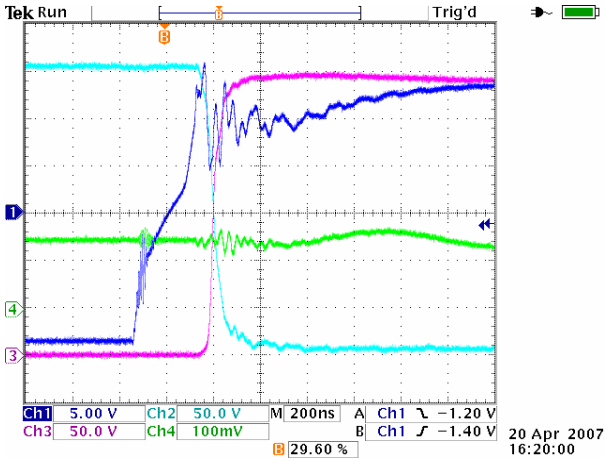


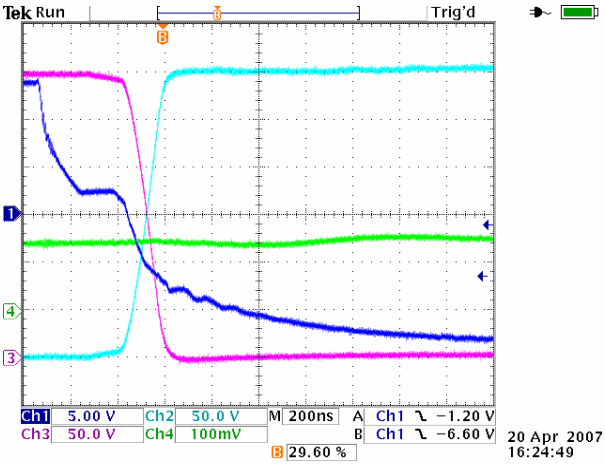
Appendix fig 4 Temperature card

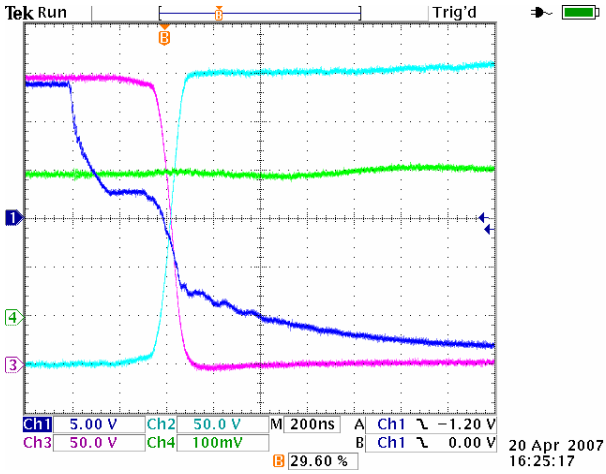
Appendix F

Scope channels as described in chapter 9.



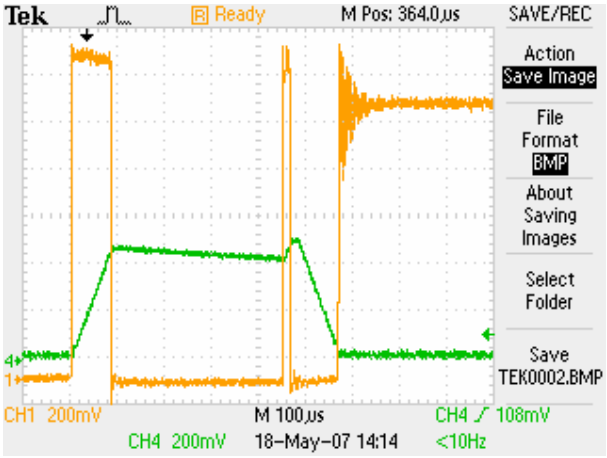


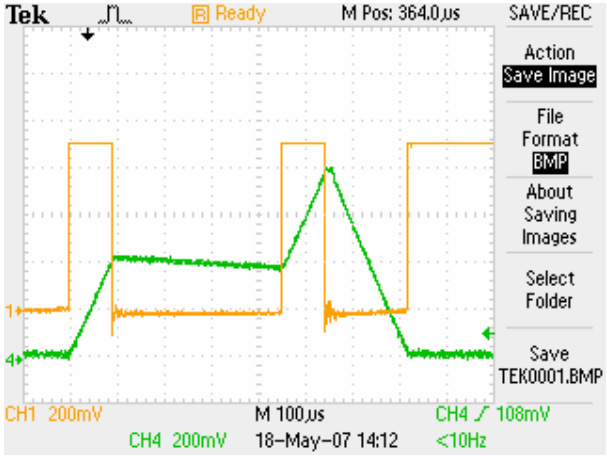


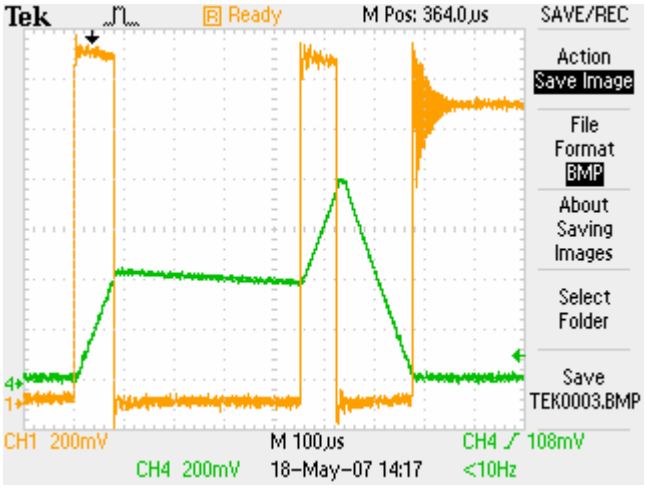


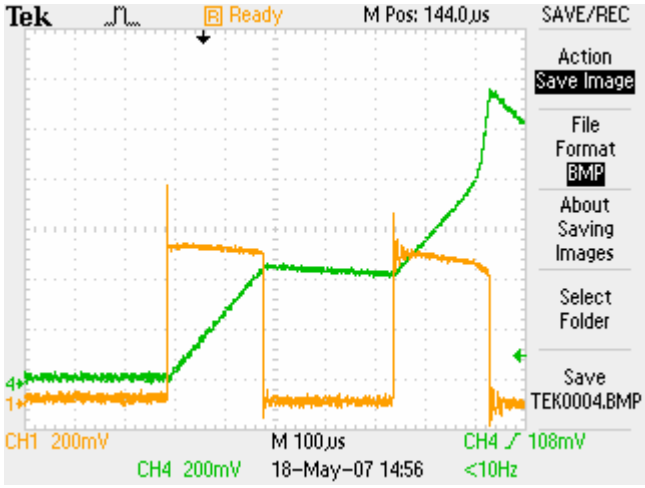
Appendix fig 5 Selection of curves for new module

Appendix G



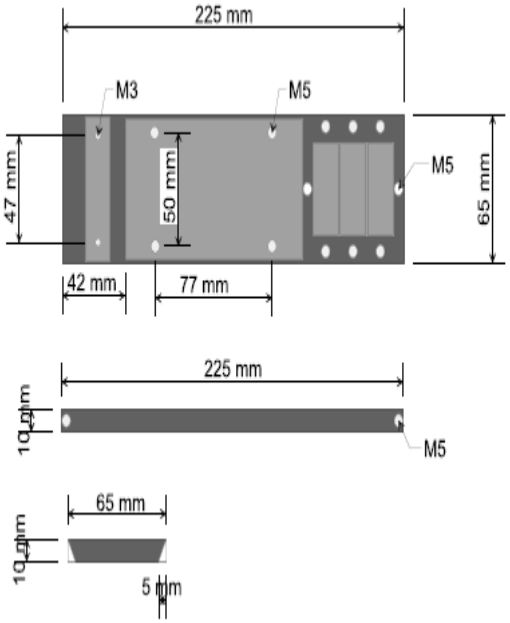






Appendix fig 6 Curves showing short circuit detection

Appendix H



Appendix fig 7 Heat spreader physical layout