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An investigation on gridconnectable single phase photovoltaic inverters

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Master of Science in Energy and Environment
Submission date: January 2010
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Problem Description

This thesis explores various photovoltaic (PV) inverter topologies and switching schemes for identifying a good 500 W single phase inverter design scheme suitable for supplying power to 230 V, 50 Hz grids. A good inverter is considered to have low total harmonics distortion (THD) output, high efficiency and low cost. Islanding considerations are not investigated.

An understanding of both practical limitations and regulated demands for the PV inverter shall be reached. Various inverter topologies shall be identified and understood through a literature study.

Based on the above investigations, selected inverter topologies shall be computer simulated to further investigate their performance. Focus is on efficiency and THD with changing output power and input voltage, which are normal phenomena for a PV inverter. One of these inverter topologies will then be further studied with different switches, in order to find which switch parameters are important for the given topology.

Based on these investigations, the promising inverter topology will be tested in the laboratory for verifying the simulated results with the actual laboratory measurements.

Based on the above simulations and the laboratory measurements a conclusion will be drawn about the most suitable topology for the above given specification goals.

Finally some ideas on further work in order to make the chosen inverter design scheme better will be presented.

Specification: The laboratory work was, in agreement with the supervisor, cancelled. Tests were supposed to be done on an already commercially available inverter, but the order did not reach NTNU in time. By the time we realised that the order would not be here in time, it was too little time left until the deadline for us to start thinking about building an inverter from scratch.

Assignment given: 18. August 2009
Supervisor: Tore Marvin Undeland, ELKRAFT

Acknowledgements

With this report I deliver my efforts of obtaining the master's degree in electrical power engineering at Norges Teknisk-Naturvitenskaplige Universitet (the Norwegian University of Science and Technology, NTNU), which is hopefully written in an understandable form of British English.

But the report would not be here without the help of others.

Firstly I wish to thank my supervisor Tore Marvin Undeland and his Doctor of Philosophy student Sverre Gjerde, both have been the main source of answers for my questions related to the assignment.

Secondly I wish to thank my fellow students at our office – Sveinung Floten, Tor Stian Haug and Behrooz Moghimian – for both their technical insight and help, but also for the good social environment which was created at the office.

Then a thank goes to Supratim Basu who helped me a lot on the construction of a good structure on my thesis. May his arm recover well from that all too unfortunate meeting with the Norwegian icy surface.

Arkadiusz Kulka and Kjetil Boysen, both at Eltek Valere, also deserve a thank with their guiding and help underways.

For helping me with the preliminary laboratory setup a great thank goes to Bård Almås and Vladimir Klubicka at the institute's service lab. It was unfortunate that the laboratory equipment did not arrive on time from Dutch manufacturer, so that the actual laboratory work was never done.

6.1.2010

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Summary (Norsk)

Flere vekselrettertopologier til omforming av kraft fra fotovoltaiske moduler som kan brukes av legfolk ble undersøkt i lys av både nasjonale og internasjonale krav, samt praktiske utfordringer. En god vekselrettertopologi burde også ha lav kostnad, høy virkningsgrad og god kvalitet på utgangskraften. I tillegg ble det sett på flere filtermuligheter, og man kom fram til at det såkalte LCL-filteret var best, fordi det dempet de uønskede frekvensene mest med relativt små kondensator- og spoleverdier.

Fem forskjellige vekselrettertopologier ble deretter presentert og utforsket: En hybrid flernivåsvekselretter, en helbru, en serieresonans buck-boost vekselretter, en sperreomformer med utfoldelseshelbru og en serieresonansomformer med utfoldelseshelbru.

Etter utforskning ble to av vekselrettertopologiene, fullbrua og den hybride flernivås-vekselretteren antatt bedre enn de andre til de oppgitte formål og krav. Disse ble dermed nærmere analysert ved hjelp av datasimularingsprogrammene SIMULINK og SPICE for å finne kvantitative argumenter for hvilken topologi som var best under de ovenfornevnte forhold. I tillegg ble filterparameterne til et foreløpig filter tallfestet.

Ut ifra dette ble det funnet ut hvilken av vekselrettertopologiene som under ellers like vilkår, var best. Da ble det funnet at den hybride flernivåsvekselretteren var mellom 0.5 til 1 prosentpoeng mer effektiv enn helbrua, samtidig var totalklirrfaktoren dens vesentlig bedre, da den va mellom fem og ti ganger bedre enn helbruas totalklirrfaktor. Dette tilsier at den hybride flernivåsvekselretteren kan ha vesentlig lavere filterparametre enn helbrua, og følgelig ha et billigere filter. Disse to faktorene gjorde at den hybride flernivåsvekselretteren ble ansett som den bedre topologien av de to, og denne ble valgt for videre tester.

Den siste simulasjonen gikk ut på å finne gode svitsjer til å utstyre den valgte hybride flernivåsvekselretteren. Her ble det funnet at for lavspenningsbrua var det mer av-

gjørende med raske svitsjer, mens for høyspenningsbrua var det viktigere med svitsjer som hadde liten elektrisk motstand når da var i på-modus. De valgte svitsjene var STY60NK30Z for høyspenningsbrua og BSC520N15NS3 G for lavspenningsbrua.

I tillegg var det meninga å utføre laboratoriumsforsøk med en valgt vekselretter-topologi, men grunnet forsinkelse i leveransene kom dessverre ikke testobjektet til rett tid, og denne delen kunne ikke utføres.

Summary (English)

Several inverter topologies for use with power conditioning of photovoltaic modules were investigated with both national and international requirements in mind, as well as also practical challenges and the ability to be user friendly for ordinary people. A good inverter topology should also be low cost, have a high efficiency and have a good output power quality. In addition several filter possibilities was investigated, and it was concluded that the LCL-filter was the best for the given conditions, since it attenuated the unwanted frequencies the best with relative small filter parameters.

Five different inverter topologies was then presented and investigated: A hybrid multilevel inverter, a full bridge inverter, a series resonant buck-boost inverter, a flyback converter with unfolding H-bridge inverter and a series resonant converter with unfolding H-bridge inverter.

After an investigation of the above mentioned criteria, two of the inverter topologies, the H-bridge inverter and the hybrid multilevel inverter, were considered better than the rest for the given requirements and purposes. These were then closer analysed with the computer simulation programs SIMULINK and SPICE in order to find quantitative arguments about which topology was the best under the above mentioned conditions. Filter parameters were also quantified.

From this it was found that the hybrid multilevel inverter was 0.5 to 1 percent point more effective than the H-bridge, at the same time the total harmonic distortion was significantly better, approximately five to ten times better than the H-bridge inverter's total harmonic distortion. This means that the hybrid multilevel inverter may have a considerably cheaper filter. Both of these factors contributed so that the hybrid multilevel inverter was regarded the better topology and this topology was selected for further tests.

The last simulation was about finding good switches to equip the hybrid multilevel inverter with. Here it was found that the decisive factor for the low voltage bridge was quick switches, whereas for the high voltage bridge it was more important to have switches with low resistance when turned on. The chosen switches were STY60NK30Z and BSC520N15NS3 G for the low voltage bridge.
In addition it was meant to perform a laboratory experiment with the selected topology, but because of a delay with the deliverance, the test object did not arrive at time, so the experiment could not be done.

1 Introduction

The sun's radiation is the most energy rich power source on earth, yet almost none of the energy is directly harnessed by mankind. In order to harness more of the sun's energy, more photovoltaic (PV) modules should be connected to grid. To assure a high quality input to the grid, a good electrical power inverter is needed. The inverter should also be designed in a way that makes it possible for the average Joe and Jane to use it without any trouble. Meaning it should be safe and simple to install and use, as well as being low cost and with little or no maintenance.

This master thesis aims to investigate single phase grid connectable inverters topologies that are powered by photovoltaic (PV) cells to be used by ordinary people. It is written at the Department of Electric power engineering at Norges Teknisk-Naturvitenskaplige Universitet (NTNU) in cooperation with Eltek Valere.

Chapter 2 shows a survey over already commercially available inverters. These represent the present class of inverters and show interesting features regarding output quality, size and simplicity.

Chapter 3 gives an introduction to photovoltaic systems and the power inverters needed to connect them to a power grid, as well requirements for the grid connection itself. This chapter also addresses the different ways of filtering the output signal and finally the possibility of storing the electric energy before it is inverted.

Chapter 4 describes several inverter topologies available and to be evaluated in this thesis. The selection is divided into isolated and non-isolated topologies. It also gives a brief introduction to some available and interesting semiconductors, and the limitations of the life time caused by the capacitors in use. Based on the above, some of the topologies are selected for further investigation.

Chapter 5 introduces the modelling tool and then the models of the selected inverters, as well as a simple driver unit. Then the programme is to be optimized for the individual topologies and tests. After some comparisons between the inverters, one of them is selected for a more thorough investigation, in which suitable switches and filter elements are found. At the end a complete system will be finished.

Chapter 7 and *chapter 8* discusses and concludes the work that has so far been done. It ends with suggesting further work which the author means would be useful for the next generation of single phase grid connectable PV inverters.

2 Survey of present inverters

Designing inverters for use with PV modules is not a new phenomenon, there already exists quite a lot of manufactures focusing on these applications. Studying their solutions is essential to get an understanding of how good a new inverter must be, in order to succeed on the world marked.

This chapter presents some already commercially available inverters and some of their specification. Ranging from the Soladin 600 (Section 2.1), the UniLynx 1800 (Section 2.2), the Fronius IG 15 (Section 2.3), Stecia Grid 500 (Section 2.4) and Sunny boy (Section 2.5). All of the inverters work on the standard European power grid with an output voltage of 230 V and 50 Hz.

2.1 Soladin 600

The Soladin 600 is a grid connectable single phase PV inverter manufactured by the Dutch company Mastervolt, their model may be seen in Figure 2-1.

Figure 2-1: The Soladin 600, a 600 W single phase grid connectable PV inverter by Mastervolt. Photo: http://www.mastervolt.com

This inverter offers a net plug for a simple and unproblematic connection to the grid. With its only 2 kg and a rated output power of 535 W, which is a very good power per weight rating. It requires an input voltage of 40 – 125 V to operate, and has an

efficiency of 93 %. It has a high frequency transformer, which offers galvanic insulation at a low weight. Harmonics are compliant to EN 61000-3-2 – European standard.

2.2 UniLynx 1800

The UniLynx 1800 is a grid connectable single phase PV inverter manufactured by the Danish company Danfoss, their model may be seen in Figure 2-2.

Figure 2-2: The Unilynx 1800, a single phase grid connectable PV inverter by Danfoss. Photo: http://www.danfoss.com

This model offers easy to use connection to the grid and PV converter. The inverter also has the option of either an outdoor or an indoor inverter, with a weight of 16 kg and 14 kg respectively. Given the rated output power of 1650 W, this is a much lower power per weight ratio than the Soladin. The input voltage may vary between 125 V and 450 V, which means that it requires more or larger solar panels than the Soladin to be able to operate. The maximum efficiency is reported to be 93.70 %. A transformer gives galvanic isolation, but it is placed on the low frequency side of the inverter, meaning it has to weigh more than the Soladin equivalent. Harmonics are compliant to EN 61000-3-2.

2.3 Fronius IG 15

The Fronius IG 15 is a grid connectable single phase PV inverter manufactured by the Austrian company Fronius International, their model may be seen in Figure 2-3.

Figure 2-3: The Fronius IG 15, a single phase grid connectable PV inverter by Fronius. Photo: http://www.fronius.com

With its 9 kg rated power input of 1300 W the power to weight ratio lies between the previous inverter types. The input voltage may range in between 150 V and 400 V, narrower than the UniLynx. The maximum efficiency is 94.2 %, which is the highest among the inverters with transformer. A high frequency (HF) transformer offers galvanic isolation. The distortion factor is impressively lower than 3.5 %.

2.4 Steca Grid 500

The Stecia Grid 500 is a grid connectable single phase PV inverter manufactured by the German company Stecasolar, a

Figure 2-4: The Steca Grid 500, a single phase grid connectable PV inverter by Stecasolar. Photo: www.stecasolar.com

This inverter only weighs 1.4 kg and has is rated 500 W, which yields the highest power to weight ratio of them all. This comes as the cost of no transformer, and which again explains the good maximum efficiency of 95.8 %, which makes it the most efficient inverter in this class. The input voltage may vary between 75 V and 170 V. The distortion factor is no more than 5 %, any compliance with a standard is not stated.

2.5 Sunny boy 1100

The Sunny boy 1100 is a grid connectable single phase PV inverter manufactured by the German company SMA.

Figure 2-5: The Sunny boy, a single phase grid connectable PV inverter by SMA. Photo: www.sma.de

Weighing 22 kg and a rated output power of 1000 W, it has a rather low power to weight ratio. The high weight probably comes from the low frequency transformer. It has a very wide input voltage range of 139 V to 320 V and a maximal efficiency of 93 %. Nothing is stated about the harmonics.

3 Overview over photo voltaic systems and converters

There is a large and growing interest in carbon free or "green" energy, giving momentum to the development of renewable energy sources. And as the general need for energy along with the energy prices continue to increase, the use of PV cells is beginning to take off, and not without reason: With an average solar radiation on earth calculated to be 342 W/m^2 [1] the sun itself is a mighty potent renewable energy source.

Of course the actual power output of a PV module will never be so high, but simply the idea of having the energy delivered on to the energy converter is an appealing thought compared to the expensive investments need to drill out oil from an oil field. In addition the PV modules are almost completely safe, unlike the contents of for example a nuclear reactor or a coal power plant. Finally they are easy to maintain, since most of the maintenance simply consists of cleaning the panel from dirt.

The cost per peak power is still rather high for PVs. In addition the output power is DC, which cannot be neither directly connected to the power grid nor used by most normal electrical devises. Subsequently the voltage needs to be converted into a 230 V and 50 Hz sinusoidal output before it can be connected to a grid.

An old way of doing this power conversion, is to connect a DC motor and a AC to each other and then let the DC motor work in motor mode, while the AC motor generates energy. This crude way of converting power produces a nice sinusoidal waveform, but has the downside that it also produces a lot of losses, especially for such small systems which PV power plants normally are.

Therefore we now normally invert the power using electrical power converters, which then acts as a grid interface. This chapter provides the current standards regarding the

grid connection of distributed energy sources. Then a PV module's characteristics will be reviewed, before the discussing converter topologies and their needed filtering. The possibility of storing the energy in a battery before reaching the grid will also be on the agenda.

3.1 Grid connected standards

Any designer of a grid connectable inverter needs to be aware of the current standards and regulations which apply in the inverter's target country. Here two common standards will be looked into, namely

- *International Electrotechnical Commission* – IEC
- *Institute of Electrical and Electronics Engineers* – IEEE

The topical standards herein are IEC 61727 [2] and IEEE Std. 1547 [3].Where the former deals with PV systems and the latter with distributed resources in general. These two standards may give us a basic understanding of the demands and limitations for the inverter designs. In addition IEEE STD 929-2000 [4] offers guidelines especially meant for PV installation, which we will also give some attention.

3.1.1 Requirements for the inverter

This thesis will now review some important inverter requirements which shall be followed when designing a new PV inverter according to the international standards discussed above, and which are mandatory in many countries.

Grounding

The negative pole of a PV panel should have the possibility of being grounded without causing safety problems.

Anti-Islanding

Both IEC and IEEE give a definition of what islanding is:

- IEC 61727: *A utility distribution system is islanded when It is out of the normal operation specifications for voltage and/or frequency. When this situation occurs, the PV system must cease to energize the utility within 2 s of loss of utility.*
- IEEE 929-2000 (definition of non-islanding inverter): *An inverter will cease to energize the utility line in ten cycles or less when subjected to a typical islanded load in which either of the following is true:*
    - *There is at least a 50 % mismatch in real power load to inverter output (that is, real power load is <50% or >150% of inverter power output).*
    - *The islanded-load power factor is <0.95 (lead or lag)*

  If the real-power-generation-to-load match is within 50% and the islanded-load power factor is >0.95, then a non-islanding inverter will cease to energize the utility line within 2 s whenever the connected line has a quality factor of 2.5 or less

The reader might have noticed that the two definitions are quite dissimilar, which is an indication of the difficulties related to measuring islanding and especially finding the exact moment of the start of an islanding. Neither of these standards should be considered to fully grasp an islanding situation, but at least the inverter must be able to handle these situations.

Further, it is reported in [5] that these the requirements are subject for change and are likely to be stricter in the future.

An inverter that energises the system even after islanding has occurred may cause problems. If the grid is turned off due to maintenance, then an inverter which continues to energise the system would pose a threat to any maintenance worker operating the grid. Similar when a fault has occurred near the inverter, and the feeding transformer's fuse has blown, it is not wanted that the inverter shall continue to energise the grid, as this will feed the fault.

Power quality

Power sent to an electric grid must have a certain quality; otherwise the whole grid might become unstable and devices with a high power quality requirement will not function. The factors treated here are limited to *voltage*, *DC-injection*, *flicker*, *frequency*, *distortion/harmonics* and *power factor*. These measurements are to be taken at the point of common coupling (PCC)

- **Voltage**

  PV systems connected to the grid normally do not have any real influence on the grid voltage. Their voltage operation range are therefore more of a protection function that is used for detecting abnormal utility, rather than regulators. Such a typical voltage detection may be as defined in [4] and shown in Table 3-1.

Voltage*	Maximum trip time**
$V < 50\%$	6 cycles
$50\% < V < 88\%$	120 cycles
$88\% < V < 110\%$	Normal operation
$110\% < V < 137\%$	120 cycles
$137 < V$	2 cycles

Table 3-1: Voltage operating range in compliance with [4]. * The nominal voltage at PCC is the base value. **"Trip time" refers to the time between the abnormal condition and the inverter ceasing to energize the utility line. The inverter will actually remain connected to the utility to allow the inverter to sense utility electrical conditions for the "reconnect" future.

- **DC-injection**

  No more than 0.5% of the rated current output shall under any circumstances be injected into the power grid. The reason for this limitation is because large and durable DC currents will eventually saturate the transform's iron core. In a saturated iron core the magnetic flux will start to find other paths outside the iron core. This means that the leakage flux will be increasingly large, and thus lowering the transformer ratio.

- **Flicker**

  Whereas the IEEE standard says that the PV system shall not create "objectable flicker", the IEC specifies limits for the flicker, rewritten in Table 3-2. For the actual calculation of flicker, please refer to the standards. Flicker is annoying for human beings, because flickering causes temporary power fluctuations that for instance causes lamps to flicker, hence its name flicker.

Limits P_{st}*	Limits P_{lt}**
≤1.0	≤0.65

Table 3-2: Flicker limits [2]. * P_{st} is the short term flicker indicator. This is the flicker severity evaluated over a short period (in minutes), where P_{st}=1 is the conventional threshold of irritability. ** P_{lt} is the long term flicker indicator. This is the flicker severity evaluated over a long period (a few hours) using successive P_{st} values.

- **Frequency**

  A working inverter shall work synchronously with the connected power grid. If the grid itself goes outside some specified frequencies, then the PV system shall stop energising the grid.

  For the North American 60 Hz grid, [3] gives the following limits for a system smaller than 30 kW: f<59.3 Hz or f>60.5 Hz – clearing time 0.16 s.

  Whereas the IEC specifies that when the frequency varies with ±1 Hz of the base value, then the system shall cease to energise the power grid within 0.2 s. If, however, the grid gets back into synchronism before these 0.2 s, then the inverter does not need to cease energising.

- **Current distortion**

  Current distortion is highly unwanted in any grid, since it may affect connected devices in a negative manner. An overview of the maximum allowed harmonic current distortion may be found in Table 3-3. The THD_i is limited to 5 % of the rated fundamental harmonic.

Individual harmonic order h (odd harmonics)*	$h<11$	$11\leq h<17$	$17\leq h<23$	$23\leq h35$	$35\leq h$
Allowed percentage	4.0	2.0	1.5	0.6	0.3

Table 3-3: Maximum harmonic current distortion in percent of rated fundamental current. *Even harmonics are limited to 25 % of the odd harmonic limits.

For further details about harmonic limits, please refer to [2], [4].

- **Power factor**

  [3] requires that in normal conditions the power factor shall be larger than 0.85 (leading or lagging) when the load is larger than 10 % of the rated power. However, the utility may allow lower power factors in order to provide reactive power compensation. For such small systems, which are investigated in this thesis, the possible contribution of reactive power to the grid is considered so small, that this possibility is excluded, and only the nominally given power factor will be considered.

Reconnection

If the inverter for some reason ceases to deliver power due to abnormal grid activity, then the inverter may be reconnected to the grid only after the power voltage and frequency has been within normal voltage and frequency ranges for at least 5 minutes.

If you always wait for the grid to fix itself, before reconnecting the smaller PV modules, then you assume that other and conventional power sources can deliver enough power to the grid. But if many small PV-modules normally contribute with a significant power, it may not be easy to get the grid up and running with just the conventional power sources. This is a delicate problem that might become a problem with the increasing use of photovoltaics.

3.2 Solar panel characteristics and PV panels

First thing that should be known about solar panels is that they provide a DC output. From an economical point of view, it is important that the maximum power point (MPP) is found. This can only be found when through detailed knowledge about the solar panel's *V-I* characteristics.

In order to characterise the PV-panels, the short circuit current (I_{SC}) and the open circuit voltage (V_{OC}) are often used. As can be seen from Figure 3-1, I_{SC} varies approximately proportionally with the sun's irradiation, whereas V_{OC} is hardly affected, and the solar irradiation's influence is normally neglected. From the same figure the reader may also see the affect of the ambient temperature. Here the change in I_{SC} is normally neglected, but V_{OC} changes at a more noticeable degree, and a PV module containing n_c solar cells in series has a voltage gradient equal to[1]:

$$\frac{dV_{OC}}{dT} = -2.3n_c[mV/K] \tag{3.1}$$

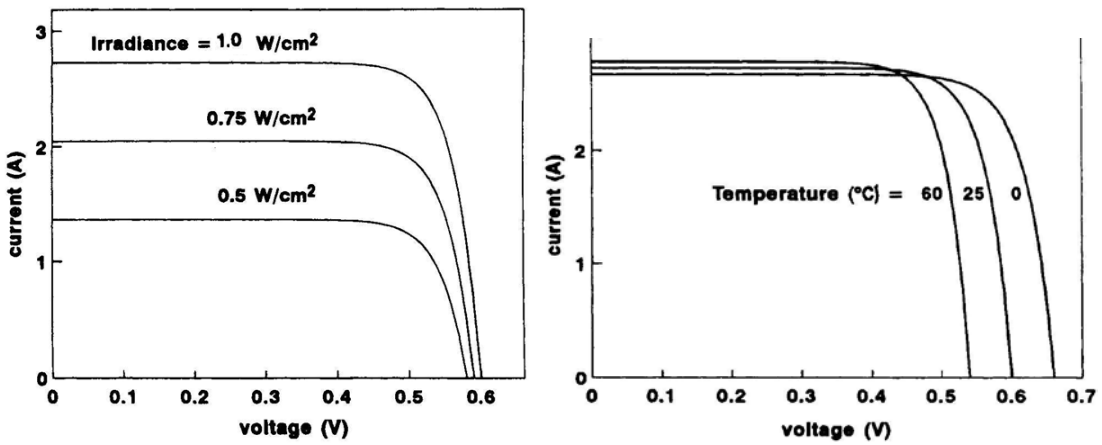

Figure 3-1: Left: Current – voltage characteristics for a typical cell with varying solar irradiance. Source: [1] Right: Current – voltage characteristics for a typical cell with varying ambient temperature. Source: [1]

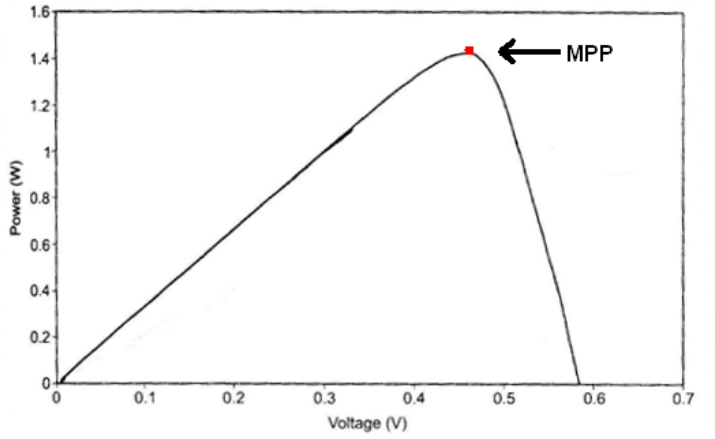

Figure 3-2: Typical power – voltage characteristic for a typical cell. Source: [1]

Now that these characteristics are better known, the power output may easily be found, as in Figure 3-2. The maximum power point (*MPP*) is then readily found. It is at all times wanted to have the PV system working as close to *MPP* as possible, since power is what generates income.

Further it is worth noticing that since the power is the product of the current and voltage, then the *MPP* will consequently be highly depended on both temperature and the sun's irradiance, both of which are hardly considered to be fixed quantities. Therefore a good inverter should be designed with a maximum power point tracker (MPPT), which at all times give a close to optimum power.
Lastly the solar cell's temperature is of interest, and may be expressed as [1]:

$$T_c = T_a + \frac{NOCT - 20}{0.8} G[°C] \tag{3.2}$$

Here T_c is the cell temperature, T_a the ambient air temperature. G is the actual sun irradiance. *NOCT* is the cell temperature when the ambient air temperature is 20 degrees Celsius and an irradiance of 0.8 kW/m^2. *NOCT* is cell specific and normally around 42-46 degrees Celsius.

An interesting feature of the PV system is the quite limited short circuit current for each PV cell; it is in the same range as the normal current. This means that any short circuiting of the system will *not* trigger normal fuses. Also, there are no easy ways of

de-energising the system during daytime, since the system will have a voltage during daylight, unless it is precisely short circuited.

3.3 Solar panel and converter configurations

How the solar panels are connected to each other has a great influence on the inverters requirements and thereby what sort of inverter should be chosen. The author of [6] presents four ways of connecting PV modules, which may be seen in Figure 3-3.

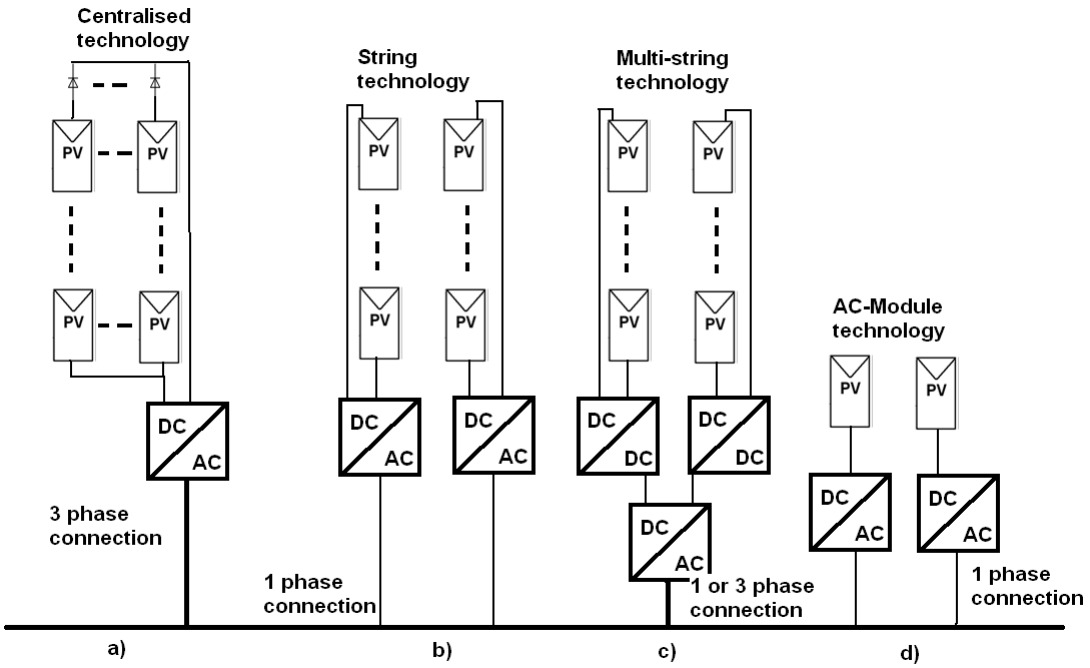

Figure 3-3: A historical overview over PV inverters. a) Past centralized technology. b) Present string technology. c) Present and future multi-string technology. d) Present and future ac-module and ac cell technologies.

Centralised inverter technology

The so called centralised technology (Figure 3-3a) implies that PV modules are connected in series until a rather high voltage is achieved. One row of these series connected inverters is called a string. These strings are then connected in parallel to achieve the wanted power. A so called string diode is placed at the end of each string, to make sure that no current flows from one string to another.

The advantage of this technology is that there is no need to boost the output voltage. Only a single inverter is needed for the whole system, meaning that the total cost for the power conditioning unit is rather low.

The drawback with this technology is among other that since the PV voltage is not boosted in the power conditioning unit, and then there is a rather high voltage on the cable to the PV system, which means that isolation becomes expensive. Secondly the MPPT is now tracking the *MPP* for a large number of PV modules, meaning that power is lost in comparison to a MPPT tracking fewer units, since estimation mismatches are bound to occur more often with so many modules.

String inverters and multi-string inverters

The string inverters are a reaction of these drawbacks. By giving each string their own inverter, then a separate MPPT may be used on each string, meaning that the power loss related to the MPPT is reduced. One may still avoid a voltage boost by adding a DC-DC converter and/or a transformer, with the same pros and cons as for the centralised inverter. Giving each string their own power conditioning unit means that the string diode and thereby also its losses is avoid, but more inverters would mean more losses here. The added number of components would mean a higher initial cost than for the centralised inverters of the same power rating.

The multi-string inverter represents a further step, where each string has its own DC-DC converter with MPPT, but these DC-DC converters are all connected to a single DC-AC converter. These multi string inverters can be looked upon as a hybrid between the centralised inverter and the string inverter, achieving a low number of components but still achieving a good *MPP*.

AC-module inverters

The AC module consists of a single PV module and a power conditioning unit. This module approach means that the initial cost to power ratio will be larger than for the other units. It also means that the MPPT operates optimally regarding mismatches with the *MPP* estimation.

More importantly it means that the user friendliness of the PV system is drastically improved because no separate inverter installation is required. This is quite important to consider, because as the other technologies require good technical understanding in connecting PV modules together, this module type is more of a “plug and play” type, and subsequently may be sold on the open market to the average man on the street, not just the professional users. Any expansion would also be easy, due to the simplicity of the system.

This converter configuration also offers the possibility of de-energising the system, as briefly discussed in section 3.2, which is a nice safety feature.

3.4 Inverter components and topologies

This section gives a brief classification of inverters; actual inverters are thorough presented in (Chapter 4). It is also deals with different components which may be used in these topologies and benefits and limitations they represent.

3.4.1 Power decupling and capacitors

This thesis focuses on single phase inverters, which means that the output power varies with time:

$$p_{grid} = 2P_{grid}\sin^2(\omega t) \tag{3.3}$$

Here P_{grid} is the averaged delivered power. Since a solar cell is considered to be a DC power source with constant power, there is obviously need for some sort of power decupling – that handles large changes in currents. The natural choice is using

capacitors. Also notice that the inverters must be dimensioned to handle two times the wanted output power.

Normally electrolytic capacitors are used on the DC side, because they have good capacitance to volume ratio [9]. Their downside is that they are polarised, meaning the designer must make sure that the capacitor under no circumstances undergoes negative voltages. Secondly their lifetime follows the Arrhenius equation with regards to both rising voltage and rising temperature. Very often the capacitor is the component which limits an inverter's lifetime.

As (3.2) suggest, the solar cell is likely to be fairly warm when producing power. So as a mean of increasing the overall system life, the inverter should have some thermal isolation between itself and the solar cell. This is especially so for plug and play inverters sold to non-technical people, who are likely to be more concerned about removing and replacing an inverter.

When designing capacitors into the inverter it is important to remember that it is required (IEC 62040-1-1) that the inverter voltage is reduced to a safe level within 5 minutes after disconnection. This is normally done with adding a resistor in parallel to the capacitor. This resistor shall cause limited power losses in normal operation.

3.4.2 Semiconductors

Any proper power conditioning unit should use some semiconductors. Here four relevant switches will be presented: Thyristor (3.4.2.1), MOSfet (3.4.2.2), IGBT (3.4.2.3) and SiC JFet (3.4.2.4).

3.4.2.1 Thyristor

The standard symbol of a thyristor may be seen in Figure 3-4a, with its ideal *I-V* characteristics shown in Figure 3-4b. A main advantage of the thyristor is that it can

block very high voltages, up to 7 kV (2 kV for inverter grade thyristors) and currents up to 3 kA.

And whereas transistors need a continuous gate voltage to conduct, the thyristor only need a gate current of some duration to stay on until zero current is reached. This means, however, that the thyristor is sensitive to transients in the system. If for instance there is no initiative for current during the gate's current pulse, then the thyristor will not turn on, and may similarly turn the thyristor off too early. There is also a risk that a large dv_f/dt may unintentionally trigger the thyristor.

The thyristor also has limited frequency range, due to the slow trigger response, meaning that the thyristors are best for high power and low frequency operations.

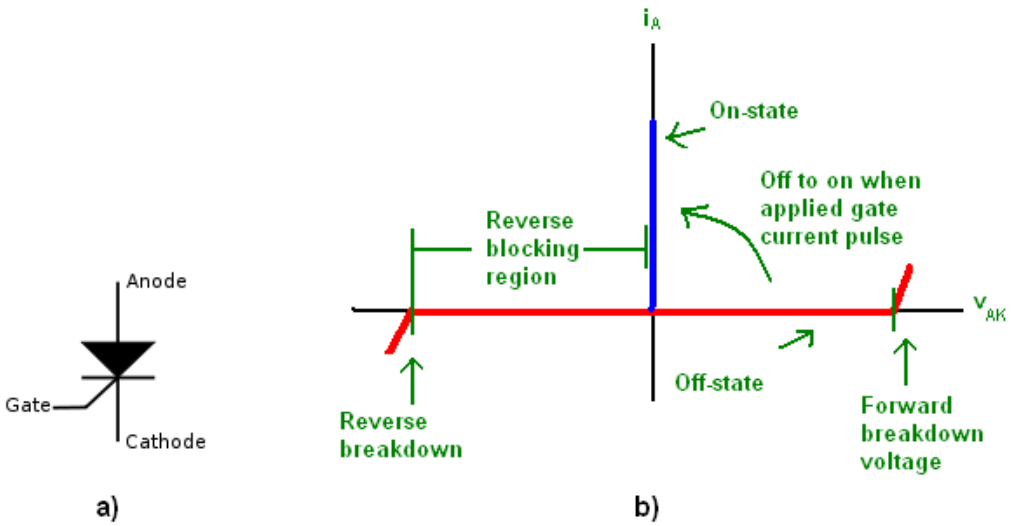

Figure 3-4: a) Thyristor symbol with pin names. b) Simplified *I-V*-characteristics for the thyristor in a.

There are also made enhanced thyristors with the ability to be turned off as well, these are called gate turn off thyristors or simply GTOs.

3.4.2.2 Mosfet

The mosfet symbol may be seen in Figure 3-5a and its corresponding *I-V*-characteristics in Figure 3-5b. Notice that the diode in anti-parallel with the switch

itself, this means that negative currents may pass through. With positive currents it requires a relative large ongoing gate signal to conduct.

Mosfets have the fastest switching speeds of the traditional switches, but have a relatively limited power capability; mosfets have max ratings at 1000 V for low current ratings and 100 A for low voltage ratings. Mosfets therefore excel at high frequency and low power applications.

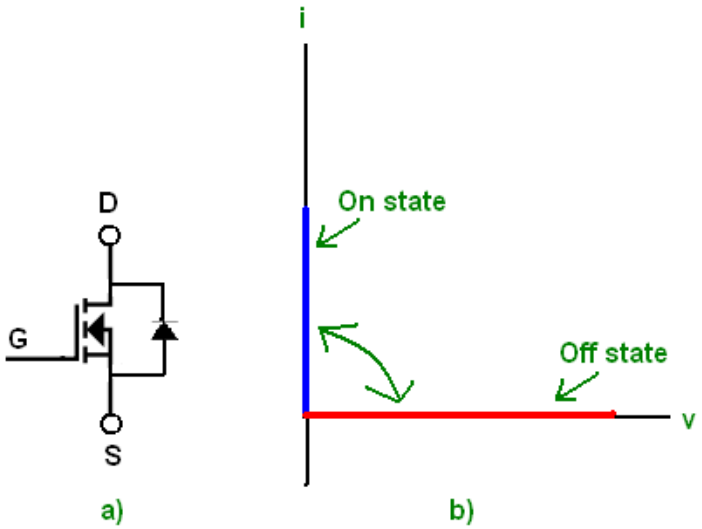

Figure 3-5: a) Mosfet symbol with pin names. b) Simplied *I-V*-characteristisc for the mosfet in a. Only positive voltage is shown.

3.4.2.3 IGBT

The IGBT symbol may be seen in Figure 3-6a and its ideal *I-V* characteristic in Figure 3-6b, including the breakdown voltages. It blocks negative voltage as well as acting as a switch for positive voltages, which is good in comparison to the mosfet who needs a diode in series to block negative currents.

The IGBTs offers a greater power capability then the mosfets as well as a better frequency rating than the thyristor, making it the best choice for medium power and medium frequency devices. It also requires a lower ongoing gate-to-emitter voltage to conduct than the mosfet. IGBTs are commercially available up to 6.5 kV and 500 A.

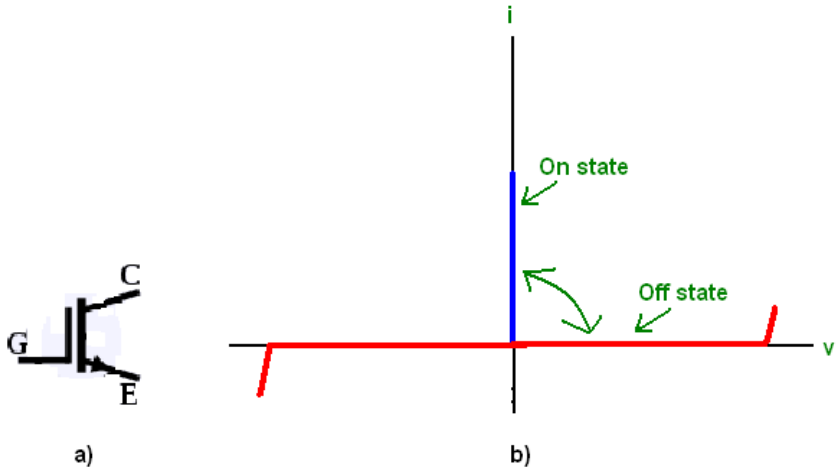

Figure 3-6: a) IGBT symbol with pin names. b) Idealised *I-V*-characteristics for the IGBT in a.

3.4.2.4 Normally OFF Silicon carbide power JFET (SiC JFet)

SiC JFets are possibly the semiconductors of the future. JFets were for just a few years ago considered having higher on-state losses and inferior switching speeds in comparison to other switch technologies [10], whereas they now are considered to be superior in both of these fields [11][12]. The required gate current is also reported to be no more than 2.5 V in comparison to the normal 10-15 V needed for IGBTs.

The symbol of the SiC JFet may be seen Figure 3-7a, along with the idealised *I-V*-characteristic in Figure 3-7b. The forward blocking voltage is normally in the range 1200 V, and like the IGBT it also has a reversed voltage blocking capability, but usually no more than 30-40. The reverse current resistance is higher than the forward current resistans

A comparison of IGBT and SiC JFet switches in a commercially available PV inverter was done in [11], and the overall maximum system efficiency was reported to rise from 93 % using IGBTs to almost 94 % using SiC JFet.

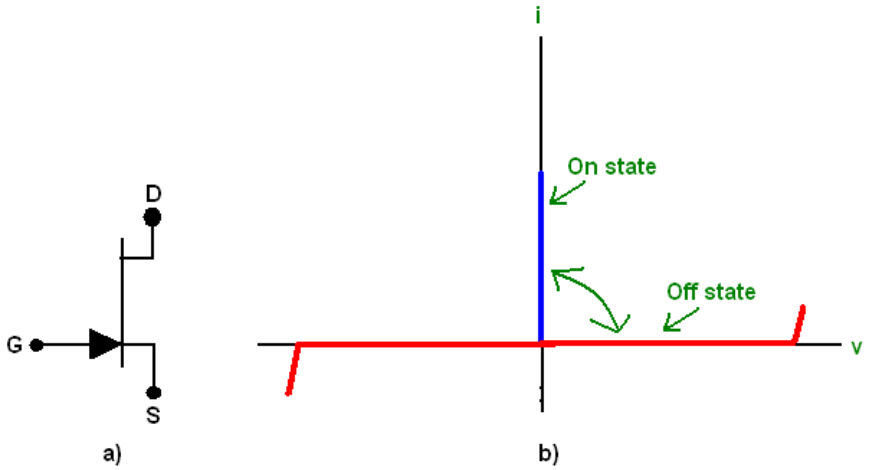

Figure 3-7: a) Sic JFet symbol with pin names. b) Idealised I-V-characteristics for the SiC JFet in a.

3.4.3 Transformer

There are many reasons for adding a transformer to a PV inverter. First of all it offers galvanic isolation, which is required in several countries [8]. Secondly, if mounted on the low frequency side, it effectively stops any DC current injection into the power grid, which effectively means that it complies with the DC injection limits discussed in section 3.1.1. And naturally it also boosts the voltage, which is often wanted when dealing with only a few PV modules.

The downside is that it represents power losses and thereby reduces efficiency that would otherwise be avoided. The issue of DC-current may also be solved with measuring equipment capable of detecting small DC currents. Finally the transformer also introduces increased costs and system size, both of which are non-negligible.

If a transformer is considered advantageous for the inverter in mind, then there is always the option of mounting it on the low frequency (LF) grid side, or embedding it in a high frequency (HF) DC-DC converter. Choosing the LF side has the advantage of no DC current injection into the grid, but suffers from large cost, size and weight, whereas HF transformers opens up an interesting field of DC-DC converter topologies with built in transformers. Modern inverters tend to use HF transformers [5].

Regardless of where the transformer is added, its equivalent circuit [6] is as shown in Figure 3-8.

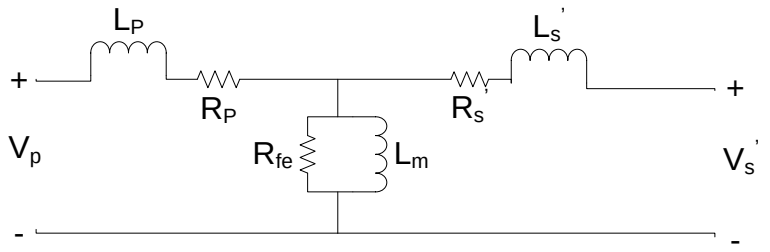

Figure 3-8: Equivalent circuit diagram of a transformer. Subscript *P* is primary side and subscript *S* is secondary side.

3.4.4 DC-DC converter

As discussed in 3.3, there is no need for a DC-DC converter if only the output voltage of the PV module is high enough, but if it is considered beneficial, then these *dual stage* inverters have some interesting features.

Roughly the DC-DC converters may be divided into HF-link converters or DC-link converters, depending on whether the DC produces a rectified high frequency output voltage or a constant value DC-link. The former technique means that the inverter would simply unfold and filter the high frequency DC-DC output. This method looks quite promising and this thesis will investigate two such options. The latter technique requires a for more traditional inverter with for instance controlling the grid current using sinusoidal pulse width modulation (PWM).

When using a HF transformer, then this is normally a built-in feature of the DC-DC inverter by the means of for instance a flyback, push-pull or variants of the H-bridge.

High power applications are best done with DC-link converters [6], but for the low power applications – which this thesis looks into – the HF-link is interesting.

3.4.5 AC-DC inverter

When designing a complete PV inverter, one must choose between single phase and three phase inverters. Single phase inverters are often favoured by power ratings below circa 5-6 kW, and subsequently three-phase above this rating.

When choosing an inverter type, there are some things to take under consideration. If a HF-link is chosen, then an inverter with a form of H-bridge is often selected, as they may easily be controlled to unfold the voltage to a sinusoidal waveform.

With a DC link one can still use a H-bridge, or even cascade connect several, as a form of multilevel inverter. Multilevel inverters main selling point is the combined voltage rating. This would require several PV strings to achieve the wanted voltage, and would mean that the last PV string would have a high potential to earth, and one would need to take insulation issues into consideration. Therefore only low level multilevel inverters are to be considered in this thesis.

3.5 Grid filter topologies

Normally the output of the inverter is not a good sine, and a filter is therefore needed to smoothen the output on the AC side of the inverter, so that the power quality reaches the requirements discussed in 3.1.1. Some frequently used grid filter topologies will be discussed and selected for further use; L-filter (Figure 3-9a), LC-filter (Figure 3-9b) and LCL-filter (Figure 3-9c).

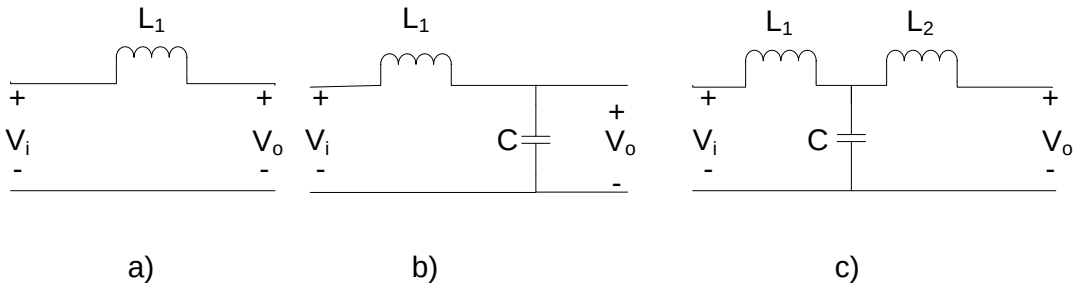

Figure 3-9: An overview over filter topologies. a) L-filter. b) LC-filter. c) LCL-filter.

3.5.1 L-filter

The simple L-filter (Figure 3-9a) is a first order filter, which means that it does not have any resonance problems. On the other side the inductance needed would be rather large for a good quality output, which means that the inductor would be more expensive than the LC-filter. A simple L-filter is therefore excluded for these types of applications.

3.5.2 LC- and LCL-filter

Designing higher order filters means that the resonance frequency needs to be taken into consideration. Shannon's sampling theorem states the sampling frequency (f_s) shall be more than two times greater than the highest signal frequency of interest, in our case the resonant frequency (f_{res}).

$$10 f_m < f_{res} < 0.5 f_{sw} \tag{3.4}$$

Further on the resonant frequency should be kept at least one decade above the modulated frequency (f_m), which in our case will be the 50 Hz grid frequency. These two limitations are summarised in (3.4). Often f_{res} is selected as close to the upper limit as possible.

The LC-filter (Figure 3-9b) would be cheaper than the LCL-filter (Figure 3-9c), but one challenge with the LC-filter is that its resonant frequency varies with the grid inductance, which is highly unwanted. The LCL-filter has the same problem, but as we will se under, it impact of grid the grid inductance is lower.

Also, if a transformer is placed on the LF side of the inverter, it can be constructed to utilise its leakage inductance as L_2 in the filter. However increasing the leakage

inductance is highly unwanted, since that would mean that flux is lost, and thereby the voltage output is lower than if no leakage flux were present.

In [9] simulations have been performed with both LC- and LCL-filters. The most interesting observations will be quoted here:

"LC-filter

- *Small changes in* L_1 *and* C *create large shifts in the resonant frequency.*
- *Increasing the load leads to a greater damping of the amplitude peak at the resonant frequency, and the resonant frequency is shifted slightly lower.*

LCL-filter

- *Small changes in* L_1 *and* C *create large shifts in the resonant frequency*
- *Adding a second* L *between the LC-filter and the load does not have a significant effect on the resonant frequency.*
- *Large variations in* L_2 *result in variations in the attenuation and phase above the resonant frequency. The larger the inductance, the higher the attenuation gets. The attenuation is higher than with the LC-filter.*
- *Increasing the load leads to a greater damping of the amplitude peak at the resonant frequency, and the resonant frequency is shifted to a higher value."*

Both of the filters introduce zeroes and poles into the design, which makes the dynamics of the system harder to control. Therefore for instance damping resistors are inserted for stability reasons, like suggested in [13] and shown in Figure 3-10. The drawback is of course the added conduction losses.

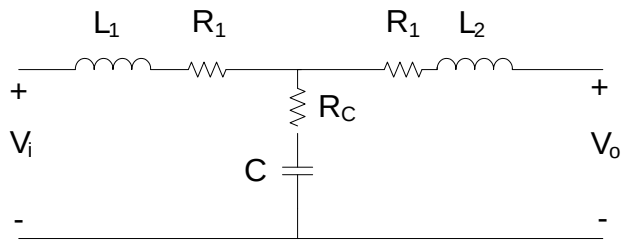

Figure 3-10: Modified LCL-filter.

The author found this variant of the LCL-filter the best, and will use it further, except in the case of resonant circuits, where the filter may be part of the inverter design itself. Some of the other alternatives were also good, but they normally introduce more components and system complexity, which is unwanted in a small power system.

The resonant frequency is given by [14] for an unmodified LCL-filter:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 C L_2}} \tag{3.5}$$

The added resistance is assumed to be so small that it will hardly influence the resonant frequency.

As a side remark, it is important to take into consideration the frequency range which human can hear, this is considered to be approximately between 20 Hz and 20 kHz. As it can be quite annoying to hear the switching of the inverter, switching frequencies will be kept outside of this range to avoid this problem.

3.6 Energy storage

It is possible to create a PV system were parts of the load are not connected directly to grid, in way that can be described as an advanced uninterruptible power supply (UPS) circuit, or simply an island configuration that works without the grid.

Area of application for such a system could for example be security cameras (like CCTV) or a computer server. In order to deliver such a system, an energy storage system is needed, like a battery or rather super capacitors in combination with a battery in the case of the computer server.

It is also possible to use a battery to compensate for a weak grid, where sudden high power taps were to be met by the battery. This is quite common, but for such small PV systems that this thesis looks into, the contribution would be negligible.

3.7 Encapsulants and lifetime

The final step when designing an inverter is to make the encapsulant or housing. The encapsulant is dependent of whether the inverter is to stand indoors or outdoors. Outdoor encapsulants obviously have more requirements, because of a more hazardous environment, e.g. humidity and temperature.

For a plug and play inverter, it is preferable to let the inverter stay outdoor if possible, so that user does not need to deal with the space of the inverter. That means that only an outdoor AC connection to the grid is needed, which is not uncommon on houses.

In order get a good lifetime of an outdoor inverter, a good encapsulant is then needed, and a good check list [19] for this encapsulant is:

- *"High thermal conductivity to ensure large lifetime of MIC (*Module integrated converter, author's comment*).*
- *Chemical resistance to humidity and most common organic solvents are essential to provide environmental protection.*
- *The coefficient of thermal expansion (CTE) should match the CTE of IMS* (Insulated Metal Substrate, author's comment*) (aluminum) to avoid mechanical stress and ensure good adhesion.*
- *Glass transition temperature (*T*,) should be higher than maximum MIC operating temperature (100°C).*
- *Low modulus and flexural strength to eliminate stress on the MIC components.*

- *Low cure temperature and short (as much as possible) curing time to keep sensitive elements (IC, electrolytic capacitors) under low temperature stress.*
- *Low level of ionic impurities (Na+, **K+,** Cl-) for high insulating resistance against temperature and humidity. "*

Due to the cost of the encapsulant, it is economical to design the inverter as compact as possible. The design of the encapsulant is important, but is considered out of scope for this thesis.

Regardless of the encapsulant, the system will always break down and some point. Table 3-4 offers an overview over component failure rate. This is of course inverters based on a specific topology, and parameters such as switching frequency and current will in other applications vary, but tendencies are quite clear; the capacitor is the component with highest failure rate. This suggests that choosing a good capacitor and operating voltage and temperature are of uttermost importance when designed a long-lifetime inverter.

Component	**Temperature [°C]**	**Failure rate based on [20]**
DC capacitors	77.0	60 % (4 electrolyte capacitors)
Control	83.5	14 % (including rest of components)
Rectifier Mosfet	85.8	(including diodes)
Converter Mosfet	83.9	10 % (including transformer)
AC-filter	86.2	8 % (including filter capacitors)
Sum		100 % (35.7 failers/10^6 h)

Table 3-4: Temperatures and failure rates of inverter components at rated mode of operation. Source: [19]

When designing plug and play inverters, it is especially important to have along inverter lifetime, since the compactness of the inverter means it would be difficult to change components, meaning that it is likely that the entire inverter must changed if one part such as a capacitor ceases to function.

4 Investigating grid connectable photovoltaic inverter topologies

In this chapter five different inverter topologies shall be investigated; H-bridge (section 4.1), series resonant buck boost inverter (SRBBI) (section 4.2), a hybrid multilevel inverter (section 4.3), flyback DC-DC converter with unfolding DC-AC inverter (section 4.4) and series resonant DC-DC converter with PWM DC-AC inverter (section 4.5). These inverters will then be compared (section 4.6) and finally two of them will be selected for further investigations in a computer simulation.

The requirement of the topologies at this stage is that they are capable of producing a fundamental harmonic which is 230 V and 50 Hz sine.

For all of the topologies it is possible to add a transformer to the AC-output side. The transformer will however not be discussed here, unless the transformer is a built-in feature of the inverter.

4.1 H-bridge

The H-bridge represents a steady and reliable inverter topology, the topology may be seen in Figure 4-1

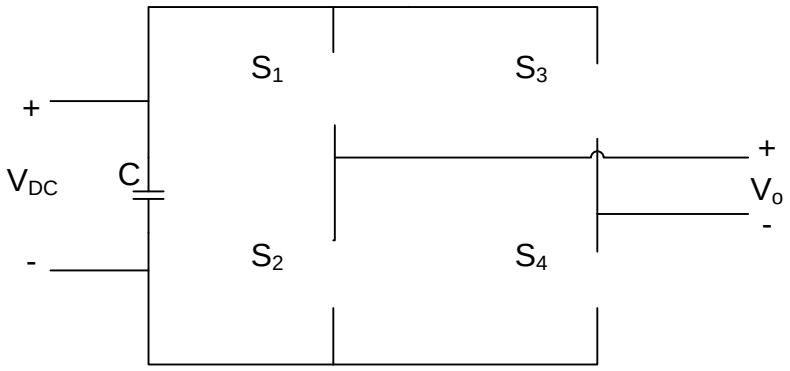

Figure 4-1: Schematic of a H-bridge inverter topology.

The inverter may operate with uni- or bipolar with PWM, square wave operation or voltage cancellation. In order to have a well functioning MPPT, there should be some possibility to control the line current, and thereby the output voltage of the PV module. This is best done with either uni- or bi-polar switching. Unipolar switching has the lowest ripple current of the two, and gives a lower *THD* than the bi-polar switching, when operating at the same switching frequency.

The unipolar switching scheme along with its idealised output may be found in Figure 4-2. The main selling points are system simplicity and small number of components, which means low cost. Given a good switching frequency, even the non-filtered inverter output has a fair *THD*. However, unless a transformer or a DC-DC converter is used, the input voltage must be quite high, due to the lack of boost capability by itself. The voltage is given in (4.1). A thorough derivation may be found in (Appendix 9)

$$V_O = m_a V_{DC} \tag{4.1}$$

The H-bridge topology will be a component of the hybrid multilevel inverter, the flyback DC-DC converter with unfolding DC-AC inverter and the series resonant DC-DC converter with unfolding DC-AC inverter, both of which we will come back to.

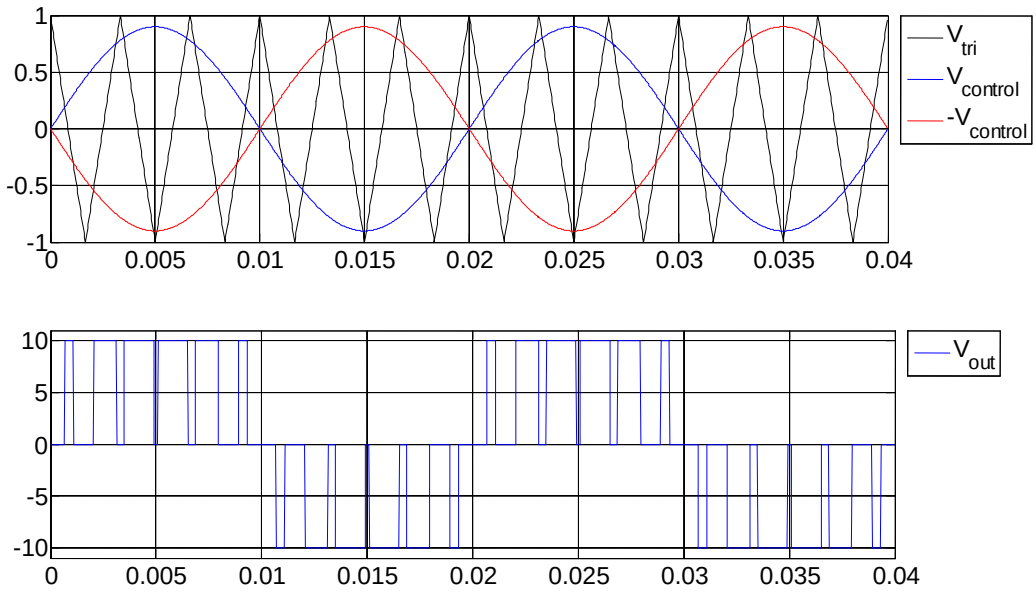

Figure 4-2: Upper: Unipolar switching scheme. Lower: Idealised output voltage. Control signal frequency is 50 Hz while the trigger signal frequency is 400 Hz. The modulation degree is 0.8.

4.2 Series resonant buck-boost inverter (SRBBI)

The series resonant buck-boost inverter was originally presented in [15]. Its topology can be seen in Figure 4-3. In order to better understand this circuit, let us have a look at the switching solution presented in the same paper.

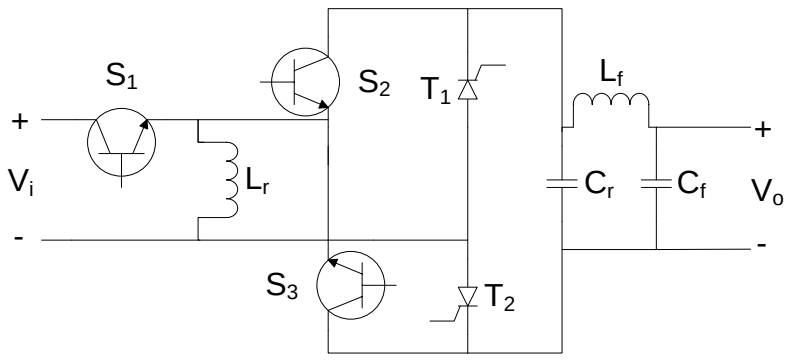

Figure 4-3: The single-stage series-resonant buck-boost inverter. [15]

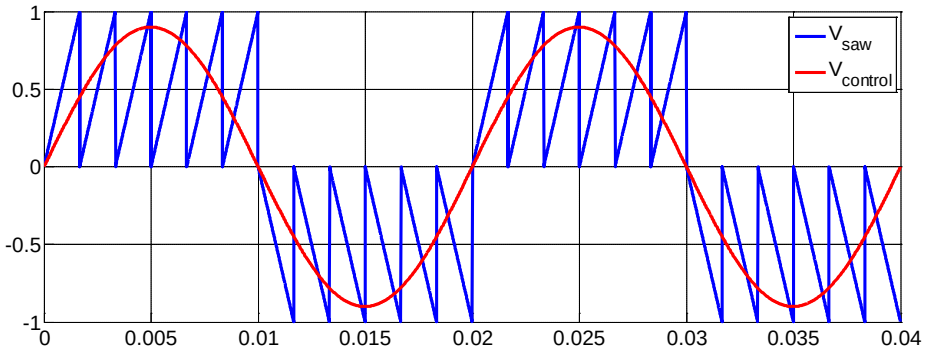

Figure 4-4: Switching scheme for the SRBBI in Figure 4-3. f_m=50 Hz, m_f=12, m_a=0.9.

Logical function	Influence on switches
$v_{control}>0$ & $v_{control}>v_{saw}$	S2 off; S3 on; T1 on; T2 off
$v_{control}<0$ & $v_{control}>v_{saw}$	S2 on; S3 off; T1 off; T2 on
$v_{control}<v_{saw}$	S1 on
$v_{control}>v_{saw}$	S1 off

Table 4-1: Switching scheme of the SRBBI. The labels correspond to those in Figure 4-3 and Figure 4-4.

The switching pattern may be seen in Figure 4-4 and the corresponding logical functions determining the switching sequence in Table 4-1. During the positive period time of $V_{control}$, S_1 will switch on every time $v_{control}<v_{saw}$, while all of the other switches are off. This means that the inductor L_r is charged and the voltage is

$$i_{Lr}(t) = \frac{V_{in}}{L_r}(t - t_{k0}) \tag{4.2}$$

t_{k0} is the start of the period, and discontinues conduction mode (CCM) of L_r is assumed. At the same time the output the two capacitors and the inductance is acting as a resonant thank, and the voltage may be found as:

$$v_{Cr}(t) = v_{Cr}(t_{k0}) - \frac{I_{Lfk}}{C_r}(t - t_{k0}) \tag{4.3}$$

Here it is assumed the current through Lf can be regarded as constant within this stage.

Then $v_{control}>v_{saw}$ ($time=t_{k1}$), and subsequently the current will cease to conduct through S_1 and start going through S_3 and T_1, thereby L_r is charging the right hand side of the inverter. This continues until the current tries go below zero at which point T_1 effectively ceases to conduct ($time=t_{k2}$). Within this stage, the following equations are true:

$$i_{Lr}(t) = I_{lfk} + [i_{Lr}(t_{k1}) - I_{lf}]\cos\omega_r(t-t_{k1}) - \frac{v_{Cr}}{Z_0}(t_{k1})\sin\omega_r(t-t_{k1}) \tag{4.4}$$

and

$$v_{Cr} = v_{Cr}(t_{k1})\cos\omega_r(t-t_{k1}) + Z_0[i_{Lr}(t_{k1}) - I_{Lfk}]\sin\omega_r(t-t_{k1}) \tag{4.5}$$

Here $\omega_r = \frac{1}{\sqrt{L_r C_r}}$ and $Z_0 = \sqrt{\frac{L_r}{C_r}}$.

In this third the current through L_r is 0, and C_r acts as a voltage source to the rest of the source:

$$i_{Lr}(t) = 0 \tag{4.6}$$

$$v_{Cr}(t) = v_{Cr}(t_{k2}) - \frac{I_{Lfk}}{C_r}(t-t_{k2}) \tag{4.7}$$

A complete derivation of these equations may be found in (Appendix 10). A similar switching scheme is done during the negative half-cycle of $v_{control}$ with S_2 and T_2.

The main selling point for this circuit is that it may boost the voltage and invert it in just one step, without any transformer or a separate DC-DC converter. This would mean a low weight and low cost due to the limited number of components – ideal for a little plug and play PV system. When using the thyristors to cut the current, this means that the switching losses should be very low, also for S_2 and S_3.

In [15] a proposed circuit operates at a 60 Hz fundamental frequency, 20 kHz resonant frequency and 40 kHz switching frequency and with a 500 W load. That may be a problem for many thyristors, since they are normally not used for more than about 500 Hz because their recovery time is quite low.

Another practical problem would be the L_r at the moment when S_1 is turned off and S_3 ($_{S2}$ for negative half) and T_1 (T_2 for negative half) is turned on. The coil acts as a current source and must lead its current somewhere, but with the slow on- and off-characteristics of the thyristor, this might be a problem. In addition the thyristors would be subject for quite large *dv/dt* from the L_r, which might cause a sudden and unwanted triggering of the wrong thyristor.

4.3 A hybrid multilevel inverter

There are currently three main ways of multilevel inverters: Using H-bridges with isolated sources, neutral point clamped (NPC) or flying capacitors.

The multilevel H-bridge requires isolated sources for each H-bridge in order to create the different levels, whereas this is not a requirement for the two other topologies. Normally these isolated sources are established using costly transformers. With modular PV systems these transformers are not necessary, since each module may act as a separate dc-source, even at the gain of efficiency, as the *MPP* estimations is better, as discussed in section 3.3. Also DC-bus balancing is avoided with an H-bridge configuration, which keeps the system simplicity down, which is good for a plug and play system. Therefore a multilevel inverter topology with H-bridges is investigated further.

In [16] a hybrid multilevel inverter is presented. The system is originally meant for a three phase system, but with only using one leg of the three phase system, a single phase system may be achieved. The topology of the inverter may be found in Figure 4-5.

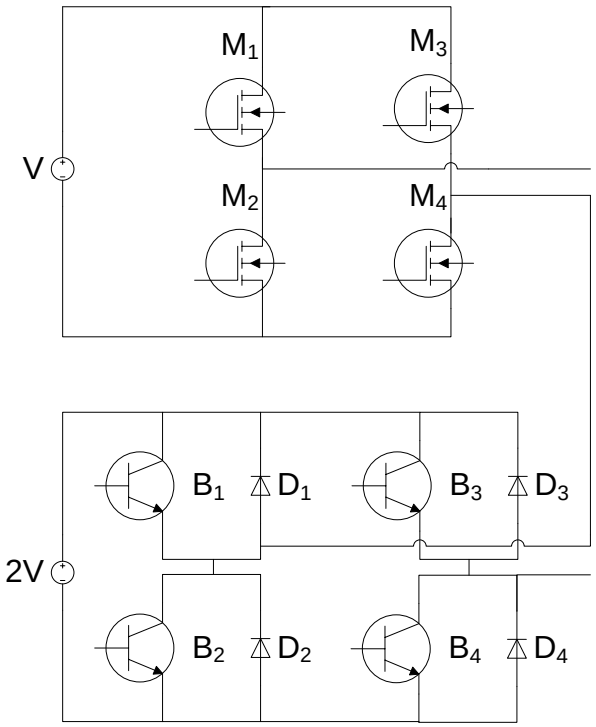

Figure 4-5: A hybrid multilevel inverter.

The output of this inverter is simply the sum of its two H-bridges, which was discussed in section 4.1. The voltage of the sources may have different input voltages, as summarised in Table 4-2. This thesis will further use the variant of the H-bridge were each voltage level is two times larger then the previous, and only two sources will used, i.e. *N* in Table 4-2 is 2.

Topology	Levels in the output
NPC	N+1
Flying capacitor	N+1
Conventional H-bridge	2N+1
Modified H-bridge*	2^{N+1}-1
Modified H-bridge**	3^N

Table 4-2: Overview over number of output levels for different topologies when *N* input voltage levels are available. *Each voltage level is two times larger than the previous. **Each voltage level is three times larger than the previous.

The main point of choosing this variant in stead of choosing the triplet variant, is because of the voltage source and its *MPP*. The PV modules must either be made so that one module is twice the physical size of the other, or it must have a DC-DC

converter to boost the voltage, and we would have a similar expansion for the triplet version. As a DC-DC converter would mean higher cost, an increased size of one of the PV modules is more wanted. A doubled size PV panel is plausible, but a tripled size PV panel would be more difficult to utilize.

The main selling points of this inverter type is that the H-bridge with the highest voltage source may be run at the fundamental frequency, whereas the second H-bridge operates at high frequency but low voltage. Subsequently the two H-bridges may use different switching technologies. In the example from [16] IGBTs are used for the low voltage, high frequency H-bridge and GTOs are used for the high voltage, low frequency H-bridge. This means that the GTOs are used to transfer the main load, while the IGBTs are used to increase the power quality. Because of the low voltages from the PV-modules, utilizing IGBTs and GTOs would be an exaggeration, but a similar approach with Mosfets and BJTs would be plausible.

The switching scheme of this topology is perhaps the most complex of all the circuits. A simple unipolar or bipolar switching scheme would be hard to create, since there are two different frequencies involved. Manjrekar et al. [17] offers a solution which can be summarised as this:

A command signal given the wanted instantaneous output signal is sent to a comparator, if the wanted output signal is higher than the voltage of the low voltage source, than the high voltage H-bridge is turned on, similar for negative values. The output voltage of the high voltage bridge ($2V$, 0 or $-2V$) is then compared to the wanted instantaneous output voltage, and the difference between these two voltages are the control signal for the PWM modulated low voltage bridge, so that it produces $1V$, 0 or $-1V$ at its output.

A detailed flow chart may be found in (Appendix 11) and a typical output response can be seen in Figure 4-6. The command signal represents the instantaneous wanted output signal.

A drawback this multilevel inverter, is that when the wanted output voltages are only 230 V, then the advantage of using different switches are of less importance, since even mosfets in a normal H-bridge can handle the power. Secondly it requires more components then the other topologies, which means higher cost. Lastly it requires several PV modules which must be correctly interconnected, this lowers the user friendliness wanted in plug and play PV systems.

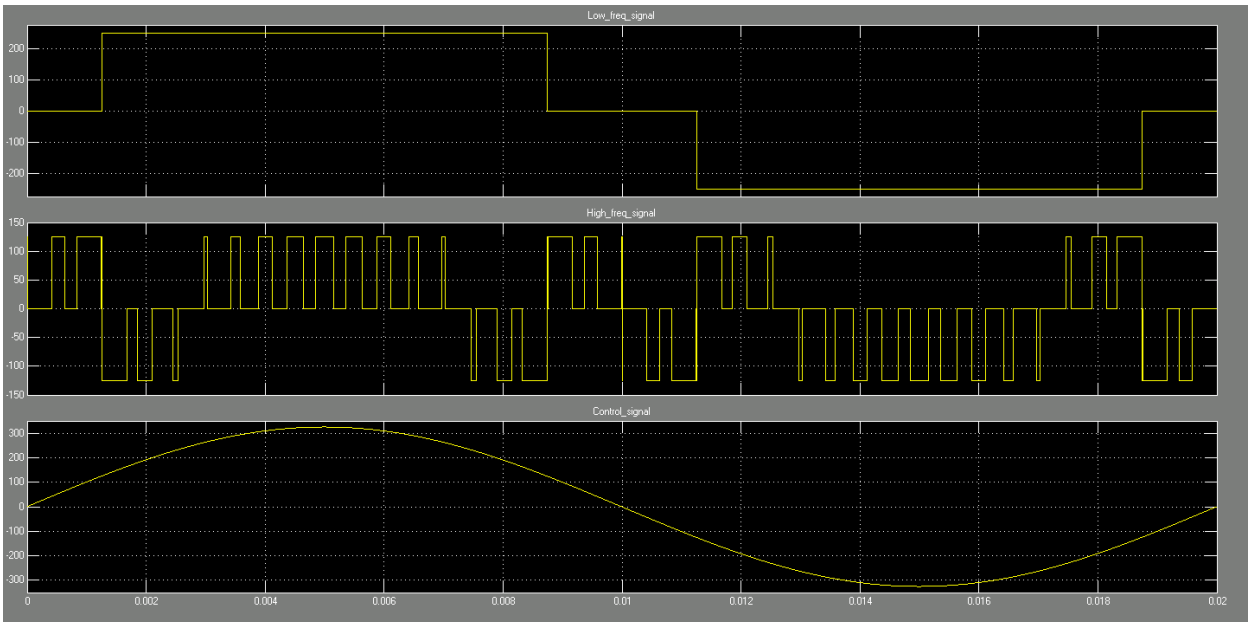

Figure 4-6: Ideal output signals for the high voltage H-bridge (upper graph) and the low voltage H-bridge (middle graph). The voltages sources are 250 V and 125 V respectively, and frequencies are 50 Hz and 2kHz respectively. The command signal (bottom graph) is a 50 Hz sin with an amplitude of 325 V.

4.4 Flyback converter with PWM DC-AC inverter /with unfolding AC-DC inverter

The flyback converter with PWM DC-AC inverter was first presented in [18], and its topology may be seen in Figure 4-7. The inverter is a standard H-bridge, and was described in section 4.1.

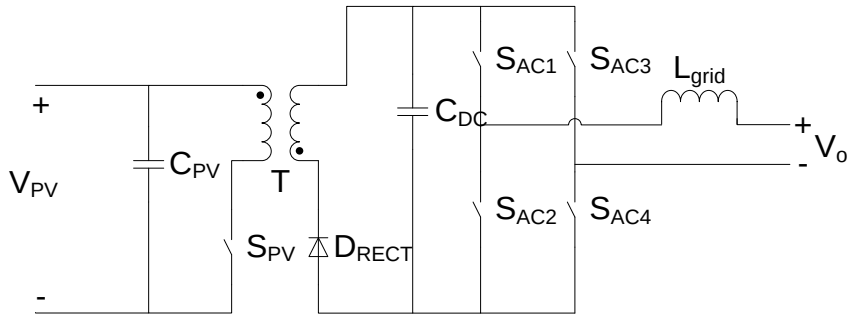

Figure 4-7: A flyback converter with PWM DC-AC inverter. Source: [18]

The flyback converters output voltage can be found to be [10]:

$$V_{DC} = V_{PV} a \frac{D}{1-D} \tag{4.8}$$

The inverter output voltage would then be:

$$V_O = V_{PV} a \frac{D}{1-D} m_a \tag{4.9}$$

a is the transformer winding ratio. A more in dept derivation may be found in (Appendix 12).

The difference from H-bridge is that the flyback inverter allows smaller input voltages and gives galvanic insulation, meaning the inverter does not require a large PV system to operate.

An important consequence of adding a capacitor at both sides of the transformer is that C_{DC} can handle the power decoupling needed between the grid and the PV module without having so many farads, as if it was on the low voltage DC side. In addition it also means that only the H-bridge inverter needs to be dimensioned for two times the output power.

Please also notice that it possible to use the flyback inverter to produce rectified sine waves, which the H-bridge then can unfold at its zero voltage crossings. Thus only

S_{PV} operates at high frequency. This would lead to less power losses for the H-bridge, both since they now would operate at only two times the fundamental frequency and due to the low voltage being cut off during the switching.

Of these two uses of the same topology, the use with the unfolding inverter looks the most promising, due to the expected lower power losses. However, when using the unfolding inverter, it is very important that the input voltage and current has a voltage and current which are very close to being in phase with each other; otherwise the unfolding will create a large distortion.

4.5 Series resonant DC-DC converter with PWM DC-AC inverter

The series resonant DC-DC converter with bang bang DC-AC inverter is presented in [8], and a modified version of this is presented here (Figure 4-8), namely the series resonant DC-DC converter with unfolding DC-AC inverter. The changes consist of removing two diodes, one between S_{AC1} and S_{AC3}, and another between S_{AC2} and S_{AC4}. Secondly the S_{AC1} through S_{AC4} switches with the unipolar switching scheme as presented in section 4.1, i.e. without the "bang bang". This is basically the same the same topology as in section 4.4, just that the DC-DC converter now is a series resonant DC-DC converter rather than a flyback converter.

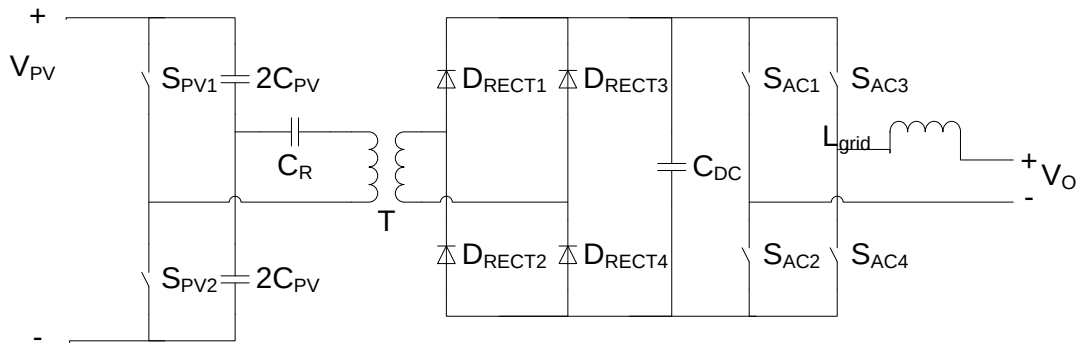

Figure 4-8: Series resonant converter with unfolding DC-AC inverter

The capacitance C_R together with the transformer's leakage inductance forms a resonant tank and is designed so that S_{PV1} and S_{PV2} switch close to the zero voltage crossings. This means that it can operate at much higher frequency then the flyback inverter and still get the same switching losses.

The downside is expected to introduce a higher transformer current, which would increase the transformer currents. Generally it is expected that the efficiency is high at low loads, but decreases as the load increases [8].

4.6 Selection for further investigation

This section focuses on discussing the inverter topologies, for finally selecting two inverter topologies for further studies.

The SRBBI (section 4.2) has an inherent boost element with neither a transformer nor a separate DC-DC stage. This is likely to create a very cost efficient system, and even give a fair *THD*. The coil in parallel with the voltage source might be problematic, as it is supposed to have quite large currents at the time of switching, and thereby all of the switches will be quite stressed at this point. This problem is assumed to be problematic and this inverter is therefore not selected for further studies.

Then one inverter with a built-in transformer is to be investigated; the series resonant DC-DC converter with PWM DC-AC inverter (section 4.5) looks promising with low losses, but the reported large losses at higher loads are not good, and since it is wanted to use the inverter at as high powers as the ratings allowed, this does not seem as a good choice for further studies.

The flyback DC-DC converter with unfolding DC-AC inverter (section 4.4) is a good choice since it has fewer components then the prior inverters, in particular there are less capacitors, which as we remember from Table 3-4 being the main reason for

inverter breakdowns. On the other side the power factor before the unfolding converter must be very close to unity, otherwise it suffers from heavy current distortion when trying to unfold the voltage at its zero crossing.

The H-bridge (section 4.1) is a good topology, both because of its simplicity and good output power quality. It is also the most compact inverter, due to the single stage topology. This is also a drawback, as it lacks a boost capability. But since the output voltage is no more than 230 V, a voltage boost capability is not necessary with many available PV modules. The H-bridge is selected for further studies.

The hybrid multilevel inverter (section 4.3) offers improved output power quality compared to the H-bridge, given the same total input voltage level. And because of the low frequency on the high power module, the switching loss is low. Each voltage source would have a lower voltage than the one H-bridge. The downside here is that two different PV modules are needed, one that produces *n* volts, and one that produces *2n* volts, or a series connection of two n volts PV modules. This problem is considered to be easy to overcome, even for non-technical personnel, and the hybrid multilevel inverter is therefore selected for further investigation.

5 Modelling and optimisation of preferred types

In this chapter the two selected inverter topologies will be modelled and simulated in SPICE and Simulink, so that a better understanding about them is reached. There will also be an optimalisation of the programme, so that it operates accurately. Then the actual simulation will be done; first a comparison of the two inverter topologies selected in the previous chapter will be done. After carefully judging, one of the inverter topologies will be chosen for further and more in-depth investigation

5.1 Readying the programme

Before the actual simulation is done, it is needed to optimise the programme, so that the output signal is as accurate as needed.

Since all of the simulations that shall be presented here are to be in steady state, it is important to ensure that steady state is indeed achieved. A rough but good way of doing this is to let the simulation run one time for a large time period, and visually inspect when the periods do not change from one to another, and then start the data logging a few periods *after* this steady state has been achieved.

When this step has been reached within acceptable levels, then a fine tuning of the maximum allowed time steep is in need. For the first time simulation the author uses a maximum simulation step of one tenth of that of the fastest switching speed.

Still working on the maximum allowed time step, we now need to do a fourier analysis of voltages and currents of relevance. In order to get a good fourier analysis later, the user manual suggest to set the maximum time step to be 10 times lower than then the period of the last harmonic with a “sizeable” amplitude. This will most likely

increase the simulation time quite drastically, but should also give a very accurate fourier analysis.

In order to reduce the calculations speed, or to increase the accuracy of the calculations, the minimum accuracy of among others the voltages and currents may be altered.

5.1.1 The energy source

As seen in section 3.2, a PV module may be considered neither an ideal voltage source nor an ideal current source, so power decoupling is needed. For the case of the two inverter types selected, a large capacitor is needed at the input of the inverter. This is selected so that the voltage seen by the rest of inverter can be considered constant despite of the varying power.

The power sources used in the simulation programmes are not able to handle the complex pattern for the PV-modules' current and voltage. Therefore the voltage over the capacitor is modelled as an ideal voltage source, which means that neither the PV-module nor the capacitor itself with their characteristics will be represented in the models. This does of course limit the accuracy of the model, but the impact would be fairly low.

5.1.2 The simulation software

This thesis uses two different programmes, Simulink and SPICE, in order to calculate different values. Spice is in general a more accurate programme than Simulink, because it uses accurate switching characteristics of accurate switching models. Whereas Simulinks software uses much more ideal switches, but calculates much faster and it is easier to set up the software correctly. Most importantly it calculates *THD* much faster than SPICE

So what is done in this thesis is to use Simulink for *THD* analysis, as the *THD* is not expected to vary much with different switches. But in order to include switching losses from different switch manufactures, this will be calculated in SPICE.

5.2 Building the model – H-bridge

When designing the H-bridge inverter, we start by defining the limits wherein it shall be able to work, so that proper switches can be chosen. The minimum operating value must be over √2*230 V, otherwise it will not produce a proper output signal according to (4.1). With a margin, we define 330 V as the minimum input voltage. Further we define the maximum allowed load to be 600 W or 120 % of rated value. This gives a maximum current 3.6 A, as seen in (5.1).

$$I_{DC,MAX} = \frac{2P_{MAX}}{V_{DC,MIN}} = \frac{2*600W}{330V} = 3.6A \tag{5.1}$$

Then the maximal allowed voltage input is defined to be 450 V. If we include a safety margin, we can say that the switches shall handle at least 4 A and 500 V.

The SPICE inverter model may be seen in Figure 5-1. The switching scheme is unipolar, as explained in section 4.1.

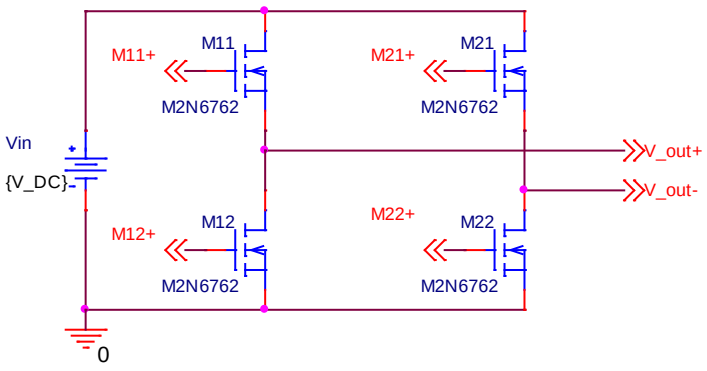

Figure 5-1: H-bridge model in SPICE.

To find a good filter, it is useful to know how the harmonic spectre of the H-bridge looks like. To find this, a harmonic analysis in SPICE was done on the output voltage and current when operating at rated power and voltages, the result may be seen in Figure 5-2 and with a close up of the first 20 harmonics in Figure 5-3. Note that the first harmonic has been cut in the latter figure, in order to increase the readability.

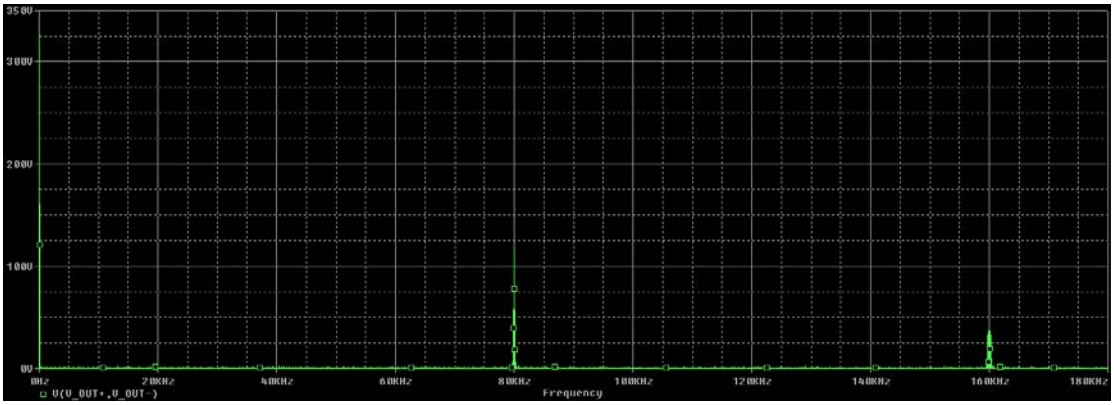

Figure 5-2: Overview over the harmonics between 0 Hz and 180 kHz for the H-bridge operating at m_a=0.835, V_{DC}=400 V and R_{load}=105 Ω.

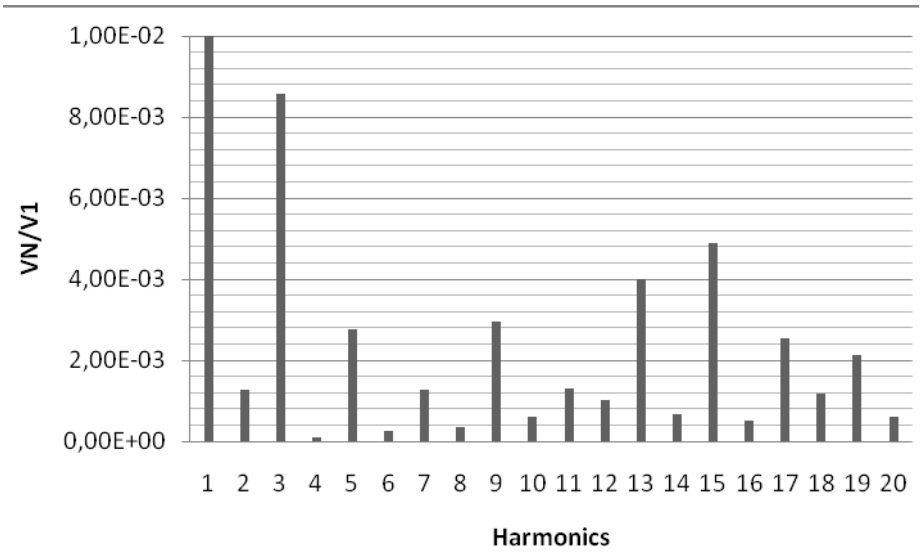

Figure 5-3: Analysis of the 20 first harmonics. The voltages have been nominalised with respect to the first harmonic. NB! V_1 has been cut off for a better visual at 0.01, but its actual length is defined as unity.

As can be seen in these plots, the advantage of the H-bridge inverter when running unipolar switching scheme is that the first significant harmonic cluster occurs at two times the switching frequency, which for this case is about 80 kHz. The first 20 harmonics are rather small and all are below 1 % of the fundamental. This means that only the THD_i must be adjusted to be in accordance with the regulations as discussed in section 3.1. In practice these lower order harmonics will be higher, due to for

instance implemented dead time [10], but this will not be an object for discussion in this thesis.

A good method of selecting the converter side filter inductance, L_2 in Figure 3-10, is found in [21] and restated here in (5.2). In this equation ω_n and V_n are the nth harmonic's frequency and voltage and current respectively, and I_n is maximum allowable current harmonic.

$$L_1 = \max\left(\frac{V_n}{\omega_n I_n}\right) \tag{5.2}$$

The first harmonic of some magnitude is $f=(2m_f-1)f_1$ [10] or 79.95 kHz in this case, where m_f is the frequency modulation; $m_f = \frac{f_s}{f_1}$. $V_{1599,peak}$ was found to be 115 V before the filter, and it is presumed that this voltage more or less entirely will be over L_1. $I_{1,peak}$ and $I_{1599,peak}$ was at the same time 3.0 A and 1.1 A. If we at the peak current of this harmonic be 10 % of the fundamental harmonic, then the corresponding L_1 would be 0.76 mH, which also seem as a reasonable sized inductor for this power rating.

A good filter capacitance can be found by selecting it to be 12 % of the base value as suggested in [9], mathematically shown in (5.3). For this inverter this yields 3.6 μF. This means that the filter's theoretical resonant frequency is at about 3 kHz, which is well within the requirements of (3.4).

$$C = 0.12\frac{P_{rated}}{\omega_1 V_{rated}^{\ 2}} \tag{5.3}$$

Now a good grid side filter inductance, L_2 in Figure 3-10, shall be found. The requirements from section 3.1.1 are the limiting factors. All of the 20 first harmonics are already in the unfiltered topology under the requirements, so the THD_i is decisive for the power quality requirements.

A parameter sweep was done on the filter circuit shown in Figure 5-4, L_2 varies between 0.2 mH and to 1.4 mH with increments of 0.4 mH, the result is plotted as a bode diagram in Figure 5-5. Here it can be seen that the resonant frequency does not vary significantly.

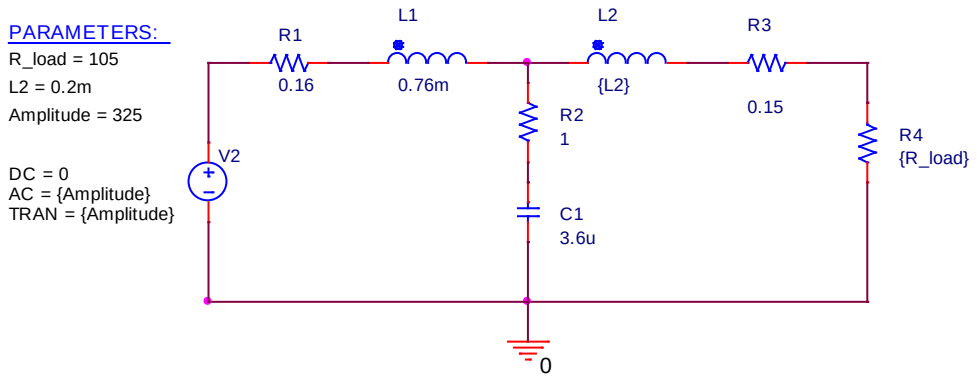

Figure 5-4: LCL-filter modeled in PSpice including damping.

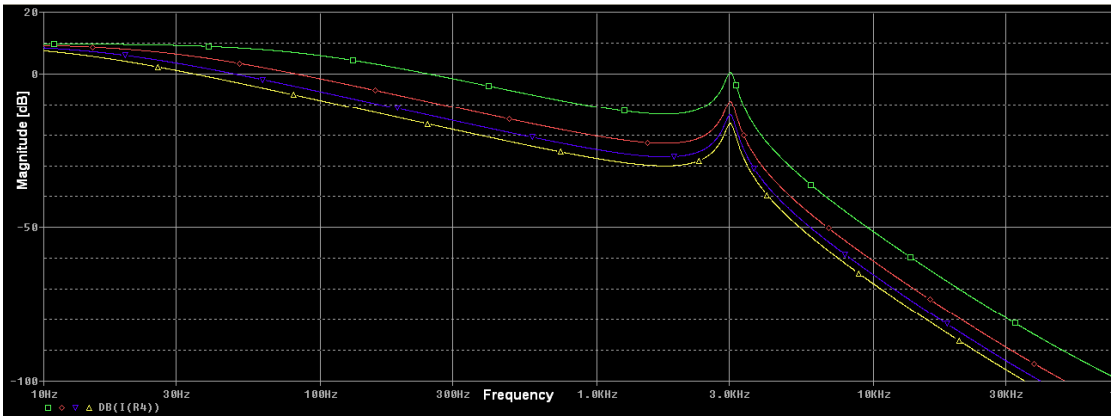

Figure 5-5: Bode diagram of the output diagram. *L2* varies between 0.2 mH and 1.4 mH with increments of 0.4 mH.

In order to get a reasonably physically sized filter at low cost and also reducing its voltage drop, the focus is on limiting the size of L_2, subsequently L_2 is set to 0.2 mH. The values are summarised in Table 5-1. L_2 is considered to be the sum of the filter's inductance and the grid's inductance.

L_1	C	L_2	f_{res}
0.76 mH	3.6 µF	0.2 mH	3.0 kHz

Table 5-1: Filter values for the H-bridge.

5.3 Hybrid multilevel inverter

Now we shall model the hybrid multilevel inverter, as can be seen in Figure 5-6. Since this is two cascaded H-bridges, which together are going to handle the same power as the single H-bridge from last chapter, the current ratings of the switches must therefore be the same, i.e. 4 A.

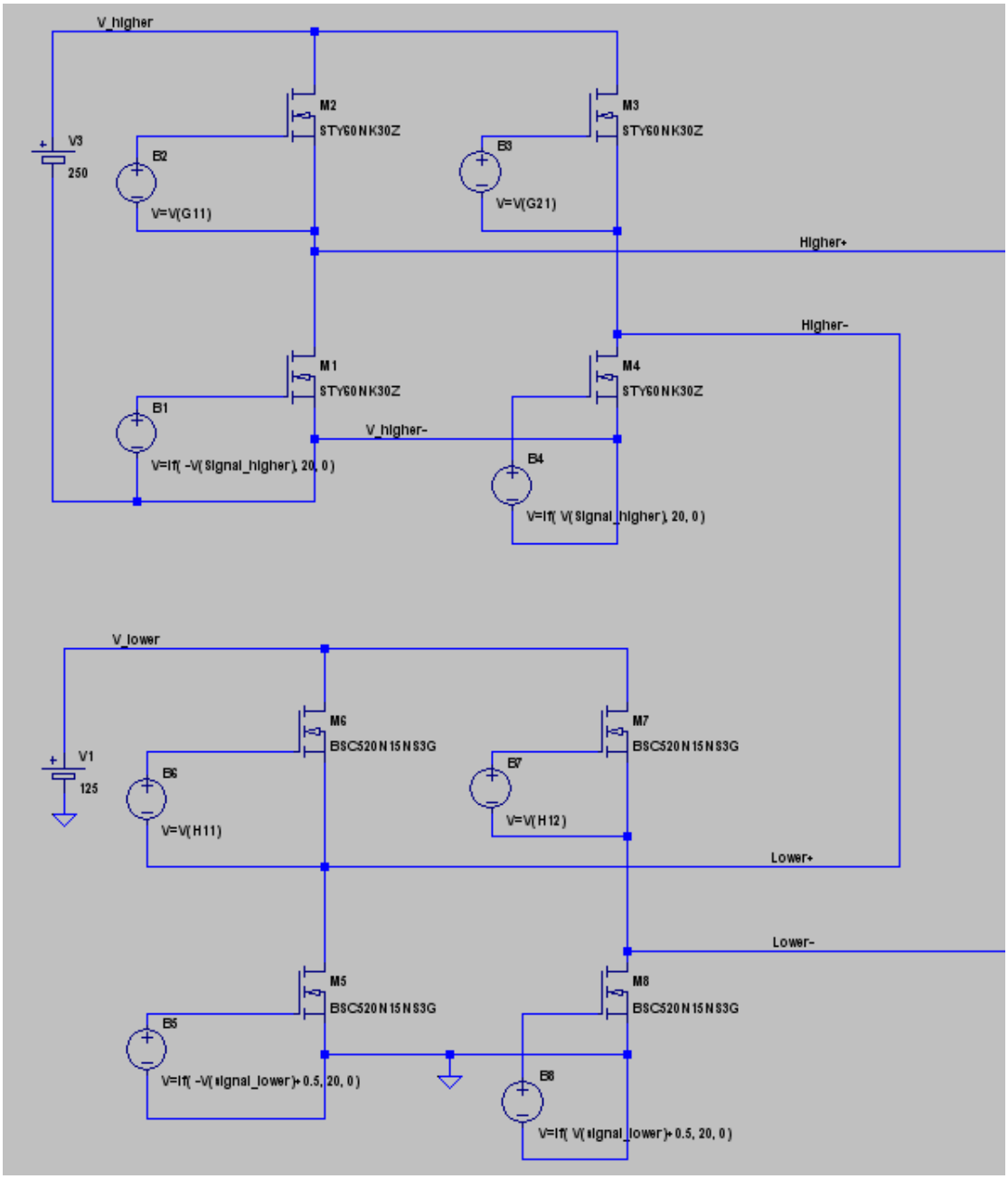

Figure 5-6: The hybrid multilevel inverter modelled in SPICE.

Then the maximum allowed voltage rating needs to be defined. If we say that the total input voltage shall be the same as for the previous case, i.e. 450 V, then the two voltages ratings become 150 V and 300 V for the low and high voltage bridges, respectively.

Since both of the bridges are of relative small voltages, the author thinks that all of the switches should be Mosfets. For the high frequency bridge, this is obviously a good choice, sine it switches fast at low voltages. But for the low frequency bridge, this is of little importance. Nevertheless a mosfet is selected here as well, because the ratings are of relative low voltage, despite that it is labelled the "high voltage" bridge.

Now we take a look to the filter design. The low frequency bridge will have its first significant harmonics already at the third harmonic, so if we just had this H-bridge then designing a filter would be rather difficult. Fortunately the high frequency H-bridge smoothens the voltage, so that the effective output switching frequency is actually 40 kHz, and thereby the first harmonics of significance are found around 80 kHz, similar as for the single H-bridge. However the amplitude of each switch is now reduces to one third, which should reduce the harmonics quite nicely. The same filter as for the single H-bridge is selected, in order to observe whether if the filtered output quality really is better for the hybrid multilevel inverter.

The driver circuit can be found in Figure 5-7, and is based on the driver circuit found in [17].

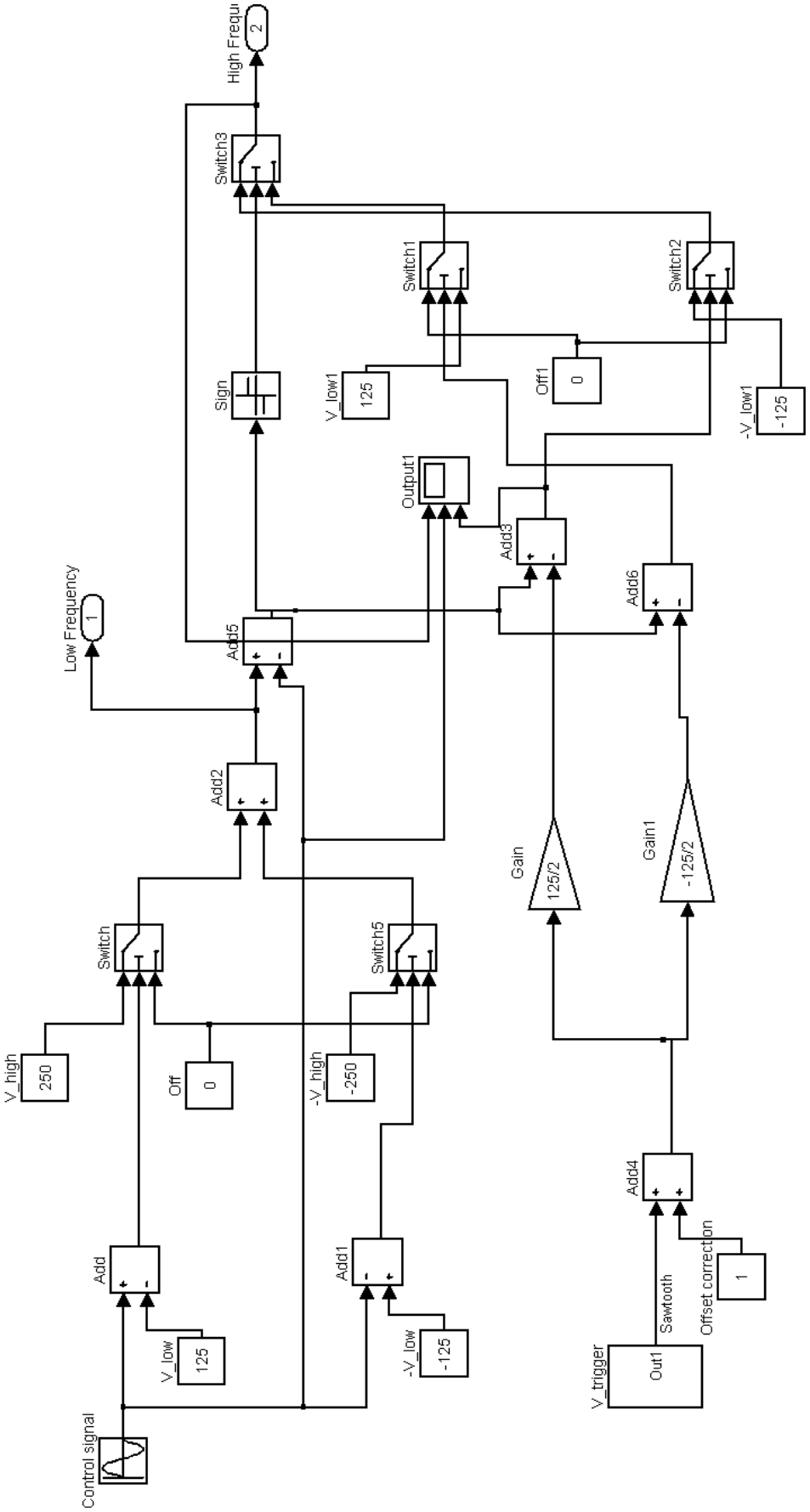

Figure 5-7: Driver circuit for the hybrid multilevel inverter seen in Figure 5-6.

5.4 Simulation results

In this section the two selected inverter topologies are simulated at different output powers and input voltages in order to contain data about losses and THD_i. First general comparisons of the two inverter topologies are done. Then one of the topologies are selected as the best for the given criteria, when this is done some simulations with different switches will be tested to find out which switch gives the best efficiency. This will be tested at different output power and input voltages.

5.4.1 Comparison of the H-bridge and the multilevel inverter

For the initial investigation, simulations will be done when both of the topologies uses Mosfets of the type SPA11N60C3 from Infineon, some of its characteristic parameters are summed up in Table 5-2. This switch is over-dimensioned because it at this point is more interesting to find the differences between the two topologies rather than finding a good switch at this stage of the investigation.

Parameter	*Value*
V_{DS}	650 V
I_D	11 A
R_{on}	0.38 Ω
Turn on delay time	10 ns
Turn off delay time	44 ns
Rise time	5 ns
Fall time	5 ns

Table 5-2: Some parameters for the SPA11N60C3 from Infineon, taken from its datasheet.

Both of the inverters' high frequency switches were run at 40 kHz, the output for one period for the two may be seen in Figure 5-8 and Figure 5-9 for respectively the H-bridge inverter and the hybrid multilevel inverter. Even at first glance it is easy to se that the hybrid multilevel inverter's output waveform is much less distorted than the corresponding H-bridge output waveform. This is also conformed in the harmonic analysis, which yields a *THD* of 75 % for the H-bridge inverter, but only 23 % for the

hybrid multilevel inverter; the multilevel's distortion is only about 1/3 of the of its competitor.

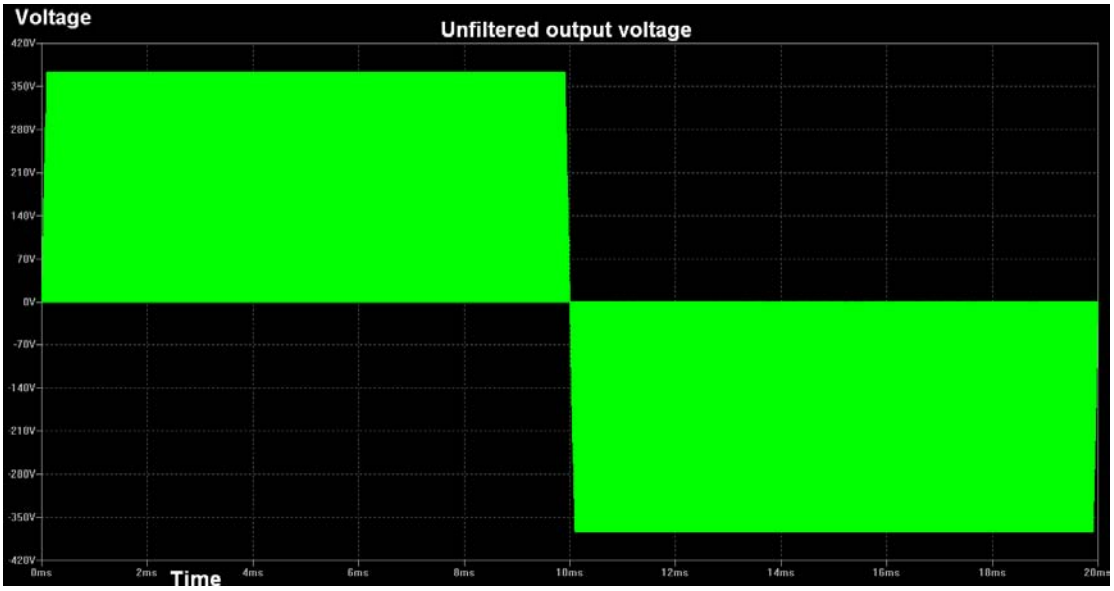

Figure 5-8: Unfiltered output voltage over one time period for the H-bridge inverter, fs= 40 kHz. Vin=375. Grid sizes – vertical: 70 V, horizontal 2ms.

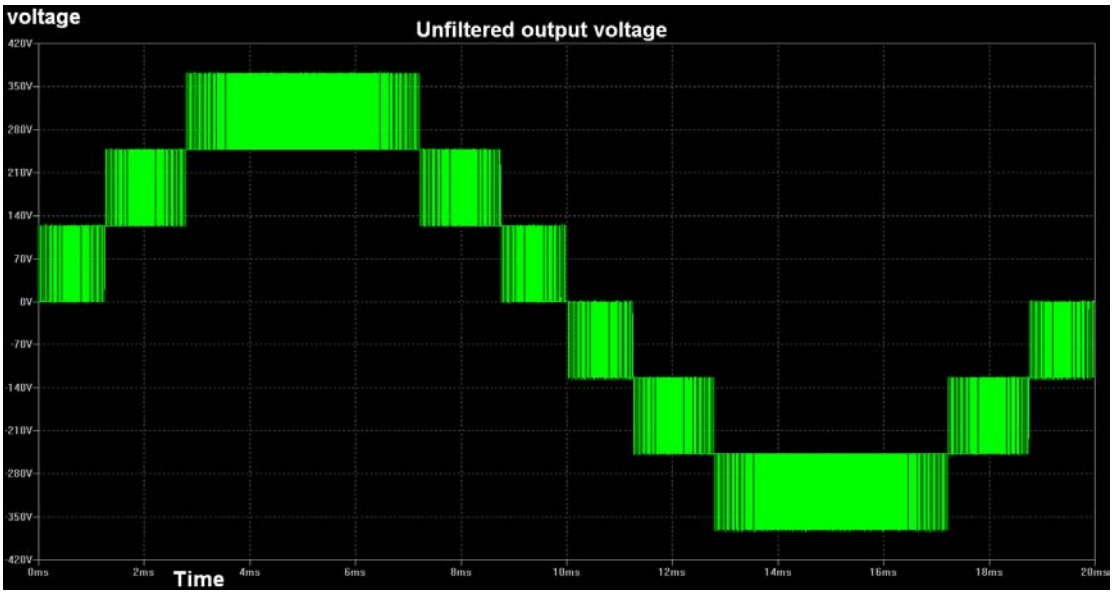

Figure 5-9: Unfiltered output voltage over one time period for the hybrid multilevel inverter, fs= 40 kHz. Vin=375. Grid sizes – vertical: 70 V, horizontal: 2 ms.

The better voltage quality is also confirmed through fourier analysis of the output waveform, shown in Figure 5-10 and Figure 5-11 for respectively the H-bridge inverter and the hybrid multilevel inverter. Both of the inverters have their harmonic clusters around multiples of their switching frequency, but the H-bridge an effective switching frequency of two times that of the hybrid multilevel inverter. Thus the H-

bridge's output is in this respect easier to filter, since the LCL-filter's attenuation is higher for higher frequencies, as may be seen in Figure 5-5. On the other side, the magnitudes of all the other harmonic clusters are much higher, meaning that the filter would have to handle much larger ripples and its associated energy, thus the hybrid multilevel inverter is better in this respect.

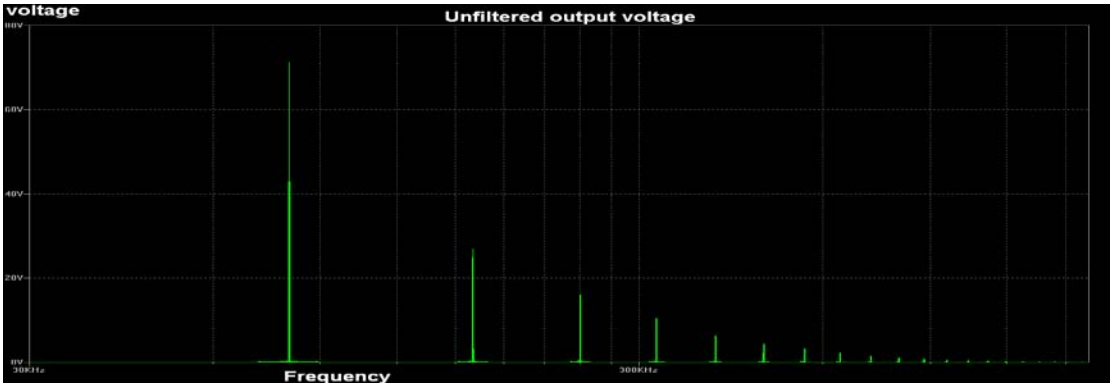

Figure 5-10: Fourier analysis of the output voltage for the H-bridge. Grid sizes – Vertical: 20 V, Horizontal: 10 kHz. Note that the fundamental harmonic is not shown.

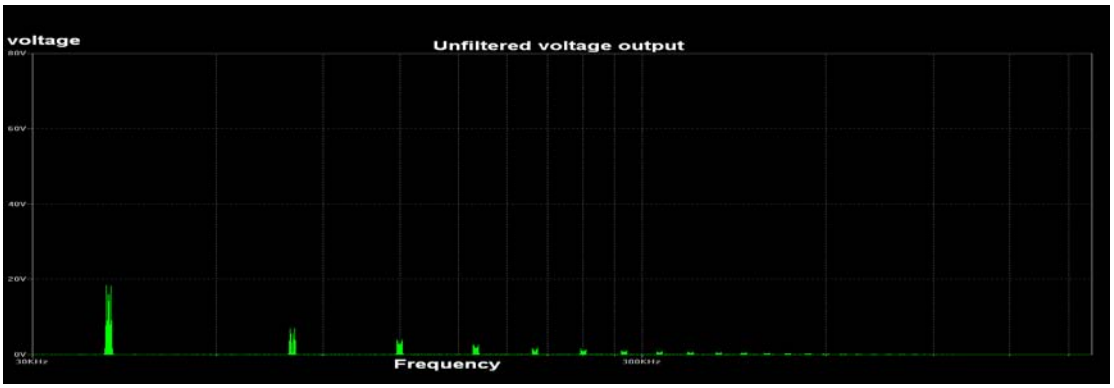

Figure 5-11: Fourier analysis of the output voltage for the hybrid multilevel inverter. Grid sizes – Vertical: 20 V, Horizontal: 10 kHz. Note that the fundamental harmonic is not shown.

The power losses of the H-bridge and the hybrid multilevel inverter are at this point 2.06 % and 3.54 % respectively. This means that even though the single H-bridge inverter has fewer components, and thereby the switch resistance at on state (R_{on}) of all the switches is lower, the hybrid multilevel inverter reaches lower losses because all of the switching is done at lower voltages, and thereby the losses associated with the transition between on and off are greater.

Now the filter from Table 5-1 will be added, and the test results are summed up in Table 13-1 and Table 13-2, and drawn in Figure 5-12, for the H-bridge inverter and

the hybrid multilevel inverter respectively. The output voltage's fundamental harmonic is always adjusted to be 230±2 V and 50 Hz. The output load is set to 106 Ω, or approximately 500 W at 230 V.

In Figure 5-12 it can be seen, that the hybrid multilevel inverter has an efficiency of approximately 1 percent point higher than just one H-bridge. It can also be seen that the efficiency decreases with increasing input voltage. This is because of an increase in the magnitude of the current when the switches are on, which subsequently means that both the losses due to both R_{on} and the transition between on and off are increased.

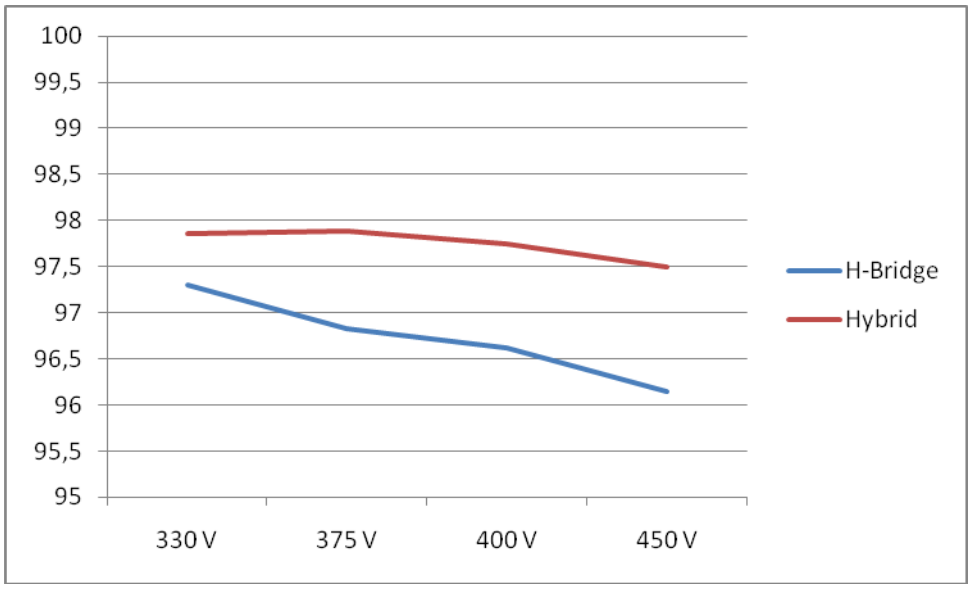

Figure 5-12: Efficiency versus input voltage for the H-bridge and hybrid multilevel inverter.

In Figure 5-13 it can be seen, that an increased input voltage also causes an increasing THD_i at higher input voltages, because the unfiltered ripple voltage is larger. Here it is also confirmed that the THD_i for the hybrid multilevel inverter is much lower for the H-bridge inverter. This again is because each switching in the hybrid multilevel inverter represents a lower change the output voltage.

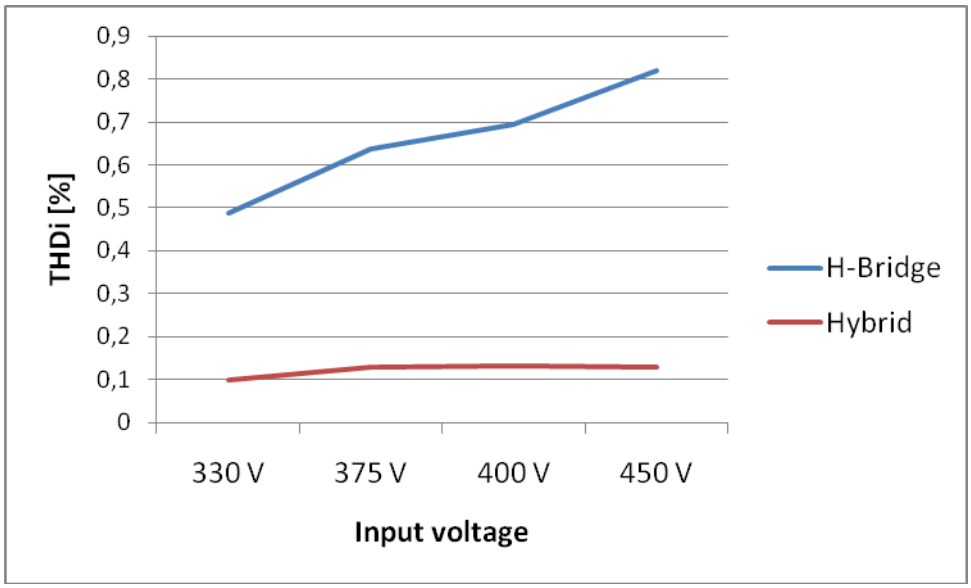

Figure 5-13: *THD*$_i$ versus input voltage for the H-bridge and hybrid multilevel inverter.

The next simulation was done at different desired output power levels. To achieve different voltage power levels, a resistor was calculated by the formula: $R_{load} = \frac{V^2}{P}$. The input voltage set to 375 V for both types. The results may be seen in Table 13-3 and Table 13-4, and drawn in Figure 5-14.

Here we can see that the efficiency at all simulations is best for the hybrid multilevel inverter for the entire power range. Another interesting thing is that the inverter efficiencies are decreasing rapidly for power ranges lower than about 200 W or 20 % of rated value, which is not unusual for a clouded day.

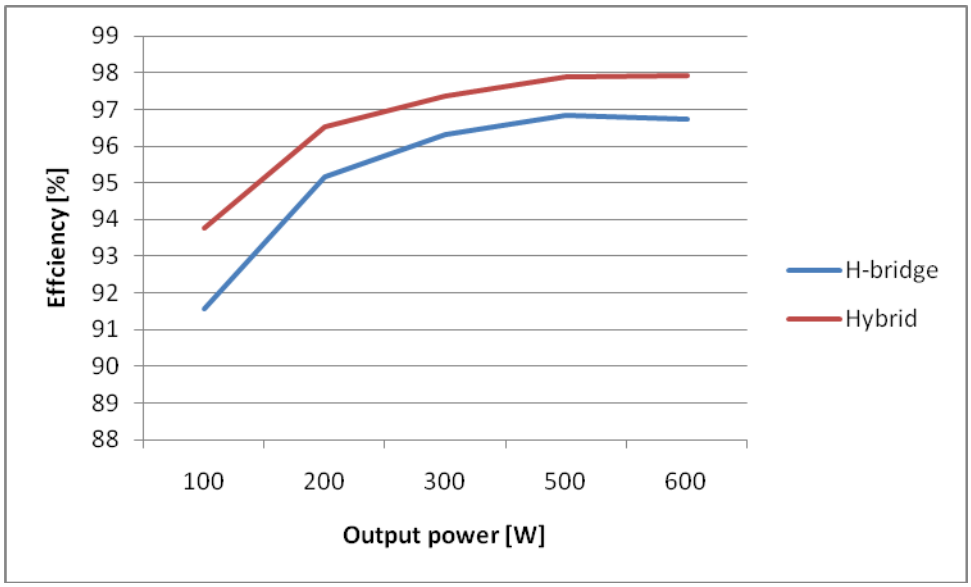

Figure 5-14: Efficiency versus output power for the H-bridge and hybrid multilevel inverter.

Next we will have a look at the THD_i for the same sample, which may be seen in Figure 5-15, and the entire data can be found in Table 13-3 and Table 13-4 for the H-bridge inverter and hybrid multilevel inverter. The hybrid multilevel inverter has a small decrease in THD_i with respect to power, but the H-bridge decreases its THD_i rather drastically in comparison. This can be explained by understanding that the current ripple is dependent of the time period and input voltage, and not the output power. This means that with lower power, and thus lower current, the ripple part of the total current increases. For the hybrid multilevel inverter the ripples part of the total current do increase, but it is still a relative small part of the total current. If the test was to go to even lower power ranges, then the THD_i would eventually start to rise drastically for the hybrid multilevel inverter as well.

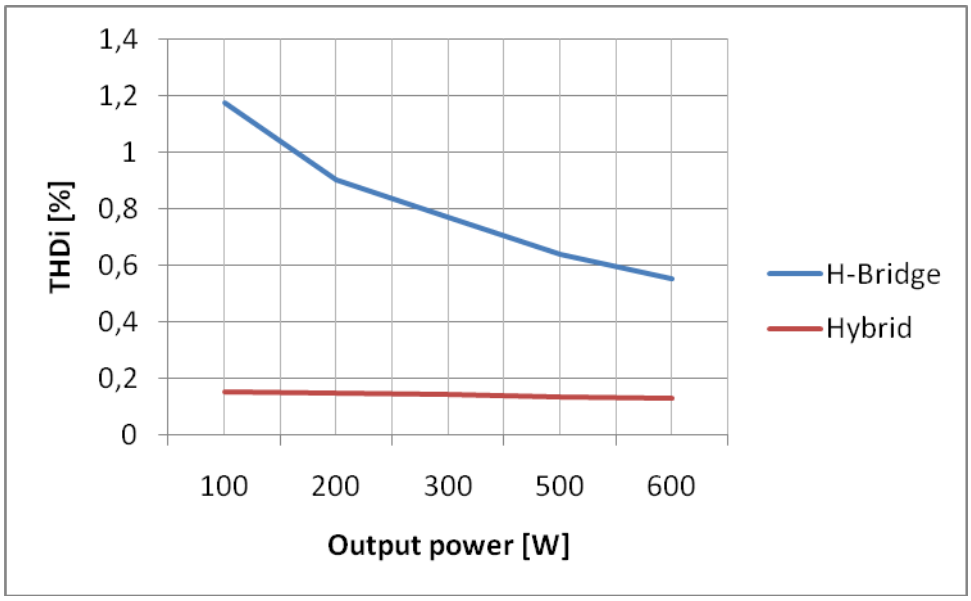

Figure 5-15: *THD*$_i$ versus output power for the H-bridge and hybrid multilevel inverter.

5.5 Selection of an inverter topology and further studies

Given the so far superiority of the hybrid multilevel inverter in the simulation in terms on both efficiency and harmonics, further studies will be on this inverter topology. Some more proper switches will be used. Further it was found that the filter was "too good", in sense that it filtered the harmonics to be far better than what was required. Subsequently its parameters could be lowered, and thereby lowering their production cost. This is especially important for the inductors as they are normally in specifically for the specific product, and are not mass produced.

5.5.1 THD$_i$

In subsection 5.4.1 it was found that the worst case scenario for the *THD*$_i$ was at high voltages and low output powers. Thus testing the inverter at its maximum allowable voltage and the minimum allowable output power should yield the highest possible *THD*$_i$. The minimum allowed power is hereby defined to 50 W.

After some testing, a satisfying filter was found, and its parameters may be found in

L_1	C	L_2	f_{res}	*Worst case* THD_i
50 µH	1.9 µF	50 Hµ	16 kHz	3.547 %

Table 5-3: New and optimalised filter for the multilevel hybrid inverter

A simulation was done, and the THD_i at this point was found to be 3.56 %, which is within the requirements.

5.5.2 Different switches

Now the focus will be on different switches and comparing these. First the difference between different switches at the bridge with low frequency and high voltage will be compared, then the same thing will be done with the other bridge.

High voltage switch selection

First three switches are selected for simulation on the high voltage bridge, the three selected switches are shown in Table 5-4 with some selected data from their respective datasheets. These three will for the sake of simplicity be called H1, H2 and H3 in this text. It can be noted that H1 has the lowest on resistance and H3 the highest, but the transition times is worst for H1 and better for the two others.

Parameter	*STY60NK30Z (H1)*	*SPB04N5C3 (H2)*	*M2N6759 (H3)*
V_{DS}	300 V	560 V	350 V
I_D	60 A	4.5 A	4.5 A
R_{on}	45 mΩ	0.95 Ω	1.5 Ω
Turn on delay time	50 ns	10 ns	30 ns
Turn off delay time	150 ns	70 ns	55 ns
Rise time	90 ns	5 ns	35 ns
Fall time	60 ns	5 ns	55 ns

Table 5-4: Some parameters from STY60NK30Z (STMicroelectronics), SPB04N50C3 (Infineon) and M2N6759 (Fairchild) taken from their respective datasheet.

The simulation was carried out using the switch which is called L2 in Table 5-5 and the results may be seen graphically in Figure 5-16 and the detailed data in Table 13-5.

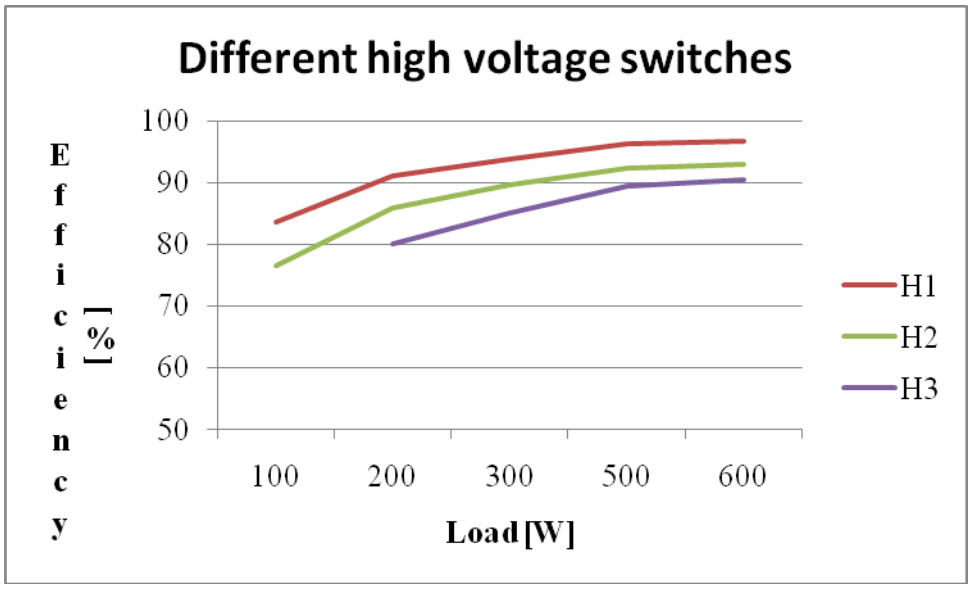

Figure 5-16: Efficiency – load characteristics for the switches of Table 5-4.

As can be seen in the figure, the on-resistance is the major factor when achieving a good efficiency for the high voltage bridge. Given these results the switch H1 is chosen for further use in this paper.

Low voltage switch selection

For the low voltage bridge three different switches was found and these is shown in Table 5-5, and still using H1. Here L1 has the highest on-resistance and L3 the lowest, but the transition related values is best for L2.

Parameter	*IRF223 (L1)*	*BSC520N15NS3 G (L2)*	*STB40NS15 (L3)*
V_{DS}	150 V	150 V	150 V
I_D	4 A	21 A	40 A
R_{on}	0.5 Ω	52 mΩ	42 mΩ
Turn on delay time	100 ns	7 ns	25 ns
Turn off delay time	40 ns	10 ns	45 ns
Rise time	60 ns	4 ns	85 ns
Fall time	60 ns	3ns	n/a

Table 5-5: Some parameters from IRF223 (Harris Semiconductor), BSC520N15NS3 G (Infineon), STB40NS15 (STMicroelectronics) taken from their respective datasheet.

The simulation results are shown graphically in Figure 5-17 and more in detail in Table 13-6. As clearly seen in the figure, the switch with the lowest on-resistance is not at all any good for this application, whereas L2 with the lowest transition related

values is the best choice, with L1 just below it, despite L1's high on-resistance – about ten times larger than that of the two other switches.

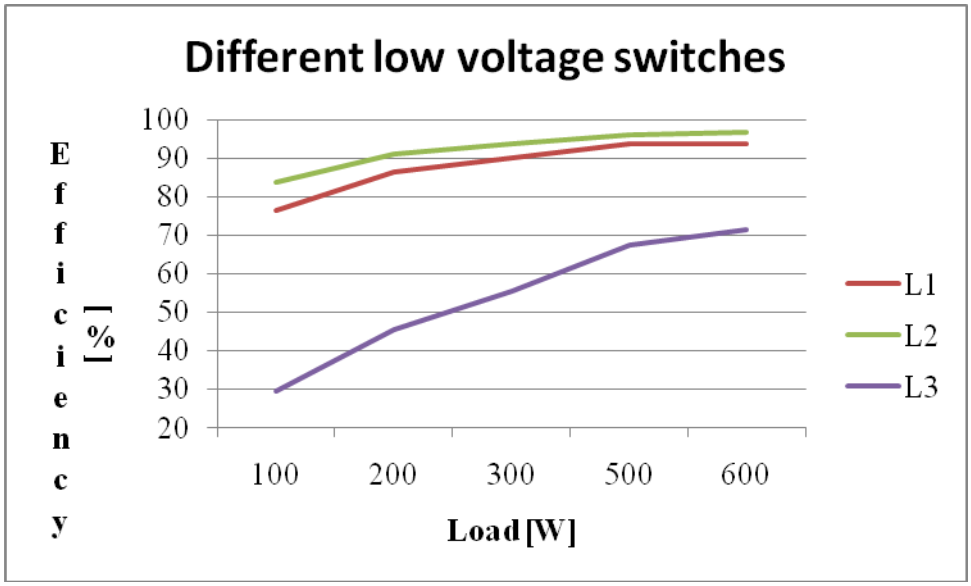

Figure 5-17: Efficiency – load characteristics for the switches of Table 5-5

L2 is subsequently chosen for the final converter.

An overview of all of the choices for the hybrid multilevel inverter may be seen in Table 5-6.

Switch for high voltage bridge	STY60NK30Z (H1)
Switch for low voltage bridge	BSC520N15NS3 G (L2)
L_1	50 µH
C	1.9 µF
L_2	50 µH

Table 5-6: Overview over the final component choice.

6 Discussion

Out of the five inverter topologies originally proposed, the H-bridge and the hybrid multilevel inverter was selected after a discussion about the pros and cons of all of the inverter topologies. This is mostly because both of them are robust technologies, and generally considered to have high efficiencies.

The wanted voltage output level was considered so small that there would be no specific need to boost the voltage, especially since even small PV modules can generate voltages of the about 400 V wanted for the H-bridge, which had the highest input voltage demand.

6.1 Comparison between the H-bridge inverter and the hybrid multilevel inverter

The H-bridge was then assumed to have the worst THD_i of the two inverter topologies, and a filter was design based on simulations on an unfiltered H-bridge inverter with a simple resistive load. A good filter was calculated, and the result gave a filter with L_1=0.76mH, C=3.6µF, L_2=0.20 mH and f_{res}= 3.0 kHz. In order to compare the two inverter topologies at similar basis, the same filter was used for the hybrid multilevel topology.

When all other factors are the same, it was simulated that the THD_i for the H-bridge inverter is between five and ten times as large as for the hybrid multilevel inverter. The reason for this drastically improvement of the THD_i is the increase of the number of output voltage levels.

Also with respect to efficiency the hybrid multilevel inverter scores better than the H-bridge inverter, as it is about 0.5 to 2 percent points more efficient. Due to an increased number of switching elements, the total on-resistance of the entire inverter system has to be larger for the hybrid multilevel inverter when all switching elements are of the same type. The reduction here is therefore associated with the switches' transition from on to off.

The H-bridge inverter excels in the fact that is requires only four elements for the DC to AC. However, this alone does not mean that the inverter is cheaper. The investigated hybrid multilevel inverter has twice the number of parts, but each of these may be selected to be of lower ratings than a comparable H-bridge inverter and thus the individual components may be cheaper for the hybrid multilevel inverter. In addition the hybrid multilevel's filter does not need to be that large, as the THD_i is lower. Especially for coils this is important, since these are often manufactured specifically on demand, unlike capacitors which are mass produced at many sizes. On the other side two separated PV modules are needed for the hybrid multilevel inverter, which would increase the overall initial cost of the system, without bringing a mentionable improvement of the MPPT.

Another interesting point is that the efficiency for output powers near the nominal output power was not that different for the two inverter topologies. This means that when the solar irradiation is expected to not vary that much, and thereby producing a more or less constant output power over large time periods, as the is quite normal in the parts of the world which are closer to the equator, then a single H-bridge might be more beneficial then a similar hybrid multilevel inverter.

A similar tendency is spotted when looking at the THD_i versus output power; the difference in THD_i between the H-bridge inverter and the hybrid multilevel inverter is not that large around nominal power. But reducing the filter sizes would also mean a reduction of the allowable output power, because a certain THD_i must not be exheed for all allowable power ranges, even though it is not expected to operate there at large time periods.

Even though the H-bridge may have its working areas, for the overall case, both the THD_i and efficiency concludes that the hybrid multilevel inverter should be chosen.

One criticism of these simulations and the author's decision is that although the two inverter topologies used the same switches, it can be argued that one could have built two parallel H-Bridges in order to take the same load as the hybrid inverter. Or one could use a set of two parallel mosfets at all places where the H-bridge now has only one mosfet. Now both of the inverters would have the same number of transistors, and the H-bridge would most likely have a much better efficiency, because the pure conduction losses would be better, both because the current has two paths in stead of just the one, but also because the lowered current through each mosfet would yield a smaller resistance in each individual resistance as well, since the mosfets would operate at lower temperatures. This would mean that the cooling elements of the mosfets could be smaller, thus reducing its price.

However, at one point one the analysis must come to an end, the author therefore felt that the above mentioned advantages of the hybrid multilevel inverter outweighs the eventual benefits of increasing the number of transistors in the single H-bridge.

6.2 Further investigation of the hybrid multilevel inverter

The comparison of different switches for the high voltage and low voltage bridge on the hybrid multilevel inverter concluded that for the high voltage bridge, it is most important to find a switch type with low on-resistance, as the losses associated with the transition itself is not that important. As for the low voltage bridge the opposite is the case; here low transition times are more important than the on-resistance.

Improvements of this inverter may then be made by changing the mosfets on the *low voltage bridge* with SiC JFets. The reason for this is that especially the transition

times of the SiC JFets are a lot better then for the mosfets, and therefore it would make the most sense to change the switches on this bridge.

SiC JFet models was unfortunately not available for the author, otherwise these would also be tried in the SPICE models.

It should be noted that even though the losses associated with the on-resistance are of less importance for the low voltage bridge in comparison to the switching losses, this is highly dependent on the modulated frequency. This thesis used a relative high frequency of 40 kHz, but if this frequency was set lower, perhaps to only 2 kHz, this might mean that the conduction losses through the mosfets would be the main loss factor. At low frequencies even the single H-bridge inverter may be better than the hybrid inverter for precisely the same reason.

Another possible problem, which has not yet been addressed, is that the output voltage has not yet been run through a regulator. In a weak grid the voltage command of the inverter may have to be less sinusoidal, in order to compensate for other electrical elements' un-sinusoidal behaviour. Given the already relative complexity of the PWM-generation in this unregulated simulation, it might prove difficult to find a potent regulator scheme for this topology. However, this thesis limits itself to an ideal grid at the output, so this question, although important, is considered out of scope. For grid connectable inverters of these power ratings, the problem with an un-sinusoidal net will anyway be limited, since these powers can not make a large impact on the general impact on the general power flow.

7 Conclusion

A good 230 V, 50 Hz, grid connectable PV inverter was designed with a power rating of 500 W and a nominal input voltage of 375 V. Its topology is two cascaded H-bridges, with one bridge running at a low voltage but high frequency and the second bridge is running at a high voltage but fundamental frequency. The final switches for this topology were found to be STY60NK30Z and BSC520N15NS3 G for the high and low voltage bridge respectively. This topology has more than 96 % efficiency when operating close to the nominal output power and input voltage.

The hybrid multilevel inverter requires more than one power source, which has its disadvantages, since the same power could without doubt come from a single larger power source. But its advantages regarding both distortion and efficiency led to the choice of the hybrid multilevel inverter.

It may also prove to be hard to find a good regulator for the inverter, since its PWM already at the unregulated case we have investigated is rather complex, and it will not be less complex when a regulator is in place.

7.1 Proposition for further work

The first thing that should be done, is to do an actual experiment with the inverter which was presented in this thesis, in order to verify whether the simulation results are close to the real-life results.

Then the power source should be modelled more like an actual PV module and an input capacitor to act as a power decoupling. This would also mean that the source would vary some over time, as natural phenomena like for instance clouds have impact on the produced power. For this to be done a good regulator needs to be developed, as the input voltage would vary.

Another suggestion for further work would be to use SiC JFet instead of mosfets. These transistors should give a better efficiency than the mosfets, but they are also likely to have a higher cost and might due to bottlenecks in the production not be practically implemented in a commercial inverter in the nearest time.

In this thesis it has only been understood that a MPPT is needed, and what it would require from the inverter, but an algorithm for finding the MPP should be either developed or found in a literature study.

Also the facts stated in this thesis are stated based on a relative small working area. The inverter should be tested at different switching frequencies and with different filters. The problem with the filter used in this thesis, is that the resistance there is more or less picked at random. In practice the computer model of the filter has to be adjusted according to what the real life measurements yields.

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9 Appendix – H-bridge equations

This appendix presents a derivation of equations needed to mathematically explain the H-bridge. The terminology is the same as used in section 4.1.

In order to find the voltage gain of a full-bridge converter, we can start by assuming that the wanted frequency (f_1) of the output signal is much lower than the switching frequency of the PWM trigger signal (f_s). This allows us to look upon the control voltage ($v_{control}$) as constant over one switching period (T_m). The sequence for one switching period may be seen in Figure 9-1, if we assume that $\hat{V}_{tri} > \hat{V}_{control}$.

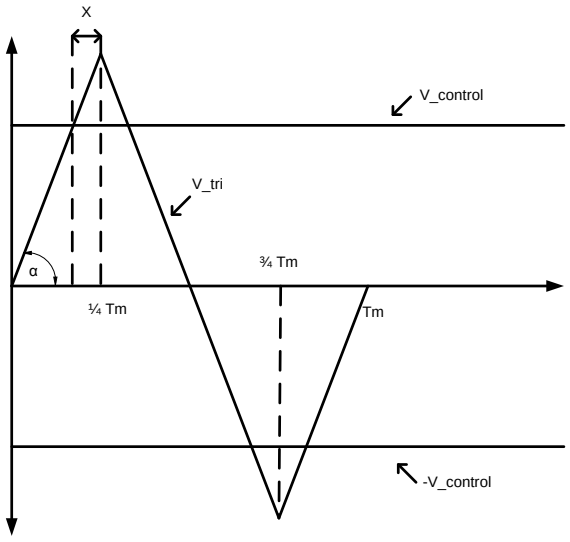

Figure 9-1: One switching period of PWM with unipolar switching if $f_1 >> f_s$.

Now the averaged voltage over one switching period may be found, V_{o0}.

$$V_{o0} = \frac{1}{T_m}\int_0^{T_m} v_{ao}(t)dt$$

$$= \frac{V_{in}}{T_m}\left(\int_0^{\frac{1}{4}T_m - x} dt + \int_{\frac{1}{4}T_m - x}^{\frac{1}{4}T_m + x} 0dt + \int_{\frac{1}{4}T_m + x}^{\frac{3}{4}T_m - x} dt + \int_{\frac{3}{4}T_m - x}^{\frac{3}{4}T_m + x} 0dt + \int_{\frac{3}{4}T_m + x}^{T_m} dt\right)$$

$$= \frac{V_{in}}{T_m}\left(\left(\frac{1}{4}T_m - x\right) + \left(\frac{3}{4}T_m - x\right) - \left(\frac{1}{4}T_m + x\right) + T_m - \left(\frac{3}{4}T_m + x\right)\right)$$

$$V_{o0} = \frac{V_{in}}{T_m}(T_m - 4x) \tag{5.4}$$

The *x* can readily be found by looking at the geometrics of the triangles:

$$\frac{4\hat{V}_{tri}}{T_m} = \frac{\hat{V}_{tri} - v_{control}}{x}$$
$$\Rightarrow x = \frac{(\hat{V}_{tri} - v_{control})T_m}{4\hat{V}_{tri}}$$

This yields:

$$V_{o0} = V_{in}\frac{v_{control}}{\hat{V}_{tri}} \tag{5.5}$$

$v_{control}$ would necessarily follow the its sine pattern over time, meaning that the instantaneous average would also follow this pattern, meaning that

$$v_{a1}(t) = V_{in}\frac{\hat{V}_{control}}{\hat{V}_{tri}}\sin(2\pi f_s t) \tag{5.6}$$

It is also possible to let $v_{tri}<v_{control}$. If $v_{tri} << v_{control}$ the output would be more and more a single square in each system period. The amplitude of the first harmonic can then be found using a mathematical engineering book:

$$\hat{V}_{o1} = \frac{1}{\pi}\int_{-\pi}^{\pi} vo(t)\sin t dt$$
$$= \frac{Vin}{\pi}(\left[\cos t\right]_{-\pi}^{0} - \left[\cos t\right]_{0}^{\pi})$$

$$V_{o1} = \frac{4}{\pi}V_{in} \tag{5.7}$$

This is the maximum output of this switch.

10 Appendix – SRBBI equations

Here follows a derivation of some equations needed to mathematically understand the series resonant buck-boost inverter. The stages and terminology are the same as in section 4.2.

Stage I

The current over the conductor can be found by using Kirchoff's voltage law:

$$V_{in} = V_{Lr} = L_r \frac{di_{Lr}}{d\tau}$$
$$i_{Lr}(t_{k0}) = 0$$
$$i_{Lr}(t) = \frac{V_{in}}{L_r} \int_{t_{k0}}^{t} d\tau = \frac{V_{in}}{L_r}(t - t_{k0})$$

The voltage can be found using Kirchoff's current law:

$$I_{Lfk} = -i_{Cr}(t) = -C_r \frac{dV_{Cr}}{d\tau}$$
$$I_{Lfk} \int_{t_{k0}}^{t} d\tau = -C_r \int_{V_{Cr}(t_{k0})}^{V_{Cr}(t)} dV_{Cr}$$
$$V_{Cr}(t) = V_{Cr}(t_{k0}) - \frac{I_{Lfk}}{C_r}(t - t_{k0})$$

Stage II

First we have the two initial conditions:

$$v_{Cr}(t_{k1})$$

$$\frac{dv_{Cr}(t_{k1})}{dt} = \frac{1}{C_r}(i_{Lr}(t_{k1}) - I_{Lfk})$$

Then we can use Kirchoff's voltage law to find our voltage:

$$\frac{d^2 v_{Cr}(t)}{dt} + \frac{1}{L_r C_r} v_{Cr}(t) = 0$$

$$\Rightarrow s^2 V_{cr} - s v_{Cr}(t_{k1}) - \frac{1}{C_r}(i_{Lr}(t_{k1}) - I_{Lfk}) + \frac{1}{L_r C_r} V_r = 0$$

$$V_{Cr} = \frac{s v_{Cr}(t_{k1}) + \frac{1}{C_r}(i_{Lr}(t_{k1}) - I_{Lfk})}{S_2 + \frac{1}{L_r C_r}}$$

$$\Rightarrow v_{Cr}(t) = v_{Cr}(t_{k1})\cos[\omega_r(t - t_{k1})] + Z_0(i_{Lr}(t_{k1}) - I_{Lfk})\sin[\omega_r(t - t_{k1})]$$

From this the inductor current may readily be found:

$$i_{Lr}(t) = I_{Lfk} + C_r \frac{dv_{Cr}(t)}{dt}$$

$$= I_{Lfk} - \frac{1}{Z_0} v_{Cr}(t_{k1})\sin[\omega_r(t - t_{k0})] + (i_{Lr}(t_{k1}) - I_{Lfk})\cos[\omega_r(t - t_{k0})]$$

Stage III

The inductor current has been cut thanks to the thyristor, so

$$i_{Lr}(t) = 0$$

And the voltage can be found in a similar manner as in stage III

$$V_{Cr}(t) = V_{Cr}(t_{k2}) - \frac{I_{Lfk}}{C_r}(t - t_{k2})$$

11 Appendix – Hybrid multilevel inverter: Flow chart of the logical driver

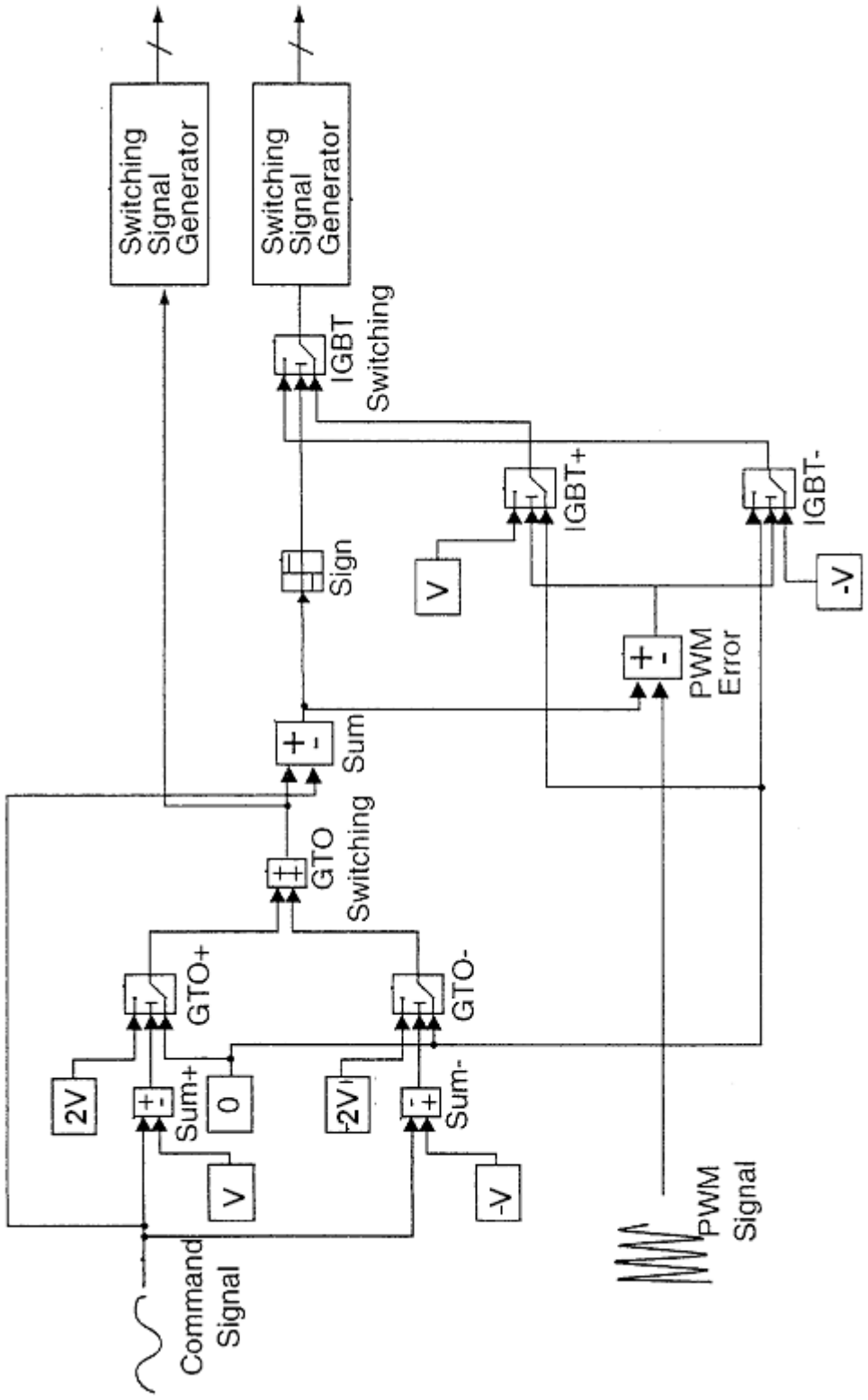

Figure 11-1: Flowchart of the switching scheme of a hybrid multilevel inverter. Source: [17]

12 Appendix – Flyback converter with PWM DC-AC inverter

This appendix presents some derivations of equations needed to get a mathematical understanding of the flyback inverter, the H-bridge part of this inverter has already been explored in (Appendix 9).

First the time starts at t_0 when S_{PV} is turned on, and is kept on until t_1 is reached. In this time period the flux in the transformer ($\Phi(t)$) may expressed as

$$\Phi(t) = \Phi(t_0) + \frac{V_{PV}}{N_1} t; t_0 \leq t < t_1 \tag{5.8}$$

where N_1 is the number of windings on the primary side. This is because of no current flows through the secondary transformer side, due to D_{RECT}, meaning all of the energy is stored magnetising the transformer core.

When S_{PV} is turned off, the diode on the secondary side allows conduction, and the flux is tapped from the secondary winding:

$$\Phi(t) = \Phi(t_1) - \frac{V_O(t - t_1)}{N_2}; t_1 \leq t < t_2 \tag{5.9}$$

where N_2 is the number of windings on the secondary side. From these two equation we get:

$$\Phi(t_2) = \Phi(t_0) + \frac{V_{PV}}{N_1} t_1 - \frac{V_{DC}}{N_2}(t_2 - t_1) \tag{5.10}$$

In steady state $\Phi(t0) = \Phi(t2)$, which leads to:

$$
\begin{aligned}
V_{DC} &= \frac{N_2}{N_1} V_{PV} \frac{t_1}{t_2 - t_1} \\
&= \frac{N_2}{N_1} V_{PV} \frac{D}{(1-D)} \\
&= a V_{PV} \frac{D}{(1-D)}
\end{aligned}
\tag{5.11}
$$

13 Appendix – Simulation results

Here the numerical values for the different simulations are listed. The simulations are all from chapter 5.

Input voltage	Switch losses [W]	Efficiency [%]	Input power [W]	THD_i [%]
330 V	13.762	97.3	509.98	0.4876
375 V	16.152	96.83	509.22	0.6375
400 V	17.593	96.62	521.17	0.6936
450 V	20.226	96.14	524.36	0.8199

Table 13-1: The effect that the input voltage has on losses, H-Bridge inverter. Output power was 500 W. All switches are SPA11N60C3.

Input voltage	Switch losses [W]	Efficiency [%]	Input power [W]	THD_i [%]
330 V	9.7233	97.86	505.14	0.1001
375 V	10.777	97.88	506.24	0.1299
400 V	11.408	97.74	506.89	0.1331
450 V	12.704	97.50	508.23	0.1276

Table 13-2: The effect that the input voltage has on losses, Hybrid multilevel inverter. Output power was 500 W. All switches are SPA11N60C3.

Output power [W]	Switch losses [W]	Efficiency [%]	Input power [W]	THD_i [%]
600	20.367	96.75	627.37	0.5542
500	16.152	96.83	509.22	0.6375
300	11.309	96.33	307.8	0.7725
200	10.025	95.18	208.82	0.9007
100	9.2655	91.51	109.2	1.177

Table 13-3: The effect that the output load has on losses, H-Bridge. Input voltage was 375 V. All switches are SPA11N60C3.

Output power [W]	Switch losses [W]	Efficiency [%]	Input power [W]	THD_i [%]
600	12.531	97.91	599.68	0.1299
500	10.777	97.88	506.24	0.1351
300	8.0092	97.36	304.53	0.1442
200	7.1475	96.52	205.52	0.1476
100	6.6216	93.76	106.16	0.1500

Table 13-4: The effect that the output load has on losses, Hybrid multilevel inverter. Input voltage was 375 V. All switches are SPA11N60C3.

Load [W]	STY60NK30Z (H1)		SPB04N5C3 (H2)		M2N6759 (H3)	
	Efficiency [%]	Input power [W]	Efficiency [%]	Input power [W]	Efficiency [%]	Input power [W]
100	83.69	122.87	76.55	132.15	n/a	n/a
200	91.05	225.75	85.94	234.58	80.05	252.99
300	93.77	328.63	89.59	336.25	85.11	354.28
500	96.23	533.06	92.38	539.17	89.45	553.26
600	96.73	636.02	93.02	639.87	90.42	651.81

Table 13-5: Efficiency for different switch types in the high voltage bridge and at different loads. The switch type at the low voltage bridge was BSC520N15NS3G for all tests. Total input voltage was 375 V.

Load [W]	IRF223		BSC520N15NS3 G		STB40NS15	
	Efficiency [%]	Input power [W]	Efficiency [%]	Input power [W]	Efficiency [%]	Input power [W]
100	76.52	133.69	83.69	122.87	29.51	348.46
200	86.36	235.72	91.05	225.75	45.37	453.06
300	90.06	337.33	93.77	328.63	55.50	555.18W
500	93.81	538.58	96.23	533.06	67.53	759.7
600	93.71	638.62	96.73	636.02	71.36	862.13

Table 13-6: Efficiency for different switch types in the low voltage bridge and at different loads. The switch type at the high voltage bridge was STY60NK30Z for all tests. Total input voltage was 375 V.

14 Appendix – Datasheets

The switches used in this the simulations in chapter 5 have datasheets which may be found in the electronic appendix named “switches.zip”.