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Stability Investigation of an Advanced Electrical Rail Vehicle

Investigation of the Effect of Nonlinearity Introduced by a Switching Model of an Advanced Electrical Rail Vehicle on the General Performance and The Stability Limits

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Problem Description

In this work an investigation of stability is going to be performed using a detailed model of an electrical locomotive developed in EMTDC/PSCAD. The stability limits obtained using this model are going to be compared to those limits obtained by using a simplified model suggested in previous work [1]. The effects of the non linearity introduced by including a detailed switching model of the inverter are going to be assessed by observing the general performance of the system and a proposal for improving such performance will be attempted. In addition to this, influence of the variation of different system parameters such as operating frequency of the converter are also going to be investigated to assess the effects of the non linearity neglected in the simplified model on the general performance of the real system and on the stability limits.

Reference

[1] Danielsen, S., Fosso, O.B., Molinas, M., Suul, J.A. & Toftevaag, T., Simplified models of a single-phase power electronic inverter for traction power system stability analysis – development and evaluation, Submitted to Electric Power System Research in 2008.

Assignment given: 19. January 2009
Supervisor: Marta Molinas, ELKRAFT

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PREFACE

This report comprises the final Master thesis, and documents the work during the last semester of my education at the Department of Electrical Power Engineering, NTNU. I was part of the two years International masters program for MSC in Electrical Power Engineering. The two years in NTNU has been enjoyable years of interesting studies, hard work, personal development and technical progress. The thesis work is done in collaboration with Jernbaneverket (The Norwegian Railway Administration); Where Steinar Danielsen has been the main contact.

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First and foremost I offer my sincerest gratitude to my supervisor, Professor Marta Molinas, who has been supporting me with her enormous knowledge and ideas. I appreciate her vast knowledge and hard work. I also would like to mention the paper we wrote in connection to this thesis work which will be presented on the EPE2009 conference is a success because of her initiative idea, guidance and encouragement.

I gratefully acknowledge Steinar Danielsen (PHD), my co-supervisor in the thesis work, I am very much honored to have him as a co-supervisor and I would like to thank him for his valuable guidance, comments and advice throughout the thesis work.

I would also pass my very special thanks to my family for the support and encouragement they provided me throughout my entire life.

Last but not least I want to thank all my classmates, friends and everybody who has supported me directly or indirectly for the accomplishment of this thesis work.

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July 2009

MOTIVATION

An advanced electrical rail vehicle is modeled using the simulation software SIMPOW for stability analysis purpose [1]. The system in SIMPOW is modeled with three major simplifications:

- PWM switching: The switching of pulse width modulated (PWM)-switch model is not included, instead the converter is represented by an average representation of the converter by neglecting the detailed semiconductor switching effect on the system.
- Inverter and DC-link structure: There may be several DC-links per vehicle and several line and motor inverters in parallel to each DC-link in real life scenario. In this model all the vehicle's DC-links are aggregated into one large one.
- A simple representation of the motor side is included. A simplified load representation is assumed in the proposed model by connecting the DC-link directly to a load. However, the influence of the motor side and its control system cannot always be neglected as it might be a source of instability

In order to make the model closer to the real life system there is a need to reduce these simplifications. In this thesis a detailed model of advanced electric rail vehicle which reduces one of the simplifications of the SIMPOW model will be modeled. A detailed electrical rail vehicle which includes the pulse width modulated (PWM)-switch of the line inverter will be modeled with the simulation software EMTDC/PSCAD. In order to see the effect of this detailed semiconductor switching on the general performance of the model, an average model will be compared and the effects of the non-linearity will be analyzed in this thesis work.

The simulation software tool EMTDC/PSCAD is chosen for this thesis work for three basic reasons:

- A simple user interface: PSCAD (Power Systems CAD) is a powerful and flexible graphical user interface to the world-renowned EMTDC solution engine. PSCAD enables the user to schematically construct a circuit, run a simulation, analyze the results, and manage the data in a completely integrated, graphical environment. Online plotting functions, controls and meters are also included, so that the user can alter system parameters during a simulation run, and view the results directly.

- Accepted by power electronic engineers in the energy conversion group of Norwegian University of Science and Technology (NTNU).The EMTDC/PSCAD tool is used in the energy conversion group for detail modeling of semiconductor switching.

- To make possible communication between the two electrical power engineering groups in NTNU: Normally the Power system group in NTNU uses the traditional simulation software tool SIMPOW, however the energy conversion group uses the EMTDC/PSCAD for detail system modeling of the power electronics components and semiconductor switching, with the purpose of making a possible communication between the two group there is a need to re-model the SIMPOW model using the simulation software EMTDC/PSCAD. In this case the model will be accessible both in SIMPOW and EMTDC/PSCAD simulation software's for the purpose of further study and research discussions.

- The average model is modeled as proposed in [1] without including (PWM)-switch of the line inverter. The PWM is simplified into a controlled current source that calculates the DC-current based on the AC-side power divided by the DC-link voltage, at the converter DC-side of the model. In the converter AC-side the PWM is simplified by a controlled voltage source which is controlled by the reference AC-voltage from the inverse park transformation block output.

INVESTIGATION OF THE EFFECT OF NON-LINEARITY INTRODUCED BY A SWITCHING MODEL OF AN ADVANCED ELECTRICAL RAIL VEHICLE ON THE GENERAL PERFORMANCE AND THE STABILITY LIMITS

ABSTRACT

Reducing grid harmonics and increasing grid stability are both major issues for the operation of rail vehicles. For stability investigation of complex power systems, simplified system models are in need in order to reduce the model complexity and the simulation time. In this thesis work the effect of modelling a voltage source converter (VSC) for traction power system with and without the detailed pulse width modulated (PWM)-switch model is modeled as shown in Figure 1 in PSCAD and analyzed, more focus is given for the circled area of Figure 1.

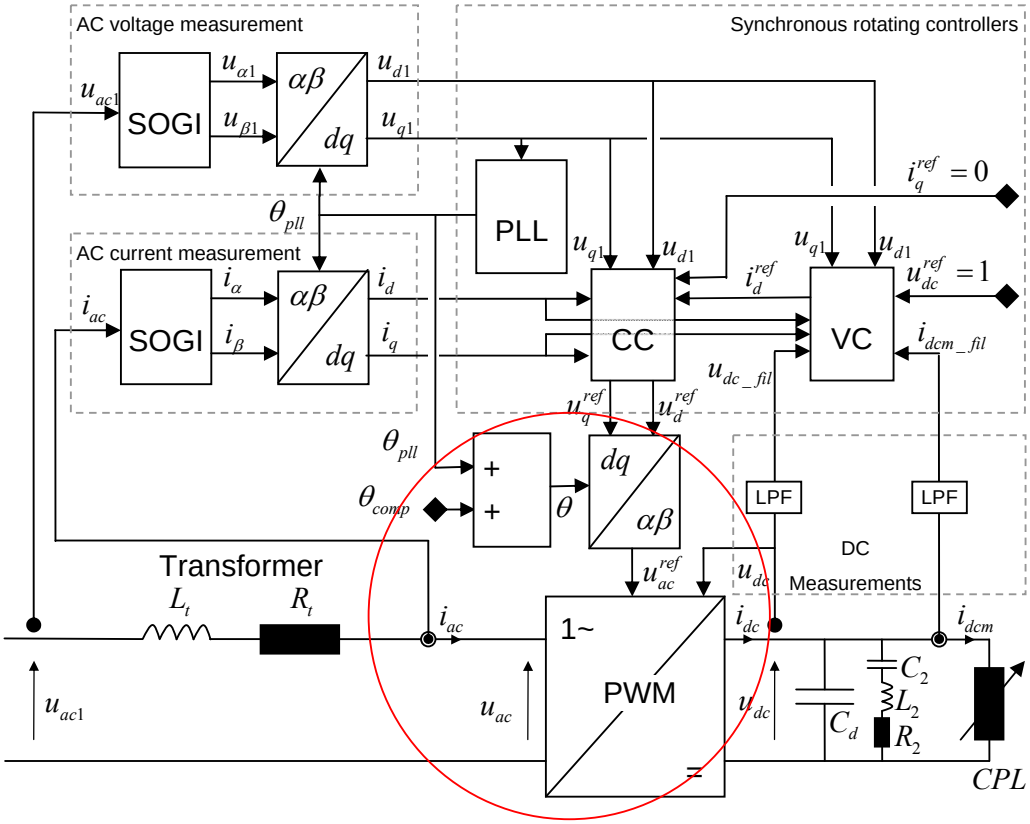

Figure 1 Single line equivalent circuit and block diagrams of the model

Effect of different operating conditions for the switching model on the harmonic content of the system is also analyzed. The same disturbance is imposed for the two models and the low frequency oscillation of the DC- link voltage response is compared and analyzed. The effect of semiconductor switching on the stability limit of the system is also investigated. Furthermore, the performance of a PWM time delay compensation technique during transient is analyzed.

The result shows that in the model including the switching the DC- link voltage oscillation is damped and has a better stability margin compared to the average model. In the detailed switching model a converter loss is included while in the average model a no loss ideal case scenario is considered.

As far as the switching harmonic is considered, the switching model with an operational condition of a high switching frequency and a switching frequency with an integer multiple of the fundamental frequency has a low harmonic content on the system compared to the operating condition of a low switching frequency which is not integer multiple of the fundamental frequency. A unipolar voltage switching technique has also a tremendous advantage over the bipolar voltage switching technique as far as this harmonic content in the system is concerned. Using a unipolar voltage switching technique reduces the harmonic content in the overall railway system.

For triangular carrier modulators, an average time delay from the reference voltage to the actuated PWM terminal voltage of half the switching frequency is assumed .The delay in DC-link voltage control loop caused by the switching dead-time effect was improved by compensation of dead-time in the inverse-park transformation block of the control loop. The comparison of the compensated and non-compensated model proves that the compensated model is better in terms of the overshoot of amplitude of transient.

1. BACKGROUND

1.1 ELECTRIC TRACTION SYSTEM

In the latest years there has been an enormous acceleration in railway traction development. This has run in parallel with the development of power electronics and microprocessors. What have been the accepted norms for the industry for, sometimes, 80 years, have suddenly been thrown out and replaced by fundamental changes in design, manufacture and operation. Many of these developments are highly technical and complex.

The main task for an electrical locomotive is to convert electrical energy delivered from the overhead contact line into mechanical energy required from the traction motors in order to run the train. Electrical traction system has several advantages when compared to traditional diesel system. To mention some: electrical traction has lower energy cost, preservation of limited oil reserves, environmental friendly operation, possibility of energy recovery when braking, no need of carrying the power generator on the vehicle unit (less weight), high service speed over 200kph and heavy mass transit only viable with electric traction , lower maintenance cost, and so on. However traction systems have also high initial cost for catenaries and power supply networks. [2]

1.2 POWER SUPPLY OF RAIL VEHICLE

The electric railway needs a power supply that the trains can access at all times. It must be safe, economical and user friendly. It can use either DC or AC supply. Transmission of power is always along the track by means of an overhead wire, Figure 2, or at ground level, using an extra, third rail laid close to the running rails. AC systems always use overhead wires, DC can use either an overhead wire or a third rail; both are common. Both overhead systems require at least one collector attached to the train so it can always be in contact with the power. Overhead current collectors use a pantograph. The return circuit is via the running rails back to the substation. The running rails are at earth potential and are connected to the substation.

Figure 2 shows a connection of the power supply overhead contact line and the rail vehicle by means of the pantograph. Each subsection is isolated from its neighbor by a section insulator in the overhead contact as shown in this picture. The subsections can be joined through special high speed section switches.

Figure 2 Picture of overhead contact line

Since 1992 in most Europe including Sweden, Norway, Germany, Switzerland and Austria a single phase 15KV and 16 2/3Hz alternating-current system for long distance railway has been used. [2]

Modern rail traction vehicles operating at the Central European single-phase 16 2/3Hz overhead line employ a four-quadrant converter at the line side to feed a DC link, to which the machine-side inverter is connected, feeding the traction motors [3]. For a project aiming detail modeling of the traction system a detail semiconductor switching model is needed.

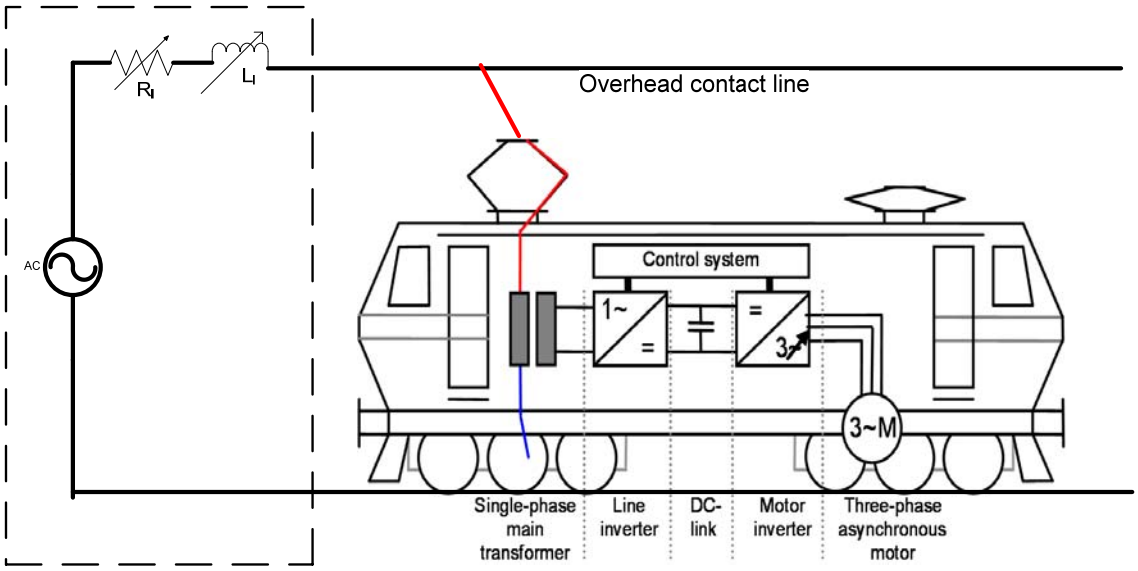

Figure 3 Schematic representation of electric rail vehicle including substation and locomotive.

In a single-phase AC traction power system, the vehicle interface to the rest of the power supply is a power electronic converter as shown as the line inverter in **Figure 3**. Such a vehicle is often called an advanced electrical rail vehicle or an inverter vehicle.

The substations and the variable position of the locomotive along the railway line are represented by a voltage source behind variable L_l and R_l , The line parameters in the PSCAD model are modeled with a standard resistance and inductance model in the PSCAD library , However for the purpose of stability investigation this parameters of the line are calculated by using the required line length and the fundamental frequency of the system, this parameters are altered manually on the system model by setting the calculated values of the inductance and resistance values in the model.

In this thesis work a single phase 60km line, 16.5KV and 16 2/3Hz AC-system advanced electrical rail vehicle with its advanced control system will be modeled using EMTDC/PSCAD as suggested in the previous work [1]. The thesis work is intending to study the factors or operating conditions of the system that reduces grid harmonics and effects of semiconductor switching on the general performance of the low frequency oscillation on stability studies.

The switching model in PSCAD will be more detailed since it comprises the detail semiconductor switching. The average model in PSCAD, which is the exact duplicate of the average model suggested in [1], will be compared and analyzed with the detail switching model for the purpose of investigation of the effect of non-linearity introduced by a switching model of an advanced electrical rail vehicle on the general performance and for the evaluation of the stability limits associated with low frequency power oscillations stability studies.

In section one of this thesis work the background studies of a general electric rail vehicle will be explained. Section 2 presents an introduction of this thesis work in short. Section 3 gives the system model description. The detail PSCAD system modeling will be presented in section 4 of this thesis work. Section 5 explains about the dead time compensation technique and finally the simulation results and the conclusion will be presented in section 6 and section 7 of this thesis work report.

2. INTRODUCTION

Modern electrical locomotives are equipped with a number of power electronic equipment and advanced digital control technology. This improves the performance of the locomotive, but also introduces a lot of new dynamical phenomena of interaction with the railway power supply. For the latest years, the topic of poorly damped low frequency oscillations has been in focus. In some cases these oscillations have resulted in instability of the traction power system [5].

In order to study the interaction between the power electronic component and the rest of the railway traction power system, models close to reality have to be developed [6], [7]. In general, power system modelling includes a number of simplifications in order to reduce the model complexity and the simulation time. A typical simplification is to neglect the impact of the semiconductor switching during dynamical stability studies [1]. However in this thesis work the effect of the presence of semiconductor switching, which is the main source of harmonics and nonlinearity in the power system, is considered to evaluate possible impacts on the low frequency behaviour of the system stability studies.

A VSC for traction power system with and without the detailed PWM switching model of an electrical locomotive using EMTDC/PSCAD simulation tool is made based on the simplified (average) model suggested in [1].The detailed model takes into consideration the non-ideal pulse width modulated (PWM)-switch model with the purpose of evaluating the proposed averaged model accuracy, using the refined model for semiconductor devices, to observe the low frequency oscillation response.

The main advantage of the proposed switching model is that it takes into account the nonlinear effects of power devices and makes it possible to estimate the dissipated power in the different circuit devices and to evaluate the effect of the semiconductor devices on the general performance of the system low frequency behavior.

The averaged model is limited since the semiconductor devices nonlinearities and the simple switching and static characteristics of these devices are neglected. In this detailed semiconductor switching model, a non-ideal pulse width modulated switch model are

considered .Moreover in this thesis work, the compensation technique proposed in [8] is used to compensate for the delay caused by the dead-time of the switching devices.

3. SYSTEM MODEL DESCRIPTION

The system under study for this thesis work is a single-phase PWM inverter connecting an AC-system and a DC-system in rail vehicle application as shown in Figure 4 .

The AC- system includes:

- An ideal voltage source for 16 2/3 Hz having amplitude of $\sqrt{2} \cdot 16.5$ kV
- A 60 km overhead contact line having impedance of (0.19+j0.21) Ω/km and
- The vehicle main 15 kV/1.558 kV step down transformer.

The DC-system reflects the vehicle DC-link with:

- The DC-link capacitance C_d of 40 mF,
- The second harmonic resonance tank C_2, L_2 and R_2 tuned on 33.4 Hz in order to reduce the second harmonic ripple given by the single-phase system power pulsations and
- A constant power load (*CPL*) drawing a current i_{dcm} (see equation (1)) as a simplified equivalent for the motor side.

$$i_{dcm}(t) = P_m^{ref}(t) / u_{dc}(t) \tag{1}$$

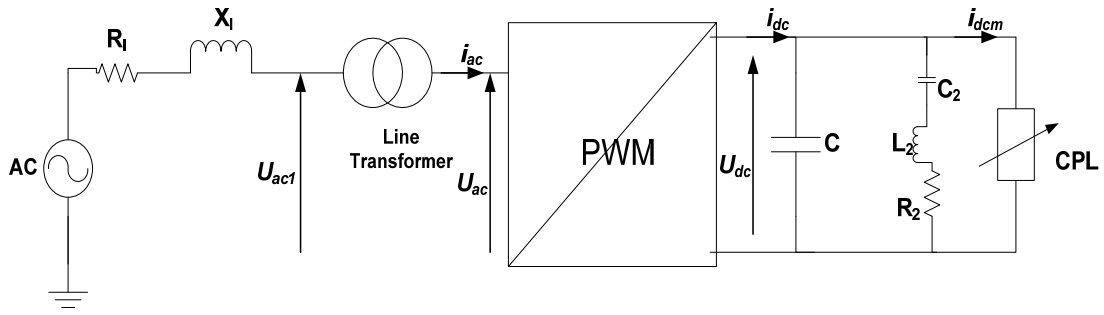

Figure 4 Schematic representation of the electrical system under investigation.

The control system as shown in Figure 1 for the line inverter consists of the synchronization controller which is a phase locked loop (*PLL*) that constantly tracks the phase of the line

voltage u_{ac1} for orientation of the direct (*d*) and quadrature (*q*) axis reference frame in which the other controllers rotate.

A second-order generalized integrator (*SOGI*) [9] is used for generation of an artificial orthogonal voltage as input to the *PLL*. And the SOGI is well applied to a filter measurement for the control system by filtering the line current and voltage of the switching model.

The DC-link voltage proportional-integral controller *VC* compares the measured DC-link voltage u_{dc_fil} to its constant reference and together with the fed forward measured motor current i_{dcm_fil} calculates the active current reference i_{dref} for the current controller based on the ratio between the measured DC and AC voltages, u_{dc_fil} and u_{d1} respectively (see Figure *1*).

The AC-current proportional-integral controllers (*CC*) compare the measured *d*- and *q*-axis (i_d and i_q) to the respective active and reactive current references i_d^{ref} and i_q^{ref}. The two axes are decoupled over the transformer impedance X_t in order to allow independent control of active and reactive power. The reactive power is controlled to be zero at the vehicle transformer line side, i.e. i_{ac} in phase with u_{ac1}.

A detailed switching model of single-phase PWM inverter with a triangular carrier frequency of 250Hz and a reference voltage of u_{ac}^{ref} with unipolar voltage switching technique is included for the switching model. In railway application system it is common to use the unipolar voltage switching. This type of switching has the advantage of doubling the effective switching frequency as far as the output harmonics are concerned, compared to the bipolar switching scheme [2], [4] .

In the average model, Figure 5, the PWM is simplified into a controlled current source that calculates the current based on the AC-side power divided by the DC-link voltage, at the converter DC-side of the model, v_{dc} as shown in equation (2).

$$i_{av}(t) = [i_{ac}(t) * u_{ac}(t)] / u_{dc}(t) \tag{2}$$

In the converter AC-side the PWM is simplified by a controlled voltage source which is controlled by the reference AC-voltage from the inverse park transformation block output u_{ac}^{ref} .

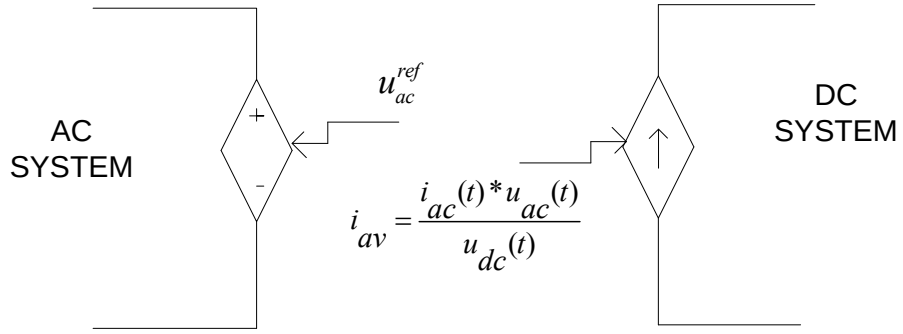

Figure 5 Schematic representation of the PWM in the average model.

In addition, a *SOGI* is used for measurement of the line current i_{ac} as well. First-order low-pass filters are used for measurement of the u_{dc} and i_{dcm} .

4. SYSTEM MODELLING IN PSCAD

4.1 SYNCRONIZATION SYSTEM

1) PLL for Synchronization of θ

A phase-locked loop (PLL) is a synchronization control system that generates a signal that has a fixed relation to the phase of a reference signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. The PLL block diagram shown in Figure 6 consists of three basic functional blocks which is the phase detector (*PD*), a loop filter or proportional-plus-integral controller (*LF*) and a voltage controlled oscillator *(VCO)* [1], [10].

The PLL constantly tracks the phase of the line voltage u_{ac1} for orientation of the direct (*d*) and quadrature (*q*) axis reference frame in which the other controllers rotate.

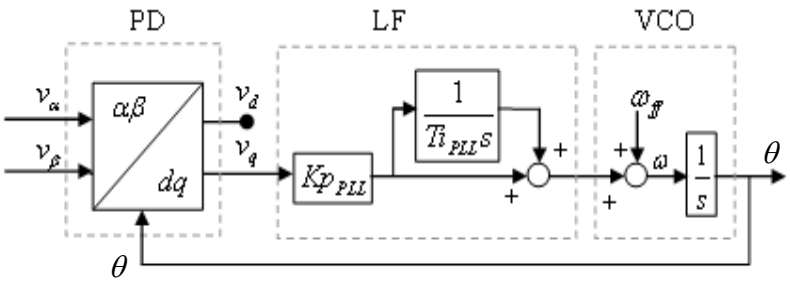

Figure 6 Block diagram of the PLL.

The phase detector is a circuit capable of delivering an output signal that is proportional to the phase difference between its two input signals. In the scenario shown in Figure 6 the *PD* compares the phase of the input reference signal to be tracked, $\omega t + \theta_0$, to the phase given by the voltage controlled oscillator $(VCO), \theta$. The two input signals v_α and v_β are orthogonal (i.e. 90 degrees shifted in phase) and expressed as in equation (3).

$$\begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} = U \begin{bmatrix} \cos(\omega t + \theta_0) \\ -\sin(\omega t + \theta_0) \end{bmatrix} \tag{3}$$

Where ω is the instantaneous angular frequency of the input signal.

The phase detector block is modelled in PSCAD as equation 4, which is the αβ to dq transformation block for the voltage and current in Figure 1, is the so called Park transformation.

$$\begin{bmatrix} U_{d1} \\ U_{q1} \end{bmatrix} = \begin{pmatrix} \cos(\theta_{pll}) & \sin(\theta_{pll}) \\ -\sin(\theta_{pll}) & \cos(\theta_{pll}) \end{pmatrix} \begin{bmatrix} U_{a1} \\ U_{b1} \end{bmatrix} \tag{4}$$

The transform from one complex coordinate system to another complex coordinate system, creates a local reference frame rotating with the fundamental frequency given by the *VCO* as shown in equation (3). In this rotating frame, the direct axis component U_{d1} should be in phase with the fundamental of the input signal $U_{\alpha 1}$ as U_q is controlled to zero by the *PLL*. This means that the quadrature axis component U_q should be equal to zero, which is taken care of the proportional-integral effect of the loop filter (*LF*).

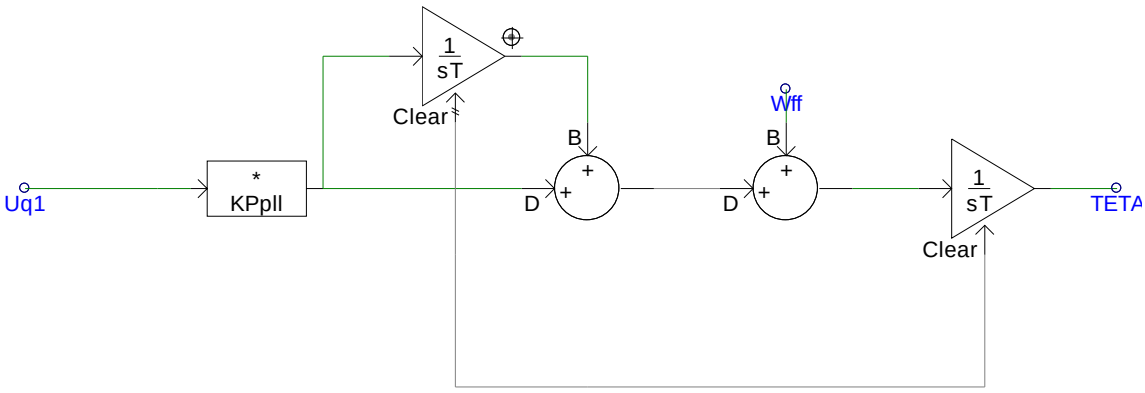

Figure 7 PLL Model as modeled in PSCAD

Figure 7 shows the PLL model as implemented in PSCAD. When modeling the PLL Integrator in PSCAD an integrator reset that will avoid problems due to integrator windup is

included. The frequency $\omega_{ff} = 2\pi f_1$ added in the *VCO* is a feed forward of the fundamental of the input signal U_α in order to initialize the PLL and reduce the pull-in time. The phase output from the *PLL* is often only running from 0 to 2π (modulus 2π) as it else will cause overflow in the control system as times goes towards infinity.

2) Second Order Generalized Integrator (SOGI)

In a single-phase system in the stationary reference frame, no orthogonal signal to the time domain voltage or current exists. Different methodologies for creating an artificial perpendicular signal has been suggested [11], but a second order generalized integrator (*SOGI*) [9] is used in the model proposed in [1]. The block diagram of the *SOGI* proposed in [1] is shown in **Figure 8** and the transfer function is shown in equation (5).

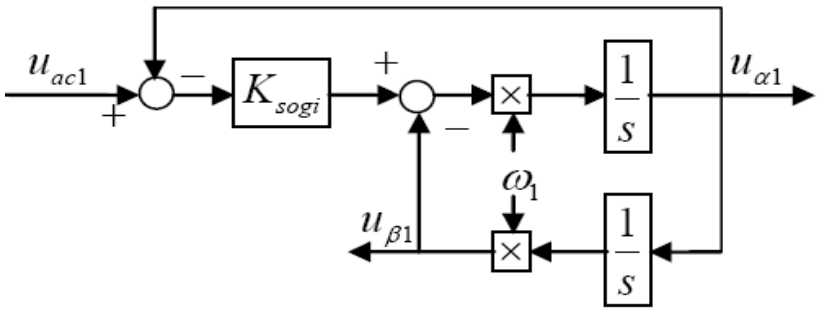

Figure 8 Block diagram of the SOGI.

$$H_{SOGI} = H_\alpha(s) = \frac{U_{\alpha 1}(s)}{U_{ac1}(s)} = \frac{K_{SOGI}\omega_1 s}{s^2 + K_{SOGI}\omega_1 s + \omega_1^2} \tag{5}$$

Where ω_1 is defined as the fundamental angular frequency of the system.

The SOGI model in PSCAD which is represented by the SOGI block in Figure 1 both for the current and the voltage is modeled in PSCAD as shown in **Figure 9** and **Figure 10**

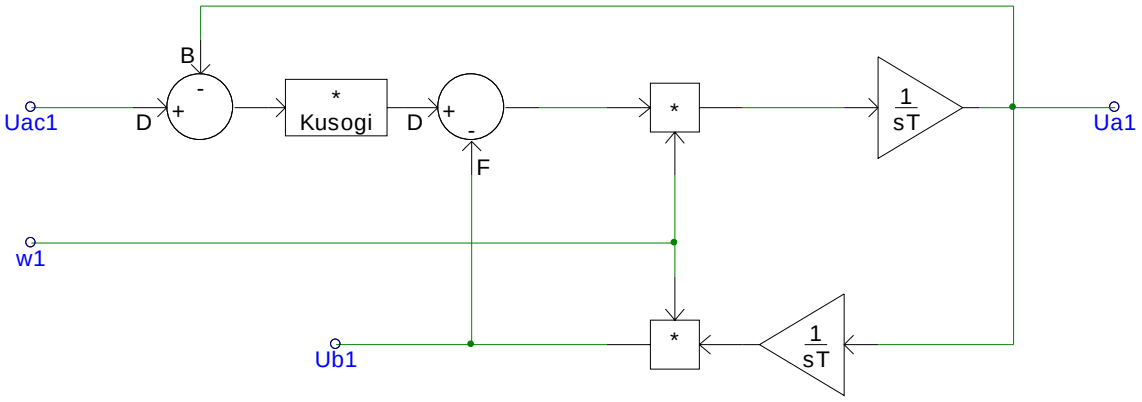

Figure 9 SOGI Model for the voltage in PSCAD

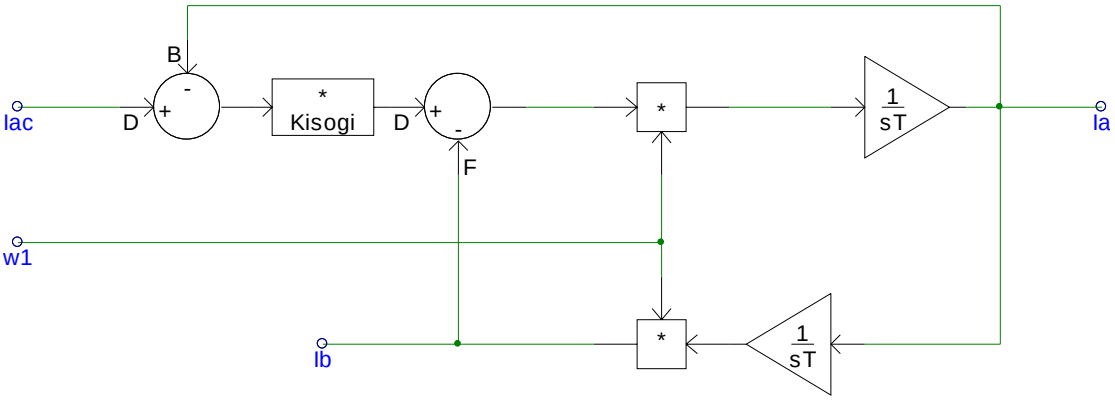

Figure 10 SOGI modell for the current in PSCAD

4.2 VOLTAGE CONTROLLER

The voltage controller block labeled as VC on Figure 1 controls the active power flow keeping the DC-link voltage u_{dc} to its reference value $u_{dc}^{ref} = 1\,\text{pu}$ by calculating the reference current i_d^{ref} for the current controller (*CC*). The voltage controller is a proportional-integral controller (*PI*) as shown in the block diagram of Figure 11.

The filtered and measured motor current i_{dcm_fil} is fed forward and added to the regulator output ξ resulting in a needed DC current i_{dc}^{ref} to close the voltage deviation. This DC current is recalculated to a needed AC current given by the ratio between measured DC-link voltage u_{dc_fil} and the line voltage u_{d1} which is responsible for decoupling between DC voltage and AC voltage. This is the direct axis component in the local rotating dq-system, i.e. the amount of current needed in phase with the line voltage u_{ac1}.

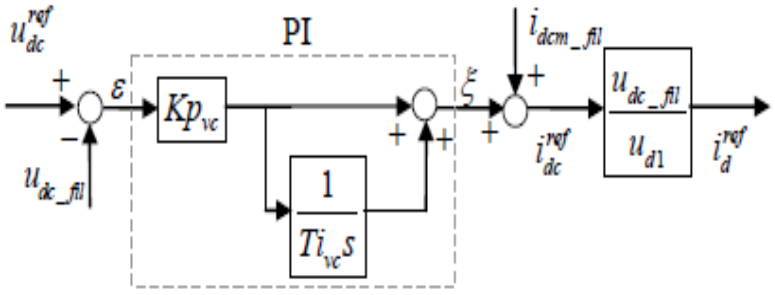

Figure 11 Block Diagram for DC link Voltage Controller.

The voltage controller is modeled in PSCAD as shown in Figure 12 . This model is the exact duplication of the block diagram in Figure 11 which is the proposed model for the voltage controller in [1].

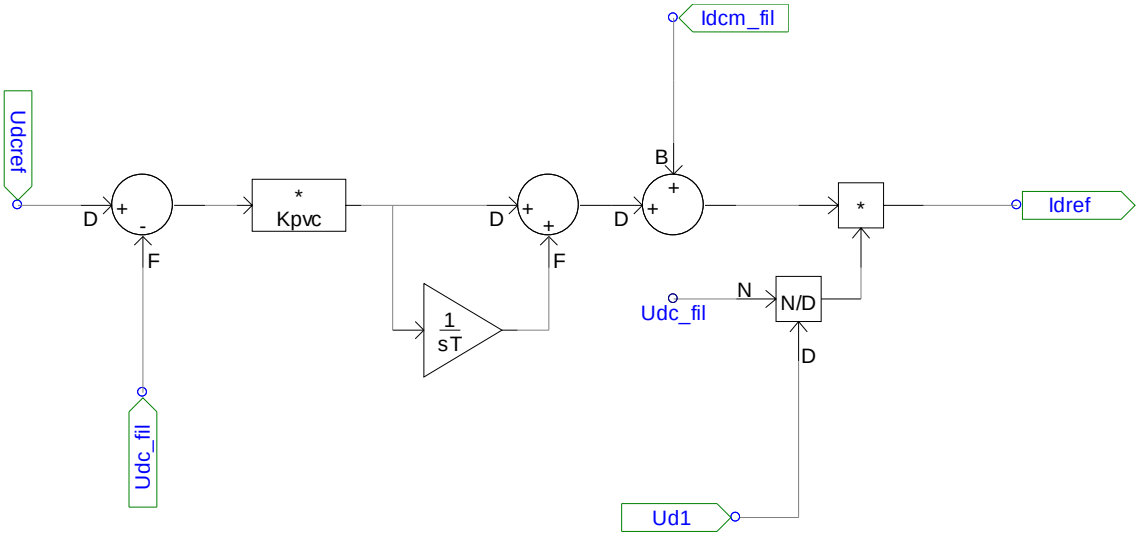

Figure 12 Voltage controller as modeled in PSCAD.

4.3 CURRENT CONTROLLER

In PWM converters for ac applications, vector control systems can be utilized to obtain independent control of the active and reactive powers. One of the most advantageous characteristics of vector control is that vectors of ac currents and voltages occur as constant vectors in steady state, and hence static errors in the control system can be avoided by using PI controllers. A vector control technique with a block diagram shown in Figure 13**Error! Reference source not found.** is suggested in [1] for the current controller loop.

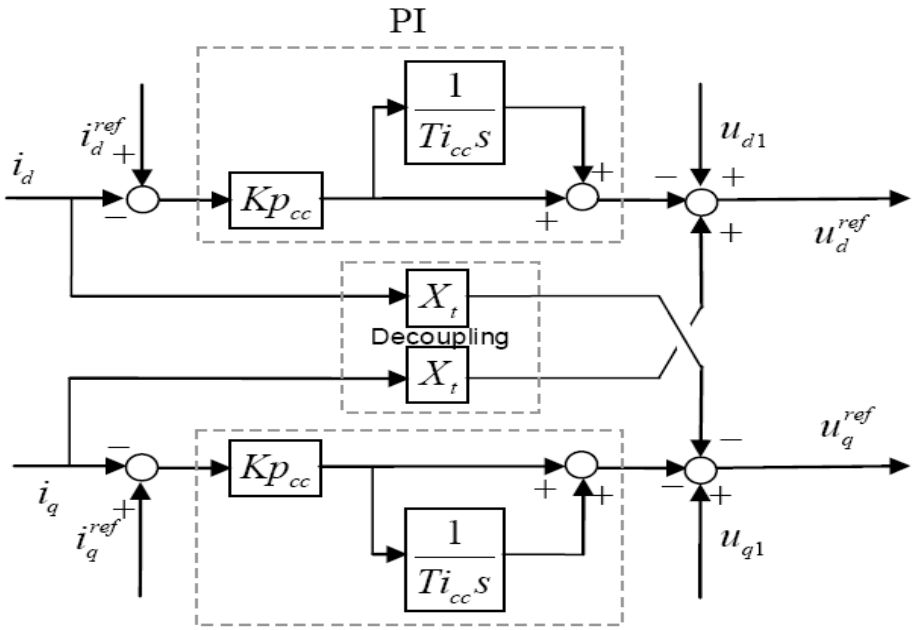

Figure 13 Block diagram of the current controller.

The current controller (*CC*) block shown in Figure 1 converts the reference currents given from the active and reactive (if present) power control into a voltage reference for the *PWM* and its internal modulation. As shown in the block diagram the active and reactive power are controlled independently with DC-valued signals in a rotating reference frame.

The integrator outputs in steady-state correspond to voltage drop over the main transformer and are subtracted from the measured line voltages, u_{d1} and u_{q1}, resulting in the reference voltages, u_d^{ref} and u_q^{ref}, for the *PWM*. The two control loops are decoupled through the cross

feeding of $i_{d/q}.X_t$. The *CC* integral part is also used to remove the steady-state impact of mismatch between the actual and the model inductances leading to imperfect decoupling.

The PSCAD model of the current controller which is the exact duplicate of the model suggested in [1] is shown in Figure 14.

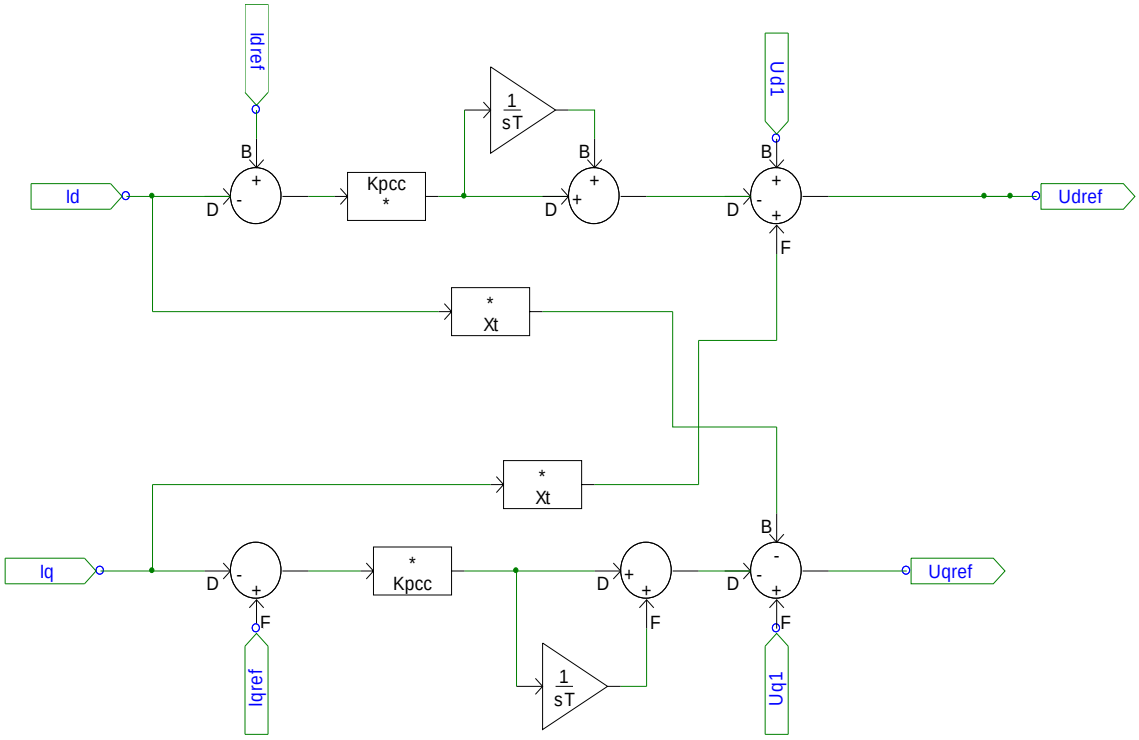

Figure 14 Current controller as modelled in PSCAD.

The DC valued voltage references, u_d^{ref} and u_q^{ref} ,are converted in an AC values by use of the inverse Park's transform ($dq/\alpha\beta$) . The inverse park transformation block is modeled in PSCAD as shown in equation (6).

$$\begin{bmatrix} U_a^{ref} \\ U_b^{ref} \end{bmatrix} = \begin{pmatrix} \cos(\theta_{pll}) & -\sin(\theta_{pll}) \\ \sin(\theta_{pll}) & \cos(\theta_{pll}) \end{pmatrix} \begin{bmatrix} U_d^{ref} \\ U_q^{ref} \end{bmatrix} \tag{6}$$

4.4 POWER ELECTRONICS CONVERTERS

With utilization of voltage source inverters, AC traction motors are presently common in electric railway traction applications. Several AC motors such as switched reluctance, permanent magnet synchronous and asynchronous motors are being used widely in electrified traction applications. Meanwhile, induction motors are being used as the most popular AC motors for the electrified traction systems [12]. Every electric railway locomotive manufacturing company uses one of the mentioned motor structures for traction force generation which is needed to run the train sets.

Converter controlled electric drive is finding applications in many new land-based systems, ranging from heavy armored vehicles to public transportation buses and automobiles. An example of a configuration of a PWM single-phase rectifier in railway application is shown in Figure 15. The source power is supplied through a pantograph and a transformer. The leakage inductance of a transformer plays a role of an inductor filter.

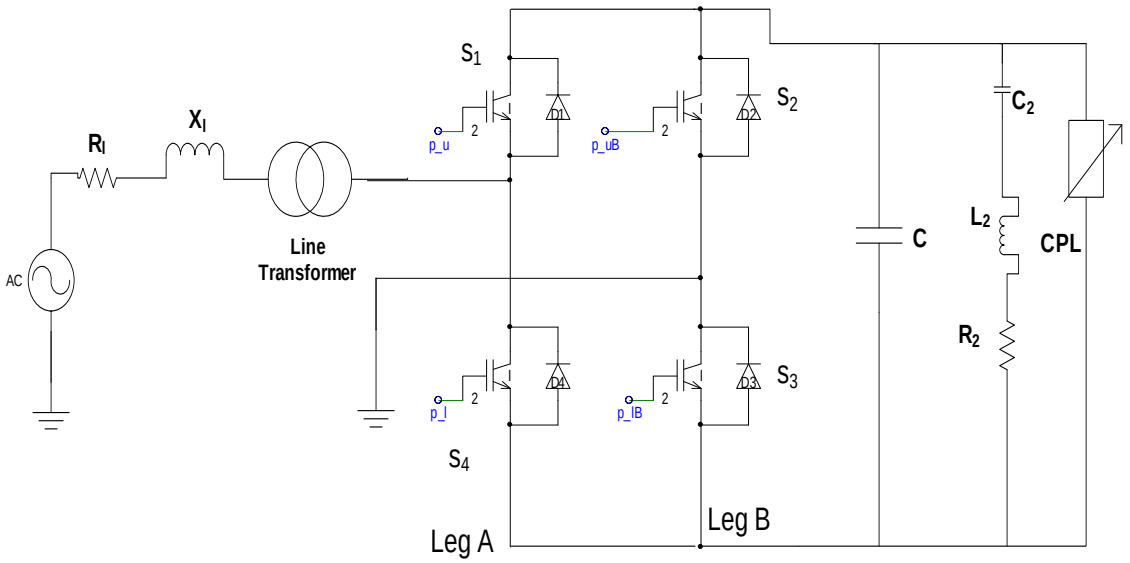

Figure 15 Structure of a single-phase PWM rectifier for traction applications.

The inverter consists of four switching devices (represented as ideal IGBT switches) connected in the form of a bridge. The control scheme is implemented using a unipolar

voltage switching technique with two control signals and two comparator circuits. The driving signals for the switch devices are generated from the comparator circuit output.

The reference voltage, u_{ac}^{ref}, and the inverse of the reference voltage, $-u_{ac}^{ref}$, is compared in two different comparator circuits with the triangular carrier signal. The signal output from the comparator is applied as a driving signal for the switching circuit in order to control the ON and OFF of the bridge circuit in the inverter.

Figure **16** shows the comparator circuits and its output driving signals as modeled in PSCAD. The control signal p_U is the output signal from the first comparator which compares u_{acref} and *tri* (the triangular carrier signal), this control signal is used to drive S_1 and its inverse p_I is used to drive S_4 in leg A of Figure 15. The driving signals for leg B are generated from the second comparator which compares $-u_{acref}$ and *tri* (the triangular carrier signal), p_UB and p_IB, which drives switches S_2 and S_3 respectively.

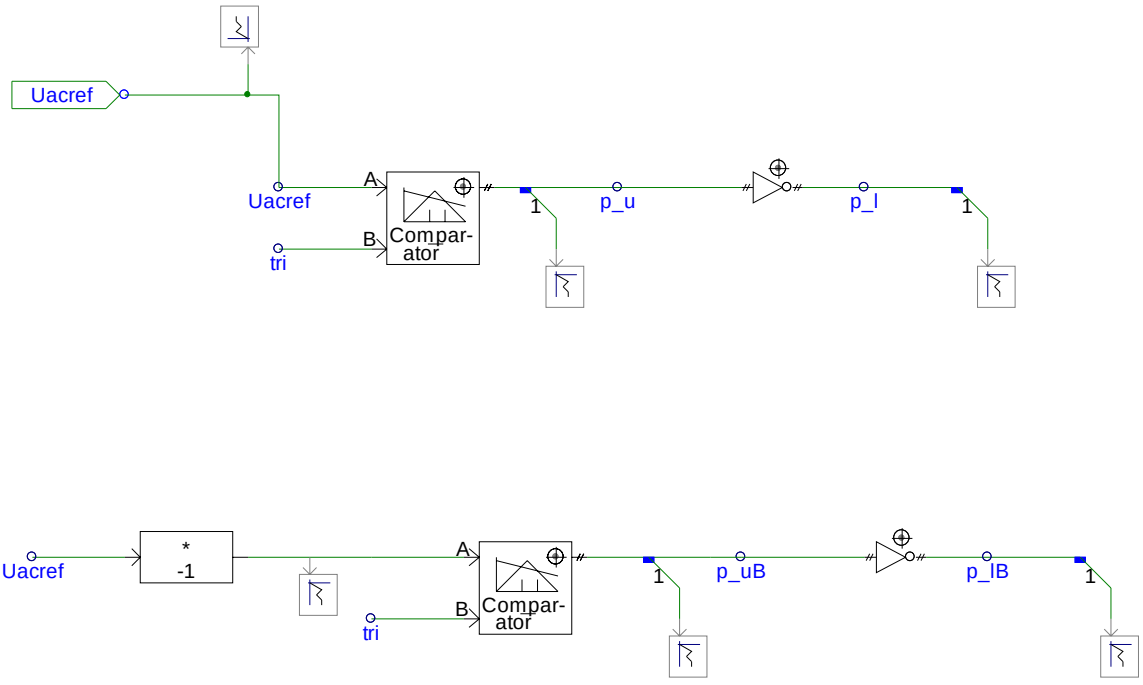

Figure 16 Comparator circuit for the PWM control.

In the unipolar switching scheme the output voltage changes between positive and zero, or between zero and negative voltage levels. To produce a sinusoidal output voltage waveform of variable frequency and amplitude, a sinusoidal reference signal (u_{ac}^{ref}) is compared with the triangular waveform (V_{tri}). The amplitude modulation index (m_a), which controls the RMS value of the output voltage, is defined as in equation (7).

$$m_a = U_{ac}^{ref}(peak) / V_{tri}(peak) \tag{7}$$

Where $u_{ac}^{ref}(peak)$ is the peak amplitude value of the reference voltage and $V_{tri}(peak)$ is the peak value of the triangular, carrier, waveform.

Leg A and leg B of the full-bridge inverter are controlled separately by comparing V_{tri} with u_{ac}^{ref} and V_{tri} with -u_{ac}^{ref}. The resulting waveforms are used to control the switches as in equation (8) and equation (9).

In leg A:

$$\begin{aligned} u_{ac}^{ref} &> V_{tri} \quad \text{S1 ON} \\ u_{ac}^{ref} &< V_{tri} \quad \text{S4 ON} \end{aligned} \tag{8}$$

And
In leg B:

$$\begin{aligned} -u_{ac}^{ref} &> V_{tri} \quad \text{S3 ON} \\ -u_{ac}^{ref} &< V_{tri} \quad \text{S2 ON} \end{aligned} \tag{9}$$

The mechanism of the comparator for generating the driving signals p_U and p_UB for switch S_1 and S_3 are shown in Figure 17 and Figure 18 . Note that the driving signals for S_4 and S_2, p_I and p_IB, will be automatically created as the inversion of p_U and p_UB respectively. The

figures clearly shows that whenever the reference signal is greater than the triangular carrier signal the driving signal will be one in magnitude which can be interpreted as ON switch and its zero(OFF switch) when the reference signal is less than the triangular carrier signal.

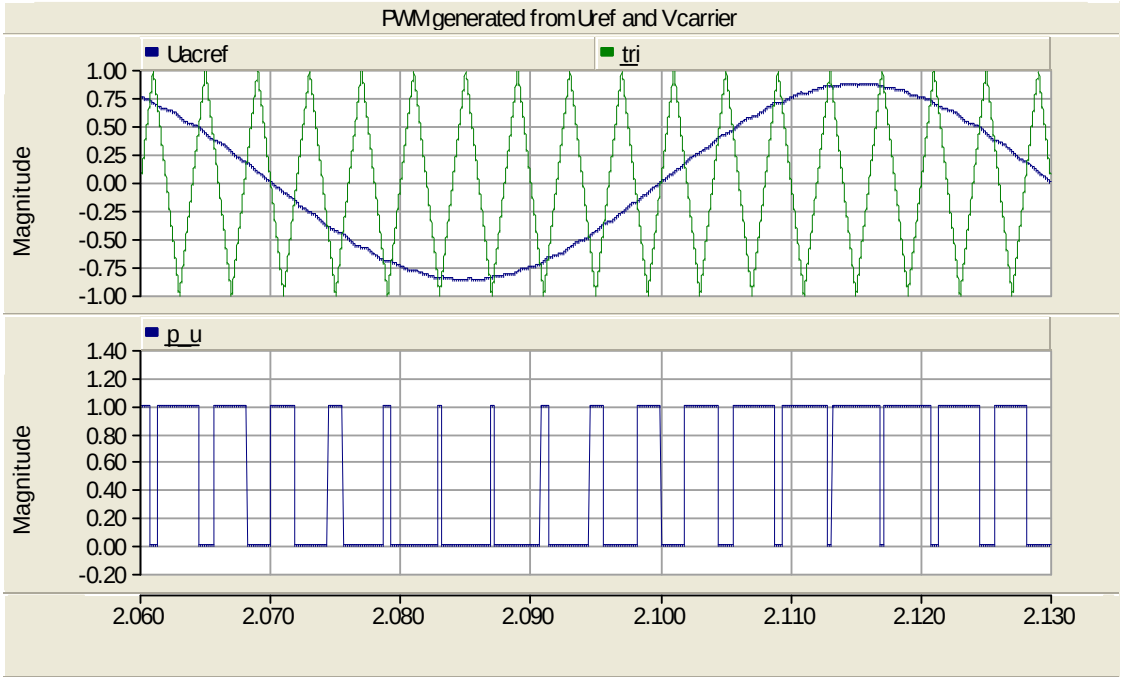

Figure 17 PWM signals for leg A

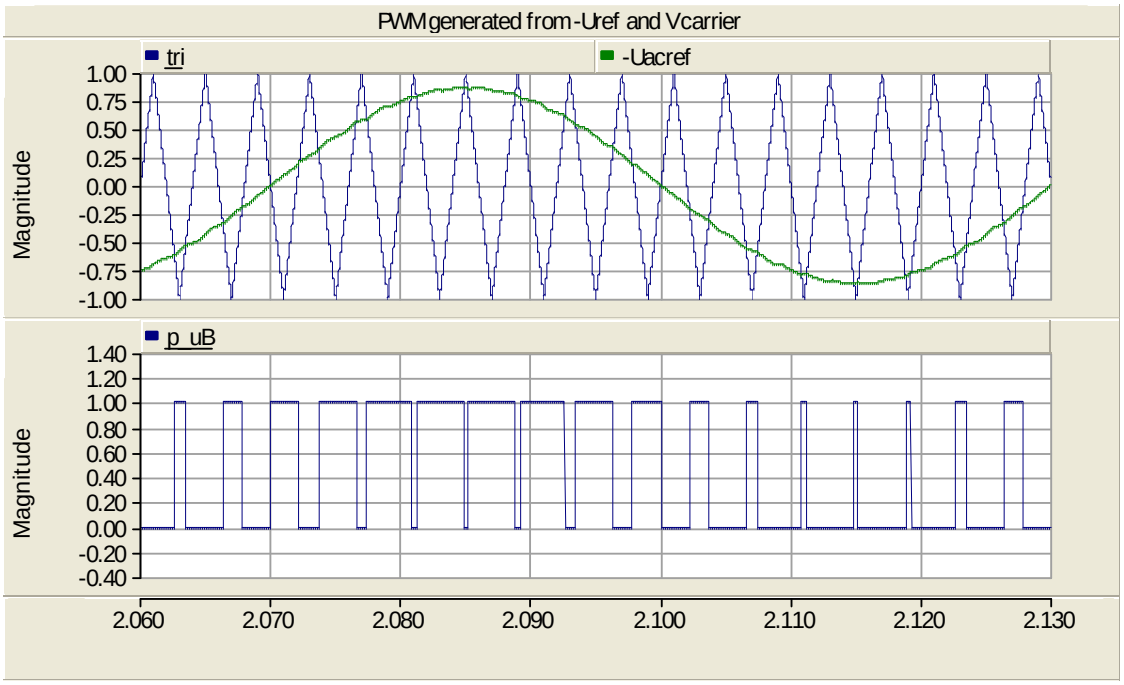

Figure 18 PWM signals for leg B

The voltage obtained as a result of the PWM switching is shown in Figure 19. In the DC-link voltage the second harmonic ripple with a frequency of twice the line frequency (33.33Hz) and a relatively high frequency ripple with a frequency of twice the switching frequency (500Hz) due to unipolar can be seen in the figure.

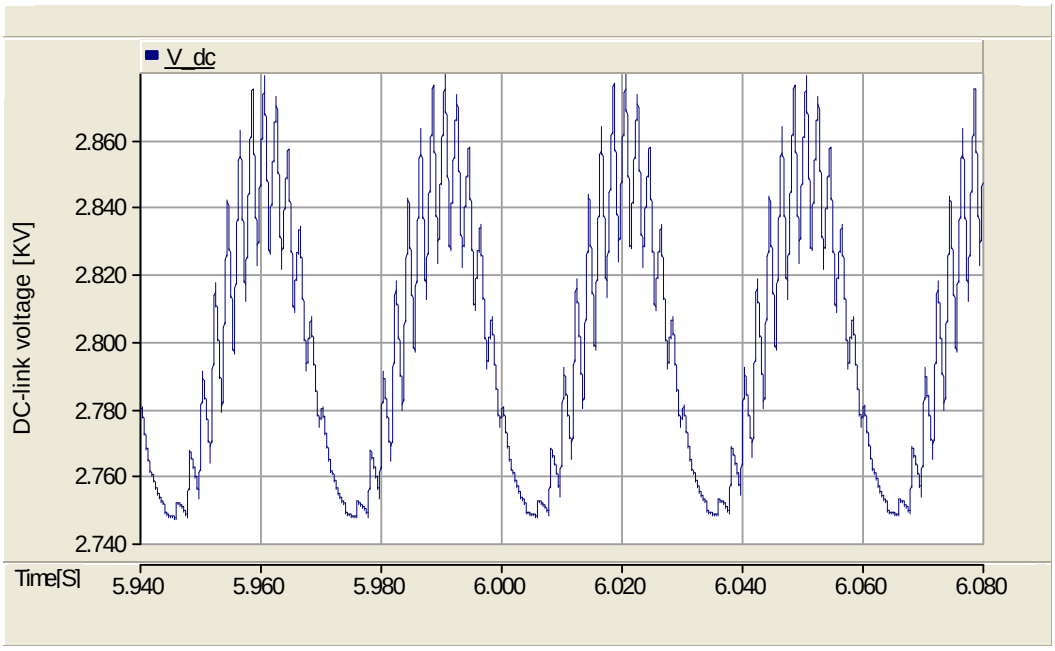

Figure 19 DC-Link voltage measured in PSCAD.

From the control point of view, the converter is considered as an ideal voltage source with a time delay, the output voltage of the converter is assumed to follow a voltage reference signal, u_{ac}^{ref} with an average time delay equals half of the switching cycle, due to PWM switching [16].

$$Y(s) = \frac{1}{1 + sTa} \tag{10}$$

4.5 MODELLING OF OTHER SYSTEM COMPONENTS

1) Modelling of the transformer in PSCAD

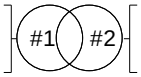

Figure 20 Transformer component in PSCAD Library

A transformer component models, as shown in Figure 20 , of 1-phase, 2-winding transformer which is based on the classical modeling approach is used from the PSCAD library for the transformer model [13].

2) Modelling the comparator

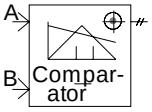

Figure 21 Comparator component in PSCAD Library

This component compares two inputs. It outputs a pulse when one signal crosses the other, or it outputs a level output when one signal is above the other, depending on the specified output type. Interpolation compatibility is enabled in the model, then the interpolated information (i.e. for the exact time the two inputs cross each other) is generated by the device and sent to the output. When interpolation is utilized, this device is very accurate even at larger time steps.

3) Modelling of the load

A constant power load is modeled in PSCAD as shown in Figure 22 by using a controllable current source and a divider. The divider divides the constant power, $P = 3.67MW$ by the measured DC-link voltage, *V_dc* in the figure, and calculates the magnitude of the controlled current source which is indicated as *i_1*.

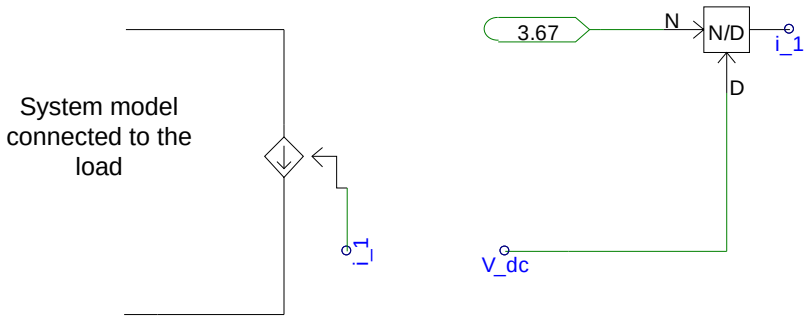

Figure 22 Constant power load as modeled in PSCAD

5. DEAD-TIME DELAY COMPENSATION TECHNIQUE

The up to date technology in motor control provides an adjustable voltage and frequency to the terminals of the motor through a pulse width modulated (PWM) voltage source inverter drive. In this type of drives, a dead-time exists due to non-ideal characteristic of power switching devices. Although the dead-time is short, it causes deviations from the desired fundamental output voltage. Despite the fact that each deviation does not significantly affect the fundamental voltage, the accumulated deviations result in reduced fundamental output voltage, distorted machine currents, and torque pulsations. The dead-time problem has already been investigated and several techniques of compensation has been proposed [14], [15].

For triangular carrier modulators, an average time delay from the reference voltage u_{ac}^{ref} to the actuated PWM terminal voltage u_{ac1} of half the switching frequency is assumed [16]. This average delay can be compensated by manipulating the synchronous rotating reference frame angle θ_{pll} as proposed in [8].

The analysis in [8] shows that the correction can be implemented as a modified $\alpha\beta$ transformation. It is also possible to implement a stand-alone correction, $v_{corr}(t)$ as in equation (11) and (12) where the inverter command vector is denoted as $v(t)$.

$$v_{corr}(t) = e^{j\omega 1(t)\tau} v(t) \tag{11}$$

On real-value vector form:

$$v_{corr}(t) = \begin{pmatrix} \cos\omega_1(t)\tau & \sin\omega_1(t)\tau \\ -\sin\omega_1(t)\tau & \cos\omega_1(t)\tau \end{pmatrix} v(t) \tag{12}$$

The compensation angle, θ_{comp}, in equation (13) for $\tau = \frac{1}{2} T_{sw}$ and $\omega_1(t) = 2\pi f_1$ is given by the switching frequency f_{sw} and the fundamental frequency, f_1, as shown in equation (14). This

angle is compensated for the pulse width modulated (PWM)-switch model in *dq* to *αβ* transformation block as shown in the circled area of Figure 1.

$$\theta_{comp} = \omega_1(t)\tau\,[rad] \tag{13}$$

$$\theta_{comp} = \frac{\pi f_1}{f_{sw}}[rad] \tag{14}$$

6. SIMULATION RESULTS

6.1 DIFFERENT LOAD TYPE COMPARISONS

Three different load types are modeled in PSCAD to see the influence of the load type in the low frequency behavior, for each load type the response of the DC-link voltage for a step in 3.67MW step in motor power is added at 60km line is analyzed and the average and switching models are compared.

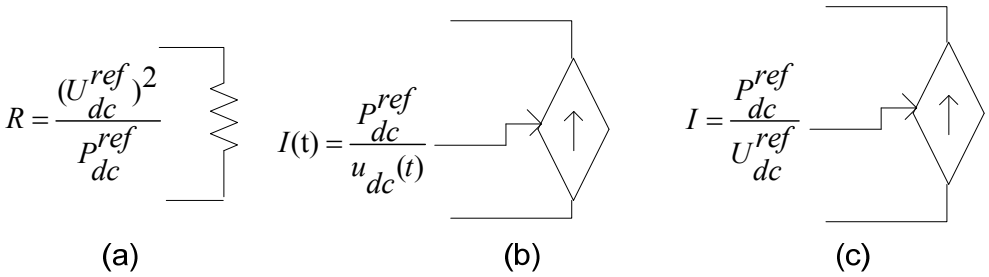

Figure 23 Schematic representation of the three different load models.(a) constant resistance, (b) constant power, (c) constant current.

The three different load types, Figure 23, are constant resistance, constant current and constant power. The constant resistance is modeled as a constant resistance value calculated as in equation (15).

$$R = \frac{(U_{dc}^{ref})^2}{P_{dc}^{ref}} = \frac{(2.8kV)^2}{3.67MW} = 2.136\Omega \tag{15}$$

The constant current source is modeled as a constant current source which is calculated by a controllable current source where its value is calculated as in (16)

$$I = \frac{P_{dc}^{ref}}{U_{dc}^{ref}} = \frac{3.67MW}{2.8kV} = 1.311kA \tag{16}$$

The constant power load is modelled as a controllable current source, which value is calculated by a constant power load value, P_{dc}^{ref} divided by the measured DC-link voltage u_{dc} as shown in equation (17).

$$I(\mathrm{t}) = \frac{P_{dc}^{ref}}{u_{dc}(t)} \text{ where } P_{dc}^{ref} = 3.67MW \tag{17}$$

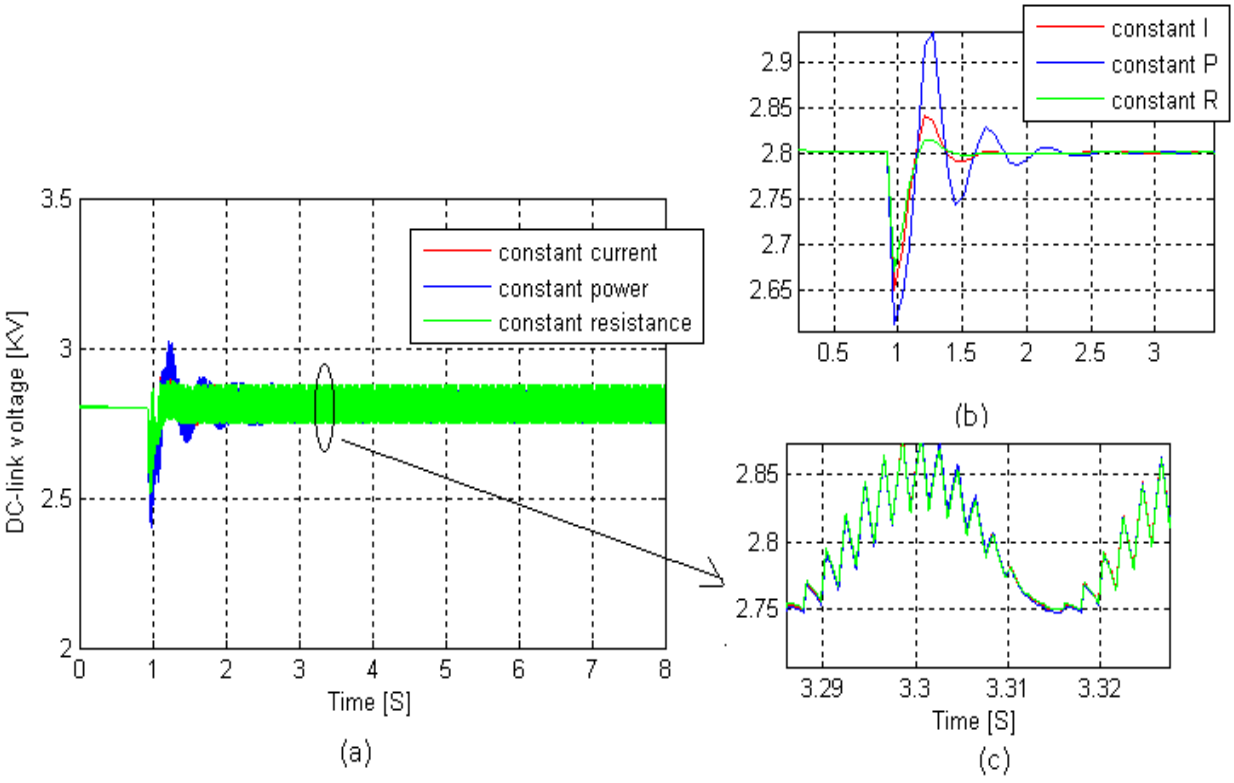

Figure 24 (a) DC-Link voltage response comparisons for three different load types in the switching model (b) Low frequency behavior of the three different load responses on the DC-link voltage (c) Switching harmonics and Second harmonic oscillation in steady state for the three different load comparisons.

The comparison of these three different load types for the three types of loads for both the average and switching model of the DC-link voltage response is shown in Figure 24 and Figure 25 .

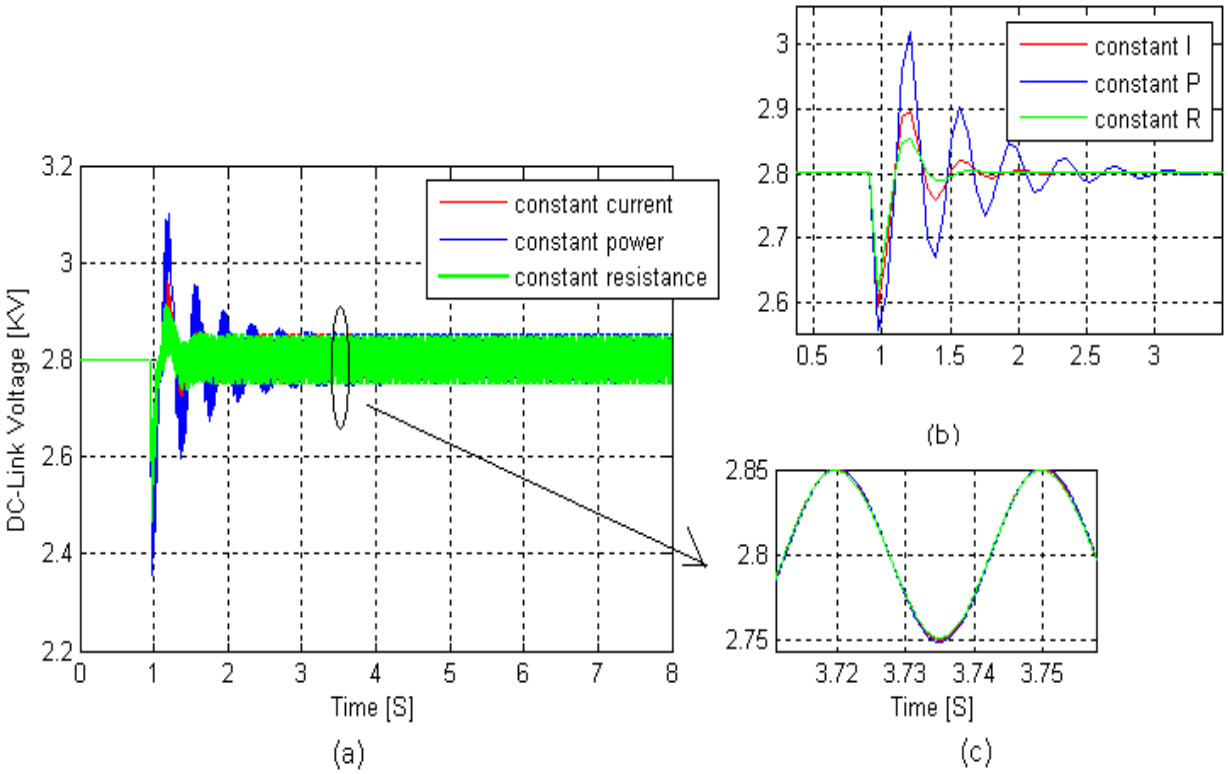

Figure 25 (a) DC-Link voltage response comparisons for three different load types in the average model (b) Low frequency behavior of the three different load responses on the DC-link voltage (c) Second harmonic oscillation in steady state for the three different load comparisons.

The constant power load has high overshoot and longer settling time for both the average and the switching model. The constant current load has a lower overshoot and a shorter settling time when compared to the constant power load, the constant resistance load model has the best result of all the three loads in terms of amplitude of overshoot and settling time. However in all the three load cases the frequency of oscillation of the DC-link voltage is the same.

The average model is more oscillatory than the switching model, compare Figure 24 (b) and Figure 25 (b), for all the load types. Also the frequency of oscillation for the average model is higher than the switching model for all the three load types. The comparison for average and switching model is further analyzed for the constant power load in section 6.3 of this report.

6.2 HARMONIC ANALYSIS ON THE SWITCHING MODEL

The extensive use of drives and electronic control devices in the railway systems can cause problems of power quality and consistency in the traction load supply. Distorted voltage and current waveforms, RMS voltage variations, frequency shifts, unbalances, electromagnetic disturbances can cause damages as the lack of stability of the supply or unsafe conditions. High harmonic values in the voltage spectrum can cause problems to the correct operation of railway supply and electronic control devices [17], [18]. As a matter of fact it could be interesting to analyze and study how different operating conditions in a PWM converter modeling affect the harmonics contents in the system.

This section of the thesis work aims in studying and analyzing how different operating conditions of the PWM switching will affect the harmonics on the railway system applications. The model developed in this project will be used for this analysis purpose. The effect of type of voltage switching and switching frequency on the AC and DC side of the switching model will be studied and analyzed in this section of this thesis work.

1) Unipolar and bipolar switching (f=250 Hz)

a) Bipolar Voltage switching

The harmonics of a line current are limited by the transformer leakage inductance, but an increase leakage inductance means a larger fundamental voltage drop, a larger converter voltage will be necessarily. This subsection analyzes the effect of the voltage switching method in the AC side of the converter voltage. Figure 26 shows the converter AC voltage, measured in PSCAD, denoted as E_{a1}, for bipolar voltage switching for a 250Hz frequency.

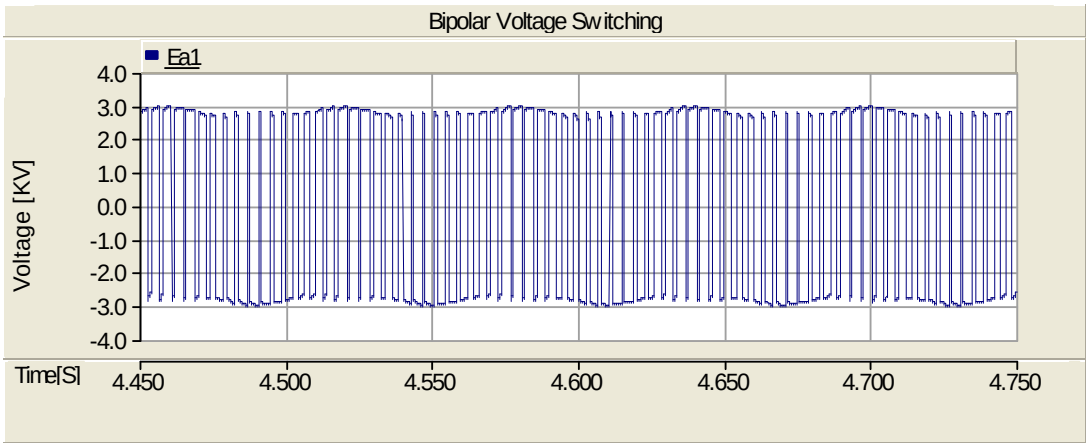

Figure 26 Bipolar voltage switching converter AC side voltage as measured in PSCAD

To determine the harmonic magnitude and phase of the converter AC side voltage as a function of time the Fast Fourier Transform (FFT) method in PSCAD is used. In this FFT analysis the input signals are first sampled before they are decomposed into harmonic constituents.

Figure 27 shows the harmonics in the inverter output voltage wave form appear as sidebands. Centered around the switching frequency and its multiples, that is around harmonics m_f, $2m_f$, $3m_f$ and so on. Where m_f the frequency modulation ratio as is is defined in equation (18).

$$m_f = \frac{f_s}{f_1} = \frac{250Hz}{16\frac{2}{3}Hz} = 15 \tag{18}$$

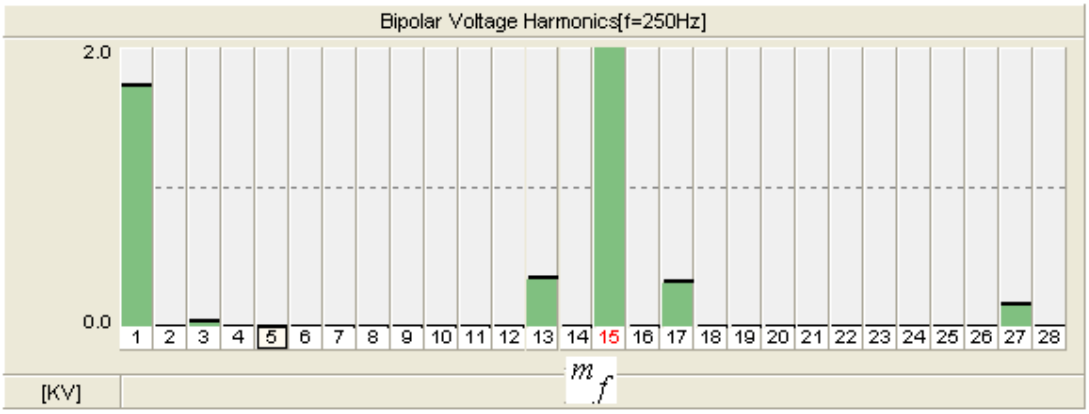

Figure 27 FFT analysis of the harmonic spectrums in the AC side bipolar switched voltage

The figure in the X-axis shows the value of m_f where at $m_{f=15}$, $m_{f=2*15}$, $m_{f=3*15}$ and so on the harmonics appear with its side bands, In this figure only he first harmonics at $m_{f=15}$ is visible, and its side bands appear at $m_{f=13}$ and $m_{f=17}$.

b) Unipolar voltage switching

The advantage of this type of switching is effectively doubling the switching frequency as far as the output harmonics are concerned, compare to the bipolar switching scheme. Figure 28 shows the measured AC side converter voltage as measured in PSCAD.

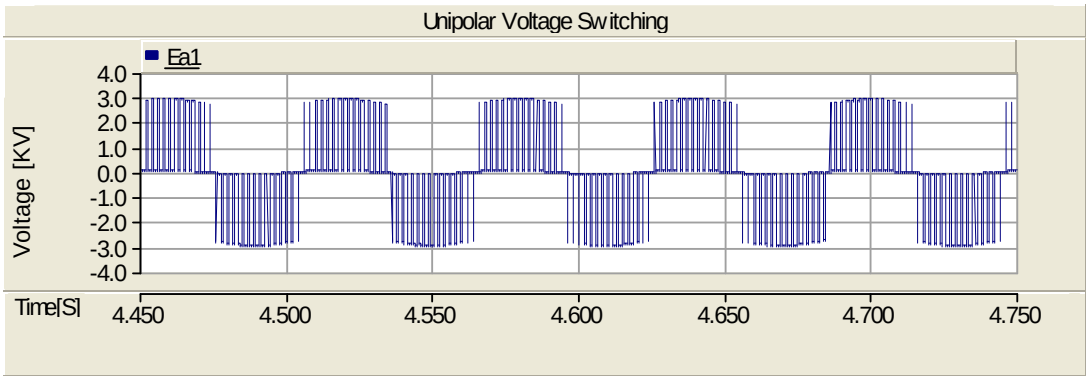

Figure 28 Unipolar voltage switching converter AC side voltage as measured in PSCAD

The FFT analysis of the unipolar switched voltage is shown in Figure 29. The advantage of effectively doubling the switching frequency appears in the harmonic spectrum of the output voltage waveforms. Where the lowest harmonic appears as sidebands of twice the switching frequency.

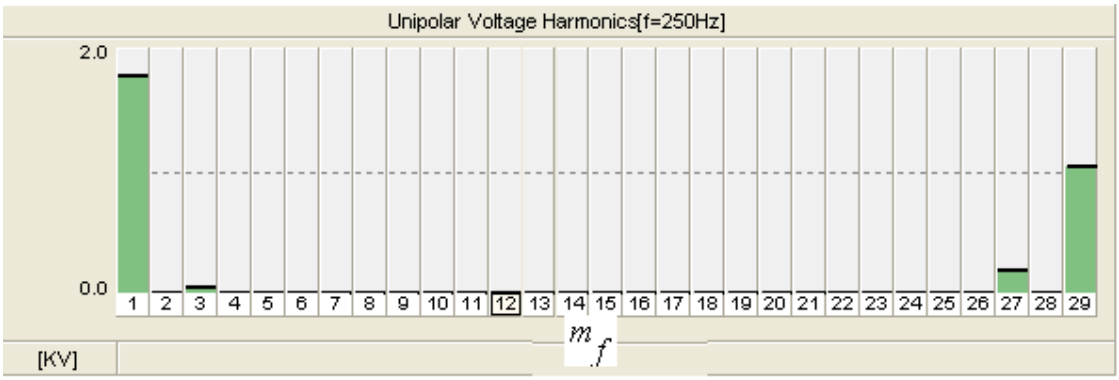

Figure 29 FFT analysis of the harmonic spectrums in the AC side unipolar switched voltage

Comparing Figure 27 and Figure 29 , we can clearly see the advantage of effectively doubling the switching frequency, the harmonics at $m_{f=15}$ and its side bands are disappeared in unipolar voltage switching. In unipolar voltage switching the harmonics will appear only at $2m_f$, $4m_f$, and so on.

c) Comparison of Bipolar and unipolar switching

In Figure 26 we observe that the output voltage from the converter switches between positive and negative voltage levels, this is the reason why this type of switching is called a PWM with bipolar voltage switching. However in unipolar voltage switching, Figure 28, when a switching occurs, the output voltage changes between zero and positive voltage levels or between zero and negative voltage levels. For this reason this type of PWM scheme is called unipolar voltage switching, as opposed to the PWM with bipolar voltage switching.

The unipolar voltage switching scheme has the advantage of effectively doubling the switching frequency as far as the output harmonics are concerned, compared to the bipolar switching model. Also the voltage jumps at each switching is reduced to $V_{\_d}$ instead of $2V_{\_d}$ in the case of bipolar voltage switching. In unipolar voltage switching the dominant harmonic

voltages centered around the frequency modulation ratio m_f disappear, thus resulting in significantly lower harmonic content.

This harmonic current also affects the DC-link motor current; Figure 30 shows the comparison of the harmonic content of the load current in the unipolar and bipolar switching. Using unipolar voltage switching results in a smaller ripple in the current on the DC side of the converter, as compared to the bipolar voltage switching. Therefore using the unipolar voltage switching reduces the content of harmonics in the motor current.

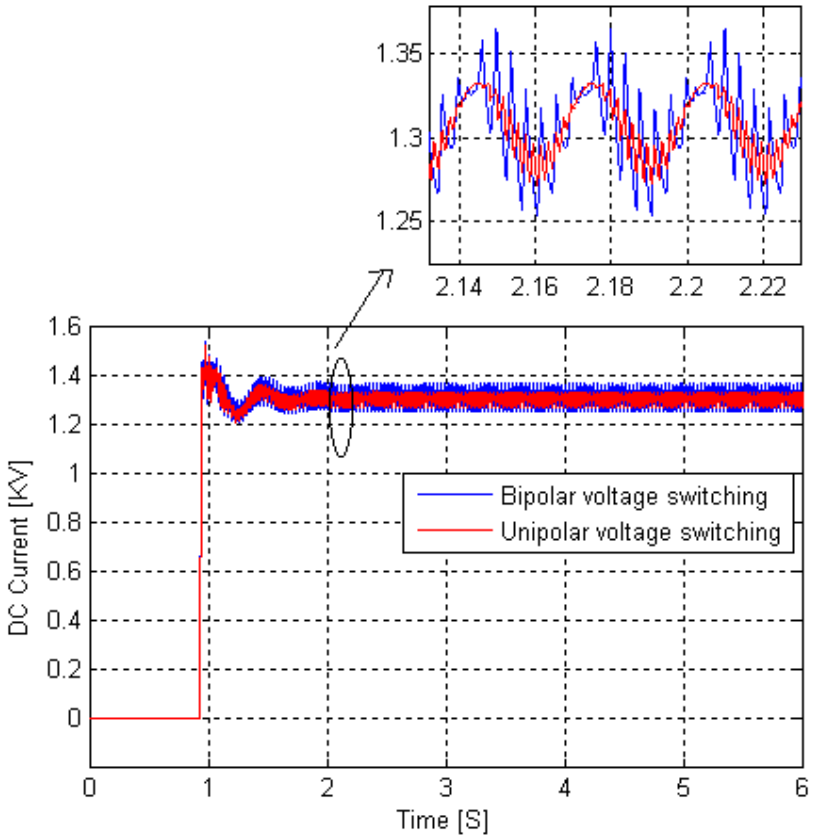

Figure 30 DC-Link motor current comparisons for unipolar and bipolar voltage switching technique.

Based on this analysis result in the current section of the thesis work the unipolar voltage scheme should be used for railway application since as low harmonics as possible is preferred in this application. Therefore a unipolar voltage switching scheme is used in the other sections of the thesis work.

2) Effect of the different operating switching Frequency on the performance of the system and stability limit

The literature on drives says that when the controlled frequency is an exact sub multiple of the switching frequency of the converter there will not be sub harmonics [4], [19]. On basis of this, it could be interesting to see this effect by making the analysis of the effect of the operating frequency on the low frequency stability of the system. The effect of the non exact sub multiple relationships can have on the stability limit will be analyzed. Since the frequency of control is fixed to 16 2/3Hz, the analysis will be made on trials with different sets of switching frequencies for the same limit length of line.

a) Worst case scenario

The worst case scenario would be when the control frequency is not exact submultiples of the switching frequency. Low frequency and non integer multiple of the switching frequency is taken. f_s=225Hz

$$\frac{f_s}{f_1} = \frac{225Hz}{16\frac{2}{3}Hz} = 13.5$$

b) Best case scenario

The best case scenario would be when the switching frequency is a multiple of the controlled frequency and higher. In this case a frequency of 1000Hz is taken.

$$\frac{f_s}{f_1} = \frac{1000Hz}{16\frac{2}{3}Hz} = 60$$

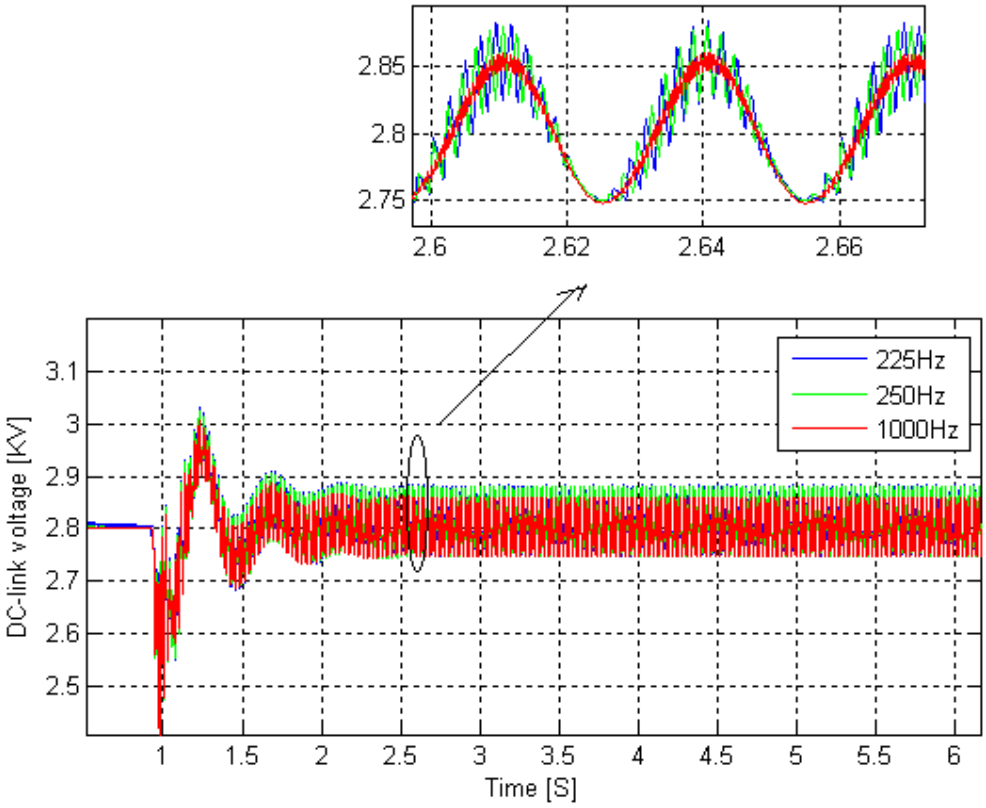

Figure 31 Comparisons of Harmonic content of the DC-link voltage on different frequencies of the switching PWM rectifier.

The comparisons result, Figure 31, shows that for the best case scenario of operating frequency, when a high switching frequency and integer multiple of the fundamental frequency is used, the content of harmonic is lower compared to the worst case scenario, when a low switching frequency and non integer multiple of the control frequency is used.

Figure 32 Shows there is slight amplitude difference on the amplitude of the overshoot on the low frequency oscillation of the DC-link voltage. As far as harmonic is concerned the high frequency switching is the best .However based on this analysis result it is difficult to say anything how this operating frequency affects the low frequency stability of the system.

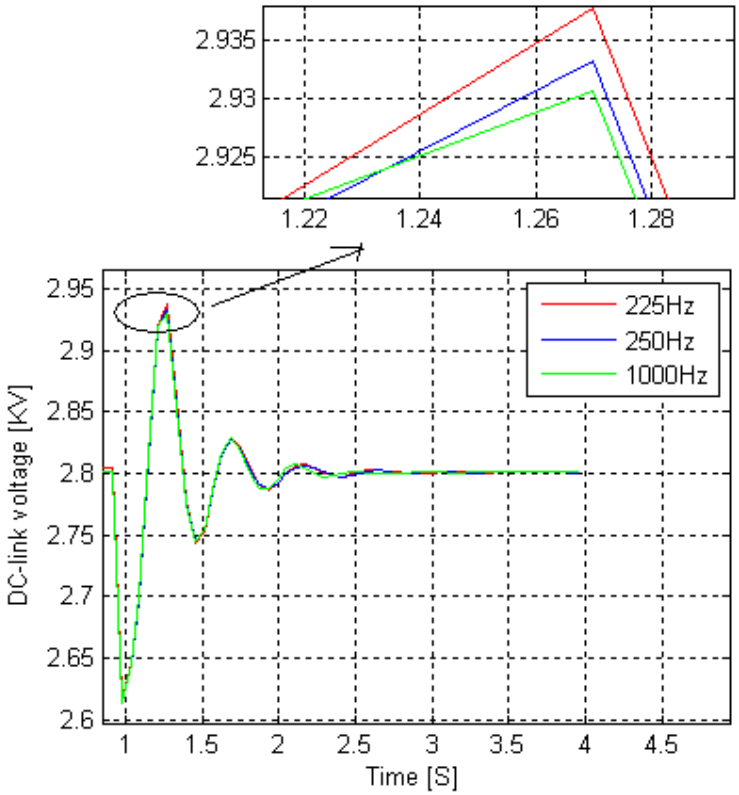

Figure 32 Comparisons of low frequency oscillation of DC-link voltage on different operating frequencies

6.3 COMPARISON OF SWITCHING AND AVERAGE MODELS

The result shown in Figure 33 compares the average model and the switching model of the DC-link voltage when a 3.67MW step in motor power is added at 60km line. In both curves it is observed the typical second harmonic ripple twice the line frequency as expected in this case. In addition, in the switching model a ripple due to the semiconductor switching which is twice the switching frequency due to use of unipolar voltage switching is observed.

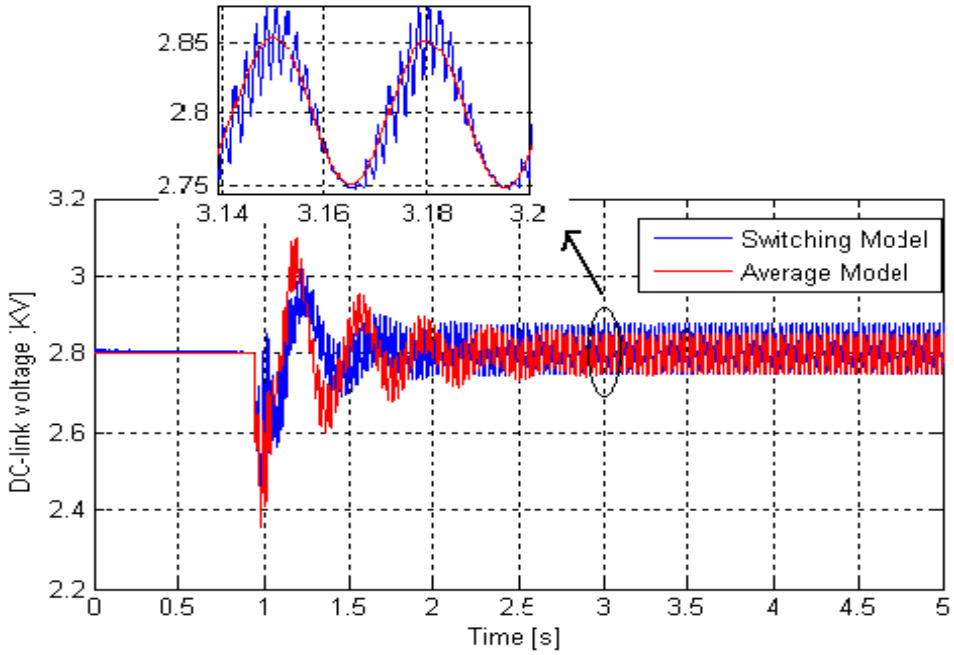

Figure 33 Response in DC-link voltage when a 3.67MW step in motor power is added at 60km line for the two models.

In order to see the low frequency behavior of this response for the two models Figure 33 is averaged in a period of $T = 1/f_1[\text{sec}]$ and is shown in Figure 34.

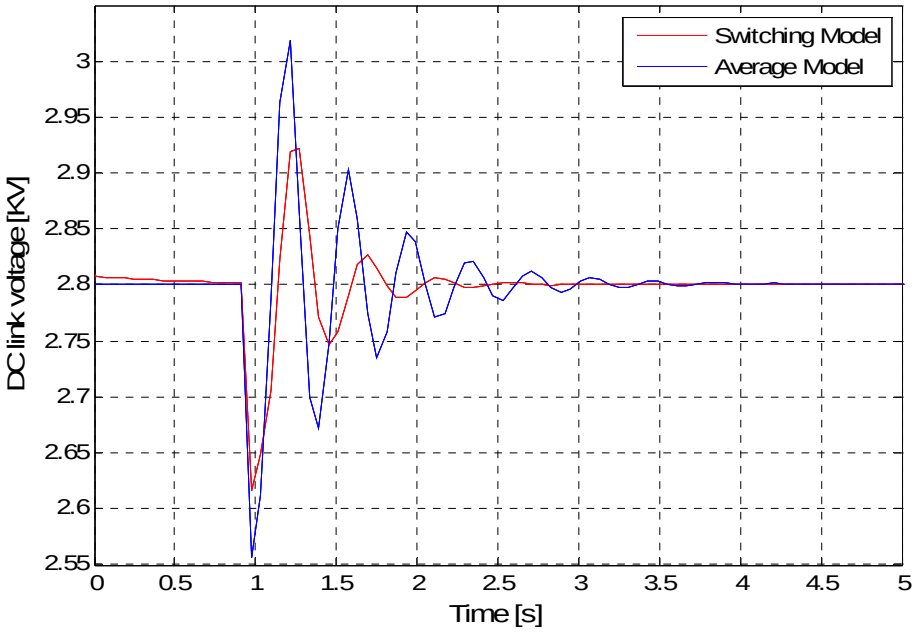

Figure 34 Low frequency oscillation of DC-link voltage compared for the two models.

Table 1: Comparison of switching and average models

	Average model	Switching model
Settling time	2.5seconds	1.5seconds
Frequency of oscillation	2.67Hz	2Hz

The frequency of oscillation and the settling time for the switching and average model is calculated and estimated from the oscillation graph and the calculated and estimated values are given in Table 1. As we can see in the table the switching model has a better damping, less settling time and lower amplitude overshoot (Figure 34).

6.4 EFFECTS OF CONVERTER LOSS ON THE SYSTEM DAMPING

In the switching model the losses in the converter (the averaged dissipated power $P_D(t)$ in the semiconductor devices) can be obtained by subtracting the power output, $P_{output}(t)$, from the converter to the power input, $P_{input}(t)$, to the converter as shown in equation (21).

$$P_D(t) = P_{input}(t) - P_{output}(t) \tag{21}$$

This loss when the load consumes 3.67MW power is calculated in PSCAD and shown in Figure 35. The converter has a loss of 0.218MW which is 6% of the total power. A first-order low-pass filter is used for measurement of the loss. The on state loss in the converter can be calculated by using equation (22) which is the on state resistance R times the square of the current. The default value of the on state resistance in the switching devices is used in the PSCAD model, which is R=0.01Ω.

$$Onstate\_losses = I^2 R \tag{22}$$

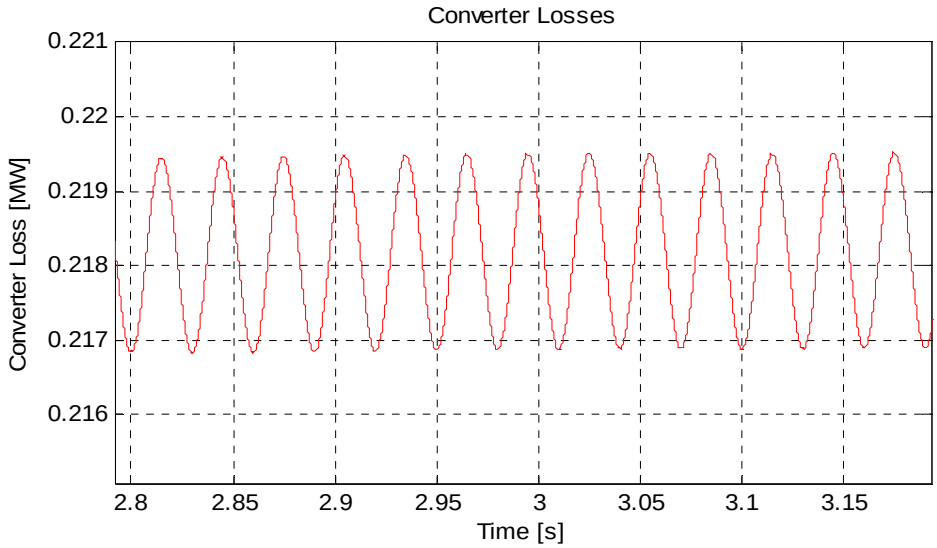

Figure 35 Calculated converter loss by equation (21) in PSCAD.

It could be interesting to see the effect of ohmic loss on the low frequency stability of the system. The effect of this loss on the low frequency oscillation of a system is further analyzed by altering the value of the on state resistance R in the PSCAD converter model. This test is performed with the purpose of analyzing the effect which losses have on a damping effect on the low frequency behavior of the system and the comparisons of the DC-link voltage for different losses is shown in Figure 36.

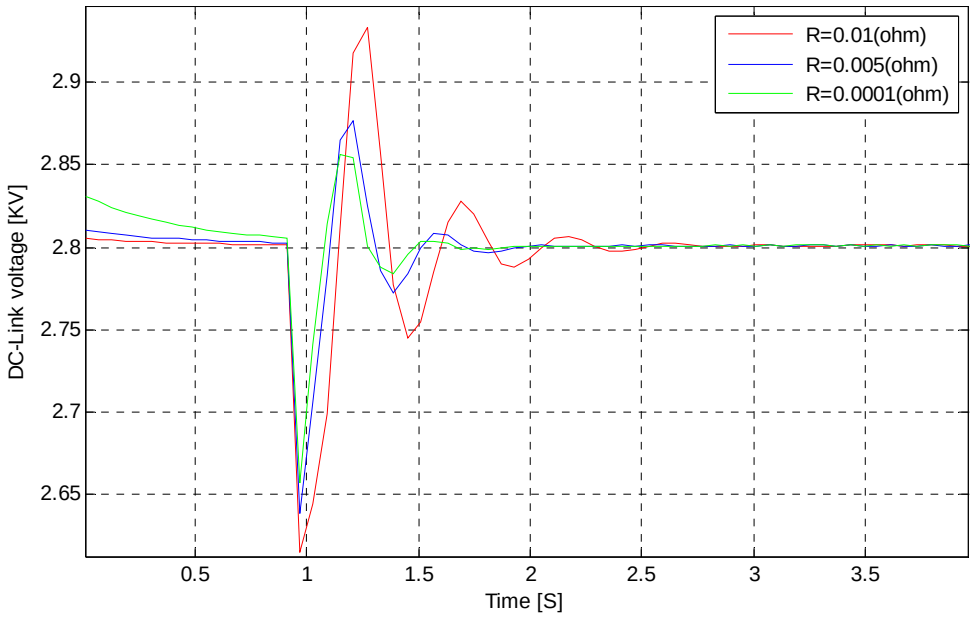

Figure 36 Comparison of the DC-link voltage oscillation for different values of on state resistance of the converter.

The result shows that as the losses decrease the overshoot and the settling time decreases as well and the model with the lowest switching loss is more damped. This analysis was done to prove if the damping in the switching model is due to the effect of the ohmic losses in the converter and the analysis proves the losses will not add a damping effect on the switching model. But there is a minimum loss at R=0.0001Ω in the converter that can't be removed even if the on state resistance value is further decreased.

6.5 STABILITY LIMIT INVESTIGATION FOR AVERAGE AND SWITCHING MODELS

For the purpose of investigating the stability limit of the models a time simulation method is carried out in EMTDC/PSCAD. The line length is increased by increasing the line parameters in the model. Figure 37 shows the DC- link voltage measurement for different line lengths at no load scenario. The line length is increased in both the switching model and average model and the plots are shown in the right and left side of Figure 37 respectively.

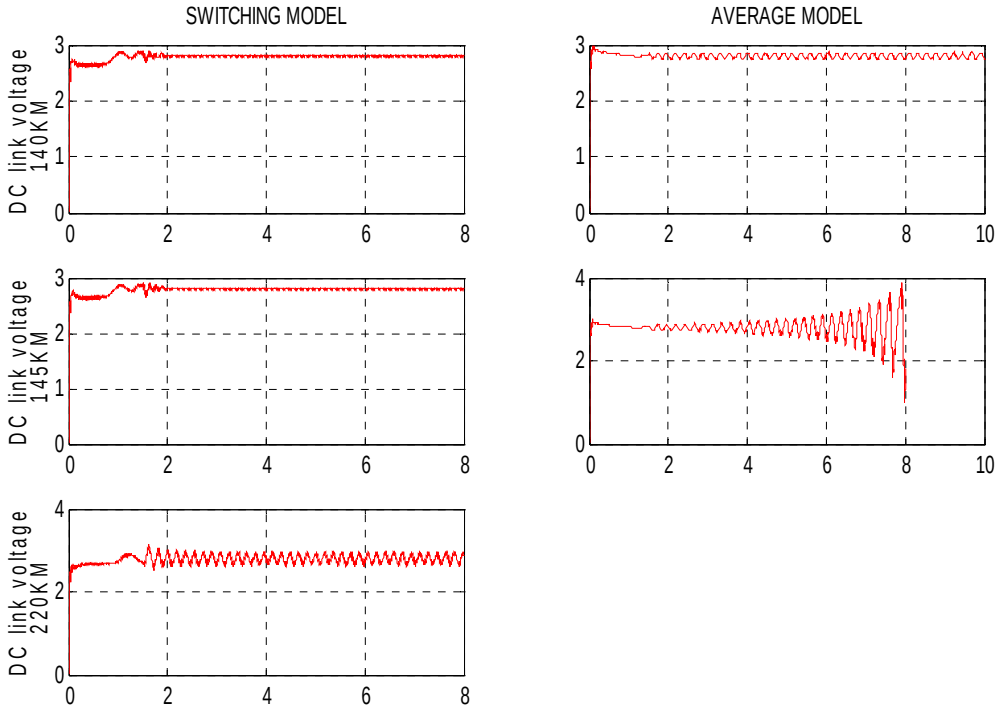

Figure 37 Stability limit investigation on the average and switching model

The result in the figure shows at 145km the average model DC-link voltage is oscillating and the amplitude of oscillation is growing. This is DC-link voltage instability. However, at the same line length the switching model DC-link voltage is well damped.

6.6 COMPARISON OF THE DEAD-TIME COMPENSATED AND NON-COMPENSATED MODELS

Figure 38 shows the comparison of DC-link voltage response for a 3.67MW step in motor power between the dead-time compensated model and non-compensated model.

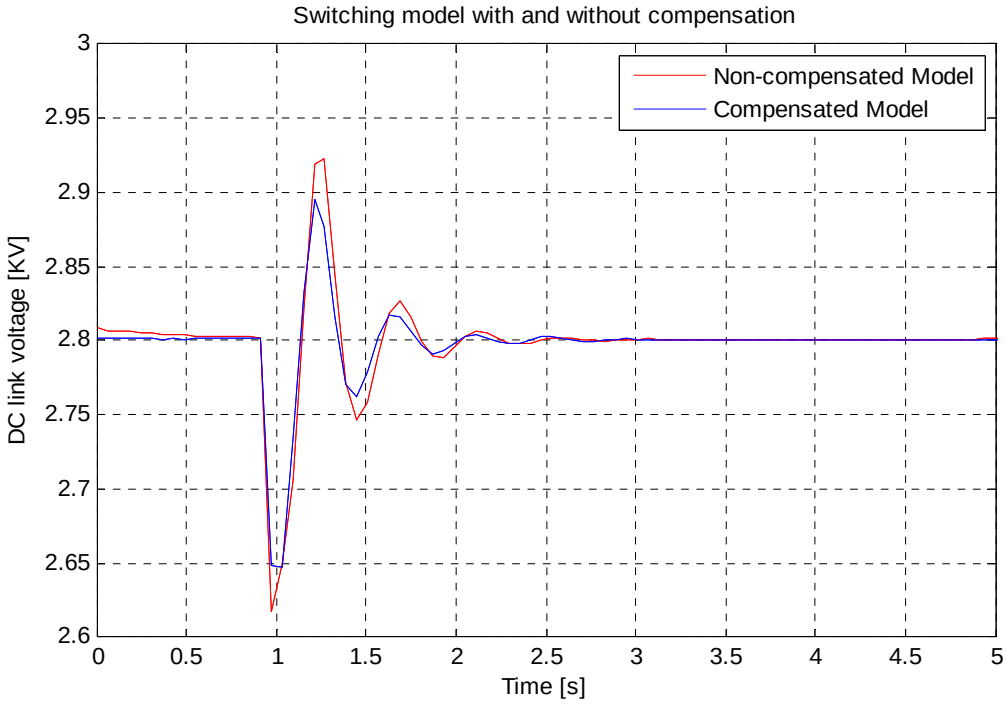

Figure 38 DC-link voltage response with and without the dead-time compensation.

The simulation is carried out to improve the delay in DC- link voltage control loop caused by the switching dead-time by using the proposed compensation method in the inverse-park transformation block of the control loop.

Comparison of the dead-time compensated and non-compensated models is shown in Figure 38. The delay is compensated during transients as can be seen from the figure and can be neglected in the average model since semiconductor switching is not included in the simplified model. Moreover, the delay in DC- link voltage control loop caused by the switching dead-time effect was improved in terms of transient overshoot by compensation of dead-time in the inverse-park transformation block of the control loop.

7. DISCUSSION

In this thesis work an advanced electric rail vehicle for traction power system application with and without including the detailed PWM switching of the semiconductor of the line inverter is designed and tested in the PSCAD/EMTDC simulation environment. The purpose has been to study and analyze the effect of semiconductor switching on the general performance of the system low frequency oscillation and to analyze the harmonics content and effect on the various operating condition of this semiconductor switching. The effect of semiconductor switching on the low frequency behavior of the DC-link voltage when a 3.67MW step power is added at 60km line is investigated. Furthermore, the performance of a PWM time delay compensation technique is analyzed.

In the low frequency oscillation comparison shown previously in Figure 34 the switching model is more damped and has lower overshoot compared to the average model. This result agrees with the stability limit investigated in Figure 37, which gives the switching model a longer stability limit.

The switching model has a detail converter model which adds 6% converter loss as described in the previous section. The phenomenon which adds a damping effect is not well understood, however this analysis indicates that modeling the switching of the semiconductor results in an increase damping effect on the low frequency behavior of the system.

8. CONCLUSSION

In this thesis work VSC for traction power system with and without including the detailed PWM switching is modeled. The effect of semiconductor switching on the low frequency behavior of the DC-link voltage when a 3.67MW step power is added at 60km line is investigated. In addition a long line stability test at no load is performed in the average and switching models for the purpose of investigating the damping effect. Furthermore, the performance of a PWM time delay compensation technique is analyzed.

Load step and long line stability test results both agrees and gives a better damping effect on the switching model compared to the average model. From the presented results, the average model gives less realistic representation of the converter dynamics concerning transient oscillations. The detailed model with the PWM switching gives a closer to reality representation of the system from the low frequency behavior point of view. The tremendous advantage of unipolar voltage switching technique and high operating frequency has been proved and analyzed as far as harmonic in the system is concerned. Moreover, the delay in DC- link voltage control loop caused by the switching dead-time effect was improved by compensation of dead-time in the inverse-park transformation block of the control loop.

In order to study the low frequency behavior for stability limit investigation of a traction systems, a detailed semiconductor switching (PWM) - model, which takes into account the semiconductor nonlinearity needs to be modeled and well understood.

9. FURTHER WORK

A good understanding of the switching model and the sources of its damping effects is necessarily to see effect of the semiconductor switching on the low frequency stabilities of the system, though the thesis is tried to analyze and explain the problems a further investigation is required. For example:

- The same investigation could also be done with the average model by including an equivalent representation of the effect of the switching action that can give the same low frequency response as in the detailed switching model.
- Bode plots could be used.
- Analysis of oscillatory modes from closed loop transfer function.
- The detail motor side load could also be included in order to see the influence of the motor side and its control system as it might also be a source of instability and it also brings the model more close to real life system.

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APPENDIX

A. DETAIL PSCAD MODELLING

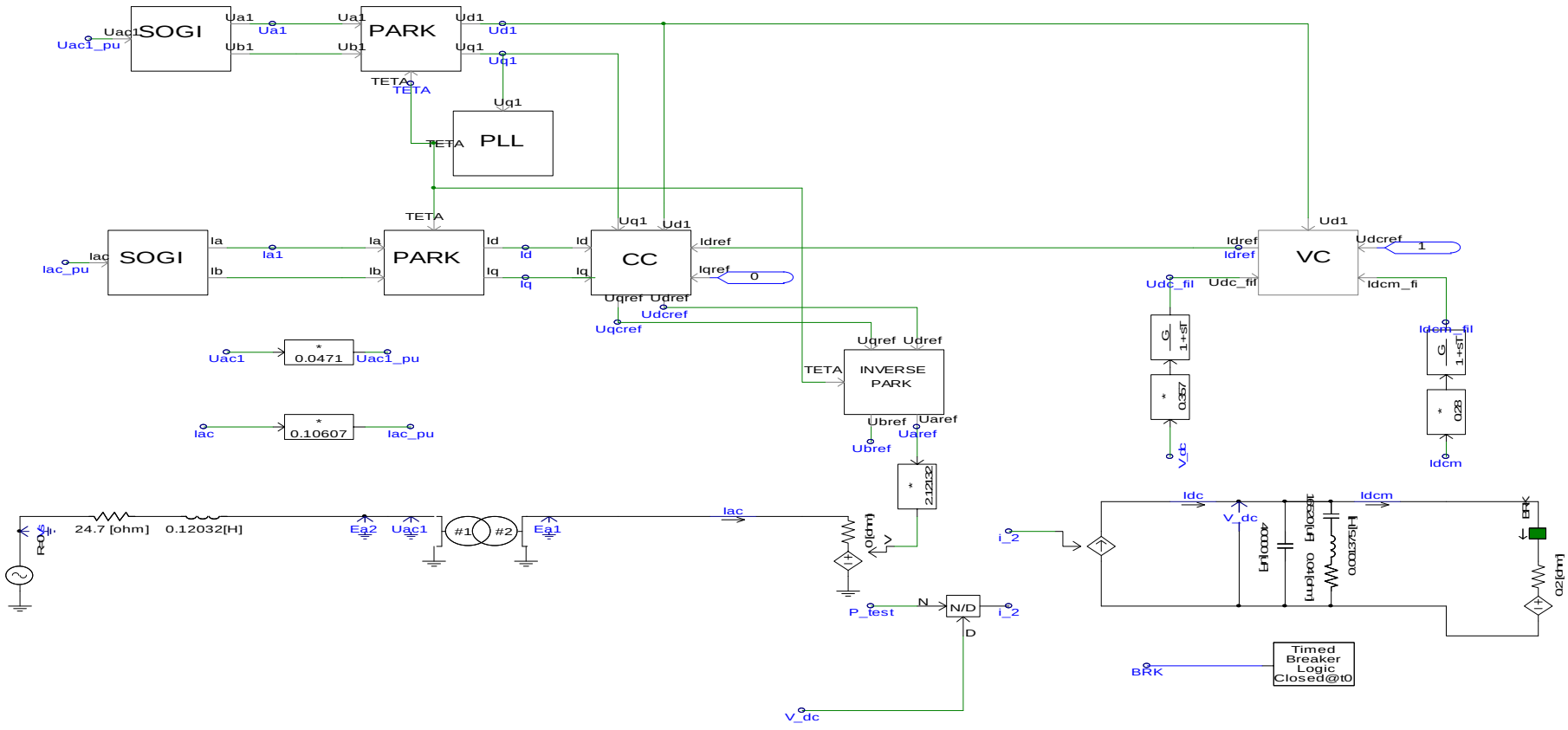

Figure 39 Single line diagram for the average model in PSCAD

Figure 39 shows the screen shot taken from EMTDC/PSCAD user interface. This figure is taken in the no-load model of PSCAD for the purpose of stability limit investigation for the average model. The different blocks in the figure are the component models of the system as explained in the report, Also the detail model of this components can be viewed in the original PSCAD model attached with this report in a CD-ROM.

In the figure the blocks that changes U_{ac1} to U_{ac1pu} and I_{ac} to I_{ac1_pu} are the per unit system converting method. The detail per unit system used in the PSCAD modeling will also be explained in the subsequent appendix.

The block that multiplies Iac and Ea1, see Figure 40, calculates the AC power p_test and this power is divided by the measured DC-link voltage to calculate the controllable current source i_2 .

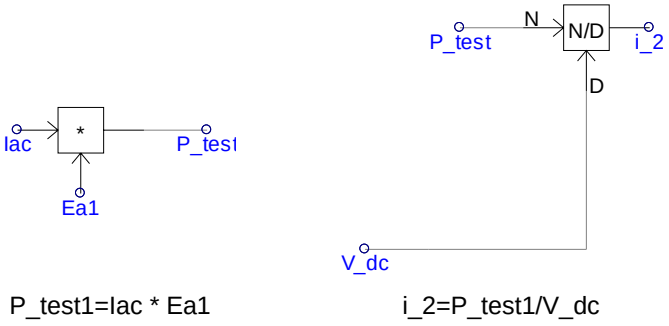

Figure 40 AC Power and DC link current calculation for the average model.

1) Implementation of constant resistance load in PSCA

The constant resistance load in PSCAD is modeled as shown in Figure 41 , a time breaker logic component is used in the PSCAD library using this component, it is possible to initially set the state of the breaker being controlled to OFF (open) or ON (closed). This breaker logic is used in the model to apply a step resistive load for the system when the switch is closed.

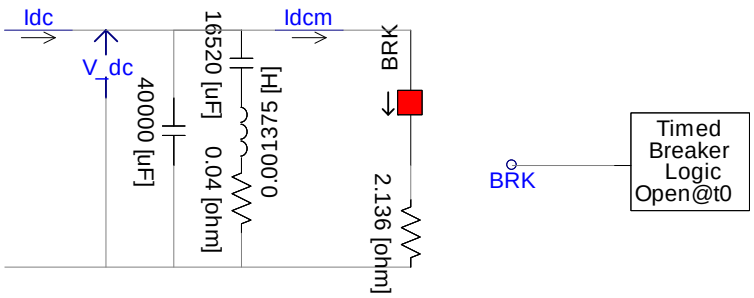

Figure 41 Constant Resistance load in PSCAD

2) Implementation of constant current load in PSCAD

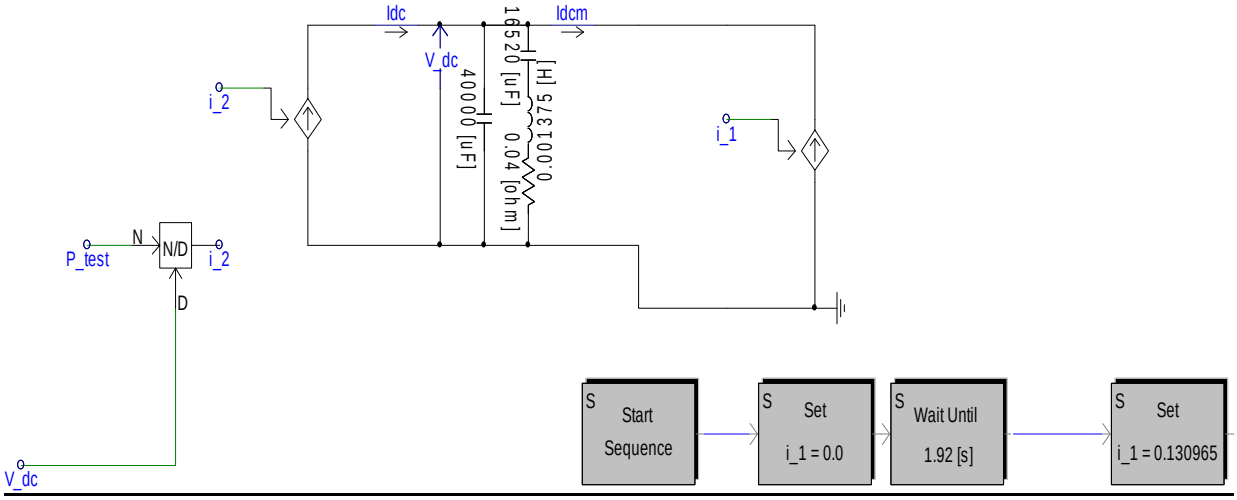

Figure 42 Constant Current load in PSCAD

The constant current load is modeled in PSCAD as shown in Figure 42. A sequencer is used to apply the step in the motor power.

3) Implementation of constant power load circuit in PSCAD

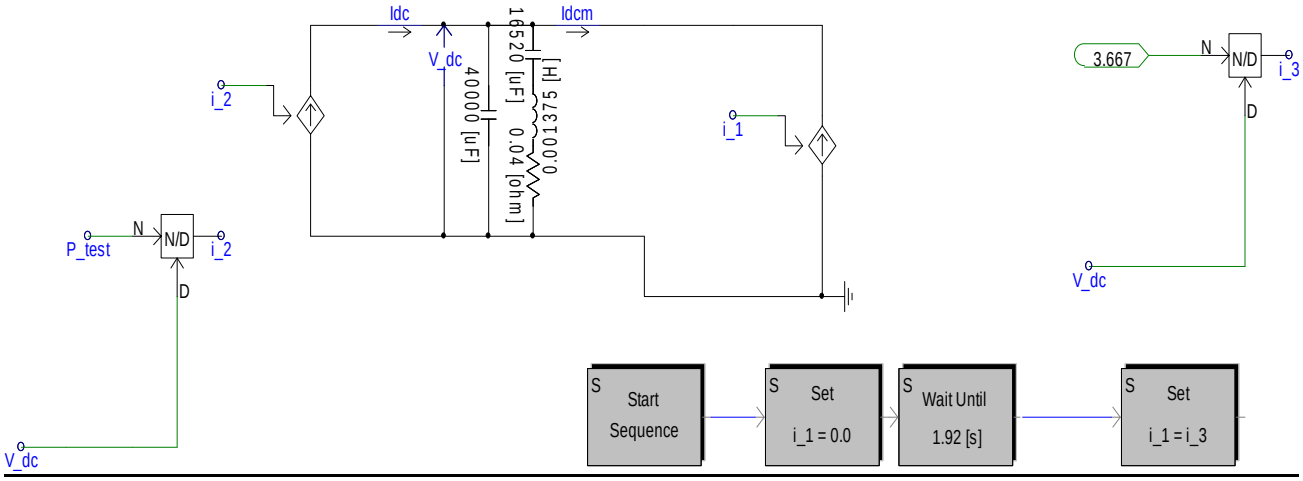

Figure 43 CPL load circuit in PSCAD

The constant power load model for the average model is shown in Figure 43 the step load is modeled using a sequencer circuit in the PSCAD library.

B. PER UNIT CALCULATION OF THE PSCAD MODEL

The PSCAD model works in physical units, However for the control system it is significant to use a per unit converting calculation in the PSCAD model. These conversions will be explained briefly in this section.

Per unit values are calculated only for the signals that goes to the control system, Each of these calculation and numeric's used in the PSCAD model are explained below.

1. The measured AC voltage U_{ac1} that goes to the SOGI control block is calculated to its per unit value U_{ac1_pu} is recalculated as:

$$U_{ac1\_pu} = \frac{U_{ac1}}{15kV * \sqrt{2}} = \frac{U_{ac1}}{21.2132kV}$$

$$21.2132^{-1} = 0.0471$$

This can be seen in the single diagram of the PSCAD model as shown in Figure 44, Uac1 is multiplied by the inverse of the base voltage.

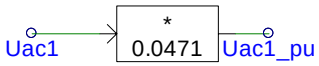

Figure 44 per unit conversion for U_{ac1}

2. I_{ac} that goes from the physical system to the SOGI control system, The pu conversion is :

$$I_{acBASE} = \frac{10MVA}{1.5kV} X\sqrt{2} = 9.428kV$$

$$I_{ac\_pu} = \frac{I_{ac\_pu}}{I_{acBASE}}$$

$$9.428^{-1} = 0.10607$$

This can be seen in the PSCAD model as shown in Figure 45; I_{ac} is multiplied by the inverse of the base current.

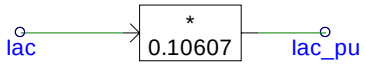

Figure 45 per unit conversion for I_{ac}

3. In the average model U_{aref} is multiplied by the base voltage of the low voltage side of the transformer :

$$1.5kVX\sqrt{2} = 2.12132$$

4. V_dc input to the VC is multiplied by the inverse of the DC side base voltage, which is :

$$2.8^{-1} = 0.357$$

5. I_{dcm} input to the VC is multiplied by inverse of DC side base current:

$$I_{dcBASE} = \frac{10MVA}{2.8kV} X\sqrt{2} = 3.571kV$$

$$3.571^{-1} = 0.28$$

C. LINE INDUCTOR AND RESISTANCE CALCULATION FOR DIFFERENT LINE LENGTH

For long line stability test, the values of the line parameters are calculated below: This values used in PSCAD model are given in Table 2.

$$R = 0.19\frac{\Omega}{km}$$

$$X_l = 0.21 \frac{\Omega}{km}$$

$$L = \frac{X_l}{\omega} = \frac{X_l}{2 * \pi * 16.667} = \frac{X_l}{104.72} H$$

Table 2 Values of inductor and resistor values for different line length.

No	Line length[km]	R[Ω]	L[H]
1	60	11.40	0.12032
2	75	14.25	0.15040
3	80	15.20	0.16043
4	100	19.00	0.200535
5	120	22.80	0.240642
6	125	23.75	0.250668
7	130	24.7	0.260695
8	135	25.65	0.270722
9	140	26.6	0.280749
10	150	28.5	0.300802

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Impact of PWM switching on modeling of low frequency power oscillation in electrical rail vehicle

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Keywords

«Traction application», « Rail vehicle», « voltage source converter», « pulse width modulation», «Single phase system»

Abstract

Simplified system models are in need for stability investigation of complex power systems in order to reduce the model complexity and the simulation time. In this paper the effect of modelling a voltage source converter (VSC) for traction power system with and without the detailed pulse width modulated (PWM)-switch model is modeled in PSCAD and analyzed. The same disturbance is imposed for the two models and the low frequency oscillation of the DC- link voltage response is compared and analyzed. The effect of semiconductor switching on the stability limit of the system is also investigated. Furthermore, the performance of a PWM time delay compensation technique during transient is analyzed.

The result shows that in the model including the switching the DC- link voltage oscillation is damped and has a better stability limit compared to the average model. In the detailed switching model a converter loss is included while in the average model a no loss ideal case scenario is considered.

The delay in DC- link voltage control loop caused by the switching dead time effect was improved by compensation of dead time in the inverse-park transformation block of the control loop.The comparison of the compensated and non-compensated model proves that the compensated model is better in terms of the overshoot of amplitude of transient.

Introduction

Modern electrical locomotives are equipped with a number of power electronic equipment and advanced digital control technology. This improves the performance of the locomotive, but also introduces a lot of new dynamical phenomena of interaction with the railway power supply. For the latest years, the topic of poorly damped low frequency oscillations has been in focus. In some cases these oscillations have resulted in instability of the traction power system [1].

In order to study the interaction between the power electronic component and the rest of the railway traction power system, more realistic models have to be developed [2], [3]. In general, power system modelling includes a number of simplifications in order to reduce the model complexity and the simulation time. A typical simplification is to neglect the impact of the semi-conductor switching during dynamical stability studies [4]. However for more realistic results, the presence of semiconductor switching which is the main source of harmonics and non-linearity in the power system should be considered to evaluate possible impacts on stability.

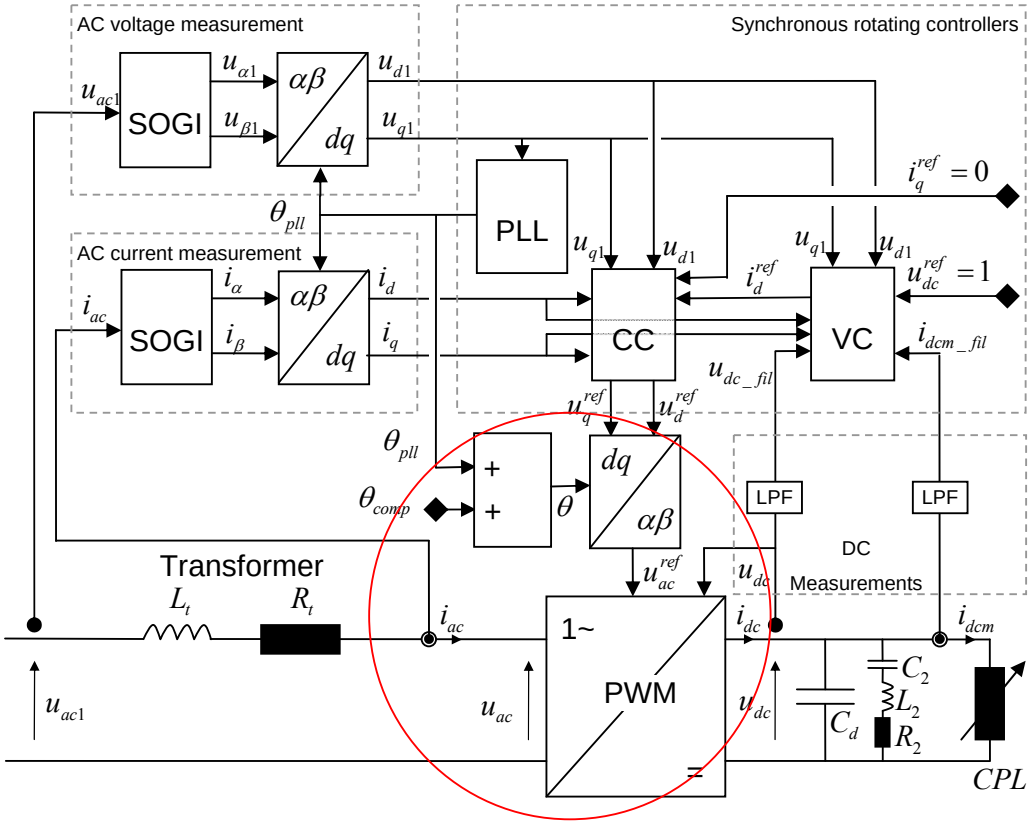

Fig 1 Single line equivalent circuit and block diagrams of the model

A VSC for traction power system with and without the detailed PWM switching model of an electrical locomotive using EMTDC/PSCAD simulation tool is made based on the simplified (average) model suggested in [4] and giving more focus on the circled area of Fig 1.

The detailed model takes into consideration the non-ideal pulse width modulated (PWM)-switch model with the purpose of evaluating the proposed averaged model accuracy, using the refined model for semiconductor devices, to observe the low frequency oscillation response. The main advantage of the proposed switching model is that it takes into account the nonlinear effects of power devices and makes it possible to estimate the dissipated power in the different circuit devices and to evaluate the effect of the semiconductor devices on the general performance of the system low frequency behavior.

The averaged model is limited since the semiconductor devices nonlinearities are neglected. In this detailed semiconductor switchiching model, a non-ideal pulse width modulated switch model which takes into account the semiconductor non-linearity and the simple switching and static characteristics

of these devices are considered .Moreover in this paper, the compensation technique proposed in [5] is used to compensate for the delay caused by the dead time of the switching devices.

System Model Description

The system under study is a single-phase PWM inverter connecting a simple AC-system and a simple DC-system as shown in

Fig **2**. The AC- system includes: an ideal voltage source for 16 2/3 Hz having amplitude of $\sqrt{2} \cdot 16.5$ kV, a 60 km overhead contact line having impedance of (0.19+j0.21) Ω/km and the vehicle main 15 kV/1.558 kV step down transformer.

The DC-system reflects the vehicle DC-link with the DC-link capacitance C_d of 40 mF, the second harmonic resonance tank C_2, L_2 and R_2 tuned on 33.4 Hz in order to reduce the second harmonic ripple given by the single-phase system power pulsations, a constant power load (*CPL*) drawing a current i_{dcm} (see equation (1)) as a simplified equivalent for the motor side.

$$i_{dcm}(t) = P_m^{ref}(t) / u_{dc}(t) \tag{1}$$

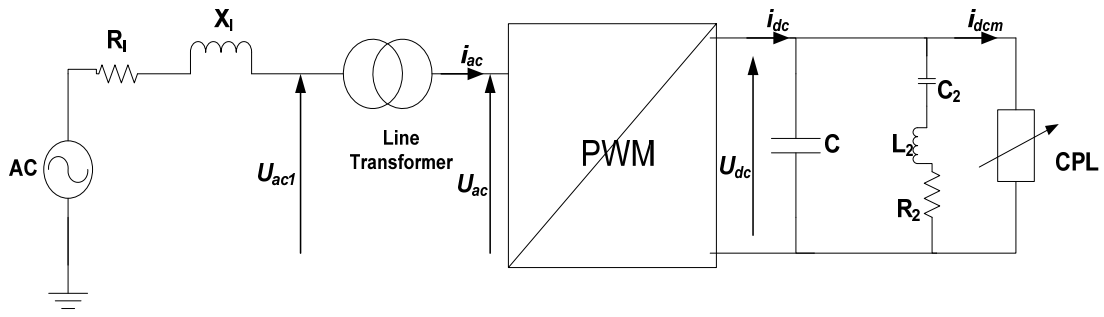

Fig 2 : Schematic representation of the electrical system under investigation.

The control system for the line inverter consists of the synchronization controller which is a phase locked loop (*PLL*) that constantly tracks the phase of the line voltage u_{ac1} for orientation of the direct (*d*) and quadrature (*q*) axis reference frame in which the other controllers rotate. A second-order generalized integrator (*SOGI*) [6] is used for generation of an artificial orthogonal voltage as input to the *PLL*.

The DC-link voltage proportional-integral controller *VC* compares the measured DC-link voltage u_{dc_fil} to its constant reference and together with the fed forward measured motor current i_{dcm_fil} calculates the active current reference i_{dref} for the current controller based on the ratio between the measured DC and AC voltages, u_{dc_fil} and u_{d1} respectively (see Fig 1).

The AC-current proportional-integral controllers (*CC*) compare the measured *d*- and *q*-axis (i_d and i_q) to the respective active and reactive current references i_d^{ref} and i_q^{ref}. The two axes are decoupled over the transformer impedance X_t in order to allow independent control of active and reactive power. The reactive power is controlled to be zero at the vehicle transformer line side, i.e. i_{ac} in phase with u_{ac1}.

A detailed switching model of single-phase PWM inverter with a triangular carrier frequency of 250Hz and a reference voltage of u_{ac}^{ref} with unipolar voltage switching technique is included for the switching model. In railway application system it is common to use the unipolar voltage switching. This type of switching has the advantage of doubling the effective switching frequency as far as the output harmonics are concerned, compared to the bipolar switching scheme [7], [8] .

In the average model,

, the PWM is simplified into a controlled current source that calculates the current based on the AC-side power divided by the DC-link voltage, at the converter DC-side of the model, v_{dc} at shown in equation (2).

$$i_{av}(t) = [i_{ac}(t) * u_{ac}(t)] / u_{dc}(t) \tag{2}$$

In the converter AC-side the PWM is simplified by a controlled voltage source which is controlled by the reference AC-voltage from the inverse park transformation block output u_{ac}^{ref}.

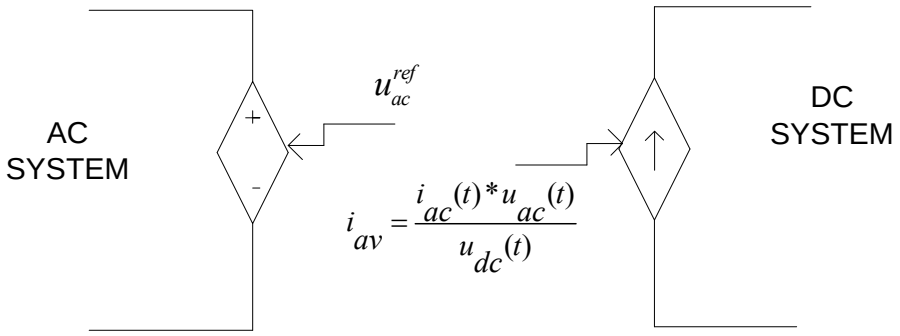

Fig 3 : Schematic representation of the PWM in the average model.

In addition, a *SOGI* is used for measurement of the line current i_{ac} as well. First-order low-pass filters are used for measurement of the u_{dc} and i_{dcm}.

Dead-time delay compensation technique

The up to date technology in motor control provides an adjustable voltage and frequency to the terminals of the motor through a pulse width modulated (PWM) voltage source inverter drive. In this type of drives, a dead time exists due to non-ideal characteristic of power switching devices. Although the dead time is short, it causes deviations from the desired fundamental output voltage. Despite the fact that each deviation does not significantly affect the fundamental voltage, the accumulated deviations result in reduced fundamental output voltage, distorted machine currents, and torque pulsations. The dead-time problem has already been investigated and several techniques of compensation has been proposed [9], [10].

For triangular carrier modulators, an average time delay from the reference voltage u_{ac}^{ref} to the actuated PWM terminal voltage u_{ac1} of half the switching frequency is assumed [11]. This average delay can be compensated by manipulating the synchronous rotating reference frame angle θ_{pll} as proposed in [5].

The analysis in [5] shows that the correction can be implemented as a modified $\alpha\beta$ transformation. It is also possible to implement a stand-alone correction, $v_{corr}(t)$,as in equation (3) and (4).where the inverter command vector is denoted as *v (t)*.

$$v_{corr}(t) = e^{j\omega 1(t)\tau} v(t) \tag{3}$$

On real-value vector form:

$$v_{corr}(t) = \begin{pmatrix} \cos\omega_1(t)\tau & \sin\omega_1(t)\tau \\ -\sin\omega_1(t)\tau & \cos\omega_1(t)\tau \end{pmatrix} v(t) \tag{4}$$

The compensation angle, θ_{comp}, in equation (5) for $\tau = \frac{1}{2} T_{sw}$ and $\omega_1(t) = 2\pi f_1$ is given by the switching frequency f_{sw} and the fundamental frequency, f_1, as shown in equation (6). This angle is compensated for the pulse width modulated (PWM)-switch model in *dq* to *αβ* transformation block as shown in the circled area of Fig 1.

$$\theta_{comp} = \omega_1(t)\tau\,[rad] \tag{5}$$

$$\theta_{comp} = \frac{\pi f_1}{f_{sw}}[rad] \tag{6}$$

Simulation Results

Switching and average model comparison

The result shown in Fig 4 compares the average model and the switching model of the DC-link voltage when a 3.67MW step in motor power is added at 60km line. In both curves it is observed the typical second harmonic ripple twice the line frequency as expected in this case. In addition, in the switching model a ripple due to the semiconductor switching which is twice the switching frequency due to use of unipolar voltage switching is observed.

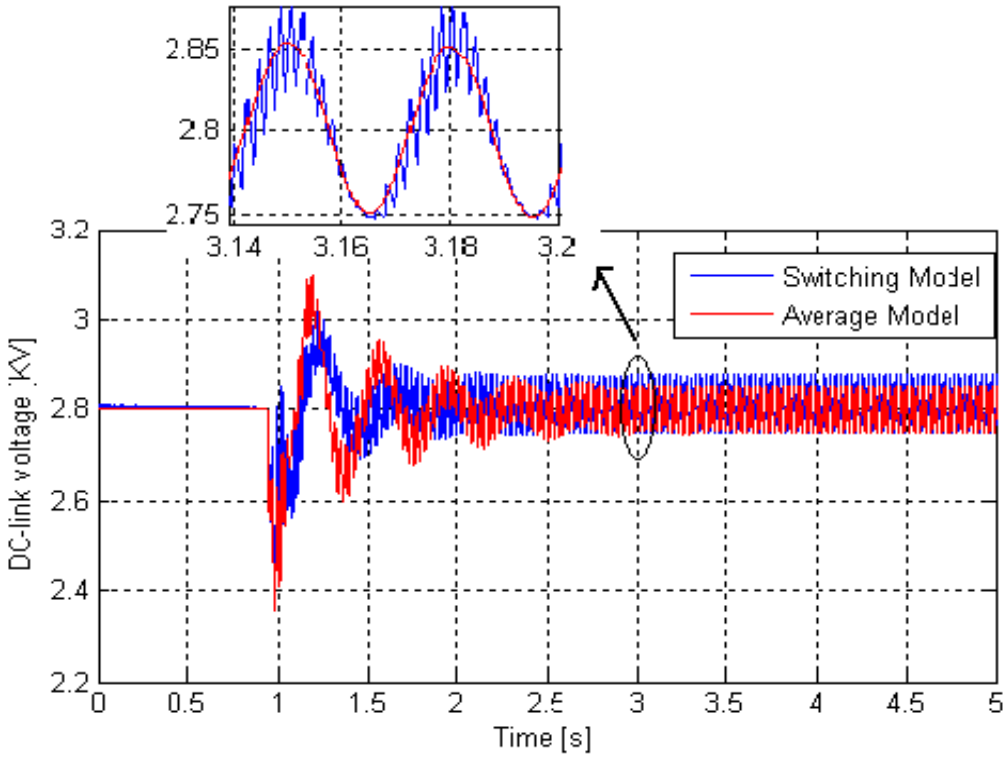

Fig 4 : Response in dc-link voltage when a 3.67MW step in motor power is added at 60km line for the two models.

In order to see the low frequency behavior of this response for the two models Fig 4 is averaged in a period of $T = 1/f_1[\text{sec}]$ and is shown in Fig 5.

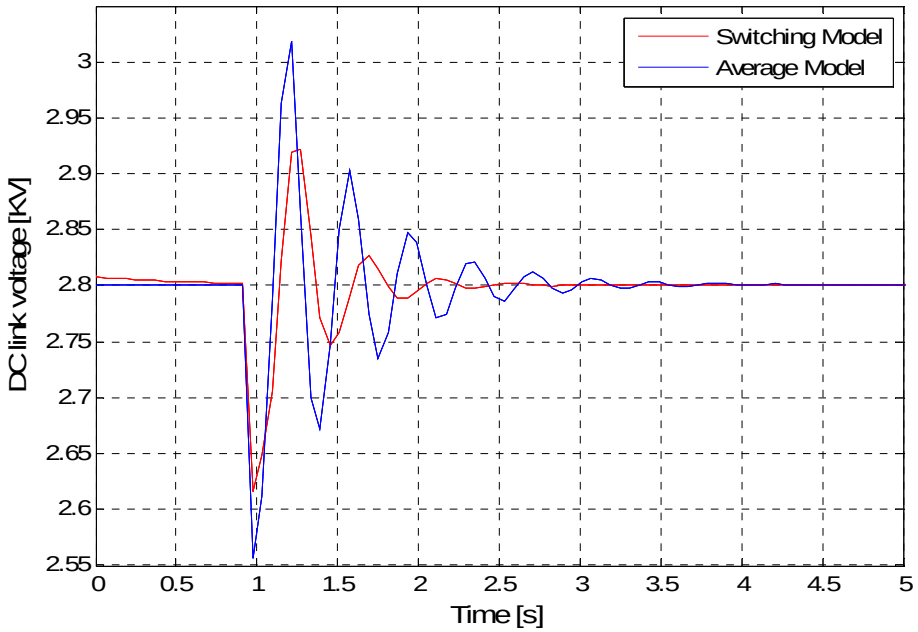

Fig 5 : Low frequency oscillation of DC-link voltage compared for the two models.

Table 2: Comparison of switching and average model

	Average model	Switching model
Settling time	2.5seconds	1.5seconds
Frequency of oscillation	2.67Hz	2Hz

The frequency of oscillation and the settling time for the switching and average model is calculated and given in Table 1. As we can see in the table the switching model has a better damping, less settling time and lower amplitude overshoot (Fig 5).

In the switching model the losses in the converter (the averaged dissipated power $P_D\ (t)$ in the semiconductor devices) can be obtained by subtracting the power output, $P_{output}\ (t)$, from the converter to the power input, $P_{input}\ (t)$, to the converter as shown in equation (7).

$$P_D(t) = P_{input}(t) - P_{output}(t) \tag{7}$$

This loss when the load consumes 3.67MW power is calculated in PSCAD and shown in Fig 6. The converter has a loss of 0.218MW which is 6% of the total power. A first-order low-pass filter is used for measurement of the loss.

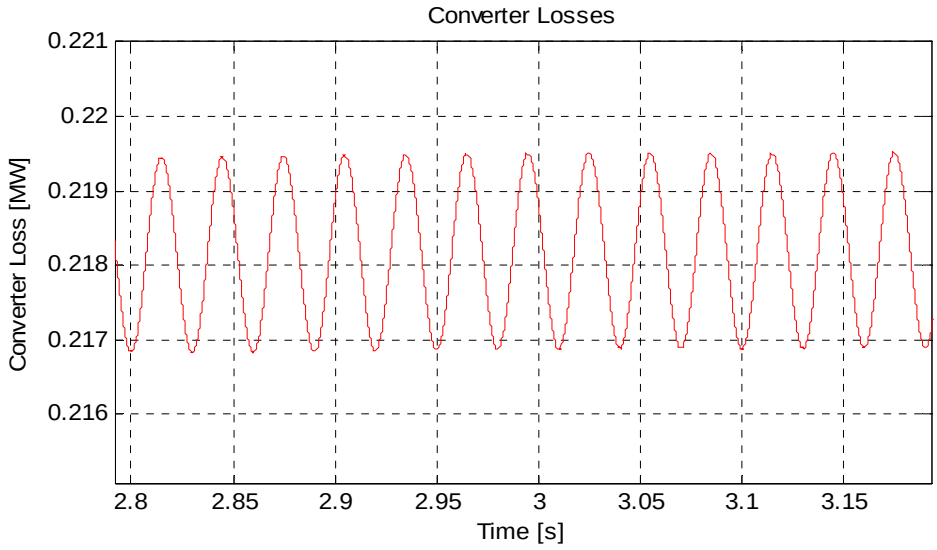

Fig 6: Calculated converter loss by equation (7) in PSCAD.

Stability limit investigation for average and switching model

For the purpose of investigating the stability limit of the models a time simulation method is carried out in EMTDC/PSCAD. The line length is increased by increasing the line parameters in the model. Fig 7 shows the DC- link voltage measurement for different line lengths at no load scenario. The line is increased in both the switching model and average model and the plots are shown in the right and left side of Fig 7 respectively.

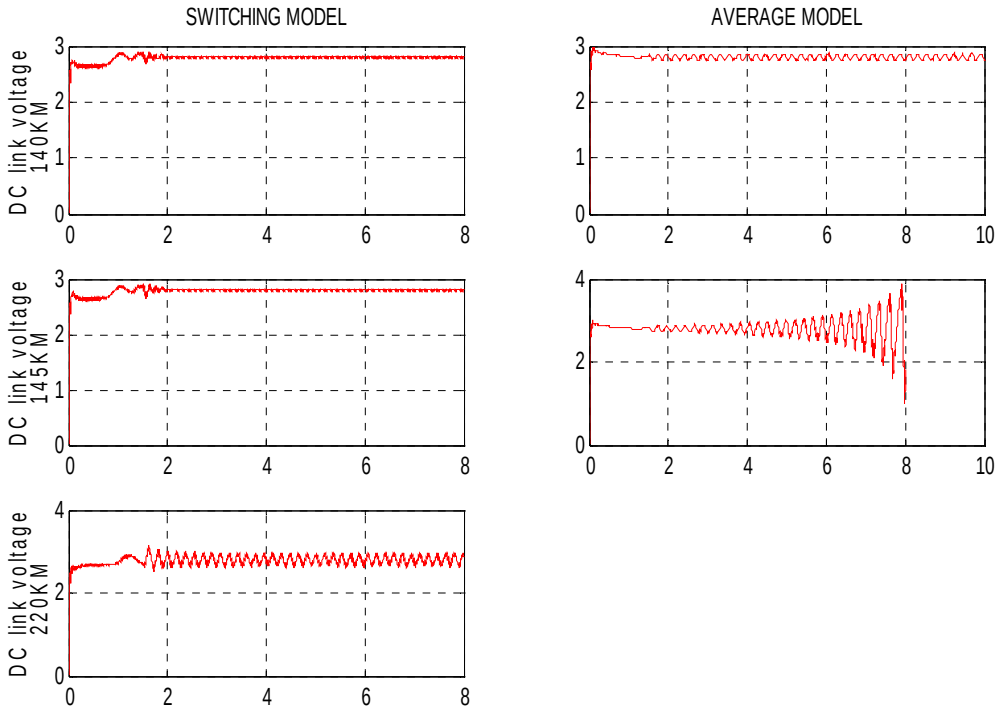

Fig 7 : Stability limit Investigation on the average and switching model

The result in the figure shows at 145km the average model DC-link voltage is oscillating and the amplitude of oscillation is growing. This is DC-link voltage instability. However, at the same line length the switching model DC-link voltage is well damped.

In the low frequency oscillation comparison shown previously in Fig 5 the switching model is more damped and has lower overshoot compared to the average model. This result agrees with the stability limit investigated in Fig 7 which gives the switching model a longer stability limit.

The switching model have a detail converter model which adds 6% converter loss as described previously, The phenomenon which adds a damping effect is not well understood however this analysis proves that the switching of the semiconductor adds a damping effect.

Compensated and non-compensated model

Fig 8 shows the comparison of dc-link voltage response for a 3.67MW step in motor power between the dead time compensated model and non-compensated model.

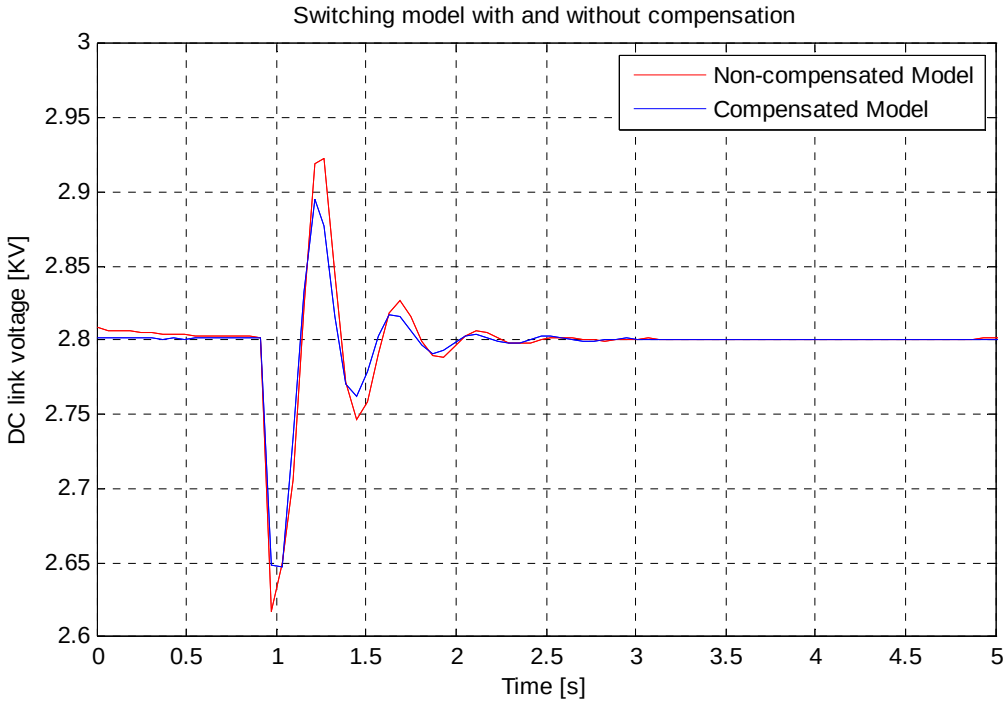

Fig 8: DC-link voltage response with and without the dead time compensation.

The simulation is carried out to improve the delay in DC- link voltage control loop caused by the switching dead time by using the proposed compensation method in the inverse-park transformation block of the control loop.

The dead- time compensated and non-compensated comparison is shown in Fig 8. The delay is compensated during transients as can be seen from the figure and can be neglected in the average model since semiconductor switching is not included in the simplified model. Moreover, the delay in DC- link voltage control loop caused by the switching dead time effect was improved in terms of transient overshoot by compensation of dead time in the inverse-park transformation block of the control loop.

Conclusion

In this paper VSC for traction power system with and without including the detailed PWM switching is modeled. The effect of semiconductor switching on the low frequency behavior of the dc-link voltage when a 3.67MW step power is added at 60km line is investigated. Furthermore, the performance of a PWM time delay compensation technique is analyzed.

From the presented results, the average model gives less realistic representation of the converter dynamics concerning transient oscillations. Therefore the detailed model with the PWM switching gives an improved representation of the system from the low frequency behavior point of view. Moreover, the delay in DC- link voltage control loop caused by the switching dead time effect was improved by compensation of dead time in the inverse-park transformation block of the control loop.

In order to study the low frequency behavior for stability limit investigation of a traction system, a detailed semiconductor switching (PWM) - model, which takes into account the semiconductor non linearity needs to be modeled and well understood. The same investigation could also be done with the average model by including an equivalent representation of the effect of the switching action that can give the same low frequency response as in the detailed switching model.

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E. DETAILED PSCAD MODEL USED IN THE THESIS

The detailed PSCAD models and the matlab code used in this thesis work are attached in a CD-ROM.