CHAPTER 5

Amplifiers

In the realm of instrumentation, signals coming from sensor outputs can be quite weak, and in such cases some signal enhancement clearly may be desirable. That is, signal amplification is needed. Indeed, amplification is one of the fundamental manipulations that can be performed on a signal. Amplifiers have played a key role throughout the history of electronics, appearing first in vacuum tube form, then as transistor-based designs, and most recently packaged into integrated circuits.

The advent of integrated circuit amplifiers has transformed the world of applied electronics (including instrumentation) because these amplifiers are complete units. The amplifier embedded within a package might contain dozens of transistors in a complex circuit, but the user need not be troubled by the details of the design. The "chip" only requires simple power supply connections and is promptly up and running. Consistency of performance and reliability are hallmarks of modern integrated circuits.

In its ideal form, an amplifier generates an output that is A times the input, regardless of the input signal strength or frequency. Real amplifiers have limitations in both respects, but for the moment we shall assume ideal behavior.

A differential amplifier (see Fig. 5.1) has two inputs, usually labelled + and −, or equivalently, *noninverting* and *inverting*.

The output voltage is given by the fundamental relationship

$$\boxed{V_{\text{out}} = A\,(V_+ - V_-)}, \tag{5.1}$$

where A is the amplifier gain. Of course, if the inverting input is grounded, then $V_{\text{out}} = A\,V_+$, so the behavior reverts to a conventional single-channel amplifier. In other words, the single-input amplifier can be thought of as simply a special case of the more general differential amplifier.

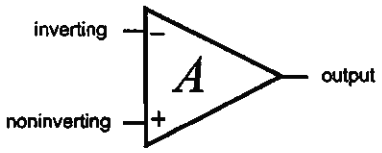

FIGURE 5.1. Symbol for a differential amplifier with intrinsic gain A.

An equivalent circuit model for a differential amplifier is shown within the dashed rectangle in Fig. 5.2. A source feeding the amplifier "sees" an input resistance r_{in}. Looking into the output terminal, the amplifier appears as a source equal to $A\ V_{in}$ feeding a series output resistance r_o. For an ideal amplifier, $r_{in} \rightarrow \infty$ and $r_{out} \rightarrow 0$.

The differential form of the amplifier has assumed preeminence because so many differential amplifiers are commercially available as integrated circuits. As a matter of fact, it is a rather special form of differential amplifier that is in widespread use: the so-called *operational amplifier*. An ideal op-amp is just an ideal differential amplifier with an exceedingly large gain ($A \rightarrow \infty$). Actual integrated circuit op-amps have typical gains of 10^4–10^6.

In use, a differential amplifier must be connected to the required power supplies. For many if not most IC devices, bipolar supplies are needed, say ±15 V, and so three pins on the IC package are assigned to $+V_{bias}$, $-V_{bias}$, and ground. Reality dictates that the amplifier output cannot exceed the positive supply level (sometimes termed the positive "rail"), nor can the output fall below the negative rail. This means, for example, that with ±15 V supplies, a differential input of 2 V coupled with a gain of $A = 100$ would only generate an output of approximately 15 V, not $100 \times 2 = 200$ V. For most applications, this saturating behavior must be avoided in order for the output to remain a linear function of the input. Nonlinearities generally lead to the undesirable effects of distortion.

Given the earlier remark about the enormous gain of operational amplifiers, and the observation concerning power supplies and saturation, it might seem that an op-amp would be almost useless for conditioning all but the tiniest signals. This would indeed be the case, except that op-amps are not normally employed

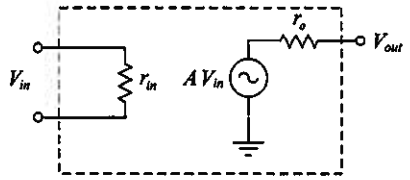

FIGURE 5.2. Equivalent internal circuit for the differential amplifier.

in bare form. With the addition of a few resistors, amplifiers possessing improved performance and reasonable overall gain can be achieved, as we shall now see.

5.1 NONINVERTING AMPLIFIER

Consider the schematic in Fig. 5.3. The combination of R_1 and R_F acts as a simple voltage divider on V_{out}, so

$$V_1 = \frac{R_1}{R_1 + R_F} V_{\text{out}}.$$

Also, from the fundamental relationship for a differential amplifier,

$$V_{\text{out}} = A\,[V_{\text{in}} - V_1]\,.$$

Combining these two expressions,

$$V_{\text{out}} = A\left[V_{\text{in}} - \frac{R_1}{R_1 + R_F} V_{\text{out}}\right]$$

or

$$V_{\text{out}} = V_{\text{in}}\left[\frac{A}{1 + A\frac{R_1}{R_1+R_F}}\right],$$

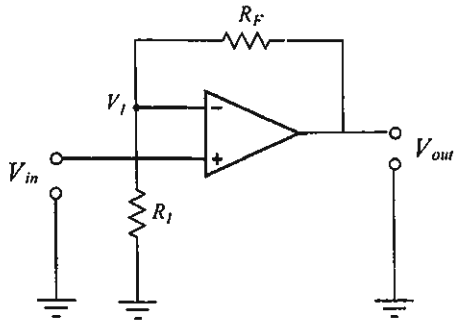

FIGURE 5.3. Noninverting amplifier based on a single op-amp.

and finally

$$V_{\text{out}} = V_{\text{in}} \left[\frac{1}{\frac{1}{A} + \frac{R_1}{R_1+R_F}} \right]. \tag{5.2}$$

The square bracket in this equation is a numerical factor relating output to input voltage for the particular configuration selected here. If the circuit in Fig. 5.3 is taken as a single entity with an input and an output, then this numerical factor is its gain. To distinguish this gain from the parameter A, which is an intrinsic property of the bare differential amplifier, A is termed the *open-loop gain*, and the amplification factor for the complete configuration is called the *closed-loop gain*, G. Hence,

$$G = \frac{1}{\frac{1}{A} + \frac{R_1}{R_1+R_F}}. \tag{5.3}$$

As noted earlier, an op-amp is a differential amplifier with enormous open-loop gain, in which case Eq. (5.3) has the limiting form

$$\boxed{\lim_{A\to\infty} G = 1 + \frac{R_F}{R_1}}, \tag{5.4}$$

so the closed-loop gain is set by the ratio of the two resistors. For a real op-amp, the open-loop gain might be something like 100,000 (an almost useless value, as was noted earlier), but the closed-loop gain can easily be set to more desirable levels such as 5, 10, or 50.

Because the square bracket in Eq. (5.2) is always a positive quantity, the polarity of the output voltage is the same as the polarity of the input. Hence, this configuration is referred to as a noninverting amplifier.

Input Resistance

Combining the schematic for the noninverting amplifier (Fig. 5.3) with the equivalent circuit for an op-amp (Fig. 5.2), we obtain as a composite representation Fig. 5.4. The driving source feeding V_{in} must also supply an appropriate input current I_{in}. The effective input resistance is thus

$$R_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}}. \tag{5.5}$$

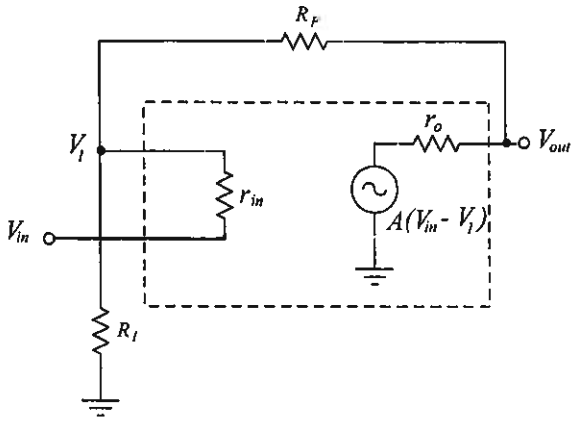

FIGURE 5.4. Combination of external wiring and internal equivalent circuit for a complete noninverting configuration.

The input current may be expressed

$$I_{\text{in}} = \frac{V_{\text{in}} - V_1}{r_{\text{in}}}. \tag{5.6}$$

Furthermore, if r_{in} is large compared to both R_1 and R_F,

$$V_1 = \frac{R_1}{R_F + R_1} V_{\text{out}} \tag{5.7}$$

and, using Eq. (5.2) for V_{out},

$$V_1 = \left[\frac{R_1}{R_F + R_1}\right] V_{\text{in}} \left[\frac{1}{\frac{1}{A} + \frac{R_1}{R_1 + R_F}}\right]. \tag{5.8}$$

Substituting this expression for V_1 into Eq. (5.6) and simplifying,

$$\boxed{R_{\text{in}} = r_{\text{in}} \left[1 + A \frac{R_1}{R_1 + R_F}\right]}. \tag{5.9}$$

As this equation makes clear, the effective input resistance (R_{in}) of the noninverting configuration is increased over the input resistance (r_{in}) of the bare op-amp, and if the open-loop gain A is large, the increase in this resistance will be substantial.

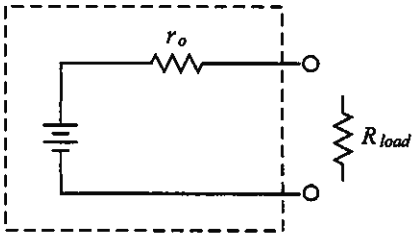

FIGURE 5.5. Preliminary consideration for determining amplifier output impedance.

Output Resistance

Suppose a battery and a resistor are connected in series, as indicated in Fig. 5.5. The output voltage will drop to exactly one-half if a load resistor equal in value to the internal resistance is added. This observation provides a method for determining output resistance:

- the output resistance is equal to that value of external load which will cause the ouput signal to drop by 50%.

Now apply this concept to the noninverting amplifier. As a first step, note that the equations leading to Eq. (5.2) must be modified when there is a load resistance.

$$V_1 = \frac{R_1}{R_1 + R_F} V_{\text{out}}$$

as before, but

$$\frac{A\,[V_{\text{in}} - V_1] - V_{\text{out}}}{r_o} = \frac{V_{\text{out}}}{R_L} + \frac{V_{\text{out}} - V_1}{R_F}. \tag{5.10}$$

Equation (5.10) expresses current conservation at the output node (see Fig. 5.6). From this pair of relations, the noninverting amplifier closed-loop gain can be derived:

$$G = \frac{1}{\left[\frac{R_1}{R_1+R_F} + \frac{1}{A}\right] + \frac{r_o}{AR_L} + \frac{r_o}{A(R_1+R_F)}}. \tag{5.11}$$

Comparing this to Eq. (5.3), it is apparent that the addition of a finite load resistance (R_L) on the amplifier output causes the closed-loop voltage gain to

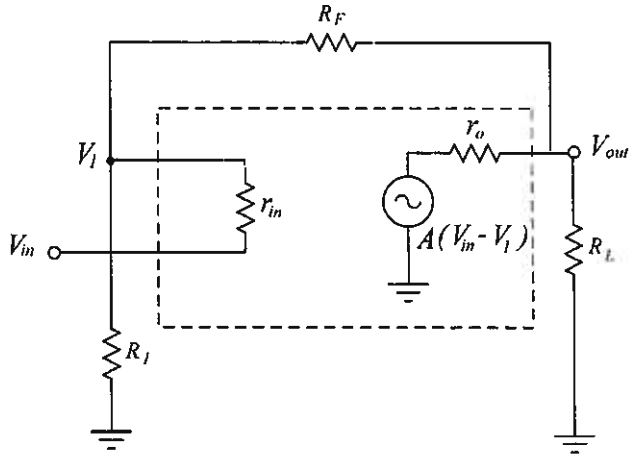

FIGURE 5.6. Addition of load resistance to the noninverting amplifier.

diminish. Incidentally, this expression differs slightly from Eq. (5.3), even when the limit $R_L \to \infty$ is reimposed. This is because the op-amp output resistance r_o is now accounted for, whereas it was not included in the slightly simplified derivation of Eq. (5.3).

Now let us determine the special value for a load resistance R_L such that the closed-loop gain from Eq. (5.11) becomes just half the value it has when $R_L \to \infty$—this will of course then equal the output resistance we are seeking. The algebra is a little tedious, but straightforward, and leads to

$$R_{\text{out}} = R_L = r_o \left[\frac{1}{1 + \frac{AR_1 + r_o}{R_1 + R_F}} \right]. \tag{5.12}$$

Neglecting r_o compared to AR_1, we arrive at

$$\boxed{R_{\text{out}} = r_o \left[\frac{1}{1 + A\frac{R_1}{R_1 + R_F}} \right]}, \tag{5.13}$$

which is the required expression for the output resistance of the noninverting amplifier. Clearly, a large open-loop gain A will cause the output resistance to become even smaller than the bare op-amp value of r_o.

Remarks

Equations (5.9) and (5.13) show that the input resistance is raised whereas the output resistance is lowered in the noninverting configuration. Both effects, if

anything, are desirable in an amplifier. The origin of this behavior is the feedback provided by resistor R_F. Note that in the limit $R_F \to \infty$, these equations lead to $R_{\text{in}} = r_{\text{in}}$ and $R_{\text{out}} = r_{\text{o}}$, as expected.

Now, reconsider Eq. (5.8):

$$V_1 = \left[\frac{R_1}{R_F + R_1}\right]\left[\frac{1}{\frac{1}{A} + \frac{R_1}{R_1 + R_F}}\right] V_{\text{in}}.$$

It is immediately apparent from this expression that

$$\lim_{A\to\infty} V_1 = V_{\text{in}}. \tag{5.14}$$

Therefore, the potential at the inverting input to the op-amp is held continuously to almost exactly match the potential at the noninverting input.

$$\boxed{V_- \simeq V_+}. \tag{5.15}$$

This property is also a direct consequence of the negative feedback provided by R_F.

5.2 INVERTING AMPLIFIER

The second standard configuration for an op-amp is shown in Fig. 5.7. As always, $V_{\text{out}} = A\left[V_+ - V_-\right]$, and since $V_+ = 0$ here,

$$V_{\text{out}} = -AV_1.$$

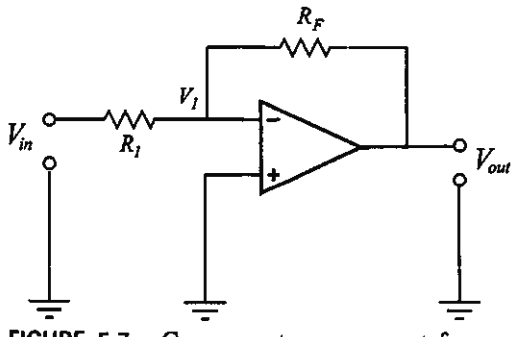

FIGURE 5.7. Component arrangement for an inverting amplifier based on a single op-amp.

Also, from current conservation at the inverting node,

$$\frac{V_{\text{in}} - V_1}{R_1} = \frac{V_1 - V_{\text{out}}}{R_F}.$$

From these two expressions is obtained

$$V_{\text{out}} = V_{\text{in}} \left[\frac{-\frac{R_F}{R_1}}{1 + \frac{1}{A}\left[\frac{R_1 + R_F}{R_1}\right]} \right]. \tag{5.16}$$

Hence, the closed-loop gain is

$$G = -\left[\frac{R_F}{R_1}\right] \left[\frac{1}{1 + \frac{1}{A}\left[\frac{R_1 + R_F}{R_1}\right]} \right]. \tag{5.17}$$

The negative sign here means that a positive input becomes a negative output, and conversely. Thus, this configuration is called an inverting amplifier. For op-amps, the limiting gain is

$$\boxed{\lim_{A \to \infty} G = -\left[\frac{R_F}{R_1}\right]}. \tag{5.18}$$

Once again, the closed-loop gain is set by just the ratio of two resistors.

Input Resistance

The equivalent circuit for an inverting configuration is shown in Fig. 5.8. The input resistance is defined by

$$R_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}}.$$

But

$$I_{\text{in}} = \frac{V_{\text{in}} - V_1}{R_1}.$$

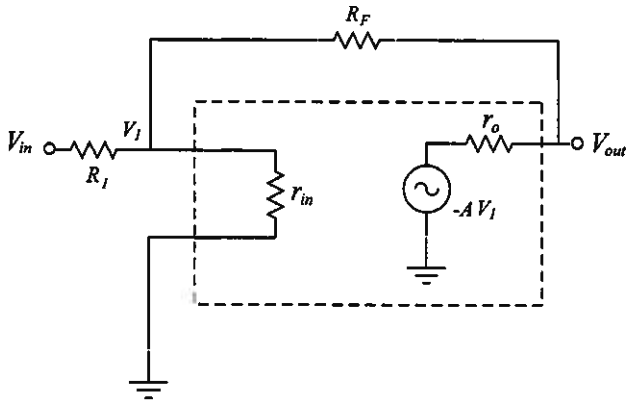

FIGURE 5.8. Inverting amplifier with internal equivalent circuit for the op-amp included.

Also, neglecting the voltage drop across r_0,

$$V_1 = -\frac{V_{\text{out}}}{A}$$

and V_{out} is given by Eq. (5.16). From these three relationships and assuming r_{in} to be very large compared to R_F, one obtains

$$R_{\text{in}} = R_1 \left[\frac{1 + \frac{1}{A}\left(\frac{R_1 + R_F}{R_1}\right)}{1 + \frac{1}{A}} \right], \tag{5.19}$$

which can also be written

$$\boxed{R_{\text{in}} = R_1 + \frac{R_F}{A+1}}. \tag{5.20}$$

In the limit of large open-loop gain,

$$R_{\text{in}} = R_1. \tag{5.21}$$

Thus the internal resistance of the op-amp, r_{in}, is not present in the net input resistance of this configuration.

Output Resistance

The output resistance can be obtained by first determining the closed-loop voltage gain when an external resistance R_L is added to the output and then finding what value of this load will drop the output amplitude by half. The result of this process

is that the output resistance of the inverting configuration is

$$\boxed{R_{\text{out}} = r_0 \left[\frac{1}{1 + A\frac{R_1}{R_1 + R_F}} \right]}, \tag{5.22}$$

which is identical to the expression [Eq. (5.13)] for the output resistance in the noninverting amplifier.

Remark

In the previous sections on the noninverting and inverting amplifiers, the closed-loop gains [Eqs. (5.3) and (5.17)], input resistances [Eqs. (5.9) and (5.19)], and output resistances [Eqs. (5.13) and (5.22)] all contained a common term

$$\beta \equiv \frac{R_1}{R_1 + R_F} = \frac{1}{1 + \frac{R_F}{R_1}}, \tag{5.23}$$

which is often called the *feedback factor*, since it quantifies the proportional amount of negative feedback.

5.3 DIFFERENCE AMPLIFIER

A third important configuration is shown in Fig. 5.9. Current conservation at the inverting and noninverting nodes gives

$$\frac{V_a - V_-}{R_1} = \frac{V_- - V_{\text{out}}}{R_F} \tag{5.24}$$

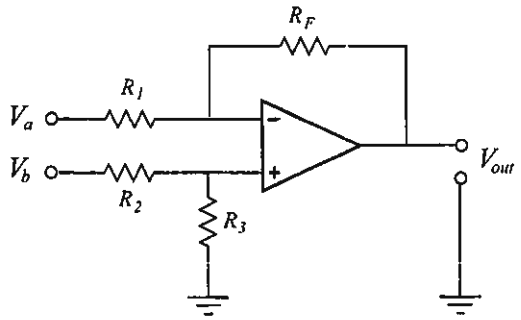

FIGURE 5.9. Difference amplifier based on a single op-amp.

or

$$V_- = \frac{R_1 R_F}{R_1 + R_F}\left[\frac{V_a}{R_1} + \frac{V_{\text{out}}}{R_F}\right], \tag{5.25}$$

and

$$\frac{V_b - V_+}{R_2} = \frac{V_+}{R_3} \tag{5.26}$$

or

$$V_+ = \frac{R_2 R_3}{R_2 + R_3}\frac{V_b}{R_2}. \tag{5.27}$$

Let us explicitly include at this point the assumption of a virtually ideal op-amp having extremely large open-loop gain and nearly infinite internal input resistance (r_{in}). Then, as we saw in the general result given in Eq. (5.15), negative feedback causes the potential at the inverting input to track the potential at the noninverting input: $V_+ = V_-$. Equating the right-hand sides of Eqs. (5.25) and (5.27),

$$\boxed{V_{\text{out}} = \left[\frac{1 + \frac{R_F}{R_1}}{1 + \frac{R_2}{R_3}}\right] V_b - \left[\frac{R_F}{R_1}\right] V_a}. \tag{5.28}$$

Hence, the output voltage is a weighted difference of the input voltages. If we make the particular choice

$$\frac{R_F}{R_1} = \frac{R_3}{R_2} = k, \tag{5.29}$$

then

$$V_{\text{out}} = k\,(V_b - V_a)\,. \tag{5.30}$$

In other words, this specific condition on the resistor ratios yields an output which is just a constant times the difference in the input voltages.

5.4 SUMMING AMPLIFIER

As a final important and useful configuration, consider the circuit shown in Fig. 5.10. Equating currents entering and leaving the connection node at the

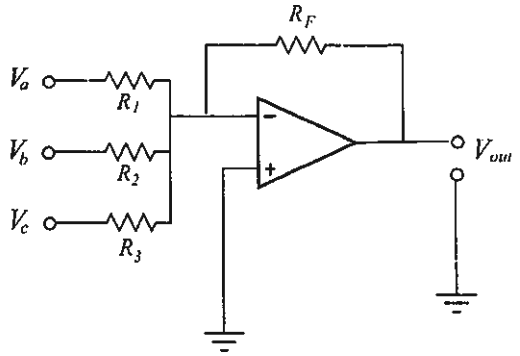

FIGURE 5.10. Summing amplifier based on a single op-amp.

inverting input,

$$\frac{V_a - V_-}{R_1} + \frac{V_b - V_-}{R_2} + \frac{V_c - V_-}{R_3} = \frac{V_- - V_{\text{out}}}{R_F}. \tag{5.31}$$

Again, the equality of potentials at the inverting and noninverting inputs is invoked: $V_+ = V_-$. But $V_+ = 0$ in this circuit, so

$$\frac{V_a}{R_1} + \frac{V_b}{R_2} + \frac{V_c}{R_3} = -\frac{V_{\text{out}}}{R_F}. \tag{5.32}$$

Finally,

$$\boxed{V_{\text{out}} = -\left[\left(\frac{R_F}{R_1}\right)V_a + \left(\frac{R_F}{R_2}\right)V_b + \left(\frac{R_F}{R_3}\right)V_c\right]}. \tag{5.33}$$

Therefore, the output voltage is a weighted sum of the input voltages (with a final inversion). By choosing appropriate resistor ratios, the weights can be set to any desired values, including unity.

This example included three input voltages, V_a, V_b, V_c, but the choice was arbitrary. In other words, any number of input voltages may be summed, and the extension of Eq. (5.33) is obvious.

5.5 FREQUENCY RESPONSE

In the previous sections of this chapter, the op-amp open-loop gain A has been treated as a constant. However, in reality this parameter varies with signal frequency. As might be expected of any ac function, a harmonic input signal of given frequency will experience both amplitude and phase changes in its passage

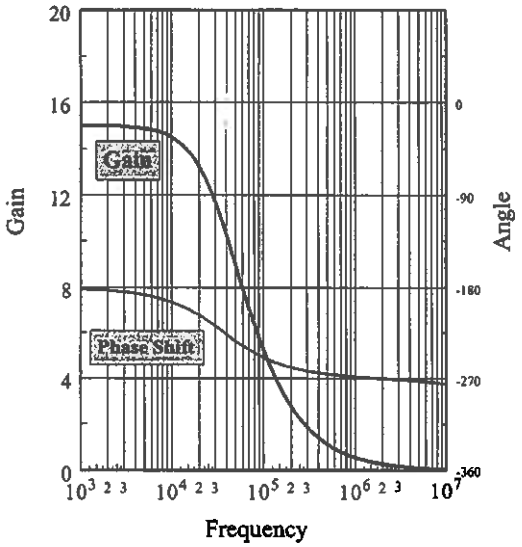

FIGURE 5.11. Gain and phase response for an inverting amplifier with $R_1 = 1$ kΩ and $R_F = 15$ kΩ.

through the op-amp. Figure 5.11 depicts these properties as they might be encountered for an inverting configuration based on a representative op-amp. The data were generated by a CAD circuit simulator package which accurately predicts real op-amp behavior.

In this sample design, R_1 was chosen to be 1 kΩ, and R_F was 15 kΩ. The expected closed-loop gain [Eq. (5.18)] would be -15. The gain magnitude is indeed equal to 15 for frequencies up to about 4000 Hz, after which there is a decided rolloff with increasing frequency. At $f \simeq 5 \times 10^5$ Hz, the gain equals unity. Above this frequency, $G \leq 1.0$ and the circuit actually attenuates the input signal rather than amplifying it.

Notice also that the phase shift begins at -180 degrees. This is due to the external conditions of the circuit, namely that it is in this case an inverting configuration (a noninverting circuit would initially exhibit 0 degrees). Figure 5.11 also reveals that additional amounts of shift develop as the frequency is changed. At high frequencies, the phase drops by an additional 90 degrees, resulting in a net value of about -270 degrees. This effect is caused by internal circuit characteristics of the op-amp itself.

It is common practice to express amplifier gain in units of decibels (dB), where the definition is contained in

$$G(\text{dB}) = 20 \log \left[\frac{V_{\text{out}}}{V_{\text{in}}} \right]. \tag{5.34}$$

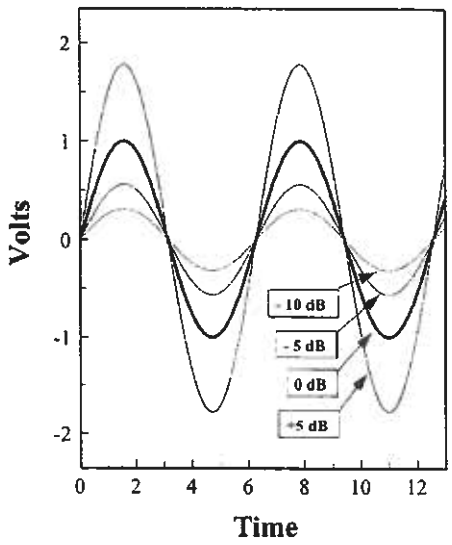

FIGURE 5.12. Illustration of relative magnitudes of a hypothetical ac signal increased and decreased in 5 dB increments.

As a visual aid to the decibel scale, Fig. 5.12 shows a hypothetical reference signal (in boldface), which serves as the 0 dB level, together with waveforms at +5 dB, −5 dB, and −10 dB. These units are quite nonlinear, as can be appreciated from the fact that 20 dB corresponds to a voltage ratio of 10, whereas 40 dB indicates a ratio of 100.

For the present example, the magnitude of the gain at low frequencies would be $20 \log(15) = 23.5$ dB.

As Fig. 5.13 illustrates, the high-frequency rolloff of the gain becomes almost linear when the vertical scale is in dB and the frequency axis is logarithmic.

The dashed line that approximates this linear limit has a slope of 20 dB/decade; that is, for each increase in frequency by a factor of 10 there is a corresponding drop in gain by a factor of 10. This line intercepts the low-frequency gain level (23.5 dB) at a value of f called the *corner frequency*, f_c; here $f_c \approx 4 \times 10^4$ Hz. Whereas the specific numbers that appear in Figs. 5.11 and 5.13 are particular to a given type of operational amplifier (324 in this example), the slope of the linear asymptote is the same for all op-amps. The reason for such a rate of decrease of gain will be made clear in the next section.

From the preceding discussion, it can be seen that to a first approximation amplifier gain is flat to a corner frequency, after which it rolls off at 20 dB/decade.

To push this illustrative example a little further, we now examine the effects of changing the feedback resistor in the inverting configuration, first to 5 kΩ

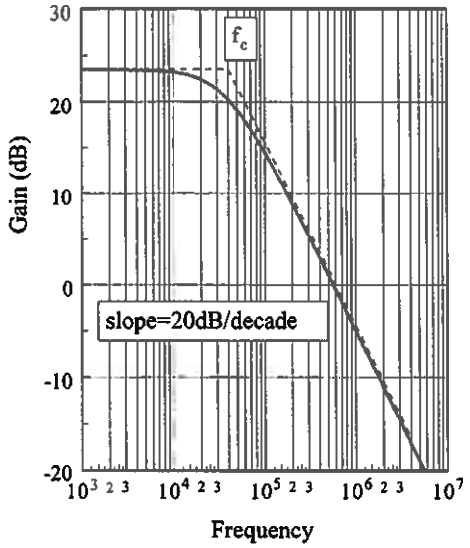

FIGURE 5.13. Gain versus frequency of the inverting amplifier using a vertical scale in decibels. The high-frequency rolloff is 20 dB per decade.

and then to 1 kΩ. In the first case, the magnitude of the low-frequency gain [Eq. (5.18)] should be 5 K/1 K = 5, which is 20 log(5) = 13.9 dB. In the second case, the gain is unity, which is equivalent to 20 log(1) = 0 dB. These two cases are combined with the previous example in Fig. 5.14.

Note that for designs possessing a smaller closed-loop gain, the corner frequency is higher. The corner frequency at unity gain (0 dB) can be estimated from the graph at about 2×10^5 Hz, an increase by a factor of nearly 5 over f_c when the gain was 15. Put another way, circuits with lower gain postpone rollover until higher frequencies. This can be viewed as a tradeoff of closed-loop gain for increased bandwidth.

The inverse of all of this is also true: higher closed-loop gains are matched by reduced bandwidth. The ultimate limit of this process is the bare op-amp itself, where the gain reverts to the open-loop value A. To quote a real-world example, the ubiquitous type 741 op-amp is listed as having $A \approx 2 \times 10^5$ and $f_c \approx 8$ Hz! The exceptionally small open-loop corner frequency coupled with the unmanageable gain (meaning its output will saturate with almost any input signal) makes an isolated op-amp fairly restricted in application.

Negative feedback therefore has at least two (there are actually more) beneficial effects: (1) reduction of net gain to more desirable levels; (2) increase in bandwidth to more usable levels.

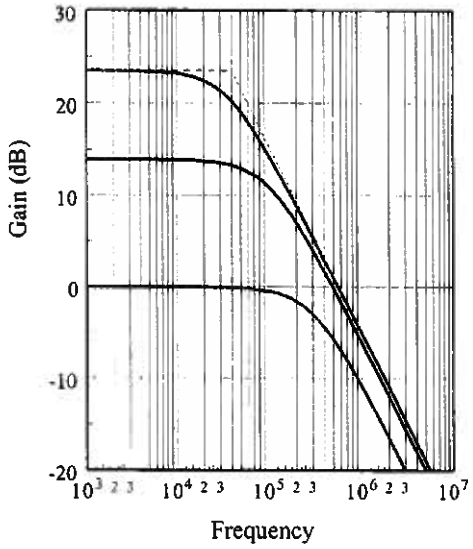

FIGURE 5.14. The previous example of an inverting amplifier, but with several different choices for the feedback resistor (and hence the gain). Notice that reduced gain is accompanied by increased bandwidth.

Complex Gain

To model the frequency dependence of an op-amp, the open-loop gain can be written as a complex function.

$$\boxed{A = A_0 \frac{1}{1 + j\left(\frac{f}{f_c}\right)}}. \tag{5.35}$$

Here, A_0 is the gain amplitude, f is the signal frequency, and f_c is a second constant, which will turn out to be a corner frequency. In complex notation, a harmonic signal is of the general form $V_0 e^{j(\omega t + \theta)}$. Suppose then we take the product of an input signal $V_{\text{in}} = V_1 e^{j\omega t}$ with a gain as expressed in Eq. (5.35):

$$V_{\text{out}} = V_1 e^{j\omega t} \, A_0 \frac{1}{1 + j\left(\frac{f}{f_c}\right)}. \tag{5.36}$$

Observing that

$$\frac{1}{1 + j\left(\frac{f}{f_c}\right)} = a \, e^{j\phi} \tag{5.37}$$

with

$$a = \frac{1}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}}, \tag{5.38}$$

$$\phi = \tan^{-1}\left[-\frac{f}{f_c}\right]. \tag{5.39}$$

Then,

$$V_{\text{out}} = V_1 \left[\frac{A_0}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}}\right] e^{j(\omega t + \phi)}. \tag{5.40}$$

This demonstrates that the magnitude of the amplified signal at low frequency is equal to $V_1 A_0$ and that it rolls off with increasing frequency (as the square root in the denominator becomes increasingly large). Additionally, the output leads the input by the phase angle ϕ given in Eq. (5.39). The two functions a and ϕ are plotted in Fig. 5.15. The similarity to Fig. 5.11 is obvious. Note that the phase

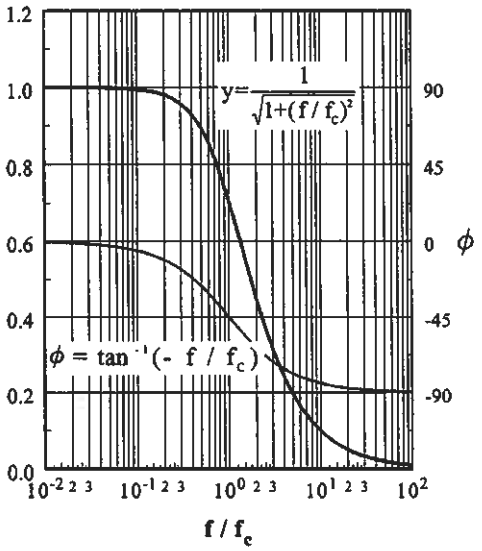

FIGURE 5.15. Magnitude and phase response expected from the complex representation of the op-amp open-loop gain function.

shift here, which reaches −90 degrees at high frequencies, is an intrinsic property of the amplifier model. The phase shift in Fig. 5.11 includes an additional −180 degrees because of the external inverting connection.

In the high-frequency limit, Eq. (5.38) becomes simply $a \rightarrow y = (x)^{-1}$, where $x = (f/f_c)$. In decibels, this is

$$y(\text{dB}) = 20\log[x^{-1}] = -20\log[x],$$

so at $x = 1$ (the corner frequency) $y = 0$ dB; at $x = 10$, $y = -20$ dB; at $x = 100$, $y = -40$ dB, and so on. This function, plotted on a graph with a logarithmic x axis, is a straight line beginning at the corner frequency and dropping at a rate of 20 dB/decade. In other words, it is the same type of high-frequency rolloff that was illustrated in Fig. 5.13.

Clearly, the complex gain given in Eq. (5.35) successfully replicates both the amplitude and phase transformations inherent in real op-amps.

Gain Bandwidth

As a further insight, suppose the noninverting configuration is reexamined with the formerly fixed A replaced with expression (5.35). We begin with Eq. (5.3) and for convenience use the feedback factor β as defined in Eq. (5.23). Hence,

$$G = \frac{1}{\frac{1}{A} + \beta},$$

which becomes

$$G = \frac{1}{\frac{1+j\frac{f}{f_c}}{A_0} + \beta}$$

or

$$G = \frac{A_0}{(1 + A_0\beta) + j\left(\frac{f}{f_c}\right)}. \tag{5.41}$$

This equation may be rewritten in the standard form

$$G = G_0\left[\frac{1}{1 + j\left(\frac{f}{f_c}\right)}\right] \tag{5.42}$$

with

$$G_0 = \frac{A_0}{1 + A_0\beta}, \tag{5.43}$$

$$f_c^* = (1 + A_0\beta)\, f_c. \tag{5.44}$$

Comparing Eq. (5.35) for the open-loop condition and Eq. (5.42) for the closed-loop configuration, it is apparent that the closed-loop gain has been reduced from A_0 to $A_0/(1 + A_0\beta)$, while the corner frequency has been increased from f_c to $(1 + A_0\beta)f_c$. An important observation we can make from these results is that

$$G_0 f_c^* = \frac{A_0}{1 + A_0\beta}(1 + A_0\beta)f_c = A_0 f_c. \tag{5.45}$$

In other words, the product of gain and bandwidth is the same for the bare op-amp as it is for the complete noninverting configuration.

As an exercise, the preceding procedures could be repeated for the inverting configuration, beginning with Eq. (5.17).

PROBLEMS

Problem 5.1. A noninverting amplifier has a feedback resistor $R_F = 5$ K and has the inverting input coupled to ground through a 20 K resistor. The op-amp has an open-loop gain $A = 20{,}000$, an input resistance $r_{in} = 100$ K, and an output resistance $r_o = 5\ \Omega$.

1. What is the voltage gain? [Ans. 1.2499].
2. What is the overall input resistance? [Ans. 1600 Meg].
3. What is the net output resistance? [Ans. 0.000312 Ω].

Problem 5.2. An op-amp is specified as having an open-loop gain of 150,000 and an open-loop bandwidth (corner frequency) of 10 Hz.

1. What is the approximate open-loop gain at 10 kHz? [Ans. 150].
2. If this op-amp is used in a noninverting configuration with $R_F = 40$ K and $R_1 = 10$ K, what will be the closed-loop gain and bandwidth? [Ans. 5 and 300,000 Hz].

CHAPTER 6

Special-Purpose Circuits

In the previous chapter, the basic properties of operational amplifiers were summarized, and a number of standard configurations were discussed. It was shown, for example, that very simple arrangements of a few resistors in combination with an op-amp could provide noninverting or inverting amplification. These circuits are actually both usable and useful for boosting weak sensor signals and for performing analog addition and subtraction.

Many other special-purpose circuits exist that are capable of performing unique transformations on analog signals. Several of these are discussed in the following sections.

6.1 UNITY-GAIN BUFFER

The noninverting configuration was discussed in the previous chapter; the schematic is repeated here (Fig. 6.1). Assuming a very large open-loop gain, the closed-loop gain was found to be

$$G = 1 + \frac{R_F}{R_1}.$$

Suppose now this arrangement is forced to the limit $R_F \to 0$ and $R_1 \to \infty$. A schematic incorporating these limits is depicted in Fig. (6.2). The closed-loop gain obviously becomes

$$\boxed{G = 1.0}. \tag{6.1}$$

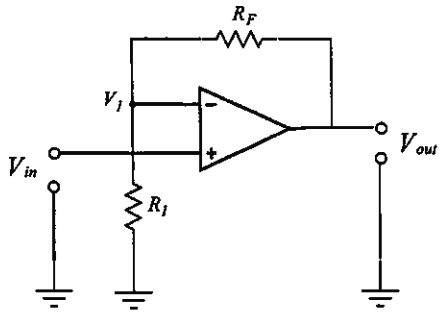

FIGURE 6.1. Noninverting amplifier.

Hence, output equals input. This may seem a rather pointless achievement until the input and output resistances are considered.

The input resistance is given by Eq. (5.9) in the appropriate limit, which is

$$\boxed{R_{\text{in}} = r_{\text{in}}\,[1 + A]}. \tag{6.2}$$

Typically, this will be extremely large, since r_{in} is large and A is very large. The output resistance is given by Eq. (5.13) in the appropriate limit. It is

$$\boxed{R_{\text{out}} = r_{\text{out}}\left[\frac{1}{1+A}\right]}. \tag{6.3}$$

For r_{out} small and A very large, clearly R_{out} is extremely small.

This circuit thus has unity gain, extremely high input resistance, and extremely small output resistance. These properties make it ideal for use as a buffer to isolate one section of a circuit from another.

As an example, consider the schematic in Fig. 6.3. The circuitry (the purpose of which we are not concerned with here) contained in the box labeled B has some input resistance r_{in}. Now, if the value of r_{in} is **not** very large compared to the resistor R_x, then directly attaching box B across R_x (omitting the buffer) would produce a parallel combination, R_x and r_{in}, whose resistance would certainly be less

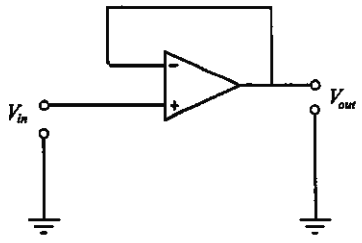

FIGURE 6.2. Unity-gain buffer.

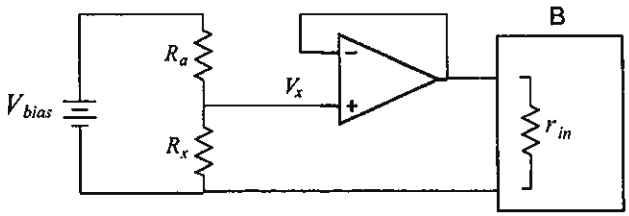

FIGURE 6.3. Use of a buffer to isolate one circuit from a second circuit whose input resistance is not large.

than the original R_x. This would decrease the voltage V_x so the subsequent signal transformations produced by B would not reflect the original signal across R_x.

On the other hand, if the buffer is inserted as shown, then R_x would be shunted only by a nearly infinite input resistance. Virtually no alteration in the signal V_x would occur.

6.2 INSTRUMENTATION AMPLIFIER

A special circuit with very useful properties is illustrated in Fig. 6.4.

Because the input pair of op-amps, A_1 and A_2, each have negative feedback resistors R, the potential at each noninverting input approximately equals the potential at the corresponding inverting input, as seen earlier in Eq. (5.15). This implies that the potential at the top of R_S is V_1, while the potential at the bottom of R_S is V_2.

Now, either $V_1 > V_2$ or $V_2 > V_1$. The operation of the circuit does not depend on which case applies, so without loss of generality we choose the situation $V_1 > V_2$. Consequently, $v_a > v_b$ and there will be a current flow I from v_a toward v_b down through the chain R, R_S, R.

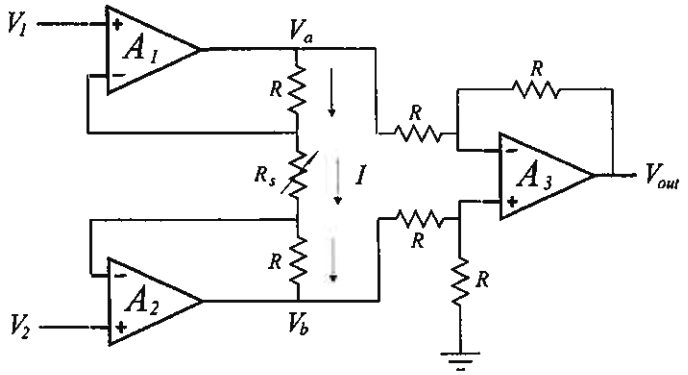

FIGURE 6.4. Instrumentation amplifier constructed from three op-amps. R_S is a single gain-setting resistor.

With these points in mind, the circuit operation may be derived as follows. Clearly,

$$IR_S = V_1 - V_2$$

or

$$I = \frac{V_1 - V_2}{R_S}.$$

Thus, since $v_a - V_1 = IR$,

$$v_a = V_1\left[1 + \frac{R}{R_S}\right] - V_2\left[\frac{R}{R_S}\right]. \tag{6.4}$$

Likewise, $V_2 - v_b = IR$, so

$$-v_b = V_1\left[\frac{R}{R_S}\right] - V_2\left[1 + \frac{R}{R_S}\right]. \tag{6.5}$$

Amplifier A_3 is configured in a standard difference arrangement and has an output given by Eq. (5.30),

$$V_{\text{out}} = k\,(v_b - v_a),$$

where $k = R/R = 1$ in this case. Using Eqs. (6.4) and (6.5),

$$\boxed{V_{\text{out}} = \left[1 + 2\frac{R}{R_S}\right](V_2 - V_1)}. \tag{6.6}$$

Thus, the overall circuit action is to provide differential amplification of the two inputs and to do so with a gain that is set by the resistor values R and R_S.

In an instrumentation amplifier, op-amps A_1, A_2, A_3 together with all resistors R are considered as internal to the device, whereas R_S may be viewed as the single external component: a gain-setting resistor. (Instrumentation amps are available commercially packaged as single-chip integrated circuits; in this form, R_S literally is an external component.) With this technique, gains of several hundred are easily achieved. Because the signal voltages V_1 and V_2 are fed directly to op-amp noninverting terminals, the input impedance of an instrumentation amplifier is very large ($\sim 10^9\ \Omega$).

Finally, it should be noted that any common voltage that might be present in both inputs V_1 and V_2 will be canceled in the output because of the differencing action in Eq. (6.6). For this reason, difference amplifiers, and instrumentation amplifiers in particular, are very useful when the signals of interest are superimposed on large, shared baselines.

Because of the imperfections of real circuits and amplifiers, the amplified output is better expressed by something like

$$V_{\text{out}} = G_D(V_2 - V_1) + G_C\left(\frac{V_2 + V_1}{2}\right). \tag{6.7}$$

That is, there is both a differential gain G_D, as in Eq. (6.6), and a common gain G_C, which operates on the average input. Ideally, G_C should be near zero, but a finite value implies that the output voltage will be contaminated by a buried component whose origin is not the signal of interest.

The ability to cancel shared baselines is quantified by a parameter known as the *common-mode rejection ratio* (CMRR). It is defined as

$$\text{CMRR} = \frac{G_D}{G_C}. \tag{6.8}$$

Obviously, in the ideal case with $G_C = 0$, CMRR would be infinite. Actual instrumentation amps can achieve CMRRs of about 10^5 or larger.

6.3 LOG AND ANTILOG AMPLIFIERS

Suppose an instrumentation application generates a signal which at times is quite small, whereas at other times it is comparatively large. This property is known as wide dynamic range. Audio signals often fall in this category, ranging from very soft to very loud. Wide dynamic range poses difficulties when further electronic processing of the signal is planned because either the low levels may drop out or the high levels may overload the electronics. A workaround is found in the technique of *compression*, where the signal is in effect rescaled, say with a *logarithmic converter*. After processing, an inverse scaling, or *decompression*, is applied. Clearly, an *antilog converter* would be needed for this task.

Alternatively, suppose that a transducer signal (transducers will be treated in Part III) is an exponential function of the physical parameter being monitored. This could, for example, apply to a thermistor temperature sensor. In such a

case, the transducer output can be *linearized* by passing it through a circuit with inverse scaling properties—a logarithmic converter.

The key to obtaining the desired nonlinear output from an op-amp circuit is the use of an appropriate nonlinear feedback element. A semiconductor diode is described by an expression of the form

$$I = I_0 \left[e^{qV/kT} - 1 \right], \tag{6.9}$$

where I is the current flowing through the diode, I_0 is the so-called reverse bias saturation current (a constant for any particular device), q is the electronic charge, V is the voltage across the diode, k is Boltzmann's constant (1.38×10^{-23} joule per kelvin), and T is the diode temperature expressed in absolute degrees (kelvin). At or near room temperature ($T \approx 300$ K), the factor kT/q is approximately 0.025 V. Hence, for even modest diode voltages

$$I \simeq I_0 \, e^{qV/kT}. \tag{6.10}$$

Log

When a diode is placed as illustrated in Fig. 6.5, the voltage output may be derived as follows. Clearly, $V_- = 0$ and so $I = V_{\text{in}}/R$. But this current also flows through the diode, and furthermore the diode voltage is expressed by $V = -V_{\text{out}}$. Hence,

$$\frac{V_{\text{in}}}{R} = I_0 \, e^{-qV_{\text{out}}/kT}$$

or

$$V_{\text{out}} = -\frac{kT}{q} \ln\left(\frac{V_{\text{in}}}{I_0 R}\right), \tag{6.11}$$

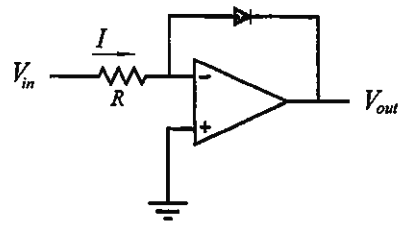

FIGURE 6.5. Log amplifier.

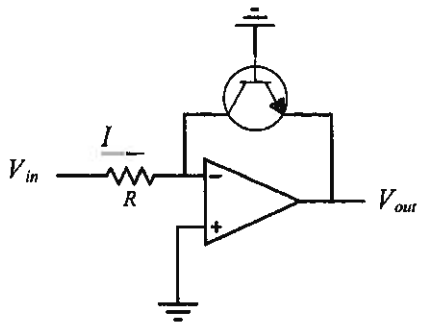

FIGURE 6.6. Log amplifier using an NPN transistor in place of a diode.

and finally

$$\boxed{V_{\text{out}} = -\left[\frac{kT}{q}\right]\ln(V_{\text{in}}) + \left[\frac{kT}{q}\ln(I_0 R)\right]}. \tag{6.12}$$

This expression is of the form $V_{\text{out}} = -a \ln V_{\text{in}} + b$, so the output voltage is a logarithmic function of the input voltage.

It is also possible to use an NPN transistor connected as shown in Fig. 6.6 to achieve essentially the same behavior. Note that the collector and base are both at ground potential, and that with positive V_{in} and consequently negative V_{out}, the base-emitter junction is forward-biased.

Antilog

For antilog operation, the resistor and diode are simply interchanged as indicated in Fig. 6.7. Now the equation for V_{out} is derived as follows. The forward diode drop is V_{in}. Hence,

$$I \simeq I_0 \, e^{\frac{qV_{\text{in}}}{kT}}. \tag{6.13}$$

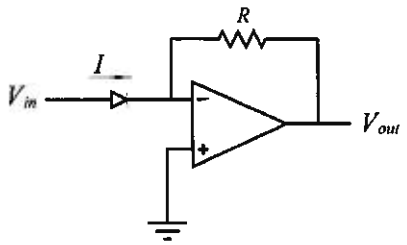

FIGURE 6.7. Antilog amplifier.

Also,

$$IR = -V_{\text{out}}. \tag{6.14}$$

Thus,

$$\boxed{V_{\text{out}} = -[I_0 R]\ e^{\left(\frac{q}{kT}\right)V_{\text{in}}}}. \tag{6.15}$$

In this case, the output voltage is an exponential (antilog) function of the input.

6.4 CONSTANT CURRENT SOURCE

Figure 6.8 shows an op-amp circuit that provides a current I to a load R_L. Because $V_- \approx V_+$ is assured by the negative feedback and $V_+ = 0$, the current through the input resistor is just

$$I = \frac{V_{dc}}{R}. \tag{6.16}$$

Virtually all of this current then flows through the load on account of the extremely high inpedance at the input terminals of the op-amp. In other words, the load current I is set only by V_{dc} and R and is independent of the particular value of the load resistance. Hence, the circuit depicted in Fig. 6.8 acts as a constant current source.

6.5 VOLTAGE AND CURRENT CONVERSION

Voltage-to-Current Converter

If the dc voltage input to Fig. 6.8 is replaced by a variable source as in Fig. 6.9, then the output current becomes

$$\boxed{I_{\text{out}} = \frac{V_{\text{in}}}{R}}. \tag{6.17}$$

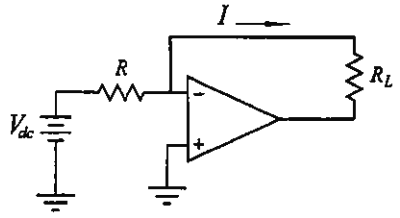

FIGURE 6.8. Constant current source.

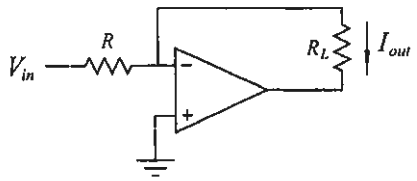

FIGURE 6.9. Voltage-to-current conversion circuit.

Thus, the input voltage has been transformed into an output current flowing through the load resistor.

Another possibility for voltage-to-current conversion is the arrangement in Fig. 6.10. For this circuit, the current I_{out} flows through R_L and R, so

$$I_{out} = \frac{V_-}{R}.$$

But $V_- = V_+ = V_{in}$,

$$I_{out} = \frac{V_{in}}{R}. \tag{6.18}$$

This is exactly the same as expression (6.17), so the two variants provide identical voltage-to-current conversion.

Differences exist in other aspects of the circuits. The input impedance of Fig. 6.10 is very high—a desirable condition for a voltage sensor in the same way that an ideal voltmeter has high input impedance, whereas the design of Fig. 6.9 is basically an inverting amplifier with an input impedance [see Eq. (5.21)] of only R. On the other hand, the dynamic range of the inverting configuration is larger.

Current-to-Voltage Converter

The inverse of the operation discussed in the previous section is current-to-voltage conversion. Analyzing the circuit shown in Fig. 6.11, and observing that

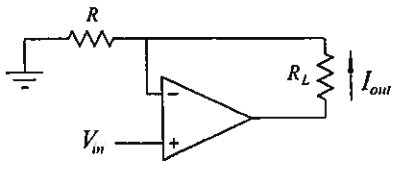

FIGURE 6.10. A second arrangement for voltage-to-current conversion.

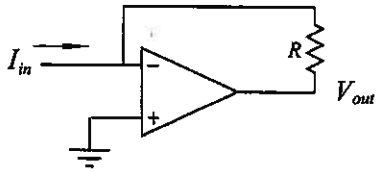

FIGURE 6.11. Current-to-voltage conversion.

the input current flows through the output resistor R,

$$\boxed{V_{\text{out}} = -I_{\text{in}}R}, \tag{6.19}$$

where $V_- = V_+ = 0$ has been applied. This configuration can be regarded as a limiting form of the standard inverting amplifier (Chapter 5) for which the input impedance was [Eq. (5.21)] R_1, which is zero in this case. Thus, the impedance that this converter presents to the source of current I_{in} is extremely small—a desirable property in the same sense that an ideal ammeter has nearly zero impedance.

6.6 ANALOG INTEGRATION AND DIFFERENTIATION

In the earlier section on log and antilog circuits, it was seen how the equivalent of either of two particular mathematical operations could be performed on given input voltages. Summing and differencing amplifiers, discussed in the previous chapter, are of course the analogs of addition and subtraction. Electronic counterparts of other mathematical operators also exist, including the functions of multiplication, division, and square root. In this section, we consider integration and differentiation.

Integrators

The quantity of charge on a capacitor and the potential difference across the capacitor are related: $Q = CV_C$. Therefore,

$$\frac{dQ}{dt} = C\frac{dV_C}{dt}.$$

But the rate of change of the charge residing on the capacitor plates is simply a current flowing onto or off of those plates, so

$$I_C = C\frac{dV_C}{dt} \tag{6.20}$$

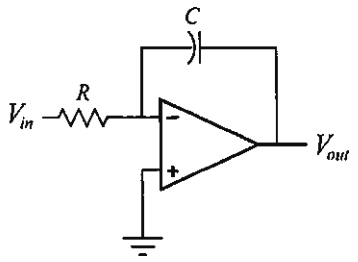

FIGURE 6.12. Analog integrator.

is the capacitor current. Notice that in the steady state (i.e., dc conditions) $I_C = 0$, which means simply that a capacitor can "carry" only ac currents.

Considering Fig. 6.12, this capacitor current is seen to be just V_{in}/R because, as usual, $V_- = V_+ = 0$. Hence,

$$\frac{V_{\text{in}}}{R} = -C\frac{dV_{\text{out}}}{dt}, \tag{6.21}$$

where we have used the fact that $V_{\text{out}} = -V_C$. From Eq. (6.21), it is evident that

$$\boxed{V_{\text{out}} = -\frac{1}{RC}\int V_{\text{in}}\, dt}, \tag{6.22}$$

so the output voltage is a time integration of the input voltage.

To illustrate the operation of an integrator, the circuit shown in Fig. 6.13 was created in the software simulation package PSpice (a product of MicroSim Corporation). Notice that a second op-amp has been added—it has a gain of 1 and is included simply to invert the integrator output. In this particular case, the overall response should be

$$V_{\text{out}} = \frac{1}{RC}\int V_{\text{in}}\, dt.$$

The voltage input was chosen to be a pulse sequence of amplitude 1.0 V, pulse width of 1.5 sec, and period of 2.5 sec. Figure 6.14 is a plot of the PSpice circuit simulation results. The output voltage is clearly seen to be just the integral of the input signal. Two further comments are in order. First, the PSpice schematic includes a timed switch which is placed across the integrating capacitor. This switch opens 0.01 sec after the simulation begins and guarantees that C_1 is initially discharged. Second, it should be remembered that op-amp output voltages cannot exceed power supply levels. With certain input waveforms it is quite easy to saturate the integrator output.

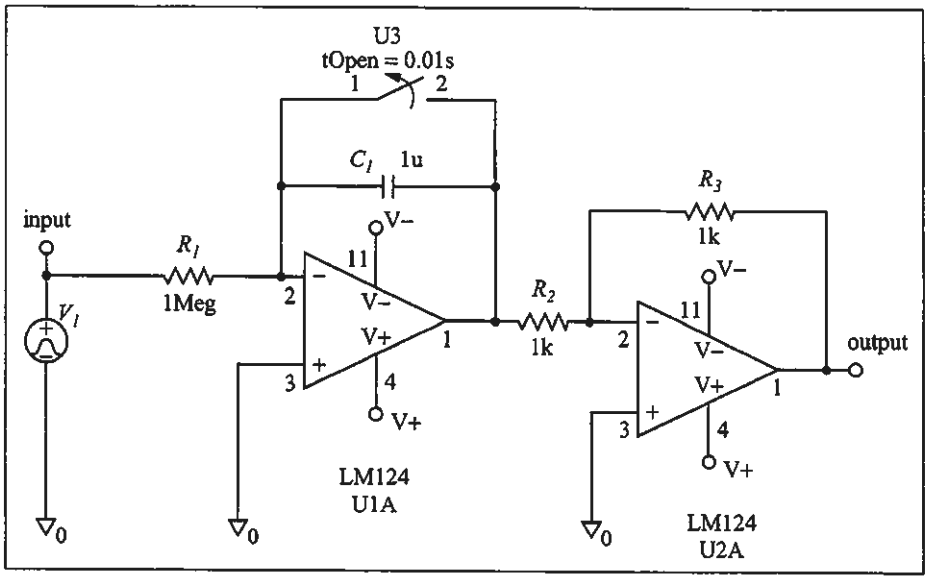

FIGURE 6.13. PSpice schematic of an analog integration circuit. The second op-amp is simply acting as an inverter.

Differentiators

By simply interchanging the resistor and capacitor in the integrator, a differentiator is formed. To see this, consider Fig. 6.15. As before, the capacitor current is the rate of change of charge buildup on the capacitor, so

$$I_{\text{in}} = C\frac{dV_{\text{in}}}{dt}. \tag{6.23}$$

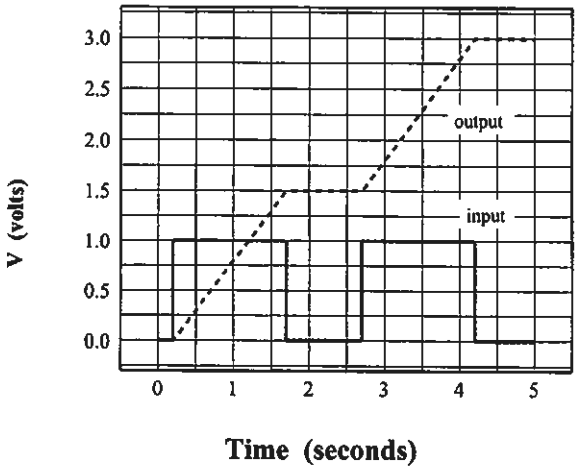

FIGURE 6.14. PSpice simulation results for the integrator.

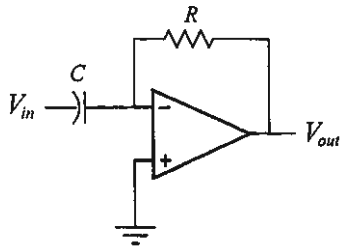

FIGURE 6.15. Analog differentiator.

But

$$V_{\text{out}} = -I_{\text{in}}R,$$

and thus

$$\boxed{V_{\text{out}} = -RC\frac{dV_{\text{in}}}{dt}}. \tag{6.24}$$

Therefore, this circuit "differentiates" the input signal.

As with the integrator, the operation can be demonstrated with the aid of a PSpice simulation. The schematic for this example is shown in Fig. 6.16. The 1 nF capacitor across R_1 is included to prevent ringing oscillations at the output of the first op-amp which otherwise occur when the input voltage pulse reaches its corner points. Here, too, an inverting stage has been added for convenience in

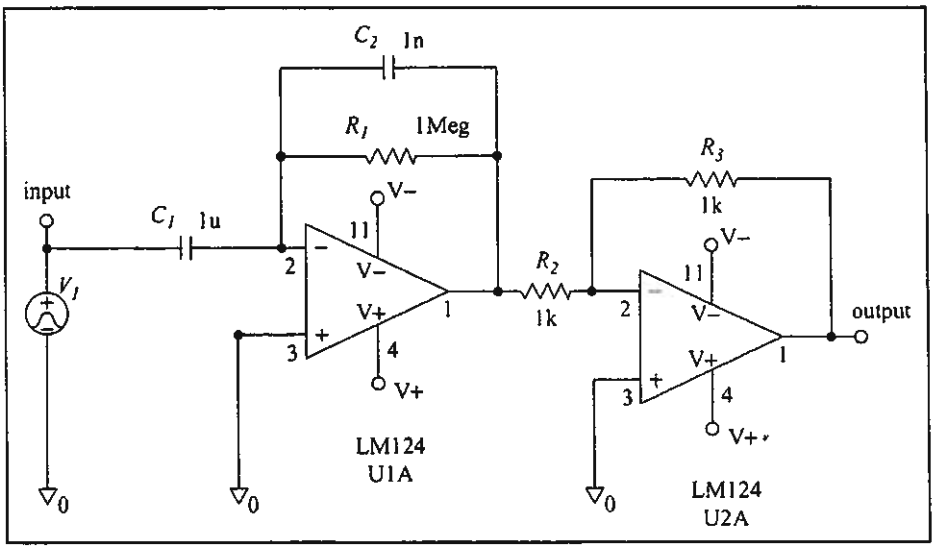

FIGURE 6.16. PSpice schematic for an analog differentiator. The second op-amp functions simply as an inverter.

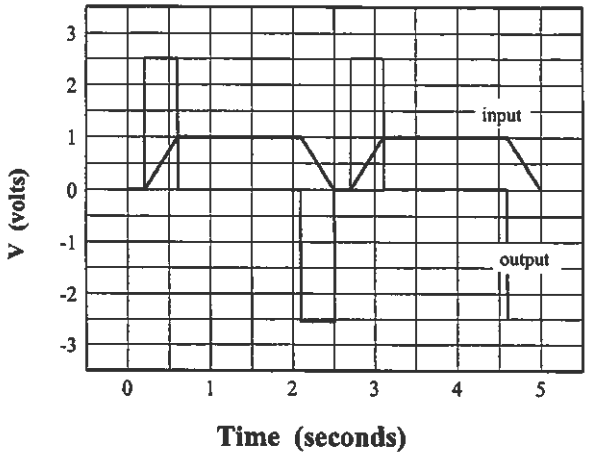

FIGURE 6.17. PSpice simulation results for the analog differentiator.

representing the output, which is plotted in Fig. 6.17. Where the input signal is flat (constant), the derivative is zero and the output is zero. During the linear ramp phases of the input, the slope is constant, and the output rises or falls abruptly to the value 2.5 V.

PROBLEMS

Problem 6.1. Consider the sawtooth waveform shown in Fig. 6.18. The vertical axis is in volts and the horizontal axis is in seconds.

1. If this signal is fed to an integrator circuit with $R = 1$ Meg and $C = 5\ \mu$F, describe the resulting output waveform. Caution: the integral of a linear function is not itself a linear function.
2. If this signal is fed to a differentiator circuit with $R = 1$ Meg and $C = 5\ \mu$F, describe the resulting output waveform.

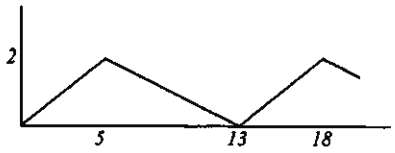

FIGURE 6.18. Problem 6.1.

Problem 6.2. The PSpice circuit shown in Fig. 6.19 is made up of three stages: a log amplifier, an inverter, and an antilog amplifier. Suppose the input waveform is the same as shown in the previous problem. Calculate and plot the expected waveforms at Out1 and Out2.

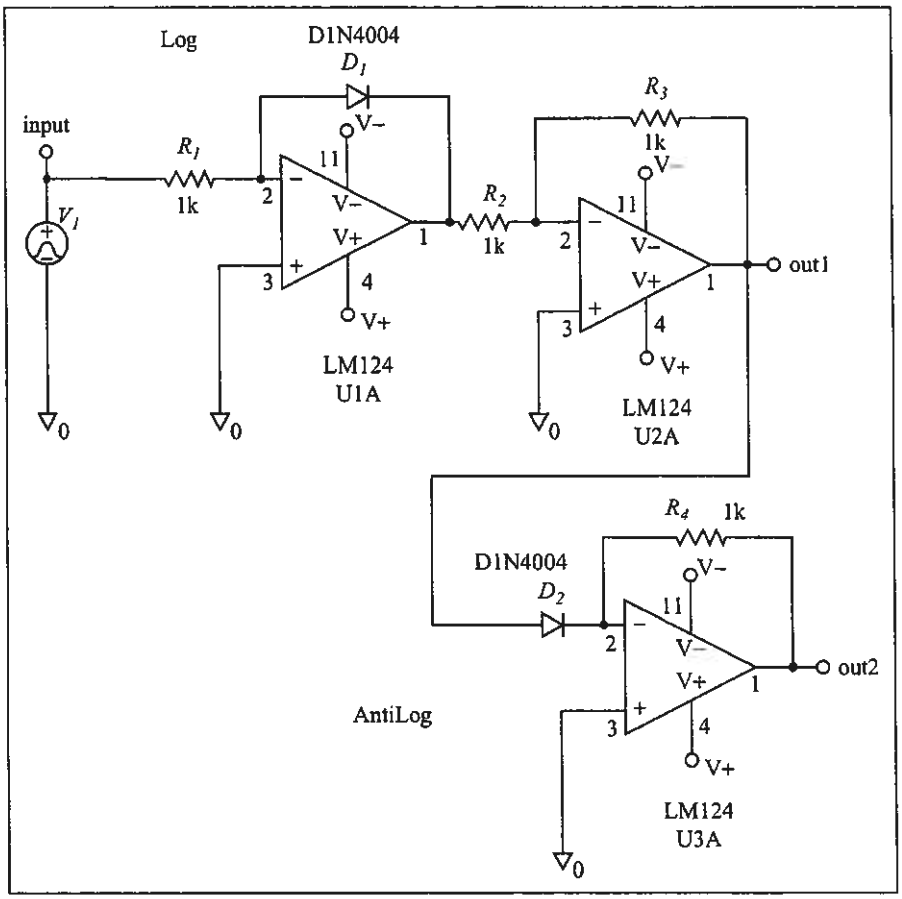

FIGURE 6.19. Problem 6.2.

CHAPTER 7

Waveform Generators

Instrumentation systems frequently require a source of repetitive voltage waveforms. The repetition rate, stated in cycles per second, or Hz, can range from one waveform in many seconds, minutes, or hours, to hundreds, thousands, or millions of waveforms per second. At the extreme ends of the spectrum—that is, exceptionally slow or fast signals—specialized generating circuits and techniques may be required. This chapter deals primarily with the more common intermediate range of approximately a few cycles per second to nearly one megahertz.

Any periodic waveform satisfies the condition $v(t + T) = v(t)$, where T is the repeat interval, or *period*. There are a number of standard waveform shapes that are encountered in applications. The most common is certainly a sinusoidal voltage signal of the general form $v(t) = A \sin(2\pi f t + \phi)$, where A is the amplitude, f is the frequency, and ϕ is a phase shift indicating a displacement in time between the zero point of the "clock" and the sine wave itself. The period and frequency are of course related through $\omega = 2\pi f$. In addition to the sine wave, there are rectangular pulses and square waves, as well as triangular and sawtooth shapes, and finally so-called arbitrary waveforms.

The next section deals with the generation of sinusoidal voltage signals. Other shapes are then discussed.

7.1 OSCILLATORS

Feedback is the process of routing a portion of the output of a circuit back to the input. In Fig. 7.1, the block represents a network, which introduces an attenuation α and a phase shift ϕ in the feedback loop.

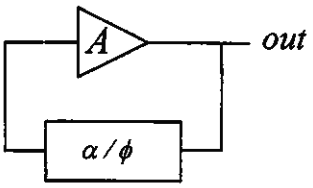

FIGURE 7.1. Amplifier with feedback loop. The feedback network introduces an attenuation α and phase shift ϕ.

In the two preceding chapters, the feedback path in the various amplifiers was purely resistive. Because of this, the associated external phase shift was zero. The feedback path terminated at the op-amp inverting input, so the net effect was a form of partial signal cancellation. This arrangement constitutes negative feedback and was an essential aspect of the inverting and noninverting configurations discussed previously. Negative feedback reduces the overall gain, improves stability, and increases bandwidth.

The opposite situation, in which some portion of the output is returned in-phase to the amplifier, would be expected to have correspondingly opposite results: decreased stability and increased gain. The most common situation where instability is actually a target of the design process is that of electronic oscillators. Positive feedback is thus the key to insuring that oscillations occur in circuits. An oscillator is specified by a number of attributes, such as frequency range, output, stability, and so forth. In many instances, enhancements in one attribute can only be achieved at the expense of others, or in overall circuit complexity. Because of this, no single oscillator design emerges as "best." On the other hand, a few designs have achieved the status of standards because they represent good compromises among the competing requirements. Several of these classics will now be presented as a means of illustrating oscillator fundamentals.

Wien-Bridge Oscillator

The schematic depicted in Fig. 7.2 represents a Wien-bridge oscillator.

The network in the box labeled Z will pass an attenuated and phase-shifted portion of the output back to the noninverting op-amp input. For sustained oscillations to occur, the losses induced in Z must be just compensated by the closed-loop gain of the amplifier. Too little gain and the oscillations will damp away; too much gain and the oscillations will grow uncontrollably. In addition, the phase shift brought about by passage through Z must equal 0 or destructive interference will occur. This process is analogous to the synchronized pumping required to maintain the periodic motion of a swing.

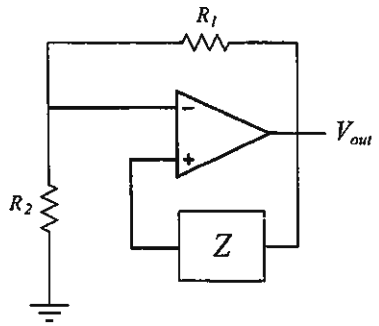

FIGURE 7.2. Oscillator using positive feedback to the noninverting input.

The signal returned through Z may be viewed simply as the voltage input to the noninverting configuration comprised of the op-amp, R_1 and R_2. Thus [see Eq. (5.4)],

$$V_{\text{out}} = \left[1 + \frac{R_1}{R_2}\right] V_+.$$

In a Wien-bridge oscillator, Z is a so-called lead–lag network of the type shown in Fig. 7.3, where V_{out} and V_+ match the symbols in the previous diagram.

In complex notation,

$$\frac{V_+}{V_{\text{out}}} = \frac{Z_b}{Z_a + Z_b} \tag{7.1}$$

with

$$Z_a = R - j\left(\frac{1}{\omega C}\right) \tag{7.2}$$

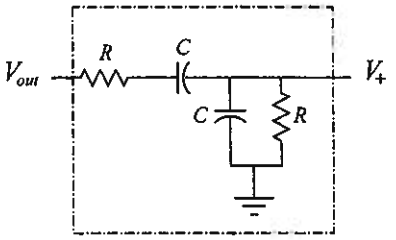

FIGURE 7.3. Lead-lag network used in the feedback path of the Wien-bridge oscillator.

and

$$Z_b = [R^{-1} + j\omega C]^{-1}. \tag{7.3}$$

After a little algebra, one finds for the magnitudes

$$\boxed{\left|\frac{V_+}{V_{\text{out}}}\right| = \frac{1}{\sqrt{9 + \left(R\omega C - \frac{1}{R\omega C}\right)^2}}} \tag{7.4}$$

and for the phase between V_+ and V_{out}

$$\boxed{\phi = \arctan\left[\frac{\frac{1}{R\omega C} - R\omega C}{3}\right]}. \tag{7.5}$$

The right-hand sides of Eqs. (7.4) and (7.5) are obviously frequency-dependent. At very low or high frequencies, the phase shift has limiting values of $+\frac{\pi}{2}$ (V_+ leads V_{out}) and $-\frac{\pi}{2}$ (V_+ lags V_{out}), respectively. The relative amplitude drops away at both low and high frequencies and reaches a maximum at the special value

$$\boxed{\omega_0 = \frac{1}{RC}} \tag{7.6}$$

for which $|V_+| = \frac{1}{3}|V_{\text{out}}|$. This can easily be seen by rewriting Eq. (7.4) as

$$\left|\frac{V_+}{V_{\text{out}}}\right| = \frac{1}{\sqrt{9 + \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2}}. \tag{7.7}$$

Similarly,

$$\phi = \arctan\left[\frac{\frac{\omega_0}{\omega} - \frac{\omega}{\omega_0}}{3}\right], \tag{7.8}$$

and it is evident that the phase shift is zero at $\omega = \omega_0$.

The lead–lag circuit thus displays resonance at the frequency ω_0. The Wien bridge of Fig. 7.2 will exhibit sinusoidal oscillations at this same frequency if, as discussed earlier, the amplifier closed-loop gain equals 3. This requirement is easily met by choosing $R_1 = 2R_2$.

The properties of the lead–lag network can be illustrated by a specific example. The schematic in Fig. 7.4 was drawn in PSpice. The resulting simulation data

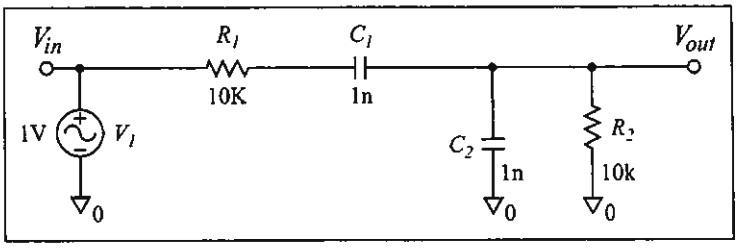

FIGURE 7.4. PSpice schematic of a lead–lag network.

are plotted in Fig. 7.5, and it is clear that a resonance occurs at $f = 15.9$ kHz, in agreement with Eq. (7.6). Also, as expected, at this frequency the phase shift of the network is 0.

Improved Wien-Bridge Oscillator

The preceding discussion assumed ideal behavior from the components, including the op-amp itself. In reality, deviation of resistor values from nominal, op-amp imperfections, and thermal drift, all imply that the Wien bridge might not actually generate stable oscillations at the resonant frequency. Revising basic oscillator designs so that stability ensues is a subject in itself. The following discussion is meant only to illustrate the process.

The filament in an incandescent bulb is a resistive element chosen for its ability to operate at elevated temperatures. An ideal resistor is described by constant R. In contrast, self-heating causes the filament resistance to increase in a manner

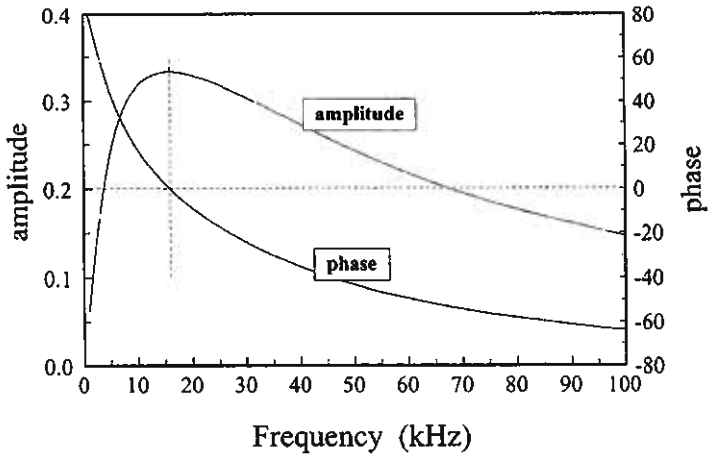

FIGURE 7.5. Results of a PSpice simulation of the lead–lag network. The vertical dotted line marks the resonant frequency at which the network is most transparent and the phase shift is zero.

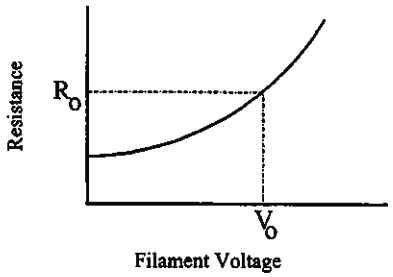

FIGURE 7.6. Hypothetical characteristic of the filament in an incandescent lamp. Points along the curve correspond to higher filament temperatures, and hence higher resistances.

depicted in Fig. 7.6. Suppose the operating point R_0, V_0 lies on the characteristic of a particular bulb, as indicated.

The bulb can now be substituted for one of the gain-setting resistors of the Wien bridge oscillator, as shown in Fig. 7.7.

With the nominal resistance of R_0, the closed-loop gain is 3, as required.

When the circuit is first turned on, the bulb is cold and its resistance R_{filament} is at a minimum well below R_0. The closed-loop gain $(1 + 2R_0/R_{\text{filament}})$ is thus greater than 3, which overcompensates for the lead–lag attenuation of $\frac{1}{3}$. This means that inevitably some small fluctuation will be amplified into larger and larger oscillations, so the circuit is self-starting.

Now, consider what happens if the system begins to drift away from the conditions for sustained oscillation. Suppose the net gain climbs above 3. Then, the oscillator output will increase, and so will the voltage appearing across the bulb. This in turn will result in an increase in filament resistance Fig. 7.6, and

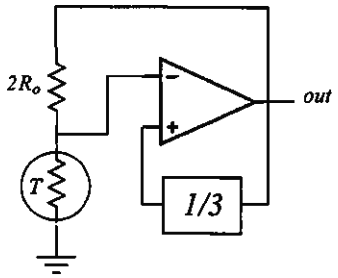

FIGURE 7.7. Improved Wien-bridge oscillator employing an incandescent lamp as a form of automatic gain control for self-starting and stability.

hence a decrease in closed-loop gain, so the output will drop and the system will move back to its intended bias point.

If, instead, the gain drifted below 3, then the oscillator output would temporarily drop, R_{filament} would become less than its target value R_0, and the closed-loop gain would increase, bringing the system back to its intended bias point.

Hence, this improved design for the Wien-bridge oscillator is thus both self-starting and stable.

Phase-Shift Oscillator

In the Wien-bridge oscillator, a portion of the output was fed back to the noninverting amplifier input. This then required that the network phase shift be zero for positive signal reinforcement. It is also possible to direct the feedback signal to the inverting amplifier input, provided the phase shift is, in such a case, 180 degrees. This is necessary because the inverting input itself introdces a further 180 degrees, bringing the combined total up to the positive feedback target of 360 degrees. Such an approach is taken in the phase-shift oscillator (Fig. 7.8).

The oscillator output is fed back to the inverting amplifier consisting of the op-amp together with R_1 and R_f. The closed-loop gain is $-\frac{R_f}{R_1}$ [see Eq. (5.18)].

The feedback network is the chain of resistors and capacitors. An analysis of the $R-C$ ladder yields

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{\left(1 - \frac{5}{(2\pi fRC)^2}\right) - j\left(\frac{6}{2\pi fRC} - \frac{1}{(2\pi fRC)^3}\right)}, \tag{7.9}$$

where V_{in} is the voltage at the input to the ladder (i.e., the op-amp output). The factor in brackets following j is zero for

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{6}RC}}. \tag{7.10}$$

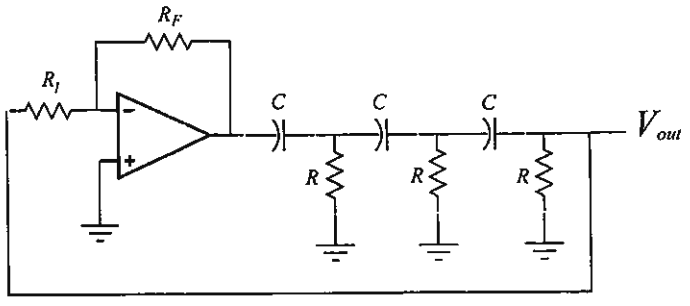

FIGURE 7.8. Phase-shift oscillator.

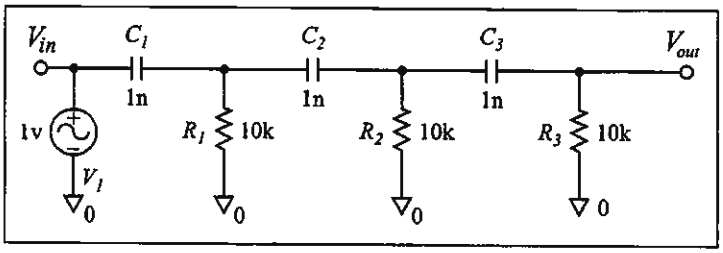

FIGURE 7.9. PSpice schematic of the R-C ladder from a phase-shift oscillator.

At this frequency, the relative output is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{1}{29}. \tag{7.11}$$

Therefore, the phase-shift oscillator will run at the frequency given by Eq. (7.10) when the compensating amplifier gain is set by

$$\frac{R_f}{R_1} = \frac{1}{29}. \tag{7.12}$$

As an example, consider the PSpice schematic in Fig. 7.9. The simulation results (Fig. 7.10) indicate a phase shift of 180 degrees at a frequency of 6.5 kHz, in agreement with Eq. (7.10). The relative output at this frequency is $\frac{1}{29}$, again as expected.

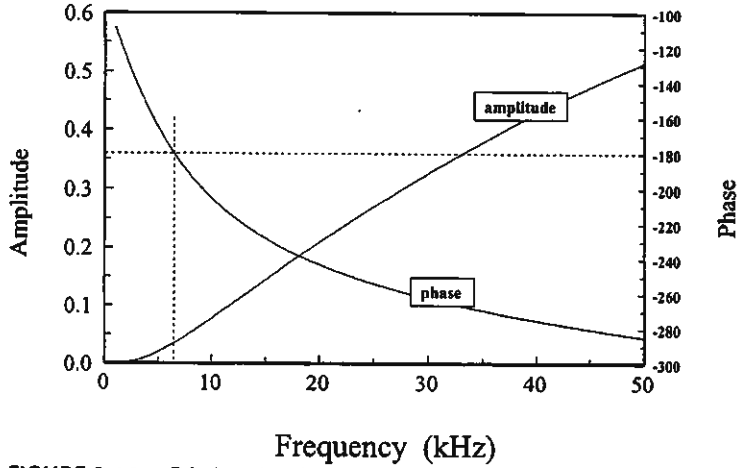

FIGURE 7.10. PSpice simulation results for the R-C ladder. The dotted vertical line marks the oscillator frequency f_0 at which the amplitude is $\frac{1}{29}$ and the phase shift is 180 degrees.

7.2 PULSE GENERATORS

As already noted, the Wien-bridge and phase-shift circuits produce sinusoidal voltage oscillations at the design frequencies. Continuous streams of square pulses are another commonly needed format. Such pulses may be *unipolar*, ranging up and down between a baseline of zero and some peak value, or *bipolar*, where the excursions are bounded between $\pm V_{peak}$. The repeat time for each pulse cycle is the *period*, and the ratio of time in the high-voltage state to the total period is the *duty cycle* of the pulse stream.

To illustrate the process of pulse generation, we now examine two well-known circuits.

Relaxation Oscillator

In the circuit shown in Fig. 7.11, the op-amp output is applied as positive feedback through the voltage divider composed of R_2 and R_3. Because of the positive feedback, the op-amp output will be driven rapidly to positive saturation $V_{out} = +V_{max}$ when $V_+ > V_-$ and will jump to negative saturation $V_{out} = -V_{max}$ when $V_+ < V_-$.

The voltage at the noninverting input is

$$V_+ = V_{out}\frac{R_3}{R_2 + R_3}. \tag{7.13}$$

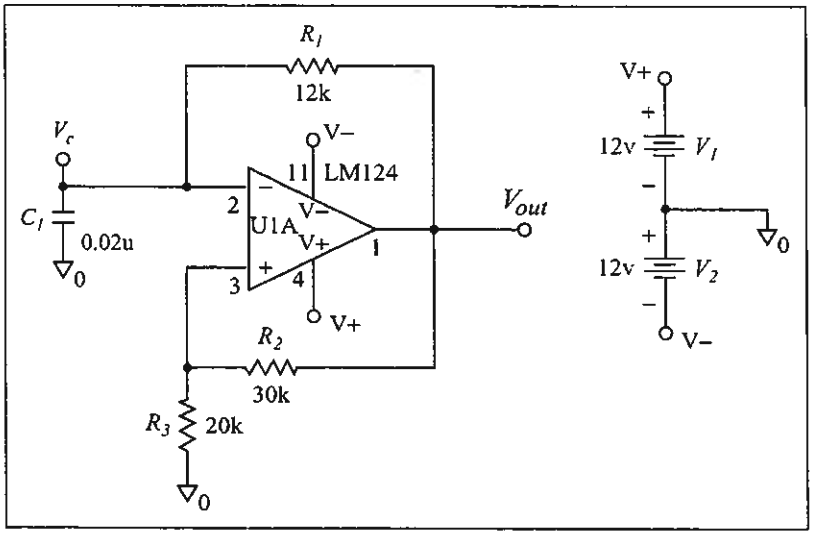

FIGURE 7.11. PSpice schematic of a relaxation oscillator.

To begin, suppose that V_{out} is at $+V_{max}$. Then V_+ will be the fraction of V_{max} specified by Eq. (7.13). The output voltage is also applied to the combination R_1, C_1, with the result that the capacitor charges through R_1. The time constant for this process is $\tau = R_1C_1$. The capacitor voltage V_{cap} (which is just V_-) will increase until it reaches $V_{max}\frac{R_3}{R_2+R_3}$, at which time the op-amp output will almost instantaneously switch down to $-V_{max}$. The voltage at the noninverting input to the op-amp is still given by Eq. (7.13) but is now a negative quantity, and the capacitor will begin to discharge through R_1. This process will continue until the capacitor voltage has dropped from $+[V_{max}\frac{R_3}{R_2+R_3}]$ to $-[V_{max}\frac{R_3}{R_2+R_3}]$. Then, the op-amp will again be driven into positive saturation and its output will switch to $+V_{max}$, and so on.

Thus, the capacitor voltage appears as a sequence of alternating charge and discharge intervals, and the op-amp output is a matching series of pulses with amplitude $\pm V_{max}$.

Consider a charging segment. The equation for the capacitor voltage as a function of time is

$$V_{cap}(t) = V_{max} - \left[V_{max}\frac{R_3}{R_2+R_3} + V_{max}\right] e^{-\frac{t}{\tau}}. \tag{7.14}$$

As required, the initial voltage is $V_{cap}(0) = -[V_{max}\frac{R_3}{R_2+R_3}]$, while the limiting value is $V_{cap}(t \to \infty) = V_{max}$. The time ($T_1$) required for V_{cap} to rise to the upper switching value is obtained by setting the left-hand side of Eq. (7.14) to $+[V_{max}\frac{R_3}{R_2+R_3}]$. The result is

$$e^{-\frac{T_1}{\tau}} = \frac{V_{max}\left[1 - \frac{R_3}{R_2+R_3}\right]}{V_{max}\left[1 + \frac{R_3}{R_2+R_3}\right]} \tag{7.15}$$

or

$$e^{\frac{T_1}{\tau}} = \frac{R_2 + 2R_3}{R_2}. \tag{7.16}$$

From this, the period of the square waves, $T = 2T_1$, is obtained:

$$\boxed{T = 2(R_1C_1)\ln\left(1 + \frac{2R_3}{R_2}\right)}. \tag{7.17}$$

The results from a PSpice simulation are plotted in Fig. 7.12. The capacitor charging and discharging cycles are clearly seen. The expected period of the

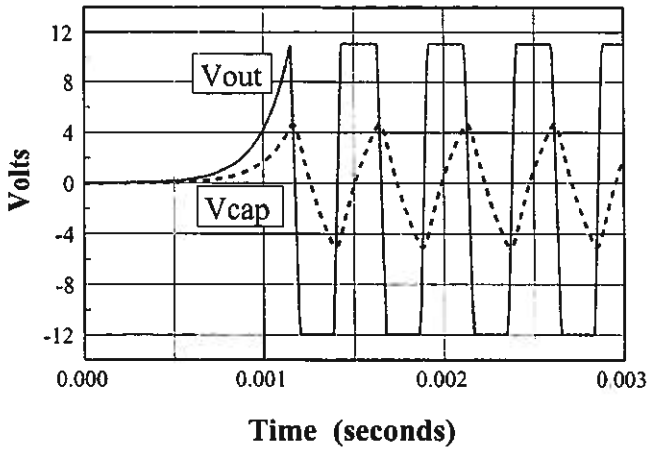

FIGURE 7.12. PSpice simulation results for the relaxation oscillator. An initial start-up phase lasts about a millisecond.

oscillations would be

$$T = 2(12\ \text{K} \times 0.02\ \mu\text{F})\ \ln\left(1 + \frac{2 \times 20\ \text{K}}{30\ \text{K}}\right) = 0.407\ \text{msec},$$

which agrees reasonably with the data in the figure.

555 Timer

For straightforward applications requiring square waves, the so-called 555 chip has become the integrated circuit of choice. This device is available from a number of manufacturers, one or two to a DIP package, and in both bipolar and CMOS versions. It is very economical and easy to use.

As depicted in Fig. 7.13, the 555 contains a pair of op-amp comparators, a flip-flop, an output amplifier, and a discharge transistor. There are in addition three matched resistors (5 KΩ) running from the positive power supply V_{cc} to ground. The external connections and components shown in this figure are particular to operating the 555 in its *astable* mode—that is, in a free-running state.

Basically, the oscillations are the result of repeated charge and discharge cycles of capacitor C. Charging toward V_{cc} through R_1 and R_2 takes place when the transistor is "off." Discharging toward ground through just R_2 occurs when the transistor is "on."

Suppose a charging interval is in progress. The transistor is "off" and V_{cap} is rising. Due to the internal resistor chain, the comparators are set to trip at $\frac{1}{3}V_{cc}$ and $\frac{2}{3}V_{cc}$. When V_{cap} finally reaches $\frac{2}{3}V_{cc}$, the output of the upper comparator

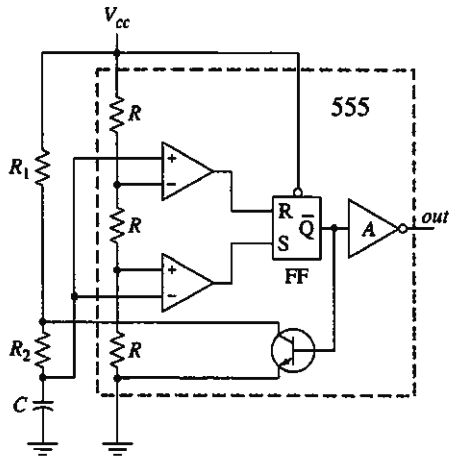

FIGURE 7.13. Block diagram of a 555 timer. The shaded boundary frames the chip contents; the remaining components are external to the IC.

will switch positive, thus resetting the flip-flop and causing $\bar{Q} = 1$. The resulting positive voltage on the base of the transistor switches it "on," initiating a discharge sequence.

The capacitor voltage will decay until it reaches $\frac{1}{3}V_{cc}$, at which point the lower comparator output will abruptly go positive, setting the flip-flop to $\bar{Q} = 0$. This low voltage on the base of the transistor will turn it "off," thus initiating a new charge cycle.

The equation for the capacitor voltage as it rises from $\frac{1}{3}V_{cc}$ towards a limiting value of V_{cc} is

$$V_{\text{cap}}(t) = V_{cc} - \left[-\frac{1}{3}V_{cc} + V_{cc}\right] e^{-\frac{t}{\tau_1}}, \tag{7.18}$$

where the charging time constant is $\tau_1 = (R_1 + R_2)\,C$. But of course the process abruptly terminates at the upper trip point of $\frac{2}{3}V_{cc}$. Hence, the time, T_1, for a charging segment can be obtained from

$$\frac{2}{3}V_{cc} = V_{cc} - \left[-\frac{1}{3}V_{cc} + V_{cc}\right] e^{-\frac{T_1}{\tau_1}}.$$

Thus,

$$T_1 = [(R_1 + R_2)\,C]\ \ln(2). \tag{7.19}$$

Similarly, the discharge through R_2 follows

$$V_{\text{cap}}(t) = \left[\frac{2}{3}V_{cc}\right] e^{-\frac{t}{T_2}}. \tag{7.20}$$

This terminates when V_{cap} reaches $\frac{1}{3}V_{cc}$ and the time required is

$$T_2 = [R_2 C]\ \ln(2). \tag{7.21}$$

The time T for a complete charge/discharge cycle for the 555 is then

$$\boxed{T = [(R_1 + 2R_2)\, C]\ \ln(2)}. \tag{7.22}$$

The 555 output will be high while $\bar{Q} = 0$; that is, during charging intervals. The ratio of the time during which the output is high to the total period of the repetitive square waves is the duty cycle.

$$\text{duty cycle} = \frac{T_1}{T_1 + T_2} = \frac{R_1 + R_2}{R_1 + 2R_2}. \tag{7.23}$$

Since $T_1 > T_2$, as is evident from Eqs. (7.19) and (7.21), the duty cycle can never fall below 50%, whatever the values of the two resistors may be.

A PSpice simulation with components $R_1 = 2.2$ K, $R_2 = 4.7$ K, and $C = 22$ nF produced the waveforms shown in Fig. 7.14. For these values, we expect $T_1 = 0.105$ msec, $T_2 = 0.072$ msec, and $T = 0.177$ msec, in good agreement with the observed data.

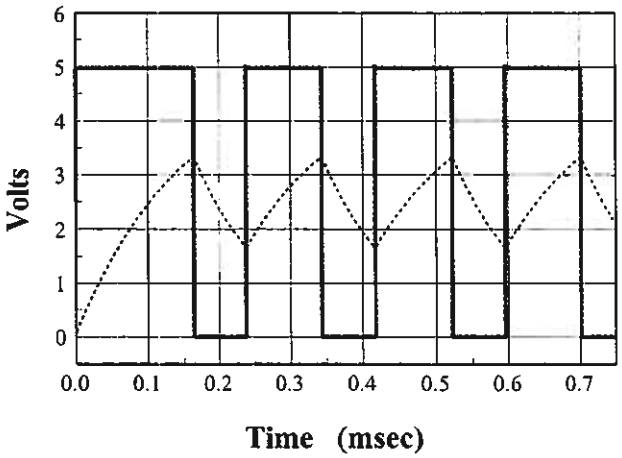

FIGURE 7.14. PSpice simulation results for a free-running 555 oscillator. The square wave is the final chip ouput; the other waveform is taken from the capacitor and shows charging and discharging cycles.

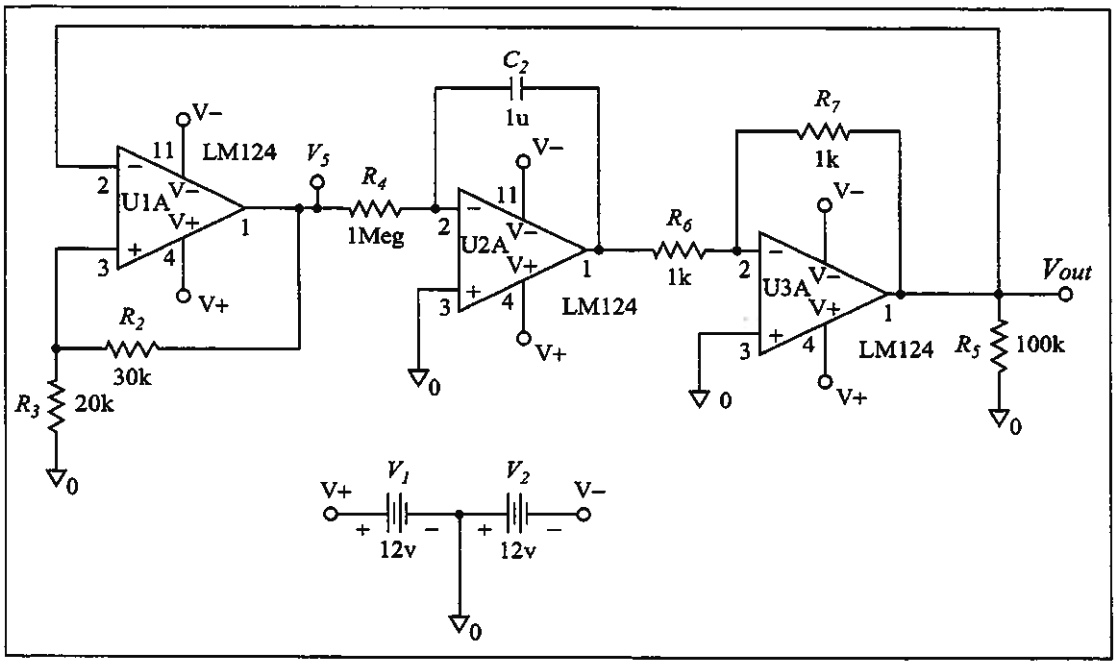

FIGURE 7.15. Sawtooth waveform generator composed of a Schmitt trigger, an integrator, and an inverter.

Sawtooth Waveform

When a dc voltage is applied to an integrator (see previous chapter), the output will be a linear ramp. This property can serve as the basis of a sawtooth waveform generator. Consider the PSpice schematic shown in Fig. 7.15.

As in the relaxation oscillator, the first op-amp acts as what is called a Schmitt trigger, its output rapidly switching to $\pm V_{\max}$ whenever the inverting input either just drops below or just rises above the fraction $\frac{R_3}{R_2+R_3}$ of the present output. Thus, there are two trip points

$$\text{UTP} = +\frac{R_3}{R_2 + R_3} V_{\max},$$

$$\text{LTP} = -\frac{R_3}{R_2 + R_3} V_{\max}.$$

The net result is that the output will remain at $+V_{\max}$ as long as the inverting input remains below the upper trip point (UTP). Once UTP is exceeded at the inverting input, the output will switch to $-V_{\max}$ and remain at that value until the inverting input drops below the lower trip point (LTP). Again, the output is constant as long as the inverting input remains below UTP, when switching once more will take place. The voltage interval between UTP and LTP is known as the *hysteresis* of the Schmitt trigger.

Let us suppose that the first op-amp is delivering $+V_{max}$ to the second op-amp, which is wired as an integrator. The output of this second op-amp satisfies Eq. (6.21), which after inversion by the third unit becomes

$$\frac{dV_{out}}{dt} = \frac{V_{max}}{R_4C_2}, \tag{7.24}$$

so V_{out} ramps up linearly with slope $\frac{V_{max}}{R_4C_2}$. This rising output will ultimately reach the upper trip point (UTP), and when it does the first op-amp will switch to $-V_{max}$ and the final output will ramp down according to

$$\frac{dV_{out}}{dt} = -\frac{V_{max}}{R_4C_2}. \tag{7.25}$$

When the lower trip point (LTP) is reached, the first op-amp will return to $+V_{max}$ and ramping up will occur. Thus, the V_{out} will consist of alternating up and down ramps, which range from UTP to LTP. The time T_{up} or T_{down} required for either up or down ramping can be determined from the slopes.

$$\boxed{T_{up} = T_{down} = \left[\frac{2R_3}{R_2 + R_3}\right] R_4C_2}. \tag{7.26}$$

For the example shown in the schematic, this gives

$$T_{up} = T_{down} = 0.8 \text{ sec}.$$

The results of a PSpice simulation of the circuit are plotted in Fig. 7.16.

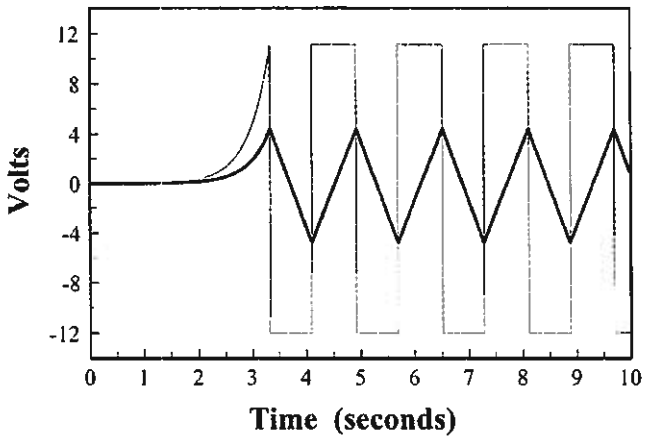

FIGURE 7.16. PSpice simulation results for the sawtooth generator. Both the Schmitt output (square) and final output (sawtooth) are shown. A start-up transient is present.

After an initial start-up, the expected triangular output waveform is observed. This sawtooth ranges between the upper and lower trip points, which for this example are at ±40% of the op-amp saturation voltage. The circuit also provides a square wave at the output terminal of the first op-amp, as illustrated in Fig. 7.16.

7.3 CRYSTAL OSCILLATORS

The oscillators discussed earlier in this chapter shared at least one important feature—a frequency-selective element placed in a feedback loop. For the Wien-bridge circuit, this element was a lead–lag network. Generally speaking, oscillators perform best when the frequency selection is "sharp." This usually results in precise tuning and stability.

Quartz crystals are a common choice for the required frequency-selective devices in oscillators. As a material, quartz is piezoelectric. This means that its particular atomic structure results in the generation of an electric potential whenever the crystal is mechanically deformed. The reverse is also true: the application of an electric field across the crystal results in a mechanical deformation. A consequence of these two properties is that a quartz crystal may be shaped by cleaving, cutting, grinding, and polishing until its precise dimensions support an electromechanical resonance. That is, for some specific frequency of electrical excitation, the wavelength of the mechanical oscillations induced by the piezoelectric effect matches a physical dimension of the crystal. Like the acoustic waves in an organ pipe, the system is "tuned" by its shape.

A quartz crystal for use in electronics is a two terminal device—a pair of leads emerge from the package. An equivalent circuit that captures most of the essential electrical properties of a crystal is shown in Fig. 7.17.

This consists of a series branch with resistance, capacitance, and inductance, together with a capacitive parallel branch. The component values for this equivalent circuit are of course dependent on the specific crystal.

As an example, the device model QZS32768 from the PSpice simulation library was examined; its impedance properties are shown in Fig. 7.18. There is a series resonance at 32,768 Hz and a parallel resonance slightly above that, as

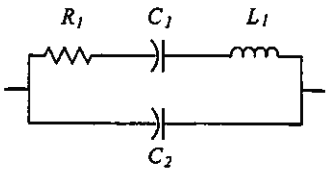

FIGURE 7.17. Equivalent circuit of a quartz crystal.

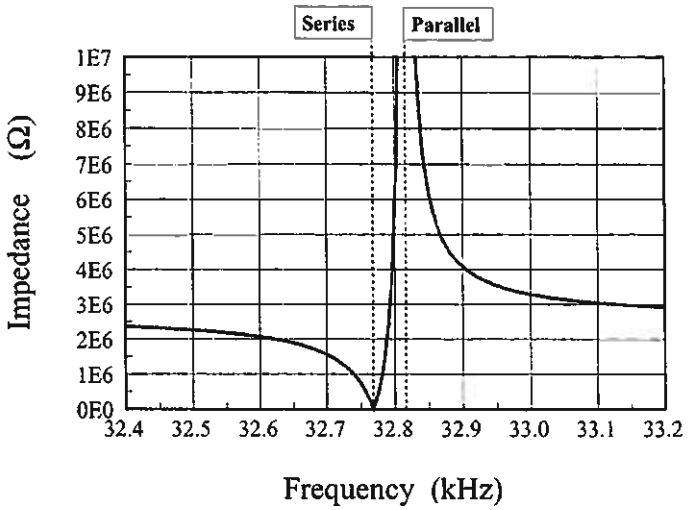

FIGURE 7.18. Impedance of PSpice library model QZS32768 crystal.

indicated in the figure. Note the sharpness of the resonances. (Figure 7.18 has a considerably expanded horizontal scale.)

In Fig. 7.19, this crystal is embedded in the positive feedback loop of an op-amp. For this PSpice simulation, the pulse generator V_3 was found necessary to kick-start the oscillator. Only a very brief single pulse was required for this purpose.

The results of the simulation are shown in Fig. 7.20. Both the signal V_{xtal} (light trace) and V_{out} (bold trace) are shown. As expected, the oscillations occur at the resonance of 32,768 Hz (period of 30.52 μsec).

7.4 REMARKS

The preceding sections have described just a few typical sine wave and sawtooth waveform generators. Many other circuits serve as the basis of both custom and commercial designs, and there are a number of books that provide more depth on this topic. These references can be sources of valuable technical detail, including coverage of specialized areas such as high-frequency and low-frequency oscillators, as well as techniques for improving stability, particularly with respect to thermal drift.

The advent of microprocessors and custom integrated circuits has drastically altered the face of instrumentation, especially in terms of the range of commercial products now available. These are in reality complex systems (although they are not necessarily costly), and not the sort of simple circuit that could easily be replicated on a workbench.

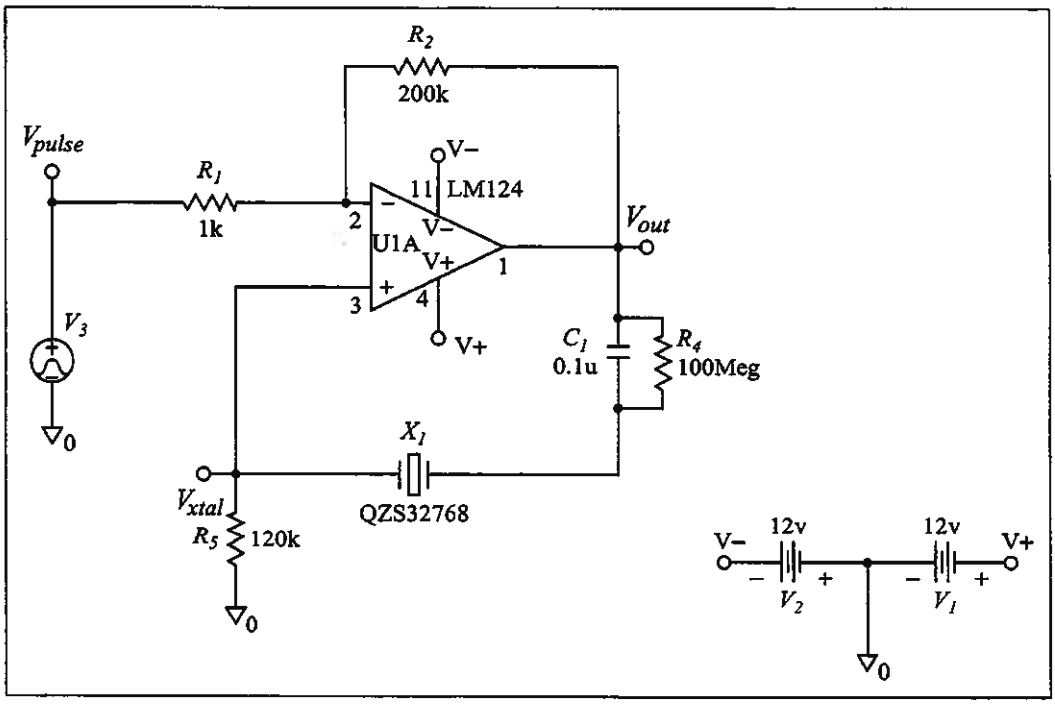

FIGURE 7.19. Example of an oscillator employing a quartz crystal in a positive feedback loop. The pulse generator was needed to initiate oscillations.

Arbitrary waveform generators fall within this category. As the name implies, an arbitrary waveform generator is able to create a repetitive signal of any desired shape. The user must deliver to the instrument a prescription of the waveform, usually as a string of perhaps thousands of numbers representing a discrete sampling of the waveshape. This data array then resides in system memory within the

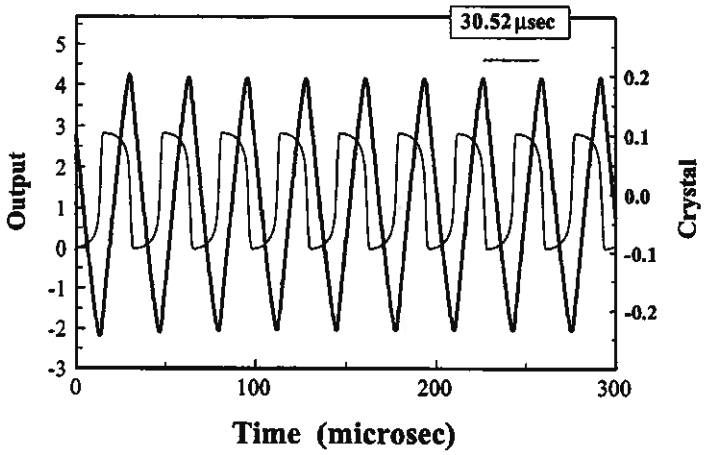

FIGURE 7.20. PSpice simulation of a crystal oscillator. The circuit output is the bold waveform. Also indicated is the time-dependent voltage at the top of R_5.

instrument and is used in combination with digital-to-analog converters (DAC) and controllers to synthesize the final signal.

Performance is dependent upon the speed of the DACs, the number of bits allocated to each memory location, and the size of memory. For example, suppose an instrument has a memory array consisting of 1024 8-bit words. The vertical resolution of any synthesized waveform will then be 1 part in $2^8 = 256$, or better than $\frac{1}{2}\%$. Further, suppose for this example that the maximum conversion speed of the DACs is 100 nsec. One complete sweep of the stored waveform would then take at least $1024 \times 10^{-7} = 0.1024$ msec. This corresponds to a maximum output frequency from the generator of 9765 Hz.

PROBLEMS

Problem 7.1. Choose component values for the lead–lag network shown in Fig. 7.4 so that it can be used in a Wien-bridge oscillator with a target frequency of 50 kHz.

Problem 7.2. Choose component values for the R-C ladder shown in Fig. 7.9 so that it can be used in a phase-shift oscillator intended to run at 25 kHz.

Problem 7.3. Select new component values in the relaxation oscillator shown in Fig. 7.11 so that the output has a period of 1.00 msec.

Problem 7.4. Select external components for the 555 timer so that it oscillates with a period of 0.50 msec .

Problem 7.5. Using the schematic of Fig. 7.15, design a sawtooth waveform generator that will run at 5 Hz.