Using a CLC Low-Pass Filter to Reduce the Consequences of Aging in Steady-State Regime of DC-DC Converters

Acácio M. R. Amaral
POLYTECHNIC INSTITUTE OF COIMBRA, ISEC / IT
Rua Pedro Nunes – Quinta da Nora
P - 3030 -199 Coimbra, Portugal
Tel.: +351 / (239) – 790200
Fax: +351 / (239) – 790201
E-Mail: acacio@isec.pt
URL: http://www.isec.pt/~acacio

A. J. Marques Cardoso
UNIVERSITY OF COIMBRA, FCTUC / IT
Department of Electrical and Computer Engineering
Pólo II – Pinhal de Marrocos
P - 3030 - 290 Coimbra, Portugal
Tel.: +351 / (239) – 796232
Fax: +351 / (239) – 796247
E-Mail: ajmcardoso@ieee.org

Keywords

«Design», «Passive filter»,«Switched-mode power supply»

Abstract

This paper presents a filter that can be used in the design of DC-DC converters, in order to mitigate the pernicious effects of the electrolytic capacitor's equivalent series resistance (ESR), in steady state regime. The aging of electrolytic capacitors, used for smoothing the output voltage manifests itself by the increase of their ESR, and as a consequence of that, the output voltage ripple becomes very large. In this manner, the study of solutions to this problem is a very important subject for converters designers in low and medium power range. This paper shows that the use of a CLC filter reduces significantly the output voltage ripple without increasing too much the converter size. A study about the additional filtering expenses, like the impact on converter size and cost will be presented. Several theoretical, simulated and experimental results are presented for a buck type DC-DC converter, with different output filters, operating in the continuous conduction mode (CCM).

Introduction

Most electronic equipment today requires an input power source with high power quality, which on one hand, respects all requirements related with electromagnetic interference (EMI), power factor correction and minimum output voltage ripple, and on the other hand, guaranties small size and weight and high efficiency. The compromise between these demands is very difficult to establish. The switch mode DC-DC converters must have lossless components. Two basic groups of components are available in switch mode DC-DC converters: the switching components, such as diodes and transistors, and the reactive components, such as inductors and capacitors. Thus the energy is pumped around the circuit by the switching components, while reactive components act as intermediate energy stores and input-output reservoirs [1]. Unfortunately, these different components own some parasitic elements. The non-ideal

behavior of energy storage components is very important in a switch mode DC-DC converter, where there is a rapidly change of voltages and currents [2].

Real capacitors come in many forms, but almost all are built from two conducting plates or films, separated by an insulation layer [3]. Thus, an aluminum electrolytic capacitor consists of two foils (anode and cathode foils) with paper interleaved, impregnated with liquid electrolyte, connected to terminals and scaled in a can. The foils are high-purity aluminum and are etched with billions of microscopic tunnels to increase the surface area in contact with the electrolyte; this construction delivers colossal capacitance [3], which gives them an excellent relation capacitance/size. The capacitance of an aluminum electrolytic capacitor can be computed by:

$$C = 8.855 \times 10^{-8} \frac{\varepsilon \times S}{d} \tag{1}$$

where, ε is the dielectric constant, S is the surface area (cm^2) and d is the thickness (cm) of the dielectric [3].

In a real electrolytic capacitor, the wires and plates have resistance and inductance, besides that, the insulation is not perfect, thus there is a leakage resistance [2].

Fig. 1 shows the equivalent circuit of an electrolytic capacitor, where C is the equivalent capacitance, R_w is the wire resistance, ESL is the equivalent series inductance (wire inductance) and R_{Leak} is the leakage resistance.

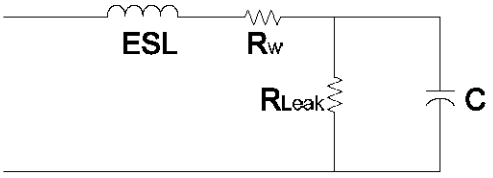

Fig. 1: Equivalent circuit of an electrolytic capacitor [2].

Simplifying the circuit of Fig. 1, it is possible to define the total resistive losses as the equivalent series resistance, ESR, given by [2]:

$$ESR = R_W + \frac{1}{w^2 R_{Leak} C^2} \tag{2}$$

Thus the impedance of an electrolytic capacitor can be expressed as:

$$Z = ESR - j\frac{1}{w C} + j w ESL \tag{3}$$

The dissipation factor, DF, is often used to indicate the quality of the capacitor, and represents the ratio of resistance to reactance. For lower frequencies, it can be expressed as:

$$DF = 2 \times \pi \times f \times C \times ESR \tag{4}$$

$$ESR \cong \frac{DF}{2 \pi f C} \tag{5}$$

ISBN : 90-75815-08-5

Using (5), it is possible to conclude that low ESR can be achieved either through the use of very large capacitors or, through the selection of high operating frequencies.

The ESL is typically about some nH, so it can be considered negligible. Thus, if the converter is operating below the resonant frequency of the electrolytic capacitor, the equivalent circuit of the capacitor can be modeled by an ESR and a capacitive reactance [2].

Just as electrical conductivity, the capacitance of the electrolytic capacitor rises with the increase of temperature; however DF and ESR decrease. The DF increases with frequency, while ESR decreases slower than the increase of DF [3].

The life of an electrolytic capacitor is largely dependent on environmental and electrical factors. Environmental factors include temperature, humidity, atmospheric pressure and vibration. Electrical factors include operating voltage, current ripple and charge-discharge duty cycles. The temperature is the most critical one. The increase of temperature in an electrolytic capacitor results from the increase of the ambient temperature, or from the internal heating due to the current ripple. The increase of temperature accelerates the chemical reaction, which produces gas within the capacitor. This gas is diffused through the end seal and, as a consequence, the volume of electrolyte decreases. In this manner, the capacitance decreases, while ESR and DF increase [4].

An old rule-of-thumb says that an electrolytic capacitor is near its lifetime, when it has lost about 40% of its electrolyte, which means that the ESR should be about three times its initial value [5].

Buck Converter

The buck converter is a step-down converter, which means that the output voltage is always less than the input voltage. This converter is used in many switching power supplies, in high performance DC motor control and in a wide range of electronics circuits applications [2]. It can operate in two conduction modes: the continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The prototypes studied in this work operate in CCM, which means that, in steady state regime, the inductor current never reaches zero.

Fig. 2 shows the schematic of this converter as well as its equivalent circuits during conduction and non-conduction stage.

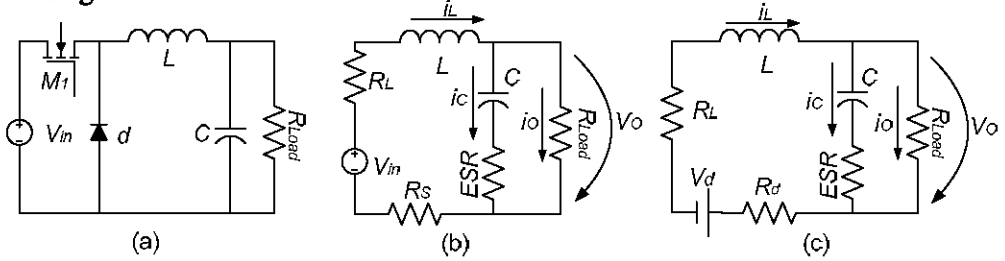

Fig. 2: Schematic of the buck converter (a), equivalent circuit during conduction stage (b), and non-conduction stage (c).

Symbols used in the Fig. 2 are as follows:

- R_S : Resistance of the MOSFET during the conduction stage.
- R_L : Resistance of the inductor.
- R_d : Resistance of the diode during its conduction stage.
- L : Inductance of the inductor.

C : Capacity of the electrolytic output capacitor.
ESR : Equivalent series resistance of the output electrolytic capacitor.
R : Load resistance.
V_{in} : Converter input voltage.
V_d : Forward voltage drop in the diode.
i_c : Capacitor current.
i_L : Inductor current.
i_O : Converter output current.
v_O : Converter output voltage.

In this work three different prototypes were developed, whose schematics are presented in Fig. 3.

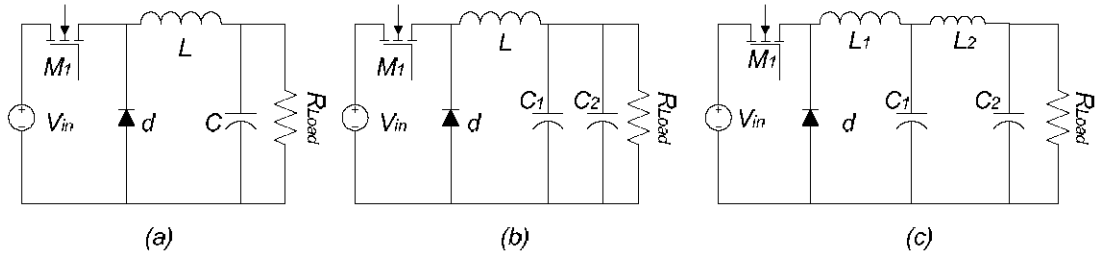

Fig. 3: Schematic of the three prototypes developed: (a) basic buck converter; (b) buck converter with two capacitors in parallel; (c) buck converter with a CLC filter.

For simulation purposes, the state space averaging technique was used in this work. So, first the state space equations corresponding to the two stages were obtained, and then averaged over a switching cycle, as it can be seen in (6):

$$\frac{d\dot{X}}{dt} = A\ \ X + b\ \ V_{in} + c\ \ V_d \tag{6}$$

For the converter shown in Fig 3 (a), the chosen state variables were the inductor current, i_L, and the capacitor voltage, v_C, where:

$$\frac{d\dot{X}}{dt} = \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix},\ X = \begin{bmatrix} i_L \\ v_c \end{bmatrix},\ A = \begin{bmatrix} \left(-\frac{R_L + R_S\ D_1 + R_d\ D_2}{L} - \frac{ESR\ R}{(R+ESR)L} \right) & \frac{-R}{(R+ESR)L} \\ \frac{R}{(R+ESR)C} & \frac{-1}{(R+ESR)C} \end{bmatrix},\ b = \begin{bmatrix} \frac{D_1}{L} \\ 0 \end{bmatrix},\ c = \begin{bmatrix} \frac{-D_2}{L} \\ 0 \end{bmatrix}$$

For the converter shown in Fig 3 (b), the chosen state variables were the inductor current, i_L, and the capacitors voltages, v_{C1} and v_{C2}, where:

$$\frac{d\dot{X}}{dt} = \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{c1}}{dt} \\ \frac{dv_{c2}}{dt} \end{bmatrix},\ X = \begin{bmatrix} i_L \\ v_{c1} \\ v_{c2} \end{bmatrix},\ A = \begin{bmatrix} \left(-\frac{R_L + R_S\ D_1 + R_d\ D_2}{k_{11}} - \frac{K_2}{K_0} \right) & \left(-\frac{1}{k_{11}} - \frac{K_2}{K_0\ R} - \frac{K_3}{K_0} \right) & \frac{K_3}{K_0} \\ \frac{K_4}{K_0} & \left(-\frac{K_4}{K_0\ R} - \frac{K_5}{K_0} \right) & \frac{K_5}{K_0} \\ \frac{K_6}{K_0} & \left(-\frac{K_6}{K_0\ R} - \frac{K_7}{K_0} \right) & \frac{K_7}{K_0} \end{bmatrix},\ b = \begin{bmatrix} \frac{D_1}{k_{11}} \\ 0 \\ 0 \end{bmatrix},\ c = \begin{bmatrix} \frac{-D_2}{k_{11}} \\ 0 \\ 0 \end{bmatrix}$$

$$k_{11} = L\,;\, k_{12} = ESR_1\ C_1\,;\, k_{22} = \left(C_1 + \frac{ESR_1\ C_1}{R}\right);\, k_{23} = C_2\,;\, k_{32} = C_1\ ESR_1\,;\, K_{33} = -ESR_2\ C_2\,;\, K_1 = k_{22}\ k_{33} - k_{23}\ k_{32}\,;$$

$$K_0 = k_{11}\left(k_{22}\ k_{33} - k_{23}\ k_{32}\right);\, K_2 = -k_{12}\ k_{33}\,;\, K_3 = k_{12}\ k_{33}\,;\, K_4 = k_{11}\ k_{33}\,;\, K_5 = -k_{11}\ k_{23}\,;\, K_6 = -k_{32}\ k_{11}\,;\, K_7 = k_{22}\ k_{11}\,;$$

For the converter shown in Fig 3 (c), the chosen state variables were the inductors currents, i_{L1} *and* i_{L2}, and the capacitors voltages, v_{C1} and v_{C2} , where:

$$\frac{d\dot{X}}{dt} = \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{c1}}{dt} \\ \frac{dv_{c2}}{dt} \end{bmatrix},\ X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{c1} \\ v_{c2} \end{bmatrix},\ A = \begin{bmatrix} a_{11} & a_{12} & a_{13} & 0 \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & 0 & 0 \\ 0 & a_{42} & 0 & a_{44} \end{bmatrix},\ b = \begin{bmatrix} \frac{D_1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix},\ c = \begin{bmatrix} -\frac{D_2}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix},\ a_{11} = \left(-\frac{R_{L1} + R_S\ D_1 + R_d\ D_2}{L_1} - \frac{ESR_1}{L_1}\right)$$

$$a_{12} = \frac{ESR_1}{L_1},\ a_{13} = -\frac{1}{L_1},\ a_{21} = \frac{ESR_1}{L_2},\ a_{22} = \left(-\frac{R_{L2}}{L_2} - \frac{ESR_1}{L_2} - \frac{ESR_2\ R}{L_2\left(R + ESR_2\right)}\right),\ a_{23} = \frac{1}{L_2},\ a_{24} = \left(-\frac{1}{L_2} + \frac{ESR_2}{\left(L_2\left(R + ESR_2\right)\right)}\right)$$

$$a_{31} = \frac{1}{C_1}, a_{32} = -\frac{1}{C_1}, a_{42} = \frac{R}{C_2\left(R + ESR_2\right)}, a_{44} = -\frac{1}{C_2\left(R + ESR_2\right)}$$

The values of the input voltage, V_{in}, of the conduction time, t_{ON}, of the period, T, and of the load resistance, R_{Load}, are 66 V, 9 μs, 18 μs and 10 Ω, respectively, for the three prototypes.

Theoretical Analysis

From Fig. 2 and disregarding R_d, R_L, R_S and V_d, it is possible to represent the theoretical curves of the inductor voltage, v_L, and of the inductor current, i_L, as in Fig.4.

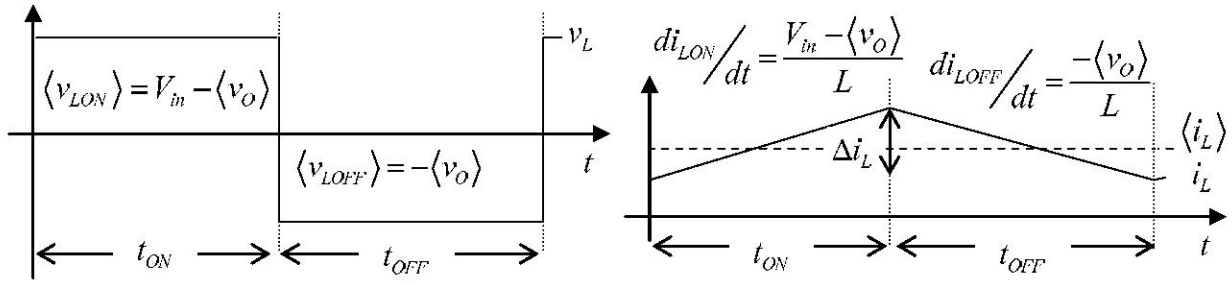

Fig. 4: Theoretical curves of v_L and i_L.

Symbols used in the Fig. 4 are as follows:

$\langle v_{LON} \rangle$	:	Mean value of the inductor voltage during the conduction stage.
$\langle v_{LOFF} \rangle$	:	Mean value of the inductor voltage during the non-conduction stage.
$\langle v_O \rangle$	:	Mean value of the output voltage.
t_{ON}	:	Transistor conduction time.
t_{OFF}	:	Transistor non-conduction time.
Δi_L	:	Inductor current ripple.

ISBN : 90-75815-08-5

Using the principle of inductor volt-second balance for steady state regime, it is possible to write:

$$\left(V_{in}-\langle v_O\rangle\right)t_{ON}=\langle v_O\rangle t_{OFF}\Rightarrow V_O=\frac{t_{ON}\,V_{in}}{\left(t_{ON}+t_{OFF}\right)}=D_{ON}\,V_{in} \tag{7}$$

From Fig. 4, it is possible to conclude that the inductor current is characterized by a d.c. component and an a.c. component. The d.c. component is totally transferred to the load, since the capacitor impedance is proportional to the inverse of the frequency, in this case zero; thus it is possible to write:

$$\langle i_L\rangle=\langle i_O\rangle=\frac{\langle v_O\rangle}{R_{Load}}=\frac{D_{ON}\,V_{in}}{R_{Load}} \tag{8}$$

However the a.c. component of the inductor current will find two paths. Each path will present a different resistance to the a.c. component of the inductor current. If an ideal capacitor is considered, and the frequency and capacitance are too high, almost all of this a.c. component is transferred to the branch of the capacitor; thus, an exiguous part of the a.c. inductor current would be transferred to the load. Unfortunately, a real capacitor has some parasitic elements such as the ESR, as it can be seen in Fig. 1. In this way, there is a portion of the a.c. inductor current that is transferred to the load. The objective of this work is to present a solution to this problem.

Using Fig. 4, it is possible to write:

$$\Delta i_L=\frac{di_{LON}}{dt}\,t_{ON}=\frac{\left(V_{in}-\langle v_O\rangle\right)}{L}\,t_{ON}=\frac{V_{in}\left(1-D_{ON}\right)}{L}\,t_{ON}=\frac{V_{in}\left(D_{ON}-D_{ON}{}^2\right)}{L}\,T \tag{9}$$

$$\Delta i_L=-\frac{di_{LOFF}}{dt}\,t_{OFF}=\frac{\langle v_O\rangle}{L}\,t_{OFF}=\frac{V_{in}\,D_{ON}}{L}\,t_{OFF}=\frac{V_{in}\,D_{ON}D_{OFF}}{L}\,T=\frac{V_{in}\left(D_{ON}-D_{ON}{}^2\right)}{L}\,T \tag{10}$$

where, D_{ON} is the relation between the transistor conduction time and the period of the signal, D_{OFF} is the relation between the transistor non-conduction time and the period of the signal, and T is the period of the signal.

Using the Fourier analysis, it is possible to conclude that the fundamental component of a triangular waveform with a duty cycle of 50% is much larger (>80%) than the other components, so the three filters can be studied using a sinusoidal analysis technique. In this way, considering the converter of Fig. 3 (a), it is possible to write:

$$\begin{cases}\hat{i}_L=\hat{i}_c+\hat{i}_O\\ \hat{v}_O=\hat{i}_c\left(-j\,X_C+ESR\right)\Rightarrow\hat{i}_L=\dfrac{R_{Load}\,\hat{i}_O}{\left(-j\,X_C+ESR\right)}+\hat{i}_O,\ \text{since}\ \begin{cases}ESR_A\gg X_{CA}\\ ESR_B\gg X_{CB}\end{cases}\Rightarrow\Delta i_O\cong\dfrac{\Delta i_L}{\left(1+\dfrac{R_{Load}}{ESR}\right)}=\dfrac{\Delta i_L\;ESR}{\left(ESR+R_{Load}\right)}\\ \hat{v}_O=\hat{i}_O\,R_{Load}\end{cases} \tag{11}$$

From (11) it is possible to write:

$$\Delta V_O\cong\frac{\Delta i_L\;ESR\,R_{Load}}{\left(ESR+R_{Load}\right)} \tag{12}$$

Considering the converter of Fig. 3 (b), it is possible to write:

ISBN : 90-75815-08-5

$$\begin{cases} \hat{i}_L = \hat{i}_{c1} + \hat{i}_{c2} + \hat{i}_O \\ \hat{v}_O = \hat{i}_{c1}\left(-j\,X_{C1} + ESR_1\right) \\ \hat{v}_O = \hat{i}_{c2}\left(-j\,X_{C2} + ESR_2\right) \\ \hat{v}_O = \hat{i}_O\,R_{Load} \end{cases}, \text{since} \begin{cases} ESR_A \gg X_{CA} \\ ESR_B \gg X_{CB} \end{cases} \Rightarrow \Delta i_O \cong \frac{\Delta i_L}{\left(1 + \frac{R_{Load}}{ESR_1} + \frac{R_{Load}}{ESR_2}\right)}$$

$$\Delta i_O \cong= \frac{\Delta i_L\; ESR_1\; ESR_2}{\left(ESR_1\; ESR_2 + R_{Load}\left(ESR_1 + ESR_2\right)\right)} \tag{13}$$

Considering the converter of Fig. 3 (c), it is possible to write:

$$\begin{cases} \hat{i}_{L1} = \hat{i}_{L2} + \hat{i}_{c1} \\ \hat{i}_{L2} = \hat{i}_O + \hat{i}_{c2} \\ \hat{v}_O = \hat{i}_{c2}\left(-j\,X_{C2} + ESR_2\right) \\ \hat{v}_O = \hat{i}_O\,R_{Load} \\ \hat{i}_{c1}\left(-j\,X_{C1} + ESR_1\right) = \hat{i}_{L2}\left(-j\,X_{L2} + R_{L2}\right) + \hat{v}_O \end{cases}, \text{since} \begin{cases} ESR_A \gg X_{CA} \\ ESR_B \gg X_{CB} \Rightarrow \Delta i_O \cong \dfrac{\Delta i_L}{\left(1 + R_{Load}\left(\dfrac{1}{ESR_1} + \dfrac{1}{ESR_2}\right) + \dfrac{X_{L2}}{ESR_1}\left(1 + \dfrac{R_{Load}}{ESR_2}\right)\right)} \\ X_{L2} \gg R_{L2} \end{cases}$$

$$\Delta i_O \cong \frac{\Delta i_L\; ESR_1\; ESR_2}{ESR_1\; ESR_2 + R_{Load}\left(ESR_1 + ESR_2\right) + X_{L2}\left(ESR_2 + R_{Load}\right)} \tag{14}$$

Using (9) and (13), it is possible to compute the value of L_2:

$$L_2 \simeq \frac{ESR_1\; ESR_2\left(\dfrac{V_{in}\left(D_{ON} - D_{ON}{}^2\right)T}{L_1\;\Delta i_O} - 1\right) - R_{Load}\;\left(ESR_1 + ESR_2\right)}{2\,\pi\,f\left(ESR_2 + R_{Load}\right)} \tag{15}$$

where, $\hat{i}_L, \hat{i}_c, \hat{i}_O$ are the a.c. components of the inductor, capacitor and output current, $\hat{v}_O$ is the a.c. component of output voltage, ESR_1 and ESR_2 are the equivalent series resistances of capacitors C_1 and C_2, and f is the operating frequency.

Experimental and Simulated Results

In this work three different filters were implemented by considering used capacitors in order to appreciate their performance. Since the capacitors used were new, it was necessary to make them old. Thus, first it was necessary to know their ESR intrinsic value, which was accomplished through the use of expressions (9), (12) and observing the experimental waveform of Δv_O (Fig. 5). In this manner, their ESR intrinsic value, at an operating frequency of approximately 55.5 kHz, was found to be of 0.06 Ω. Fig. 5 shows the experimental waveform of the basic buck converter presented in Fig. 3(a), considering a new capacitor.

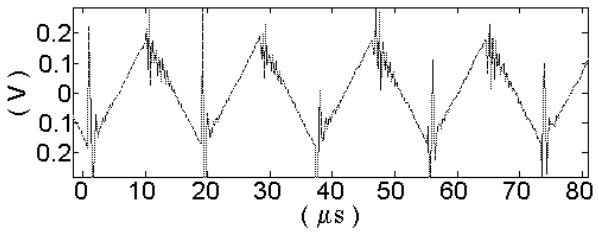

Fig. 5 Experimental waveform of Δv_O for the converter presented in Fig. 3 (a), with a new capacitor.

Fig. 6 shows the simulated waveform of Δv_O for the basic buck converter of Fig. 3 (a), considering a new capacitor.

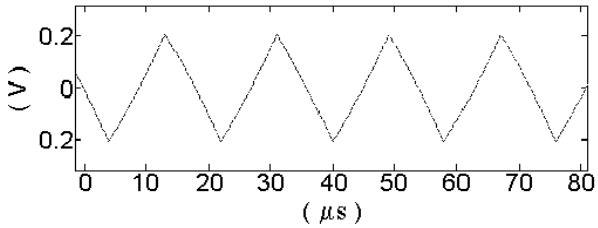

Fig. 6 Simulated waveform of Δv_O for the converter presented in Fig. 3 (a), with a new capacitor.

Comparing Fig. 5 and Fig. 6, it is possible to conclude that the ESR intrinsic value of the electrolytic capacitors used was well estimated.

As it was mentioned in the introduction, an old capacitor would present an ESR of approximately three times its initial value. In this manner, it is possible to conclude that the capacitors used can be considered old when their ESR value is approximately 0.18 Ω. Consequently, to simulate old capacitors, a resistance of 0.1 Ω was introduced in series with the new capacitor. In this way, the total ESR value of the electrolytic capacitors would be:

$$ESR_{TOTAL} = ESR_{INTRINSEC} + Resistance = 0.06 + 0.1 = 0.16\,\Omega$$

Table I shows the different considered cases.

Table I: Different considered cases

Case	Fig	L_1	L_2	C_1	ESR_1	C_2	ESR_2
(units)	-	(μH)	(μH)	(μF)	(Ω)	(μF)	(Ω)
I	*3 (a)*	*44*	-	*470*	*0.16*	-	-
II	*3 (b)*	*44*	-	*470*	*0.16*	*470*	*0.16*
III	*3 (c)*	*44*	*1.5*	*470*	*0.16*	*470*	*0.16*
IV	*3 (c)*	*44*	*3*	*470*	*0.16*	*470*	*0.16*

Fig. 7 shows the simulated and experimental waveforms of Δv_O for the first case study described in Table I.

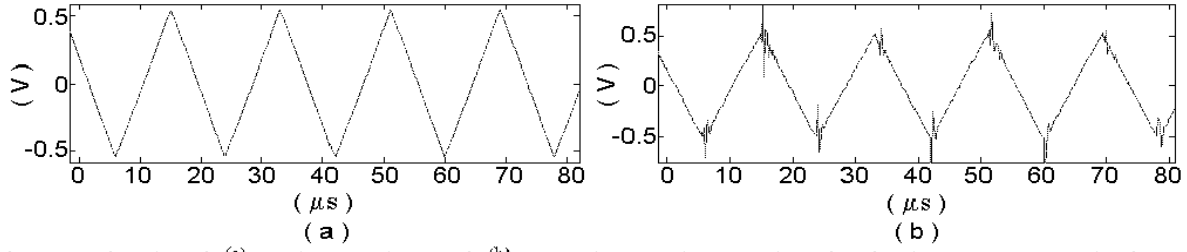

Fig. 7: Simulated [(a)] and experimental [(b)] waveform of Δv_O, for the basic converter of Fig. 3 (a), considering and old capacitor, $ESR_{Total} = 0.16\,\Omega$.

Using (9) and (11), it is possible to compute the output voltage ripple for case *I* (Fig. 7):

$$\Delta V_O \Big\|_{Case\,I} = R_{Load}\,\Delta i_O \cong \frac{V_{in}\left(D_{ON} - D_{ON}^{\,2}\right) ESR\, T\, R_{Load}}{L\left(ESR + R_{Load}\right)} = \frac{66\times\left(0.5 - 0.5^2\right)\times 0.16\times 18\times 10^{-6}\times 10}{44\times 10^{-6}\times\left(0.16 + 10\right)} \cong 1.06\,V$$

ISBN : 90-75815-08-5

From (12), it is possible to conclude that, for the basic buck converter, the increase of output voltage is almost linear with the increase of ESR.

Fig. 8 shows the simulated and experimental waveforms of Δv_O, for the situation *II* described in Table I.

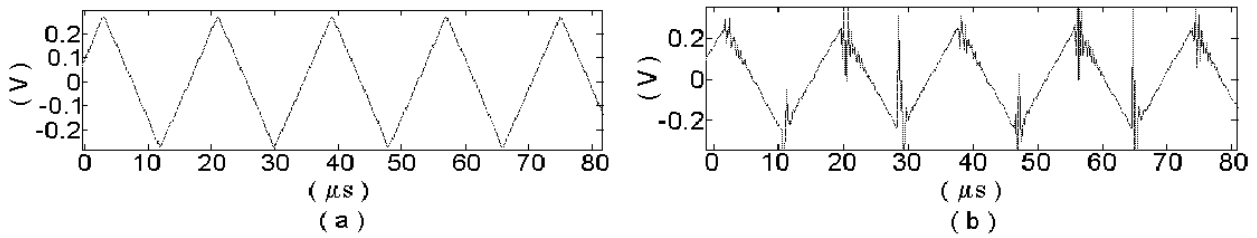

Fig. 8: Simulated [(a)] and experimental [(b)] waveforms of Δv_O, for the converter of Fig 3 (b), considering an ESR of 0.16 Ω, for both capacitors.

Using (9) and (13) it is possible to compute the output voltage ripple for the case study *II*:

$$\Delta V_O\Big\|_{Case\ II} = R_{Load}\ \Delta i_O \cong \frac{V_{in}\left(D_{ON} - D_{ON}^{\ 2}\right) T\ ESR_1\ ESR_2 R_{Load}}{L\left(ESR_1\ ESR_2 + R_{Load}\left(ESR_1 + ESR_2\right)\right)} = \frac{66\times\left(0.5-0.5^2\right)\times 18\times 10^{-6}\times 0.16\times 0.16\times 10}{44\times 10^{-6}\times\left(0.16\times 0.16+10\times\left(0.16+0.16\right)\right)} = 0.54\,V$$

Fig. 9 shows the simulated and experimental waveforms of Δv_O for the case *III* described in Table I.

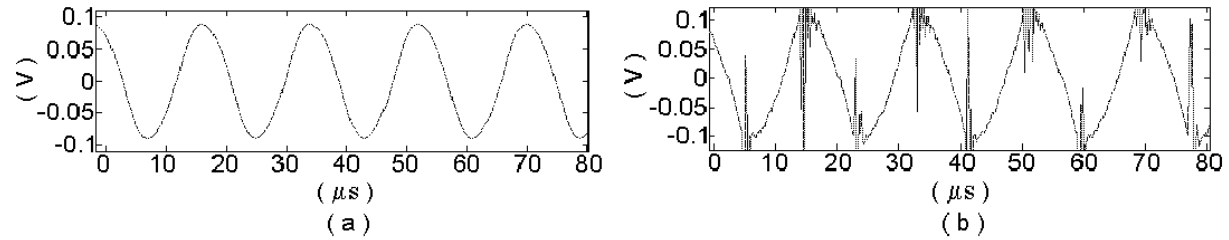

Fig. 9: Simulated [(a)] and experimental [(b)] waveforms of Δv_O, for the converter of Fig 3 (c), considering L_2 = 1.5 μH and ESR = 0.16 Ω, for both capacitors.

Using (9) and (14) it is possible to compute the output voltage ripple for the case study *III*:

$$\Delta v_O\Big\|_{Case\ III} \cong \frac{R_{Load}\ V_{in}\left(D_{ON} - D_{ON}^{\ 2}\right) T\ ESR_1\ ESR_2}{\left(ESR_1\ ESR_2 + R_{Load}\left(ESR_1 + ESR_2\right) + 2\,\pi\ f\ L_2\left(ESR_2 + R_{Load}\right)\right) L_1} = \frac{76.03\times 10^{-6}}{\left(3.2256+5.32\right)\times 44\times 10^{-6}} \cong 0.2\,V$$

If it was required an eighth of the initial voltage ripple (Δv_O = 0.125 V), according to (15) L_2 should take the value of approximately 3 μH. Fig. 10 shows the experimental and simulated waveforms of Δv_O for the case *IV* described in Table I.

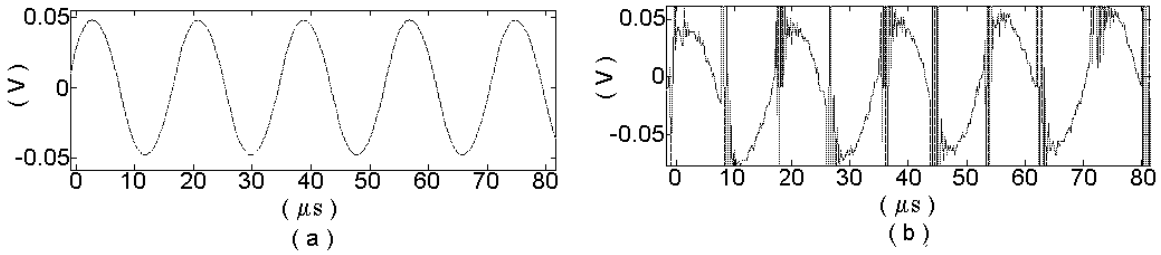

Fig. 10: Simulated [(a)] and experimental [(b)] waveforms of Δv_O, for the converter of Fig 3 (c), considering a L_2 = 3 μH and ESR = 0.16 Ω, for both capacitors.

From the observation of Figs. 7, 8, 9 and 10, it is possible to conclude that the use of two used capacitors in parallel, with the same ESR value, allows the reduction of the output voltage ripple to half of its initial value (when compared with the use of a single capacitor), and through the use of a CLC filter this value can be reduced to less than one fifth, when $L_2 = 1.5\ \mu H$ or to an eighth of its initial value, when $L_2 = 3\ \mu H$.

Performance versus impact of filter size and cost on the converter

Table II shows a comparison between the three different filters regarding their performance, size and cost.

Table II: Performance, size and cost of the three filters

Δv_O for an $ESR_1 = ESR_2 = 0.16\Omega$				Filter dimensions (ℓ x d) (mm)				Cost
Fig.3	theoretical	simulated	experimental	L_1 40 μH, 11A	L_2 3 μH, 9A	C_1 (mF) 0.47	C_2 (mF) 0.47	€ (euros)
a	1.06 V	1.08 V	1.08 V	7.5 x 29	-	16 x 30	-	4.45 €
b	0.54 V	0.54 V	0.49 V	7.5 x 29	-	16 x 30	16 x 30	5.17 €
c	0.12 V	0.10 V	0.11 V	7.5 x 29	25 x 7	16 x 30	16 x 30	7.05 €

From Table II, it is possible to conclude that with a small increase in size and cost of the output filter of switch mode DC-DC converters, a significant improvement in its response can be achieved. Fig. 11 shows the experimental output voltage ripple waveforms, for the three situations considered in Table II.

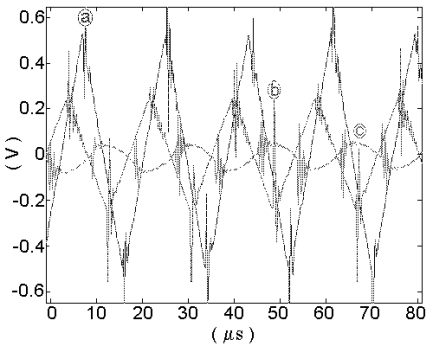

Fig. 11: Experimental waveforms of Δv_O, for the three cases considered in Table II.

Conclusions

One of the most serious problems in switch mode DC-DC converters is the effect of ESR in steady state regime. Thus, this paper presented an output filter that can be used in order to reduce the pernicious effect of the electrolytic capacitor's ESR in steady state regime. Some experimental, theoretical and simulated results were presented and showed a significant reduction of output voltage ripple, without increasing too much the size and cost of the converter.

References

[1].G. Oliver, Chaos in Buck Converter, Doctoral Thesis, Universitat Politècnica de Catalunya, April, 1997, pp.7-12.

[2]. Philip T. Krein. Elements of Power Electronics, Oxford University Press, New York, 1998.

[3]. Technical Notes, CAT.8101D, Nichicom Corporation

[4]. Precautions and Guidelines, CAT. Nº.E1001E, Nippon Chemi-Con Corporation, http://www.chemi-con.co.jp/english/catalog_e/TECH_NOTE/al_4e.html, 2005.

[5]. Michael L. Gasperi. Life Prediction Model for Aluminum Electrolytic Capacitors, IAS'96, October, 1996, pp 1347-1351.

[6]. Roland E. Thomas. The Analysis and Design of Linear Circuits, Prentice Hall, New Jersey, 1998.