A Sampling Algorithm for Digitally Controlled Boost PFC Converters

David M. Van de Sype, Koen De Gussemé, Alex P. Van den Bossche, and Jan A. Melkebeek
Electrical Energy Laboratory (EELAB)
Department of Electrical Energy, Systems and Automation (EESA), Ghent University
St-Pietersnieuwstraat 41, B-9000 Gent, Belgium
E-mail: vandesype@elmape.rug.ac.be, tel.: +32-9-2643420, fax: +32-9-2643582

Abstract – **Digital control of a boost power factor correction (PFC) converter requires sampling of the input current. As the input current contains a considerable amount of switching ripple and high frequency switching noise, the choice of the sampling instant is very important.**

To avoid aliasing without employing a (very) high sampling frequency, the sampling is synchronized with the pulse width modulation (PWM). Sampling algorithms employing this technique successfully reject the input current ripple but are not immune to the high frequency switching noise present on all sampled signals. Therefore, a new sampling algorithm, intended for center-based or symmetric PWM, is deduced with as most important features: switching noise immunity, straightforwardness, accurate measurement of the averaged input current and the need for only few processor cycles. The operating principle, design issues and a theoretical study of the input current error induced by the sampling algorithm due to sampling instant timing errors are derived. All theoretical results are validated experimentally by using a digitally controlled boost PFC converter switching at 50kHz.

I. Introduction

Most electronic and power electronic equipment uses DC internally. If supply from the AC grid is desired, conversion from AC to DC is required. For the low power range (<3.5kW), the widely employed single phase diode rectifiers constitute a nonlinear load to the mains. As a result, their AC input current waveform contains numerous harmonics of important magnitude, causing resonances, voltage waveform distortion, etc. [1]. To reduce the magnitude of the input current harmonics of rectifiers, power factor correction (PFC) is used.

To obtain a high power factor in single phase applications, the boost converter operating in continuous conduction mode (CCM), is often used. This is illustrated by the numerous papers covering this topic [3]–[9]. The reasons for the popularity of the boost converter for PFC are [2]: good silicon usage, smooth current waveform with reduced input filter requirements, and simple drive and control circuitry compared to other types of PFC converters.

For reasons of price, in most cases the control algorithms for single-phase PFC converters are implemented as analog circuits. For the near future, as the price/performance ratio of digital processors is expected to decrease further, there is a fair chance that the analog control circuits will be abandoned in favor of digital implementations. This tendency can be illustrated by the recent interest in digital control of PFC converters [4]–[9]. As the bandwidth of the voltage control loop is relatively low, requiring no fast ADC nor fast processor, the voltage control loop is easily implemented digitally [4]–[7]. Papers reporting full digital control, including the fast current control loop, have appeared only recently [8], [9].

This paper deals with an essential part of any digital control algorithm: the sampling algorithm. The sampling algorithm for the boost PFC converter published in [9] guarantees switching noise immunity and is intended for end-of-on-time asymmetric PWM. The new sampling algorithm described in this paper is intended for symmetric or center-based PWM. The main features of the new sampling algorithm are: switching noise immunity, straightforwardness, accurate measurement of the averaged input current and the need for only few processor cycles. The feasibility of the proposed algorithm and the theoretical results obtained, are verified experimentally by using a digitally controlled boost PFC converter.

II. Digital Control of the Boost PFC Converter

Fig. 1 shows the circuit diagram employed. For the purpose of digital control, the analog control variables (the input current i_L, the input voltage v_{in} and the output voltage v_o) must be converted to digital quantities by the ADC converter. The process of sensing the control variable, amplifying the sensor output to the appropriate range and the analog-to-digital conversion, can be represented as a division of the analog control variables by their respective reference values (I_L^{ref}, V_{in}^{ref} and V_o^{ref}).

Like its analog counterpart, the digital controller consists of a current loop and a voltage loop. For the current loop, the input current $i_{L,n}$ is subtracted from the commanded input current $i_{L,n}^*$. The resulting current error $i_{e,n}$ is fed to the current loop controller, a digital PI-controller. Finally, the output, the duty-ratio d_n, is provided to the digital PWM, controlling the switch S. The commanded input current $i_{L,n}^*$ is derived by multiplying the input voltage $v_{in,n}$ with the value for the desired input conductance of the PFC converter $g_{e,n}$. The latter is provided by the voltage loop controller.

III. Sampling Algorithms

A. Problem Definition

The switching of the boost converter causes a switching ripple with large magnitude in the input current (Fig. 2, lower trace). Hence, an accurate reconstruction of the sampled input current is possible only if the sampling frequency is sufficiently higher than the switching frequency ($f_{sam}>10f$). As the switching frequency is already high ($f>20$kHz), a much higher sampling rate is hard to reach and will leave the processor not enough cycles to perform the necessary

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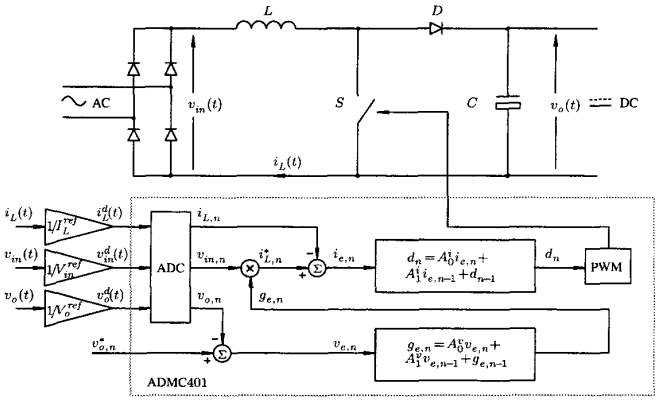

Fig. 1. A digitally controlled boost PFC converter.

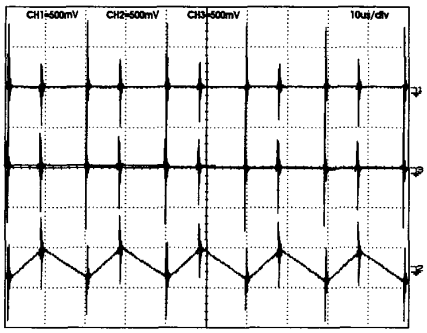

Fig. 2. The three control variables before the ADC. Signals from top to bottom: the output voltage, the input voltage, the input current.

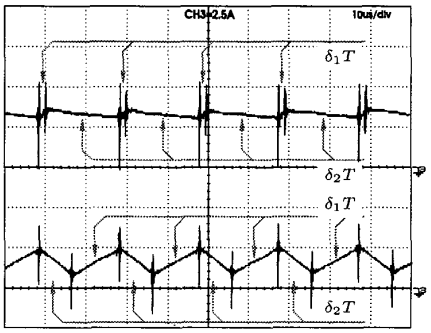

Fig. 3. The input current seen by the ADC. **Upper trace**: small duty-ratio. **Lower trace**: larger duty-ratio.

calculations for control. Using a lower sampling frequency will cause aliasing. By inserting a prefilter before the ADC, aliasing can be avoided, but this conflicts with the need for a large bandwidth of the current control loop. However, if the sampling frequency is synchronized with the switching frequency, the switching ripple becomes a hidden oscillation, not appearing in the reconstructed signal. Moreover, if the sampling frequency is chosen equal to the switching frequency, a large bandwidth of the current control loop is possible, while ample time is left for the processor to perform the necessary control calculations. For all sampling algorithms described in this paper the sampling frequency is equal to the switching frequency.

For the purpose of digital control, three control variables must be sampled (Fig. 1): the input current, the input voltage and the output voltage. Due to switching noise coupled to the sensors and to the signal chain during switching transitions, high peaks appear on all control variables offered to the ADC (Fig. 2). As the sampling of a real ADC lasts a finite time, the accuracy of the sampled output is affected by sudden changes of the sampled input during the sampling. Consequently, the occurrence of high frequency switching noise during the sampling process will result in improper system behaviour due to large errors on the value of the obtained samples. Hence, a careful selection of the sampling instants is necessary.

B. Rising-Edge-Sampling and Falling-Edge-Sampling

For the rising-edge-sampling (RES) algorithm or for the falling-edge-sampling algorithm (FES), the center of the on-time or the center of the off-time of the switch S are used as a reference for the sampling instants. As for symmetric or center-based PWM the middle of the on-time and off-time always remains fixed within the switching period, samples are rendered at a steady sampling rate. This allows to apply the z-transform to the obtained samples, leading to a straightforward approach for the current control loop design. Moreover, if the samples are taken in the middle of the rising edge of the measured inductor current (for RES, time $\delta_1 T$ in Fig. 3 and Fig. 5) or in the middle of the falling edge of the measured inductor current (for FES, time $\delta_2 T$), the produced samples are a direct measure for the averaged inductor current $\langle i_L \rangle$, allowing accurate shaping of the input current waveform. To compensate for the phase-lag induced by the lowpass filters in the signal chain, and for the delay between the switching command of the processor and the actual switching of the switch S, a delay τ_d is introduced between the center of the PWM commands and the sampling instants.

Neither the RES algorithm, nor the FES algorithm are immune to high frequency switching noise. For duty-ratios

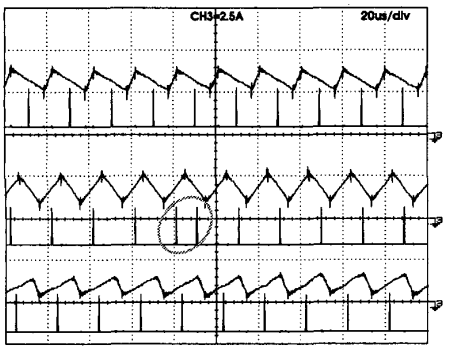

Fig. 4. The sampling instants for the AES algorithm ($\delta_c = 0.5$). **Upper traces:** $d_n < \delta_c$. **Center traces:** $d_n \approx \delta_c$. **Lower traces:** $d_n > \delta_c$.

close to 0, the accuracy of the samples obtained by RES (Fig. 3, upper trace, instants $\delta_1 T$) suffers from the high frequency switching noise present on all signals. The same applies for FES, for duty-ratios close to 1. As for PFC boost converters, the duty-ratio ranges from 1 (at the zero-crossing of the grid voltage) to almost 0 (for high line voltage or low output voltage), neither RES, nor FES provide accurate samples under all conditions.

C. Alternating-Edge-Sampling

As the switching noise immunity for RES is only affected at duty-ratios close to zero, and for FES at duty-ratios close to unity, switching noise immunity can be tremendously improved by using alternately RES for large duty-ratios however FES for small duty-ratios. For the boost PFC converter the duty-ratio continuously shuffles back and forth from zero (or close to zero) to unity. Thus the DSP needs to decide cycle by cycle upon the sampling edge for the next cycle. The resulting sampling algorithm is called alternating-edge-sampling (AES).

To allow the DSP to decide upon the sampling edge for the next cycle a cross-over duty-ratio δ_c must be chosen. Hence, if the duty-ratio is larger than δ_c, RES is chosen, while if the duty-ratio d_n is smaller than δ_c FES is chosen. This is illustrated in Fig. 4. The value of the cross-over duty-ratio δ_c is chosen in the vicinity of $1/2$, guaranteeing good switching noise immunity. One take-over from RES to FES or vice-versa occurs once every quarter of the mains period (Fig. 9). To avoid erroneous multiple transitions, hysteresis can be added to the value of δ_c, with hysteresis band Δ. Thus, the transition from RES to FES takes place when $d_n < \delta_c - \Delta$ and the transition from FES to RES occurs for $d_n > \delta_c + \Delta$.

Both RES and FES produce samples that accurately reflect the value of the average input current $\langle i_L \rangle$, but neither of them guarantee immunity against high frequency switching noise. The new sampling algorithm is based on RES and FES, but assures good switching noise immunity. As a result, the new sampling algorithm inherits the accurate averaged input current sampling and is intended for combination with center based or symmetric PWM.

IV. Input Current Distortion Induced by the Sampling Algorithm

A. Assumptions

To allow the calculation of the input current distortion caused by the sampling algorithm, some assumptions are made:

- The line voltage is sinusoidal with magnitude $\widehat{V}_g$ and angular frequency ω_g:

$$v_g(t) = \widehat{V}_g \sin(\omega_g t). \tag{1}$$

- The converter operates in CCM.
- There is no high frequency switching noise present on the sampled signals. Hence, sampling errors due to high frequency switching noise are not taken in account.
- As the converter dynamics are fast compared to the AC line frequency, the quasi-static approximation is employed. This implies that the converter operates near equilibrium with a slowly moving quiescent operating point. Hence, the input voltage $v_{in}(t)$ and output voltage $v_o(t)$ exhibit only small variations during one switching period. Even though the input current $i_L(t)$ alters quickly in a switching period, its properties, the input current ripple and the averaged input current, can be represented by slowly varying continuous functions of time: $\Delta i_L(t)$ and $\langle i_L \rangle(t)$, respectively.
- The current controller assures perfect tracking of the commanded input current, or:

$$i_{L,n} = i^*_{L,n} = g_{e,n} v_{in,n}. \tag{2}$$

- The desired input conductance of the PFC converter remains constant, or $g_{e,n} = g_e$. Consequently, no input current distortion is induced by the voltage control loop.
- The output capacitor C (Fig. 1) has a very large capacitance value. Therefore, the output voltage is nearly constant, or $v_o(t) \approx V_o$.

Achieving a resistive input for PFC converters is desirable, as this results in a high power factor and in damping of possible resonances of the feeding grid. A resistive input is obtained if the current controller makes the averaged input current $\langle i_L \rangle$ accurately trace the waveform of the input voltage:

$$\langle i_L \rangle(t) = G_e v_{in}(t) = G_e \widehat{V}_g \left| \sin(\omega_g t) \right|, \tag{3}$$

with G_e the emulated input conductance of the PFC converter. However, with digital control the current controller uses the sampled input current instead of the averaged input current to shape the input current. Because of the large switching ripple of the input current i_L, the position of the sampling instants within the switching period determines the deviation of the obtained input current samples from the averaged input current value (Fig. 5 $\delta_1' T$ instead of $\delta_1 T$). As the sampled input current is used for control instead of the

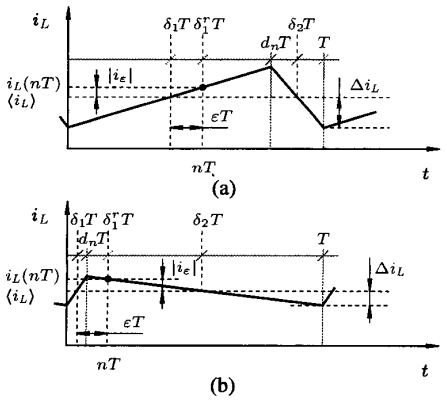

Fig. 5. The sampling instants for the RES, FES and AES algorithms.

averaged input current, the latter may differ from (3), yielding input current distortion. Since the position of the sampling instants within the switching period is determined by the sampling algorithm, the latter will have a profound effect on the distortion of the input current. If the zeroth sampling moment defines $t=0$, the difference between the averaged input current and the input current sample for the n-th sampling instant is:

$$i_\varepsilon(nT) = \langle i_L \rangle(nT) - i_L(nT). \tag{4}$$

Inspection of Fig. 1 combined with (1) and (2) leads to:

$$\begin{aligned} i_L(nT) &= g_{e,n} \left(\frac{I_L^{ref}}{V_{in}^{ref}} \right) \widehat{V}_g \left| \sin(\omega_g nT) \right| \\ &\triangleq G_e \widehat{V}_g \left| \sin(\omega_g nT) \right|, \end{aligned} \tag{5}$$

or the input current samples represent a rectified sinusoid in phase with the input voltage (1). Consequently, the current i_ε in (4) represents the deviation of the averaged input current from the desired input current.

B. Rising-Edge-Sampling and Falling-Edge-Sampling

Under quasi-steady-state conditions, the samples obtained by using the RES or FES algorithm are an accurate measure for the averaged inductor current $\langle i_L \rangle$. However, if the real sampling instants, $\delta_1^r T$ for RES (Fig. 5) and $\delta_2^r T$ for FES (not shown), differ from the 'ideal' sampling instant or $\delta_1 T$ and $\delta_2 T$, respectively, the acquired samples deviate from the averaged inductor current. The timing error εT is caused by a mismatch between the introduced delay τ_d and the delay it is compensating for: the sum of the delay induced by the low-pass filters in the signal chain, and the delay between the switching command of the processor and the actual switching of the switch S.

If the samples for the RES algorithm correspond to the sampling instant $\delta_1^r T$ instead of to the 'ideal' sampling instant $\delta_1 T$ (Fig. 5(a)), the n-th sample of the input current is:

$$i_L(nT) = \langle i_L \rangle(nT) + \varepsilon T \left. \frac{\mathrm{d}i_L}{\mathrm{d}t} \right|_{\substack{rising \\ edge}}. \tag{6}$$

Using (4), the input current error becomes:

$$i_\varepsilon(nT) = -\varepsilon T \left. \frac{\mathrm{d}i_L}{\mathrm{d}t} \right|_{\substack{rising \\ edge}}. \tag{7}$$

For the boost converter operated in CCM under quasi-static assumptions, the input current slope during the on-time of the switch is:

$$\left. \frac{\mathrm{d}i_L}{\mathrm{d}t} \right|_{\substack{rising \\ edge}} = \frac{2\Delta i_L(nT)}{d_n T}, \tag{8}$$

while the input current ripple can be expressed as:

$$\Delta i_L(nT) = (1-d_n) d_n \frac{V_o T}{2L} \triangleq 4(1-d_n) d_n \Delta I_L^{max}, \tag{9}$$

with ΔI_L^{max} the maximum input current ripple or the input current ripple when the duty-ratio is at 50%. Combining (8) and (9) with (7) yields:

$$i_\varepsilon(nT) = -8\varepsilon \Delta I_L^{max} (1-d_n). \tag{10}$$

For a sinusoidal line voltage and a constant output voltage, the duty-ratio becomes:

$$d_n = 1 - \frac{v_{in}(nT)}{V_o} = 1 - \alpha \left| \sin(\omega_g nT) \right|, \tag{11}$$

with $\alpha = \widehat{V}_g / V_o$. Hence, the input current error (10) becomes:

$$i_\varepsilon(nT) = -8\varepsilon \Delta I_L^{max} \alpha \left| \sin(\omega_g nT) \right|. \tag{12}$$

A similar analysis for the input current error when using the FES algorithm leads to:

$$i_\varepsilon(nT) = 8\varepsilon \Delta I_L^{max} d_n, \tag{13}$$

or,

$$i_\varepsilon(nT) = 8\varepsilon \Delta I_L^{max} \left(1 - \alpha \left| \sin(\omega_g nT) \right| \right). \tag{14}$$

For RES the input current error is described by (12). However, if the duty-ratio is small ($d_n/2 < \varepsilon$ as in Fig. 5(b)) the sampling instant occurs during the falling edge instead of during the rising edge. Hence, for a small duty-ratio the input current error is not (7), but:

$$i_\varepsilon(nT) = -\frac{d_n T}{2} \left. \frac{\mathrm{d}i_L}{\mathrm{d}t} \right|_{\substack{rising \\ edge}} + \left(\varepsilon - \frac{d_n}{2} \right) T \left. \frac{\mathrm{d}i_L}{\mathrm{d}t} \right|_{\substack{falling \\ edge}}. \tag{15}$$

As the relative timing error ε is in most cases small ($\leq 1\%$), this situation only occurs for small duty-ratios. Since the slope of the input current during the falling edge is very small for small duty-ratios, the input current error can be approximated by:

$$i_\varepsilon(nT) \approx -\frac{d_n T}{2} \left. \frac{\mathrm{d}i_L}{\mathrm{d}t} \right|_{\substack{rising \\ edge}} = -\Delta i_L(nT). \tag{16}$$

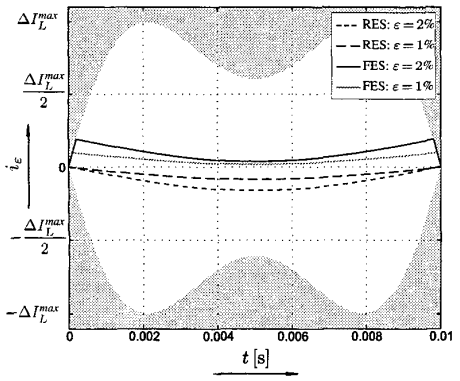

Fig. 6. The error on samples caused by the different sampling algorithms for $\alpha = 0.81$ (during half a mains period).

A comparable situation occurs for the FES algorithm when the duty-ratio is large ($(1 - d_n)/2 < \varepsilon$). Under these conditions the input current error can be approximated by:

$$i_\varepsilon(nT) \approx \Delta i_L(nT). \tag{17}$$

The resulting current error, for RES a combination of (12) and (16) and for FES a combination of (14) and (17), is depicted in Fig. 6 for various values of the relative timing error ε. The grey area encompasses the area of possible measurement errors on the input current due to the sampling algorithm. As the measurement error can't be larger in magnitude than the input current ripple, the edge of the grey area is expressed as $\pm\Delta i_L(t)$. Although for FES, (14) and (17) are clearly distinguishable, for RES (16) is not visible. This is due to the fact that for the boost PFC converter the duty-ratio reaches unity (at the zero-crossing of the grid voltage) but never becomes smaller than $(1-\alpha)$. Hence, for the FES algorithm the conditions are met to apply (17) while for RES (16) only applies when α is close to unity, thus only for a high line voltage or a low output voltage.

Both (12) and (14) show that the current error i_ε is proportional to the relative timing error ε and the maximum input current ripple ΔI_L^{max}. Consequently, the input current error can be reduced by designing the converter for a low input current ripple and by diminishing the relative timing error. As the current error i_ε is independent of the rms-value of the input current, the influence of the input current error on the input current waveform is best visible at low power.

For the RES algorithm, the input current error (12) (Fig. 6) only contains a fundamental component pulsating with the grid frequency. As the voltage control loop will compensate for a difference between input and output power by changing the commanded input conductance, the timing error for the RES algorithm will have no effect on the waveshape of the input current of the PFC converter. However, for the FES algorithm the input current error is nonsinusoidal ((14) and Fig. 6). As only the error on the fundamental of the input current is compensated for by the voltage control loop, odd order harmonics are induced in the input current. Consequently, keeping the timing error εT small is important when applying the FES algorithm.

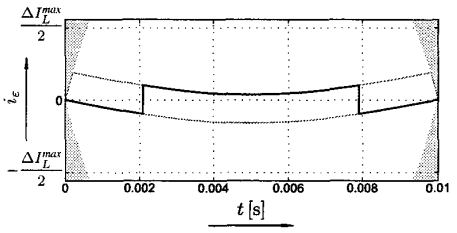

Fig. 7. The error on samples caused by the AES algorithms for $\alpha = 0.81$ and $\varepsilon = 2\%$ (during half a mains period).

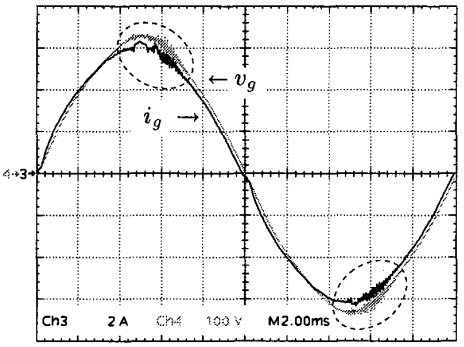

Fig. 8. Input current distortion caused by erroneous samples obtained with the RES algorithm for low output voltage ($V_g = 230$V, $V_o = 340$V).

C. Alternating-Edge-Sampling

As the AES algorithm switches between RES and FES, the input current error is a combination of the input current error curves for both algorithms (Fig. 7). At the crossover of the grid voltage, the duty-ratio is larger than the crossover duty-ratio δ_c. The samples are taken during the rising edge and the input current error is inherited from the RES algorithm. As the grid voltage rises, the duty-ratio sets until it reaches δ_c. At this point the sampling edge is moved to the falling edge. Consequently, the input current error adopts the input current error of the FES algorithm. Hence, each time the algorithm switches between RES and FES, the input current error abruptly jumps between the according input current error curves as depicted in Fig. 7.

If the cross-over duty-ratio δ_c is chosen equal to 0.5, the AES algorithm always chooses the sampling edge that provides the smallest magnitude for the input current error, or:

$$|i_\varepsilon^{AES}| = \min(|i_\varepsilon^{RES}|, |i_\varepsilon^{FES}|). \tag{18}$$

Nevertheless, in the presence of a timing error, the input current error caused by the AES algorithm is nonsinusoidal and will cause harmonic distortion of the input current. As a consequence, maintaining a low input current distortion requires small values of the timing error εT.

V. Experimental Results

The sampling algorithms were tested by using an experimental setup. The entire control for the boost PFC con-

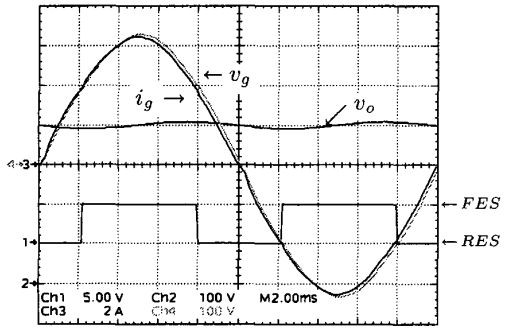

Fig. 9. Key waveforms for the PFC converter using the AES algorithm ($P_o = 1000$W).

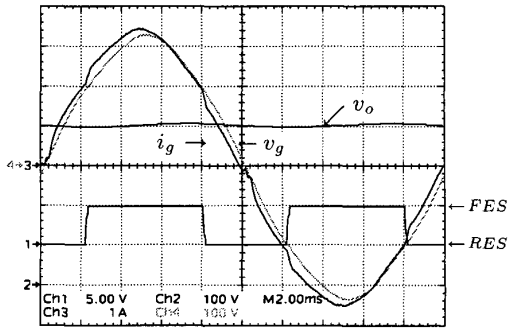

Fig. 10. Input current distortion caused by a relative timing-error $\varepsilon = 2\%$ for AES ($P_o = 500$W).

verter was implemented on the ADMC401 of Analog Devices. The S and D switches of the boost rectifier are MOSFET SPP20N60S5 and diode RURP3060 respectively. The passive components used have $L = 1$mH and $C = 470\mu$F. The converter switches at 50kHz, supplies 400V DC at the output and is rated at 1kW output power for an input voltage range of 190V–264V AC. For the cross-over duty-ratio of the new sampling algorithm $\delta_c = 0.5$ has been chosen.

Due to the high frequency switching noise, samples obtained by using the RES algorithm or the FES algorithm may be erroneous, causing improper system behavior. The sensitivity to high frequency switching noise is demonstrated in Fig. 8, for RES combined with a low output voltage. For a low output voltage the duty-ratio reaches zero close to the top of the grid voltage. Hence, the input current distortion caused by faulty samples of the RES algorithm appears here. As the internal impedance of the feeding grid is not zero, distortion of the grid voltage is also observed. For FES, line current distortion due to switching noise, is expected close to the zero crossing of the line current. However, as the high frequency switching noise is less pronounced at low input current, FES shows less problems of immunity than RES. None of our experiments using the FES algorithm have revealed any line current distortion caused by erroneous samples. Nevertheless, high frequency switching noise immunity can't be guaranteed for the FES algorithm.

The sampling instants for the AES algorithm are shown in Fig. 4. This figure clearly demonstrates the principle of operation of this algorithm. For large duty-ratios the sampling instant occurs at the center of the rising edge of the input current (lower trace), while for small duty-ratios the center of the falling edge of the input current is used (upper traces). Somewhere in between the sampling edge is changed (center traces). Although the hysteresis band Δ is zero, no erroneous transitions occur. Fig. 9 shows the key operating waveforms of the boost PFC converter employing full digital control. 'Trace 1' indicates the sampling edge chosen by the sampling algorithm. As the relative timing error is easily reduced below 0.5% ($\varepsilon T < 100$ns), the effect of the input current error is not visible. In order to make the input current error clearly visible, the relative timing error was artificially increased to 2% ($\varepsilon T = 400$ns) and the output power was reduced to 500W (Fig. 10). Due to the timing error, an input current error is induced comparable with Fig. 7. The change of sampling from rising edge to falling edge or vice-versa is clearly visible as a fast change in the input current. However, as the employed current controller is not ideal (as assumed for the theoretical analysis), the match between the theoretical input current waveform (Fig. 7) and the experimental waveform (Fig. 10) is not perfect.

VI. Conclusion

A new sampling algorithm has been presented with as most important features: switching noise immunity, straightforwardness, accurate measurement of the averaged input current and the need for only few processor cycles. These features make the proposed sampling algorithm extremely fit for digital control of boost PFC converters.

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