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Energy Management Systems on Board of Electric Vehicles, Based on Power Electronics

Thesis for the degree of Philosophiae Doctor

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Preface

The tale of the Electric Vehicle is an interesting one. The subject has generated passionate discussions since the advent of personal transportation for the masses, in the beginning of the 19th century. Since then, countless times the electric car has been announced as the next world-saving technology, and an equivalent number of times the same technology has been discarded as hopeless.
Now, on the verge of increasing oil prices and environmental awareness, once again there are enthusiasts convinced that the struggle may have come to an end, and the public can finally enjoy the pleasure of driving quiet, non-polluting vehicles. This thesis is intended to be a small contribution to the cause of this wonderful historical loser that is the electric car.

It has to be said that if it was not for Marta, the thesis would probably be about the application of power electronics to some kind of active filtering technique for power quality: certainly a technically sound and important subject, but not nearly as charming as automotive. It was Marta that convinced me that I should have dedicated myself to this theme and, as it is too often the case, she proved right: working on the thesis has been a stimulating and rewarding experience, to the point that I am almost sad that it has finally come to an end.

During the four-year-long stay at NTNU, I have become a richer person, and have struggled to become a better one. I have received the best gift a man could ask for, and her name is Virginia. I have seen our eldest daughter, Sofia, growing up and learning a number of languages that I would have not dreamed about when I was her age. I have witnessed Marta fulfilling one of her objectives as she was appointed with Professorship. Obviously, a single page is hardly enough to thank for all that.

Special thanks go to my supervisor, prof. Tore Undeland, who backed my decision of such a sudden shift in the working subject and has worked hard to establish contacts with the Norwegian electric car company Th!nk, whose economical help has been very helpful for building the experimental prototypes.

The support of my co-supervisor, prof. Yoichi Hori, has also been fundamental, bringing his knowledge and working experience with supercapacitors applied to electrical transportation, and hosting me in Tokyo University for three months.

During my research stay at ENO, I have enjoyed exchanging ideas with my fellow PhD candidates Erik, William and Pål, and with my friend Supratim: I thank them all for the time they have spent, listening to my problems and ideas, and for the suggestions that those discussions have brought forward.

Moreover, I wish to express my gratitude to Vladimir and Bård, who helped me building the experimental prototypes, and to Inger and Eva who have been my references for solving all kind of administrative matters.

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Trondheim, December 2008

Giuseppe Guidi

Abstract

The core of any electric vehicle (EV) is the electric drive train, intended as the energy conversion chain from the energy tank (typically some kind of rechargeable battery) to the electric motor that converts the electrical energy into the mechanical energy needed for the vehicle motion.
The need for on-board electrical energy storage is the factor that has so far prevented pure electric vehicles from conquering significant market share. In fact electrochemical batteries, which are currently the most suitable device for electrical energy storage, have serious limitations in terms of energy and/or power density, cost and safety. All those characteristics reflect in pure electric vehicles being outperformed by standard internal combustion engine (ICE) based vehicles in terms of driving range, time needed to refuel and purchase cost.
Electric vehicles do have their distinctive advantages, being intrinsically much more efficient, operating at zero emissions at the pipe, and offering a higher degree of controllability that can potentially enhance driving safety. No wonder then, that electric energy storage technology has attracted considerable R&D investments, resulting in new traction battery packs that are getting closer and closer to the industrial targets.
In this scenario of EV technology gaining momentum, power electronics engineers have to come up with newer solutions allowing for more efficient and more reliable utilization of the precious on-board energy that comes in a form that cannot be directly utilized by the motor. At present, most of the research in the area of power electronics for automotive is focused in volume and cost reduction techniques. The increase in power density is pursued by developing components that can be operated at higher temperature, thus relieving the requirements on cooling.
In this thesis, the focus is on the development of alternative topologies for the power electronics converters that make use of some peculiarities of the energy storage components and of the electrical drive train in general, rather than being a mere component-level optimization of well established topologies.
A novel converter topology is proposed for hybridization of the energy source with a supercapacitor-based power buffer being used to assist the main traction battery. From the functional point of view, the topology implements a bidirectional DC/DC converter.

Making use of the fact that the battery terminal voltage is close to constant, an arrangement for the supercapacitors is devised allowing for bidirectional power flow by using power electronics devices of lower ratings than the ones needed in conventional DC/DC converters. At the same time, much smaller magnetic components are needed. Theoretical analysis of the operation of the proposed converter is given, allowing for optimized design. A full-scale experimental prototype rated at 30 kW, intended for use in a pure EV, has been built and tested. Results validate the theory and show that no particular impediment exist to the deployment of the concept in practical applications.

Another concept introduced in the thesis is an architecture where the traction inverter is embedded in the energy storage device. The latter is constituted by several modules, as in the case of modern Li-ion battery systems, and each module is equipped with a local power electronics interface, making it functionally equivalent to a controllable voltage source. The result is a modular, distributed system that can be engineered to have very high reliability and also to exhibit self-healing properties. A prototype with a minimum number of modules has been built and tested. Results confirm the effectiveness of the system, and make it a good candidate for deployment in applications where reliability is the most important requirement.

Introduction

Power electronics plays an important role in the modern automotive industry, helping carmakers to improve the performance of their fleet while reducing energy consumption and emissions.
In electric vehicles (EV), where there is at least one electric motor contributing to the traction effort, power electronics converters are used to control the bidirectional power flow between the electrical energy tank (usually a rechargeable battery) and the motor. Additional converters are necessary when there are several electrical sources with different terminal characteristics that share the duty of supplying the motor. Due to the limited amount of energy per unit of mass that can be stored in electrochemical batteries, or in any other kind of electrical energy storage device to date, efficiency of the overall conversion chain is paramount. Moreover, on-board space is a very valuable commodity in automotive, leading to strict requirements in volume reduction, with resulting increase in power density of the required converters. Needless to say, higher efficiency and higher power density have to be achieved while decreasing the cost and increasing the reliability.
Taking the traction inverter as an example, the targets above are mainly being pursued by the introduction of advanced thermal management [1] and by the replacement of unreliable components like the electrolytic capacitors with analogous components built with a different technology [2]. New materials like SiC are also being investigated for the switching devices, in order to extend the working temperature range and to reduce losses [3,4]. However, from the topological point of view, the classical six-switches inverter structure is not likely to be replaced, and the only allowance for change is coming from the proposals of several soft switching techniques for loss reduction [5,6].
One aspect that influences the design of the overall power train is modularity, meaning that there is very little interaction at the design stage between the engineering teams working on the energy source (the advanced traction battery) and those working on the power electronics that should enable the energy exchange between that source and the traction motor. The battery module should make energy available at its terminals that should be possible to exchange at a sufficiently high rate (power) with sufficiently high efficiency, while the terminal voltage remains within reasonable range. The inverter

should be able to supply the motor, over the whole terminal voltage range of the battery. It is clear that the modular approach introduces some constraints in the specifications at the boundary between blocks (the DC-link voltage, in this specific case) that are in principle not related to the main purpose of the drive train: simply exchange energy at a given rate between the source and the motor.
Following this line of reasoning, it is possible that blending the design of the battery pack with that of the traction inverter leads to different system topologies that are worth to investigate. One of them, based on modular architecture where there is no neat distinction between the battery pack as a whole and the traction inverter, is investigated in the thesis.
When combining two energy sources having different electrical characteristics at the terminals, a power electronics interface is needed to allow controllable power flow. Specifications of the required converter are often given in terms of min-max of the input and output voltage and current, according to the characteristics of the sources. A deeper understanding of the dynamic electrical behaviour of the sources may however lead to a more optimized converter design. A practical application of this approach, where the capacitive behaviour of supercapacitors, along with the constant voltage behaviour of battery is explicitly taken into account during the converter design stage, can be found in the thesis.

Main contribution

The thesis has aimed at finding new methods for the interconnection of the classical components of an electrical traction system, based on dedicated power electronics topologies.
Throughout the thesis, the drive system as a whole has been considered, trying to take advantage of system-related aspects that are normally overlooked in a component-oriented approach.
Main contribution can be stated as follows:

- Introduction of a new power electronics converter topology for bidirectional power flow control between a supercapacitor-based power buffer and a battery, or any other energy source having DC terminal voltage characteristics.
- Detailed theoretical description of the concept, forming the basis for optimized converter design. It has been shown that the resulting converter uses considerably less silicon and much smaller magnetic components compared to standard topologies.
- Experimental verification of the power buffer on a real-scale prototype, showing that the concept is feasible and that the claimed advantages can be achieved in practice.
- Proposal of a distributed architecture where the traction inverter is embedded in the battery pack; in this vision, the energy tank is constituted by a large number of battery modules, each equipped with a power electronics interface, making it functionally equivalent to a controllable voltage source. Outstanding reliability is achieved due to the distributed nature of the system.
- Realization of the distributed architecture with a minimum number of modules, showing the self-healing property of such a distributed, intelligent system.

Thesis outline

The thesis is logically divided into four parts.

Chapter 1 and Chapter 2 contain background information needed for the understanding of the original concepts introduced later in the thesis.
In particular, Chapter 1 focuses on basic description of the main components found in the electrical drive train of pure electric vehicles (EVs) and internal combustion – electric hybrid vehicles (HEV); Emphasis is put on the electrical energy storage devices (batteries and supercapacitors), and the modelling of their electrical characteristics. Readers that are already familiar with the basic characteristics of an electric drive train and have some basic knowledge about traction batteries and supercapacitors may consider skipping this introductory chapter.
Chapter 2 describes the hybridization of the source of electrical energy on board of EVs; the combination of battery and supercapacitor is analyzed in detail, and its advantages are highlighted.

Chapter 3 to Chapter 5 describe the newly developed power electronics converter for power flow control between a supercapacitor-based power buffer and a battery, and are therefore the core of the thesis.
Chapter 3 gives the theoretical foundations of the proposed system and the equations governing its ideal operation are presented. Guidelines for optimal design of the system are also developed, based on an analytical approach.
Chapter 4 addresses the several issues arising when real-world components are utilized to build the converter, setting the basis for actual implementation of the proposed principle.
Chapter 5 contains details about the design and implementation of a real-scale prototype based on the proposed topology, intended for use in a small city vehicle like the Norwegian Th!nk EV. Experimental results are presented, demonstrating the feasibility and the advantages of the newly developed concept.

Chapter 6 describes the concept of a redundant, self-healing architecture for the implementation of the traction inverter in the drive system of an EV. A multilevel structure based on cascaded H-bridges, particularly well suited for battery EVs, is used to develop a decentralized, modular topology featuring a high degree of reliability. Both simulations and experimental results are presented, with some emphasis on the hardware design and on the communication system necessary to achieve redundancy and self-healing.

Finally, conclusions are drawn in Chapter 7, along with possibilities for further investigation and development in the field of power electronics applied to electrical transportation.

Publications generated by the PhD research work

Journals

1. **G.Guidi**, T.Undeland, Y.Hori, "An Interface Converter with Reduced Volt-Ampere Ratings for Battery-Supercapacitor Mixed Systems". IEEJ Trans. on Ind. Applicat. (D), Vol.128, No.4, 2008.
2. **G.Guidi**, T.Undeland, "Redundant and Self-Healing Drive System for Pure EV Based on Low Voltage Building Blocks". The World Electric Vehicle Association Journal, WEVA, Vol.1, 2007.

International, peer-reviewed, conferences

1. **G.Guidi**, T.Undeland, Y.Hori, "Optimized Power Electronics Interface for Auxiliary Power Buffer Based on Supercapacitors". Proc. of IEEE Vehicular Power Propulsion Conference VPPC08, Harbin, China, 2008.
2. **G.Guidi**, T.Undeland, Y.Hori, "An Optimized Converter for Battery-Supercapacitor Interface". Proc. of Power Electronics Specialists Conference PESC07, Orlando, 2007.
3. **G.Guidi**, T.Undeland, Y.Hori, " An Interface Converter with Reduced Volt-Ampere Ratings for Battery-Supercapacitor Mixed Systems". Proc. of Power Conversion Conference PCC07, Nagoya 2007.
   (Awarded as Best Paper in PCC '07).
4. **G.Guidi**,T.Undeland, "Redundant and Self-Healing Drive System for Pure EV Based on Low Voltage Building Blocks". Proc. of Electric Vehicle Symposium, EVS21, Yokohama, 2006.
5. **G.Guidi**, T.Undeland, Y.Hori, "Effectiveness of Supercapacitors as Power-Assist in Pure EV Using a Sodium Nickel-Chloride Battery as Main Energy Storage". Accepted for presentation at EVS24, 13-16 May, 2009, Stavanger, Norway.
6. P.Anreassen, **G.Guidi**, T.Undeland, "Digital variable frequency control for zero voltage switching and interleaving of synchronous buck converters", Proc. of EPE-PEMC 2006, Portoroz, Slovenia, 2006
7. S.Basu, T.Undeland, **G.Guidi**, "Voltage and current ripple considerations for improving ultra-capacitor lifetime while charging with switch mode converters", European Conference on Power Electronics and Applications, EPE 2007, Aalborg, Denmark.
8. J.I.Leon, **G.Guidi**, L.Franquelo, T.Undeland, S.Vazquez, "Simple control algorithm to balance the DC-link voltage in multilevel, four-leg, four-wire diode clamped converters", Proc. of EPE-PEMC 2006, Portoroz, Slovenia, 2006

LIST OF ABBREVIATIONS

CAN	Controller Area Network
CRC	Cyclic Redundancy Check
DOD	Depth Of Discharge
DSP	Digital Signal Processor
EDLC	Electric Double Layer Capacitor
EMI	Electro-Magnetic Interference
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FCV	Fuel Cell Vehicle
HB	Half Bridge
HC	Half Controlled
HEV	Hybrid Electric Vehicle
IC	Internal Combustion
ICE	Internal Combustion Engine
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
LPF	Low Pass Filter
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
OCV	Open Circuit Voltage
PWM	Pulse Width Modulation
SC	Supercapacitor
SOC	State Of Charge

TABLE OF CONTENTS

1 OVERVIEW OF EV TECHNOLOGY

1.1 Electric drive train

An electric drive train is a system that converts electrical energy into mechanical energy and, in its most classical form can be seen as constituted by four main elements:

- An electrical energy source;
- An electric power flow controller;
- An electric motor;
- A mechanical load

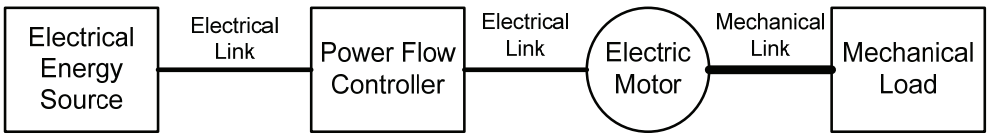


Fig. 1.1 – Basic structure of an electric drive train.

In some cases, the power flow can be reversed, allowing energy to be transferred back from the load to the electrical energy source. This operating mode in often referred to as "regenerative operation" or "regenerative braking".

All kinds of electric vehicles feature at least one electric drive train. In pure EV, the energy source is typically a rechargeable battery (secondary battery), and the electric motor is the only machine contributing to the traction effort. Fuel cell vehicles (FCV) have a very similar drive system, with the only difference that the primary source of electrical energy is a fuel cell; FCVs usually feature hybrid electric source (see chapter 2) to allow for regenerative operations and to achieve better efficiency. Hybrid vehicles (HEV) feature at least one additional internal combustion (IC) engine, contributing to the traction effort. In those vehicles, IC engine and electrical machine(s) can be coupled in a variety of ways, giving rise to several architectures whose description can be found in [7]. Detailed description of HEV is beyond the scope of the thesis, and the only characteristic that is pointed out here is that the structure of the electric drive trains can still be assumed to be same as in Fig. 1.1. Moreover, all kinds of HEVs include an

electrical energy storage device (typically a secondary battery) to allow for regenerative braking.
It is customary to model the drive train in terms of power flow between each component. Such an approach has the obvious advantage of being independent of the nature of the power itself (mechanical, electrical, thermal, and so on), allowing for complex systems to be analyzed within a simple theoretical frame.
Following this approach, the load is simply modelled as some kind of device asking for a given power profile; most of the power is used to originate the motion of the vehicle (traction effort), but some other part can be related to static electrical loads, like on-board air conditioning, lighting, and so on. In order for the power-flow model to describe accurately the system behaviour, efficiency of each component along the flow of power has to be properly modelled.
The electric motor is simply a reversible converter of electrical energy into mechanical energy, and its behaviour in the power-flow model is completely described by its conversion efficiency. Therefore, in principle, for power flow analysis it is not necessary to know the electrical details of the motor. In reality, there are many kinds of electrical motors that can be used for traction, the most widespread being DC motors, AC asynchronous motors, AC synchronous motors, switched reluctance motors. They all have different performance characteristics and all come with several design variations. What is common to them is that the efficiency is highly dependent on the operating conditions (speed, torque, voltage, current). The simple representation of the motor with its efficiency implies therefore a good deal of approximation, unless the power flow model is complemented with a more detailed description of the machine that can evaluate the efficiency at any given time.
The electric power flow controller is typically a power electronics converter that converts the electrical power at the terminals of the energy source into a form of electrical power that is suitable to supply the motor terminals in order to achieve the torque and speed at the shaft as required by the mechanical load. The power electronics converter is fully described by its efficiency in the power-flow model. Similarly to what was discussed for the motor, efficiency of any power converter is a complicated function of the operating conditions and detailed modelling of the converter topology may sometimes be necessary.
The electrical energy source can be modelled as a device that can either supply or store electrical energy with an operating efficiency that is normally a function of the power level. In the power flow model, in addition to the efficiency, at least a mean for establishing the amount of energy that can be supplied (or stored) by the source at any given time is necessary. As in the case of other components in the drive chain, efficiency of the energy source can be a complicated function of the operating conditions (terminal voltage, operating temperature, and so on).
From the aforementioned considerations, it is clear that starting from the high-level, macroscopic representation of the drive system in terms of power-flow, as shown in Fig. 1.2, any of the components' models can be refined to include detailed description of its structure and to give a means for precise evaluation of the efficiency to be used in the macroscopic model. The level of details that is needed is strictly dependent on the aim of the model.

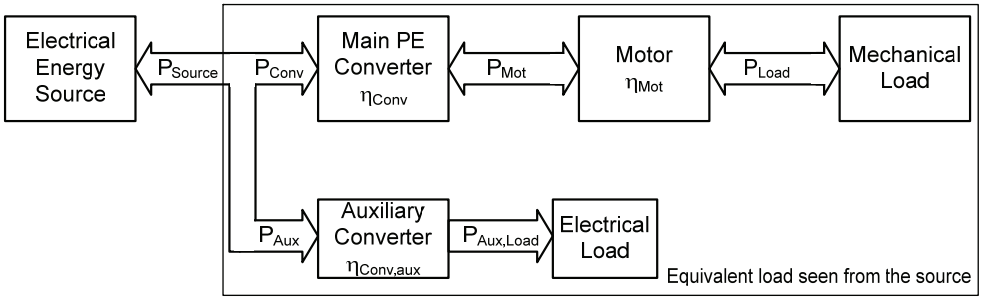


Fig. 1.2 – Macroscopic modelling of the drive train in terms of power flow.

From chapter 2 to chapter 5, the focus is on the analysis and design of the power electronics needed to control the power flow between the different components constituting the electrical energy source and the rest of the system, generally referred to as load. In this context, the electrical link between the energy sources and the load has to be modelled in detail, while the rest of the system (the "load") is simply seen as a "black-box" electrical subsystem with DC-like terminal characteristics.
In chapter 6, the aim is the analysis and design of a particular kind of traction inverter, embedded with the energy source. In this case, detailed topological modelling of the power electronics in the inverter is necessary.
The rest of this chapter is dedicated to the description of some of the commonest kind of electrical energy sources used in EVs, and the models that can be used to describe them.

1.2 Battery technology

Battery is a key component for any kind of pure electric vehicle, since to date it is the only device that can store enough electric energy to give the vehicle a reasonable driving range. A basic understanding of how battery works and what are their basic electrical characteristics and their major drawbacks is therefore necessary when trying to design an electric drive train.
In simple terms, a battery is a device that converts chemical energy to electric energy. The basic element of any battery is called a "cell", and is typically constituted by two electrodes and the electrolyte; the chemical reaction between the electrodes and the electrolyte is responsible for the generation of electricity. In most batteries (secondary batteries, or rechargeable batteries), the chemical reaction can be reversed, and electrical energy can be stored into chemical form, charging the battery.
For traction applications, the most important functional parameters for a battery are as follows:

- **Specific energy** (and energy density); the amount of energy stored for unit of mass (unit of volume).
- **Specific power** (and power density); the amount of power per unit of mass (unit of volume) that can be drained from the battery.
- **Cell voltage**; terminal voltage of an elementary cell.
- **Efficiency**; the ratio between the energy supplied by the battery and the energy required to return the battery to the state before discharge.
- **Operating temperature**.
- **Self discharge rate**.

- **Lifetime and cycle life**.
- **Recharge rate**; the rate at which energy can be returned to the battery.

In addition to the functional requirements, safety and cost also play a key role in the choice of the most suitable battery for a given application.
The best known and most widely used battery for traction systems is the lead acid battery. Although those batteries have a long history and their technology is quite mature, achievable performance does not quite match the requirements of an electric vehicle. In particular, specific energy is typically limited to about 30 *Wh/kg*, making it virtually impossible to achieve a driving range of few hundred kilometres for an EV that would use such a battery as main energy storage. Moreover, the cycle life of lead acid batteries is relatively poor, if deep discharge is required. On the other hand, cost is quite low and no particular safety issues exist related to the use of those batteries for high power, traction applications.
As a matter of fact, virtually all modern designs tend to discard the use of lead acid, and the battery chemistry is usually chosen among one of the following:

- Nickel metal hydride (NiMH);
- Sodium metal chloride (ZEBRA®);
- Lithium ion (Li-ion).

NiMH batteries bring a roughly twofold improvement in specific energy with respect to lead acid and, although their introduction into the market is relatively recent, they are now being produced with quite high volume. This is mainly because NiMH is the battery employed in the most successful IC-electric hybrid vehicle, the Toyota Prius, and in virtually any other commercial car of the same kind. However, the energy content of such a battery is still quite low and, perhaps more important, there are some concerns about the cycle life when the battery is cycled very deeply. The latter is a key factor, especially in applications like pure EV, when utilization of most of the energy available in the battery is vital to achieve reasonable driving range. It is a fact that the cycling life of virtually any kind of battery decreases exponentially with the depth of discharge [8] and, so far, the designer of hybrid IC-electric vehicles have been forced to use largely oversized batteries and use just a tiny bit (no more than 20%) of their potential energy content just to ensure a proper cycle life. It comes then to no surprise that for more energy intensive vehicles, like plug-in hybrids or pure electric, the NiMH chemistry tends to be replaced by more energy-dense options.
Sodium-nickel chloride (ZEBRA® , Zero Emissions Battery Research Association) [9] is the most promising kind of battery within the family of sodium-based chemistries. Such a battery needs to operate at the relatively high temperature of about 320 °*C*, and therefore additional system components are required to install the battery on board of EVs. In spite of that, specific energy is among the highest available (about 100 *Wh/kg*), and battery packs specifically developed and fully tested for automotive applications are commercially available. On the downside, specific power is not very high, and recharge time can be long. Perhaps even more important, the technology is proprietary of a single company (MES-DEA) causing some difficulties for widespread utilization in high numbers; for the same reason, it is quite difficult to find independent data about the performance characteristic of such a battery. ZEBRA® battery is given particular attention in this thesis, since it is the one deployed on the Norwegian Th!nk EV used as basis for the design of the system proposed in chapter 5.

There seems to be consensus about the fact that lithium-based batteries have the highest potential in terms of achievable energy density. They have been used extensively in portable electronics, but higher power packs are being developed by several companies, trying to meet the expectations of the many car manufacturers willing to have them as the main electric energy storage devices in next-generation plug-in IC-electric hybrids [10,11] or pure EVs [12,14]. Lithium-based batteries can also be designed to have relatively high specific power, and prototypes have been built allowing for very quick recharge by use of state-of-the-art nanotechnologies [15]; however, it should be noted that the increase in power density is usually achieved by trading off energy density. Although several high-performance (and high price) prototypes [16,17] have been developed based on lithium batteries, there are still some significant hurdles to large scale deployment of such high-power battery stacks. To begin with, cost is still too high to be readily accepted by the automotive community. Moreover, there is still not enough data to ensure proper operation of those stacks over a sufficiently long period of time, compatible to the requirements of the automotive industry. Last, but very important, there are still some safety concerns, due to the thermal runaway experienced by some lithium-based battery packs [18] that can occasionally lead to dramatic failures, especially when trying to recharge the batteries at temperature below freezing; to prevent accidents and ensure proper battery life, modern packs are equipped with complex monitoring and protection circuitries, and modified design of the battery cells are also being proposed [19,20], claiming the virtual elimination of the likelihood of a catastrophic failure.

Table 1-1 – Nominal parameters of several battery technologies

	Lead Acid	NiMH	ZEBRA	Lithium-ion
Specific energy	20-35 Wh/kg	50-70 Wh/kg	120 Wh/kg	100-200 Wh/kg
Energy density	50-90 Wh/l	150-200 Wh/l	180 Wh/l	150-250 Wh/l
Specific power	250 W/kg	< 1000 W/kg	180 W/kg	< 2000 W/kg
Nominal cell voltage	2.1 V	1.2 V	2.58 V	3.6 V
Temperature range	-20C to 60C	-20C to 50C	N.A.	-20C to 50C
Number of cycles @80% Depth Of Discharge	700	2000	1500	2000

Basic performance indexes of the battery chemistries discussed so far are reported in Table 1-1, and their respective Ragone plots (energy versus power in logarithmic scale) are given in Fig. 1.3. It should be noted that while data for lead acid, NiMH and ZEBRA are believed to be quite accurate, Lithium batteries come in many different variations from several start-up companies that are now trying to conquer the market. Some of them are quite aggressive and have pretty bold claims in terms of energy and power density, as well as cycle life, and is therefore difficult to cite reliable, realistic figures. All figures have significant spread, as it is evident in the Ragone plot, depending on the particular technological process, and on the energy/power trade-off of a particular battery. It is possible that technological breakthrough in the very dynamic

field of lithium batteries may yield performances that significantly differ from the guideline in the table, especially regarding the operating temperature and the cycle life.

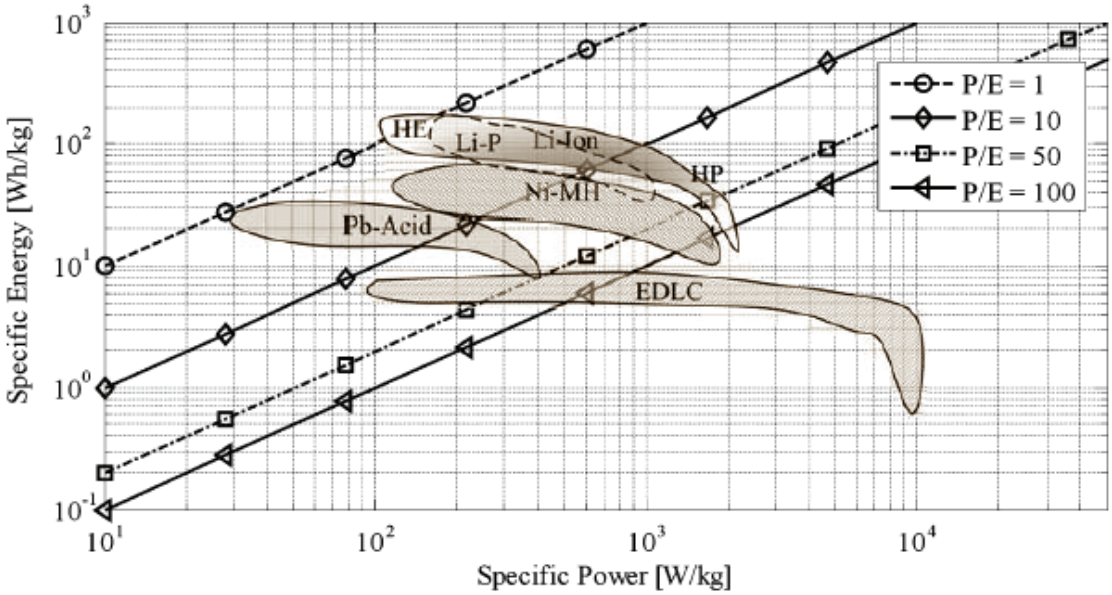


Fig. 1.3 – Ragone plot of several battery types (from [21]).

Data shows that from the point of view of achievable performance, both in terms of energy density and power density, lithium batteries are certainly superior to all other battery chemistries, and that is why virtually all automotive companies are investing in the technology. Only supercapacitors (EDLC) outperform lithium batteries for applications where very large power/energy (P/E) ratios are required.
However, Ragone plots give no information about achievable lifetime, safety issues and cost, that are at present the aspects preventing a widespread use of lithium batteries in automotive.

1.2.1 Modelling of batteries for power electronics applications

For the electrical engineer that has to design the drive system of an electric vehicle, it is important to have a model describing the behaviour of the battery at the terminals. Due to their electrical characteristics, batteries are often modelled as voltage sources with internal resistance, as shown in Fig. 1.4.

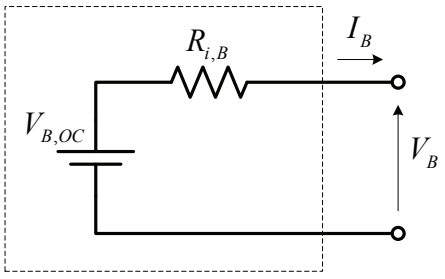


Fig. 1.4 – Basic Thevenin equivalent circuit of a battery.

Such a circuit is apparently very simple, but in order for it to describe accurately the behaviour of a real battery, both the open circuit voltage (OCV) (indicated as $V_{B,OC}$ in the figure) and the internal resistance $R_{i,B}$ must be changed according to the state of charge (SOC) of the battery. This is true for all battery technologies, even though the dependency may be very different according to the particular chemistry and technology. As an example, Fig. 1.5 shows the OCV and the internal resistance of a ZEBRA cell as a function of the SOC. The same quantities are shown in Fig. 1.6 for a lithium-ion cell.

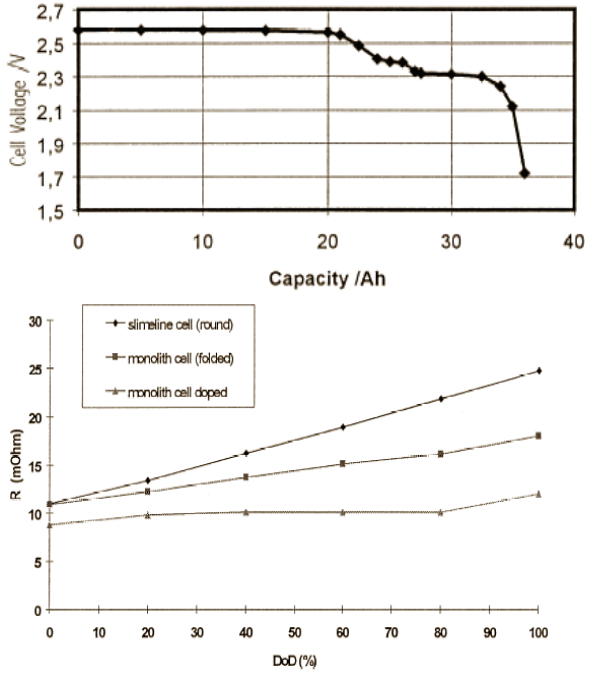


Fig. 1.5 – OCV and internal resistance (from [22]) variation of a ZEBRA cell with the SOC.

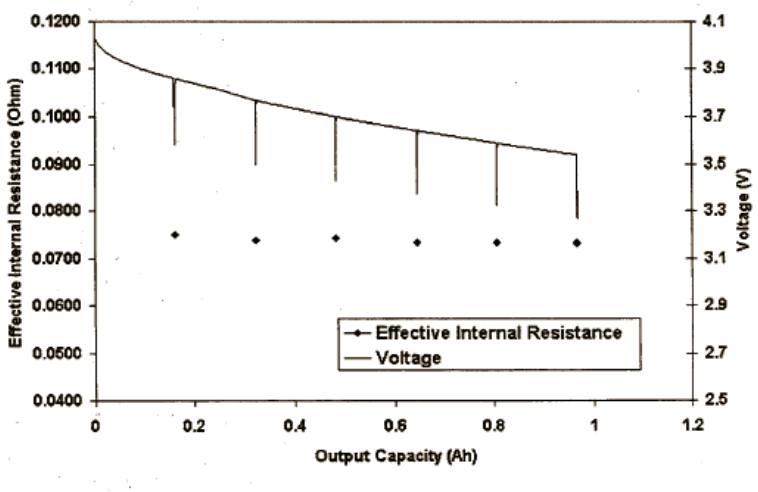


Fig. 1.6 – OCV and internal resistance variation of a lithium-ion cell with the SOC (from [23]).

OCV and internal resistance are in general dependent on temperature, too. If that is an issue, a thermal model of the battery has to be added to the electrical one. Fortunately, in the case of ZEBRA, the cell temperature is kept relatively constant by a thermal

management system embedded in the battery pack, and such complication is then unnecessary.
Since information about the battery SOC is needed to determine the electrical parameters to be used in the Thevenin-equivalent model, a means for calculating it must be included in the model. The most classical way of doing it is by using the so-called Peukert model of battery behaviour [24]. The method was developed originally to describe the behaviour of lead acid batteries, but has been extended also to other chemistries. As a starting point of this model, the constant value called "Peukert" capacity of the battery under study is defined as:

$$C_p = I^k \cdot T \quad (Ah) \tag{1.1}$$

In the definition above, I is the discharge current expressed in Ampere, T is the discharge time expressed in hours and k is an empirical coefficient (Peukert coefficient), which is a function of the particular battery technology. It is noticed that if such a coefficient is unity, then the Peukert capacity is same as the nominal capacity of the battery. Peukert coefficient is significantly higher than one in lead acid batteries (typically around 1.2), but is almost unity for ZEBRA and Li-ion. Lately, doubts have been raised about the applicability of the empirical Peukert method to modern batteries [25], but for the purpose of this thesis, the method is believed to yield sufficient accuracy.
In the elementary time interval dt (seconds), if the current flowing out from the battery terminals is I, then the incremental charge removed from the battery is:

$$dq_p = I^k \cdot dt \tag{1.2}$$

If the current is flowing into the battery (recharge), the same kind of equation is valid, but the correction due to the Peukert coefficient does not apply.
The total charge removed from the battery at time t is therefore:

$$Q_{rem}(t) = \int_{t_0}^{t} I(t)^k \, dt \tag{1.3}$$

Assuming the battery to be full at the initial time t_0, the SOC and depth of discharge (DOD) at time t are then calculated as:

$$DOD(t) = \frac{Q_{rem}(t)/3600}{C_p}; \qquad SOC(t) = 1 - DOD(t) \tag{1.4}$$

The electrical model in Fig. 1.4, can then be used together with the SOC estimator defined by (1.1) to (1.4) and the parameter adaptation taken from battery characteristics, such as those given in Fig. 1.5 or Fig. 1.6. The result is a closed-form model describing the electrical behaviour of the battery throughout the whole discharging process.
Apart from the already mentioned dependency on the cell temperature, that has not been considered, the model above is also unable to predict the dynamic behaviour of the battery, due to pseudo-capacitance effects. To that purpose, more complex electrical equivalents have been developed in the literature [26-28]**.** However, as long as the battery model is used to predict performance of a vehicle in terms of achievable range, acceleration, and so on, those refinements have little effect and are therefore not further discussed.

1.3 Supercapacitors

Supercapacitors (SC) are also known in the literature as Ultracapacitors or, more scientifically, Electrical Double Layer Capacitors (EDLC). As the latter name suggests, charge storage in these devices is based on the double layer effect, first described in [29] by Helmholtz in 1861. Although the effect has been known for many years, and several refined models have been developed since then, its application to the development of devices with extremely high capacitance is relatively new [30]. The first commercial double layer capacitor was introduced in the '80s by NEC, and only in the late '90s the technology has received worldwide attention due to the many possible applications of such devices, leading to a considerable increase in performance and decrease in price.
SCs are interesting to the automotive industry as energy storage device, since they have the following basic characteristics:

- **Very high specific power** (typically 10-100 times higher than traction batteries);
- **Perfectly reversible operation**; their efficiency during charging is same as the efficiency during discharge.
- **Long lifetime and good cycling capabilities**, meaning that they can be fully charged and discharged an extremely high number of times without significant degradation of their electrical characteristics.

In all the aforementioned aspects, SCs largely outperform electrochemical batteries. What prevents SCs from actually replacing batteries in the design of the energy tank for pure electric propulsion systems is their relatively poor specific energy, which is in the order of 10 *Wh/kg* for the best commercially available devices (about one order of magnitude lower than good traction batteries).
Even though vehicles powered only by SCs have been built [31,32], the commonest application of those devices in automotive has been as power-assist for some other kind of energy source (typically a traction battery in pure EV applications). This kind of application will be extensively described in chapter 2.
Main characteristics of SCs as energy storage devices are reported in Table 1-2. The values refer to commercially available devices, and are therefore expected to undergo significant improvements in the near future.
An in-deep description of modern SC technology, along with a comprehensive theoretical analysis of the double layer, can be found in [33]; some of the most important characteristics of those devices are reported here, since they are very useful when trying to utilize those devices in applications related to energy storage.
SCs store energy in the electric field formed by two charge distributions of opposite polarity, and are therefore characterized by their capacitance C_{SC}. The amount of stored energy is a function of the terminal voltage, and is given by:

$$E = \frac{1}{2} C_{SC} V_{SC}^{\ 2} \tag{1.5}$$

The concept behind SC is to maximize the energy storage capability by increasing the capacitance of the device. For a simple geometry of two conductive plates of surface S divided by an insulating material of width d and permittivity ε, the capacitance is expressed by:

$$C = \varepsilon \cdot \frac{S}{d} \tag{1.6}$$

In a double layer capacitor the formula above does not apply exactly, due to the more complex spatial distribution of charge and related electric field, however the qualitative dependency on surface area and distance remain unchanged, and those are the factors that are exploited by the current SC technology to obtain very high capacitance values in limited volume.
Surface area is maximized by the use of very porous materials, with carbon being currently the choice in most commercial products. Improved materials, like carbon nanotubes [34,35], are also been investigated to further increase the active electrode surface.
Maximization of surface is important, but what is really peculiar of double layer capacitor is the absence of a real insulator; the charge distribution is only due to the surface interaction between a solid material (the electrode) and a liquid solution (the electrolyte), forming a layer of charge accumulation (the double layer) over a distance of few molecules, thus giving rise to strikingly high value of capacitance. Unfortunately, that is also the reason why the operating voltage of SC is limited to few volts (less than 3 V in commercial devices). In fact, due to the very short width of the charge distribution, even a relatively low voltage causes large electric field; moreover, unlike ordinary capacitors where most of the electric field is located within the insulating material (dielectric), in SCs the electric field is directly applied to the electrolyte and electrode (see Fig. 1.7). This will ultimately cause electrolyte (and in some cases electrode) decomposition, with subsequent pressure built-up and rapid decrease of component lifetime [36].

Table 1-2 – Best-case typical parameters of commercial supercapacitors.

Specific energy	< 10 Wh/kg
Energy density	< 10 Wh/l
Specific power	10 kW/kg
Power density	10 kW/kg
Rated cell voltage	< 3.0 V
Temperature range	-40C to 70C
Number of cycles	$> 10^6$

Since, according to (1.5), increasing the operating voltage would cause a quadratic increase in energy density of the device, intensive research is ongoing to find new materials; however, the higher and higher electric field at the solid-electrolyte interface may give rise to local periodic material deformations as well as reduction-oxidation phenomena of the same nature of those normally exploited in electrochemical batteries. Although those effects add to the apparent “capacitance” of the device, they are not due to the simple charge accumulation as in ordinary capacitors, or in the pure double layer capacitor and are, for that reason, referred to as *pseudo-capacitance*. Devices that utilize actively these kinds of phenomena have been built [37], but some concerns are still present about their long-term stability, since they can be considered half-way between SCs and batteries.

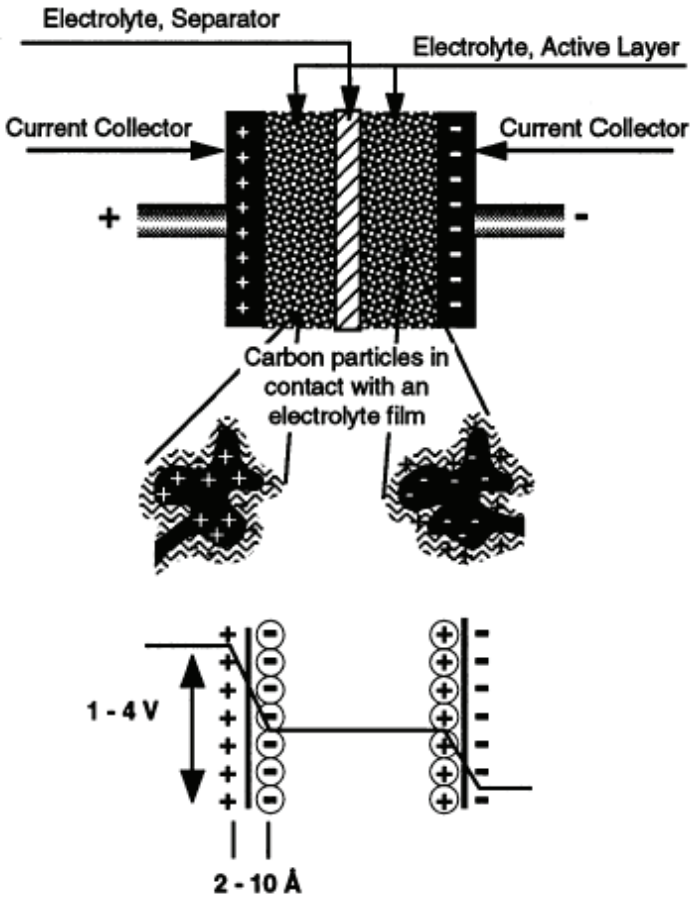


Fig. 1.7 – Structure of double layer capacitor and corresponding simplified voltage distribution (taken from [38]).

1.3.1 Modelling of supercapacitors for power electronics applications

Electrical characteristics at the terminals of an actual supercapacitor are quite different from those of an ideal capacitor. Several resistive components appear in the current path of the device schematically shown in Fig. 1.7, giving rise to an equivalent series resistance (ESR). The simplest model for the device is therefore the one in Fig. 1.8.

Fig. 1.8 – Single R-C model for an actual supercapacitor

Some leakage current inevitably flows, tending to discharge the capacitor. That would require the addition of a parallel resistance in the R-C model above, to take self-discharge into account. However, such a phenomenon is typically quite slow (time constant of several hours) and in most cases where the interest is in modelling the dynamics of the charge/discharge process (several seconds), its contribution can be neglected.

Deeper investigation on the physical structure of the device, taking into account the distributed nature of the resistance and capacitance of the porous electrode, suggests a more refined model made up of cascaded R-C pairs [38], as shown in Fig. 1.9.
Such a model can be experimentally verified by executing spectroscopic analysis of the terminal impedance, as done for instance in [39,38]. Results are schematically shown in Fig. 1.10 and can be synthesized as follows:

- At very low frequency (less than about 1 Hz), the impedance is reasonably well described by a simple R-C series network with constant values of both capacitance (the DC-capacitance) and resistance (the DC-ESR).
- At relatively high frequency (above about 100 Hz), the capacitance is reduced to a very small fraction of its DC value, and the component behaviour is essentially resistive, with a "high frequency" ESR that is smaller than the DC-ESR.
- At intermediate frequency, both ESR and equivalent capacitance increase with decreasing frequency, giving rise to the distinctive 45 degree-slope region in the complex impedance plane.

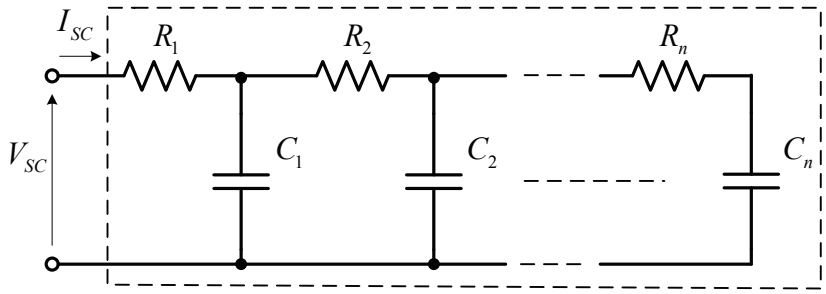


Fig. 1.9 – Cascaded R-C model for an actual supercapacitor

Adding to the complexity of the system in Fig. 1.9 is the fact that R-C parameters are in general dependent on both temperature and operating voltage [40,41].
For the power electronics designer, the impedance characteristic in Fig. 1.10 has the important implication that in spite of the huge value of their DC-capacitance, SCs are of no help in filtering high frequency components typical of PWM converters, as they are almost purely resistive at those frequencies. In order to avoid excessive power dissipation within the SC cells and the consequent increase of temperature, it is good practice to connect a filtering capacitor with good high frequency characteristics in parallel with the SC bank [42,43]. The importance of this simple and relatively inexpensive countermeasure should not be overlooked, since it can significantly increase the lifetime of the SC bank in many applications.
This practical aspect also makes it possible to use the simplified R-C model of Fig. 1.8 with DC-values of both ESR and equivalent capacitance to describe the behaviour of a SC in an actual circuit. In fact, if a large, low ESR, bypass capacitor is placed in parallel with the SCs, high frequency components will be almost completely shunted away from the supercaopacitor, and the high frequency branch of the impedance characteristic can be neglected without significant loss of information.

However, if filtering capacitor is not present (or is not sufficient) and high frequency ripple current does flow through the SCs, the high-frequency ESR of the devices has to be used to evaluate the losses due to such high frequency components.

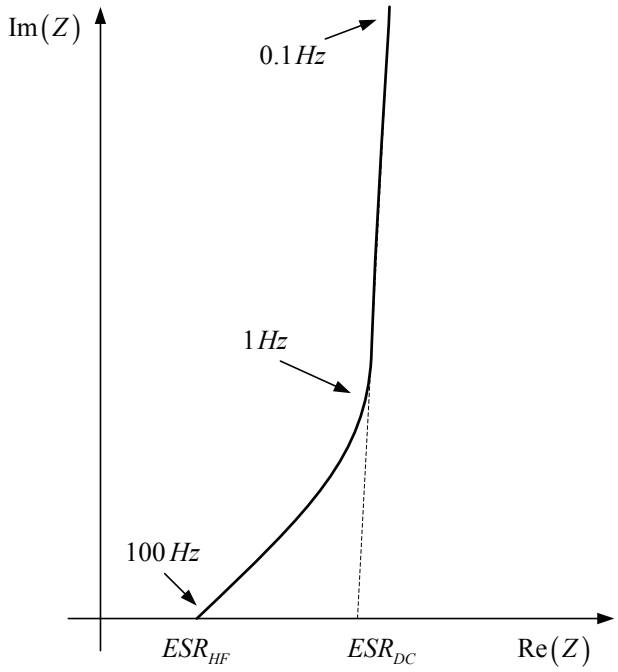


Fig. 1.10 – Schematic representation of Nyquist impedance plot of a typical SC cell.

2 HYBRID ENERGY SOURCES – COMBINATION OF BATTERIES WITH SUPERCAPACITORS

2.1 Hybrid energy sources

Generally speaking, any kind of arrangement that allows for use of energy from more than one source can be defined as hybrid. Considering the variety of fossil fuels, battery types, alternative fuels and so on, the number of possible combinations is overwhelming. Main factors behind the need for hybridization of the energy source in automotive are:

- Improved performance;
- Improved economy;
- Improved vehicle lifetime;
- Flexibility.

Except for the latter aspect, where for example a given IC engine is designed to run from different kind of fossil fuels or biofuels [44] just for the sake of increased availability, the basic idea behind hybridization is to utilize in a synergic way different sources of energy, with the aim to combine their individual advantages and, at the same time, mitigate their weak points.

A typical example is the combination of fossil fuel (used to supply an IC engine) with some kind of electrochemical energy storage (typically a battery driving an electric motor) used in the increasingly popular hybrid vehicles (HEV) of which the Japanese carmaker Toyota with its Prius has been the forerunner. In this arrangement, the superb energy density of the fossil fuel is combined with the ability to recuperate the kinetic energy of the vehicle into the battery for later use; also, vehicle efficiency can be improved by properly splitting the effort of the engine and the electric motor according to operating conditions. Overall, the hybridization results in a vehicle having better fuel economy and higher performance than the equivalent “IC only” counterpart.

Although HEVs are by now an industrial reality experiencing an exponential growth, they will not be further discusses in this context. The focus will instead be on pure

electric vehicles (no IC engine at all), where hybridization consists in the use of more than one type of electrical energy storage. Fuel cell vehicles (FCV) and the related problems of hydrogen production and storage, although recognized as being an extremely interesting technology, are also beyond the scope of this thesis. However, it is pointed out that most of the concepts related to hybridization discussed in the following will readily apply to FCV, since in virtually every implementation the slow dynamics of the fuel cell require the use of some kind of additional power source, like a battery or a supercapacitor bank.

A typical drive system with hybridized electrical energy source is shown in Fig. 2.1. At this stage, the power flow controllers are assumed to be ideal, meaning that the power that flows from the *i*-th energy source $P_{SRC,i}$ is exactly equal to the one commanded by the power sharing algorithm $P_{SRC,i,ref}$. It is hereby noticed that if there is no energy storage within the power flow controllers, energy conservation requires that:

$$P_{Load} = P_{SRC,1} + P_{SRC,2} + \ldots + P_{SRC,n} \tag{2.1}$$

Therefore, only $(n-1)$ power flow controllers are strictly needed.

In general, the hybrid energy system can consist of any number of sources, although in most practical implementation *n* is limited to two. In this simple but significant case, the system can be implemented according to any of the topologies in Fig. 2.2. The redundant structure has the advantage of complete decoupling between the electrical characteristics (terminal voltage and current) of each source and those of the load, but needs more power processing components and its overall efficiency and cost may be negatively affected. On the other hand, in the case of the minimal structure, the load must share some of the electrical characteristics of the unprocessed source (either its terminal voltage or current, depending on the kind of connection). The choice of the topology depends on the particular application, taking into account the characteristics of each source as well as those of the load.

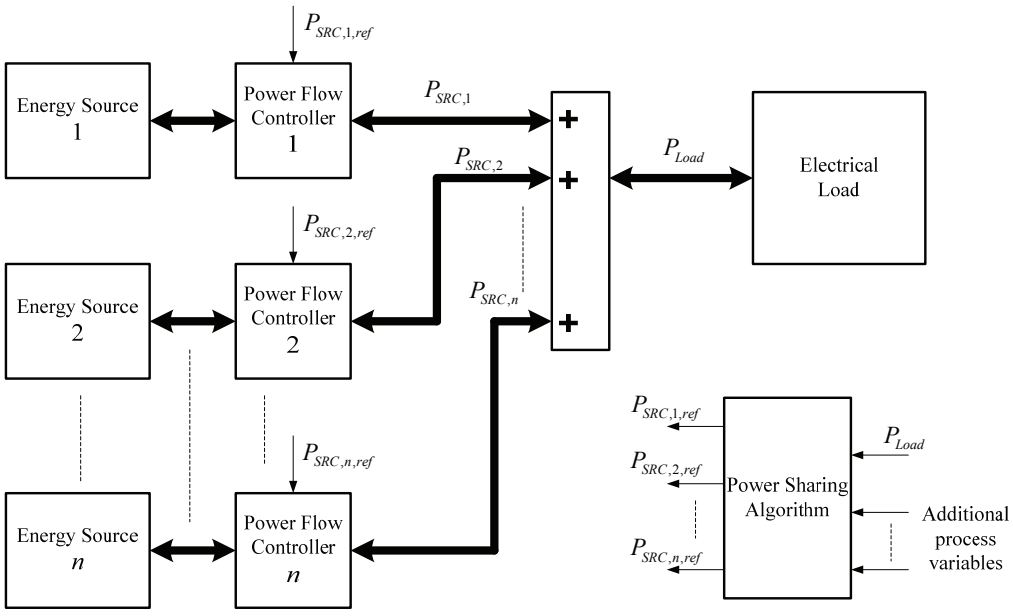
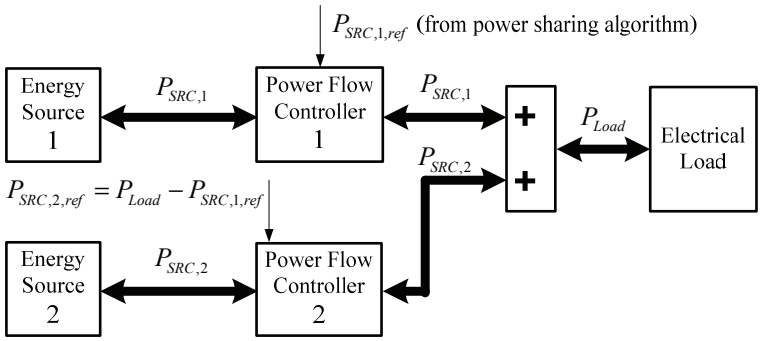
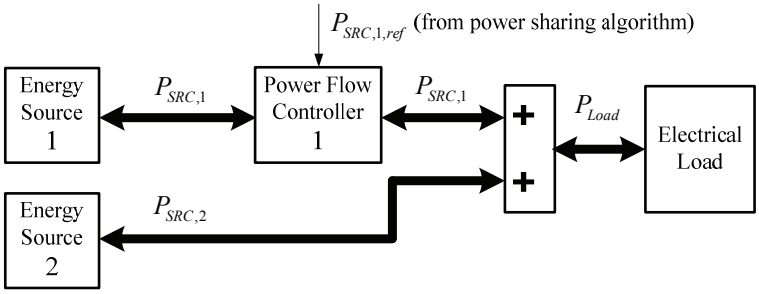


Fig. 2.1 – Hybridized electrical energy source.



a. – Redundant structure



b. – Minimum structure

Fig. 2.2 – System with two energy sources – Architectures for independent power flow control.

2.2 Battery-Supercapacitor combination

In a pure EV, the ideal energy tank should satisfy the following basic operational requirements:

- Sufficient amount of energy storage capability, in order to achieve a satisfactory driving range between recharges;
- Sufficient power capabilities, so that the necessary power required for propulsion can be supplied to the motor in any reasonable driving condition;
- Quick charging time, in order to increase vehicle availability;
- Sufficient lifetime, both in terms of calendar life and number of charge/discharge cycles.

In addition, there are a number of other requirements which are not directly related to the performance of the EV, but still are of utmost importance:

- Safety, both during normal operation and in case of accidents;
- Cost.

Having in mind the results of the review in chapter 1, it is apparent that at present the only kind of electrical energy storage device that can give sufficient energy density to achieve a reasonable driving range is the electrochemical battery. In particular, according to Table 1-1, Lithium batteries and Sodium-Chloride batteries have the best specific energy figures among all the rechargeable batteries to-date.

When considering power density, results are very different. Sodium-Chloride batteries have poor power density; Lithium batteries still score fairly well, but they are largely outperformed by supercapacitors.
In light of those very simple considerations, it seems that a combination of an energy dense battery pack with a power dense supercapacitor bank can combine the advantages of both technologies. Of course, the hybrid system is more complex, and possibly has higher initial cost than a classical battery-only design.
There is intensive research activity on Li-based batteries trying to increase their specific power, and some of them [45] are showing promising results; however, it should not be overlooked that there is always a design trade-off according to which, for a given technology, trying to increase the power density will always result in reduced energy density. The use of hybridization would allow for independent optimization of the two concurrent sources for highest specific energy and highest specific power, respectively.
Whether a hybrid energy source is really advantageous and, if yes, to what extent, is still very controversial, due to the many variables involved in the evaluation of those systems. In the following, some of the aspects related to the design of hybrid battery-supercapacitor systems are analyzed, trying to give answer to such a basic question.

2.2.1 Power flow control within systems with hybrid energy source

The power sharing algorithm used by the controller in Fig. 2.1 must be designed with the aim of getting the best out of each individual source. A proper strategy should be able to achieve one or more of the following objectives:

- Maximized driving range (can also be stated as maximized overall efficiency);
- Minimum component stress, resulting in extended system life-time.

Stated in simple terms, the operating principle of hybrid energy source is expressed by the following paradigms:

- The primary energy source (the battery) is the one with the highest energy content and should therefore supply the average power needed by the load; Steady power flow ensures minimum losses and reduced stress. Since the battery cycle-life is currently the most critical factor for the system overall life-time, the latter aspect is particularly important.
- The secondary energy source (the supercapacitor) should assist the battery by providing/absorbing the momentary load power peaks. Due to relatively low internal resistance, they can efficiently handle large power bursts; moreover, their life-time will not be significantly affected by this intermittent operation, provided their thermal limits are not exceeded.

Although apparently straightforward, those principles are not easy to implement in practice. In fact, the load requirement is not known a-priori, making the concept of ideal power sharing a non-deterministic one. In addition, optimal power sharing will depend on the state of the individual energy sources (SOC, internal resistance, etc.), introducing several additional variables and constraints to the optimization problem. Moreover, while efficiency and achievable driving range are relatively easy to measure, effects on system life-time are not as apparent.

To date, there is no standard solution to the problem of optimal power sharing described above. There is however plenty of publications on the subject, mainly divided in three categories according to the kind of algorithm used:

- Heuristic algorithms, based on simple practical assumptions reflecting the basic principles reported above [46-48]. Main advantage of those algorithms is that they do not need a-priori information about the particular driving pattern; only some general specifications of the system components are needed, making the strategy easy to implement.
- Deterministic algorithms based on analytical minimization of losses [49-52]. Typically, information about the driving pattern is needed for proper optimization, along with detailed information about the system structure and electrical specifications of each component. The optimization process is complicated by the physical constraints (limited energy available in the SC-buffer, maximum current in and out of the battery, etc.) present in the system.
- Non-deterministic algorithms, utilizing stochastic methods, fuzzy logic and/or neural networks trying to achieve a real time solution of the optimization problem [53-56]. These methods are very popular for solving complex optimization problems that are not easy to express in closed mathematical form; performance can be very dependent on the particular implementation and training and, in any case, optimality cannot be guaranteed for every particular driving pattern.

Although the design of an efficient power sharing algorithm is of great importance, it is not the aim of this thesis to discuss extensively on the subject.
In order to illustrate the operating principle and highlights the main advantages and drawbacks of a hybrid system, an algorithm belonging to the first category above is developed. Such a power sharing algorithm is shown in Fig. 2.3 and its operating principle is explained in the following. The algorithm evaluates the share of the load power that must be handled by the SC-based power buffer $P_{SC,ref}$, using as input for the calculation the vehicle speed v, the SOC of the traction battery and the power required by the load P_{Load}.

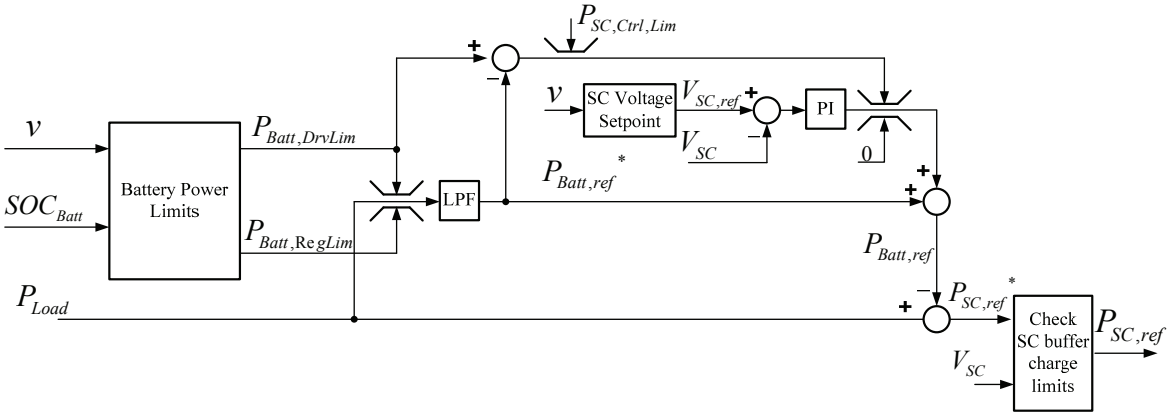


Fig. 2.3 – Heuristic power sharing algorithm between a battery and a supercapacitor bank.

In the simple case of only two energy sources, (2.1) is written as:

$$P_{Load} = P_{SC} + P_{Batt} \tag{2.2}$$

The load power requirements consist of the following components [57]:

1. Base load (on-board electrical loads, including air conditioning), P_{base};
2. Rolling resistance P_{roll};
3. Aerodynamic drag, P_{drag};
4. Gravitational load during uphill/downhill driving, P_g;
5. Inertial load during acceleration/braking, P_{acc}.

The first 4 components are "steady components", meaning that they can remain nearly constant for long time. Due to this characteristic, they should be supplied by the primary energy source, in order not to deplete the power buffer (secondary source). On the other hand, power for acceleration and braking, due to its quick transient nature, should come from (or be sunk by) the power buffer. With this strategy in mind, the first step is to estimate the "steady loads":

$$P_{Load,steady} = P_{base} + P_{roll} + P_{drag} + P_g = P_{base} + k_{roll} \cdot |v| \cdot Mg\cos\psi + k_{drag} \cdot |v|^3 + Mg\sin\psi \tag{2.3}$$

In the equation above, *M, v* are the total vehicle mass and speed, respectively; ψ is the inclination of the road surface. The coefficients k_{roll}, k_{drag} are known from vehicle geometry and weight, and can be considered constant for the degree of accuracy that is here required.

Total steady power in (2.3) can be either positive (load requires power) or negative (load is giving power back to the sources), with the latter being possible only in the case of downhill driving. In principle, the amount of power defined by (2.3) is the one that should be supplied by the battery; however, it is first necessary to check for absolute power limitations given by the battery manufacturer that are normally a function of the SOC. It is noticed that if the system is properly designed, the battery should always be able to supply positive load requirements; however, in the case of regeneration, it is possible that especially at high SOC, the energy sent back by the load exceeds the battery's capability, and the negative value given by (2.3) has to be clamped.

The setpoint for the battery power is finally determined by multiplying the value obtained above by a coefficient k_{mar} slightly bigger than unity, in order to leave some margin for SOC control of the SC bank (as will be described later) and for unavoidable parameter mismatch in the evaluation of (2.3); the reference is also smoothed by a simple first order low pass filter, to avoid fast gradients that may have adverse effect on battery lifetime:

$$P_{Batt,ref}^{\ *} = \frac{k_{mar}}{1+\tau s} \cdot P_{Load,steady} \tag{2.4}$$

As a consequence, the SC bank will have to supply the rest, in order to satisfy (2.2). This can be done, unless the buffer has reached its SOC limits.

The problem with this algorithm is that it does not take into any account the limitation of the energy content in the SC-based power buffer. It is then possible that during operation, due to unavoidable parameter mismatch, the SC buffer becomes either

completely depleted or completely filled. When that happens, its contribution to the load power requirement disappears, leaving the battery as the only available source.
Ideally, the SC buffer should be operated so that in any given instant, it is able to accept energy from the load if sudden braking occurs or, conversely, it is able to supply acceleration power to the load as required by the driver. That means the SOC of the buffer should be controlled as a function of the speed, following the simple argument that if the vehicle is running at low speed, the power buffer should be kept close to full, in order to be prepared for sudden acceleration. Conversely, if the vehicle is running at high speed, the power buffer should be close to empty, so that it can readily accept the braking power that may be sent back from the load.
Braking energy that can be expected from the load at any given instant is at most equal to the kinetic energy of the vehicle, and is therefore varying with the square of the speed:

$$E_{\mathrm{Re}g,Max} = \frac{1}{2} M \cdot v^2 \tag{2.5}$$

On the other hand, the energy that can be accepted by the SC-based power buffer for a given SOC is expressed as:

$$\Delta E_{SC} = \frac{1}{2} C_{SC} \cdot \left({V_{SC,Max}}^2 - {V_{SC}}^2 \right) \tag{2.6}$$

If the buffer has to be able to accept all the possible energy that could be sent back from the load, its terminal voltage should then be controlled to:

$$V_{SC}(v) \le \sqrt{{V_{SC,Max}}^2 - \frac{M}{C_{SC}} v^2} \tag{2.7}$$

It is beneficial to apply (2.7) with the sign of equality so that, at the same time, the amount of energy already present in the power buffer is maximized. Such energy can be used for acceleration.
Once the desired SC voltage has been calculated by (2.7), a standard P-I controller can be used to force the actual SC voltage to track its reference. Obviously, the energy necessary for such a tracking process must come from the battery and it is therefore necessary to decide how much effort should be put into this process. This is done by properly shaping the upper and lower limits of the P-I controller generating the additional term of the battery power needed for SC voltage tracking, as shown in Fig. 2.3. The idea is to operate the voltage tracking as a low priority process, using as little battery energy as possible. In addition, the lower output limit of the voltage regulator is set to zero, meaning that no energy can be sent back directly from the SC bank to the battery; this is done in order to avoid unnecessary power loops within the system and their associated losses.

2.2.2 Simulation of a battery-supercapacitor hybrid energy source

In order to highlight the advantages of a battery-supercapacitor energy source against a battery-only system, Matlab-Simulink® [13] simulations are performed, representing a particular case study of a small, pure electric, city vehicle. The overall model of the system is reported in Fig. 2.4.

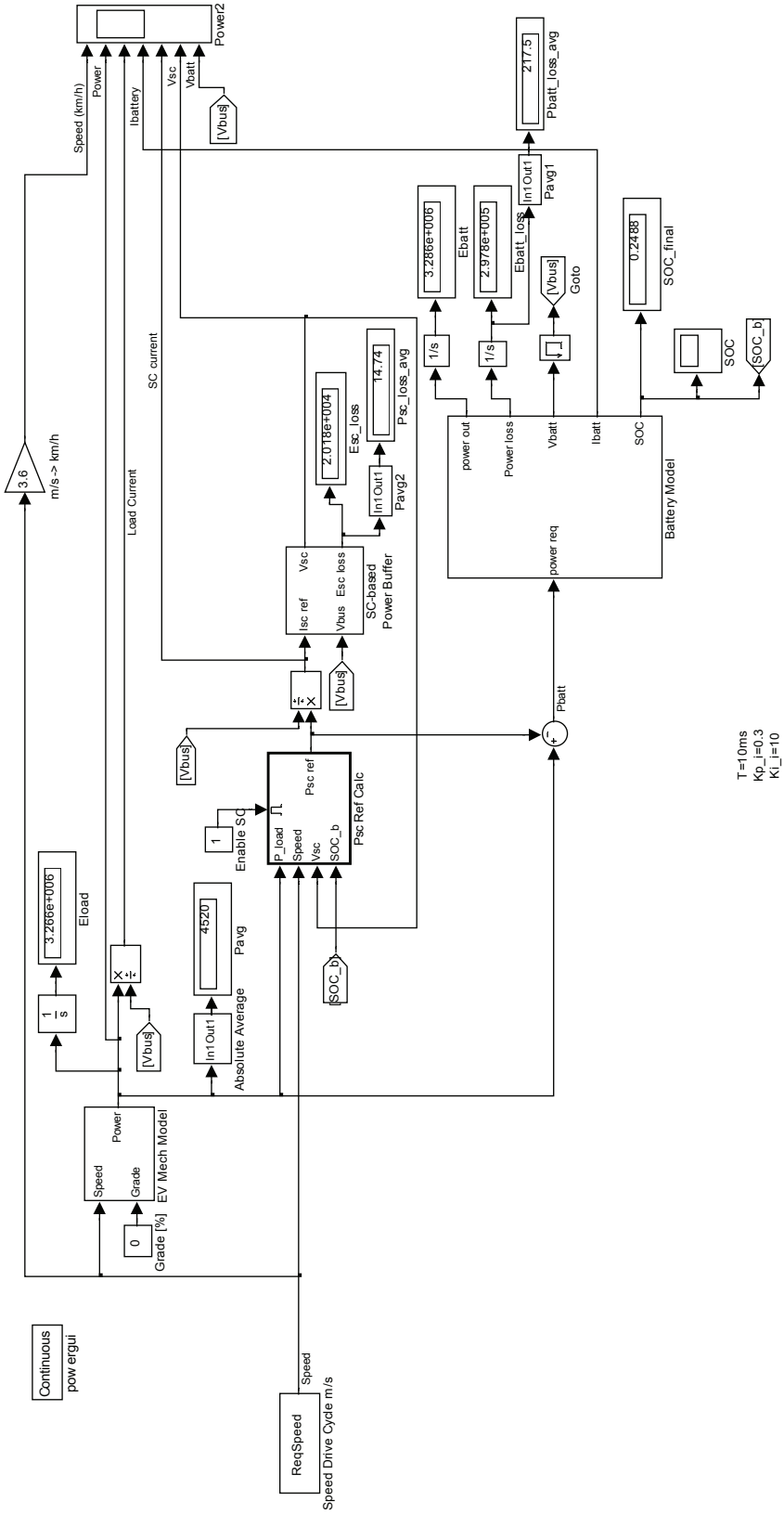


Fig. 2.4 – Simulation model of a battery-supercapacitor .hybrid system.

Main modelling assumptions are as follows:

- Electric power required by the vehicle is calculated by imposing a given speed profile, taking into account a simplified vehicle dynamics, including rolling resistance, aerodynamic drag, grading and electric base load. When the SC-based power buffer is used, its weight is added to the vehicle mass;
- Electric drive train (electric motor, inverter, transmission system) is assumed to have an overall efficiency of 80%, constant over the whole operating range;
- Battery is modelled with a Thevenin equivalent circuit (see section 1.2.1) with both open circuit voltage and internal resistance variable according to the SOC. No capacity variation with the level of output power is considered;
- Supercapacitors are modelled with a simple R-C network. Their losses are evaluated assuming an ideal Half-Bridge interface (see section 1.3.1). Both capacitance and internal resistance are assumed constant; the power control is assumed to be ideal, meaning that the SC buffer will deliver (or absorb) the amount of power calculated by the power sharing algorithm.
- Power sharing algorithm is the one described in the previous section.

Simulation parameters are given in Table 1-2; they are derived from basic mechanical and electrical specifications of the Norwegian Th!nk City EV [14] equipped with a ZEBRA battery [9]. Supercapacitor electrical specifications are those of the bank based on Maxwell's MC-type cells [58] designed in Chapter 5.

Table 2-1 – Parameters of the simulated hybrid electric energy source system for city EV.

Vehicle	Mass	$M_{EV} = 920\,kg$
	Rolling constant	$k_{rr} = 0.11W/\left(kg \cdot m^2/s^3\right)$
	Dragging constant	$k_{drag} = 0.75W/\left(m^3/s^3\right)$
Battery	Open Circuit Voltage	$OCV = \begin{cases} 278V\ @100\%\,SOC \\ 254V\ @20\%\,SOC \end{cases}$
	Internal resistance	$R_{Batt} = \begin{cases} 486\,m\Omega\ @100\%\,SOC \\ 702\,m\Omega\ @20\%\,SOC \end{cases}$
	Mass	$M_{Batt} = 180\,kg$
Supercapacitor bank	Capacitance	$C_{SC} = 23.9\,F$
	Internal resistance	$R_{SC} = 38\,m\Omega$
	Voltage limits	$V_{SC,Max} = 240V$ $V_{SC,Min} = 120V$
	Mass	$M_{SC} = 50\,kg$
Control parameters	SC voltage regulator	$k_P = 0.3;\quad k_I = 0.1$
	Smoothing filter for $P_{b,ref}$	1st order LPF, $\tau = 2\,s$

Table 2-2 – Main characteristics of the two standard drive cycles used in simulation.

Cycle name	Duration (s)	Distance (km)	Avg. speed (km/h)	Max speed (km/h)	% of time @ zero speed	Max. accel.	Max braking
ECE-EUDC	1224	10.6	31.1	90.0	26.6	0.15*g*	-0.15*g*
FUDS	1369	12.0	31.5	91.2	17.7	0.11*g*	-0.14*g*

Two different standard drive cycles are used to illustrate the behaviour of the hybrid energy source system (see Table 2-2):

- European standard ECE-EUDC combined drive cycle;
- American standard FUDS urban drive cycle.

The former is a rather simple pattern consisting of periods of constant acceleration and periods of constant velocity. It is presented here, since it is the standard with which all the European car manufacturer (including Th!nk EV) have to refer when stating their vehicle's performance in terms of achievable range and emissions; however, due to the smoothness of the speed profile, such a pattern is not closely resembling actual city driving and is obviously not very well suited to highlight the advantages of the hybrid energy source, that aims at lowering the battery losses by peak-power shaving.
On the other hand, the FUDS cycle is derived from actual urban driving data, and exhibits continuously variable speed over the whole cycle, making the effect of the hybrid energy source much more evident.
Simulation results of a single cycle with and without the SC-based power buffer are shown in Fig. 2.5 to Fig. 2.10, and some of the most significant figures of merit are reported in Table 2-3.

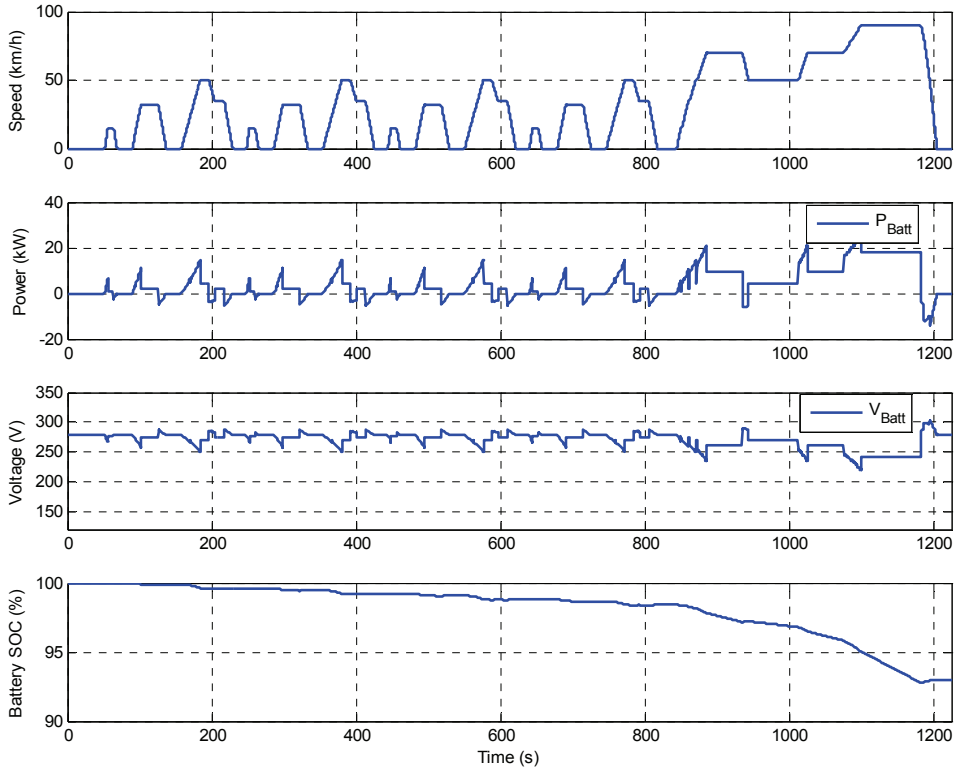


Fig. 2.5 – Simulation of a complete ECE-EUDC cycle, battery only, initial SOC = 100%.

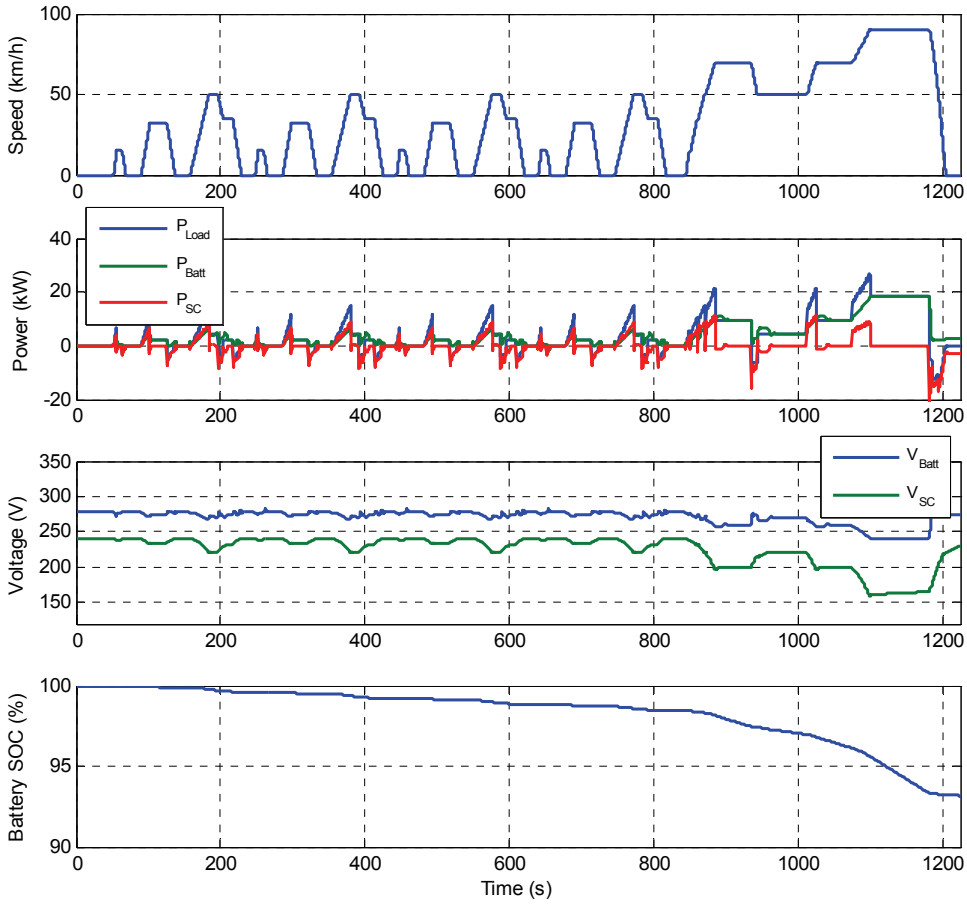


Fig. 2.6 – Simulation of a complete ECE-EUDC cycle, battery plus SCs, initial SOC = 100%.

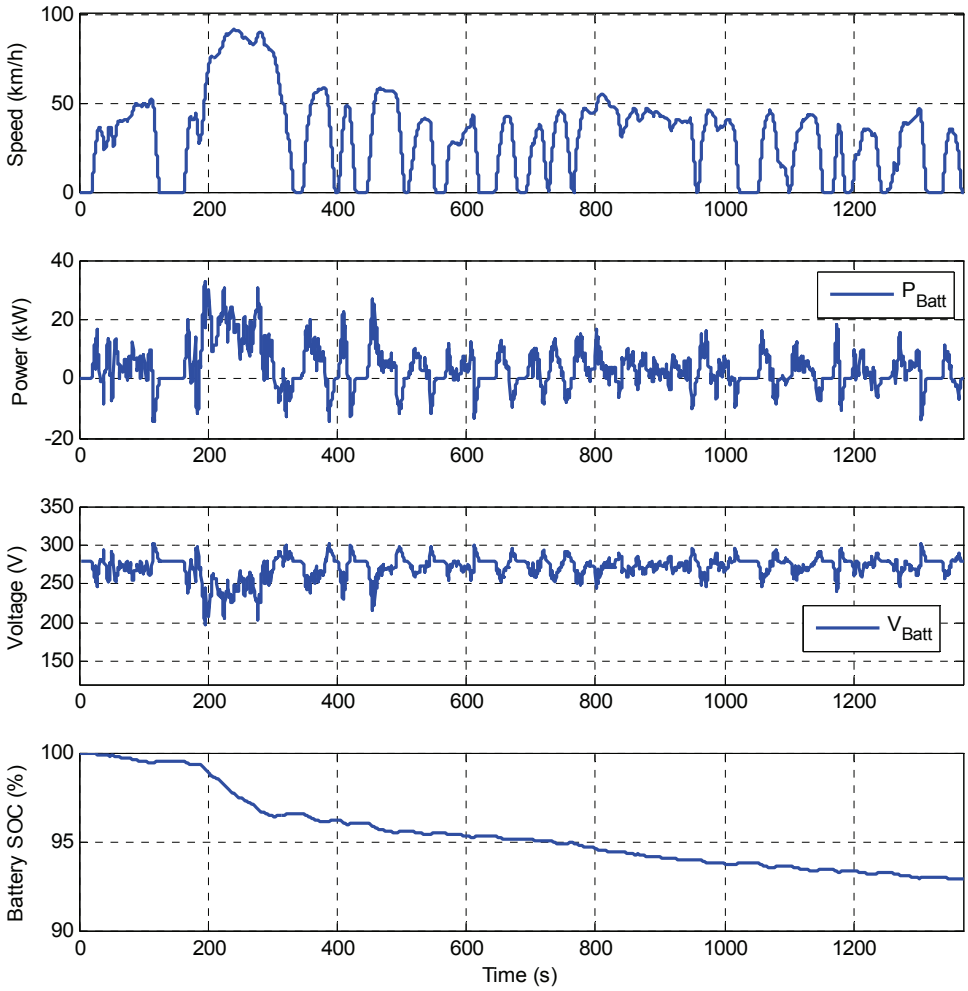


Fig. 2.7 – Simulation of a complete FUDS cycle, battery only, initial SOC = 100%.

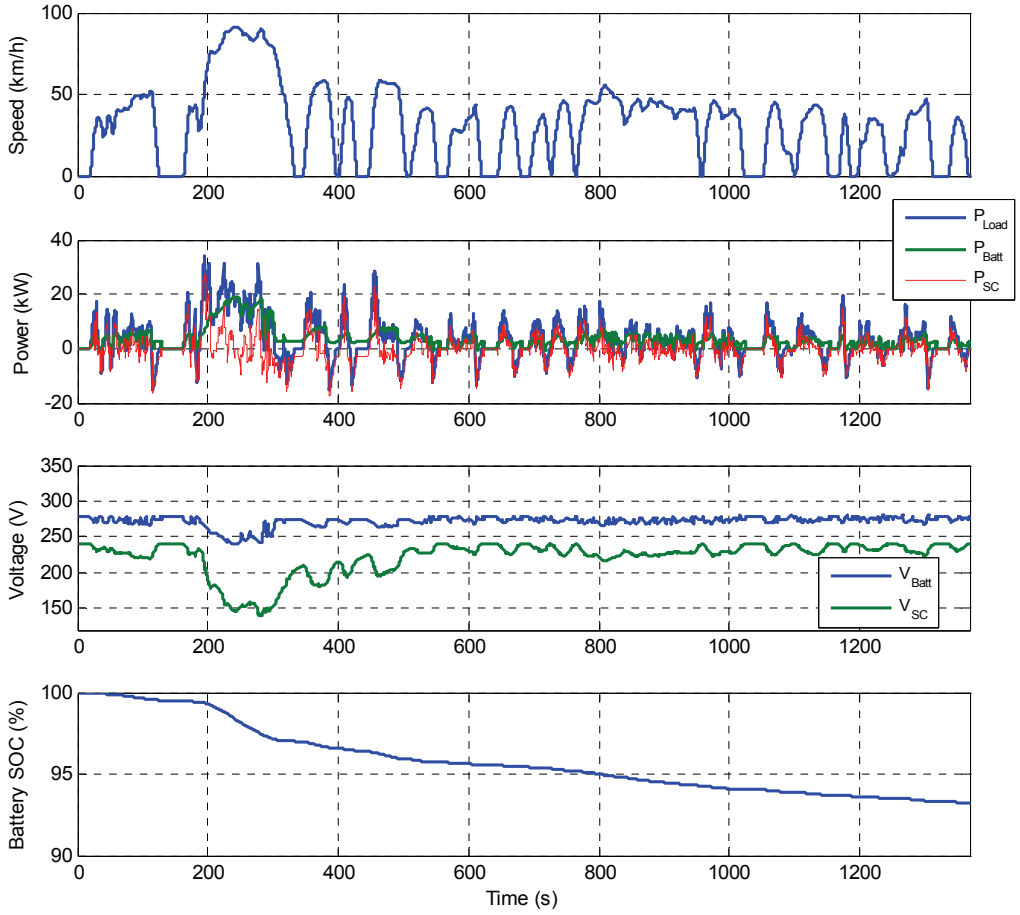


Fig. 2.8 – Simulation of a complete FUDS cycle, battery plus SCs, initial SOC = 100%.

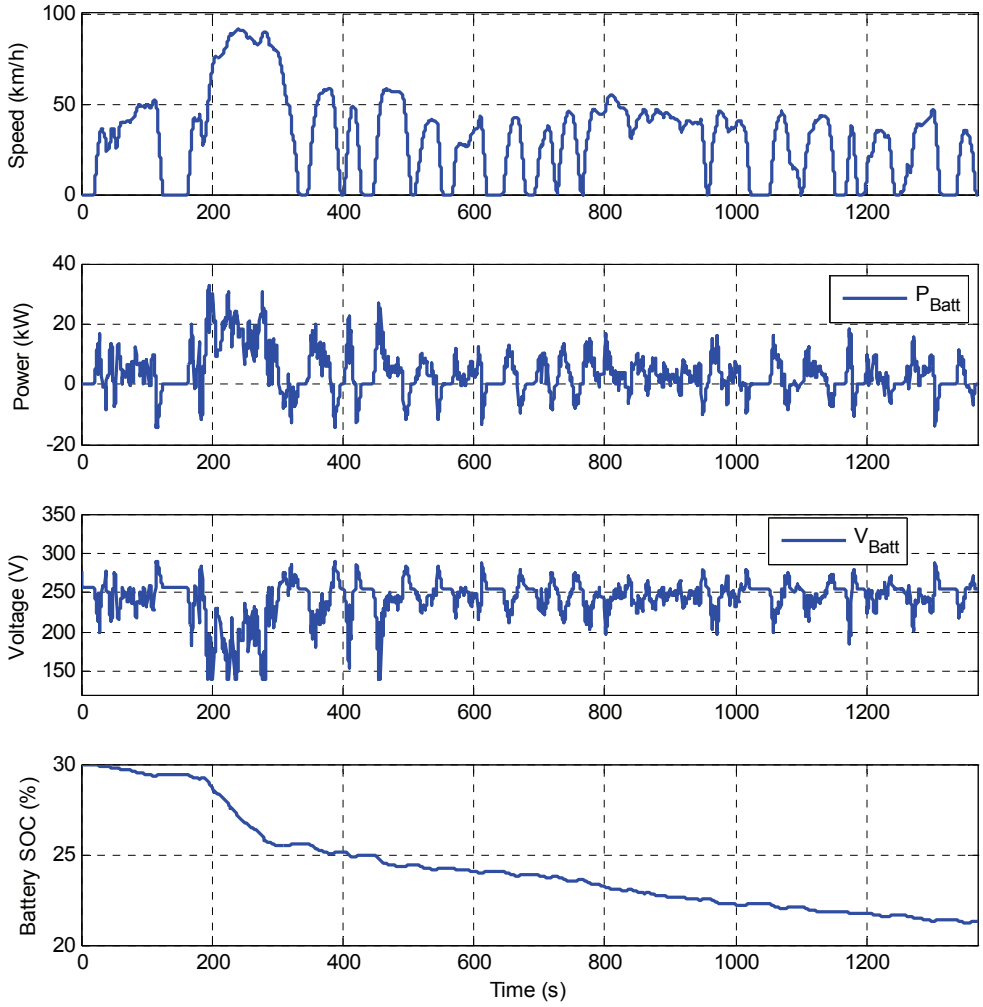


Fig. 2.9 – Simulation of a complete FUDS cycle, battery only, initial SOC = 30%.

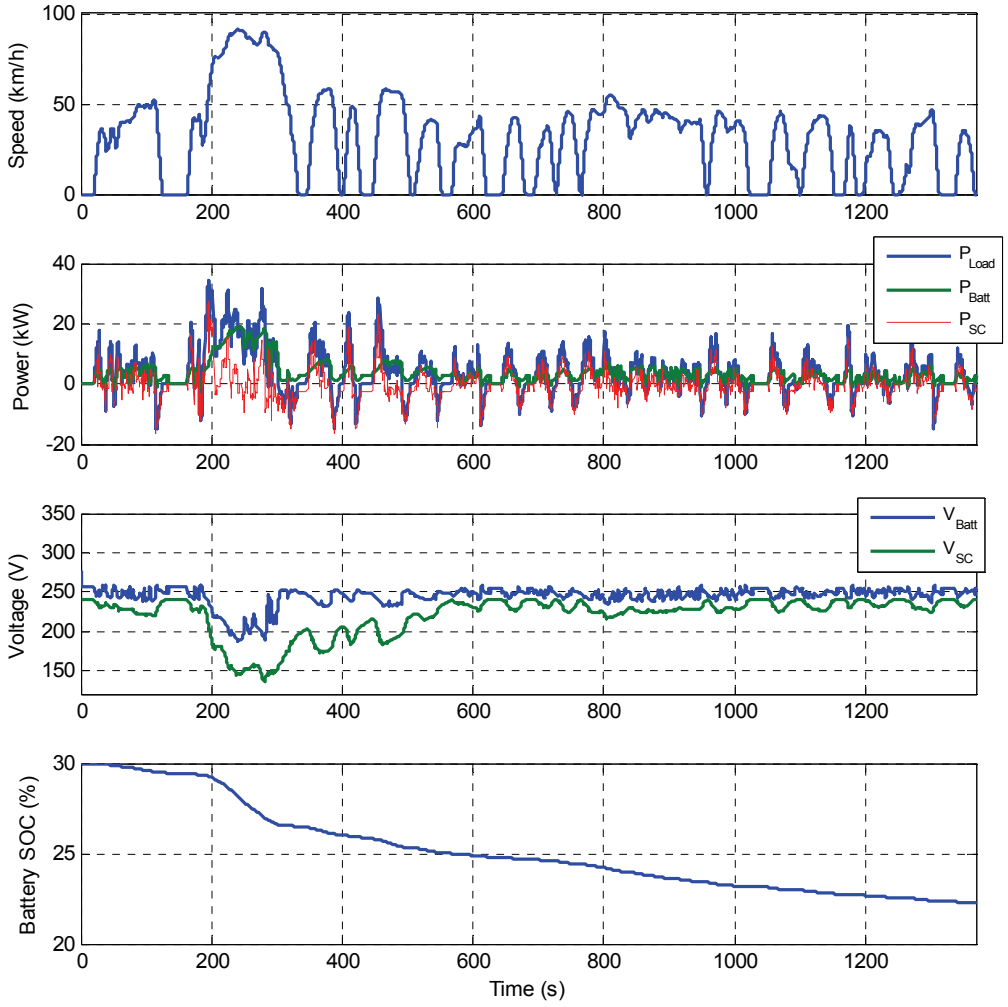


Fig. 2.10 – Simulation of a complete FUDS cycle, battery plus SCs, initial SOC = 30%.

Table 2-3 – Simulation results.

Simulated conditions	Average power Loss in Energy Source (W)		Used battery energy (pu)		Projected range extension due to hybridization	Loss reduction in the battery due to hybridization
	Hybrid Source	Battery only	Hybrid Source	Battery only		
ECE-EUDC, SOC(0)=100%	Batt: 334 SC: 9.8	463	0.068	0.070	2.9%	27.9%
ECE-EUDC, SOC(0)=30%	Batt: 707 SC: 9.4	1019	0.081	0.086	5.8%	30.6%
FUDS, SOC(0)=100%	Batt: 203 SC: 22.0	473	0.068	0.071	4.2%	57.1%
FUDS, SOC(0)=30%	Batt: 398 SC: 21.7	1031	0.078	0.087	10.3%	61.4%

Before proceeding to the interpretation of simulation data, it has to be acknowledged that results can vary if a different power sharing algorithm is deployed, but the essence will remain the same. On the other hand, the picture may vary if different kind of vehicles (buses, trucks, large SUVs) and/or different kind of driving cycles (highway driving with sustained constant, high speed operation) are considered; here, the analysis is limited to relatively small-sized pure EV used mostly for urban driving.
In this context, it can be said that the addition of the SC-based power buffer has the effect of increasing the overall efficiency. Effect is much more pronounced in the FUDS cycle, where the load power is continuously varying and acceleration/deceleration phases are more demanding. Moreover, the presence of the power buffer is shown to be particularly beneficial at low battery SOC, where losses increase due to the combined effect of lower OCV and higher internal resistance of the battery.

2.2.3 Effect of battery-supercapacitor hybridization on key performances of a pure electric city vehicle

In this section, the previously presented results are critically analyzed, trying to draw some conclusions about the actual impact of the use of an expensive SC-based power buffer on some key performance indexes of the EV.

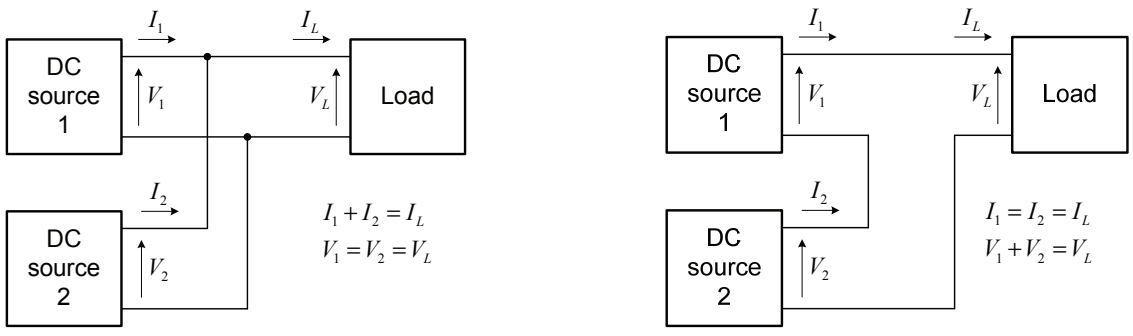
- **Extension of driving range** – Driving range is recognized as a serious limitation of pure EV; as a consequence, range extension is one of the most claimed advantages of a hybrid energy source. According to the simulations, the improved efficiency resulting from the use of the power buffer yields a range extension in the order of 5% for realistic city driving. Admittedly, this figure can be slightly improved by the use of more sophisticated power sharing algorithms; however, the numbers in Table 2-3 show that even if we were able to eliminate completely the losses in the energy source (that is the limit case of a perfect power buffer), the improvement in driving range would be below 20%. This improvement is not likely to be a sufficient motivation for the deployment of such an expensive solution; it is in fact reasonable to argue that utilizing the extra money, volume and weight necessary for the power buffer to install a slightly bigger battery would lead to a better gain in driving range. In this specific case, according to data in Table 2-3, if the battery is enhanced with a mass equal to that of the SC buffer, and assuming unchanged energy density, the available energy would be increased by about 27%, which is certainly much beyond any reasonable figure for the range extension achievable by using an SC-buffer.
- **Improved vehicle performance** – The use of the power buffer has the potential to make the acceleration performance of the EV virtually independent of the battery SOC; on the other hand, a battery-only vehicle may experience some loss of power capabilities towards the very end of the battery discharge. In principle, the use of SCs in combination with oversized power electronics converters can substantially improve the short-term acceleration performance and the regenerative braking capabilities of the EV. However, steady state performance like maximum speed, or maximum sustained gradeability cannot be improved. It is hereby noticed that the power limitation of the battery is not likely to be a major problem in pure EV, due to the fact that a relatively large (and therefore

quite powerful) battery is anyway needed in order to ensure reasonable driving range and maximum speed. For instance, in the Think EV, the battery is specified to be able to supply the peak power of the motor all the way down to 10% SOC, even though the simulation in Fig. 2.9 shows that the voltage of a depleted battery may decrease to unacceptable levels during hard acceleration (excessively low battery voltage may limit the achievable speed; this aspect is not modelled in the simulation). The picture can be quite different in the case of ICE-electric hybrids, where battery size is considerably smaller; however, this kind on vehicles is not discussed here.

– **Improved system lifetime** – The most remarkable effect of the SC-buffer is the drastic reduction of the losses in the battery. For the realistic FUDS cycle, such a reduction ranges from a minimum of 57.1% (battery initially full) to a maximum of 61.4% (battery towards the end of discharge). Arguably, augmenting the battery mass by the amount corresponding to the weight of the SC buffer would decrease the losses, for the same power requirements. However, such a reduction is much less than what is achieved by the deployment of the supercapacitors. Reducing the stress on the battery can have significant effect on the lifetime of this component, which happens to be the most critical element of a pure electric EV, and arguably the one that most of all has hindered the commercialization of electric cars. It is very difficult to establish a precise relationship between the average losses in the battery and its lifetime, and more data should be gathered on the matter; however, if the natural correlation between the two aspects is confirmed, the resulting extension of the battery life could be a very convincing argument for the use of a SC-based power buffer in pure electric vehicles.

2.3 Power electronics solutions for controllable power flow in battery-supercapacitors hybrid energy sources

The power flow within the hybrid energy system is controlled by means of dedicated circuits, indicated as *power flow controllers* in Fig. 2.2. They can be very different according to the type of sources and load they have to interface; in our analysis the two sources are one battery and one supercapacitor bank. The ultimate load is an electric motor, but what the sources see is the input of the drive system, which is actually a DC link. Since, at the point of interconnection, sources and load have DC terminal characteristics, the interfaces for power flow control in Fig. 2.2 are constituted by DC-DC converters.



(a) – Parallel connection (b) – Series connection

Fig. 2.11 – Electrical connection of two DC sources for power sharing.

From the electrical point of view, the two sources can be connected in parallel or in series, in order to sum up the individual power contribution, as shown in Fig. 2.11.
In the following, only parallel connection is considered, as it is the most common in practice. Although the redundant configuration in Fig. 2.11-a is sometimes used [59] in order to get a DC-link voltage that is completely independent from the terminal voltage of all the sources, elimination of one converter is desirable, since it reduces the system complexity and cost and may increase overall efficiency.
The configuration in Fig. 2.12 is usually preferred in pure EV applications, due to the relatively constant terminal voltage of the battery constituting an ideal input to the drive system; moreover, direct connection between the battery and the load ensures that there are no added losses on the main power path.

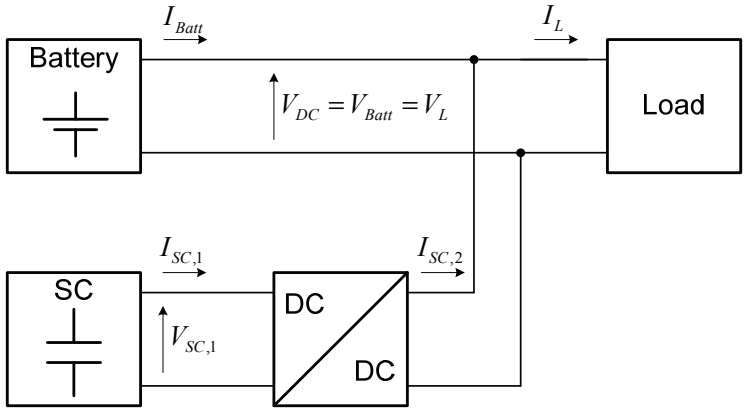


Fig. 2.12 – Battery-SC hybrid system with direct battery connection.

The DC/DC converter used to interface the SC bank to the DC-link has to satisfy the following general requirements:

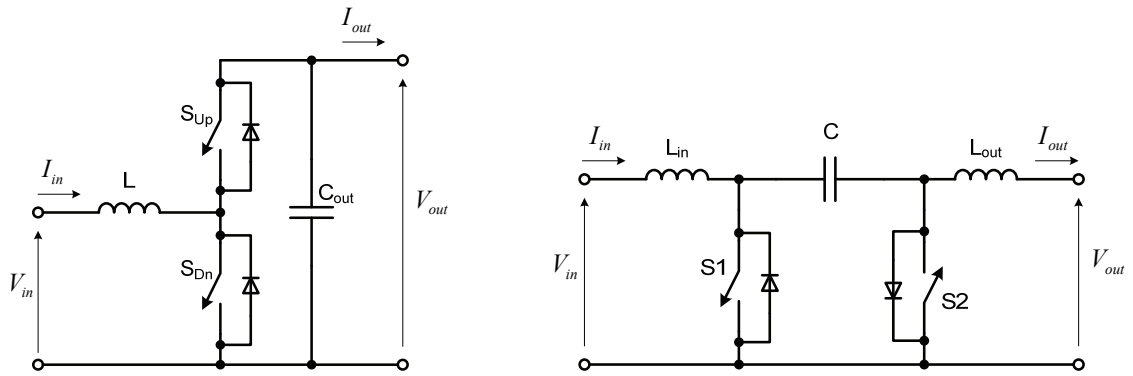
- Bidirectional, controllable power flow;
- Widely variable input (SC-side) voltage;
- Peak power handling capability equal to the peak power requirements of the load;
- Virtually constant output voltage, equal to the DC-link voltage.

Galvanic isolation between the SC bank and the DC-link is normally not a requirement, meaning that non-isolated converter topologies can be used; a transformer stage can still be necessary if the SC-side voltage is much lower than the DC-link [60,61]. However, in the power buffer application for pure EV, the power level is such that it is feasible to design the SC bank with a rated voltage that is comparable to the DC-link voltage, and isolated DC-DC converter will not be further discussed.
At least two standard topologies are presented in most classical power electronics textbooks [62] satisfying the basic specifications given above:

- Half Bridge;
- Cúk.

Those two converters are shown in Fig. 2.13. Indeed, the use of a bidirectional converter based on the Half Bridge topology for the combination of a battery with a supercapacitive bank was already proposed in the early ‘90s [62], when supercapacitors were still far from industrial deployment.

A detailed comparison between the two topologies in Fig. 2.13, and their suitability for the application in Fig. 2.12 is found in [64], where it is recognized that the Half Bridge (HB) topology is superior in terms of power density, due to the very bulky inductors needed by the Cúk converter to achieve the same performance. Moreover, voltage and current stress on the semiconductor switches of the HB are less than in Cúk. On the other hand, a bigger capacitor is needed on the DC-link side of HB, to filter the discontinuous current.



(a) – Half-Bridge (b) - Cúk

Fig. 2.13 – Classical solutions for bi-directional, non-isolated DC-DC converter.

Power electronics design almost invariably implies trading off between achievable efficiency, volume and cost reduction, with the weight given to each factor being dependent on the application. In the specific case of the HB converter employed in a pure electric EV like the one simulated in the previous paragraph, efficiency is important. In fact, the assumption behind the use of a hybrid source is that large burst of power are handled more efficiently by the power buffer than by the traction battery; since the latter is still quite an efficient device (average efficiency over the FUDS cycle is above 80% in the simulation case study), the use of a lossy converter on the power path of the SC buffer could bring the overall efficiency of the hybrid arrangement down to the same level of a battery-only system.

Weight obviously affects the vehicle driving range, since it increases the power needed for the motion. Volume of the converter does not directly affect the power need, if the vehicle external shape is not changed; however, the space occupied by the converter could in principle be occupied by some additional energy storage or by some other components, making volume minimization an important goal.

Cost is the most important issue in automotive, and EVs are no exception. Since the energy source is the most expensive part of the whole EV, careful design is necessary to keep the cost at affordable levels.

Although probably the best solution among all the conventional topologies, Half Bridge still has some serious limitations. Overall power density is limited by the bulky high-current inductor; moreover, the voltage and current stress on the solid state switches is high due to the widely variable voltage transfer ratio required by the application. For a given device technology, Volt-Ampere ratings of the switches indicate the amount of silicon required to implement the solid state switches of the converter, thus having direct impact on the converter size and cost.

The size of the inductor can be reduced by interleaving the modulation of several HB legs [65,66]. However, this technique leads to a more complex system, and does not reduce the overall Volt-Ampere requirements for the switches.

Soft-switching techniques can be applied to the HB [67,68] or to other topologies [69-73], with the aims of increasing the power density by increasing the switching frequency and improving the converter efficiency by virtually eliminating switching losses. On the downside, those techniques tend to increase the complexity of the converter, since additional components are necessary to achieve zero voltage and/or zero current switching of the main solid state switches; moreover, the voltage and current ratings of the main switches is normally higher (or at least not lower) that in the hard switched converters, in order to allow for resonant behaviour. One advantage of soft switching topologies that should not be overlooked is the potential for reduced EMI emission [74,75].
As a matter of fact, in the majority of published papers about battery-supercapacitor hybrid energy systems, the power flow control is achieved by a simple, hard switched, HB converter as the one in Fig. 2.13 [76,77,65]. Operating principle of such a converter is analyzed in detail later in the thesis, as it will also serve as base case for comparison with the newly proposed topology to be presented in the next chapter.

3 OPTIMIZED CONVERTER FOR BATTERY-SUPERCAPACITOR INTERFACE

In the previous chapter, standard power electronics solutions enabling for controllable, bidirectional power flow between two energy sources are presented. Such solutions are general purpose, and do not take into account some peculiar characteristics of a battery-supercapacitor hybrid energy source:

- The battery voltage does not vary much during a charge/discharge cycle of the SC-based power buffer;
- It is not advised to operate the SC buffer at very low SOC, since efficiency would be low due to the increased ESR losses.

Based on those considerations, it is possible to develop a dedicated, optimized converter structure allowing for controllable, bidirectional power flow using less resources (less silicon in the power electronics switches, smaller magnetic components, etc.) and/or with better operating efficiency.

The basic idea used to design the optimized topology is to split the SC buffer in two parts, as shown in Fig. 3.1. The lower part of the SC buffer will charge/discharge with the load-side current I_{HC} and is therefore referred as "uncontrolled SC bank"; the higher part of the SC buffer ("controlled SC bank") has a half bridge connected across its terminals, and the charge/discharge current is therefore dependent on the state of the switches. With such an arrangement, since only a fraction of the power being exchanged between the SC buffer and the load is processed through a power electronics converter, less losses and a small converter are to be expected, compared to the base case of a fully rated half bridge as the one in Fig. 2.13.

In the following, it will be shown that the proposed converter is indeed able to control the power flow, and that a proper design ensures that a very good part of the energy contained in the SC buffer can be transferred to the load.

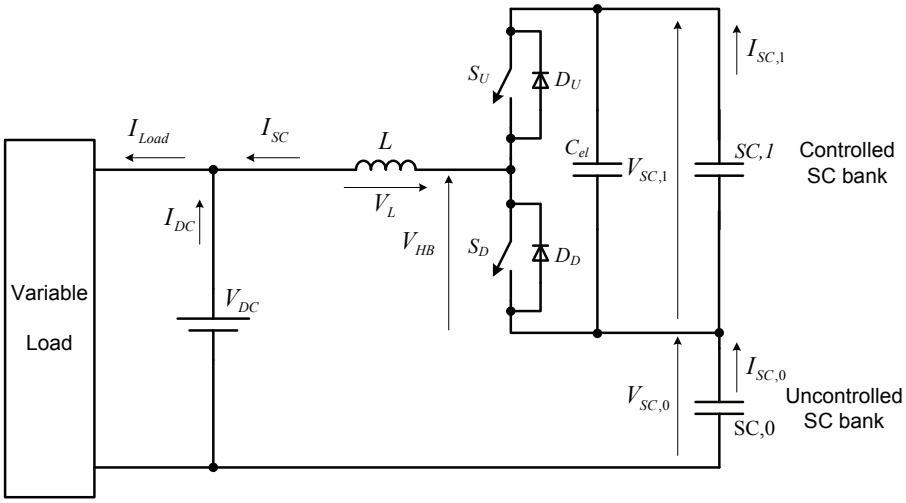


Fig. 3.1 – Proposed topology for SC-based power buffer interfaced to a load supplied by a main battery

3.1 Operating Principle

Due to the presence of the diodes D_U and D_D, the following voltage constraints apply:

$$V_{SC,1} + V_{SC,0} \geq V_{DC} \tag{3.1}$$

$$V_{SC,0} \leq V_{DC} \tag{3.2}$$

In order to simplify the analysis, it is assumed here that the switches S_U and S_D are complementarily controlled, meaning that at any given time one and only one of them is ON. Also, the dead time necessary to avoid shoot-through is neglected. Then, the system is analyzed using local average for all quantities over each switching period T_{SW} (see Fig.3.2).

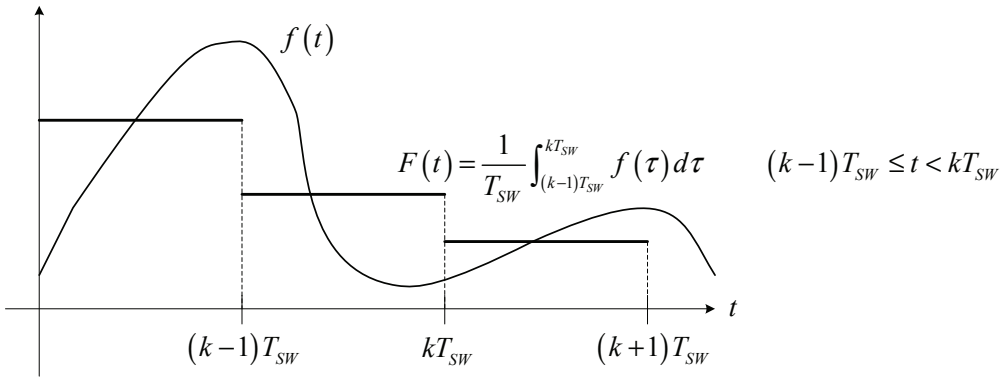


Fig. 3.2 – Locally averaged quantity over a switching period

The duty cycle of the half bridge is defined at any switching period as the ratio between the ON time of the upper switch and the total period:

$$D = \frac{T_{S_U,ON}}{T_{SW}} \tag{3.3}$$

By definition, such a quantity is time-discrete in nature (it is defined every T_{SW}); however, if we are analyzing phenomena that have much slower dynamics than the

sampling period, we can assume the duty cycle, as well as all the other locally averaged quantities, as being time-continuous.
In all operating conditions satisfying both (3.1) and (3.2), it is possible to control the current I_{SC} acting on the duty cycle D of the half bridge.
Due to the series connection, current $I_{SC,0}$ flowing through the lower SC bank is always equal to the inductor current, while the current in the upper SC bank $I_{SC,1}$ is related to the inductor current by the bridge duty cycle:

$$I_{SC,0} = I_{SC} \tag{3.4}$$

$$I_{SC,1} = I_{SC} \cdot D \tag{3.5}$$

The voltage across each SC bank will evolve according to the well known equation:

$$\frac{dV_{SC,x}(t)}{dt} = \frac{1}{C_{SC,x}} \cdot I_{SC,x}(t) \qquad x = 0,1 \tag{3.6}$$

where $C_{SC,x}$ are the equivalent capacitances in Farad of the two SC banks.
Comparing the two equations in (3.6), using (3.5), we get:

$$dV_{SC,1} = \frac{C_{SC,0}}{C_{SC,1}} \cdot D \cdot dV_{SC,0} \tag{3.7}$$

Referring to Fig.3.1, we can write the voltage balance equation:

$$V_{DC} = -V_L + V_{HB} + V_{SC,0} \tag{3.8}$$

Expressing the converter output voltage as function of the duty cycle D, neglecting the energy stored in the inductor (SC energy is orders of magnitude higher), and assuming therefore the system to be almost always in dynamic steady state [62] during a charge/discharge cycle, the voltage balance reduces to:

$$V_{DC} = D \cdot V_{SC,1} + V_{SC,0} \tag{3.9}$$

Solving for D and substituting in (3.7), we can derive the differential equation relating the voltages across the two SC banks:

$$V_{SC,1} \cdot dV_{SC,1} = \frac{C_{SC,0}}{C_{SC,1}} \cdot \left(V_{DC} - V_{SC,0}\right) \cdot dV_{SC,0} \tag{3.10}$$

Such equation can be solved for any given set of initial conditions $V_{SC,0}(0)$ and $V_{SC,1}(0)$:

$$V_{SC,1}(t) = \sqrt{{V_{SC,1}}^2(0) + \frac{C_{SC,0}}{C_{SC,1}}\left(2\left(V_{DC} - V_{SC,0}(0)\right) \cdot \Delta V_{SC,0}(t) - {\Delta V_{SC,0}}^2(t)\right)} \tag{3.11}$$

with $\Delta V_{SC,0}(t) = V_{SC,0}(t) - V_{SC,0}(0)$.
The most remarkable aspect of (3.11) is that the voltage (or, equivalently, the SOC) of the controlled SC bank $V_{SC,1}$ is a unique function of the voltage of the uncontrolled bank $V_{SC,0}$, and such a function does not depend on the particular shape of the converter output current. This allows us to use the design degree of freedom given by the capacitance ratio of the two SC banks to properly shape the charge/discharge trajectory

of the power buffer. In particular, the capacitance ratio is related to the upper and lower voltage limits during SC power cycling by:

$$\frac{C_{SC,0}}{C_{SC,1}} = \frac{{V_{SC,1,Max}}^2 - {V_{SC,1,\min}}^2}{\left(V_{SC,0,Max} - V_{SC,0,\min}\right)\left(2V_{DC} - V_{SC,0,Max} - V_{SC,0,\min}\right)} \tag{3.12}$$

3.2 Energy Cycling Capabilities

In this chapter, the amount of energy that can be cycled in and out the SC-based power buffer is calculated, under the constraints posed by the topology.

If the voltage at the terminal of a capacitive storage device of capacitance C_{SC} is allowed to vary between $V_{SC,\min}$ and $V_{SC,Max}$, the amount of energy that can be cycled in and out from the device is:

$$E_{SC,cycle} = \frac{1}{2} \cdot C_{SC} \cdot \left(V_{SC,Max}^2 - V_{SC,\min}^2\right) \tag{3.13}$$

The energy utilization ratio ρ_E can be defined as:

$$\rho_E = \frac{E_{SC,cycle}}{E_{SC,Max}} = \frac{\left(V_{SC,Max}^2 - V_{SC,\min}^2\right)}{V_{SC,Max}^2} \tag{3.14}$$

In the proposed system there are two separate SC banks, each cycling between its own minimum and maximum voltage. The energy utilization ratio is then expressed as:

$$\rho_E = \frac{E_{SC,tot,cycle}}{E_{SC,tot,Max}} = \frac{C_{SC,0}\left(V_{SC,0,Max}^2 - V_{SC,0,\min}^2\right) + C_{SC,1}\left(V_{SC,1,Max}^2 - V_{SC,1,\min}^2\right)}{C_{SC,0} \cdot V_{SC,0,Max}^2 + C_{SC,1} \cdot V_{SC,1,Max}^2} \tag{3.15}$$

Obviously, it is desirable to have ρ_E as close to unity as possible, in order to make good use of the energy storage capability of the power buffer in use.

In the topology of Fig.3.1, the voltage across the uncontrolled SC bank is limited by (3.2). It would be possible to use a lower value for the maximum allowed voltage across the bank, but the choice:

$$V_{SC,0,Max} = V_{DC} \tag{3.16}$$

maximizes the energy content of the uncontrolled part of the power buffer, thus leading to the smaller possible converter.

> Note: This is somewhat similar to the choice commonly made in case of a standard Half-Bridge interface, where a condition similar to (3.16) is imposed to minimize the size of the power electronics and magnetic components.

The maximum voltage across the controlled SC bank is not constrained by the topology; it is only limited by the voltage withstanding capabilities of the switching devices and the SC bank itself. In the following it is assumed that the voltage rating of the controlled bank is equal to the one of the uncontrolled bank:

$$V_{SC,1,Max} = V_{SC,0,Max} = V_{DC} \tag{3.17}$$

Note: This choice leads to a voltage rating for the switching devices equal to the base case of a standard Half-Bridge interface. A generalization will be given in section 3.5.

Let us define the design parameter "capacitance ratio" x as:

$$x = \frac{C_{SC,0}}{C_{SC,1}} \tag{3.18}$$

Also, let us normalize the voltages across each SC bank to the battery voltage:

$$v_{SC,0} = \frac{V_{SC,0}}{V_{DC}}, \qquad v_{SC,1} = \frac{V_{SC,1}}{V_{DC}} \tag{3.19}$$

Assuming as initial condition that both SC banks are fully charged to their maximum voltage, equal to the rated voltage, (3.11) simplifies to:

$$v_{SC,1}(t) = \sqrt{1 - x\left(1 - v_{SC,0}\right)^2} \tag{3.20}$$

The minimum voltage of each SC bank is determined by solving (3.1) with the sign of equality, taking (3.20) into account. This yields:

$$v_{SC,0,\min} = 1 - \frac{1}{\sqrt{1+x}}, \qquad v_{SC,1,\min} = \frac{1}{\sqrt{1+x}} \tag{3.21}$$

The energy utilization ratio takes then the remarkably simple form:

$$\rho_E = \frac{E_{SC,tot,cycle}}{E_{SC,tot,Max}} = \frac{2x}{(1+x)\sqrt{1+x}} \tag{3.22}$$

The equation above tells us that only the capacitance ratio determines how much of the theoretically available energy in the SC banks can actually be used by the topology in Fig.3.1. The energy utilization ratio is plotted in Fig.3.3, showing a maximum value:

$$\rho_{E,Max} = \rho_E\big|_{x=2} = 0.77 \tag{3.23}$$

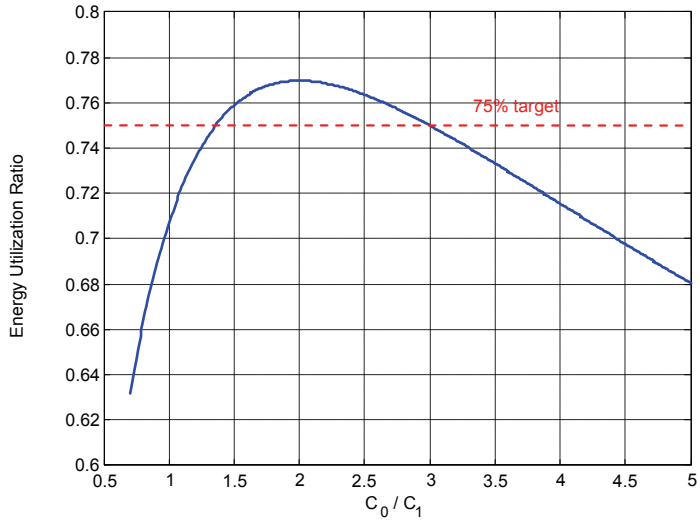


Fig. 3.3 – Energy Utilization Ratio

Note: In [78], the capacitance ratio has been selected by direct application of (3.12), imposing the intuitive condition of both SC banks cycling between 100% and 50% of the battery voltage, resulting in exactly 75% energy utilization ratio. Here, such a choice ($x = 3$) has been shown to be less than optimal in terms of utilization of the energy contained in the SC buffer.

3.3 Comparison of the Proposed System to an Equivalent Half-Bridge Based System

Before even attempting to compare two different systems, it is necessary to define criteria for equivalence. In this context, two different Battery-SC systems are considered to be equivalent if the following general conditions are met:

1. The batteries in the two systems are identical;
2. Both systems allow for controllable, bidirectional power flow to/from the SC-based power buffer at the same maximum rate $P_{out,\max}$, throughout the whole charge/discharge process;
3. Both systems have the same energy storage capability in the respective SC buffer;
4. Both systems are able to utilize the same fraction of such total energy, while being charged/discharged at rated power;

Let us now consider the two systems in Fig.3.4. On the left side (Fig.3.4.a) is a conventional system in which the SC-based power buffer is interfaced to the battery by a Half Bridge; Fig.3.4.b shows the proposed topology, referred in the following as Half Controlled (HC) for brevity. Equivalence condition 1. is quite straightforward, and in terms of voltages it can be stated as:

$$V_{DC,HB} = V_{DC,HC} = V_{DC} \tag{3.24}$$

Equivalence condition 2. implies:

$$P_{out,\max} = V_{DC} \cdot I_{HB,\max} = V_{DC} \cdot I_{HC,\max} \Rightarrow I_{HB,\max} = I_{HC,\max} = I_{out,\max} \tag{3.25}$$

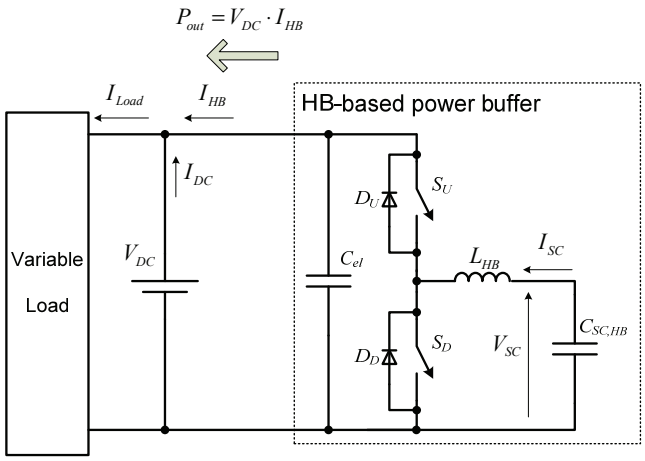
Equivalence condition 3 can be expressed as:

$$E_{SC,HB} = E_{SC,HC} \Rightarrow \frac{1}{2} C_{SC,HB} \cdot V_{SC,HB,\max}^2 = \frac{1}{2}\left(C_{SC,0} \cdot V_{SC,0,\max}^2 + C_{SC,1} \cdot V_{SC,1,\max}^2 \right) \tag{3.26}$$

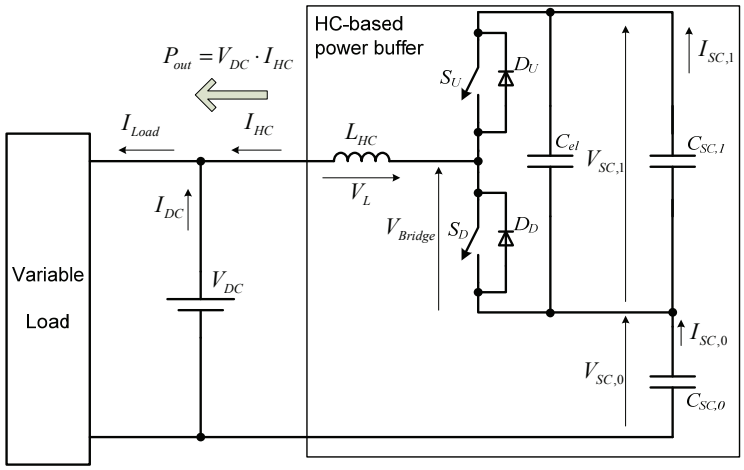
Taking (3.17) into account, and assuming that the SC bank of the HB-based system has a rated voltage equal to the battery voltage, the equivalence of stored energy translates into:

$$E_{SC,HB} = E_{SC,HC} \Rightarrow C_{SC,HB} = C_{SC,0} + C_{SC,1} \tag{3.27}$$

Equivalence condition 4. requires some additional considerations. In the previous chapter it has been shown that the fraction of the SC energy that can be extracted from the SC banks using the HC topology is slightly above 75% for a wide range of capacitance ratios between 1.3 and 3. Therefore, an equivalent HB-based system must also have the capability of extracting 75% of the energy available in its SC buffer at rated converter power.



a – Conventional HB-based power buffer



b – Proposed HC-based power buffer

Fig. 3.4 – Two topologies for active, bidirectional interface of SC-based power buffers

3.3.1 Required Volt-Ampere rating of converter switches

Assuming all components to be ideal, the switches in the HB converter have to withstand a voltage equal to the DC-side voltage:

$$V_{SW,HB} = V_{DC} \tag{3.28}$$

If we assume the converter to be lossless, then in steady state the power flowing at the SC side must be equal to the power flowing at the battery side of the converter:

$$V_{SC} \cdot I_{SC} = V_{DC} \cdot I_{HB} \tag{3.29}$$

According to (3.14), in order to be able to transfer at least 75% of the total energy stored in the SC bank to the load, the voltage of the SC bank must be allowed to vary from its rated value to half of it. Therefore:

$$I_{SC,Max} = \frac{V_{DC} \cdot I_{out,Max}}{V_{SC,Min}} = \frac{V_{SC,Max}}{V_{SC,Min}} \cdot \frac{V_{DC}}{V_{SC,Max}} \cdot I_{out,Max} = 2 \cdot \frac{V_{DC}}{V_{SC,Max}} \cdot I_{out,Max} \tag{3.30}$$

The current above is also the maximum current that must flow into the switches of the half-bridge. Minimum current rating is obtained if the SC buffer can be charged up to the battery voltage (cannot be higher, due to the clamping effect of the diode in the HB topology).

Combining (3.28) and (3.30), we get the minimum required VA rating of the switches employed in the HB-based system:

$$S_{SW,HB} = 2 \cdot V_{DC} \cdot I_{out,Max} = 2 \cdot P_{out,\max} \tag{3.31}$$

In the HC-based system, the switches have to withstand a voltage equal to the maximum voltage across the controlled SC bank. Therefore, according to (3.17):

$$V_{SW,HC} = V_{DC} \tag{3.32}$$

The current flowing in the switches is always equal to the DC-side current, resulting in switch rated current given by:

$$I_{SW,HC} = I_{out,\max} \tag{3.33}$$

Minimum VA rating of the switches employed in the HC system is then:

$$S_{SW,HC} = V_{DC} \cdot I_{out,Max} = P_{out,\max} \tag{3.34}$$

Direct comparison of (3.34) with (3.31) shows that the HC system can be built with solid state switches having half of the VA rating of what would be necessary for an equivalent HB system.

3.3.2 Idealized Voltage-Current waveforms during constant power discharge

Case 1 – Half Bridge based topology (HB)

The SC buffer is giving constant power P_{dis} to the load. Therefore:

$$I_{HB}(t) = I_{dis} = \frac{P_{dis}}{V_{DC}} = \text{constant} \tag{3.35}$$

Let us assume the SC bank to be initially charged at rated voltage $V_{SC,HB}(0) = V_{DC}$. During the cycle the bank voltage and current will evolve according to:

$$V_{SC,HB}(t) = V_{DC} \cdot \sqrt{1 - \frac{2}{C_{SC,HB}} \cdot \frac{I_{dis}}{V_{DC}} \cdot t} \tag{3.36}$$

$$I_{SC,HB}(t) = I_{dis} \cdot \frac{V_{DC}}{V_{SC,HB}(t)} = \frac{I_{dis}}{\sqrt{1 - \frac{2}{C_{SC,HB}} \cdot \frac{I_{dis}}{V_{DC}} \cdot t}} \tag{3.37}$$

The duty cycle of the HB is expressed by:

$$D_{HB} = \frac{V_{SC,HB}(t)}{V_{DC}} = \sqrt{1 - \frac{2}{C_{SC,HB}} \cdot \frac{I_{dis}}{V_{DC}} \cdot t} \tag{3.38}$$

According to (3.36), the time required to discharge the initially full SC buffer to $V_{DC}/2$, corresponding to 75% energy extraction is:

$$T_{dis,HB} = \frac{3}{8} \cdot \frac{V_{DC}}{I_{dis}} \cdot C_{SC,HB} \tag{3.39}$$

In addition to the locally averaged waveforms, we must also evaluate the switching components related to the operation of the switches, as shown in Fig.3.5.
The instantaneous current flowing out from the SC bank (inductor current) is then expressed as:

$$i_{SC,HB} = I_{SC,HB} + i_{SC,HB,ripple} \tag{3.40}$$

with:

$$i_{SC,HB,ripple} = \begin{cases} \dfrac{V_{DC} - V_{SC,HB}}{2L} \cdot \left(2t - DT_{SW}\right) & 0 \le t < DT_{SW} \\ \dfrac{V_{SC,HB}}{2L} \cdot \left(\left(1-D\right)T_{SW} - 2\left(t - DT_{SW}\right)\right) & DT_{SW} \le t < T_{SW} \end{cases} \tag{3.41}$$

being the zero-average ripple component; such a component has its maximum amplitude when the SC-side voltage is half of the DC-side voltage ($D_{HB,Max\_ripple} = 0.5$).
Assuming perfect filtering action, the current in the electrolytic capacitor is given by:

$$i_{Cel,HB}\left(t\right) = \begin{cases} i_{SC,HB} - I_{dis} & 0 < t < DT_{SW} \\ -I_{dis} & DT_{SW} < t < T_{SW} \end{cases} \tag{3.42}$$

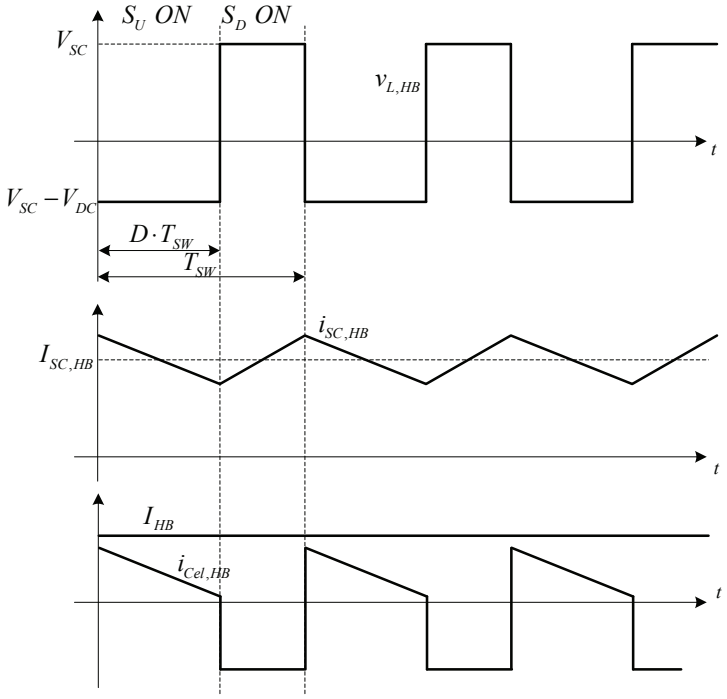


Fig. 3.5 – Switching waveforms, HB topology.

Case 2 – Proposed topology (HC)

The SC buffer is giving constant power P_{dis} to the load. Therefore:

$$I_{HC}(t) = I_{dis} = \frac{P_{dis}}{V_{DC}} = \text{constant} \tag{3.43}$$

Due to the series connection, $I_{SC,0} = I_{dis}$, and the voltage across the lower bank varies linearly with time:

$$V_{SC,0}(t) = V_{DC} - \frac{I_{dis}}{C_{SC,0}} \cdot t \tag{3.44}$$

According to (3.20), the voltage across the controlled SC bank is then:

$$V_{SC,1}(t) = \sqrt{{V_{DC}}^2 - x \cdot \left(\frac{I_{dis}}{C_{SC,0}} \cdot t \right)^2} \tag{3.45}$$

The duty cycle of the switches, according to (3.9), is:

$$D_{HC}(t) = \frac{V_{DC} - V_{SC,0}}{V_{SC,1}} = \frac{I_{dis}}{C_{SC,0}} \cdot \frac{t}{\sqrt{{V_{DC}}^2 - x \cdot \left(\frac{I_{dis}}{C_{SC,0}} \cdot t \right)^2}} \tag{3.46}$$

The current flowing through the controlled SC bank is:

$$I_{SC,1}(t) = I_{dis} \cdot D_{HC}(t) = \frac{{I_{dis}}^2}{C_{SC,0}} \cdot \frac{t}{\sqrt{{V_{DC}}^2 - x \cdot \left(\frac{I_{dis}}{C_{SC,0}} \cdot t \right)^2}} \tag{3.47}$$

The time needed to discharge at constant power 75% of the energy contained in an initially full SC buffer can be calculated by solving the equation:

$$0.25 \cdot \left(C_{SC,0} + C_{SC,1} \right) {V_{DC}}^2 = C_{SC,0} \cdot V_{SC,0}\left(T_{dis}\right)^2 + C_{SC,1} \cdot V_{SC,1}\left(T_{dis}\right)^2 \tag{3.48}$$

using the expressions (3.44) and (3.45) for the individual bank voltages. This yields:

$$T_{dis,HC} = \frac{3}{8} \cdot \frac{V_{DC}}{I_{dis}} \cdot \frac{x+1}{x} \cdot C_{SC,0} \tag{3.49}$$

The switching component of the inductor current (Fig.3.6) is expressed as:

$$i_{HC} = I_{HC} + i_{HC,ripple} \tag{3.50}$$

with:

$$i_{HC,ripple} = \begin{cases} \frac{V_{SC,1} + V_{SC,0} - V_{DC}}{2L} \cdot \left(2t - DT_{SW}\right) & 0 \le t < DT_{SW} \\ \frac{V_{DC} - V_{SC,0}}{2L} \cdot \left(\left(1-D\right) T_{SW} - 2\left(t - DT_{SW}\right) \right) & DT_{SW} \le t < T_{SW} \end{cases} \tag{3.51}$$

being the zero-average ripple component; In general, worst case ripple and duty cycle at which such a ripple occurs are dependent on the capacitance ratio, as shown in Fig.3.7. Notice that for any reasonable value of x, the worst-case current ripple in the inductor of the HC system is lower than the one in the HB system, assuming the same inductance value and the same switching frequency for both cases.
Assuming perfect filtering action, the current in the electrolytic capacitor is given by:

$$I_{Cel,HC}(t)=\begin{cases} I_{dis}-I_{SC,1} & 0<t<DT_{SW} \\ -I_{SC,1} & DT_{SW}<t<T_{SW} \end{cases} \tag{3.52}$$

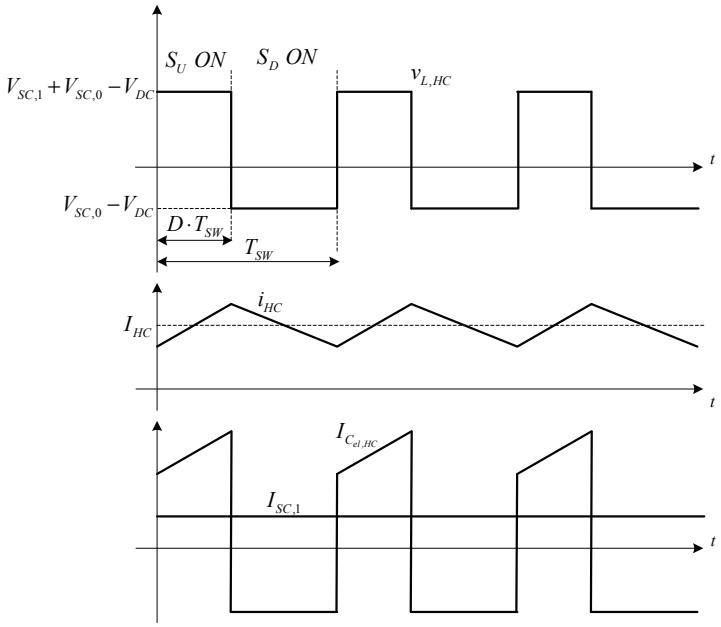


Fig. 3.6 – Switching waveforms, HC topology.

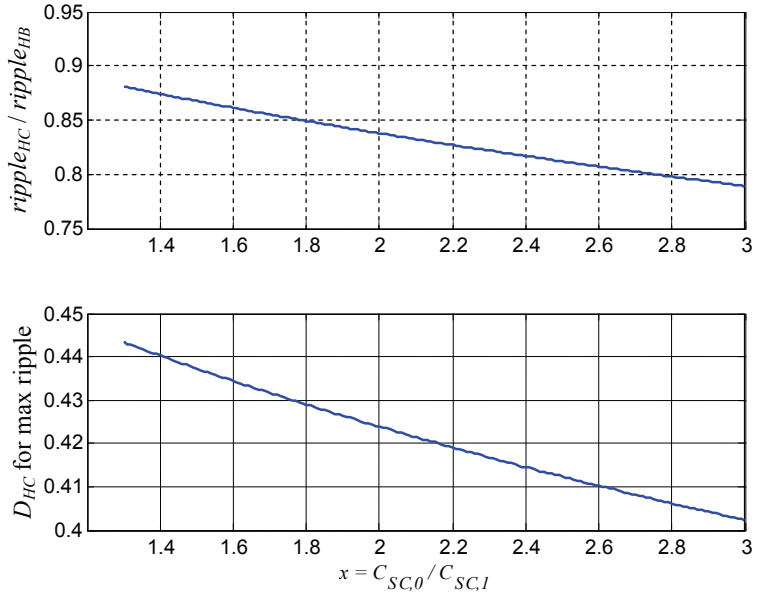


Fig. 3.7 – Worst case ripple as a function of the capacitance ratio x.

3.4 Evaluation of System Losses

So far, in developing the equations that govern the operation of the HC system of Fig.3.1, all components have been assumed as lossless. In reality, losses will arise when power is cycled in and out the SC-based buffer. Main sources of losses are:

Supercapacitors: electrical resistivity of the electrodes is not zero; also, losses are generated in the electrolyte. A general expression for the losses is quite involved and depends on the actual voltage distribution inside the device [33]. According to the considerations in chapter 1, an equivalent series resistance is associated to the component; such a resistance is assumed to be constant with voltage and frequency.

Solid State Switches: Whatever the technology used to implement the switches (MOSFET, IGBT, etc.), those components exhibits both conduction and switching losses. The former are due to finite conductivity of the material when the switch is ON, while the latter arise from the non-instantaneous switching between the ON and OFF states, causing the switch to operate for short time with both high current (the ON state current) and high voltage (the OFF state voltage).

Inductor: The finite conductivity of the winding material (typically copper) leads to ohmic losses; at the same time, hysteresis and eddy current losses are generated in the ferromagnetic core.

Capacitors: similarly to supercapacitors, losses arise when current flows in electrolytic capacitors. Again, a constant equivalent series resistance ESR is assumed for those components.

If series resistance of each component is included in the circuit analysis, the resulting current and voltage waveforms during constant power discharge will in general be different from the ones calculated in the previous section. However, since by design losses are a relatively small part of the energy being cycled out of the SC buffer, it is possible to approximate the losses as caused by the idealized current flowing into the non-ideal components. The proposed approach gives results that are quite accurate, as will be confirmed by detailed simulation. A significant advantage of this simplified procedure is the derivation of relatively simple analytical expressions for the losses that can be used in the design phase, and that allow for immediate comparison between different topologies.
A further aspect to be considered is that losses during a charge/discharge cycle are in general dependent on the voltage-current trajectory followed during that particular cycle. In this context a simple constant power discharge is considered.

3.4.1 Losses in the Supercapacitor Banks

The amount of energy dissipated into the ESR of the supercapacitors in the HB-based system of Fig.3.4.a is expressed as:

$$E_{SC,HB} = \int_0^{T_{dis,HB}} I_{SC,HB}^2 \cdot ESR_{SC,HB} \cdot dt \tag{3.53}$$

Using (3.37) and (3.39), we can evaluate the amount of losses during a constant power discharge from full SC voltage to half of it, corresponding to the transfer of 75% of the total SC energy to the load:

$$E_{SC,HB} = ESR_{SC,HB} \cdot \int_0^{Tdis,HB} \frac{{I_{dis}}^2}{1 - \frac{2}{C_{eq}} \cdot \frac{I_{dis}}{V_{DC}} \cdot t} \cdot dt = {I_{dis}}^2 \cdot ESR_{SC,HB} \cdot T_{dis,HB} \cdot \int_0^1 \frac{1}{1 - \frac{3}{4}t'} dt' =$$
$$= {I_{dis}}^2 \cdot ESR_{SC,HB} \cdot T_{dis,HB} \cdot \left(\frac{8}{3}\ln 2\right) \approx 1.85 \cdot {I_{dis}}^2 \cdot ESR_{SC,HB} \cdot T_{dis,HB} \quad (3.54)$$

In case of the HC-based system of Fig.3.4.b, losses in the Supercapacitors are composed of two different terms:

$$E_{SC,HC} = E_{SC,0} + E_{SC,1} = \int_0^{T_{dis,HC}} \left(I_{SC,0}^2(t) \cdot ESR_{SC,0}\right) dt + \int_0^{T_{dis,HC}} \left(I_{SC,1}^2(t) \cdot ESR_{SC,1}\right) dt \quad (3.55)$$

Using (3.4), (3.47) and (3.49), we can evaluate the amount of losses during a constant power discharge of 75% of the total SC energy to the load:

$$E_{SC,HC} = I_{dis}^2 \cdot ESR_{SC,0} \cdot T_{dis,HC} + I_{dis}^2 \cdot ESR_{SC,1} \cdot \int_0^{T_{dis,HC}} \frac{I_{dis}^2 \cdot t^2}{{C_{SC,0}}^2 \left({V_{DC}}^2 - x \cdot \left(\frac{I_{dis}}{C_{SC,0}} t\right)^2\right)} dt =$$
$$= {I_{dis}}^2 \cdot T_{dis,HC} \cdot \left(ESR_{SC,0} + ESR_{SC,1} \cdot \left(\frac{8 \cdot \operatorname{arctan} h\left(\frac{3(x+1)}{8\sqrt{x}}\right)}{3\sqrt{x}(x+1)} - \frac{1}{x} \right) \right) \quad (3.56)$$

In order to compare the losses in the SC banks of the two systems (3.53) and (3.55), the concept of equivalence previously defined has to be applied. In particular, due to (3.27), the capacitances of the SC banks in the HC-based system can be expressed in terms of the capacitance of the SC bank of the HB-system as:

$$C_{SC,0} = \frac{x}{x+1} \cdot C_{SC,HB}, \qquad C_{SC,1} = \frac{1}{x+1} \cdot C_{SC,HB} \quad (3.57)$$

The ESR of the banks in the HC system can also be related to the ESR of the bank in the HB system by applying the so-called "*constant Ohm-Farad product*" principle. According to this principle, the capacitance C_1 and the internal resistance ESR_1 of a given bank are related to the homologous quantities C_2, ESR_2 of another bank by:

$$C_1 \cdot ESR_1 = C_2 \cdot ESR_2 \quad (3.58)$$

Note: Intuitively, the constant ohm-farad product can be explained by considering the parallel connection of n identical capacitors (or Supercapacitors) having capacitance C and equivalent series resistance R. The resulting equivalent capacitor will have a capacitance numerically equal to nC and an ESR numerically equal to R/n. Obviously, the Ohm-Farad product of the "big" capacitor made up of parallel connection of n "small" capacitors is same as the Ohm-Farad product of any of the n "small" capacitors. As a matter of fact, capacitors (or supercapacitors) built with the same technological process tend to follow (3.58) quite closely.

Applying (3.58) to the SC banks whose capacitances are related by (3.57), we get:

$$ESR_{SC,0} = \frac{x+1}{x} \cdot ESR_{SC,HB}\,, \qquad ESR_{SC,1} = (x+1) \cdot ESR_{SC,HB} \tag{3.59}$$

Furthermore, we may notice that the discharge times given by (3.39) and (3.49) coincide in the case of equivalent systems, whose bank capacitances are related by (3.57). This had to be expected since the analysis has been carried neglecting losses, and if the systems contained initially the same amount of energy, the time needed to discharge 75% of such energy at the same constant power will be equal, regardless of the power electronics interface in use.
With the above mentioned arguments, (3.56) can be expressed in terms of the capacitance and equivalent series resistance of the equivalent HB-based system:

$$E_{SC,HC} = I_{dis}^2 \cdot ESR_{SC,HB} \cdot T_{dis,HB} \cdot \left(\frac{8(x+1)}{3\sqrt{x(x+1)^2}} \cdot \arctan h\left(\frac{3(x+1)^2}{8\sqrt{x(x+1)^2}} \right) \right) \tag{3.60}$$

This expression makes it very easy to compare the overall losses in the SC banks of the two equivalent systems in Fig.3.4. In particular, it is interesting to look at the ratio between the losses in the SC banks of the two systems:

$$\rho_{E_{SC}} = \frac{E_{SC,HC}}{E_{SC,HB}} = \frac{(x+1)}{\ln 2\sqrt{x(x+1)^2}} \cdot \arctan h\left(\frac{3(x+1)^2}{8\sqrt{x(x+1)^2}} \right) \tag{3.61}$$

Such a function is reported in Fig.3.8, and carries the following main information:

- Losses arising in the SC banks of the HC-based system are always higher than losses in the SC bank of an equivalent HB-based power buffer;
- The actual ratio between those losses is dependent on the capacitance ratio of the HC-based system, and has a minimum value $\rho_{E_{SC},\min} = 1.084$ for $x_{\min\_SC\_loss} = 2.56$;
- Difference in SC losses between the two systems is below 10% for a wide range of capacitance ratios.

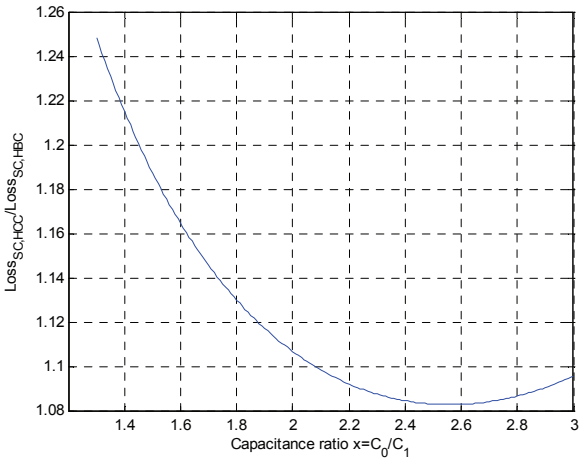


Fig. 3.8 – Ratio of SC losses as a function of x.

Distribution of SC losses in HC-based system

In the HB-based power buffer there is only one bank of Supercapacitors. Since such a bank is normally made up of series/parallel connection of many nominally identical SC cells, it is obvious that each of the constituting cells is equally stressed.

However, in the HC-based system there are two different SC banks that are charged and discharged with different current and are therefore in general subjected to different stresses. It is therefore meaningful to look at how losses are distributed among the two SC banks, and in order to do so we can define the ratio of per-unit losses as follows:

$$\rho_{SC\_loss} = \frac{E_{SC,0}}{x \cdot E_{SC,1}} = \left(\frac{8x^2}{3\sqrt{x(x+1)^2}} \cdot \operatorname{arctan} h\left(\frac{3(x+1)^2}{8\sqrt{x(x+1)^2}} \right) - x \right)^{-1} \tag{3.62}$$

In the definition above, the principle of constant Ohm-Farad ratio has been applied to the two SC banks; an extension of that principle also implies that a capacitor having x times the capacitance can also accept x times as much losses.

The function in (3.62) is plotted in Fig.3.9, suggesting the following considerations:

- In general, individual cells of different SC banks are unequally stressed;
- It exist an optimal capacitance ratio $x_{opt\_SC\_loss\_ratio} = 2.4$, for which all cells in the system are equally stressed, assuming constant current charge/discharge;
- For values of x smaller that the optimal, the uncontrolled SC bank is more stressed, and vice-versa.

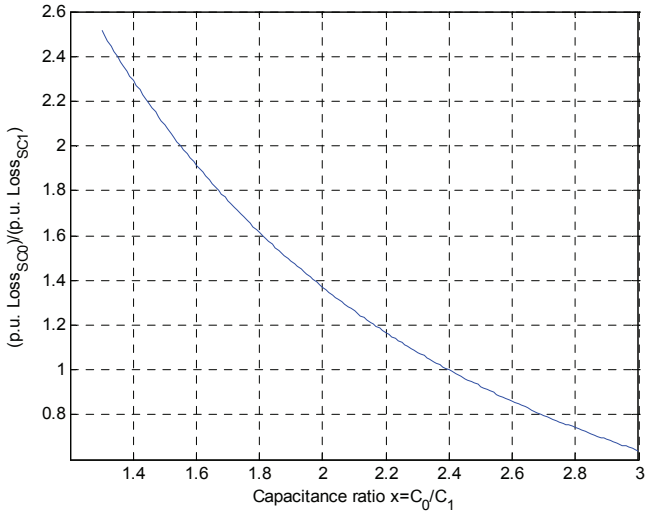


Fig. 3.9 – Distribution of SC losses in HC-based system as a function of x.

3.4.2 Losses in the Solid State Switches

Modelling the conduction losses

The Voltage-Current characteristics of a solid state switch during the ON state (conduction) are typically non-linear, as shown in Fig. 3.10. The simple assumption of an equivalent ON-state resistance for the switch is accurate enough for unipolar devices (MOSFET), but does not match the behaviour of bipolar devices (for instance IGBT or

diode), which are the most likely used in the voltage and current range of interest in traction applications for electric vehicles.
The most widespread approximation used to model the behaviour of a bipolar switch in its conductive state is to assume the forward voltage v_f as composed by a constant voltage drop $V_{f,0}$ (the junction or threshold voltage) and a resistive drop caused by the differential resistance r_f (see Fig.3.10):

$$v_f = V_{f,0} + r_f \cdot i_f \tag{3.63}$$

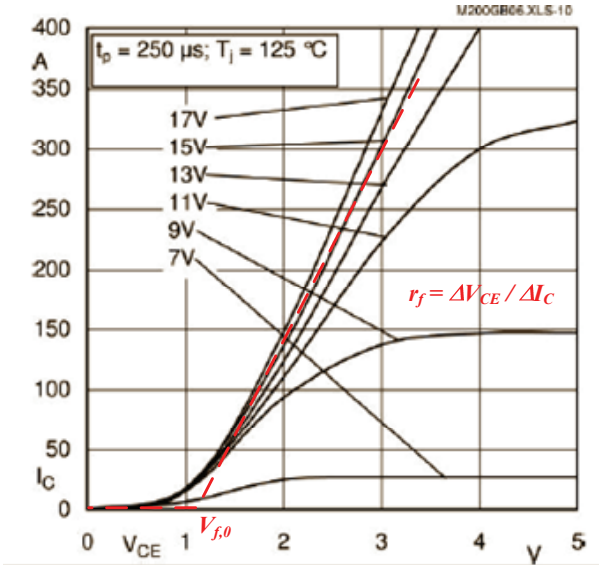


Fig. 3.10 – ON-state Voltage-Current characteristic of a bipolar switch. Datasheet data (Semikron SKM200GB063), and corresponding piecewise linear approximation.

Over each switching period, the ON-state losses of the switch can therefore be evaluated as:

$$\begin{aligned} P_{SW,cond,Tsw} &= \frac{1}{T_{SW}} \cdot \int_0^{T_{SW}} \left(v_f \cdot i_f \right) dt = V_{f,0} \cdot \frac{1}{T_{SW}} \cdot \int_0^{T_{SW}} i_f dt + \frac{1}{T_{SW}} \cdot \int_0^{T_{SW}} \left(r_f \cdot {i_f}^2 \right) dt \\ &= V_{f,0} I_f + r_f {I_{f,rms}}^2 \end{aligned} \tag{3.64}$$

where we have defined I_f as the local average of the current flowing into the switch over a switching period, and $I_{r,rms}$ as the local *rms* value of the current over a switching period.

Modelling the switching losses

Switching waveforms of modern solid state devices are highly non-linear. In general, the finite rise/fall times of current and voltages across a commutating switch will give rise to losses at each commutation, as shown in Fig.3.11. For IGBTs used in bridge configuration with an inductive load, loss figures are usually given in data sheets in terms of switching energy dissipated at each transition, as a function of current and voltage to be commutated, and for a given circuit configuration (mainly, the gate resistance is of importance for IGBTs).

$$\Delta E_{SW,switching} = f\left(V_{OFF}, I_{ON}, R_G\right) \tag{3.65}$$

A first order approximation is to fix a value for the gate resistance (the gate driver is known by design and does not change during operation) and consider linear dependency of the switching energy for both voltage and currents:

$$\Delta E_{SW,switching} = K_{SW}\left(V_{OFF,rat}, I_{ON,rat}\right) \cdot \frac{V_{OFF} \cdot I_{ON}}{V_{OFF,rat} \cdot I_{ON,rat}} \tag{3.66}$$

where the constant K_{SW} is taken from the component data sheet, and can incorporate IGBT turn-on, turn-off and diode reverse recovery losses. Second order dependency on the commutated current can also be added, if deemed necessary.

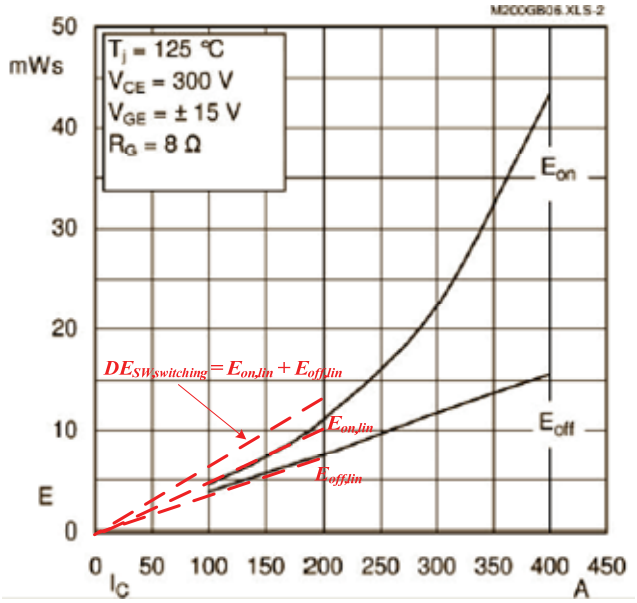


Fig. 3.11 – Switching losses. Datasheet data (Semikron SKM200GB063) and linear approximation up to the device rated current.

Conduction losses in HB-based system

Similarly to what was done to evaluate the losses in the SC banks, we will calculate losses during a constant power discharge of 75% of the initial SC energy content.

When power is transferred from the SC bank to the load side, current is flowing either through the switch S_D when the switch is ON, or through the diode D_U when the switch is OFF. According to (3.64), and looking at Fig.3.5, the energy lost during a switching period is:

$$\begin{aligned} P_{SW,cond,Tsw} &= P_{IGBT,cond} + P_{Diode,cond} \\ &= \left(V_{f,0,I} \cdot \left(1 - D_{HB}\right) \cdot I_{SC,HB} + r_{f,I} \cdot \left(1 - D_{HB}\right) \cdot I_{SC,HB}^{\ 2}\right) + \left(V_{f,0,D} \cdot D_{HB} \cdot I_{SC,HB} + r_{f,D} \cdot D_{HB} \cdot I_{SC,HB}^{\ 2}\right) \end{aligned} \tag{3.67}$$

In the equation above, we have implicitly assumed that the current is piecewise constant over the switching period; this is true if the smoothing inductance is big and the switching frequency is sufficiently high. In order to further simplify the analysis, we

will also assume the same conduction characteristics for the switch (assumed to be an IGBT) and diode, leading to:

$$P_{SW,cond,Tsw} = V_{f,0} \cdot I_{SC,HB} + r_f \cdot I_{SC,HB}^{\ 2} \tag{3.68}$$

The energy dissipated in the switches due to conduction losses over the whole discharge process is found integrating (3.68), using the expression (3.37) and (3.39) for the SC-side current and the discharge time:

$$\begin{aligned} E_{S,cond,HB} &= \int_0^{Tdis} P_{SW,cond,Tsw} dt \\ &= V_{f,0} \cdot I_{dis} \cdot T_{dis} \cdot \int_0^{Tdis} \frac{1}{\sqrt{1 - \frac{2}{C_{SC,HB}} \cdot \frac{I_{dis}}{V_{DC}} \cdot t}} dt + r_f \cdot I^2_{\ dis} \cdot T_{dis} \cdot \int_0^{Tdis} \frac{1}{1 - \frac{2}{C_{SC,HB}} \cdot \frac{I_{dis}}{V_{DC}} \cdot t} dt \\ &= \left(\frac{4}{3} \cdot V_{f,0} \cdot I_{dis} + \frac{8}{3} \ln 2 \cdot r_f \cdot I^2_{\ dis} \right) \cdot T_{dis} \end{aligned} \tag{3.69}$$

Switching losses in HB-based system

Switching losses over a complete discharge cycle at constant power are found by integrating (3.66), and considering that in the time unit there are $\frac{1}{T_{SW}} = f_{SW}$ pairs of commutations, each pair contributing to the losses with the amount $\Delta E_{SW,switching}$:

$$\begin{aligned} E_{SW,switching,HB} &= \int_0^{Tdis} \Delta E_{SW,switching} \cdot f_{SW} = f_{SW} \cdot \int_0^{Tdis} K_{SW}\left(V_{OFF,rat}, I_{ON,rat}\right) \cdot \frac{V_{DC} \cdot I_{SC,HB}(t)}{V_{OFF,rat} \cdot I_{ON,rat}} dt \\ &= \frac{4}{3} \cdot K_{SW}\left(V_{OFF,rat}, I_{ON,rat}\right) \cdot \frac{V_{DC} \cdot I_{dis}}{V_{OFF,rat} \cdot I_{ON,rat}} \cdot f_{SW} \cdot T_{dis} \end{aligned} \tag{3.70}$$

Notice that the current used in the equation above is the SC-side current, which has been assumed nearly constant over a switching period.

Conduction losses in HC-based system

The current flowing into the switches of the HC-based system is the load-side current. Similarly to the HB case, there is one and only one device conducting at any given instant. In the case of power flowing from the SC bank to the load, the switch S_U is conducting when commanded ON, while the diode D_D is conducting when the upper switch is OFF. Resulting conduction losses over a switching period are:

$$\begin{aligned} P_{SW,cond,Tsw} &= P_{IGBT,cond} + P_{Diode,cond} \\ &= \left(V_{f,0,I} \cdot D_{HC} \cdot I_{HC} + r_{f,I} \cdot D_{HC} \cdot I_{HC}^{\ 2}\right) + \left(V_{f,0,D} \cdot (1 - D_{HC}) \cdot I_{HC} + r_{f,D} \cdot (1 - D_{HC}) \cdot I_{HC}^{\ 2}\right) \end{aligned} \tag{3.71}$$

Again, we have neglected the contribution of the ripple current. If same conduction characteristics are assumed for both IGBT and diode, we get:

$$P_{SW,cond,Tsw} = V_{f,0} \cdot I_{HC} + r_f \cdot {I_{HC}}^2 \tag{3.72}$$

Integrating (3.72) over the whole discharge cycle, we get the total cycle losses due to conduction of the switches:

$$E_{S,cond,HC} = \int_0^{Tdis} P_{SW,cond,T_{SW}} dt = \left(V_{f,0} \cdot I_{dis} + r_f \cdot {I_{dis}}^2 \right) \cdot T_{dis} \tag{3.73}$$

Switching losses in HC-based system

The integration of the elementary switching losses over the whole discharge period results in:

$$E_{SW,switching,HC} = \int_0^{Tdis} \Delta E_{SW,switching} \cdot f_{SW} = f_{SW} \cdot \int_0^{Tdis} K_{SW}\left(V_{OFF,rat}, I_{ON,rat}\right) \cdot \frac{V_{SC,1}(t) \cdot I_{HC}}{V_{OFF,rat} \cdot I_{ON,rat}} dt$$

$$= f_{SW} \cdot \frac{K_{SW}\left(V_{OFF,rat}, I_{ON,rat}\right)}{V_{OFF,rat} \cdot I_{ON,rat}} \cdot I_{dis} \cdot \int_0^{Tdis} V_{SC,1}(t)\, dt$$

$$= f_{SW} \cdot \frac{K_{SW}\left(V_{OFF,rat}, I_{ON,rat}\right)}{V_{OFF,rat} \cdot I_{ON,rat}} \cdot I_{dis} \cdot V_{DC} \cdot T_{dis} \cdot \frac{1}{16}\sqrt{64 - \frac{9(x+1)^2}{x}} + \frac{4\sqrt{x}\arctan\sqrt{\frac{9(x+1)^2}{64 \cdot x - 9(x+1)^2}}}{3(x+1)} \tag{3.74}$$

Comparison of losses in the converter switches

Direct comparison of conduction losses in the switches of the two topologies is not straightforward. From (3.69) and (3.73), the ratio of conduction losses is:

$$\frac{E_{SW,cond,HC}}{E_{SW,cond,HB}} = \frac{V_{f,0,HC} + r_{f,HC} I_{dis}}{\frac{4}{3} V_{f,0,HB} + \frac{8}{3} \ln 2 \cdot r_{f,HB} I_{dis}} \tag{3.75}$$

In general, forward characteristics of the devices used in the HB-based topology are different from those of the HC-based topology, due to the different VA rating required. For the sake of comparison, we may assume that the power switches (IGBTs and diodes) are designed to have a forward voltage drop of 2.5 V at rated current, and a junction voltage of about 1.0 V:

$$\begin{aligned} V_{f,0} &= 1.0V \\ r_f \cdot I_{rat} &= 1.5V \end{aligned} \tag{3.76}$$

If a current rating equal to $I_{rat} = 2I_{dis}$, (minimum needed in case of the HB topology) is used for the devices in both topologies, the loss ratio in (3.75) becomes:

$$\left(\frac{E_{SW,cond,HC}}{E_{SW,cond,HB}} \right)_{same\ switch\ rating} = \frac{1.0 + 0.75}{\frac{4}{3} + \frac{8}{3} \ln 2 \cdot 0.75} = 0.64 \tag{3.77}$$

That means, 36% reduction of the conduction losses is possible by using the HC-based topology, if the same solid state switches are deployed.

Perhaps a more interesting comparison is when the solid state devices are optimized in both topologies, leading to a current rating of the switches in HC that is half of the one in HB. In this case, the conduction loss ratio becomes:

$$\left(\frac{E_{SW,cond,HC}}{E_{SW,cond,HB}}\right)_{optimized\ switches} = \frac{1.0+1.5}{\frac{4}{3}+\frac{8}{3}\ln 2 \cdot 0.75} = 0.92 \tag{3.78}$$

The result above is quite remarkable, since it shows that 8% reduction of conduction losses is achieved by the HC topology, even if switches having half of the current capability (and therefore double differential resistance, according to (3.76)) are used.
The ratio of switching losses between the two topologies is readily evaluated from (3.70) and (3.74). Such a ratio is only slightly dependent on the capacitance ratio used in the HC converter, as it is shown in Fig.3.12.

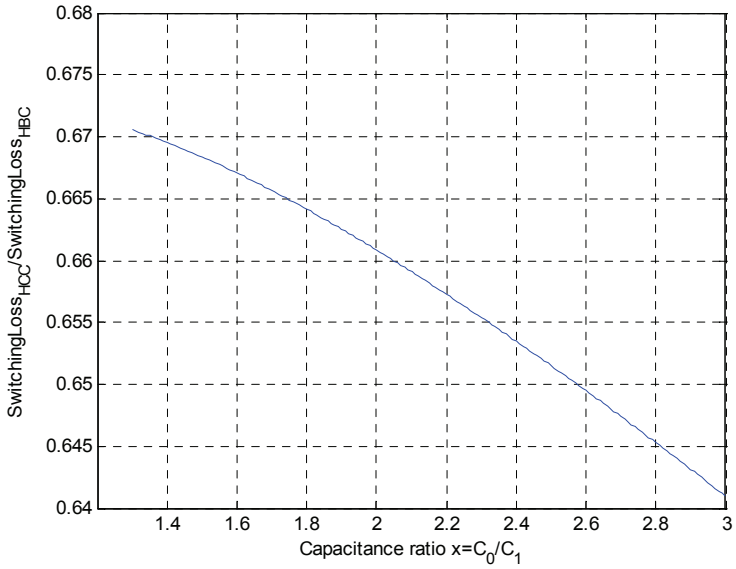


Fig. 3.12 – Relative switching losses of HC as compared to HB.

In the figure, it is assumed that the same device is used in both topologies, leading to about 34% reduction of switching losses in the HC-based system. If different switches are used, the switching loss figure from the datasheet has to be used in order to evaluate the actual ratio.

3.4.3 Losses in the smoothing inductor

In either system of Fig.3.4, the inductor is designed so to have a relatively small current ripple, in order to avoid unnecessary losses in the battery (HC-system) or in the supercapacitors (HB system). Copper losses in the inductors can therefore be evaluated by considering a ripple-free inductor current:

$$E_{L,Cu,HB} = \int_0^{Tdis} \left(R_{L,HB} \cdot {I_{SC,HB}}^2\right) dt = \frac{8}{3}\ln 2 \cdot R_{L,HB} \cdot {I_{dis}}^2 \cdot T_{dis} \tag{3.79}$$

$$E_{L,Cu,HC} = \int_0^{Tdis} \left(R_{L,HC} \cdot {I_{HC}}^2\right) dt = R_{L,HC} \cdot {I_{dis}}^2 \cdot T_{dis} \tag{3.80}$$

Note: The ripple current component will generate losses according to the AC resistance of the winding that can in general be much higher than the DC resistance used in (3.79) and (3.80); if care is not taken in designing the windings for the operating switching frequency (for instance by using thin copper foils as conductors), even a small AC current ripple can still give rise to unacceptable copper losses.

Core losses in the inductor can be divided into hysteresis and Eddy current losses, and are only due to the ripple component of the current (and consequently of the flux density). Exact calculation of such losses is quite complex and can be found in many classical textbooks, like for instance [79]. It is however common engineering practice to evaluate the AC component of the flux density B_{ac} in the core due to the ripple current excitation for a given physical construction of the inductor, and then use loss figures $P_c\left(W/kg\right)$ given by the core manufacturer as function of the AC flux density and excitation frequency to find the total losses in the core. Obviously, such approach is difficult to generalize and losses have to be evaluated case-by-case.
Even if approximated mathematical relationships are used to express core losses as function of AC flux density and ripple frequency, of the form:

$$P_{c,tot} = k_{core} \cdot {f_{SW}}^{a} \cdot {B_{ac}}^{b} \tag{3.81}$$

with k_{core}, a, b being real constants depending on the particular core in use, comparison of core losses in the two inductors found in HB-based and HC-based systems is not immediate. This is because the designs are subject to very different constraints in terms of peak current that the inductor has to withstand, as it is stated by (3.37) and (3.43). As a result, the only thing that can be positively concluded is that in order to obtain the same ripple current, the inductor needed in the HC-based system will be much smaller than the one needed in the HB-based system, since the peak current requirement is halved. How this will influence losses is not obvious and must be evaluated for each specific design. An example is given in section 5.2.2.

3.4.4 Losses in the electrolytic capacitor

In the two systems of Fig.3.4, an electrolytic capacitor is used to smooth the current on the high-voltage side of the half bridge. The capacitor is in parallel with the battery in HB-based system and with the upper SC bank in HC-based system; here it is assumed that the ESR of the capacitor is always much lower than the one of the device in parallel with it, so that the whole ripple current is handled by the electrolytic, as shown in Fig.3.5 and Fig.3.6. The internal resistance of the electrolytic is also assumed constant over the frequency range of interest.
For the capacitor in the HB-based system, by direct calculation of local *rms* value applied to (3.42) and assuming the inductor current to be almost constant over the switching period, we calculate:

$$\begin{aligned} E_{Cel,HB} &= \int_0^{T_{dis}} \left({I_{Cel,rms}}^2 \cdot ESR_{Cel,HB} \right) dt \\ &= ESR_{Cel,HB} \cdot \int_0^{T_{dis}} \frac{1}{T_{SW}} \cdot \left(\int_0^{DT_{SW}} \left(I_{SC}(\tau) - I_{dis} \right)^2 d\tau + \int_{DT_{SW}}^{T_{SW}} \left(-I_{dis} \right)^2 d\tau \right) dt \\ &= ESR_{Cel,HB} \cdot {I_{dis}}^2 \cdot \int_0^{T_{dis}} \frac{(1-D)}{D} dt = \frac{1}{3} ESR_{Cel} \cdot {I_{dis}}^2 \cdot T_{dis} \end{aligned} \tag{3.82}$$

Similarly, for the capacitor in the HC-based system we can use (3.52) to calculate the losses over a complete discharge cycle:

$$\begin{aligned} E_{Cel,HC} &= \int_0^{T_{dis}} \left({I_{Cel,HC,rms}}^2 \cdot ESR_{Cel,HC} \right) dt \\ &= ESR_{Cel,HC} \cdot \int_0^{T_{dis}} \frac{1}{T_{SW}} \cdot \left(\int_0^{DT_{SW}} \left(I_{dis} - I_{SC,1}(\tau) \right)^2 d\tau + \int_{DT_{SW}}^{T_{SW}} \left(-I_{SC,1} \right)^2 d\tau \right) dt \\ &= ESR_{Cel,HC} \cdot {I_{dis}}^2 \cdot \int_0^{T_{dis}} \left(D_{HC} \cdot (1 - D_{HC}) \right) dt \end{aligned} \tag{3.83}$$

The integral above can be solved analytically, but the solution is not reported here, since it is unnecessarily complex. Instead, it is informative to look at the ratio of the capacitor losses between the two systems:

$$\rho_{Cel} = \frac{E_{Cel,HC}}{E_{Cel,HB}} \tag{3.84}$$

Such a ratio is reported in Fig.3.13, having assumed the same ESR for the capacitor in the two systems.

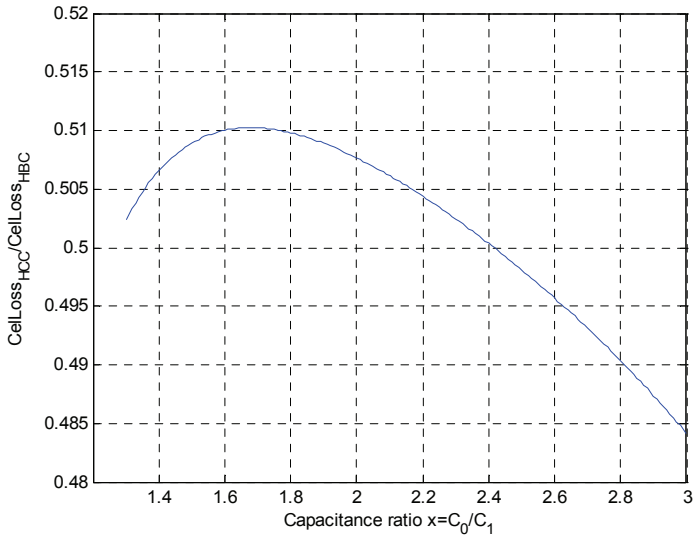


Fig. 3.13 – Relative losses in the electrolytic capacitor.

The figure shows that losses are approximately half in the HC-based system, with very little effect of the capacitance ratio used in the design.
In DC-DC converter applications, the amount of capacitance used for smoothing is often determined based on allowed losses in the capacitor itself due to the ripple current; this criteria is in fact more stringent than the requirements on the allowable voltage ripple, at least if electrolytic capacitors are used [1]. That means that a smaller capacitor (double ESR for the same rated voltage, to get the same losses) could be used in the HC-system, to keep the same loss level of the HB-system, without significantly affecting the filtering performance.

3.5 Generalized equations of HC system for optimal design

The main reason for the proposal of the HC-based system is the minimization, in terms of size and cost, of the power electronics converter used to control the power flow between a load supplied by a main battery and a power buffer based on supercapacitors.
In section 3.1, the voltage constraint (3.17) has been used to develop a system whose converter features switches having half VA rating compared to a standard solution. However, while the voltage of the uncontrolled SC bank has the upper bound equal to (3.17) dictated by the topology itself, there is no obvious reason why the voltage rating of the controlled SC bank cannot be higher than the battery voltage. In the previous section, that voltage limitation has been introduced in order to get the same voltage rating for the switching devices used in the HC-system and in the HB-system. It is however interesting to look at the consequences of allowing higher voltage across the controlled SC bank.
With the introduction of the additional degree of freedom given by $v_{SC,1,Max}$, the maximum voltage allowed across the controlled bank normalized to the battery voltage, it is necessary to extend the concept of "equivalent HB-based system". The principle of equal amount of stored energy given in (3.26) leads to the following relationship between the capacitances of the banks:

$$C_{SC,HB} = C_{SC,0} + C_{SC,1} \cdot v_{SC,1,\max}^2 \tag{3.85}$$

The equation above, together with the definition of the capacitance ratio in (3.18) yields:

$$C_{SC,HB} = C_{SC,0} \cdot \left(1 + \frac{v_{1,Max}{}^2}{x}\right) = C_{SC,1} \cdot \left(x + v_{1,Max}{}^2\right) \tag{3.86}$$

With the assumption of constant Ohm-Farad product, inverse relationships hold for the ESR of the banks.
The generalized expression for the energy utilization ratio in (3.22) becomes:

$$\rho_E = \frac{E_{SC,tot,cycle}}{E_{SC,tot,Max}} = 1 - \frac{x(x+1) + x\left(v_{SC,1,Max}{}^2 - 2v_{SC,1,Max}\sqrt{x+1}\right) + v_{SC,1,Max}{}^2}{(x+1)\left(x + v_{SC,1,Max}{}^2\right)} \tag{3.87}$$

For any given value of the bank rated voltage, it is possible to find the capacitance ratio that maximizes the energy utilization ratio:

$$x_{opt} = \frac{v_{SC,1,Max} \cdot \left(1 + \sqrt{v_{SC,1,Max}{}^2 + 8}\right)}{2} \tag{3.88}$$

If the capacitance ratio is chosen according to (3.88), the resulting optimized energy extraction is only a function of the rated voltage of the controlled SC bank, as shown in Fig.3.14

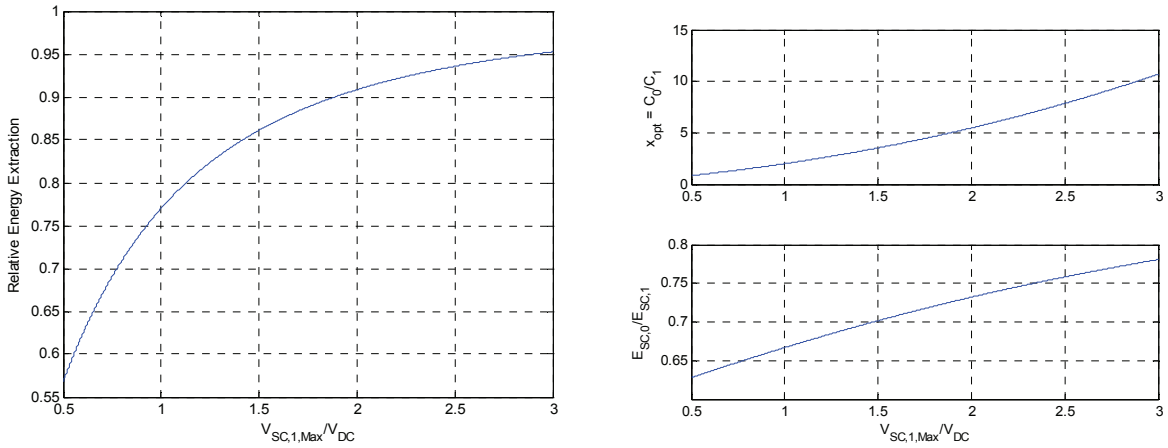


Fig. 3.14 – Optimal energy utilization in generalized HC-based system.

Another interesting aspect to be evaluated is the VA rating of the solid state switches needed to implement the HC-based system with generalized voltage rating of the controlled SC bank, as compared to the equivalent HB-based system. Following the same line of reasoning as in section 3.3.1, we can write:

$$\frac{S_{SW,HC}}{S_{SW,HB}} = \frac{v_{SC,1,Max} \cdot V_{DC} \cdot I_{dis}}{V_{DC} \cdot \frac{I_{dis}}{\sqrt{1-\rho_E}}} = v_{SC,1,Max} \cdot \sqrt{1-\rho_E} \tag{3.89}$$

If, for simplicity, we assume to use a capacitance ratio close to the one that maximizes the energy utilization, we can then substitute (3.88) into (3.89), eliminating the dependency on x and obtaining the ratio of the converter switches VA rating as a function of the voltage across the controlled SC bank, resulting in the curve of Fig.3.15.

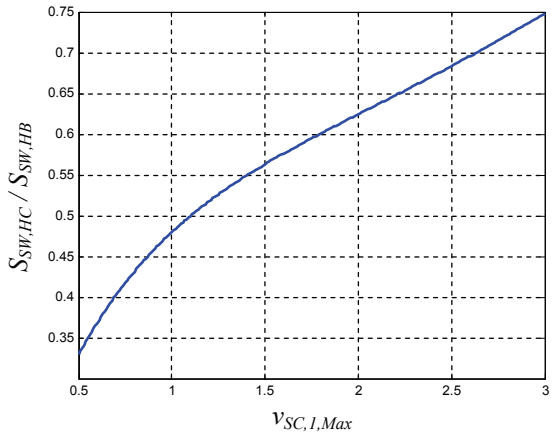


Fig. 3.15 – Relative VA rating of switches in generalized HC-based system.

Combining the results in Fig.3.14 and Fig.3.15, we can draw the following conclusions: By increasing the voltage rating of the "controlled" SC bank, it is possible to increase the percentage of energy contained in the SC banks that can actually be transferred to the load; however, at the same time, the VA rating of the required switches increases and approaches the VA rating of switches utilized in the equivalent HB-based system.

Normalized voltage ratings smaller than unity lead to poor energy utilization, and should therefore be avoided;
Normalized voltage rating higher than unity reduces the main advantage of HC-system of using considerably smaller solid state devices, making the solution less attractive. Increasing $v_{SC,1,Max}$ has also the undesirable effect of increasing the number of elementary SC cells to be series connected to form the bank.
In addition to the energy utilization capability and the reduction of the VA rating of the switches, it is also important to understand how the system efficiency is affected by a change in voltage rating of the controlled SC bank.
Similarly to what was done in section 3.4.1, the losses in the SC banks of the generalized HC-based system are compared to those of the single SC-bank in the equivalent HB-based system, by the definition of the loss ratio:

$$\rho_{E_{SC}} = \frac{E_{SC,HC}}{E_{SC,HB}} \tag{3.90}$$

The normalized loss distribution among the two SC banks of the HC system originally defined in (3.62) can also be generalized as:

$$\rho_{SC\_loss} = \frac{v_{SC,1,Max}^{\ 2} \cdot E_{SC,0}}{x \cdot E_{SC,1}} \tag{3.91}$$

Analytical details are omitted, since they are similar to those presented in the case of unity rated voltage, but it should be clear that now both $\rho_{E_{SC}}$ and ρ_{SC_loss} are a function of two design parameters $v_{SC,1,Max}$ and x.
Instead of giving 3D maps of the resulting loss ratios for any possible combination of the design parameters, which would certainly look fancy but would perhaps be of limited practical utility, we will concentrate on two particular values of $v_{SC,1,Max}$ and look at how the characteristics of the system evolve.

Case study 1: $v_{SC,1,Max} = 1.5$

According to (3.87), the energy utilization ratio can be expressed as a function of the remaining design parameter x, as shown in Fig.3.16. As expected, increasing the rated voltage of the upper bank leads to the possibility of using a bigger fraction of the total energy available in the SC buffer. In this particular case, more than 84% of the available energy can be transferred to the load for capacitance ratios between 2.4 and 5.2.
The loss ratio in (3.90) is evaluated for different discharge cycles at constant power and reported in Fig.3.16. The green line represents the loss ratio over a deep discharge cycle (84% of the initial SC energy transferred to the load), while the blue line is the loss ratio over a shallow discharge cycle (75% of the initial SC energy transferred to the load). It is apparent that, similarly to what was found in the base case of $v_{SC,1,Max} = 1.0$, losses in the SC banks of the HC-based system are always slightly higher than those of the equivalent HB-based system. Moreover, the loss ratio does not vary much if the cycle depth is changed.
In Fig.3.16, the loss distribution among the two SC bank of the HC-based system given by (3.91) is plotted, for deep and shallow discharge cycles at constant power. What is of

significance is that by designing with a capacitance ratio corresponding to good energy utilization and low SC losses will not necessarily balance losses among the two banks.
In this case study, a capacitance ratio around 4.5 would seem appropriate. According to (3.89), such a design will give a relative VA rating of the switches equal to about 0.58. If the system has to undergo deep cycles, particular care must be taken that the temperature of the SC cells of the controlled SC bank does not exceed safe operating limits.

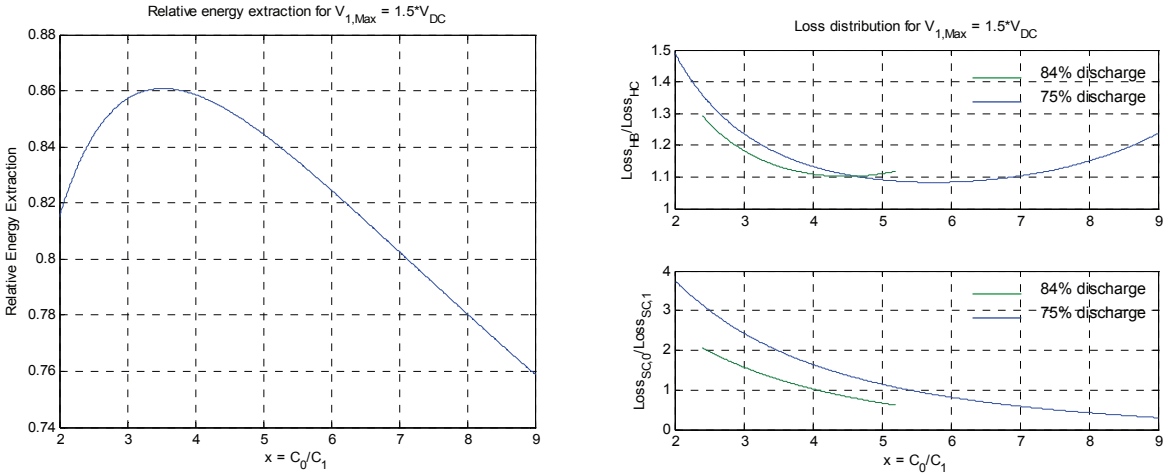


Fig. 3.16 – Characteristics of generalized HC-based system with $v_{1,SC,Max} = 1.5$.

Case study 2: $v_{SC,1,Max} = 2.0$

Energy utilization and loss figures for this case study resulting from deep (89%) and shallow (75%) discharge cycles at constant power are given in Fig.3.17. A good design value for the capacitance ratio would be around 7.0, yielding a relative energy extraction of approximately 90% and reasonable losses for either kind of cycle. The problem of unbalanced losses in the two banks of the SC system is getting worse with increasing $v_{SC,1,Max}$, and is quite hard to get a thermally balanced system, since the stress on the two banks is very dependent on the depth of the cycle.
The switches necessary to implement the topology gets more similar to those of an equivalent HB-based system, the normalized VA ratio being about 0.63.

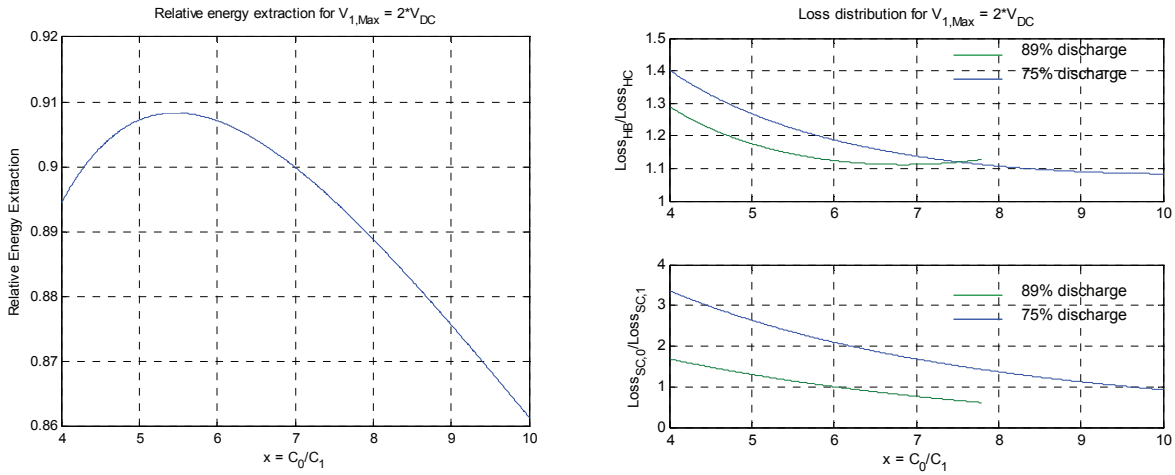


Fig. 3.17 – Characteristics of generalized HC-based system with $v_{1,SC,Max} = 2.0$.

From the arguments above, it looks that the only advantage of increasing the voltage rating of the controlled SC bank beyond the battery voltage is the increased relative energy extraction that can be achieved. However, this comes with the cost of increasing the necessary VA rating of the switches. The situation is somehow similar to the HB-based system: increases energy cycling capabilities are possible if the current rating of the switches is increased. But the fact that HB-based systems are seldom designed to harvest more than 75% of the SC energy at rated power is not only because of the bigger switches that would be necessary, but mainly because utilizing the remaining bit of energy in the SC buffer has very little sense, as explained in the following.

3.5.1 Ideal limit for the utilization of the SC energy

One of the main reasons why an SC-based power buffer is used in conjunction with a battery is to increase the overall system efficiency. If the *ESR* of the SC bank used in a standard HB-based system is equal to $ESR_{SC,HB}$, than at a given SOC of the bank, the incremental losses in the SCs are:

$$dE_{SC} = I_{SC}{}^2 \cdot ESR_{SC,HB} \cdot dt = \left(ESR_{SC,HB} \cdot \frac{V_{DC}{}^2}{V_{SC}{}^2} \right) \cdot I_{dis}{}^2 \cdot dt = ESR_{SC,HB,eq} \cdot I_{dis}{}^2 \cdot dt \qquad (3.92)$$

An obvious result is that the incremental losses increase as the bank voltage decreases. According to (3.92), discharging the SC bank gives rise to the same losses that would result from a stiff voltage source (battery) having an internal resistance equal to $ESR_{SC,HB,eq}$. Obviously, there will be a point at which $ESR_{SC,HB,eq}$ will become equal to the actual internal resistance of the battery in use on the load-side of the power buffer; from that point on, trying to extract energy from the SC buffer will result in more losses than taking the energy directly from the battery. The breakeven point is:

$$ESR_{DC} = ESR_{SC,HB,eq} \Rightarrow \frac{V_{SC,\min}}{V_{DC}} = \sqrt{\frac{ESR_{SC,HB}}{ESR_{DC}}} \Rightarrow \rho_{E,Max} = 1 - \frac{ESR_{SC,HB}}{ESR_{DC}} \qquad (3.93)$$

For instance, if the battery has an internal resistance that is five times the *ESR* of the SC bank, the minimum voltage to be allowed is about 45% of the battery voltage, corresponding to an energy utilization of 80%. In practice, due to the converter losses, the breakeven condition is reached for a higher voltage (lower energy utilization) than the one predicted by (3.93).

In HC-based system the energy utilization is improved by increasing $v_{SC,1,Max}$. Following the same line of reasoning as above, we can define the equivalent internal resistance of each SC bank, as a function of the bank voltages:

$$\begin{aligned} ESR_{HC,SC0,eq} &= ESR_{SC,0} \\ ESR_{HC,SC1,eq} &= ESR_{SC,1} \cdot \left(\frac{v_{SC,0} - 1}{v_{SC,1}} \right)^2 \end{aligned} \qquad (3.94)$$

While the equivalent *ESR* of the uncontrolled SC bank is constant throughout the cycling and equal to the physical *ESR* of the bank, the controlled bank has an increasing ESR with the depth of discharge. This is the reason why, similarly to the HB-based

system, increasing the energy extraction leads to decreased efficiency. Fig.3.16 and Fig.3.17 show that the loss increase is in the same order of the loss increase in HB-based systems and is therefore reasonable to conclude that from the point of view of efficiency, even for the HC-based system, increasing the energy extraction beyond the limit determined by (3.93) is detrimental.

4 ISSUES FOR ACTUAL CONVERTER IMPLEMENTATION

The operating principle and governing equations of the proposed converter presented in the previous chapter have been based on the assumption of ideal components. Even the loss analysis was performed starting from the voltage and current waveforms calculated under ideal conditions. In this chapter, the effect of losses on the operation of the converter is clarified, and countermeasures are presented.

4.1 The Effect of Losses on Converter Operation

Several sources of losses have been identified in section 3.4. A detailed analysis including all those losses will easily lead to equations that are difficult to handle and is therefore ruled out. The effect of non ideal components can be best understood by running a detailed simulation of the system and compare the results with the ideal case of chapter 3. To this aim, the simulation model shown in Fig. 4.1 has been implemented in Matlab-Simulink® [13].

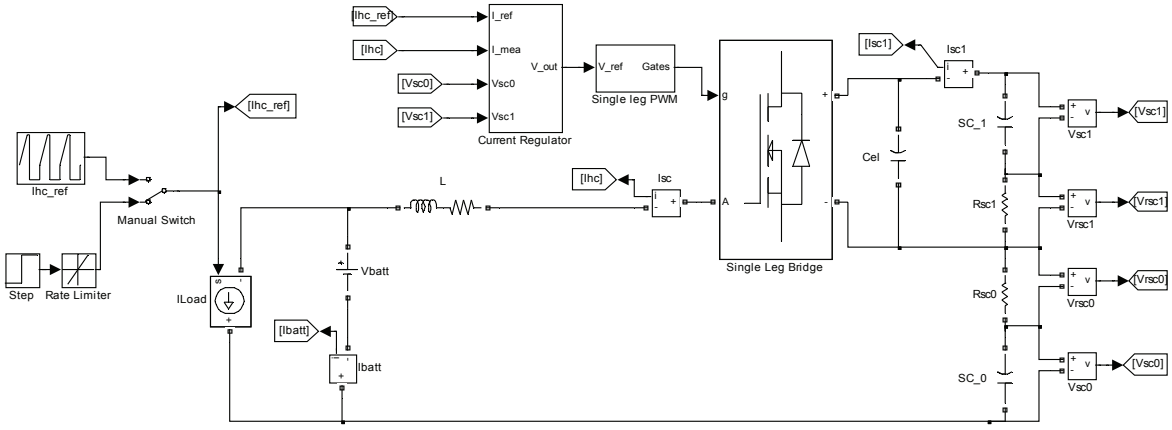


Fig. 4.1 – Simulink model of the HC-based power buffer

In the model, *ESR* of each SC bank is made explicit, while the parameters of the block "Single Leg Bridge" allow for simulation of conduction losses in the semiconductor switches. Copper losses in the inductor are included by means of a series resistance R_{Cu}.

Core losses in the inductor cannot be modelled by a simple resistance in series with the main current flow; however, since the ripple current is by design small, so will be the ripple on the magnetic flux density in the core, which is responsible of such losses. For that reason, the effect of core losses is not included in the simulation.
Losses in the electrolytic capacitor are assumed to be small, and are expected to have negligible effect on system performance; they are not included in the simulation.
Switching losses in the semiconductor switches are not included in the model, either, since they are not expected to give a major contribution to the overall system losses. If necessary, the model can be refined to include all the sources of losses.
An actual case study relating the order of magnitude of each component of the losses is reported in section 5.4.3.
All the relevant parameters of the simulated system are reported in Table 4-1. Notice that the capacitance ratio of the system is $x = 2.3$, and the constant Ohm-Farad product principle has been applied. Equivalent resistance of the components are selected in order to have an ideal efficiency of about 95% over a complete constant power discharge at rated power, which is a reasonable value in practice.

Table 4-1 – Main parameters of simulated HC-based power buffer.

Battery Voltage	240 V
Uncontrolled SC bank (SC0)	5.0 F, 240 V, ESR = 68 $m\Omega$
Controlled SC bank (SC1)	2.17 F, 240 V, ESR = 156 $m\Omega$
Smoothing Inductor	1.0 mH (f_{SW} = 10 kHz), R_{Cu} = 2.5 $m\Omega$
Converter Switches	$R_{f,D} = R_{f,IGBT}$ = 16 $m\Omega$
Constant power discharge:	30 kW (125 A at 240 V)

The time needed to discharge 75% of the initial SC energy in the case of an ideal system is calculated from (3.49) as:

$$T_{dis,75} = 5.16\,s \tag{4.1}$$

Trying to force a discharge current of rated value for the time calculated above, results in the situation of Fig.4.2. The following important characteristics can be deduced:

- Energy utilization capability is reduced to about 70.5% from an ideal value calculated by (3.22) of about 76.5%. Current controllability is lost if trying to extract more energy from the buffer.
- The voltage distribution among the two banks deviates from the basic ideal relationship in (3.20).

In order to explain the simulation results, let us consider the simplified equivalent circuit of the system in the two possible switching states shown in Fig.4.3.

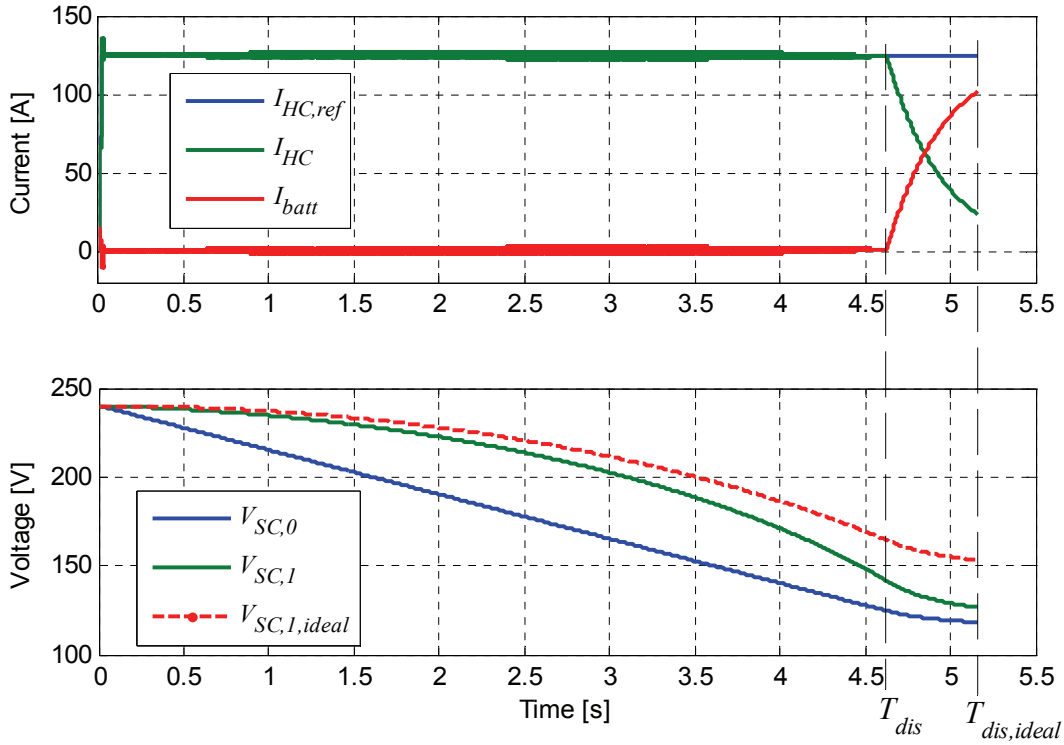


Fig. 4.2 – Simulation of HC-based power buffer for rated power discharge, including effect of losses.

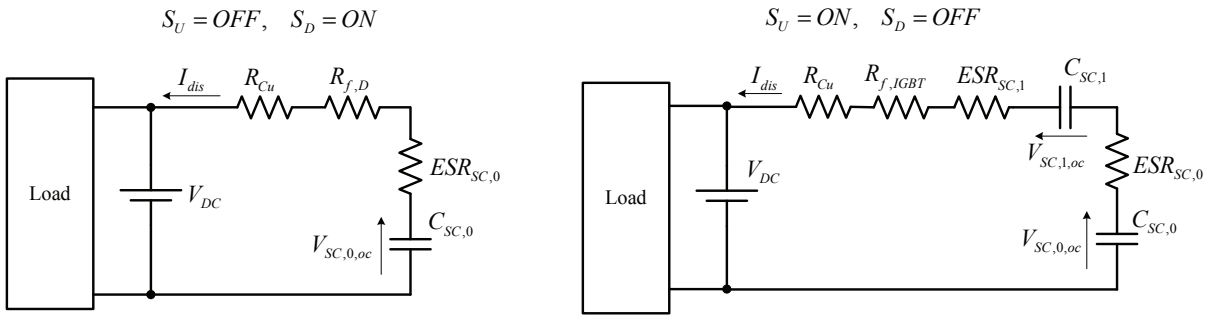


Fig. 4.3 – Equivalent circuit of HC-based power buffer for the two possible switching states.

Under the simplifying but reasonable assumption of $R_{f,D} \approx R_{f,IGBT}$, we can conclude that both the inductor resistance and the semiconductor static on-state resistance are effectively in series with the ESR of the uncontrolled SC bank, regardless of the switching state. Let us then define the new equivalent resistances:

$$\begin{aligned} R_{0,eq} &= R_{Cu} + R_f + ESR_{SC,0} \\ R_{1,eq} &= ESR_{SC,1} \end{aligned} \tag{4.2}$$

The voltage balance defined by (3.1) with the sign of equality, indicating the lower limit of discharge, in case of current flowing into non-ideal supercapacitors is rewritten as:

$$V_{SC,0,oc} + V_{SC,1,oc} = V_{DC} + \left(R_{0,eq} + R_{1,eq}\right) \cdot I_{dis} \tag{4.3}$$

$V_{SC,0,oc}$ and $V_{SC,1,oc}$ are the open circuit voltages across each SC bank. Obviously, the higher the discharge current, the higher must be the sum of the bank voltages at the end of discharge, meaning that more energy will remain in the buffer that cannot be transferred to the load. An exact solution of (4.3) is difficult to find, but a good first order estimation can be obtained by assuming (3.20) to be still valid. With the values in Table 4-1, this results in:

$$v_{SC,0,\min} = 0.486, \quad v_{SC,0,\min} = 0.627 \quad \Rightarrow \quad \rho_E \approx 0.717 \tag{4.4}$$

This result is in good agreement with the simulation.
The fact that the voltage across the two banks does not follow the ideal trajectory in (3.20), means that actual losses in the SC banks will be different from the value calculated by (3.56). In particular, the energy lost in the uncontrolled SC bank during discharge is the same as calculated assuming ideal waveforms, since the current $I_{SC,0}$ is indeed constant, due the action of the current controller; however, the current $I_{SC,1}$ does not follow the equation (3.47), because the duty cycle is different from (3.46), due to the voltage drop over the internal resistances of the SC banks.
When current is flowing, the voltage balance (3.9) must still be satisfied, leading to:

$$D_{HC} = \frac{V_{DC} - V_{SC,0,oc} + R_{0,eq} \cdot I_{dis}}{V_{SC,1,oc} - R_{1,eq} \cdot \left(D_{HC} \cdot I_{dis} \right)} \tag{4.5}$$

Comparing (3.46) with (4.5), it is easy to recognize that during a discharge process it is always $D_{HC} > D_{HC,ideal}$ and, as a consequence, $I_{SC,1} > I_{SC,1,ideal}$. The losses in the controlled SC bank given by (3.56) are therefore underestimated. In principle, it is possible to calculate the exact duty cycle during discharge from (4.5), and then calculate the losses. However, this will lead to complicated equations that are difficult to solve in parametric closed form. We can instead modify (4.5) as follows:

$$\begin{aligned} D_{HC} &\approx D_{HC,ideal} + \underbrace{\left({D_{HC,ideal}}^2 \cdot \frac{ESR_{SC,1} \cdot I_{dis}}{V_{SC,1,oc}} + \frac{ESR_{SC,0} \cdot I_{dis}}{V_{SC,1,oc}} \right)}_{\Delta D_{HC}} \\ D_{HC,ideal} &= \frac{V_{DC} - V_{SC,0,oc}}{V_{SC,1,oc}} \end{aligned} \tag{4.6}$$

In the derivation above we have made use of the approximations:

$$\begin{aligned} &V_{SC,0,oc} \ll ESR_{SC,0} \cdot I_{dis} \\ &V_{SC,1,oc} \gg ESR_{SC,1} \cdot I_{dis} \\ &\frac{1}{1-k} \approx 1 + k, \qquad |k| \ll 1 \end{aligned} \tag{4.7}$$

The losses in the controlled SC bank can then be evaluated as:

$$E_{SC,1} \approx ESR_{SC,1} \cdot \int_0^{T_{dis}} \left(D_{HC,ideal} + \Delta D_{HC} \right)^2 I_{dis}{}^2 dt$$
$$\approx E_{SC,1,ideal} + ESR_{SC,1} \cdot I_{dis}{}^2 \cdot \int_0^{T_{dis}} 2 \left(D_{HC,ideal} \cdot \Delta D_{HC} \right) dt \quad (4.8)$$

It should be pointed out that in (4.6) the voltages across the SC banks are in principle unknown, and do not follow the ideal relation in (3.20). However, in order to calculate a reasonable estimation of the correction term for the losses, we can still assume such a relationship to hold, leading to a closed form solution for (4.8). Since in reality during discharge the voltage across the controlled bank is always lower than its ideal value, the losses calculated by (4.8) will still be a defective estimation.
Figure 4.4 shows the difference between the calculated losses and the actual (simulated) ones. It is noticed how the losses in the controlled SC bank are severely underestimated towards the end of the discharge cycle by using ideal waveforms; the error can reach about 39% for a 95% efficient discharge cycle. A more accurate value of the losses is obtained by applying the correction given in (4.8), even though the maximum error is still quite high (20%). Better approximations can be devised, but the increasing analytical complexity makes them not much easier to use than the results of a detailed simulation.

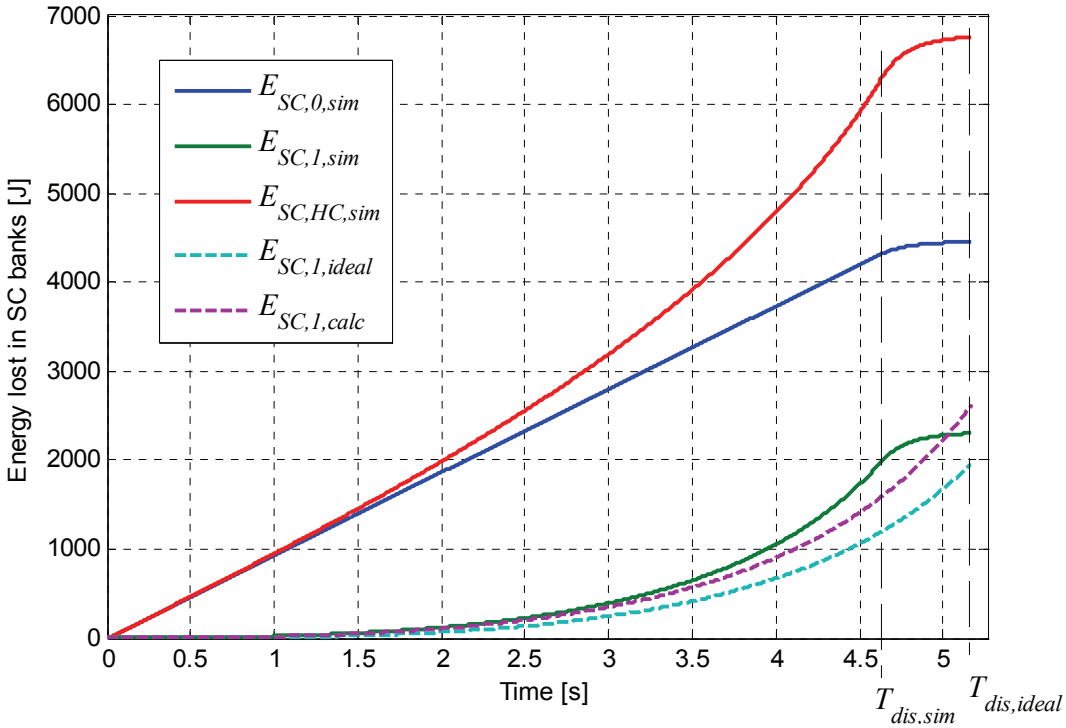


Fig. 4.4 – Energy lost in the SC banks during a complete discharge at constant power.

From the results of this investigation, one could be tempted to conclude that all the considerations about losses made in Chapter 3 are severely hindered by the large error introduced by the assumption of ideal voltage and current waveforms. However, 39% underestimation of losses in the controlled SC bank reflects in only 12% underestimation of the total SC losses for the system under study.
Furthermore, the underestimation of losses also occurs in the equivalent HB-based system, due to a similar phenomenon. It can be verified by simulation that for the same

constant power discharge here presented, losses in the SC bank of the equivalent HB-based system are about 15% higher than what is estimated by (3.54) at the end of discharge, defined as the point when constant power can no longer be delivered to the load due to reached current limitation on the SC-side. The comparison between the two idealized systems reflects therefore what would happen in the actual case where losses are present in both systems.
Since in the HC-based system only the losses in the controlled SC bank are grossly underestimated, it is reasonable to think that the sharing between the two banks does not follow the trend predicted by (3.62) and reported in Fig.3.9. Although that is true, the fact that complete discharge is no longer possible eases the stress on the controlled bank, which is concentrated towards the end of the cycle, somehow balancing the underestimation of losses; from the simulation results the actual normalized ratio of the individual bank losses can be evaluated as $\rho_{SC,loss,actual} = 0.96$. Such a value is not too far from the theoretical value $\rho_{SC,loss,ideal} = 1.08$, calculated according to (3.62).

4.2 Dynamic Voltage Balancing

So far, we have seen that the presence of losses reduces the amount of energy that can be extracted from the SC buffer during a discharge process. However, since losses are non conservative and acts always against any attempt to transfer energy in and out the SC bank, the same reduction effect also arises during a charging process: we are able to put into the SC buffer less than the maximum amount of energy that the buffer can ideally contain. Stated in other terms more related to the topology, the voltage across the controlled SC bank will always tend to drift away from its ideal trajectory, regardless of the direction of the power flow.
This phenomenon is clearly shown by the simulation result in Fig.4.5, where the system is cycled at rated power between the practical voltage limits defined by (3.1) and (3.2). In this particular simulation, the amount of capacitance has been reduced by a factor of 5 with respect to the values in Table 4-1, in order to speed-up the simulation. For the same reason, all the resistances has been scaled down by only a factor of 1.67, resulting in a much less efficient system than the original one, thus amplifying the voltage drift.
As expected from the previous arguments, the controlled SC bank tends to be discharged over time, with eventual lost of energy cycling capability. After some time, all the SC energy will be "trapped" into the uncontrolled SC bank, with no possibility of transferring it to the load. In a well designed system losses will be lower than in this limit case, and the drift phenomenon will take longer to occur, but it will eventually and inexorably take place, leading to the disappointing conclusion that the system cannot be used as it is, in practice.
The solution is to use an additional circuit that can transfer energy from the uncontrolled SC bank to the controlled one, so that the ideal voltage relationship stated in (3.20) is ensured throughout cycling. Ideally, such a system should not contribute to losses and should therefore be made out of non-dissipative components.
Fig.4.6 shows the circuit used for dynamic balancing. The topology was first proposed in [80] for lossless equalization of the voltage across individual SC cells, but its application can be easily extended to SC banks.

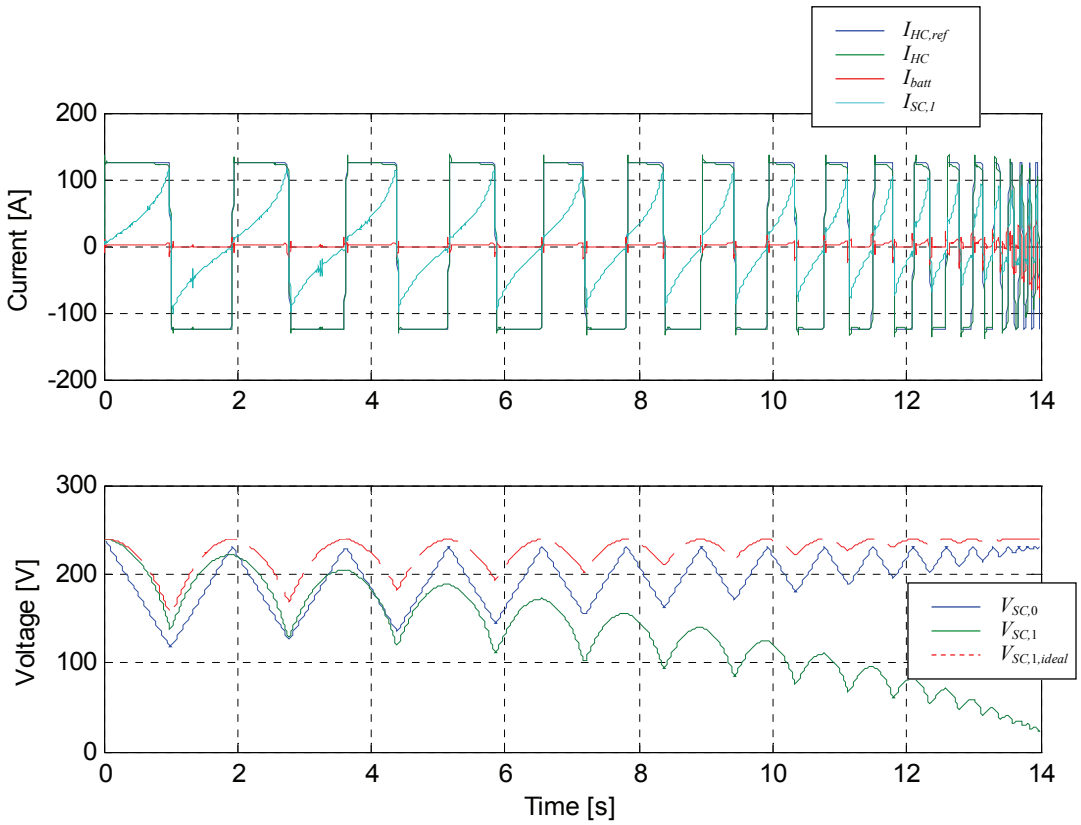


Fig. 4.5 – Cycling characteristics of the HC-based power buffer in presence of losses.

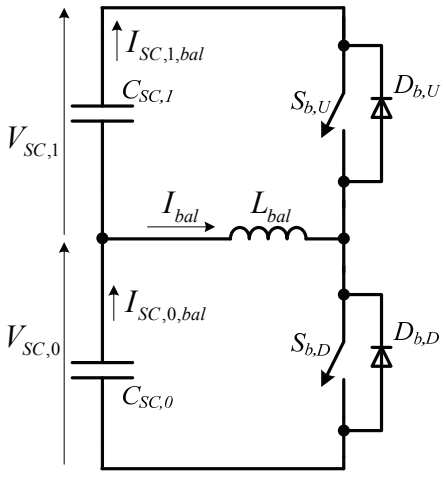


Fig. 4.6 – Loss-less dynamic balancing circuit.

With the current direction as in the figure, energy is transferred from the lower SC bank to the upper SC bank. According to the results above, that should always be the case during cycling, making the pair $S_{b,D}$, $D_{b,U}$ not strictly necessary. The simplified waveforms of the balancing circuit are reported in Fig. 4.7.

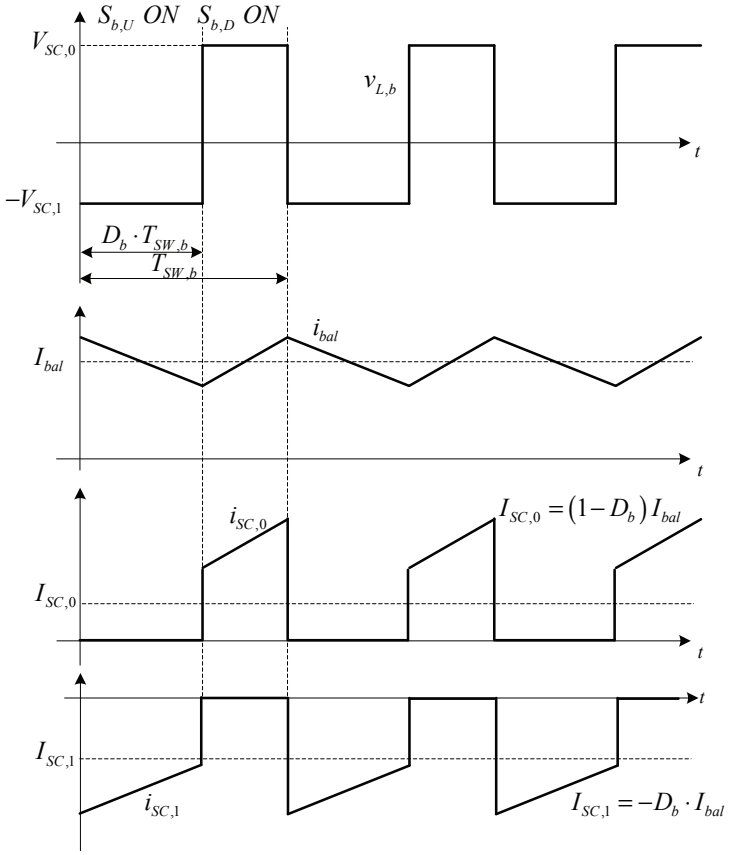


Fig. 4.7 – Balancing circuit waveforms under dynamic steady state.

When current is flowing in the inductor, the voltage changes across each SC bank over a switching period according to:

$$\begin{aligned} \Delta V_{SC,0} &= -\frac{1}{C_{SC,0}}(1-D_b) I_{bal} \cdot T_{SW,b} \\ \Delta V_{SC,1} &= \frac{1}{C_{SC,1}} D_b \cdot I_{bal} \cdot T_{SW,b} \end{aligned} \tag{4.9}$$

The resulting balancing action is therefore given by:

$$\Delta V_{SC,1} - \Delta V_{SC,0} = \left(\frac{D_b}{C_{SC,1}} + \frac{1-D_b}{C_{SC,0}} \right) I_{bal} \cdot T_{SW,b} = \frac{1}{C_{SC,0}} \cdot \left(1 + (x-1) D_b\right) \cdot I_{bal} \cdot T_{SW,b} \tag{4.10}$$

In dynamic steady state, the duty cycle of the balancing circuit can be expressed as:

$$D_b = \frac{V_{SC,0}}{V_{SC,0} + V_{SC,1}} \tag{4.11}$$

showing that there is a non-linear relationship between the balancing current and the voltage changes. In particular, since the voltage dynamics is slow compared to the switching period, (4.10) can be seen as an integrator with variable gain as the duty cycle varies between zero and unity. The gain variation is related to the capacitance ratio x.

A simple control system that keeps the voltage balancing according to the ideal relationship (3.20) is shown in Fig. 4.8. The inner PI-based loop controls the balancing current to a reference value that is defined by an external P-loop driven by the voltage error. Notice that due to the presence of the pure integration in the voltage response (4.10), a simple proportional action is sufficient to ensure zero steady state error in the voltage control. If deemed necessary, an integral action can be added in order to have zero voltage tracking error during voltage ramps (charge/discharge at high current).

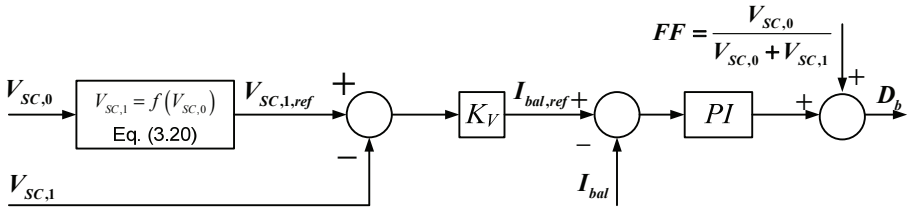


Fig. 4.8 – Control system for dynamic voltage sharing.

In order to prove the effectiveness of the balancing circuit, the same simulation as in Fig. 4.5 is repeated with the HC-based power buffer equipped with the proposed balancing circuit and related control system. Results are reported in Fig. 4.9.

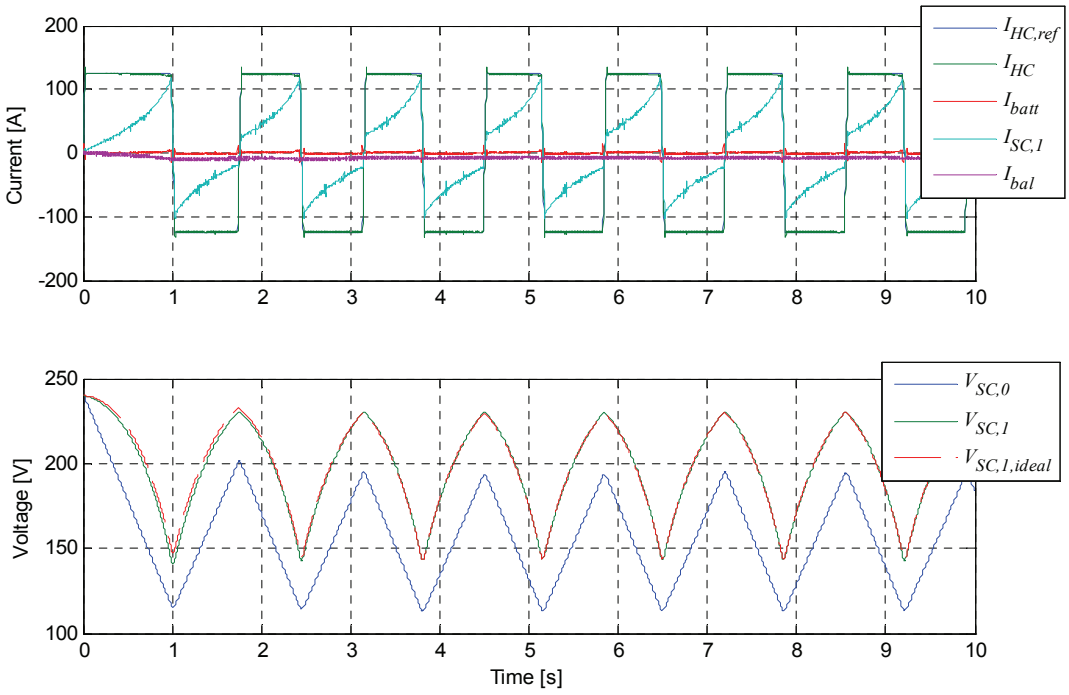


Fig. 4.9 – Cycling characteristics of the HC-based power buffer in presence of losses with proposed dynamic balancing circuit.

As expected, the SC-based power buffer can now be cycled continuously without losing its ability to exchange power with the load. The dynamic balance fixture ensures ideal voltage sharing throughout the cycles and, what is remarkable, the required balancing current is very small compared to the rated charge/discharge current. In the simulated system, in spite of the unrealistically high value of the losses, a balancing current of only 7.5 A is needed to track the ideal voltage trajectory while the buffer is cycling with

125 A of output current. In other words, the current rating of the switches used in the balancing bridge of Fig. 4.6 can be only 6% of the current rating of the switches used in the main HC converter.
In practice there may be other factors besides losses that can alter the ideal voltage sharing, such as unavoidable tolerance in the capacitance of the banks, variation of the actual bank capacitance as a function of the voltage, variation of the DC-side voltage due to internal resistance of the battery. The dynamic balancing circuit should therefore be able to compensate for all these factors. An exact analytical determination of the current rating needed for the balancing switches is therefore very difficult; however, an initial rule of thumb could be to fix the maximum balancing current in a rather conservative way as 10% of the rated HC converter current, and confirm this value with detailed simulation.

4.3 Pre-charge of SC banks

One of the problems that have to be solved for successful implementation of the HC-based power buffer is the so-called pre-charge of the SC banks to the minimum voltage level ensuring current controllability. Moreover, the initial conditions of the bank voltages should satisfy the ideal relationship (3.20), so that maximum energy cycling capability is ensured.
Let us consider the basic HC configuration in Fig. 4.10. When the main contactor SW_{main} is closed, if the initial voltage of the SC banks $V_{SC,tot} = V_{SC,1} + V_{SC,2}$ is lower than the battery voltage V_{DC}, there will be an inrush current flowing through the converter upper diode, as indicated in the figure. Such a current is not controllable by the switches and is limited only by the stray resistance of the circuit, resulting in the destruction of the converter if no countermeasure is taken. The inrush current lasts until the natural voltage balance between the battery voltage and the total SC voltage is reached.

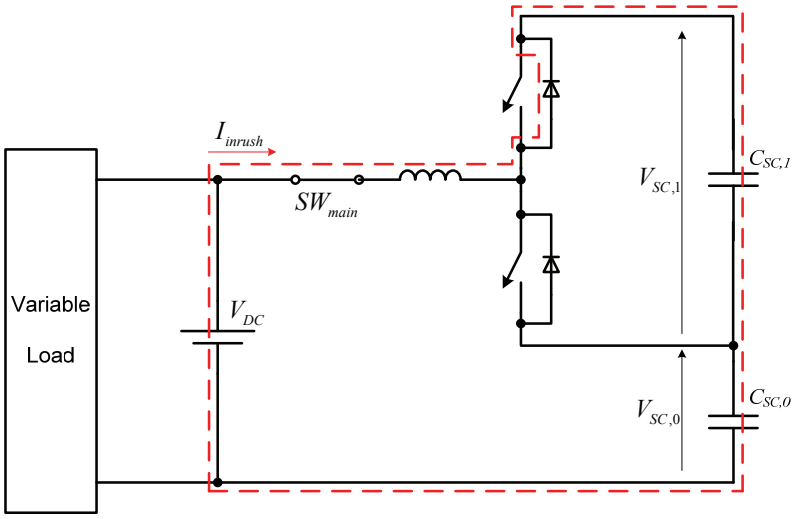


Fig. 4.10 – Inrush current phenomenon.

According to the arguments above, pre-charge is said to be completed when the following conditions are met:

$$\begin{cases} V_{SC,tot} \geq V_{DC} \\ V_{SC,1} = \sqrt{{V_{DC}}^2 - x\left(V_{DC} - V_{SC,0}\right)^2} \end{cases} \tag{4.12}$$

There are a number of methods that can be used to limit the inrush current and preset the individual voltages across the SC banks. Some of them are reported in the following.

4.3.1 Pre-charge through a switched resistor

Perhaps the most straightforward method to limit the SC charging current is to put a resistor on the current path, as shown in Fig. 4.11. From the figure, we may also notice that according to the state of the switch S_D, we can choose whether to charge only the lower SC bank (S_D is ON) or both SC banks in series (S_D is OFF).
Obviously, for a given value of the pre-charge resistor, the voltage balance is reached more quickly if the SC banks are charged in series, resulting in:

$$V_{SC,tot}(t) = V_{DC} + \left(V_{SC,tot}(0) - V_{DC}\right) \cdot e^{-t/\left(R_{prc}C_{tot}\right)}, \qquad C_{tot} = \frac{C_{SC,0} \cdot C_{SC,1}}{C_{SC,0} + C_{SC,1}} \tag{4.13}$$

At balancing, the voltages across the SC banks will be:

$$V_{SC,0}(t_{bal}) = \frac{C_{SC,1}}{C_{SC,0} + C_{SC,1}} \cdot V_{DC}\ , \qquad V_{SC,1}(t_{bal}) = \frac{C_{SC,0}}{C_{SC,0} + C_{SC,1}} \cdot V_{DC} \tag{4.14}$$

In general, such voltages do not satisfy the relationship (3.20), needed for ideal operation of the HC-based power buffer. However, after closing the main contactor SW_{main}, the system can be temporarily operated with reduced energy cycling, until the action of the dynamic balancing circuit enforces the ideal voltage sharing.

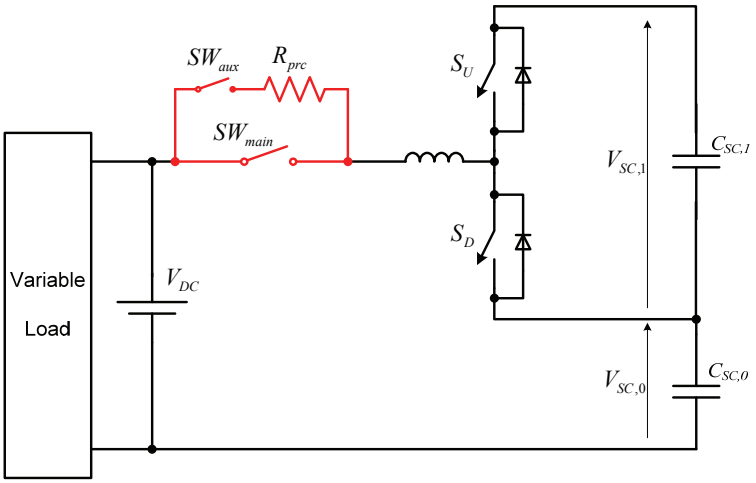


Fig. 4.11 – Pre-charge circuit based on switched resistor.

In principle, it would also be possible to divide the pre-charge operation in two phases. At first, only the lower SC bank is charged through R_{prc} and S_D; after a proper time $t_{prc,1}$, S_D is open and both banks are charged in series. By properly choosing the time

$t_{prc,1}$, ideal voltage sharing can be obtained right at the end of the pre-charge. However, this method would lead to higher losses in the pre-charge resistor and is therefore not developed any further.

Pre-charge through a switched resistor is commonly used in standard industrial converters like for instance diode rectifiers connected to a capacitive DC-link. However, its application to the HC-based system poses some major problems, due to the huge capacitance involved.One obvious concern is efficiency. It is in fact well known that charging a capacitive device at constant voltage results in 50% efficiency, regardless of the value of the charging resistance. Since the energy content of the SC bank is substantial, so would be the losses during the pre-charge process, wasting precious energy that could have been used by the load.

Losses in the resistor also produce a considerable amount of heat that has to be dissipated. This results in a bulky and expensive resistor and will also pose challenges related to the presence of parts operating at high temperature within the system.

The extent of the above mentioned problems is best understood with an actual example, like the power buffer designed for the Think EV (see Chapter 5). In this particular case the SC banks have capacitances $C_{SC,0} = 16.7F$, $C_{SC,1} = 7.2F$, and the nominal battery voltage is $V_{DC} = 280V$. The energy to be dissipated in the pre-charge resistor is then:

$$E_{prc} = \frac{1}{2} C_{tot} {V_{DC}}^2 = 197.2kJ \tag{4.15}$$

Just to give an idea, that amount of energy is equivalent to 20kW for 10s, or 3.3kW for 1 minute, or 1kW for 3 minutes and 20 seconds. Theoretically, according to (4.13), the charging time is infinite and the current asymptotically tends to zero; however, for practical purposes, we can consider pre-charge to be completed when the voltage imbalance is smaller than a given threshold ΔV_{prc_end}. In this case study, such a threshold is chosen so that the current resulting from shorting out the pre-charge resistor is less than 10 A, with a total stray resistance of the circuit that is dominated by the battery internal resistance equal to about 0.5 Ω. Therefore:

$$\Delta V_{prc\_end} = V_{DC} - V_{SC,final} < R_{stray} \cdot 10A \approx 5V \tag{4.16}$$

If we want to achieve pre-charge in 200 seconds from an initially empty SC buffer, resulting in about 1kW average power, then we have to select a resistance value so that:

$$R_{prc} = \frac{T_{prc}}{C_{tot}} \cdot \frac{1}{\ln\left(V_{DC} / \Delta V_{prc\_end}\right)} \approx 10\Omega \tag{4.17}$$

As a consequence, the peak power dissipated by the resistor and the corresponding overload factor are:

$$P_{R,peak} = \frac{{V_{DC}}^2}{R_{prc}} = 7.8kW \quad \Rightarrow \quad k_{ovl} = \frac{P_{R,peak}}{P_{R,avg}} = 7.8 \tag{4.18}$$

Due to the considerable overload, care must be taken when dimensioning the resistor under those operating conditions.

As a design reference, a resistor from REO UK, Ltd. [81], designed to dissipate $1kW$ with short time overload and forced air cooling has the following dimensions in mm: 210x300x350; during operation at $1kW$ it may reach about $300°C$. Even though that is just an example, it is safe to conclude that in order to achieve reasonable charging time, a bulky, lossy and expensive resistor is necessary.
Yet another aspect to be considered is that due to the exponential nature of the charging process, pre-charge time will be quite long even if the initial voltage imbalance is limited. As an example, let us consider the case in which the initial total SC voltage is already 75% of the battery voltage; since the threshold voltage remains the same, inverting (4.17) yields a charging time:

$$T_{prc,75} = R_{prc} \cdot C_{tot} \cdot \ln \frac{V_{DC}/4}{\Delta V_{prc\_end}} \approx 133s \tag{4.19}$$

which is not much shorter than the charging time needed for completely empty SC banks (200s).

4.3.2 Pre-charge through an auxiliary buck converter

In order to improve pre-charge efficiency and to reduce the size and cost of additional components, it is desirable to charge the SC banks at constant current with no dissipative components. This can be achieved by the addition of a basic buck converter, as shown in Fig. 4.12. Also in this case, the state of the switch S_D determines whether only the lower bank is charged, or the series connection of both banks.

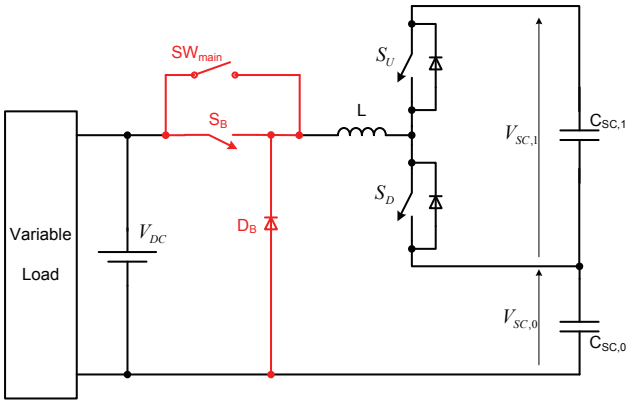


Fig. 4.12 – Pre-charge circuit with auxiliary Buck converter.

In order to achieve pre-charge, the buck converter constituted by the controllable switch S_B, the diode D_B and the inductor L is operated, with the main contactor SW_{main} open. The current rating of the auxiliary switch and diode determines how quickly the SC banks can be charged. After the SC banks have been pre-charged to the battery voltage, the main contactor is closed and neither S_B nor D_B takes part in the main power flow from between the load and the SC banks. It is therefore possible to keep the switch and the diode much smaller than the switches in the main converter, thus reducing the additional cost and volume.
Another significant advantage of this circuit compared to the switched resistor is that since the charging current can be controlled independently of the voltage difference

between the battery and the SC banks, a much shorter time is needed to pre-charge when the initial voltage of the SC banks is close to the battery voltage.
Assuming constant current charge, the minimum precharge time necessary to achieve voltage balance from empty SCs is related to the charging current by:

$$I_{prc} \cdot T_{prc} = Q_{SC,tot,final} = C_{tot} \cdot V_{DC} \tag{4.20}$$

In the case of the HC-based power buffer designed for Think EV, if we want a precharge time of 3 minutes we get a charging current of about 8 A. Considering that the system is designed to handle 30 kW power flow between the load and the SC banks, and that the minimum battery voltage is assumed to be 240 V, the ratio between the current rating of the main switches and that of the auxiliary switch is:

$$\frac{I_{S_B,rat}}{I_{Main,rat}} = 0.064 \tag{4.21}$$

Since now the circuit used for pre-charge is ideally lossless, it may be convenient to use the switch S_D to distribute the charge in order to get ideal voltage sharing as soon as the voltage balancing is reached, even though doing this will lengthen the voltage balancing process. Here is how the procedure would work.
Let us assume that the two SC banks are initially charged to $V_{SC,0,ini}$ and $V_{SC,1,ini}$, respectively. At voltage balancing, taking into consideration (3.20), the bank voltages $V_{SC,0,fin}$ and $V_{SC,1,fin}$ are given by (3.21). The net charge that should be put only into the lower SC bank is then calculated as:

$$\Delta Q = C_{SC,0} \cdot \left(V_{SC,0,fin} - V_{SC,0,ini}\right) - C_{SC,1} \cdot \left(V_{SC,1,fin} - V_{SC,1,ini}\right) \tag{4.22}$$

Therefore, pre-charge with S_D closed is executed until the voltage across the lower bank is increased by a value:

$$\Delta V_{SC,0} = \frac{\Delta Q}{C_{SC,0}} \tag{4.23}$$

After that, the switch S_D is open and both SC banks are charged in series. Since they will now receive the same charge, at voltage balancing they will reach the target voltages $V_{SC,0,fin}$ and $V_{SC,1,fin}$. The main contactor can then be closed, and the HC-based power buffer is ready to be operated with maximum energy availability from the very beginning.
In the system in Fig. 4.12, in order to minimize the number of extra components needed for pre-charge, the same inductor used by the main HC-converter is also used by the pre-charge buck converter. This may pose some challenges, since the resulting current ripple during pre-charge may be significant compared to the current rating of S_B and D_B.

4.3.3 Pre-charge through the balancing circuit

With the simple addition of some static relays, the dynamic balancing circuit can be used to pre-charge the SC banks, as indicated in Fig. 4.13.
The circuit has three operation modes:

- Pre-charge (SW_{main} = OFF, $SW_{aux,1}$ = ON, $SW_{aux,2}$ = OFF);

– Redistribution (SW_{main} = OFF, $SW_{aux,1}$ = OFF, $SW_{aux,2}$ = ON);
– Normal operation (SW_{main} = ON, $SW_{aux,1}$ = OFF, $SW_{aux,2}$ = ON).

During the pre-charge phase, the DC source is connected to the upper balancing switch through the auxiliary contactor $SW_{aux,1}$. The lower SC bank is then charged through the buck converter constituted by the upper balancing switch $S_{b,U}$, the free-wheeling diode of the lower balancing switch $S_{b,D}$ and the balancing inductor L_{bal}. Pre-charge lasts until enough energy is stored in the SC banks, so that after redistribution the total SC voltage is higher than the battery voltage.

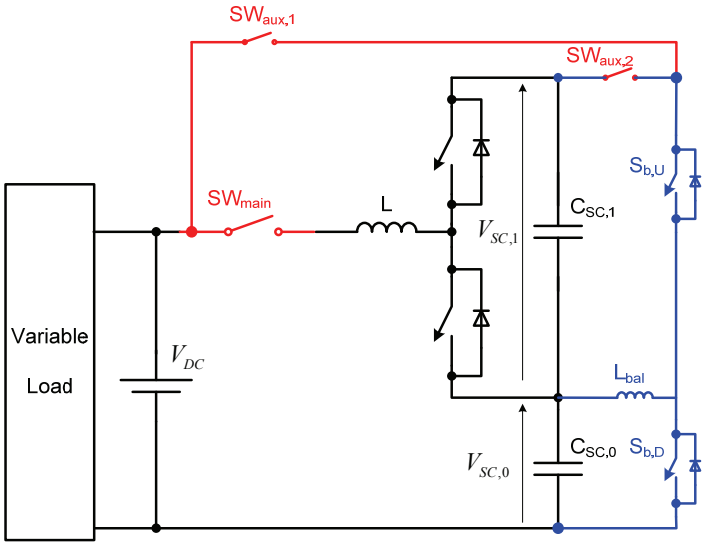


Fig. 4.13 – Pre-charge using dynamic balancing circuit.

When enough energy is stored in the SC banks, pre-charge is complete, but the total SC voltage may still be lower than the battery voltage. Then redistribution is performed by transferring energy between the two SC banks, causing the total SC voltage to increase until it finally overcomes the battery voltage; during this operation SW_{main} and $SW_{aux,1}$ are open, while $SW_{aux,2}$ is closed.
After voltage levelling is achieved, auxiliary contactors are open, the main contactor SW_{main} is closed and normal operation of the HC-based power buffer can start.
The mechanism of pre-charge and energy redistribution is not very straightforward and requires further explanation. Suppose that the two SC banks are initially charged at voltages $V_{SC,0}(0)$ and $V_{SC,1}(0)$; if we want the ideal voltage balancing to hold true, the bank voltages at balancing $V_{SC,0,fin}$ and $V_{SC,1,fin}$ are given by (3.21). The resulting energy contents are:

$$E_{SC}(t_{ini}) = \frac{1}{2}\left(C_{SC,0}{V_{SC,0,ini}}^2 + C_{SC,1}{V_{SC,1,ini}}^2\right)$$
$$E_{SC}(t_{fin}) = \frac{1}{2}\left(C_{SC,0}{V_{SC,0,fin}}^2 + C_{SC,1}{V_{SC,1,fin}}^2\right) \quad (4.24)$$

During the pre-charge phase, the amount of energy $\Delta E = E_{SC}(t_{fin}) - E_{SC}(t_{ini})$ is put into the lower SC bank, whose terminal voltage will then rise to the value:

$$V_{SC,0}\left(t_{prc,1}\right)=\sqrt{\frac{2\cdot\Delta E}{C_{SC,0}}-V_{SC,0,ini}{}^{2}} \tag{4.25}$$

At this point, the pre-charge phase is ended and the redistribution phase begins. Since the process is lossless, energy is conserved while transferring charge between the two banks. Finally, the voltage balance is reached, automatically satisfying (4.12).
An obvious advantage of the circuit in Fig. 4.13 is that it does not require any additional switching devices to perform constant current pre-charge. Only one main contactor (present in all configurations), and two auxiliary contactors are needed. The auxiliary contactors do not carry the main current and can be commutated at zero current. They can therefore be small and cheap.
From the discussion above, it is clear that the time needed for pre-charge is dictated by the rating of the dynamic balancing circuit.
One disadvantage of this solution against the one in Fig. 4.12 is that pre-charge has to be done by first charging the lower SC bank and then transfer part of the energy to the upper bank. A somewhat longer waiting time is needed compared to the system using a dedicated buck converter for pre-charge, even assuming the same current rating for the semiconductor switches.

5 CONVERTER DESIGN FOR THE CITY CAR "TH!NK EV"

The concepts introduced in the previous chapters need to be validated experimentally. To this aim, several laboratory prototypes have been built.
At first, the theory behind the operation of the HC-based power buffer has been proven by the use of a reduced-scale prototype, as reported in [78,82]. The system, whose main specifications are summarized in Table 5-1, is shown in Fig. 5.1. Due to the low voltage level, MOSFET devices are used to implement the main converter switches. Since the aim of this prototype was only to investigate the validity of the basic equations developed in chapter 3 to describe the behaviour of the HC system, no particular effort was put into the design and optimization of the converter components and details about the design are therefore not reported here.

Fig. 5.1 – Reduced-scale prototype of HC-based power buffer

The reduced-scale prototype allowed concluding that the operation of the HC converter was in accordance to the theoretical analysis previously presented. However, a full-scale HC system had to be developed in order to show all the advantages of the proposed topology as well as its weaknesses.

Table 5-1 – Main specifications of the reduced-scale experimental setup

Battery	Sealed Lead-Acid 12V, 10Ah, $R_{int} \approx 80m\Omega$
SuperCapacitor elementary cell	Maxwell BCAP 350F $(\pm 20\%)$, 2.5V, $ESR_{DC} = 3.2m\Omega\,(\pm 25\%)$
Uncontrolled SC bank	6 series by 3 parallel array of cells 175F, 15V, $ESR_{DC} \approx 6.4m\Omega$
Controlled SC bank	6 series array of cells 58.3F, 15V, $ESR_{DC} \approx 20.4m\Omega$
Main switching devices	HEXFET power MOSFET, IRF3805S-7P 55 V, 160 A, $R_{DS,on} = 2.6\ m\Omega$
DC inductor	0.5 mH, 65 A
Balancing switching devices	MOSFET IRF7341 55 V, 3.8 A

The pure Electric Vehicle "Think City" shown in Fig. 5.2 [14] was then selected as benchmark for the implementation of an HC-based power buffer.

Fig. 5.2 – Th!nk City EV (image taken from the internet)

5.1 System Specifications

The drive train of the vehicle under consideration is composed of few basic components, as shown in Fig. 5.3. The supercapacitor-based power buffer has to be interfaced to the battery terminals through the proposed DC-DC converter topology.
The only source of energy originally on board of the vehicle is a high temperature, sodium nickel chloride-based traction battery (ZEBRA® battery), whose main electrical specifications are given in Table 5-2.
The traction motor in use is a liquid cooled 3-phase induction motor (see Table 5-2) supplied from the main battery through a dedicated, IGBT-based inverter.

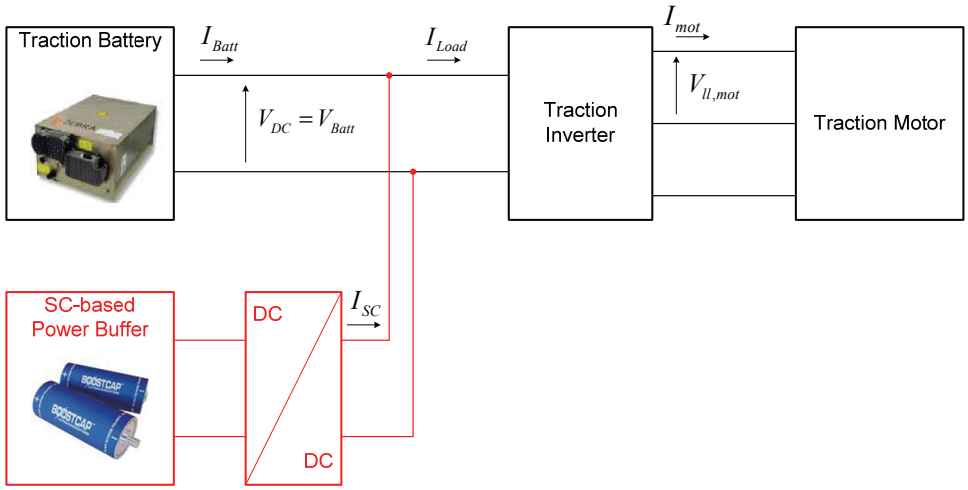


Fig. 5.3 – Main drive train components of the Th!nk City EV and the proposed SC-based power buffer

Table 5-2 – Main electrical specifications of Th!nk City drive train

Traction Battery	Battery Type	ZEBRA®, Z5-278-ML3P-76
	Rated Energy	$E_{r,Batt} = 21.2\,kWh$
	Open Circuit Voltage	$OCV = 278V\ @85\%\ SOC$ $OCV = 254V\ @20\%\ SOC$
	Internal Resistance	$R_{i,batt,\min} = 0.43\,\Omega \quad @\ 95\%\ SOC$ $R_{i,batt,Max} = 0.65\,\Omega \quad @\ 20\ \%\ SOC$
	Peak power	$P_{Max,Batt} = 32\,kW\ @\ 2/3\,OCV, 30\,s$
	Total weight	$180\,kg$
Traction Motor	Motor Type	Induction, liquid cooled, 3-ph, 122 Hz, 4 poles,
	Rated Power	$P_{r,mot} = 18\,kW$
	Peak Power	$P_{Max,mot} = 30\,kW$ for 30 s
	Rated Voltage	$V_{r,mot} = 127\,V_{ll,rms}$
	Rated Current	$I_{r,mot} = 100\,A_{rms}$
	Power Factor	$PF_{mot} = 0.80$
	Rated Speed	$n_{base} = 3625\,r/\min$
	Maximum Speed	$n_{Max} = 10000\,r/\min$
Traction Inverter	Rated Power	$P_{r,inv} = 18\,kW$
	Peak Power	$P_{Max,inv} = 30\,kW$ for 30 s
	Max. DC voltage	$V_{DC,Max} = 600\,V$

Obviously, the system also includes many other components like for instance an integrated battery charger, a DC/DC converter to step down the traction voltage to the automotive standard 12 *V*, a battery management system and so on. Such components are not described in detail, since they do not directly affect the design of the power buffer.

From the specifications in Table 5-2, it results that maximum power that can be cycled in and out the supercapacitor-based power buffer cannot exceed 30 *kW*, due to the power handling limitation of the traction inverter. The required amount of usable energy in the power buffer is dictated by the particular drive cycle and is not easy to determine; a simple heuristic approach is adopted, stating that the buffer should contain enough energy to accelerate the vehicle at full power for at least 16 s, which is the time needed to reach a speed of 80 km/h from standstill.

Some additional considerations are needed to decide the rated voltage of the SC banks. As it was pointed out in chapter 3 for both HB-based and HC-based DC-DC converter topologies, in order to optimize the VA rating of the power electronics switches, the SC bank rated voltage should be equal to the battery terminal voltage. However, the latter is not constant and depends on several factors like the battery State Of Charge (SOC) and the battery current. The OCV of the ZEBRA battery has a very nonlinear behaviour, with two different voltage plateaus, as shown in Fig.1.5. At very low SOC, the OCV of the battery is about 10% lower than the OCV of a fully charged battery, resulting in about 250 *V* minimum OCV for the battery in Table 5-2. The terminal voltage of the battery is further reduced due to internal resistance, when power is being supplied from the battery itself; the associated voltage drop can be substantial when the battery alone is supplying the load, as can be calculated from the internal resistance data in Table 5-2. However, when the power buffer is in use, most of the power required by the load will be supplied from the SC banks, relieving the battery and thus keeping its terminal voltage to values close to the OCV. The situation is very well described by the simulations in Fig.2.9 and Fig.2.10.

If the SC bank rated voltage is higher than the battery voltage, then the theoretical energy storage capability of the banks is not fully exploited as the proposed converter topology does not allow for charge of the uncontrolled SC bank beyond the battery terminal voltage. Using the whole energy storage capability of the SC banks is crucial to ensure proper system operation and to protect the battery as much as possible from heavy cycling, especially at low SOC.

From the considerations above, and adding some safety voltage margin, the rated voltage of the SC banks is fixed to 240 *V*, as shown in Table 5-3 along with the other main specifications of the power buffer.

Table 5-3 – Main specifications of the supercapacitor-based power buffer

Available Energy	$\geq 480\,kJ \quad (30\,kW\ for\ 16\,s)$
Rated Power	30 *kW*
Rated SC bank voltage	240 *V*

5.2 SC-based power buffer design based on proposed optimized topology

The proposed topology based on the so-called HC converter was extensively described in chapter 3; the basic structure of the full scale prototype is shown in Fig. 5.4, and a more detailed schematic diagram of the laboratory setup is reported in Fig. 5.5. Details about the design of the main components of the system are given in the following sections.

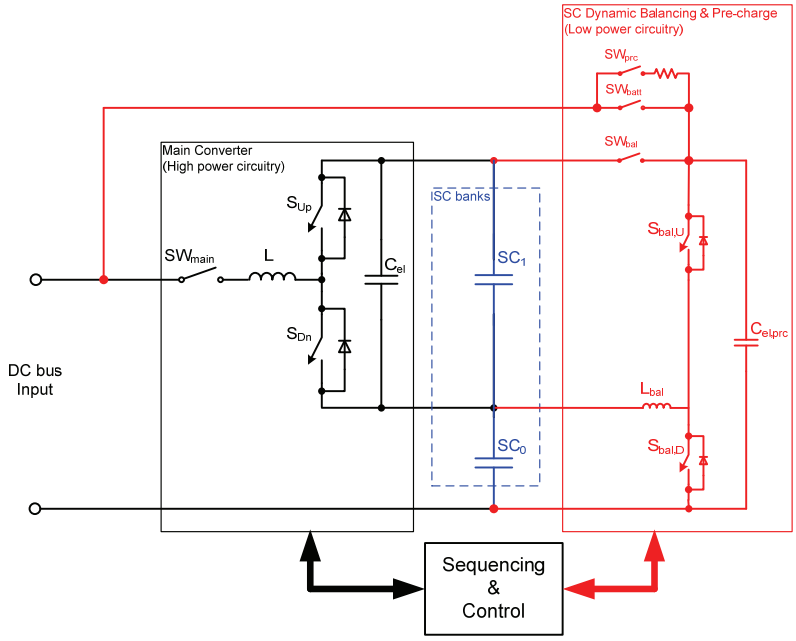


Fig. 5.4 – Basic structure of the full scale prototype of SC-based power buffer with HC converter.

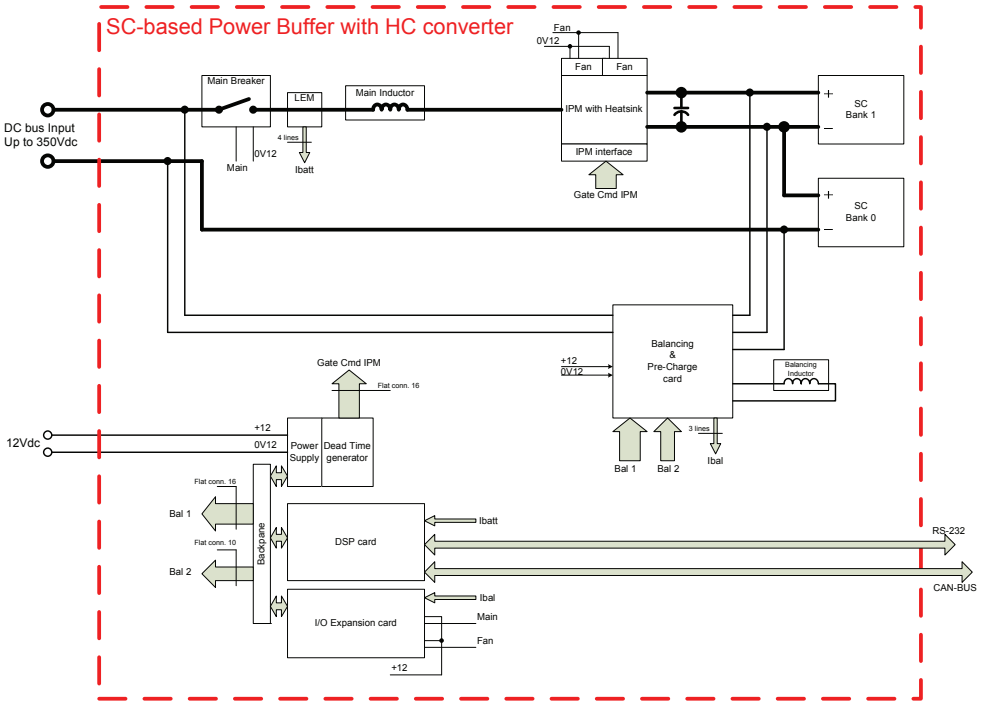


Fig. 5.5 – Overall schematic of the SC-based power buffer with HC converter.

5.2.1 SC bank design

According to the specifications in Table 5-3 and assuming that 75% of the total energy in the bank will be available for use by the load, the necessary bank capacitance is calculated as:

$$C_{SC,HB} \geq \frac{1}{0.75} \cdot \frac{2 \cdot E_{avail}}{V_{SC,rat}^2} = 22.2\,F \tag{5.1}$$

When the HC topology is used, such a capacitance is split into two banks, each having the same rated voltage of 240 V. Designing with a capacitance ratio $x = 2.5$ that minimizes the SC losses, the two banks have respective capacitances (see (3.57)):

$$C_{SC,0} = \frac{x}{x+1} \cdot C_{SC,HB} = 15.9\,F, \qquad C_{SC,1} = \frac{1}{x+1} \cdot C_{SC,HB} = 6.3\,F \tag{5.2}$$

For practical implementation of the banks, SC cells from Maxwell Technologies [58] are used, due to their high performance in terms of energy and power density and to their availability on the market at reasonable price. The cells rated for high power levels as the ones we are interested in all have a rated operating voltage of 2.7 V. Therefore, the banks must be assembled by series connecting N_s cells:

$$N_s \geq \frac{V_{SC,rat}}{V_{cell,rat}} = 89 \tag{5.3}$$

Choosing $N_s = 90$, so to have some additional voltage margin, each bank of the HC-based power buffer will be made of elementary cells having ideally the following capacitance:

$$C_{SC,0,cell} = N_s \cdot C_{SC,0} = 1431\,F, \qquad C_{SC,1,cell} = N_s \cdot C_{SC,1} = 567\,F \tag{5.4}$$

Obviously, such odd capacitances are not readily available and we have to use the closest commercial values, resulting in the final choice:

$$\begin{cases} C_{SC,0,cell} = 1500\,F \\ C_{SC,1,cell} = 650\,F \end{cases} \quad \Rightarrow \quad x = 2.3 \tag{5.5}$$

The resulting capacitance ratio is slightly different from the design value, but is still acceptable in terms of energy availability (77% theoretical) and SC losses. Main characteristics of the banks are given in Table 5-4.

After dimensioning of the banks has been carried out based on requirements on energy content, it is necessary to confirm that the banks are able to handle the power needed by the load without exceeding their thermal limits.

Although SCs have very good power density, ranging from 3.8 *kW/kg* for the smaller 650 F cells to 4.3 *kW/kg* for the 1500 F cells, their thermal characteristics are not as good. Under free convection, the thermal resistances are 6.5 °*C/W* and 4.5 °*C/W* for the 650 F and 1500 F cells, respectively. Since the maximum operating temperature is also quite low (less than 65 °*C*) and should be kept as low as possible in order to increase lifetime, thermal management could be critical.

Table 5-4 – Main specifications of the SC banks designed for 30 kW, 240 V, HC-based power buffer

Uncontrolled Bank SC0	Bank capacitance	$C_{SC,0} = 16.7\,F$
	Bank Rated Voltage	$V_{SC,0,\max} = 243\,V$
	Bank ESR	$ESR_{SC,0} = 56.7\,m\Omega$
	Number of cells	90, series connected
	Elementary cell type	BCAP1500 E270 (Maxwell Technologies)
	Bank weight (SC cells only)	28.8 *kg*
	Bank volume (including enclosure)	64 litres
	Bank rated power	$P_d = 124\,kW$
	Bank rated energy	492 *kJ*
Controlled Bank SC1	Bank capacitance	$C_{SC,1} = 7.2\,F$
	Bank Rated Voltage	$V_{SC,1,\max} = 243\,V$
	Bank ESR	$ESR_{SC,1} = 103.5\,m\Omega$
	Number of cells	90, series connected
	Elementary cell type	BCAP0650 E270 (Maxwell Technologies)
	Bank weight (SC cells only)	18.0 *kg*
	Bank volume (including enclosure)	52 litres
	Bank rated power	$P_d = 68.4\,kW$
	Bank rated energy	213 *kJ*

Assuming a worst case ambient temperature of 50 °*C*, that leaves space for a 15 °*C* increase of temperature in the SC cells due to internally generated losses. Resulting *rms* current limit is then:

$$I_{rms,max,650} = \sqrt{\frac{\Delta T_{\max}}{ESR_{650} \cdot R_{th,650}}} = 45\,A$$
$$I_{rms,max,1500} = \sqrt{\frac{\Delta T_{\max}}{ESR_{1500} \cdot R_{th,1500}}} = 73\,A \qquad (5.6)$$

It is therefore clear that the SC banks cannot thermally withstand continuous operation at rated power; however, that is not likely to happen in the EV application when the SC buffer is used as auxiliary power source to help the battery. In general, the power required from the buffer is a complicated function of the particular drive cycle and of the control algorithm in use; the simulations in chapter 2 shows that for the two kind of standard drive cycles that were analyzed, worst case average losses in the SC bank amount to about 22 *W* (see Table 2-3). Each of the SC cells constituting the banks will then dissipate a minuscule amount of power; even considering that the power dissipation is not steady over time, but has very high peaks during hard acceleration and

braking, and taking into account that in real driving there may be more demanding cycles than those considered by the standard, the thermal margin appears to be enough not to require any additional means for forced cooling. Experimental verification, possibly on a real vehicle driven on actual road, is still deemed necessary.
Fig. 5.6 shows a picture of the banks after assembly made in our workshop. Voltage balancing within each SC bank is achieved by using commercially available balancing circuits supplied by Maxwell Technologies together with the SC cells.

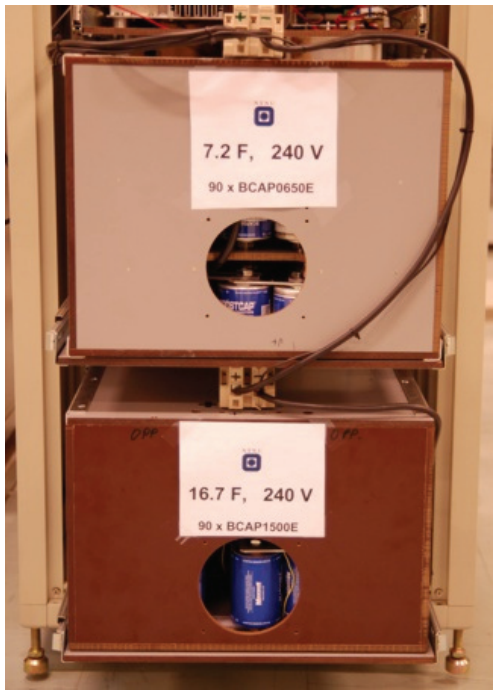


Fig. 5.6 – The SC banks used in the full scale prototype.

5.2.2 Smoothing inductor design

In the system of Fig. 5.4, the smoothing inductor has two major roles: it limits the current ripple that generates losses without contributing to useful power transfer, and it limits the peak current flowing in the semiconductor switches. Besides the obvious implications on efficiency, the first aspect may have direct influence on the battery lifetime, which is one of the most critical factors in EV applications.
On the other hand, a large inductance value will result in a bulky and heavy component that is undesirable, due to volume and weight limitations on board. A proper design of the inductor, with special emphasis on the selection of a suitable core material is therefore paramount in EV applications.
An estimation of the required inductance can be obtained from the application of (3.51). Assuming a worst case peak current ripple equal to 15% of the rated DC current of the inductor, a switching frequency of 10 *kHz* and a battery voltage equal to the lowest possible value of 240 *V*, we get:

$$L_{HC} \approx 0.13\,mH \tag{5.7}$$

The inductance above will result in a peak current in the converter switches (and in the inductor itself) equal to about 144 *A*. Assuming that all the ripple current has to be

handled by the battery, this will result in about 75 W of additional losses due to the worst case internal resistance, which is less than the thermal losses necessary to keep the battery temperature to the operating level of about 270 °C.

Table 5-5 – Two alternative inductor designs for the real-scale prototype of HC-based power buffer

Inductor 1	Design Inputs	Inductance at full load	0.13 mH
		Max peak-peak ripple @ 10 kHz	38 A
		Max DC current	125 A
		Peak current	144 A
		Core Material	METGLAS® alloy 2605SA1
	Design Outputs	Core size	AMCC200 (double U-core)
		N. of turns	21
		Winding type	Copper foils (67 mm, 0.5 mm)
		Total airgap	3.3 mm (2 airgaps of 1.7 mm each)
		Core loss	39 W
		Copper loss	47 W
		Total Weight	2.87 kg
		Temperature rise @ rated current	67 °C
Inductor 2	Design Inputs	Inductance at full load	0.065 mH
		Max peak-peak ripple @ 10 kHz	76 A
		Max DC current	125 A
		Peak current	163 A
		Core Material	METGLAS® alloy 2605SA1
	Design Outputs	Core size	AMCC168S (double U-core)
		N. of turns	27
		Winding type	Copper foils (14 mm, 0.2 mm)
		Total airgap	4.7 mm (2 airgaps of 2.4 mm each)
		Core loss	86 W
		Copper loss	40 W
		Total Weight	2.12 kg
		Temperature rise @ rated current	70 °C

Due to the high peak current in the inductor, it is important to use a core material with high saturation flux density. Classical laminated iron is an option, but the high frequency switching components may induce excessive core losses. Some amorphous alloys [83] exhibit a relatively high saturation flux density (B_{max} = 1.5 T), with much lower core losses compared to standard iron and are therefore chosen in this context, resulting in the design labelled as “Inductor 1” in Table 5-5.

An alternative design, labelled as “Inductor 2” in Table 5-5, is obtained by loosing the requirement on the allowable ripple, resulting in a smaller value of the required inductance. However, this reflects in a higher peak current. As a result, even though the inductor is physically smaller (about 25% lighter) than the one obtained in the previous design, the gain is not as substantial as one could have expected from a 50% reduction

of the inductance. Core losses are significantly increased, due to the increased current ripple. Increased ripple also means increased losses in the battery, which would now be equal to about 300 *W*. Moreover, the peak current that the semiconductor switches have to withstand is increased by 14%.
Considering advantages and drawbacks of each design, the one labelled as "Inductor 1" has been preferred and realized in our workshop (Fig. 5.7).

Fig. 5.7 – Inductor used for the real scale prototype of HC-based power buffer.

It should be noticed that the inductors in Table 5-5 are designed for continuous operation at rated power (30 *kW* at 240 *V*). This may be necessary in the laboratory setup, where continuous cycling at maximum power can be executed to assess the performances of the power electronics converter, but is overrated for the EV application. According to simulation data in chapter 2, the average of the absolute value of power over one driving cycle that is handled by the SC buffer is well below 5 *kW*. Therefore, also taking into account the quite high overload factor for several seconds, it is possible to design the smoothing inductor for a much lower value of *rms* current than the one considered in Table 5-5, while keeping the same requirement on the peak current. Doing so leads to a much lighter inductor, more suitable to the EV application under consideration.
In chapter 3, it has been claimed that one of the definite advantages of the HC topology is the need of a much smaller inductor, as compared to HB topology, if the same peak-to-peak current ripple has to be achieved.

Table 5-6 –Inductor designs for the HB-based power buffer

Design Inputs	Inductance at full load	0.16 mH
	Max peak-peak ripple @ 10 kHz	38 A
	rms current (complete discharge at rated power)	170 A
	Peak current	269 A
	Core Material	METGLAS® alloy 2605SA1
Design Outputs	Core size	AMCC800A (double U-core)
	N. of turns	21
	Winding type	Copper foils (69 mm, 0.8 mm)
	Total airgap	6.0 mm (2 airgaps of 3.0 mm each)
	Core loss	36 W
	Copper loss	81 W
	Total Weight	7.5 kg
	Temperature rise @ rated current	50 °C

The statement is proved by looking at the inductor in Table 5-6, designed for the HB-based topology according to the same specifications for the power buffer, as in Table 5-3. Using the same core material, and thus the same peak flux density, such inductor is 2.6 times heavier than the one used by the HC-based topology.

5.2.3 Design of the main power circuit for HC converter

Each of the main switches in Fig. 5.4 must withstand a voltage equal to the rated voltage of the SC bank SC1 that is 243 *V*. The natural choice is therefore a standard 600 *V* IGBT module, embedding in one component both active switches as well as associated antiparallel diodes. The maximum current flowing into the switches during normal operation is the inductor peak current, equal to 144 *A*.
Due to the operating principle of the HC converter, the system has to be able to operate with duty cycle varying from zero to unity with rated current flowing. There are then three different operating conditions according to the SOC of the SC banks, each having a different distribution of losses within the power module:

1. Beginning of discharge (end of charge), with bridge duty cycle close to zero and current flowing almost always in the diode;
2. End of discharge (beginning of charge), with bridge duty cycle close to unity and current flowing almost always in the IGBT;
3. Intermediate charge state, when current is flowing alternatively in the IGBT and in the diode for a fraction of the switching period.

Due to the relatively high energy content of the SC buffer, each condition may last for a time that is longer than the thermal time constants related to the heat transfer from junction to ambient. Total amount of losses within the power module is not very different in the three cases above; however, in the latter condition, losses are distributed between two solid state devices (one IGBT and one diode) and are therefore easier to dissipate.
From the thermal point of view, condition 1 is the most demanding for the following reasons:

- In virtually all kind of power modules, the thermal resistance of the diodes is higher than that of the IGBTs. This is due to the smaller active area needed for diodes in order to achieve the same current rating.
- Condition 2 arises when the bank is close to empty, meaning that the voltage across the bridge is lower. Thus, switching losses will be lower than those in Condition 1.

From the electrical specifications, the ideal choice would be a module rated for 600 *V*, 150 *A*, such as, for instance, the latest trench-gate IGBT module from Semikron [84] SKM145GB066D. Considering the operating condition of the circuit labelled as 1 in the above, according to the worst-case datasheet parameters of the free-wheeling diode (FWD) embedded in the module, we get the following conduction losses in the diode:

$$P_{c,FWD} = V_{f0,FWD} \cdot I_{HC,rat} + R_{f,FWD} \cdot I_{HC,rat}^2 \approx 190\,W \tag{5.8}$$

Switching losses in the diode are quite small, and in this specific operating condition amounts to about 23 *W*. Losses in the IGBT are almost exclusively switching losses and

amount to about 93 W. The worst-case temperature difference between the heatsink and the diode junction is therefore:

$$\Delta T_{j-h,FWD} = \left(P_{c,FWD} + P_{sw,FWD}\right) \cdot \left(R_{th(j-c),FWD} + R_{th,(c-h)}\right) + P_{sw,IGBT} \cdot R_{th,(c-h)} \approx 122\,°C \qquad (5.9)$$

In the equation above, the temperature rise due to the power dissipated in the IGBT has been neglected, since it is quite small in this operating condition.
Since, according to the manufacturer, it is not advised to operate the junction above 150 °C, (5.9) would imply a maximum heatsink temperature of 28 °C, which can be hard to achieve.
It is therefore necessary to use a more powerful module, in order to allow for operation with a higher heatsink temperature. Within the same device family, the module SKM195GB066D features a rated current of 200 A, with 600 V voltage blocking capability. Repeating the same thermal calculations as above, it can be shown that with this module the ΔT_{j-h} of the FWD is limited to about 95 °C, allowing for operation with a maximum heatsink temperature of 55 °C. This is still quite low, but it may give sufficient margin for designing the cooling system; if that is not the case, an even bigger power module should be deployed.
Management of the heat sink temperature is somehow made easier by the already mentioned fact that in the EV application, the average power processed by the converter over a complete driving cycle is much lower than the peak power of 30 kW used to design the switches. Overloads up to that level can last for several seconds, making them equivalent to steady state conditions as far as the junction-to-sink thermal behaviour is concerned. However, the heat capacity of the heat sink has a much higher value and may efficiently smooth the temperature variation due to the peaks of dissipated power.
The power modules considered above were not readily available for the realization of the prototype, and the Intelligent Power Module (IPM) from Fuji Electric [85] 6MBP150RTB060 has been used instead. This IPM features a complete inverter bridge (6 IGBT, 6 FWD), with each device rated for 600 V, 150 A. Characteristics of the devices are quite similar to those of the equivalent 150 A Semikron module considered earlier, and therefore the results in (5.8) and (5.9) still hold, meaning that continuous cycling at rated power is possible only if the heatsink temperature is kept below 28 °C. This aspect has to be taken into account during the experiments.
Besides the power semiconductors, the IPM also includes gate driver and protection circuitry, simplifying prototyping. In the implementation of the system in Fig. 5.4, only one out of three of the IPM bridge legs is actually used, as clearly seen in Fig. 5.8.

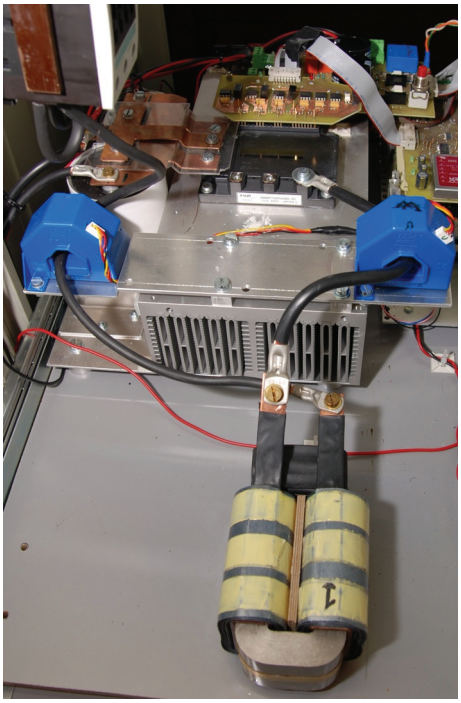


Fig. 5.8 – Main power circuit of the HC-based power buffer.

5.2.4 Design of the balancing and pre-charge circuit

According to the theory presented in chapter 4, the current rating of the balancing switches can be selected in the order of less than one tenth of that of the main converter switches. However, voltage withstanding capability must be double. With these specifications in mind, the latest generation IGBT from Infineon [86] IKW15N120T2 has been identified as the most suitable device. Such an IGBT can be hard-switched at a frequency up to 40 *kHz* at 600 V and rated current. Using relatively high frequency allows for considerable size reduction of the balancing inductance (see Fig. 5.4); obviously, switching losses increase, but since the balancing circuit handles relatively little power, its losses are not going to be an important factor for the efficiency of the overall system.

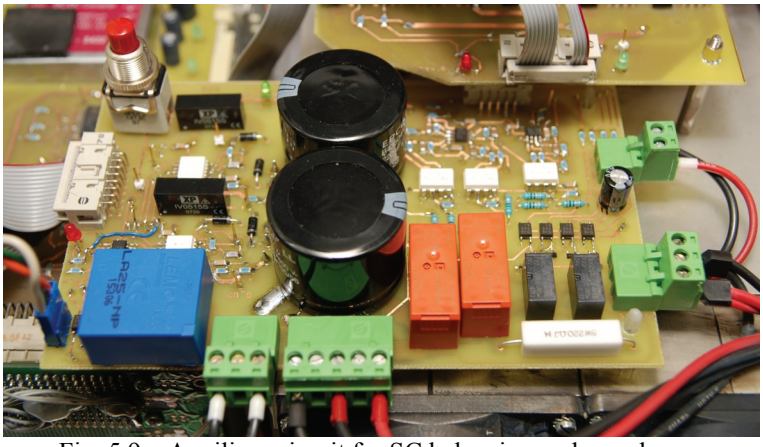


Fig. 5.9 – Auxiliary circuit for SC balancing and pre-charge.

The circuit for balancing and pre-charge is shown in Fig. 5.9; the PCB also includes the necessary gate driving circuit for the IGBTs, the pre-charge relays and SC bank voltage sensing circuitry. The PCB is assembled on the same heatsink as the main converter.

5.2.5 Digital controller board

The whole system in Fig. 5.4 is digitally controlled. A general-purpose control card [87] developed in our department has been deployed, based on the TMS320F2812 fixed point DSP from TI. Such a DSP has all the necessary resources for the generation of PWM signals for both the main bridge and the balancing bridge, as well as the needed computational power for simultaneous real-time control of the main power flow and balancing process.
The digital control card also features RS-232 serial communication used for servicing, and CAN interface for seamless integration with the vehicle management system.
Dedicated circuitry has been added to generate the local power supply derived from the standard 12 V normally available in automotive and for signal adaptation to/from the IPM and sensors, as shown in Fig. 5.10.

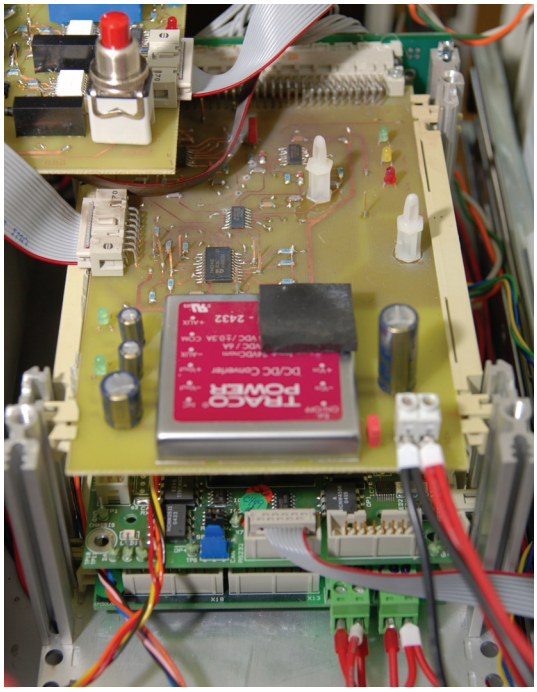


Fig. 5.10 – Digital control circuitry.

5.3 Digital control system for the proposed SC-based power buffer

Block diagram of the overall control system for the power buffer is reported in Fig. 5.11. The only external input to the buffer is the main current command $I_{SC,ref}$. In the hybrid source EV application, such a reference is generated by the power sharing algorithm as described in chapter 2.

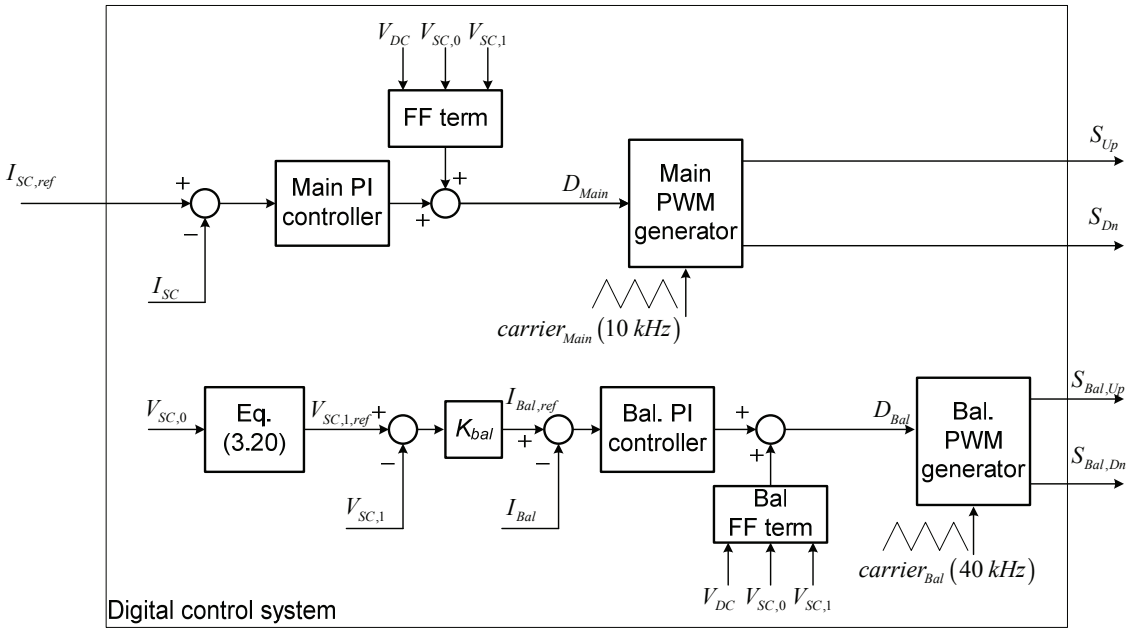


Fig. 5.11 – Control structure of the SC-based power buffer.

During normal power buffer operation there are two independent control loops being executed simultaneously, one for the control of the main buffer current I_{SC}, and the other for the management of the dynamic voltage balancing between the two SC banks. Those control algorithms use internal measurements of the main buffer current I_{SC}, the balancing current I_{bal}, the terminal voltage of each SC bank $V_{SC,0}$,$V_{SC,1}$ and the battery voltage V_{DC} to perform their tasks.

The whole control structure in Fig. 5.11 has been digitally implemented in the aforementioned DSP, with the two control loops executed every 100 μs (10 *kHz* rate), and the timing diagram showing the synchronization between the control algorithm and the triangular carriers used for PWM of the two bridges is reported in Fig. 5.12.

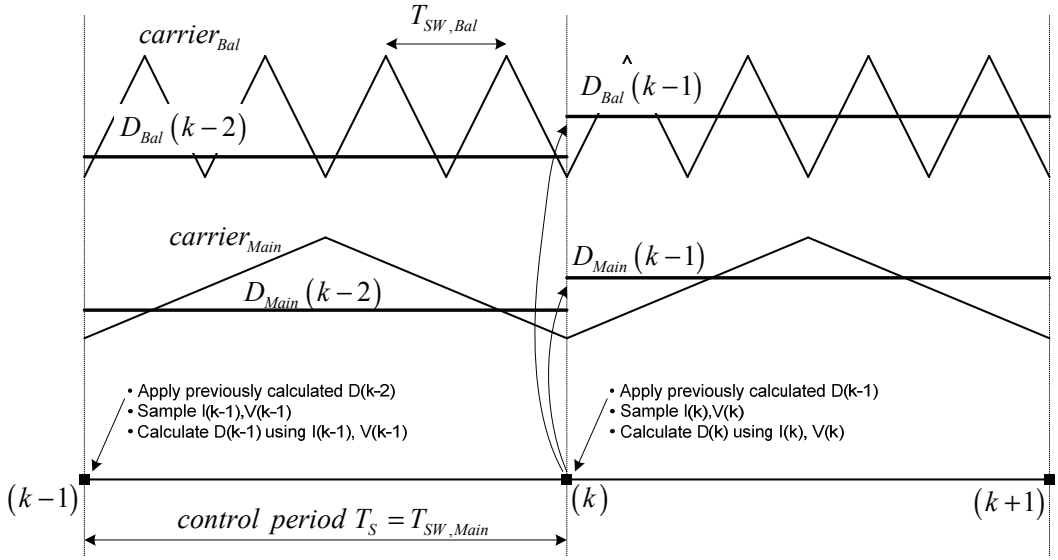


Fig. 5.12 – Timing of the digital control system and synchronization with PWM.

5.3.1 Main current controller

With reference to Fig. 3.1, the current flowing in the inductor is given by:

$$L\frac{di_{SC}}{dt} = V_{HB} + V_{SC,0} - V_{DC} \tag{5.10}$$

Since the current control will have response time in the order of few milliseconds, it is reasonable to consider the voltage across the supercapacitor banks and the battery voltage as constant quantities in such a time frame.
Expressing the bridge voltage as a function of the duty cycle, and splitting the contribution of a feed-forward term and the output of the P-I regulator, we get:

$$L\frac{di_{SC}}{dt} = D\cdot V_{SC,1} + V_{SC,0} - V_{DC} = \left(D_{FF} + \Delta D\right)\cdot V_{SC,1} + V_{SC,0} - V_{DC} \tag{5.11}$$

Having defined the feed-forward term as:

$$D_{FF} = \frac{V_{DC} - V_{SC,1}}{V_{SC,0}} \tag{5.12}$$

Assuming the converter to be ideal, the transfer function between the control input (the output of the regulator) and the controlled variable (the converter current) reduces to:

$$I_{SC} = \frac{V_{SC,1}}{s\cdot L}\cdot\Delta D \tag{5.13}$$

In the digital implementation, there is one sampling delay between the actual calculation of the control input and its actuation by the PWM of the two switches in the bridge, as shown by Fig. 5.12. Moreover, the time-discrete nature of the control action is taken into account by adding an extra delay equal to half of the sampling period. As a result, the transfer function in (5.13) is corrected as:

$$I_{SC} = \left(\frac{V_{SC,1}}{s\cdot L}\cdot\frac{1}{1+T_{del}\cdot s}\right)\Delta D; \qquad T_{del} = \frac{3\cdot T_s}{2} \tag{5.14}$$

Given the simplicity of (5.14), a standard P-I controller has been employed; the controller is then implemented in digital form for calculation by the DSP as [88]:

$$\Delta D(k) = K_P\left(1+\frac{T_s}{T_i}\cdot\frac{z}{z-1}\right)\cdot\left(I_{SC,ref}(k) - I_{SC}(k)\right) \tag{5.15}$$

With the z-operator representing a time shift corresponding to one sampling instant:

$$u(k+1) = z\cdot u(k); \qquad u(k-1) = z^{-1}\cdot u(k) \tag{5.16}$$

The regulator gain and time constant are calculated in order to maximize the achievable phase margin, according to the well-known method of symmetrical optimum [89], resulting in the expressions:

$$K_P = \frac{L}{2\cdot V_{SC,1}\cdot T_{del}}, \qquad \frac{T_s}{T_i} = \frac{1}{6} \tag{5.17}$$

The gain above is not constant, due to the term $V_{SC,1}$; however, that term is known (measured) and very slowly varying, compared to the dynamics of the control loop, making the real-time adaptation of the regulator gain in (5.17) possible.
As reported in the literature [90], the closed loop system designed according to the criterion of symmetrical optimum will have a step response characterized by 43% overshoot, $3.7 \cdot T_{del}$ rise time and $16.3 \cdot T_{del}$ settling time. Such a high overshoot is not desirable in a current controller, and some kind of reference shaping is normally used [90].
Fig. 5.13 shows the step response of the main current in the real-scale prototype when the controller has been tuned according to (5.17). It is apparent that the current response has lower overshoot and slower response than what was expected.
This is believed to be caused by the following:

- Actual inductance, at this current level, is much higher than the one used in the calculation of the controller gain (more than 0.2 *mH* instead of the nominal 0.13 *mH*, as reported in Table 5.5). More details about this discrepancy are given in section 5.4.1.
- There is a considerable damping effect due to the resistive components on the current path that are not modelled by (5.14). Main contribution is the ESR of the supercapacitors, but also the IGBTs and the inductor itself have their own losses. If necessary, those resistive components can be inserted into the model and the controller can be more precisely tuned. However, in this particular case, the additional damping only increases the stability of the closed loop system, and the experimental response in Fig.5.13 is assumed to be satisfactory.

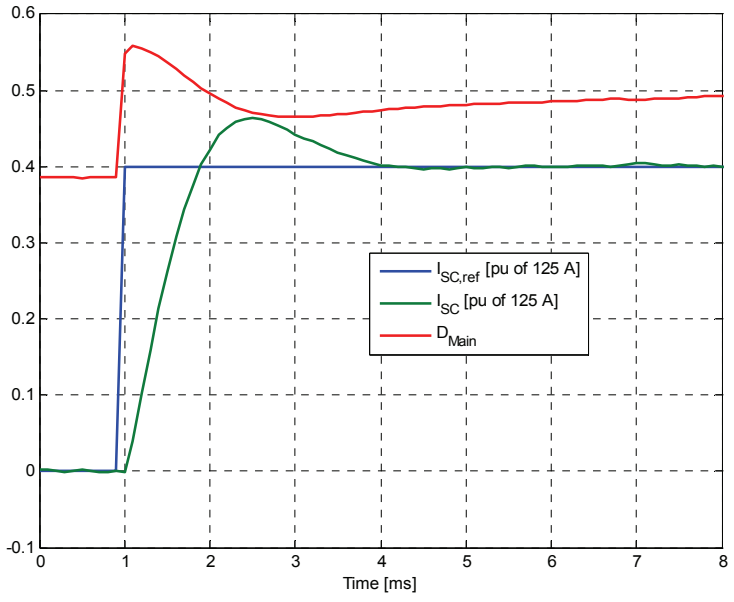


Fig. 5.13 – Experimental step response of the main converter current in the full-scale prototype.

5.3.2 Voltage balancing algorithm

The balancing process has been described in detail in chapter 4.2, and the control diagram is given in Fig. 4.8. Structure of the inner balancing current control loop is

identical to the current loop described in the previous paragraph. The feed-forward term for the duty cycle of the balancing bridge is:

$$D_{FF,bal} = \frac{V_{SC,0}}{V_{SC,0} + V_{SC,1}} \tag{5.18}$$

The transfer function between the output of the current regulator and the balancing current is therefore:

$$I_{bal} = \left(\frac{V_{SC,0} + V_{SC,1}}{s \cdot L} \cdot \frac{1}{1 + T_{del,bal} \cdot s} \right) \Delta D_{bal} \tag{5.19}$$

In order to minimize the size of the inductor, the switching frequency of the balancing bridge is selected to be 40 *kHz*. However, the balancing control algorithm is still executed every 100 μs (10 *kHz* rate). The total delay time in the control action is therefore:

$$T_{del,bal} = T_s + \frac{T_{sw}}{2} = \frac{9}{8} T_s \tag{5.20}$$

The symmetrical optimum criterion yields the following gains for the P-I controller:

$$K_{P,bal} = \frac{L_{bal}}{2 \cdot \left(V_{SC,0} + V_{SC,1} \right) \cdot T_{del,bal}}, \qquad \frac{T_s}{T_{i,bal}} = \frac{2}{9} \tag{5.21}$$

As a result, the closed-loop transfer function of the balancing current control becomes:

$$W_{Ibal,cl} = \frac{I_{bal}}{I_{bal,ref}} = \frac{1 + 4 \cdot T_{del,bal} \cdot s}{1 + 4 \cdot T_{del,bal} \cdot s + 8 \cdot T_{del,bal}^2 \cdot s^2 + 8 \cdot T_{del,bal}^3 \cdot s^3} \tag{5.22}$$

The outer loop for voltage balancing employs a simple proportional controller, which is enough to ensure zero steady-state error, due to the pole in the origin introduced by the relationship between the balancing current and the voltage redistribution among the SC banks, as seen in (4.10), and more explicitly expressed in the following:

$$\Delta V_{SC,1} - \Delta V_{SC,0} = \Delta V = \left(\frac{1 + (x - 1) D_b}{s \cdot C_{SC,0}} \right) I_{bal} \tag{5.23}$$

The expression above describes a pure integrator with a slowly variable gain, since the duty cycle of the balancing bridge is not constant during the balancing process. However, we can assume the duty cycle to be almost equal to 0.5 during normal converter operation (meaning $V_{SC,0} \approx V_{SC,1}$), and (5.23) simplifies into:

$$\Delta V_{SC,1} - \Delta V_{SC,0} \approx \left(\frac{1 + x}{s \cdot 2C_{SC,0}} \right) I_{bal} \tag{5.24}$$

Since the dynamics of the integrator above is much slower than the dynamics of the current control in (5.22), the latter can be assumed as instantaneous, as far as the design of the proportional gain for voltage balancing is concerned, resulting in the simplified system of Fig. 5.14.

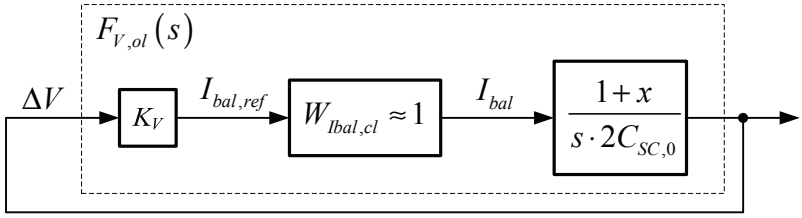


Fig. 5.14 – Simplified system for design of voltage balancing control loop.

Such a system has 90 degrees phase margin for any value of the proportional gain K_V, since we have neglected the faster dynamics of the current control loop. In practice, a high gain is neither necessary nor effective, since the convergence speed of the voltage balancing process is mainly determined by the maximum allowed balancing current, as clearly shown in Fig. 5.16.
In the thesis, the proportional gain is calculated so to obtain the maximum balancing current (10 A in the experimental setup) for a given voltage unbalance threshold $\Delta V_{bal,thr}$, fixed to 10 V in the experiments. As a result:

$$K_V = \frac{I_{bal,Max}}{\Delta V_{bal,thr}} = \frac{10[A]}{10[V]} = 1\left[\Omega^{-1}\right] \tag{5.25}$$

Bode plots of the resulting open-loop transfer function $F_{V,ol}$, taking also into account the dynamics of the inner current control loop are shown in Fig. 5.15. As expected, the phase margin is very close to 90 degrees.

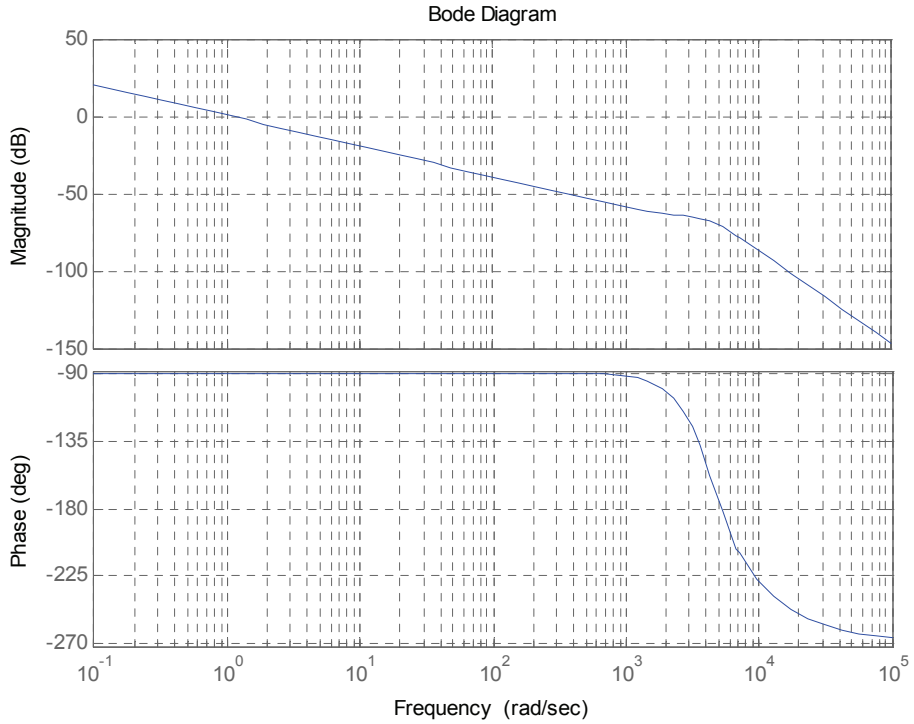


Fig. 5.15 – Bode plot of the open-loop transfer function of the voltage balancing process.

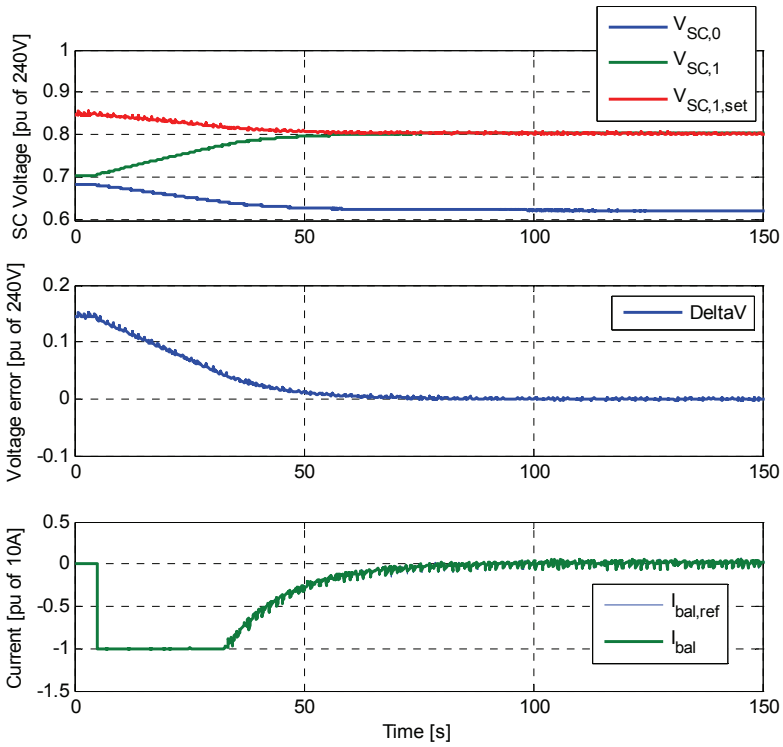


Fig. 5.16 – Experimental response of the voltage balancing system, starting from considerable unbalance.

5.4 Experimental Results

Due to the unavailability of a real traction battery, the SC-based power buffer has been tested by connecting its terminals to the 220 *V* DC network available in our laboratory facility at NTNU. The DC network is obtained from the AC mains by means of a standard, thyristor-based, bidirectional converter that also controls the voltage level. The dynamic behaviour of such a DC source is therefore different from that of a traction battery, especially during quick transients. However, the steady state characteristics are similar, making the tests meaningful.

Practical limitations introduced by the available voltage source are:

- The DC voltage level is limited to 220 *V*, while the power buffer has been designed to work with a traction battery having a nominal OCV of about 280 *V*, as seen in Table 5-2. In particular, the SC banks have a rated voltage of 240 *V*, which cannot be fully exploited.
- The current in and out the DC source is limited to 100 *A* by the installation. Rated current of the power buffer is 125 *A* (30 *kW* at 240 *V*), meaning that only 80% of the rated buffer current can be used for testing. Overall, power can be cycled in and out the SC-based buffer at a maximum rate of 22 *kW*, instead of the design value of 30 *kW*.

In a typical application, such as the one in Fig. 5.3, the power buffer helps the primary energy source to supply a time-varying load. In the lab experiments, however, there is no additional load, and the whole power flows between the SC-based buffer and the DC network emulating the battery. This configuration still allows for testing of the power

buffer, but cannot be used to assess the performances of the hybridized energy source, where the presence of the load is essential.
The configuration of the system used in the laboratory to test the behaviour of the proposed SC-based power buffer is shown in Fig. 5.17.

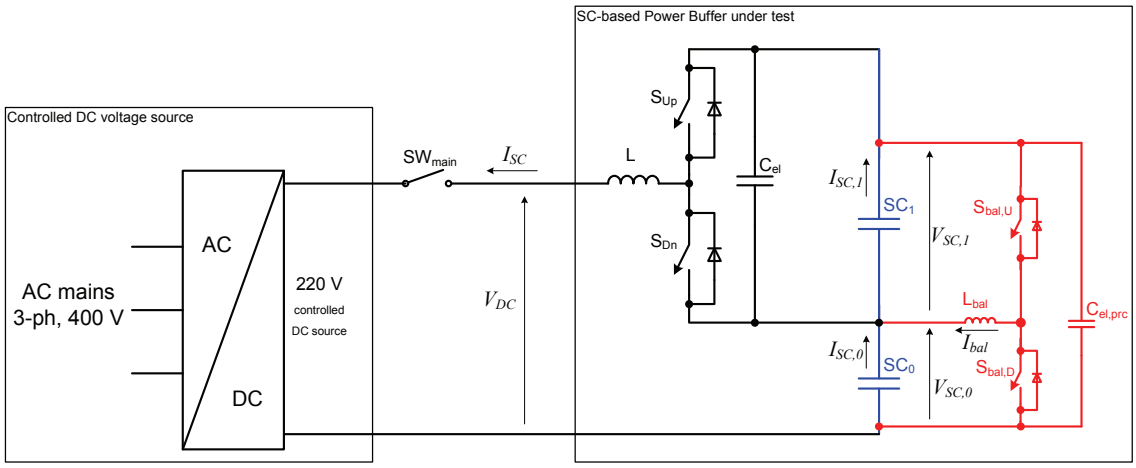


Fig. 5.17 – Experimental setup for testing of proposed power buffer.

5.4.1 Switching waveforms

The experimental results in Fig. 5.18 show the switching components of the different currents within the power buffer. As predicted by (3.51), the ripple on the output current of the SC-based buffer I_{SC} varies with the duty cycle of the main converter, which is in turn a function of the SOC of the SC banks. When the SC-buffer is close to full (Fig. 5.18-a), the ripple is very small, and reaches its maximum for a duty cycle of about 0.42, corresponding to an intermediate SOC of the buffer (Fig. 5.18-b). Ripple also increases when the DC component (the useful one) of I_{SC} increases, due to saturation of the inductor core (Fig. 5.18-c and Fig. 5.18-d).
Experimental data reveals an effective value of the smoothing inductance of about 2.0 *mH* at 100 *A*, which is considerably higher than the design value of 0.13 *mH* at 125 *A* given in (5.7) and Table 5-5. The reason for such a difference is a mistake made during the assembly of the inductor, resulting in a total airgap shorter than the design value of 3.3 *mm*. The higher inductance is no problem for the converter operation (ripple is reduced), but a shorter airgap increases the flux density in the inductor core, decreasing the peak current capability of the inductor from its design value. Fortunately, no hard saturation arises at 100 *A*, and the inductor can be safely used in the experiments. However, for the DC current level to be raised to the design value of 125 *A*, and for the inductor to be able to operate at higher core temperature, the airgap length has to be increased according to Table 5-5.
The switching ripple on the balancing current I_{bal} is almost independent of the SOC of the power buffer, since the duty cycle of the balancing bridge is always around 50%, as shown in the experiments of Fig. 5.18. Peak-to-peak ripple of about 2 *A* has been achieved by using a relatively high switching frequency of 40 *kHz*, as compared to the main bridge that is operated at 10 *kHz*, as it is evident from the figures.

Fig. 5.18-d shows that the ripple on the current $I_{SC,1}$, flowing through the SC bank SC1, is very small, indicating that the whole switching ripple in (3.52) is actually absorbed by the electrolytic capacitor C_{el} in Fig. 5.17.

5.4.2 SC-based power buffer operation

The experiment in Fig. 5.19 is intended to prove the validity of the theory developed in chapter 3, regarding the prediction of the charge/discharge trajectory of the two SC banks by (3.20). Since the power cycling takes place at low rate (within 0.15 pu of the rated buffer current), there are little losses in the system, and the trajectory of the voltage across the bank SC1 closely follows the ideal one, with no need for forced balancing. The small difference between the ideal trajectory $V_{SC,1,ref}$, calculated by (3.20), and the actual one $V_{SC,1}$ is due to the following second-order factors:

- Though small, losses in the system are not exactly zero;
- The capacitance of the two banks may differ from the nominal values, due to production tolerances;
- The theory of double layer capacitors predicts that capacitance is varying with the operating voltage, and this aspect is neglected by (3.20);
- The DC-link voltage is not exactly constant;
- There are unavoidable measurement errors that are integrated over the very long time of the experiment, causing a small drift.

The situation is quite different in the experiment of Fig. 5.20, where the level of power exchanged between the SC-based buffer and the DC-link is close to rated. In this case losses are no longer negligible, and the DC-link voltage is far from being constant, due to the droop characteristics of the voltage regulator embedded in the AC/DC converter used to control the DC-link. As a result, the actual voltage trajectory quickly drifts away from the ideal one, as theoretically predicted in chapter 4.

Fig. 5.21 is the experimental test corresponding to the simulation in Fig. 4.5, where rated power is cycled in and out the SC-based buffer. Losses cause the controlled bank SC1 to be depleted after few cycles, with consequent loss of power cycling capability. Experiments agree with the simulation, confirming the need for dynamic balancing in real-world applications.

The same power cycles are repeated in the experiment of Fig. 5.22, which is the equivalent of the simulation in Fig. 4.9. The balancing process is shown to be effective, allowing for continuous cycling without loss of energy storage capability. In the experiment, the current limitation of the dynamic balancing circuit is fixed to 10 A. Such a low current is not enough to allow for perfect voltage tracking, and $V_{SC,1}$ differs from $V_{SC,1,ref}$ during hard transients; however, the voltage is brought back to the ideal value as soon as the power flow decreases and the balancing action overcomes the effect of losses. According to the drive cycles simulations in section 2.2.2, the periods of high power request from the SC-buffer are interleaved with relatively long rest periods, making a more powerful balancing circuit unnecessary.

The experiment in Fig. 5.23 shows what happens if the topological charge-limiting constrain expressed by (3.2) is reached, and the supervising system is still trying to push energy into the SC-buffer. Due to the presence of the diode across the switch S_{Dn} (see

Fig. 5.17), the voltage $V_{SC,0}$ is clamped, and the buffer current I_{SC} can no longer be controlled by the duty cycle of the main bridge. The resulting condition is a dynamic equilibrium described by the equation:

$$I_{SC}(t)=\frac{V_{SC,0,oc}(t)-V_{DC,oc}}{\left(R_{DC}+ESR_{SC,0}\right)}=\frac{V_{SC,0,oc}(0)-V_{DC,oc}-\frac{1}{C_{SC,0}}\cdot\int_0^t I_{SC,0}(\tau)\,d\tau+}{\left(R_{DC}+ESR_{SC,0}\right)} \tag{5.26}$$

Above, $V_{DC,oc}$ and $V_{SC,oc}$ are the open circuit voltages of the DC source and the bank SC0, respectively; R_{DC} is the equivalent resistance due to the droop characteristic of the DC source; sign notation is according to Fig. 5.17, and the initial time is the time when the self-limiting mode is entered. In the derivation of (5.26), the contribution of the inductance is neglected, since the associated time constant is orders of magnitude shorter than the one associated to the SC bank.
The solution of (5.26) is easily determined as:

$$I_{SC}(t)=I_{SC}(0)\cdot e^{-t/\tau},\qquad \tau=\left(R_{DC}+ESR_{SC,0}\right)\cdot C_{SC,0} \tag{5.27}$$

As long as the DC-link voltage is not higher than the rated voltage of the bank SC0, operating in such a self-limiting mode is perfectly allowed.
It should be noticed that even if the charging current cannot be controlled to any value below the equilibrium threshold resulting from (5.27), current control is immediately restored if the reference is put above such a threshold, as demonstrated by the experiment.
A similar situation arises if the discharge of the SC-buffer is extended beyond the topological limit imposed by (3.1), as shown by the experiment in Fig. 5.24. In this case the dynamic equilibrium is described by the equation:

$$\begin{aligned} I_{SC}(t)&=\frac{V_{SC,0,oc}(t)+V_{SC,1,oc}(t)-V_{DC,oc}}{\left(R_{DC}+ESR_{SC,0}+ESR_{SC,1}\right)}\\ &=\frac{V_{SC,0,oc}(0)+V_{SC,1,oc}(0)-V_{DC,oc}-\left(\frac{1}{C_{SC,0}}+\frac{1}{C_{SC,1}}\right)\cdot\int_0^t I_{SC,0}(\tau)\,d\tau}{\left(R_{DC}+ESR_{SC,0}+ESR_{SC,1}\right)} \end{aligned} \tag{5.28}$$

The solution is still a decaying exponential:

$$I_{SC}(t)=I_{SC}(0)\cdot e^{-t/\tau},\qquad \tau=\left(R_{DC}+ESR_{SC,0}+ESR_{SC,1}\right)\cdot\frac{C_{SC,0}C_{SC,1}}{C_{SC,0}+C_{SC,1}} \tag{5.29}$$

Operating the power buffer in this mode poses no problem to the integrity of the components; current controllability is recovered as soon as the current reference is set below the dynamic current threshold defined by (5.29), as confirmed by the experiment.

5.4.3 SC-based power buffer efficiency

It is of utmost importance to determine the charge/discharge efficiency that can be achieved by the proposed SC-based power buffer, especially when high power has to be cycled in and out the SC banks.

Fig. 5.25 shows the procedure adopted for the calculation of efficiency. The buffer is first charged at maximum allowed power, and the DC-link voltage V_{DC} and the current I_{SC} are recorded. Energy supplied by the DC source during the charging process, lasting for the time T_{chg} is then numerically evaluated as:

$$E_{chg} = \int_0^{T_{chg}} V_{DC}(t) \cdot I_{SC}(t)\, dt \tag{5.30}$$

After some time, the buffer is fully discharged at maximum power, and the energy sent back to the DC source is computed as:

$$E_{dis} = \int_0^{T_{dis}} V_{DC}(t) \cdot I_{SC}(t)\, dt \tag{5.31}$$

Since the final energy stored in the SC bank after the discharge process is the same as the initial energy stored before the beginning of charge, the energy dissipated throughout the whole cycle is simply given by:

$$E_{loss,cycle} = E_{chg} + E_{dis} \tag{5.32}$$

and the average power dissipated during the cycle is:

$$P_{loss,cycle} = \frac{E_{chg} + E_{dis}}{T_{chg} + T_{dis}} \tag{5.33}$$

The cycle efficiency is then calculated as:

$$\eta_{cycle} = \frac{\left(T_{chg} + T_{dis}\right) \cdot P_{loss,cycle}}{E_{chg} - E_{dis}} \tag{5.34}$$

In practice, the procedure above is iterated over *n* consecutive cycles, and results are averaged, in order to minimize the effect of measurement errors. Rest periods between successive charges and discharges have been inserted, in order to give enough time to the dynamic balancing to equalize the bank voltages thus allowing for stable cycling, as explained in an earlier section. Rest periods (equalizing periods) do not significantly affect the calculation of losses or efficiency, since the main bridge is not operated during rest time, and the only energy dissipated during those periods is due to the low-power balancing circuit, that is assumed to be negligible.

Following the aforementioned procedure, the average cycle loss related to the experiment in Fig. 5.25 has been quantified in about 1.2 *kW*.

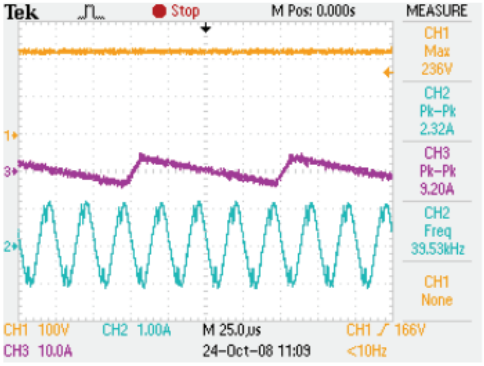
In order to prove the consistency of this result, a theoretical calculation of losses during a constant power cycle has been carried out, according to the equations developed in section 3.4, and the results are summarized in Table 5.6.

Given the general difficulty of getting accurate measurements of power losses as difference between two relatively big quantities, as described by (5.33), the agreement between the theoretical calculations and the measurements is surprisingly good.

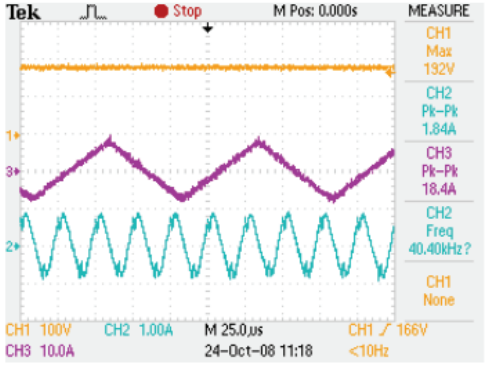
Moreover, the experimental cycle in Fig. 5.25 differs somewhat from the theoretical one assumed in the calculations of Table 5-7, since the actual cycle cannot be extended to the theoretical limits due to the presence of equivalent series resistances, and since the actual discharge trajectory of the bank SC1 does not follow exactly the theoretical one on which calculations are based. It is therefore likely that different sources of error have acted in opposite directions, cancelling each other.
Nonetheless, it is certainly possible to conclude that measured losses are in the order of magnitude that is predicted by the theory, and the resulting efficiency of the experimental prototype of the SC-based power buffer is satisfactory.

Table 5-7 –.Theoretical system losses averaged over a complete discharge cycle at 100 A current

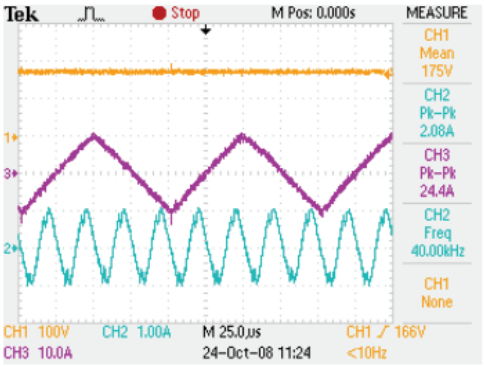
Component	Conditions	Equation	Calculated. losses
Bank SC0	$ESR = 56.7\ m\Omega$	(3.56)	567 W
Bank SC1	$ESR = 103.5\ m\Omega$	(3.56)	212 W
Solid state switches, conduction	$V_{f,0} = 1V;\quad R_f = 8\,m\Omega$	(3.72)	180 W
Solid state switches, switching	$E_{SW,tot} = 17\,mJ\,@\,300V, 100A$ $f_{sw} = 10\,kHz$	(3.74)	125 W
DC inductor	Table 5.5	-	86 W
Smoothing capacitor	$ESR = 10\ m\Omega$	(3.83)	17 W
Total			1187 W
Cycle efficiency	$P_{cycle} = 220V \cdot 100A = 22.0kW$		94.7 %



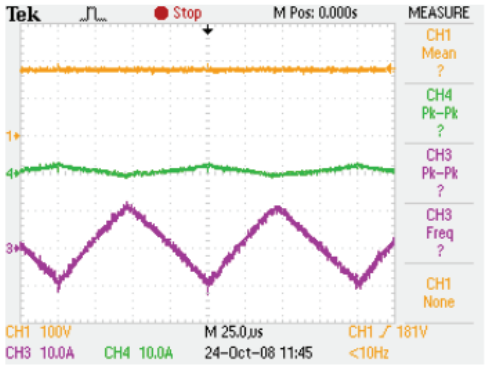
(a) – SC banks close to full; No load.



(b) – SC banks at intermediate SOC; No load.



(c) – SC banks at intermediate SOC; 100 *A* load.



(d) – SC banks at intermediate SOC; 100 *A* load.

Ch1 (orange): Voltage across SC1, $V_{SC,1}$ (100 V/div);

Ch2 (cyan): AC component of balancing current, I_{bal} (1 A/div);

Ch3 (purple): AC component of power buffer output current, I_{SC} (10 A/div);

Ch4 (green): AC component of current through the bank SC1, $I_{SC,1}$ (10 A/div);

Fig. 5.18 – Switching ripple on the currents of the SC-based power buffer.

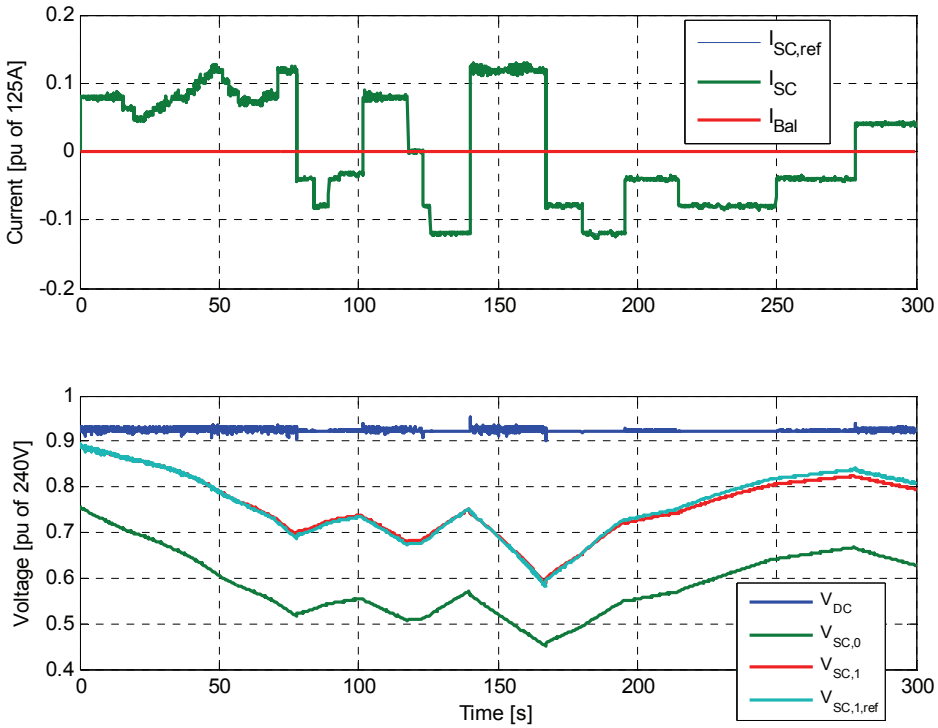


Fig. 5.19 – Cycling with arbitrary load current shape, at low power level, with no balancing action.

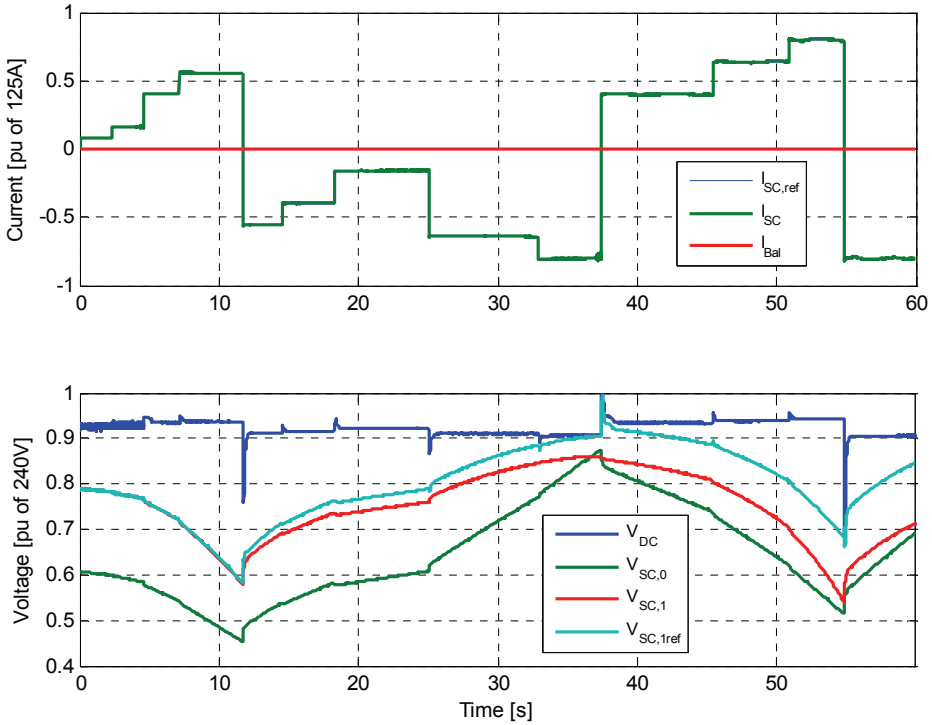


Fig. 5.20 – Cycling with arbitrary load current shape, at high power level, with no balancing action.

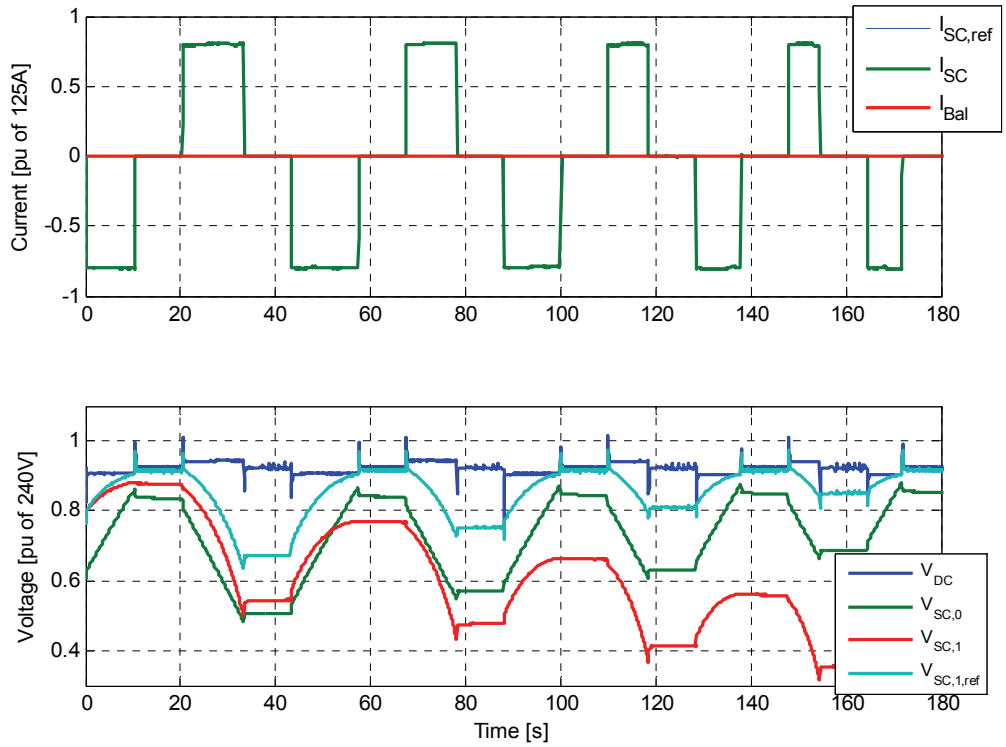


Fig. 5.21 – Cycling with constant power, with no balancing action.

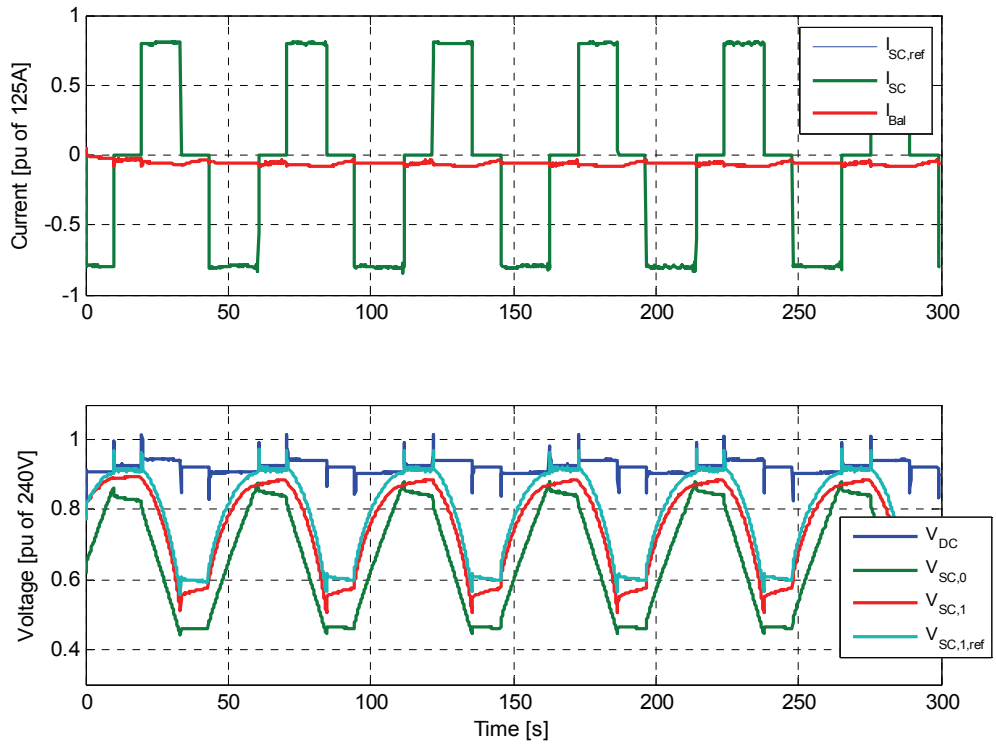


Fig. 5.22 – Cycling with constant power, with balancing action.

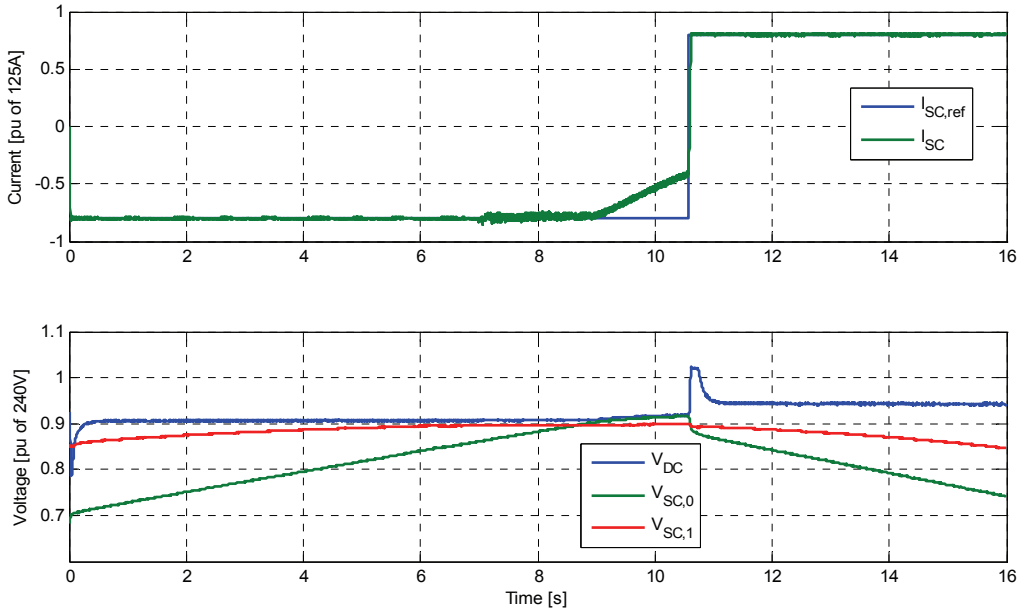


Fig. 5.23 – Charge limit of the SC-based power buffer with HC converter topology.

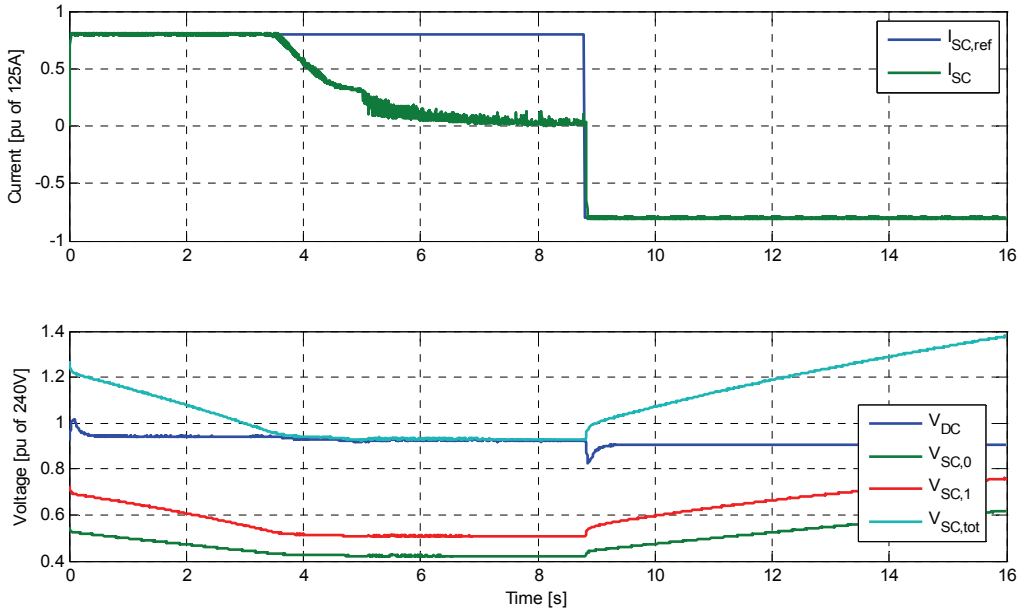


Fig. 5.24 – Discharge limit of the SC-based power buffer with HC converter topology.

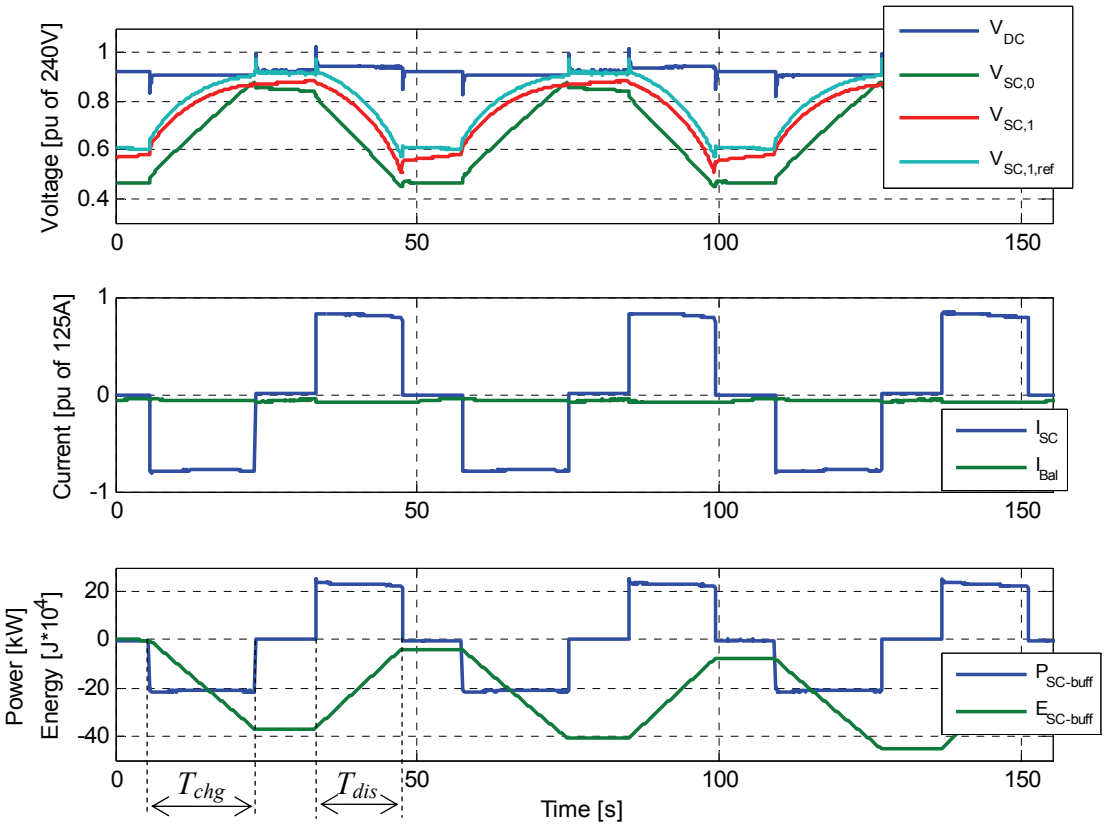


Fig. 5.25 – Cycles at constant power, with calculation of losses and cycle efficiency.

6 DISTRIBUTED INVERTER STRUCTURE BASED ON CASCADED H-BRIDGE TOPOLOGY

This chapter describes the concept of a redundant, self-healing architecture for the implementation of the traction inverter in the drive system of an EV. A multilevel structure based on cascaded H-bridges, particularly well suited for battery EVs, is used to develop a decentralized, modular topology featuring a high degree of reliability.
Most of the content has been published in [91], but additional information can be found in the thesis, mainly about the proposed and developed control strategy and the dedicated serial protocol that has not been previously published.

6.1 Introduction

Multilevel power electronics converters based on cascaded H-bridge are well known in the literature [92] and have been mainly used in high power applications due to their potential of achieving very low harmonic distortion with moderate switching frequency [93]. Their application as main interface converter between the battery system and the motor of electric vehicles has also been proposed in [94], taking advantage of other characteristics of the topology that are particularly beneficial in automotive:

- The galvanically isolated power supplies for all the H-bridges are readily available by properly arranging the connections of the battery pack;
- Due to the low frequency and low voltage switching, EMI emissions can be reduced, compared to a standard inverter topology;
- When not operating, the highest voltage present in the system is the DC-bus voltage of each H-bridge that can be designed as low as 42 V, resulting in a system that is safer to access and service.

Here, the idea is taken a step further by considering the multilevel-multicell topology as a distributed system, in order to make full use of its inherent redundancy. By proper design of both hardware and software control structure, the system is able to maintain its operation in the event of different kind of failures, making it an ideal candidate for applications where reliability and availability are the most important issues.

6.2 System Description

The modular structure of the drive system based on the cascaded H-bridge topology is shown in Fig. 6.1. A system with a 3-phase AC motor is considered, as that is the commonest configuration found in practice, but the principle can easily be extended to supply a motor with any number of phases, or even a DC motor.

Each phase of the distributed converter is made up of *N* series connected building blocks that are functionally equivalent to controllable voltage sources. This is achieved by providing each building block with an isolated DC voltage source and an H-bridge, as shown in Fig. 6.2.

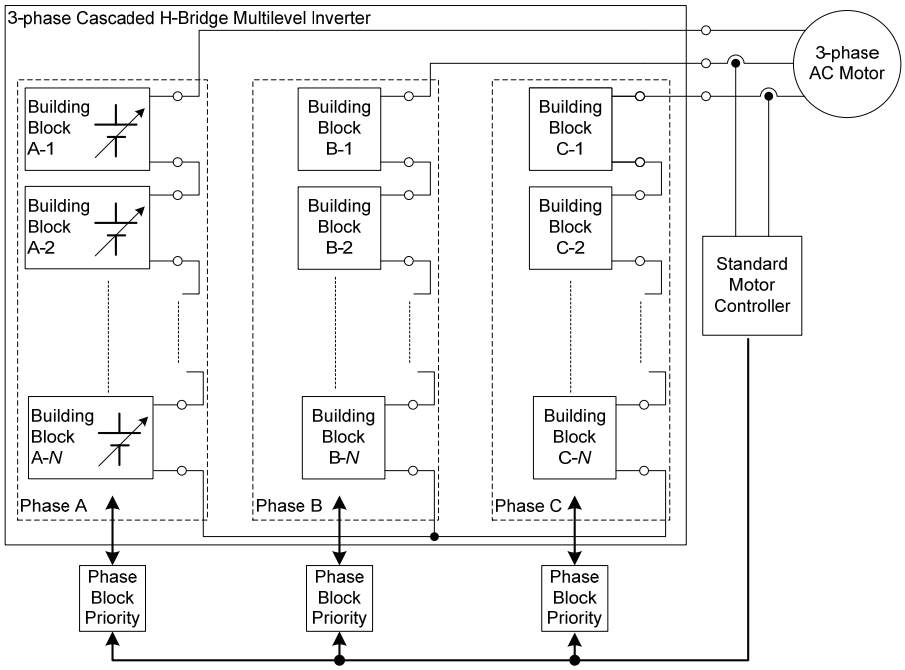


Fig. 6.1 – 3-phase configuration of a cascaded multicell architecture based on identical building blocks.

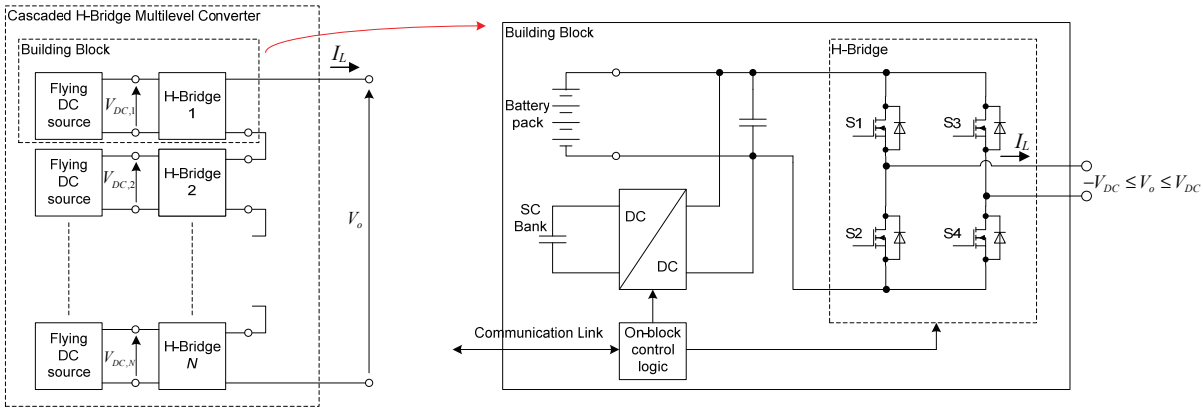


Fig. 6.2 – Basic Cascaded H-Bridge Multilevel converter (one phase), and related building block

In the figure, a hybridized source including an SC-based power buffer is considered, as the one extensively described in the previous chapters; however, it is pointed out that

the nature of the isolated DC source is of no relevance for the operation of the cascaded structure, and a simple battery could just as well be used.
Each building block is equipped with local control logic, responsible for the interaction of the block with the rest of the system. Typically the block is able to determine the local energy and voltage availability, as well as the local state of health, and is able to communicate all the "state" information to the outside, through the communication link. At the same time, the block receives from the outside the command about the voltage that should be generated at the output terminals during the next switching period.
The motor controller in Fig. 6.1 is any standard algorithm, like for instance vector control for AC motor. It takes phase current (and possibly speed) measurements as inputs and calculate desired phase voltages to be generated by the converter at the motor terminals in order to achieve the desired torque and speed.

6.3 Operating Principle and Dynamic Charge Balancing

With reference to Fig. 6.2, at any given instant each building block equipped with a DC voltage source of value V_{DC} is able to generate at its output terminals three different voltage levels:

$$\begin{cases} +V_{DC} & \text{if S1 and S4 are ON;} \\ -V_{DC} & \text{if S2 and S3 are ON;} \\ 0 & \text{if S1 and S3 are ON, or S2 and S4 are ON;} \end{cases} \tag{6.1}$$

In the very common case of identical DC voltage sources for all the N building blocks in a phase leg, the resulting output (phase-to-neutral) voltage of the converter in Fig. 6.2 is then discretized with $(2N+1)$ levels, the output voltage step being equal to the individual DC voltage V_{DC}. Several different techniques can then be used to generate the desired average output voltage over a given switching period T_{sw} [95,96].
Here, a PWM technique similar to the one in [97] is used. The idea is to operate all but one building block in continuous mode over a switching period, in order to minimize switching losses.
An important characteristic of the cascaded topology is that all individual blocks in a given phase chain are indistinguishable, as far as output voltage generation is concerned, provided they all have the same DC voltage behind the H-Bridge. This degree of freedom is exploited to achieve charge balancing among the N energy sources in the phase leg.
Let us suppose that we need to generate a given positive output voltage V_o over a switching period. In general, an integer $\bar{N}$ will exist, so that:

$$\bar{N} \cdot V_{DC} \le V_o \le \left(\bar{N}+1\right) \cdot V_{DC}, \text{ with } 0 \le \bar{N} \le N-1 \tag{6.2}$$

One way to generate the desired voltage is to divide the N blocks into three categories. $\bar{N}$ blocks will be operated in "fully on" mode, each contributing with V_{DC} to the output voltage. One block will be operated in PWM mode, with a duty cycle:

$$D = \frac{V_o - \bar{N} \cdot V_{DC}}{V_{DC}} \tag{6.3}$$

The remaining $N-\bar{N}-1$ blocks will be operated in "zero" mode, as described in (6.1). As a result:

$$V_o = \bar{N} \cdot V_{DC} + D \cdot V_{DC} \tag{6.4}$$

The same method applies to negative output voltage, with the only difference that the "fully on" blocks and the block doing PWM will all generate negative output voltage. It is apparent that the one described above is not the only method to generate a given output voltage. For instance, a pair of blocks operated in "zero" mode could instead be operated in "fully on" mode, generating positive and negative voltage, respectively, annihilating each other.

The degrees of freedom in output voltage generation can be used to balance the load of each independent source behind the H-Bridges. From the switches topology depicted in Fig. 6.2, it is apparent that for a given load current I_L, the current flowing through the DC source behind the bridge is I_L itself if the block output voltage is $+V_{DC}$, $-I_L$ if the block output voltage is $-V_{DC}$; no current flows through the DC source when the block output voltage is zero. As a result, assuming V_o and I_L positive (reasoning is reversed in case of discordant signs of output voltage and load current), if the voltage generation method described in the previous chapter is used, in a switching period T_{sw}, $\bar{N}$ sources will deliver the same amount of energy to the load:

$$E_1 = T_{sw} \cdot V_o \cdot I_L \tag{6.5}$$

The block doing PWM will deliver a smaller amount of energy to the load:

$$E_2 = D \cdot T_{sw} \cdot V_o \cdot I_L \tag{6.6}$$

All the remaining blocks will deliver no energy to the load.

Whatever the technology employed for the N DC sources, they will always be characterized by a certain amount of stored energy. In order to optimize the performance of the system, it is mandatory that all the sources participate evenly to the energy trade with the load. In more precise terms, the SOC of all sources should be kept balanced at all times. In order to achieve balancing, the SOC of all sources is periodically evaluated by the local logic of each building block (see Fig. 6.2) and sent to the respective Phase Block Priority calculator. If in the switching period to come the energy will flow from sources to load (V_o and I_L have the same sign), highest priority for voltage generation is given to the block with highest SOC, while lowest priority is assigned to the most discharged source. Highest priority means that the block will be the first one to be operated in "fully on" mode, thus contributing with the maximum amount of energy given by (6.5). On the other hand, the block with lowest priority will be most likely operated in "zero" mode (unless output voltage close to the maximum limit is required), thus preventing further discharge. The Phase Block Priority block then calculate the duty cycle of each block in its phase leg, according to the priority, and send that information to the building blocks.

From the reasoning above, it should be clear that the N DC sources forming the basic cascaded converter need not be identical. As long as SOC can be evaluated accurately, ideal utilization of sources is still possible even in case of sources with different energy storage capabilities.

6.4 Redundancy and Self-Healing properties

The basic definition of redundancy implies that the system must be able to maintain its operation even after a certain number of faults have happened.
Self-healing is defined as the ability of the system to automatically reconfigure itself following a permanent fault, and restore operation.
In the architecture of Fig. 6.2, all N blocks of a phase leg are equivalent, and the phase output voltage is the sum of the individual blocks output voltage. That implies that if any one of the blocks is out of order, the remaining $N-1$ blocks can still operate provided that the faulty block has its output terminals short-circuited. Obviously, the voltage capability of the phase leg is reduced by a factor $1/N$, showing that if the number of levels increases, the derating following a fault becomes smaller.
As far as a block fault is concerned, self-healing can be achieved by putting a relatively inexpensive relay in parallel with the bridge output, thus bypassing the block. It is responsibility of the local control logic of each building block to detect the fault, bypass the output and communicate to the outside the block inability to participate to the voltage generation process.
It may be argued that losing a block will also reduce the driving range by the same factor as the voltage ($1/N$), since one battery pack is no longer used. If the fault is in the battery pack itself, then the loss in driving range is unavoidable, but if the fault is in the H-bridge, the energy stored in the battery pack can still be used by properly arranging the connections between the N H-Bridges and the N battery packs in the system. This is shown in Fig. 6.3 for the particular case of N=5. If the H-bridge of the block x (x=1..N) is faulty, the corresponding battery pack is then connected to the H-bridge of either block $x-1$ or $x+1$, which will therefore have a source with double capacity compared to all the others. Using the charge balancing method described above, it is still possible to operate the system using the whole energy available.

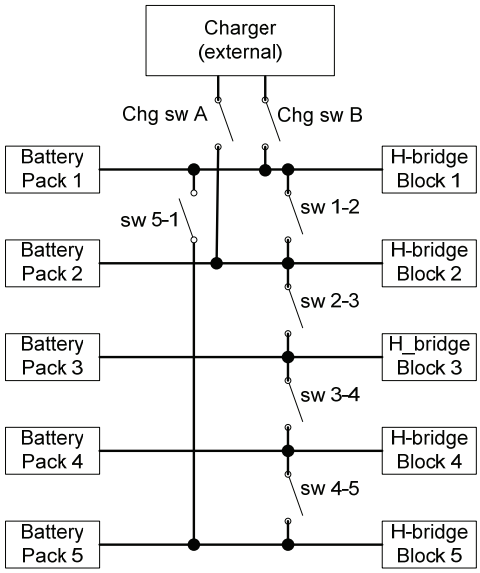


Fig. 6.3 – Ring connection of the battery packs for single H-bridge fault handling

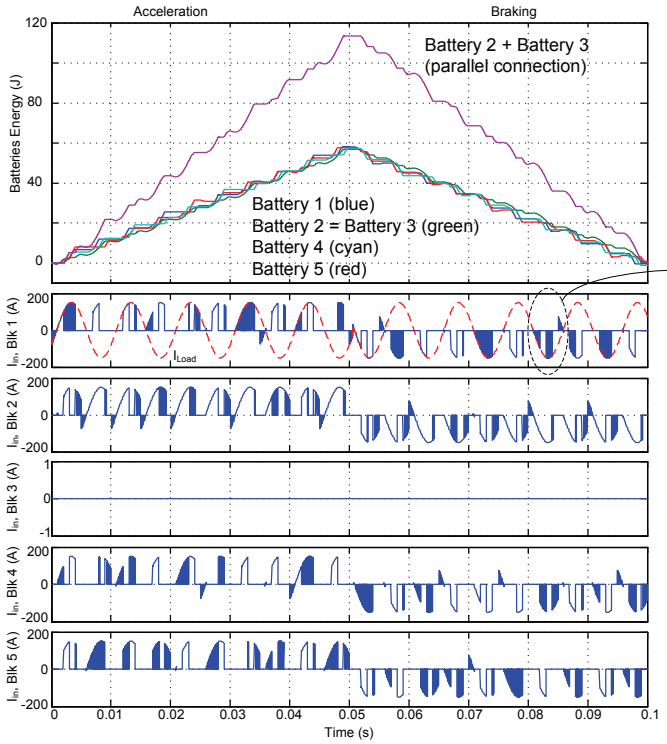
The on-board logic of the building block with the faulty H-bridge must be able to detect the fault and communicate the state to the outside. The supervising logic can then reconfigure the system according to Table 6-1, and resume operation.

Notice that the combination of switches in Fig. 6.3 (ring topology) will also allow for parallel charging of all battery packs from a single, low voltage charger, if desired. With a redundant charge switch, it is also possible to isolate a single faulty battery pack during parallel charging, as described in Table 6-1.

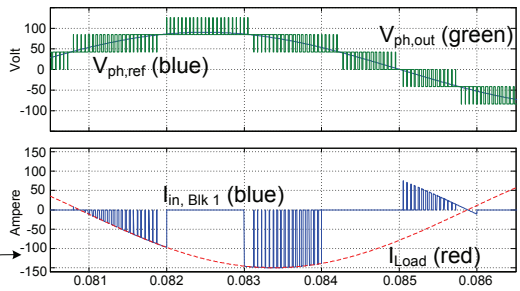
Table 6-1 – Battery pack connection

Operating Mode	**Charge Switches**	**Ring switches**
Normal operation	Both OFF	All OFF
Operation with Block *x* faulty	Both OFF	Switch *x*-*x*–1 (or *x*-*x*+1) ON All other switches OFF
Battery charge	Either or both ON	All ON
Battery charge with battery pack *x* faulty	ON if not connected to *x*	Switches *x*-*x*–1 and *x*-*x*+1 OFF; All other switches ON

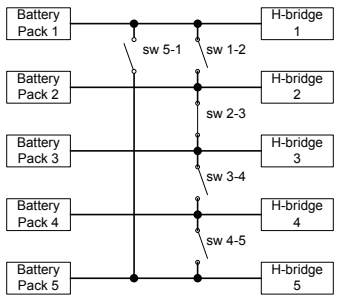
The single-leg system in Fig. 6.2 has been simulated to show its behaviour in case of a fault in one of the H-bridges. Results are shown in Fig. 6.4; during the simulation, the faulty H-bridge (HB3) is bypassed on the output side and the corresponding battery pack (BP3) is connected in parallel with one of the adjacent packs (BP2), resulting in a building block having double capacity.



(a) – Energy sharing during acceleration/braking with H-bridge 3 faulty and H-bridge 2 having double amount of energy available on the DC-side



(b) – Enlarged view of inverter output voltage (one phase) and input current to H-bridge 1



(c) – Battery packs connection in case of H-bridge 3 faulty

Fig. 6.4 – Simulation results; operation of a leg of the cascaded multicell converter with a faulty H-bridge

Throughout the simulation, the converter leg is controlled to output a sinusoidal voltage having a peak value of 90 *V*, and the load current is assumed to be purely sinusoidal, with constant amplitude of 150 *A* (peak); the load power factor is positive at first (p.f.=0.85), and becomes negative at *t*=0.05 s (p.f.= -0.85).
Results confirm that the charge-balance control algorithm successfully keeps the charge on each battery pack balanced, by properly handling the switching priorities. As a consequence, average current flowing through the source behind HB2 is twice than those of the other blocks. It is important to notice that even if HB2 has to process more power than in the case of a healthy system, the H-bridge is able to do so without overrating the solid state switches, since both rated current and rated voltage remain unchanged.
The fault in one of the five H-bridges constituting the leg reduces the output voltage capability by 20%; since each battery pack has a nominal voltage of 42 *V*, the maximum voltage that can be generated by the leg is 168 *V*. The voltage and current waveforms resulting from the proposed switching strategy can be seen in Fig. 6.4-b; since only one of the H-bridges is pulse width modulated in each switching period, the output voltage always have steps never exceeding the single battery voltage of 42 *V*. The battery-side current is discontinuous and, in addition to the fundamental DC and to the high frequency switching components, its spectrum has a low frequency component at twice the output frequency. This is peculiar of the cascaded multicell topology, and is inherited from the characteristics of single-phase systems; main problem with the additional, low frequency component of the DC-side current is that it poses some extra requirements on the smoothing capacitor that must be connected at the input of the H-bridge.

6.5 Design considerations

It will be assumed that a propulsion system for a city EV equipped with the AC motor in Table 6-2 has to be designed according to the converter topology discussed so far.

6.5.1 Selecting Number of Levels and Individual Voltage of Building Blocks

In the selection of the ideal voltage ratings of the single building block, many concurrent factors have to be considered, ranging from efficiency to safety. The problem is similar to the one faced by the consortium that developed the new 42 *V* automotive standard. It seems therefore reasonable to use that same voltage level for the building blocks. This choice yields the practical advantage of availability of high-volume, low-cost, automotive-graded devices for the implementation of the solid state switches of the H-bridges.
Once the block voltage is fixed, the number of levels is determined according to the maximum voltage requirement of the load:

$$N_{lev} \geq \frac{\sqrt{2} \cdot V_{ll,rms}}{1.15 \cdot \sqrt{3} \cdot V_{block,min}} = \frac{\sqrt{2} \cdot 220}{1.15 \cdot \sqrt{3} \cdot 32} = 4.9 \tag{6.7}$$

In the equation above, the minimum DC-side voltage of each block has been assumed as low as 32 *V*, resulting from typical end-of-discharge voltage of a lead-acid battery pack rated at 36 *V*. In the calculation, standard 3-phase PWM modulation with 3rd harmonic

insertion [98] has been considered, without any overmodulation. As a result, the number of building blocks per phase is fixed to 5, yielding an 11 steps waveform for the phase output voltage.

Table 6-2 – System specifications

AC Motor	
PM synchronous	3-phase, 220V, 3000rpm, 8 $poles$ P_{rat}=15kW, P_{peak}=40kW
Cascaded multilevel inverter	
Number of levels per phase	N=5
Voltage of each battery pack	36V (nominal)
Switching devices	Automotive MOSFET IRF3805S-7P 160A, 55V, $R_{DS,on}$=2.6$m\Omega$@T_j=25C
Individual SC bank (optional)	16 X BCAP0350 (2.5V, 350F)
Hypothetical 2-level inverter	
Battery voltage (DC-Link)	350 V
Switching devices	Trench IGBT SKM195GB066D 600V, 200A

Main characteristics of the multicell converter are reported in Table 6-2, along with the specifications of a hypothetical 2-level inverter that is functionally equivalent to the proposed multilevel structure.

6.5.2 Efficiency and EMI considerations

At first glance, it appears that increasing the number of levels will have detrimental effect on efficiency. In fact, the number of switching devices along the load current path (phase-to-phase) is always 4N, resulting in 4N times the conduction losses (ohmic losses in case of unipolar devices like MOSFETs) of a single device. By comparison, in the standard 3-phase inverter there are only two devices on the phase-to-phase current path. However, for technological reasons, the on-state resistance of MOSFETs of the same current ratings tends to increase exponentially with the blocking voltage capabilities. In particular, it can be shown that for an ideal MOSFET structure, the resistance per unit area $R_{on,sp}$ of a device is [99]:

$$R_{on,sp} = K \cdot \left(BV_{pp} \right)^{2.5} \tag{6.8}$$

where BV_{pp} is the reverse voltage the device has to withstand and K is a constant.

From (6.8) it is clear that series connection of $2N$ low voltage devices will result in lower conduction losses as compared to a single device of N-times higher voltage ratings. In reality, the comparison is more complex, since the optimum technology for the switching devices depends on the required voltage blocking capabilities. At 36 V level, as in the case of the building block of the cascaded converter proposed here, MOSFETs are the correct choice; however, an hypothetic 2-level inverter driving the same motor load would have a DC-link voltage higher than 300 V, making IGBT the preferred device, as shown in Table 6-2.
Fig. 6.5 shows a comparison between losses in the proposed cascaded converter and in a standard 2-level inverter of equivalent ratings; the losses are analytically calculated at rated inverter output voltage, varying the power absorbed by the load.

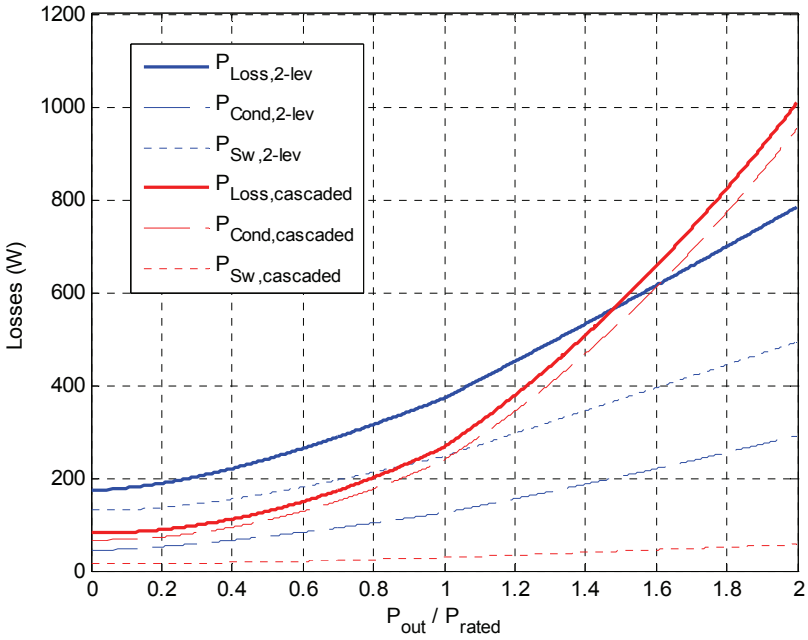


Fig. 6.5 – Comparison of losses in the switching devices of the proposed cascaded multicell converter and of a standard 2-level, 3-phase inverter.

Losses in the IGBT inverter are calculated using the methods first presented in [100]; similar results can also be obtained using the loss calculator developed by the device manufacturer [101]. In the case study, switching frequency of the IGBT inverter is fixed to 12 kHz.
Conduction losses in the MOSFET-based cascaded inverter are assumed to be purely resistive, since the anti-parallel diodes (see Fig. 6.2) will only conduct current for a very short period of time (the dead time of the block being operated in PWM mode):

$$P_{cond,MOSFET} = R_{DS} \cdot I_D^2 \tag{6.9}$$

In evaluating (6.9), R_{DS} should be the resistance of the device at the target junction temperature, here assumed to be $100°C$; I_D is the *rms* value of the load current.
For simplicity, PWM switching frequency of the cascaded inverter is also fixed to 12 kHz. This will actually give a much better voltage waveform than the 2-level inverter. However, since only one out of N blocks is operated in PWM mode in each switching period, the equivalent switching frequency will be N times lower. This, added to the fact

that MOSFET devices exhibit in general much better switching characteristics than IGBT, due to the unipolar nature of the current inside the semiconductor, explains why switching losses are so small in the case of cascaded inverter.
From Fig. 6.5 it results that the IGBT inverter has lower losses when operated at peak power, but the cascaded inverter is more efficient all the way from no load up to about 1.5 times the rated power. Since a typical driving cycle (see chapter 2) will imply operation below this breakeven point for most of the time, it is reasonable to conclude that the cascaded inverter has potential for better efficiency, overall.
Moreover, since losses in the cascaded inverter are dominated by conduction losses, it is possible in principle to modify the design process for the switching devices, yielding a MOSFET with lower conduction losses at the expense of higher switching losses; in this particular application, this would result in an overall reduction of losses, making the proposed architecture even more favourable.
Electromagnetic emissions from the converter are mainly due to the steep current slopes resulting from PWM. There are at least two reasons why the cascaded multilevel topology described so far is expected to be superior in terms of EMI when compared to standard 2-level hard-switched topologies. First of all, due to the multilevel structure, voltage steps due to the switching devices are reduced in height to the individual DC link voltage. Secondly, and perhaps even more important, since the switching losses of the converter are shown to be very low, it is possible to slow down the commutation of each MOSFET, reducing the current slope and therefore EMI considerably; the resulting increase in switching losses due to the slower commutation will not affect the efficiency in any significant way.
Slowing down the switching speed of MOSFETs from their rated capabilities will also have another very favourable consequence: reduction of the over-voltage peak across the switch at each commutation. This allows for the use of lower voltage devices, like the one mentioned in Table 6-2, having 55 V reverse blocking capabilities when the DC link voltage can be as high as 42 V. Such a small voltage margin would hardly be feasible otherwise, even if the breakdown capabilities of modern MOSFETs are exploited. As already mentioned, the use of devices with lower blocking voltage will reduce the conduction (dominating) losses.

6.5.3 System Layout and Control Structure

As suggested by Fig. 6.1, from the system integrator point of view the system is made up of identical modules (the Building Blocks), embedding DC source, H-Bridge, configuration relays and digital control logic. The two output terminals are connected to form the desired topology (could be single leg, 3-phase wye, 3-phase delta, n-phase, etc.). Extra connections are needed for the battery charger and to achieve redundancy as described in section 6.4. However, if the building block is properly engineered, the connection can be considerably simplified, as suggested in Fig. 6.6. Moreover, each converter leg of a Wye topology can be in physically different locations on board of the vehicle, and the interconnection between them is limited to one power line. In addition, each leg has to be connected to one motor phase, to the charger and to the master controller.
In order to simplify cabling and to increase reliability, the communication within the system is purely serial.

Such a decentralized converter needs a dedicated control structure. In this work, a standard motor controller operates as master and calculates the voltage needed at the load terminals. A second control module, also logically located at master level, will then figure out a proper way to synthesize the required voltage, with the additional control target of keeping the SOC of all blocks properly balanced. In principle, there will be one of those modules for each phase leg (Fig. 6.1). The building blocks are slave modules; they communicate to the master their voltage availability and their current SOC, and receive in turn the switching command.

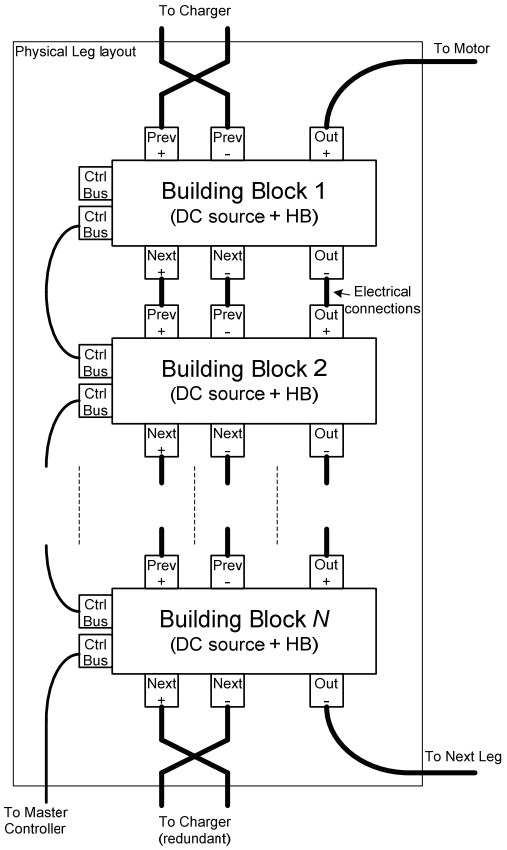


Fig. 6.6 – Leg physical layout and suggested cabling

6.6 Serial Communication Protocol for Distributed Operation

The serial communication in the system of Fig. 6.1, Fig. 6.2 and Fig. 6.6 must serve the following purposes:

- Allow for proper voltage synthesis at the load terminals by synchronization of the individual switching of each H-bridge;
- Ensure communication of the slaves' state to the master for proper system configuration at start-up and following faults.

Moreover, if the overall system must tolerate any single fault in any of its components, the communication system itself must:

- Continue to operate properly in case of any single fault on any of the building blocks;
- Continue to operate if there is a single fault on the communication bus itself.

The latter requirement dictates the presence of hardware redundancy for the communication bus, such as for example replicated channels with redundant bus guardian on each module (block) [102]. Analysis of all possible communication failure modes and the associated handling for fault containment is well beyond the scope of the thesis. A good introduction can be found in [103]; more detailed implementations of fail safe and redundant communication systems applied to automotive already exist, the most promising being TTP/C [104] and FlexRay [105].
Either of those protocols could be well suited for the implementation of the synchronized PWM required by the cascaded H-bridge architecture. However, the general purpose protocols have much functionality that is not required in this simple case; a simple custom time-triggered protocol is therefore developed to meet the specific requirements of the multi-phase, multi-cell converter described do far.
Time-triggered protocols are those in which the communication activity is driven by the progress of time. By contrast, in event-triggered protocols (like the famous CAN), communication is driven by the occurrence of events. The former class is more suitable for systems with high degree of dependability [106]. In particular, protocols based on TDMA (Time Division Multiple Access), provide deterministic access timing to the bus, considerably simplifying the implementation of the multicell PWM and, at the same time, detection of defective modules.
In the architecture of Fig. 6.1 there are logically three kinds of nodes on the communication bus:

- The motor controller (one node);
- Phase leg priority and voltage generation modules (n-nodes, with n being the number of phases in the topology);
- Standard building blocks (n by N modules)

The physical arrangement is not univocal, since more logical functions could be performed by a single physical node. For simplicity, the star configuration in Fig. 6.7 is assumed, where there is only one master node, responsible for the motor control algorithm as well as for the phase priority and PWM generation of all phases, from which n independent bus lines originate to form a star.

In order to achieve the highest degree of reliability, distributed systems should not rely on any particular element to be the master. This is for the obvious reason that the lost of the unique master prevents the system from continuing its operation. However, in the architecture of Fig. 6.7, it is implicitly assumed that the signal electronics constituting the master module is much more reliable than the battery packs and the power electronics with associated gate drivers in the converter building blocks.
The communication protocol has been developed with the aim of being as efficient as possible during the normal operation of the converter, where all the N modules of each phase leg are cooperating to the output voltage generation process. To begin with, the bus cycle is logically synchronized to a virtual PWM triangular carrier used for the generation of the switching patterns of each H-bridge. The situation is depicted in Fig. 6.8.

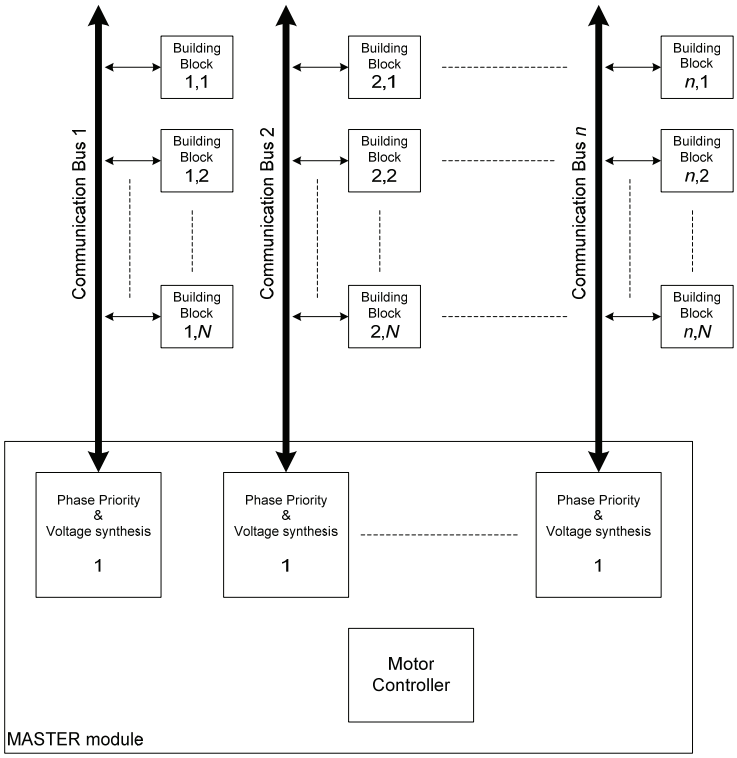


Fig. 6.7 – Topology of the communication system; *n* independent buses with one concentrated master.

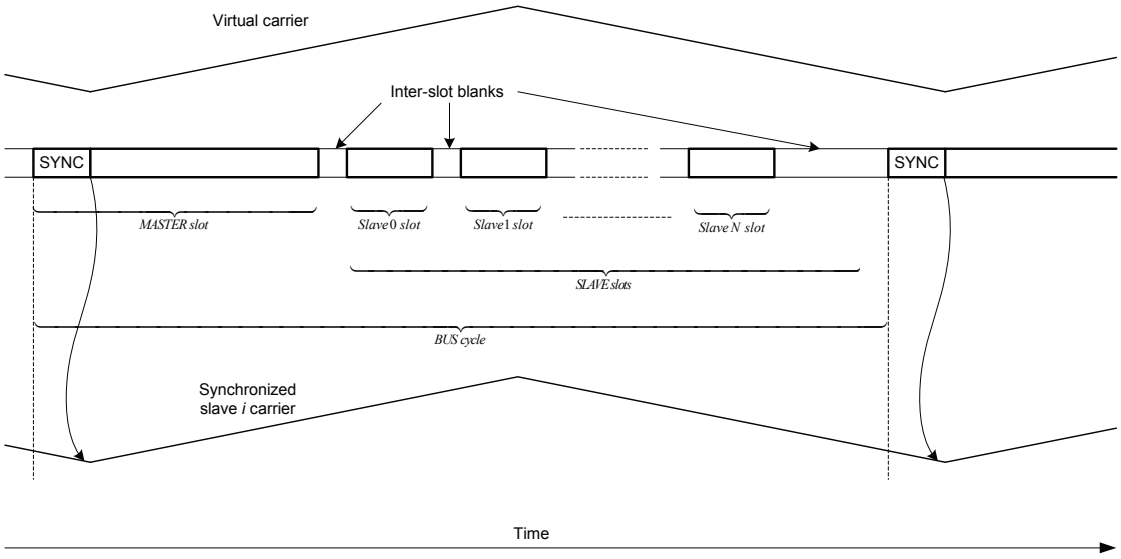


Fig. 6.8 – Bus cycle and its synchronization to the virtual PWM carrier

In practice, the master broadcasts a synchronization message (SYNCH) at the beginning of each virtual carrier cycle; all slaves receive the SYNCH and synchronize their local triangular carrier to this event. This mechanism is used to make sure that a global concept of time exists in the whole network. Accuracy of the synchronization method is determined by the maximum propagation time of the signals over the physical bus line

(from master to the furthest slave) and by the relative drift of the local clock generators on board of each module during the time period between successive synchronizations.
The SYNCH message is the beginning of the bus cycle, and there must be a SYNCH message from the master for each carrier period. Such a message is very simple, consisting of a single byte with fixed value (the SYNCH).
The first fraction of the bus cycle is allocated to the master that sends the SYNCH message followed by other service messages; during normal converter operation, the master will send the command for voltage generation to all the slaves in the chain during this phase of the bus cycle, as described later.
The second part of the bus cycle is allocated to the slaves. Each slave has its own slot, where he can transmit up to 5 bytes, normally containing information about local state and measurements.
The distributed system in Fig. 6.7 has different operating phases:

1. Wake-up, Self-Test and Synchronization (WSS);
2. Configuration of cascaded converter (CFG);
3. Operation (OP)

At power-on, or following a global reset, each module (master and slaves) initializes itself to the WSS state. In this state, the master only sends SYNCH signals over the bus at regular intervals, and waits for replies from the slaves. Each slave executes its self-test and starts sending the result to the master, using its statically allocated slot in the bus cycle.
After some time, the master will have information about all the active slaves (building blocks) and will start configuring the network. In particular, the output of the faulty blocks will be bypassed, and all the healthy DC sources will be connected to a healthy H-bridge.
Once the cascaded converter is configured, the master tells the active slaves to go into the OP state, and normal operation begins.
The message sent over the communication bus during CFG will not be described in detail, since not all the functionalities have actually been implemented, due to limitation in time and resources.
On the other hand, the protocol allowing for converter operation has been fully developed and implemented, and is therefore described in the following.

6.6.1 Communication protocol during converter operating phase

During normal converter operation, the master sends the PWM generation message to all slaves in a phase chain. Assuming that a phase leg can contain up to twelve building blocks, the format of the 6-bytes long PWM message is given in Fig. 6.9.

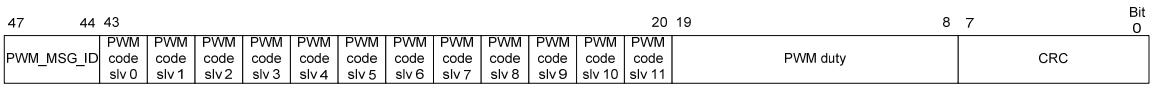


Fig. 6.9 – PWM message from master to slaves

The first nibble $[b_{47},\ldots,b_{44}]$ is a fixed code (the message ID), indicating the meaning of the message; All slaves will read this code and understand that a PWM message is coming. The following part of the message is a sequence of twelve two-bit codes (one

for each slave in the chain, according to their logical address), whose meaning is given in Table 6-3.

Table 6-3 – Codes for output voltage generation of each slave

0 0	The block should output zero voltage
0 1	The block should output maximum positive voltage
1 0	The block should output maximum negative voltage
1 1	The block should be operated in PWM

Notice that in order to minimize commutations and improve the voltage waveforms, for every switching period there will be only one block operated in PWM mode, and therefore only one out of the sixteen bit-fields can contain the code [1 1].
Then it follows the 12-bit PWM_DUTY field $[b_{19},\ldots,b_8]$, specifying the duty cycle of the only H-bridge in the chain that has to operate in PWM mode over the next switching period; that represents the 12-bit binary coding of a number between -1 and +1.
The last byte is a CRC (Cyclic Redundancy Check) that is used by the slaves to verify the integrity of the received message.
The implicit limit of this implementation is that there can be no more than twelve slaves connected to the phase chain; in terms of the converter architecture, that means $N \leq 12$.
Only one message from the master is sufficient to convey the information for the synthesis of the converter output voltage to all building blocks; in order to increase the likelihood of correct reception by all the slaves, the same message can be broadcasted by the master more than once, according to the time availability within the master slot (see Fig. 6.8). Only one correct reception by each slave will be sufficient for proper voltage synthesis.
Once the *i*-th slave (the slave with logical address *i*, with *i* being a number between 0 and 11) has received the master message in Fig. 6.9 and has verified its integrity through CRC, it determines the state of the switches of its H-bridge by decoding the bits $[b_{43-2i}, b_{43-2i-1}]$ and, if necessary, the duty cycle.
Every slave then acknowledges the correct reception of the master message by filling its dedicated slot in the second part of the bus cycle.
Each slave message is made up of 5 bytes, whose meaning during normal converter operation is shown in Fig. 6.10.

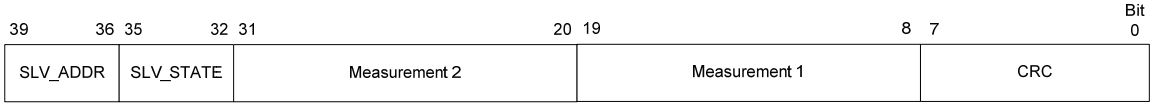


Fig. 6.10 – Message from slave to master

The first four bits $[b_{39},\ldots,b_{36}]$ are the logical address of the sending slave; that information is somehow redundant, since the slot occupied by the message is already an indication of who the sending slave is. It can be used by the master for further consistency check, to make sure that none of the slaves has lost synchronism.
The bits $[b_{35},\ldots,b_{32}]$ contains information about the state of the sending slave; one of the bits inform the master about the correct reception of the last PWM message, while another tells the master if any abnormal condition is present that prevents the slave from

participating to output voltage synthesis. Details about the remaining state bits are omitted here, for brevity.
There are then two 12-bit long fields, $[b_{31},\ldots,b_{20}]$ and $[b_{19},\ldots,b_{8}]$, containing the measurements of two slave-local quantities, namely the available DC voltage and the SOC of the source. The master will use those values to determine the priorities for voltage generation in the next bus cycle.
Finally, there is a CRC field, $[b_{7},\ldots,b_{0}]$, used by the master to check data consistency.
In a normal bus cycle, when no errors occur, the master sends the SYNCH message followed by the PWM message (possibly repeated); all the slaves correctly receive those messages and reply accordingly, signalling back to the master that everything is fine. However, during a bus cycle, any of the following may occur:

- One or more slaves fail to receive the SYNCH and/or PWM message (either because the message is corrupted or a slave has lost synchronism;
- The master does not receive acknowledgment of correct reception by one or more slaves.

Those errors may be either permanent or temporary. It is therefore desirable to try to ride-through the error, interrupting the operation only when the error persists. To that purpose, both master and slaves have some simple, built-in error handling strategies:

- In each reply, the slave communicates to the master whether it has received correctly SYNCH and PWM messages. If not, it just keeps on operating as usual, utilizing the most recent PWM command it has correctly received; It is up to the master to decide when the number of receiving errors require the generation of a global alarm, suspending operation.
- The master keeps on normal operation until the number of missing acknowledgments reaches a given threshold. Only at this point, a global alarm is generated.

Only the master can generate a global alarm. For safety reasons, such alarm is sent over the network on a dedicated, and possibly redundant, line (not the bus line). Following a global alarm, the system restarts from the WSS state and a new configuration is made possible (self-healing).

6.6.2 The physical layer of the bus and the practical implementation

The standard EIA-485 is used to implement the physical layer of the serial communication bus. The standard provides differential balanced signals over two wires (normally a twisted pair), resulting in excellent noise immunity for data communication up to 35 Mbit/s over relatively short distances (up to 10 m).
Asynchronous communication with start/stop bits is employed, avoiding the need for a dedicated clock line. Start and stop bit(s) are the only overhead to be added to the higher level messages described in the previous section.
As already mentioned, a dedicated alarm line is also provided. To increase noise immunity, also this line has been implemented with a differential pair.
The protocol described in the previous section has been completely implemented in software on a TMS320F2812 DSP. All slaves, as well as the master, are equipped with such a DSP/microcontroller. The F2812 has internal peripherals that can handle in hardware the asynchronous transmission with start/stop bits, with baudrate up to about

10 Mbit/s. At such a speed, a single bit is transmitted in 100 ns; taking into account also the overhead due to the start/stop bits of the asynchronous frame, the PWM message in Fig. 6.9 requires a minimum bus slot of 5.1 μs. Each slave slot has a minimum duration of 4.3 μs; since there are 12 slave slots, assuming single slot duration of 5 μs and a safety blanking time of 1 μs between two adjacent slots to allow for synchronization errors, the total time allocated to slaves in the bus cycle is 71.0 μs.
The switching frequency of the building block operated in PWM has been chosen as 10 kHz, resulting in a total bus cycle of 100 μs. Resulting allocation of the bus cycle is reported in Fig. 6.11, showing that there is enough time for repeated transmission of the PWM message from the master.

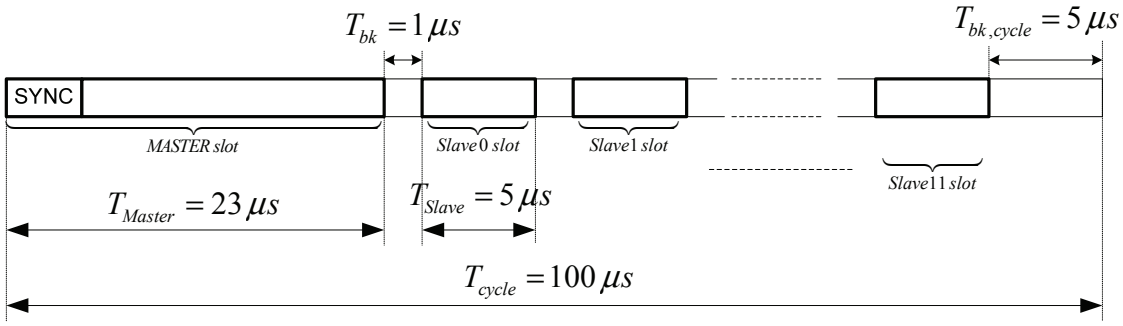


Fig. 6.11 – Allocation of the bus cycle in the actual implementation.

6.7 Experimental Setup and Results

In order to validate the proposed concepts, a fully operational prototype with a minimum number of modules has been built. The system, as shown in Fig. 6.12, consists of a single leg converter made of two identical building blocks. The local DC link of each building block is made up of a series connection of three standard 12 *V*, 10 *Ah* sealed lead acid batteries, resulting in 36 *V* rated voltage. Solid state devices used for the H-Bridges are the ones in Table 6-2. The converter is loaded by a separately excited DC motor, coupled to another controllable machine.
The control hardware features all the characteristics described in the previous sections and so does the time-triggered serial protocol, making expansion of the system by either adding more blocks in series or forming a Wye connection to achieve a three phase output rather straightforward.
The basic experiment of Fig. 6.13-a shows a constant current discharge of the 5 level system (*N*=2) with no charge balancing. Output voltage of the converter is fixed to 50.4 *V* (0.7 pu, having assumed the base voltage equal to the nominal voltage of the batteries), and the load is a DC motor, absorbing about 10 *A* throughout the experiment. Discharge is stopped as soon as the lowest battery voltage reaches 0.92 pu (about 33 *V*). End of discharge is easily noticed in the figure, since the terminal voltage of the batteries suddenly rises to the open-circuit value when the current drops to zero. Priorities in the modulation algorithm are fixed and block 1 has always higher priority than block 2. As expected, the battery pack connected to block 1 run out of energy faster than block 2, resulting in about 26 *min* of available operating time before the minimum allowed terminal voltage is reached.

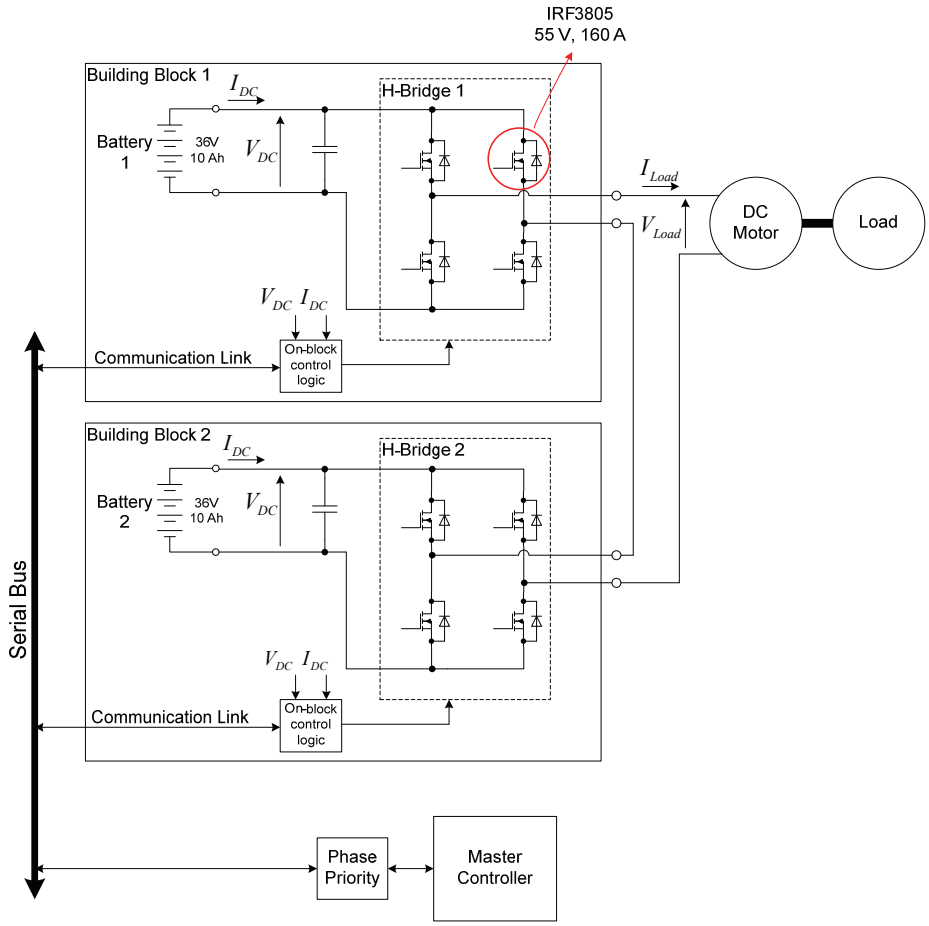


Fig. 6.12 – Simplified experimental setup with a single leg architecture, *N*=2.

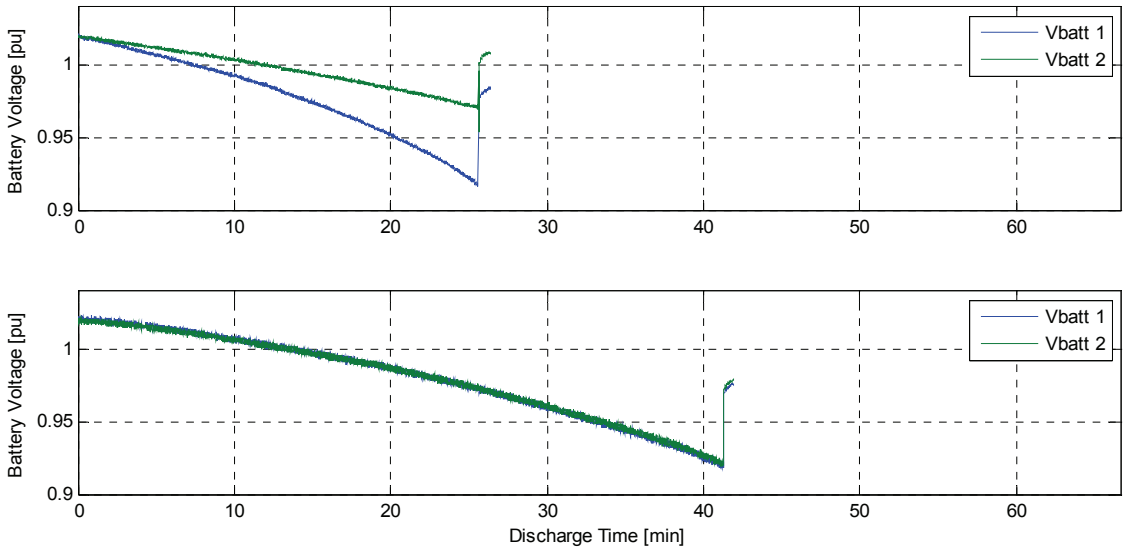


Fig. 6.13 – Experimental results of battery discharge at constant load voltage (0.7 pu) and constant load current (0.7 pu); From top to bottom:

(a) - With no control for energy sharing; block1 has always higher priority than block 2;

(b) - Energy sharing by dynamic assignment of priorities based on on-line monitoring of SOC;

In Fig. 6.13-b, all conditions above remain unchanged, but the proposed charge balancing algorithm is enabled and switching priorities between blocks are dynamically assigned by the master controller. It can be seen that both blocks discharge equally, resulting in optimal utilization of the energy, as witnessed by the extended operating time of about 41 *min*.
It should be noticed that during this experiment the SOC of each block is evaluated locally by the corresponding slave with a very simple algorithm, assuming the SOC to be a function of just the battery voltage and the current; an improved SOC estimation algorithm is desirable, and that can be implemented without affecting in any way the operation of the master controller responsible for global charge balancing, since it only receives information about SOC of each block, and need not to know how that number is evaluated.

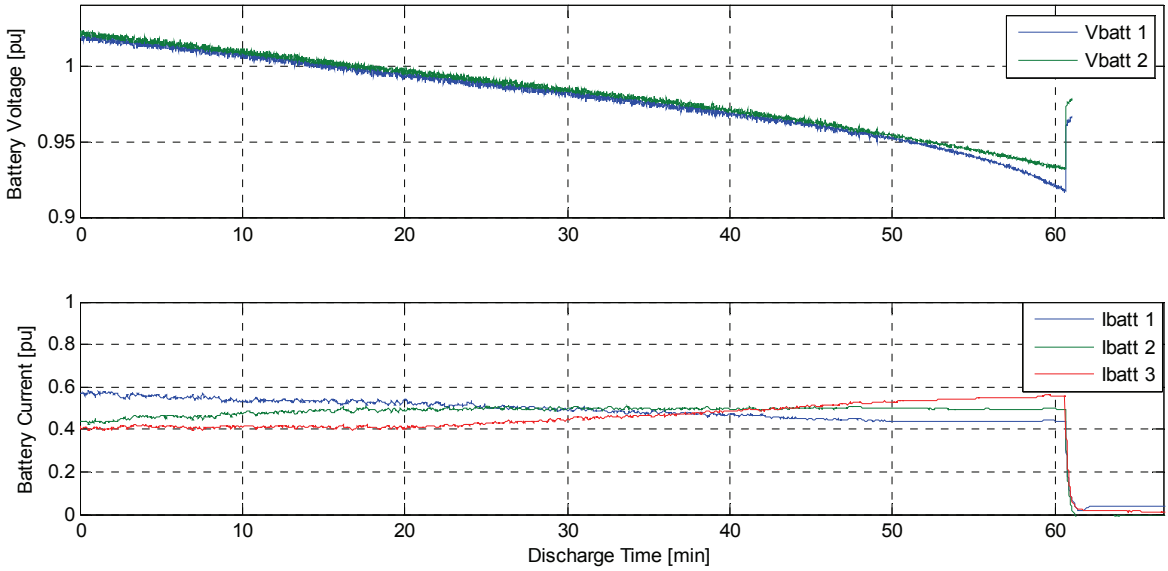


Fig. 6.14 – Experimental results of constant power discharge of a system composed by two H-Bridges and three battery packs, two of which are connected in parallel; From top to bottom:
Terminal voltage at the input of each H-Bridge;
Average current flowing from each battery pack (packs 2 and 3 are in parallel);

In the experiment of Fig. 6.14, one extra battery pack (36 *V*, 10 *Ah*) has been connected in parallel to block 2. This condition mimics the case of a system with *N*=3, with one of the three H-bridges being out of order and the corresponding battery pack connected instead to one of the healthy blocks in order to be able to use all the energy available in the system. Results confirm that the three packs discharge equally up to a point very close to the end of discharge. The resulting operating time is about 61 *min* that is about 1.5 times the operating time obtained in the experiment of Fig. 6.13-b, where the available energy was 33% smaller (2 battery modules, instead of 3). Non ideal balancing towards the end of the test is due to the poor evaluation of the SOC of each block, as pointed out earlier, and also to the poorly matched characteristics of the batteries in use. Fig. 6.14-b shows the average current flowing on each of the three battery packs during the test (1.0 pu is equal to 10 *A*, which is the 1C rating of the batteries in use). Ideally, they should be identical throughout the experiment. While the

difference between I_1 and the other currents is mostly due to poor SOC estimation, the difference between I_2 and I_3 is fully due to the different internal impedance of the two nominally identical battery packs. In fact, the terminals of the two packs are connected in parallel with no control whatsoever for current sharing. In particular, it may be noticed that the sharing algorithm is trying to assign lower priority to the most discharged block 1 towards the end of the experiment, but even so, the voltage across that block falls more quickly than the voltage across the block who is given higher priority (and who is asked for more current).
Even with all limitations and inaccuracies discussed above, operating range close to ideal has been achieved.

6.8 Concluding remarks

Cascaded multilevel topology is a promising alternative to be used as interface between the energy storage devices (batteries and/or SCs) and the electrical load on board of electric vehicles. Besides the advantages in terms of voltage quality, safety, EMI and, most likely, efficiency, the cascaded inverter has the unique feature of being inherently redundant, making it an ideal starting point to build highly dependable systems for applications with very strict requirements in terms of reliability.
Several aspects related to both operating principle and practical realization of a cascaded multilevel converter suitable for EVs have been analyzed, with special emphasis on self-healing and post-fault operation.
A working prototype with a reduced number of building blocks has been realized and tested. It is believed that the proposed topology, if equipped with a suitable control system designed for reliability and fault-tolerance, can be deployed in special applications when quality and safety concerns offset the increase of complexity that the multilevel, multicell topology brings with it.
The proposed topology appears to be particularly well fitted for modern Li-ion battery packs developed for automotive [107]. In fact, those packs are constituted by a large number of relatively independent modules (similar to the building blocks), each featuring a good deal of local intelligence for monitoring the state of health of the cells, and communicating with a higher level (pack level) logic. Such a hierarchic structure helps preventing local failures from propagating to the whole pack, and adapting that structure to the one proposed in this chapter, would only imply adding a simple H-bridge at the output terminals of each module.

7 CONCLUSION

7.1 Concluding remarks

The thesis has investigated power electronics-based solutions to control the power flow between the several elements of the electric drive train found on-board of electric vehicles.

A new topology has been proposed for a power buffer based on supercapacitors (SC). The system consists of two series-connected SC banks and a half-bridge controlling only the fraction of the power flow related to one of them.
It has been demonstrated that such a configuration allows for bidirectional power flow control by using semiconductor devices that are rated for as little as half the current of the devices that would be needed to build a conventional half-bridge interface. Moreover, the size and weight of the magnetic component needed for boosting and current filtering is considerably reduced.
After thorough theoretical investigation, the concept has been experimentally demonstrated by building a full-scale 30 *kW* prototype intended for use as power support for the traction battery on board of the Norwegian Th!nk City electric car.
Practical problems related to the implementation, like dynamic control of the voltage across the two SC banks and initial pre-charge, have been addressed and working solutions have been proposed and demonstrated.
It is pointed out that the use of the proposed topology is by no means limited to automotive applications. The concept is suitable for any kind of applications where the energy stored in supercapacitors has to be exchanged with a system having constant terminal voltage characteristics. Possible fields of application include (but are not limited to):

- Energy storage for distributed power systems, where small generators are interfaced to the grid by an intermediate DC-link;
- Power buffer for railway traction systems;
- Power buffer for fuel cell-based systems.

A distributed architecture has been devised for the traction inverter that is particularly suitable for use with modern, lithium-based, battery packs. In this proposal, the battery cells are organized in low voltage modules, and each module is equipped with an H-bridge, making it functionally equivalent to a controllable voltage source. The inverter is then built by connecting all the identical modules, giving rise to a distributed structure that can be engineered to have excellent fault-tolerance and that can be able to re-configure itself after failure of one or more of its elementary building blocks.
Simple prototypes of the elementary building block have been built, and the whole decentralized control structure has been implemented, demonstrating the feasibility of the concept.
The resulting system appears to have considerable complexity, since and the building blocks have to include local "intelligence", as well as power electronics components. However, last-generation lithium-ion battery modules are already equipped with complex cell-level monitoring systems, and the additional features needed for the implementation of the distributed inverter are not likely to increase complexity and cost significantly.
Though the application of the distributed inverter architecture seems unlikely for general purpose electric car, it may become an option in special fields where reliability and availability are primary concerns.

7.2 Prospects for future investigation

The SC-based power buffer has been tested as a stand-alone component. The next natural step should be its inclusion in an actual drive train.
Of particular interest is the deployment of a real traction battery, instead of the controlled DC-link used in the thesis.
Actual driving conditions should be investigated, and resulting data should be used for optimized thermal design of the proposed converter.
Besides road tests, a laboratory setup where characteristics of each component of the drive train, including the SC-based power buffer, can be analyzed in a strictly controlled manner, has been planned as shown in Fig. 7.1. At present, the system has been partially built; the traction battery is still unavailable and control of the two motors is under development.

The distributed inverter concept should be applied to an actual lithium-ion battery pack. Of particular interest is the effect that may have on the battery lifetime the possibility to control the individual energy flow from each low voltage block, and the ability to minimize the usage of blocks showing degrading performance.

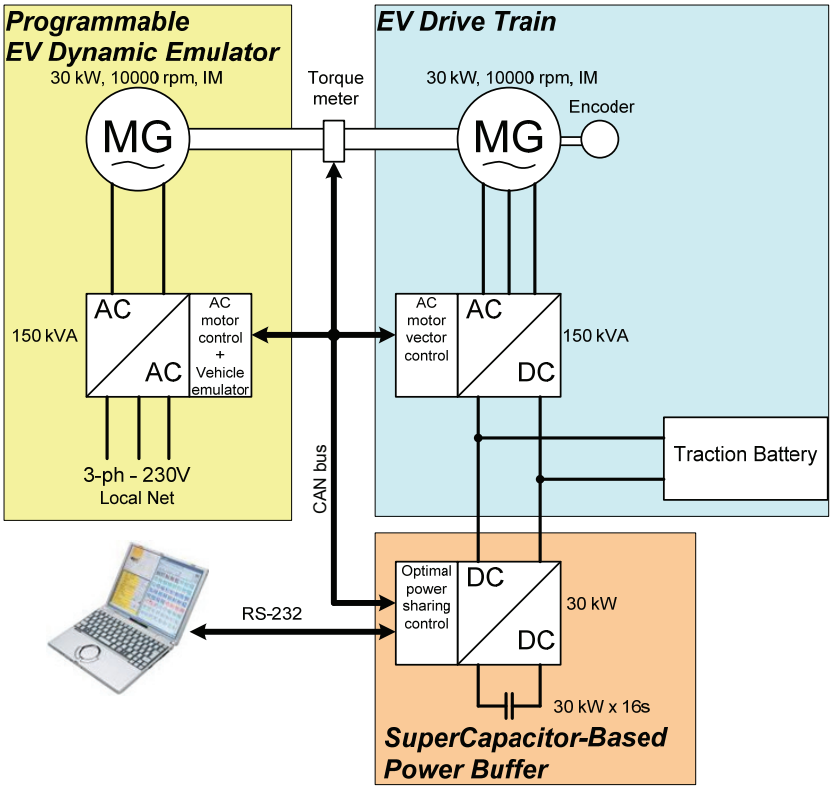


Fig. 7.1 – Setup for automated test of electric drive train components

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