

Gate controlling MPCs as Part of a cascaded MPC Structure, used for harmonic Mitigation in a Ship Power System

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Preface

This document is a Master thesis submitted to the Department of engineering cybernetics at the Norwegian University of Science and Technology (NTNU). The work documented in this Thesis was carried out in the spring of 2018, from January to June. The assignment is defined by NTNU in collaboration with Ulstein Blue Ctrl AS. All work is carried out at NTNU, and its available facilities. The reader is assumed to have some understanding of ship power systems as well as Model Predictive Control (MPC) and harmonic mitigation. This work is conducted within a context defined by [6], which proposed an MPC-based approach for system-wide harmonic mitigation in a ship power system. The simulation model of a ship power system used in [6], inlcuding a model of an Active Power Filter (APF) designed for harmonic mitigation was available at a starting point of this work. This simulation model was implemented in Matlab and Simulink version 2017b. The model included an MPC used for system-wide harmonic mitigation, implemented in C++ and ACADO and a hysteresis controller to control the APF currents. This work has focussed on the design and evaluation of MPC-based ontrol strategies for the APF in the system configuration from [6]. All investigated MPC strategies for control of the APF have been implemented as part of this thesis and have been simulated using computers provided NTNU and the Department of engineering cybernetics. The main MPC implementations have been developed in ACADO, although some FCS-MPC implementations were simulated using Yalmip. The simulations including the APF and ship power system have been conducted with Matlab 2017b and Simulink. Jon Are Suul has been consulted throughout the thesis, providing reference information on control of APFs and MPC-based control of power electronic converters. Espen Skjong from Ulstein has been consulted regarding MPC implementation, and suggested the use of ACADO for the work in this thesis

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- Jon-Are Suul: For coordinating the process. Maintaining contact with Espen, and supplying the problem description. Aiding with details on problem formulation and supplying relevant background material. As well as helping with the cascaded MPC implementation.
- Espen Skjong: For supplying the simulation model, and post processing scripts. Scripts used to generate harmonic spectra and measure THD.

Executive Summary

English

This thesis studies the effect of controlling gate switches in an APF using FCS-MPC. This gave a cascaded MPC structure. Where internal states and a calculated reference from the first MPC is used by a second MPC. The second MPC was designed to track the reference. An FCS-MPC with continuous variables was designed and compared to existing benchmark implementations. Including an ILS-FCS-MPC, an ICS-MPC and a hysteresis controller.

The CCV-FCS-MPC was implemented in ACADO. It was based an existing ILS-FCS-MPC. Using an existing model formulation. The cost function was tuned based on theory on Sequantial Quadratic Programmin (SQP). Using a trial and error method to arrive at the final cost function expression. All gate controlling implementations were then verified in a simplified version of the ship power system. Then implemented in the Cascaded MPC structure with the existing harmonic mitigating MPC.

First reference tracking performance and power loss was measured. Results show that an CCV-FCS-MPC with a tuned cost function outperforms hysteresis controllers, ICS-MPC with PWM and an existing ILS-FCS-MPC. With a reduction in SSE of at least 50% compared to any other implementation, while also reducing power loss.

Results show that THD in a ship power system is reduced for all MPC implementations, compared to a hysteresis controller. Both for an ICS-MPC, an ILS-FCS-MPC and a CCV-FCS-MPC. The CCV-FCS-MPC with a tuned cost function outperforms all other tested implementations. It reduces generator current THD by over 20% compared to any other implementation. While also reducing power loss and maintaining bus voltage THD. Compared to the hysteresis controller.

Norsk

Denne oppgaven studerer effekten av å kontrollere DC til AC bryterstruktur for kraftelektronikk, ved hjelp av Model Prediktiv Kontroll (MPK). Referansen var gitt av en MPK med minimering av harmoniske komponenter som objectiv. Dette ga en kaskadestruktur med to MPK'er. Interne tilstander og en beregnet referanse fra den første MPK'en ble brukt av den andre. Den andre MPK'en var designet for å følge referansen. En Finitt Kontroll Set Model Prediktiv Kontroller (FKS-MPK) med kontinuerlige kontrollvariabler ble designet og sammenlignet med eksisterende løsninger. Disse innebefattet en FKS-MPK med diskrete kontrollvariable, en Infinitt

Kontroll Set MPK (IKS-MPK) og en hysteresekontroller.

FKS-MPK'en med kontinuerlige kontroll variable ble implementert i ACADO. Den var basert på modellformularingen en eksisterende FKS-MPK med diskrete kontrollvariabler. Kostnadsfunksjonen ble bestemt på bakgrunn av teori om Sekvensiell Kvadratisk Programming (SKP). Ved prøving og feiling ble det endelige kostnadsfunksjonsuttrykket bestemt. Alle MPK implementasjoner ble deretter verifisert i en forenklet versjon av kraftelektronikksystemet. Før de ble implementert i kaskadestrukturen med den eksisterende MPK'en.

Resultatene viste at (FKS-MPK) med kontinuerlige variabler hadde best ytelse. Både med tanke på referansefølging og effekttap. Den ga en reduksjon i kvadratisk avvik på minst 50% sammenlignet med andre implementasjoner, samtidig som effekttapet ble redusert.

Resultatene viser at THD i et skipssystem er redusert for alle MPK-implementasjoner, sammenlignet med en hysterese-kontroller. Både for IKS-MPK'en og for FKS-MPK med både diskrete og kontinuerlige kontrollvariabler. FKS-MPK med kontinuerlige kontrollvariabler ga bedre resultater enn alle andre testede implementtasjoner. THD på generatorstrømmer ble redusert med over 20 % sammenlignet med alle andre implementasjoner. I tillegg ble effekttap THD på busspenninger redusert.

Contents

	Pref	àce	i					
	Ack	nowledgment	ii					
	Exe	cutive Summary	iii					
1	Intr	ntroduction						
	1.1	Background	3					
	1.2	Objectives	5					
	1.3	Approach	5					
	1.4	Contributions	6					
	1.5	Limitations	6					
	1.6	Outline	6					
2	Theory							
	2.1	Model Predictive Control (MPC)	9					
		2.1.1 Problem formulation	9					
		2.1.2 Principle of Sequential quadratic programming	12					
	2.2	MPC for gate control in power electronics	13					
	2.3	Finite Control Set Model Predictive Control	13					
	2.4	Integer Least square formulation of FCS-MPC	14					
		2.4.1 Problem formulation	14					
	2.5	FCS-MPC without binary variables	19					
	2.6	Estimating losses in a power converter	20					
		2.6.1 Switching losses	20					
		2.6.2 Total harmonic distortion	21					
	2.7	Clark Transformation	21					
	2.8	PWM for controlling gate switches	22					
	2.9	LCL oscillations	23					
	2.10	MPC for harmonic mitigation in a ship power system	23					
		2.10.1 Model of the ship power system	24					

		2.10.2	2 MPC implementation	25
3	Imp	olemen	itation of gate controllers	29
	3.1	Testin	ng gate controlling MPCs outside the cascaded structure	29
		3.1.1	Single MPC iteration	30
		3.1.2	Multiple FCS-MPC iterations in Test Circuit	31
	3.2	Imple	ementation basis for all gate controlling MPCs	32
		3.2.1	Model inspiration	32
		3.2.2	reference frame for control	32
		3.2.3	Verification in test circuit	33
	3.3	FCS-N	MPC using yalmip	33
		3.3.1	Reformulating binary control variables	33
	3.4	Conti	nuous Control Variable FCS-MPC using Acado	34
		3.4.1	Model formulation and setup	34
		3.4.2	Initial cost function	35
		3.4.3	Cost function tuning, optimizing binary control and reference tracking	36
		3.4.4	Continuous control variables to binary	42
		3.4.5	Finding optimal <i>q</i> _{discrete} values	42
	3.5	ICS-N	1 PC	42
		3.5.1	MPC formulation	42
		3.5.2	cost function	43
		3.5.3	PWM	43
	3.6	Casca	ded MPC implementation	44
		3.6.1	Control structure	44
		3.6.2	Injecting estimated bus voltage	46
		3.6.3	Ship power model	46
		3.6.4	Base harmonics compensation	46
	3.7	Test o	f complete setup	46
		3.7.1	Performance measurement	47
		3.7.2	Test cases	48
4	Res	ults		51
	4.1	Perfo	rmance of the gate controlling implementations	52
		4.1.1	Graphical presentation of current tracking capability	52
		4.1.2	SSE for all implementations	53
		4.1.3	Current tracking of CCV-FCS-MPC versus hysteresis controller	55
		4.1.4	Current tracking of CCV-FCS-MPC versus ICS-MPC	56
		4.1.5	Current tracking of CCV-FCS-MPC versus ILS-FCS-MPC	56
1	4.1	Perfor 4.1.1 4.1.2 4.1.3 4.1.4 4.1.5	rmance of the gate controlling implementationsGraphical presentation of current tracking capabilitySSE for all implementationsCurrent tracking of CCV-FCS-MPC versus hysteresis controllerCurrent tracking of CCV-FCS-MPC versus ICS-MPCCurrent tracking of CCV-FCS-MPC versus ILS-FCS-MPC	52 52 53 53 54 50 50

Bibliography 70					
A	Acro	onyms		69	
	6.2	Recor	mmendations for Further Work	68	
	6.1	Sumn	nary and Conclusions	67	
6	Con	clusio	ns	67	
		5.3.3	CCV-FCS-MPC versus ISL-FCS-MPC	66	
		5.3.2	CCV-FCS-MPC versus ICS-MPC	65	
		5.3.1	CCV-FCS-MPC versus Hysteresis controller	65	
	5.3	All pe	rformances relative to toggles	64	
		5.2.3	THD versus other MPC controllers	64	
		5.2.2	THD versus hysteresis controller	64	
		5.2.1	THD in all cases	63	
	5.2	Perfo	rmance of the CCV-FCS-MPC in cascaded MPC structures	63	
		5.1.5	Current tracking versus ILS-FCS-MPC	63	
		5.1.4	Current tracking versus ICS-MPC	62	
		5.1.3	Current tracking versus hysteresis controller	62	
		5.1.2	Number of toggles in all cases	62	
		5.1.1	current tracking capability in all cases	61	
	5.1	Perfo	rmance of the CCV-FCS-MPC	61	
5	Dise	cussio	n	61	
		4.2.4	Microgrid THD values of CCV-FCS-MPC versus ILS-FCS-MPC	60	
		4.2.3	Microgrid THD values of CCV-FCS-MPC versus ICS-MPC	59	
		4.2.2	Microgrid THD values of CCV-FCS-MPC versus hysteresis controller	59	
		4.2.1	Microgrid THD values for all test cases	58	
	4.2	Perfo	rmance in a cascaded MPC structure	58	
		4.1.9	Number of toggles of CCV-FCS-MPC compared to ILS-FCS-MPC	58	
		4.1.8	Number of toggles of CCV-FCS-MPC compared to ICS-MPC	57	
		4.1.7	Number of toggles of CCV-FCS-MPC compared to hysteresis controller	57	
		4.1.6	Number of toggles for all implementations	56	

CONTENTS

Chapter 1

Introduction

The start of this masters thesis is an introduction to the problem. Why it is interesting, what objectives are defined. In addition a short summary of how the thesis is structured.

1.1 Background

A common ship power system concists of a diesel generetor, and an electric motor. This setup means electrical energy has to be transferred efficiently. Harmonics in the electrical grid contribute to power loss. This in turn increases fuel use and costs. Harmonic mitigation in such a micro-grid is therefore important. Prior to this thesis, an Active Power Filter (APF) for harmonic mitigation has been implemented in such i grid. The APF uses Model Predictive Control (MPC) to generate a filter current reference. Then gate switches, controlled by a hysteresis controller, to create AC-current. This thesis investigates the effect of adding different MPC implementations to this configuration. To tracking a current reference by controlling gate switches.

A second MPC will result in a cascaded MPC structure. The first will generate a continuous current reference. The second will track the reference using gate switches. Such an implementation has little documented performance. Results could therefore have significant impact in increasing efficiency in ship power systems.

Problem Formulation

Two sub-problems were defined in this thesis. The first was to design an different MPCs for controlling gate switches. Tracking the current reference as good as possible. The second objective was to document the behaviour as good as possible. In order to establish what MPC implementation performed best in the cascaded structure.

Related work

A system model is essential when using MPC and when studying harmonic influences. Such a model is defined in detail in [6]. In addition to containg the harmonic mitigation MPC, and a bechmark Hysteresis gate switch controller. The harmonic mitigating MPC formed the first part of the cascaded MPC structure. The work in this thesis was done based on the model and AFE implementation in [6]. Work could then be based on the original MATLAB and Simulink code. The AFE is implemented by a DC voltage source connected to a three phase system via gate switches. The output of the gate switches is connected to an LCL circuit, which in turn is connected to one of the voltage buses in the ship power system.

An FCS-MPC for controlling gate switches is implemented in [1]. Using the same gate switch, LCL and power source structure as in [6]. Here the optimization problem is reformulated into an Integer Least Square (ILS) Problem. In this paper the ILS problem is solved using sphere decoding. An algorithm used for solving Integer least square problems. In [3], an FCS-MPC problem is reformulated to contain continuous control variables. This paper investigates optimal cruise control for electrical vehicles. Optimizing electric power usage with respect to pedal travel. The binary control variable was a braking force either being zero, or a constant value. This was modelled as a continuous variable. Then a cost function term was added penalizing any other values than the binary. This work formed a basis for one of the MPC implementations in this thesis.

The remaining literature was used for minor work. The book [12] presents theory on Sequantial Quadratic Programming (SQP). SQP formed the basis for one simulation software that was used. Information on SQP was then used to tune one of the algorithms. Additional literature was used for smaller parts in this thesis.

What Remains to be Done?

All the MPC that were used for the second part of the cascaded MPC had to be implemented. This also meant the original MPC had to be altered, in order to make the cascaded MPC function. No alterations were made to the functionality, only the structure of the output was changed.

1.2 Objectives

The main objectives of this thesis are to

- 1. Design a cascaded MPC structure for harmonic mitigation in a ship power system.
- 2. Implement different MPCs that are capable of controlling gate switches connected to three phases.
- 3. Quantify how well the different MPCs perform relative to other existing gate controller implementations.

1.3 Approach

Three different MPCs were implemented. The first was a Continuous Control Variable Finite Control Set MPC (CCV-FCS-MPC). It was implemented in Toolkit for Automatic Control and Dynamic Optimization (ACADO). First a C++ file was written. This was then exported to a Matlab Executable (MEX) file and simulated. The ACADO implementation was based on the model formulation and initial cost function setup in [1]. The cost function of the CCV-FCS-MPC was optimized by trial and error. Based on the theory of SQP from [12]. The CCV-FCS-MPC was designed on its own before integrating it into a cascaded MPC structure. The cost function term from [3] was considered optimal when all control variables fell within 10% of one of the binary variables.

When the CCV-FCS-MPC was completed, it was implemented in Simulink via a Matlab Function block. This was then integrated in the existing APF and ship power system structure from [6]. The continuous control variables were rounded to the nearest binary value, then sent to the gate switches. Performance was optimized by varying control horizon and sampling time, and other internal control variables. In total 8 test cases were studied in order to find an optimal configuration.

The next two MPC implementations was an Infinite Control Set MPC (ICS-MPC) and the FCS-MPC from [1]. The ICS-MPC was implemented using ACADO, a MEX file and a Matlab Function block. This generated a continuous voltage reference, and PWM was used to generate the gate switching signals. The FCS-MPC was implemented in YALMIP, and integrated in Simulink using an Interpreted Matlab Function.

Performance of all the implementations, including the existing hysteresis controller, was quantified. Total Harmonic Distortion, Sum of Squares Error (SSE) and the number of toggles done by the gate switches was measured.

1.4 Contributions

This thesis contain two main contributions. The first is the design of the CCV-FCS-MPC. Which is a new way of implementing an FCS-MPC for controlling gate switches in power electronics. It is an implementation that could be used for any control problem involving gate switches. The second contribution is the cascaded MPC structure used in harmonic mitigation.

1.5 Limitations

Computer simulations are only an approximation of reality, and results will always differ from real world experiments. Another limiting factor is the number of test cases. Due to long simulation times, few test cases were studied. With a larger number of test cases, performance would have been better documented.

1.6 Outline

The outline of this thesis is presented below. With relevant comments on what is contained in each section.

- Preface: A description of where this work was conducted, and what resources were available.
- Acknowledgments: Gratitude to people supporting this work.
- Summary: A short presentation of what is done for this thesis, and why. Both in Norwegian and English.
- Section 1. Introduction: Presentation of the problem defined as objectives, related work and limitations.
- Section 2. Theory: Presenting relevant background information for this thesis. Regarding MPC control theory, FCS-MPC implementations, ship power systems and other minor relevant subjects.
- Section 3. Methodology: Presentation on how the CCV-FCS-MPC was designed, implemented and optimized. How benchmark implementations were made. Then how all implementations were tested and quantified.

1.6. OUTLINE

- Section 4. Results: Simulation results from the 8 test cases of the CCV-FCS-MPC, including benchmark results. This included plots of current tracking capability, bar graphs of THD, SSE and toggles, and tables of CCV-FCS-MPC performance relative to benchmark.
- Section 5. Discussion:
- Section 6. Conclusion and Further Work:
- Bibliography

Chapter 2

Theory

This chapter presents relevant theory on MPC, MPC used on gate controllers and FCS-MPC and how to use FCS-MPC without binary variables. In addition some relevant concepts in power electrics are presented. These include Total Harmonic Distortion (THD), Clark Transformation and Pulse Width Modulation(PWM). The last section presents the harmonic mitigating MPC and the model of the ship power system.

2.1 Model Predictive Control (MPC)

This section will give a brief presentation on how MPC problems are formulated. This involves going from an optimisation problem, through a state space model to formulate MPCs. The solution method SQP is also presented.

2.1.1 Problem formulation

At the core of any Model predictive control problem an optimization problem. The basic idea with this is to find either the maximum or minimum of an expression. This expression can be both linear and nonlinear, and involve multiple factors. When solving such problems with a computer certain algorithm have to be formulated. It is then beneficial to formulate optimization problems on a standard form.

Optimization problems

Optimization problems can, in it's simplest form be expressed as equation 2.1.

$$\min_{\mathbf{z}} \quad f_{opt}(\mathbf{z}) \tag{2.1}$$

Here f_{opt} is called the objective function. While z is a vector of variables referred to as control variables [12, p- 2]. To find a maximum, f_{opt} is multiplied by -1. This formulation is often insufficient. In most cases there are restrictions on the control variables. The control variables have to stay either on a certain path, or within an area. The formulation 2.1 then becomes 2.2.

$$\begin{array}{ll} \min_{z} & f_{opt}(z) \\ \text{subject to} & \\ c_{i}(z) = 0, \quad i \in \mathscr{E} \\ c_{i}(z) \geq 0, \quad i \in \mathscr{I} \end{array}$$
(2.2)

The set \mathscr{E} defines all equality constraints. Where some control variables are forced to stay on a certain path. The set \mathscr{I} defines the set of inequality constraints. They define areas the solution has to lie within. All $c_i(\mathbf{x})$ are scalar expressions with respect to the control variables in \mathbf{x} [12, p-2].

MPC formulation for a linear system

In Model Predictive Control the control variables are defined as control inputs to a system. Model predictive control involves calculating N sets of control variables forward in time. The variable N is known as the control horizon. Calculations are based on the predictive behaviour of the system derived from the model. In order to solve such a problem, it is advantageous to reformulate it to the form 2.2. Consider the linear discretized state space equation for a MIMO system from u to y.

$$\boldsymbol{x}_{k+1} = A\boldsymbol{x}_k + B\boldsymbol{u}_k \tag{2.3}$$

$$\boldsymbol{y}_k = C\boldsymbol{x}_k \tag{2.4}$$

Here T_s defines the step length, or sample time, of model prediction. An MPC problem with control horizon N = 1 is formulated as.

$$\min_{\boldsymbol{u}} \qquad f_{opt}(\boldsymbol{y}_{k+1}, \boldsymbol{x}_{k+1}, \boldsymbol{u}_k)$$

subject to
$$\boldsymbol{x}_{k+1} - A\boldsymbol{x}_k - B\boldsymbol{u}_k = 0$$

$$\boldsymbol{y}_{k+1} - C\boldsymbol{x}_{k+1} = 0$$
(2.5)

In this problem a cost function calculated from future predicted states and outputs is minimized with respect to the control variables u_k . In most cases there will also be inequality constraints. In most MPCs this is done over longer control horizons. States and outputs at any time within the control horizon can be expressed as.

$$x(k+m) = \mathbf{A}^{m} \mathbf{x}(k) + \sum_{l=0}^{m-1} \mathbf{A}^{m-1-l} \mathbf{B} u(k+l)$$
(2.6)

$$y(k+m) = CA^{m}x(k) + \sum_{l=0}^{m-1} CA^{m-1-l}Bu(k+l)$$
(2.7)

for
$$m = 0, ..., N - 1.$$
 (2.8)

The optimal control problem for any *N* can be formulated as.

$$\begin{array}{ll}
\min_{\boldsymbol{U}_{k}} & f_{opt}(\boldsymbol{Y}_{k}, \boldsymbol{X}_{k}, \boldsymbol{U}_{k}) \\
& \text{subject to} \\
& \boldsymbol{x}_{k+1} - A\boldsymbol{x}_{k} - B\boldsymbol{u}_{k} = 0 \\
& \boldsymbol{y}_{k+1} - C\boldsymbol{x}_{k+1} = 0 \\
& \boldsymbol{x}_{k+2} - A^{2}\boldsymbol{x}_{k} - AB\boldsymbol{u}_{k} = 0 \\
& \boldsymbol{y}_{k+2} - CA\boldsymbol{x}_{k+1} - CB\boldsymbol{u}_{k} = 0 \\
& \vdots \\
& \boldsymbol{x}_{k+N} - A^{m}\boldsymbol{x}(k) - \sum_{l=0}^{m-1} A^{m-1-l}B\boldsymbol{u}(k+l) = 0 \\
& \boldsymbol{y}_{k+N} - CA^{m}\boldsymbol{x}(k) - \sum_{l=0}^{m-1} CA^{m-1-l}B\boldsymbol{u}(k+l) = 0
\end{array}$$
(2.9)

Where

$$Y(k) = [\mathbf{y}^{T}(k+1) \cdots \mathbf{y}^{T}(k+N)]^{T}$$

$$X(k) = [\mathbf{x}^{T}(k+1) \cdots \mathbf{x}^{T}(k+N)]^{T}$$

$$U(k) = [\mathbf{u}^{T}(k) \cdots \mathbf{u}^{T}(k+N-1)]^{T}$$
(2.10)

This resulting optimization problem is solved as one. Meaning all control variables for the entire control horizon are calculated simultaneously. In model predictive control this problem can be solved at each time increment kT_s , $k \in 1, 2, 3, ...$ This way only the first control vector u_k is used to control the system. It can be solved less often. This way more of the calculated U(k) vector is used to control the system. The formulation in 2.9 is known as Infinite Control Set Model Predictive Control (ICS-MPC). This is characterized by continuous control variables.

2.1.2 Principle of Sequential quadratic programming

Consider an optimization problem on the form below, with a non-quadratic cost function.

$$\min_{\mathbf{x}} f(\mathbf{x}) \tag{2.11}$$

$$a_i^T x = b_i, \quad i \in \mathscr{E}$$
(2.13)

$$a_i^T x \ge b_i, \quad i \in \mathscr{I}$$
 (2.14)

(2.15)

This problem can be solved using Sequential Quadratic Programming (SQP). The principle of this method is outlined in [12, p- 531], and rewritten below. The non-quadratic cost function can be approximated to the quadratic form

$$\min_{\mathbf{x}} \quad f_m + \nabla f_m^T p + \frac{1}{2} p^T \nabla_{\mathbf{x}\mathbf{x}} \mathscr{L}_m p \tag{2.16}$$

$$A_m p + c_m = 0 \tag{2.18}$$

$$\mathscr{L}(x,\lambda) = q(x) - \sum_{i \in \mathscr{E} \cup \mathscr{I}} \lambda_i c_i(x)$$
(2.19)

This problem can be solved using an iterative method known as Newtons method.

$$\begin{bmatrix} x_{m+1} \\ \lambda_{m+1} \end{bmatrix} = \begin{bmatrix} x_m \\ \lambda_m \end{bmatrix} + \begin{bmatrix} p_x \\ p_\lambda \end{bmatrix}$$
(2.20)

$$\begin{bmatrix} \nabla_{xx}^2 \mathscr{L}_m & -A_m^T \\ A_m & 0 \end{bmatrix} \begin{bmatrix} p_x \\ p_\lambda \end{bmatrix} = \begin{bmatrix} -\nabla f_m \\ -c_m \end{bmatrix}$$
(2.21)

An initial guess x_0 is made, and the method iterates until convergence. This is the most basic of SQP methods. More advanced methods exists, and the problem can also have inequality constraints. However the concept of quadratic approximation, and iteration until convergence is the same.

2.2 MPC for gate control in power electronics

MPC can be used to control many different applications in power electronics. These include Active Front Ends, Active Filters or a Matrix Converters [15]. Many different implementations for controlling gate switches with MPC have been formulated. The simplest method is using ICS-MPC to generate voltage references. Then to generate gate signals with PWM [16]. A more advanced method is to directly have the MPC generate the gate signals [17]. This is known as Finite Control Set Model Predictive Control (FCS-MPC). This method is typically more computationally expensive, but has better performance. Computational expenses is one of the major factors limiting the development of MPC for gate controllers. This is especially the case for FCS-MPCs. A typical power electronics application switches the gate switches at several kilohertz. Meaning an FCS-MPC would have to solve an optimization problem in under a millisecond, in many cases in even shorter time. In order to work around this, a method called sphere decoding has been developed for solving FCS-MPCs less expensively [18] ,[19]. The first MPC controlled drive entered the marked in 2011. As a result of continuous hardware improvements for data processing, such as the FPGA [14].

2.3 Finite Control Set Model Predictive Control

Finite Control Set Model Predictive Control(FCS-MPC) involves control variables with a finite set of permitted values. Meaning the control variables either can be integers, decimals, or some other finite set of real, or complex numbers. Any FCS-MPC problem, with a linear cost function and constraints, can be modelled as a Mixed Integer Linear Programming(MILP) problem



Figure 2.1: Converter and LCL circuit for current control[1, p-1]

. Where all or some of the control variables are positive integers. An example is presented in equation 2.22 [10, p- 12].

$$\begin{array}{ll} \underset{x,z}{\text{minimize}} & f_1 x + f_2 z\\ \text{subject to} & A_1 x + A_2 z \le b\\ & z & \text{integer} \end{array}$$
(2.22)

Any MILP problem is NP-complete [10, p- 12]. The computational cost for solving it is then defined as \bigcup {NTIME(n^k)| $k \le 1$ } [11, p- 78]. A computational cost of n^k means the problem in best case can be solved in polynomial time. While in some cases require exponential time to solve. Those FCS-MPC problems take too long time to solve for most applications, for longer control horizons.

2.4 Integer Least square formulation of FCS-MPC

In [1] FCS-MPC is used to control gate switches. In this paper a grid connected converter is used to control current in an LCL circuit. A Circuit diagram of the implementation is depicted in figure 2.1. This section presents how the model and cost function is formulated. Then presents how it is reformulated into an Integer Least Square(ILS) problem.

2.4.1 Problem formulation

To formulate the problem two steps are involved. The first is to formulate a linear control model. The second is to formulate the cost function and MPC.



Figure 2.2: Per-phase model of the LCL-filter [1, p-1]

Controller model

Figure 2.2 present a single phase representation of the circuit in figure 2.1. The states variable is defined as $x = [\mathbf{i}_1 \ \mathbf{i}_2 \ \mathbf{v}_c]^T$. It contains the input currents, output currents, and the capacitor voltages. The currents are defined in the $\alpha\beta$ frame, with $\mathbf{i}_1 = [\mathbf{i}_{1\alpha} \ \mathbf{i}_{1\beta}]$. The control variables are defined as $\mathbf{u} = [u_1 \ u_2 \ u_3]^T$. These are restricted to $u_1, \ u_2 \ u_3 \in \{-1, 1\}$. Grid voltages are defined as $\mathbf{v}_g = [v_{ga} \ v_{gb} \ v_{gc}]^T$. $\mathbf{K}_{\alpha\beta}$ denotes the rotation matrix from abc-frame to $\alpha\beta$ frame, using the Clark Transform from 2.7. The linear system model is expressed as equations 2.23 and 2.24.

$$\frac{d\boldsymbol{x}(t)}{dt} = \boldsymbol{F}\boldsymbol{x}(t) + \boldsymbol{G}\boldsymbol{u}(t) + \boldsymbol{P}\boldsymbol{v}_{g}(t)$$
(2.23)

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) \tag{2.24}$$

$$\boldsymbol{F} = \begin{bmatrix} \frac{R_c + R_1}{-L_1} & 0 & \frac{R_c}{L_1} & 0 & \frac{1}{-L_1} & 0\\ 0 & \frac{R_c + R_1}{-L_1} & 0 & \frac{R_c}{L_1} & 0 & \frac{1}{-L_1}\\ \frac{R_c}{L_2} & 0 & \frac{R_c + R_2}{-L_2} & 0 & \frac{1}{L_2} & 0\\ 0 & \frac{R_c}{L_2} & 0 & \frac{R_c + R_2}{-L_2} & 0 & \frac{1}{L_2}\\ \frac{1}{C} & 0 & \frac{1}{-C} & 0 & 0 & 0\\ 0 & \frac{1}{C} & 0 & \frac{1}{-C} & 0 & 0 \end{bmatrix}$$

$$\boldsymbol{G} = \begin{bmatrix} \frac{V_D}{2L_1} & 0 & 0 & 0 & 0\\ 0 & \frac{V_D}{2L_1} & 0 & 0 & 0 & 0 \end{bmatrix} \boldsymbol{K}_{\alpha\beta}$$

$$(2.26)$$

$$\boldsymbol{P} = \begin{bmatrix} 0 & 0 & \frac{1}{-L_2} & 0 & 0 & 0\\ 0 & 0 & 0 & \frac{1}{-L_2} & 0 & 0 \end{bmatrix} \boldsymbol{K}_{\alpha\beta}$$

$$\begin{bmatrix} k_1 & 0 & 0 & 0 & 0\\ 0 & k_1 & 0 & 0 & 0 & 0\\ 0 & k_1 & 0 & 0 & 0 & 0 \end{bmatrix}$$
(2.27)

$$\boldsymbol{C} = \begin{bmatrix} 0 & k1 & 0 & 0 & 0 & 0 \\ 0 & 0 & k2 & 0 & 0 & 0 \\ 0 & 0 & 0 & k2 & 0 & 0 \\ 0 & 0 & 0 & 0 & k3 & 0 \\ 0 & 0 & 0 & 0 & 0 & k3 \end{bmatrix}$$
(2.28)

The model Matrixes F,G and P are then discretized with exact discretiation. The results is the system equations 2.29, 2.30 and 2.31. Here T_s is the sampling time, and k denotes the current position in time.

$$A = e^{FTs} \tag{2.29}$$

$$B = -F^{-1}(I - A)G (2.30)$$

$$T = -F^{-1}(I - A)P (2.31)$$

The model formulation in 2.23 and 2.24 then become.

$$x(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{B}\mathbf{u}(k) + \mathbf{T}\mathbf{v}_g(t)$$
(2.32)

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) \tag{2.33}$$

Model Predictive control

Optimization is achieved by minimizing the cost function 2.34. Here y_e denotes the state errors. The second term represents the objective to lower switching losses. This is achieved by minimizing the switching frequency. Which is weighted by the factor λ_u .

$$J = \sum_{l=k}^{k+N-1} ||\boldsymbol{y}_{e}(l+1)||_{2}^{2} + \lambda_{u} ||\Delta \boldsymbol{u}(l)||_{2}^{2}$$
(2.34)

$$\mathbf{y}_{e}(k+1) = \mathbf{y}^{*}(k+1) - \mathbf{y}(k)$$

$$\Delta \mathbf{u}(k) = \mathbf{u}(k) - \mathbf{u}(k-1)$$
(2.35)

In [1], the problem is then reformulated. Firstly the model formulation is simplified. Equation 2.32 is successively applied to itself. Resulting in equation 2.36. Inserting 2.36 into 2.33 resulting in equation 2.37. The model can then be written as equations 2.39 and 2.40.

$$x(k+m) = A^{m} \mathbf{x}(k) + \sum_{l=0}^{m-1} A^{m-1-l} \mathbf{B} u(k+l) + \sum_{l=0}^{m-1} A^{m-1-l} \mathbf{T} \mathbf{v}_{\mathbf{g}}(k+l)$$
(2.36)

$$y(k+m) = CA^{m}x(k) + \sum_{l=0}^{m-1} CA^{m-1-l}Bu(k+l) + \sum_{l=0}^{m-1} CA^{m-1-l}Tv_{g}(k+l)$$
(2.37)

for
$$m = 0, ..., N - 1.$$
 (2.38)

$$Y(k) = [\boldsymbol{y}^{T}(k+1) \quad \cdots \quad \boldsymbol{y}^{T}(k+N)]^{T}$$
(2.39)

$$Y(k) = \Gamma \boldsymbol{x}(k) + \Upsilon \boldsymbol{U}(k) + \Psi \boldsymbol{V}_{\boldsymbol{g}}(K)$$
(2.40)

where (2.41)

$$\boldsymbol{\Gamma} = \begin{bmatrix} \boldsymbol{C}\boldsymbol{A} & \boldsymbol{C}\boldsymbol{A}^2 & \boldsymbol{C}\boldsymbol{A}^3 & \cdots & \boldsymbol{C}\boldsymbol{A}^N \end{bmatrix}$$
(2.42)

$$\Upsilon = \begin{vmatrix} CB & 0 & \cdots & 0 \\ CAB & CB & \cdots & 0 \\ \vdots & \vdots & \vdots \\ CAN^{-1}B & CAN^{-2}B & CB \end{vmatrix}$$
(2.43)

$$\Psi = \begin{bmatrix} CA^{N-1}B & CA^{N-2}B & \cdots & CB \end{bmatrix}$$

$$\Psi = \begin{bmatrix} CT & 0 & \cdots & 0 \\ CAT & CT & \cdots & 0 \\ \vdots & \vdots & & \vdots \\ CA^{N-1}T & CA^{N-2}T & \cdots & CT \end{bmatrix}$$
(2.44)

Second the cost function is rewritten. Inserting 2.40 into 2.34 results in equations 2.45 and 2.46.

$$J = ||\mathbf{\Gamma}\mathbf{x}(k) + \mathbf{\Upsilon}\mathbf{U}(k) + \mathbf{\Psi}\mathbf{V}_{\mathbf{g}}(k) - \mathbf{Y}^{*}(k)||_{2}^{2} + \lambda_{u}||\mathbf{SU}(k) - \mathbf{Eu}(k-1)||_{2}^{2}$$
(2.45)

$$J = ||\mathbf{\Gamma}\mathbf{x}(k) - \mathbf{Y}^{*}(k)||_{2}^{2} + ||\mathbf{\Psi}\mathbf{V}_{\mathbf{g}}(k)||_{2}^{2} + \lambda_{u}||\mathbf{Eu}(k-1)||_{2}^{2} + 2[\mathbf{\Gamma}\mathbf{x}(k) - \mathbf{Y}^{*}(k)]^{T}\mathbf{\Upsilon}\mathbf{U}(k) + 2[\mathbf{\Gamma}\mathbf{x}(k) - \mathbf{Y}^{*}(k)]^{T}\mathbf{\Upsilon}\mathbf{U}(k) + 2[\mathbf{\Upsilon}\mathbf{U}(k)]^{T}\mathbf{\Psi}\mathbf{V}_{\mathbf{g}}(k) - 2\lambda_{u}[\mathbf{Eu}(k-1)]^{T}\mathbf{SU}(k) + U(k)^{T}\{\mathbf{\Upsilon}^{T}\mathbf{\Upsilon} + \lambda_{u}\mathbf{S}^{T}\mathbf{S}\}\mathbf{U}(k)$$
(2.46)

Here *S* and *E* are given in [2, appendix]. Presented in equation 2.47.

$$S = \begin{bmatrix} I & 0 & \cdots & 0 \\ -I & I & \cdots & 0 \\ 0 & -I & \cdots & 0 \\ \vdots & \vdots & & \vdots \\ 0 & 0 & \cdots & I \end{bmatrix}, \quad E = \begin{bmatrix} I \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$
(2.47)

The cost function can be rewritten to the more compact form in equation 2.48.

$$J = \theta(k) + 2\Theta^{T}(k)\boldsymbol{U}(k) + ||\boldsymbol{U}(k)||_{\boldsymbol{\theta}}^{2}$$
(2.48)

$$\theta(k) = ||\mathbf{\Gamma}\mathbf{x}(k) - \mathbf{Y}^{*}(k)||_{2}^{2} + ||\mathbf{\Psi}\mathbf{V}_{\mathbf{g}}(k)||_{2}^{2} + \lambda_{u}||\mathbf{E}\mathbf{u}(k-1)||_{2}^{2} + (2.50)$$

$$2[\mathbf{\Gamma}\mathbf{x}(k) - \mathbf{Y}^{+}(k)]^{T} \Psi \mathbf{V}_{\mathbf{g}}(k)$$

$$\boldsymbol{\Theta} = \left\{ [\boldsymbol{\Gamma} \boldsymbol{x}(k) - \boldsymbol{Y}^*(k)]^T \boldsymbol{\Upsilon} + \boldsymbol{V}_{\boldsymbol{g}}(k)^T \boldsymbol{\Psi}^T \boldsymbol{\Upsilon} - \lambda_u [\boldsymbol{E} \boldsymbol{u}(k-1)]^T \boldsymbol{S} \right\}^T$$
(2.51)

$$\boldsymbol{Q} = \boldsymbol{\Upsilon}^T \boldsymbol{\Upsilon} + \lambda_u \boldsymbol{S}^T \boldsymbol{S} \tag{2.52}$$

Finding the optimal control sequence can then be done solving the least square problem

$$\boldsymbol{U}_{opt}(k) = \underset{\boldsymbol{U}(k)}{\arg\min} ||\boldsymbol{H}\boldsymbol{U}(k) - \boldsymbol{\bar{\boldsymbol{U}}} unc(k)||_{2}^{2}$$

where
$$\boldsymbol{U}_{unc} = -\boldsymbol{Q}^{-1}\boldsymbol{\Theta}(k)$$

$$\boldsymbol{H}^{T}\boldsymbol{H} = \boldsymbol{Q}$$

$$\boldsymbol{\bar{\boldsymbol{U}}}_{unc}(k) = \boldsymbol{H}\boldsymbol{U}_{unc}(k)$$

(2.53)

2.5 FCS-MPC without binary variables

FCS-MPC has in most cases an exponential computational cost, as stated in section 2.3. One trick to mitigate this is presented in paper [3]. This paper discusses how MPC can be used to minimize electric energy consumption in an electric vehicle. The car model has one control input. This input is accelerator pedal travel. The force at the wheels as a function of pedal travel is presented in figure 2.3. The vehicle experiences a constant energy recovery brake force for negative pedal positions.

The optimization problem is formulated to take two inputs. The first is a break force F_{break} , and the second is a traction force F_{trac} . The break force is either zero or the constant value $F_{brake,min}$, making it a binary control variable. These control actions must act independently. Meaning no break force is applied when a traction force is applied. The optimization problem in [3, equation- 13] is presented in equations 2.54. Due to t_4 , F_{break} will tend to one of the two binary values, while remaining a continuous variable.



Figure 2.3: Discontinuous control input: as soon as the accelerator pedal is released, the force at the wheels steps to constant negative value. [3, figure- 2]

$$min \int_{s_0}^{s_{end}} (t_1 + t_2 + t_3 + t_4 + t_5)$$
(2.54)

with
$$t_1$$
 to t_3 being energy consumption terms, and (2.55)

$$t_4 = Q_4 (-F_{break}(s)^2 + F_{brake,min}F_{brake}(s))^2$$
(2.56)

$$t_5 = Q_5 (F_{trac}(s) F_{brake}(s))^2$$
(2.57)

2.6 Estimating losses in a power converter

For any switching power converter there is always a trade-off. Higher switching frequency means better reference tracking. This saves electric power as a greater proportion of active power is delivered to all components on the AC power-grid. However energy is always lost when switching any transistor or switch. Higher switching frequency then results in a greater loss of power. Both switching losses and harmonic distortion losses will be discussed below.

2.6.1 Switching losses

Chapter eight in [5] discusses the switching losses in a MOSFET. When opening a MOSFET two things happen. The Voltage from drain to source, V_d , switches from V_{DC} to 0, while the drain current, Id, switches from 0 to $I_d(t_{sw} + t_{fall})$. Where $I_d(t_{sw} + t_{fall})$ is the current through the MOSFET when V_d has fallen to zero. When closing the MOSFET I_d goes to zero, while V_d goes to V_{DC} [5]. In [5, figure- 8.3] power loss in one switching of a power converter is defined as current multiplied by voltage integrated over the switching time. Where the switching time is



Figure 2.4: The area under Vds(t)xId(t) defines the switching cost [5, figure-8.3]

the time it takes for the MOSFET to toggle states. Figure 2.4 shows how switching cost is defined graphically.

2.6.2 Total harmonic distortion

Harmonic components of a sinusoidal signal do in most cases not contribute to usable electrical power. Harmonic distortion is then a way to quantify harmonic power loss. Total harmonic distortion (THD) represents the influence of harmonics on a signal in one value.

"It is a measure of the effective value of the harmonic components of a distorted waveform, which is defined as the rms of the harmonics expressed in percentage of the fundamental ... component...". [4, p. 19]

THD related to current is defined as in equation 2.58 [4, p. 19]. $I^{(i)}$ is the i-th harmonic of the current signal I(t). And is given as the FFT output at $f = i \cdot f_b$. Here f_b is the frequency of the fundamental current component. Related to voltage the formula is the same. Advantages of using THD is that it can easily be calculated, and is commonly used. Disadvantages is that details on spectrum information is lost [4, p. 19].

$$THD_i = \frac{\sqrt{\sum_{h=2}^{\infty} (I^{(h)})^2}}{I^{(1)}}$$
(2.58)

2.7 Clark Transformation

A balanced three phase system satisfies equation 2.59 [9, equation. 2.6]. This constraint removes one degree of freedom from three phase system. Balanced three phase currents and voltages can



Figure 2.5: Reference frames and vector projections of the clark transform

then be represented using only two variables. This is the essence of the clark transform, which is a conversion from the stationary abc-frame to the stationary $\alpha\beta$ -frame. Figure 2.5 displays the A-axis, B-axis and C-axis of a balanced three phase system, and how the α -axis and β -axis are defined relative to those.

$$a_A(t) + a_B(t) + a_C(t) = 0 (2.59)$$

equation 2.60 defines the transformation between the two systems. A factor of $\frac{2}{3}$ is multiplied to ensure signals in both reference frames have the same amplitude. A third component is also added to the $\alpha\beta$ -frame, resulting in an $\alpha\beta$ 0-frame. However for a three phase system with equation 2.59 holding, the 0-component is zero.

$$\begin{bmatrix} a_{\alpha}(t) \\ a_{\beta}(t) \\ a_{0}(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} a_{A}(t) \\ a_{B}(t) \\ a_{C}(t) \end{bmatrix}$$
(2.60)

2.8 PWM for controlling gate switches

In many cases control of gate switches is done by generating a continuous voltage references. In this case PWM is used to generate control signals. Figure 2.6 displays how this is done for one of three phases. The triangle wave carrier signal of the upper figure is of much higher frequency than the voltage control signal. The gate switch for the phase in question switches on when the voltage control signal is higher than the triangle carrier signal. When the voltage control signal is lower, the gate switches off. The switching frequency is constant, and equal to the frequency



Figure 2.6: Control scheme for PWM control of gate switches [8, p-15]

of the triangle wave.

2.9 LCL oscillations

Using gate switches to create AC voltage induces noise on the AC lines. To mitigate this an LCL filter is often fitted at the AC output of the gate switches. With the inductances in series, and capacitor in parallel. This structure is also present in 2.8. Here the capacitor and both inductors also have internal resistances. All LCL circuits have a resonance frequency. For LCL filters without resistances this is given as equation 2.61 [13, p-293].

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{2.61}$$

2.10 MPC for harmonic mitigation in a ship power system

This section presents the harmonic mitigating MPC with hysteresis controller, and ship power system model derived in [6]. The ship power system is displayed with figures and mathematical models. The problem formulation of the MPC is presented mathematically.

Parameter	Value
L_{G1}	0.2 [pu]
L_{G2}	0.2 [pu]
L_{MB}	0.04 [pu]
R_{G1}	$0.1 \cdot L_{G1} \cdot \omega[pu]$
R_{G2}	$0.1 \cdot L_{G2} \cdot \omega[pu]$
R_{MB}	$0.1 \cdot L_{MB} \cdot \omega[pu]$
Generator 1	1 MVA
Generator 2	1 MVA
Motor 1	1 MVA
Motor 2	MVA
Active filter	200kVa
Voltage (RMS)	690V 50kHz

Table 2.1: Power grid parameters of the ship power system



Figure 2.7: Model of the ship power system from [6, p-77]

2.10.1 Model of the ship power system

Before optimizing harmonics, a model of the ship power system needs to be derived, which is done in [6, section- 3.2]. This is based on a simplified equivalent of a marine Platform Supply Vessel (PSV) power system[6, page- 76]. It contains two AC lines, two diesel generators, an Active power filter and two motor loads. A block diagram of this is presented in figure 2.7. Here the generators, GEN1 and GEN2, supply their own AC power bus. A transformer is connected to each bus, followed by a 12-pulse rectifier, a DC to AC converter and an electric motor. The parameter values in this circuit is presented in table 2.1.



Figure 2.8: Simplified implementable model of the ship power system from [6, p-104]

Parameter	Parameter values
L_1	0.30 [mH]
L_2	0.30 [mH]
R_1	0.03 [Ω]
R_2	0.03 [Ω]
R_C	10.0 Ω
С	30.0 <i>µ</i> F

Table 2.2: Parameters for the LCL filter between bus 2 and the APF [6]

Implementable electric circuit

In [6] this model is further simplified and altered in order to simulate the APF in Simulink. This model is depicted in figure 2.8. The DC to AC converters and motors are switched for a resistor and capacitor in parallel. A filtration circuit is added between Bus 2 and the APF. An LCL circuit is added between the APF and bus 2. Parameter values for the LCL circuit is given in table 2.1. A shunt capacitor is added in parallel to each load. These are added in order to decouple the states representing current in the inductors. The voltage over these capacitors were also used to measure THD on the bus voltages. The generator currents are indicated by i_{G1} and i_{G2} .

2.10.2 MPC implementation

Harmonic mitigation is done using Model Predictive Control generating a reference for the active filter currents. This MPC is further investigated in this section. Reference tracking is done using a hysteresis controller, controlling gate switches. The MPC is implemented in the abcframe. *"This is a desired property, which might be crucial in the pursue of meeting the application's real-time demands" [6, p- 131, line- 4]*. The DC-source supplying the active filter currents through gate switches is not grounded. As a consequence, the three phases of *I*_{AF} are balanced. In a balanced three phase system independent phase control is impossible. As a result the abcframe reference is clark-transformed to $\alpha\beta$ 0-frame, the zero component is then set to zero, before the reference is transformed back to abc-frame.

Overall MPC structure

The model predictive control is formulated as equation set 2.62 [6, p-129].

$$\min_{\mathbf{x}(t), \mathbf{z}(t), \mathbf{u}(t)} \quad V(\mathbf{x}(t), \mathbf{z}(t), \mathbf{u}(t)) = \int_{t_0}^{t_0 + T} l(\mathbf{x}(t), \mathbf{z}(t), \mathbf{u}(t)) dt
\dot{\mathbf{x}}(t) = f(\mathbf{x}(t), \mathbf{z}(t), \mathbf{u}(t))
g(\mathbf{x}(t), \mathbf{z}(t), \mathbf{u}(t)) = 0
h(\mathbf{x}(t), \mathbf{z}(t), \mathbf{u}(t)) \le 0
\forall t \in [t_0, t_0 + T]$$
(2.62)

The equality constraint $g(\cdot)$ and inequality constraint $h(\cdot)$ is further specified in [6, section-5.2.1]. State and control vectors are given below.

$$\boldsymbol{x} = [\boldsymbol{i}_{G1}^{T}, \boldsymbol{i}_{G2}^{T}, \boldsymbol{i}_{MB}^{T}, \boldsymbol{v}_{S1}^{T}, \boldsymbol{v}_{S1}^{T}]$$

$$\boldsymbol{z} = [\boldsymbol{i}_{L1}^{T}, \boldsymbol{i}_{L2}^{T}]$$

$$\boldsymbol{u} = \boldsymbol{i}_{AF} = [i_{AF,a}, i_{AF,b}, i_{AF,c}]$$
(2.63)

With the cost matrices $Q_{1,2,3}$ the cost function $l(\cdot)$ is given as.

$$l(\boldsymbol{x}(t), \boldsymbol{z}(t), \boldsymbol{u}(t)) = \boldsymbol{i}_{G1}^{T} Q_1 \boldsymbol{i}_{G1} + \boldsymbol{i}_{G2}^{T} Q_2 \boldsymbol{i}_{G2} + \boldsymbol{u}^{T} Q_u \boldsymbol{u}$$
(2.64)

Dynamics

The dynamics equation $f(\cdot)$ is derived 2.65. Which in turn is derived from Kirchhoff's laws applied to the circuit in figure 2.8.

$$L_{G1} \frac{d\mathbf{i}_{G1}}{dt} = -R_{G1} \mathbf{i}_{G1} - \mathbf{v}_{C1}$$

$$C_{1} \frac{d\mathbf{v}_{C1}}{dt} = \mathbf{i}_{G1} - \mathbf{i}_{MB} - \mathbf{i}_{L1}$$

$$L_{MB} \frac{d\mathbf{i}_{MB}}{dt} = \mathbf{v}_{C1} - \mathbf{v}_{C2} - R_{MB} \mathbf{i}_{MB}$$

$$C_{2} \frac{d\mathbf{v}_{C2}}{dt} = \mathbf{i}_{MB} + \mathbf{i}_{G2} - \mathbf{i}_{L2} + \mathbf{i}_{AF}$$

$$L_{G2} \frac{d\mathbf{i}_{G2}}{dt} = -R_{G2} \mathbf{i}_{G2} - \mathbf{v}_{C2}$$
(2.65)

Load currents

When using a 12-pulse rectifier the load will introduce harmonics back into the power grid. For a 12 pulse rectifier these harmonics are of order 11, 13, 23, 25, 35 etc. Meaning the load currents i_{L1} and i_{L2} are modelled as ideal current sources. These are mathematically given by equation 2.66.

$$\boldsymbol{I}_{Lj}(t) = \begin{bmatrix} \Sigma_{i} I^{a}_{L,j,i} \sin(i(\omega t + \phi^{a}_{L,j,i})) \\ \Sigma_{i} I^{b}_{L,j,i} \sin(i(\omega t + \phi^{b}_{L,j,i} - \frac{2\pi}{3})) \\ \Sigma_{i} I^{c}_{L,j,i} \sin(i(\omega t + \phi^{c}_{L,j,i} + \frac{2\pi}{3})) \end{bmatrix} \quad \forall i \in H, j \in 1, 2$$
(2.66)

H is the set of harmonics to b mitigated. The angular velocity $\omega = 2\pi f$, with *f* being the fundamental component. $I_{L,j,i}^k$ and $\phi_{L,j,i}^k$ are the harmonic amplitudes and phases for $k \in a, b, c$.
Chapter 3

Implementing and testing gate controlling MPCs, and defining test cases for cascaded MPC

This chapter describes the implementation of all gate controlling MPCs. First is a description of two test setups that were used to test gate controlling MPCs outside the cascaded structure. Then a mathematical formulation of three gate controlling MPCs, and how these were aquired. Finally there is a description of the test cases that were simulated for the cascaded MPC structure.

3.1 Testing gate controlling MPCs outside the cascaded structure

Testing all implementations was done using two test setups. Initial tests were done by simulating a single iteration of the algorithm. Measuring computation times, and getting a rough idea of reference tracking performance. While system wide tests were done using a simplified version of the model from section 2.10.1. Here the main goal was to simulate on a simpler circuit, simplifying debugging.



Figure 3.1: Reference signal sent to the hysteresis controller

3.1.1 Single MPC iteration

All gate controlling MPCs were designed to track a current reference. For the single iteration this reference had to be designed manually. For the MPC in section 2.10.2 the overall objective was harmonic mitigation. Meaning the MPC designed in this thesis had to be good at tracking harmonics in a current signal. As described in section 2.10.1 a 12-pulse rectifier load injects harmonics of order 11,13,23 and 25 being the most significant. As a result, a signal with harmonics 11 and 13 was sent as a reference to the single MPC iteration. A mathematical description is given in equation 3.1-3.2.

$$i_{ref,a} = \frac{i_{ref,ampl}sin(11\omega t)}{11} + \frac{i_{ref,ampl}sin(13\omega t)}{13}$$
(3.1)

$$i_{ref,b} = \frac{i_{ref,ampl}sin(11\omega t - \frac{2\pi}{3})}{11} + \frac{i_{ref,ampl}sin(13\omega t - \frac{2\pi}{3})}{13}$$
(3.2)

$$i_{ref,c} = \frac{i_{ref,ampl} sin(11\omega t + \frac{2\pi}{3})}{11} + \frac{i_{ref,ampl} sin(13\omega t + \frac{2\pi}{3})}{13}$$
(3.3)

When choosing the amplitude of the current reference, the generated reference signal was compared to the reference signal given by the APF when implemented with a hysteresis controller. In figure 3.1 the reference from the MPC to the hysteresis controller is displayed. Here the maximum amplitude is around 120 Amperes. The amplitude of the reference to the FCS-MPC was then chosen accordingly. As the single MPC iteration test was not used to generate any results in this thesis, some deviation were accepted. The result was the reference signal shown in figure 3.2.

For all gate controlling MPCs in this thesis generator voltages are external states. External states needs to be estimated forward in time when used in MPCs. For all testing with a single MPC iteration, the generator voltage is estimated to be as described below, with $V_b = 690 \frac{sqrt2}{sqrt3}$.



Figure 3.2: Current reference signal when testing the FCS-MPC



Figure 3.3: Test circuit implemented in simulink [1, p- 1]. Parameter values are given in table 2.1

$$V_{g} = \begin{bmatrix} V_{b}sin(\omega t) \\ V_{b}sin(\omega t - \frac{2\pi}{3}) \\ V_{b}sin(\omega t + \frac{2\pi}{3}) \end{bmatrix}$$
(3.4)

3.1.2 Multiple FCS-MPC iterations in Test Circuit

The test circuit used for simulating the FCS-MPC was copied from the circuit in figure 2.1. This is again presented in figure 3.3. Parameter values are taken from [6, table- 4.1], and are presented in table 2.1.

Simulations on the test circuit ran for 0.01 seconds. As for the single FCS-MPC iteration case, the choice of reference signal i important. Therefore the same reference signal is given to the test circuit as to the single FCS-MPC iteration. This signal is given in figure 3.2. Here the signal is continued over the entire simulation time with 500 samples added. In order to make sure the FCS-MPC had a reference signal even at the last iteration.

3.2 Implementation basis for all gate controlling MPCs

Implementation of both an ICS-MPC and an FCS-MPC was done for this thesis. In this section a general presentation is made, with challenges and decisions common for both implementations. First a presentation of where and how the model were derived. Followed by a presentation on choosing the right reference frame of control. Then How the test circuit from section 3.1.2 were used to verify all implementations.

3.2.1 Model inspiration

All MPC implementations done in this thesis were based on the model in equations 2.32 and 2.33. These are rewritten below in equation set 3.5. How the model matrices A, B and T are derived is presented in section 2.4.1.

$$\begin{aligned} \mathbf{x}(k+1) &= \mathbf{A}\mathbf{x}(k) + \mathbf{B}\mathbf{u}(k) + \mathbf{T}\mathbf{v}_{g,k} \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) \end{aligned} \tag{3.5}$$

3.2.2 reference frame for control

The matrixes *A*, *B*, *T* and *C* in equation 3.5, are all presented in $\alpha\beta$ -frame. This is further specified in section 2.4.1. When controlling in the $\alpha\beta$ -frame the three phase system has to be balanced. Meaning equation 2.59 has to hold. When the three phase system is balanced, the zero component of the clark transform will be zero. This component can then be removed, leaving only the α and β component. As discussed in section 2.10.2 the master MPC is implemented in the abc-frame. The current reference given to the MPCs is then in abc-frame. Due to an ungrounded DC voltage source, the MPCs could still be implemented in $\alpha\beta$ -frame. In figure 3.3, and the APF block in figure 2.8, the DC voltage is not connected to ground. Hence the current entering the LCL-filter and gate switches in one or two phases, has to return the remaining phases. Meaning that the sum of currents at L2. The current at L2 is also the current controlled by the MPCs. Therefore the MPCs could be implemented in the $\alpha\beta$ -frame.

3.2.3 Verification in test circuit

Before any implementation was inserted into the cascaded MPC structure in the complete ship power system model, they were tested. These tests were conducted on the test circuit from figure 3.3. The purpose of these tests was to ensure all MPC implementations functioned in Simulink as well as Matlab. It also made sense to test Simulink implementations in a controlled environment, with a controlled generator voltage. No results from these test are displayed in this thesis.

3.3 FCS-MPC using yalmip

One option for a gate controlling MPC was using an Integer Least Square FCS-MPC (ILS-FCS-MPC) as described in section 2.4. The ILS-FCS-MPC was implemented using YALMIP to solve 2.53. The optimization problem is rewritten below.

$$J = \theta(k) + 2\boldsymbol{\Theta}^{T}(k)\boldsymbol{U}(k) + ||\boldsymbol{U}(k)||_{\boldsymbol{Q}}^{2}$$
(3.6)

(3.7)

$$\theta(k) = ||\mathbf{\Gamma}\mathbf{x}(k) - \mathbf{Y}^*(k)||_2^2 + ||\mathbf{\Psi}\mathbf{V}_{\mathbf{g}}(k)||_2^2 + \lambda_u ||\mathbf{E}\mathbf{u}(k-1)||_2^2 + \sum_{\mathbf{r}} (3.8)$$

$$2[\mathbf{\Gamma}\mathbf{x}(k) - \mathbf{Y}^*(k)]^T \Psi \mathbf{V}_{\mathbf{g}}(k)$$

$$\boldsymbol{\Theta} = \left\{ [\boldsymbol{\Gamma} \boldsymbol{x}(k) - \boldsymbol{Y}^{*}(k)]^{T} \boldsymbol{\Upsilon} + \boldsymbol{V}_{\boldsymbol{g}}(k)^{T} \boldsymbol{\Psi}^{T} \boldsymbol{\Upsilon} - \lambda_{u} [\boldsymbol{E} \boldsymbol{u}(k-1)]^{T} \boldsymbol{S} \right\}^{T}$$
(3.9)

$$\boldsymbol{Q} = \boldsymbol{\Upsilon}^T \boldsymbol{\Upsilon} + \lambda_{\mu} \boldsymbol{S}^T \boldsymbol{S}$$
(3.10)

The model matrices $A, B, C, \Gamma, \Upsilon$ and Ψ were all calculated in advance. On each iteration $\Theta, Q, U_{unc}, \tilde{U}_{unc}$ and H were calculated. Then the optimal control sequence U_{opt} were solved for. Overall the control flow could then be expressed as figure 3.4. For all simulations in the cascaded MPC structure λ_u was chosen as small as possible at $\lambda_u = 10^{-8}$.

3.3.1 Reformulating binary control variables

where

The ILS-FCS-MPC generated control signals with binary values ± 1 . In Simulink control variables had be the binary variables 0 or 1. Each control variable value were passed through the function



Figure 3.4: Flow chart of simulation with least-square FCS-MPC

$$u_{new} = \frac{1}{2}(u_{old} + 1) \tag{3.11}$$

Gates were controlled by u_{new} .

3.4 Continuous Control Variable FCS-MPC using Acado

As mentioned in section 2.3, solving an FCS-MPC problem might result in exponential computational cost. It was then interesting to implement the FCS-MPC without the use of binary variables. This was called a Continuous Control Variable FCS-MPC (CCV-FCS-MPC). Implementation was done using the method outlined in section 2.5. Here all control variables are maintained continuous, while a cost function term is added, forcing control variables to binary values.

3.4.1 Model formulation and setup

ACADO accepts a discrete state space model when solving MPC problems. This meant the discretized model from 3.5 could be directly implemented in ACADO. The overall FCS-MPC formulation could then be derived by reformulate equation 2.9 to accommodate the model in equation 3.5. The results is the model formulation in equations 3.12 and 3.13.

$$\begin{array}{l} \min_{\boldsymbol{U}_{k}} \quad J(\boldsymbol{Y}_{k}, \boldsymbol{X}_{k}, \boldsymbol{U}_{k}) \\ & \text{subject to} \\ \boldsymbol{x}_{k+1} - A\boldsymbol{x}_{k} - B\boldsymbol{u}_{k} - T\boldsymbol{v}_{g,k} = 0 \\ \boldsymbol{y}_{k+1} - C\boldsymbol{x}_{k+1} = 0 \\ \boldsymbol{x}_{k+2} - A^{2}\boldsymbol{x}_{k} - AB\boldsymbol{u}_{k} - T\boldsymbol{v}_{g,k+1} = 0 \\ \boldsymbol{y}_{k+2} - CA\boldsymbol{x}_{k+1} - CB\boldsymbol{u}_{k} = 0 \\ \vdots \\ \boldsymbol{x}_{k+N} - \boldsymbol{A}^{N}\boldsymbol{x}(k) - T\boldsymbol{v}_{g,k+N-1} - \sum_{l=0}^{N-1} \boldsymbol{A}^{N-1-l}\boldsymbol{B}\boldsymbol{u}(k+l) = 0 \\ \boldsymbol{y}_{k+N} - \boldsymbol{C}\boldsymbol{A}^{N}\boldsymbol{x}(k) - \sum_{l=0}^{N-1} \boldsymbol{C}\boldsymbol{A}^{N-1-l}\boldsymbol{B}\boldsymbol{u}(k+l) = 0 \\ |\boldsymbol{u}_{i,j}| \leq 1.1 \quad \forall i \in \{k, k+1, \dots, k+N-1\}, \quad \forall j \in \{1, 2, 3\} \end{array} \right)$$
(3.12)

Where

$$Y(k) = [\mathbf{y}^{T}(k+1) \cdots \mathbf{y}^{T}(k+N)]^{T}$$

$$X(k) = [\mathbf{x}^{T}(k+1) \cdots \mathbf{x}^{T}(k+N)]^{T}$$

$$U(k) = [\mathbf{u}^{T}(k) \cdots \mathbf{u}^{T}(k+N-1)]^{T}$$

$$C = \operatorname{diag}(1, 1, 1, 1, 1, 1)$$
(3.13)

3.4.2 Initial cost function

The cost function had to be tuned and tested. In order to do that, an initial guess had to be made. The cost function could be based on the cost function for the ILS-FCS-MPC. This is given in equation 3.6. In addition, a similar term as the one given in equation 2.57 was added. The resulting initial cost function is given in equation 3.14. The first term ensure accurate reference tracking. The current reference from the APF is given by $y^*(k)$. The second term is associated with switching loss. Penalizing a change in the control variables, from one timestamp to the next. The third term f(u(l)) is the term forcing continuous variables over to binary form. It has zeros at ± 1 for all three phases. The three control variables u_1 , u_2 and u_3 are then forced to either -1 or 1. Control variables u_{123} control current in phase a, b and c respectively. In some parts of this section these descriptions are used simultaneously.

$$J = \sum_{l=k}^{k+N-1} ||\mathbf{y}_{e}(l+1)||_{2}^{2} + q_{control}||\Delta \mathbf{u}(l)||_{2}^{2} + q_{discrete}f(\mathbf{u}(l))$$
(3.14a)

$$y_e(k+1) = y^*(k+1) - y(k)$$
 (3.14b)

$$\Delta \boldsymbol{u}(k) = \boldsymbol{u}(k) - \boldsymbol{u}(k-1) \tag{3.14c}$$

$$f(\boldsymbol{u}(k)) = \left\| \left\{ \sum_{i=1}^{i=3} (u_i(k) - 1)(u_i(k) + 1) \right\} \right\|_2^2$$
(3.14d)

3.4.3 Cost function tuning, optimizing binary control and reference tracking

As mentioned, the cost function in 3.14 had to be tuned. In this tuning process the focus was to achieve binary control variables while maintaining good reference tracking. This is not an easily quantifiable specification. As a result tuning was done largely using graphical information when measuring reference tracking. Binary variables were achieved when all control variables within the control horizon fell within 10% of one of the two binary values. Switching cost was not an important metric at this stage. The variable $q_{control}$ was kept at zero for all testing done in this section. All tuning was done with $q_{states} = 1$. In the tuning process the FCS-MPC was run for one iteration. During which the CCV-FCS-MPC was set to track the reference in figure 3.2. Predicted states and calculated control variables were then plotted and analyzed. Simulations were done with control horizon N = 30, and sampling time $T_s = 20\mu s$.

Changing *qdiscrete*

Initially the only tuning was done by changing $q_{discrete}$. Maintaining the cost function expression from 3.14. Figure 3.5b shows the control variables. The green horizontal lines are situated at ±0.9. These indicate the threshold for the control variables being within 10% of ±1. In this case the control variables do not meet the desired requirements. The variable $q_{discrete}$ was then increased by factors of 10 until the control variables met the desired requirements. At $q_{discrete} = 10^6$ the control variables met the requirements. This procedure was used throughout the cost function optimization. The system then has the response given in figure 3.5c with the controls in figure 3.5d. State tracking is in this case not optimal. Both the α and β state feature unwanted oscillations. With the α phase oscillating the most. This performance motivates a change in the cost function structure, because changing the weights to an acceptable binary value tracking, introduced unwanted oscillations in the states.



Figure 3.5: Control variables and states when simulating with initial cost function guess

Changing cost function expressions

The first key objective when changing the cost function structure had to do with the binary variable term f(u(k)). In figure 3.5b the control variables tend to operate as continuous variables. This is clearest from 0.6 to 0.8 μ seconds for u_a and u_b . The third control variable u_c also show signs of continuous behaviour for the entire control horizon. As discussed above when $q_{discrete}$ is optimized, the states experience unwanted oscillations. An idea was then to change the expression f(u(k)) in equation 3.14. Figure 3.6 visually display the binary cost term for one phase. The graph f_1 display the initial guess for the binary cost term. In order to compensate for the non binary behaviour seen in figure 3.5b this was changed. Full binary behaviour is achieved with a purely square function. Which is infinite at any other points than ± 1 , where it is zero. This would make the optimization problem in-feasible. As a result a compensation had to be made by increasing the power of u. The best results were achieved with $f_2 = ((u^4-1)(u^4-1))^2$ displayed in figure 3.6. Here the binary cost term much closer resemble a desired square wave.

Figure 3.7 display the results when simulating with $f_2 = ((u^4 - 1)(u^4 - 1))^2$ as the binary cost term. Here the continuous behaviour close to ± 1 , as seen in the previous case, is almost mitigated. In 3.7b the states do not experience continuous behaviour to the same extent. However the control variables tend to take values between ± 0.5 . When $q_{discrete}$ is optimized, reference tracking performance is greatly improved over the initial cost function guess, as shown in figure 3.7c. Oscillations in particularly the α -state is reduced. Though the oscillations are reduced, more



Figure 3.6: Normalized cost function binary penalization terms

progress could be made.

When simulating with $f^2 = ((u^4 - 1)(u^4 - 1))^2$ and $q_{discrete} = 1$, control variables often fell between ±1. This can be explained considering the binary cost term, plotted as f_2 in figure 3.6. The term f_2 is almost constant between ±0.5. The solver used by Acado is Qpoases. This is an SQP interior point method for solving non-quadratic optimization. SQP is an iterative algorithm, converging when the step-size goes toward zero. This is discussed further in section 2.1.2. When the cost function almost constant between ±0.5, the Jacobian ∇f and Hessian $\nabla_{xx}^2 \mathscr{L}$ will tend toward zero in this area. The step length of x in equation 2.21 reduces to $A_m p_x = 0$. This means the SQP algorithm will more easily converge between ±0.5 when using $f^2 = ((u^4 - 1)(u^4 - 1))^2$. This was no problem when using f_1 . The third and final binary cost term was then a combination of the two. The expression $u^2 - 1$ was added to the term to be squared. This expression is the square root of the initial cost term f_1 . Resulting in the cost function term $f_3 = ((u^4 - 1)(u^4 - 1) + u^2 - 1)^2$. A term maintaining the binary behaviour of f_2 , while mitigating the constant region between ±0.5 of f^1 . This is displayed divided by 4 in 3.6. Here it is shown that f_3 feature the hard binary penalization close to ±1 of f_2 , without the close to constant area.

Figure 3.7 display the results when simulating with $f_3 = ((u^4 - 1)(u^4 - 1) + u^2 - 1)^2$ as the binary cost term. Here the control variables do not tend to fall between ±0.5 as in the previous case. In 3.8b the states are much closer to acceptable binary behaviour. As a result the reference tracking is greatly improved when simulating with optimized $q_{discrete}$. In 3.8c the oscillations seen in both 3.5c and 3.7c are almost gone. However performance can still be improved. At this stage the binary cost term is considered optimal enough. The focus is then shifted to the reference tracking term $\mathbf{y}_e(k+1) = \mathbf{y}^*(k+1) - \mathbf{y}(k)$.

The focus considering the reference tracking term was to increase the power of the error. The reasoning behind this was to make the control variables shift more frequently to improve reference tracking. In figure 3.8d only the control variable u_a is switching. Increasing the power of the error term would penalize state deviations harder, as the current reference is between ±100, and not ±1. This would in turn encourage the FCS-MPC to switch more, in order to



Figure 3.7: Control variables and states when simulating with binary cost term changed to $f_2 = ((u^4 - 1)(u^4 - 1))^2$



Figure 3.8: Control variables and states when simulating with binary cost term changed to $f_3 = ((u^4 - 1)(u^4 - 1) + u^2 - 1)^2$



Figure 3.9: Control variables and states when increasing switching cost

achieve this. Optimal performance was found when changing the state deviation cost term to $y_e(k+1) = (y^*(k+1) - y(k))^3$. Results from this is shown in figure 3.9

Here the reference tracking when using optimal $q_{discrete}$ is almost perfect. As seen in figure 3.9c, where the oscillations from previous simulations are mitigated to an acceptable degree. As assumed above this is achieved by more frequent switching, both by u_a and u_b . Which is shown in figure 3.9d. This performance is considered good enough. And the design of the FCS-MPC is done. The resulting cost function then became.

$$J = \sum_{l=k}^{k+N-1} ||\mathbf{y}_{e}(l+1)||_{2}^{2} + q_{control}||\Delta \mathbf{u}(l)||_{2}^{2} + q_{discrete}f(\mathbf{u}(l))$$
(3.15a)

$$\mathbf{y}_{e}(k+1) = (\mathbf{y}^{*}(k+1) - \mathbf{y}(k))^{3}$$
 (3.15b)

$$\Delta \boldsymbol{u}(k) = \boldsymbol{u}(k) - \boldsymbol{u}(k-1) \tag{3.15c}$$

$$f(\boldsymbol{u}(k)) = \left\| \left\{ \sum_{i=1}^{i=3} (u_i(k)^4 - 1)(u_i(k)^4 + 1) + u_i(k)^2 - 1 \right\} \right\|_2^2$$
(3.15d)



Figure 3.10: Control variables and states when simulating with binary cost term and state deviation term optimized

Cost function tuning, investigating switching cost

With reference tracking and binary switching at an acceptable level, switching cost was investigated. At this testing stage the main focus was in investigating how penalizing switching cost effected performance. Both regarding reference tracking, and performance of binary variables. Tuning was done by changing $q_{control}$. Leaving the switching cost expression from 3.14. The point of this analysis was to see what values of $q_{control}$ maintained acceptable performance. This was done in order to know what $q_{control}$ values to test the CCV-FCS-MPC implementation with in the cascaded MPC structure. Simulations were done with control horizon N = 30, and with $T_s = 20\mu s$. Optimal binary tracking was used, with $q_{discrete} = 10^7$ as found previously.

Many different values were tested, and $q_control$ could be increased to 10^7 . At this point the control variables started behaving continuously. This behaviour can be seen in figure 3.10b. Here the control variables also switch less frequently than in 3.9d. When simulating with $q_control = 10^4$ the control variables behave as binary control variables. This behaviour is shown in figure 3.10d. Switching was also more frequent than for $q_{control} = 10^7$, and less frequent than for $q_{control} = 0$. Which is as expected. In both the studied cases reference tracking is good as seen in 3.10a and 3.10c.

3.4.4 Continuous control variables to binary

Continuous control variables can not be used for controlling gate switches. Control variables from the CCV-FCS-MPC were mapped to binary values. Each control variable value were passed through the function

$$u_{new} = \lfloor \frac{1}{2} (u_{old} + 1) \rceil \tag{3.16}$$

Gates were controlled by u_{new} .

3.4.5 Finding optimal *q*_{discrete} values

The CCV-FCS-MPC was simulated with three different sampling times in the cascaded MPC structure, 10,20and40 μs . For each sampling time a different optimal $q_{discrete}$ had to be found. These were found as mentioned above. The CCV-FCS-MPC was simulated for one iteration with N = 30. The control variable $q_{discrete}$ was increasingly multiplied by factors of 10, until the control variables were between 10% of the desired values. For $T_s = 10\mu s$ this was found at $q_{discrete} = 10^7$, $T_s = 20\mu s \Rightarrow q_{discrete} = 10^8$ and $T_s = 40\mu s \Rightarrow q_{discrete} = 10^{11}$

3.5 ICS-MPC

One method when controlling gate switches in power electronics is to use an ICS-MPC to generate a voltage reference and using PWM to generate binary switching signals. This was done using a simplified version of the MPC from section 3.4.

3.5.1 MPC formulation

The discrete model from equation 3.5 was used in the ICS-MPC. Meaning the overall MPC formulation is the same as for the CCV-FCS-MPC. This is reformulated in 3.17. $\min_{\boldsymbol{U}_k} \quad J(\boldsymbol{Y}_k, \boldsymbol{X}_k, \boldsymbol{U}_k)$

subject to

$$x_{k+1} - Ax_k - Bu_k - Tv_{g,k} = 0$$

$$y_{k+1} - Cx_{k+1} = 0$$

$$x_{k+2} - A^2x_k - ABu_k - Tv_{g,k+1} = 0$$

$$y_{k+2} - CAx_{k+1} - CBu_k = 0$$
(3.17)
:

$$\begin{aligned} \boldsymbol{x}_{k+N} &- \boldsymbol{A}^{N} \boldsymbol{x}(k) - \boldsymbol{T} \boldsymbol{v}_{g,k+N-1} - \sum_{l=0}^{N-1} \boldsymbol{A}^{N-1-l} \boldsymbol{B} \boldsymbol{u}(k+l) = 0 \\ \boldsymbol{y}_{k+N} &- \boldsymbol{C} \boldsymbol{A}^{N} \boldsymbol{x}(k) - \sum_{l=0}^{N-1} \boldsymbol{C} \boldsymbol{A}^{N-1-l} \boldsymbol{B} \boldsymbol{u}(k+l) = 0 \\ |\boldsymbol{u}_{i,j}| &\leq 1 \quad \forall i \in \{k, k+1, ..., k+N-1\}, \quad \forall j \in \{1, 2, 3\} \end{aligned}$$

Where

$$Y(k) = [\mathbf{y}^{T}(k+1) \cdots \mathbf{y}^{T}(k+N)]^{T}$$

$$X(k) = [\mathbf{x}^{T}(k+1) \cdots \mathbf{x}^{T}(k+N)]^{T}$$

$$U(k) = [\mathbf{u}^{T}(k) \cdots \mathbf{u}^{T}(k+N-1)]^{T}$$

$$C = \operatorname{diag}(1, 1, 1, 1, 1, 1)$$
(3.18)

3.5.2 cost function

The cost function for the ICS-MPC was based on the cost function for the ILS-FCS-MPC formulation in 2.34. Where the first term penalizes deviation from the current reference. While the second term penalizes switching cost. As the output of the ICS-MPC is a continuous voltage reference, the second term is unnecessary. Leaving the following cost function.

$$J = \sum_{l=k}^{k+N-1} ||\boldsymbol{y}_{e}(l+1)||_{2}^{2}$$
(3.19)

3.5.3 PWM

In an ICS-MPC switching cost is controlled by the PWM switching frequency. As discussed in section 2.1.1, ICS-MPC involves continuous control variables. Meanwhile control inputs to gate

switches in power electronics are binary variables. PWM then had to be used to go from voltage references to gate switching signals. This method is outlined in 2.8.

3.6 Cascaded MPC implementation

All MPC implementations were now designed and implemented. The most important study of this thesis could then be conducted. Simulating the gate controlling MPC together with the harmonic mitigation MPC on the model of a ship power system. This section will present the overall implementation. How both MPC's were related to each other and the ship power model. How both the current reference and internal states of the Harmonic MPC were transferred. Then how different step-lengths were handled. Finally presenting some of the simplifications made during the study.

3.6.1 Control structure

This topic has already been mentioned throughout this thesis, so this presentation will be brief. Figure 3.11 displays the overall structure. The Harmonic Mitigation MPC ran with intervals of $T_{s,HMPC} = 0.01s$ with a prediction horizon of N = 220 samples and $12.5\mu s$. 220 samples over $12.5\mu s$ means a sampling period of $56.8181\mu s$. One of the parameters for testing the gate controlling MPC was sampling period. These periods ranged from $10\mu s$ to $50\mu s$. Meaning both $I_{af,ref}$ and $V_{bus2,pred}$ had to be upsampled. Upsampling is done by assuming linear behavior og the original signal between two sampling points. Figure 3.12 shows the result of this process applied to an input signal with sampling time of $56.8181\mu s$. The signal is upsampled to $T_s = 10\mu s$.

In all simulations the gate Control MPC was run on every sample. In order for the gate control MPC to have a sufficient current reference there was a limit to the control horizon and sampling time. The harmonic mitigating MPC ran every 0.01s producing a reference of 0.0125s. This left a maximum control horizon in time of 0.0025s or 2.5ms for the gate controlling MPC. Any longer control horizon in time meant the predicted current reference would be too short. A control horizon in time is defined as $N \cdot T_s$ for the gate controlling MPC. With a minimum sampling time of $T_s = 10\mu s$, this left a maximum control horizon of N = 250. The maximum sampling time of $T_s = 40\mu s$ gave the minimum control horizon of N = 62 samples.



Figure 3.11: Flow chart of cascaded MPC structure



Figure 3.12: Upsampling the signal $sin(13 \cdot 50 \cdot 2\pi t)$

3.6.2 Injecting estimated bus voltage

The generator voltage from the test setup in figure 3.3 is now changed for the voltage v_2 in figure 2.8. This voltage is an internal state in the harmonic mitigating MPC. These are written as the states v_{s1} and v_{s2} in equation 2.63. Internal states in an MPC are estimated ahead in time. They could then were used as bus voltage estimates in the gate controlling MPCs. The gate controlling MPCs ran with a lower sampling time than the harmonic mitigating MPC. Voltage levels on bus 2 were then measured and used as initial voltage values for each iteration of the gate controlling MPCs.

3.6.3 Ship power model

The ship power system from figure 2.8 was used for all simulations. With model parameters from table 2.1 and most parameters from 2.2. Motors 1 and 2 were set to pull 0.45[pu] of power. One significant simplification was made. Constant DC voltage was assumed. In the original simulations done in [6] DC voltage was controlled with a PI controller.

3.6.4 Base harmonics compensation

The cascaded MPC implementation resulted in some delays. From measurements to the output of the first MPC, and from input to output on the second MPC. This resulted in a base harmonic component in the active filter current for all MPC implementations. This was mitigated by adding the same component to the reference phase shifted 180 degrees. The result of this is shown in figure 3.13. Notice that the base harmonic component is not fully mitigated. However this was deemed sufficient. This was used for all MPC implementations. Not only the CCV-FCS-MPC.

3.7 Test of complete setup

The complete control structure was now tested. In this testing procedure the complete circuit in 2.8 was simulated for 0.2 seconds. The gate controlling implementations were turned on after 0.1 seconds. In order to allow the bus voltages and generator currents to settle. Performance was measured by the performance of reference tracking, by the total overall switching cost and by total harmonic distortion on generator currents and bus voltages.



Figure 3.13: Tracking a zero current reference with the CCV-FCS-MPC with $T_s = 20 \mu s$ and N = 15

3.7.1 Performance measurement

Below will be a presentation on how the relevant performance characteristics were measured. In addition to why each of them is important.

reference tracking

The overall objective of the cascaded MPC structure is harmonic mitigation. The harmonic mitigation MPC is assumed well implemented. Meaning that the current reference it gives out is the best for harmonic mitigation. The best thing the gate switching MPC can do is then to follow this reference. One simple way of quantifying this is the sum of square errors which is given as

$$E_{ssq} = \sum_{k=\frac{0.1}{2dt_{sim}}}^{\frac{T_{sim}}{dt_{sim}}} (I_{af,ref} - I_{af})^2 \cdot dt_{sim}$$
(3.20)

 E_{ssq} is calculated from when the gate controlling implementation is turned on until the end of the simulation. In addition to sum of squares error reference tracking is analyzed visually. Which is done by plotting the current vs the reference.

switching cost

Harmonic mitigation is done using gate switches. As stated in 2.6.1 each time a gate switch is toggled, power is lost. Switching cost can then quantified by counting the number of toggles done on all switches from 0.1*s* to 0.2*s*. The true switching cost of one toggle is defined as the

integral of current and voltage over the switching period. Over time the overall switching cost will be almost proportional to the number of toggles. The proportionality rate is not discussed in this thesis.

THD

THD is the overall performance measurement in [6, p- 131, line- 4]. As staded in 2.6.2, THD is an effective and simple measurement of the influence of harmonic components on a distorted waveform. THD is quantified by

$$THD_i = \frac{\sqrt{\sum_{h=2}^{\infty} (I^{(h)})^2}}{I^{(1)}}$$
(3.21)

This is calculated continously by the already implemented THD block in simulink. The THD investigated in all simulation cases is the one found at t = 0.2. At the end of all simulations.

3.7.2 Test cases

The performance of the cascaded MPC structure was now measured. Performance criteria was reference tracking, switching cost and THD. The CCV-FCS-MPC was tested the most. With sampling times T_s at $10\mu s$, $20\mu s$ and $40\mu s$. When deciding the control horizons LCL oscillations were concidered. As stated in 2.9 LCL circuits have an oscillating frequency. Inserting the parameter values from table 2.2 into equation 2.61 gives a resonance frequency of $f_r = 2372Hz$. Indicating a resonance period of $T_r = 421.5\mu s$. This would indicate that a control horizon of N = 43 is needed for $T_s = 10\mu s$. Since $T_s N = 10\mu s \cdot 43 = 430\mu s \ge 421.5\mu s = T_r$. However this does not concider the resistances of the LCL filter. The FCS with continous variables was simulated for one iteration, with initial capacitor voltage at zero. When the initial capacitor is not equal to the steady state voltages, the currents in the system experiences oscillations before settling. Simulating with $T_s = 10\mu s$ and N = 30 yields the results in figure 3.14. Here the entire period of the LCL oscillation is contained within 30 samples. Meaning a control horizon in time of $N \cdot T_s = 300\mu s$ is sufficient.

Test cases then became as sat up in table 3.1. For the MPC implementations the lower control horizon bound was $N \cdot T_s \ge 300 \mu s$. The CCV-FCS-MPC saw the greatest variety in test cases. The lowest sampling time was $T_s = 10$. Where N = 30 was needed to meet the required control horizon. Due to computational costs, N was not increased further. For $T_s = 20$ the lowest possible control horizon was N = 15. Here the simulation duration was not an issue, meaning



Figure 3.14: Oscillations in the β phase when simulating with capacitor voltage initialized at zero

N = 30 was possible. For $T_s = 40$ the lowest possible control horizon is 8 samples. Here though control horizons of 10 and 35 samples were simulated. Both the ILS-FCS-MPC and ICS-MPC were benchmarks to the CCV-FCS-MPC. Both were then tested with N = 30 and $T_s = 20$. The ICS-MPC was ran with PWM switching frequencies of 5kHz and 20kHz. This was in order to get the low end and high end of the performance spectrum in terms of reference tracking. For the CCV-FCS-MPC four values of $q_{control}$ were tested.

		FCS-MPC Continous							ILS-FCS-I	MPC	ICS-	MPC	Hysteresis
$T_s[\mu s]$	10	20			40		20		20		-		
Ν	30	15			30		10	35	30			30	-
f_{sw} or q_c	0	0	0	10 ²	10^{6}	10^{8}	0	0	-		5kHz	25kHz	-

Table 3.1: Test cases for cascaded MPC implementations

Chapter 4

Results

This chapter will display the results from the simulation cases in table 3.1. All results are taken from simulating with the cascaded MPC implementation on the complete ship power system model. No results are displayed from simulations on the test circuit, or single MPC iterations. Results are displayed in two sections. The first focuses on the isolated performance of the MPC implementations. It contains plots of active filter currents versus references. As well as tables quantifying SSE and toggles. The second part focuses on cascaded MPC performance. With tables quantifying THD in the ship power system. THD were measured on i_{G1} , i_{G2} , v_1 and v_2 in figure 4.1. The damping resistor R_D is only present when simulating the hysteresis controller. All gate controller MPCs were implemented as described in figure 4.2. It was quickly established that the CCV-FCS-MPC performed the best. All results then show what performance improvements comes from using CCV-FCS-MPC instead of the two other MPCs and the hysteresis controller. This compares the experimental CCV-FCS-MPC to the other established implementations. These are referenced as benchmarks for the rest of the thesis.



Figure 4.1: Simplified implementable model of the ship power system from [6, p-104]



Figure 4.2: Flow chart of cascaded MPC structure

4.1 Performance of the gate controlling implementations

Results in this section contain current tracking data and toggle data of all implementations. First a presentation of active filter currents versus references for all implementations in 3.1. Graphically showing the quality of reference tracking for all implementations. Reference tracking is then quantified in two ways. The first is a plot of SSE for all implementations. The second are tables quantifying SSE of the CCV-FCS-MPC relative to benchmarks. Data showing switch toggles is first displayed graphically in a plot. Then by tables quantifying performance of CCV-FCS-MPC relative to the bechmarks.

4.1.1 Graphical presentation of current tracking capability

Figure 4.4 shows how all implementations perform regarding reference tracking. From figure 4.3 it can be seen that the hysteresis controller has the worst performance. Here the active filter currents overshoot the reference both at negative and positive edge, and at low and high amplitudes. The hysteresis controller is tracking the reference with the current directly at the gate controllers. In figure 4.1 this is listed as the gate current I_{C2} . The active filter current will then not follow the reference. The ICS-MPC and ILS-FCS-MPC perform similarly. Both implementations perform good at high amplitudes, but struggle at lower.



Figure 4.3: Reference tracking of the Hysteresis controller

The active filter currents are quite similar in form for all three implementations as well as is seen in 4.4a, 4.4b and 4.4c. Indicating that ICS-MPC performance is independent of switching frequency. For the CCV-FCS-MPC performance is visually best with $T_s = 10\mu s$ in figure 4.4d and with $T_s = 20\mu s$ in figures 4.4e and 4.4f. These perform almost identical, with some higher frequencies when $T_s = 20\mu s$. When N = 30 and T_s is maintained at $20\mu s$, reference tracking is almost the same. Increasing T_s to $40\mu s$ has a significant effect on performance. This is shown in 4.4g and 4.4h. Introducing deviations both when the reference has high and low amplitude. Performance is also visually better with N = 10 as opposed to N = 35. When investigating the effect of changing $q_{control}$, results are similar. Figures 4.4f, 4.4i and 4.4j are almost identical. Indicating similar performance for $q_{control} = 0$, $q_{control} = 10^2$ and $q_{control} = 10^4$. In figure 4.4k some oscillations are introduced.

4.1.2 SSE for all implementations

Table 4.5 shows SSE data for all implementations. The CCV-FCS-MPC outperform all benchmarks, except when $T_s = 40 \mu s$. Lowest SSE is achieved with $T_s = 10$ and N = 30, and $T_s = 20$ and N = 15. Both having a control horizon in time of $300 \mu s$. Results are better for smaller values of N, when T_s is constant. This can be seen for $T_s = 20$, where SSE is smaller for N = 15 than for N = 30. It is also shown when $T_s = 40$, where SSE is smaller for N = 10 than for N = 35. For all



Figure 4.4: Current tracking in phase A for all implementations, from 0.18s to 0.2s.



Figure 4.5: SSE of all implementations, $q_{control}$ is abbreviated to qc for readability. For cases where qc is not listed, it is zero.

CCV-FCS-MPC implementations, SSE is lowest for phase a. For increasing values of $q_{control}$ SSE increases only significantly when $q_{control} = 10^8$.

4.1.3 Current tracking of CCV-FCS-MPC versus hysteresis controller

Table 4.1 displays the performance of all CCV-FCS-MPC implementations relative to using a hysteresis controller. A value of 0.5 in the SSEa row, means that implementation halves SSE for phase a. It is clear that all CCV-FCS-MPC configurations outperforms the hysteresis controller. Reduction in SSE is above 80% in the two best cases. When $T_s = 10$ and N = 30, and $T_s = 20$ and N = 15. When $T_s = 40 \mu s$ and N = 35 the reduction is around 3% averaged for all phases. Which is the worst performance of the CCV-FCS-MPC

Table 4.1: Proportional sum of square error for the CCV-FCS-MPC relative to the hysteresis controller

		CCV-FCS-MPC									
$T_s[\mu s]$	10			20		40		-			
N	30	15		3	0		10	35	-		
f_{sw} or q_c	0	0	0	10 ²	10^{4}	10^{8}	0	0	-		
SSEa	0,18	0,16	0,18	0,20	0,19	0,21	0,77	0,95	1,00		
SSEb	0,20	0,20	0,24	0,26	0,25	0,25	0,87	0,93	1,00		
SSEc	0,21	0,19	0,25	0,25	0,26	0,29	0,91	1,02	1,00		

4.1.4 Current tracking of CCV-FCS-MPC versus ICS-MPC

Table 4.2 compare the CCV-FCS-MPC and ICS-MPC. The ICS-MPC with $f_s w = 25kHz$ is not included. As seen in 4.5 SSE is similar both for $f_s w = 5kHz$ and $f_s w = 25kHz$. Only results for $T_s = 20$ and N = 30 are included. In order to compare implementations when simulated with the same control horizon and sampling time. Results show that the CCV-FCS-MPC reduces SSE by 50-55%. Depending on the value of $q_{control}$.

Table 4.2: Proportional sum of square error for the CCV-FCS-MPC relative to ICS-MPC with $f_{sw} = 5kHz$

	(CCV-FC	С	ICS-MPC	
$T_s[\mu s]$		2	20		
Ν		3	30		
f_{sw} or q_c	0	10 ²	10^{4}	10 ⁸	5kHz
SSEa	0,35	0,39	0,36	0,40	1,00
SSEb	0,46	0,50	0,49	0,49	1,00
SSEc	0,46	0,47	0,47	0,53	1,00

4.1.5 Current tracking of CCV-FCS-MPC versus ILS-FCS-MPC

Results in table 4.3 show that the CCV-FCS-MPC reduces SSE by 55-60% compared to the ILS-FCS-MPC. With equal control parameters $T_s = 20$ and N = 30.

Table 4.3: Proportional sum of square error for the CCV-FCS-MPC relative to ILS-FCS-MPC

	(CCV-FCS-MPC							
$T_s[\mu s]$		20							
Ν		30							
q_c	0	10 ²	10^{4}	10^{8}	-				
SSEa	0,28	0,31	0,29	0,32	1,00				
SSEb	0,40	0,44	0,42	0,42	1,00				
SSEc	0,41	0,42	0,43	0,48	1,00				

4.1.6 Number of toggles for all implementations

Number of toggles for each simulation case is displayed in 4.6. The CCV-FCS-MPC is performes best, except when $T_s = 10$. Best results are achieved with $T_s = 40$. The Hysteresis controller, ILS-FCS-MPC and ICS-MPC switching at 5kHz performs almost the same. While the ICS-MPC



Figure 4.6: Number of toggles of the gate switches for all implementations

switching at 25kHz is the worst. Switching over 4 times as often as the best option. Performance is visually equal for all other values of $q_{control}$, other than 10^8 . Increasing $q_{control}$ has less effect than increasing T_s .

4.1.7 Number of toggles of CCV-FCS-MPC compared to hysteresis controller

Table 4.4 compare the CCV-FCS-MPC. Comparison is done for number of toggles of the gate switches. CCV-FCS-MPC with $T_s = 10$ increases toggles by 11%. All other implementations decrease toggles. Best results is achieved by having $T_s = 40 \mu s$. Where toggles are decreased by 61% and 62%.

Table 4.4: Proportional number of switch toggles for the CCV-FCS-MPC relative to the hysteresis controller

		CCV-FCS-MPC								
$T_s[\mu s]$	10		20					0	-	
N	30	15		30				35	-	
f_{sw} or q_c	0	0	$0 10^2 10^4 10^8$				0	0	-	
Switchings	1,11	0,69	0,70 0,69 0,69 0,57				0,38	0,39	1,00	

4.1.8 Number of toggles of CCV-FCS-MPC compared to ICS-MPC

In table 4.5 toggles are compared between CCV-FCS-MPC and ICS-MPC with $f_s w = 5kHz$. Results are only showed for equal values for T_s and N. The CCV-FCS-MPC decrease toggles by between 22% for $q_{control} = 0$, and 36% for $q_{control} = 10^8$

Table 4.5:	Proportional	number o	f switch	toggles	for the	e CCV-F	CS-MPC	relative to	o ICS-I	MPC
with f_{sw} =	= 5kHz									

	(CCV-FC	3	ICS-MPC	
$T_s[\mu s]$		2	20		
Ν		3	30		
f_{sw} or q_c	0	10 ²	10^{4}	10 ⁸	5kHz
Switchings	0,78	1,00			

4.1.9 Number of toggles of CCV-FCS-MPC compared to ILS-FCS-MPC

Reduction in toggles by using CCV-FCS-MPC compared to ILS-FCS-MPC is listed in table 4.6. Toggles are reduced 7%, 8%, 9% and 24% with increasing values of $q_{control}$.

Table 4.6: Proportional number of switch toggles for the CCV-FCS-MPC relative to ILS-FCS-MPC

	(CCV-FCS-MPC							
$T_s[\mu s]$		20							
N		30							
q_c	0	10 ²	10^{4}	10^{8}	-				
Switchings	0,93	0,92	0,91	0,76	1,00				

4.2 Performance in a cascaded MPC structure

This chapter contains THD results from the cascaded MPC structure. All cases in table tab 3.1 were used to control gate switches. First THD for both generator currents and bus voltages are presented for all test cases. Then tables comparing performance of the CCV-FCS-MPC to all other gate switch controllers are included.

4.2.1 Microgrid THD values for all test cases

THD values in the microgrid is presented in figure 4.7. The bus voltages has almost the same THD for CCV-FCS-MPC with $T_s \leq 20\mu s$, ICS-MPC and ILS-FCS-MPC. Within these results the worst results are found with $q_{control} = 10^8$. The best results are found for $T_s = 10$. The CCV-FCS-MPC with $T_s \geq 20\mu s$ increases bus voltage THD around 50 % compared to when $T_s \geq 20\mu s$. The hysteresis controller generates the highest bus voltage THD values.

For THD on the generator currents the continuous FCS-MPC with $T_s \le 20\mu s$ performs the best. Followed by continuous FCS-MPC with $T_s \ge 20\mu s$, the ILS-FCS-MPC and the ICS-MPC all performing similarly. The hysteresis controller generate the highest generator current THD. All implementations results in lower THD on the voltage on bus 1 than on bus 2, and on currents from generator 1 than generator 2.



Figure 4.7: THD results from all simulation cases in the cascaded MPC structure

4.2.2 Microgrid THD values of CCV-FCS-MPC versus hysteresis controller

Table 4.7 compares the CCV-FCS-MPC controller to the hysteresis controller. The CCV-FCS-MPC reduces THD on all measurements. THD reduction is greatest on the generator currents than the bus voltages for all CCV-FCS-MPC implementations. Results indicate that larger N values reduce bus voltage THD. While generator current THD values are increased. This can be seen both when $T_s = 20\mu s$ and when $T_s = 40\mu s$.

		CCV-FCS-MPC									
$T_s[\mu s]$	10			20		40		-			
N	30	15	30					35	-		
f_{sw} or q_c	0	0	0	10 ²	10^{4}	10^{8}	0	0	-		
THD V _{bus1}	0,40	0,44	0,43	0,44	0,43	0,53	0,71	0,65	1,00		
THD V _{bus2}	0,32	0,36	0,36	0,37	0,36	0,46	0,63	0,58	1,00		
THD Igen1	0,38	0,41	0,42	0,44	0,42	0,46	0,58	0,63	1,00		
THD Igen2	0,30	0,30	0,34	0,36	0,33	0,36	0,44	0,46	1,00		

Table 4.7: Proportional THD for the CCV-FCS-MPC relative to hysteresis controller

4.2.3 Microgrid THD values of CCV-FCS-MPC versus ICS-MPC

Differences in cascaded MPC implementations using CCV-FCS-MPC versus ICS-MPC is quantified in table 4.8. The ICS-MPC is implemented with $f_{sw} = 5kHz$. Results show that for equal T_s and *N* values the CCV-FCS-MPC will increase bus voltage THD. With $q_{control} = 10^8$ this increase is at 27% for both buses. For lower $q_{control}$ values, the increase ranges from 1% to 4% averaged for both buses. For all values of $q_{control}$ generator current THD is decreased. Ranging from 20% for $q_{control} = 10^8$, to 25% for $q_{control} = 10^8$ averaged for both buses. In all cases bus voltage THD is decreased most on bus 2. While generator current THD is decreased most for generator 1.

	(CCV-FC	3	ICS-MPC	
$T_s[\mu s]$		2	20		
N		3	30		
f_{sw} or q_c	0	10 ²	10^{4}	10^{8}	5kHz
THD V _{bus1}	1,03	1,05	1,03	1,27	1,00
THD V_{bus2}	0,98	1,03	1,00	1,27	1,00
THD Igen1	0,72	0,75	0,72	0,78	1,00
THD Igen2	0,78	0,82	0,77	0,83	1,00

Table 4.8: Proportional THD for the CCV-FCS-MPC relative to ICS-MPC with $f_{sw} = 5kHz$

4.2.4 Microgrid THD values of CCV-FCS-MPC versus ILS-FCS-MPC

Table 4.9 compares the CCV-FCS-MPC and ILS-FCS-MPC implementations, with respect to THD values in the micro-grid. The CCV-FCS-MPC decreases bus voltage THD for bus 1, exept when $q_{control} = 10^8$. THD on bus 2 voltages are increased between 2% and 26% in all cases. THD on both generator currents are reduced. The reduction is the same for both generators in all test cases.

		CCV-FCS-MPC								
$T_s[\mu s]$		20								
Ν		30								
q_c	0	10 ²	10^{4}	10 ⁸	-					
THD V _{bus1}	1,02	1,04	1,03	1,26	1,00					
THD V_{bus2}	0,95	0,99	0,96	1,22	1,00					
THD Igen1	0,76	0,79	0,76	0,82	1,00					
THD Igen2	0,77	0,81	0,76	0,82	1,00					

Table 4.9: Proportional THD for the CCV-FCS-MPC relative to ILS-FCS-MPC

Chapter 5

Discussion

This section highlights the most significant results. This is done in the order the results are presented. In addition to presenting some important correlations and anomalies. Discussing possible causes for these, and their significance. Finally THD and SSE results are combined with switching cost results to form an Overall Performance Score(OPC) for all implementations.

5.1 Performance of the CCV-FCS-MPC

In chapter 4.1 results on current tracking ability and power loss is presented individually. In this section they are discussed together to find correlations and compare performance. In order to better establish the best performing implementation.

5.1.1 current tracking capability in all cases

Results indicate that for the CCV-FCS-MPC bigger N values implies poorer reference tracking. Both when looking at plots of the APF currents in section 4.1.1, and for SSE values in section 4.1.2. This is unexpected for an MPC implementation. One possible causes for this are inaccuracies in the model. Model inaccuracies could cause the state predictions to drift within the control horizon. Resulting in non optimal control variables. This is however unlikely as the model is an exact ideal representation of the LCL circuit. However there could be inaccuracies in the bus voltage fed from the original MPC. If this is an inaccurate prediction, estimates could drift with longer control horizons. Both of states and control variables. A decreased sampling time T_s improves reference tracking. This is shown by the current plots in 4.4 and the SSE values in 4.5. From these results it can also be concluded that $T_s = 20\mu s$ is sufficient. $T_s = 20\mu s$ does improve SSE, however toggles are almost doubled. Halving the sampling time also more than doubles the computational cost. SSE and graphical results indicate that increasing $q_{control}$ reduced current tracking performance. However this was only noticeable in one of the simulation cases. In order to understand the effect $q_{control}$ fully, a further study is needed. The SSE values for the CCV-FCS-MPC in figure are all lower for phase a. One possible cause is delays. Current and voltage measurements are transformed to $\alpha\beta$ -frame and then sent to the MPC. Delays could lead to greater distortions in the β -frame than the α -frame. Since the a and α -frame is the same.

5.1.2 Number of toggles in all cases

Results from figure 4.6 show that sampling time has more effect on the number of toggles, than $q_{control}$. This indicates that $q_{control}$ should have been investigated further. If it had been, this thesis would present deeper knowledge on the CCV-FCS-MPC. Changing the switching cost expression could also have been done. For the same reason. The same results show that $T_s = 20\mu s$ significantly reduces toggles compared to $T_s = 10\mu s$. Further cementing what is stated above that using $T_s = 10\mu s$ is unnecessary.

5.1.3 Current tracking versus hysteresis controller

Results in sections 4.1.3 and 4.1.7 show that the CCV-FCS-MPC is better than the hysteresis controller. Better with respect to both reference tracking and toggles in all cases. At maximal reduction of SSE the number of toggles were reduced. And at maximal reduction of toggles SSE was reduced. This means that depending on the objective, weather it is switching loss in the gate switches, or reference tracking, the CCV-FCS-MPC can significantly improve performance.

5.1.4 Current tracking versus ICS-MPC

In section 4.1.4 and 4.1.8 it is shown that the CCV-FCS-MPC outperform the ICS-MPC. The voltage reference sent from the ICS-MPC would imply perfect reference tracking. This can be stated since the reference is perfectly tracked for the CCV-FCS-MPC with $q_{discrete} = 1$. Independent of the cost function expression. As shown in figures 3.5a. The ICS-MPC is the CCV-FCS-MPC with $q_{discrete} = 0$. Meaning there are significant errors in the PWM which generates the gate switch

signals. The CCV-FCS-MPC toggles between 22% and 36% less, while having between 47% and 65% less SSE.

Results also show about 10% more reduction for the CCV-FCS-MPC in phase a, than phase b and c. This could indicate that errors in the alpha beta conversion effect the CCV-FCS-MPC more than the ICS-MPC. As explained above these errors could be the effect of delays in the cascaded MPC structure. Meaning that mitigating these delays are more important for the CCV-FCS-MPC based on these results. However some other factor than delays could be responsible for the different behaviour of SSE in the three phases.

5.1.5 Current tracking versus ILS-FCS-MPC

The CCV-FCS-MPC outperforms the FCS-MPC implemented with the integer least square method. Shown by the results in sections 4.1.4 and 4.1.8. These improvements are most likely due to the differences in cost function. Nothing can be said about the CCV-FCS-MPC using continuous control variables. It would have been interesting to see what effect that has on performance.

5.2 Performance of the CCV-FCS-MPC in cascaded MPC structures

This section discusses cascaded MPC performance. In addition to THD results, switching cost results are also considered. Making it easier to establish the overall best implementation to use for gate switch control in a cascaded MPC structure.

5.2.1 THD in all cases

The CCV-FCS-MPC has greater effects on generator currents than other implementations. As stated in section 4.2.1. This is expected, since the overall objective of the APF is to minimize harmonics in the generator currents. Since the CCV-FCS-MPC is better at tracking the given reference, THD for generator currents are expected to be lower for the CCV-FCS-MPC. SSE and generator currents are however not correlated. For instance did the CCV-FCS-MPC with $T_s = 10 \mu s$ reduce SSE by over 80% compared to the hysteresis controller. As seen in table 4.1. While the same reduction in generator current THD was 64% averaged over the two buses. As seen in table 4.7. The CCV-FCS-MPC implementation with $T_s = 40 \mu s$ and N = 10 reduced SSE by

15% compared to the hysteresis controller averaged over all 3 phases. As seen in table 4.1. For generator THD the averaged THD reduction is 49%. As seen in tables 4.7. All CCV-FCS-MPC implementations perform more evenly regarding generator THD than SSE.

There seems to be a correlation between the number of toggles and bus voltage THD. In figure 4.7 bus voltage THD is highest for $q_{control} = 10^8$ when N = 30 and $T_s = 20\mu s$. The other three cases with different $q_{control}$ values, have equal and lower bus voltage THD. For number of toggles in table 4.6 all other $q_{control}$ values than $q_{control} = 10^8$ toggles the same amount. The implementation with $q_{control} = 10^8$ toggles fewer times. The same can be said when comparing $T_s = 10\mu s$ to $T_s = 20\mu s$ and N = 15. This indicates that if low bus voltage THD is essential, choose an implementation that switches more often. This could be one reason to choose $T_s = 10\mu s$ instead of $T_s = 20\mu s$ and N = 15.

5.2.2 THD versus hysteresis controller

As mentioned above SSE and generator current THD is not correlated. Reduction in THD is much more even for all implementations, espessially on the generator currents. Meaning the $T_s = 40 \mu s$ implementation is more useful in the cascaded MPC structure. If lower switching and computational cost is desired. Performance is best with lower sampling time, but the difference is smaller than for reference tracking.

5.2.3 THD versus other MPC controllers

Compared to both the ILS-FCS-MPC and ICS-MPC the CCV-FCS-MPC reduces generator current THD between 23% and 18%. While maintaining bus voltage THD, except when $q_{control} = 10^8$. These results are achieved with fewer toggles.

5.3 All performances relative to toggles

This section contanis an analysis comparing overall SSE and THD performance against switching cost. This will quantify what implementation has the overall best performance. These results are not accurate. This is because while toggles are a good indicator of switching cost, it is not accurate. Results are again presented for the relative performances from using CCV-FCS-MPC instead of using benchmarks. The reduction in THD and SSE is multiplied by the reduction in toggles. The result is an overall performance score (OPC). SSE results are averaged over all 3
phases, then multiplied with number of toggles. THD scores are averaged over the two busses or generators, then multiplied with number of toggles.

5.3.1 CCV-FCS-MPC versus Hysteresis controller

Multiplying the results in tables 4.1 and 4.7 by the results in table 4.4 gives the OPC scores in 5.1. These results show that $T_s = 20\mu s$ is optimal for reference tracking. Which confirms previous findings. Results also show than $T_s = 40\mu s$ is ideal for mitigation of both generator current-and bus voltage THD. A lower sampling period has been shown to mitigate more of the THD. However the higher sampling leads to much lower switching cost.

Table 5.1: Overall performance of CCV-FCS-MPC vesrus hysteresis controller, with switching cost factored in

	FCS-MPC Continous							Hysteresis	
$T_s[\mu s]$	10		20				40		-
Ν	30	15	30				10	35	-
f_{sw} or q_c	0	0	0	10 ²	10^{4}	10 ⁸	0	0	-
OPC SSE	0,22	0,13	0,16	0,16	0,16	0,14	0,33	0,37	1,00
OPC THD Voltage	0,39	0,27	0,27	0,28	0,27	0,28	0,26	0,24	1,00
OPC THD Current	0,37	0,24	0,26	0,27	0,25	0,23	0,19	0,21	1,00

5.3.2 CCV-FCS-MPC versus ICS-MPC

Multiplying the results in tables 4.2 and 4.8 by the results in table 4.5 gives the OPC scores in 5.2. In this table a higher $q_{control}$ leads to better OPC on reference tracking and on THD on the generator currents. Lower switching cost then is more significant than better reference tracking in the OPC. The optimal $q_{control}$ for lowest bus voltage THD is between 10⁴ and 10⁸. This again indicates the significance of lower switching cost.

Table 5.2: Overall performance of CCV-FCS-MPC vesrus ICS-MPC with $f_{sw} = 5kHz$

	FCS-MPC Continous			ICS-MPC	
$T_s[\mu s]$		2	20		
N		3	30		
f_{sw} or q_c	0	10 ²	10^{4}	10^{8}	5kHz
OPC SSE	0,33	0,35	0,33	0,30	1,00
OPC THD Voltage	0,78	0,79	0,77	0,80	1,00
OPC THD Current	0,58	0,60	0,56	0,51	1,00

5.3.3 CCV-FCS-MPC versus ISL-FCS-MPC

Multiplying the results in tables 4.3 and 4.9 by the results in table 4.6 gives the OPC scores in 5.3. Results show the same characteristics for $q_{control}$ as in table 5.2. There is also less reduction in OPC on the THD values than in 5.2. This indicates that if CCV-FCS-MPC is not available for the cascaded MPC structure, it is best to implement the ILS-FCS-MPC instaed of any other benchmark. This also says that FCS-MPC is the best implementation for gate control in a cascaded MPC structure.

	FCS	S-MPC	LSQ		
$T_s[\mu s]$		20			
Ν		30			
q_c	0	10 ²	10^{4}	10 ⁸	-
OPC SSE	0,34	0,36	0,35	0,31	1,00
OPC THD Voltage	0,91	0,93	0,90	0,94	1,00
OPC THD Current	0,71	0,74	0,69	0,63	1,00

Table 5.3: Overall performance of CCV-FCS-MPC vesrus ILS-FCS-MPC

Chapter 6

Conclusions and Recommendations for Further Work

This chapter views the results against the objectives of this thesis. In addition to presenting shortcomings with this study and future work within the research area of cascaded MPC and CCV-FCS-MPC.

6.1 Summary and Conclusions

This thesis studies the effect of controlling gate switches in an APF using FCS-MPC. This gave a cascaded MPC structure, where internal states and a calculated reference from the first MPC is used by a second MPC. The second MPC is designed to track the reference. The second MPC was implemented as a CCV-FCS-MPC, an ILS-FCS-MPC and an ICS-MPC. In addition an existing hysteresis controller was tested. Their performance on harmonic mitigation and reference tracking was quantified and compared. Meaning all objectives of this thesis was fulfilled.

First reference tracking performance and power loss was measured. Results show that an CCV-FCS-MPC with a tuned cost function outperforms hysteresis controllers, ICS-MPC with PWM and an existing ILS-FCS-MPC. With a reduction in SSE of at least 50% compared to any other implementation, while also reducing power loss. THD in a ship power system is reduced for all MPC implementations, compared to a hysteresis controller. Both for an ICS-MPC, an ILS-FCS-MPC and a CCV-FCS-MPC. The CCV-FCS-MPC with a tuned cost function outperforms all other tested implementations. It reduces generator current THD by over 20% compared to any other implementation. While also reducing power loss and maintaining bus voltage THD.

For the CCV-FCS-MPC results show that a sampling time of $20\mu s$ is optimal for reference track-

ing. This is the case both with, and without switching cost factored in. A negligible improvement can be seen when sampling at = $10\mu s$. However greater computational- and switching cost means $20\mu s$ is the best option. Sampling at $40\mu s$ gives SSE over four times higher compared to using $20\mu s$. However a sampling time of $40\mu s$ is still a good option in the cascaded MPC structure. Generator current THD is only increased by 46%. With switching cost factored in, a sampling time of $40\mu s$ gave the best results for the cascaded MPC. Results in this thesis showed that longer control horizons increased both reference tracking error, and generator current THD. Only bus voltage THD was reduced.

6.2 Recommendations for Further Work

Furter work on a short term basis is centered around improvements in simulations. As mentioned in chapter 5. The simulation setup results in delays in the cascaded MPC structure. This needs to be minimized. One possible way to improve this is to integrate the two MPC's into one.

It would also be interesting to study what effects the continuous control variables have on FCS-MPC performance. As mentioned in section 5.1.5 any performance differences found in this study are found with different cost functions. The ILS-FCS-MPC and CCV-FCS-MPC should then be studied with the same cost function.

More work also needs to be done to find optimal implementation of the CCV-FCS-MPC. As mentioned above objective five of this thesis is not fulfilled. Meaning a bigger study on the effect of sampling time control horizon, and cost function parameters are needed.

A further study should also be done on switching cost. This thesis only measures the number of times the gate switches toggle. Switching cost dependant of other factors. Meaning complete switching cost needs further analysis to be established.

Medium and long term future work is centered on hardware implementation. In order to make the cascaded MPC and CCV-FCS.MPC implementable, hardware testing is needed. This means to run the cascaded MPC in real time, with a gate switching MPC sampling at $10 - 40\mu s$. This could create challenges. Solving an MPC that often is computationally expensive. Meaning furter studies and perhaps harware improvements are needed.

Appendix A

Acronyms

MPC Model Predictive Control

FCS-MPC Finite Control Set Model Predictive Control

ICS-MPC Infinite Control Set Model Predictive Control

PWM Pulse Width Modulation

CCV-FCS-MPC Continuous Control Variables Finite Control Set Model Predictive Control

ILS-FCS-MPC Integer Least Square Finite Control Set Model Predictive Control

SQP Sequential Quadratic Programming

APF Active Power Filter

THD Total Harmonic Distortion

MILP Mixed Integer Linear Programming

ILS Integer Least Square

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