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Solid State Circuit Breakers In Medium Voltage Direct Current Systems

Designing, improving and optimizing solid
state circuit breakers for MVDC applications

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Abstract

This thesis is presented to the Norwegian University of Science and Technology as partial fulfillment of the requirements for the degree of Master of Technology in the program of Energy and Environmental Engineering with specialization in Electrical Energy Engineering.

In this text three different solid state circuit breakers (SSCB) for medium voltage direct current (MVDC) systems have been investigated, namely the interrupting, the current limiting and the resistive topologies. In particular, design strategies for each breaker topology has been proposed emphasizing the optimal design of passive elements with regard to different design goals. These design goals include the minimization of total breaking time, maximum fault current, ratings and required number of power semiconductor devices, size of passive components, on-state losses and transient response during no-fault conditions while at the same time maximizing the reliability and controllability of the system.

The breaker topologies designed using the proposed strategies have been simulated for a variety of cases to investigate different design trade-offs. The trade-offs found in the results shows how important it will be to design the breakers and optimize them according to the specific application to which it is to be used. Furthermore the improvement of important parameters with regard to applied power electronic devices have been investigated. How these improvements could potentially affect the performance of the breakers is an important result of the performed analysis' and simulations. The effects of external parameters such as the sensing and coordination equipment and strategies are also discussed and showed to be of great importance.

The findings of the literature study performed in context to this thesis [1] will be shortly summarized in the theory part. These findings include topics on general MVDC systems, its applications and fault mechanisms as well as solid state circuit breakers found in literature. Relevant theory of power semiconductor devices and the modeling of RLC circuitry will also be included.

Analyzing and designing the different breaker topologies will be the main part of this text. The topologies are analyzed using state-space representation and design strategies are proposed for each topology. These design strategies also sheds light on different limitations regarding available technology.

To verify the proposed design strategies, a simulation of a simplified MVDC transmission system has been designed in Simulink. Using this system, all the topologies have been simulated using comparable parameters derived from commercially available technology.

The results of the simulations are compared and any peculiarities discussed. In particular the feasibility of the different topologies for different applications are discussed.

Specific suitability between topologies and applications are discussed as well as possible novel improvements of the topologies. A possible novel topology integrating the current limiting circuit breaker with a buck converter is proposed as a result of the the performed analysis. This however without further in-depth investigation of proposed topology.

Contents

1 Introduction

In context to this thesis, a literature study of medium voltage direct current (MCDC) systems and solid state circuit breakers (SSCB) was performed as a specialization project. The work performed in this thesis will partly be based on the findings in this literature study which will be referred to as [1].

Medium Voltage (MV) direct current (DC) systems is defined in the voltage range 1.5-35 kV [2]. While DC has been integrated in LV and HV systems, it has yet not seen the same penetration in MV systems. The main reason for this has been the lack of technology needed for this specific voltage range and in particular for the purposes usually associated with it [3].

The MV range is usually related to distribution or collector systems whose requirements has previously hindered the implementation of DC. These hindrances are particularly related to insufficient ratings and performance of power semiconductor devices and as well as their price. With recent and future technological advances however, this trend seems to close in on a turning point. Recently The integration of MVDC in a vast variety of applications such as micro grids, collector grids for offshore wind and solar power, marine vessels and industrial applications have been considered. For such applications MVDC may offer advantages such as easy interconnecting of generation and storage devices, reduced number of power conversion stages, no synchronization of phase angles, reduced ratings of cables and switchgear, no reactive voltage drop, easier implementation of high speed and variable frequency operation, no bulky low frequency AC transformers and fully controlled power flow [4].

One of the main challenges of implementing MVDC systems that still impedes its development is the design of proper and satisfactory fault handling technology. Due to inherently low cable inductances in the short distances related to MVDC applications, fault currents quickly rise to unacceptable values and is in need of very fast fault breaking mechanisms. Traditional mechanical AC circuit breakers (ACCB) are too slow to perform this action and since there is no natural zero crossing in DC systems their technology is not applicable. New SSCBs have been proposed in literature to provide fast current interrupting and isolation. Although hybrid DCCB have been proposed and are considered cheaper than its solid state counterpart, they are much slower and bulkier [5].

A literature study on solid state circuit breakers and MVDC systems was performed in [1]. While many topologies of solid state circuit breakers have been proposed and tested, there has not been seen a proper comparison of breaker topologies. In order to investigate the feasibility of such breakers in future MVDC systems, the design and optimization of the breaker topologies is essential. Different applications have different requirements and it will thus be important to investigate how the different parameters in the design process can be suited to such requirements. Furthermore it will be important to realize how technological improvements may affect the feasibility of such systems.

The findings of [1] also suggests that much like in the case of converter technologies, the solid state breakers will all have their suitable application. There may be no single best topology, but rather different degree of suitability regarding different applications. It should thus be interesting to investigate the particularities of the breaker topologies and how these may suit different requirements and application specific needs.

2 Theory

2.1 MVDC systems

2.1.1 Advantages and challenges of DC systems

There are many advantages in choosing DC over AC. the total number of power conversion stages will be reduced due to simplification of interconnecting different types of generation and storage devices [3]. There is obviously no need for synchronization of phase angle and frequency between different generators and loads since there is no phase angle in DC. Also, voltage regulation happens in the converters which eliminates the need for heavy low frequency AC transformers. The same power is transferred by a lower maximum voltage, so size and ratings of cables and switchgear is reduced. The power rating of the cables are further increased by the lack of skin effect seen in AC cables and voltage drop caused by the reactive power is eliminated [4]. The connection of machines to a DC grid will allow the machine to run with variable frequency and in high speed operation which reduces the weight of the motor or generator and improves the efficiency [2].

Fault handling is one of the main challenges in implementng DC systems. Difficult fault conditions owing to the low inductance of cables as well as the lack of natural zero crossing is among the main impeding factors of implementing such systems.

The power flow can be categorized as both an advantage and a challenge. On one side, the elimination of reactive power simplifies the power flow control to only being dependent on the voltage and current. Through the use of power electronic converters the voltages and currents and thus the power flow is fully controllable. On the the other hand, developing a power flow strategy that shares the voltage control between different converter stations, in particular VSC stations has been proven to be challenging. In addition to this, proper dynamic modeling of the power electronic converters are more complicated than the modeling of AC systems. The power electronic converter and their feedback control loop also introduces challenges when assessing the stability of the system [3]. Table 1 summarizes the advantages and challenges of implementing MVDC distribution networks [1].

Table 1: Summary of advantages and challenges in implementing DC distribution networks [1].

Advantages	Challenges
Interconnecting generation and storage devices	Complicated dynamic modelling
Reduced number of power conversion stages	Fault detection
No synchronization of phase angles	Current interruption
Size/ratings of cables and switchgear reduced	Complicating the power flow control
No reactive voltage drop	
High speed and variable frequency operation for connected generator/motor	
No low frequency AC transformers (reduced size/weight)	
Fully controlled power flow	

2.1.2 DC faults

Faults happening in DC systems have the potential of being much worse than in its AC counterpart. In DC systems there does not exist any natural zero crossing. Due to this and the fact that MVDC systems in particular have short line distances meaning low line inductance [4], DC faults can potentially causing severe damage to equipment if not handled correctly.

For DC systems there exists two different types of faults; short circuit (SC) faults and open circuit (OC) faults. Due to its low fault path resistance, the SC faults are the most severe. If an OC fault is left undetected for a long time however, it may cause several other system failures [3]. In this text the SC fault being the most dangerous will be considered.

The location of the fault may also affect the severity of the fault condition. Table 2 shows different kind of faults and their relative frequency in HVDC systems according to [6].

Table 2: Faults locations and relative frequency in HVDC systems 2010 [6].

Fault location	Relative frequency
Converter faults	11.7%
DC equipment faults	14.6%
Transmission line SC	9.2%
AC equipment faults	32.1%
Control system faults	21.6%
Other faults	10.8%

2.2 MVDC applications and challenges

2.2.1 Maritime vessels

MVDC systems have a promising future for many applications. One such application is the electrification of on-board distribution systems in the ship industry. At the time being, all-electric ships (AES) mainly uses AC distribution systems. Recent literature however suggests the future of AES' distribution systems to be MVDC systems, in particular for marine vessels [7] [8] [2]. Using MVDC distribution will have many advantages such as weight reduction and possible economic gain due to fewer converter stages, reduction of cable sizes and elimination of low frequency transformers, ease of integration of energy storage systems (ESS), reduction of required generator capacity, improved survivability and reliability [9] as well as improved efficiency due to implementation of variable speed generators and improved performance of propulsion system [10]. Specifically for Naval vessels is the compatibility with modern electric weaponry.

Recent literature suggests a zonal distribution system to be the most beneficial in terms of reliability and survivability [2] [7]. An example of such a system for a marine vessel can be seen from the diagram in figure 1. The required DC breakers is also depicted in figure 1.
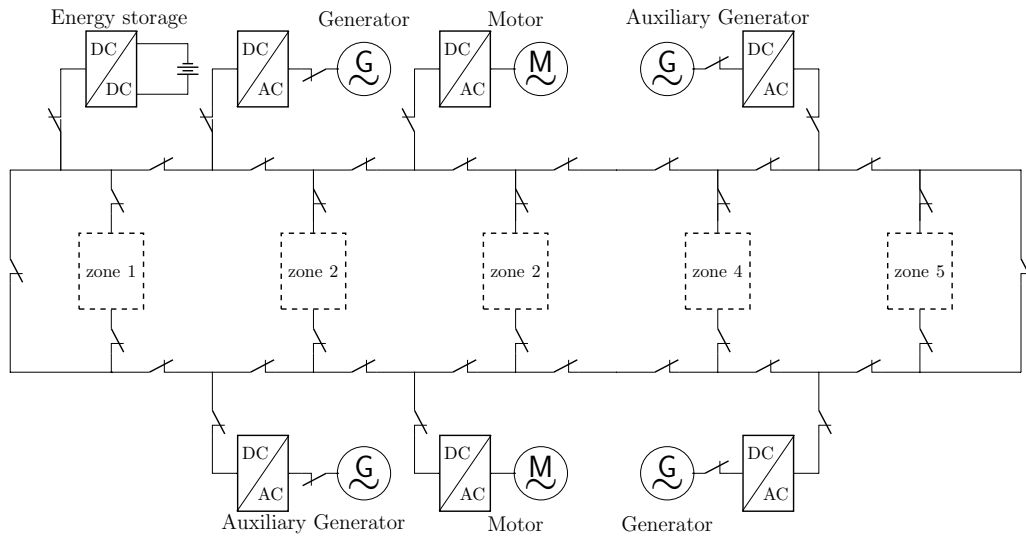
Figure 1: A block diagram of a naval zonal distribution system suggested for MVDC integration [2].

2.2.2 Collector grids

Collector grids reffers to the grid interconnecting many distributed energy sources such as wind turbines or solar panels. The power produced by such forms of generation is first collected in a collector grid before being transfered to the main grid [11].

According to literature, applying MVDC technology for such collector grids may have many benefits. For off-shore wind farms for example, using MVDC in place of MVAC is directly translatable to the reduction of size of required components and transmission lines. A reduction in size means less construction of off-shore platforms and less transportation, while lower weight can reduce construction cost of wind turbine towers etc. [11] [12]. MVDC collector grid can offer a variety of technical advantages as well such as easier implementation of variable speed turbines, better fault handling and easier control [13].

Using MVDC collector grids for large scale solar power plants can also be beneficial in terms of efficiency and investment cost. Solar panels produce DC power, so a DC collector grid eliminates the need for inverters [3]. The resulting system can also be both more reliable and have a faster response time than traditional systems [14].

2.2.3 Microgrids for distribution

In light of the recent trends to decentralize the energy production often referred to as distributed generation (DG) as well as an increase in the consumption of DC loads, using MVDC microgrids for local or islanded didstribution may be beneficial [15] [16] [17]. Figure 2 illustrates how such a microgrid could look like.

MVDC Bus

HVDC link   DC/DC   DC/DC   Energy Storage   Battery, Fuel Cell, Etc.

DC generator (PV plant)   DC/DC   DC/DC   DC Loads   Charging stations, LVDC grid, Future DC-loads*

Variable speed AC generator (wind turbines)   DC/DC

AC Grid   AC/DC   DC/AC   AC Loads   LVAC-Grid, AC machnes, etc.

*DC-houses, DC-industrial facilities, Data centers
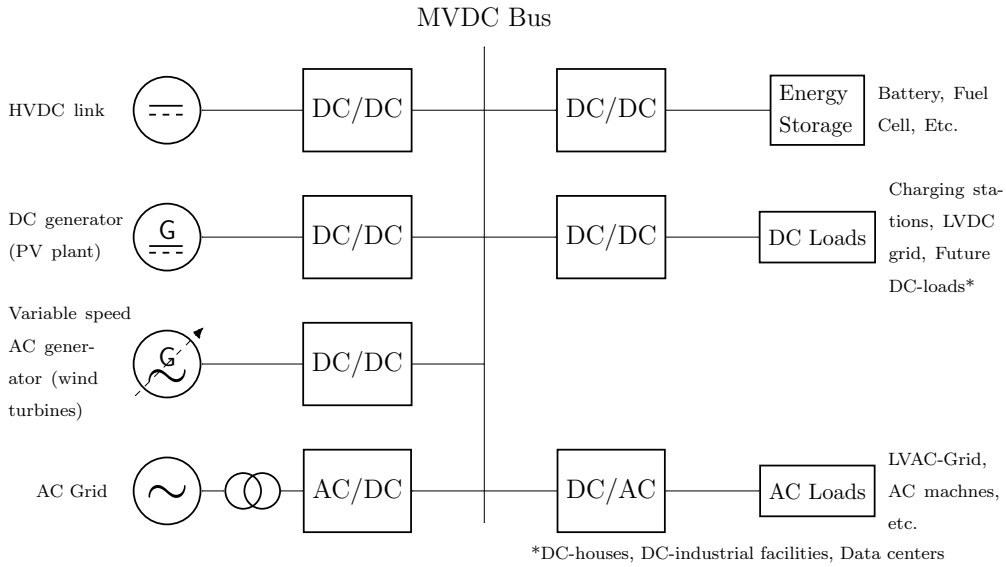
Figure 2: A block diagram of a generic MVDC distribution grid

2.2.4   Other applications

[16] suggest that MVDC distribution may be beneficial for inductrial distribution systems such as an islanded mine cite microgrid.

In [18] using MVDC for long distance high speed railways is suggested.

2.3   Coordination and sensing of faults

Fault coordination will refer to the process of deciding weather or not there exists a fault condition and potentially differentiating the fault types and locating the fault. Sensing of faults will refer to the process of actually implementing sensory equipment to sense the currents and voltages needed in order to discover a fault.

The most time consuming out of these process' is the coordination of faults. In fact, one coordination strategy is simply using an over current relay (O/C relay) technique which is basically only sensing at the point of interest. According to [19], this may happen as fast as $0.8\,\mu s$. The sensing delay time can thus be assumed to be around $1\,\mu s$ and generally much lower than the coordination time.

As of the coordination strategy, it may or may not be very time consuming depending on the strategy used. There are generally two main categories of coordination between fault clearing devices, namely localized fault management (LFM) and centralized fault management (CFM) [20]. LFM is mainly based on relay techniques and can thus be considered to consist of sensing solely. CFM however has a centralized control system that localizes the fault and categorizes it.

Obviously LFM will be much faster than LFM since it needs no means of comunication. Some traditional LFM methods are O/C relays such as the one investigated in [20], distance protection as reported by [21] or active impedance estimation as reported by [22]. Distance protection attempts to estimate the distance to the fault by calculating the apparent resis-

tance based on the measured current and voltage. The active impedance estimation method uses power electronic converters to inject current spikes into the system and measures the corresponding voltage transients. Using this measurement, the active impedance is calculated and has to satisfy some predefined conditions

A more modern way of realizing LFM includes using traveling waves as reported by [23]. The feasibility of using this method in MVDC was reported by [8]. Yet another way of realizing LFM is using artificial intlligence (AI) together with signal processing techniques such as short Fourier transform (SFT) or wavelet transform (WT) [24]. The processed signals are sent through an artificial neural network (ANN) trained to determine the fault type and location. ANNs with a three layer structure is proposed by both [24] and [25].

As for the CFM strategies, the performance reported in literature is much slower. [26] describes a graph traversal method for detection based on the percentage differential scheme (PDF) for detection and identification.

[20] uses an Adapted Percentage Differential Protection (APDP) scheme which implies that instead of using RMS values as in the regular PDP scheme, the APDP uses instantaneous values enabling the CFM to act faster.

In CFM schemes, it is important to notice that approximately $10\,\mu s/km$ needs to be added to the coordination time as it takes time to transfer the data between the coordination points [27].

Table 3 sums up the results of the comparison of coordination strategies found in the literature study performed in relation to this text [1]

Table 3: Summary of coordination strategies [1].

Method	Coordination time	Advantages	Disadvantages
O/C relays (LFM) [19]	0.8-3 µs	+ Very fast + Reliable + No inter communication	- Susceptible to noise and load change - Initial coordination impossible - No location
O/C relays (LFM) with neighbour communication [28]	7000 µs	+ Simple + Sensitive	- Susceptible to noise and load change - Reliability affected by intercommunication
Distance protection (LFM) [21] [20]	$1000\frac{\text{µs}}{\text{m}}$	+ Simple + Reliable + No interconnection	- Very slow - Susceptible to load and system parameter change - Not sensitive
Active impedance [22] [24]		+ So inter communication + Easily integrated in converter control + Very sensitive	- Very susceptible to noise - Can only be implemented in converters
CFM	1000-5000 µs	+ Simple + Sensitive	- Reliability affected by intercommunication
Traveling waves [29]	$1-5$ µs	+ Sensitive + Accurate + No intercommunication + Very sensitive + Very fast	- Difficult to implement in practical systems
ANN [25] [24]		+ Accurate + No intercommunication + Very sensitive + Presumably fast	- Complex - High computational Requirements

2.4 Solid state circuit breakers in the literature

Solid state DCCBs can be categorized by how they handle the residual inductive energy from the fault or by how they clear the fault, namely the interrupting, the current limiting, the resistive [9] and the resonant type CB.

The interrupting category handles the residual energy by using snubber circuitry together with a dissipating element, usually a metal-oxide varistor (MOV). Both snubbers and MOV are placed in parallel with the main switch.

In the limiting category, a freewheeling line-to-line path is provided, either by means of diode or an active switch. The inductive energy stored in the system is in this case dissipated in the freewheeling path.

In the resistive DCCB the active switches is configured in such a way so that when a fault is detected, the equivalent circuit of the breaker turns in to a resistance for the residual inductive power to be dissipated in.

The resonant type DCCB creates a zero crossing by using LCR circuitry. These topologies enables the use of load-commutated thyristors.

2.4.1 Interrupting topologies

Figure 3 shows a schematic diagram of a bi-directional interrupting type breaker. The blue dashed line represents the current path during normal operation. After the switching device S is opened, the current is commuted through a snubber circuit represented by the green dashed line. Lastly the current is diverted through the MOV where all residual energy is dissipated. The final stage is represented by the red dashed line. As can be seen from the figure, a breaker is placed both on the positive and negative poles. This may not be a necessity depending on the system configuration and grounding. Figure 3 a), b) and c) represents different configurations of the switching device S seen in literature. The configuration in a) is a bi-directional connection of two integrated gate bi-polar transistors (IGBT). A topology using a bi-directional connection of SiC JFETS in place of IGBTs is presented by [30] and a similar topology using MOSFETs is investigated by [31]. The topology implementing MOSFETs uses paralleled TVS diodes as the dissipating component, but its ratings are comparatively low with a breaking of 450 A at 270 V. Unidirectional approaches using series connected IGBTs is presented by [32].

Thyristor based topologies similar to that in figure 3 b) using SiC emittor turn-off (ETO) thyristor devices is reported by [5] and [33].

A topology combining the fast acting property of IGBTs and the low loss property of super gate turn off thyristors (SGTO) is proposed by [34] using a configuration similar to the one seen in figure 3 c).
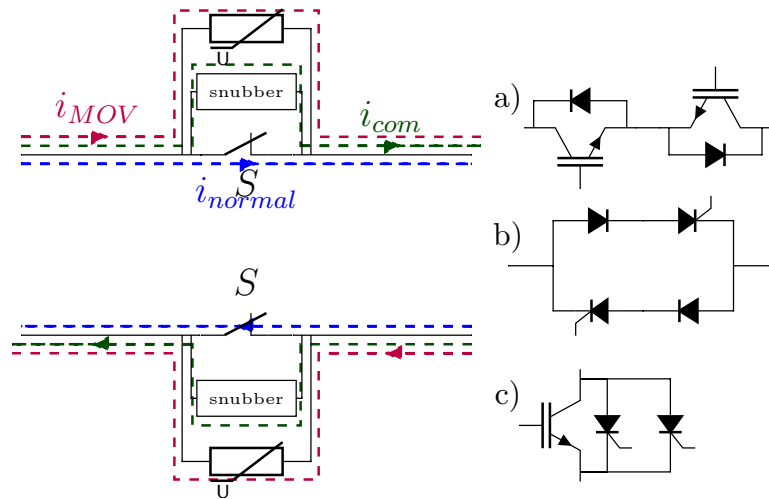
Figure 3: Schematic diagrams of a generic current interrupting DCCB with its breaking stages and different solutions for main switches. a) bidirectional connection of IGBTs, b) bidirectional connection of IGCTs, c) hybrid IGCT + IGBT solution.

2.4.2 Limiting topologies

The schematic diagram of a general bi-directional current limiting breaker can be seen in figure 4. The current path during normal operation is represented by the blue dashed line. When the breaking action is initiated, the current commutates through the path illustrated by the green dashed line. Finally the residual energy is dissipated in through a freewheeling path represented by the red dashed line.
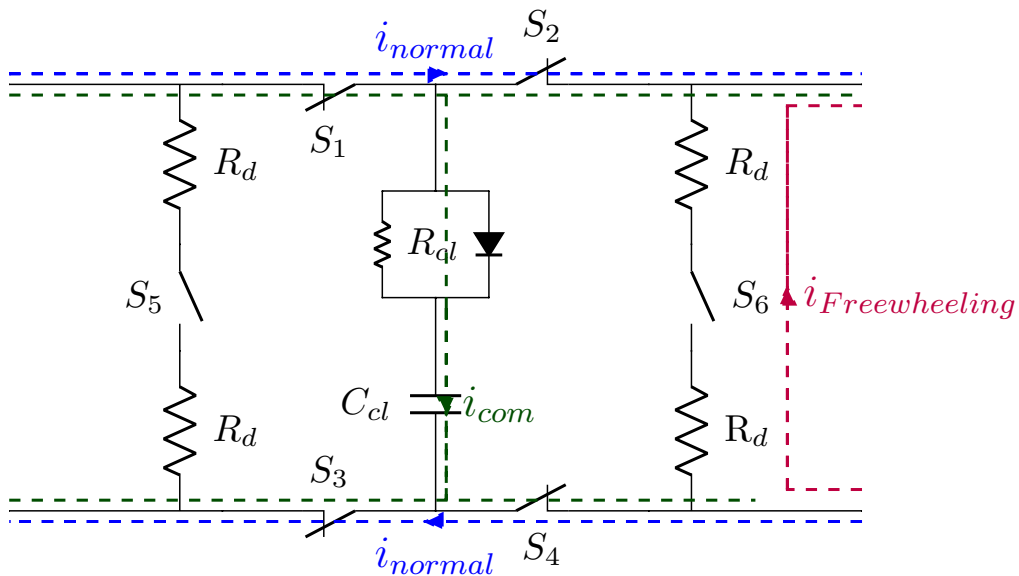
Figure 4: Schematic diagram of a generic bi-directional current limiting DCCB. Current flows in the different stages of current limiting is also shown.

A topology similar to the one seen in figure 4 using SiC MOSFETs and Si IGBTs has been simulated by [9].

A unidirectional circuit breaker is proposed by [35] similar to figure 5 a) using a MOV to depress over voltages. A similar approach is investigated by [36] without the use of an MOV.

In [37] a simple shunt connection with a JFET and a diode similar to the schematic diagram in figure 5 where the JFETS inherent current limiting capability is taken advantage of. This topology is however specifically for depressing capacitor discharges.
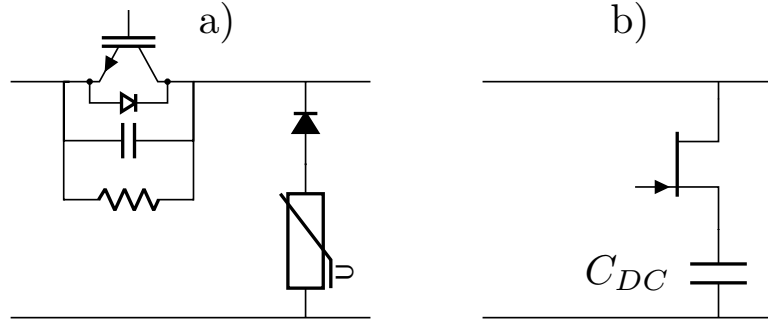
Figure 5: Schematic diagrams of two different current limiting topologies, a) with a MOV in the freewheeling path [35] and b) specifically made for limiting the capacitor discharge [37].

2.4.3 Resistive topologies

Figure 6 shows the schematic diagram of a generic resistive topology [9]. This figure shows the topology used in one phase-leg. Depending on the system, the breaker may or may not be implemented in both the positive and negative leg. The residual inductive power is dissipated in R_d and the voltage clamping is performed by C_{cl}. The topology is bi-directional, but a uni-directional device could be achieved by replacing S_2 and S_3 or S_1 and S_4 by a diode in the direction of power transfer. The switching devices could be any active controllable switch.
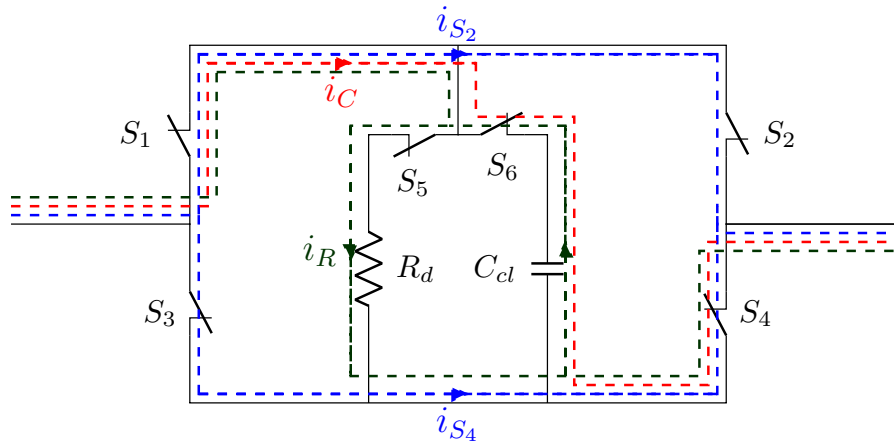
Figure 6: Schematic diagram of a generic resistive DCCB toplogy and its current paths in the current limiting phase.

In this topology breaking is initiated by opening the main switching S_2 and S_3 if the current direction is in the direction as indicated by figure 6. The fault current is then commuted through the clamping capacitor C_{cl}. Then when the voltage over this capacitor reaches a value defined by the control strategy higher than the nominal system voltage, the center switches are activated. The fault current is then dissipated trough the dissipative resistance R_d. If the energy is not dissipated before the current starts rising again several other cycles of switching may be needed. The center switches are then switched off again and the capacitor is re-charged. This switching cycle is performed until the current is effectively reduced to zero.

The topology shown in figure 7 a) is modelled and simulated by [9] using MOSFETs as the active switches. In this paper the resistive topology is simulated with turn off currents of over 2kA and turn-off voltages of over 7kV. A uni-directional approach is investigated by [38] also using IGBTs and diodes in place of S_1 and S_4. This topology can be seen in figure 7 b).
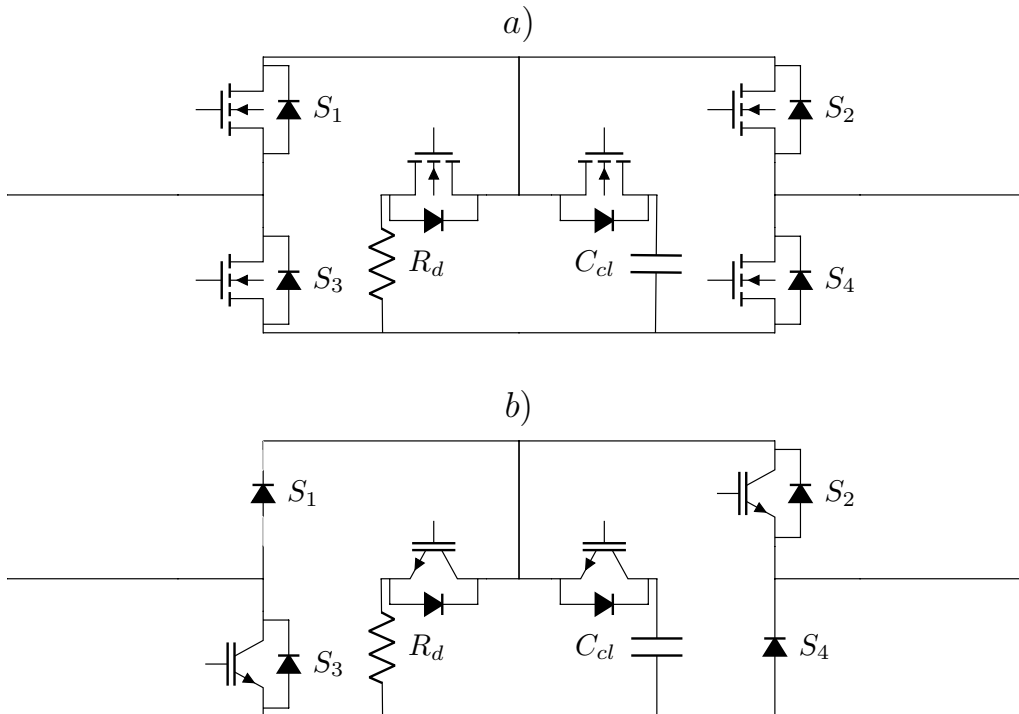
Figure 7: Schematic diagram of resistive DCCB topologies. a) MOSFETs used as active switches in a bidirectional topology [9] and b) IGBTs used in a unidirectional approach [38].

2.4.4 Resonance topologies

The resonance topologies are made in such a way that during normal operation, the circuit breaker has as little effect on the total system as possible. Figure 8 shows a generic resonance breaker with its general working principle. During faults, a resonance circuit will be activated by the transient current, i_{trans} seen in figure 8 causing a resonance current that is fed back to the system forcing the fault current to drop to zero. After the current is driven to zero, the main switch can be closed by gating if it is a fully controllable switch, or is naturally turned off at zero current if it is a thyristor. After the turn-off of the main switch, the residual energy

is dissipated in the resonance circuitry. The resonance circuit and the connection to it differ from different topologies and it shapes the fault current response of the specific breaker.
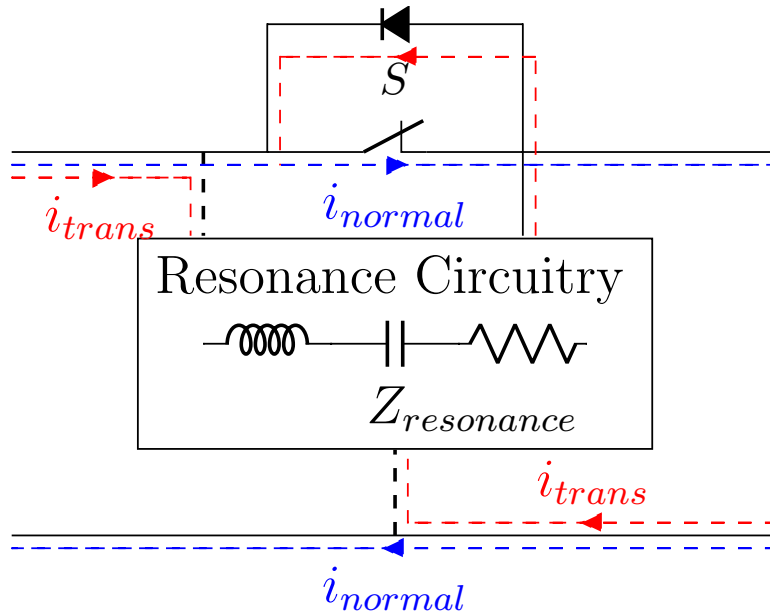
Figure 8: A schematic diagram of a generic resonance breaker and its operation principle.

The resonance topology can be further devided into three sub-categories [1];gate commuted topologies, coupled inductor topologies and Z-source topologies.

Gate commuted topologies Figure 9 shows two examples of gate commuted resonance topology as proposed by [39] and [40]. In these topologies the breaking is initiated by gating of switches connecting the resonance circuitry.
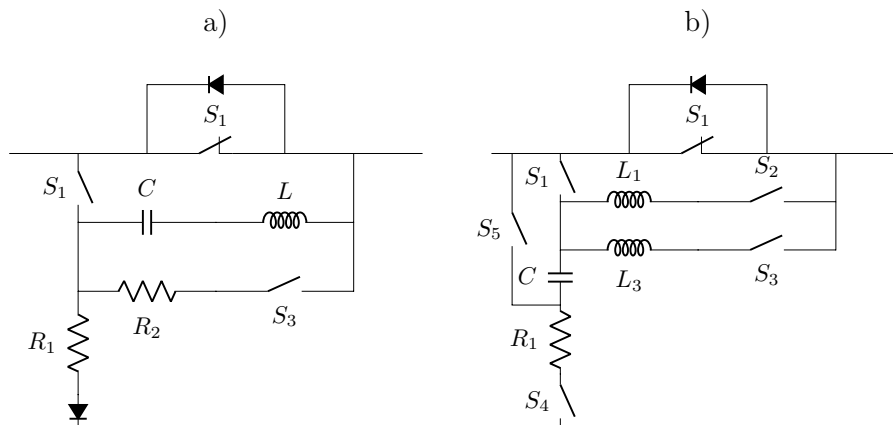
Figure 9: Two different gate commuted resonance topologies, a) as proposed by [39] and b) as proposed by [40].

Coupled inductor topologies In the coupled inductor topologies the breaking happens through self commuting according to the relationship given by the coupled inductors. Figure 10 shows two examples of this topology investigated by [41].
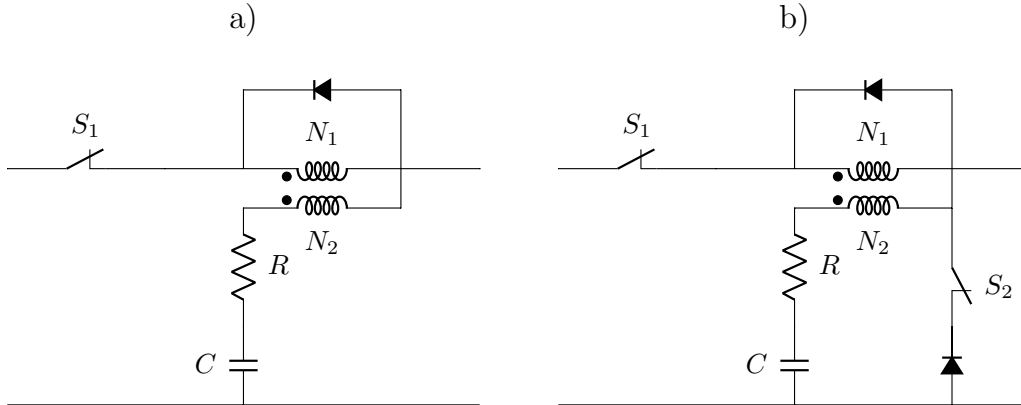
Figure 10: Coupled inductor resonance topologies. a) shows the regular topology and b) shows an altered vertion that allows for manual turn-off [41].

Z-source topologies Many different Z-source topologies have been proposed. In all of these topologies the connected resonance circuitry form a Z-connection between the lines. Figure 11 shows the most basic Z-source topologies as introduced by [42] and [43].
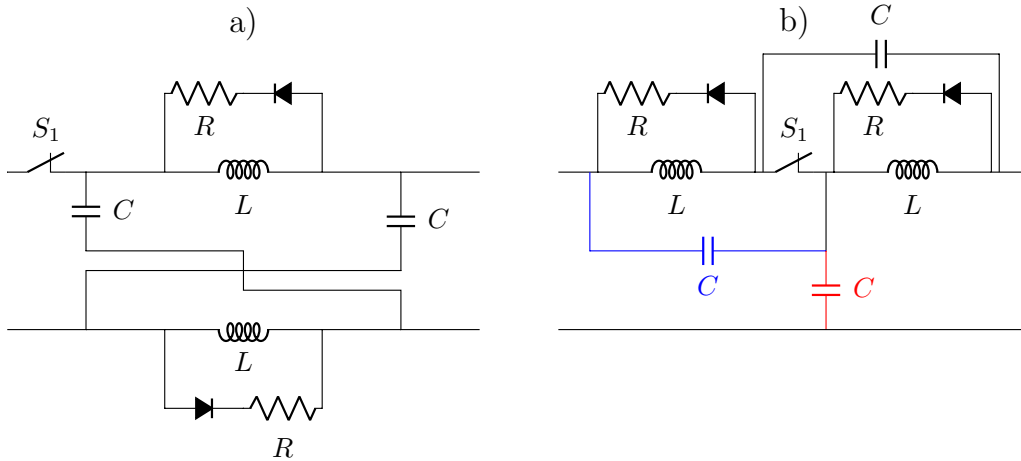
Figure 11: schematic diagrams of Z-source topologies. a) shows the classical crossed topology [42] and b) shows both the series (red colour) and parallel (blue color) topologies.

Figure 12 shows two bi-directional toplogogies proposed by [44] and [45]. The topologies are improved by reducing the required size of passive elements.
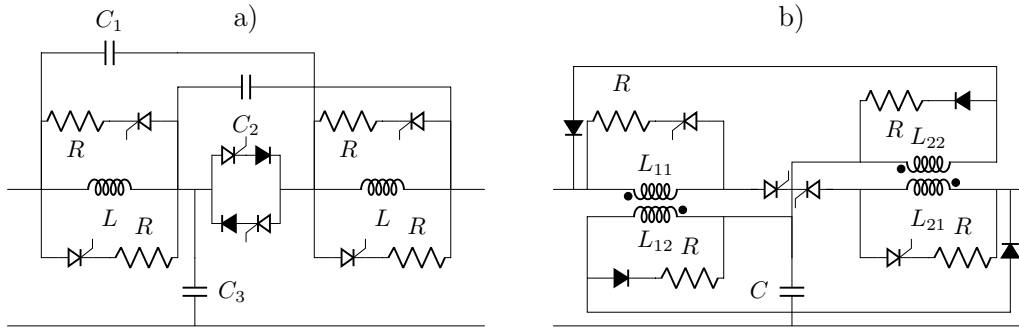
Figure 12: schematic diagrams of two bi-directional Z-source resonance topologies. a) as proposed by [44] and b) a topology with coupled inductors proposed by [45].

Two modified versions of the series Z-source topology are introduced by [46]. These topologies uses current sharing in order to allow transient step changes in the load without activating the circuit breaker. This current sharing is achieved by adding another shunt connected capacitor to the left of S_1 in the series Z-source shown. The modified versions can be seen in figure 13 and by using either inductors (a) or resistors (b) in series with both the shunt connected capacitors, current sharing is achieved with a relationship given by the passive elements. This way, the relationship between the passive elements in the two shunts can be predetermined to allow step changes in the load up to several times the rated load.
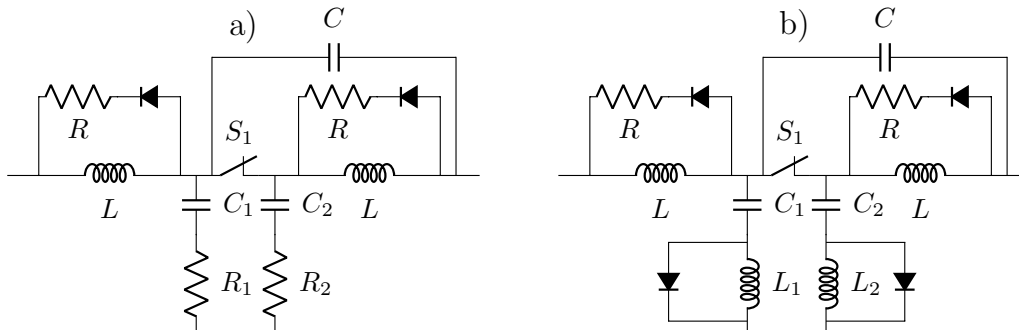
Figure 13: Modified series Z-source breakers. a) using resistors and b) using inductors [46]

A very important feature with the self commuting resonance topologies is that the fault current seen by the source is abruptly driven to zero and the source is thus protected to a very hgh degree compared to the other breaker topologies. In addition to this, self commuting means less complicated control system and cheaper switching devices since the use of thyristors is enabled. These topologies does however on the other hand require large passive elements and can only be triggered by means of relay techniques. This means that the breakers may open even under no-fault conditions. In addition to this there will be a lot of transients during operational changes such as load or voltage steps or other variations.

2.4.5 Summary of topologies found in literature

In Table 4 a general summary of the different DC breaker topologies based on the findings of [1] can be seen. Table 5 summarizes the results of [1] comparing the DC breakers found in literature.

Method	Documented current limiting time	Advantages	Disadvantages
Current interrupting	0.8-70 μs	+ Very fast + Few semiconductor devices + Well documented + Few gate drivers (more reliable)	- High current stress on switches - Voltage sharing difficult - higher losses - very dependant on sensing/initial coordination
Current limiting	150-2500 μs	+ Possibility of full control + Less voltage stress on switches + Lower losses + Fault current not reflected to source + Can reduce required turn-off capability + Can reduce required current limiting reactor	- Complicated control (less reliable) - Voltage sharing very difficult - Very dependant on sensing/initial coordination - Not well documented - Many semiconductor devices - May cause unwanted transient effects
Ressistive	20-900 μs	+ Fully controllable + less voltage stress on switches + less current stress' on switches + Modularity achievable + Can be fast + No snubbers required	- complicated control (less reliable) - Voltage sharing very difficult - Dependant on sensing/initial coordination - Not well documented - Many semiconductor devices - High requirements for resistor energy dissipation
Resonance	200-4000 μs	+ Possibility of controlled turn on/off + Considerably less current stress on switches + Lower losses + Less dependant on Sensing/initial coordination + Use of Thyristors + Soft turn off and possibly turn on + Well documented + Simple control (reliable) + Fault current possibly not reflected to source + No snubbers required	- Slow - Bulky - Limited coordination - Limited control - High requirements for passive elements - Causes unwanted transient effects - May trip during load changes

Table 4: Summary of solid state DCCB topologies

Topology & switching device(s)	L_l[µH]	$t_{breaking}$[µs]	V_{off}[V]	I_{off}[A]
Interrupting IGBT [32] (experimental)	1	8/13	740/790	600/900
Interrupting IGBT + SGTO [34] (expreimental)		140	2300	350
Interrupting Self powered SiC JFET [19] (experimental)		0.8-3	400	180
Interrupting Sic JFET [30] (experimental)	20	10	600	60
interrupting SiC MOSFET [31] (experimental)		70 10	270 270	450 250
Interrupting GaN-on-Si HEMPT (experimental) [47]		0.8	300	45
Limiting Surge Less [35] IGBT	3500	2500	360	24
Limiting Bi-directional [9] IGBT (simulation)	50	600	1200	5000
Limiting JFET [37]	150		-	-
Ressistive MOSFET (Simulation) [9]	2 2	20 40	7150 6200	2250 1350
Ressistive IGBT (Experimental) [48]		900	1000	600
Resonance Normal Thyristor (Simulation) [39]	100	400	380	13.1
Resonance Inductor Thyristor (experimental) [41]	-	300	400	16
Resonance Mod. Ser. Z-source Thyristor (experimental) [46]	-	4-500	100	5
Resonance Z-source Coupled Thyristor (experimental) [46]	-	200	120	3
Resonance Mod. par. Z-source Thyristor (experimental) [49]	-	4000	20	10

Table 5: Characteristics of different DCCB topologies.

2.5 Power semiconductor devices

2.5.1 Relevant characteristics of power semiconductor devices for solid state DCCB applications

Power semiconductor devices come with a datasheet with the purpose of characterizing the specific device in detail. These datasheets contains all the parameters required to estimate the devices performance in terms of both steady state and dynamic behaviour with regard to both the electrical, mechanical, magnetic and thermal aspect of the design. For the purpose of designing solid state DCCB however, a few specific characteristics are especially important. To simplify the process of designing such breakers, the power semiconductor devices will be assumed to be completely characterized by these characteristics.

Maximum rated breakdown voltage, V_B: The maximum rated break down voltage will be denoted by V_B and is the maximum voltage the device is able to withstand before it breaks down to an uncontrollable state. The processes of break down may be different depending on the type of device. Exceeding this value is typically characterized by a sudden increase in leakage current. Most commonly this voltage limit is associated with avalanche multiplication [50].

Maximum rated Current, I_M: The maximum rated current is the maximum current the device may withstand and will be denoted by I_M. This value may not be exceeded due to a number of reasons depending on the type of device. Typically this value may represent the rated value at which the device temperature does not exceed a specific temperature, at which internal contacts is not evaporated or at which the external contactor looses its ability to handle the current [50].

Maximum rated power dissipation or load integral, P_M or $I^2_{t,M}$: The maximum power dissipation is related to the maximum temperature at which the device can withstand without being damaged and is denoted by P_M. It can be expresses in terms of thermal properties as;

$$P_M = \frac{T_{j,max} - T_c}{R^\phi_{j,c}} \tag{1}$$

Where $T_{j,max}$ is the maximum rated junction temperature, T_c is the case temperature and $R^\phi_{j,c}$ is the thermal resistance between the device junction and the case [50].

Specifically for diodes and thyristors is the maximum load integral, here denoted as $I^2_{t,M}$. This value translates to the maximum allowable energy dissipated in the device and is a function of time. It can be found by performing the following integral;

$$I^2_{t,M} = \int_{t_0}^{t_0+t_p} I^2 dt \tag{2}$$

Where t_0 is the starting time, t_p is specified by the manufacturer, usually as $10\,\text{ms}$ representing half a sine wave. For the application of solid state DCCB however t_0 can be defined as the moment the fault incurs and t_p the moment at which the current is successfully driven to zero.

Maximum allowable rate of voltage and current change, v_M' and i_M': The Maximum allowable rate of voltage and current change will be denoted by v_M' and i_M' respectively. In the case of no snubber circuitry, v' is found by;

$$v' = \frac{dv}{dt} = \frac{v_{noff}}{t_{vr}} \tag{3}$$

Where v_{off} is the voltage at turn-off and t_{vr} is the voltage rise time.

If an RCD snubber circuit is used, v' can be assumed only to be dependant on the capacitor of the snubber circuit.

In the case of solid state DCCB application the most relevant and interesting value of i' is the rate of rise of the fault current. This can be assumed only to be dependant on the total series inductance of the system, including DC-line inductance, stray inductances as well as current limiting inductances if relevant.

Turn-on and turn-off delay time, $t_{d,on}$ and $t_{d,off}$: The delay turn-on and turn-off is directly associated with the charging and discharging if the gate [50] and will be denoted by $t_{d,on}$ and $t_{d,off}$ respectively. These values will be important in investigating the breaking times of the solid state DCCB.

On-state resistance R_{on} and on-state voltage V_{on}: All power semiconductor devices will have losses when conducting. These losses are represented by an equivalent resistance, here denoted by R_{on}. Although bipolar devices also have a voltage drop associated with the on-state losses (e.g. conductivity modulation in IGBTs), this can be combined into the R_{on} equivalent when considering steady state operation which will be the case when the DCCB is not performing the breaking action. It is these steady state losses that are interesting for this application since the power semiconductor devices are turned on during normal operation.

2.6 Response of RLC circuitry

As seen in section 2.4, the solid state circuit breakers uses snubber circuitry or other connections of passive elements in order to protect the switching devices and to drive the fault current to zero. The equivalent circuits of the breaker topologies during faults will therefore include different configurations of RLC circuitry. Thus in order to analyze the topologies response during fault conditions a general way of analyzing such RLC circuits should be in place.

In this section the response of RLC circuitry will be investigated. A structured way of analyzing such circuits and how its parameters will affect the total design will be presented.

2.6.1 General second degree systems

The most general second order system is given by the following transfer function;

$$G_{2nd} = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} n(s) \tag{4}$$

Where ω_0 is the natural frequency of the system and ζ is the damping factor. The natural frequency decides the undamped frequency of the response. The damping factor work as to dampen the ringing of the response and alters the frequency according to;

$$\omega_d = \omega_0 \sqrt{1 - \zeta^2}$$

Where ω_d is the frequency of the response ringing.

The numerator term $n(s)$ can be any irrational function with a numerator of degree ≤ 2 and denominator of degree ≤ 1. In this text, for practical reasons, the numerator of $n(s)$ will only be considered to be ≤ 1. In particular, three different numerator terms will be investigated.

$n(s) = K = n_i$, where K is an arbitrary constant will be referred to as the impulse response of the system with an impulse magnitude of K.

$n(s) = Ks = n_{i0}$ will be referred to as the zero-pole impulse response with an impulse magnitude of K.

$n(s) = \frac{K}{s} = n_s$ will be referred to as the step response of the system with a step magnitude of K.

Any numerator term can then be divided into parts on the following form;

$$n(s) = n_i + n_{i0} + n_s$$

Furthermore the solution of the second order system can have three distinct cases depending on the value of the damping factor ζ, namely the under damped, critically damped and over damped cases where $0 \leq \zeta < 1$, $\zeta = 1$, and $\zeta > 1$ respectively. Typical waveform for the discussed responses can be seen in table 6.

From table 6 it is interesting to note that the impulse response is delayed by $\frac{\pi}{2}$ rad relative to the step response. The Impulse response with zero is delayed again delayed by $\frac{\pi}{2}$ rad relative to the regular impulse response. This is due to the fact that the impulse response

is the derivative of step response and the zero-pole impulse response is the derivative of the impulse response.

The maximum magnitude of the responses for the three cases is $2K$, $K\omega$ and $K\omega^2$ respectively where K is some arbitrary constant. The magnitude, or overshoot of the responses decreases with increasing ζ.

Table 6 shows the solutions and relevant characteristics for the step and impulse response.

The solutions $c(t)$ can be found by inverse Laplace transformation of equation 2.6.1. The time of maximum peak t_{max} is found by differentiating the solutions $c(t)$ and solving for zero. Substituting t_{max} in the solutions $c(t_{max})$ yields the maximum peak. The settling time is defined to be the time until the response is bounded by a 2% increment compared to the steady state solution $c(\inf)$. This is found by solving $c(t) = 0.02$. Settling time is independent of the numerator term.

Table 6: A table illustrating the responses of over-, under- and critically damped second order systems.

	Under damped, $\mathbf{0 \geq \zeta < 1}$
Step response $\frac{K}{s}$	$C = 1 - exp\big(-\zeta\omega_0 t\big)\Big[\cos\big(\omega_d t\big) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\big(\omega_d t\big)\Big]$ $C_{max} = 1 - exp\big(-\zeta\omega_0\frac{\pi}{\omega_d}\big)\Big[\cos\big(\pi\big) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\big(\pi\big)\Big]$ $t_{max} = \frac{\pi}{\omega_d}$
Impulse response K	$C = \frac{\omega_0}{\sqrt{1-\zeta^2}}\exp\big(-\zeta\omega_0 t\big)\Big[\sin\big(\omega_d t\big)\Big]$ $C_{max} = \omega_0\exp\Big(-\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\big(\frac{\sqrt{1-\zeta^2}}{\zeta}\big)\Big)$ $t_{max} = \frac{1}{\omega_d}\tan^{-1}\big(\frac{\sqrt{1-\zeta^2}}{\zeta}\big)$
Settling time	$t_s^{2\%} = \frac{4}{\zeta\omega_0}$
	Critically damped, $\zeta = 1$
Step response	$C = 1 - \exp\big(-\omega_0 t\big)\Big[1 + \omega_0 t\Big]$ $C_{max} = 1$ $t_{max} = N/A$
Impulse response K	$C = \omega_0^2 t\exp\big(-\omega_0 t\big)$ $C_{max} = \omega_0\exp\Big(-\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\big(\frac{\sqrt{1-\zeta^2}}{\zeta}\big)\Big)$ $t_{max} = \frac{1}{\omega_d}\tan^{-1}\big(\frac{\sqrt{1-\zeta^2}}{\zeta}\big)$
Settling time	$t_s^{2\%} = \frac{4}{\zeta\omega_0}$
	Over damped, $\zeta > 1$
Step response	$C = 1 + \frac{\omega_0}{1\sqrt{\zeta^2-1}}\Big[\frac{\exp\big(-s_1 t\big)}{s_1} - \frac{\exp\big(-s_1 t\big)}{s_1}\Big]^{a)}$ $C_{max} = 1$ $t_{max} = N/A$
Impulse response K	$C = \frac{\omega_0}{2\sqrt{\zeta^2-1}}\Big[\exp\big(-s_1 t\big) - \exp\big(-s_2 t\big)\Big]^{a)}$ $C_{max} = \omega_0\exp\Big(-\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\big(\frac{\sqrt{1-\zeta^2}}{\zeta}\big)\Big)$ $t_{max} = \frac{1}{\omega_d}\tan^{-1}\big(\frac{\sqrt{1-\zeta^2}}{\zeta}\big)$
Settling time $t_s^{2\%}$	$T \leftarrow \exp\big(-K*T\big)\Big[\cosh\big(T\big) + K\sinh\big(T\big)\Big] = 0.02$ $t_s^{2\%} = \frac{T}{|D|}, \quad K = \frac{E}{D}, \quad E = -\frac{s_1+s_2}{2}, \quad D = -\frac{s_2-s_1}{2}$

Table 7: Characteristics of the step and impulse response.
a) $s_1 = \omega_0\big(\zeta + \sqrt{\zeta^2-1}\big)$, $s_1 = \omega_0\big(\zeta - \sqrt{\zeta^2-1}\big)$

2.6.2 Series RLC example

Figure 14 shows a circuit with a series connection of a resistor (R), an inductor (L) and a capacitance (C). This circuit will be used throughout this section as an example to illustrate how the RLC circuitry will be analyzed. As will be seen in section 3 this particular circuit will also be very relevant to the behaviour of solid state circuit breakers.
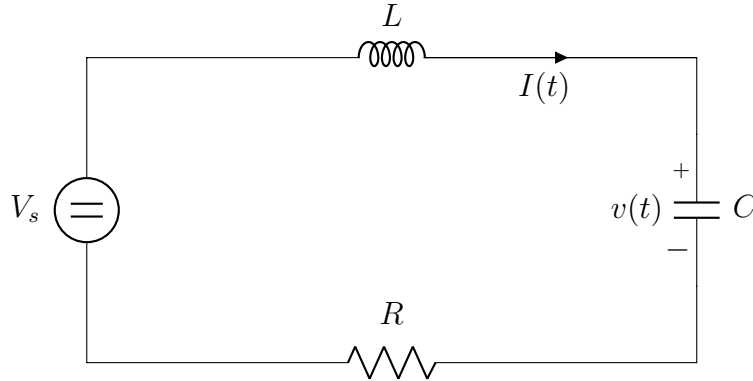
Figure 14: Schematic diagram of a series RLC circuit.

The time solution of circuits more complicated than the one shown in figure 14 can become tedious and difficult to comprehend and analyze. Instead of finding the the complete analytical expression of the circuits behaviour, the circuit will be investigated using Laplace transform and transfer function.

Using Kirchoffs Voltage Law (KVL) the circuit can be expressed as;

$$V_s = L\frac{di}{dt} + v + Ri \tag{5}$$

$$i = C\frac{dv}{dt} \tag{6}$$

Taking the Laplace transform of (5) and (6) yields;

$$\frac{V_s}{s} = Lsi - Li(0) + v + Ri \tag{7}$$

$$i = Csv - Cv(0) \tag{8}$$

Treating the initianl conditions i(0) and v(0) as sources, and rewriting as $\mathbf{Ax} = \mathbf{b}$, where;

$$\mathbf{x} = \begin{bmatrix} v \\ i \end{bmatrix}, \ \mathbf{b} = \begin{bmatrix} \frac{V_s}{s} + Li(0) \\ Cv(0) \end{bmatrix}, \ \mathbf{A} = \begin{bmatrix} 1 & R + Ls \\ Cs & -1 \end{bmatrix} \tag{9}$$

With the solution expressed as $\mathbf{x} = \mathbf{A}^{-1}\mathbf{b}$, system (57) becomes;

$$\mathbf{x} = \frac{\dfrac{1}{LC}}{\dfrac{1}{LC} + \dfrac{R}{L}s + s^2} \begin{bmatrix} 1 & R + Ls \\ Cs & -1 \end{bmatrix} \begin{bmatrix} \dfrac{V_s}{s} + Li(0) \\ Cv(0) \end{bmatrix} \tag{10}$$

This is a recognizable second order transfer function. Introducing the standard second order transfer function or the natural response as;

$$G_n = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{11}$$

The natural frequency ω_0, the damping factor ζ and the dampened frequency of the system can thus be given as;

$$\omega_0 = \frac{1}{\sqrt{LC}}, \quad \zeta = \frac{R}{2}\sqrt{\frac{C}{L}}, \quad \omega_d = \omega_0\sqrt{1 - \zeta^2} \tag{12}$$

Now, from equation 10, the current and the voltage can be given as;

$$v = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \left[\underbrace{\frac{V_s}{s}}_{step} + \underbrace{Li(0)}_{impulse} + \underbrace{CRv(0)}_{impluse} + \underbrace{CLsv(0)}_{impulse+zero} \right] \tag{13}$$

$$i = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \left[\underbrace{CV_s}_{impulse} + \underbrace{LCsi(0)}_{impulse+zero} - \underbrace{Cv(0)}_{impulse} \right] \tag{14}$$

For convenience, the following compact form will be used in this text;

$$\mathbf{x} = G_n \begin{bmatrix} \dfrac{1}{\omega_0^2}v(0) & Li(0) + CRv(0) & V_s \\ \dfrac{1}{\omega_0^2} & C(V_s - v(0)) & 0 \end{bmatrix} \begin{bmatrix} s \\ 1 \\ \dfrac{1}{s} \end{bmatrix} \tag{15}$$

The form given in equation (15) is very useful in a design context because it intuitively describes the contribution of the source and the initial conditions by them selves and combines them as the sum of step- and impulse responses as well as zero-impulse responses. The contributions from the initial conditions can be very interesting, especially in circuits that abruptly change their characteristics before steady state is reached. As will be seen in section 3, this is usually the case when working with circuit breakers.

To illustrate the power of equations 13 and 14 table 8 shows what impact of increasing the initial condition as well as increasing the R, L, and C will have on the current, $i(t)$ and voltage $v(t)$ and their response time t_{ss}.

Table 8: A table illustrating the effects of increasing the prameters in equations 13 and 14 on the current and voltage response $i(t)$ and $v(t)$. t_{ss} is the time to reach steady state.

	$L \uparrow$	$C \uparrow$	$R \uparrow$	$v(0) \uparrow$	$i(0) \uparrow$
$i(t)$	$\dfrac{di}{dt} \downarrow$ $t_{ss} \downarrow$	$i_{peak} \uparrow$ $t_{ss} \downarrow$	$i_{peak} \downarrow$ $t_{ss} \downarrow$	$i_{peak} \downarrow$ t_{ss} -	$i_{peak} \uparrow$ t_{ss} -
$v(t)$	$v_{peak} \uparrow$ $t_{ss} \downarrow$	$\dfrac{dv}{dt} \downarrow$ $t_{ss} \downarrow$	$v_{peak} \downarrow$ $t_{ss} \downarrow$	$v_{peak} \downarrow$ t_{ss} -	$v_{peak} \uparrow$ t_{ss} -

3 Design of solid state DCCB

3.1 General design goals

Although there may be many different goals for the design of solid state DCCB, some are more general and obvious than others. Based on the literature review of these breakers performed in [1], for the purpose of this text, the following design goals will be considered.

3.1.1 Minimizing of breaking time

This minimizing of breaking time will be defined as the total time from when the breaker receives the fault signal and the fault clearance process is initiated to the time when the current is successfully driven to zero. In general, this time interval will depend heavily on both the breaker topology as well as the chosen power semiconductors. In addition to this, it is expected to be a high dependency between the breaking time and the total line reactance of the system since this is what governs the current rising slope. The detection and coordination of the fault will also have a large impact on this. In general, if it takes a long time before the fault is detected and thus communicated to the breaker, the fault current will increase more and there will thus be a larger fault energy to be dissipated in the breaker.

3.1.2 Minimizing of passive devices

Passive devices such as inductors and capacitors will be needed in different ways depending on the topology of the breaker. Snubber circuitry will be needed to protect the power semiconductor devices against over-voltages and over-currents and in some topologies, charging capacitors or resonance circuitry may be required in order to drive the fault current to zero. Since high power passive elements are both expensive and bulky, designing them to be as small as possible, yet being able to perform their task as required is crucial in order to minimize economic impact as well as size and weight of the breaker.

3.1.3 Minimizing of maximum fault current

The maximum fault current is mainly affected by how quickly the fault is detected and communicated to the breaker. The different breakers do however offer different dynamic behaviour that may affect this. Resonance type breakers autonomously starts the breaking process without the need for sensing of fault. Such breakers are thus expected to be able to limit this current more effectively than other topologies.

3.1.4 Minimizing ratings and required number of power semiconductor devices

Since the power semiconductor devices themselves will be a large part of the economic investment, the rating and number of such devices should be minimized. In addition to this, a large number of such devices may complicate the design.

3.1.5 Controllability

Controllability is here referred to as the ability to control the current through the breaker. This may not be required by the application, but can have positive impacts on the fault managing

process by limiting the current to a defined magnitude until fault coordination is finished to decide if the breaker should open or close. Some topologies may offer this ability, while it would be impractical or impossible in other topologies. A higher degree of controllability is generally associated with a more complex breaker.

3.1.6 Minimization of on-state losses

The on-state losses are the losses that the breaker incur on the system during normal operation. These losses are mainly dependant on the choice of power semiconductor devices. It is important that these are as low as possible in order to provide an efficient solution. Low on-state losses also translates to cheaper and smaller heat sinks.

3.1.7 Transient response to no-fault conditions

The dynamic behaviour of the breakers during no-fault conditions should be considered when relevant. This mainly applies to resonance type breakers.

3.1.8 Reliability

The reliability of the breaker is regarded as the breakers ability to perform the breaking action under a vast variety of conditions without failing. Reliability is very important since failure to initiate the breaking action can cause high currents to destroy important and expensive equipment.

3.2   Design system

Figure 15 shows the schematic diagram of a simplified DC transmission line with a DC power source V_i and a load represented by a resistnce R_L. This is the system that will be considered for the desing purposes in this section and used in the simulations to be performed in section 4. In this figure the breaker is represented as a switch S and the DC cables are simplified and modelled as having only a line inductance of $L_{tot} = L_1 + L_2$. It is assumed that $R_L >> R_l$ where R_l is the line resistance and is thus assumed negligible. The fault branch with fault resistance R_f is placed between L_1 and L_2 to illustrate the fault location. $L_1 = L_{tot}$ will thus modulate a fault happening close to the load and $L_1 = 0$ will modulate a fault happening close to the breaker. As will be further discussed in this section, in order to limit the fault current through the switching device of the breaker, a current limiting inductor will be required. This current limiting inductor will be denoted by L_s as seen in figure 15.
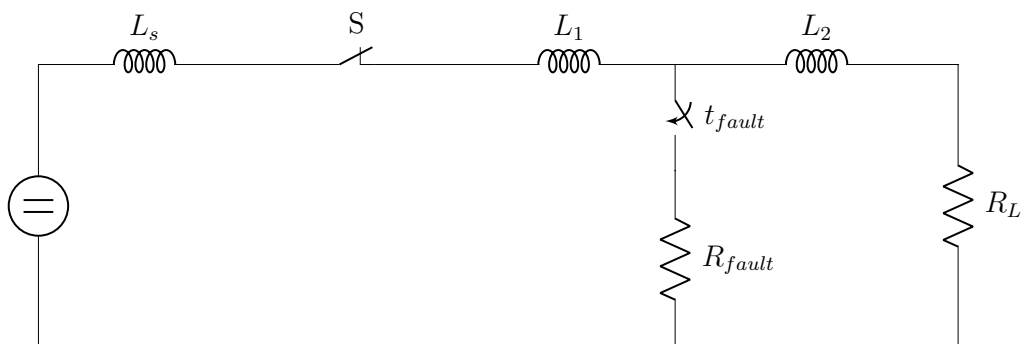
Figure 15: Schematic diagram of the system considered in this text for the design process.

For the purposes of this text the breakers illustrated as S in figure 15 will only be considered as unidirectional.

3.3 Interrupting topologies
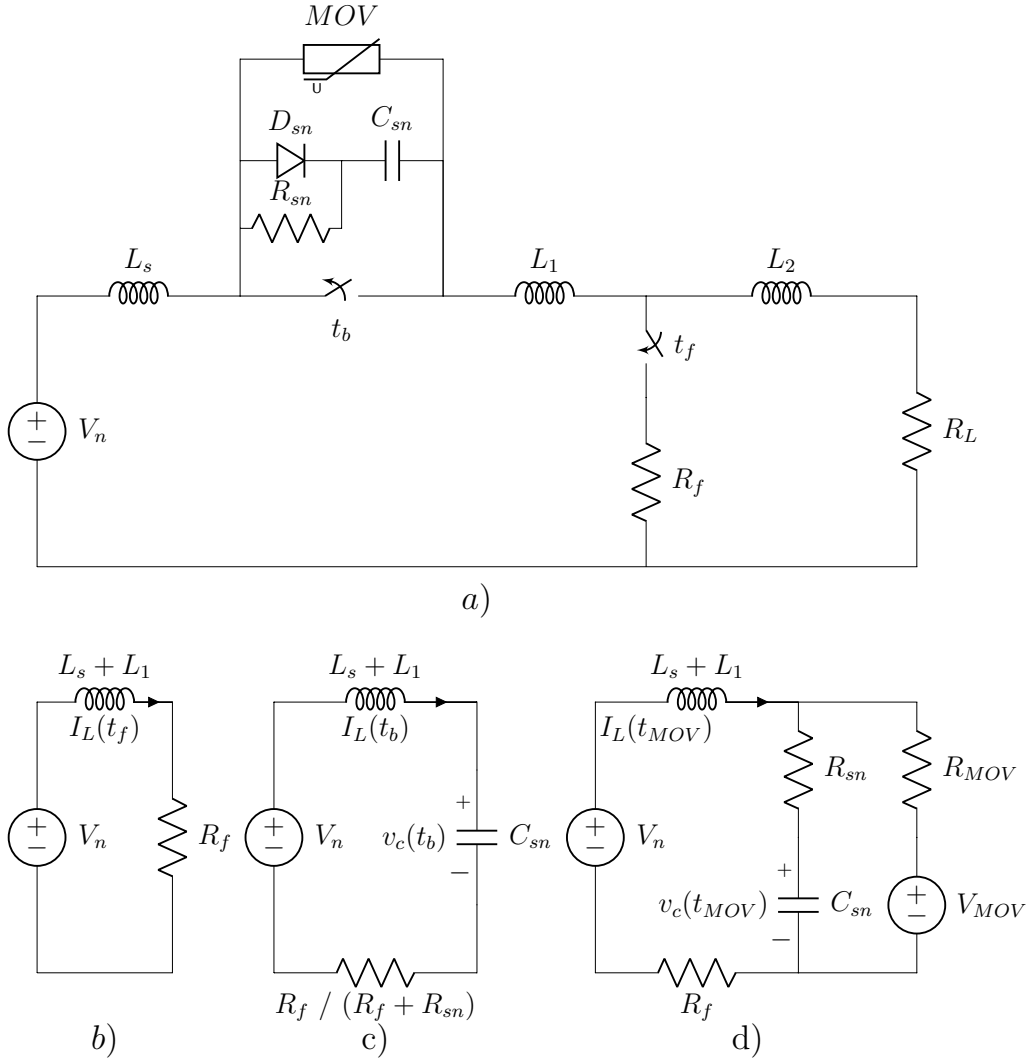
Figure 16: a) Schematic diagram an interrupting DCCB implemented in the design system. b) Equivalent circuit after fault occurs at time t_f. c) Equivalent circuit after the switch opens at time t_b with resistance R_f and eqeuvalent circuit after MOV has stopped conducting with resistance $R_f + R_{sn}$. c) Equivalent circuit when MOV clamping voltage is reached at time t_{MOV}

3.3.1 Steady state

At steady state, the nominal current, I_n flows through the load, R_L driven by the DC nominal voltage, V_n. This phase is where the breaker losses are investigated. In reality, the switch S_1 will be a power semiconductor device such as MOSFET, IGBT or a Thyristor configuration. These devices will have an on-state resistance R_{on}. The bipolar devices (IGBT and thyristor) will have an on-state voltage drop, V_{on} in addition to this.

The snubber capacitance, C_{sn} and the MOV will in practice have a leakage current that can be modelled as a large shunt resistance. Although these shunt resistors will have a non

linear behaviour, they can be modelled to be constants during steady state. The voltage over the capacitor and MOV during steady state is equal to the voltage drop over the switch S_1 (semiconductor device in practice). Since the MOV and capacitor must be rated according to the expected over voltages which will be bigger than the nominal voltage V_n. The voltage drop over the switching element will be much lower than this, and the leakage current in both the capacitance and MOV can thus be regarded as negligible.

The nominal power loss of the circuit breaker can thus be given as;

$$P_b = I_n R_{on}^2 + I_n V_{on} \tag{16}$$

Where the term, with V_{on} is not regarded in the case of the switching element being a unipolar device such as a MOSFET or JFET.

3.3.2 Stage 1: Occurrence of fault

During stage 1 seen in figure 16 b) the short circuit fault has occurred, but the switch S_1 has not yet been switched of. The fault current will short through the fault resistance R_f and increase in magnitude very fast. Analyzing the circuit diagram in figure 16 b) and assuming $R_f = 0$ the rate of change in the fault current in this phase ca be given by;

$$\frac{dI_f}{dt} = \frac{1}{(L_s + L_1)}V_n \tag{17}$$

Assuming worst case scenario where $L_1 = 0$, the current limiting inductance L_s must be chosen so that the maximum $\frac{di}{dt}$ limit of the switching element is not surpassed. The first design criterion of the interrupting breaker is thus;

$$L_s = \frac{V_n}{\frac{di}{dt}_{max}} \tag{18}$$

Where $\frac{di}{dt}_{max}$ is the maximum allowed rate of rise current in the chosen switching element.

If the the maximum allowed rate of rise of the current is not given in the datasheet, it can be calculated as;

$$\frac{di}{dt}_{max} = \frac{I_{max} - I_n}{t_b} \tag{19}$$

Where I_{max} is the maximal rated current through the switching device and t_b is the time it takes before the breaking is initiated by the switching device referred to as the total delay time.

It may also be worth checking if the maximum rate of current change is consistent with the maximal rated current for the specific design. To make sure that no maximal ratings are violated, the inductance L_s should be designed as;

$$L_s \geq \frac{V_n}{argmin[\frac{di}{dt}_{max}, \frac{I_{max} - I_n}{t_b}]} \tag{20}$$

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3.3.3 Stage 1-2: Commutation

In the previous paragraphs, instant commutation between the switching device and the snubber has been assumed. In reality the current through the switch will not instantly drop to zero, but undergo a commutation process depending on the type of power semiconductor device. This commutation may affect the design in two different ways. It may slow down the total time used for breaking. Secondly it may alter the choice of L_s or C_{sn} due to large power dissipation in the switching device.

The commutation process is the time interval between stage 1 and 2 seen in figure 16 b) and c). During this time the current in the switching device will decrease according to the falling time of the chosen power semiconductor device. This falling time is different from uni-polar and bi-polar devices.

For unipolar devices such as MOSFETs anf JFETs, falling time will be defined as, t_{fall} and is the time from when the current through the switching device starts to decrease, to the the time where it is practically regarded as zero (i.e not considering leakage).

Bipolar devices such as IGBTs, GTOs and IGCTs will have two distinct falling times t_{fall1} and t_{fall2}. t_{fall1} is the time from when the current starts decreasing until it reaches 10% of its original value. t_{fall2} on the other hand is the time from t_{fall1} to the time when the current reaches its virtually zero value (not considering leakage). This last part is generally slower and referred to as the tailing time.

The power dissipation in the switching device can be a limiting design factor. Assuming that the falling of the current through the switching element, i_{S_1} and the current through the capacitor i_C is linear and given by;

$$i_{S_1} = I(t_b)[1 - \frac{t}{t_{fall}}] \tag{21}$$

$$i_C = \frac{I(t_b)}{t_{fall}}t \tag{22}$$

The voltage over the capacitor is thus given by;

$$v_c = \frac{1}{C}\int_{t_b}^{t} i_c dt = \frac{I(t_b)}{2Ct_f}t^2 \tag{23}$$

Then, the power dissipated in the switching device is;

$$P_{S_1} = i_{S_1}v_c = \frac{I(t_b)^2}{2Ct_f}[t^2 - \frac{t^3}{t_{fall}}] \tag{24}$$

An extrema of the power can by fund by;

$$\frac{dP_{S_1}}{dt} = \frac{I(t_b)^2}{2Ct_f}[2t - \frac{3t^2}{t_{fall}}] = 0 \rightarrow t = \frac{2}{3}t_{fall} \tag{25}$$

Sice the expression $k[2t - \frac{3t^2}{t_{fall}}]$ is a combination of a the strictly increasing linear term $2t$ and the concave term $\frac{3t^2}{t_{fall}}$, the extrema found at $t = \frac{2}{3}t_{fall}$ is indeed a maximum value of the function. The maximum power dissipation in the switch can thus be given by;

$$P_{max} = \frac{2I(t_b)^2}{27C}t_{fall} \tag{26}$$

A maximum rating of the power dissipation in the switching device P_{off} can be found in or calculated from the data sheet and should be considered in the design.

If the maximum rating is a limiting factor in the design, the capacitor should be design to;

$$C = \frac{2I(t_b)^2}{27P_{max}}t_{fall} \tag{27}$$

3.3.4   Stage 2: Switch off

Stage 2 is illustrated by Figure 16 b) and is when the switch S_1 has been successfully turned off. This happens at time t_b. The time t_b depends on many factors. In particular the sensing and coordination scheme of the breaker will have a huge impact on this time. The delay time of the chosen switching element will also affect this. In addition to this the closed loop inductance may also extend this time in the case of using threshold current values to trigger the breaker. For example if the breaker is designed to break the current for any current larger than I_{thresh} it will initially take the current;

$$\Delta t_{thresh} = \frac{L_s[I_{thresh} - I_n]}{V_n} \tag{28}$$

seconds to reach this value. It will also be a time delay related to the sensing equipment t_{delay1} and turn-off delay in the switching element t_{delay2} adding up to the total delay time of t_b. This delay time will thus add on to the maximum fault current with;

$$\Delta I_{delay} = \frac{V_n t_b}{L_s} \tag{29}$$

This all adds up to,

$$t_b = t_{thresh} + t_{delay}, \quad I(t_b) = I_{thresh} + I_{delay} \tag{30}$$

Looking at figure 16 it can be seen that this is the same RLC circuit analyzed in section 2.6 with initial conditions $i(0) = I(t_b)$ and $v(0) = 0$.

Since R_f and L_1 are set and L_s already chosen, the only parameter to design is the capacitor C_{sn}.

As discussed in section 3, the switching element will have a limit associated with the rate of rise of the voltage $\frac{dv}{dt}$. Assuming that R_f is very small, the voltage over the switch S_1 can

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be assumed to be equal to the capacitor voltage v_c. Also assuming that the maximum current $I(t_b)$ is instantly commutated to the snubber capacitor, The maximum current that will flow through the capacitor v_c can be assumed to be $I(t_b)$. With this in mind the maximum rate of rise of the the voltage over the capacitor and thus over the S_1 can be expressed as;

$$\frac{dv_c}{dt}_{max} = \frac{I(t_b)}{C_{sn}} \tag{31}$$

Thus if the rate of voltage rise is a limiting factor, the capacitor C_{sn} should be designed according to;

$$C_{sn} = \frac{I(t_b)}{\dfrac{dv_c}{dt}_{max}} \tag{32}$$

Where $\dfrac{dv_c}{dt}_{max}$ is the maximum rate of change of the voltage allowed in the switching element.

The capacitor should thus be designed either according to the power limitation of the switching device, or the $\dfrac{dv_c}{dt}_{max}$ limitation.

3.3.5 Stage 3: Activation of MOV

Figure 16 d) shows the schematic diagram of the circuit when the MOV is activated. This happens when v_c reaches the MOVs clamping voltage V_{cl} at time t_{MOV}.

Since the rate of rise of the capacitor voltage v_c in stage 3 is already established, the time interval in stage 3 t_c can be approximated by;

$$\Delta t_c = \frac{C_{sn}V_{clamp}}{I(t_b)} \tag{33}$$

Asuuming that the rate of rise of voltage v_c stays linear during stage 3.

The time when the MOV clamping voltage V_{cl} is reached and the MOV starts to conduct is thus given by;

$$t_{MOV} = t_b + t_c \tag{34}$$

At this time the current through the inductor is $I(t_{MOV})$.

Using the same strategy for analyzing the circuit given in figure 16 d) as was performed in section 2.6, the following system of equations is obtained.

Using KVL and Kirchoffs current law (KCL) the circuit can be expressed as;

$$V_s = L\frac{di_L}{dt} + v_{MOV} \tag{35}$$

$$v_{MOV} = R_{sn}C\frac{dv_c}{dt} + v_c \tag{36}$$

$$i_L = \frac{v_{MOV}}{R_{MOV}} - \frac{V_{cl}}{R_{MOV}} \tag{37}$$

Where R_{MOV} is the effective resistance of the MOV when it is conducting after reaching its clamping voltage V_{cl}.

Taking the Laplace transform of (37) yields;

$$\frac{V_s}{s} = L[si_L - i_L(t_{MOV})] + v_m \tag{38}$$

$$v_m = R_{sn}Cv_c s - R_{sn}v_c(t_{MOV}) + v_c \tag{39}$$

$$i_L = \frac{v_m}{R_m} - \frac{V_c l}{R_m s} \tag{40}$$

Treating the initial conditions $i_L(t_{MOV}) = I_0$ and $v_c(t_{MOV}) = V_0$ as sources, and rewriting as $\mathbf{Ax} = \mathbf{b}$, where;

$$\mathbf{x} = \begin{bmatrix} i_L \\ v_{MOV} \\ v_c \end{bmatrix}, \quad \mathbf{b} = \begin{bmatrix} \dfrac{V_s}{s} + LI_0 \\ R_{sn}CV_0 \\ \dfrac{V_{cl}}{R_m s} \end{bmatrix}, \quad \mathbf{A} = \begin{bmatrix} Ls & 1 & 0 \\ 0 & -1 & R_{sn}Cs \\ -1 & \dfrac{1}{R_m} & 0 \end{bmatrix} \tag{41}$$

With the solution expressed as $\mathbf{x} = \mathbf{A}^{-1}\mathbf{b}$, system (57) becomes;

$$\mathbf{x} = \frac{\tau_L^{-1}}{s + \tau_L^{-1}} \begin{bmatrix} 0 & \tau_L I_0 & \dfrac{V_i}{R_m} - \dfrac{V_{cl}}{R_m} \\ 0 & LI_0 + \tau_L V_{cl} & V_i \\ \tau_L v_0 & v_0 + \dfrac{LI_0}{\tau_C} + \dfrac{\tau_L V_{cl}}{\tau_C} & \dfrac{V_i}{\tau_C} \end{bmatrix} \begin{bmatrix} s \\ 1 \\ \dfrac{1}{s} \end{bmatrix} \tag{42}$$

Where;

$$\tau_L = \frac{L}{R_m}, \quad \tau_C = R_{sn}C \tag{43}$$

This is a recognizable first order system. Looking at equation (42), it is interesting to note that the current as well as the voltage over the MOV and thus over the switch is independent of the snubber resistance R_{sn}. Since the clamping voltage V_{cl} is larger than then source voltage V_s, the current response during this stage can seen as the impulse response with magnitude I_0 minus the step response with magnitude $\frac{V_i - V_{cl}}{R_m}$ of a first order system with time constant τ_L.

This means that the time it will take the current to reach zero is a function of the time constant τ_L, the current at which the MOV is activated $i_L(t_{MOV})$ and the difference between the clamping voltage V_{cl} and the source voltage V_s.

The voltage seen by the switching device is the same as the voltage over the MOV v_{MOV}. As seen in equation (42), this voltage can be expressed as the sum between a step response of magnitude V_i, and the impulse response of magnitude $I_0 R_m + V_{cl}$. This means, although ambiguously that V_{cl} should always be bigger than V_i in order for the voltage v_{MOV} to decrease.

The peak voltage over the switching device can also in this case be seen to be $V_{cl} + I_0 R_{MOV}$, where I_0 is the peak current through the capacitor which occurs at at the same time as the voltage reaches V_i. Before this, the circuit is a regular series RLC circuit as analyzed in section 2.6. The initial current of stage 3 can thus be given by;

$$I_0 = \sqrt{I(t_b)^2 + \frac{C_s}{L_s} V_i} \tag{44}$$

Although having a large V_{cl} compared to the source voltage V_i can drastically reduce time it will take for the current to reach zero, it should be noted that that this means an increase in peak voltage as seen by the switching device. This again will lead to over dimensioning of the power semiconductor device used for the switching device. In some cases however, since the choice of semiconductor device may fall upon one with already higher rating than the nominal system voltage, this relationship can be used to minimize the breaking time.

In any case, the clamping voltage should be chosen according to the following constraint;

$$V_{cl} = V_{max} - R_{MOV} I_0 \tag{45}$$

where V_{max} is the maximum allowable voltage over the switching device S and I_0 is the worst case initial current at the time of MOV activation.

It should be noted that if R_{MOV} or I_0 is too high, $V_{cl} < V_i$ which is unacceptable. A proper choice of MOV that minimizes the static MOV resistnce R_m is therefore crucial. If the choice of MOV is unable to guarantee $V_i < V_{cl} \leq V_{max}$, based on its static resistance characteristics, L_s must be chosen such that;

$$V_{max} - R_{MOV} I_0 \geq V_n \tag{46}$$

Given L_s and C_s, the MOV resistance must be less than;

$$R_{MOV} \leq \frac{V_{max} - V_{cl}}{I_0} \tag{47}$$

Given the nature of MOVs, a device with an effective resistance satisfying equation (47) at least somewhere in the range $[V_n, V_{max}]$ should be chosen if possible.

As $L_s \rightarrow \inf$, the initial MOV current $I_0 \rightarrow I_{max}^S$, so an absolute maximum resistance in order to satisfy $v_{MOV} < V_{max}$ and $V_{cl} > V_i$ can be given by;

$$R_{MOV}^{max} = \frac{V_{max} - V_i}{I_{max}^S} \tag{48}$$

The MOV resistance must thus stay below this value in order for the breaker to function properly and for the constraints to be guaranteed.

Finally, the voltage over the capacitor v_c can also be seen in equation (42). The dynamics of this voltage during this stage is a rather unimportant and trivial relationship. The choice

of the snubber resistance R_{sn} plays a bigger role in the final stage of the breaking process to be discussed. It should be noted that it may be worthwhile to revisit this relationship to make sure that the rated limits of the capacitor itself are not violated.

In equation (42) it also becomes apparent that the fault current can reach high values peaking at I_0. Since a minimum capacitance is already designed and cannot be lowered, the only way to decrease this peak is to further increase the current limiting inductance L_s. If there exists a limit to the fault current, for example due to the protection of the power source, the requirement for the current limiting inductor would be;

$$L_s \geq C \frac{V_i^2}{{I_{max}^f}^2 - I(t_b)^2} \tag{49}$$

3.3.6 Stage 4: MOV deactivated

At this stage, the voltage over the MOV has dropped to its clamping voltage, V_{cl} and the MOV stops carrying current. Since $v_c > V_s$, the current through the capacitor will be in the opposite direction and flow through the snubber resistance R_{sn}. The system circuit can then be represented by the schematic circuit diagram seen in figure 16 c) again, only this time with resistance $R_f + R_{sn}$. Since this circuit has already been analyzed both in section 2.6 and previously in this section, the same results yields for this stage. Now, The addition of snubber resistance R_{sn} will decide the final stage of the response. It is obvious that the voltage over the switching device will approach V_s and the current i_L has already fallen to zero.

Revisiting equation (13) it can be seen that the voltage response is reduced to the sum of a step response of magnitude V_s, an impulse response of magnitude $\sqrt{\frac{C}{L}} R_s n V_{cl}$ and a zero-impulse response of magnitude V_{cl} of the second order system given by;

$$\omega_0 = \frac{1}{\sqrt{LC}}, \quad \zeta = \frac{R_{sn}}{2}\sqrt{\frac{C}{L}}, \quad \omega_d = \omega_0\sqrt{1-\zeta^2} \tag{50}$$

From equation (6), it can be seen that the current is reduced to the impulse response of the same second order system with magnitude $\frac{V_s - V_{cl}}{L}$.

From these relationships it becomes apparent that R_{sn} first of all decides the damping factor ζ and thus the main form of the response as well as ω_d. Secondly, the amplitude of the voltage, as well as the current is a strictly increasing function of V_{cl}. It should be noted that if R_{sn} is chosen to be critically-, or over damped, there will in practice be no ringing and thus no amplitudes to consider. If, on the other hand, R_{sn} is chosen so that the system is under damped, the will be ringing, causing the current through the capacitor to go positive. If the current through the capacitor is positive, the snubber resistance is shorted and the system will characterized in the same way as in stage 2. Thus during ringing, the characteristics of the system will alternate between the second order system given by (50) and (12).

Because the fault resistance R_f is difficult to estimate and may in some cases be very close to 0, the damping of of the system when the current is positive may be very small. To avoid unnecessary ringing, a good strategy for the design of the snubber resistance R_{sn} is to design

it so that the system is critically damped in the worst case. Since the loop inductance L may vary, from equation (50) it is obvious that the worst case, being when $L_1 = L_{tot}$ yields the lowest damping factor ζ. Following this strategy, the following design criteria will guarantee the final response to be critically- or over damped for all situations, eliminating all ringing;

$$R_{sn} = 2\sqrt{\frac{(L_s + L_{tot})}{C_{sn}}} \tag{51}$$

Where L_{tot} is the maximum line inductance that occurs when the fault is close to the load.

It should be noted however that the snubber resistance will also affect the voltage over the snubber diode D_{sn}. Since the voltage seen by this diode is equal to the voltage over the snubber resistance R_{sn} it is obvious that a lower value of R_{sn} will cause lower voltage handling requirements for this diode. Thus when designing the breaker, this relationship may also be considered. Further reducing R_{sn} from 51 will cause ringing and thus a trade-off between the degree of ringing in the system and the voltage requirements of the snubber diode exists.

3.3.7 Summary of Interrupting topology design

The following equations shows the design criteria of the passive elements based on the discussion in the previous paragraphs. These criteria is based on the maximum ratings of the switching device $\frac{di}{dt}_{max}$, $\frac{dv}{dt}_{max}$, I_{max}^S, P_{max} and V_{max} as well as the maximum allowable fault current I_{max}^f

$$L_s \geq \frac{V_n}{argmin[\frac{di}{dt}_{max}, \frac{I_{max} - I_n}{t_b}]}, \tag{52}$$

$$L_s \geq C \frac{V_n^2}{{I_{max}^f}^2 - I(t_b)^2}, (If\ I_{max}^f\ exists) \tag{53}$$

$$C_{sn} \geq argmax\left[\frac{I(t_b)}{\frac{dv_c}{dt}_{max}},\ \frac{2I(t_b)^2}{27P_{max}}t_{fall}\right], \tag{54}$$

$$R_{sn} = 2\sqrt{\frac{(L_s + L_{1,max})}{C_{sn}}} \tag{55}$$

$$V_{cl} = V_{max} - R_m I_0 \tag{56}$$

Table 19 sums up the considerations that should be taken when choosing the switching device, designing the driver and sensing circuitry as well as choosing the MOV with regard to achievable design goals.

The reduction of I_{max} and V_{max} is directly associated with the reduction of the power semiconductors voltage and current rating and thus directly associated with the reduction of price and weight. The reduction of LCR is also directly associated with the reduction of price and weight. Efficiency is indirectly associated with the reduction of both price and weight through the design of the heat sink and dissipation of electrical energy. The higher the efficiency

the smaller heat sink is required. Speed, on the other hand, while not associated with price or weight, it is an important design goal itself in order to provide survivability. It should however be noted that the breaker will be much faster than its mechanical counterpart.

Table 9: A table summarizing the relationship between choice of switching device and MOV as well as design of driver and sensor circuitry and achievable design goals. I_{max} is the maximum current through the switching device, V_{max} is the maximum voltage seen by the switching device, and RLC is the size of the passive elements L_s, C_{sn} and R_{sn}.

	Efficiency ↑	Speed ↑	I_{max} ↓	V_{max} ↓	LCR ↓	$I_{f,max}$ ↓
Switching device	$\min(R_{on})$ $\min(V_{on})$	$\min(t_{delay})$ $\min(t_{fall})$ $\max(\frac{di}{dt}_{max})$ $\max(\frac{dv}{dt}_{max})$ $\max(I_{rated})$	$\min(t_{delay})$	Only reduced by means of MOV	$\max(\frac{di}{dt}_{max})$ $\max(\frac{dv}{dt}_{max})$ $\max(I_{rated})$ $\min(t_{fall})$	$\min(t_{delay})$ $\max(\frac{di}{dt}_{max})$
Driver & sensor		$\min(t_{thresh})$	$\min(t_{thresh})$		$\min(t_{thresh})$	$\min(t_{thresh})$
MOV	$\min(R_{stray})$	$\min(R_{MOV})$ $\max(V_{cl} - V_i) > 0$	not reduced by means of MOV	$\min(V_{cl} - V_i) > 0$		$\min(V_{cl})$

3.4 Limiting Topology

a)

b)

c)   d)   e)
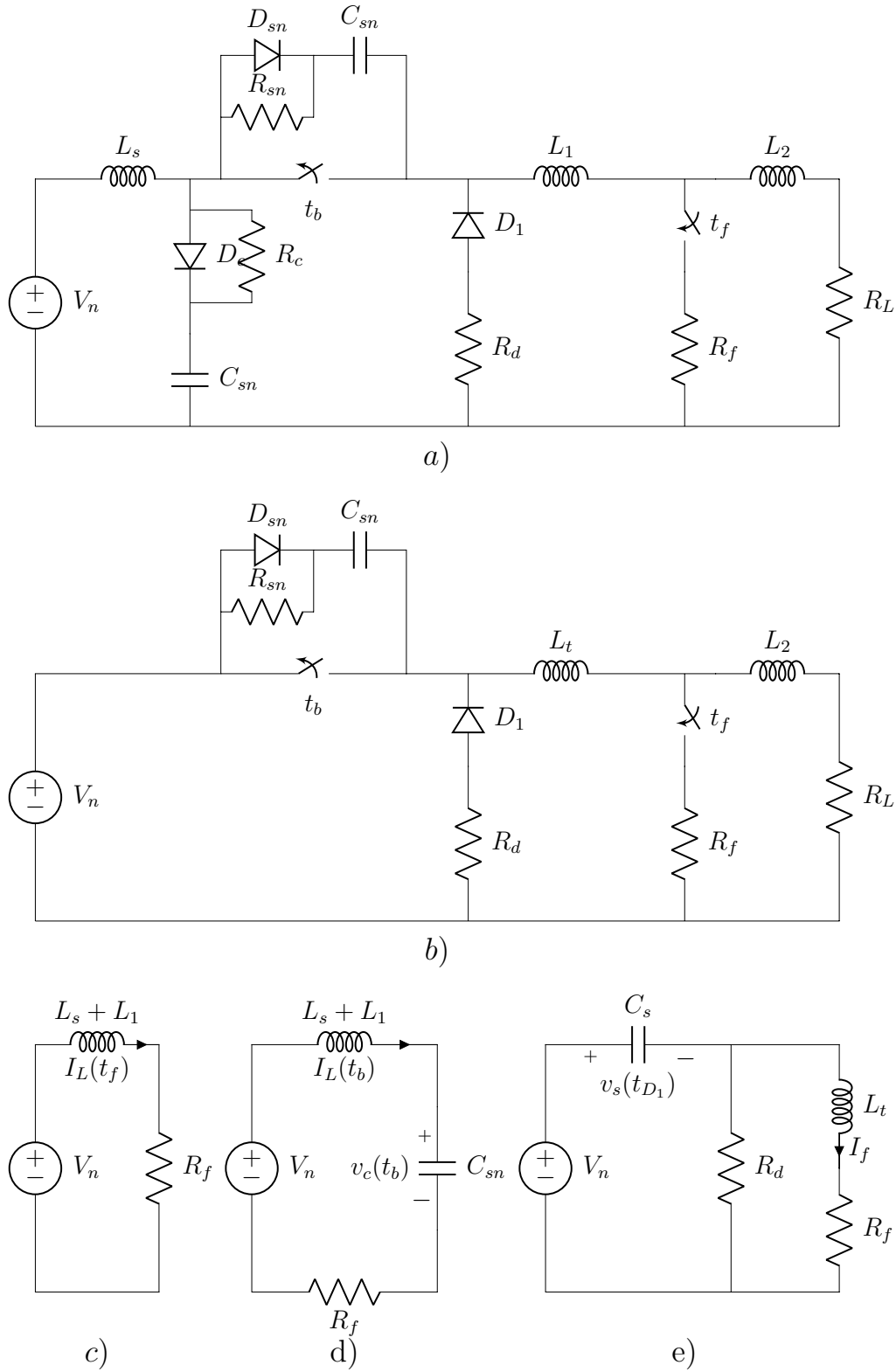
Figure 17: a) Schematic diagram the limiting DCCB implemented in the design system. b) Schematic diagram the limiting DCCB with current limiting inductor L_s moved to after the breaker and clamping capacitor emitted. c) Equivalent circuit after fault occurs at time t_f. d) Equivalent circuit after the switch opens at time t_b with resistance R_f. c) Equivalent circuit when D_1 starts conducting at time t_{D_1}.

3.4.1 Steady state

The steady state considerations for this topology will be exactly similar to that of the interrupting breaker. This is assuming that leakage current through diode D_1 as seen in figure 17 is negligible. In practice this leakage current may cause higher power losses during steady state conditions.

3.4.2 Phase one: occurrence of fault

Figure 17 a) illustrates the equivalent circuit for the original circuit. Assuming that R_s and R_f are negligible and using the same strategy to analyze the circuit as discussed in section 2.6, the following system is obtained when a fault occurs;

$$\mathbf{x} = \begin{bmatrix} v_c \\ i_{Ls} \\ i_f \end{bmatrix}, \quad \mathbf{b} = \begin{bmatrix} \dfrac{V_s}{s} + L_s I_0 + C R_{cl} V_0 \\ C V_0 \\ C R_{cl} V_0 - L_1 I_0 \end{bmatrix}, \quad \mathbf{A} = \begin{bmatrix} C R_{cl}s + 1 & L_1 s & 0 \\ Cs & -1 & 1 \\ C R_{cl}s + 1 & 0 & -L_2 s \end{bmatrix} \quad (57)$$

With the solution expressed as $\mathbf{x} = \mathbf{A}^{-1}\mathbf{b}$, system (57) becomes;

$$\mathbf{x} = \frac{\frac{\omega^2}{L_{tot}}}{d} \begin{bmatrix} C_{cl}L_s L_1 V_0 & L_{tot}C_{cl}R_{cl}V_0 & L_1 V_i & 0 \\ C_{cl}L_s L_1 I_0 & C_{cl}L_1(V_i - V_0) + L_{tot}C_{cl}R_{cl}I_0 & L_{tot}I_0 + C_{cl}R_{cl}V_i & V_i \\ C_{cl}L_s L_1 I_0 & C_{cl}L_s V_0 + L_{tot}C_{cl}R_{cl}I_0 & L_{tot}I_0 + C_{cl}R_{cl}V_i & V_i \end{bmatrix} \quad (58)$$

Further arranging yields;

$$\mathbf{x} = \frac{\omega^2}{d} \begin{bmatrix} \dfrac{1}{\omega^2}V_0 & \dfrac{1}{\omega}2\zeta V_0 & \dfrac{L_{eq}}{L_s}V_i & 0 \\ \dfrac{1}{\omega^2}I_0 & \dfrac{1}{\omega}[\dfrac{\sqrt{L_{eq}C_{cl}}}{L_1}(V_i - V_0) + 2\zeta I_0] & I_0 + \dfrac{C_{cl}R_{cl}}{L_{tot}}V_i & \dfrac{1}{L_{tot}}V_i \\ \dfrac{1}{\omega^2}I_0 & \dfrac{1}{\omega}[\dfrac{\sqrt{L_{eq}C_{cl}}}{L_1}V_0 + 2\zeta I_0] & I_0 + \dfrac{C_{cl}R_{cl}}{L_{tot}}V_i & \dfrac{1}{L_{tot}}V_i \end{bmatrix} \begin{bmatrix} s \\ 1 \\ \dfrac{1}{s} \\ \dfrac{1}{s^2} \end{bmatrix} \quad (59)$$

Where;

$$\omega = \frac{1}{\sqrt{L_{eq}C_{cl}}}, \qquad\qquad \zeta = \frac{R_{cl}}{2}\sqrt{\frac{C_{cl}}{L_{eq}}}, L_{eq} = \frac{L_s L_1}{L_{tot}}, \qquad (60)$$

$$d = s^2 + 2\zeta\omega s + \omega^2, \qquad\qquad L_{tot} = L_s + L_1 \qquad\qquad (61)$$

The main purpose of the design in this phase is to limit the fault current seen from the switching element. Looking at equation (59) it is obvious that the clamping capacitor C_{cl} is

contributing to several over current components. The clamping capacitor is however needed to limit the over voltages caused by the current limiting inductor.

In this design, the power flow is unidirectional and thus it would only make sense to place the breaker as close to the converter or power supply as possible. In fact, even with bi-directional topologies a breaker would need to be placed at both ends since a circuit breakers can only protect down stream systems.

With this in mind, the current limiting inductor can be placed immediately after the breaker in stead of in front. This will still yield the required current limiting effect during the first phase of the fault. At the same time, as will be seen, this will contribute to amplified current limiting ability if required. The inductance in front of the breaker will thus be reduced to a negligible stray inductance between the breaker and the power source. In this case the clamping capacitor loses its purpose and can be emitted.

The system is thus reduced the schematic diagram seen in figure 17 b). During the first stage when the fault has occurred, but the breaker has not yet initiated, the system is reduced to the schematic diagram seen in figure 17 c). This is a first order system similar to phase one of the interrupting topology in paragraph 3.3. The constraints on the current limiting inductor will thus be the same and given by;

$$L_s \geq \frac{V_n}{argmin[\frac{di}{dt}_{max}, \frac{I_{max}-I_n}{t_b}]}, \tag{62}$$

$$\tag{63}$$

3.4.3 Commutation phase

Since D_1 is turned off during the commutation, this phase will be similar to the commutation of the interrupting breaker and its schematic diagram can be seen in figure 17 d). Thus following the same steps as in section 3.3, the optimizing design criteria for the capacitor can be given as;

$$C_s \geq argmax \left[\frac{I(t_b)}{\frac{dv_c}{dt}_{max}}, \; \frac{2I(t_b)^2}{27P_{max}}t_{fall} \right] \tag{64}$$

$$\tag{65}$$

3.4.4 Phase two: activation of D_1

As soon as commutation is finished, the voltage over the switch has reached V_i. At this time t_D, the diode D_1 is no longer reversed biased and starts conducting. A schematic diagram of the circuit during this phase can be seen in figure 17 e).

Using the same technique for analyzing the circuit as described in section 2.6, the system can now be characterized by $\mathbf{Ax} = \mathbf{b}$;

$$
\mathbf{A} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & -1 & L_t s \\ -C_s s & \dfrac{1}{R_d} & 1 \end{bmatrix}, \quad \mathbf{b} = \begin{bmatrix} \dfrac{1}{s} V_i \\ I_f L_t \\ -C_s V_s \end{bmatrix}, \mathbf{x} = \begin{bmatrix} v_c \\ v_d \\ i_f \end{bmatrix} \tag{66}
$$

The solution can be expressed as $\mathbf{x} = \mathbf{A}^{-1}\mathbf{b}$;

$$
\mathbf{x} = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \begin{bmatrix} \dfrac{1}{\omega_0^2} V_s & \dfrac{L_t}{R_d} V_i + L_t I_f & V_i \\ \dfrac{1}{\omega_0^2}(V_i - V_s)^{\,0} & -I_f L_t & 0 \\ \dfrac{1}{\omega_0^2} I_f & \dfrac{L_t}{R_d} I_f + C_s(V_i - V_s)^{\,0} & 0 \end{bmatrix} \begin{bmatrix} s \\ 1 \\ \dfrac{1}{s} \end{bmatrix} \tag{67}
$$

where;

$$
\omega_0 = \frac{1}{\sqrt{C_s L_t}}, \quad \zeta = \frac{1}{2R_d}\sqrt{\frac{L_t}{C_s}}
$$

The term $(V_i - V_s)$ is zero beacause the diode D_1 starts conducting once the capacitor voltage v_s is equal to the nominal input voltage V_i. The initial condition of the capacitor voltage will thus be equal to the nominal input votage. To estimate the over voltage on the switch S_1, the assumption that the zero-impulse response of the voltage v_c in equation (67) has reached zero by the time the regular impulse response reaches its peak is made. This assumtion is based on the analyses of 2nd order systems in section 2.6. Following the analyses from section 2.6 it will also be assumed that the total peak voltage over S_1 will occur at the same time as the peak of the impulse response part in equation (67), $\dfrac{L_t}{R_d}V_i + L_t I_f$. This will cause a relatively small error since in reality, the total peak voltage will be shifted slightly due to the difference in steepness of the impulse and step part of the response.

The occurrence of the peak for the impulse response part can be given as;

$$
t_{max} = \frac{1}{\omega_d}\tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \tag{68}
$$

For the critically damped case, where $\zeta = 1$, the peak voltage over S_1 can be given as

$$
C_{max} = C_{impulse}^{crit}(t_{mas}) + C_{step}^{crit}(t_{max}) \tag{69}
$$

Inserting t_{OS} in to the solutions of the impulse and step response for the under damped case and adding them together as $\zeta \to 0$ yields;

42

$$V_{max} = \omega_0 K_1 \exp(-\frac{\omega_0}{e}) + K_2\big(1 - \exp(\frac{\omega_0}{e})(1 + \frac{\omega_0}{e})\big) \tag{70}$$

Glancing at equation 3.4.4 it is obvious that even for the critical case the over voltage over S_1 will be way to big for practical cases. It can thus be concluded that ζ must be designed to be over damped. The peak voltage in this case can be given by;

$$V_{max} = \omega_0 K_1 \exp(-\zeta\omega_0 t_{max}) + K_2(1 + \frac{\omega_0}{2\sqrt{\zeta^2 - 1}}\big(\frac{\exp(-s_1 t_{max})}{s_1} - \frac{\exp(-s_2 t_{max})}{s_2}\big) \tag{71}$$

where,

$$K_1 = \frac{V_i * L_t}{R_d} + I_f * L_t, \qquad\qquad K_2 = V_i$$
$$s_1 = \omega_0\big(\zeta + \sqrt{\zeta^2 - 1}\big), \qquad\qquad s_1 = \omega_0\big(\zeta - \sqrt{\zeta^2 - 1}\big)$$

The first term in equation (71) is the magnitude of the first peak of the impulse response occuring at time t_{OS}. The second term is the solution of the step response at t_{OS}.

For over damped second order systems, the overshoot will decrease with increasing ζ. The time to reach steady state will at the same time decrease. There will thus be a trade-off between the total breaking time of the breaker and the required blocking voltage of the switching elements.

The settling time of the system can be found table **??** in section 2.6 as;

$$\exp\big(-K * t\big) * \big(cosh(t) + K * sinh(t)\big) = 0.02 \rightarrow t_s^{2\%} \tag{72}$$

where;

$$K = \frac{E}{D}, \quad E = -\frac{s_1 + s_2}{2}, \quad D = -\frac{s_2 - s_1}{2}$$

Equations (71) and (72) cannot be solved explicitly in terms of R_d and t respectively. A numerical solution should thus be found.

In a design context a maximum voltage over the switch should be defined. This maximum voltage V_{max} depends solely on the chosen switching device and must be at least bigger than the system voltage V_i. From Equations (71) and (72), it is obvious that the higher voltage the switching device can withstand, the faster the current can be driven to zero. Since no explicit solution for the settling time is found, it is however not so obvious that there exists an optimal value of R_d that enables minimum voltage overshoot compared to the gain in settling time. Up to some value of R_d the settling time is reduced drastically compared to the increase in voltage overshoot. After this value, the voltage overshoot keep increasing while the decrease in settling time is minimal.
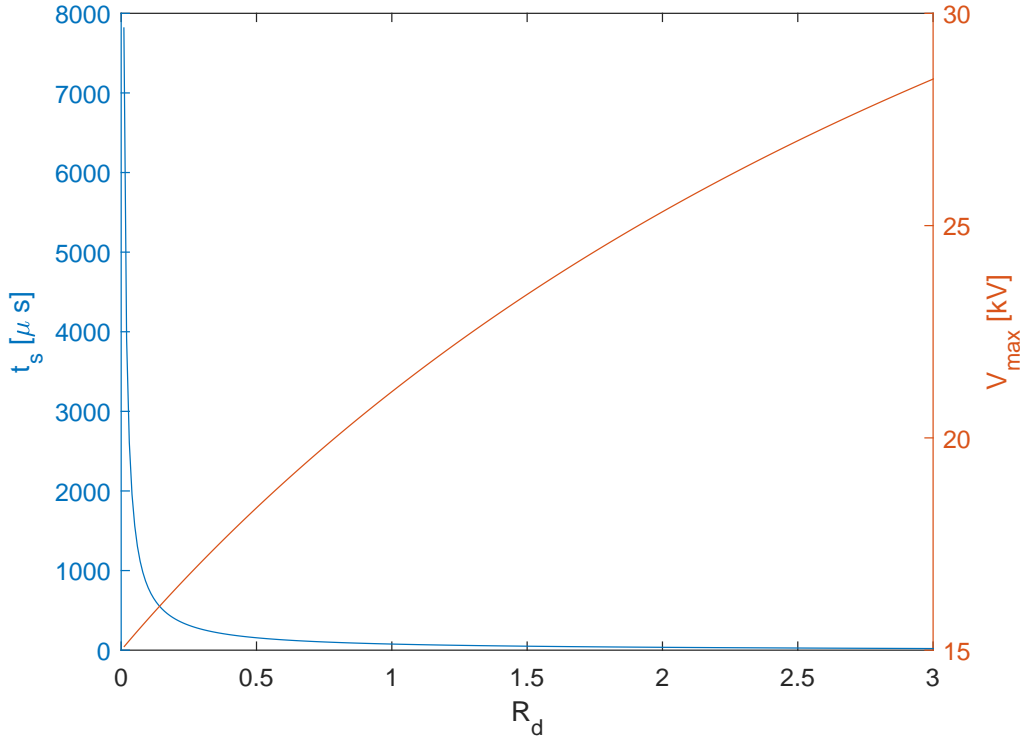
Figure 18: Design example to illustrate the trade-off between voltage overshoot and settling time as function of R_d. Variables used for the example: $V_i = 15\,\mathrm{kV}$, $V_s = 15\,\mathrm{kV}$, $I_f = 7670\,\mathrm{kA}$, $C_s = 0.5\,\mathrm{\mu F}$, $L_t = 20\,\mathrm{\mu H}$.

Figure 18 shows a design example to illustrate the trade-off between voltage overshoot and settling time. As seen in this figure, the dissipating resistance should be chosen low enough so that the maximum voltage over the switch, V_{max} is acceptable, but at the same time high enough so that the settling time does not grow unnecessarily long. It should also be noted that from equation (67) it can clearly be seen that since the amplitude of the impulse response part of the voltage v_s is linearly dependent on $L_f I_f = L_f I_{max}$, the peak voltage V_{max} will also be linearly dependent on the time of breaking t_b as seen from the design criteria of the current limiting inductor in paragraph 3.3.

It can also be seen from equation (67) that the response of the fault current i_f will be strictly decreasing. This is due to the fact that the amplitude of the zero-impulse part is bigger than the amplitude of the impulse part of the current response. This is assuming that $L_t < R_d$ which is a reasonable assumption based on the observations in this section. A more formal way of assuring this relationship can be seen from the following relationships.

$$i_f^{0i}(t_1) = i_{f,max}^{0i}, \quad i_f^{0i}(t_2) = 0 \frac{di_f^{0i}}{dt} < 0, \quad \frac{d^2 i_f^{0i}}{dt^2} > 0,$$

$$i_f^i(t_1) = 0, \quad i_f^i(t_2) = i_{f,max}^i, \quad \frac{di_f^i}{dt} > 0, \quad \frac{d^2 i_f^i}{dt^2} < 0$$

$$i_{f,max}^{0i} > i_{f,max}^i \rightarrow \frac{(i_{f,max}^{0i} + i_{f,max}^i)}{dt} < 0, \forall t \in [0, t_1]$$

It can thus be concluded that the maximum fault current is the same as the maximum current through S_1 used to design the current limiting inductor in phase one. This will thus also be dependent on breaking time t_b.

Another interesting observation is that since the system must be designed to be over damped, There will be no use for the snubber resistance R_s. The reason for this is that the current will never be negative in an over damped system and will thus never flow through this resistance.

3.4.5 Current limiting capabilities

As seen in figure 17 the limiting breaker looks very much like a buck converter only with a resistance in the freewheeling path. The inductor is the sum of the current limiting inductance and the maximum line inductance $L_t = L_s + L_{max}^{line}$. Given a proper control technique this may be utilized to actively control the current through the breaker.

The most obvious reason such a function would be beneficial is in the case of faults happening elsewhere in a multi-terminal system. This could still cause huge over currents to flow through the breaker and load even though there is no fault on this particular line. In many cases this would trip the breaker. By using its current limiting capabilities, the limiting breaker topology could still deliver power to the load and dissipate any excess energy in the dissipating resistance R_d instead of completely isolating the not faulty part as well.

3.4.6 Summary of limiting topology

The optimal values of the current limiting inductor and the snubber capacitor will be the same as for the interrupting topology. The snubber resistance will, on the other hand, be zero.

$$L_s \geq \frac{V_n}{argmin[\frac{di}{dt}_{max}, \frac{I_{max}-I_n}{t_b}]}, \tag{73}$$

$$C_{sn} \geq argmax\left[\frac{I(t_b)}{\frac{dv_c}{dt}_{max}}, \frac{2I(t_b)^2}{27P_{max}}t_{fall}\right], \tag{74}$$

$$R_{sn} = 0 \tag{75}$$

The dissipating resistance R_d must be optimized with regards to allowable maximum voltage over the switching device and the settling time of the system according to;

$$V_{max} = \omega_0 K_1 \exp(-\zeta\omega_0 t_{max}) \tag{76}$$

$$+ K_2(1 + \frac{\omega_0}{2\sqrt{\zeta^2 - 1}}(\frac{\exp(-s_1 t_{max})}{s_1} - \frac{\exp(-s_2 t_{max})}{s_2}) \tag{77}$$

$$t_s \leftarrow \exp\big(-K*t\big)*\big(cosh(t) + K*sinh(t)\big) = 0.02 \tag{78}$$

Table 10 shows a summary of the trade-off associated with the design goals. This table is very similar to table 19. The only differences are seen in the R_d row in table 10 as compared to the MOV row in table 19.

Table 10: A table summarizing the relationship between choice of switching device and dissipating resistance R_d as well as design of driver and sensor circuitry and achievable design goals. I_{max} is the maximum current through the switching device, V_{max} is the maximum voltage seen by the switching device, and LC is the size of the passive elements L_s, C_{sn}.

	Efficiency ↑	Speed ↑	I_{max} ↓	V_{max} ↓	LC ↓	$I_{f,max}$ ↓
Switching device	min(R_{on}) min(V_{on})	min(t_{delay}) min(t_{fall}) max($\frac{di}{dt}_{max}$) max($\frac{dv}{dt}_{max}$) max(I_{rated})	min(t_{delay})	Only reduced by means of R_d	max($\frac{di}{dt}_{max}$) max($\frac{dv}{dt}_{max}$) max(I_{rated}) min(t_{delay}) min(t_{fall})	min(t_{delay}) max($\frac{di}{dt}_{max}$)
Driver & sensor		min(t_{thresh})	min(t_{thresh})		min(t_{thresh})	min(t_{thresh})
R_d		max(R_d) < $R_d^{crit} ki$ max(V_{max})	Not reduced by means of R_d	min(R_d)		

3.5 Resistive topology

a)

b)   c) **Phase one**   d) **Phase two**

Figure 19: a) Schematic diagram the resistive DCCB implemented in the design system. b) Equivalent circuit after fault occurs at time t_f. c) Equivalent circuit after the main switches opens at time t_b. This phase is in this text referred to as phase one. d) Equivalent circuit when center switches are closed. This phase will be referred to as phase two.

3.5.1 Steady state

Steady state operation of the resistive topology will be similar to the the steady state operation of both the interrupting and limiting topologies. The only difference is that the nominal current I_n now splits equally between the two branches with switches S_1 and S_2. In each branch, there is also a diode, which is different from the other topologies.

The power dissipation in one branch is given by;

$$P_b = 2\left[\frac{I_n{}^2}{4}R_{on} + \frac{I_n}{2}V_{on} + \frac{I_n{}^2}{4}R_d\right] \tag{79}$$

$$= \frac{I_n{}^2}{2}R_{on} + I_n V_{on} + \frac{I_n{}^2}{2}R_d \tag{80}$$

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Where R_{on} is the on-state resistance of the switching device used for switches S_1 and S_2 and R_d is the on-state resistance of the diodes. V_{on} is not regarded in the case of the switching deivice being a unipolar device such as a MOSFET or JFET.

3.5.2 Stage 1: Occurrence of fault

Stage one is the exact same as for the interrupting and limiting topology only that the current through S_1 and S_2 will be half of that of the main switches in the other topologies. Assuming worst case scenario with $L_t = L_s$ ($L_1 = 0$), The maximum rate of change in the current through S_1 and S_2 can be given by

$$\frac{di}{dt}_{max} = \frac{V_n}{2L_s} \tag{81}$$

Thus the maximum current through switching devices S_1 and S_2 is;

$$\frac{I_n}{2} + \frac{V_n}{2L_s}t_b \tag{82}$$

As will be seen, the current through the center switches will be much higher. Thus the current limiting inductor L_s should be designed in order to limit the current through the center switches.

Equations (81) and (82) will however be useful in choosing the diodes and potentially de-rating S_1 and S_2 after designing the breaker.

3.5.3 Stage 1-2: commutation of S_1 and S_2

The commutation between stage one and two is similar to the interrupting and limiting topology. However, since this topology has two branches that split the current, the stress on the switching device will be reduced.

The maximum power dissipation in switches S_1 and S_2 can be given, following the same analysis as in section 3.3 as;

$$P_{max}^{S12} = \frac{2(I_{max}^S)^2}{27C}t_{fall} \tag{83}$$

And the following constraint on the capacitor can thus be given;

$$C = \frac{2(I_{max}^S)^2}{27P_{max}^{S12}}t_{fall} \tag{84}$$

3.5.4 Stage two and four: Phase one, main and center switches off

Following the same line of reasoning as in section 2.6, the circuit in figure 19 c) can be given by

$$\mathbf{x} = \frac{\omega_0^2}{s^2 + \omega_0^2} \begin{bmatrix} \dfrac{1}{\omega_0^2} V_0 & L I_0 & V_i \\ \dfrac{1}{\omega_0^2} I_0 & C(V_i - V_0) & 0 \end{bmatrix} \begin{bmatrix} s \\ 1 \\ \dfrac{1}{s} \end{bmatrix} \tag{85}$$

where;

$$\omega_0 = \frac{1}{\sqrt{L_t C}}, \quad R_f \approx 0$$

The fault resistance R_f is assumed to be zero.

3.5.5 Stage three: Phase two, center switches on

The circuit in figure 19 d) can be presented as $\mathbf{Ax} = \mathbf{b}$, where;

$$\mathbf{x} = \begin{bmatrix} i_L \\ v_c \end{bmatrix}, \quad \mathbf{b} = \begin{bmatrix} \dfrac{V_s}{s} + L I_0 \\ C V_0 \end{bmatrix}, \quad \mathbf{A} = \begin{bmatrix} 1 & Ls \\ Cs + \dfrac{1}{R_d} & -1 \end{bmatrix} \tag{86}$$

With the solution expressed as $\mathbf{x} = \mathbf{A}^{-1}\mathbf{b}$, system (86) becomes;

$$\mathbf{x} = \frac{\omega_0^2}{s^2 + 2\omega_0\zeta s + \omega_0^2} \begin{bmatrix} \dfrac{1}{\omega_0^2} V_0 & L I_0 & V_i \\ \dfrac{1}{\omega_0^2} I_0 & C(V_i - V_0) + \dfrac{L}{R_d} I_0 & \dfrac{V_i}{R} \end{bmatrix} \begin{bmatrix} s \\ 1 \\ \dfrac{1}{s} \end{bmatrix} \tag{87}$$

where;

$$\omega_0 = \frac{1}{\sqrt{L_t C}}, \quad \zeta = \frac{1}{2R_d}\sqrt{\frac{L}{C}}, \quad R_f \approx 0$$

3.5.6 Switching between phase one and two

From section 2.6, the maximum value of the voltage over the capacitor and thus over switches S_1 and S_2 during phase one can be found to be;

$$v_c = V_0^1 \cos\left(\omega t\right) + \sqrt{\frac{L}{C}} I_0 \sin\left(\omega t\right) + V_i\big[1 + \cos\left(\omega t - \pi\right)\big] \tag{88}$$

Differentiating term (88) and putting it equal to zero yields the time of the peak voltages of phase one;

$$t_{peak}^1 = \frac{1}{\omega_0} \tan^{-1}\left[\frac{\sqrt{\frac{L}{C}}I_0}{V_0 - V_i}\right] + n\frac{\pi}{2\omega_0} \tag{89}$$

After the fault has been sensed, the fault current has already reached a high value and the initial current I_0 can thus be assumed to be relatively big. From the impulse part of the voltage response in system (86) it is thus easy to see that if the breaker stays in this phase, the over voltage due to the initial current will reach unacceptable values. It can thus be concluded that a switching to phase two should be performed at least once before final turn-off is initiated. Furthermore, from the term in equation (88), it is obvious that the lowest peak will occur when $V_0^1 = V_i$. As will be seen this is also the point where the current during phase two is at it lowest, thus also minimizing I_0^1, so switching from phase two to phase one so that $V_0^1 = V_i$ makes sense in every way.

Thus assuming that the final turn-off occurs after switching from phase two at least once and that the initial voltage V_0^1 is equal to the source voltage V_i from reasons to be discussed. This assumption leads to a considerable simplification of (88) when (89) is inserted and the maximum voltage can be expressed as;

$$V_{max}^1 = V_i \cos\left(\frac{\pi}{2}\right) + \sqrt{\frac{L}{C}}I_0 \sin\left(\frac{\pi}{2}\right) + V_i\left[1 + \cos\left(\frac{\pi}{2} - \pi\right)\right] = V_i + \sqrt{\frac{L}{C}}I_0^1 \tag{90}$$

The maximum current during phase one will occur at $v_c^2 = V_i$ and is;

$$I_{max}^1 = \sqrt{I_0^{1^2} + \frac{C}{L}V_i^2} \tag{91}$$

During phase two, given an under damped system, the sum of the solutions of the impulse with zero response part and the step response part, excluding the impulse response is;

$$V_i - \exp\left(-\zeta\omega_0 t\right)\left[V_i \cos(\omega_d t) + V_i\frac{\zeta}{\sqrt{1 - \zeta^2}} \sin(\omega_d t) - V_0 \cos(\omega_d t) + \frac{\zeta}{\sqrt{1 - \zeta^2}}V_0 \sin(\omega_d t)\right]$$

$$\tag{92}$$

The term in 3.5.6 is again minimized when $V_0 = V_i$ where the impulse with zero cancels out the peak of the step response. From (91), the initial current of phase two must thus be I_{max}^1 and the voltage peak of phase two will be given by;

$$V_{max}^2 = V_i - 2\frac{\zeta \exp\left(-\zeta\omega_0 t_{max}\right)}{\sqrt{1 - \zeta^2}} \sin(\omega_d t_{max}) + V_{impulse}^{max} \tag{93}$$

$$= V_i - 2\frac{\zeta \exp\left(-\zeta\omega_0 t_{max}\right)}{\sqrt{1 - \zeta^2}} \sin(\omega_d t_{max}) + LI_0^2\omega_0 \exp\left(-\zeta\omega_0 t_{max}\right) \tag{94}$$

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where;

$$t_{max} = \frac{1}{\omega_d} \tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right), \quad I_0^2 = I_{max}^1 = \sqrt{I_0^{1^2} + \frac{C}{L}V_i^2}, \quad I_0^1 = I_n + \frac{V_n}{L}t_b$$

The current during phase two, given an under damped system is;

$$i^2 = i_{0-impulse}^2 + i_{impulse}^2 + i_{step}^2 \tag{95}$$

The minima of this current will occur at $v_c^2 = V_i$ at $t = \dfrac{\pi}{\omega_d}$, simplifying equation (95) to;

$$I_{min}^2 = -I_0^2 \exp\left(-\zeta\frac{\pi}{\sqrt{1-\zeta^2}}\right) + \frac{V_i}{R_d}\left[1 + \exp\left(-\zeta\frac{\pi}{\sqrt{1-\zeta^2}}\right)\right]; \tag{96}$$

This current will be the initial current after switching back to phase one again.

It is now obvious that the voltage over the capacitor and thus over the switching devices can be controlled by means of switching on and off the center switches. In order for both the fault current to be driven to zero and the voltage to be driven back to the nominal voltage V_i, the system must return to phase one. While there are probably many ways of designing the switching sequence in order for this to happen, two strategies will in this text be discussed.

Strategy one   Strategy one will minimize the breaking time by utilizing phase two only once before breaking the current during phase two. An important observation is that given I_{max}^1 and I_{min}^2, the rate of change of V_{max}^2 and V_{max}^1 with regards to L is negative and positive definite respectively for all $L > L_{min}$ given that the system is under damped. L_{min} is the minimum inductance, being the inductance seen by the circuit when the fault occurs close to the breaker.

$$\frac{V_{max}^1(L)}{dL} > 0, \frac{V_{max}^2(L)}{dL} < 0, \forall L \in [L_{min}, L_{max}] \mid \zeta \leq 1 \tag{97}$$

Since the voltage seen by switching devices S_1 and S_2 is V_{max}^1 during phase one and V_{max}^2 during phase two, it makes sense that the dissipative resistance R_d should be chosen so that $V_{max}^1(L_{max}) = V_{max}^2(L_{min})$. The resistance R_d will thus be chosen so that for some $L_{min} \leq L \leq L_{max}$, the maximum voltages V_{max}^1 and V_{max}^2 is equal and less than both end ranges $V_{max}^1(L_{max})$ and $V_{max}^2(L_{min})$. An upper bound for the maximum voltage as seen by the switching devices can thus be guaranteed to be $V_{max}^1(L_{max}) = V_{max}^2(L_{min})$.

This way the potential of each stage is taken advantage of and an upper bound for the voltage seen by the switching elements is guaranteed and minimized.

Following this, the optimal resistance R_d guaranteeing the lowest voltage peak is found by solving equation (109) in terms of R_d;

$$R_d \leftarrow V_{max}^1(L_{max}) = V_{max}^1(L_{min}) \tag{98}$$

Using this strategy, the current will be turned off during stage four. Due to the diodes seen in figure 19 the voltage will stay at V_{max}^2 and the energy stored in the capacitor during stage four will stay stored until the breaking action is terminated with a last switching to phase one where the voltage will be driven to nominal values.

Strategy two Strategy two will minimize the voltage overshoot by switching between stage three and four in order to dissipate all energy stored in the capacitor. In order to dissipate the energy stored in the capacitor at the same time as driving the current to zero, a switching sequence between phase one and two can be performed. If the switching from phase two back to phase one is performed at some threshold $V_{Thresh} > V_i$, the current will decrease until the voltage over the capacitor reaches V_i. Then switching back to åhase two at V_i and then back to phase one at V_{Thresh}. The following relationship will hold;

$$\frac{di_c^1}{dt} \leq 0, \frac{di_c^2}{dt} \leq 0 \ \forall \ t \mid v_c \geq V_i \tag{99}$$

$$\frac{dv_c^1}{dt} \geq 0, \frac{dv_c^2}{dt} \leq 0 \ \forall \ t \mid V_i \leq v_c \leq V_{max}^1 \tag{100}$$

Using this strategy, as long as $V_{thresh} > V_i$ the current can be guaranteed to go to zero. The maximum voltage overshoot can be limited to V_{max}^2 which can be designed by choosing R_d. If some maximum allowable overshoot $V_{thresh} > V_i$ is decided upon, for example based on the maximum ratings of the switching devices, equation 88 can be but equal to V_{thresh} in order to find the resistance R_d that limits the voltage overshoot to this maximum value. Then during phase two, switching back to phase one should be performed at this maximum voltage in order to utilize the switching devices capacity to its maximum and limit the total breaking time. Obviously, the lower this maximum allowable voltage overshoot is, the lower the resistance gets and the more dampened the system gets. It is thus a clear trade-off between total breaking time and maximum voltage overshoot. The designer should keep this in mind when choosing the switching devices and thus the V_{max}. A good strategy to minimize the total breaking time would be to design the resistance R_d so that the system is critically damped for the case when the fault occurs furthest away from the breaker and the inductance is L_{max}. That is if the voltage overshoot in the case when the fault occurs close to the breaker with L_{min} is acceptable.

The final choice on the value of resistance should thus be;

$$R_d \leftarrow V_{max}^2 = V_{thresh}, \ R_d < R_{crit} = \frac{1}{2}\sqrt{\frac{L_{min}}{C}}, \ V_{thresh} > V_i \tag{101}$$

With this strategy, the practical implementation of the switching control is a hysteresis band controller with bounds $[V_{max}, V_i]$. The center switches S_{C1} and S_{C2} turn on when $v_c = V_{max}$ and off when $v_c = V_i$ to guarantee a decreasing current as stated by equation (100).

The first switching from phase one to phase two must however happen at i_{max}^1, occurring at $v_c = V_i$ to guarantee a strictly decreasing fault current. Since with $v_c = V_i$ the design of R_d guarantees a voltage peak lower than V_{max} during phase two, the breaker should stay in this phase until $v_c = V_i$ again. At this point the fault current is I_{min}^2 and the center switches should thus be switched in order for the the current not to start increasing.

This first switching sequence can be implemented by identifying the peak of the current during phase one and turning on the center switches once the peak is reached. Since the current is already guaranteed to be strictly decreasing after this, this condition will not interfere with the voltage hysteresis control. The first voltage peak will thus be guaranteed to be lower than V_{max}.

If online parameter identification is possible, for example using adaptive control schemes, the total breaking time can be minimized by assuring that the first voltage peak always reaches V_{max}. In this case the first switching sequence from phase one to phase two occurs at the current I_0^2 at which phase two peaks at $V_{max}^2 = V_{max}$ according to equation (94).

Table 11 sums up the the important relationships in each stage of the turn of sequence for both strategy one and two.

<div align="center">Table 11</div>

	I_0	V_0 Strategy 1 / 2	$v(t_{switch})$ Strategy 1 / 2	$i(t_{switch})$	v_{max}
stage 1	I_n	0 / 0	0 / 0	$I_b = I_n + \dfrac{V_i}{L}t_b$	0
stage 2 (phase one)	$I_0^1 = I_b$	0 / 0	V_i / V_i	$I_{max}^1 = \sqrt{I_0^{2^2} + \dfrac{C}{L}V_i^2}$	V_i
stage 3 (phase two)	$I_0^2 = I_{max}^1$	V_i / V_i	V_i / V_{max}^2	$\begin{aligned} I_{min}^2 &= -I_{max}^1 \exp\left(-\zeta\dfrac{\pi}{\sqrt{1-\zeta^2}}\right) \\ &+ \dfrac{V_i}{R}\left[1 + \exp\left(-\zeta\dfrac{\pi}{\sqrt{1-\zeta^2}}\right)\right]\end{aligned}$	$\begin{aligned} V_{max}^2 &= V_i - 2\dfrac{\zeta\exp\left(-\zeta\omega_0 t_{max}\right)}{\sqrt{1-\zeta^2}}\sin(\omega_d t_{max}) \\ &+ LI_{max}^1\omega_0\exp\left(-\zeta\omega_0 t_{max}\right)\end{aligned}$
stage 4 (phase two)	$I_0^1 = I_{min}^2$	V_i / V_{max}^2	V_i / V_i	—	$V_i + \sqrt{\dfrac{L}{C}}I_{min}^2$

3.5.7 Limiting the current through the center switches

As seen in figure 19, the center switch S_{C1} will be subject to the highest current and the current through S_{C2} will always satisfy $i^{C2} < i^{C1}$.

The maximum current through center switch S_{C1} can be given by;

$$I_{max}^{C1} = \frac{V_{max}}{R_d} \tag{102}$$

Thus if I_{max}^{C1} breaches the ratings of the chosen power semiconductor device with the constraints on L_s based on the limits of switches S_1 and S_2, a new strategy of choosing the dissipative resistance and current limiting inductor must be developed.

If this is the case, in order to guarantee that I_{max}^{C1} is lower than some maximum rating I_{thresh}, the dissipative resistance is chosen to be;

$$R_d > \frac{V_{thresh}}{I_{thresh}} \tag{103}$$

Then in order to guarantee that the voltage over the capaciotor and thus the voltage over switches S_1, S_2 and S_{C1} is lower than the maximum voltage rating V_{thresh}, equation (94) must be solved in therms of L_s;

$$L_s \leftarrow V_{max}^2 = V_{thresh} \tag{104}$$

Following these constraint, the current and voltage over switch S_{C1} will be guaranteed to to be lower than its rated values.

3.5.8 Limiting the fault current seen by the source

Since the fault current i_f is reflected back to the source, there may be a maximum allowed fault current in order to protect the power source specifically freewheeling diodes in the power source. This maximum current is given by (91) and can only be limited by decreasing the size of capacitor C or increasing the current limiting inductance L_s. Since a minimum capacitor value is already found from the power rating of the switching device, the only option left is further increasing the inductor. Thus based on equation (91) if such a maximum fault current limit exists the current limiting inductor should be design according to;

$$L_s > \frac{CV_i^2}{{I_{max}^f}^2 - {I_0^1}^2} \tag{105}$$

3.5.9 Summary of resistive topology

The optimal values of the current limiting inductor and the capacitor will be the same as for the interrupting topology bacause the first two stages is essentially the same.

$$L_s \geq \frac{V_n}{argmin[\frac{di}{dt}_{max}, \frac{I_{max} - \frac{I_n}{2}}{2t_b}]}, \tag{106}$$

$$C \geq argmax\left[\frac{I(t_b)}{\frac{dv_c}{dt}_{max}}, \frac{2I(t_b)^2}{27P_{max}}t_{fall}\right], \tag{107}$$

$$\tag{108}$$

The dissipating resistance R_d must be optimized either with regard to minimized breaking time using strategy one;

$$R_d \leftarrow V_{max}^1(L_{max}) = V_{max}^1(L_{min}) \tag{109}$$

Or with regard to maximum allowed over voltage using strategy two;

$$R_d \leftarrow V_{max}^2 = V_{thresh}, \ R_d < (R_{crit} \mid L_{max}) \tag{110}$$

Table 12 shows a summary of the trade-off associated with the design goals. The table is very similar to table 10.

Table 12: A table summarizing the relationship between choice of switching device and dissipating resistance R_d as well as design of driver and sensor circuitry and achievable design goals. I_{max} is the maximum current through the switching devices, V_{max} is the maximum voltage seen by the switching devices, and LC is the size of the passive elements L_s, C_{sn}.

	Efficiency ↑	Speed ↑	I_{max} ↓	V_{max} ↓	LC ↓	$I_{f,max}$ ↓
Switching device	$\min(R_{on})$ $\min(V_{on})$	$\min(t_{delay})$ $\min(t_{fall})$ $\max(\frac{di}{dt}_{max})$ $\max(\frac{dv}{dt}_{max})$ $\max(I_{rated})$	$\min(t_{delay})$	Only reduced by means of R_d	$\max(\frac{di}{dt}_{max})$ $\max(\frac{dv}{dt}_{max})$ $\max(I_{rated})$ $\min(t_{delay})$ t_{fall}	$\min(t_{delay})$ $\max(\frac{di}{dt}_{max})$
Driver & sensor		$\min(t_{thresh})$	$\min(t_{thresh})$		$\min(t_{thresh})$	$\min(t_{thresh})$
R_d		$\max(R_d) < R_d^{crit}ki$ $\max(V_{max})$	Not reduced by means of R_d	$\min(R_d)$		

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4 Simulations

4.1 The simulated MVDC system

The system to be simulated will be the one shown in figure 15 and discussed in section 3. The parameters used for these simulations is shown in Table 13.

Table 13: Table of parameters used for the MVDC system to be simulated.

V_N[kV]	I_N[kA]	R_L [Ω]	L_{tot} [µH]	P_N[kW]
15	1.5	10	100	22.5

4.2 General simulation considerations

In literature, the few comparisons done between different solid state breaker topologies have been failing to produce comparable results. It is crucial that when comparing topologies the circumstances and design goals are in line with each other. In addition to this it is very important that each breaker is designed and optimized for the same conditions. In section 3, a design strategy for each breaker topology was found and parameters that improve its effectiveness identified. In order to properly compare them the following will be considered;

1. Available power electronic components will be used in order to guarantee that each breaker type is realizable. The same switching devices will be used for simulating all topologies to make them comparable.

2. The topologies will be designed according to the same set of design goals and constraints. In particular they will be optimized with regard to a set of constraints (V_{max}, I_{max}^f, I_{max}^S, P_{max}) related to the limits of the switching device and power source.

3. The improvement of the breakers effectiveness will be investigated by re-optimizing for the change in parameters that affect the design. The change in these parameters will be the same for all breaker types so that the improvements are also comparable. These changes in parameters include the reduction of the breaking delay time t_b, the increase of maximum allowable voltage V_{max}, the increase of allowable current through the switching device I_{max}^S and maximum allowable fault current I_{max}^f as well as improved power handling capabilities P_{max}. While most of these improvements are achieved through choosing a better power electric device, the reduction of breaking delay time is also achieved through improvement of sensing equipment. The specific design and dimensioning of the passive devices will not be considered. They will be assumed to be realizable and comparable by size.

   In an attempt to generalize the results achieved in this paper the breaker topologies will not be simulated for a series of different power electric devices. This would make it difficult to identify and isolate the parameters that improve the breakers and the degree to which each topology is improved by such isolated parameter changes.

   The strategy for the simulations to be performed will consist of the following;

1. A common commercially available and suitable power electronic device will be chosen for the switching device for all the topologies. This choice together with the system to be considered will cover the base case of the simulations.

2. V_{max} will be increased to emulate an improvement in the blocking voltage of the power electronic device or over dimensioning by series connections.

3. An increase of I_{max}^S will emulate the improvement of the maximum current rating of the power electronic device or over dimension by parallel connections.

4. A decrease in breaking delay time t_b will emulate the improvement of the power electric device turn-off delay time or the improvement in sensing and coordination equipment related to the breaker.

5. A reduction of snubber capacitor will emulate the increase of maximum power rating or a reduction in the falling time of the power electronic device.

6. The power source will be taken into consideration by investigating the current reflected back to the source. This current will contain information of how the freewheeling diodes of the the source must be designed.

7. The location of the fault will be considered by simulation of different ralationships between L_1 and L_2 as described in section 3.

8. A case using commercially available SiC devices will be constructed and simulated to investigate what the future of such devices may hold with regard to the application of MVDC solid state circuit breakers.

The results following these simulations will then be compared and analyzed based on the following properties;

1. Required size of passive components.

2. Total breaking time t_{tot}.

3. Maximum fault current reflected to the source I_{max}^{source}.

4. Required rating of diodes used in the topology.

5. Other Topology specific traits will also be discussed.

4.2.1 The base case

For the base case, the IGBT summarized by table 14 will be used.

In order to reach a blocking voltage higher than $V_n = 15\,\text{kV}$, at least 4 of these devices must be series connected reaching a blocking voltage of $18\,\text{kV}$. The maximum current rating is based on the peak collector current of the IGBT. In order to limit the number of parallel connected devices, this value will also be used as the maximum allowable current through the switching devices of all topologies I_{max}^S.

Table 14: Table of relevant characteristics of the IGBT used for the base case. Values are given by data sheet [?].

Model	referred to as	V_B[kV]	I_{max}[kA]	$\frac{dv}{dt}{}_{max}[\frac{kV}{s}]$	$\frac{di}{dt}{}_{max}[\frac{kA}{s}]$	I^2t [A²s]	t_{fall}[µs]	t_{delay}[µs]	P_{max}[kW]
ABB 5SNA 3000K452300 StakPak IGBT Module	IGBT 1	4.5	6	-	-		0.75	5.13	31.2

The base case will also assume an additional turn-off delay time of 5 µs for the delay in sensing and coordination equipment. This value is based on the findings of [1] summed up in table 3 in section 2.3.

Due to the series connection of IGBTs, the effective maximum power rating P_{max} will be four times higher than the rating given by the datasheet of a single IGBT. The relevant parameters in the base case will thus be given as seen in table 15.

Table 15: Relevant characteristics of the simulation base case.

Device	Series connections	Parallel connections	Tot. number of devices	V_{max}[kV]	I_{max}[kA]	t_{delay}[µs]	P_{max}[kW]
IGBT1	4	1	4	18	6	10.13	124.8

4.2.2 The SiC case

A commercially available SiC switching device will be chosen for the simulations in this case. This is to illustrate how the breaker topologies perform with a completely different switching device as well as investigating SiC devices feasibility in this application.

The chosen device and its characteristics can be seen in table 16. This device is to the authors knowledge the commercially available SiC MOSFET with the highest voltage rating.

Table 16: Table of relevant characteristics of the SiC MOSFET used for the SiC case. Values are given by data sheet [51] and rate of change values from [?].

Model	referred to as	V_B[kV]	I_{max}[kA]	I_D[kA]	$\frac{dv}{dt}{}_{max}[\frac{kV}{µs}]$	$\frac{di}{dt}{}_{max}[\frac{kA}{µs}]$	I^2t [A²s]	t_{fall}[µs]	t_{delay}[µs]	P_{max}[kW]	R_{on}/V_{on}[mΩ/V]
Cree C2M0045170D Silicon Carbide MOSFET	SiC MOSFET	1.7	0.16	0.078	19.5	11	-	0.018	0.048	0.52	25/-

In order to comply with the system ratings a total of 21 parallel strings each with 10 series connected SiC MOSFETS is needed to achieve a current rating of I_n and a blocking voltage higher than V_n as described in section 3. While 9 series connected devices would suffice to achieve a blocking voltage of V_n, one more device is added to provide some slack for over voltages for seasons to become apparent. This adds up to a total of 210 discrete MOSFET devices. According to data sheet [51], the device is easily connected in parallel to achieve higher drain source current or in series to achieve higher blocking voltages.

The reason why SiC MOSFETs is more easily parallel connected is that its on-resistance has a positive thermal coefficient and a narrow part-to-part parameter distribution [52].

Connecting this many devices in series and parallel may however seem unlikely to yield good current and voltage sharing properties. MOSFETs are also infamously known for their poor voltage sharing properties. In [53] two 1.7 kV SiC MOSFETS is successfully series connected using a series of RC-snubber circuitry for dynamic voltage sharing suppressing the voltage difference to a high degree. The snubber capacitors are in the nF range and is unlikely to interfere with the snubber circuitry of the circuit breakers themselves having snubber capacitors in the range of µF as will be seen in section 4. This technique however seems unlikely to successfully connect 10 devices in series without causing serious voltage difference.

Nevertheless, assuming that this many devices can be successfully connected, table 17 shows the total characteristics of the equivalent switching device.

Table 17: Relevant characteristics of the simulation base case.

Device	Series connections	Parallel connections	Tot. number of devices	V_{max}[kV]	I_{max}[kA]	I_D[kA]	t_{delay}[µs]	P_{max}[kW]	R_{on}/V_{on}[mΩ/V]	P_{on}[W]/[%]
SiC MOSFET	10	21	210	17	3.36	1.512	5.048	109.2	11.9/-	17.85/0.0076%

4.3 Simulation of Interrupting topology

Figure 20 shows the Simulink block diagram of the int4errupting topology which is to be simulate. As can be seen, the MOV is approximated by a diode with forward voltage V_{cl} and an on-state resistance of R_{MOV}. The snubber diode will have maximum current equal to the maximum fault current I_{max}^f and its voltage characteristics will be shown in the simulation results.
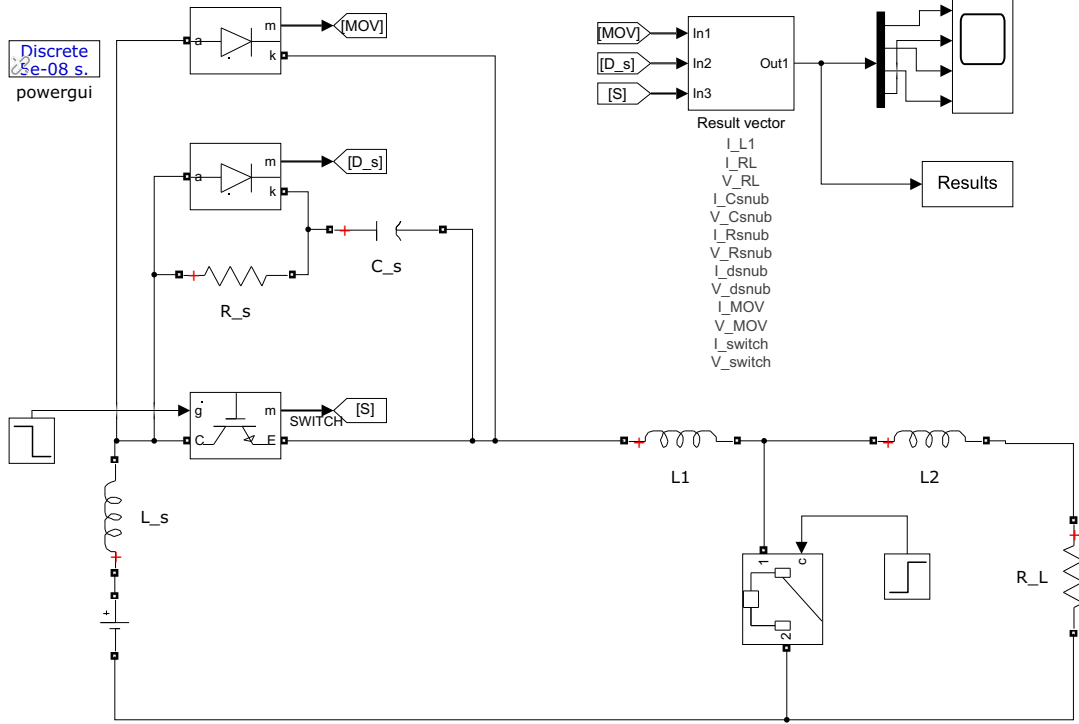
Figure 20: Simulink block diagram for simulation of the interrupting topology

4.3.1 The base case

As discussed in section 3, In order for the MOV to be able to suppress a specified over voltage, its effective resistance must be lower than

$$\lim_{L_s \to \infty} R_m^{max} = \frac{V_{max} - V_c}{I_n} = 1.33\,\Omega \tag{111}$$

This is however unrealistic and the expected maximum MOV resistance will be lower than this due to limits on the current limiting inductance.

Based on all performed simulations, in order to stay within current constraints of the IGBT, the current limiting inductance will be in the range of $10^1 - 10^2\,\mu\text{H}$. In order to stay within the power constraints on the other hand, the snubber capacitance must be in the range of $10^0\,\mu\text{F}$, the initial MOV current can thus be expected to be;

$$I_0 = \sqrt{{I_{max}^S}^2 + \frac{C_s}{L_s}{V_n}^2} = \sqrt{[I_n + \frac{V_n}{L_s}t_b]^2 + \frac{C_s}{L_s}{V_n}^2} \approx 3\,\mathrm{kA} = 2I_n$$

A more realistic estimation of the maximum MOV resistance is thus;

$$\lim_{L_s \to \infty} R_m^{max} = \frac{V_{max} - V_c}{I_n} = 0.66\,\Omega \tag{112}$$

Assuming an even worse with $C_s = 10\,\mu\mathrm{F}$ and $L_s = 10\,\mu\mathrm{H}$ would yield a maximum MOV resistance of $R_m = 0.11\,\Omega$. In order to assume the base case with good margin, the MOV resistance will thus be assumed to be $R_m = 0.1\,\Omega$ which is lower than the maximum allowable MOV resistance. This low MOV resistance will emulate an improvement in the MOV devices or maybe the use of future SiC transient voltage suppressors (TVS). In fact, it may even be attainable through multiple parallel and series connections of suitable MOV devices. The specification of MOV design will be considered in section 4.3.2. Furthermore, if SiC TVS diodes could be used, R_m would possibly be reduced by more than two orders of magnitude and its I-V characteristics much more linear [54].

Since the MOV resistance is lower than its maximum allowable value, the regular design process as described in section 3 will be used to decide L_s, C_s and R_s. Figure 21-25 shows the simulation results of the base case with its respective improvements. An explanation of these simulations will be summed up in section 4.3.4.
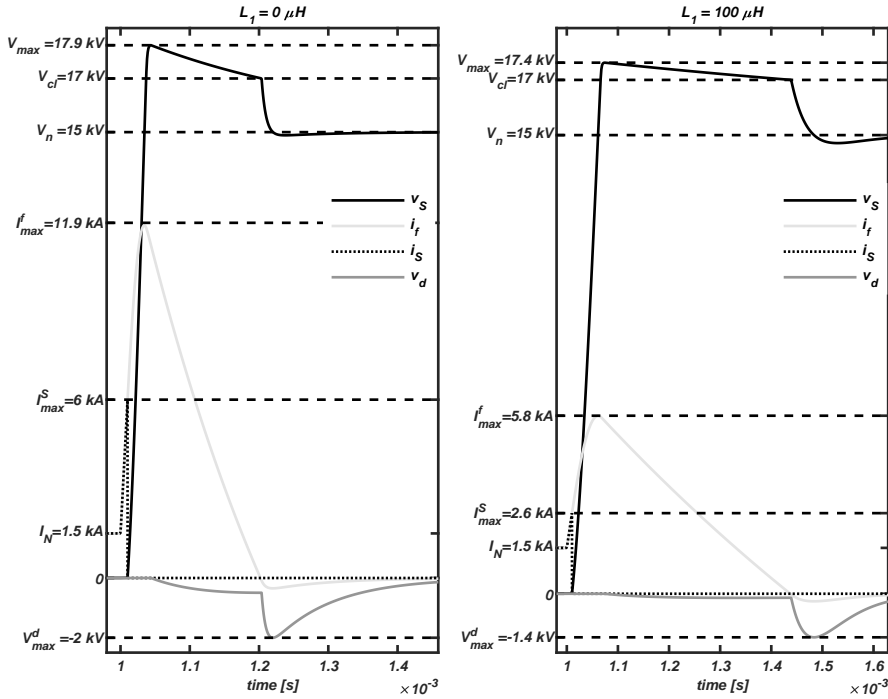
Figure 21: Simulation results of the base case with $R_m = 0.1\,\Omega$.

Figure 22: Simulation results of the base case with $R_m = 0.1\,\Omega$ with $V_{max} = 1.5V_{max}^{base}$.

Figure 23: Simulation results of the base case with $R_m = 0.1\,\Omega$ with $t_b = 0.5t_b$.
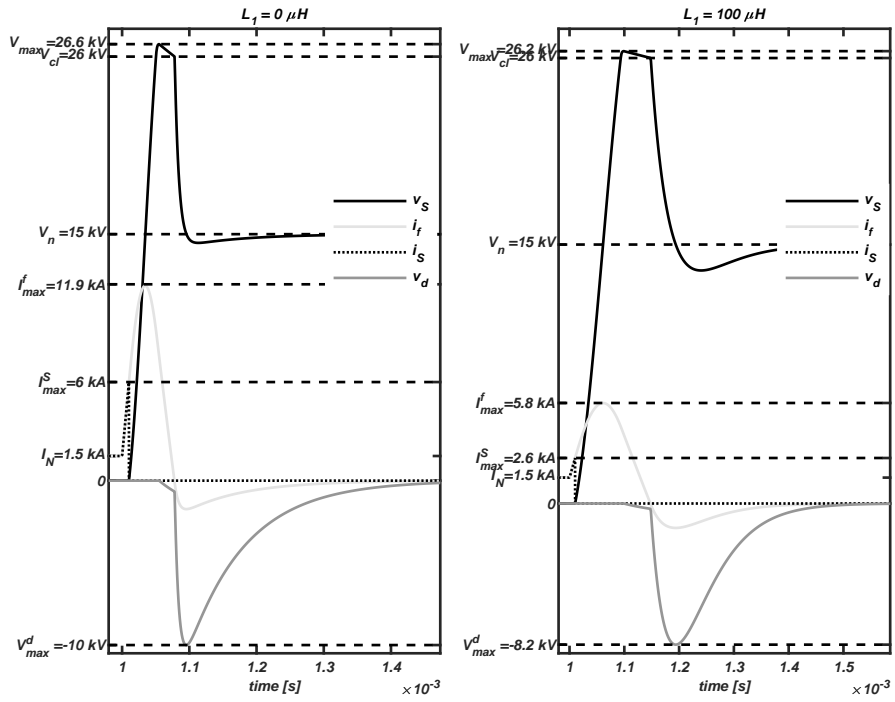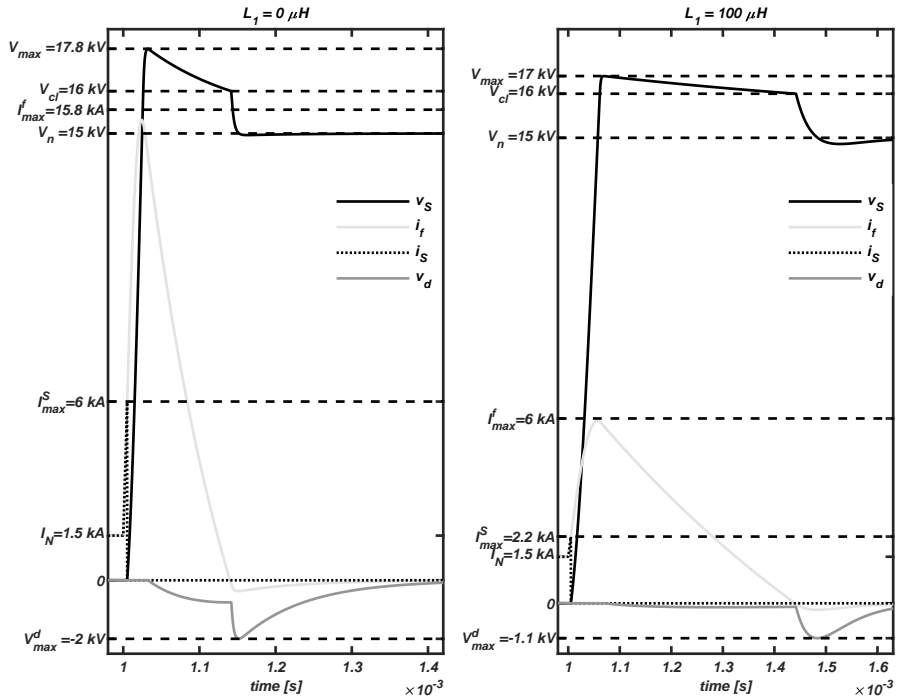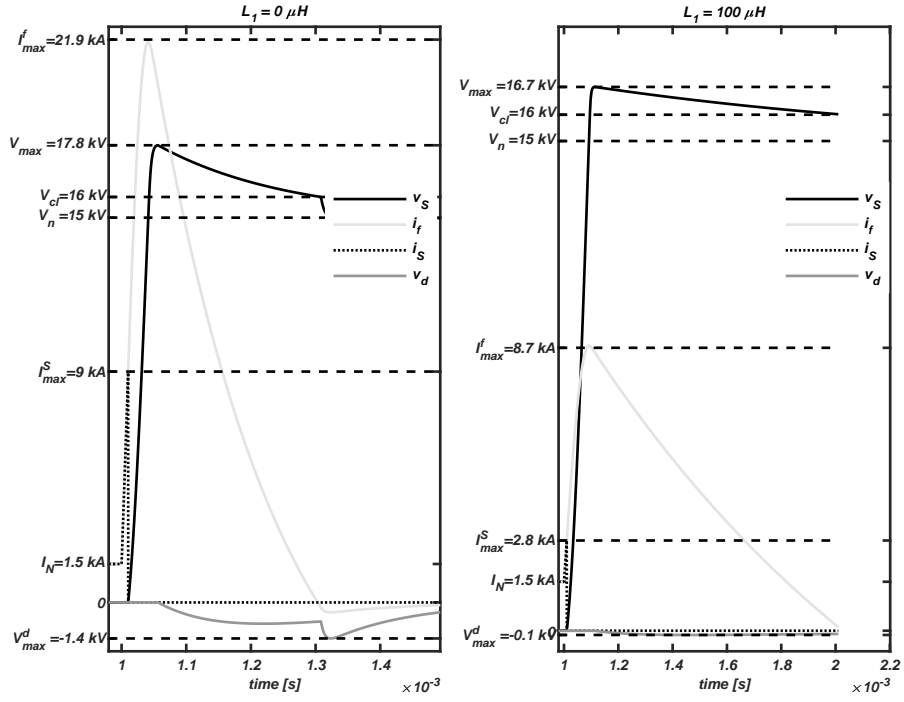
Figure 24: Simulation results of the base case with $R_m = 0.1\,\Omega$ with$I_{max}^S = 1.5 I_{max}^{S,base}$.
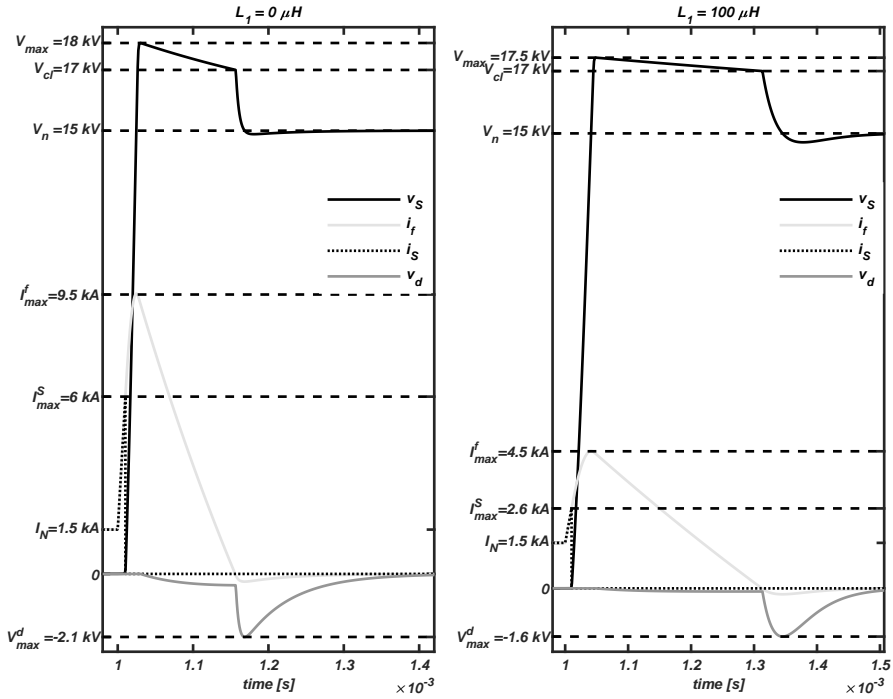

Figure 25: Simulation results of the base case with $R_m = 0.1\,\Omega$ with $C_s = 0.5 C_s^{base}$.

4.3.2 More specific MOV considerations

The application of circuit breakers is not the usual application for MOVs. The strategy used for choosing MOVs in other application is thus also different. As will be seen the application of circuit brakers will apply close to zero voltage on the MOV during normal operation. Only when the breaker is initiated will the MOV see any significant voltage. Leakage current will thus not be an issue.

The maximum current that will flow through the breaker will be in the range of thousands of Ampere. The linear region of high power MOVs I-V characteristics typically conducts current in the range of 10^{-4} to 10^3 Amperes [55]. Since $1000\,\text{A}$ is comparably small to the maximum current that will be seen by the breaker, approximating such an MOV as a diode that starts to conduct at V_{cl} with $i_{mov} \approx 1000\,\text{A}$ should be a reasonable approximation. The clamping voltage will thus from here on be defined as the voltage at which the MOV is conducting a current approximately in the $1000\,\text{A}$ range. The nominal system voltage should be in the mid range of the MOVs linear reagon.

Furthermore using the resistance in the MOV at a voltage of $v_{MOV} = V_{cl} + \frac{V_{max}-V_{cl}}{2}$ should yeild a reasonable approximation of the MOVs resistance in the applicable range unless $V_{max} >> V_n$ which is not the case.

In fact, the over voltage $V_{OV} = V_{max} - V_{cl}$ seen by each MOV device will be relatively small due to the requirement of series connecting of devices and can be given by;

$$V_{OV}^i = \frac{V_{max} - V_{cl}}{n} \tag{113}$$

Where V_{OV}^i is the over voltage seen by a single MOV device and n is the number of series devices. Based on the nature of the application and the discussion in section 3 it is a requirement that $V_n < V_{cl} < V_{max}$. The maximum voltage V_{max} should also be comparably close to the nominal voltage V_n in order for the switching devices not to be over dimensioned. Thus the assumption that MOV resistance is linear in the range $[V_{cl}, V_{cl} + V_{OV}^i]$ is not a far of estimation.

Figure 26 shows the I-V characteristics of Littlefuse HA 32mm series. If an MOV resistance lower than the maximum allowable value were to be realized one of the lower I_v characteristic of figure 26 should be chosen to avoid the need for parallel connections. The *V131CA32* model will have a conduction of approximately $1000\,\text{A}$ at $V_m = 300\,\text{V}$. This means that approximately 57 such MOV device would have to be series connected to realize a clamping voltage of $V_m \approx 17\,\text{kV}$ as given by the results of the base case simulations. This would yield an over voltage aboce the clamping voltage of approximately $18\,\text{V}$ on each device and a resistance of approximately $0.3\,\Omega$ per device. This yelds a total resistance of $17.1\,\Omega$ which is too high. Going the other way, trying to limit the number of series connestions, the *V661HA32* model could be chosen.
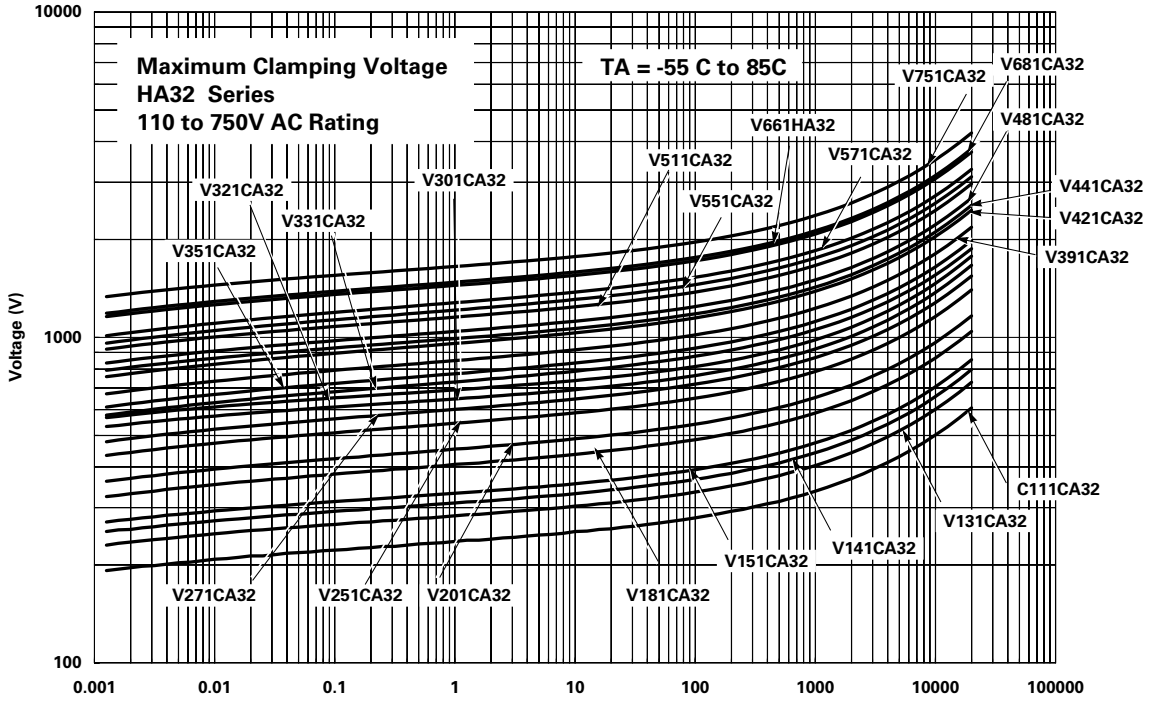
Figure 26: I-V characteristics of Littlefuse HA 32mm series.

Based on the above Discussion, choosing V661HA32 requires around 8 series connections to reach the desired clamping voltage of the base case given by the design criteria from section 3. This means according to the datasheet, a conduction of approximately 200 A at V_n and approximately 1000 A at a clamping voltage $V_{cl} \approx 17$ kV for the base case as describe in section 4.2.1. This yields an MOV resistance of approximately 0.7 Ω for each MOV device and a total of 5.6 Ω at $v_{MOV} = V_{cl} + \frac{V_{max} - V_{cl}}{2} \approx 17$ kV. A total of 10 parallel branches is thus required to reach an MOV resistance below the estimated maximum allowed MOV resistance. This means a total of 80 connected MOV devices.

It should be noted that these are crude estimations used to compute comparable results between the topologies. In a real design context a more complex model of the MOV should be used.

With this MOV resistance and with a discrete selection of devices, the optimal clamping voltage in unattainable without series branches considering the maximum MOV resistance of $R_m < 0.66$ Ω. In an attempt to reduce the number of MOV devices, in particular the number of series branches an increased maximum allowable voltage V_{max} than the one decided upon in the base case could be considered. This means that another IGBT must added in series to obtain a maximum voltage of 22.5 kV. Now the maximum allowed MOV resistance is increased to 1.83 Ω. Adding another IGBT would increase it further to 3.33 Ω. The required number of series connections is in this case reduced to two, yielding an MOV resistance of approximately 2.8 Ω.

In order to reduce the over voltage to V_{max}, the inductance must be increased further from the value decided by the switching divides limits to approximately $L_s = 49$ µH.

It should be noted that since the inductance must be increased due to high MOV resistance, the full potential of the switching device in terms of maximum rated current will not be utilized.

65

The base case is now updated as shown in table 18. This case will be referred to as *case 2*.

Table 18: Relevant characteristics of *case 2* simulation base case.

Device	Series connections	Parallel connections	Tot. number of devices	V_{max}[kV]	I_{max}[kA]	t_{delay}[µs]	P_{max}[kW]	L_s[µH]
IGBT1	6	1	6	27	6	10.13	187.8	49

Figure 27 shows the simulation results of *case 2*.
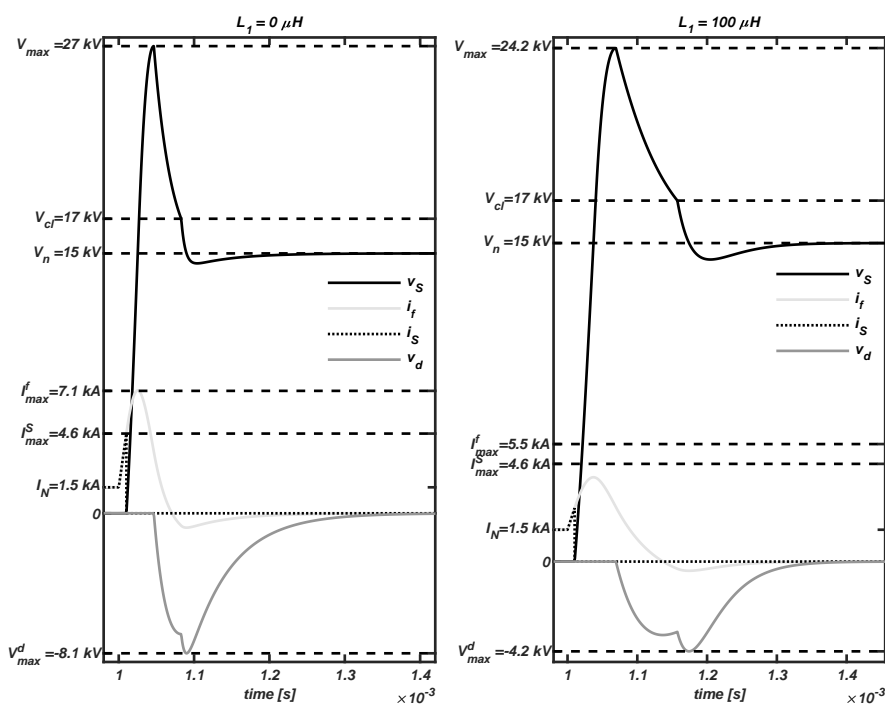

Figure 27: Simulation results of case 2 with $R_m = 1.6\,\Omega$.

4.3.3 The SiC case

For this case the characteristics given by table 17 will be used. Furthermore a MOV resistance of $R_{MOV} = 0.1\,\Omega$ will be used in order to try and isolate the improvements and disadvantages of using SiC MOSFETs.

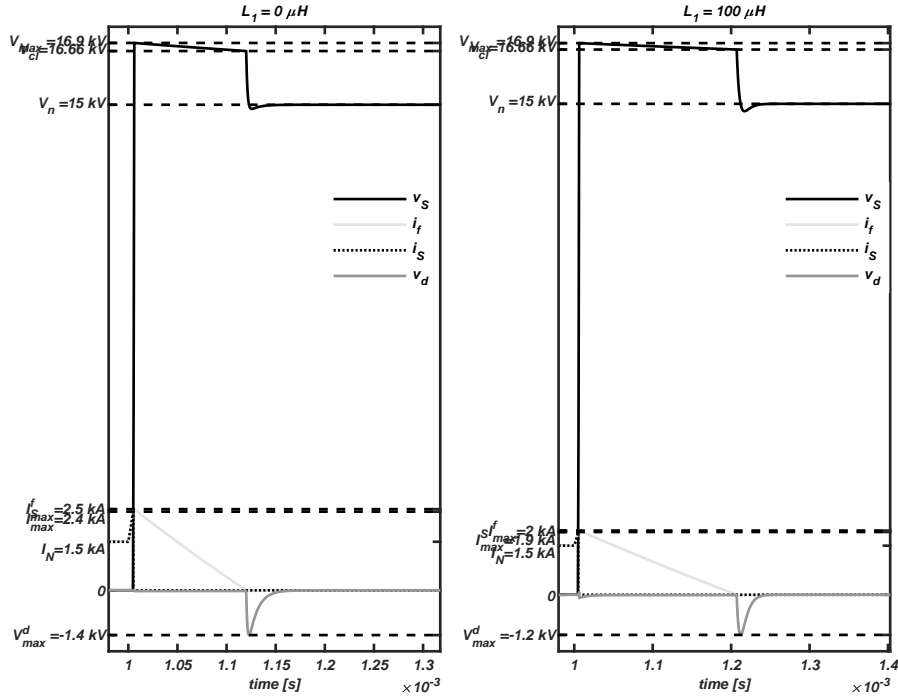Figure 28 shows the simulation results of the *SiC case*.

Figure 28: Simulation results of the SiC case with $R_m = 0.1\,\Omega$.

4.3.4 Summary of interrupting simulation results

Table 19 summarizes the results of the different test conditions simulated for the interrupting topology.

If V_{max} were to increase, there would only be a slight improvement in the total breaking time t_b while all other parameters seems to stay the same other than an increase in the diode requirements. It should however be noted that the fault current passes through zero before the calculated total breaking time t_{tot}. The time to reach zero current is improved a lot by increasing V_{max} while the time to reach steady state zero value is not.

The most prominent effect of decreasing the total delay time t_b (switching device delay time + sensing/coordination delay) is the reduction of required current limiting inductance which is reduced linearly with the reduction of t_b. Total breaking time is reduced slightly for lower values of fault inductance L_1 and the voltage requirement of the diode is increased. The maximum fault current I_{max}^f is also increased. It should be noted that increasing the current limiting inductance back to the base case value reduces I_{max}^f to 10.92 kA which is below $I_{max}^{f,base}$ while t_b stays approximately equal to t_{tot}^{base}.

Increasing the maximum allowable current through the switching device I_{max}^S does not seem to have other positive effects than slightly decreasing the current limiting inductance L_s. All other parameters are worsened except for a decrease in required voltage for the diode. In particular, the required size of the snubber capacitance C_s is increased a lot.

The increase of the switching device power capabilities modeled by a decrease in C_s, decreases all parameters except for the slight increase in required diode voltage characteristics.

For *case 2* all parameters are improved except for the diodes voltage characteristics. This is however at the cost of adding two more switching devices (in this case of type *IGBT1*). In

this case a realistic choice of MOV was considered.

Using currently commercially available SiC MOSFETs improved almost all main parameters of the design. This is however given that a large amount of discrete devices could be interconnected in order to achieve wanted ratings or that devices of higher ratings were available. Expetedly the $\frac{dv}{dt}_{max}$ requirements of the diodes in the topology is however increased drastically. This is due to the low turn-off time of the MOSFET requiring a smaller capacitor meaning the diodes will be subject to higher stress' The required size of the current limiting inductor is on the other hand increased. This is owing to current available SiC MOSFETs technological hindrance of creating larger wafers. The SiC MOSFETS thus have lower current carrying capacity. In order to limit the number of required parallel connected devices the current must be reduced by adding a larger current limiting inductor.

Potentially,the maximum allowed MOV resistance could be increased drastically using SiC devices. This is due to the SiC devices fast switching capabilities requiring a lower snubber capacitor and reducing the total delay time. With the results from *case 2* seen in table 19 the maximum allowed MOV resistance is increased to approximately $1\,\Omega$. With a further reduction of total delay time for example by improving the total sensing and coordination time to $1\,\mu s$ the maximum allowed MOV resistance would be further increased to approximately $1.4\,\Omega$ which is closing in on the theoretical value of $1.66\,\Omega$ as discussed previously in this section.

Table 19: Summary of results for the interruptive topolgy

Conditions	$L_t = 0\,\mu H$			$L_t = 100\,\mu H$			LCR requirements			Diode requirements				
	V_{max} [kV]	I_{max}^f [kA]	t_{tot} [µs]	V_{max} [kV]	I_{max}^f [kA]	t_{tot} [µs]	L_s [µH]	C_s[µF]	R_s [Ω]	I_{max} [kA]	V_{max} [kV]	$\frac{di}{dt}_{max}$ [$\frac{kA}{\mu s}$]	$\frac{dv}{dt}_{max}$ [$\frac{kV}{\mu s}$]	$\int i^2$ [A²s]
Base case $(R_m = 0.1\,\Omega)$	17.92	11.86	259	17.37	5.82	429	33.77	16.03	5.7782	11.86	1.42	0.44	0.36	2896
$V_{max} = 1.5V_{max}^{base}$	26.56	11.86	273	26.2	5.82	385	33.77	16.03	5.7782	11.86	8.18	0.44	0.36	4408
$t_b = 0.5t_b^{base}$	17.84	15.45	220	16.99	5.88	430	16.88	16.03	5.4013	15.45	3.37	0.89	0.37	3638
$I_{max}^S = 1.5I_{max}^{S,base}$	17.82	21.86	293	16.66	8.73	1001	20.26	36.06	3.6525	21.86	0.58	0.74	0.24	11344
$C_s = 0.5C_s^{base}$	17.97	9.49	220	17.5	4.53	307	33.77	8.01	8.1717	9.49	1.59	0.44	0.56	1203
Case 2 ($R_m = 2.8\,\Omega$)	26.96	7.09	220	24.18	3.97	255	49	6.26	9.7556	7.09	4.23	0.31	0.88	965
SiC case	16.91	2.51	118	16.85	1.96	203	81.42	0.14	72.5562	2.51	1.23	0.18	14.23	6

4.4 Simulation of limiting topology

Figure 29 shows the Simulink block diagram of the limiting topology which is to be simulated. There are two diodes in this topology. The snubber diode will be referred to as D_s and the freewheeling diode will be referred to as D_f. As will be seen, the requirements for the two diodes will be very different. The current through D_f will be shown in the simulation results. The maximum voltage over this diode will be equal to the nominal system voltage V_n. For the snubber diode D_s, the voltage will be shown in the simulation results. The maximum current through this diode will be equal to the maximum fault current I_{max}^f.
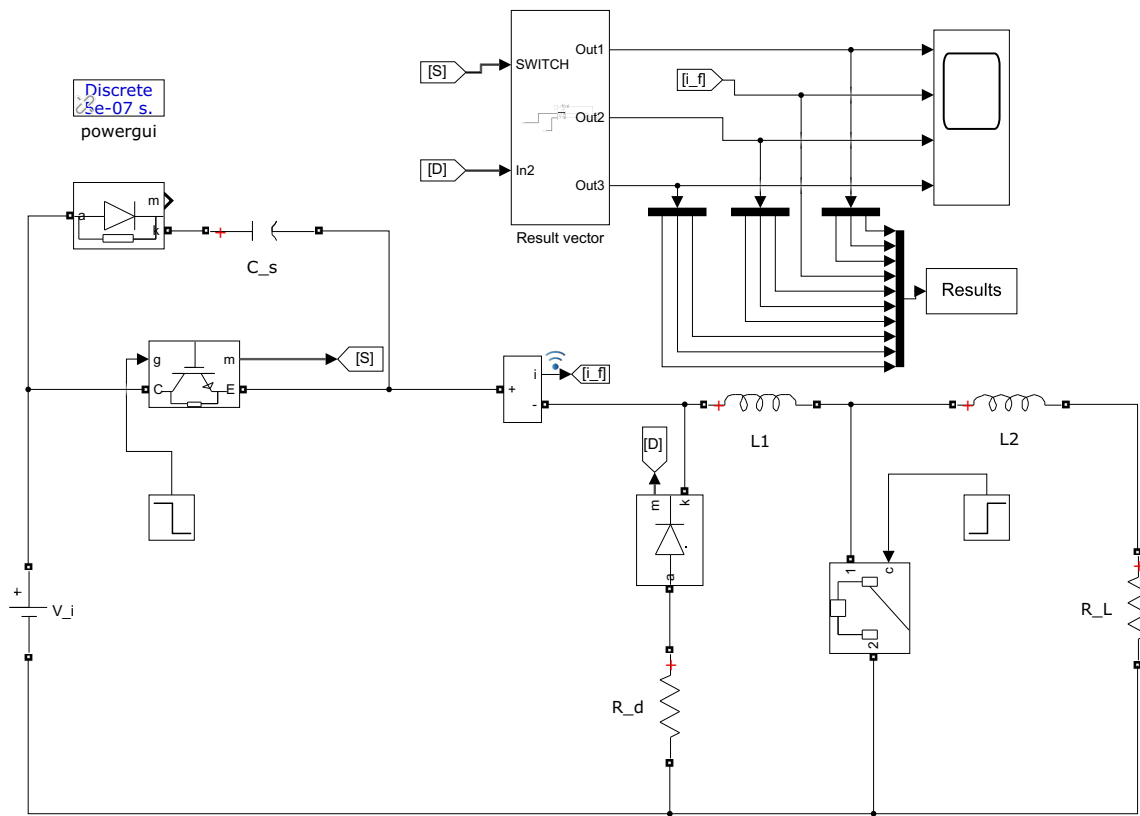
Figure 29: Simulink block diagram for simulation of the interrupting topology

4.4.1 The base case

The base case will be given as described in section 4.2.1. No particular discrepancies such as the modeling of MOV for the interrupting topology is present for this topology. All the parameters for all different simulation cases are designed according to the design approach suggested in section 3.

Figure 30-34 shows the simulation results according to the simulation strategy discussed in section 4.2. The simulation will be further elaborated in section 4.4.4.
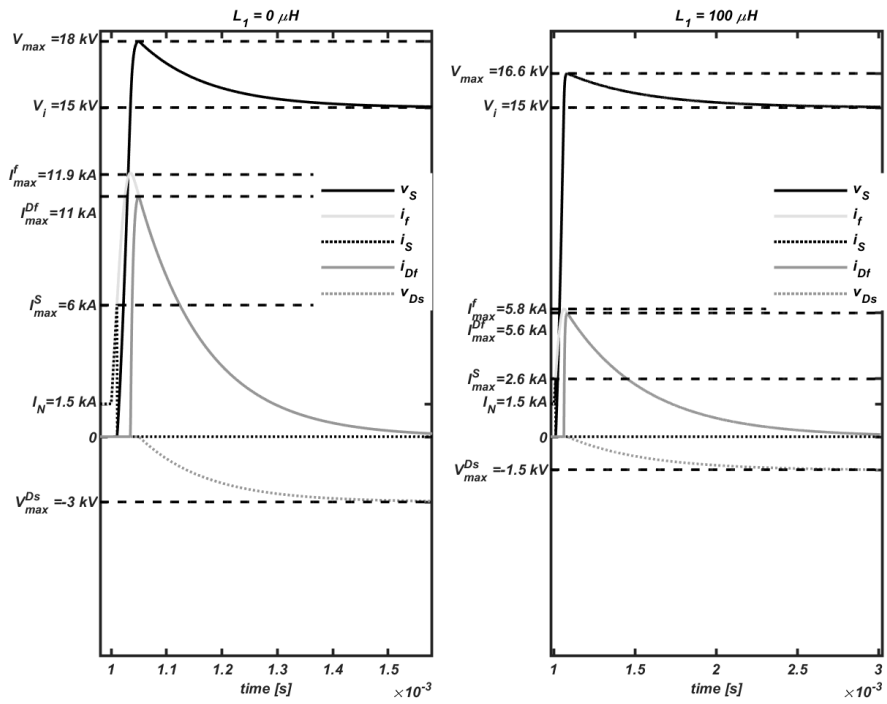
Figure 30: Simulation results of the base case for the limiting topology.
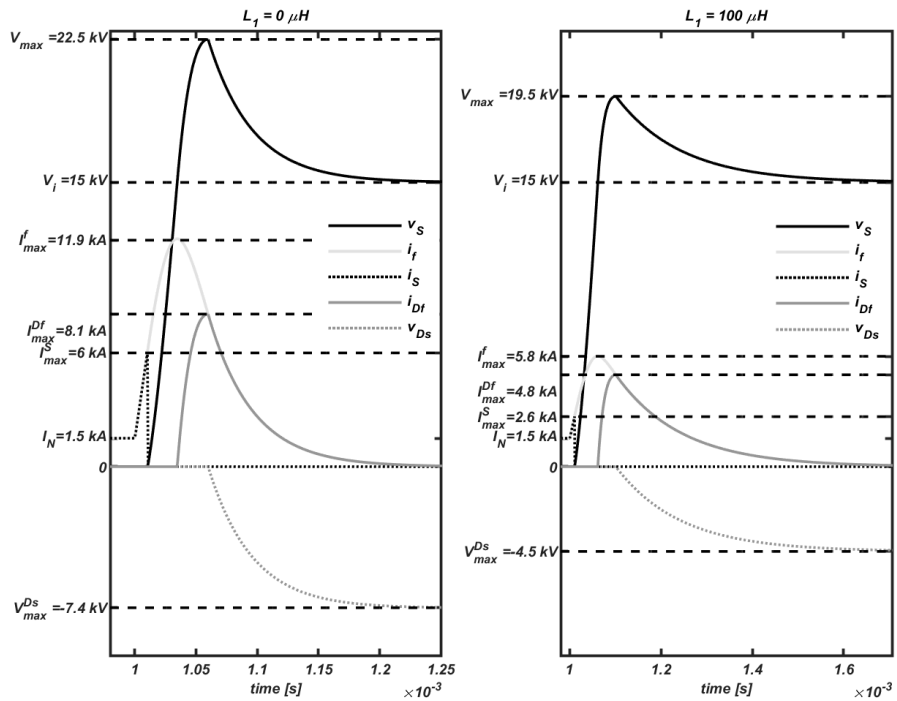
Figure 31: Simulation results of the base case for the limiting topology with $V_{max}^{S} = 1.5 V_{max}^{S,base}$.
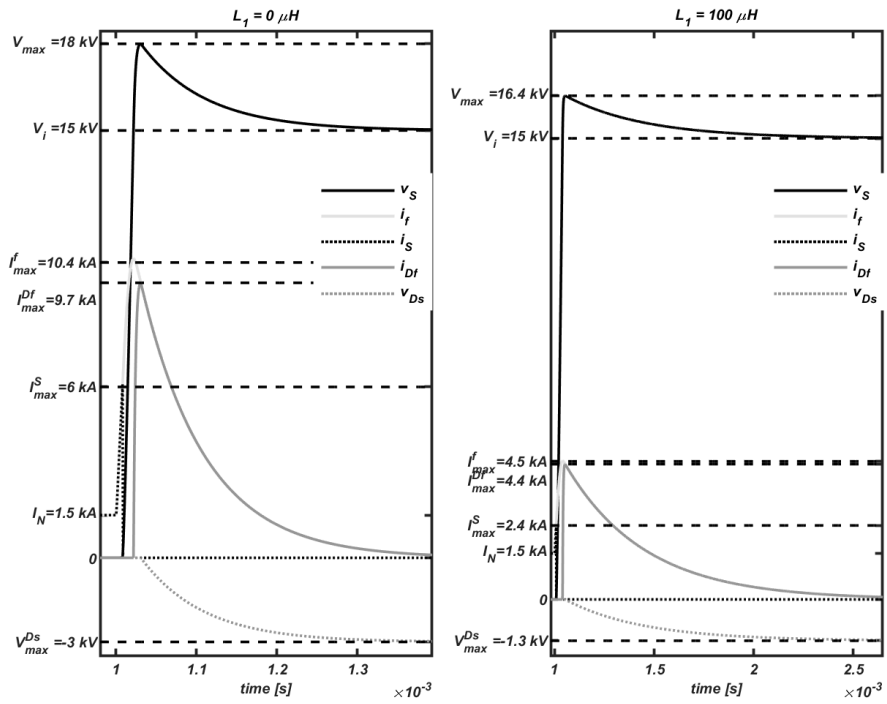
Figure 32: Simulation results of the base case for the limiting topology with $t_b = 0.5 t_b^{base}$.
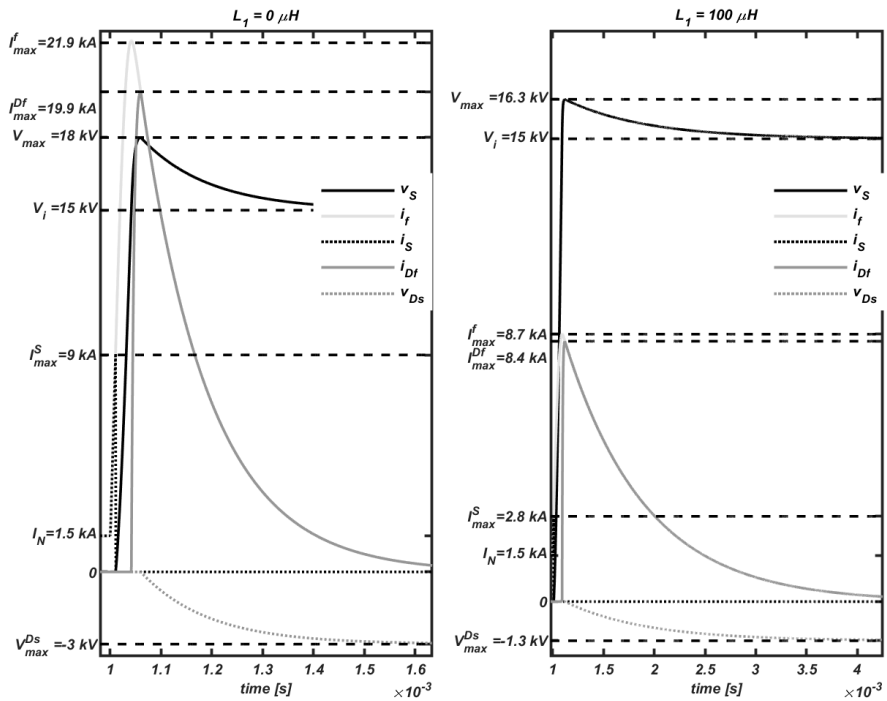
Figure 33: Simulation results of the base case for the limiting topology with $I_{max}^S = 1.5 I_{max}^{S,base}$.
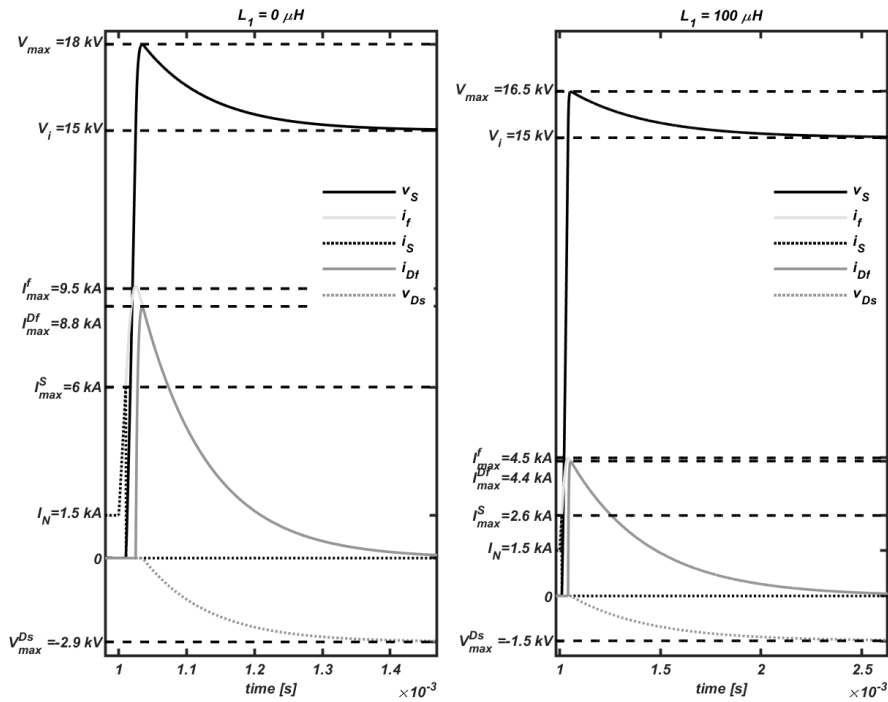
Figure 34: Simulation results of the base case for the limiting topology with $C_s = 0.5 C_s^{base}$.

4.4.2 Current limiting mode

In the current limiting mode the breaker will be able to limit the fault current to a specified value. This may be useful for a number of reasons to discussed in section 5.

In the simulation of this mode, a simple hysteresis band control strategy will be used just to prove its operation. The main switch S_1 will switch on again when a fault current of $I_n - 100\,\text{A}$ and then off again when $I_n + 100\,\text{A}$ is reached. To properly design the control strategy and protect the components consideration to the effective switching frequency should be taken. This analyses will however not be included in this text.

Figure 35 shows the simulation results of the limiting breaker in current limiting mode with parameters decided by the base case as given in section 4.2.1.
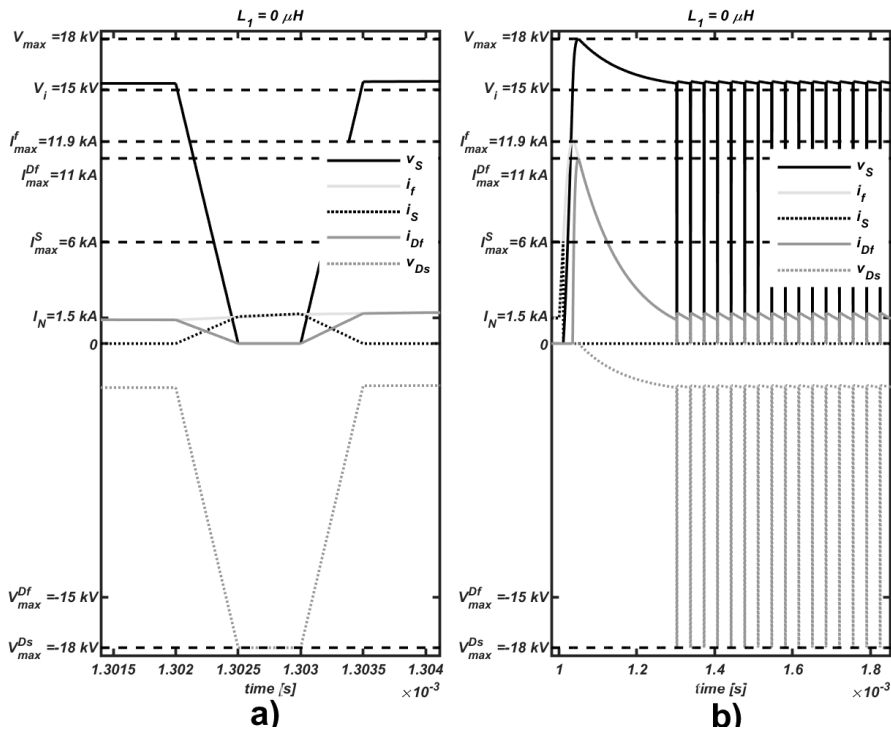
Figure 35: Simulation results of the base case in current limiting mode through fault path. a) Shows the switching characteristics during current limiting. b) Shows the switching as the current reaches steady-state.

4.4.3 The SiC case

The parameters in table 17 is used for the simulation of the SiC case. No particular design considerations is needed for this case. Figure 36 shows the simulation results of the SiC case using the limiting topology.
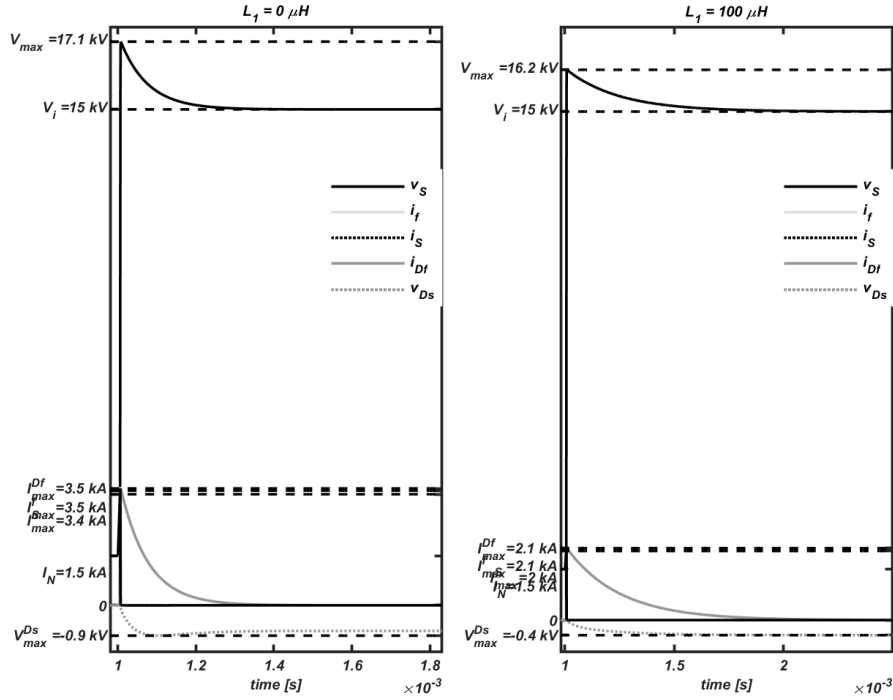
Figure 36: Simulation results of limiting topology for the SiC case.

4.4.4 Summary of limiting simulation results

Table 20 summarizes the results the different simulation conditions for the limiting topology.

In general for this topology the total breaking time t_{tot} increases drastically as the fault inductance L_1 increases. This increase however seems to be very efficiently limited by an increase in V_{max}. This increase does not seem to notably affect any other important parameters.

Decreasing the total delay time t_b (turn-off delay of switch + sensing coordination delay) by a factor of 0.5 reduces both the maximum fault current I_{max}^f, the total breaking time t_{tot}, the required current limiting inductance L_s and halves the required snubber capacitance C_s. The diode requirements are also generally decreased except for $\frac{di}{dt}$ and $\frac{dv}{dt}$ requirements..

Increasing the maximum allowed current through the switching device I_{max}^S does not seem to have any positive effects other than slightly decreasing the required current limiting inductance L_s. In addition the this, the required size of the snubber capacitor C_s is doubled when I_{max}^S is increased by a factor of 1.5.

Increasing the switching devices power handling capabilities P_{max} decreases both the total breaking time t_{tot} as well as the maximum fault current I_{max}^f. Diode requirements are also reduced exept for the $\frac{dv}{dt}$ requirements.

The current limiting action of the breaker also seems to work and stays consistent with the results of the base case. The only difference between the breaking and the limiting of the fault current is that it puts more stress on the diodes. The maximum current through D_f is approximately doubled and the maximum voltage of D_s is increased to V_{max}.

Table 20: Summary of results for

Conditions	$L_t = 0\,\mu H$			$L_t = 100\,\mu H$			LCR requirements			Diode requirements (D_f/D_s)				
	V_{max} [kV]	I_{max}^f [kA]	t_{tot} [μs]	V_{max} [kV]	I_{max}^f [kA]	t_{tot} [μs]	L_s [μH]	C_s[μF]	R_s [Ω]	I_{max} [kA]	V_{max} [kV]	$\frac{di}{dt}_{max}\left[\frac{kA}{\mu s}\right]$	$\frac{dv}{dt}_{max}\left[\frac{kV}{\mu s}\right]$	$\int i^2$ [A²s]
Base case	18.02	12.02	529	16.56	5.84	1975	33.77	16.02	0.27561	5.64/12.02	15/1.5	0.44/0.04	0.35/0.75	8589/2789
$V_{max} = 1.5V_{max}^{base}$	27.08	12.02	201	23.84	5.84	313	33.77	16.02	2.6493	3.34/12.02	15/8.71	0.44/0.26	0.21/0.75	481/4078
$t_b = 0.5t_b^{base}$	18.04	10.51	343	16.39	4.52	1597	25.22	8.01	0.31506	4.4/10.51	15/1.35	0.59/0.05	0.55/1.29	4301/1248
$I_{max}^S = 1.5I_{max}^{S,base}$	18.01	22.04	583	16.28	8.68	3200	20.26	36.05	0.15132	8.44/22.04	15/1.27	0.74/0.06	0.23/0.61	31414/11253
$C_s = 0.5C_s^{base}$	18.03	9.55	419	16.52	4.54	1578	33.77	8.01	0.34313	4.41/9.55	15/1.47	0.44/0.04	0.55/1.18	4381/1148
Current limiting mode	18.02	12.02	302	-	-	-	33.77	16.02	0.27561	10.95/12.02	15/17.99	0.44/0.53	0.68/0.75	35417/2789
SiC case	17.05	3.58	281	16.23	2.13	949	40.71	0.14	0.57994	2.12/3.58	15/0.45	0.37/0.01	15.39/25.18	448/9

4.5 Simulation of resistive topology

Figure 37 shows the Simulink block diagram of the resistive topology which is to be simulated. There are two distinct diodes in this topology. The center diode creating a freewheeling path for the center switch S_{C2} will be referred to as D_C. There is also two diodes in the two main paths. These will however have the exact same response and characteristics and will be referred to as D_S. The maximum current flowing through D_C qnd D_S will be the same as the maximum fault current in the breaker I_{max}^f. The voltage over diode D_C will be equal to the voltage over the center switching device S_{C2}. This voltage will be very low since the current always will flow through a low resistance path due to the freewheeling diode D_C. The voltage over this diode will thus be neglected.
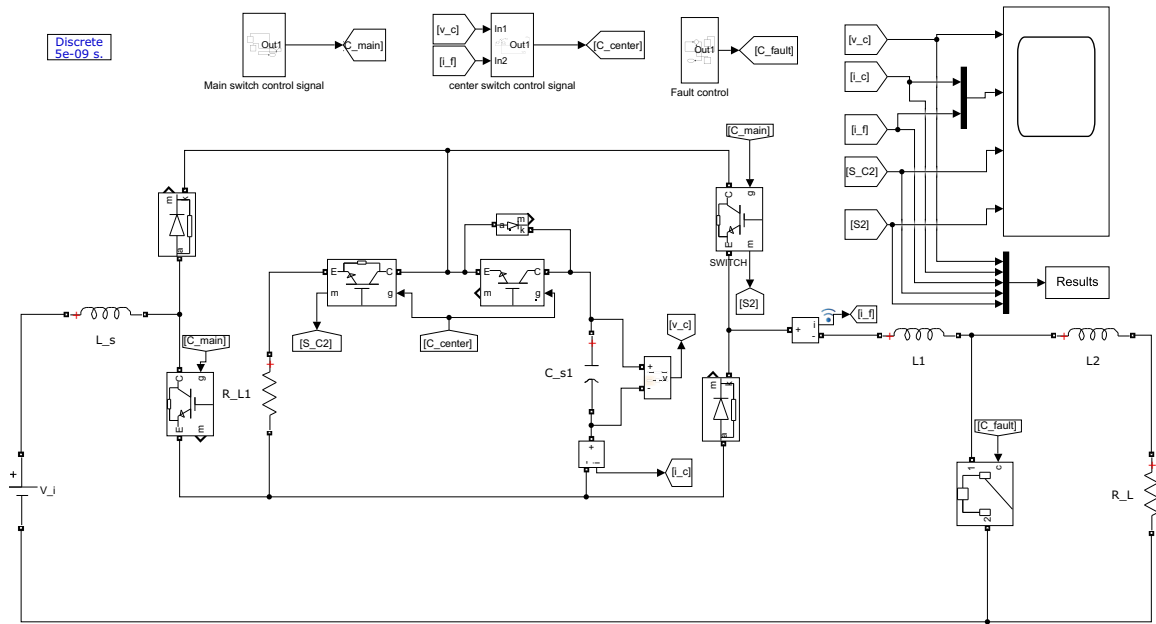
Figure 37: Simulink block diagram for simulation of the resistive topology

4.5.1 The base case

The base case will be given as discussed in section 4.2.1. Furthermore it will be assumed that the impedance of the fault path can be sensed. This sensing of impedance could either be performed directly by measuring the fault currents rate of change or by applying some adaptive control scheme using estimators. It should be noted that this strategy can be carried out to different degrees of accuracy.

By using measured or estimated inductance L_1, the time when the first switching cycle from phase one to phase two must occur to assure the first peak reaches V_{max} can be calculated on-line. This would require very fast and accurate sensors and a complicated drive circuit.

Another way to realize this strategy is to design a threshold inductance L_{thresh} or equivalently a threshold rate of rise current $\frac{di}{dt}_{thresh}$. This threshold should represent the inductance where the current in phase two immediately starts decreasing at $v_c = V_{max}$. Thus if $L_s > L_{thresh}$

the first switching from phase one to phase two occurs at $v_c = V_{max}$. If $L_s < L_{thresh}$ the first switching occurs at $v_c = V_i$. This way discrepancies in the modeling of the breaker can more easily be accounted for by adjusting L_{thresh} and the threshold can be designed in such a way as to assure that V_{max} is never breached. This however comes at the cost of slightly slower response in the interval $0 < L_s < L_{thresh}$.

Figure 38-42 shows the simulation results for the base case and its emulated improvements as discussed in section 4.2.1. The simulation will be further elaborated in section 4.5.5. In all these simulations, strategy two has been used and deemed most beneficial. Strategy one will be discussed as a separate case.
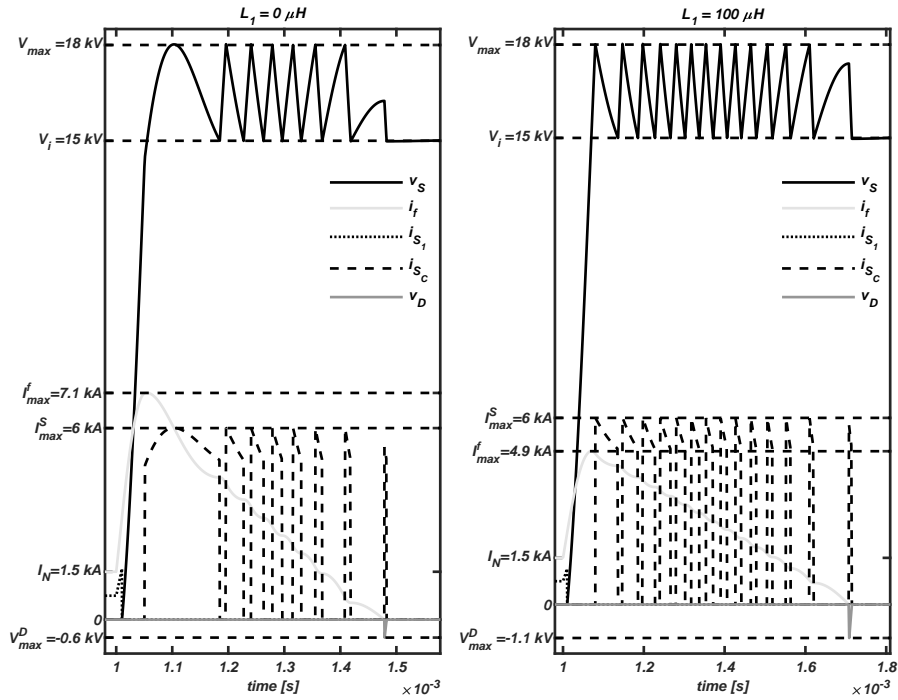
Figure 38: Simulation results of the base case for the resistive topology.

Figure 39: Simulation results of the base case for the resistive topology with $V_{max} = 1.5V_{max}^{base}$.
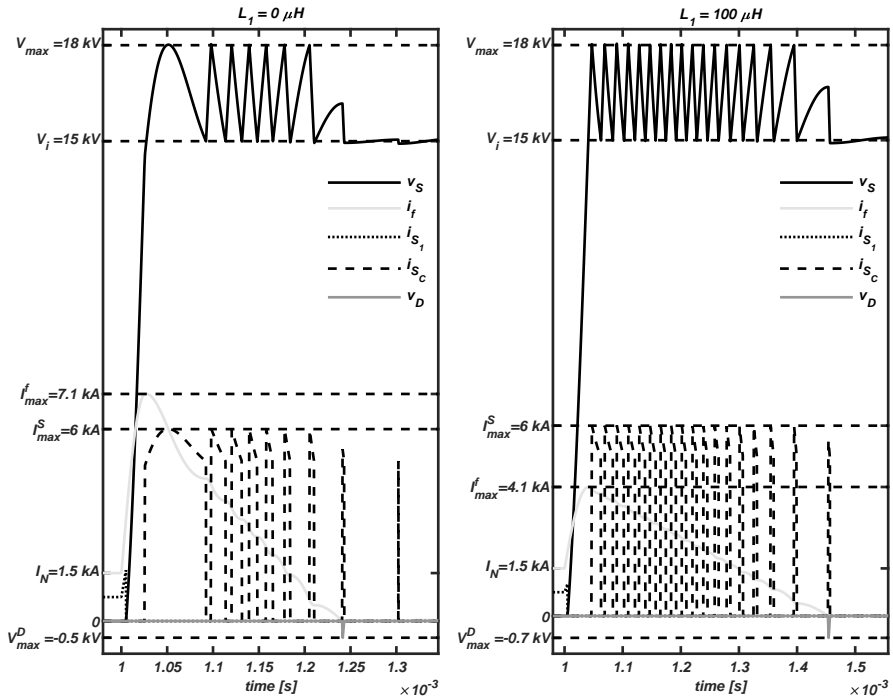
Figure 40: Simulation results of the base case for the resistive topology with $t_b = 0.5t_b^{base}$.
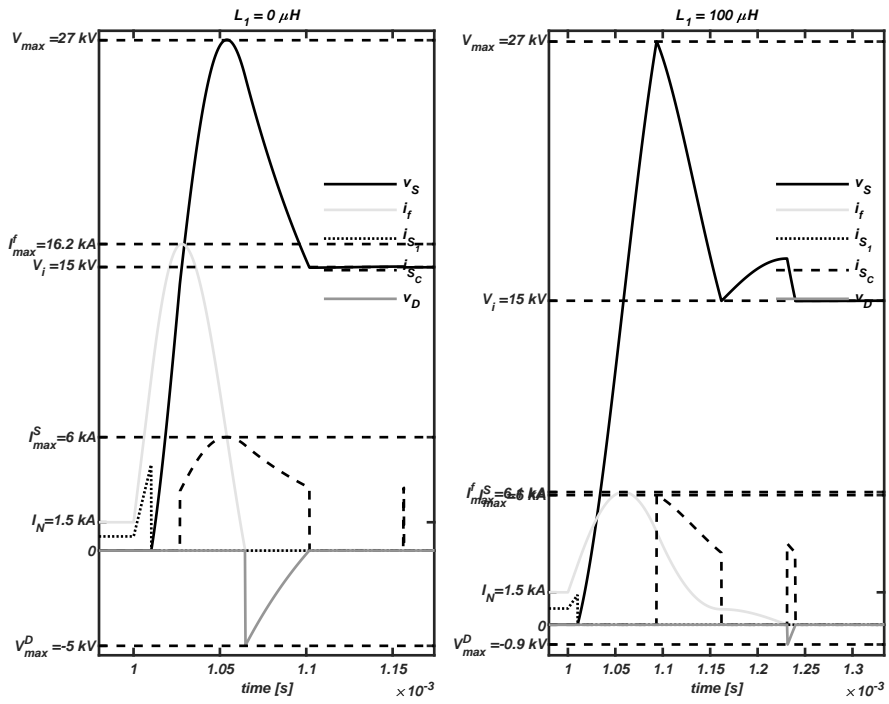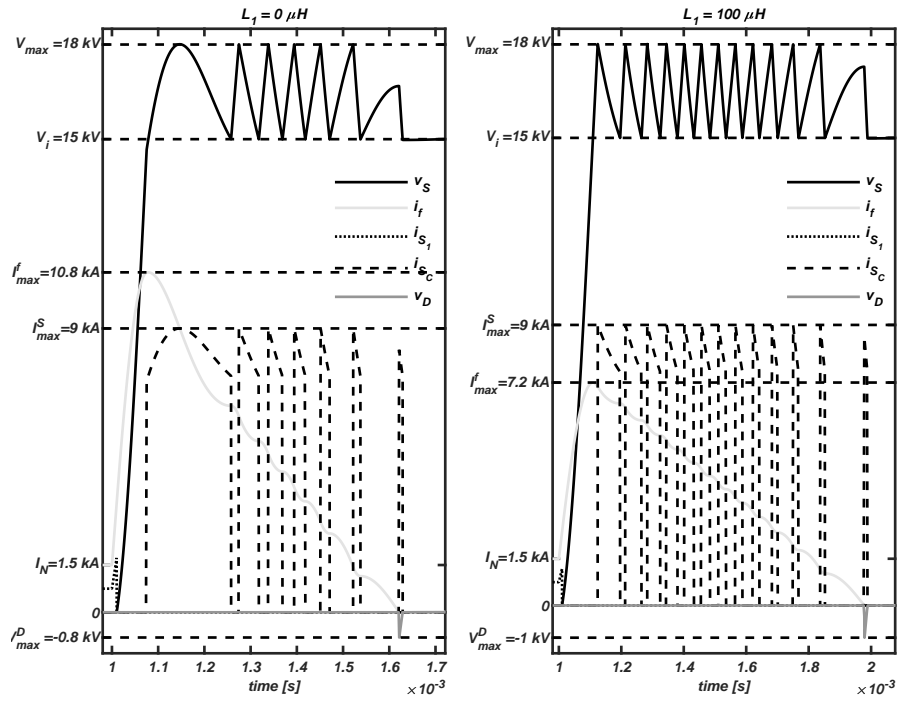
Figure 41: Simulation results of the base case for the resistive topology with $I_{max}^S = I_{max}^{S,base}$.
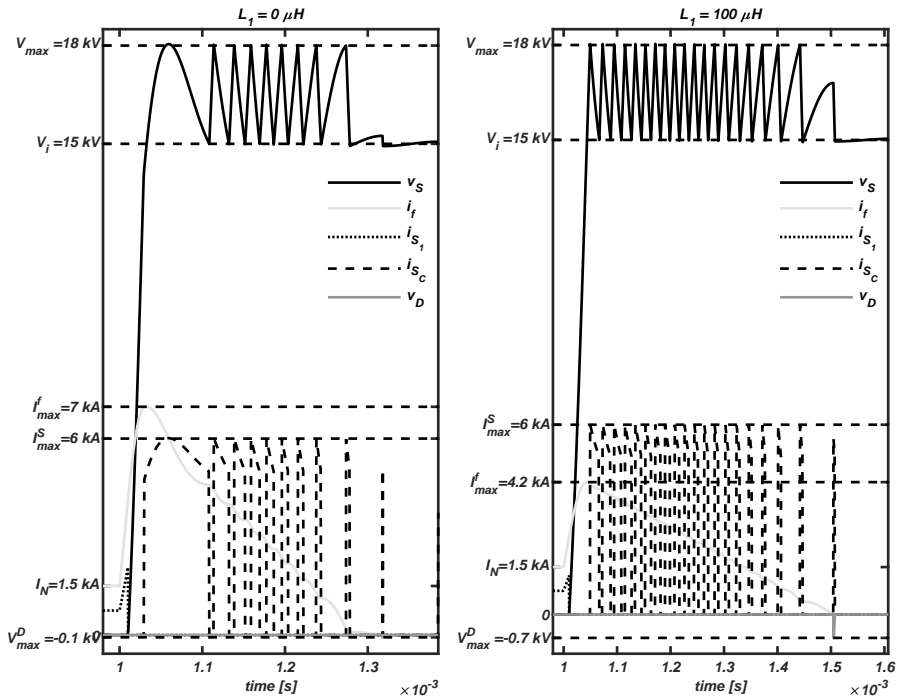
Figure 42: Simulation results of the base case for the resistive topology with $C_s = 0.5 C_s^{base}$.

4.5.2 Simulation results with and without L_1 sensing/estimation

In figure 43 the breakers performance with and without the opportunity of sensing can be seen. In the graph to the right, the first switching occurs at the same conditions as it would for $L_1 = 0$. On the right side the first switching occurs at V_{max} since $L_1 > L_{thresh}$. Since the breaker will be designed for the worst case scenario which will be the same independent on the opportunity of sensing the fault impedance, most of the rated values of the breaker will be independent on this. As seen in figure 43 however, the breaker will drive the current to zero much faster for fault inductances $L_1 > 0$. In figure 43 the total breaking time with sensing is 675 μs with $L_1 = 80$ μs. The total breaking time without sensing is 880 μs with $L_1 = 80$ μs.
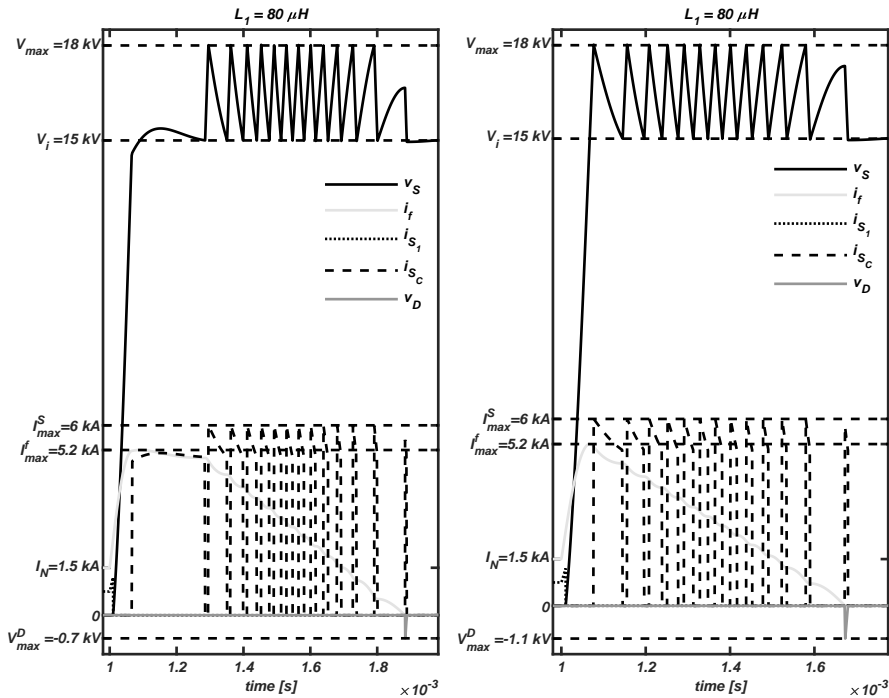
Figure 43: Simulation results of the base case for the resistive topology with and without sensing of L_1.

4.5.3 Strategy one

Strategy one will as discussed in section 3 minimize the breaking time while at the same time minimizing the maximum voltage overshoot V_{max} if only one switching cycle is used. This strategy will also minimize the required current limiting inductance L_s to its minimum requirements in regard to the switching device according to the analysis in section 3. In the simulation of this strategy no proper considerations have been taken related to the the actual switching control. The switching between the phases is performed using a clock just to prove its function.

Figure 44 shows the results of running the base case with this strategy. The maximum allowable blocking voltage of the switching devices is however not considered in this case.

If this strategy was to be realized, as seen in figure 44 a total of 7 of the IGBTs used in the base case would have to be series connected to reach the maximum voltage of 28.4 kV.
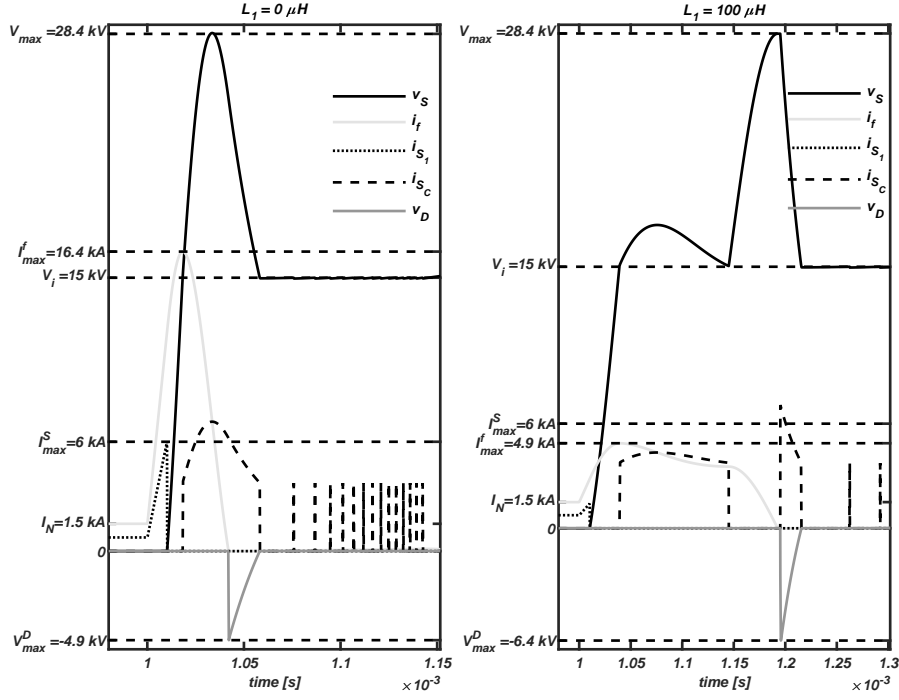
Figure 44: Simulation results of the base case for the resistive topology using strategy one.

4.5.4 The SiC case

According to the analysis in section 3, the resistive topology should operate under damped in phase two. Since the resistance R_d will be limited by;

$$\frac{V_{max}}{R_d} \geq I_{max}^C,$$

and the current limiting inductance is limited by I_{max}^S, the capacitance must be increased according to;

$$\frac{1}{2R_d}\sqrt{\frac{L_{max}}{C}} < 1$$

in order to achieve an over dampened system.
The capacitance will thus be given by;

$$C = \frac{L_{max}}{4R_d^2} = 1.59\mu\text{F},$$

where L_{max} is is the maximum fault path inductance being the sum of $L_s = 62.49\,\mu\text{H}$ and $L_{max}^1 = 100\,\mu\text{H}$. L_s is found according to the same constraints as in the base case in section 4.2.1.

The reason why this is relevant in this case is due to SiC superior switching characteristics having a falling time approximately three orders of magnitudes lower than the IGBT used in the base case.

Figure 45 shows the result of the simulation of the resistive topology for the SiC case.
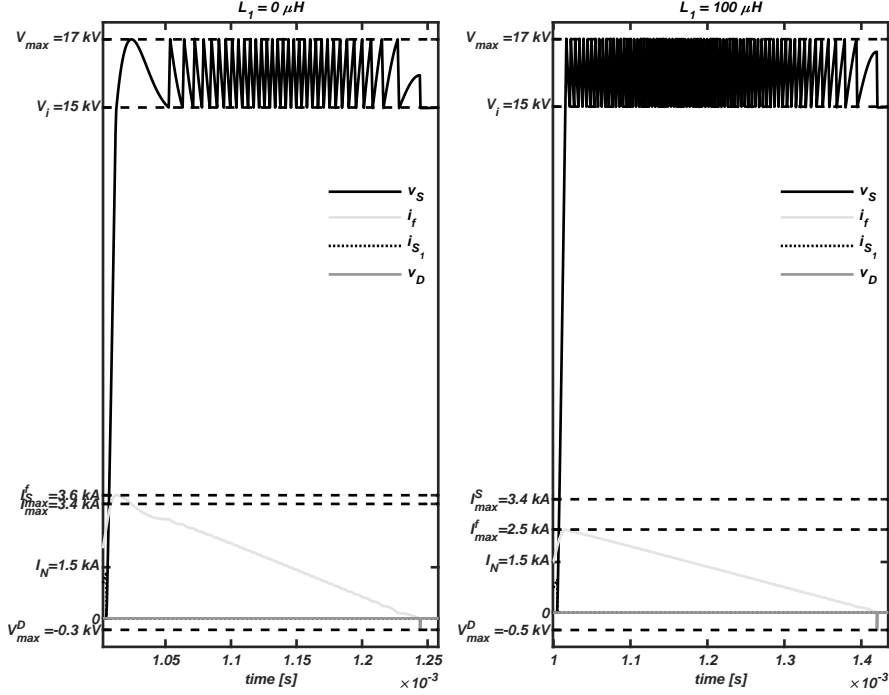
Figure 45: Simulation results of resistive topology for the SiC case.

4.5.5 Summary of results for the resistive topology

Table 21 summarizes the results of the different test conditions simulated for the resistive topology.

As seen in the table, increasing the maximum allowable blocking voltage of the switching devices V_{max} drastically decreases the total breaking time t_{tot} and as well as the required size of the current limiting inductance. This does however come at the cost of drastically increasing the maximum fault current that will be reflected back to the source and cause high demands on the power source freewheeling diodes. These effects could also be achieved through over dimensioning the breaker by adding more switching devices in series.

Decreasing the total delay time t_b (turn-on delay of switch + sensing/coordination delay) approximately halves the total breaking time. At the same time both the required size of the current limiting inductor and the snubber capacitance is halved. Maximum fault current is not affected.

Increasing the maximum allowed current through the switching device does not seem to have any positive effects on the design other than slightly decreasing the required current limiting inductance. The required size of the capacitance is also doubled.

Increasing the switching devices power handling capabilities P_{max} almost halves the total breaking time and decreases the required current limiting inductance.

Using strategy one seems to achieve the same as increasing the V_{max} which is not surprising because it requires approximately the same increase in V_{max}. The diodes current integrals $\int i^2$ does however increase quite drastically.

In the resistive topology, for the SiC case all parameters are improved as well as decreasing the required current limiting inductance. The capacitor had to be increased from its minimal value in order to assure an under damped scenario. This however results in a value still lower than the base case resultsf.

Table 21: Summary of results for the resistive topology

Conditions	$L_t = 0\,\mu\text{H}$			$L_t = 100\,\mu\text{H}$			LCR requirements			Diode requirements				
	V_{max} [kV]	I^f_{max} [kA]	t_{tot} [µs]	V_{max} [kV]	I^f_{max} [kA]	t_{tot} [µs]	L_s [µH]	C_s [µF]	R_s [Ω]	I_{max} [kA]	V_{max} [kV]	$\frac{di}{dt}_{max}$ $[\frac{kA}{µs}]$	$\frac{dv}{dt}_{max}$ $[\frac{kV}{µs}]$	$\int i^2$ [A²s]
Base case	18.03	7.1	478	18.02	4.93	710	89.96	16.03	3	7.1/7.1	1.1/-	0.17/0.17	0.44/-	8140/2868
$V_{max} = 1.5 V^{base}_{max}$	27.02	16.22	74	27.01	6.14	233	20.06	16.03	4.5	16.22/16.22	0.9/-	0.75/0.75	1.01/-	8525/5165
$t_b = 1.5 t^{base}_b$	18.03	7.1	246	18.04	4.07	457	44.98	8.01	3	7.1/7.1	0.7/-	0.33/0.33	0.89/-	4347/1458
$I^S_{max} = 1.5 I^{S,base}_{max}$	18.01	10.78	621	18.01	7.15	977	77.91	36.06	2	10.78/10.78	1/-	0.19/0.19	0.3/-	23638/8865
$C_s = 0.5 C^{base}_s$	18.04	6.97	285	18.04	4.18	507	57.83	8.01	3	6.97/6.97	0.7/-	0.26/0.26	0.87/-	5131/1628
Base case Strategy 1	28.43	16.43	52	28.37	4.88	202	14.47	8.01	4.0017	16.43/16.43	6.4/-	1.04/1.04	2.05/-	28901/15377
SiC case	17.02	3.62	241	17.01	2.46	416	62.49	1.59	5.0595	3.62/3.62	0.5/-	0.24/0.24	2.28/-	1600/403

5 Discussion

5.1 General discussion on breaker performance

5.1.1 Increasing V_{max}

As discussed in section 4, increasing the maximum allowable voltage V_{max} is realized through an improvement of power electronic switching device, the selection of a device with higher blocking voltage or by simply series connecting more switching devices or even series connecting the breakers themselves. The more series connections, the higher the total equivalent resistance in the main path of the breaker. This will cause higher power losses during normal operation. therefor series connecting devices for the sake of improving the turn-off characteristics may in general be unwanted.

As seen in section 4 in all breaker topologies except from the interrupting topology, the total breaking time is greatly reduced. For applications requiring super fast breaking times, increasing V_{max} might be worth considering. Particularly for the limiting topology an increase in the maximum allowable voltage over the main switch drastically reduces total breaking time for higher values of fault inductance (equivalent to faults further away from the breaker).

Generally the maximum fault current is greatly increased as V_{max} is increased. This is however not the case for the limiting topology where I_{max}^f stays the same independent on the maximum allowable voltage given the design method in section 3. This is due to an increase in the dissipative resistance R_d being a direct result of an increase in V_{max}.

In the resistive topology the required current limiting inductance is greatly reduced by an increase in V_{max} unlike the other topologies where it says the same.The maximum fault current is on the other hand greatly increased. Higher demands on the freewheeling diodes in the power source would thus be required, but could be balanced out by further increasing the current limiting inductance L_s.

Thus increasing V_{max} seems pointless for the interrupting topology while being a huge advantage for the limiting topology. For the resistive topology a trade-off between V_{max}, I_{max} and the size of L_s is expected. This is classical example of the trade-off between prize, weight and performance and should be optimized for the specific application in mind.

5.1.2 Increasing I_{max}^S

Increasing the maximum allowable current through the switching device I_{max}^S can only seem to reap the benefit of decreasing the size of the current limiting inductance L_s for all topologies. Most other characteristics are worsened by allowing a higher current let through the switching device. While it may be of some use for low weight, compact applications, it will based on the results in section 3 be considered unfitting to improve the breaker in this manner.

5.1.3 Decreasing t_b

Decreasing the total delay time t_b is realized through an improvement of the switching device turn-off delay time, or the improvement of the sensing equipment and/or fault coordination system. Based on the discussion in section 2.3, 2.5 and the results in section 4 this appears to be one of the main potentials for breaker improvement. All though still improved, the

interrupting topology seems to reap the least benefit from this improvement. For the other topologies all parameters are greatly improved by reducing t_b.

The reduction of the total delay time t_b can thus be seen to be a key design goal. Particularly interesting is the fact that this is the only improvement that can be realized without improving the switching device used in the breakers.

5.1.4 Increasing P_{max}

The increase of the switching devices power handling capabilities P_{max} greatly improves all breaker topolgies reducing maximum fault current I_{max} and the total breaking time t_b as well as decreasing the required size of passive elements. This is also intuitive since the higher power dissipation the switching device is able to tolerate, less support is required to limit this power dissipation. After all, the main objective of the supporting circuit in a circuit breaker is to provide a path for the excess energy to be dissipated.

Based on the results in section 4 improving the switching devices power handling capabilities may be the most effective way of improving the breaker topologies.

5.1.5 Using SiC devices

Using commercially available SiC MOSFETs could improve all breaker topologies drastically. This is given that a large number of switching devices can be effectively series- and parallel connected. An improvement in the SiC devices themselves such as improved blocking voltage and maximum drain source current could reduce the required number of devices needed to interconnect. Such devices seems to be under development and technological advances in this field is expected since SiC devices is still far from realizing its theoretical limits.

The use of SiC devices will however have cause higher $\frac{dv}{dt}_{max}$ requirements for the diodes in all the topologies. Specifically for the interrupting topology, using SiCs inherently fast switching capabilities could increase the maximum allowable MOV resistance which could be a key factor in realizing this breaker topology.

5.2 Comparison of breaker topologies

On – state power losses would be the same for all breaker topologies given that the same power electronic switching device is used as the main switch and that an equal amount of device is series connected. Due to the two parallel paths in the resistive topology, it will have the lowest on-state power losses. This topology does however require two extra diodes in the main paths contributing to the power losses. The power loss contributed by the diodes will be comparably small to the power losses of the active switching device chosen. It should however be noted that if a parallel path is constructed in the limiting or the interrupting topology, power losses in these topologies would be even lower than the resistive topology since these would not require an extra diodes in the main path. Furthermore The freewheeling path in the limiting topology will be subject to some leakage current through the diode in this path. Thus if results were to be normalized with regard to parallel connected switching devices, the interrupting topology would have the least power losses. Realistically however, with problem of designing an MOV with low enough resistance the interrupting topology may as seen in section ?? be subject to the need of adding more switching devices in series considerably adding to the total on-state power loss of the breaker.

In terms of **complexity** the interrupting topology has the lowest number of required power electronic devices. The limiting topology requires one more diode compared to the interrupting topology and the resistive three given that the parallel diode of center switch S_C2 has to be an external diode and the in-body diode of the switching device cannot be used. In addition to this, the resistive topology would require three more active switching devices as compared to the two other topologies. It should however be noted that the diodes in the resistive topology requires very low blocking voltage compared to the diodes in the other topologies. If the current limiting function of the limiting topology were to be utilized, the diodes in this topology would need to be rated for much higher power compared to the other two topologies. Due to the switching nature of the resistive topology and the limiting topology when run in current limiting mode, the control system and driver circuitry for these topologies would need to be more complex than the interrupting topology. The interruptig topology is thus the simplest solution in terms of control, driver circuitry and number of components.

The **maximum fault current** is similar in both the interrupting and limiting topology. The resistive topology allows for a lower fault current to seen by the source. If V_{max} is increased however the resistive topology sees the larges fault current. This could however be normalized by increasing the current limiting inductance. It should be noted however that the liting topolgy the fault current seen by the source is quickly driven to zero as the diode in the freewheeling path starts to conduct. The power dissipation in the source is thus greatly limited in this topology.

Totalbreakingtime is generally lowest for the interrupting topology. The limiting topology has the slowest breaking times for faults happening further away from the breaker. In the resistive topology the potential for fast breaking time seems to be the largest if V_{max} was allowed to increase.

Requirements of passive devices is comparable for both the limiting and interrupting topology. The capacitance however can more easily be reducing in the limiting topology also by external improvement of the total delay time. The resistive topology generally has the largest requirements for passive devices, but also seems to have the greatest potential for reduction of these requirements given improvements in the switching devices and sensing/coordination

system.

In terms of **controllability**, the limiting topology can actively be controlled to force the current to a specific value. The interrupting topology however can only be turned completely off. Given the nature of the resistive topology it is possible that some degree of controllability is achievable with this topology. It will however require more work to determine the feasibility of this.

5.3 Topology specific advantages and potential improvements

5.3.1 Current limiting topology as uninterruptible power supply

As discussed in section 3 and shown in section 4, the limiting topology is able to limit the current to a specified value. This feature may be very useful in some applications.

Very often, MVDC systems are related to different kinds of multi-terminal systems such as micro grids, on-board ship distribution, off-shore distribution etc. In these multi-terminal systems faults that occurs elsewhere in the system may cause over currents or over voltages to non-faulty parts of the system. If the circuit breakers coordination system is able to differentiate the faulty from the non-faulty conditions, the current can be limited using the limiting breaker topology until the faulty part of the system has been isolated. This current limiting action may not be possible using the converters since the fault conditions can still be quite severe even if they happen elsewhere. With the limiting breaker however the current limiting action is performed through the dissipative component R_d where excess energy can be dissipated. Thus whenever such faults occurs elsewhere in the system, the limiting breaker can quickly assume nominal values instead of completely driving the current to zero. This may be particularly useful in supplying uninterruptable loads.

Another advantage of this feature is that it may give the power systems control more time to react to the fault thus balancing the rest of the system before the current is completely driven to zero. This way the breaker work as to simulate a load equal to the load shorted by a short circuit. The breaker can thus simulate this load and then gradually drive the current to zero in a manner that makes it easy for the power systems controller to balance the rest of the power system.

5.3.2 Integrating the limiting breaker in DC-DC converters

The similarities between the limiting solid state circuit breaker and a buck converter gives reason to believe that such a breaker could be integrated with DC-DC converters. The most obvious and simplest possibility is to integrate the breaker with a buck converter. In this case the main switch S_1 would be common for both the breaker and the converter. Two freewheeling paths would be needed. One for the buck action and one for the breaker action.

There would be many ways to realize such an integration. The most controllable way would implement switches in both freewheeling paths. During normal operation the buck path would be actively switching while the breaker path would be open. During faulty conditions, the buck path would be opened and the breaker path would actively be switched or stay on to drive the current to zero. This would however require one more switching device as compared to having separate converter and breaker. Both switching devices would need to be able to handle a blocking voltage equal to the nominal system voltage. The switching device in the

breaker path would also need to be able to withstand high fault currents. The only advantage of this device would thus be to make it more compact and limit the stray components between converter and breaker.

Another way would be to only have a switching device in the buck path. Designing the dissipative resistance of the breaker path to be much higher than the resistance of the freewheeling diode in the buck path would ensure minimal current to flow through the breaker path when the buck path is active. It is not unlikely that the dissipative resistance could be designed to be at least in the range of 10^3 times higher than the resistance of the freewheeling diode in the buck path. Based on the results in section 4 designing the dissipative resistance in the $10^0 - 10^1\Omega$ range should be reasonable. According to [56] the total resistance of a freewheeling diode with the required ratings is in the range of $10^{-4}\Omega$ while the switching device could be expected to be in the $10^{-3}\Omega$ range. The current flowing through the buck path during the freewheeling part of the buck action would then be around 99.9 %. Furthermore, the switch in buck path would not need to be able to withstand larger currents than the nominal rating of the buck converter. The number of switching devices in the main path is thus reduced to one compared to the two needed for the separate solution. This would also mean that the need for a constantly on switching device is eliminated. This could possibly reduce the total power loss. The integrated device would also combine the buck inductance and the current limiting inductance of the breaker as well as combining the snubber circuitry. This device would thus also be a more compact solution, limiting the stray components and reducing the number of required passive components. More work is however required in order to decide if this solution is even realizable. Figure 46 shows the schematic diagram of how such a converter could look like.
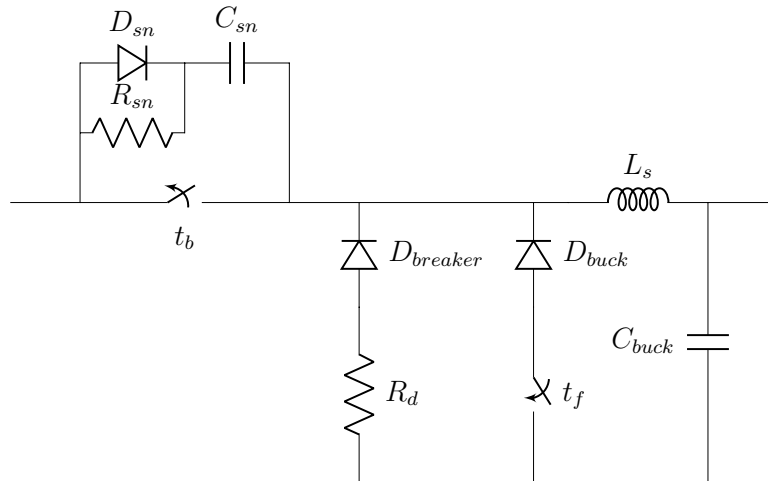

Figure 46: Schematic diagram of a possible novel topology for the integration of the limiting breaker topology in a buck converter.

The required switch in the Buck-path does in fact transform the topology to a half bridge converter. It is also possible that similar configurations can be performed with different converter types.

6 Conclusion and future work

6.1 Conclusion

Improving the power electronic device used for switching in terms of V_{max}, I_{max}, P_{max}, P_{loss}, t_{delay} and t_{fall} will improve the breakers performance. While V_{max}, I_{max} and P_{max} can be improved by adding several devices in series- and parallel connection, this requires a lot of devices. Often, devices can be difficult to connect either in series or parallel due to challenges regarding the current- or voltage sharing capabilities of different devices. t_{delay} and t_{fall} however, can only be improved by selection of power electronic device or improvement of the devices themselves.

Increasing V_{max} either by series connection or by selection or improvement of semiconductor device seems to improve the speed of all topologies. The limiting topology is particularly improved in terms of improving the breaking time of faults with higher fault inductance. Increasing V_{max} comes with the trade-off of increased fault current and diode requirements for the diodes needed in the topologies. An increase in fault current will also be directly translatable to higher requirements for the power source since the maximum fault current of all these topologies is reflected back to the source. In the limiting topology however the freewheeling path takes over the fault current after the maximum fault current is reached limiting the required $\frac{di}{dt}$ requirements of the power source.

Improving the maximum allowed current through the breaker emphasizes the reduction of the current limiting inductance needed in the topologies. faster breaking times is generally also seen. This does also come with the trade-off of increased fault current through the breaker. A clear trade-off between the required current limiting inductor and the fault current seen by the source can thus be found.

The total delay time of the breaker is a combination of the switching devices turn-off time and the delay time associated by the coordination and sensing strategy of the breaker. Reducing this delay time seems to be of top most importance in improving breaker performance. The reduction of delay will reduce the passive device requirements, reduce the turn-off time as well as reduce the fault current seen by the power source. This is also the only way of improving the breaker topologies without improving the power electronic semiconductor device used for switching. Efforts to reduce the delay time associated with sensing and coordination should thus be made.

Decreasing the capacitor used in all topologies is mainly achieved by increasing the switching devices power handling capabilities or by decreasing the current falling time of the devices. This will also reduce the fault current seen by the power source as well as reduce the total breaking time.

The interrupting topology is the simplest topology offering the lowest requirements in terms of required power semiconductor devices. it also offers some of the fastest breaking times without the need of further increasing the maximum allowable voltage over the switching device. This is however assuming that an MOV of satisfactory characteristics can be found. This may not be the case and practical implementation of the breaker is complicated by the MOV operation. In impriving this breaker topology it is crucial that the clamping voltage of the MOV happens abruptly and that the effective resistance of the MOV is reduced to a low enough value. The constant clamping value also means that the voltage will always reach at least this value when a fault occurs. This means that unnecessarily high over voltages and fault currents will occur regardless of the actual operation voltage. For power source where the

voltage is variable this may not be a suitable topology.

The limiting topology offers the largest degree of controllability. It also seems to be the slowest topology, particularly for faults of higher fault inductance. The breaking time of this topology is very sensitive to the increase of V_{max}. Another huge advantage of this topology is that the freewheeling path provides an alternative route to the fault current. While the maximum fault current is still seen by the power source, the power dissipated in the power source is greatly reduced. This topology may also be combined with DC-DC converters of certain types. This does however require more research.

While the resistive topology is the most complicated topology requireing a large amount of semiconductor devices, it also seems to be the topology with the highest potential of reducing passive element requirements and total breaking time. It may thus be very suitable for compact fast acting applications.

The power losses in all topologies is governed by the chosen switching device. The key factor in reducing this will thus be the improvement of power semiconductor devices. The implementation of SiC technology thus seems very interesting. Not only does SiC devices offer a much lower on-sate resistance, it may also enable the use of uni-polar devices such as MOSFETs that does not have an on-state voltage drop, further reducing the power losses.

Using SiC MOSFETs further seems to drastically improve all breaker topologies. With current technology however, it seems unlikely that the required current, voltage and power rating of mid-range MVDC ($\approx 15\,\mathrm{kV}$) applications is achievable. With future devices reaching a higher blocking voltage and current carrying capabilities the compatibility of SiC with MVDC solid state breakers will potentially be very advantageous. In particular SiC MOSFETs have very low turn-off delay and current falling time which will be a huge advantage together with the low on-state resistance. Such devices could also potentially reduce the limitations caused by too high effective resistance in available MOVs.

The results achieved in this paper shows how important it will be to choose a suitable topolgy and optimize it specifically for the application for witch it is to be used. All topologies have their advantages and short comings and different topologies may be suitable even within the same system. The interrupting topology for example may be very suitable for reliable and simple interruption of a constant DC grid fault. The limiting topology on the other hand can work as to assure the deliverance of power to un-interruptable loads or controlling the fault current in sensitive areas of the system. For applications requiring super fast and compact solutions such as under water applications connected to MVDC distribution grids the resistive topology may be a good choice.

6.2 Future work

There are still a lot of research needed in the filed of medium voltage DC circuit breakers. In this paper the power source has been modelled as an ideal DC voltage source. In order to capture the dynamics of a realistic system however, a more detailed and realistic model should be used. Furthermore in a realistic model, the stray components should also be considered. A proper model of the switching device should also be included in order to capture how its dynamics affect the design.

In this text only two different kinds of switching devices was simulated in a simplified manner. The Si IGBT and the SiC MOSFET. A more detailed investigation of SiC switching

devices should be performed. In particular the feasibility of achieving the required power ratings either through series and parallel connections or by technological future prospects. The feasibility of using other switching devices such as the GTO, the JFET or The interconnection of different devices should also be further investigated.

While many trade-offs and improvement parameters have been identified, important factors such as economical feasibility and structural properties have not been directly considered. In order to optimize a breaker for a specific application a relationship between the investigated parameters and the price, weight and dimension should be investigated. With these trade-offs optimizing a breaker for a certain real applications would be the next step.

The Characteristics of commercially available MOVs was found to be a huge limiting factor in the interrupting topology. More reasearch in developing such devices for the specific purpose of MVDC circuit breakers should be attempted. The feasibility of using other clamping devices such as TVS diodes should also be investigated. Improvement of all semiconductor technologies can be seen in light of recent SiC technological improvements. It can thus also be expected that devices such as TVS diodes may see the same improvements in the future as well enabling more fitting characteristics for the application of MVDC circuit breakers.

The resonance topology was not included in this text. It is however on the basis on [1] suspected that also these breaker topologies (the resonance breaker having many sub-topologies) will be suiting for certain applications. These topologies should thus also be compared to all the other topologies.

A   MATLAB code for designing and simulating the Interrupting topology

```matlab
1
2  %%%Adjustable parameters
3  clear all
4  figure
5  descreteMOV=0;
6  R_des = 2.8;
7  V_des = 17000;
8  P_des = 187.8e3;
9
10  %General system parameters
11
12  V_N = 15e3;       %DC voltage [V]
13  I_N = 1.5e3;      %Nominal system current
14  R_L = V_N/I_N;
15  I_thresh = 3000; %current sensing threshold for breaking
16  R_fault = 0.000001;
17
18  for i = 1:2
19
20  t_sense = 5e-6;            %Time when fault is sensed [s]
21  t_s_delay = 5-13e-6;
22  t_fall = 0.75e-6;
23  I_max = 6000;    %Max current of swithing device
24  V_max = 18000;   %Max voltage of switching device
25  P_max = 124.8e3;
26  if i == 2
27  L_1 = 99.999e-6;    %Inductance between breaker and fault
28  elseif i == 1
29      L_1 = 0.001e-6;
30  end
31
32  %time parameters
33  t_f = 1e-3;               %Time of fault insidence [s]
34  t_b = t_s_delay + t_sense;    %total delay
35  t_open = t_f + t_b;   %time when switch is ctually opened
36  t_stop = t_open + 1e-3;               %Stop simulation
37
38  L_max = 100e-6;
39  L_2 = L_max-L_1;     %Inductance between fault and load
40
41  %Snubber circuit
42  V_fds = 1e-9;             %forward voltage of snubber diode [V]
```

```matlab
43  R_ds = 1e−9;            %on−state resistance of snubber diode [Ohm]
44  C_s = 2*I_max^2*t_fall/(27*P_max);          %snubber capacitance [F]
45  L_s = V_N*t_b/(I_max−I_N);      %inductance before breaker
46
47
48   I_Smax = I_N + V_N*t_b/(L_1+L_s);
49
50  %MOV (modeled as a diode)
51  if descreteMOV==1
52      R_MOV = R_des;
53      V_MOV = V_des;
54      syms L_des
55      I_Smax_des = I_N + V_N*t_b/(L_des);
56      C_des = 2*I_Smax_des^2*t_fall/(27*P_des);
57       I_fmax_des= sqrt(I_Smax_des^2+C_des*V_N^2/(L_des));
58
59     eq = R_MOV*I_fmax_des+V_MOV−V_max;
60     eq = C_des*V_N^2/(((V_max−V_MOV)/R_MOV)^2−I_fmax_des/2);
61       sol = vpasolve(eq,L_des,10e−6);
62      L_s = abs(double(sol(1)));
63  L_s = 49e−6
64      I_Smax = I_N + V_N*t_b/(L_s);
65      is(i)= I_N + V_N*t_b/(L_s);
66       C_s = 2*I_Smax^2*t_fall/(27*P_des);
67
68  else
69  R_MOV = 0.1;  %on state resistance of diode [Ohm]
70  V_MOV = V_max−R_MOV*sqrt(I_max^2+C_s*V_N^2/(L_s));   %clamping
        voltage (in this case forward voltage) [V]
71  end
72  if V_MOV < V_N
73      V_MOV = V_N;
74       error('unable to supress overvoltage')
75  end
76
77  R_s = 2*sqrt((L_s+L_max)/C_s); %snubber resistance [Ohm]
78
79  %Main switch (Semiconductor device)
80   R_on = 1e−3;            %equilvalent on−state resistance of main switch
        %turn−on delay of switch
81
82   %I_Smax = I_N + V_N*t_b/(L_1+L_s);
83
84  I_fmax= sqrt(I_Smax^2+C_s*V_N^2/(L_1+L_s));
85
```

```matlab
86  %Run simulation
87
88  sim('interrupting_breaker.slx')
89
90  %Storing variables in following format
91
92  %[time (1); I_L1 (2); I_RL (3); V_RL (4); I_Csnub (5); V_Csnub (6);
93  %I_Rsnub (7); V_Rsnub (8); I_dsnub (9); V_dsnub (10); I_MOV (11);
94  %V_MOV (12); I_switch (13); V_switch (14)]
95
96  S1 = size(Results.time); n = S1(1);
97  S2 = size(Results.Data); m = S1(2) + S2(2);
98
99  Variables = zeros(m,n);
100
101 Variables = [Results.time, Results.Data];
102 V1 = [];
103 V2= [];
104 I1 = [];
105 I2= [];
106
107 %%%% T_0
108 s = size(Variables(:,13));
109 for j = 1:s(1)
110     if abs(round(Variables(j,2),0))  <= round(I_fmax*0.02,0) &&
            Variables(j,1)>1.005e-3
111 t_0{i} = num2str(round(Variables(j,1)*1e6-1000,0));
112 t0 = Variables(j,1);
113 t0_ind = j;
114     break
115
116     end
117 end
118
119 V1(1:S1(1))=V_N;
120 VSmax(1:S1(1))=max(Variables(:,14));
121 Vd(1:S1(1))=min(Variables(1000:end,10));
122 Vm(1:S1(1))=V_MOV;
123
124 I1(1:S1(1))=I_Smax;
125 I2(1:S1(1))=I_fmax;
126 I3(1:S1(1))=I_N;
127
128 subplot(1,2,i)
129
```

```matlab
130   plot(Variables(:,1),Variables(:,14),'-k',Variables(:,1),Variables
          (:,2),'-y',...
131       Variables(:,1),Variables(:,13),':k', Variables(:,1),Variables
              (:,10),'-g',Variables(:,1),V1,'--k',Variables(:,1),...
132     VSmax,'--k',Variables(:,1),I1,'--k',Variables(:,1),I2,'--k',
            Variables(:,1),Vd,'--k',Variables(:,1),Vm,'--k')
133   if V_max > I_fmax
134   ylim([Vd(1)-500,VSmax(1) + 500])
135   else
136      ylim([Vd(1)-500,I_fmax + 500])
137   end
138
139
140   legend({'v_S','i_f','i_S','v_d'},'position',[0.3823+0.442*(i-1)  0.6
          0.05  0.1],'EdgeColor',[1  1  1])
141
142
143   xlim([t_f-20e-6,t0+200e-6])
144
145   I_fmax_str = num2str(round(I_fmax/1000,1));
146   I_max_str = num2str(round(I_Smax/1000,1));
147   V_i_str = num2str(round(V_N/1000));
148   V_max_str = num2str(round(VSmax(1)/1000,1));
149   Vd_str = num2str(round(Vd(1)/1000,1));
150   I_N_str = num2str(round(I_N/1000,1));
151   Vm_str = num2str(round(V_MOV/1000,2));
152
153
154   L_str = num2str(round(L_1*1e6,1));
155   t_str = num2str(round(t_b*1e6,1));
156
157   yval=[0 I_Smax V_N I_fmax VSmax(1) Vd(1) I_N V_MOV];
158   ylabels={'0', ['\newlineI_{max}^S=' I_max_str ' kA'],['V_{n} ='
          V_i_str ' kV'],...
159       ['I_{max}^f=' I_fmax_str ' kA'], ['V_{max} =' V_max_str ' kV'
              ],...
160       ['V_{max}^d =' Vd_str ' kV'],['\newlineI_{N}=' I_N_str ' kA'],['
              V_{cl}=' Vm_str ' kV']};
161   [yval,ylabels] = sort_val_labels(yval,ylabels);
162
163   yticks(yval)
164   yticklabels(ylabels)
165
166    a = get(gca,'YTickLabel');
167    set(gca,'YTickLabel',a,'fontsize',8)
```

```
168
169  title (['L_1 = ' L_str ' \muH'])
170
171  xlabel ('time [s]')
172
173
174  %%%% find values %%%%
175
176
177  Vmax{i} = num2str (round (max (Variables (:,14))/1000,2));
178  Imaxf{i} = num2str (round (max (Variables (:,2))/1000,2));
179  Lreq{i} = num2str (round (L_s*1e6,2));
180  Creq{i} = num2str (round (C_s*1e6,2));
181  Rreq{i} = num2str (R_s);
182  dImax = Imaxf{1};
183  dVmax = num2str (round (abs (min (Variables (:,10)))/1000,2));
184  didt = num2str (round (V_N*1e-9/L_s,2));
185  t_f_ind = find (Variables (:,1)==t_f,1);
186  t0_ind = find (round (Variables (100:end,2),1)==0,1);
187  i2{i} = num2str (round (trapz (Variables (:,1), Variables (:,9).^2),0));
188  dvdt = num2str (round (I_fmax(1)*1e-9/C_s,2));
189  end
190
191  %%%% print to latex table format %%%%%
192
193  %  L = 0  & L = 100 &  passive elements &      diode requiremets
                %%%%%
194  % Vm&Im&t & Vm&Im&t &        L & C R          Im & Vm & di/dt & dv/dt &
         i^2 dt
195
196  tab_str = [  ' & ' Vmax{1} ' & ' Imaxf{1} ' & ' t_0{1} ' & ' ...
197               Vmax{2} ' & ' Imaxf{2} ' & ' t_0{2} ' & ' Lreq{1} ' & '
                    ...
198               Creq{1} ' & ' Rreq{1} ' & ' dImax ' & ' dVmax ' & ' didt
                    ...
199               ' & ' dvdt ' & ' i2{1} ' \\[9pt]']
```

B   MATLAB code for designing and simulating the current limiting topology

```
1  %%%Adjustable parameters
2  clear all
3  figure
4  for i = 1:2
5
```

```matlab
6
7  t_sense = 5e-6;    %Time when fault is sensed [s]
8
9  t_s_delay = 0.048e-6;
10 t_fall = 0.018e-6;
11 I_max = 3360;    %Max current of swithing device
12 V_max = 17000;    %Max voltage of switching device
13 P_max = 109.2e3;
14 if i == 2
15 L_1 = 99.999e-6;    %Inductance between breaker and fault
16 elseif i == 1
17     L_1 = 0.001e-6;
18 end
19 %time parameters
20 t_f = 1e-3;            %Time of fault insidence [s]
21 t_b = t_s_delay + t_sense;    %total delay
22 t_open = t_f + t_b;    %time when switch is ctually opened
23 t_stop = t_open + 1e-3;            %Stop simulation
24 %General system parameters
25
26 V_N = 15e3;    %DC voltage [V]
27 I_N = 1.5e3;    %Nominal system current
28 I_thresh = 3000;  %current sensing threshold for breaking
29
30 L_max = 100e-6;
31 L_2 = L_max-L_1;    %Inductance between fault and load
32 L_s = V_N*t_b/(I_max-I_N);    %inductance before breaker
33 L_t = L_s+L_1;
34
35 R_L = V_N/I_N;   %Load resistance
36 R_fault=0.00001;            %Fault resistance
37
38 %Main switch (Semiconductor device)
39  R_on = 1e-3;            %equilvalent on-state resistance of main switch
     %turn-on delay of switch
40
41  I_Smax(i) = I_N + V_N*t_b/(L_1+L_s);
42
43 %Snubber circuit
44 V_fds = 0.8;            %forward voltage of snubber diode [V]
45 R_ds = 1e-3;            %on-state resistance of snubber diode [Ohm]
46 C_s = 2*I_Smax(1)^2*t_fall/(27*P_max);            %snubber capacitance [F
     ]
47
48
```

```matlab
49  I_fmax(i)= sqrt(I_Smax(i)^2+C_s*V_N^2/(L_1+L_s));
50
51  if i == 1
52  %R_d
53  syms x t
54
55  omega = 1/sqrt(C_s*L_t);
56  zet = sqrt(L_t/C_s)/(2*x);
57
58  OS_v = omega*(V_N*L_t/x+I_fmax*L_t)*exp(-(zet/sqrt(1-zet^2))*atan(
        sqrt(1-zet^2)/zet));
59
60  t_OS = atan(sqrt(1-zet^2)/zet)/(sqrt(1-zet^2)*omega);
61
62  s1 = omega*(zet+sqrt(zet^2-1));
63  s2 = omega*(zet-sqrt(zet^2-1));
64
65  c_v = (1 + omega*(exp(-s1*t_OS)/s1- exp(-s2*t_OS)/s2)/(2*sqrt(zet
        ^2-1)))*V_N;
66
67  tot = OS_v + c_v - V_max;
68
69  R_d = vpasolve(tot,x,1);
70  end
71
72  %time to 2%
73
74    zet = sqrt(L_t/C_s)/(2*R_d);
75
76  s1 = omega*(zet+sqrt(zet^2-1));
77  s2 = omega*(zet-sqrt(zet^2-1));
78
79  syms t
80
81  D = -(s1-s2)/2;    E = -(s1+s2)/2;        K = E/D;
82
83  time = exp(-K*t)*(cosh(-t)-K*sinh(-t))-0.02;
84
85  OS_v = omega*(V_N*L_t/R_d+I_fmax*L_t)*exp(-(zet/sqrt(1-zet^2))*atan(
        sqrt(1-zet^2)/zet));
86
87  sol = vpasolve(time,t);
88  t2(i) =abs(sol)/abs(D)
89
90  %Run simulation
```

```matlab
91  R_d = double(R_d);

92

93  sim('Limiting_breaker.slx')

94

95  %Storing variables in following format

96

97  %[time (1); I_L1 (2); I_RL (3); V_RL (4); I_Csnub (5); V_Csnub (6);
98  %I_Rsnub (7); V_Rsnub (8); I_dsnub (9); V_dsnub (10); I_MOV (11);
99  %V_MOV (12); I_switch (13); V_switch (14)]

100

101  S1 = size(Results.time); n = S1(1);
102  S2 = size(Results.Data); m = S1(2) + S2(2);

103

104  Variables = zeros(m,n);

105

106  Variables = [Results.time, Results.Data];
107  V1 = [];
108  V2= [];
109  I1 = [];
110  I2= [];

111

112  V1(1:S1(1))=V_N;
113  VSmax(1:S1(1))=max(Variables(:,2));
114  Vd(1:S1(1))=min(Variables(:,6));
115  Id(1:S1(1))=max(Variables(:,5));
116  Vds(1:S1(1))=min(Variables(:,8));

117

118

119  I1(1:S1(1))=I_Smax(i);
120  I2(1:S1(1))=I_fmax(i);
121  ymin=-1000;

122

123  subplot(1,2,i)

124

125  plot(Variables(:,1),Variables(:,2),'-k',Variables(:,1),Variables
         (:,3),'-y',...
126       Variables(:,1),Variables(:,4),':k',Variables(:,1),Variables(:,5)
             ,'-g',...
127       Variables(:,1),Variables(:,8),':g',Variables(:,1),Variables(:,9)
             ,'-k',...
128       Variables(:,1),V1,'--k',Variables(:,1),VSmax,'--k',Variables
             (:,1),...
129       I1,'--k',Variables(:,1),I2,'--k',Variables(:,1),Id,'--k',
         Variables(:,1),Vds,'--k')

130
```

```matlab
131   if  V_max > I2(1)
132   ylim([Vds(1)-500,V_max + 500])
133   else
134       ylim([Vds(1)-500,I2(1) + 500])
135   end
136
137   legend({'v_S','i_f','i_S','i_{Df}','v_{Ds}'},'position'
          ,[0.3823+0.442*(i-1) 0.6 0.05 0.1],'EdgeColor',[1 1 1])
138
139
140   Id_str = num2str(round(Id(1)/1000,1));
141   I_fmax_str = num2str(round(I_fmax(i)/1000,1));
142   I_max_str = num2str(round(I_Smax(i)/1000,1));
143   V_i_str = num2str(round(V_N/1000));
144   V_max_str = num2str(round(VSmax(i)/1000,1));
145   Vd_str = num2str(round(Vd(i)/1000,1));
146   I_N_str = num2str(round(I_N/1000,1));
147   Vds_str = num2str(round(Vds(1)/1000,1));
148
149
150   L_str = num2str(round(L_1*1e6,1));
151   t_str = num2str(round(t_b*1e6,1));
152
153   yval = [];
154   ylabels = [];
155
156   yval=[0 I_Smax(i) V_N I_fmax(i) VSmax(i) I_N Vd(i) Id(1) Vds(1)];
157   ylabels={'0', ['\newline\newline\newlineI_{max}^S=' I_max_str ' kA'
          ],['V_{i} =' V_i_str ' kV'],...
158       ['\newline\newlineI_{max}^f=' I_fmax_str ' kA'], ['V_{max} ='
          V_max_str ' kV'],...
159       ['\newline\newlineI_{N}=' I_N_str ' kA'],['V_{max}^{Df} ='
          Vd_str ' kV'],['I_{max}^{Df}=' Id_str ' kA'],['V_{max}^{Ds} =
          ' Vds_str ' kV']};
160   [yval,ylabels] = sort_val_labels(yval,ylabels);
161
162   yticks(yval)
163   yticklabels(ylabels)
164
165    a = get(gca,'YTickLabel');
166    set(gca,'YTickLabel',a,'fontsize',8)
167
168   title(['L_1 = ' L_str ' \muH'])
169
170   xlabel('time [s]')
```

```matlab
171
172
%%%% find values %%%%
%%%% T_0
s = size(Variables(:,3));
for j = 1:s(1)
    if abs(round(Variables(j,2),0)) <= round((VSmax(i)-V_N)*0.02+
        V_N,0) && Variables(j,1)>1.2e-3
t_0{i} = num2str(round(Variables(j,1)*1e6-1000,0));
t0 = Variables(j,1);
t0_ind = j;
    break

    end
end

xlim([t_f-20e-6,Variables(t0_ind,1)+50e-6+500e-6])

Vmax{i} = num2str(round(max(Variables(:,2))/1000,2));
Imaxf{i} = num2str(round(max(Variables(:,3))/1000,2));
Lreq{i} = num2str(round(L_s*1e6,2));
Creq{i} = num2str(round(C_s*1e6,2));
Rreq{i} = num2str(double(R_d));
dsImax = Imaxf{1};
dfImax = num2str(round(max(Variables(:,5))/1000,2));
dfVmax = num2str(round(V_N/1000,2));
dsVmax = num2str(round(-Vds(1)/1000,2));
didtf = num2str(round(V_N*1e-9/L_s,2));
didts = num2str(round(-Vds(1)*1e-9/L_s,2));

t_f_ind = find(Variables(:,1)==t_f,1);
t0_ind = find(round(Variables(100:end,2),1)==0,1);
if2{i} = num2str(round(trapz(Variables(:,1), Variables(:,5).^2),0));
is2{i} = num2str(round(trapz(Variables(:,1), Variables(:,7).^2),0));
dvdts = num2str(round(I_fmax(1)*1e-9/C_s,2));
dvdtf = num2str(round(max(Variables(:,5))*1e-9/C_s,2));

end

%%%% print to latex table format %%%%%

%   L = 0   & L = 100 &   passive elements &   diode requiremets
    %%%%%
% Vm&Im&t & Vm&Im&t &       L & C R        Im & Vm & di/dt & i^2 dt
```

```matlab
214   tab_str = [ '&' Vmax{1} '&' Imaxf{1} '&' t_0{1} '&' ...
215           Vmax{2} '&' Imaxf{2} '&' t_0{2} '&' Lreq{1} '&' ...
              ...
216           Creq{1} '&' Rreq{1} '&' dfImax '/' dsImax '&' ...
              dfVmax '/' dsVmax '&' didtf ...
217           '/' didts '&' dvdtf '/' dvdts '&' if2{1} '/' is2{1} ...
              ' \\[9pt]']
```

C MATLAB code for designing and simulating the resistive topology

```matlab
1   clear all
2   figure
3   for i =1:2
4   %%%Adjustable parameters
5
6   strategy = 2; %choose strategy 1 or 2
7   t_sense = 5e-6;  %Time when fault is sensed [s]
8   t_reclose = 2e-3;
9   t_s_delay = 0.048e-6;
10  t_fall = 0.018e-6;
11  I_max = 3360;    %Max current of swithing device
12  V_max = 17000;   %Max voltage of switching device
13  P_max = 109.2e3;
14  I_max_C = 3360;
15  if i == 2
16  L_1 = 99.999e-6;    %Inductance between breaker and fault
17  elseif i == 1
18      L_1 = 0.001e-6;
19  end
20  %time parameters
21  t_f = 1e-3;           %Time of fault insidence [s]
22  t_b = t_s_delay + t_sense;    %total delay
23  t_open = t_f + t_b;   %time when switch is ctually opened
24  t_stop = t_open + 1e-3;                %Stop simulation
25  %General system parameters
26
27  V_N = 15e3;      %DC voltage [V]
28  I_N = 1.5e3;     %Nominal system current
29  I_thresh = 3000; %current sensing threshold for breaking
30
31  L_max = 100e-6;
32  L_2 = L_max-L_1;     %Inductance between fault and load
33  L_s = V_N*t_b/(I_max-I_N/2)/2; %inductance before breaker
34  L_t = L_s+L_1;
```

```matlab
35  L_t_max = L_max + L_s;

36

37

38  R_L = V_N/I_N;    %Load resistance
39  R_fault=0.00001;         %Fault resistance

40

41  %Main switch (Semiconductor device)
42    R_on = 1e-3;          %equilvalent on-state resistance of main switch
        %turn-on delay of switch

43

44    I_Smax(i) = I_N/2 + V_N*t_b/(L_s)/2;

45

46  %Snubber circuit
47  V_fds = 0.8;         %forward voltage of snubber diode [V]
48  R_ds = 1e-3;         %on-state resistance of snubber diode [Ohm]
49  C = 2*I_Smax(1)^2*t_fall/(27*P_max);       %snubber capacitance [F]

50

51

52

53  %R_d and switching limits
54  tswitch = 1.145e-3;
55       toff = 1.195e-3;
56    if strategy == 1

57

58        [R_d,I_min_2,I_02,V_max] = resistive_opt_t(L_s,L_t_max,C,V_N,
            I_N,t_b)
59        I_s = V_N/R_d;

60

61        R_d = double(subs(R_d));
62          if isempty(R_d) == 1 || R_d <= 0
63              error('optimal R could not be solved. Try changing initial
                  guess')
64          end
65    elseif strategy == 2
66        tswitch = 1.05e-3;
67        [R_d,I_min_2,I_02,L_s,C] = resistive_opt_V(L_s,L_1,C,V_N,I_N,
            V_max,I_max_C,t_b);
68        if isempty(R_d) == 1 || R_d <= 0
69            error('optimal R could not be solved. Try changing initial
                guess')
70        end
71    end

72

73

74  %Run simulation
```

```matlab
75  if I_min_2 < 0
76      I_min_2 = 0;
77  elseif I_min_2 > I_02
78      I_min_2 = I_02 -1;
79  end
80
81  %I_min_2 = real(I_min_2);
82
83  sim('resistive.slx')
84
85  %Storing variables in following format
86
87  %[time (1); v_S (2); i_f (3); i_S (4) ]
88
89  S1 = size(Results.time); n = S1(1);
90  S2 = size(Results.Data); m = S1(2) + S2(2);
91
92  Variables = zeros(m,n);
93
94  Variables = [Results.time, Results.Data];
95  V1 = [];
96  V2= [];
97  I1 = [];
98  I2= [];
99
100 I_fmax(i)=max(Variables(:,3));
101
102 V1(1:S1(1))=V_N;
103 V2(1:S1(1))=V_max;
104 Vd(1:S1(1))=min(Variables(:,6));
105
106 I1(1:S1(1))=I_Smax(i);
107 I2(1:S1(1))=I_fmax(i);
108 ymin=Vd(1)-500;
109
110 %%%% T_0
111 s = size(Variables(:,1));
112 for k = 100:s(1)
113     if round(double(Variables(k,3)),0) <= round(I_fmax*0.02,0)
114 t_ind = k+100;
115 t_0{i} = num2str(round(Variables(t_ind,1)*1e6-1000,0));
116     break
117     end
118 end
119
```

```matlab
120    subplot(1,2,i)
121
122    plot(Variables(:,1),Variables(:,2),'-k',Variables(:,1),Variables
           (:,3),'-y',...
123        Variables(:,1),Variables(:,4),':k',...%Variables(:,1),Variables
               (:,5),'--k',...
124        Variables(:,1),Variables(:,6),'-g',...
125        Variables(:,1),V1,'--k',Variables(:,1),...
126        V2,'--k',Variables(:,1),I1,'--k',Variables(:,1),I2,'--k',
               Variables(:,1),Vd,'--k')
127    xlim([t_f-20e-6,Variables(t_ind,1)+100e-6])
128    ylim([ymin,V_max + 500])
129
130    legend({'v_S','i_f','i_{S_1}',... 'i_{S_C}',
131        'v_D'},'position',[0.38+0.442*(i-1) 0.6 0.05 0.1],'box','off')
132
133    I_fmax_str = num2str(round(I_fmax(i)/1000,1));
134    I_max_str = num2str(round(I_Smax(i)/1000,1));
135    V_i_str = num2str(round(V_N/1000));
136    V_max_str = num2str(round(V_max/1000,1));
137    Vd_str = num2str(round(Vd(1)/1000,1));
138    I_N_str = num2str(round(I_N/1000,1));
139
140
141    L_str = num2str(round(L_1*1e6,1));
142    t_str = num2str(round(t_b*1e6,1));
143
144    yval = [];
145    ylabels = [];
146
147    yval=[0 I_Smax(i) V_N I_fmax(i) V_max I_N Vd(1)];
148    ylabels={'0', ['I_{max}^S=' I_max_str ' kA'],['V_{i} =' V_i_str ' kV
           '],...
149        ['I_{max}^f=' I_fmax_str ' kA'], ['V_{max} =' V_max_str ' kV'
               ],...
150        ['I_{N}=' I_N_str ' kA'], ['V_{max}^D =' Vd_str ' kV']};
151    [yval,ylabels] = sort_val_labels(yval,ylabels);
152
153    yticks(yval)
154    yticklabels(ylabels)
155
156     a = get(gca,'YTickLabel');
157     set(gca,'YTickLabel',a,'fontsize',6)
158
159    title(['L_1 = ' L_str ' \muH'])
```

```matlab
160
161  xlabel('time [s]')
162
163
164  %%%% find values %%%%
165
166
167  Vmax{i} = num2str(round(max(Variables(:,2))/1000,2));
168  Imaxf{i} = num2str(round(max(Variables(:,3))/1000,2));
169  Lreq{i} = num2str(round(L_s*1e6,2));
170  Creq{i} = num2str(round(C*1e6,2));
171  Rreq{i} = num2str(double(R_d));
172  dImax = Imaxf{1};
173  dVmax = num2str(round(-Vd(1)/1000,1));
174  didt = num2str(round(V_N*1e-9/L_s,2));
175  t_f_ind = find(Variables(:,1)==t_f,1);
176  t0_ind = find(round(Variables(100:end,2),1)==0,1);
177  is2(i) = round(trapz(Variables(:,1), Variables(:,8).^2),0);
178  Is2 = num2str(max(is2));
179  ic2(i) = round(trapz(Variables(:,1), Variables(:,9).^2),0);
180  Ic2 = num2str(max(ic2));
181  dvdt = num2str(round(I_fmax(1)*1e-9/C,2));
182
183  end
184
185  %%%% print to latex table format %%%%%
186
187  %   L = 0   & L = 100 &   passive elements &   diode requiremets
           %%%%%
188  % Vm&Im&t & Vm&Im&t &         L & C R         Im & Vm & di/dt & i^2 dt
189
190  tab_str = [ ' & ' Vmax{1} ' & ' Imaxf{1} ' & ' t_0{1} ' & ' ...
191              Vmax{2} ' & ' Imaxf{2} ' & ' t_0{2} ' & ' Lreq{1} ' & '
                ...
192              Creq{1} ' & ' Rreq{1} ' & ' dImax '/' dImax ' & ' dVmax
                '/' '-' ' & ' didt '/' didt ...
193              ' & ' dvdt '/' '-' ' & ' Is2 '/' Ic2 ' \\[9pt]']
```

C.1   MATLAB code for function resistive$_opt_t$

```matlab
1  function [R_d, I_min_2, I_02, V_max] = resistive_opt_t(L_min,L_max,C,
      V_i,I_n,t_b)
2
3  syms R
4
5
```

```matlab
6   zeta_max = sqrt(L_max/C)/(2*R);          zeta_min = sqrt(L_min/C)/(2*R);
7  omega_max = 1/sqrt(L_max*C);              omega_min = 1/sqrt(L_min*C);
8  omega_d_max = omega_max*sqrt(1-zeta_max^2);  omega_d_min = omega_min*
       sqrt(1-zeta_min^2);
9
10  I_01_max = I_n + V_i*t_b/L_max;          I_01_min = I_n + V_i*t_b/L_min;
11  I_02_max = sqrt(I_01_max^2 + C*(V_i^2)/L_max);          I_02_min = sqrt(
       I_01_min^2 + C*(V_i^2)/L_min);
12
13  t_m = atan(sqrt(1-zeta_min^2)/zeta_min)/(sqrt(1-zeta_min^2)*
       omega_min);
14  V_im= I_02_min*(L_min*omega_min*exp(-zeta_min*omega_min*t_m));
15  V_diff = V_i*2*(zeta_min/sqrt(1-zeta_min^2))*sin(omega_min*sqrt(1-
       zeta_min^2)*t_m)*exp(-zeta_min*omega_min*t_m);
16
17  V_m_2 = V_i + V_im - V_diff;
18
19  I_min_2 = -I_02_max*exp(-zeta_max*pi/sqrt(1-zeta_max^2))+V_i*(1+exp
       (-zeta_max*pi/sqrt(1-zeta_max^2)))/R;
20
21  V_m_1 = sqrt(L_max/C)*I_min_2+V_i;
22
23  eq = V_m_2 - V_m_1;
24
25  R_d=vpasolve(eq,R,10);
26
27  I_min_2 = -I_02_max*exp(-zeta_max*pi/sqrt(1-zeta_max^2))+V_i*(1+exp
       (-zeta_max*pi/sqrt(1-zeta_max^2)))/R;
28  I_min_2 = double(subs(I_min_2,R_d));
29  I_02 = double(I_02_min);
30  V_max = double(subs(V_m_2,R_d));
31  end
```

C.2   MATLAB code for function resistive$_o pt_V$

```matlab
1  function [R_d,I_min_2, I_02,L_s,C] = resistive_opt_V(L_s,L_1,C,V_N,
       I_n,V_max,I_max_C,t_b)
2
3  %Find R
4   syms R
5
6  zeta = sqrt(L_s/C)/(2*R);
7  omega = 1/sqrt(L_s*C);
8  omega_d = omega*sqrt(1-zeta^2);
9
10  I_01_R = I_n + V_N*t_b/L_s;
```

107

```matlab
11   I_02_R = sqrt(I_01_R^2 + C*(V_N^2)/L_s);
12    t_m = atan(sqrt(1-zeta^2)/zeta)/(sqrt(1-zeta^2)*omega);
13    V_im= I_02_R*(L_s*omega*exp(-zeta*omega*t_m));
14    V_diff = V_N*2*(zeta/sqrt(1-zeta^2))*sin(omega*sqrt(1-zeta^2)*t_m)*
         exp(-zeta*omega*t_m);
15
16    V_m_2 = V_N + V_im - V_diff;
17
18    eq = V_m_2 - V_max;
19
20    R_d=vpasolve(eq,R,1);
21    R_d=double(R_d);
22
23    if V_max/R_d >= I_max_C
24        R_d = V_max/I_max_C;
25
26        syms L_s
27   C = (L_s+100e-6)/(R_d^2)/4;
28
29   zeta = sqrt(L_s/C)/(2*R_d);
30   omega = 1/sqrt(L_s*C);
31   omega_d = omega*sqrt(1-zeta^2);
32
33   I_01_L = I_n + V_N*t_b/L_s;
34   I_02_L = sqrt(I_01_L^2 + C*(V_N^2)/L_s);
35    t_m = atan(sqrt(1-zeta^2)/zeta)/(sqrt(1-zeta^2)*omega);
36    V_im_L= I_02_L*(L_s*omega*exp(-zeta*omega*t_m));
37    V_diff_L = V_N*2*(zeta/sqrt(1-zeta^2))*sin(omega*sqrt(1-zeta^2)*t_m
         )*exp(-zeta*omega*t_m);
38
39    V_m_2_L = V_N + V_im_L - V_diff_L;
40
41
42    eq = V_m_2_L - V_max;
43
44    L_s =vpasolve(eq,L_s,100e-6);
45    L_s = double(L_s);
46    C = (L_s+100e-6)/(R_d^2)/4;
47
48   %Find initial conditions
49   L_t = L_s+L_1;
50   zeta1 = sqrt(L_t/C)/(2*R_d);
51   omega1 = 1/sqrt(L_t*C);
52   omega_d = omega1*sqrt(1-zeta1^2);
53
```

```matlab
54   I_01 = I_n + V_N*t_b/L_t;
55   I_02 = sqrt(I_01^2 + C*(V_N^2)/L_t);
56
57   %strategy if L is sensed
58   %if L_1<80e-6
59   syms I_switch
60    t_m1 = atan(sqrt(1-zeta1^2)/zeta1)/(sqrt(1-zeta1^2)*omega1);
61   V_im_switch= I_switch*(L_t*omega1*exp(-zeta1*omega1*t_m));
62    V_diff_switch = V_N*2*(zeta1/sqrt(1-zeta1^2))*sin(omega1*sqrt(1-
        zeta1^2)*t_m1)*exp(-zeta1*omega1*t_m1);
63
64    eq_switch = V_N + V_im_switch - V_diff_switch - V_max;
65
66    I02 = vpasolve(eq_switch,I_switch,1000);
67    I_02 = double(subs(I02,L_s));
68   %end
69
70   I_min_2 = -I_02*exp(-zeta1*pi/sqrt(1-zeta1^2))+V_N*(1+exp(-zeta1*pi/
        sqrt(1-zeta1^2)))/R_d;
71
72    else
73        %Find initial conditions
74   L_t = L_s+L_1;
75   C = (L_s+100e-6)/(R_d^2)/4;
76   zeta = sqrt(L_t/C)/(2*R_d);
77   omega = 1/sqrt(L_t*C);
78   omega_d = omega*sqrt(1-zeta^2);
79
80   I_01 = I_n + V_N*t_b/L_t;
81   I_02 = sqrt(I_01^2 + C*(V_N^2)/L_t);
82   I_min_2 = -I_02*exp(-zeta*pi/sqrt(1-zeta^2))+V_N*(1+exp(-zeta*pi/
        sqrt(1-zeta^2)))/R_d;
83   L_s=L_s;
84    end
85
86   end
```

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