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Power Factor Correction for a Bidirectional On-Board Charger for Electric Vehicles and Plug-in Hybrid Electric Vehicles

A fundamental study of the bidirectional totem-pole PFC

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Abstract

With the beginning implementation of a ”smart grid” in industrialized countries increasing the load flexibility of customers, as well as communication with the grid operators, a potential market for bidirectional on-board chargers (OBC) is emerging. The OBC is the electric vehicle charger located within the vehicle, operating as a link between the DC-voltage battery and the AC grid voltage in electricity sockets anywhere, thus working at a universal voltage range (85Vrms-265Vrms) with rated power in the range of 1.9kW to 3.5kW. To maximize the real power drawn by these OBCs, they are designed with power factor correction (PFC) converters at the AC grid interface, shaping the drawn AC current sinusoidally and in phase with the AC voltage, to maximize the power factor. Thus, a bidirectional OBC would necessarily require a bidirectional PFC. In this master's thesis, a simulation model is developed for a bidirectional totem-pole PFC, attempting to verify the use of this topology as the mentioned bidirectional OBC PFC. The work is focused on describing the basic bidirectional operation of the bidirectional totem-pole PFC, deriving expressions for currents, voltages and losses, as well as for the gate logic and control system. Average current mode control is used, with cascaded current and voltage control including PI controllers and Symmetrical optimum tuning. To verify the simulation model for the power levels and demands of an OBC, the main components are dimensioned to achieve 98% efficiency at 230Vrms, 3.5kW and 90kHz switching frequency, implementing GaN eHEMTs in the fast-switching leg of the totem-pole. At last, simulations are performed, showing that the PFC is able to achieve a power factor of 0.998 and a THD of 5% in both G2V and V2G, without a DM filter on the AC side.

Sammendrag

Etter hvert som implementeringen av ”smarte nett” er i ferd med å skyte fart i industrialiserte land, med økt lastfleksibilitet på kundesiden og økt kommunikasjon mot nettoperatørene, begynner det å åpne seg et marked for bidireksjonelle såkalte ”on-board chargers” (OBC-er). En OBC er elbilladeren som er plasserte inne i elbilen og fungerer som en link mellom elbilbatteriet - som krever DC-spenning - og AC-spenningen i strømuttaket, hvilket betyr at den må designes for å operere ved universell AC-spenning (85Vrms-265Vrms) og nominelle effektnivåer mellom 1.9kW og 3.5kW. For å maksimere den reelle effekten trukket av OBC-en, er de designet med såkalte ”power factor corretion”-omformere (PFC-er) på AC-siden ut mot nettet. Denne kontrollerer AC-strømmen som trekkes til å være formet som en sinus og i fase med AC-spenningen på nettet, for på den måten å maksimere effektfaktoren. Av den grunn, vil nødvendigvis en bidireksjonell OBC behøve en bidireksjonell PFC. I denne masteravhandlingen vil det bli utviklet en såkalt bidireksjonell ”totem-pole PFC”, mens det forsøkes å verifisere hvorvidt dennetopologien egner seg for bruk i en bidireksjonell PFC for en OBC. Hovedfokus for oppgaven vil ligge i å beskrive hvordan en bidireksjonell totem-pole PFC fungerer grunnleggende, mens det vil utledes uttrykk for strømmer, spenninger og tap i omformeren, samt gate-logikken og kontrollsystemet. ”Average current mode” brukes i kontrollsystemet, med dobbel kontrollsløyfe med strøm- og spenningskontroll, begge to med PI-regulatorer dimensjonert med Symmetrisk optimum. For å verifisere simuleringsmodellen for de aktuelle spennings- og effektnivåene, dimensjoneres de viktigste komponentene til å opnå 98% virkningsgrad ved 230Vrms, 3,5kW og 90kHz switchefrekvens, med GaN eHEMT-er implementert i det hurtigswitchende totem-pole-benet. Til slutt ble det utført simuleringer av modellen, og disse viser at den bidireksjonelle totem-pole PFC-en oppnår en effektfaktor på 0.998 og en THD på 5% både under G2V og V2G, uten filter på AC-siden.

Preface

This master's thesis is conducted during the spring 2018, and it is the finishing work of a master's degree in Energy and Environmental Engineering at the Norwegian University of Science and Technology (NTNU), Department of Electric Power Engineering. The thesis focuses on power electronics, and it is a continuation of a specialization project performed during the autumn 2017, both of which have been announced and guided by Valeo Siemens eAutomotive.

I would like to thank my supervisor, Roy Nilsen, for his valuable guidance and support through numerous guidance sessions throughout the year, and co-supervisor, Tore M. Undeland, for his expert advice. My sincere gratitude goes to Torbjørn Sørsdahl at Valeo Siemens for his effort, advice and guidance throughout the year. Thanks also to the rest of the staff at Valeo Siemens in Drammen who were ready to answer any of my questions without hesitation, during my stays there through the year.

Finally, I would like to place a warm thanks to my family for their loving support, and to my favourite Ingunn for letting me know when it is time to go home for the night.

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Abbreviations

AC:	Alternating Current
CCM:	Continuous Conduction Mode
CrCM:	Critical Conduction Mode
DAB:	Dual Active Bridge
DC:	Direct Current
DCM:	Discontinuous Conduction Mode
DM:	Direct Mode
DSO:	Distribution System Operator
EMI:	Electromagnetic Interference
ESR:	Equivalent Series Resistance
EV:	Electric Vehicle
G2V:	Grid-to-Vehicle
GaN:	Gallium Nitride
HEMT:	High Electron Mobility Transistor
MOSFET:	Metal-Oxide-Semiconductor Field-Effect Transistor
OBC:	On-Board Charger
PCB:	Printed Circuit Board
PHEV:	Plug-in Hybrid Electric Vehicle
PLL:	Phase-Locked Loop
PWM:	Pulse Width Modulation
RMS:	Root Mean Square
SHBM:	Single H-Bridge Modulation
SiC:	Silicon Carbide
THD:	Total Harmonic Distortion
V2G:	Vehicle-to-Grid
V2H:	Vehicle-to-Home
ZCS:	Zero-Current Switching
ZVS:	Zero-Voltage Switching

Chapter 1

Introduction

This master's thesis is a continuation of a specialization project work performed on the same topic.[4] For that reason, some of the work described in this thesis is based on some of the work performed and described in the specialization project report. The following figures are retrieved from the specialization project report:

- Figure 1.1
- Figure 2.1
- Figure 2.2
- Figure 2.3

Furthermore, the following sections contain large portions of text reproduction from the abovementioned specialization project report:

- Section 1.1
- Section 1.2
- Section 2.1
- Section 2.2

1.1 Motivation

In the quest of securing a more sustainable and renewable electric energy supply in industrialized countries, the implementation of a ”smart grid” is picking up pace. The smart grid concept incentivizes more distributed renewable electricity production and increased consumption flexibility for the customer.[5] This development is exemplified by the extensive roll-out of advanced electricity consumption measurement systems for all households in Norway and numerous countries in the European Union, as well as an increasing amount of distributed solar power built in e.g. Germany and California. [6, 7, 8, 9] The first tendency introduces a potential for substantial increase in communication and control at the consumer side of the electric power grid. The second introduces a possible problem of over-production at times of day with high solar irradiation, giving stability issues for the utilities [10]. Combined, these two imply both a possibility and a need for distributed energy storage in the grid, connecting battery storage units at the consumer end to even out the big hourly differences in power production.

One part of this distributed energy storage could be the main batteries of electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs) when these are connected to the electricity supply at home or at work. The number of EVs and PHEVs on the roads is increasing, and with that comes a big battery capacity that could be utilized for purposes other than vehicle propulsion. One example of such utilization is using EV batteries as electricity grid stabilizers through vehicle-to-grid (V2G) charging. At any time when a big load or generating unit is connected to or disconnected from the grid, there is an immediate power imbalance which causes a change in grid frequency. [11, Chapter 9] To ensure that the frequency stays within the limits of stability, charging or discharging a fleet of cars connected to the grid could cover some of this immediate power imbalance before the slower generators reacts after some seconds or minutes to completely cover the whole imbalance. A potential issue for EVs and PHEVs when enabling bidirectional charging is that the number of cycles increases. Since the battery degrades with every cycle, this would help degrade the battery faster.[12, 13] With this sort of V2G solution, however, utilizing the EV batteries as grid stabilizers, the charging and discharging would be high-power for a short period of time, meaning the battery would not fully charge or discharge. Such solutions are being tested these

days, where EV owners are paid for having their batteries available for the utility to draw or inject power whenever needed.[14, 15, 16] Furthermore, if one is to fully exploit the grid-conditioning potential of the bidirectional OBC, it could also be modified to be able to deliver and consume reactive power, serving as a reactive power compensator. [17]

Another possibility is that the battery owners control the power flow themselves, e.g. to store energy when the electricity price is low, say, when the car is connected to a power supply at work. Later in the evening the power could be sold back to the grid at a higher price, earning money from the price difference. Otherwise it could be supplied to the household when the electricity price is high, saving money. Moreover, a discussed concept is vehicle-to-home (V2H) charging, which allows the car battery to serve as an emergency power source, supplying critical loads during power outages.[18] Yet another possibility for exploiting the EV battery energy, is using the battery to provide standard grid-voltage AC power within the car, supplying applications like PC chargers, refrigerators or TVs. Furthermore, when campers today are in need of AC power for various devices, such as lighting, microwaves, small cooktops or again refrigerators, they use a DC-AC inverter connected to a bank of regular 12V car batteries.[19] If an AC power supply is made available also in the exterior of the EV, then this could replace the need for such solutions and even increase the available energy compared to the 12V battery bank.

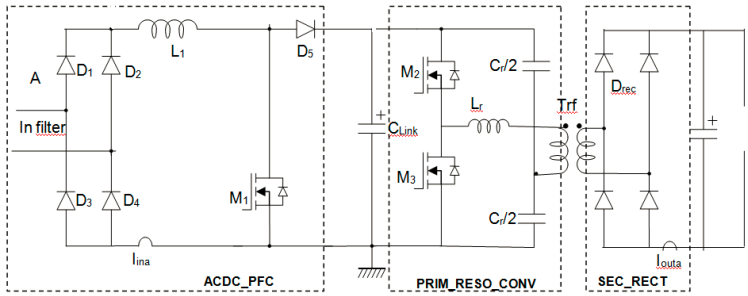


Figure 1.1: A sketch of the current Valeo Siemens OBC topology [1]

1.2 The Bidirectional On-Board Charger

A key to utilizing PHEV/EV batteries for non-propulsion purposes could be implementing a bidirectional on-board charger (OBC). Being located within the car, the OBC is an important part of any EV; it is the interface between the DC-voltage EV battery and standard AC power outlets, such as the wall socket at home or in the workplace. Since at the moment, vehicles are standing still during large parts of the day, mostly at home or at work, bidirectional charging should be enabled while connected at these locations. To avoid making the owners of house and workplace invest in DC charging stations, the on-board charger could be made with bidirectional power flow capability to enable V2G charging during this time. Moreover, providing solutions like in-car or exterior grid-voltage AC power supplies would require the DC-AC conversion to happen within the car. Enabling bidirectional conduction capability in OBCs could thus indeed be useful, both for V2G charging and the in-car or exterior solution.

One challenge of a standardized OBC solution is that it has to be able to operate efficiently in a universal AC-voltage range (85-265Vrms), since the grid voltage differs between countries and the charger should be able to operate anywhere.[20] Consequently, the input power will also vary, with maximum power ranging roughly between 1.4 kW and 3.5kW, depending on the AC voltage.[21] Another challenge is that since the OBC is located within the car, it has to be small in size and light in weight, to minimize the physical footprint of the charger and extend the range of the vehicle.

The OBC most often comprises two stages.[22] This is exemplified by the sketch

of the OBC topology used by Valeo Siemens eAutomotive (hereby referred to as Valeo Siemens) reproduced in figure 1.1. Firstly, there is an AC-DC grid interface rectifier with power factor correction (PFC), sinusoidally shaping the drawn AC current in phase with the AC supply mains voltage, to maximize the power factor and remove low-order harmonics, while controlling the voltage ripple at the DC-link capacitor. The switching frequency of the PFC has to be kept high, in order to minimize the size of the inductor and the AC-side filter. At the same time, a higher switching frequency causes higher switching losses, reducing the efficiency. Also, IEC 61000-4-6 defines limits to the emitted EMI in the frequency range of 150kHz to 30MHz, so setting the switching frequency to exceed this lower limit would mean that all of the harmonics needs to be filtered, increasing the size of the filter. Cascaded through the DC-link with this PFC is a DC-DC converter with a high-frequency transformer for galvanic isolation. The DC-DC is controlling the battery-side voltage to be constant, for optimal performance. High switching frequency in the isolated DC-DC converter is decisive to minimize the weight and size of inductors and the transformer, again decreasing the size and weight of the whole OBC. However, in this case higher switching frequency does of course also cause higher switching losses. The efficiency has to be kept high, defined by Valeo Siemens to be above 94%, to maximize the charging speed.[1] The combined maximization of efficiency and power density (kW/dm^3) is always going to be a trade-off, as explained in [23] with the Pareto front and exemplified with a boost PFC, where at a certain optimal limit, the increasing one is going to require a complementary decrease in the other. This is the compromise of an OBC, where the wish is both high efficiency and high power density. Price is also an important factor, as an OBC would be mass produced and should not lead to a big increase in vehicle cost.

Up until this point, the majority of commercial OBC solutions have been made unidirectional, allowing only grid-to-vehicle (G2V) charging. To make the OBC capable of bidirectional power flow and V2G, there can be no passive diode bridge rectifiers or standalone freewheeling diodes. Some diodes can be removed, implementing more compact solutions, while some have to be replaced by transistors, making the whole charger more complex in terms of control. Every transistor needs its own drive circuit, meaning more transistors can also potentially require a bigger charger volume. For that reason minimizing the number of transistors is

something that has to be considered when developing a bidirectional OBC.

With the smart grid still in its birth, the nature of bidirectional charging is still not clear, and different potential modes of operation present different demands for the charger. If operated with the interior power outlet, using it for small TVs, refrigerators or laptop chargers, the charger would most likely be working at a low load for a long period of time. On the other hand, if the vehicle is connected to the grid, working in V2G operation, it could, as mentioned, either be used to sell the battery power to the utility for a good price at times of high demand, or the DSO could use the charger capacity for grid stabilizing purposes. The first case could give an even, high power transfer for hours at a time, while the latter would provoke power transfers at maximum rated power for seconds or minutes. The stress on components and operating efficiency would obviously be quite different in these different cases, and it would be difficult to optimize the charger design for all modes of operation. For that reason, it will be assumed in this evaluation that the charger will during V2G most often be under the control of the distribution system operator (DSO) to regulate stability. Therefore, the relevant PFC topologies will be evaluated considering operation at maximum load for short periods of time. The basis of this decision is that this type of operation has already been tested and considered. The lower efficiency when supplying interior power supply is considered to be of less importance because the drawn power will be lower, and thus the stress and power dissipation will be small.

1.3 The bidirectional PFC

Having understood the basic composition of an OBC, it is clear that in order to make a bidirectional OBC it is necessary with a bidirectional PFC. However, to design a bidirectional PFC, it is also necessary to understand the basic operation of a unidirectional PFC. A literature review on unidirectional and bidirectional PFCs was performed in the specialization project, and is attached in appendix B. This PFC introduction is based on that analysis. As stated there and above, the PFC is the grid interface of an OBC or another universal power supply, shaping the drawn AC current sinusoidally and in phase with the AC voltage, and controlling the internal DC-link voltage. The conventional boost PFC is structured as in the OBC topology in figure 1.1, consisting of a passive rectifier cascaded with a regular boost converter.[24, ch. 7-4] Here, the switching of the boost transistor is modulated to shape the fundamental inductor current according to the rectified AC voltage seen from the rectifier.

The PFC operates either in continuous conduction mode (CCM), critical conduction mode (CrCM) or discontinuous conduction mode (DCM), all of which are explained in more detail and visualized in appendix B. CCM and CrCM are the most commonly used, where CCM has the advantage of lower current ripple, applying less stress on the semiconductors and inductor and requiring a smaller direct-mode (DM) ac-side current filter, but at the same time yielding hard switching in both turn-on and turn-off with corresponding higher switching losses. CrCM, on the other hand, enables zero-current switching (ZCS) and possible zero-voltage switching (ZVS) due to the current reaching zero every switching cycle, reducing switching losses but at the same time generatng a large current ripple of twice the average current, increasing the stress on the components. For higher power applications it is common to operate in CCM, because the stress on the components would otherwise get too high.[2]

An obvious disadvantage of the boost PFC with regard to bidirectional conduction ability is the the presence of passive diodes both in the rectifier bridge and the freewheeling diode, and so these need to be removed. A first step in that direction is including the operation of the transistor and freewheeling diode into the rectifier bridge, making it a so-called bridgeless PFC, of which there are many variations.[25, 26] This integration has advantages with regards to losses, as the

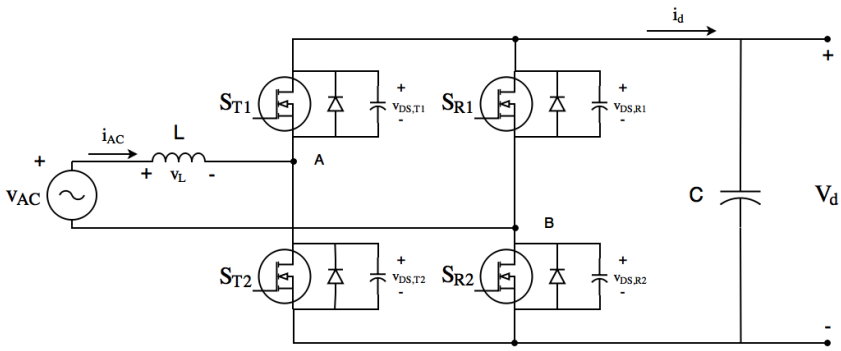


Figure 1.2: The basic bidirectional PFC topology

number of semiconductors in the conduction path is reduced from 3 to 2, reducing especially the conduction losses. Two simple and compact bridgeless topologies with regards to number of semiconductors are the basic bridgeless PFC and the totem-pole PFC, presented in figure B.3 in the appendix. In these topologies, the transistors are ”taking turns” operating as boost transistor every other half cycle and remaining turned off (basic bridgeless) or operating as the freewheeling diode (totem-pole) in the other. Out of the two, the basic bridgeless PFC has previously been the preferred topology, with the totem-pole PFC disregarded because of large reverse recovery losses in the MOSFET body diode during CCM operation.[25] On the other hand, a drawback of the basic bridgeless PFC is increased common mode (CM) noise due to the DC-link zero-potential floating with respect to the AC ground. This is explained in more detail in appendix B.

In recent advances, however, the totem-pole PFC has been found increasingly interesting when substituting the rectifier diodes for slow-switching MOSFETs, enabling negative current. That creates a bidirectional PFC topology, the bidirectional totem-pole PFC shown in figure 1.2. For lower-power applications, it has been found that techniques such as triangular current mode (TCM) and CrCM valley switching, enabling low- or zero-voltage switching by discharging the transistor parasiic capacitances through short-term negative currents, can increase efficiency of the totem-pole PFC. This is explained in more detail in appendix B.[3, 27, 28] Interleaving the fast-switching leg, hereby called the totem-leg, i.e. paralleling more than one totem-leg, also improves the efficiency and reduces the stress on the semiconductor components.[27, 29] This is however for lower power lev-

els; at the high power levels of an OBC (3.5kWmax) it is still desirable with CCM operation, to have component stress at a satisfying level. Moreover, given the size restriction of an OBC and that the DM filter does in fact make up one third of the OBC volume, it is beneficial that the lower current ripple in CCM implies a smaller DM filter size.[1]

Beneficially, the most recent advances in wide-bandgap power semiconductor devices show that the Gallium Nitride (GaN) High-Electron-Mobility Transistor (HEMT) has been shown to give improvements on the performance of totem-pole PFCs, when used in the fast-switching totem-leg. A literature study has been performed on GaN HEMTs and their application in bidirectional PFCs, and the results are presented in the paper attached in appendix C. The most notable advantage for application in the totem-pole PFC is that, unlike the MOSFET, the GaN HEMT does not contain a reverse body diode, thus solving the problem of reverse recovery losses during CCM operation. Moreover, the GaN HEMTs show superior conduction and switching characteristics all over, due to the combination of high breakdown field and the low-resistivity 2DEG layer. This is explained in more detail in appendix C. In [30] is presented a 1.5kW, 65kHz CCM-operated totem-pole PFC, showcasing an efficiency of 99%. Moreover, it is found through the literature study that currently most 1-phase bidirectional two-stage OBCs proposed in the scientific literature are using the bidirectional totem-pole PFC shown in figure 2.1 [31, 32, 33]. In fact, most proposed 1-phase bidirectional PFCs overall are using the bidirectional totem-pole topology [34, 35]. This indicates that it is possible to design an efficient 3.5kW CCM-operated bidirectional totem-pole PFC. For that reason, the bidirectional totem-pole PFC will be the topology of choice going forward in this master's thesis.

1.4 Scope of work

Although a few cases of the bidirectional totem-pole PFC has appeared in the scientific literature, as presented in the previous section, the author has not come across any verification of the nature its fundamental bidirectional operation. For that reason, the main objective of this master's thesis is to fill that hole, by deriving and developing a fundamental simulation model describing the bidirectional totem-pole PFC and its bidirectional operation. This simulation model will be implemented in Simulink. To verify the use of the bidirectional totem-pole PFC in a bidirectional OBC, the simulation model will be implemented with off-the-shelf components and a control system meeting some demands of a bidirectional OBC and PFC, shown in tables 1.1 and 1.2. The thesis is written in cooperation with Valeo Siemens eAutomotive and is intended to be a building block for further work on a bidirectional OBC, verifying or dismissing the bidirectional totem-pole PFC as a technology to take further. In that sense, describing the currents, voltages and losses in the basic operation of the topology will be important.

The topology will be investigated using MOSFETs and GaN HEMTs as the transistors, disregarding possible solutions with IGBTs. Furthermore, the PFC efficiency will be optimized for a standard AC voltage of 230Vrms, not designing from the efficiency at 120Vrms. The design will be aiming to approach the current Valeo Siemens PFC designs with regards to switching frequency and efficiency, to use similar components and compare performance. As for the control system and gate logic design, an emphasis will be put on making a solution which can be adapted to existing unidirectional boost PFC control systems and gate drives, to create a flexible solution. For the PFC control average current mode control, whith cascaded current and voltage loops containing PI controllers with Symmetrical optimum tuning.

In **chapter 2**, the basic operation of the bidirectional totem-pole PFC is described, deriving expressions for the currents and losses in the boost inductor, DC-link capacitor and transistors.

Chapter 3 will cover the design and dimensioning of the components, in particular the boost inductor, transistors and DC-link capacitor.

In **chapter 4** the bidirectional totem-pole control will be developed, deriving the

Table 1.1: Demands and specifications for the bidirectional universal OBC, from [1]

Parameter	Value
G2V	
Output DC voltage range	200Vdc - 1000Vdc
Max. output DC current	12 Adc
Input AC voltage range	85Vrms - 275Vrms
Max. input AC current	16Arms
Max. input frequency	45Hz - 65Hz
Max. power	3.5kW
Efficiency	$> 94\%$
Max. apparent power	3680VA
Lifetime	10 000 hours
V2G	
Input DC voltage range	200Vdc - 1000Vdc
Max. input DC current	12 Adc
Output AC voltage range	100Vrms - 250Vrms
Max. output AC current	16Arms
Max. output frequency	45Hz - 65Hz
Max. power	3.5kW
Efficiency	$> 91\%$
Max. apparent power	3680VA
THD	$< 3\%$
Lifetime (uncertain)	10 000 hours

gate drive and control system logic and tuning controllers and verifying through simulations.

Chapter 5 shows the results of some system level simulations.

Chapter 6 will discuss the design feasibility by evaluating simulation model shortcomings and comparing performance with existing solutions.

Table 1.2: PFC-specific demands and specifications

Parameter	**Value**
Efficiency G2V	>98%
Efficiency V2G	>97%
Min. DC-link voltage	340V
Max. DC-link voltage ripple	20V
Max. inductor current ripple	20%

Chapter 2

Basic operation of the bidirectional totem-pole PFC

Based on the reasoning in the introduction, the bidirectional totem-pole PFC was chosen as the most promising bidirectional PFC topology, and so now the operation of this topology must be explained in more detail. It is acknowledged that in order to comply with the current ripple restrictions of 20% (table 1.2), it is necessary to run the bidirectional totem-pole PFC in CCM. This section will consider its basic CCM operation, covering V2G discharging and G2V charging. Moreover, current and voltage waveforms will be derived and portrayed for the main components of the converter, including the boost inductor, the transistors and the DC-

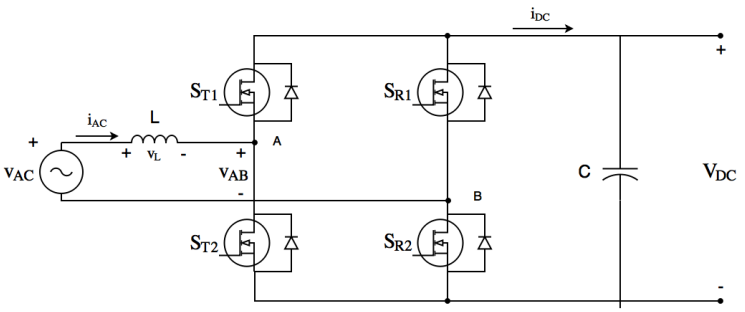


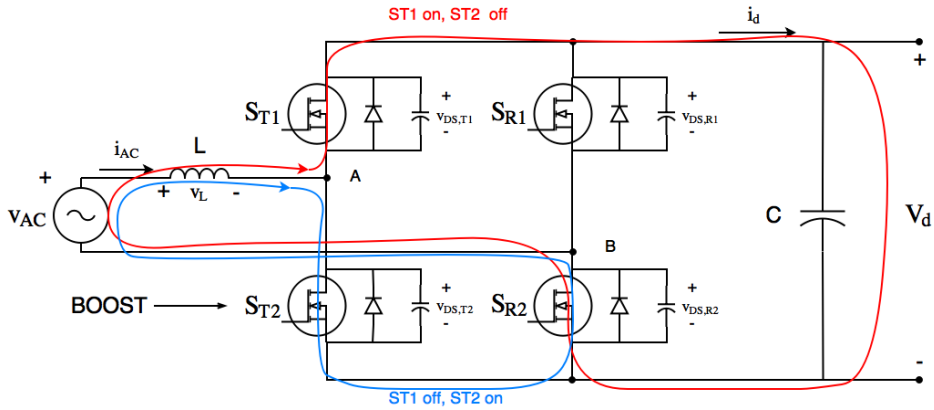
Figure 2.1: The basic bidirectional totem-pole topology

link capacitor. Expressions will be developed for RMS currents and conduction and switching losses for these components. The relevant bidirectional totem-pole topology is shown in figure 2.1, and in the following all variables and parameters will be referred to the notation in this figure.

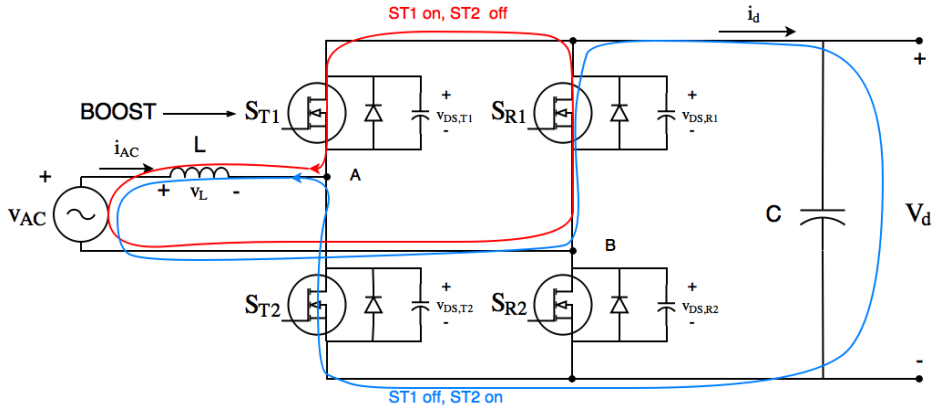
2.1 G2V operation

In G2V operation, with power flow from AC source to DC link, the totem pole is operated as a boost converter with PWM switching, to shape the fundamental waveform of the AC current i_{AC} like a sine in phase with the AC voltage v_{AC}. [24] The operation is sketched in figure 2.2. During the positive mains half cycle, the lower totem-leg switch, S_{T2} is operated with boost PWM switching (figure 2.2a), while the upper totem-leg switch S_{T1} is operated complementarily; when S_{T1} is on S_{T2} is off, and vice versa. S_{R2} is always on during the positive half cycle. During the negative mains voltage half cycle, S_{T1} is operated as a boost, S_{T2} is complementary and S_{R1} is conducting. The AC current is governed by (2.1), and from that controlled by the average v_{AB}, which is again controlled by the time-varying duty cycle, to be shaped like in figure B.2.

$$v_L = v_{AC} - v_{AB} = L\frac{di_{AC}}{dt} \tag{2.1}$$



(a) Mains voltage positive half cycle



(b) Mains voltage negative half cycle

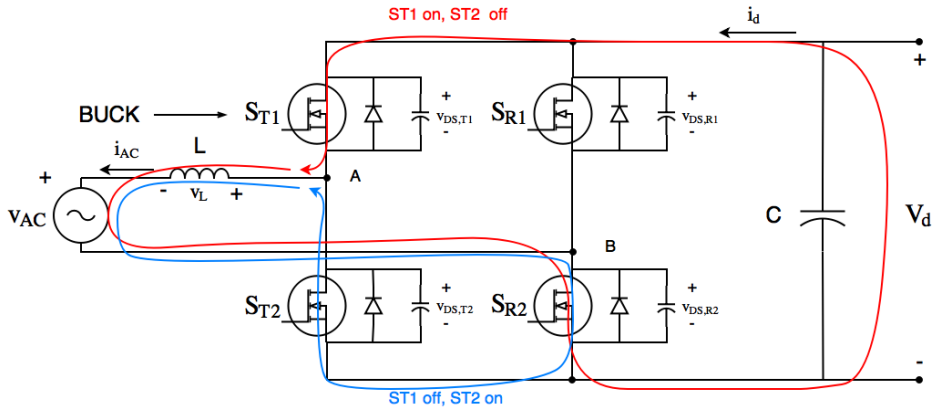
Figure 2.2: The G2V operation of the bidirectional totem-pole PFC.

2.2 V2G operation

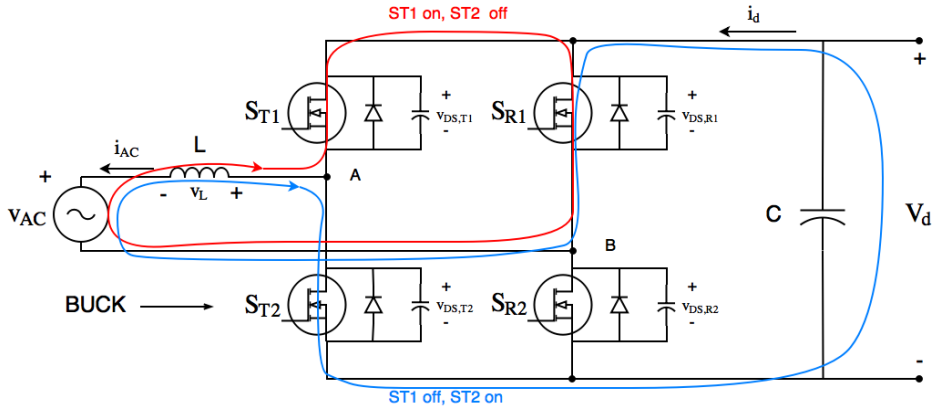
Conversely, with power flow from DC link to AC side in V2G operation, the totem-pole is operated as a buck converter, stepping down the voltage from the DC-link to AC-side [24]. The operation is sketched in figure 2.3. In this case, during the positive mains voltage half cycle, S_{T1} is operated with buck PWM switching, S_{T2} is complementary and S_{R2} is conducting, as indicated in figure 2.3a. During negative half cycle, S_{T2} is buck PWM controlled, S_{T1} is complementary and S_{R1} is conducting, as indicated in figure 2.3b. With AC current defined positive from DC-side to AC-side the inductor voltage changes polarity, so that the current is governed by (2.2).

$$v_L = v_{AB} - v_{AC} = L\frac{di_{AC}}{dt} \tag{2.2}$$

Still, this means the current is controlled by the time-varying duty cycle of the buck-operated switch, controlling v_{AB}, as it is in the boost operation.



(a) Mains voltage positive half cycle



(b) Mains voltage negative half cycle

Figure 2.3: The V2G operation of the bidirectional totem-pole PFC.

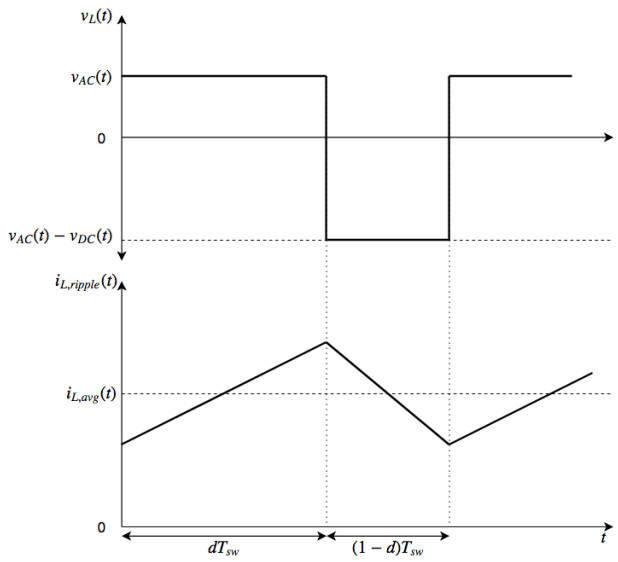


Figure 2.4: CCM i_L and v_L ripple over one switching period

2.3 Boost inductor

For this section, when evaluating inductor currents, i_L and I_L will be referring to the instantaneous and RMS currents through the inductors, whereas I_{AC} will be referring to the RMS AC current drawn from the grid.

2.3.1 Current waveforms and ripple

As explained in section 2.1, the bidirectional totem-pole operates as a boost converter during G2V charging. Thus, the inductor current and voltage waveforms over one totem-leg switching period during the positive mains half cycle will be as shown in figure 2.4.[24, ch. 7-4]. During negative half cycle the ripple will be exactly mirrored over the time axis.

As can be found combining figure 2.4 and (2.1), the inductor current ripple at any given point in the AC mains cycle can be given as

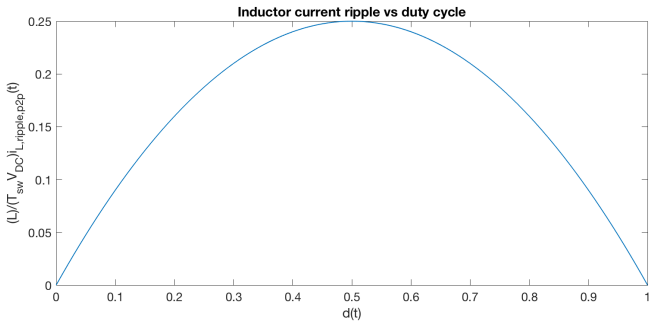


Figure 2.5: Boost CCM Δi_L vs duty cycle

$$\Delta i_L(t) = \frac{1}{L}\int_{t=0}^{d\cdot T_{sw}} v_{AC}(t)dt \ , \tag{2.3}$$

where d is the duty cycle at this point. Since $f_{sw} \gg f_{AC}$, $v_{AC}(t)$ and can be considered constant over one switching period, giving from (2.3):

$$\Delta i_L(t) = \frac{T_{sw}}{L} d(t) v_{AC}(t) \tag{2.4}$$

Finally using the boost converter voltage ratio from [24, ch. 7-4],

$$\frac{v_{DC}(t)}{v_{AC}(t)} = \frac{1}{1-d(t)} \ , \tag{2.5}$$

(2.4) can be rewritten as follows:

$$\Delta i_L(t) = \frac{T_{sw} v_{DC}(t)}{L} d(t)\big(1-d(t)\big) \ . \tag{2.6}$$

This equation (2.6) is solved graphically in figure 2.5, assuming $v_{DC}(t)$ is approximately constant and equal to $v_{DC}(t) \approx V_{DC}$. Figure 2.5 shows that $\Delta i_L(d)$ has a parabolic shape, peaking at $d = 0.5$.

For illustration, the current through the inductor, i_{AC}, during G2V over a whole mains cycle is shown in figure 2.6. The average inductor current and the AC mains voltage are shown as well for comparison, and they show that the fundamental AC current is more or less in phase with the AC voltage.

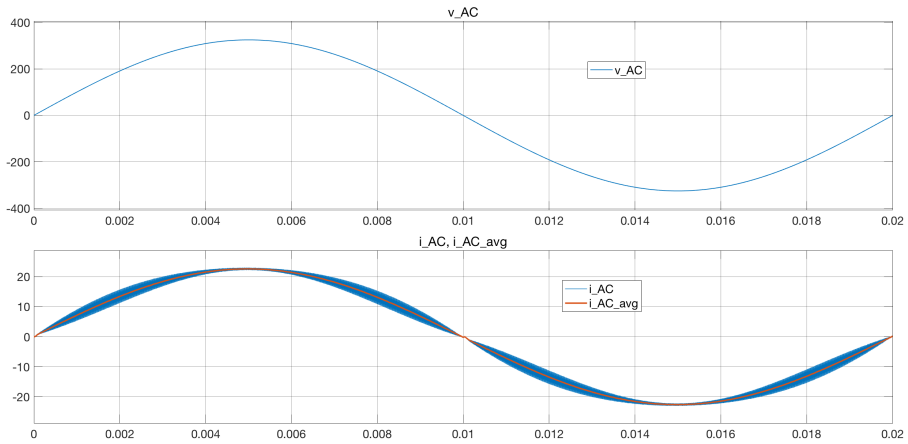


Figure 2.6: The inductor current compared to the AC mains voltage throughout one mains cycle.

2.3.2 Conduction losses

The inductor conduction losses mainly comprises two parts: copper losses, which are resistive losses from the resistance in the inductor windings, and core losses, who are mostly due to eddy current losses end hystheresis losses in the magnetic core.[24, ch. 30-1] The hysteresis losses are highly dependent on the core material, but is always given on the following form:

$$P_{L,hyst} = k \cdot f^a \cdot B_{AC}^q \,, \tag{2.7}$$

where k, a and q are material dependent constants, f is the magnetic flux oscillation frequency and B_{AC} is the AC magnetic flux density.[24, ch. 30-1-2] Eddy current losses are also core dependent, given on the form:

$$P_{L,eddy} = \frac{q^2 \omega^2 (B_{AC} + B_{avg})^2}{24 \rho_{core}} \,, \tag{2.8}$$

where ω is the angular frequency of the flux oscillations, B_{avg} is the flux density constant flux offset and ρ_{core} is the charge density of the core material.[24, ch. 30-1-4] As mentioned, the copper losses are resistive losses due to the winding resistance, and so they are given by:

$$P_{L,copper} = R_{L,copper} I_L^2 \ , \tag{2.9}$$

where I_L is the RMS inductor current and $R_{L,copper}$ is the inductor winding resistance. Acknowledging that the core flux density $B \propto I$ by Ampere's law, as well as that q often takes a value close to 2,[24, ch. 30-1-2] it can be seen from (2.7), (2.8) and (2.9) that all of these losses have a nearly proportional relation to to I_L^2. Thus, a simplification will be made going forward, merging all of these losses into one equivalent resistance at the given frequency, called R_L, giving the following loss equation:

$$P_L \approx R_L I_L^2 \ . \tag{2.10}$$

As mentioned, the inductor current ripple must be less than 20%, and for that reason it is assumed that

$$I_L \approx I_{AC} \ , \tag{2.11}$$

meaning (2.9) can be rewritten:

$$P_L \approx R_L I_{AC}^2 \ . \tag{2.12}$$

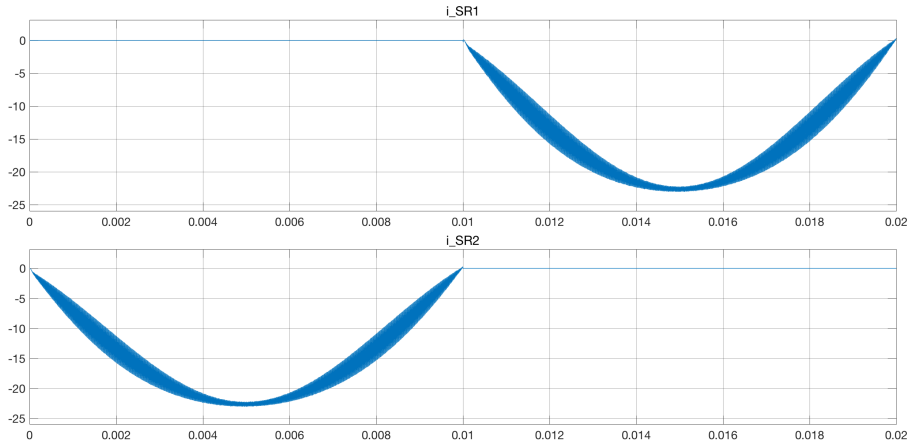


Figure 2.7: The rectifier-leg transistor drain-source currents throughout one mains cycle during G2V.

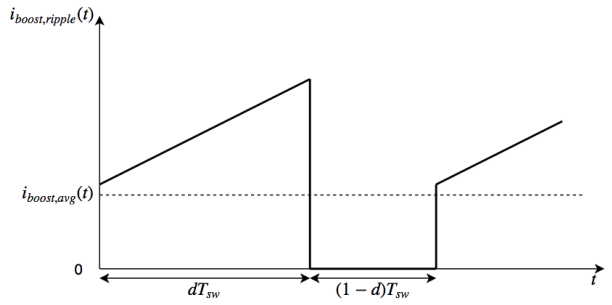
2.4 Transistors

2.4.1 Current waveforms and ripple

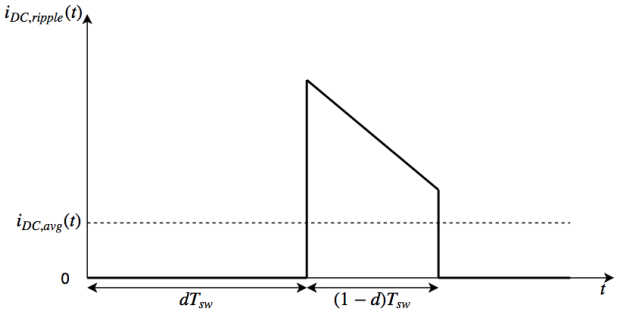
Rectifier-leg switches

The currents through the transistors will be quite different for the two legs of the totem pole. Simplest are the rectifier legs, who conduct for a whole mains half-period each, as shown in sections 2.1 and 2.2. S_{R1} conducts during negative mains half cycle, S_{R2} conducts during the positive. Therefore, the current ripple during the conducting half-cycle of these rectifier-leg transistors will be shaped like the inductor current ripple in figure 2.4.

Figure 2.7 illustrates the drain-source currents of the rectifier-leg transistors throughout the mains cycle during G2V charging. The drain-source currents are evidently always negative during G2V, confirming the operation description from section 2.1. During V2G the currents will, oppositely, always be positive.



(a) The current through the boost switch at an arbitrary point in the AC mains cycle.



(b) The totem-pole output current to the DC link at an arbitrary point in the AC mains cycle.

Figure 2.8: The current ripple of the totem-leg switches during positive mains half cycle in G2V operation.

Totem-leg switches

The current of the two totem-pole transistors depend highly on the duty cycle d of each of the switches, since the transistors obviously only conducts while they are on. The modulation is different for the different transistors in each mains half-cycle, as mentioned in sections 2.1 and 2.2, and so the switching-period current waveform of each of the transistors will be different as well. To simplify the analysis, switching-period current waveforms will here be shown for the *boost switch* and the *boost complementary switch* during *G2V*. During *V2G*, the boost complementary switch which will be equivalent to the *buck switch*, with the same current waveform, and the boost switch will be equivalent to the *buck complementary switch*.

Deriving the switching-period current waveforms from figure 2.4, the boost switch conducts during dT_{sw}, whereas the boost complementary switch conducts during $(1-d)T_{sw}$. Hence, the switching-period current waveforms through the boost switch and the boost complementary switch for an arbitrary duty cycle d can be given as in figures 2.8a and 2.8b, respectively. The current through the boost complementary switch is the current that is passed from the totem-pole to the DC-link, and is therefore denoted $i_{DC}(t)$.

Throughout one mains cycle in G2V operation, the currents of the two switches will be shaped as in figure 2.9. As explained in section 2.1, S_{T2} is the boost switch during positive half-cycle, having the switching-period current waveform drawn in figure 2.8a, whereas during negative half-cycle it is the complementary switch, having the switching-period current waveform drawn in figure 2.8b, with negative polarity. S_{T1} is exactly opposite. During V2G, the currents have the same shape, but with opposite polarity.

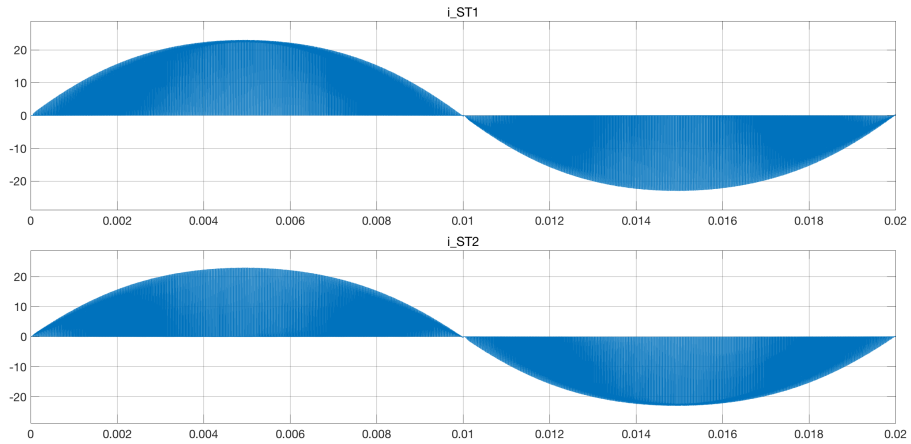


Figure 2.9: The totem-leg transistor drain-source currents throughout one mains cycle during G2V.

2.4.2 Conduction losses

In the following it will be assumed that *MOSFETs* or *GaN HEMTs* are chosen for both the rectifier leg and the totem leg. In the case of other relevant transistor technologies, such as IGBTs, the conduction losses would not be resistive, but caused by forward voltage and average current through the transistors.

Rectifier-leg switches

To evaluate the conduction losses in the transistors, expressions have to be developed describing the RMS currents through the transistors. For the rectifier switches S_{R1} and S_{R2}, this is trivial, since they will be conducting for half an AC mains period each:

$$I_{SR}^2 = \frac{1}{2\pi}\int_{\omega t=0}^{\pi} i_L^2(\omega t)\, d\omega t = \frac{1}{2} I_L^2 \,. \tag{2.13}$$

Implementing (2.11) in (2.13), we get for each of the rectifier switches:

$$I_{SR} = \frac{1}{\sqrt{2}} I_{AC}. \tag{2.14}$$

Totem-leg switches

In the case of the fast-switching totem-leg switches, S_{T1} and S_{T2}, the RMS current through each of the transistors depends on the time-varying duty cycle d_{ST} of the relevant transistor. The discrete-form equation for the RMS current through one of the totem-leg switches can be given as follows:

$$I_{ST}^2 = \frac{1}{2\pi} \sum_{k=0}^{f_{sw}/f_{AC}} d_{ST}[k] i_L^2[k] \ , \tag{2.15}$$

where k represents one single switching period at one point in the AC mains cycle, f_{sw} is the switching frequency, f_{AC} is the AC mains frequency and d in this case is the duty cycle of any of the two totem-leg switches. Taking into account that f_{sw} will be chosen so that $f_{sw} \gg f_{AC}$, (2.15) can be approximated as a continuous integral over the whole AC mains cycle:

$$I_{ST}^2 = \frac{1}{2\pi} \int_{\omega t=0}^{2\pi} d(\omega t) i_L^2(\omega t) \, d\omega t \ . \tag{2.16}$$

Moreover, since S_{T1} and S_{T2} are switched complementarily, (2.16) can be simplified. Dead time required between turn-off of one transistor and turn-on of the other to avoid cross-conduction is neglected, since it is assumed very small.[24] The complementary switching means one of the switches are always conducting, and as explained in sections 2.1 and 2.2, the roles of the two switches interchange every half cycle. Thus, based on the current waveforms for the boost and complementary switch in figures 2.8a and 2.8b, (2.16) can be rewritten as follows:

$$I_{ST}^2 = \frac{1}{2\pi} \left(\int_{\omega t=0}^{\pi} d(\omega t) i_L^2(\omega t) \, d\omega t + \int_{\omega t=0}^{\pi} \big(1 - d(\omega t)\big) i_L^2(\omega t) \, d\omega t \right) \tag{2.17}$$

$$= \frac{1}{2\pi} \int_{\omega t=0}^{\pi} \big(d(\omega t) + 1 - d(\omega t)\big) i_L^2(\omega t) \, d\omega t \tag{2.18}$$

$$= \frac{1}{2\pi} \int_{\omega t=0}^{\pi} i_L^2(\omega t) \, d\omega t \tag{2.19}$$

$$= \frac{1}{2} I_L^2 \tag{2.20}$$

This derivation from (2.17) to (2.20) shows that due to the symmetry of the topology, both of the totem-leg switches are conducting in total in half of the AC-mains voltage cycle. This gives the same RMS current in both of the totem-leg switches as in the rectifier-leg switches:

$$I_{ST} = \frac{1}{\sqrt{2}} I_{AC} \, . \tag{2.21}$$

Based on the derived RMS current expressions in (2.14) and (2.21), the conduction losses in each of the transistors can be determined as follows:

$$P_{cond} = \frac{1}{2} I_{AC}^2 R_{DS,on}. \tag{2.22}$$

2.4.3 Switching losses

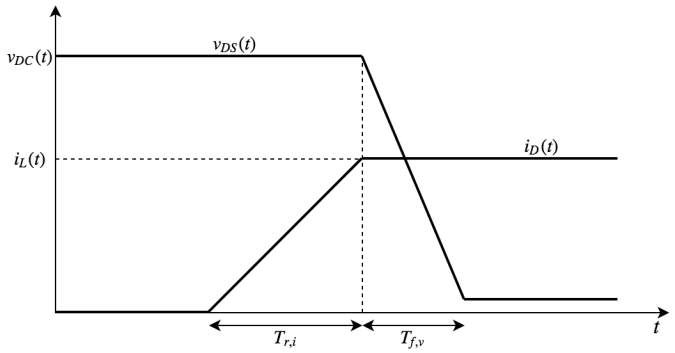
Now that the transistor conduction loss expressions have been established, the next thing needed to estimate the transistor losses is an estimation of the switching losses. As with the derivation of the conduction losses, the following will assume MOSFETs or GaN HEMTs as the chosen transistor technology.

Based on the MOSFET switching characteristics described in [24, ch. 22-5-2], the switching waveforms can be approximated as in figure 2.10. As appears in [36], the switching characteristics of a GaN HEMT can be estimated in a similar way, so figure 2.10 and the following derivations are hence considered valid for both transistor types. The switching energy E_{sw} is given as $\int v_{DS}(t) \cdot i_D(t) \, dt$ over the switching transient duration, giving the following equation based on figure 2.10:

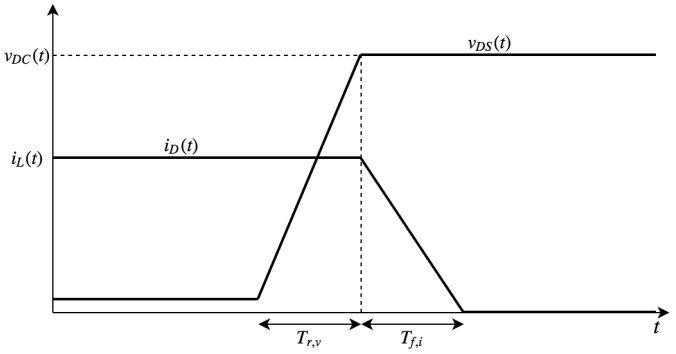
$$E_{sw}[k] = E_{on}[k] + E_{off}[k] = \frac{1}{2}(T_{r,i} + T_{f,v} + T_{r,v} + T_{f,i}) v_{DC}[k] i_L[k], \tag{2.23}$$

where v_{DC} and i_L are, respectively, the average DC voltage and inductor current over the switching period.

In order to find a simple expression for the switching power P_{sw}, (2.23) is averaged over half an AC mains cycle. Current and voltage rise and fall times are obviously dependent on $v_{DC}(t)$ and $i_L(t)$, making it somewhat more complex. However,



(a) Turn-on



(b) Turn-off

Figure 2.10: Approximation of the switching characteristics of a MOSFET.

$v_{DC}(t)$ will have a ripple of less than 20%,(table 1.2) meaning it can be assumed to be approximately constant and equal to V_{DC}, again giving approximately constant $T_{r,v}$ and T_{f_v}. Since we are mostly interested in a rough estimate of the losses for transistor dimensioning purposes, it is assumed for simplicity going forward that also the current rise and fall times do not vary much with time. To clean up the expression, we set total switching commutation time $T_{sw,comm} = T_{r,i} + T_{f,v} + T_{r,v} + T_{f,i}$. An expression for the average switching energy is obtained:

$$E_{sw,avg} = \frac{1}{\pi}\int_{\omega t=0}^{\pi} E_{sw}(\omega t)d\omega t = \frac{1}{2}T_{sw,comm}V_{DC}I_{AC,avg} \ , \tag{2.24}$$

where the average AC current over one half period, $I_{AC,avg}$, is given as

$$I_{AC,avg} = \frac{1}{\pi}\int_{\omega t=0}^{\pi} i_{AC,avg}(\omega t)d\omega t = \frac{2\sqrt{2}}{\pi}I_{AC} \ . \tag{2.25}$$

This gives approximate transistor switching power loss:

$$P_{sw} = f_{sw} * E_{sw,avg} = \frac{f_{sw}}{2}T_{sw,comm}V_{DC}I_{AC,avg} \ . \tag{2.26}$$

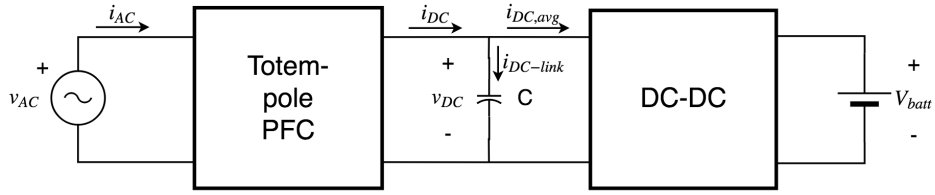


Figure 2.11: Illustration of he DC-link capacitor, voltage and currents

2.5 DC-link

Now, having established current waveforms and losses for the other main components of the totem-pole PFC, the same can be done for the DC-link capacitor. The assignment of the DC-link capacitor is to remove as much as possible of the 100Hz and high-frequency ripple in voltage and current from the PFC to the DC-DC converter feeding the battery. Due to size limitations of this capacitor, it is practically not possible to remove all of this ripple, leaving a small 100Hz ripple to be compensated in the DC-DC converter. All variables and parameters in the following derivations are referred to figure 2.11.

2.5.1 Current waveforms and ripple

From figure 2.11 the DC-link current can be written:

$$i_{DC-link} = i_{DC} - i_{DC,avg} \ . \tag{2.27}$$

The current sent from the PFC to the DC-link, i_{DC}, is the current passed through the boost complementary switch, with ripple shown in figure 2.8b. Thus, the current ripple consumed by the DC-link capacitor is equal to this current minus the average DC current going into the DC-DC converter, as in figure 2.12.

The DC-side currents during a whole mains period are depicted in figure 2.13, showing a rectified i_{DC}, a small 100Hz ripple on $i_{DC,avg}$ due to the necessary small DC-voltage ripple and $i_{DC-link}$ as the sum of these in accordance with (2.27).

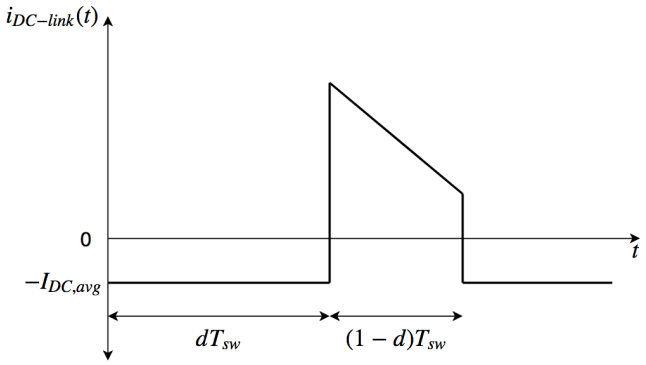


Figure 2.12: The current through the DC-link capacitor over one totem-leg switching period

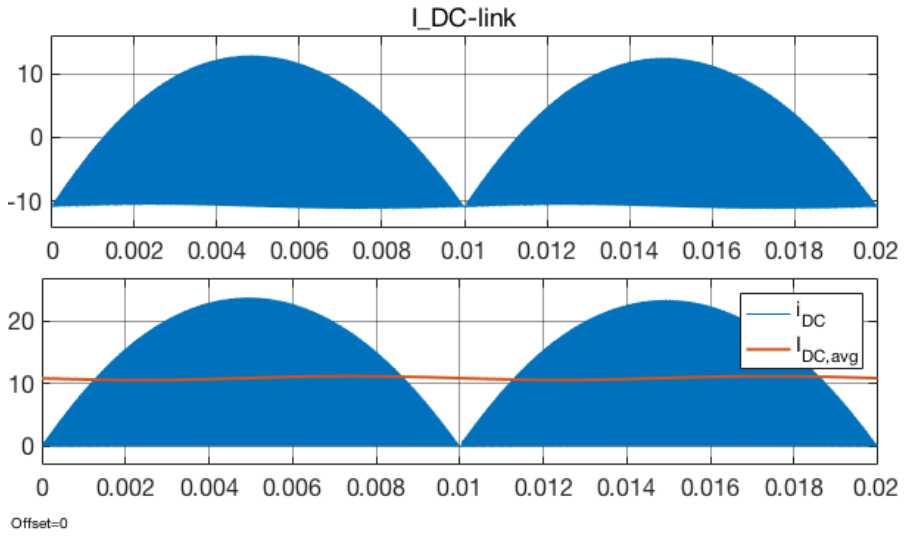


Figure 2.13: The DC-side currents throughout one mains cycle during G2V.

2.5.2 Conduction losses

Like in the other main components of the totem-pole PFC, there are some losses in the DC-link capacitor which need to be taken into account in the PFC design. These are mostly dielectric losses and electrode losses, often simplified as conduction losses due to an internal equivalent series resistance (ESR) of the capacitor. [37] A loss expression can be given as

$$P_{DC-link} = I_{DC-link}^2 \cdot \text{ESR} \,, \tag{2.28}$$

where $I_{DC-link}$ is the RMS current through the DC-link capacitor. With $I_{DC,avg}$ assumed constant, the DC-link current $i_{DC-link}$ consists of all of the harmonics in i_{DC}. As explained in [24, ch. 3-2-4-1], using superposition of harmonic signals, the DC-link RMS current can again be given as follows:

$$I_{DC-link} = \sqrt{I_{DC,rms}^2 - I_{DC,avg}^2} \,, \tag{2.29}$$

where $I_{DC,rms}$ is the RMS-value of the current from the totem pole to the DC-side and $I_{DC,avg}$ is both the RMS and the constant value of the current to the DC-DC converter. Since i_{DC} is always the current through the complementary boost switch, and exploiting that i_{DC} is symmetric every half period, the RMS current I_{DC} can be given from (2.13) over one half period:

$$I_{DC}^2 = \frac{1}{\pi} \int_{\omega t=0}^{\pi} d_{compl}(\omega t) i_{AC}^2(\omega t) \, d\omega t \,, \tag{2.30}$$

where d_{compl} is the duty cycle of the complementary switch. It will be shown later in section 4.2.1 that the duty cycle $d_{compl}(\omega t) \propto v_{AB,1}(\omega t) = \hat{V}_{AB} \sin(\omega t + \phi_{AB})$ from figure 2.1. Hence, (2.30) can be rewritten

$$I_{DC}^2 = \frac{1}{\pi} \int_{\omega t=0}^{\pi} \hat{d}_{compl} \sin(\omega t + \phi_{AB}) \left(\hat{I}_{AC} \sin(\omega t)\right)^2 d\omega t \,, \tag{2.31}$$

where ϕ_{AB} is the phase angle of $v_{AB}(\omega t)$ referred to $v_{AC}(\omega t)$. The peak duty $\hat{d}_{compl}$ will be, using the basic boost converter properties from [24, ch. 7-4] and that the

duty cycle of the complementary switch is given as $d_{compl} = 1 - d_{boost}$:

$$\hat{d}_{compl} = 1 - d_{boost,min} = \frac{\hat{V}_{AC}}{V_{DC}} \, . \tag{2.32}$$

Implementing (2.32) in (2.31) and solving, the DC RMS current becomes

$$I^2_{DC,rms} = \frac{8}{3\pi} \frac{\hat{V}_{AC}}{V_{DC}} I^2_{AC} \cos(\phi_{AB}) \, . \tag{2.33}$$

Implementing (2.33) in (2.29), the RMS current in the DC-link is given as follows:

$$I_{DC-link} = \sqrt{\frac{8}{3\pi} \frac{\hat{V}_{AC}}{V_{DC}} I^2_{AC} \cos(\phi_{AB}) - I^2_{DC,avg}} \, , \tag{2.34}$$

which easily gives the conduction losses when implementing in (2.28):

$$P_{DC-link} = \left(\frac{8}{3\pi} \frac{\hat{V}_{AC}}{V_{DC}} I^2_{AC} \cos(\phi_{AB}) - I^2_{DC,avg} \right) \cdot \mathrm{ESR} \, . \tag{2.35}$$

Chapter 3

Components dimensioning

Dimensioning the components is obviously important for building a physical embodiment of the PFC, but it is important for building the basic simulation model as well. Various parameters in the PFC will affect the currents and voltages at different points in the topology; e.g. loss considerations in boost inductor and transistors dictating the average DC-link voltage, DC-link capacitor dictating the DC-link voltage ripple and the boost inductor – along with the DC-link voltage – dictating the AC current ripple. This chapter will revolve around dimensioning the key components of the totem-pole PFC: The boost inductor, the transistors and the DC-link capacitor. The components will be dimensioned assuming *maximum power flow* both in G2V and V2G mode. This is justified by the following: During G2V, the consumer should be able to charge its car at maximum power when required, and, during V2G, the OBC is likely to operate as a grid stabilizer supplying the grid at maximum power, as argued in section 1.1. All parameters and variables will be referred to figure 2.1.

3.1 DC-link capacitor

The DC-link capacitor plays an important role in an OBC, suppressing much of the DC-link voltage ripple to keep the voltage as constant as possible without exceeding the DC-link capacitor size limitations. This DC-link voltage is controlled by the PFC, making the DC-link capacitor central in PFC design. The battery on the DC-side of the OBC requires DC voltage. Thus, a big part of the DC voltage 100Hz ripple must be suppressed in the DC link before DC-DC converter compensates the rest. The DC-DC converter is often less efficient at compensating big variations in input voltage and current, meaning it is beneficial keeping the ripple low at its input.[1] Moreover, since the PFC is working in boost operation during G2V charging and buck during V2G discharging, another key reason for minimizing the ripple is ensuring that the instantaneous DC-link voltage is always higher than the instantaneous AC voltage. Moreover, the DC-link capacitor is the most limiting component to the lifetime of the OBC, and so the current rating should be chosen as high as possible and the ESR as low as possible to minimize the wear and tear of the capacitor. [1]

3.1.1 DC-link rated voltage

Valeo Siemens define for this application that the peak-to-peak 100Hz voltage ripple at the DC-link should be held at 20V, as specified in table 1.2. Furthermore, it is critical for the boost operation in G2V and buck operation in V2G that the instantaneous DC-link voltage is always higher than the instantaneous magnitude of $v_{AC}(t)$, as shown in figure 3.1. To allow for some delay in the voltage control, a certain margin, V_{margin}, needs to be added. This margin is for this converter set at

$$V_{margin} \geq 5\text{V} \ .$$

As a consequence, with the peak-to-peak ripple of 20V, the average DC-link voltage has to be set at

$$V_{DC} \geq \hat{V}_{AC} + 15\text{V} \ .$$

At AC voltages of 230Vrms (325Vpeak) and lower, complying with the above-mentioned restrictions is not an issue, due to the minimum limit for V_{DC} set at 340

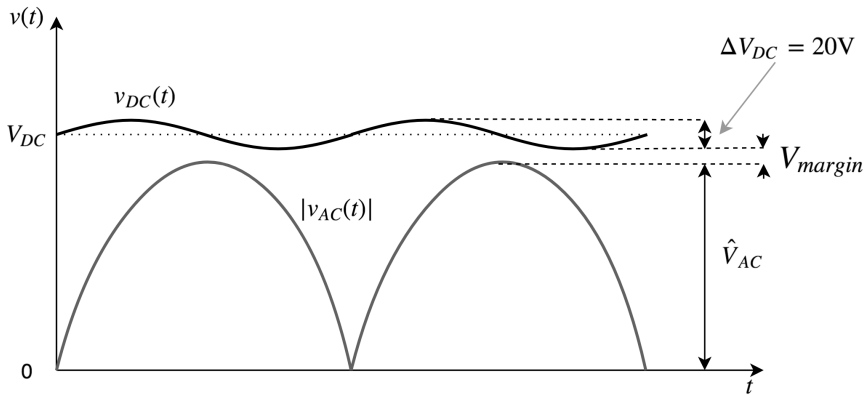


Figure 3.1: DC-link voltage design requirements compared to AC mains voltage.

V (table 1.2). Furthermore, since the switching losses increase with increasing DC-link voltage, by (2.26), keeping the DC-link voltage as low as possible will reduce the switching losses. Looking at the PFC in isolation, it would therefore loss-wise be beneficial to have V_{DC} lower than 340V for V_{AC} lower than 230Vrms, but this would increase the current from the PFC to the DC-DC, increasing the conduction losses of the DC-DC converter. This is the reason for the 340V $V_{DC,min}$ limit, ensuring efficient operation of the DC-DC converter by keeping a narrow input voltage range. Thus, for every peak voltage lower than 330V, the DC-link voltage is set at

$$V_{DC} = V_{DC,min} = 340 \quad \text{when} \quad \hat{V}_{AC} \leq 325\text{V} \, .$$

For peak AC voltages exceeding 325V, it is exploited that the DC-link voltage is regulated by the PFC, as will be explained later in the thesis, and therefore can also be changed according to the AC voltage. The DC-link voltage is set to follow the mains voltage as closely as possible, given the restriction that $v_{DC}(t)$ should always be higher than $v_{AC}(t)$ with a DC-link voltage peak-to-peak ripple of 20V. Thus, the average DC-link voltage V_{DC} is controlled, both in G2V and V2G, according to the following equation:

$$V_{DC} = \hat{V}_{AC} + 15\text{V} \quad \text{when} \quad \hat{V}_{AC} > 325\text{V} \, . \tag{3.1}$$

Based on this the maximum rated DC-link voltage in this design can be found to be

$$V_{DC,max} = \sqrt{2} \cdot 275\text{V} + 10\text{V} = 400\text{V} \ .$$

3.1.2 DC-link rated current

Finding the minimum DC-link current rating can be done easily using figures 2.12 and 2.13 to recognize that the maximum DC-link current can be given as

$$I_{DC-link,max} = \hat{I}_{AC,max} - I_{DC,avg,min} \ , \tag{3.2}$$

where $I_{DC,avg,min}$ is the minimum DC current at max power, which is given from the max power and minimum average DC-link voltage:

$$I_{DC,avg,min} = \frac{3500\text{W}}{400\text{V}} = 8.75\text{A} \ ,$$

and the maximum DC-link current becomes, from (3.2):

$$I_{DC-link,max} = \sqrt{2} \cdot 16\text{A} - 8.75\text{A} = 13.87\text{A} \ .$$

However, as mentioned earlier, the current rating should be chosen higher than this to minimize the wear and tear of the DC-link capacitor.

3.1.3 DC-link capacitance value

The DC-link capacitance value is chosen in order to filter the 100Hz fundamental component of the totem-pole DC-side voltage to give the desired DC-link peak-to-peak voltage ripple of 20V. This is governed by the basic equation for a capacitor:

$$\Delta v_{DC,1}(t) = \frac{1}{C} \int_t i_{DC-link,1}(t) \, dt \ . \tag{3.3}$$

Table 3.1: Key parameters for the relevant electrolytic capacitor used by Valeo Siemens today. [1]

Parameter	Value
V_{rated}	450Vdc
$I_{ripple,rated}$	3.1Arms
$C_{nominal}$	360μF

The fundamental component is of course sinusoidal, and so the integral will naturally be biggest over one positive or negative half period of $i_{DC-link,1}$. Integrating over the positive half period, and inserting ωt with $dt = d\omega t/\omega$, the voltage ripple becomes:

$$\Delta V_{DC,1} = \frac{1}{\omega_1 C} \int_{\omega_1 t=0}^{\pi} \hat{I}_{DC-link,1} \sin(\omega_1 t)\, d\omega_1 t \ , \tag{3.4}$$

$$= \frac{2}{\omega_1 C} \hat{I}_{DC-link} \ . \tag{3.5}$$

It becomes clear swapping ω_1 with ω_n in (3.5) that it is indeed sufficient to design C from the fundamental current, as $\Delta V_{DC,n}$ is then inversely proportional to ω_n, showing that the fundamental frequency has the biggest voltage ripple.

The capacitance value can now be found solving (3.5) for C and inserting values. A Fourier analysis performed in Simulink on the signal shown in figure 2.13 reveals that the fundamental component of $i_{DC-link}$ has amplitude $\hat{I}_{DC-link} = 10.81$A, equal to $I_{DC,avg}$, and a frequency $f_1 = 100$Hz. Using $\Delta V_{DC,1} = 20$V, the capacitance becomes:

$$C_{min} = \frac{2\hat{I}_{DC-link}}{\omega_1 \Delta V_{DC,1}} = 1.72\text{mF} \tag{3.6}$$

3.1.4 Capacitor choice

For the choice of capacitor, it is important to choose a capacitor type with low ESR and high current rating, since the capacitor is the most limiting component to the lifetime of the OBC, and high losses and approaching the current rating decreases

the lifetime of the capacitors. A good way of solving this is connecting several capacitors in parallel, reducing the current and losses in each of the capacitors. To match the lifetime of the current OBC technology at Valeo Siemens, it is chosen to use the same capacitor. Due to confidenciality the exact model name or datasheet can not be shown in this thesis, but it is an electrolytic capacitor, and some of its key parameters are summarized in table 3.1.

With the given $C_{nominal} = 360\mu\text{F}$ it is apparent that 5 capacitors connected in parallel is required to match the required minimum capacitance value in (3.6), giving total capacitance

$$C = 5 \cdot 360\mu\text{F} = 1.8\text{mF} .$$

Checking the RMS current through each of the capacitors, the total DC-link RMS current can first be found from (2.34). Assuming close-to-zero phase angle ϕ_{AB} due to the low inductance and using minimum DC-link voltage and maximum power for maximum DC-link current, the DC-link RMS current becomes

$$I_{DC-link} = \sqrt{\frac{8 \cdot 325\text{V}}{3\pi \cdot 340\text{V}}(16\text{A})^2 - (10.8\text{A})^2} = 9.54\text{A} .$$

Acknowledging that the current in each of the capacitors will be one fifth of the total DC-link RMS current, the RMS current through each of the capacitors will be

$$I_{DC-link,cap} = \frac{1}{5} \cdot 9.54\text{A} = 1.9\text{A} ,$$

which is well below the maximum rated ripple current of the relevant capacitor in table 3.1.

No ESR is given in the datasheet, but with three capacitors connected in parallel, and at the same power level, Valeo Siemens experience power losses $< 0.5W$, which is negligible. In this case, with five capacitors connected in parallel, the losses will be even lower due to lower currents through each of the capacitors. This lower current stress in each of the capacitors should also imply a longer lifetime expectancy of the charger.

3.2 Transistors

The right choice of transistors is a key part of the design of any switch-mode converter. In this case, the transistors are chosen along with the switching frequency to comply with the desired efficiency of the whole charger. Moreover, the transistors have to withstand the expected RMS currents, peak blocking voltages and peak currents. Aided by a heat sink, the transistors should also be able to handle its own dissipated heat without melting.

In the following, the design process for choosing and dimensioning the totem-leg and rectifier-leg transistors will be described chronologically. The reason for this is that converter design is an iterative process, making assumptions and updating them based on the results throughout the design process. While dimensioning the totem-leg transistors, the switching frequency, f_{sw} will also be chosen. This because the transistors will be designed to match the required efficiency, requiring the switching losses to be within the allowed losses restriction that follows this efficiency.

3.2.1 Choice of transistor technology

Totem-leg transistors

When choosing the transistor technology for each of the switches it is important to first evaluate the requirements of the switch. First of all, figures 2.2 and 2.3 show that the current should be able to flow in both directions through all of the switches. Secondly, the totem-leg switches need to be able to handle high-frequency switching, preferably around 100kHz (appendix A), while also keeping the losses sufficiently low to comply with the efficiency requirement of 98% in G2V and 97% in V2G. A high switching frequency has several benefits regarding especially the power density of the OBC; it minimizes the size of magnetic-core components, as is shown further for the boost inductor in section 3.3, and it minimizes the size of the AC-side direct mode (DM) filter required to comply with the grid-side current noise limitations, declared in the design specifications in appendix A.

In this frequency range, and at a required rating of around $\sim$400V and $\sim$22.5A, two transistor technologies stand out as promising solutions: Power MOSFETs

and GaN HEMTs. MOSFETs and GaN HEMTs both have bidirectional conduction capability by nature, due to their symmetrical structure.[38] This is beneficial, as it would be sufficient the transistor as the only semiconductor component in each of S_{T1} and S_{T2}. Furthermore, they are both efficient at high switching levels, much due to the lack of minority carriers having to be moved in and out of the transistor during switching, as is the case in many other transistor technologies, such as IGBTs and BJTs. [24] However, there are differences in the performance of these two transistor technologies when working as totem-leg switches, owing to their structural differences highlighted in [38]. This is also explained in more detail in the paper written on GaN HEMTs in appendix C, and the following argumentation on GaN HEMTs is based on the contents of this paper. The paper states that although GaN as a material has higher breakdown field and band gap than SiC and Si, which initially gives a higher resistivity in the transistor, the two-dimensional electron gas (2DEG) layer ensures that the GaN HEMT has a lower $R_{DS,on}$ than MOSFETs for the same breakdown voltage. Moreover, the higher breakdown field of GaN allows for smaller physical embodiments of the transistors compared to Si and SiC MOSFETs at the same rated breakdown voltage, again giving smaller parasitic capacitances and thus faster switching transients and lower switching losses. Another significant advantage of the GaN HEMT is that, unlike MOSFETs, it does not have a reverse body diode. According to [25], the reverse recovery losses of the MOSFET reverse body diodes during CCM operation of a totem-pole PFC are severe, and thus the lack of reverse body diodes in GaN HEMTs is beneficial with regard to losses.

However, one drawback of the GaN HEMT, besides it being a relatively new and thus not fully developed and commercialized technology, is that it has a relatively low thermal conductivity compared to Si and SiC MOSFETs. That means it will have trouble dissipating the heat generated from losses, possibly imposing some challenges in the heat sink design. On the other hand, the results from [39] suggest that the performance of GaN HEMTs are less affected by the case temperature, and so the decreased thermal conductivity might not matter anyway. Another drawback is that the GaN HEMT technology is by nature normally-on, meaning it is conducting at low gate voltage, as explained in appendix. This is undesirable, as we want the transistor to be open when the system is not energized. Therefore, it is compensated by constructing normally-off enhancement-mode HEMTs

(eHEMTs), either by changing the structure or by cascading a FET at the gate of the HEMT. This derates the switching performance of the GaN HEMT some, but still it is an improvement compared to existing technology in that regard.

All of this taken into account, the *GaN eHEMT* is chosen as the transistor technology for use in the totem-leg switches. This is because it appears most efficient in high-frequency and high-power application. This decision is backed up by calculations in section 3.2.5.

Rectifier-leg transistors

As for the rectifier-leg switches, these only really have one requirement, which is bidirectional conduction ability, due to the reverse direction of the current in V2G mode shown in figure 2.3. The switching losses are negligible, due to a switching frequency equal to the mains frequency (45Hz-65Hz), and thus it is desirable to have transistors with low conduction losses. In that sense, it will be sufficient to use slow-switching low-$R_{DS,on}$ MOSFETs. Since a more advanced transistor technology has been used in the totem-leg switches, it also becomes a question of price, especially since the OBC would be mass-produced. Thus a cheaper and simpler *MOSFET*, just complying with the loss and rating demands is preferable in the rectifier-leg switches.

Corresponding topology

The updated bidirectional totem-pole PFC topology, with GaN eHEMTs in the totem leg and MOSFETs in the rectifier leg, is shown in figure 3.2. Due to the absence of eHEMT symbols in the drawing software, eHEMTs are represented as MOSFETs with no reverse diodes.

3.2.2 Guesstimating component loss distribution

As specified in the bidirectional OBC and PFC specifications in tables 1.1 and 1.2, the efficiency of an OBC should be designed at 94% in G2V charging mode, with the efficiency of the PFC being at 98% for the standard voltage levels (230Vrms

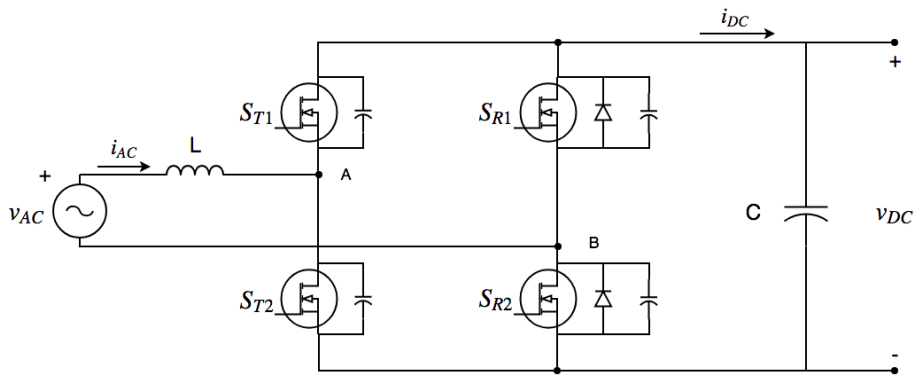


Figure 3.2: The bidirectional totem pole topology with GaN eHEMTs in the totem leg and MOSFETs in the rectifier leg.

and 110-120Vrms). [20] In G2V discharging mode, the efficiency of the bidirectional OBC is predetermined to be at least 91%, with the PFC having at least 97% for the same voltage levels. For the design of this particular totem-pole PFC, it is decided to design the charger mainly for 230Vrms and the most restrictive efficiency, $\eta_{PFC,G2V} = 98\%$. Due to the conduction losses of the transistors being independent of the AC voltage, by (2.22), the eHEMTs would have to be paralleled in order to meet the efficiency demands at 110-120Vrms. This will be discussed more in the later discussion part, but is rendered out of scope for the totem-pole model of this master's work.

The losses will be calculated using worst-case highest drain-source resistances in the transistors. Thus, it is acceptable to use a worst case efficiency of

$$\eta_{PFC,worst-case} = 97.6\% \ ,$$

which rounded up becomes 98%. During normal operation, the resistances will be lower and the efficiency higher. Using this along with rated $V_{AC} = 230$Vrms and $I_{AC} = 16$Arms, the maximum allowed PFC losses can be calculated as follows:

$$P_{loss,PFC,max} = (1 - \eta_{PFC,worst-case}) \cdot I_{AC} \cdot V_{AC} = 0.024 \cdot 16\text{A} \cdot 230\text{V} = 88.32\text{W} \ .$$

Table 3.2: Guesstimated design rule losses distribution in the bidirectional totem-pole PFC.

Losses distribution	
Totem-leg	31W
Rectifier-leg	31W
Inductor/rest of PFC	26W
Total	88W

To simplify, it is decided that the losses in the PFC should be distributed as presented in table 3.2. Since the losses will be symmetrically distributed across the two transistors in each leg, as is determined in section 2.4.2, the total losses in each of the transistors in the two legs will have to be:

$$P_{ST} = 15.5\text{W}, \quad P_{SR} = 15.5\text{W} .$$

3.2.3 Totem-leg transistors

The loss restrictions for P_{ST} are now used to determine the transistors used in the totem-leg switches along with the switching frequency to be applied on this leg. As mentioned, GaN eHEMTs are preferred over MOSFETs for the totem-leg switches due to their advantage of not having reverse body diodes. Commercial GaN eHEMTs are not too many at this moment in time, but a selection has been found from GaN Systems and these are, for the purpose of this thesis, assumed representative for the rest of the market. Two models were found to meet both the current and voltage rating demands ($>$ 22.5A and $>$ 400V) at an assumed worst-case operating junction temperature of 150°C: GS66508 and GS66516. Some key parameters acquired from the datasheets of GS66508 and GS66516 are shown in table 3.3.

The switching frequency is chosen based on the switching losses, and later the transistor model will be chosen based on the desired switching frequency. An expression for f_{sw} is found rewriting (2.26) as

Table 3.3: Some key parameters and rated values of the GaN Systems eHEMTs at $T_{case} = 25°C$.

Parameter	**GS66508**	**GS66516**
$R_{DS,on}$	50mΩ	25mΩ
$R_{DS,on}$ (@150°C)	129mΩ	67mΩ
Q_G	5.8 nC	12nC
V_{DS}	650V	650V
V_{GS}	-10V to +7V	-10V to +7V
I_{DS}	30A	60A
I_{DS} (@100°C)	25A	47A
Switching energy with $V_{DS} = 400V$		
$E_{on,rated}$	47.5μJ (@15A)	134.1μJ (@20A)
$E_{off,rated}$	7.5μJ (@15A)	14.7μJ (@20A)

$$f_{sw} = \frac{P_{sw}}{E_{sw}} \ . \tag{3.7}$$

The switching energy is calculated from the values in table 3.3, while P_{sw} is found from

$$P_{sw} = P_{transistor} - P_{cond} \ , \tag{3.8}$$

where $P_{transistor}$ is given from the design rules, and P_{cond} is calculated using (2.22). As with the drain-source current capability, since the $R_{DS,on}$ of MOSFETs and eHEMTs increase for increasing temperature, the worst-case 150°C on-state resistance must be considered when computing the expected conduction losses, as it will give the biggest losses. Applying the $R_{DS,on}$ at 150°C listed in table 3.3 and $I_{AC} = 16A$ to (2.22), the conduction losses of each of the eHEMT models are calculated as shown in table 3.4. The results show that the conduction losses of GS66508 have conduction losses that are higher than the permitted totem-leg transistor losses. That leaves *GS66516* as the only real option, and this GaN eHEMT is chosen for the totem-leg switches.

Table 3.4: Calculated conduction losses of the eHEMT models.

Model	$\mathbf{P_{cond}}$ [W]
GS66508	16.51
GS66516	8.32

Table 3.5: Estimated switching energy, losses and frequency of GS66516.

Model	$\mathbf{E_{sw,est}}[\mu\mathrm{J}]$	$\mathbf{P_{sw}}[\mathrm{W}]$	$\mathbf{f_{sw,max}}[\mathrm{kHz}]$
GS66516	71.24	7.18	100.79

3.2.4 Switching frequency

To get a good estimation of the switching losses of GS66516, the switching energy needs to be adjusted from the standard test conditions in the data sheet to fit the average DC-voltage and inductor current seen by the transistors in the totem-pole PFC. Using (2.23), where E_{sw} is assumed linearly dependent on V_{DC} and $I_{AC,avg}$, the estimated eHEMT switching energy can be found as follows:

$$E_{sw,est} = E_{sw,rated} \cdot \frac{I_{AC,avg}}{I_{DS,test}} \cdot \frac{V_{DC}}{V_{DS,test}} \ , \tag{3.9}$$

where the average AC current is, from (2.25),

$$I_{AC,avg} = \frac{2\sqrt{2}}{\pi} \cdot 16\mathrm{A} = 14.4\mathrm{A} \ .$$

Switching energy, switching power losses and switching frequency can now be calculated using (3.9), (3.8) and (3.7), inserting values from tables 3.3 and 3.4. The calculation results are shown in table 3.5. Comparing to the present-day switching frequency of Valeo Siemens OBCs at 90kHz, GS66516 allows higher switching frequencies than this, at up to 100kHz, while still complying with the losses restrictions. Setting $f_{sw} = 100\mathrm{kHz}$ could lead to an increase in power density compared to the present-day solution, for the reasons explained above. However, this increase is assumed to be relatively small for an increase in switching frequency of 11%. The increase in control speed from 90kHz to 100kHz is also small, as the requirement is that the current controller bandwidth is at least half a decade lower than the switching frequency.[40] There are also some insecurities linked to the

estimation of switching energy, due to the rough approximation in (2.24), making it sensible to choose a lower frequency than the maximum of 100kHz. Moreover, the objective of this master's thesis is to reveal whether the bidirectional totem-pole PFC is suiting for a bidirectional OBC, rather than optimizing with respect to size. Therefore, for simplicity, it is chosen to proceed with the same switching frequency as in the present-day solutions of Valeo Siemens, assuming that the increased number of gate drivers required for the totem-pole and the altered required heat sink design does not propose a big increase in the power density of the hardware OBC solution. That way, e.g. the same type of DC-link capacitor and inductor could be used in this solution, since these see the same currents and voltages for a totem-pole as for a regular boost PFC. The same AC-side DM filter could also be used, although the filtering is out of scope for this thesis. The switching frequency is set at

$$f_{sw} = 90kHz \ .$$

3.2.5 Comparison to state-of-the-art MOSFETs

Comparing to the state-of-the-art lowest-$R_{DS,on}$ power MOSFETs on the market with a rating of at least 400Vdc and 25Adc, such as Infineon's automotive power MOSFET IPW60R045CPA, these have a rated $R_{DS,on} = 45\text{m}\Omega$. Scaling to a worst-case on-state resistance at 150°C from the data sheet of IPW60R045CPA, this becomes 110mΩ, which using (2.22) gives conduction losses

$$P_{cond,MOS} = \frac{1}{2} \cdot (16\text{A})^2 \cdot 110\text{m}\Omega = 14\text{W} \ .$$

An estimation of the MOSFET switching energy using (2.24) and data for switching times from the data sheet of IPW60R045CPA gives

$$E_{sw,MOS,noRR} = \frac{1}{2} \cdot 30\text{ns} \cdot 340\text{V} \cdot 14.4\text{A} = 73.44\mu\text{J} \ ,$$

when not considering the reverse recovery losses of the body diode. That gives a maximum switching frequency, not considering reverse recovery losses, using the

same procedure as for the GaN eHEMTs:

$$f_{sw,MOS,max,noRR} = 20.42\text{kHz} .$$

If the reverse recovery losses were considered, this switching frequency would be even lower. In fact, it is found that [30] that the switching losses of a superjunction CoolMOS has 20 times more switching loss when operated in the totem-leg, due to the reverse recovery diode. This should make the GaN eHEMT GS66516 a far superior solution to the IPW60R045CPA.

However, it is worth noting that this analysis is not sufficient for concluding with absolute certainty that the GaN eHEMT is in fact the best solution, as especially the estimated switching losses are based on possibly rough approximations from uncertain parameters in the component data sheets. To get a proper overview of the losses in each of the transistors, tests should be performed, measuring the losses in each of the transistors at the relevant current and voltage operating point, e.g. using thermal measurement equipment. Nonetheless, GaN eHEMTs are, based on this switching and conduction loss analysis, considered the best solution, and GS66516 will be the transistor of choice for use in the high-frequency totem leg.

3.2.6 Rectifier-leg transistors

For the rectifier-leg transistors, the switching frequency will be equal to the mains frequency, meaning switching losses are negligible. Therefore, all that is required for the rectifier-leg transistors is bidirectional conduction ability and low conduction losses. A good choice for these transistors would thus be slow-switching MOSFETs with a low $R_{DS,on}$. Rearranging (2.22) and setting $P_{cond,SR,max} = P_{SR} =$ 17W, the span of allowed $R_{DS,on}$ for the rectifier-leg mosfets can be found as follows:

$$R_{DS,on,SR} \leq 2\frac{P_{cond,SR,max}}{I_{AC}^2} = 132.8\text{m}\Omega \tag{3.10}$$

Thus, any MOSFET with an $R_{DS,on} \leq 132.8\text{m}\Omega$, voltage rating > 400V and drain-source current capability > 22.5A would be suiting for this solution. A quick

Table 3.6: Some key parameters and rated values of MOSFET IPW60R045CPA at $T_{case} = 25°C$.

Parameter	Value
$R_{DS,on}$	45mΩ
$R_{DS,on}$ (@150°C)	110mΩ
V_{DS}	600V
V_{GS}	-20V to +20V
I_{DS}	60A
I_{DS} (@100°C)	38A
V_{SD} (Diode FV)	0.9V

search reveals many possible solutions, but Infineon's previously analyzed automotive MOSFET *IPW60R045CPA* is chosen, with key parameters shown in table 3.6.

3.3 Boost inductor

Design of magnetic components for power electronics is a research field of its own, and an overview of the challenges faced can be found in [24, ch. 30]. For the sake of this master's thesis, when designing the boost inductor, the magnetic design itself is regarded out of scope. The design process will revolve around choosing from existing inductor technologies, considering mainly three factors: Inductance value, RMS current rating and peak current rating.

3.3.1 Boost inductance value

The boost inductance value L, along with the magnitudes of v_{AC} and V_d, dictates the slope of the inductor current in every switching interval according to (2.1) and (2.2). These equations imply that a higher switching frequency would require a smaller inductance for the same maximum ripple, and likewise with a higher maximum ripple for the same frequency, as both of these cases would increase the required slope. For that reason the boost inductance, L, needs to be designed small enough to allow for the desired switching frequency and large enough limit the current ripple to its maximum allowed value.

The equations for the inductor ripple is developed in section 2.3.1. It is shown in (2.6) that the ripple is proportional to the DC-link voltage, meaning the maximum inductor current ripple occurs at the maximum DC-link voltage. Figure 2.5 also shows that the maximum inductor current ripple occurs at duty cycle $d = 0.5$. Using this information, an expression for maximum inductor current ripple is found from (2.6):

$$\Delta i_{L,max} = \frac{0.25 V_{DC,max}}{f_{sw} L} \, . \tag{3.11}$$

Solving (3.11) for L, an expression is developed for the boost inductance value:

$$L = \frac{0.25 V_{DC,max}}{f_{sw} \Delta i_{L,max}} \, . \tag{3.12}$$

Defining the AC-side current ripple to be set at 20% of peak AC current accord-

ing to the bidirectional PFC specifications presented in table 1.2, the maximum current ripple becomes $\Delta i_{L,max} = 0.2 \cdot \hat{I}_{ac} = 4.52\ A$. The switching frequency has been chosen at $f_{sw} = 90$kHz and the maximum DC-link voltage is $V_{DC,max} = 400$V. Inserting these data in (3.12), the resulting value of the boost inductance is found to be:

$$L \geq 245.82\mu\text{H} .$$

3.3.2 RMS current rating

Overly high RMS currents in magnetic core inductors can lead to saturation of its core material or overheating due to resistive losses in the windings and eddy current losses in the core.[24, ch. 30] Thus, the inductor needs to be designed with sufficient RMS current rating. It is found in section 2.3.2 and (2.11) that the RMS current in the inductor is equal to the AC-grid RMS current. That means the inductor current rating should comply with the AC current rating described in table 1.1, giving the following inductor RMS current rating:

$$I_{L,rated} = 16\text{A} .$$

3.3.3 Saturation current rating

Although continuous currents can cause magnetic core saturation in the inductor, this is a more adjacent issue with the peak currents, especially in switch-mode converters, where a current ripple is in fact necessary to control the output and input currents and voltages. [24, ch. 30] The maximum peak-to-peak current ripple is defined in table 1.2, to be 20% of the peak current value. Using that, the minimum peak current rating of the inductor can be defined as follows:

$$I_{L,sat} = (1+0.1)\sqrt{2}I_{AC,max} = 24.89\text{A}$$

Table 3.7: Estimated inductor parameters based on technology used by Valeo Siemens today.[1]

Parameter	Value
L	245.82μH
R_L	10mΩ
I_{rated}	16Arms
$P_{loss,est}$(100°C)	17W

3.3.4 Choice of inductor

Unlike the capacitor and transistors, who are mostly off-the-shelf components, the inductor is a more easily customizable component, where performance for an inductor with a certain core design is dependent on e.g. number of windings thickness of windings.[24] For this application and for the sake of the simulation model it is chosen to use the same inductor technology as is used by Valeo Siemens today, assuming that windings are chosen to achieve exactly the desired inductance. The inductor is powder-core, toroid-shaped with copper wires, and reasonable parameters based on this technology are presented in table 3.7.[1] Saturation current rating is not mentioned in the data sheet. The data for estimated power losses are found in data sheets, and comparing it to table 3.7 it is clear that it does not exceed the estimated losses of the inductor and rest of PFC.

Chapter 4

Drive and control

In a PFC, as in any other switched-mode converter, the control system and gate drivers are essential to its operation; they govern the average current through - and voltage across - the switches, controlling currents and voltages in the rest of the converter.[24, ch. 28] Control-wise, a PFC has two objectives: It needs to control the AC current to be sinusoidal and in phase with the AC voltage, and it needs to control the average value of the DC-side voltage. In the following, the gate driver logic and the control system will be developed for the ideal proposed bidirectional totem-pole PFC converter, to build the simulation model and verify the basic operation of this converter. The control system will be built using average current mode control.[41, 42, 43] Current and voltage control loops will be analyzed separately and designed with PI controllers and symmetrical optimum tuning.[44] The MATLAB scripts used for tuning are shown in appendix F. The practical implementation of the gate drivers will be neglected for this analysis.

4.1 Gate drive logic

Gate drives are the bridge between the desired linear behaviour of the converter and the highly nonlinear behaviour of the transistors. The gate drives converts a linear control signal to switch the transistors on and off so that the switching-period average currents and voltages are behaving as desired. The gate drive logic for both switching legs implemented in Simulink is shown in figure 4.1. For the explanation of the controller mechanisms the *enable* switches can be ignored, as they are simply there to turn the gate signals on or off. The *turn-on delay* blocks can also be ignored for the explanation of the gate drive logic, as they do not affect the basic theory. They are there to provide a blanking time at the turn-on of the switches, ensuring that the complementary transistor is properly turned off before turning on the relevant transistor and hence preventing cross conduction and possible malfunctioning of the transistors. [24, ch. 28-6-2]

4.1.1 Rectifier leg

Let us first look at the rectifier leg. The rectifier-leg switches change the DC-voltage polarity seen by the inductor every mains half cycle according to the AC mains voltage polarity. This ensures that the DC voltage is always of the same polarity and higher magnitude than the AC voltage, and that the power flows in the same direction in both half cycles. This is achieved by *Comparator SR* in figure 4.1, comparing the measured AC voltage to ground, giving out high voltage when $v_{AC} < 0$ and zero when $v_{AC} > 0$. As explained in sections 2.1 and 2.2, S_{R1} is always conducting during negative half cycle and S_{R2} is always conducting during the positive. That means the output gate signal of *Comparator SR* is equal to the gate voltage of S_{R1}, v_{SR1}. In this application it is assumed that the MOSFET reverse body diode will not be used, but rather that the active part of the MOSFET is turned on when conducting. Thus, S_{R2} needs to be switched complementarily to S_{R1}, meaning the gate signal needs to be the logical inverse of v_{SR1}. This is accomplished by placing the logical *NOT* operator as shown in figure 4.1. The gate signals will be distributed as following:

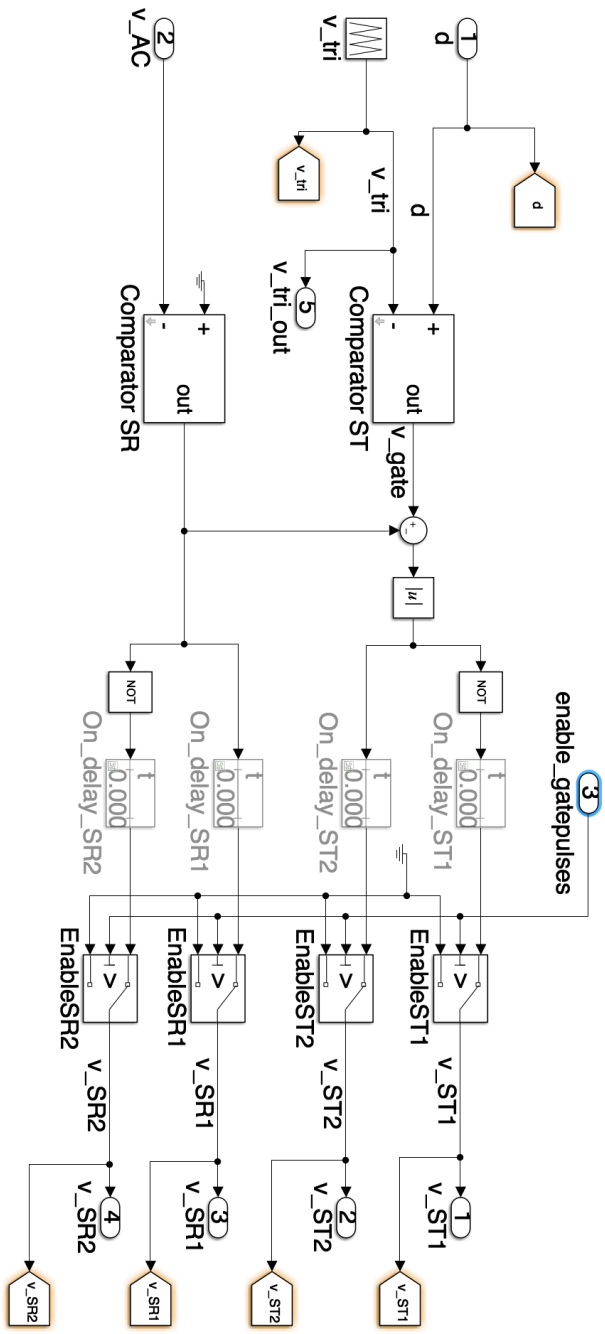


Figure 4.1: A screenshot of the PWM system implemented in Simulink.

$$
\begin{aligned}
v_{SR1}(t) &= \begin{cases} 0, & v_{AC}(t) > 0, \\ V_{high}, & v_{AC}(t) < 0, \end{cases} \\
v_{SR2}(t) &= \begin{cases} V_{high}, & v_{AC}(t) > 0. \\ 0, & v_{AC}(t) < 0. \end{cases}
\end{aligned} \tag{4.1}
$$

This is the same both in G2V and V2G, as one can see from figures 2.2 and 2.3.

4.1.2 Totem leg

The totem-leg switches are switched at high frequency with boost/buck control to shape the boost inductor current. In this case two methods are relevant for controlling the gate voltage signal to the transistors: Hysteresis and PWM. Hystheresis control is the faster control alternative, as it requires no computation of the duty cycle of the switches, but simply switches on/off when the current reaches the lower and higher ripple peak reference. However, for variation in reference signals, a varying switching frequency is achieved with hystheresis control. [40, ch. 2.3.1] This gives a great variation in the current ripple frequencies to be filtered out by the DM filter, creating difficulties in DM filter design. Using PWM, on the other hand, a constant switching frequency can be achieved in CCM, simplifying the DM filter design. For that reason, PWM is the gate voltage control method of choice for this application.

The pulse width modulator operates as the simple DC-DC pulse width modulator in [24, ch. 7-2], consisting of *Comparator ST* comparing a strictly positive control signal, duty cycle d, to a triangular reference signal v_{tri} with amplitude 1, generating a gate signal v_{gate}, as in figure 4.2. In G2V operation, this is just like in a regular boost PFC controller; the gate signal is the gate voltage of the boost switch. The difference in the totem-pole boost PFC is how this gate signal is handled. First of all, the totem-leg switches are switched complementarily, where one switch acts as the boost switch while the other imitates the boost diode, as shown in section 2.1. The GaN eHEMT does not contain a reverse body diode and no diode is connected in anti-parallel (figure 3.2), meaning the complementary switch needs to be

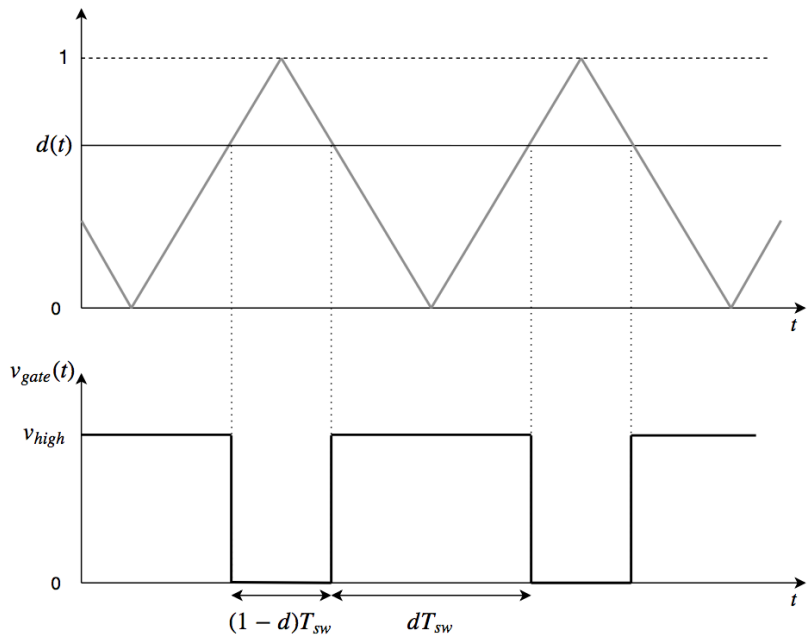


Figure 4.2: Illustration of the pulse width modulation used in this

operated actively. This is achieved with the *NOT* operator, as for the rectifier leg.

Moreover, unlike a regular boost PFC, which has a rectified boost inductor current, because of the passive rectifier at the AC-side (figure B.1), the boost inductor of the totem-pole PFC is connected to the AC-side, meaning the boost inductor current needs to be shaped as a sinusoidal AC signal oscillating from negative to positive. Still, the control signal is assumed to be the duty cycle $d(t)$ of a regular boost PFC, which is purely positive. This is compensated as explained in section 2.1, by, for every other mains half cycle, interchanging which totem-leg switch is operating as boost switch and which is imitating the diode. The effective duty cycle of the gate signal of each of the switches throughout the mains cycle can be written as follows:

$$
\begin{aligned}
d_{ST1}(t) &= \begin{cases} 1-d(t), & v_{AC}(t) > 0, \\ d(t), & v_{AC}(t) < 0, \end{cases} \\
d_{ST2}(t) &= \begin{cases} d(t), & v_{AC}(t) > 0. \\ 1-d(t), & v_{AC}(t) < 0. \end{cases}
\end{aligned}
\tag{4.2}
$$

Acknowledging that for high switching frequencies $f_{sw} \gg f_{AC}$ with gate voltage amplitudes of $V_{high} = 1$ in figure 4.2, the duty cycles can be written as follows:

$$
d(t) = v_{gate,avg}(t)\ , \quad d_{ST1}(t) = v_{ST1,avg}(t)\ , \quad d_{ST2}(t) = v_{ST2,avg}, \tag{4.3}
$$

where $v_{gate,avg}$, $v_{ST1,avg}$ and $v_{ST2,avg}$ are the floating switching-period averages of v_{gate}, v_{ST1} and v_{ST2}. Applying (4.3) to (4.2), it can be shown that the totem-leg switches gate voltages can be written as follows:

$$
\begin{aligned}
v_{ST1}(t) &= \begin{cases} 1-v_{gate}(t), & v_{AC}(t) > 0, \\ v_{gate}(t), & v_{AC}(t) < 0, \end{cases} \\
v_{ST2}(t) &= \begin{cases} v_{gate}(t), & v_{AC}(t) > 0. \\ 1-v_{gate}(t), & v_{AC}(t) < 0. \end{cases}
\end{aligned}
\tag{4.4}
$$

The gate voltages are logical signals of true or false, in this case 1 or 0. Thus, it is clear that the negative-half-cycle gate signals can be achieved by logically inverting the positive-half-cycle gate signals. To perform this logical inversion, a handy way of rewriting the gate voltages during negative half cycle can be:

$$
\begin{aligned}
v_{ST1}(t) = v_{gate}(t) &= 1 - |v_{gate}(t) - 1|\ , \quad v_{AC}(t) < 0\ , \\
v_{ST2}(t) = 1 - v_{gate}(t) &= |v_{gate}(t) - 1|\ , \quad v_{AC}(t) < 0\ .
\end{aligned}
\tag{4.5}
$$

The equation (4.5) puts the negative-half-cycle gate signals on the same form,

$v_{ST1} = 1 - u$ and $v_{ST2} = u$, as the positive-half-cycle signals in (4.4). Now, all that needs to be handled is u, which is either v_{gate} or $|v_{gate} - 1|$, depending on the mains half cycle. Using (4.5) and recognizing from (4.1), with $V_{high} = 1$, that v_{SR1} is 0 for $v_{AC} > 0$ and 1 for $v_{AC} < 0$, a simple way of handling u and creating the desired gate voltages in (4.4) can be the following:

$$\begin{aligned} v_{ST1}(t) &= 1 - |v_{gate}(t) - v_{SR1}(t)| \ , \\ v_{ST2}(t) &= |v_{gate}(t) - v_{SR1}(t)| \ . \end{aligned} \tag{4.6}$$

This is implemented in figure 4.1 with the forward connection from the rectifier-leg system to the totem-leg system.

V2G

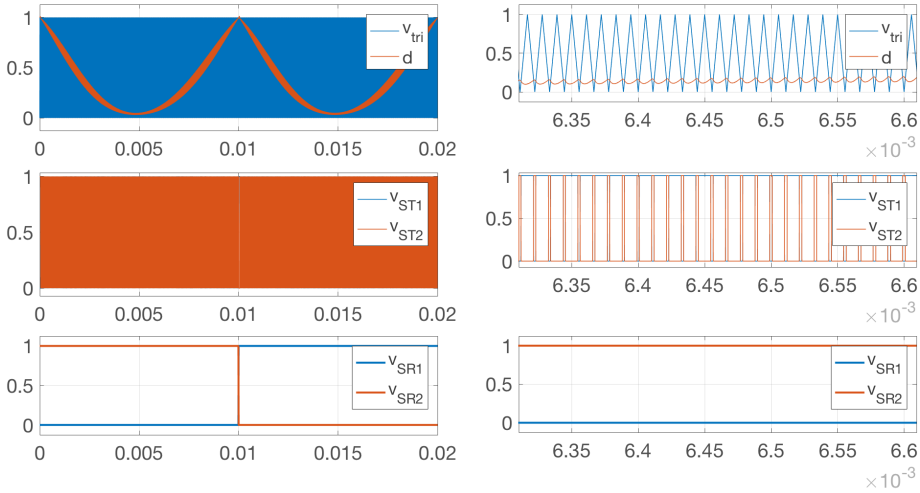
In *V2G*, the PFC operates as a buck converter from DC-link to grid, in stead of as a boost converter from grid to DC-link. However, comparing the AC to DC voltage ratios based on the duty cycle definitions of buck and boost operation, [24, ch. 7]

$$\frac{v_{AC}(t)}{V_{DC}} = \begin{cases} d_{buck}(t) & \text{for buck operation} \ , \\ 1 - d_{boost}(t) & \text{for boost operation} \ , \end{cases} \tag{4.7}$$

it is clear that $d_{buck} = 1 - d_{boost} = 1 - d$, i.e. that the boost and buck switching are complementary to each other. Thus, since the figures 2.2 and 2.3 show that the buck switch is always the complementary switch to the boost switch, the totem-leg gate voltages during V2G are also controlled by (4.2) and (4.6). In other words, the shape and phase of the gate voltages do not change during V2G

4.1.3 Waveforms

For verification of the gate drive operation a simulation is performed, with results shown in figure 4.3. It shows the duty cycle d, the triangular voltage v_{tri} and the gate voltages V_{ST1}, V_{ST2}, V_{SR1} and V_{SR2} in G2V operation, which is the same for



(a) One mains cycle **(b)** Zoomed

Figure 4.3: Duty cycle and gate drive signals over one mains cycle and zoomed in on a few switching cycles.

V2G operation. The waveforms throughout one mains cycle in figure 4.3a and over a few switching cycles in figure 4.3b show that the switches are operated complementarily according to the control laws described above.

4.2 Control system

For the PFC control system, it is necessary with two control loops: the current control loop and the voltage control loop, since the PFC is assigned to controlling both the inductor current and th DC-link voltage. The control loops are developed based on small signal modelling and quasi-steady-state approach, with the non-linear transistor currents and voltages represented as linearized currents and voltages around their switching-period average.[45, 42] In the current control loop the switching-period average inductor current is controlled to be shaped sinusoidally in phase with the mains voltage – or shifted 180 degrees in V2G, while the voltage control regulates the average DC-link voltage to be equal to a defined DC value. PI controllers are used in both the current and the voltage loop. The complete PFC control system, as implemented in Simulink, is depicted in figure 4.4. It is shown in the figure that the controllers take in measurements of the inductor AC current i_{AC}, the AC voltage v_{AC} and the instantaneous DC-link voltage v_{DC}, while the output is the boost duty cycle d that is input in the PWM system. It is assumed that all of the measured currents and voltages can in fact be measured, although the AC voltage would have to be measured through a transformer, for isolation between the control system and grid. [46] The following section will develop the current and voltage controller equations, tune the PI controllers and discuss current and voltage measurement filter design, all with reference to the Simulink model in figure 4.4. For the tuning of current and voltage PI controllers, modulus and symmetrical optimum will be used. It should also be noted that the converter could have been made to operate with reactive power compensation with some modifications of the control system to allow phase shifting of the current, but this is considered out of scope for this analysis and left for further work.

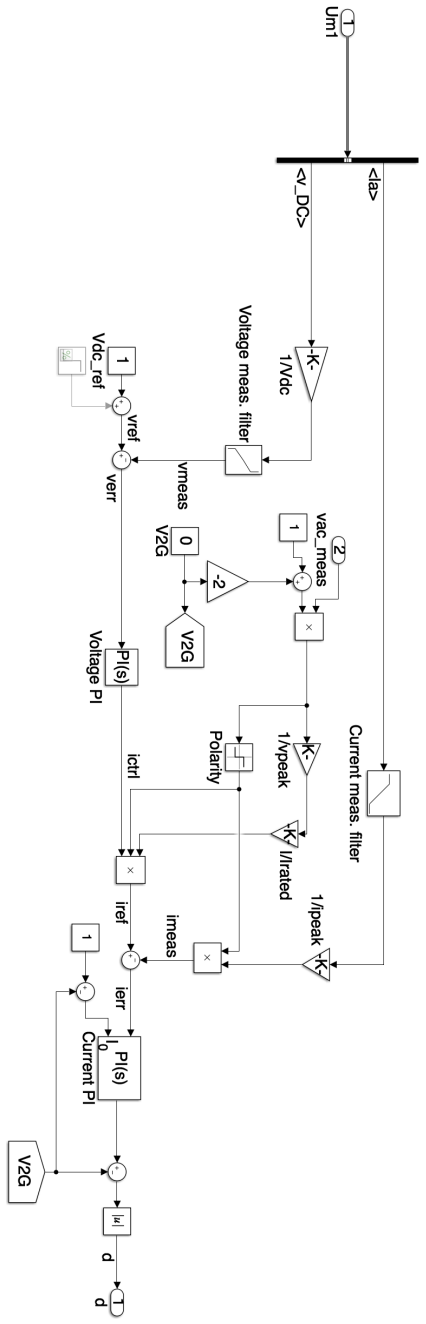


Figure 4.4: Current and Voltage control systems implemented in Simulink

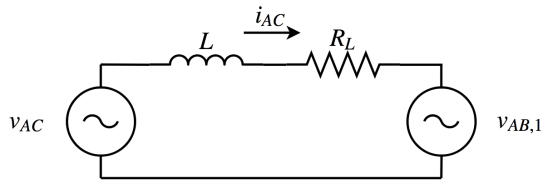


Figure 4.5: The fundamental-frequency equivalent totem-pole PFC

4.2.1 Control logic

As explained in section 4.1, the pulse width modulator is designed assuming a control signal equal to the duty cycle of the boost converter in a regular boost PFC. This choice simplifies the control system design, since the control system logic can then be largely based on existing boost PFC control systems, which is a well-developed field of research.[45] Some modifications need to be made: bidirectional power flow is enabled through some small modifications and the measured current and reference current need to be rectified; the inductor current in a regular boost PFC is rectified, as opposed to the totem-pole PFC inductor current, which is AC (section 2.3). The latter is implemented by multiplying both the inductor current and the measured inductor current with the polarity of the current reference, as shown in figure 4.4.

The implemented controller is based on the basic current mode boost PFC.[41] This control technique is beneficial for this high-power application, because it allows the desired CCM operation and constant switching frequency.[45] Normally in average current mode control, a third current slope compensation loop will be added, due to poles and zeros changing depending on the duty cycle.[43, 47] This effect is neglected for this analysis, where the current controller and voltage controller power stages will be analyzed separately, as will be shown in sections 4.2.2 and 4.2.3. The current mode control is implemented as shown in figure 4.4 and [41], by multiplying the output of the outer voltage control loop, *ictrl*, with the reference to the inner current control loop, while the current controller directly controls the duty cycle.

An expression for the time-varying duty cycle $d(t)$ can be derived using small-signal modelling and the quasi-static approach, investigating the fundamental cur-

rents and voltages; the objective is shaping the fundamental, switching-period average inductor current in phase with the AC voltage. It is common in small-signal-modelling analysis of unidirectional PFCs to model the converter and load as an emulated resistance, ensuring that the drawn power is resistive for maximum power factor. [45, 42, 46] This approach is, however, not as intuitive in a bidirectional PFC, where the converter seen from the grid will work as a power source during V2G. Although one could create a fictious negative resistance, another, perhaps more intuitive solution is modelling the totem-pole converter as a V_{DC}-driven voltage source. Looking only at the fundamental components, and exploiting that the boost inductor in a totem-pole PFC in on the AC side, the PFC can be equivalated to the simple two-voltage-source system shown in figure 4.5, based in figure 2.1. Assuming perfect operation and unity power factor, i.e. the AC voltage and current both having zero phase angle, a phasor form equation can be obtained:

$$I_{AC,1} = \frac{V_{AC} - V_{AB,1} e^{j\theta_{AB,1}}}{Z_L e^{j\theta_L}}, \quad \text{where} \quad Z_L e^{j\theta_L} = R_L + j\omega L \, . \tag{4.8}$$

The phasor form is useful in this case, because for the sake of the current controller we are only interested in the phase and amplitude of the inductor current. Investigating figure 2.1, it is clear that the gate voltage v_{AB} will take the following values:

$$v_{AB}(t) = \begin{cases} v_{DC}(t), & S_{T1} on, v_{AC}(t) > 0 \, , \\ 0, & S_{T2} on, v_{AC}(t) > 0 \, , \\ 0, & S_{T1} on, v_{AC}(t) < 0 \, , \\ -v_{DC}(t), & S_{T2} on, v_{AC}(t) < 0 \, . \end{cases} \tag{4.9}$$

From (4.9) it can be found, based on the duty cycle analysis in section 4.1.2, that the fundamental gate voltage $v_{AB,1}(t)$ can be written as follows:

$$v_{AB,1}(t) = \begin{cases} d_{ST1}(t) \cdot v_{DC}(t) = (1 - d(t)) \cdot v_{DC}(t) \, , & v_{AC} > 0 \, , \\ d_{ST2}(t) \cdot (-v_{DC}(t)) = (1 - d(t)) \cdot (-v_{DC}(t)) \, , & v_{AC} < 0 \, . \end{cases} \tag{4.10}$$

Based on (4.10), a new, equivalent duty cycle function $d_{ST,eq}(t)$ can be defined:

$$d_{ST,eq}(t) = \begin{cases} d_{ST1}(t) = 1 - d(t) \ , & v_{AC} > 0 \ , \\ -d_{ST2}(t) = d(t) - 1 \ , & v_{AC} < 0 \ , \end{cases} \tag{4.11}$$

which implemented in (4.10) gives:

$$v_{AB,1}(t) = d_{ST,eq}(t) \cdot v_{DC}(t) \ . \tag{4.12}$$

During PFC operation, the DC-voltage ripple will usually be much smaller than the average value (in this case 20V versus 340V), which means it can be approximated as constantly equal to the average DC voltage when considering the current control. Using that, (4.12) can be approximated as

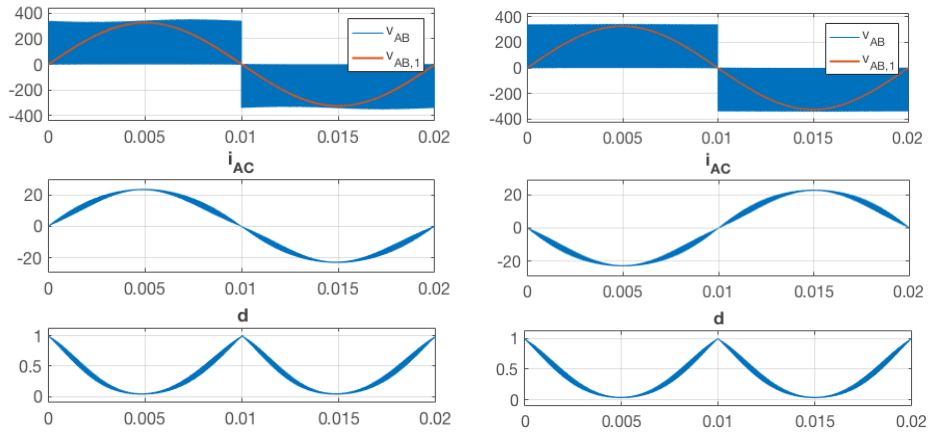
$$v_{AB,1}(t) \approx V_{DC} \cdot d_{ST,eq}(t) = V_{DC} \cdot \hat{d}_{ST,eq} \sin(\omega t + \theta_{AB,1}) \ . \tag{4.13}$$

Finally, a expression can be derived for the duty cycle, based on (4.11) and (4.13):

$$d(t) = 1 - |d_{ST,eq}(t)| = 1 - \frac{\hat{V}_{AB,1}}{V_{DC}} |\sin(\omega t + \theta_{AB,1})| \tag{4.14}$$

Comparing (4.14) to (4.8), a key take-away is that since the AC voltage and the boost inductor impedance are uncontrollable, the inductor fundamental current and thus power is controlled by the amplitude and phase of the duty cycle. Since Z_L is small, only small variations in duty cycle phase and amplitude will be necessary. The shape or polarity of the fundamental duty cycle does not change in V2G operation compared to G2V operation; it is always given by 4.14, as is shown in figure 4.6.

In the implemented current loop in figure 4.4, this is ensured by the logical inverter on the PI controller output, which is enabled during V2G. When V2G is activated, the constant source called *V2G* is set to 1, inverting the polarity of the reference current and the measured inductor current. This however also inverts the current error signal entering the PI controller. To fix this, the mentioned logical inverter is



(a) G2V **(b)** V2G

Figure 4.6: Some selected waveforms over one mains cycle in G2V and V2G operation.

enabled during V2G, correcting the waveform of the output duty cycle so that it is unchanged compared to G2V.

The inversion of the input signals to maintain the duty cycle signal shown in figure 4.6 is an advantage, as will be explained now. In the opposite case, if the reference current and measured inductor current were not inverted, the duty cycle signal would change shape every half cycle. However, since the duty cycle has to take a value between 1 and 0, the duty cycle would have to alternate between $1 - v_{AB,1}(t)/V_{DC}$ during positive mains half cycle and $-v_{AB,1}(t)/V_{DC}$ during the negative half cycle. That requires the duty cycle to drop instantaneously from 1 to 0 in the transition from positive to negative half cycle and leap instantaneously from 0 to 1 in the transition from negative to positive half cycle. Following this duty cycle path requires a nearly infinitely fast current controller, which is not possible to implement, first of all due to a restriction saying that the bandwidth of the current controller should be at least half a decade lower than the switching frequency, which is at 90kHz.[40] In comparison, the duty cycle achieved through the proposed control logic (figure 4.6) contains no sudden leaps or drops, improving stability considerably.

Having established in figure 4.6 that the control system is functioning, it is due to direct some critique towards the implemented solution. First of all, the con-

trol circuitry of the average current mode PFC controller is quite complex, with a multiplied voltage loop and current loop. This issue could have been addressed by implementing e.g. linear peak current mode control or other techniques for estimating the AC voltage, so that the voltage measurement becomes unnecessary. [42, 48] On the other hand, the control system could be implemented digitally, in which case the control circuitry would not be as complex. Another issue is the necessity of measuring the AC voltage through a voltage transformer, implying a risk of low energy density. This issue could also be addressed through the mentioned AC voltage estimation techniques, not needing to measure the voltage. In any case, the control structure provides a reference when designing new, improved control systems for bidirectional PFC converters, using e.g. the techniques mentioned above.

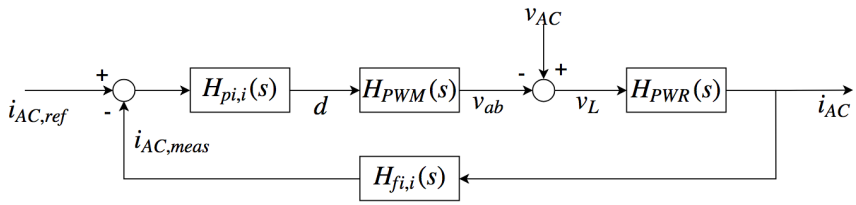


Figure 4.7: The inner current control loop

4.2.2 Current control loop

Of the two controllers, the current control loop needs to be the fastest, much due to the reference signal oscillating sinusoidally with 50Hz. In general control theory, the inner loop needs to be faster than the outer control loop to be able to provide proper response to the reference signal from the outer loop, meaning that the current loop needs to be the inner loop. Thus the current control loop will be developed first.

The general Laplace plane current control loop is chosen as shown in figure 4.7, where $H_{pi,i}(s)$, $H_{PWM}(s)$, $H_{PWR}(s)$ and $H_{fi,i}(s)$ represent the transfer functions of the PI regulator, PWM, power stage and current measurement filter, respectively. For the PI regulator, the general transfer function is as follows:

$$H_{pi,i} = K_{p,i}\left(\frac{T_{i,i}\cdot s+1}{T_{i,i}\cdot s}\right), \tag{4.15}$$

where the $K_{p,i}$ is the proportional gain and $T_{i,i}$ is the integrator time constant. This will be tuned later and is left for now. Moving to the PWM, the transfer function is dependent on the modulation technique, but is usually modelled as a switching-frequency dependent time delay. [40, ch. 3.2.5] The delay is due to the gate voltage pulse widths not being able to update continually within one switching period. In the PWM system described in section 4.1, natural-sampled triangular PWM is used, as shown in figure 4.2, which, according to [40, ch. 3.2.5], gives a time delay $T_{delay,PWM} = T_{sw}/3$ with a corresponding transfer function:

$$H_{PWM}(s) = \frac{1}{1+T_{delay,PWM}\cdot s} = \frac{1}{1+\frac{1}{3}T_{sw}\cdot s}. \tag{4.16}$$

So, to the power stage, which for the current control is approximated as solely the inductor, since the variable to be controlled is the fundamental-harmonic current through the inductor. Referring to figure 2.1, the inductor current $I_{AC}(s)$ can be expressed in Laplace transform as follows:

$$i_{AC}(s) = \frac{v_{AC}(s) - v_{ab}(s)}{R_L + L \cdot s} \ , \tag{4.17}$$

where R_L is the inductor equivalent resistance. The control variable is the bridge gate voltage $V_{AB}(s)$, while $V_{AC}(s)$ can be seen as a disturbance from the control point of view. Thus, from (4.17), the power-stage transfer function can be written

$$H_{PWR}(s) = \frac{v_{AC}(s)}{v_{AB}(s)} = \frac{1}{R_L + L \cdot s} = \frac{1}{R_L} \frac{1}{1 + \frac{L}{R_L} \cdot s} \ . \tag{4.18}$$

As for the current measurement filter, the purpose of this is to suppress switching-frequency and higher-frequency current noise going into the controller, potentially making the controller generate more harmonics. [40, ch. 3.4] Thus, a simple first-order low-pass filter is evaluated to be sufficient for this application, with transfer function:

$$H_{fi,i}(s) = \frac{1}{1 + T_{fi,i} \cdot s} \ , \tag{4.19}$$

where $T_{fi,i}$ is the current measurement filter time constant. Having established these transfer functions, the open-loop current controller transfer function becomes

$$\begin{aligned} H_{ol,i}(s) &= H_{pi,i} \cdot H_{PWM}(s) \cdot H_{PWR}(s) \cdot H_{fi,i}(s) \ , \\ &= \frac{K_{p,i}}{T_{i,i} R_L} \cdot \frac{1 + T_{i,i} \cdot s}{s \cdot (1 + T_{PWM} \cdot s)(1 + \frac{L}{R_L} \cdot s)(1 + T_{fi,i} \cdot s)} \ . \end{aligned} \tag{4.20}$$

To simplify this transfer function, it can be utilized that $T_L = L/R_L$ is considerably larger than $T_{i,i}$ and $T_{fi,i}$, the two smaller time constant, as an approximation, can be merged into one time constant $T_{sum,i} = T_{i,i} + T_{fi,i}$ in a first-order filter.[40, ch. 3] The open-loop transfer function (4.20) can be rewritten as

$$H_{ol,i}(s) = \frac{K_{p,i}}{T_{i,i}R_L} \cdot \frac{1 + T_{i,i} \cdot s}{s \cdot (1 + T_{sum,i} \cdot s)(1 + \frac{L}{R_L} \cdot s)} \ . \tag{4.21}$$

Simplifying the system from a fourth-order to a third-order system like this greatly facilitates the controller tuning that follows, and is a great advantage as such.

PI tuning: Modulus optimum

Now to the PI controller tuning, where expressions for the gain and time constant of the PI controller must be developed. As stated in the previous, the power stage time constant is $T_{PWR} = L/R_L \gg T_{sum}$. This opens for use of the controller tuning technique called *Modulus optimum*, which involves cancelling out the slowest pole with the dominant time constant, if present, by setting $T_{i,i}$ equal to the dominant time constant. [40] By doing that, the control loop is effectively reduced to a simpler second-order system. Moreover, since the less dominant time constants correspond to higher cutoff frequencies, a higher crossover frequency can be achieved for the whole current loop, while maintaining a sufficient phase and gain margin. [49]

However, an issue with the modulus optimum for this application appears when the time constant is calculated based on the inductor parameters in section 3.3. The integrator time constant is chosen:

$$T_{i,i} = \frac{L}{R_L} = \frac{245\mu\text{H}}{10\text{m}\Omega} = 0.0245\text{s} \ . \tag{4.22}$$

Taking into account that the reference signal will be a rectified 50Hz sine (figure 4.4), effectively having a frequency of 100Hz, the time period of this signal will effectively be $T_{ref} = 0.01$s. That means the reference signal is faster than the integrator time constant of the PI controller, and the controller will have difficulties following the reference signal. Section D.1 in the appendix shows a full derivation of the modulus optimum tuning parameters along with simulation results confirming that the controller is not able to follow the reference. Thus, another PI controller tuning technique is attempted, called *Symmetrical optimum*, which gives greater freedom in choosing integrator time constant.

PI tuning: Symmetrical optimum

The Symmetrical optimum tuning technique, described in [44], involves choosing the integrator time constant to lift the phase around the crossover frequency of the control loop, that way increasing the phase margin and gain margin to increase system stability. [49] For that reason, poles with large, dominant time constants that have a cutoff frequency themselves that is far away from the crossover frequency of the whole control loop can be regarded as free integrators. [44] Applying that to the current controller open-loop transfer function in (4.21), a new, approximated transfer function is developed:

$$H_{ol,i}(s) = \frac{K_{p,i}}{T_{i,i}L} \cdot \frac{1 + T_{i,i} \cdot s}{s^2 \cdot (1 + T_{sum,i} \cdot s)} \ . \tag{4.23}$$

The resulting closed-loop transfer function is:

$$H_{cl,i}(s) = \frac{1 + T_{i,i} \cdot s}{1 + T_{i,i} \cdot s + \frac{LT_{i,i}}{K_{p,i}} \cdot s^2 + \frac{LT_{i,i}T_{sum,i}}{K_{p,i}} \cdot s^3} \ . \tag{4.24}$$

From that, the PI controller parameters can be chosen based on the following Symmetric optimum design equations: [40, ch. 3.2.4]

$$T_{i,i} = \beta_i \cdot T_{sum,i} \ , \quad K_{p,i} = \frac{L}{\sqrt{\beta_i} T_{sum,i}} \ , \quad \omega_{c,i} = \frac{1}{\sqrt{\beta_i} T_{sum,i}} \ , \tag{4.25}$$

where $\omega_{c,i}$ is the crossover frequency and β_i is defined from that the phase of the transfer function is lifted from $1/(\beta_i T_{sum,i})$ to $T_{sum,i}$. The current control loop needs to be at least half a decade slower than the switching frequency to ensure that the switches are able to respond to the control signals. Thus, taking into account that the reference signal is varying with a frequency of 100Hz, the controller parameters in (4.25) are chosen from a crossover frequency as close as possible to $10^{-0.5} * \omega_{sw}$ while still keeping a β_i within reasonable values.

In order to determine the controller parameters, the current measurement filter time constant, $T_{fi,i}$, needs to be determined first. While a filter suppresses certain frequencies, it is essentially also a delay. Therefore the filter time constant is cho-

sen to limit the ripple of the duty cycle, while at the same time maintaining a fast response by not choosing the time constant too big. A certain amount of switching-frequency current ripple is inevitable in a PFC, since the boost inductor can not be chosen infinitely large, and so keeping the ripple of the current measurement at a low level is important to avoid the controller generating more harmonics. A typical design rule is keeping the duty cycle ripple amplitude in the range of 0.04 to 0.08, where a bigger ripple implies a faster response. [40, ch. 3.2.4]

Current filter design using Modulus optimum is performed in section D.1 in the appendix, and the filter time constant can be found in a similar way with Symmetrical optimum. Substituting into (D.7) the expression for $K_{p,i}$ in (4.25), an expression for the for the duty cycle ripple amplitude is achieved as follows:

$$\hat{d}_{ripple}(\omega_{ripple}) = \frac{L}{\sqrt{\beta_i} T_{sum,i}} \cdot \frac{1}{\sqrt{1+(\omega_{ripple} T_{fi,i})^2}} \cdot \frac{1}{2} \Delta I_L(\omega_{ripple}) \ . \tag{4.26}$$

Substituting β_i in (4.26) with the expression for $\omega_{c,i}$ in (4.25), another expression is obtained:

$$\hat{d}_{ripple}(\omega_{ripple}) = \omega_{c,i} L \cdot \frac{1}{\sqrt{1+(\omega_{ripple} T_{fi,i})^2}} \cdot \frac{1}{2} \Delta I_L(\omega_{ripple}) \ . \tag{4.27}$$

In (4.27), there is now two free variables governing the duty cycle ripple: $\omega_{c,i}$ and $T_{fi,i}$. As mentioned, we wish to choose the crossover frequency as close as possible to $10^{-0.5} \cdot \omega_{sw}$, while keeping β_i within reasonable limits. Maximum crossover frequency is:

$$\omega_{c,i} \leq 10^{-0.5} \cdot 2\pi \cdot 90\text{kHz} = 178823\text{rad/s}$$

A reasonable β_i is defined in [40] to range from 1 to 25. Choosing a crossover frequency

$$\omega_c = 10^{-0.8} \cdot \omega_s w = 89624\text{rad/s} \ ,$$

(4.27) is solved graphically at the switching frequency, $\omega_{ripple} = \omega_{sw}$, in figure 4.8. Prioritizing fast controller response over low control signal ripple, the duty cycle

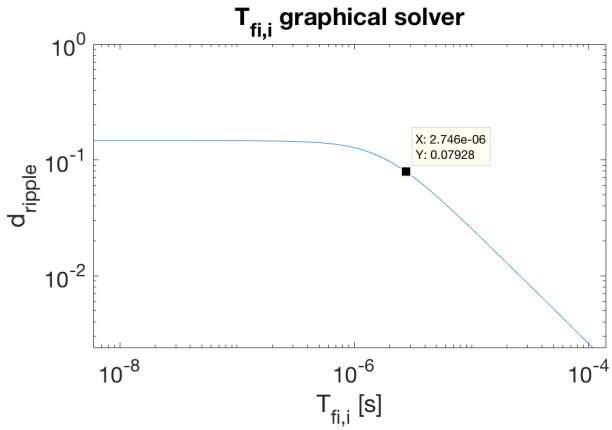


Figure 4.8: Graphical solution of (4.27) to find $T_{fi,i}$

ripple amplitude is chosen at $\hat{d}_{ripple} = 0.08$, giving

$$T_{fi,i} = 2.7 \cdot 10^{-6}\text{s} \, .$$

From (4.25) this gives $\beta_i = 3.04$, which is within the reasonable limits of 1 to 25, verifying the chosen crossover frequency. Implementing the values for ω_c, $T_{fi,i}$ and β_i into (4.25), the controller parameters are found to be

$$K_{p,i} = 1.4644 \, , \quad T_{i,i} = 19.44 \cdot 10^{-6}\text{s} \, .$$

Comparing to the integrator time constant using Modulus optimum, this $T_{i,i}$ is more than 4 decades lower, and thus also much lower than the reference signal time period at 0.01s, which should lead to a better system response.

Simulations

To verify the controller design, simulations are performed with no voltage controller connected, and the current controller tuned with the Symmetrical optimum parameters described above. The results are shown in figure 4.9, where *iref* is the per unit rectified current reference, *imeas* is the per unit rectified measured indutcor current, *ierr* is $iref - imeas$ and d is the boost-switch duty cycle control

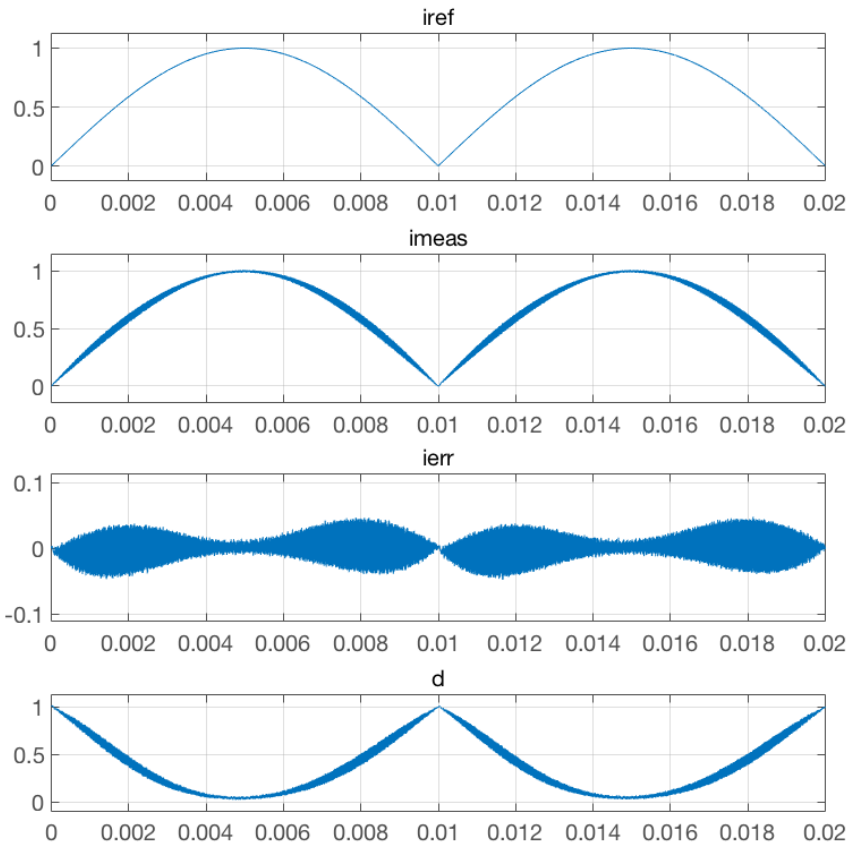


Figure 4.9: Simulation of current controller waveforms during one mains period.

signal. These results show that the inductor current following the reference almost perfectly, and the current error consists mostly of the switching-frequency ripple. Looking closely, however, there is a small 100Hz error. This is likely due to some delay in the PWM stage and the measurement filter, and could be compensated by implementing e.g. a phase-locked loop (PLL), measuring and controlling the phase of the current. [50] The PLL will, however, not be pursued further in this master's thesis, much due to the good phase response of the current loop with symmetrical optimum, and is left for further work.

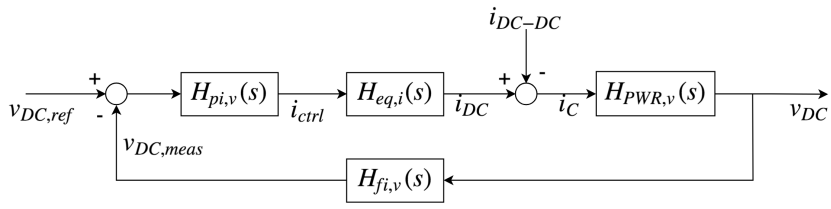


Figure 4.10: A block diagram of the voltage control loop

4.2.3 Voltage control loop

The voltage controller governs the average DC-link voltage to be held at the specified values (section 3.1). It is the outer, slower control loop; the desired average DC-voltage is set by the controller based on the grid AC voltage, and since any permanent changes in socket voltage will be small and slow for a strong grid, the control does not need to be fast.[11] Still, in the event of a sudden, larger drop in the voltage seen from the grid, e.g. due to a larger nearby load disconnecting, the slow control ensures that the DC-link voltage does not drop below its minimum value. In the opposite event, if a sudden larger voltage leap occurs on the AC-side, e.g. due to a lightning strike, this is solved by a surge diode protection, shorting the grid voltage to the DC-link capacitor when the grid voltage is higher than the DC-link voltage.[51] This reduces the voltage leap on the AC side and, if the voltage change is permanent, helps in charging the DC-link capacitor to the new, higher average voltage level.

The voltage control loop is modelled as shown in figure 4.10. As in the current loop, the PI controller can be modelled as follows:

$$H_{pi,v} = K_{p,v}\left(\frac{T_{i,v}\cdot s+1}{T_{i,v}\cdot s}\right). \tag{4.28}$$

The voltage measurement filter is there to filter out the 100Hz DC voltage ripple, which otherwise would generate harmonics in the current loop. Since the voltage loop is not required to be particularly fast, a simple low-pass filter is chosen here, as in the current loop, with the following transfer function:

$$H_{fi,v}(s) = \frac{1}{1 + T_{fi,i} \cdot s} \ . \tag{4.29}$$

Now to the equivalent current loop transfer function $H_{eq,i}(s)$. To simplify the derivation of controller parameters, it is useful to create an approximate equivalent first-order transfer function to the current controller closed-loop transfer function. Assuming that the approximation performed on the second-order voltage-source converter current loop transfer function in [52] is valid for the third order system in (4.24), the current controller can be approximated as a simple first-order delay $T_{eq,i} = 2 \cdot T_{sum,i}$. The transfer function becomes:

$$H_{eq,i}(s) = \frac{1}{1 + T_{eq,i} \cdot s} = \frac{1}{1 + 2 \cdot T_{sum,i} \cdot s} \ , \tag{4.30}$$

where $T_{sum,i}$ is as before: $T_{sum,i} = T_{PWM} + T_{fi,i}$.

At last, the voltage controller power stage is the DC-link capacitor. The DC-link voltage v_{DC} is governed by the DC-link capacitor current i_C, which is equal to $i_C = i_{DC} - i_{DC-DC}$, by $i_C(t) = C \cdot dv_{DC}/dt$. The ESR is negligible in the DC-link capacitor, thus it can be modelled as a pure capacitance. Using that, the power stage transfer function can be given as the Laplace form of the capacitor equation:

$$H_{PWR,v}(s) = \frac{v_{DC}(s)}{i_C(s)} = \frac{1}{C \cdot s} \ . \tag{4.31}$$

Looking at figure 2.1, it is evident that the only current that we can control is i_{DC}; i_{DC-DC} can be seen as a disturbance and thus be disregarded for the PI controller design later. Combining (4.28)-(4.31) with figure 4.10, the voltage controller open-loop transfer function becomes:

$$\begin{aligned} H_{ol,v}(s) &= H_{pi,v} \cdot H_{eq,i}(s) \cdot H_{PWR,v}(s) \cdot H_{fi,v}(s) \ , \\ &= \frac{K_{p,v}}{T_{i,v} C} \cdot \frac{1 + T_{i,i} \cdot s}{s^2 \cdot (1 + 2 \cdot T_{sum,i} \cdot s)(1 + T_{fi,v} \cdot s)} \ . \end{aligned} \tag{4.32}$$

As with the current controller, the two minor time constants can be merged into

one as $T_{sum,v} = 2 \cdot T_{sum,i} + T_{fi,v}$, giving new open-loop transfer function:

$$H_{ol,v}(s) = \frac{K_{p,v}}{T_{i,v}C} \cdot \frac{1 + T_{i,i} \cdot s}{s^2 \cdot (1 + T_{sum,v} \cdot s)} \ . \tag{4.33}$$

The PI parameters, $K_{p,v}$ and $T_{i,v}$, as well as the filter time constant, $T_{fi,v}$, are unknown and need to be tuned. This will be done using the Symmetrical optimum, as explained in the following:

PI tuning: Symmetrical optimum

As shown in (4.33), there is a double free integrator, which by cancelling out $(1 + T_{sum,v} \cdot s)$ by setting $T_{i,v} = T_{sum,v}$ using Modulus optimum would result in a phase of 180°, and the system would be on the limit of stability.[49] Thus, Symmetrical optimum is a better choice for the voltage control loop. The control equations become, similarly as in (4.25):

$$T_{i,v} = \beta_v \cdot T_{sum,v} \ , \quad K_{p,v} = \frac{L}{\sqrt{\beta_v} T_{sum,v}} \ , \quad \omega_{c,v} = \frac{1}{\sqrt{\beta_v} T_{sum,v}} \ , \tag{4.34}$$

In this case, the crossover frequency should be chosen at least half a decade slower than the current loop, i.e.: [40]

$$\omega_{c,v} \leq 10^{-0.5} \cdot \omega_{c,i} \ . \tag{4.35}$$

Moreover, the voltage filter can be designed using the same method as for the current measurement filter in (4.27), this time with equation:

$$\hat{I}_{ctrl,ripple}(\omega_{ripple}) = \omega_{c,v} C \cdot \frac{1}{\sqrt{1 + (\omega_{ripple} T_{fi,v})^2}} \cdot \frac{1}{2} \Delta v_C(\omega_{ripple}) \ , \tag{4.36}$$

where $\hat{I}_{ctrl,ripple}$ is the peak ripple of the output control current from the PI controller. As opposed to the current controller, the objective of the voltage measurement filter is not to enable a fast response with high crossover frequency, but rather minimizing the 100Hz $i_{ctrl,ripple}$, to minimize harmonics generated in the

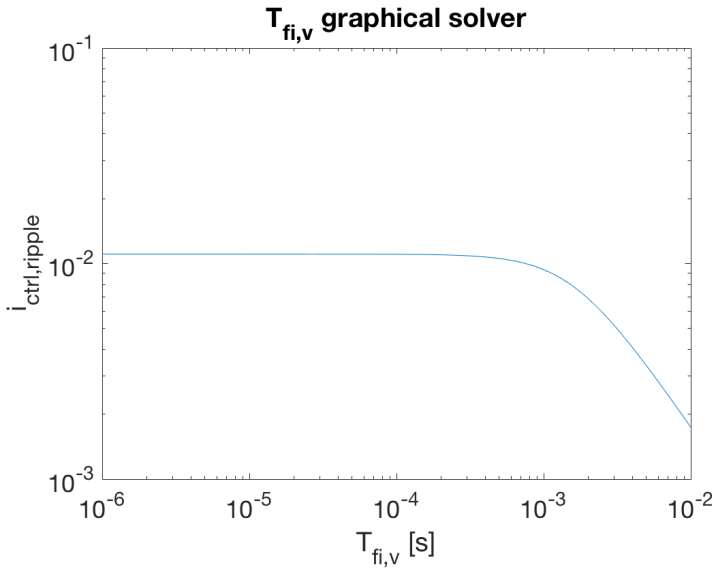


Figure 4.11: Grapical solution to (4.36), with $\omega_c = 2\pi \cdot 500$rad/s.

current controller. At the same time, choosing the crossover frequency too low will result in the controller not being able to respond to changes in reference DC voltage. Solving (4.36) graphically for various $\omega_{c,v}$ giving acceptable β_v, following the standard design rule described earlier, with control signal ripple ranging from 0.04 to 0.08, it is found through simulations that this ripple range generates some harmonics in the DC voltage and gives poorer stability performance. This generation of DC-voltage harmonics is likely due to the low frequency of the control signal, as the faster current loop is not able to dampen this ripple. It is chosen to keep $\hat{I}_{ctrl,ripple}$ at approximately 0.01. Choosing $\omega_c = 2\pi \cdot 500$rad/s, the graphical solution to (4.36) is shown in figure 4.11. The figure shows that $\hat{I}_{ctrl,ripple}$ never exceeds ~ 0.01. Thus, $T_{i,i}$ can be chosen based on (4.34) to give an acceptable β_v, which is between 1 and 25, as mentioned earlier. The filter time constant is chosen as follows:

$$T_{i,v} = 100\mu\text{s} \ ,$$

giving $\beta_v = 7.96$, which is acceptable according to the abovementioned restrictions. Inserting these values in (4.34), the controller parameters become:

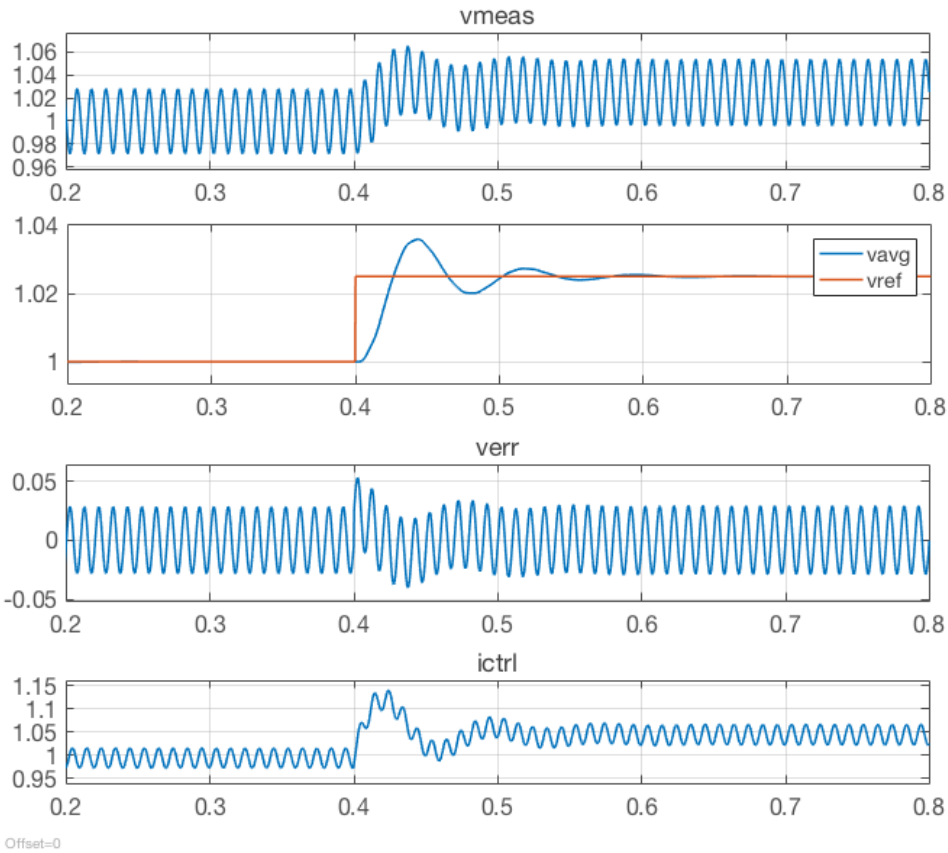


Figure 4.12: Voltage controller step response to a 10V leap in voltage reference.

$$T_{i,v} = 8.98 \cdot 10^{-4}\text{s}, \quad K_{p,v} = 0.3763, \quad \omega_{c,v} = 2\pi \cdot 500\text{rad/s} \; . \tag{4.37}$$

Simulations

A simulation of the DC voltage controller and its response to a 10V leap in reference voltage is shown in figure 4.12, where the measurements are refferred to the simulink model in figure 4.4; *vmeas* is the per unit output of the DC-link voltage measurement filter, *vavg* is the floating-100Hz-cycle average of *vmeas*, *vref* is the DC-link voltage reference, *verr* is $vref - vmeas$ and *ictrl* is the control signal to the current loop. The simulations show that the voltage is able to stabilize at the new

reference within ~ 0.2s, or roughly 20 100Hz cycles. Moreover, there is a significant overshoot in the voltage response. However, the leap in DC voltage reference might be caused by a leap in AC voltage amplitude, in which case an overshoot is better than a slower response with no overshoot, since it avoids the AC voltage amplitude being bigger than the DC voltage. This would disturb the boost operation until the AC voltage drops or the DC-link capacitor is charged through the surge diode and the necessary balance $v_{DC} > v_{AC}$ is re-achieved. A big reason for the slow response is the size of capacitance, limiting the possible dv_{DC}/dt slope, but another is probably the voltage measurement filter. A faster response could likely have been achieved using a higher-order low-pass filter or a band-stop filter, or digital filters such as e.g. a digital low pass filter. [53] All of these enable more precise filtering of the ripple frequency, while passing through more of the other frequencies, giving faster feedback in the loop. Other smart filtering techniques could also have been used, such as the voltage measurement filter applied to the simple PFC in [54], where the ripple is estimated based on current and average voltage, and then subtracted from the measured signal, leaving just the average voltage. Still, while the more advanced filter variants might give a faster and more precise response, figure 4.9 shows that stability is achieved using a low-pass filter with a good response. Supplementary DC-link voltage control from the DC-DC converter will normally also be applied, improving the stability even more. [1]

Chapter 5

System-level simulations

To verify the complete proposed converter, some simulations are performed on a system level, for maximum-power G2V and V2G operation at two AC voltage levels: 230Vrms and 120Vrms. Pictures of the complete system implemented in Simulink can be found in appendix E, except the gate drive logic and control system, who are depicted in figures 4.1 and 4.4. Components are implemented with the values computed in sections 3 and 4. There are however no GaN eHEMT models in MATLAB, so thiese are implemented as MOSFETs with no reverse recovery charge or forward voltage in the body diode, and with the same on-state resistance. The MOSFET model used, from the Simscape Power Electronics library in Simulink, does not present any possibility of including the parasitic capacitances, and so the gate charge is assumed infinitely small. Another modification is that during V2G the DC-link capacitor is exchanged for a DC voltage source. This is done to overcome that no DC-DC converter is connected at the DC-side, meaning a power source is necessary to deliver power to the grid. Due to the low ripple of the DC-link voltage at < 20Vp2p, this is approximated here as a DC voltage source equal to the average DC-link voltage. The simulations are performed with a discrete solver with constant step size $5 \cdot 10^{-8}$s.

Results of the simulations at 230Vrms G2V and V2G are shown in figures 5.1 and 5.2, respectively. Similar results are found at 120Vrms, and so these simulation results are attached in appendix G. The results at both voltage levels show that

the bidirectional totem-pole PFC is operating properly in both operation modes, with the current following the voltage in G2V and inverting in V2G, while the 100Hz DC voltage ripple and the switching-frequency current ripple within the limits defined in table 1.2. The THD of the AC current is computed in Simulink to be

$$THD_i = 0.05 \ ,$$

and the power angle, i.e. the phase angle of the fundamental AC current is computed as

$$\phi_i = 2.86^\circ \ .$$

That gives power factor: [24, ch. 3-2-4]

$$pf = \frac{1}{\sqrt{1+THD_i^2}} \cdot \cos(\phi_i) = 0.998 \ .$$

This power factor will be further improved by the implementation of a filter on the AC-side decreasing the THD of the AC current drawn from the grid. Then the OBC can comply also with the V2G THD restriction described in table 1.1.

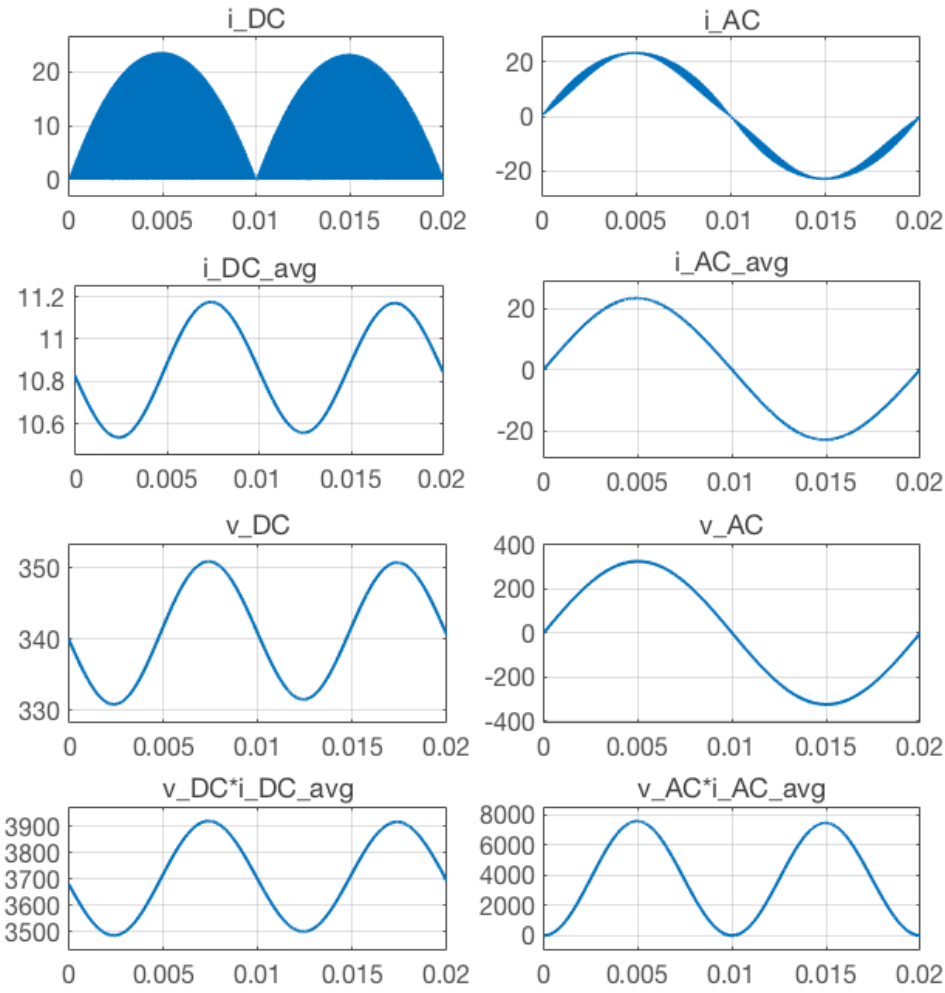


Figure 5.1: System-level simulation results at 230Vrms G2V operation.

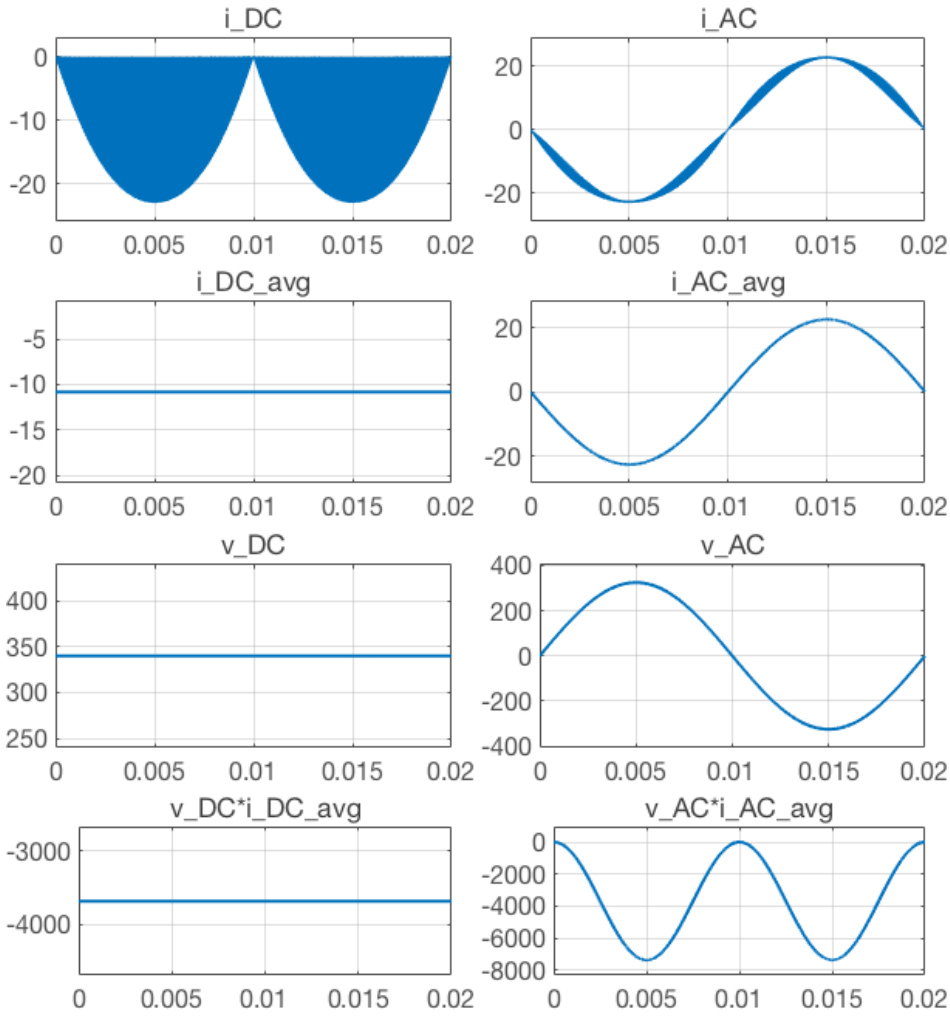


Figure 5.2: System-level simulation results at 230Vrms V2G operation.

Chapter 6

Feasibility of the bidirectional totem-pole PFC

Although the simulations showed that the proposed model is operation properly, the model is a result of some approximations and simplifications who need to be taken into account when evaluating the validity of the results and feasibility of the bidirectional totem-pole PFC. Moreover, the performance of the PFC needs to be evaluated in a bigger context, comparing it to the existing solutions on the market. In the following, the feasibility of the proposed bidirectional totem-pole PFC will be discussed, in light of the shortcomings of the simulation model and how the performance of the totem-pole PFC compares with existing unidirectional PFC solutions.

6.1 Model shortcomings

The simulation model developed and tested in the previous chapters is, as mentioned, made to derive and demonstrate the fundamental operation of a bidirectional totem-pole PFC. Thus, to limit the scope of work, some effects have been neglected which might have an effect on the performance of a potential practical implementation. For one, no parasitic inductances or capacitances, which would inevitably be present in any PCB embodiment of this bidirectional totem-pole PFC,

have been included. Though these are mostly too small to affect the fundamental waveforms of voltages and currents, e.g. parasitic stray inductances can cause overvoltages over the transistors during switching, when they experience a rapidly decreasing current, inducing a negative voltage over the inductance.[24, ch. 27-6]

Another point is that the simulations have not been made with proper GaN eHEMT simulation models, due to the lack of such a model in Simulink. In stead, they have been approximated with MOSFETs with no reverse recovery or forward voltage in the diodes, and negligible gate charge. With the infinitely small gate charges, the switching transients of the GaN eHEMTs are not included in the simulations, allowing infinitely fast switching, which is not real. If these transients were included, they would e.g. lead to some small delays in the system, which could potentially affect the stability of the control system.

Moreover, the practical implementation of the gate drives have not been discussed. GaN eHEMTs impose special requirements in the gate drives, since they require a quite large negative off-state gate voltage to avoid unwanted turn-on, as shown in table 3.3. Besides the fact the gate drive circuit imposes a delay itself, a more complex gate drive circuit might increase that delay, also possibly affecting the stability of the controllers.

Furthermore, a parasitic effect which has been proven in regular totem-pole PFCs and has been disregarded here, are current spikes that are discovered to frequently occur at the zero-crossing.[55] These are found to be caused by stored minority charges in the slow rectifier diodes, leading the diodes to be forward biased as the AC voltage switches polarity, creating a very big voltage over the inductor, again inducing a big current. Such an issue could be present in the body diodes of the rectifier-leg MOSFETs during G2V operation, when they are forward-biased.

Effects such as these and possible other problems related to parasitic effects will have to be tested in a practical prototype, in order to fully validate the bidirectional totem-pole PFC for use in a bidirectional OBC.

6.2 Loss comparison to a regular boost PFC

Setting aside the bidirectional conduction ability, which is now proven in the bidirectional totem-pole PFC, the proposed solution should be compared to a conventional boost PFC with respect to performance. If a bidirectional OBC is to be implemented, it should be able to compete with existing unidirectional PFC solutions, as the primary objective of the bidirectional OBC is still to charge the EV battery.

To evaluate the efficiency of the proposed bidirectional totem-pole PFC, it is relevant comparing the losses to a regular boost PFC. From the analysis so far it is found that the losses in the DC-link capacitor are insignificant, while rectifying the inductor current does not change the RMS and peak currents of the inductor compared to those found in section 2.3, meaning the losses should be equal. Thus, the key difference in losses exist in the semiconductor devices. First of all, the regular boost has more semiconductors in the conduction path (3) than the totem-pole (2), thus increasing the losses. Another aspect is that diodes and MOSFETs and HEMTs have different conduction loss characteristics; the conduction losses of MOSFETs and HEMTs have a dependency on $I^2_{S,RMS}$, as shown in (2.22), while the conduction losses of diodes are dependent on $I_{D,avg}$ to the power of one, assuming negligible diode resistance. The conduction losses of a diode are given as follows: [24, ch. 20-4]

$$P_{cond,diode} = V_{f,diode} \cdot I_{diode,avg} + R_{on,diode} \cdot I^2_{diode,RMS} \tag{6.1}$$

where $V_{f,diode}$ is the diode forward voltage and $R_{on,diode}$ is the diode on-state resistance. The on-state resistance of a diode is usually much smaller than the on-state resistance of a MOSFET or HEMT. As a consequence, the diode often has lower conduction losses than the MOSFET and HEMT at high power levels, while it may have bigger conduction losses at lower power levels, due to the forward voltage.

In the regular boost PFC this can be utilized by another difference between the two topologies, which becomes evident through the transistor current analysis in section 2.4. It is shown in (2.21) and (2.14) that the RMS current through the switches are dependent only on the AC RMS current. This is due to the symmetry in the totem-pole PFC, where the current has to always pass through either one

of the switches in each leg at all times, and the roles are interchanged every half cycle. This means that to minimize the transistor losses of the bidirectional totem-pole PFC it is beneficial to choose the DC-link voltage as low as possible, as is done in section 3.1.1. For a regular boost PFC, on the other hand, the roles of the transistor and the freewheeling diode do not change every half cycle, meaning the average and RMS currents through each of these are dependent on the duty cycle, which again is dependent on the DC-link voltage. It can be shown inserting $d_{boost} = 1 - \hat{V}_A C / V_{DC}$ into 2.31 that the RMS current through the boost switch in a conventional boost PFC can be expressed as

$$I_{boost} = \sqrt{I_{AC}^2 - \frac{8}{3\pi} \frac{\hat{V}_{AC}}{V_{DC}} I_{AC}^2 \cos(\phi_{AB})} \, . \tag{6.2}$$

The RMS current through the freewheeling diode, $I_{diode,RMS}$ is equal to the RMS current through the totem-leg complementary switch, described in (2.33), while the average current through the diode, $I_{diode,avg}$, is equal to the average DC-load current, which can be expressed as follows:

$$I_{diode,avg} = \frac{P_{DC}}{V_{DC}} \, . \tag{6.3}$$

The equations (2.33), (6.2) and (6.3) show that the RMS and average currents through the semiconductors in the conventional boost PFC are dependent on the DC-link voltage; the boost transistor current increases with increased DC voltage, while the freewheeling current decreases with increasing DC-voltage. Since it was established earlier that the diode performs better at high power and the transistor performs better at low power, it will be beneficial during high power power to maximize $I_{diode,avg}$ and minimize I_{boost} by setting V_{DC} at its lowest permitted level. In this application this is defined to be 340V. Oppositely, it will be optimal setting high V_{DC} during low power.

In the diode rectifier bridge, there will always be two diodes conducting, and so the losses $P_{cond,bridge}$ can be found from (6.1) with $V_{f,bridge} = 2 \cdot V_{f,diode}$, $R_{on,bridge} = 2 \cdot R_{on,diode}$, $I_{bridge,avg} = I_{AC,avg}$ (from (2.25)) and $I_{bridge,RMS} = I_{AC}$.

6.2.1 Comparison at worst-case operating temperature

Since it is assumed in the proposed design that the charger will most often be operating at maximum power, a quantitative comparison of the conduction losses in the two topologies is performed at maximum power, at worst-case temperature and with the same GaN HEMT GS66516 as before operating as boost switch in the conventional boost PFC. The operating temperature of the diode bridge is set at $T_{case,bridge} = 100°C$ to avoid thermal runaway.[56] As there exist fast-switching diodes, such as Silicon Carbide (SiC) Schottky Barrier diodes, and the DC-link voltage is equal, the switching losses are assumed to be approximately equal at approximately the same switching frequency. Assuming Diodes Incorporated GBJ2506 used for the bridge and ROHM Semiconductors SiC Schottky Barrier diode SCS220AE used for the freewheeling diode, we have $V_{f,bridge} = 1.05V$, $R_{on,bridge} \approx 0$, $V_{f,diode} = 1.50V$ and $R_{on,diode} \approx 0$. Inserting these values along with $V_{AC} = 230Vrms$, $V_{DC,avg} = 340$ and $I_{AC} = 16Arms$, the worst-case conduction losses of the conventional boost PFC is found as follows based on (2.22), (6.1),(6.2), (6.3) and (2.33):

$$P_{cond,conv,worst-case} = P_{cond,bridge} + P_{cond,diode} + P_{cond,boost} = 34.58W \tag{6.4}$$

In comparison, the total conduction loss of the proposed totem-pole PFC is equal to the conduction losses of all the transistors, calculated from the worst-case losses found in section 3.2, with GS66516 in the totem-leg and IPW60R045CPA in the rectifier-leg:

$$P_{cond,totem,worst-case} = 2 \cdot P_{cond,ST} + 2 \cdot P_{cond,SR} = 44.80W\ . \tag{6.5}$$

The results show that the totem-pole PFC imposes a substantial increase in conduction losses of 30% at the worst-case case temperature and high power, despite the decreased number of semiconductors. This is due to the different conduction loss current dependency of the MOSFETs/eHEMTs and the diodes explained above. A solution to this problem could be to exchange the rectifier-leg MOSFETs for IGBTs connected in anti-parallel with low-forward-voltage diodes. Like diodes, IGBTs are minority carrier devices, with a forward voltage the dominant cause of

conduction losses.[24, ch. 25] Thus, the conduction losses current dependency of the IGBT is going to be equal to that of the diode, meaning the totem-pole conduction losses could be reduced by introducing IGBTs anti-paralleled with diodes. That would however imply two more semiconductors in the design, which would require e.g. a larger heat sink design. One could of course also substitute the same low-resistance GaN eHEMTs used in the totem-leg, but GaN eHEMTs are more expensive than IGBTs and diodes, which are more developed technologies, and so it would likely increase the total cost of the converter.

6.2.2 Comparison at normal operating conditions

Another reason for the higher conduction losses of the totem-pole PFC at worst-case temperature is that the MOSFET and eHEMT on-state resistance has a quite big positive temperature dependency, while the the forward voltage of the diodes has a much smaller temperature dependency, as is evident in the data sheets of the chosen semiconductors of this analysis. In other words, the conduction losses of the MOSFETs and eHEMTs increase at worst-case temperature, while the conduction losses of the diodes do not change as much. In normal operation, the operating temperature will be lower than the worst-case temperature, and thus the losses in normal operation will obviously be different. The operating case temperature will typically be below 80°C, depending on the cooling technique, which would induce much smaller losses in the GaN eHEMTs and MOSFETs than at worst-case $T_{case} = 150°\text{C}$.

A new computation is performed at $T_{case} = 80°\text{C}$, with corresponding on-state resistances and forward voltages from the data sheets: $R_{DS,on,HEMT} = 37.5\text{m}\Omega$, $R_{DS,on,MOSFET} = 60\text{m}\Omega$, $V_{f,bridge} = 1.05\text{V}$ and $V_{f,diode} = 1.40\text{V}$. Substituting the new resistances into the calculations in section 3.2 and using (6.4) and (6.5) as before, the conduction losses during normal operation is computed to be:

$$P_{cond,conv,normal} = 33.16\text{W}, \quad P_{cond,totem,normal} = 24.96\text{W} .$$

These calculations show that during normal operation with $T_{case} = 80°\text{C}$, the bidirectional totem-pole PFC decreases the conduction losses by 25% compared to a conventional boost PFC. Moreover, the conduction losses of the totem-pole should

decrease more for lower load, due to the I^2 dependency, than the conventional PFC. Thus, although the switching losses are not taken into account and the loss computations might not be completely precise due to inaccuracies in the data sheets, these computations indicate that the proposed bidirectional totem-pole imposes an improvement in efficiency compared to conventional boost PFC at 230Vrms and normal operation.

6.2.3 Comparison at 120Vrms

Having established that the totem-pole PFC is efficient at 230Vrms, a similar comparison must be made at 120Vrms to evaluate over its full voltage range. In fact, as mentioned in section 3.2, a significant disadvantage of the totem-pole PFC emerges at lower voltage levels; while the power decreases to almost half when the AC voltage is changed from 230Vrms to 120Vrms, the switching losses and conduction losses of the bidirectional totem-pole PFC are unaffected by the AC voltage - only the AC current and DC voltage. This means the relative losses are almost doubled at 120Vrms, causing a big decrease in efficiency. Looking at (6.2) and (6.3) it is evident that the conduction losses of the conventional PFC are indeed dependent on the AC voltage and power. As it turns out, when the AC voltage - and power - decreases, the current through the boost switch of the conventional PFC increases while the current through the freewheling diode decreases. Based on the previous analysis of the current dependency of the conduction losses of diodes and MOSFET and HEMTs, this should mean an increase in conduction losses in the conventional PFC at 120Vrms, implying even worse efficiency.

The conduction losses of the conventional PFC at 120Vrms and worst-case operating conditions can be calculated as follows, using the same procedure as in the previous analyses:

$$P_{cond,conv,120V} = 39.82\text{W} ,$$

which, as expected, is an increase of 15% compared to the worst-case analysis at 230Vrms. Assuming all the other losses computed in chapter 3 to remain unchanged, and keeping in mind that these were designed to give more or less exactly 98% efficiency at 230Vrms and 3500kW, it is obvious that the efficiencies of both

the conventional boost PFC and the bidirectional totem-pole PFC at 120Vrms and 1.9kW will be less than 98%.

Since the PFC should be able to operate with 98% efficiency at both 120Vrms and 230Vrms, and the efficiency of this bidirectional totem-pole PFC is closer to 96% at 120Vrms normal conditions, some modifications should be made to increase the efficiency at low voltage. An example of such a modification could be connecting extra totem-leg GaN eHEMTs or rectifier-leg MOSFETs in parallel; a halving of the current through each of these transistors implies a 4-times decrease in conduction losses in each transistor, by (2.22), thus halving the conduction losses. MOSFETs and GaN HEMTs can safely be connected in parallel because of the positive temperature coefficient of the on-state resistances ensuring an even loss distribution between the paralleled transistors. There are however some challenges when connecting transistors in parallel, such as e.g. equalling the impedance of the gate circuits of both of the paralleled transistors to ensure simultaneous switching. On the other hand, it has been shown in [29] that interleaving the totem legs can give positive effects with regards to current ripple, cancelling out harmonics, meaning there are more positive effects to connecting in parallel as well. In any case, paralleling the transistors would indeed give a more complex system, making it desireable to avoid if possible. Thus another solution to this problem could be to decrease and redistribute the estimated losses in table 3.2, to e.g. have approximately the same totem-leg losses, while restricting especially the inductor and rectifier leg allowed losses. The inductor conduction losses could be decreased by increasing the core size, and the rectifier legs have no switching losses and could thus be made with smaller losses than the totem-leg. However, the first would decrease the power density, whereas the second would likely require more expensive transistors.

Chapter 7

Conclusion and Further Work

7.1 Conclusion

A fundamental simulation model of a bidirectional totem-pole PFC for bidirectional OBC purposes has been built and implemented in Simulink using off-the-shelf components while complying with the demands put forward by Valeo Siemens. General equations have been developed for the description of currents, voltages and losses in the components throughout the topology, aiding in the dimensioning of these components. Importantly, it was discovered that the transistor conduction losses in the bidirectional totem-pole are only dependent on the AC current, because of the symmetry of the topology forcing the conduction losses to be equally distributed across both transistors in each leg. The components implemented were a $246\mu H$ powder-core, toroid-shaped boost inductor with copper wires, 5 paralleled $360\mu F$ electrolytic DC-link capacitors, GaN eHEMT GS66516 for high-frequency transistors and CoolMOS IPW60R045CPA for slow-switching rectifier-leg transistors. Combined, they were computed to give an efficiency of more than 98% at a switching frequency of 90kHz.

Moreover, equations for gate logic and control system with cascaded current and voltage control have been developed and implemented in Simulink, and verified through simulations. The current and voltage controllers were implemented with PI controllers and Symmetrical optimum, giving crossover frequencies of 28kHz

and 500Hz, respectively, with good response. The simulations showed that the charger was able to operate at 120Vrms and 230Vrms max power with a power factor of 0.998 and a THD of 5% without any DM filter applied on the AC side. This was not complying with the AC current THD limitations at 3% in V2G, and thus a DM filter will have to be applied in order to meet these demands.

At last the performance of the proposed bidirectional totem-pole was compared to a conventional boost PFC at worst-case and normal operating modes at 230Vrms, and at 120Vrms. This analysis showed that the bidirectional totem-pole PFC produced higher conduction losses than the conventional boost PFC at worst-case operating conditions with case temperature 150°C. This was concluded to be because the conduction losses of the eHEMTs and MOSFETs being dependent on the current squared while for the freewheeling diode of the conventional boost they are dependent on the current to the power of one, combined with the fact that the conduction losses of the conventional PFC can be regulated by adjusting the DC-link voltage to direct more of the current through the diode and less through the boost MOSFET. However, it was shown that during normal operation, the strong temperature dependency of the MOSFET and GaN HEMT on-state resistances decreased the conduction losses to make the bidirectional totem-pole PFC more efficient than the conventional boost PFC. Still, it was shown at 120Vrms that the conduction loss - and switching loss - independence from AC voltage of the bidirectional totem-pole PFC causes the efficiency to decrease significantly at lower voltages, approaching 96% at 120Vrms. This effect is however found to be even worse in conventional PFCs.

All in all, the bidirectional totem-pole seems a promising topology for use as a bidirectional PFC, being feasible with existing off-the-shelf components, and showing good control performance in both G2V and V2G operation. It was argued in the introduction that the charger would most often be operating at max power in both G2V and V2G, and at 230Vrms max power the performing at a good efficiency $\eta > 98\%$. Moreover, at 230Vrms lower power, the totem-pole is expected to show even better performance, due to the mentioned I^2-dependency of the conduction losses in the transistors. However, at 120Vrms, the efficiency was found to not meet the demands, and so modifications would need to be made, such as connecting the high-frequency legs in parallel, in order to achieve a satisfactory efficiency at lower AC voltages. Also, importantly, the results of this simulation

model are not sufficient to verify completely the bidirectional totem-pole, as some parasitic effects and transients are ignored. A real-life prototype will have to be made to investigate the performance further.

7.2 Further Work

Picking up on that loose thread, the first suggestion for further work is to build a prototype of this bidirectional totem-pole PFC for OBC purposes, with the relevant components and with proper gate drive circuits. This way, the real-life performance of the 3.5kW bidirectional can be investigated, studying the effect of the transient behaviour of the GaN HEMTs and the gate drive circuits on the control system and the rest of the performance. It would also allow for investigation of the effect of PCB parasitics on e.g. overvoltages across the transistors during switching; at this high frequency of 90kHz it is desirable to avoid snubber circuits at the transistors, since they impose a delay in the switching, and for that reason it would be valuable to investigate any overvoltages or too high di/dt and dv/dt during switching, to evaluate the feasibility of the topology. Another transient effect of importance, is the previously mentioned current spike that is shown to occur at zero crossing is with unidirectional PFCs, due to rectifier diodes minority charges.[55] It could be interesting to see if the same effect is present with the body diodes of the rectifier-leg MOSFETs during G2V, or if implementing a bidirectional totem-pole removes this problem.

Withal, a suggestion for further work is investigating further the paralleling of GaN HEMTs in the fast-switching totem-leg, to increase the efficiency of the totem-pole at lower voltages. As mentioned this imposes stringent requirements to the gate drivers with regards to equality of gate impedance, and other issues will be present too. Also, interleaving of the totem-pole fast-switching leg with CrCM and TCM has been investigated in several papers in the literature,[29, 27] but few have investigated this interleaving in CCM.

At last, an obvious suggestion for further work is the study of a bidirectional DC-DC converter, to complete the bidirectional OBC. This will in fact be done in a master's thesis at NTNU next spring, also in cooperation with Valeo Siemens.

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Appendices

Appendix A

Valeo Siemens bidirectional OBC specifications

Valeo SIEMENS eAutomotive		NTNU master project				Doc. Ref.:	
						Doc. Rev.:	01
		Bidirectional charger				Release Date:	-
						Doc. Classif.:	**Not restricted**
		Customer:	P3	Product Line:	OBC	Project Type:	
Division:	*Hardware*	Platform:	-	Product:	-	Project Manager:	
Dev./Prod Site(s):	Drammen	Project Code:	-	Product Ref.:	-	Activity Leader:	T. Sorsdahl

Schematic and layout review and justification.

SKILL	PROJECT NAME	PLM
Hardware	Bidirectional charger	

ABSTRACT / CONCLUSION

ABSTRACT:

General specification && guidelines for design of a bidirectional on board charger for electrical and hybrid vehicles intended as a starting point / reference for a master project at NTNU.

The bidirectional charger should be designed for J1772/IEC 61851 which describes the charging standard for electrical vehicles up to level two charging with single phase current up to 32Arms/7680VA. Relevant and extended requirements are specified in this document.

There is no known standardization for bidirectional chargers at the time of creation of this document.

CIRCULATION LIST (**E** : **E-mail**, **P** : **P**aper)

Can be released ☐ Communicable with non disclosure commitment ☒ Available on site only ☐ Confidential - unavailable ☐

C	Name	Service or Company	C	Name	Service or Company	C
E			E			E

S YES ☐ NO ☑
R YES ☐ NO ☑

Template Ref: V01 TPL 07 00645
Template Rev: 01

	Written by	Reviewed by	Checked by	Approved by
Function	**Hardware Engineer**	**Referent Engineer**	**HDL**	**Department Manager**
Name	Torbjørn Sørsdahl			
Date				
Visa				

See Signature Workflow Instruction

SUMMARY

REVISION HISTORY

Revision #	Date	Modif #	Author	Modified paragraphs and kind of modification
1	13.12.2017	1	T.Sorsdahl	Initial revision

1 Global requirements

Rough expectations for performance required for bidirectional on board chargers from standards and other input.

1.1 General requirements

Id	Req Description	Range
1.1	Galvanic isolation between input and output (transformer)	4kVac
1.2	Encapsulation	IP67
1.3	Cooling system by liquid with coolant temperature	-40 ~ 85ºC
1.4	Ambient air temperature range	-40 ~ 85ºC
1.5	The charger shall meet the following lifetime (service life):	15 years 300 000 km ~ 20.000 hours total V2G && G2V

1.2 Specification G2V

Id	Req Description	Range
2.1	AC-DC Output voltage range	200 ~ 1000Vdc
2.2.	AC-DC Max output current(continuous)	12Adc
2.3	AC-DC Output current ripple	5%
2.4	AC-DC Maximum output power	3500W
2.5	AC-DC Input voltage range	85 ~ 264$V_{AC,rms}$
2.6	AC-DC Input frequency	45 ~ 65Hz
2.7	AC-DC Maximum input current	16A Max.
2.8	AC-DC Efficiency	> 94%.
2.9	AC-DC Max apparent power	3680VA
2.10	AC-DC Lifetime	10.000 hours (Eq 300.000 km)
2.11	Maximum AC leakage current	1.5mA

1.3 Specification V2G

Id	Req Description	Range
3.1	DC-AC Output voltage range	85-264Vac
3.2	DC-AC Input voltage range	200VDC~1000VDC
3.3	DC-AC Max power output	3.5kW
3.4	DC-AC Max input current	12Adc Max.
3.5	DC-AC Max output current(rms)	16A Max.
3.6	DC-AC output frequency range	45~65Hz
3.7	DC-AC efficiency	> 94%.
3.8	DC-AC THD	THD<3%
3.9	DC-AC Lifetime	10.000 hours (high uncertainty of required lifetime)
3.10	Maximum AC leakage current	1.5mA

1.4 EMC requirements

Electric vehicle minimum emc requirements for EU : R010r6e (available for free) done at Vehicle level. This specifies all emc requirements which in the end the charger also need to be according to however component level requirements are usually stricter.

<table>
<tr><th>Id</th><th>Req Description</th><th>Standard</th></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>4.1[3]</td><td>Maximum harmonics 50Hz – 2kHz

R010r6e :
Maximum allowed harmonics (input current ≤ 16 A per phase)
<table>
<tr><th>Harmonic number
n</th><th>Maximum authorized harmonic current
A</th></tr>
<tr><td colspan="2">Odd harmonics</td></tr>
<tr><td>3</td><td>2.3</td></tr>
<tr><td>5</td><td>1.14</td></tr>
<tr><td>7</td><td>0.77</td></tr>
<tr><td>9</td><td>0.40</td></tr>
<tr><td>11</td><td>0.33</td></tr>
<tr><td>13</td><td>0.21</td></tr>
<tr><td>15 ≤ n ≤ 39</td><td>0.15x15/n</td></tr>
<tr><td colspan="2">Even harmonics</td></tr>
<tr><td>2</td><td>1.08</td></tr>
<tr><td>4</td><td>0.43</td></tr>
<tr><td>6</td><td>0.30</td></tr>
<tr><td>8 ≤ n ≤ 40</td><td>0.23x8/n</td></tr>
</table></td><td>IEC 61000-3-2</td></tr>
<tr><td>4.2[2]</td><td>Supply voltage dips
Minimum requirement: Voltage reduction of 30 % of nominal voltage for 10 ms.
Minimum requirement: Voltage reduction of 50 % of nominal voltage for 100 ms.
Minimum requirement: voltage reduction >95 % of nominal voltage for 5 s.
No loss of charging state allowed reduced power acceptable</td><td>IEC 61000-4-11</td></tr>
<tr><td>4.3[2]</td><td>1,2/50 µs surges
6kV in common mode,
3 kV in differential mode</td><td>IEC 61000-4-5</td></tr>
<tr><td>4.4[2]</td><td>Conducted emission toward ac grid 150kHz-30MHz
<table>
<tr><th rowspan="2">Frequency of Emission (MHz)</th><th colspan="2">R010r6e (-6dB)</th></tr>
<tr><th>Quasi-peak dBuV</th><th>Average dBuV</th></tr>
<tr><td>0.15 – 0.50</td><td>60 to 50</td><td>50 to 40</td></tr>
<tr><td>0.50 – 5.00</td><td>50</td><td>40</td></tr>
<tr><td>5.00 – 30.0</td><td>54</td><td>44</td></tr>
</table></td><td>IEC 61000-4-6</td></tr>
<tr><td>4.5[1]</td><td>Radiated emission 30MHz-6GHz</td><td>R010r6e</td></tr>
<tr><td>4.6</td><td>Conducted emission toward battery 150kHz-30MHz
<table>
<tr><th>Frequency (MHz)</th><th>Limits and detector</th></tr>
<tr><td>0.15 to 0.5</td><td>79 dBµV (quasi-peak)
66 dBµV (average)</td></tr>
<tr><td>0.5 to 30</td><td>73 dBµV (quasi-peak)
60 dBµV (average)</td></tr>
</table></td><td>R010r6e</td></tr>
</table>

1: Outside any scope for a student task
2: For minor reference regarding switching frequency
3: Why a pfc is required.

2 Internal obc requirements

Describes recommendations to be able to the global on board charger requirements.

2.1 PFC stage or similar toward ac grid

Id	Req Description	Value	Reason
	PFC startup time to Full operation V2G	<1s	• Grid stabilization is usually in the range of seconds • It is assumed the dc/dc is running in idle mode while awaiting feedback from the grid to only need to start the PFC and not charge the dc link in addition which is time consuming.
	PFC efficiency	>97.6%	• Total effiency required 94% estimate loss split : o 40% PFC Min effiency PFC : 97.6% o 40% DC/DC Min effiency dc/dc : 97.6% o 20% Other losses Min effiency required : 98.8% o Sum 94% efficiency. • Hard to meet at 85Vrms due to the losses in the PFC can only be 37% of the value at 230V usually requring much higher rated component at a higher cost.
	PFC choke current ripple	< 20%	• Core losses for most relevant magnetic materials increases by the square of the flux density ripple so 100% ripple increases core losses by 25x compared to 20%. • This limits the maximum current ripple which has to flow in filter capacitors reducing the requirement for current capability.
	Switching frequency	100kHz < Fsw < 140kHz 450KHz< Fsw < inf	• Ac grid legal limits starts at 150kHz and if you are bellow the 2nd harmonic is above legal limits at ~ 300kHz so the filtering must be designed for 300kHz while if you are at 150kHz the filter must be designed for 150kHz leading to a much larger filter.
	Max dc link voltage ripple	< 20V	• Avoids unnecessary component stress • Maintains stable input voltage to the dc/dc
	Dc link voltage	< 340V	• Provides high voltage to the dc/dc stage while staying bellow nominal grid voltages.
	Lowest PFC power in V2G	>146 Va	• Legal standards put 8.8uF as maximum x capacitance between lines for differential mode filtering. o Energy consumption in 8.8uF = 146Va at 230V

2.2 Dc/dc or similar toward battery

Id	Req Description	Value	Reason
	Dc/dc startup time	<1s	• Grid stabilization is usually in the range of seconds
	Dc/dc efficiency	>97.6%	• Total effiency required 94% estimate loss split : ○ 40% PFC Min effiency PFC : 97.6% ○ 40% DC/DC Min effiency dc/dc : 97.6% ○ 20% Other losses Min effiency required : 98.8% ○ Sum 94% efficiency. • Low efficiency also lead to high losses complicating the cooling system required.
	Switching frequency	100kHz < Fsw < 140kHz 450KHz< Fsw < inf	• Ac grid legal limits starts at 150kHz and if you are bellow the 2nd harmonic is above legal limits at ~ 300kHz so the filtering must be designed for 300kHz while if you are at 150kHz the filter must be designed for 150kHz leading to a much larger filter.
	Topology	Three phase	• Three phase dc/dc leads to energy being transferred at 3rd harmonic reducing magnetic component sizes and filtering required.

3 Tips / fast calculations as input

- Power factor correction required for all power levels above 80W
- EMC : Conducted emission fast calculation :
  - Assume 400Vpp at the PFC output
    - 20log(400*10^6) = 172dBuV
    - Legal requirement at 150kHz 50dbuV
    - If first harmonic is placed at 150kHz filtering required :
      - 172dBuV-50dBuV = 122dBuV
      - 122dBuV = 10^(122/20) = 1.25M
      - Noise levels need to be reduced 1.25M times between the output of the pfc to the grid.
-

Appendix B

Literature review on power factor correction converters

A literature review has been performed on bidirectional and unidirectional PFCs, for use in OBCs. The following content, i.e. the whole chapter, is an excerpt from the specialization project performed in the fall semester. [4]

B.1 Power factor correction AC-DC converter

There are regulations and standards, such as the IEC 61000-3-2 or IEC 61000-6-3 directives, limiting the permitted current harmonics emissions to the grid from power supplies and other electric equipment. In OBCs and most other power supplies, this harmonic emission is dealt with by the combination of an AC-side filter, typically a passive LC filter, and a PFC AC-DC converter. The PFC controls the drawn AC current to be sinusoidal and in phase with the AC mains voltage, removing the low-frequency harmonics and maximizing the power factor, while the filter suppresses the high-frequency harmonics from the PFC converter.

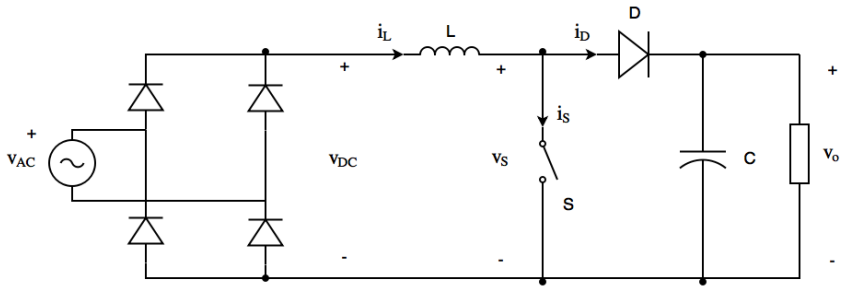
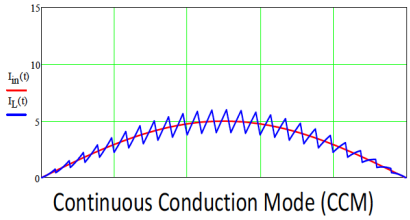


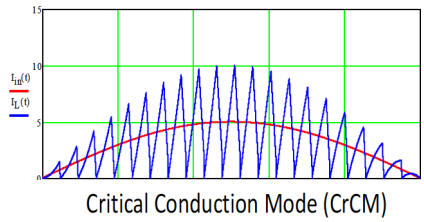
Figure B.1: The topology of a conventional boost PFC converter

B.1.1 Conventional PFC

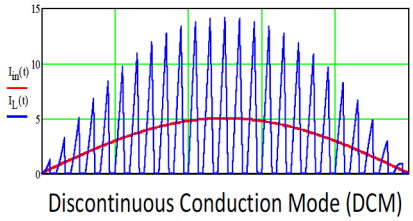
To understand the operation of a bidirectional PFC, the operation of a unidirectional PFC needs to be understood as well. Figure B.1 shows a conventional PFC converter, similar to that used in the depicted Valeo Siemens OBC topology from figure 1.1, with a passive rectifier bridge cascaded with a boost converter. The boost converter sees the rectified positive half wave of the AC voltage, and the transistor switching is pulse-width modulated to shape the fundamental component of inductor current sinusoidally in phase with this voltage. The PFC could be operated in either continuous conduction mode (CCM), critical conduction mode (CrCM) or discontinuous conduction mode (DCM), as shown in figures B.2a, B.2b and B.2c, respectively. Since CrCM is on the boundary of CCM and DCM, with current shaped like in CCM and becoming zero momentarily once every switching period, it can be said to be a special case of them both. DCM has no apparent operational advantages over CrCM, and would cause both more harmonics and a bigger current ripple for the same average current value due to the period of discontinuity [24, Chapter 7]. For that reason DCM is rarely used [2]. CCM has the advantage that it has a smaller current ripple, and thus also a smaller peak current, requiring less current capability in the MOSFETs and a smaller filter on the AC side. At the same time, there is hard switching both at turn-on and turn-off, increasing the switching losses. CrCM, on the other hand, achieves zero voltage switching (ZVS) at turn-on, giving no switching loss when the switches are turned on, but the peak-to-peak ripple is twice the average current. The ripple in CrCM implies a bigger current stress on the MOSFET, and it requires a bigger AC filter to suppress the harmonics.



(a) Continuous conduction mode



(b) Critical conduction mode



(c) Discontinuous conduction mode

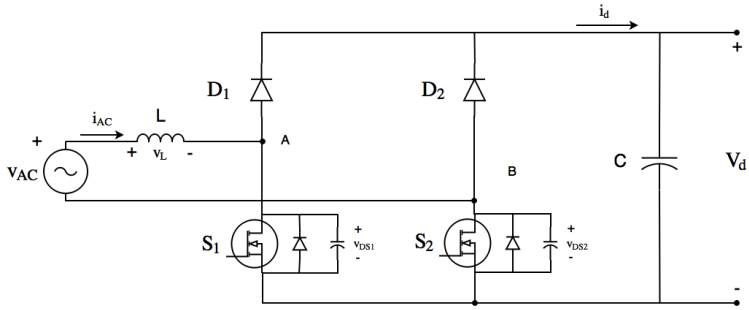
Figure B.2: The current waveforms of a boost PFC, as found in [2].

A buck converter could also have been used in stead of a boost, but that would have required a big capacitor on the output of the rectifier to ensure that the voltage is always higher than the DC-link voltage, since the buck converter needs to have a negative voltage gain in order to function [24, Chapter 7-3]. Therefore, boost PFC is a better option during charging, controlling the DC-link voltage to be higher than the maximum peak AC voltage (including ripple), so that the charger can operate at rated voltage during the whole input voltage range from 0 to peak.

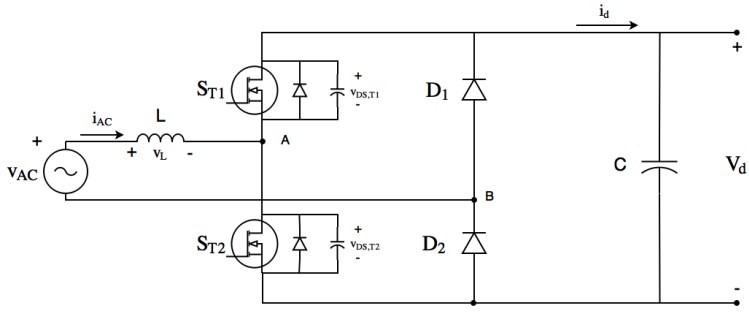
B.1.2 Bidirectional PFC

When the boost PFC is to be made bidirectional, it is obvious that both the rectifier bridge and the freewheeling diode of the boost converter needs to be replaced. The freewheeling diode can be removed by integrating the PFC switching into the rectifier bridge, as is done in several bridgeless PFC topologies in [25] and [57]. The forward voltage drop of the diodes cause conduction losses [24, Chapter 2-2], so minimizing the number of diodes in the conduction path by removing the freewheeling decreases these losses. Out of these bridgeless topologies, the basic bridgeless PFC and the totem-pole PFC are standing out with regards to simplicity and low number of semiconductors. These are depicted in figures B.3a and B.3b. For both of these topologies, the transistors are controlled such that for positive AC-voltage half cycle one transistor is in boost PWM switching mode, while the other transistor is behaving as a rectifier diode, and oppositely in the negative half cycle.

The totem-pole PFC was previously somewhat disregarded for the benefit of the basic bridgeless PFC and other bridgeless PFC topologies [25]. This because the reverse recovery body diode of the MOSFET made CCM (see figure B.2) infeasible in this topology, due to the reverse recovery current causing considerable switching losses in CCM [24, Chapters 19 - 22]. Running it in DCM would require very high current ratings for higher-power applications, such as an OBC. The basic bridgeless PFC, on the other hand, does not have these issues, and has been proven in e.g. [58] to be efficient at power levels up to 3.5 kW. On the negative side, the basic bridgeless PFC produces significant amounts of common mode noise, because the zero-potential of the DC-link side is floating compared to AC ground during negative AC mains half cycle [25, 3]. In more recent scientific works, the



(a) Basic bridgeless PFC



(b) Totem-pole PFC

Figure B.3: Bridgeless PFC topologies

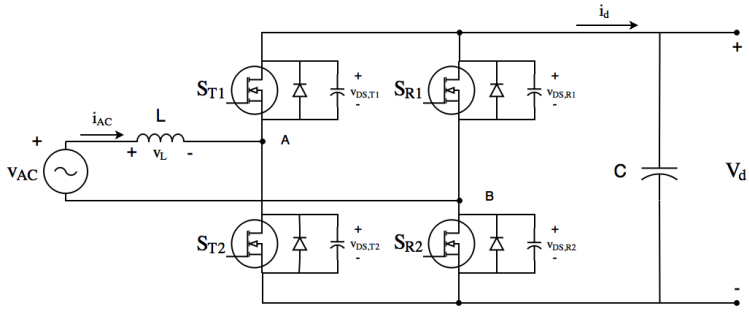
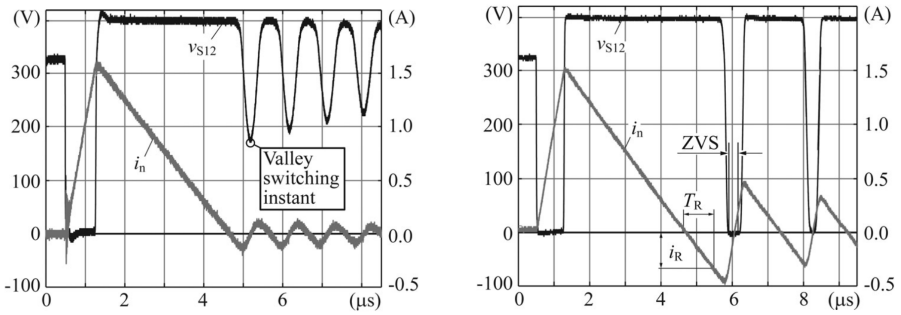


Figure B.4: The basic bidirectional PFC topology

totem-pole has been given renewed attention; there has been proposed some modulation schemes where by replacing the diodes with low-frequency MOSFETs and allowing negative current before turn-on, operating at the boundary of CCM and DCM, ZVS can be achieved through large parts of the input voltage range. This because the brief negative current helps discharge the drain-source capacitance of the blocking high-frequency MOSFET, lowering the drain-source voltage before turn-on [24, Chapter 22]. The resulting topology is the basic bidirectional H-bridge AC-DC converter, as shown in figure B.4, with one high-frequency switching leg, the totem-leg, and one rectifier leg operating at synchronous frequency. This topology obviously allows for bidirectional power flow.

One of the proposed modulation schemes is called valley filling, or valley switching [28]. The current and voltage dynamics in the MOSFETs at switching is shown in figure B.5a. In this technique the resonance between the parasitic capacitances of the high-frequency MOSFETs and the boost inductor is exploited by delaying the MOSFET turn-on until the drain-source voltage of the blocking MOSFET resonates down to a ”valley” or to zero, significantly reducing the turn-on switching losses. It is found i [28] that ZVS is achieved while $|v_{AC}| < V_{DC}/2$. The other modulation scheme is named triangular current mode (TCM) [3, 29, 27]. The switching dynamics are shown in figure B.5b. Here, instead of utilizing the resonance after MOSFET turn-off, the conducting MOSFET is kept on while the current becomes negative. The hitherto conducting switch is turned off and the complementary switch turned on when the drain-source voltage of the blocking MOSFET becomes zero, achieving ZVS throughout the mains voltage period. Withal, this technique does also require complex control due to the non-linearity of the MOSFET output capacitances making the switching timing difficult; the average current needs to be computed over every switching cycle [3]. Additionally, with the average current being dependent on the grid voltage and the drawn power, including negative current in every switching cycle gives a higher peak current ripple, sharpening the demands to MOSFET current ratings and requiring bigger AC filter current capability.

In the totem-pole topology, the high-frequency totem-legs can easily be interleaved, by operating several legs in parallel, with switching schemes phase-shifted between each leg, as has been done in [3] and [27]. This is a big advantage, as for the same charging power one could significantly reduce the current stress on each



(a) Valley switching **(b)** Triangular current mode (TCM)

Figure B.5: MOSFET switching dynamics with extended reverse conduction time, as found in [3].

of the totem-leg switches. The peak current stress was, as mentioned, previously the limiting factor for the totem-pole PFC, so interleaving has been a big factor for bringing the totem-pole PFC back in the discussion. In [3] there are three interleaved legs, which has benefits also regarding cancellation of first and second harmonics in the inductor current, while in [27] there are two interleaved legs. Using three interleaved legs, one could actually double the input power while at the same time reducing the stress on each of the totem-leg switches. The drawback of the interleaving strategy is however that the control becomes more complex [3], and obviously it would also require larger drive circuits. Interleaving is also possible with the basic bridgeless PFC, but it would require a more complex topology with more semiconductor components, as in [59].

Furthermore, recent research in wide-bandgap power semiconductor devices have shown that gallium nitride (GaN) high-electron-mobility transistors (HEMTs) can significantly improve the performance of the bidirectional totem-pole PFC, replacing the high-frequency MOSFETs [35, 60]. The GaN HEMT has a very low on-state resistance while at the same time providing a higher breakdown voltage than regular silicon MOSFETs [38, 61]. Additionally, as opposed to the MOSFET, the HEMT has no reverse body diode, and it has lower gate charge and smaller and less non-linear output capacitances than the MOSFET [62]. Also the various normally-off GaN arrangements, such as the cascode HEMT and E-mode HEMTs, have very low turn-off losses, making them ideal for boundary CCM/DCM operation with ZVS turn-on, giving virtually no switching losses and efficiencies up

to 99% at 1MHz [27, 60]. Moreover, the lack of reverse body diode, lower gate charge and smaller output capacitances reduce switching losses to such extent that a CCM-operated totem-pole becomes feasible. This is evident in [30], where a 65kHz 1.5kW CCM-operated bidirectional totem-pole PFC is proven to achieve an efficiency of 99%. The normally-off GaN HEMTs are however still a technology in development, and few commercially available solutions exist as of now, especially at the power level of an OBC (3.5kW), but the technology in this field is rapidly evolving.

Appendix C

Paper on GaN HEMTs and bidirectional PFCs

GaN HEMTs and Bidirectional Power Factor Correctors - A Review Paper

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***Abstract*—Gallium Nitride power devices is widely considered as an appealing technology within power supplies. At the same time, bidirectional power supplies is finding a growing interest, especially within distributed renewable energy and battery energy storages, presenting a need for bidirectional power factor correctors (PFCs). This paper discusses and evaluates the state-of-the-art within GaN power transistors and bidirectional PFCs, and the joint potential and present use of these technologies. Totem-pole PFCs is found to be the leading bidirectional topology in the present, and shows goods attributes together with cascode GaN HEMTs. Other promising technologies are the already commercialized gate-injection-transistors. GaN transistors are found to have a big potential for both increasing PFC efficiency and decreasing size due with high frequency.**

***Keywords*—GaN, Bidirectional PFC, GaN E-HEMT, GIT, DAB, dual active bridge**

I. Introduction

These days there is an increasing focus on distributed battery energy storage connected to e.g. intermittent renewable energy production. By its nature, such solutions will have bidirectional power flow, so a necessary effect is a growing need for bidirectional active power factor correctors (PFCs). PFCs are an important part of any electronic power supply; a PFC drastically improves the power quality of the AC power drawn by the electronic load by controlling the shape of the drawn AC current waveform. First of all it is keeping the input AC current in phase with the input AC voltage to improve the power factor and secondly it is controlling the harmonics of the drawn current by shaping it sinusoidally. High-frequency harmonics lead to unnecessary loss, heat up the components and may cause harm on electronic equipment [1]. For that reason, there are regulations limiting the permitted emission of harmonics from grid-connected power supplies and standards, such as the european IEC/EN 61000-3-2 directive, which have to be obeyed by the combination of PFCs and harmonic filters.

A. PFC converters

Traditional, conventional boost PFCs consist of a rectifier bridge and a dc-dc boost converter, as shown in figure 1[2]. When using a boost converter the DC side is able to operate at its rated voltage over the whole mains voltage period without having a big DC link cap on the output of the rectifier bridge. The passive rectifier bridge rectifies the voltage to the waveform of the absolute value of a sine, and the current is ruled

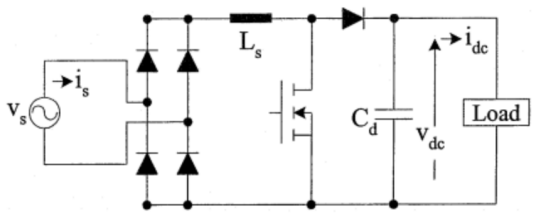
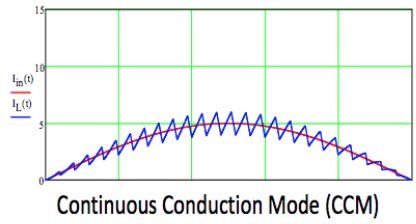
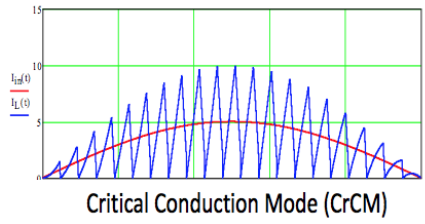


Fig. 1: Conventional boost PFC, as found in [2].



(a) Continuous conduction mode



(b) Critical conduction mode

Fig. 2: The current waveforms of a boost PFC, as found in [3].

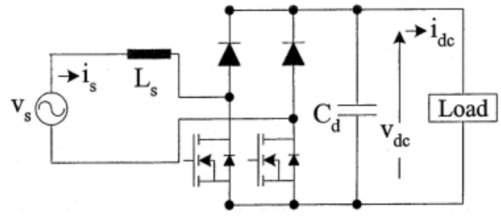
by the voltage over the inductor according to $L\ di_L/dt = v_L$. The current waveform is then shaped like a sine (figure 2) by controlling the duty cycle of the MOSFET, keeping it in phase with the voltage. The converter can either be ran in continuous conuction mode (CCM) (figure 2a) or critical conduction mode (CrCM) (figure 2b); the first gives smaller current ripple but harder switching in the MOSFET, the latter gives soft turn-on of the MOSFET, but a bigger current ripple. The boost converter is rarely operated in discontinuous conduction mode (DCM), as DCM has no apparent operational advantages over CrCM and produces more harmonics due to the discontinuous current [4, Chapter 7]. With the average AC mains current shaped like a sine, the harmonics are limited to the switching-frequency ripple, which can be compensated by a passive filter on the AC side.

The basic boost PFC converter does its duty, but has some drawbacks. Most notable is the number of semiconductor devices in the conduction path from grid to load; during charging of inductor there are two diodes and a MOSFET, while during discharge of the inductor there are three diodes. This means a lot of conduction and switching losses, and so there has been developed bridgeless PFCs, such as those presented in [2], [5] and [6], to minimize the number of semiconductor devices in the conduction path. The most simple are the basic bridgeless PFC and the totem-pole PFC, shown in figures 3a and 3b. These converters are operated such that for the positive half of the AC mains voltage period one of the MOSFETs is conducting, either through the body diode or through the MOSFET itself if it is turned on, while the other is doing the PFC switching. During the negative half period the roles are swapped. The diodes still aid with rectification. This way the number of semiconductor devices in the conduction path is reduced from three to two, reducing the losses[5].

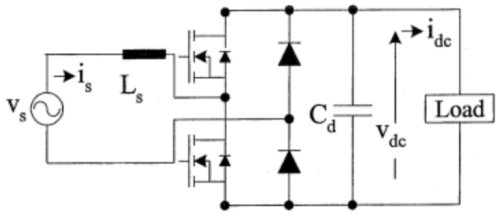
From bridgeless PFCs the way is short to bidirectional PFCs. Looking at figures 3a and 3b it is easy to see that by replacing the diodes with MOSFETs, the converter enables bidirectional power flow. This substitution even improves the efficiency of the converter, as is shown in [7], [8] and [9]. These are totem-pole PFCs where the diodes have been replaced by slow-switching MOSFETs to remove the forward voltage loss of the diodes and thus reduce the losses.

B. GaN HEMTs

To this date Si superjunction MOSFETs have been the most used transistor in front-end PFCs[10]. However, recently wide-band-gap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have gained momentum in power electronic components, especially for higher voltages >400V due to their higher breakdown voltage[11], [12]. To this date SiC is the WBG semiconductor which has seen the most progress because of its temperature stability, both allowing for smaller heat sinks through higher operating temperature and enabling use in environments with big variations in ambient temperature [13]. However, for high very high switching frequencies (MHz range) the Si SiC MOSFETs are having difficulties achieving soft switching due to the high reverse recovery charge [9]. Therefore, lately the GaN high-electron-mobility transistors (HEMTs), also called heterostructure field-effect transistors (HFETs), have become very interesting, with a very low recovery charge. Furthermore, the GaN HEMT has no reverse body diode, making it symmetrical and thus advantageous for bidirectional purposes, and it has a lower on-state resistance. This will be explained in more detail in section II.



(a) The basic bridgeless PFC



(b) The totem pole PFC

Fig. 3: The simplest bridgeless PFC topologies, as found in [2].

C. Scope of work

This review will present and investigate the state of the art in bidirectional PFC topologies, and the use of GaN HEMTs in these topologies. Section II will present the concept of GaN HEMTs, with emphasis on the electrical performance of the transistor. Section III will evaluate the state-of-the art bidirectional PFCs and the present and potential use of GaN HEMTs in these.

II. GaN HEMTs

A. Structure

The basic structure of a GaN HEMT is shown in figure 4[14]. Its foundation consists of bottom-layer semiconductor substrate (often silicon, due to low price [11]). The main GaN structure consists of AlGaN layer grown on top of a GaN channel, forming a highly conductive two-dimensional electron gas (2DEG) layer in between. Between the substrate and the GaN structure is a high-resistivity buffer layer to ensure high breakdown voltage of the transistor. A dielectric is isolating the gate contact from the AlGaN-layer to prevent gate leakage current[15] and current collapse[16].

One of the key positive attributes of the GaN HEMT lies in the 2DEG layer; GaN has a higher breakdown voltage than SiC (and much higher than Si, see figure 5[17]), which means

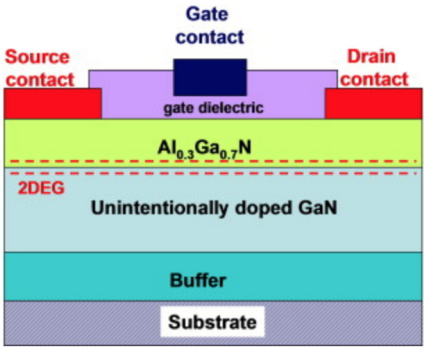


Fig. 4: The basic structure of a GaN HEMT, as found in [14]

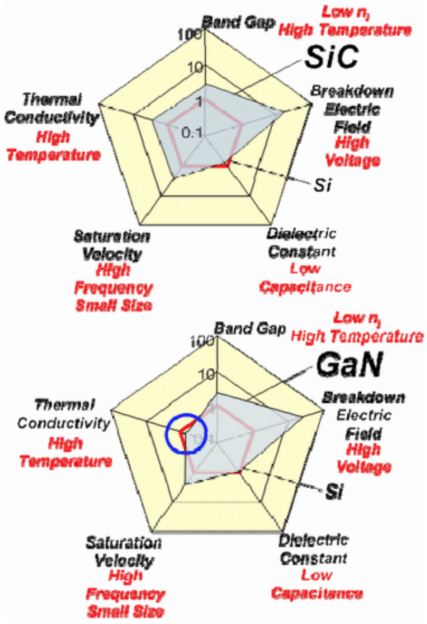


Fig. 5: Five relative material attributes of GaN versus SiC and Si, as found in [17]

the material itself has a higher resistivity. However the low-resistivity 2DEG layer in the GaN HEMT makes the on-state resistance lower than for a SiC MOSFET. Thus the conduction losses of a GaN HEMT is lower than that of a SiC MOSFET. Furthermore, both the gate charge and output capacitance of the HEMT is smaller than for a Si and SiC MOSFETs[18].

A feature which is apparent looking at the structure of the GaN HEMT in figure 4 is that there is no PN junction between source and drain in the off-state, as is present in a MOSFET. The body PN junction is what creates the reverse

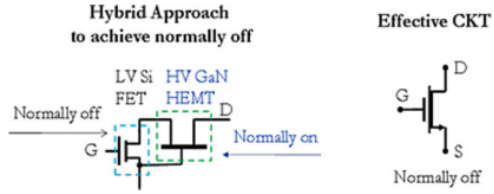


Fig. 6: The circuit diagram and resulting symbol of a cascode GaN HEMT, as found in [18].

body diode in the MOSFET, so this means that that the HEMT does not contain a reverse body diode. Thus the GaN HEMT is completely symmetrical from drain to source, making it a bidirectional in switching operation. This is a feature that comes in handy for some bidirectional converter purposes, and will be discussed further in section III.

Although seeming superior to other semiconductor materials up until this point, there is of course a drawback to GaN as well; as highlighted in figure 5, GaN has relatively lower thermal conductivity compared to both SiC and Si. Consequently, GaN transistors are not as capable of transferring dissipated heat to the environment, resulting in an increased temperature inside the transistor. This increases the risk of melting and cracking inside the transistor package. To avoid these effects, it is important to keep the losses at a low level, and since the on-state resistance is already very low, that means minimizing the switching losses. Otherwise this would have to be compensated by a bigger heat sink, increasing the converter size and weight.

B. Normally-off GaN HEMTs

The 2DEG layer does, despite its positive effects, introduce some issues. Since this layer is present without any voltage on the gate, the GaN HEMT is by nature normally on, i.e. it is conducting without an applied gate voltage. The HEMT is instead blocking when voltage is applied on the gate. In power electronics it is demanded to have normally-off transistors, so modifications have to be made in order to make a normally-off GaN HEMT-based transistor [18].

The simplest of these modifications is cascading the HEMT with a low-voltage normally-off Si FET, to form what is called a cascode GaN HEMT, as in [11], [18], [19], [20]. However, while simple in theory, such an arrangement should be made single-chip in order to reduce the inductance in bond wires and PCB traces, which is not so simple from a mechanical point of view. The circuit diagram and symbol of cascode GaN HEMT is shown in figure 6. Here the gate of the HEMT is connected to the source of the low-voltage FET, so that when there is no voltage applied to the gate of the FET there is a voltage at the gate of the HEMT, meaning the HEMT is blocking. Oppositely, when the FET gate voltage is high, the HEMT gate is at HEMT source potential, meaning the HEMT is conducting. This sort of cascade connection will necessarily make the gate charge of the HEMT slightly higher, since both the gate charge and the output capacitance of the FET will delay the gate voltage of the HEMT, not allowing for as fast switching as for the HEMT alone. Huang, X. et. al. (2014)

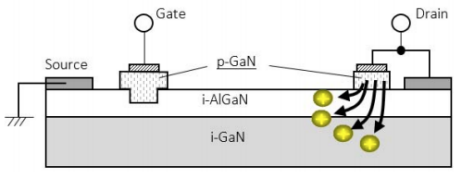


Fig. 7: The basic structure of a p-GaN hybrid drain GIT, as found in [20].

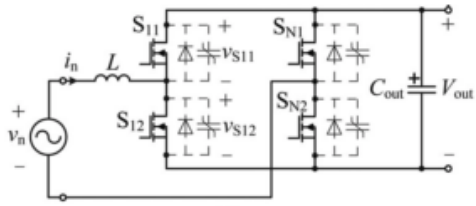


Fig. 8: A MOSFET-based bidirectional totem-pole PFC, as found in [7].

have shown that due to especially the parasitic capacitances of the low-voltage FET, the switching losses of the cascode GaN HEMT during hard turn-on are very high [21]. The same article does however reveal a mechanism that assures the hard-switched turn-*off* losses to be minimal. For that reason, the cascode HEMT should always be operated with soft-switched turn-on, while it can easily be operated with hard-switched turn-off.

Chowdhury, S. (2015) and Chen, K. et. al. (2017) are presenting some other solutions for a normally-off GaN HEMT without external FETs or other components, called E-mode GaN transistors [18], [20]. These are all in development, and have mostly not been commercialized. One type that has been commercialized, however, is the p-GaN gate injection transistor (GIT), brought up by Efficient Power Conversion. In this technology a p-type GaN layer inserted between the gate channel and the AlGaN layer. Given the right thickness and doping, this p-GaN layer could attract enough negative charges to empty the 2DEG layer[20]. This way there is no conduction channel when there is no gate voltage, and the HEMT is normally off. To solve current collapse issues, an additional p-GaN layer is connected between the drain and the AlGaN. Such a variation to the GIT is called hybrid drain GIT and is depicted in figure 7. Using these sort of E-mode GaN transistors it is possible to achieve faster switching transients and lower switching losses compared to the cascode GaN HEMT solution, since the gate charge and the parasitic capacitances of the FET are avoided. Besides, the solution is compact, avoiding any wire inductances. The downside is that these solutions are more complex and thus more expensive and they are, as mentioned, still in development.

III. Bidirectional PFCs

A. Topologies

The topology of a simple bidirectional totem-pole PFC is shown in figure 8. This exact topology is proposed in [7], but is completely based on the totem-pole PFC (see figure 3b), which has been discussed in plenty of research already [5], [22], [23], [24]. Other newer studies are also looking at the bidirectional totem-pole PFC [8], [9], [25]. The bidirectional power flow capability is in [7] actually a positive side effect of the substitution of diodes with MOSFETs to reduce conduction losses by removing diode forward voltage drop. The totem-pole leg MOSFETs S_{11} and S_{12} are switching at high frequency (several tens of kHz), while the rectifier leg MOSFETs operate at mains frequency.

The totem-pole PFC was previously discarded for the benefit of the basic bridgeless PFC (figure 3a), due to the combination of switch arrangement and too high reverse recovery charge in the body-diodes of the high-frequency MOSFETS making CCM unfeasible[5]. The converter can only operate in DCM or on the boundary of CCM/DCM, where it generates a lot of high-frequency noise with a peak-to-peak of twice the current amplitude, as can be seen in figure 2b. This again would require a large DM noise filter on the AC side. In addition, the peak current through the MOSFETs is twice of that at CCM, requiring a higher current rating of the MOSFET, and the switching losses at hard turn-off are higher. There are however drawbacks to the basic bridgeless PFC as well; it generates a lot of common-mode (CM) EMI noise due to a floating zero potential on the DC side, relative to AC ground[26]. This common mode noise is difficult to compensate and requires large CM filters, and it is a problem connected to the arrangement of the bridgeless PFC. Partly for that reason, the totem-pole has been given renewed attention, since it does not have that problem. Bidirectional front-end PFCs for power supplies that are proposed in these days are almost invariably using the bidirectional totem-pole topology [8], [9], [25], [27]. Some use an interleaved variation where the PFC switching stress is distributed across more than one parallel switching leg[7], [24], [9], [23]. Operated properly, the interleaved legs can cancel out second and third harmonics, and otherwise significantly decrease the current ripple[23]. The topology of an interleaved bidirectional totem-pole PFC is shown in figure 9. Modulation schemes called triangular current mode (TCM) have been proposed that ensure ZVS turn-on over the whole input voltage range by operating around CrCM and extending the current waveform to becoming negative at turn-on, so that the input capacitances of the MOSFETs are fully discharged before turn-on of the switches[7], [28], [23]. This modulation scheme makes bidirectional totem-pole PFCs more feasible. Be that as it may, it has some issues, with perhaps the most significant being how the negative current cause a ”dead time” in the input current, making the shape less sinusoidal, generating more harmonics. This is however partly solved in [9] using variable time control. This leads over to the next issue: the control using this modulation scheme is very complex; the average current needs to be computed accurately for each switching period, and the non-linear parasitic capacitances in the MOSFETs are hindering accurate analytic estimation of the timing parameters, thus making this computation difficult[7].

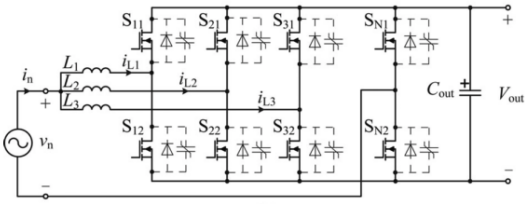


Fig. 9: A MOSFET-based interleaved bidirectional totem-pole PFC, as found in [7].

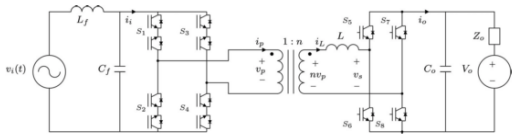


Fig. 10: The topology of an AC-DC DAB, as found in [31].

Other modulation schemes, including e.g. "valley switching", or "valley filling", give simpler control, but only gives ZVS turn-on when $v_s < 1/2V_{out}$, giving more hard switching over the mains voltage period, thus giving slighty more losses[29].

Power factor correction can also be achieved without the dedicated AC-DC PFC. Although most power supplies are two-step with an AC-DC PFC converter in series with an isolated DC-DC converter, there is an interest for the single-stage AC-DC dual active bridge (DAB) solution, especially as grid interfaces for renewable energy sources and bidirectional automotive charging[30], [31], [32], [33]. The topology of an AC-DC DAB converter is depicted in 10. The DAB interfaces in [31] and [32] achieve open-loop PFC by pulse-width modulating the DC bridge to keep the AC current in phase with the AC mains voltage. The converter also achieves ZVS in the DC bridge and ZCS in the AC bridge, it provides galvanic isolation and it has simple current control through controlling only the phase shift. It does however not achieve ZVS across the whole AC mains voltage period, as the MOSFET capacitances are not able to fully charge and discharge at low current and voltage levels. Furthermore there is a need for bidirectional switches since the input voltage switches polarity, and the MOSFET-based bidirectional switches are causing losses due to the forward voltages of the body diodes or external diodes.

B. The use of GaN in bidirectional PFCs

And so to where GaN comes into the picture in bidirectional PFCs. GaN HEMTs or e-HEMTs have the potential to improve the bidirectional PFCs, e.g. solving some of the issues mentioned with the PFCs and otherwise compressing the physical executions of these converters. One example is how the switching nature of the cascode HEMT make them ideal for the totem-pole PFC when operating in TCM; the turn-off losses of the cascode GaN HEMT are minimal and the converter achieves ZVS turn-on. Combining that with a very low on-state resistance of the GaN HEMT and the losses of the converter become astonishingly small. Liu, Z. et.al. (2015) was able to achieve a peak efficiency of 99% using that technique with cascode GaN HEMTs in two interleaved totem-pole legs and TCM[9]. The operating frequncy was 1 MHz. In general GaN has smaller parasitic capacitances, smaller gate charge and no reverse body diode, which yields faster switching transients, again giving smaller losses. This permits a higher switching frequency. Higher frequency ripple allows for smaller EMI filter and smaller magnetic components, such as inductors and high-frequency transformers (galvanic isolation) in the power supply, which is confirmed in [9], where an ten-times increase in switching frequency from 100kHz to 1 MHz led to a 50% reduction in DM EMI filter size. Ripple magnitude of the totem-poe PFC is still large, but increasing the frequency many-fold makes the ripple easier to filter out. In this specific case the issue is still the complexity of control using TCM, although the mentioned less significant non-linearity of the HEMTs might somewhat facilitate the timing in the control. More complex control requires more advanced MCUs, requiring larger control circuits. However, it is also shown in [9] that even using regular CrCM with valley switching, a peak efficiency of over 98% was achieved at 1MHz switching and 1.2 kW power.

Xue, L. et. al. has made a bidirectional totem-pole PFC using GaN e-HEMTs in the totem-pole leg, operating in CCM[8]. In this study, focus is put on the current behaviour around the voltage zero crossing. This study finds that there is a current spike at this zero-crossing, owing to dead-time of the low-frequency rectifier leg. It finds that with big difference in switching frequency between the two legs of the totem-pole PFC, there is an increased current spike at the zero crossing. This issue is mainly related to the control, and adds to the complexity of control of totem-pole PFC. It does however show that using GaN e-HEMTs, the totem-pole PFC can be ran in CCM, minimizing current ripple. The reference design GaN E-HEMT-based bidirectional totem-pole PFC made by GaN Systems also operates in CCM, enabled by the fast switching transients of the GaN HEMTs[34]. It achieves a peak efficiency of 99% and a power factor close to 1, operating at a switching frequency of 65kHz and power of 1.5 kW.

The GaN E-HEMT could also give improvement to the AC-DC DAB topology. The bidirectional MOSFET switch in the AC-bridge is causing conduction losses due to the current flowing through two of the reverse body diodes at all times (see figure 10). As previously mentioned, the GaN E-HEMT is by nature bidirectional, with no reverse body diode. Swapping the bidirectional MOSFET switches with GaN E-HEMTs would give a simpler structure, with only one gate at each switch, and the conduction losses would be substantially reduced due to the low on-state resistance. Furthermore, swapping all the switches to GaN E-HEMTS, the switching frequency could be increased, decreasing the size of the high-frequency transformer and inductor. Xue, L. et. al. (2015) made a DC-DC DAB with a peak efficiency of 98.2% when operating at 1 kW and 500MHz. Regular MOSFET-based DABs are operating around 100kHz, so this would mean a substantial decrease in the size of transformer, inductor and filter.

IV. Conclusion

This paper has discussed and evaluated GaN technologies and bidirectional PFCs, and their joint potential and present

use. The cascode GaN HEMT is looking the simplest solution to a GaN transistor, but with difficulties affiliated to compactness and high turn-on losses. However due to the ZVS turn-on of the bidirectional totem-pole, this seems a promising combination. Other GaN transistor technologies, such as the GIT E-HEMTs has seen commercialization and are looking promising both for bidirectional totem-pole PFCs and AC-DC DABs. In any case, GaN is relatively young in a power electronics context, and because of that the prices are high and there are issues connected to especially control that need to be sorted out. Despite of that, there is hardly any doubt that GaN has a future in power supplies, bidirectional or unidirectional, due to their big potential of both increasing efficiency and decreasing size.

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Appendix D

D.1 Modulus Optimum in current loop

D.1.1 PI controller parameters

Choosing $T_{i,i} = L/R_L$ and implementing to (4.21), the open-loop transfer function can be reduced to:

$$H_{ol,i}(s) = \frac{K_{p,i}}{L} \cdot \frac{1}{s \cdot (1 + T_{sum,i} \cdot s)} \ , \tag{D.1}$$

giving the following closed-loop transfer function:

$$H_{cl,i}(s) = \frac{i_{AC}(s)}{i_{AC,ref}(s)} = \frac{1}{1 + \frac{L}{K_{p,i}} \cdot s + \frac{LT_{sum}}{K_{p,i}} \cdot s^2} \ . \tag{D.2}$$

Comparing (D.2) to the standard equation for a second-order system, which is

$$H_{2.order}(s) = \frac{1}{1 + 2\zeta \frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \ , \tag{D.3}$$

expressions for the relative damping ζ and the resonant frequency ω_0 can be found as

$$\zeta = \frac{1}{2}\sqrt{\frac{L}{K_{p,i} \cdot T_{sum,i}}}\ , \quad \omega_0 = \sqrt{\frac{K_{p,i}}{L \cdot T_{sum,i}}}\ . \tag{D.4}$$

In modulus optimum, it is common setting $\zeta = 1/\sqrt{2}$. [40, ch. 3.2.3] Implementing that to (D.4), an expression for the proportional gain can be found, giving the following controller parameters:

$$K_{p,i} = \frac{L}{2 \cdot T_{sum,i}}\ , \quad T_{i,i} = \frac{L}{R_L}\ . \tag{D.5}$$

D.1.2 Current measurement filter design with Modulus optimum

As explained in section 4.2.2, the integrator time constant limits the ripple of the control signal, in this case d. The control signal ripple is caused by the proportional gain on the measured ripple. Acknowledging this and neglecting the integrator part of the PI as well as the reference current, which has no ripple, the following expression can be obtained based on figure 4.7 and (4.15): [40, ch. 3.4.1]

$$\frac{d_{ripple}(s)}{i_{AC,ripple}(s)} = K_{p,i} \cdot \frac{1}{1 + T_{fi,i} \cdot s}\ . \tag{D.6}$$

Based on D.6, the amplitude of the ripple can be expressed as follows:

$$\hat{d}_{ripple}(\omega_{ripple}) = K_{p,i} \cdot \frac{1}{\sqrt{1 + (\omega_{ripple} T_{fi,i})^2}} \cdot \frac{1}{2}\Delta I_L(\omega_{ripple})\ . \tag{D.7}$$

Substituting the expression for $K_{p,i}$ in D.5 into (**??**), an expression for the duty cycle ripple can be given as follows:

$$\hat{d}_{ripple}(\omega_{ripple}) = \frac{L}{2 \cdot T_{sum,i}} \cdot \frac{1}{\sqrt{1 + (\omega_{ripple} T_{fi,i})^2}} \cdot \frac{1}{2}\Delta I_L(\omega_{ripple})\ . \tag{D.8}$$

It is stated in [40, 3.4.1] that the control voltage ripple amplitude, in this case $\hat{d}_ripple$, should be kept at values between 0.04 and 0.08, to avoid the controller itself generating harmonics while still limiting the delay of the filter. Solving (D.8)

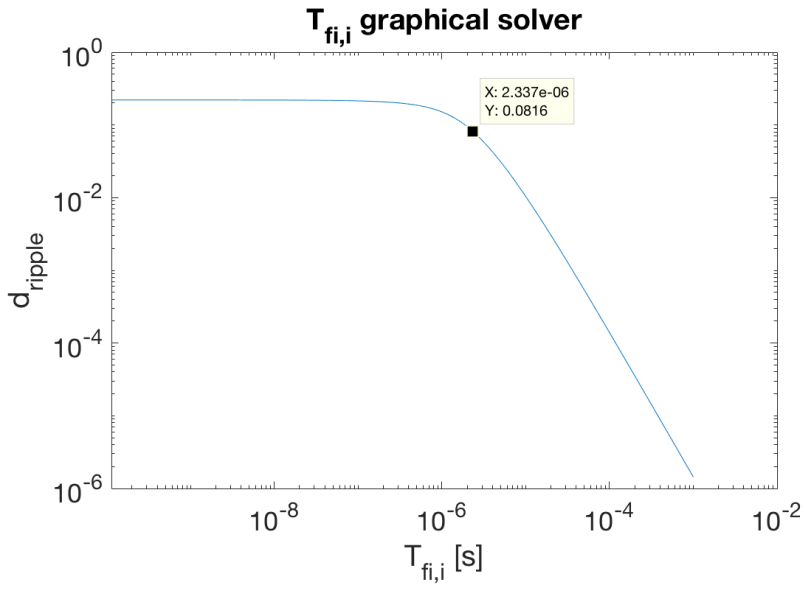

Figure D.1: Graphical solution of current filter time constant $T_{fi,i}$ with Modulus optimum.

graphically at switching frequency $\omega_{ripple} = 2\pi f_{sw}$ and choosing $\hat{d}_{ripple} = 0.08$ for fast response, as shown in figure D.1, the filter time constant is found to be:

$$T_{fi,i} = 2.4\mu\text{s} \ .$$

D.1.3 Simulations

Implementing the deduced parameters to the PI controller and the current filter, simulations could be performed for the current controller. Figure D.2 shows the waveforms through the current controller throughout one mains cycle. The figure shows that the rectified actual current *imeas* is not able to follow the reference rectified current *iref*, with measurement error *ierr* varying from 0 to 0.6.

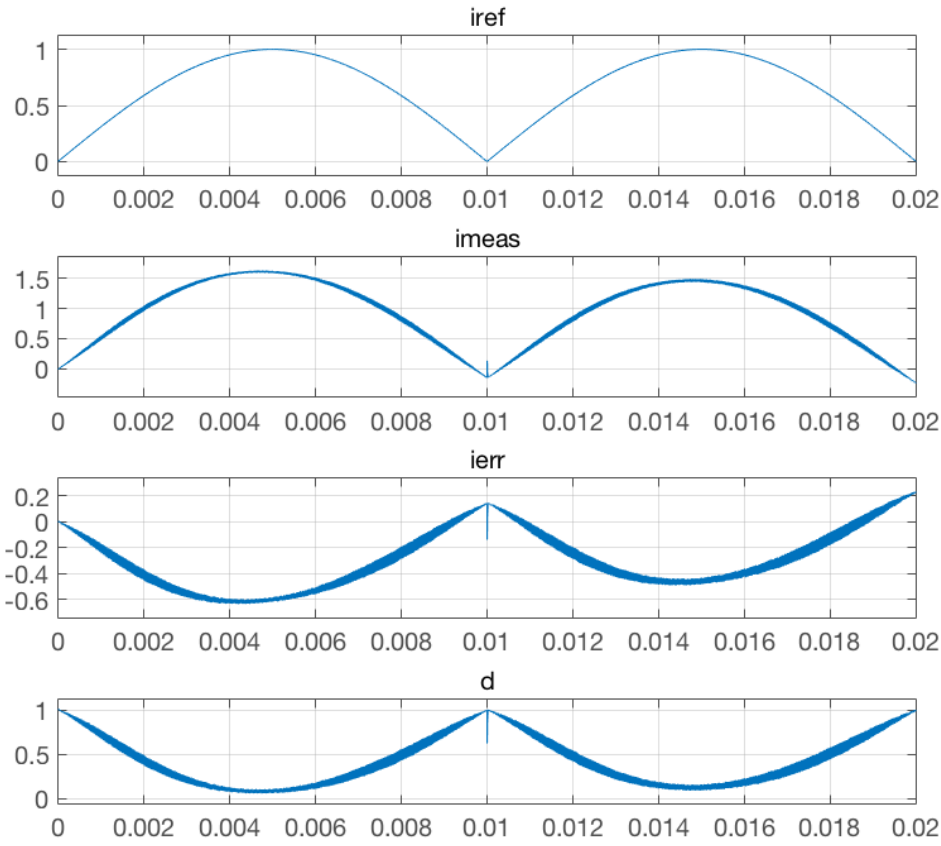

Figure D.2: Current controller waveforms over one mains period with Modulus optimum

Appendix E

Implemented Simulink model

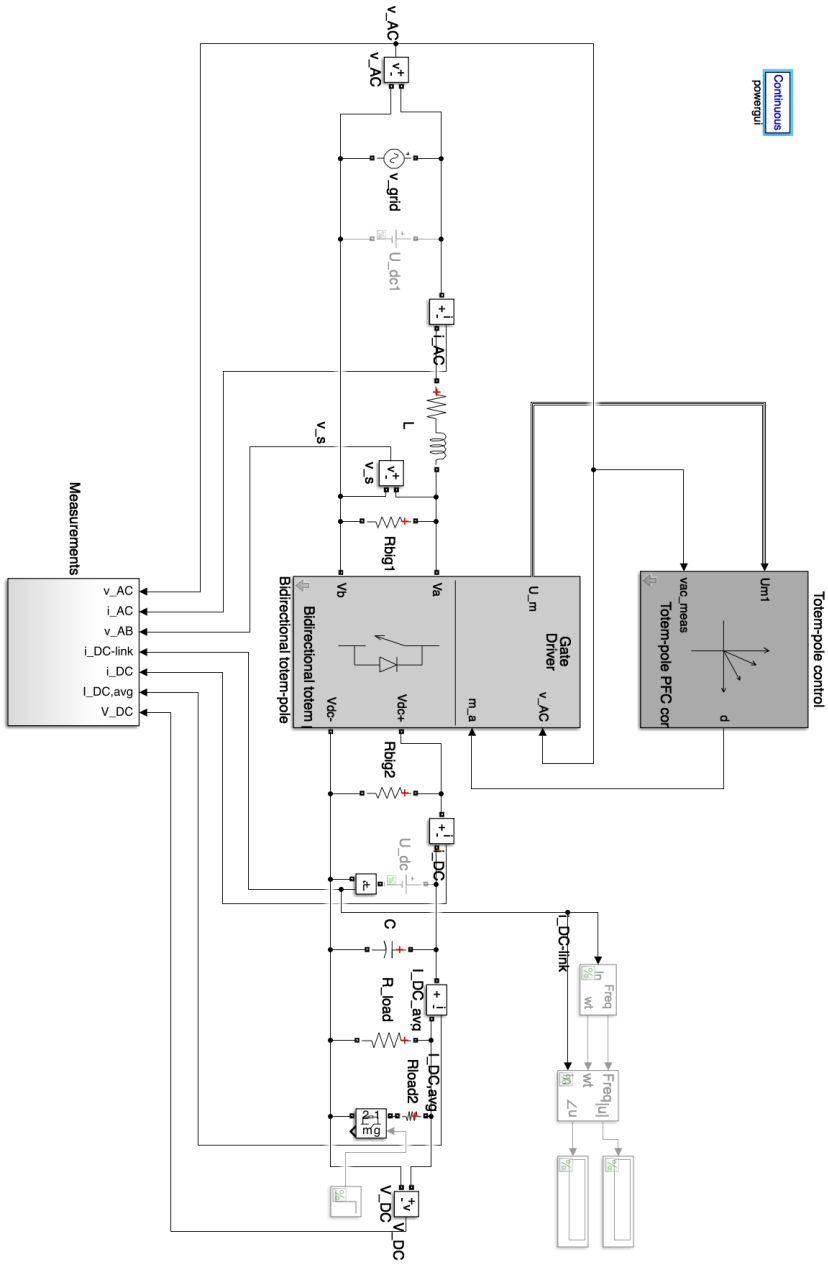

Figure E.1: The complete totem pole converter implemented in Simulink.

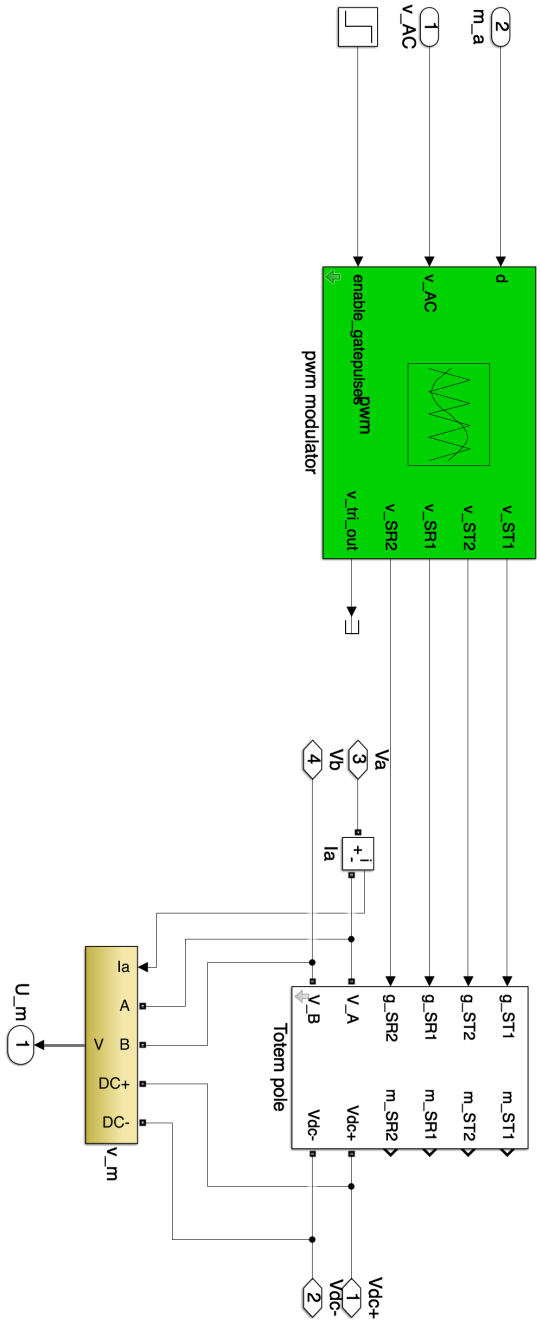

Figure E.2: The gate drive and totem-pole bridge.

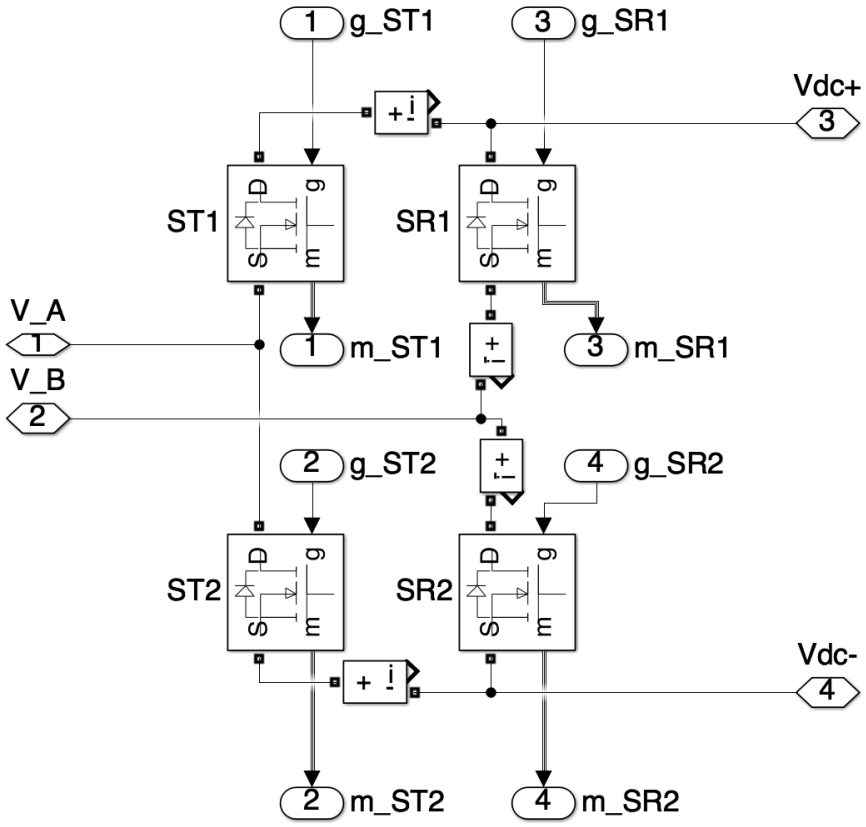

Figure E.3: The the totem-pole bridge implemented in Simulink

Appendix F

MATLAB code

F.1 Controller tuning script

```
1
2 % Chosen parameters
3
4 Vac = 230; %V
5 Vacpeak = sqrt(2)*Vac; %V
6 Vdc = 340; %V
7 Vdcmax = 400; %V
8 Iac = 16; %A
9 Iacpeak = sqrt(2)*Iac; %A
10 Pac = Vac*Iac; %W
11 fsw = 90e+03; %Hz
12 wsw = 2*pi*fsw; %Hz
13 fgrid = 50; %Hz
14
15 Kiripple = 0.2; % peak-to-peak current ripple factor
     [%/100%]
16 Kvripple = 0.1; % peak-to-peak switching frequency
     voltage ripple [%/100%]
```

```
17 ILpeak2peak = Kiripple*Iacpeak; %A
18 VCpeak2peak = 20; %V
19 Kvdc = VCpeak2peak/Vdc;
20
21
22 %Base values
23
24 Vbase = Vdc;
25 Ibase = 16*sqrt(2);
26 Rbase = Vbase/Ibase;
27
28
29 % Component dimensioning
30
31 L = 0.25*Vdcmax/(ILpeak2peak*fsw); %H
32 C = 1.8e-3; %F
33
34
35
36
37 %% CURRENT CONTROLLER design using PI and SYMMETRICAL
       OPTIMUM
38
39 %Base values
40 Vbase = Vdc;
41 Ibase = 16*sqrt(2);
42 Rbase = Vbase/Ibase;
43
44 %PU parameters
45 Lpu = L/Rbase;
46
47 %Time constants and gains
48 Tpwm = 1/(3*fsw);
49 fci = 10^(-0.8)*fsw;
50 Kfi = 1;
```

```
51 Kregi = 1;
52 Tfi=2.7e-6;
53 Tsum_i = Tfi+Tpwm;
54
55 %Symmetrical optimum
56 betai = 1/(2*pi*fci*Tsum_i)^2;
57 Tii = betai*Tsum_i;
58 Kpi = Lpu*Kregi/(Kfi*sqrt(betai)*Tsum_i);
59
60 display(Tii)
61 display(Kpi)
62
63
64 %Bode plot
65 Hol_i = tf(Kpi/(L*Tii)*[Tii 1],[Tsum_i 1 0 0]);
66 % bode(Hol_i)
67
68
69
70 %% CURRRENT CONTROLLER design using PI and MODULUS
       OPTIMUM
71
72 Rl = 10e-03; %Parasitic resistance of
73
74 %Base values
75 Vbase = Vdc;
76 Ibase = 16*sqrt(2);
77 Rbase = Vbase/Ibase;
78
79 %PU parameters
80 Lpu = L/Rbase;
81 Rlpu = Rl/Rbase;
82
83 %Time constants and gains
84 Tl = L/Rl;
```

```
85 Tpwm = 1/(3*fsw);
86 Tfi = 2.4e-6;
87 Tsum_i = Tpwm+Tfi;
88
89 f0_i = 1/(2*pi*sqrt(2)*Tsum_i);
90
91 %Modulus optimum
92 Tii = Tl;
93 Ks = 1;
94 Kpi = Lpu/(2*Ks*Tsum_i);
95
96 display(Tii)
97 display(Kpi)
98
99 %Crossover frequency (cut-off frequency)
100 wc2 = -1/(2*Tsum_i^2)+sqrt(1/(4*Tsum_i^4)+(Kpi*Ks/(Lpu
      *Tsum_i))^2);
101 wc = sqrt(wc2);
102 fc = wc/(2*pi);
103
104
105 Bode plot
106 Hol_i = tf(Kpi/L,[Tsum_i 1 0]);
107
108 bode(Hol_i)
109
110
111 %% Voltage controller design using symmetrical optimum
112
113 %PU parameters
114 Cpu = C/Rbase;
115
116 %Time constants and gains
117 ffiv = 20; %Filter cut-off frequency
118 Tfiv = 1*10^(-4);%1/ffiv; %Time constant
```

```
119 Tsum_v = Tfiv+2*Tsum_i; %Sum of delays
120
121 fcv = 500;%10^(-0.7)*fci; %Voltage loop cutoff
    frequency
122 Kfiv = 1;
123 Kregv = 1;
124
125 %Symmetrical optimum
126 betav = 1/(2*pi*fcv*Tsum_v)^2;
127 Tiv = betav*Tsum_v;
128 Kpv = Cpu*Kregv/(Kfiv*sqrt(betav)*Tsum_v);
129
130
131 display(Tiv);
132 display(Kpv);
```

F.2 Filter graphical solver

```
1 %--> Filter time constant (Belongs to
    Totem_pole_script.m, which needs to be run first)
2
3 %% Current controller with Modulus optimum
4
5 Tfistep = 1e-10;
6 Tfimax = 1e-03;
7 Tfivector = 0:Tfistep:Tfimax;
8 m_a_ripple = zeros(1,length(Tfivector));
9
10 for i = 1:length(Tfivector)
11     m_a_ripple(i) = 1/2*Kiripple*Lpu/(2*(Tpwm+Tfivector
       (i))*sqrt(1+(Tfivector(i)*2*pi*fsw)^2));
12 end
13
14 close all
15 figure
```

```
16 loglog(Tfivector,m_a_ripple)
17 title('T_{fi,i} graphical solver')
18 xlabel('T_{fi,i} [s]')
19 ylabel('d_{ripple}')
20 set(gca,'fontsize',18)
21
22
23 %% Current controller with Symmetrical optimum
24
25 wci = 2*pi*fci;
26
27 Tfistep = 1e-10;
28 Tfimax = 1e-03;
29 Tfivector = 0:Tfistep:Tfimax;
30 m_a_ripple = zeros(1,length(Tfivector));
31
32 for i = 1:length(Tfivector)
33     m_a_ripple(i) = 1/2*Kiripple*Lpu*wci/sqrt(1+(
          Tfivector(i)*2*pi*fsw)^2);
34 end
35
36 close all
37 figure
38 loglog(Tfivector,m_a_ripple)
39 title('T_{fi,i} graphical solver')
40 xlabel('T_{fi,i} [s]')
41 ylabel('d_{ripple}')
42 set(gca,'fontsize',18)
43
44
45 %% Voltage controller with symmetrical optimum
46
47 wcv = 2*pi*500;
48
49 Tfvstep = 1e-8;
```

```
50 Tfvmax = 1e-02;
51 Tfvvector = 1e-6:Tfvstep:Tfvmax;
52 i_ctrl_ripple = zeros(1,length(Tfvvector));
53
54 for i = 1:length(Tfvvector)
55     i_ctrl_ripple(i) = 1/2*Kvdc*Cpu*wcv/sqrt(1+(
           Tfvvector(i)*2*pi*2*fgrid)^2);
56 end
57
58 close all
59 figure
60 loglog(Tfvvector,i_ctrl_ripple)
61 title('T_{fi,v} graphical solver')
62 xlabel('T_{fi,v} [s]')
63 ylabel('i_{ctrl,ripple}')
64 set(gca,'fontsize',18)
```

Appendix G

System-level simulations

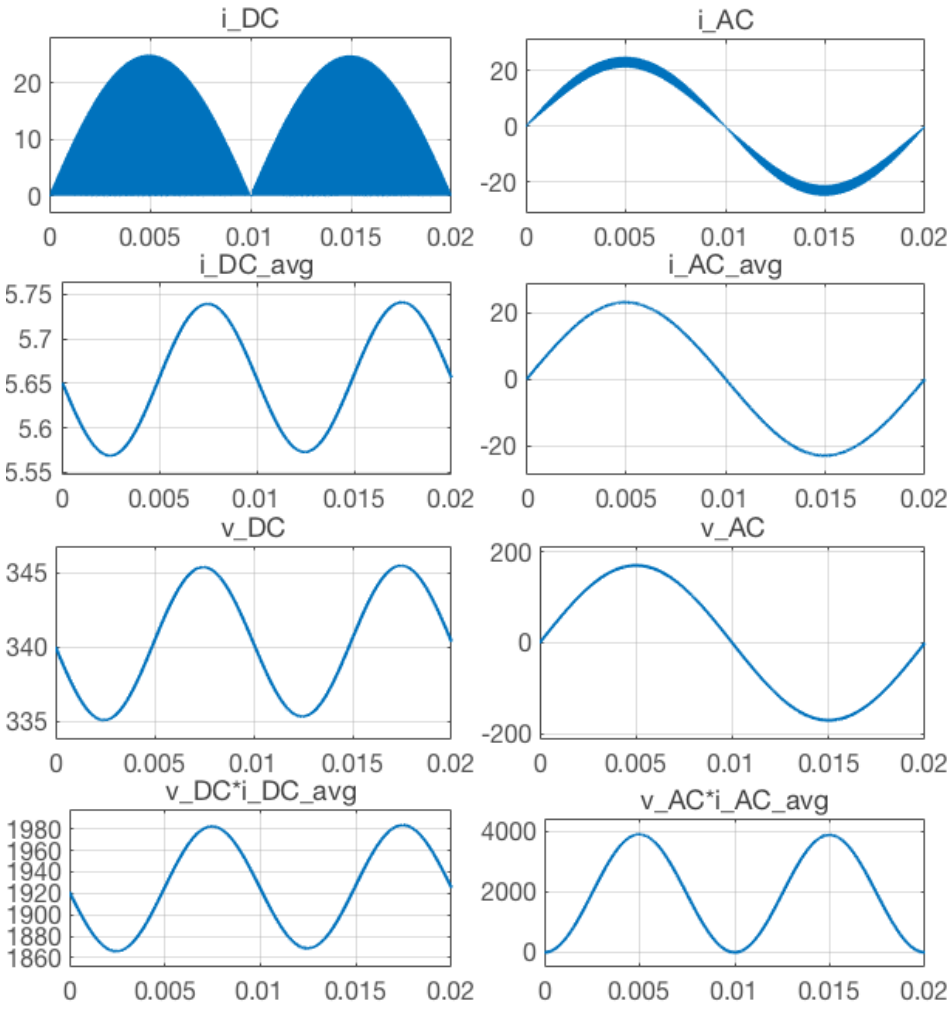

Figure G.1: System-level simulation results at 120Vrms G2V operation.

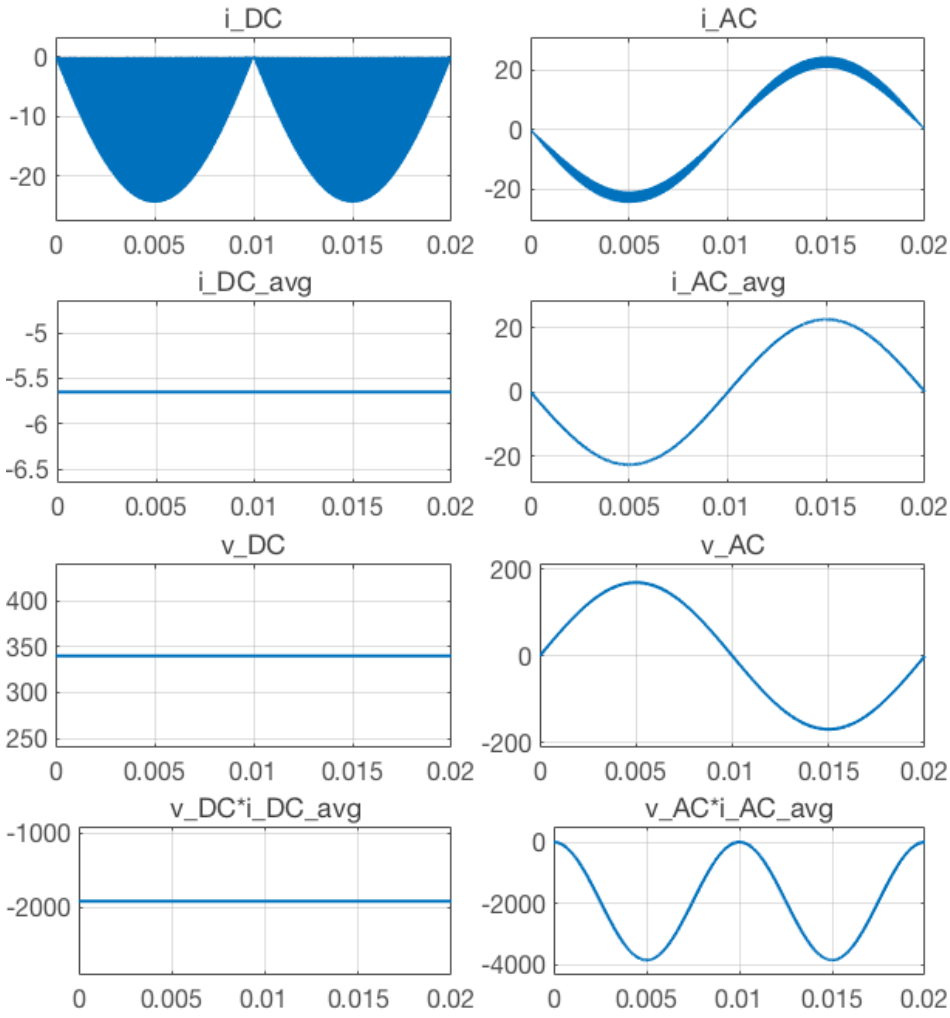

Figure G.2: System-level simulation results at 120Vrms V2G operation.