An Approach for Small Scale Power Hardware in the Loop Emulation of HVDC Cables

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***Abstract*—Long HVDC cables are difficult to emulate in laboratory settings due their complex behaviour and fast transient response. This paper presents the methodology for the design and the laboratory implementation of a HVDC cable emulator with a Power Hardware in the Loop approach. The cable representation in the real time simulation is based on the Universal Line Model present in state of the art software for electromagnetic transients analysis. The proposed cable emulation reproduces the cable dynamics up to the kHz range with present commercially available hardware. Moreover, this approach offers a higher flexibility in adapting the cable characteristics and length compared to other existing alternatives.**

I. Introduction

The future integration of offshore renewable energy sources sets the HVDC transmission as the most suitable power transport solution to interconnect multiple countries over long distances, and has incomparable advantages in case of offshore applications, especially in the North Sea [1]. However, multiterminal HVDC grids are complex systems requiring the efficient and coordinated operation of many different components. Future HVDC networks will be based on voltage source converters (VSC), due to the possibility of reversing the power flow without voltage polarity reversal and independent controllability of active and reactive power. A second key element of the HVDC network is the transmission line/cable [2], which adds fast and low transient dynamics to the grid. The modeling of the cable is pivotal to identify resonance frequencies and study the stability of the system [3]. Recently, considerable progress has been made on the validation of simulation results on HVDC systems on scaled laboratory setups. However, a common challenge is the lack of a flexible and practical approach to reproduce accurately the dynamic effects introduced by long HVDC cables. In order to improve the fidelity of laboratory tests this paper aims to reduce the dynamics missing due to poor modeling of the line/cable on HVDC systems with an approach based on Power Hardware in the Loop (PHiL) [4], [5]. This is done by introducing a physical implementation a single conductor model from the Universal Line Model (SC-ULM) [6] on a controlled voltage source that can represent dynamics with a limited frequency bandwidth (BW). The topology used for the implementation is in the PHiL systems category. Some experimental validations of HVDC systems used equivalent Π model to emulate the dynamics of the cable in scaled platforms [7]. However, this model includes fixed RL series impedance and does not accurately represent the characteristics of a cable. On the other hand a laboratory test bed with PHiL has been reported in [8], [9] where the high voltage cables are presented with real low voltage cables: the rating of the systems is 2.5/5.0 kW and 250 Vdc. The use of a short distance and a low voltage cable in the scaled laboratory setup does not necessarily ensure that the dynamics of a high voltage cable are properly emulated. Moreover, if a controlled voltage source (CVS) with high BW is available, a PHiL approach could be more convenient than connecting very long sections of low voltage cables. Therefore, the contribution of this paper is on the PHiL application of the SC-ULM used for HVDC cables [10], which broadly captures its frequency dependent behaviour.

This paper is organized as follows: Section II describes the basic theory of line/cable models in frequency domain. Section III presents the model with difference equations used on the real-time simulator. The simulation results are shown and discussed in section III-A. Section IV describes the basic PHiL theory. Section V presents the power hardware in the loop application of the cable model and the stability of the PHIL. Section VI shows the comparison of the laboratory and the simulation

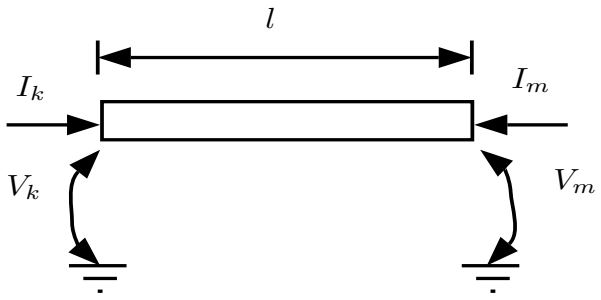

Fig. 1. Cable terminals.

results of the receiving side of the cable emulated. Finally, the conclusions are highlighted in section VII.

II. Phase modeling

The nodal current equations at the ends of the cable shown in Fig. 1 are described as a function of the frequency ω by the following equations [11].

$$\begin{aligned} -I_k(\omega) + Y_c(\omega)V_k(\omega) = \\ H(\omega)(Y_c(\omega)V_m(\omega) + I_m(\omega)) \end{aligned} \quad (1)$$

$$\begin{aligned} -I_m(\omega) + Y_c(\omega)V_m(\omega) = \\ H(\omega)(Y_c(\omega)V_k(\omega) + I_k(\omega)) \end{aligned} \quad (2)$$

where the sub-indices k, m represent the k and m extremes, $V_x(\omega)$ and $I_x(\omega)$ with $x \in k, m$ are the voltage and current at the cable ends, $Y_c(\omega)$ is the characteristic admittance described in (4) and the propagation function $H(\omega)$ is presented in (5).

$$\Gamma(\omega) = \sqrt{Z(\omega)Y(\omega)} \quad (3)$$

$$Y_c(\omega) = Z^{-1}(\omega)\Gamma(\omega) \quad (4)$$

$$H(\omega) = e^{-\Gamma(\omega)l} \quad (5)$$

where $\Gamma(\omega)$ is the propagation coefficient, l is the length of the cable, $Z(\omega)$ is the series impedance and $Y(\omega)$ is the shunt admittance.

In order to obtain a corresponding time domain model and study transient phenomena, the frequency responses $Y_c(\omega)$ and $H(\omega)$ are approximated by rational functions in the frequency domain. This can be done by using the vector fitting technique [11]. Therefore $Y_c(\omega)$ and $H(\omega)$ can be written in the Laplace domain as:

$$Y_c(s) \approx \sum_{i=1}^{p} \frac{c_i}{s + a_i} + d, \quad i = 1, ..., p. \quad (6)$$

$$H(s) \approx e^{-s\tau} \left(\sum_{i=1}^{n} \frac{c_i}{s + a_i} + d \right), \quad i = 1, ..., n. \quad (7)$$

where, a, c, d are used as the fitting parameters, p is the number of poles used for the fitting of $Y_c(s)$, and n the number of poles used for the fitting of $H(s)$. The parameter τ is the time delay introduced by the propagation function. This approximations are at the core of the model normally referred as Universal Line Model (ULM) [10], [12]. This method is consolidated and has been implemented in many electromagnetic transient programs e.g. PSCAD, EMTP-RV. The idea behind the rational functions approximation is to develop a discrete time system for equations (1) and (2).

This approximation will be discussed in the next section. The transfer function in (5) can be split in two functions as

$$H(s) = H_0(s)e^{-s\tau} \quad (8)$$

The rational functions can then be represented as a state space system taking into account the imaginary residues and poles with the form described in (9)-(10), with $x = (x_R^T, x_1^T, x_2^T)^T$. The state variables are $x_R \in \Re^{re\times 1}$, where re is the number of all the real poles, and x_1, x_2 $\in \Re^{cc\times 1}$, cc is the number of pairs of complex conjugate poles.

$$\begin{aligned} s \begin{bmatrix} \dot{x}_R \\ \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} &= \begin{bmatrix} A_R & 0 & 0 \\ 0 & A_{creal} & A_{cimag} \\ 0 & -A_{cimag} & A_{creal} \end{bmatrix} \begin{bmatrix} x_R \\ x_1 \\ x_2 \end{bmatrix} \\ &+ \begin{bmatrix} 1 \\ 2 \\ 0 \end{bmatrix} u \end{aligned} \quad (9)$$

$$y = \begin{bmatrix} C_R & C_{creal} & C_{cimag} \end{bmatrix} x \quad (10)$$

where, A_R, A_{creal}, A_{cimag} are the state matrices for the real coefficients and the complex conjugated coefficients respectively. Finally, the matrices C_R, C_{creal}, C_{cimag} are the output matrices for the real coefficients and the complex conjugated coefficients.

III. Cable model with difference equations

The model for each nodal current block interconnection is presented in Fig. 2. It is explained in the following procedure. The application of the model (9)-(10) in a simulation software requires the difference equations to use the samples of the signals. This is possible by the application of the trapezoidal rule for numerical integration. The resulting system is presented in (11)[1].

$$\begin{aligned} x_n &= (I - \frac{\Delta t}{2}A)^{-1} \left((I + \frac{\Delta t}{2}A)x_{n-1} + \frac{\Delta t}{2}Bu_{n-1} \right. \\ &\left. + \frac{\Delta t}{2}Bu_n \right) \end{aligned} \quad (11)$$

$$y_n = Cx_n + Du_n \quad (12)$$

[1]Without loss of generalization the identity matrix is used as I, with the proper size for the system.

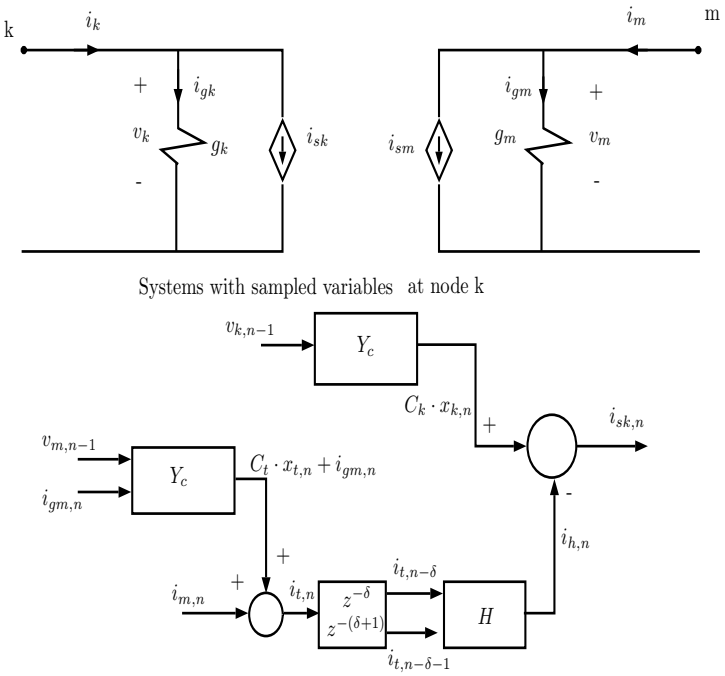

Fig. 2. Circuit and blocks representation for the sampled current at node k.

where, the subscripts n and $n-1$ represent the present and one delay samples, respectively. x_n, x_{n-1} are discrete state variables, y is the discrete output, and u is the input. It is useful to apply the following state transformation (13) to represent the system with present and past samples.

$$x_n^\epsilon = x_n - (I - \frac{\Delta t}{2}A)^{-1}\frac{\Delta}{2}Bu_n. \tag{13}$$

Therefore, the final system can be written as

$$x_n^\epsilon = \alpha x_{n-1}^\epsilon + (\alpha + I)\gamma u_{n-1} \tag{14}$$
$$y_n = Cx_n^\epsilon + (C\gamma + D)u_n \tag{15}$$

with the matrices $\alpha = (I - \frac{\Delta t}{2}A)^{-1}(I + \frac{\Delta t}{2})$ and $\gamma = (I - \frac{\Delta t}{2}A)^{-1}\frac{\Delta t}{2}B$. With Yc and H in discrete form, it is possible to model the nodal equations (1)-(2). This part can be seen as an application of Kirchhoff's current law to the discrete models. Equation (1) in the discrete time domain can be written as:

$$i_{k,n} - y_{ok,n} = -i_{h,n} \tag{16}$$

where, $i_{k,n}$ is the current at terminal k at the discrete instant n, $y_{ok,n}$ is the discrete output current at node k of the system $Y_c(\omega)V_k(\omega)$ and $i_{h,n}$ is the resulting discrete output current from the system $H(\omega)(Y_c(\omega)V_m(\omega) + I_m(\omega))$. The discrete currents are obtained by the following systems:

$$x_{k,n} = \alpha_k x_{k,n-1} + (\alpha_k + I)\gamma_k v_{k,n-1} \tag{17}$$
$$y_{ok,n} = C_k x_{k,n} + (C_k\gamma_k + D_k)v_{k,n} \tag{18}$$

where, the sub-indices for the matrices indicate the type of system, the discrete state variable of the system is $x_{k,n}$, the input is the voltage at the node at the time instants n and $n-1$. Moreover, the product $(C_k\gamma_k + D_k)v_{k,n} = g_k v_{k,n} = i_{gk,n}$ is a current measured directly from the system under simulation and g_k is an admittance. Therefore (18) is reduced to

$$y_{ok,n} = C_k x_{k,n} + g_k v_{k,n} = C_k x_{k,n} + i_{gk,n} \tag{19}$$

The current $i_{h,n}$ taking into account the delay δ (i.e. the discrete form of the delay τ) is:

$$x_{h,n} = \alpha_h x_{h,n-1} + (\alpha_h + I)\gamma_h i_{t,(n-1-\delta)} \tag{20}$$
$$i_{h,n} = C_h x_{h,n} + (C_h\gamma_h + D_h)i_{t,n-\delta} \tag{21}$$

where, $i_{t,n}$ is a temporary current variable that represents the output from the system $(Y_c(\omega)V_m(\omega) + I_m(\omega))$.

$$x_{t,n} = \alpha_t x_{t,n-1} + (\alpha_t + I)\gamma_t v_{m,n-1} \tag{22}$$
$$i_{t,n} = C_t x_{t,n} + (C_t\gamma_t + D_t)v_{m,n} + i_{m,n} \tag{23}$$

Finally, equation (16) can be modeled with the sampled variables:

$$i_{k,n} = i_{gk,n} + C_k x_{k,n} - i_{h,n} = i_{gk,n} + i_{s,n} \tag{24}$$

where, $i_{s,n}$ is the current based on past samples of the system.

$$i_{s,n} = C_k x_{k,n} - i_{h,n} \tag{25}$$

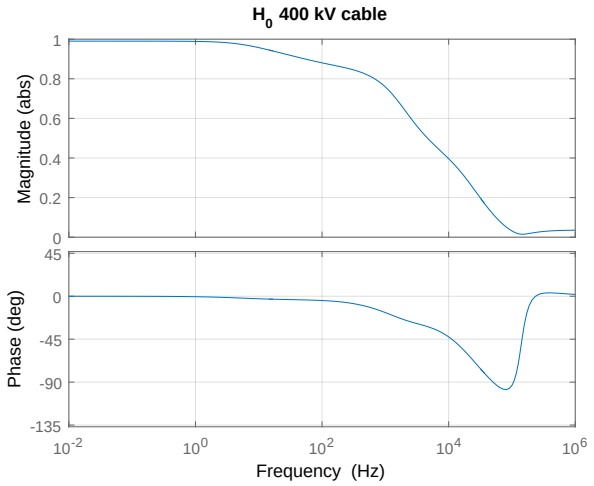

Fig. 3. Frequency response of the approximated propagation function.

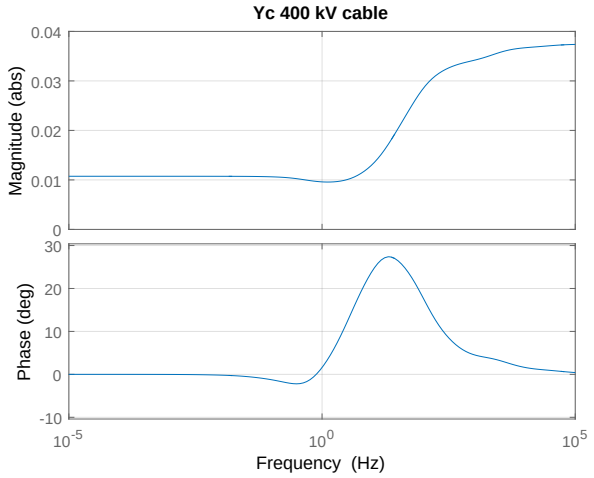

Fig. 4. Frequency response of the approximated characteristic admittance.

A. Cable example

The XLPE cable described in [2] with cross section of conductor 1800 mm^2 for 400 kV and 100 km length has the propagation function without delay ($H_0(s)$ in (8)) shown in Fig. 3. This frequency response is based on the rational function approximated by vector fitting. Additionally, the characteristic admittance with vector fitting is shown in Fig. 4.

The step response of a cable modeled in Simulink for the case of a voltage drop is shown in Fig. 5: The test is performed with two voltage sources connected at the k and m sides of the cable. The source at k supplies power with a step voltage of 400.00 kV at 0.00 s, and the voltage source at m consumes the power with 399.08 kV. The currents at the k and m sides of the cable present a fast transient scoped in the small rectangle. This step

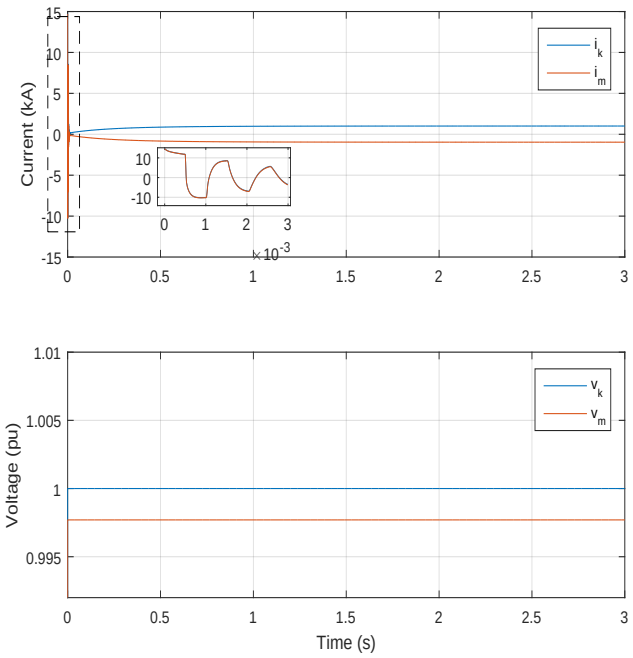

Fig. 5. Time response for the cable variables under a drop of voltage between terminals.

response at the initial part of the simulation presents a 15 kA maximum current. Finally, the steady state value sets to 1 kA for the sending current i_k.

IV. Power Hardware in the Loop Structure

Figure 6 shows the configuration of a PHiL system, with the link between the simulation environment and the physical equipment. The structure represents the connection of a real time (RT) simulator with a dashed blue rectangle, the physical system (with a dashed red rectangle) which is composed of a voltage source amplifier (V_o), a series resistor (R_p) and the device under test in this case a load impedance (Z_{Lo}). The communication and response time between subsystems are represented by the delay time τ_1 and τ_2. Additionally the voltage source amplifier controller is represented mathematically with a transfer function $F(s)$. In the RT-simulation the load is represented by a controlled current source, which is controlled with the measured current I_2 times the delay between the physical and the RT-simulator systems. The simulation system has an equivalent Thevenin circuit, with a source V_1 and the impedance Z_1. Additionally, the voltage produced in the simulation V_2 is used as reference for the physical voltage amplifier. The set of elements composed by $F(s)$ and the voltage amplifier forms the CVS. Therefore, the correct behaviour of this structure must be analyzed with the stability test. This stability is analyzed in subsection V-B.

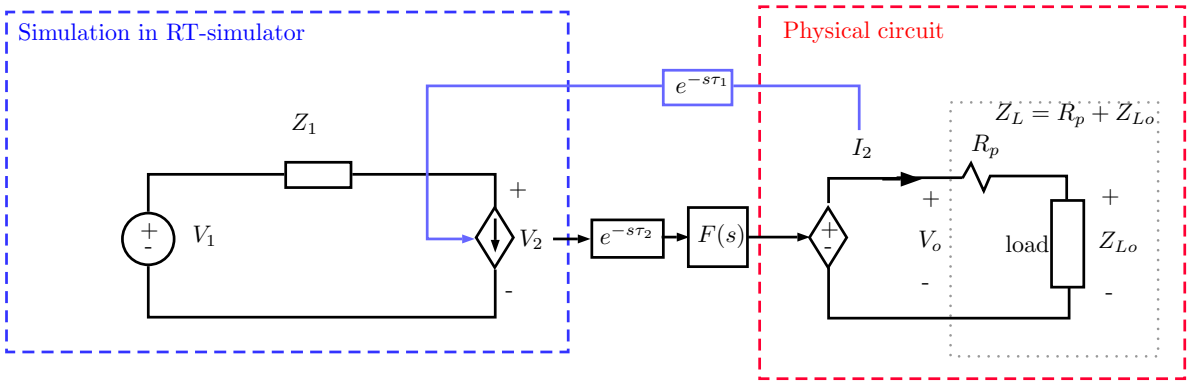

Fig. 6. PHiL general circuit.

V. Description of the PHIL structure to emulate the cable in the laboratory

The complete system for PHiL emulation is described with the block model shown in Fig. 7. The CVS has a BW of 20 kHz, four voltage amplifiers (Amp_x) are used to create the output voltage v_{ok} and v_{om}. Therefore, the practical implementation requires the use of the Thevenin equivalent highlighted with a dashed block for the cable model in Fig. 7 (i.e. Norton circuit model at sides k and m). The real time simulator (RT) is used to compute the output voltage based on the state space systems described above. In order to implement the full system, first some tests are necessary to take into account the delay between the RT and the CVS in the communication link. The following subsections present the simulation of the PHiL system taking into account the delays in the signals.

A. One side cable test with delay effects

This test is applied on a resistor load at side m as shown in Fig. 7. The system takes into account the delays of the communication link and the practical implementation of the Thevenin circuit. The practical Thevenin circuit requires the series resistor split in two parts, one part is used in the real time simulator and the remaining R_p is used as physical component in series with the load. This additional resistance is required to create a voltage drop between the CVS and the load in case a voltage controlled source is used to consume power. The voltage across R_p is compensated in the RT-simulation to minimize the error on v_m. Figure 7 shows the dashed blue rectangle that is used in the RT-simulation: it takes the measured current i_m as a load current controlled source. An ideal voltage source is used to supply power to the system.

Table I shows the parameters for the simulation of the PHiL with one side of the cable emulated with the CVS. The test uses an input voltage v_k reaching steady state at 400 V. Following, at 1 s, an 1 V step is applied. The sequence mentioned above avoids over-currents and protects the equipment at the initialization. Three different sampling periods are used for the RT-simulator ($T_{s,RT}$) to analyze the effects of the delay introduced in the system by the communications between the RT-simulator and the CVS. The corresponding performance is shown in Fig. 8: the tests present the ideal simulation with a sampling period of 10 μs, and the effect of the three delays (between 10 and 50 μs). The simulation of the PHiL system with delays has sampling period T_{main}. The simulation shows the preservation of the oscillation of the transient signal for the three sampling periods. However, the use of 50 μs sampling period for $T_{s,RT}$ leads to a delay in the time response with respect to the response with $T_{s,RT}$ =10 μs. The system results indicate marginal differences between the ideal simulation $i_{m,ideal10}$ and the simulation with delays when a sampling time of 10 μs is used ($i_{m,10}$).

TABLE I
Partameters simulation of the PHiL system.

Parameter	Value [units]
$T_{s,RT}$	50/25/10 [μs]
T_{main}	1 [μs]
R_p	350 [mΩ]
R_{load}	100 [Ω]
v_k	400 [V]

B. Stability of the one side cable emulation

The PHiL system used to emulate the cable is shown in Fig. 6. This system forms a closed loop system with input V_1 and output I_2. Moreover, the stability requirements allow the system to operate with physical stable current. The closed loop transfer function is as follows:

$$\frac{I_2(s)}{V_1(s)} = \frac{F(s)e^{-s\tau_2}}{F(s)e^{-s\tau_T}Z_1(s) + Z_L(s)} \tag{26}$$

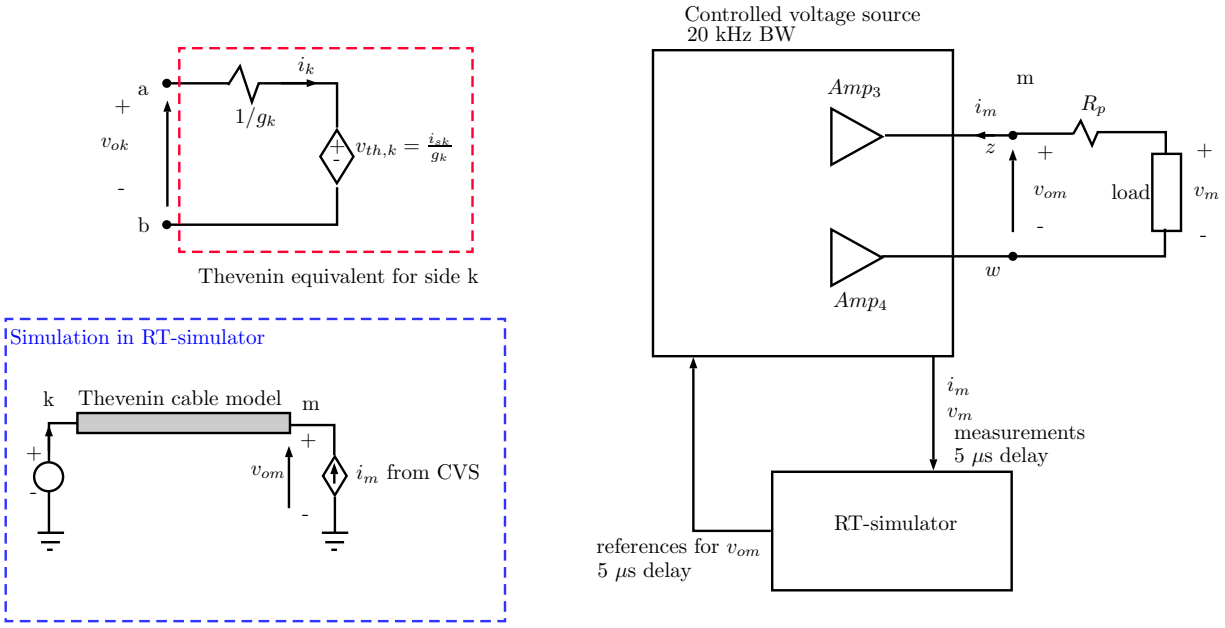

Fig. 7. Blocks representation of the PHIL system at m side.

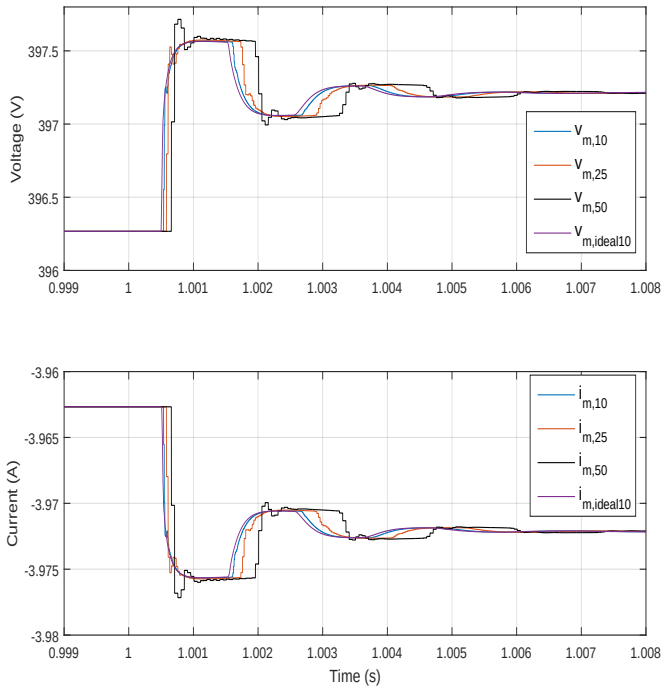

Fig. 8. Time response simulation of the half cable assuming multiple sampling times in the RT.

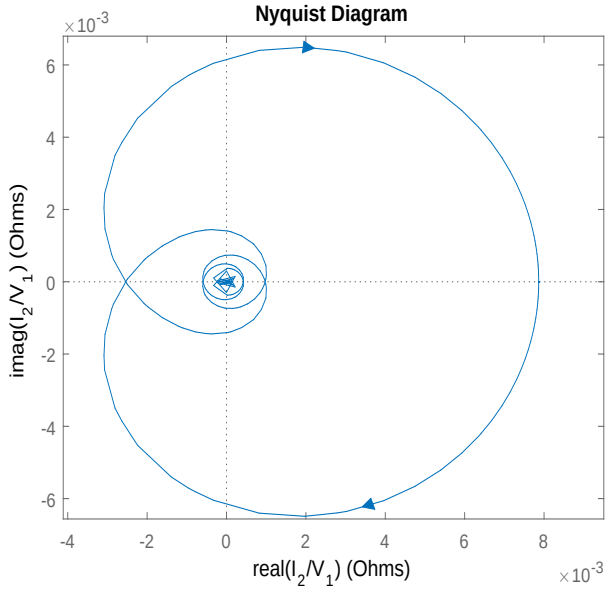

Fig. 9. Nyquist test for the PHiL general circuit.

where, I_2 is the current at the physical circuit, $V_1(s)$ is the input voltage at the simulation circuit. The system has some communication delays between the simulator and the measure point at the physical circuit. The delay from the measurement point to the simulator is τ_1 and from simulation to physical circuit is assumed as τ_2 and the sum of the delays is τ_T. The impedance at the simulation is $Z_1(s)$ and the physical load impedance is $Z_L(s)$. $F(s)$ is assumed as a first order transfer function of the physical voltage source with a limit cut-off frequency at 15 kHz, due to physical attenuation effects of the CVS below the 20 kHz.

Finally, the stability is studied with the Nyquist test of (26). The trajectory is shown in Fig. 9. It is observed that the trajectory does not cross the point $-1 + j0$, proving the stability of the system.

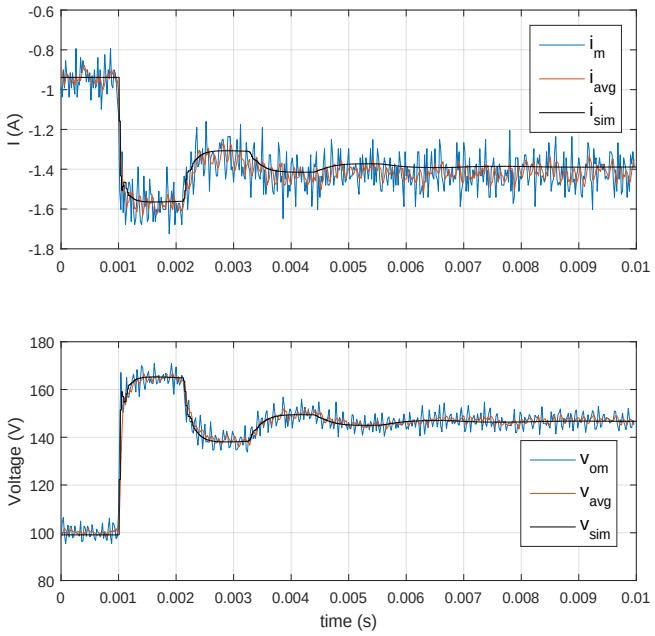

Fig. 10. Time response at the receiving side of the one side cable for the experimental test and the simulation. The sampling time is 20 μs

VI. Experimental results

Figure 10 shows the comparison of the experimental test and the simulation, with a load $Z_{Lo} = 105.6\ \Omega$. The measurements are i_m and v_{om}. The current i_{avg} and voltage v_{avg} signals of the receiving side are averaged values with a moving average filter of fourth order. The simulation current and voltage are i_{sim} and v_{sim}, respectively. A comparison of the simulation voltage and the measured voltage at the receiving side of the cable for this test is shown in Fig. 10. it is important to remark that the oscillation of the transient of the cable for a step change is preserved.

VII. Conclusions

Emulating the behaviour of long HVDC cables in a laboratory setting is quite challenging due to the inherent difficulties associated to their fast transient and their complex dynamics. This paper presented a Power Hardware in the Loop approach for emulating a dc cable where a Universal Line Model of the cable is simulated in real time. The paper presented first a stability assessment and an analysis of the impact of critical parameters as the time step of the real time simulation on the response of the PHiL configuration. This proves that the behaviour of a cable can be reproduced with sufficient accuracy with time steps in the range of a few tens of microseconds. An experimental demonstration with a controlled voltage source of 200 kVA with 20 kHz bandwidth combined with an OPAL-RT platform is then presented proving the validity and the feasibility of the proposed approach. Future work will be focused on reducing signal noise and extending the approach to a two sided cable model.

VIII. Aknowledgment

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