Noise Transfer Functions and Loop Filters Especially Suited for Noise-Shaping SAR ADCs

Harald Garvik, Carsten Wulff and Trond Ytterdal
Dept. of Electronics and Telecommunications, Norwegian University of Science and Technology (NTNU)
Trondheim, Norway

***Abstract*—Oversampling and noise-shaping have in recent years been introduced to SAR ADCs to improve the conversion accuracy. Similar to delta-sigma ADCs, this is done by means of a feedback loop containing a loop filter. In this paper, the high-level design of this loop filter is discussed, and important differences to classical delta-sigma loop filter design are pointed out. Among others, it is found that the poles of the noise transfer function, and not only the zeros, play a significant role on the conversion accuracy. Based on this, a new loop filter topology with four poles and two zeros is proposed and compared to existing loop filters. This reveals that the proposed loop filter can yield more energy-efficient noise-shaping SAR ADCs than the ones seen in the literature today.**

I. Introduction

In recent years, the most energy effective ADCs reported in the literature have been of the Successive Approximation Register (SAR) type [1]. SAR ADCs are relatively simple circuits, and only consist of a capacitive DAC, a comparator, and a digital circuit. Due to this, their energy efficiency scales well with technology as long as the target conversion accuracy is relatively low. When the conversion accuracy is increased, however, it becomes more difficult to achieve the same premium energy efficiency due to thermal noise and mismatch concerns. Different additions to the basic SAR circuit have been reported in the literature to mitigate problems like this, and an example is noise-shaping SAR ADCs (NS-SARs), reported in [2], [3], among others. The main idea of an NS-SAR is to increase the conversion accuracy by introducing oversampling and noise-shaping to the circuit, like in a delta-sigma converter. Most importantly, this noise-shapes both the quantization noise as well as the comparator circuit noise of the ADC such that it is not necessary to increase the comparator accuracy to that of the whole NS-SAR [2].

In the coverage of NS-SARs in the literature so far, an elaborate treatment of their high level design seems to be lacking. Among others, there exist open questions related to both the optimum choice of loop filter topology, and the design of the noise transfer function (NTF). In this paper, we therefore aim to advance the art of high level NS-SAR design by exploring and proposing suitable NTF design techniques, and by introducing a new loop filter topology especially suited for NS-SARs. To be able to do this conveniently, a general NS-SAR is introduced in section II, such that loop filter discussions throughout the paper can be done in terms of this. The discussion of NTF design for NS-SARs then follows in section III. Most importantly, the effect of the NTF poles are considered, and it is shown how they usually can be utilized to increase the conversion accuracy. This is in contrast to classical delta-sigma ADCs, where the NTF poles must often be used to stabilize the loop rather than increasing the performance. This observation suggests that the accuracy of NS-SARs can be increased by adding more poles to the loop filter, such as already done in the cascaded FIR-IIR filter in [2], realizing one zero and two poles. Based on this finding, the loop filter topology proposed in section IV of this paper realizes four poles in addition to two optimally placed zeros. Behavioral simulations presented in section V demonstrate that this increases the performance substantially, both compared to the filter in [2] and to a standard second order loop filter.

II. A general noise-shaping SAR

The general NS-SAR used in this paper is shown in figure 1. It differs from a normal SAR by an extra comparator input, connected to a filtered version of the DAC voltage v_{res}. The discrete time loop filter $H(z)$ used for this is clocked by a signal DONE, which triggers each time the SAR has finished a conversion. This means that only final versions of v_{res} will be sampled by the loop filter, and for a conversion n we denote such a sample as $v_{res}(n)$. The filter output in discrete time domain thus follows as $v_{res}(n) * h(n)$, where $h(n)$ is the impulse response corresponding to $H(z)$. By taking this into account when analyzing the SAR circuit, the output is obtained as[1]

$$D_{out}(n) = v_{in}(n) - v_{res}(n) * h(n) + v_q(n) \tag{1}$$

That is, the value $-v_{res}(n) * h(n)$ is added to the conversion due to the extra comparator input. $v_q(n)$ is the current quantization error, and its magnitude is bounded by the number of bits B in the SAR, like in a normal SAR ADC. It should also be noted that the loop filter must be delaying to yield a realizable system, since a conversion n will otherwise depend on $v_{res}(n)$, which is not available until after the conversion.

If we now assume that the result of the last SAR bit-cycle decision is also fed back to the DAC (this is a requirement to obtain noise-shaping), the final DAC voltage after each conversion will be

$$v_{res}(n) = D_{out}(n) - v_{in}(n) \tag{2}$$

By substituting this expression into equation (1), taking the z-transform and rearranging, we obtain

$$D_{out}(z) = v_{in}(z) + \frac{1}{1 + H(z)} v_q(z) \tag{3}$$

[1] D_{out} is treated as a quantity having units of volts, as is often common in ADC analysis. This is also done in the rest of the paper.

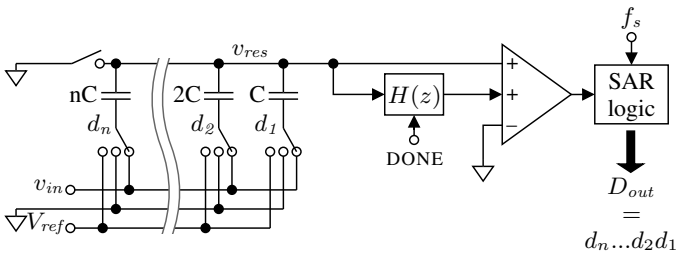

Fig. 1. The introduced general noise-shaping SAR ADC

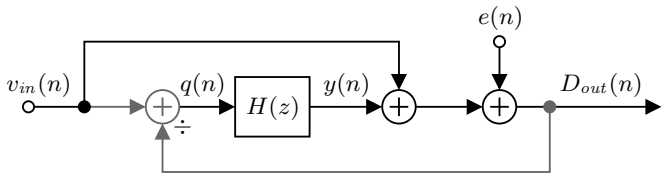

Fig. 2. Linear model for the general NS-SAR. The grey lines represent logical signal flow that does not exist as physical electrical signals.

The quantization error is thus shaped by a general transfer function $1/(1+H(z))$, which can be designed by selecting an appropriate loop filter.

We can now make a linear model of the general NS-SAR by replacing the quantization error in equation (1) with an independent white noise source $e(n)$, and then use this equation together with equation (2) to draw a signal flow schematic. The result is shown in figure 2, where the signals $y(n)$ and $q(n) = -v_{res}(n)$ have been introduced to represent the loop filter output and input. It should be noted that the source $e(n)$ can be used to represent comparator circuit noise in addition to quantization noise, because these noise contributions enter the system at the same place in the signal flow. The paths in the model that was drawn with help from equation 2 are colored grey, and it is important to realize that these represent *logical* signal flow in the system, and not actual electrical signal paths. We see that one of the results is that the analog version of $D_{out}(n)$ does not need to exist within the circuit, and there is therefore no need for an extra DAC to generate it. This is true because the SAR DAC doubles as the feedback DAC and generates $q(n)$ directly during the normal conversion process. This is a significant advantage of NS-SARs, since a normal multi-bit delta-sigma modulator will require one or more multi-bit DACs in the system.

By analysis of the model, we find that the signal transfer function is unity, and that the noise transfer function is

$$\text{NTF}(z) = \frac{D_{out}(z)}{e(z)} = \frac{1}{1+H(z)} \tag{4}$$

This is in accordance to equation (3). The unity STF of the ADC exists because of the input feed-forward path in figure 2, and makes the NS-SAR equivalent to a low-distortion delta-sigma modulator [4]. In such delta-sigma modulators, the input signal does not enter the loop filter, and its maximum voltage swing is therefore only set by the power of $e(n)$. Since an NS-SAR employs multi-bit quantization, $e(n)$ is small compared to the input signal, and the loop filter will therefore only need to handle small voltage swings.

It is important to mention that there are NS-SARs in the literature ([3] among others) that do not fit into the scheme of the general NS-SAR introduced in this paper. These converters employ feedback from v_{res} to the input of the whole ADC, and do in this way inherently realize integration. Although this is advantageous, a large share of the circuit blocks in the ADC will take part in the integration feedback loop, and thus have to be carefully designed to keep the integrator leakage acceptable. This is similar to error-feedback delta-sigma ADCs, which are also difficult to design in practice [5, Ch. 3]. Consequently, the general NS-SAR in this paper is made in accordance to the more robust structure used in [2], where integrators have to reside inside the loop filter, and thus have their leakage determined by the DC gain of their gain elements.

III. NTF DESIGN FOR NS-SARS

The principal goals of NTF design for NS-SARs are similar as for delta-sigma converters. That is, the NTF should have as much attenuation as possible inside the signal band, such that in-band noise becomes efficiently suppressed. Additionally, the maximum out-of-band gain of the NTF cannot be chosen too high, as this will lead to signal saturation at different points in the system (e.g. the quantizer/SAR or an integrator) due to high internal signal levels. This again leads to an unstable noise-shaping loop. These two goals are somewhat conflicting, since a decrease of maximum out-of-band gain often impacts the in-band attenuation.

Because of the similarity to delta-sigma converters, it is possible to use existing design techniques to design the NTF of NS-SARs. The zeros can thus be placed at DC, or optionally at other locations inside the signal band, for instance the optimal ones proposed in [6]. Pole placement for delta-sigma converters is more open, and both "design by hand" and software-based approaches exists; See for example [5, Ch. 4 and 8]. It is nevertheless well established that it is the poles that primarily affect the stability of the ADC, since they have a big impact on the out-of-band gain. Therefore, it can probably be said that the poles are most often used as a "stabilizing tool" in delta-sigma converters.

One pole placement method named CLANS is presented in [7], and considers the task as a constrained optimization problem where the objective is to maximize the in-band NTF attenuation. The optimization is done subject to a stability criterion, derived in the same paper. This can be written as

$$V_{in,\text{p-p},max} + \underbrace{\Delta\left(\sum_{i=0}^{\infty}|ntf(i)| - 1\right)}_{Y_{\text{p-p},max}} \leq \text{FSR} \tag{5}$$

and states that the input to the quantizer/SAR (the rightmost summer in figure 2), constituted by the sum of $v_{in}(n)$ and the loop filter output $y(n)$, should never exceed the SAR full scale range, FSR. It is furthermore assumed that the ADC will remain stable if this is fulfilled. This makes sense since the SAR itself is the block in the system that processes the largest signals, and will thus probably saturate first. The expression derived for $Y_{\text{p-p},max}$ is a theoretical upper bound, expressed by the NTF impulse response $ntf(n)$, and the spacing Δ between two adjacent output levels of the SAR. When the optimization is run, both $V_{in,\text{p-p},max}$, Δ, and FSR must be given.

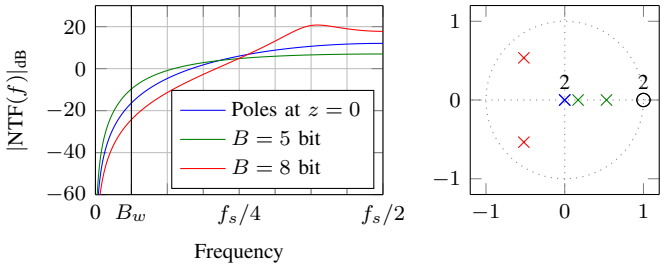

Fig. 3. NTF frequency response and pole-zero plot for NS-SARs having two zeros and two CLANS-placed poles in the NTF, and different number of bits in the SAR. Compared to a 2. order differentiator NTF. All zeros are located at DC, OSR = 8, and $V_{in,\text{p-p},max} = 0.9$.

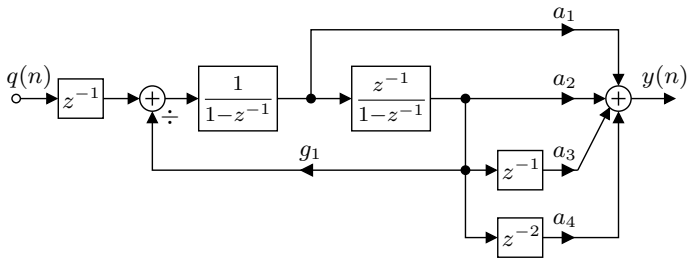

Fig. 4. The proposed loop filter. Realizes a NTF with two zeros and four poles.

Figure 3 shows the resulting frequency response and pole/zero map after some CLANS runs for a NTF having two zeros placed at DC, and two poles whose locations are determined by the optimization. $V_{in,\text{p-p},max}$ was set to 0.9. Also, a reference case where the poles are placed at $z = 0$ is included, resulting in the simple "differentiator" transfer function $\text{NTF}(z) = (1 - z^{-1})^2$. For the two CLANS runs, the number of bits B in the SAR is varied, and this in turn changes the value of Δ, which is inversely proportional to B. For $B = 5$, we see that the optimizer has to pick pole placements that lowers the maximum NTF gain to stabilize the ADC, and that this impacts the in-band attenuation, compared to the reference case. However, when B is increased to 8, a different situation arises. The optimizer is now allowed to pick pole placements yielding much higher maximum NTF gain, and this improves the the in-band attenuation significantly, compared to both $B = 5$ and the reference case. The function of the poles now is thus to increase the accuracy of the ADC, rather than just stabilizing it. This observation is very important for NS-SAR NTF design, since it is convenient to have, say, 8-9 bits in a SAR. This is in contrast to delta-sigma ADCs utilizing flash quantizers, where such bit counts are not easily realized. All in all, this suggests that optimal pole placement is crucial to maximize the performance of NS-SARs, and that poles can have a significant impact on the in-band attenuation.

IV. A Loop Filter Specially Suited for NS-SARs

The observations from the previous section hint that the accuracy of an NS-SAR can be increased by adding extra poles to the NTF, and not only extra zeros. This is attractive, because extra poles in the NTF can be realized by adding passive feed-forward paths in the loop filter, and the ADC accuracy can thus be improved in a more energy efficient manner. Based on this, we propose a filter topology especially suited for NS-SARs. The filter is depicted in figure 4, and is constituted by a resonator having extra feed-forward paths at the output. By analysis of the signal schematic and through the use of equation 4, we obtain the resulting NTF as

$$\text{NTF}(z) = \frac{1 + (g_1 - 2)z^{-1} + z^{-2}}{1 + (g_1 + a_1 - 2)z^{-1} + (a_2 - a_1 + 1)z^{-2} + a_3 z^{-3} + a_4 z^{-4}} \quad (6)$$

This NTF has a second order numerator and forth order denominator, and hence two zeros and four poles. The poles can be chosen arbitrarily by selecting values for a_{1-4}, while the zero locations can be adjusted by g_1. This coefficient is present because of the resonator feedback path, and the zero pair can be moved along the unit circle by its adjustment.

It is the extra feed-forward paths near the filter output that realizes the extra NTF poles. To implement these passively, one can sample the resonator output onto capacitors in a bank, and then use samples from this bank each clock cycle to generate the output in a capacitive summing circuit. This will more or less only increase the power consumption by increased clocking complexity, and the whole filter will therefore not use much more power than the resonator alone. It should also be noted that the circuit noise originating from the last integrator will be noise-shaped by the first one, and its size can therefore be reduced. Due to all this, it should be possible to conclude that a good circuit implementation of the proposed filter will use less than twice the power of the first integrator.

V. Comparisons by Behavioral Simulations

In order to verify the performance of the proposed filter compared to others, behavioral simulations have been conducted in Matlab. In these simulations, a loop filter is represented as a state-space model, and input into to a behavioral model of the general NS-SAR. The comparator in this model is noisy, and the noise power is set equal to the quantization noise (i.e. a 10-bit SAR will have an ENOB of 9.5). To conduct the actual simulation, the model is evaluated in the discrete time domain for an input sinusoid, and an ENOB value is finally obtained by taking FFT of the resulting output. The loop filter state-space model contains the filter coefficients, and these have to be calculated from the NTF poles and zeros prior to simulation. The NTF itself thus needs to be synthesized. This is done by using CLANS for the poles, while the zeros are simply set to DC for filters not having a resonator, and to the optimum locations found in [6] when a resonator is present.

To gain insight into the loop filter performance, it is needed to do sweeps in the design space by varying the OSR and/or the number of bits B. Each time one of these variables are changed, it is also important to re-run CLANS, as the optimizer will now be faced with a new situation. Note that $V_{in,\text{p-p},max}$ in equation (5) have to be chosen in order to run CLANS. This choice is not trivial, because very high values inhibit the choice of the best pole locations, and low values affect the performance because of low signal power. Therefore, this variable is swept in each simulated design point, and the best value used. One should also have in mind that the aim of the behavioral simulations in this paper is to show the

noise-shaping performance, and comparator thermal noise and quantization error are therefore the only error mechanisms that are modeled. This yields plots where the loop filter performance becomes clear, but it is important to remember that for example mismatch in the SAR DAC must be at acceptable levels in practical implementations.

In figure 5, NS-SARs having various filters are simulated for different values of B, while the OSR is held constant at 4. The proposed filter is included in both its presented version, a version of it not having the resonator feedback path, in addition to a version where the extra feed forward paths are also removed (i.e. $a_{3-4} = 0$). This last version only leaves two freely selectable poles and two zeros at DC, and can therefore be viewed as a "normal" second order loop filter. The versions of the proposed filter are compared against the cascaded FIR-IIR filter (1 zero at DC, 2 poles) from [2], and a theoretical NS-SAR having the second order differentiator NTF $(1-z^{-1})^2$ and a full-scale input signal. The plot shows that all the real NS-SARs have better performance than this theoretical one as B is increased to 6, and the NTF poles are thus used to boost the accuracy of the ADCs, rather than just keeping them stable.

When it comes to the performance difference between the different filters, we see that the advantage of going from the filter of [2] to a filter having two zeros at DC and two poles is quite modest (around a half bit at high B) at the selected OSR of 4. Since the last mentioned also contains one more integrator, it will have a higher power consumption that is probably difficult to justify. When the extra feed-forward paths and the resonator feedback are added to yield the proposed filter, the situation betters, and a large performance increase is achieved. This comes without any significant increase in power consumption, as discussed in section IV. Consider for instance $B = 7$, yielding 10 bit ENOB for the filter from [2], and 12 bit for the proposed filter. This is a large increase in accuracy, and as the first mentioned filter also has an active integrator, we can assume that the upgrade less than doubles the filter power consumption. The proposed loop filter is thus clearly favorable in terms of energy efficiency.

In figure 6, ENOB is plotted against OSR, while B is held at 8. This reveals that it is still the number of zeros that determines the rate of performance increase as the OSR is adjusted. This means that for very high OSR, the number of zeros are still most important, while the absolute performance enhancements realized by the poles and the resonator can be very significant for low OSR. This further shows how important it is to fully utilize these design techniques in NS-SARs, where low OSR is typically used.

VI. Conclusion

This paper has discussed high level NTF and loop filter design for noise-shaping SARs. In order to do this, a NS-SAR having a general loop filter was introduced, and its linear model was presented. NTF design for the NS-SAR was then discussed, and evidence suggesting that the poles of the NTF can be used to boost the conversion accuracy if B is sufficiently high was presented. Based on this, a loop filter having four poles and a complex conjugated zero pair was proposed, and it was postulated that its power consumption should be less than twice that of a single integrator. In behavioral simulations, the proposed filter performed considerably better than the other ones evaluated, and the significance of both the extra poles and the resonator path was demonstrated.

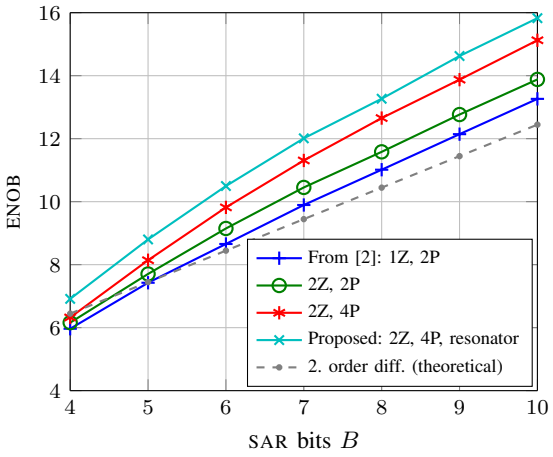

Fig. 5. ENOB achieved in behavioral simulations of NS-SARs having different loop filters, OSR of 4, and plotted against number of SAR bits. The theoretical ENOB of a 2. order differentiator modulator is also included.

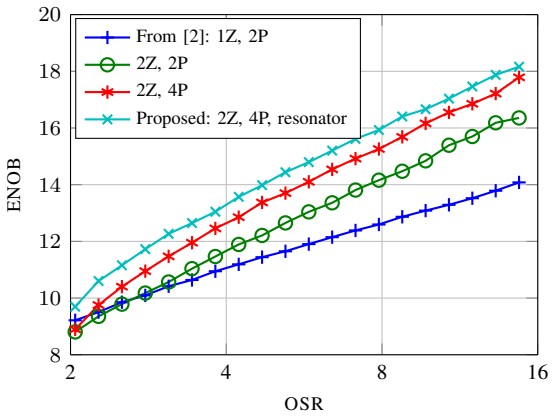

Fig. 6. ENOB achieved in behavioral simulations for NS-SARs having different loop filters, 8 bits in the SAR, and plotted against OSR.

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