Suggested Methods for Preventing Core Saturation Instability in HVDC Transmission Systems

Ian Norheim,
Norwegian University of Science and Technology
Faculty of Information Technology, Mathematics, and Electrical Engineering
N-7491 TRONDHEIM, NORWAY

February 18, 2002

URN:NBN:no-2111

URN:NBN:no-2111

Acknowledgements

This thesis was carried out under the supervision of Professor Tore M. Undeland, The Department of Electrical Power Engineering, Norwegian University of Science and Technology. I want to thank him for his valuable help during my work. I also appreciate that he allowed me to travel quite a lot during my work.

I would also like to thank Magnar Hernes and Thor Henriksen at SINTEF Energy Research for their good advice in the areas of power electronics and transformers.

I also appreciate the advice during the English editing of this thesis given by Stewart Clark at the Norwegian University of Science and Technology.

Several friends have also been a great help for me as I have worked on this thesis. Especially, I want to thank the Hauglands for their great support in the time before and after my mother passed away.

My wife Hilde has been a great encouragement and comforter to me as I have worked my way steadily through this thesis. I am deeply grateful to her.

Trondheim, February 2002

Ian Norheim

URN:NBN:no-2111

Summary

In this thesis a study of the HVDC related phenomenon core saturation instability and methods to prevent this phenomenon is performed. It is reason to believe that this phenomenon caused disconnection of the Skagerrak HVDC link 10 August 1993. Internationally, core saturation instability has been reported at several HVDC schemes and thorough complex studies of the phenomenon has been performed. This thesis gives a detailed description of the phenomenon and suggest some interesting methods to prevent the development of it.

Core saturation instability and its consequences can be described in a simplified way as follows:

It is now assumed that a fundamental harmonic component is present in the DC side current. Due to the coupling between the AC side and the DC side of the HVDC converter, a subsequent second harmonic positive-sequence current and DC currents will be generated on the AC side. The DC currents will cause saturation in the converter transformers. This will cause the magnetizing current to also have a second harmonic positive-sequence component. If a high second harmonic impedance is seen from the commutation bus, a high positive-sequence second harmonic component will be present in the commutation voltages. This will result in a relatively high fundamental frequency component in the DC side voltage. If the fundamental frequency impedance at the DC side is relatively low the fundamental component in the DC side current may become larger than it originally was. In addition the HVDC control system may contribute to the fundamental frequency component in the DC side voltage, and in this way cause a system even more sensitive to core saturation instability. The large magnetizing currents that eventually will flow on the AC side cause large zero-sequence currents in the neutral conductors of the AC transmission lines connected to the HVDC link. This may result in disconnection of the lines. Alternatively, the harmonics in the large magnetizing currents may cause overheating of filters or other components. This may also cause disconnection.

In this thesis, several ways to reduce/eliminate the core saturation instability problem are described and most of them are also demonstrated by simulations on a modified CIGRE HVDC benchmark model in PSCAD/EMTDC version 3. PSCAD/EMTDC version 3 is a powerful simulation tool which perform simulations in the time domain and offers detailed models for transformers, power electronic switches etc. To understand and have confidence in the simulation results, the transformer models, the model for the on-line frequency scanner, and models for power electronic switches are evaluated in detail.

The suggested initiatives that were successfully simulated are listed below:

1) Stabilizing loops in the control system of the HVDC link.

These loops diminish the influence of the HVDC control system on core saturation instability. Some of the loops suggested are believed to give improvements in applications where it is required that the stabilizing loop are only active for a small band of frequencies.

URN:NBN:no-2111

2) A hybrid shunt filter connected to the commutation bus on the AC side.

The hybrid filter consists of a PWM converter in addition to a passive circuit of components. It is superior to the plain passive filter because it does not cause any resonances with the AC grid and because it is not as sensitive to component drifting as passive filters. The hybrid filter prevents most of the second harmonic current generated by the HVDC converter to flow into the AC grid. This way the second harmonic component in the commutation voltages is significantly decreased.

3) A passive shunt filter connected to the commutation bus on the AC side.

Functions the same way as the hybrid shunt filter, but it may create resonances with the AC net. In addition it is more sensitive for changes in the component values than the hybrid filter.

4) A blocking LC filter between the low voltage potential and earth on the DC side

This filter blocks any fundamental frequency current from flowing on the DC side at the same time as it allows the DC component in the DC side current to flow through it. By placing the filter between the low voltage potential and earth on the DC side it does not have to sustain the DC side voltage.

It is 1) that represent the most preferable solution. It does not introduce any new components in the AC or DC grid, and it is inexpensive compared to the other solutions. The solutions in 2), 3), and 4) requires large and expensive components. However, it might be that in future schemes hybrid filters replaces passive filters on the AC side. Then it might be inexpensive and convenient to use the hybrid filters to prevent core saturation instability.

URN:NBN:no-2111

URN:NBN:no-2111

URN:NBN:no-2111

1 Introduction

This thesis focuses on an HVDC-related phenomenon called core saturation instability. The motivation for this is the problems Statnett (the Norwegian transmission system operator) has experienced on the Skagerrak HVDC link. Also internationally, several incidences of core saturation instability have been reported [12, p.180]. The aim of this thesis is to give a simple but detailed description of the phenomenon, and on the basis of this suggest methods that may prevent these occurrences.

The Skagerrak HVDC link connects the power systems in Denmark and Norway. It consists of three cables and is able to transfer about 1000 MW across the Skagerrak. On 10 August 1993 the Skagerrak HVDC link was disconnected twice. The first time the Kristiansand-Arendal AC line feeding the Norwegian station in Kristiansand failed due to the switching in of a 400 kV shunt reactor in the Danish station Tjele. It was the earth fault protection that tripped the line. As the HVDC link was disconnected transient recorders were started. The recordings showed a 35 A, 50 Hz current superimposed on the DC current flowing across Skagerrak. Later on the day an identical trip occurred but without any relation to any known event. The measured 35 A, 50 Hz current on the DC side and the disconnection because of large zero-sequence currents gives reason to believe that the problems were rooted in a phenomenon experienced in the operation of different HVDC links around the world. This phenomenon is termed core saturation instability [1]. An effort has been made by Statnett to recreate the incidents at the Skagerrak HVDC link 10 August 1993 in the simulation program PSCAD/EMTDC version 2. However, this was not successful.

In this thesis a study of core saturation is performed. To do this it is necessary to have a theoretic understanding of HVDC transmission. This is why Chapter 2 is about theory on HVDC transmission. In Chapter 3 the different factors that interact to create the phenomenon and the implications of it are described theoretically. Methods to decrease the probability of the phenomenon occurring are suggested in Chapter 4.

A simulation program, PSCAD/EMTDC version 3, has been used to simulate core saturation instability and the suggested initiatives to prevent it. Core saturation instability is a phenomenon that requires a strong time domain simulation tool with good models for switches, transformers, and control systems. Chapter 5 focuses on certain models used in PSCAD/EMTDC that are important in order to achieve successful simulation of core saturation instability and the methods that are proposed to prevent it.

The CIGRE HVDC benchmark model [26] has been used as a starting point for the simulations. It was necessary to make some modifications to this model in order to simulate core saturation instability and initiatives to prevent it. These issues are covered in Chapter 6.

In Chapter 7 it is verified by simulations that the different methods that are suggested in Chapter 4 to prevent core saturation instability really work. The models of the control systems or components used to eliminate core saturation instability are described in detail.

The conclusions of the thesis are in Chapter 8.

The appendices contain data used in the CIGRE HVDC benchmark model, simulation results and a report written for a seminar held by Norsk Elektroteknisk Forening in November 2000.

2 Theory about HVDC transmission

This chapter considers how an HVDC transmission is built up, how it works and how it is controlled. To put HVDC transmission into a context, it is also explained why and in which cases it is used.

2.1 Advantages of HVDC transmission

Historically the availability of transformers, the advent of the steam turbine as a prime mover for the generation of power, and the development of induction motors have favoured AC transmission [2]. This is why the power systems around the world are mainly AC systems. However, there are cases where HVDC transmission are necessary or preferable. In the following some elements that are positive with HVDC transmission are mentioned.

1) In the case of transmitting large amounts of power across large bodies of water it is a necessity to use HVDC transmission. Long AC cables will require too much current to charge their large capacitance. When transferring a DC current in a cable, the capacitance of the cable has no influence on the current.

2) When transferring DC the lines require no reactive compensation. However, when transferring AC there is a need for series or shunt compensation to reduce the voltage drops and line losses.

3) When transferring DC there are no skin effects in the lines. Thus, the use of the conductor cross section is better than when transferring AC. The earth impedance is also low for DC.

4) HVDC transmission can make connection between power systems that are not synchronized or operate at different frequencies possible.

5) The fast control of HVDC links makes it possible to use an HVDC link to improve the stability in the interconnected AC systems.

6) AC interconnections always reduce the overall system impedance and in this way cause an increase in the short circuit levels. The capability of existing circuit breakers may be exceeded. This is avoided with an HVDC interconnection.

7) The DC voltage on the DC line is the effective voltage. For AC lines the effective voltage is $1/\sqrt{2}$ times the peak AC voltage. Thus, more DC power can be transmitted if the AC line and DC line have the same insulation level.

8) Less conductors are required in DC transmission than in AC transmission.

The negative aspect of using HVDC transmission is the high cost of the converter stations. However, DC lines are less expensive to build than AC lines (see points 3 and 8 above). Therefore there will be a break-even distance where the cost of building AC transmission is equal to the cost of building DC transmission. Figure 2.1 shows the relation between the transferred power and the break-even distance.

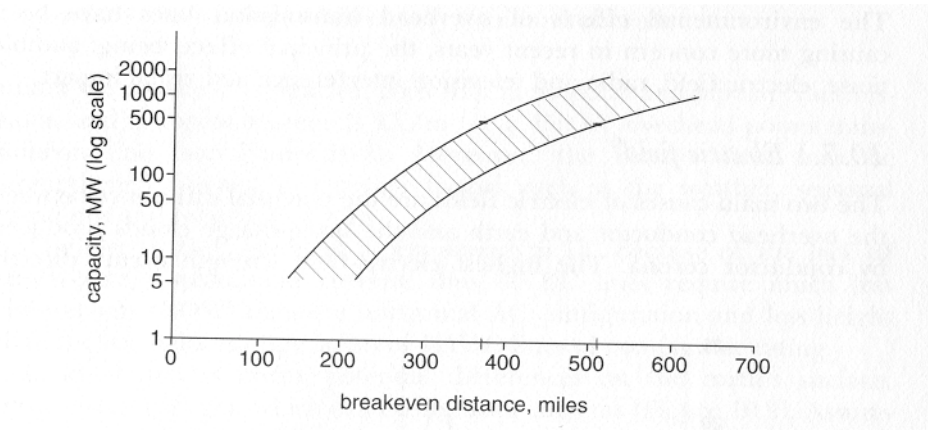


Figure 2.1 Break-even distance for HVDC transmission and AC transmission [2]

One can conclude from Figure 2.1 that HVDC lines are favourable to use when the distance between the produced electricity and the load centre are very far. There are several examples of HVDC links being used to feed load centres from distant generators. In India for instance, an HVDC link is used to transfer bulk power from Rihand-Singrauli thermal power generating complex to the load centre around Delhi [2,p.93]. The nominal power is 1500 MW and it is transferred over a distance of 814 km at ±500 kV.

If one or more submarine or underground cables are used for the transmission, the break-even distance is much less than when overhead lines are used. AC cable systems that are longer than 50 km are not practical to consider, while DC cable systems might be used for distances of more than 600 km [3]. Therefore, in the cases where the only alternative is to transport the power in long cables, HVDC transmission must be used. An example of an HVDC link using submarine cables is the Skagerrak link between Norway and Denmark. The Skagerrak link has three converter stations that provide up to 1000 MW. The three submarine cables are about 130 km.

HVDC is the obvious option if it is desirable to connect power systems with different frequencies or power systems which are not synchronized. The Sakuma interconnection in Japan connects a 50 Hz and a 60 Hz power system. It is a back-to-back interconnection that interchange up to 300 MW at ±125 kV. The intention of the link was to improve the stability in the power systems and to transfer power between the systems [2].

2.2 Principles of HVDC transmission

The aim of this section is to give an basic understanding of how an HVDC link operates. Topics which are considered are:

- Rectifier operation
- Inverter operation
- Control systems
- Harmonics
- Filtering

URN:NBN:no-2111

2.2.1 Typical HVDC schemes

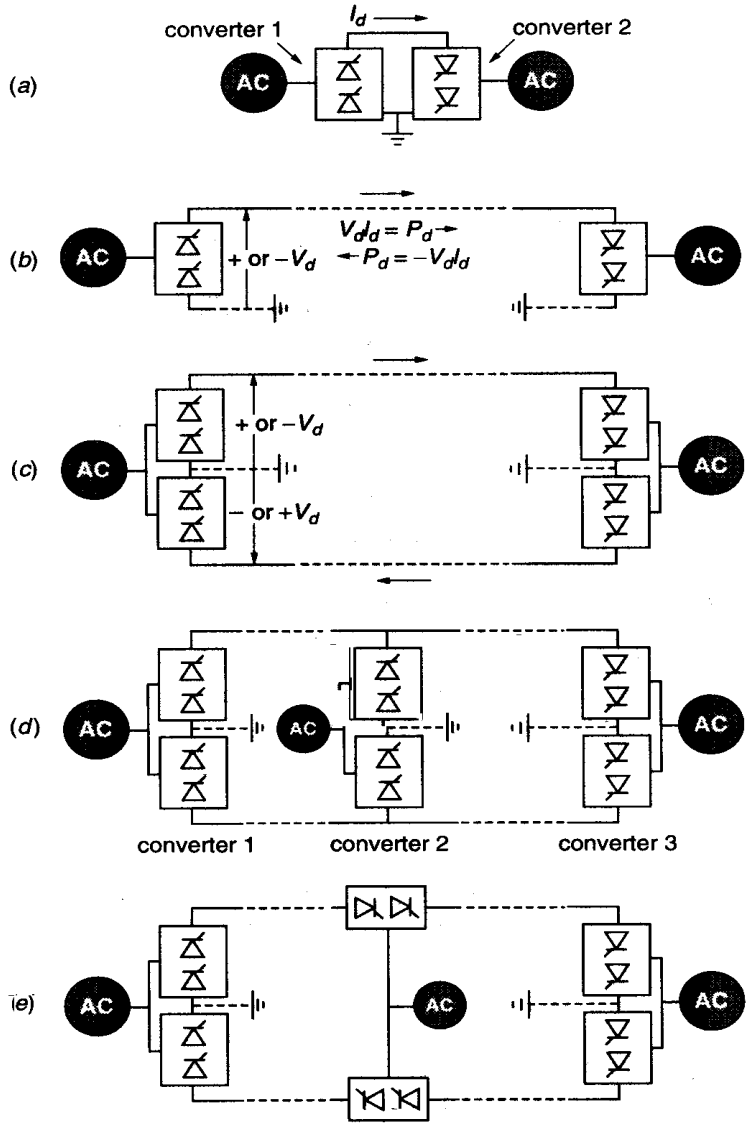


Figure 2.2 Basic HVDC transmission configuration [2].

Figure 2.2 a) shows the back-to-back interconnection. The two twelve-pulse thyristor converters are built on the same site and there are no transmission lines between them. The back-to-back interconnection may be used to interconnect AC grids with different frequencies.

The monopolar link in Figure 2.2 b) consists of two twelve-pulse thyristor converters which are joined by a single conductor line. The earth or the sea is used as the return conductor. This requires two electrodes that are able to carry the full current in the HVDC link. In this thesis the simulations and studies are done on a monopolar link. This saves time when simulating (simulating on a more complex system like a bipolar link would have required longer simulation time) and is sufficient to make a study of core saturation instability and methods to prevent it.

Figure 2.2 c) shows the bipolar link. The bipolar link consists of two monopolar link combined such that one has positive and the other negative polarity with respect to earth. When the two monopolar systems have equal current they cancel each other's earth currents to zero. Thus, the earth conductor is only used when one pole is temporarily out of service.

Figure 2.2 d) and e) shows two cases of multiterminal HVDC transmission. If converter 1 and 2 in Figure 2.2 d) operate as rectifiers, then converter 3 must be operated as an inverter. The opposite of this is also the case. Mechanical switches are necessary to achieve other rectifier-inverter combination. The series connection in Figure 2.2 e) makes it possible to tap a smaller amount of the total line power without building the high cost parallel tapping alternative.

2.2.2 Converter operation

Since the models used for simulation of HVDC transmission in this thesis consists of thyristor converters, only this type of converter is analysed. Rectifiers/inverters using GTO/IGBT are under development. Schemes using force commutated switches and with rated power up to 300 MW are being built [4].

A 6-pulse thyristor converter is shown in Figure 2.3

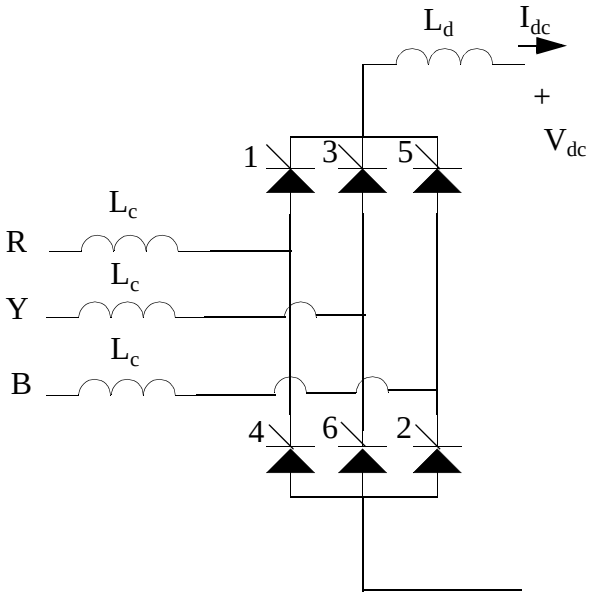


Figure 2.3 Three-phase thyristor converter

The firing angle is zero

To understand the three-phase bridge it is an advantage to start with the ideal case where the bridge is connected to an infinitely strong power system, and diode operation of the bridge. It is also assumed that L_d is very large, so that it is justified that the DC current is constant. Under these conditions the commutation is instantaneous. Figure 2.4 shows the switching sequence and the rectified voltage waveform.

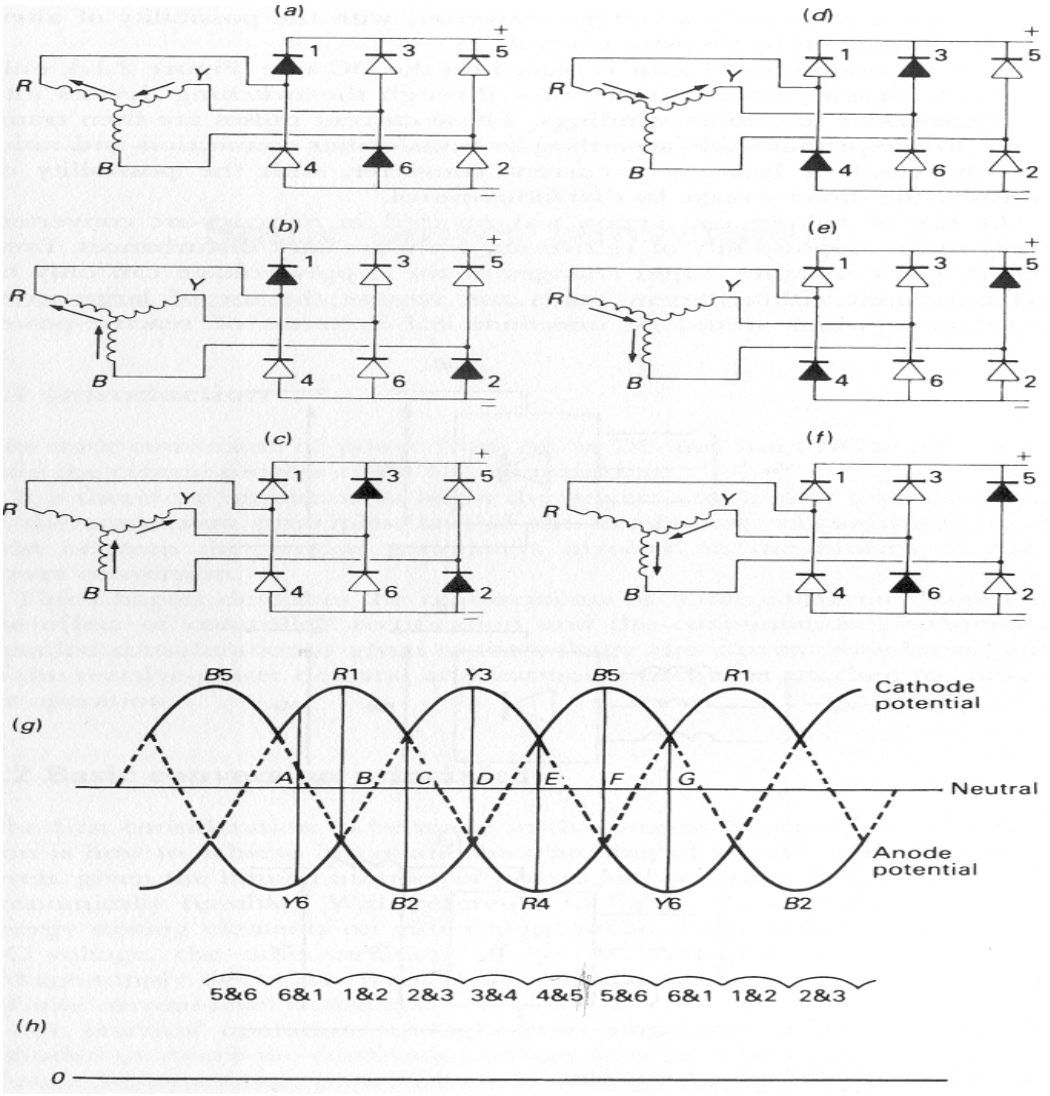


Figure 2.4 Conducting sequence of the bridge and DC voltage waveforms [2]

From Figure 2.4 it can be seen that after instant A, valves 1 and 6 will conduct and a current will flow in phase R and phase Y. At point B valve 2 becomes forward-biased, and the current I_{dc} commutates from valve 6 to valve 2. Every 60^0 a new valve becomes forward biased and the current I_{dc} commutates to this valve. Table 2.1 below shows which valves that conduct between the commutation instants.

Table 2.1 Conducting sequence

Time is between instant	A & B	B & C	C & D	D & E	E & F	F & G	G & H
The conducting valves are	6 & 1	1 & 2	2 & 3	3 & 4	4 & 5	5 & 6	6 & 1

It is clear from Table 2.1 that each valve carries the current I_{dc} for one third of a fundamental cycle of the applied voltages on the AC side.

URN:NBN:no-2111

The output voltage V_o (i.e. the voltage of the positive pole with respect to the negative pole) waveform on the DC side of the rectifier is shown in Figure 2.4 h). V_o has a harmonic frequency of six times the main frequency

The firing angle is larger than zero

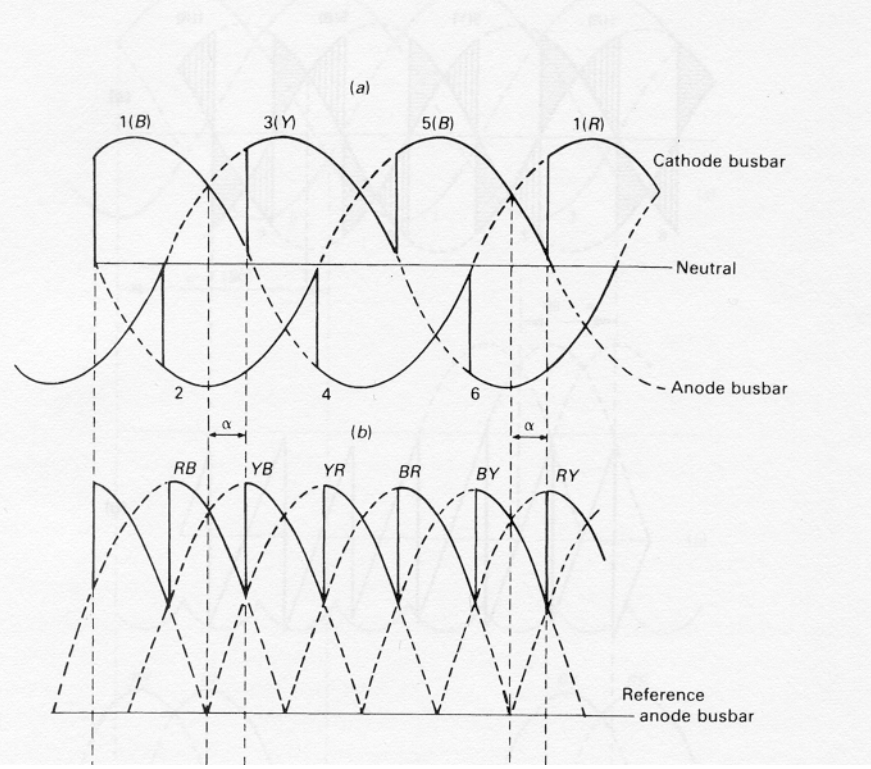


Figure 2.5 Effect of firing delay on voltage waveforms [2]
a) Common-anode and common-cathode voltages
b) Direct voltage

It is seen from Figure 2.5 that the mean of V_o is reduced because of the contribution from the firing angle α compared with the case where $\alpha=0^0$ (See Figure 2.4). The following analyses how V_o changes as α changes:

When α increases the mean value of V_o decreases. If $60^0<\alpha<90^0$ the instantaneous value of V_o in some periods becomes negative. If the DC side was connected to a pure resistive load, the unidirectional current conduction properties of the valves would prevent reverse current flow during these negative periods, and the operation of the bridge would have been intermittent. However, the large smoothing reactor maintains positive current flow during the negative periods of V_o. This means that when V_o is negative, power is transferred from the DC side to the AC side. If $\alpha=90^0$ the negative cycle of V_o equals the positive cycle of V_o, and the mean value of V_o becomes zero (see Figure 2.6). This means that no energy is transferred from the AC side to the DC side or from the DC side to the AC side during a period of V_o. If $\alpha>90^0$ the mean value of V_0 becomes negative and thus the average power (the active power) is transferred from the DC side to the AC side. The converter therefore acts as an inverter when $\alpha>90^0$.

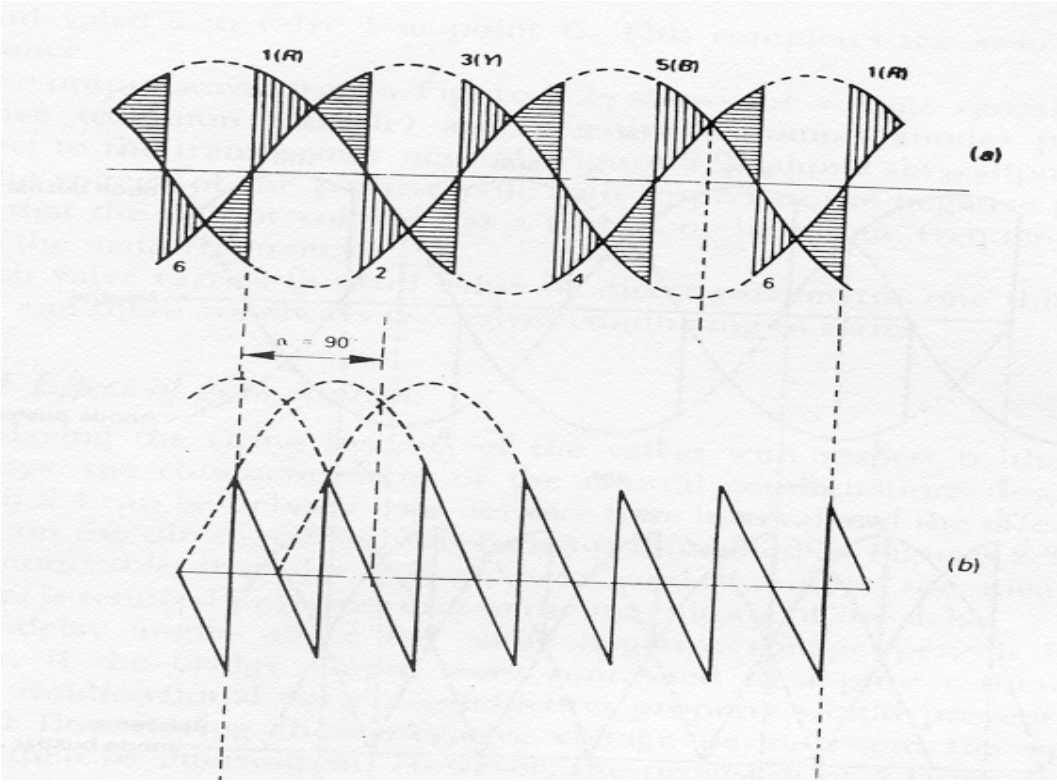


Figure 2.6 Voltage waveforms with 90 degree firing delay [2]
a) Common-anode and common-cathode voltages.
b) Direct voltage V_0.

It is important to notice that even though there is a change in the direct voltage waveform due to the firing delay, the current waveform in each phase on the AC side of the converter is still the same as it was without the firing delay. The only difference between the currents in these modes is that they are shifted by the fire angle. This is illustrated in Figure 2.7.

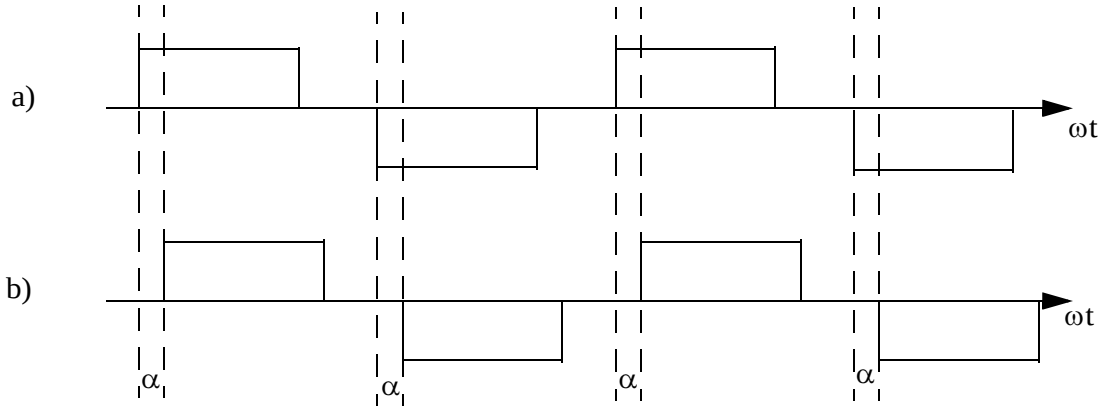


Figure 2.7 Current wave form in a phase (the applied AC side commutation voltages are equal for cases a and b)
a) The fire angle is zero
b) The fire angle is α

When $\alpha=180^0$ full inversion is achieved, and V_o will be at the same size but with opposite sign than when $\alpha=0^0$.

URN:NBN:no-2111

The real commutation process

Because of the AC network inductance and the leakage reactance of the converter transformers, the commutation between the valves in the converter is not instantaneous. The commutation process between two valves is shown below in Figure 2.8.

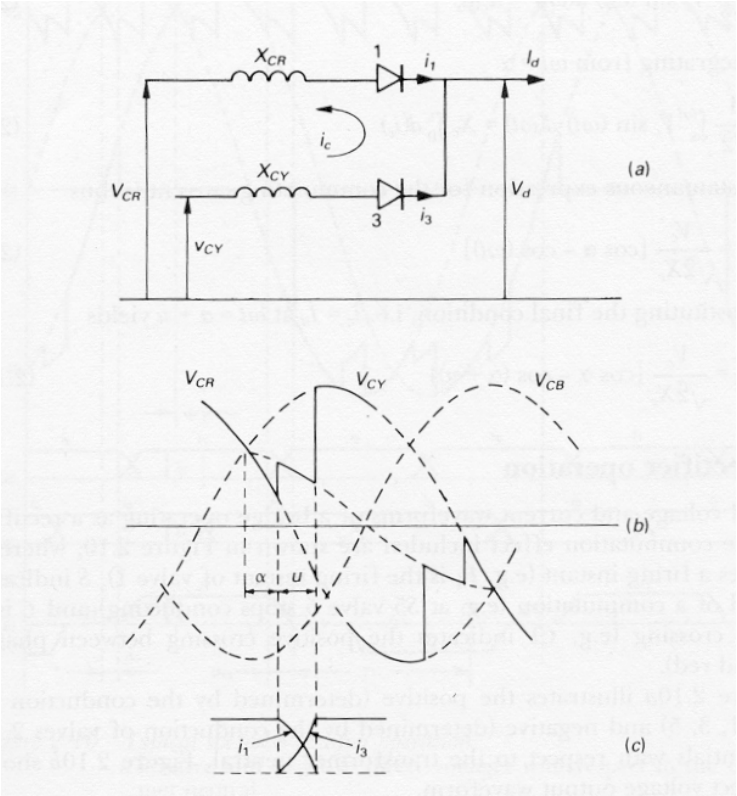


Figure 2.8 The commutation process [2]
a) Equivalent circuit of the commutation from valve 1 to valve 3
b) Voltage waveforms early and late commutations
c) The commutating currents

The mathematical expressions of the DC side current I_d and the mean DC side voltage V_d are derived in the following.

Using Figure 2.8, the commutation current i_c is derived:

$$\text{Uses: } X_C=X_{CR}=X_{CY},\ i_c=i_3-i_1,\quad v_{CY}-v_{CR} = 2\left(\frac{X_C}{\omega}\right)\frac{di_c}{dt} = \sqrt{2}V_C\sin\omega t \tag{2.1}$$

X_C, X_{CR}, and X_{CY} are the commutation reactances.
v_{CY}, and v_{CR} are phase voltages in phase Y and phase R respectively.
V_C is the rms value of the line voltage in the AC network.

From the relations above the instantaneous value of the commutation current can be derived to be:

$$i_c = \frac{V_C}{\sqrt{2}X_C}(\cos\alpha - \cos\omega t) \tag{2.2}$$

When the commutation is done, i_c equals the DC current I_d of the converter. Thus, I_d can be expressed as:

$$I_d = \frac{V_C}{\sqrt{2}X_C}(\cos\alpha - \cos(\alpha + u)) \tag{2.3}$$

u is the commutation angle.

The mean direct voltage V_d is found using Figure 2.9:

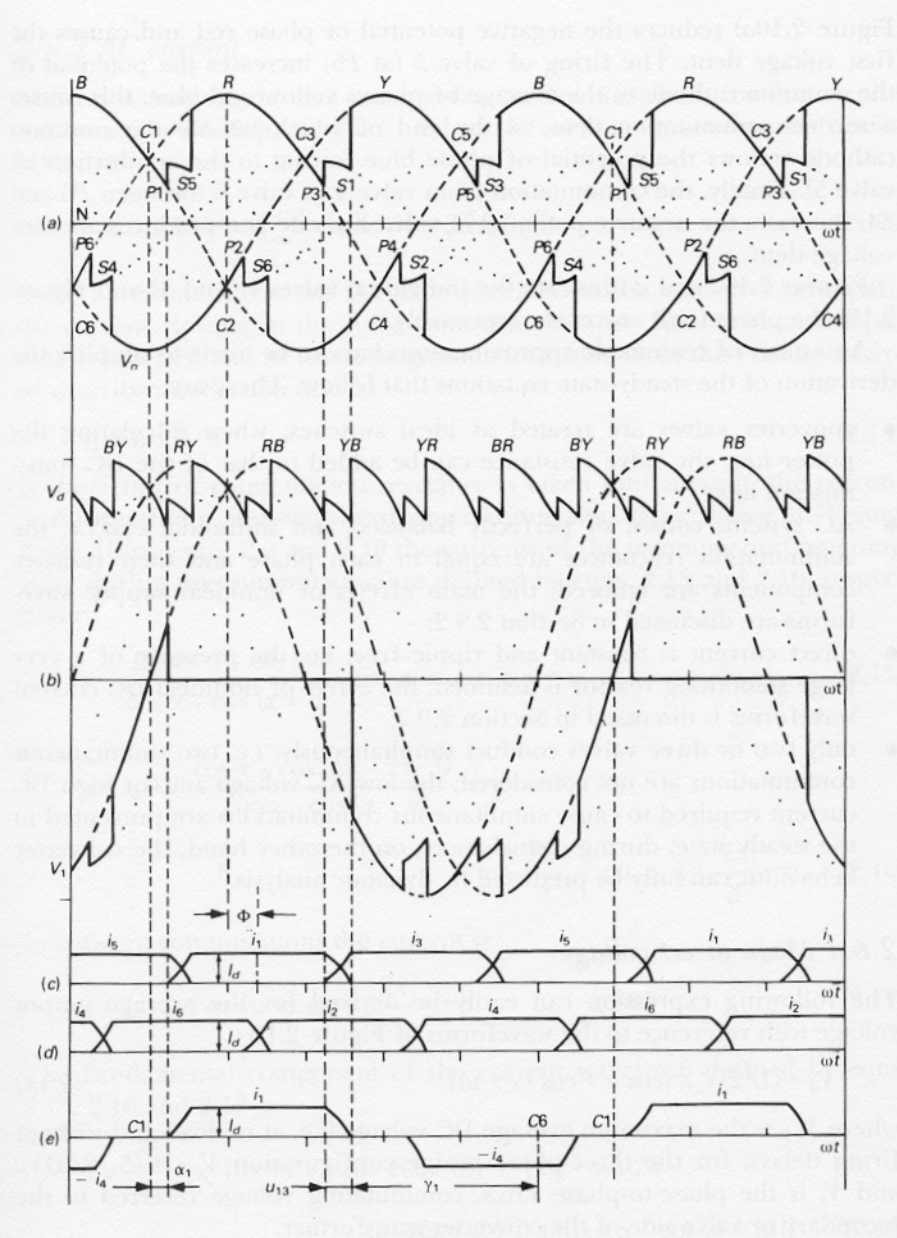


Figure 2.9 Typical six-pulse rectifier operation [2]
a) Positive and negative direct voltages with respect to the transformer neutral
b) Direct bridge voltage V_d and voltage across valve 1
c), d) Valve currents i_1 to i_6
e) AC line current of phase R

URN:NBN:no-2111

Suppose the time is zero at the crossing point C1 in Figure 2.9. The direct voltage as a function of time V_{dt} is expressed in the following way for the next 120^0 (this is derived from Figure 2.9 a) and b)):

$$V_{dt} = \sqrt{2}V_c\cos\left(\omega t + \frac{\pi}{6}\right) \quad \text{for } 0 < \omega t < \alpha \tag{2.4}$$

$$V_{dt} = \sqrt{2}V_c \cdot \cos\left(\omega t + \frac{\pi}{6}\right) + \frac{1}{2} \cdot \sqrt{2}V_c \sin\omega t = \frac{\sqrt{6}}{2}V_c\cos\omega t \ , \alpha < \omega t < \alpha + u \tag{2.5}$$

$$V_{dt} = \sqrt{2}V_c\cos\left(\omega t - \frac{\pi}{6}\right) \quad \text{for } \alpha + u < \omega t < \frac{\pi}{3} \tag{2.6}$$

The mean DC side voltage V_d is given by:

$$V_d = \frac{1}{\pi/3}\int_0^{\pi/3} V_{dt}\, d\omega t \tag{2.7}$$

If Equations (2.4), (2.5), and (2.6) are inserted in Equation (2.7) and the integral in Equation (2.7) is calculated the result becomes:

$$V_d = \frac{3\sqrt{2}}{2\pi}V_c[\cos(\alpha + u) + \cos\alpha] \tag{2.8}$$

The value of the commutation angle is often unknown and must be estimated. Thus it is preferable to express V_d as a function of I_d which is easy to measure directly. By combining information in Equations (2.3) and (2.8), V_d can be expressed by I_d:

$$V_d = V_{do}\cos\alpha - \frac{3X_C}{\pi}I_d \quad \text{where} \quad V_{do} = \frac{3\sqrt{2}}{\pi}V_c \tag{2.9}$$

Equations (2.8) and (2.9) are also valid for inverter mode. If V_d is expressed by the extinction angle the following expressions are found:

$$V_d = V_{do}\cos\gamma - \frac{3X_C}{\pi}I_d \tag{2.10}$$

$$V_d = V_{do}[\cos(\gamma + u) + \cos\gamma] \tag{2.11}$$

In practice α is more than 5^0 to secure successful turn on of the valves. If α is too small, a voltage distortion could cause the voltage across the incoming valve to be lower than the voltage across the valve that is already conducting in the moment the control system gives the firing pulse. The result would be that the attempt to turn on the valve failed. Also γ has an lower limit. Usually it is required that γ is greater than 15^0 because of the uncertainty in the commutation angle. If, for

instance, γ is small and the commutation angle is varying (for instance due to variation in the AC side voltage of the inverter) a valve could suddenly fail to turn off and the valve would conduct its rated current for a longer time than it is designed for. This could damage the valve and increase the harmonic content in currents and voltages both on the DC side and AC side. By increasing γ, this is in many cases avoided.

Power Factor

Both in rectifier mode and inverter mode the current in each phase lags the phase voltage. This is illustrated in Figure 2.10 below.

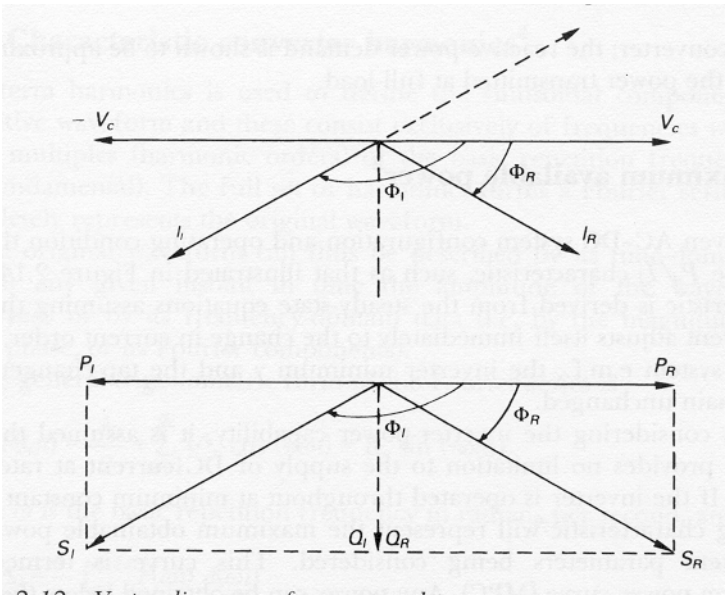


Figure 2.10 Phasor diagrams of current and power [2]. Suffix R for rectification and I for inversion.

From Figure 2.10 it can be seen that both the rectifier mode and the inverter mode consume reactive power. It is desirable to minimize the consumption of reactive power because this has a positive influence due to losses, and compensation. It can be shown that the extinction angle for inverter mode, and the firing angle for rectifier mode should be as small as possible to obtain the optimal power factor. This is done below with the assumptions of perfect filtering (no harmonic currents are injected into the AC network), and losses neglected in the converter.

The active power P is the same on the AC side as the DC side:

$$P = \sqrt{3} V_c I \cos\varphi = V_d I_d \tag{2.12}$$

The power factor cosφ is thus:

$$\cos\varphi = \frac{V_d I_d}{\sqrt{3} V_c I} \tag{2.13}$$

The fundamental component in the AC current I can be found by Fourier analysis. It turns out that:

$$I = \frac{\sqrt{6}}{\pi} I_d \tag{2.14}$$

By using expressions for V_d, I_d in Equation (2.13) the power factor can be approximated to:

$$\cos\varphi = \frac{\cos(\alpha) + \cos(\alpha + u)}{2} = -\frac{\cos(\gamma) + \cos(\gamma + u)}{2} \tag{2.15}$$

In rectifier mode cosφ is closest to one when α is at its minimum, and in inverter mode cosφ is closest to minus one when γ is at its minimum.

2.2.3 Harmonics

Harmonics are defined as sinusoidal components of a repetitive waveform which consists exclusively of frequencies that are exact multiples of the fundamental frequency [2]. The full set of harmonics gives a Fourier series which completely represents the original waveform. As seen from the waveform of the current per phase the converters in an HVDC link delivers to the AC grid (Figure 2.9 e)) it is clear that it is not sinusoidal but it has the same period time as the AC voltage. Figure 2.4 h) shows that DC side voltage of a six-pulse converter is repetitive with a certain frequency. Therefore, these signals can be represented by Fourier series. A comprehensive presentation of theory on Fourier series can be found in [5].

Harmonic components of currents and voltages may cause extra losses, overheating, and interference with nearby electronic systems [30]. In the case of resonances in the grid, even small harmonic components may cause serious problems. It is therefore very important to represent currents and voltages by Fourier series and find ways to filter the harmonics. In this section harmonics from a typical HVDC scheme is considered.

Much of the theory in this section is based on [6].

Harmonics due to HVDC converters

Mainly, HVDC converters generate harmonic voltages on the DC side and harmonic currents on the AC side. The harmonics generated are usually separated in two parts, termed characteristic harmonics and non-characteristic harmonics. The twelve-pulse converter is the most common in HVDC systems and therefore the harmonics due to this converter are the focus in this section.

Characteristic harmonics

The characteristic harmonics are the harmonics related to the pulse number of the converter configuration. They are derived on the following assumptions:

(a) The AC side voltages of the converter are displaced exactly one third of a period in time and consist only of the fundamental frequency.

(b) The DC drossel has infinite inductance, and therefore the DC current is smooth and constant.

(c) The time interval between each firing instant is constant and corresponds to the numbers of

valves in the converter.

(d) The commutation impedances are the same in the three phases.

With these assumptions a converter configuration with *p* valves generates voltage harmonics of orders *pk* on the DC side, and current harmonics of orders $pk \pm 1$ on the AC side (*k* is an integer).

Non-characteristic harmonics

The non-characteristic harmonics are the harmonics related to the non-ideal conditions when operating the HVDC converters. In practice these must be considered when choosing the different components (filters, protection, valves etc.) in an HVDC system. The orders of the non-characteristic harmonics are those not covered by the orders of the characteristic harmonics. Non-characteristic harmonics are caused by:

(a) Firing errors

(b) Asymmetrical AC voltages

(c) DC current modulation. (The harmonics on the AC side and the DC side are mutually connected. Consequently a small error which causes non-characteristic harmonics on the DC side causes non-characteristic harmonics on the AC side)

(d) Unequal commutation reactances in the phases on the AC side

Harmonics transferred from the AC side to the DC side of a twelve-pulse converter

There is a general relationship between the harmonics on the AC side and the DC side of a twelve-pulse HVDC bridge. If a positive-sequence harmonic multiple *k*+1, or a negative-sequence harmonic multiple *k-1* appears in the otherwise perfectly symmetrical commutation voltages on the AC side of the 12 pulse HVDC bridge then the frequency f_{DCk} of the harmonic voltages which appears on the DC side can be written as:

$$f_{DCk} = (12n \pm k) f_0 \tag{2.16}$$

f_0 is the fundamental frequency of the commutation voltages.

$n \in (0, 1, 2, 3, ...)$

Equation (2.16) is valid also for inter- and sub-harmonics (i.e. when *k* is not an integer)

The magnitude of the DC voltage with harmonic multitude *k* is switched across the converter in the same ratio as the fundamental voltage is, except that the fire angle delay does not reduce the magnitude of the DC harmonic voltage but merely phase shifts this voltage. Nevertheless, there might be a modification of the DC side harmonic level by up to ten per cent and also a phase shift up to 0.3 radians. This is due to that the AC voltage distortion is affecting the commutation period. By direct transfer the higher order DC voltage non-characteristic harmonics (the

harmonics when $n \geq 1$ in Equation (2.16)) are approximately reduced by a factor 1/(12*n*) compared to the non-characteristic harmonic corresponding to *n=0* in Equation (2.16), if the switching instants remains unaffected by the distortion. However, also these harmonics in the DC voltage may be modified. The spectrum which appears as a result of commutation variation does not reduce nearly as quickly as a factor of 1/(12*n*). Thus, for DC side harmonic voltages of order $12 \pm k$, the commutation-period variation is contributing substantially (maybe 50 %). The contribution from the commutation period variation becomes a more and more important factor in the DC side harmonic voltages as the frequency increases. Because of this, the level of the higher order DC side voltage harmonics can be substantially different reduced than by a factor of 1/(12*n*).

From Equation (2.16) it is clear that if *k*=0 than the DC side harmonics will have the frequency:

$$f_{DCk} = 12nf_0 \tag{2.17}$$

These are the characteristic harmonics on the DC side. They are the only harmonics present when the twelve-pulse bridge are operated under idealized conditions. The higher order harmonics in the DC side voltage will under idealized conditions be reduced compared to the DC component. The relationship on how they get reduced as a function of the frequency is given by a quite complex formula ([6], p.25). This formula also depends on the commutation angle, the fire angle, and the maximum averaged rectified voltage.

Harmonics transferred from the DC side to the AC side of a twelve-pulse converter

If a harmonic current source which generates a harmonic current with harmonic multiple k exists on the DC side of the twelve-pulse bridge under otherwise idealized operation of the bridge, then the frequencies f_{ack+} and f_{ack-} of the generated harmonic currents on the AC side can be expressed as in the following:

$$f_{ack+} = ((12n + 1) \pm k) \cdot f_0 \tag{2.18}$$

$$f_{ack-} = ((12n - 1) \pm k) \cdot f_0 \tag{2.19}$$

Equations (2.18) and (2.19) are also valid for inter- and sub-harmonics (i.e. when k is not an integer).

If the DC component of the DC side current is 2 kA and the fundamental component of the AC side current is 2.5 kA, then the harmonic currents of harmonic multiple *k*+1 and *k*-1 generated on the AC side, will have magnitude equal to $0.5 \cdot \frac{2.5}{2}$ times the harmonic current of harmonic multiple *k* on the DC side. However, the DC current distortion is affecting the commutation period. Therefore the level of the AC side harmonic currents might be modified up to 15 % and their phase angle can be modified up to 0.2 radians.

If the switching instants remain unaffected by the distortion, the higher order non-characteristic AC side harmonics (the harmonics corresponding to $n \geq 1$ in Equations (2.18) and (2.19)) are reduced by a factor approximately $1/(12n \pm 1)$ compared to the non characteristic harmonics corresponding to *n*=0 in Equations (2.18) and (2.19). However, these harmonics are influenced by the effect of the DC current distortion on the commutation period. The spectrum caused by

the variation in the commutation period reduces more quickly than that for the DC voltage (see the section above on harmonics transferred from the AC side to the DC side), but not as quickly as the characteristic harmonics. Thus, the commutation period variation is contributing substantially to the AC side harmonic currents of order $(12n+1)\pm k$ and $(12n\text{-}1)\pm k$. The contribution from the commutation period variation becomes a more and more important factor in the AC side harmonic currents as the frequency increases.

If *k=0* in Equations (2.18) and (2.19) then:

$$f_{ack+} = (12n + 1) \cdot f_0 \tag{2.20}$$

$$f_{ack-} = (12n - 1) \cdot f_0 \tag{2.21}$$

The harmonics on the AC side with frequencies given by Equations (2.20) and (2.21) are the characteristic harmonics on the AC side. They are the only harmonics present on the AC side under idealized conditions.

Harmonics in a twelve-pulse converter due to switching instant variation

Assume there is a sinusoidal variation with harmonic order *k* in the fire angle order to an HVDC converter and otherwise idealized conditions. Then there will be generated harmonic DC voltages with frequencies given by:

$$f_{DCk} = (12n \pm k)f_0 \tag{2.22}$$

Equation (2.22) is also valid when k is not an integer.

This will cause positive- and negative-sequence harmonics in the AC side current. The frequencies of these currents are given by:

$$f_{ack+} = ((12n + 1) \pm k)f_0 \tag{2.23}$$

$$f_{ack-} = ((12n - 1) \pm k)f_0 \tag{2.24}$$

The generated harmonics diminishes with increasing frequency as explained in earlier in this section.

Effects on the harmonics due to non-ideal conditions

Non-characteristic harmonics will always be present in a real HVDC scheme. In the following effects of different causes to the non-characteristic harmonics are evaluated.

a) Effects of firing errors:

Consider the ideal 120^0 rectangular pulse in Figure 2.7. This is the pulse of one of the phase currents in a AC line which is connected to a six-pulse thyristor bridge via a star-star connected transformer. The commutation angle is neglected. If one of the valves in the bridge somehow fails to fire at the instant it is meant to fire but have an extra delay of for instance 2^0 before firing

one of the pulses in the per phase currents will not last for 120^0 but only for 118^0. Because of this the phase current not can be written as a function $f(t)$ where $f(t)= -f(t+T/2)$. This means that the phase current will also contain elements of even harmonics and triple harmonics.

In a twelve-pulse HVDC converter, firing errors in a similar way as just described may destroy the half-wave symmetry of the phase currents and thus create even and triple harmonic phase currents. To include the commutation angle in the consideration above is not likely to change this statement. In modern HVDC control systems, the effect of distorted commutation voltages on the fire angle is almost eliminated because of the phase-locked loop (see Figure 2.24) used to find the right firing instances.

b) Effects of distorted and/or asymmetric AC voltages:

Distorted AC voltages can create harmonics due to firing errors. As mentioned earlier, the phase-locked loop in the firing controllers in modern HVDC links have minimized this problem.

A problem which the firing controllers not are able to deal with is unbalanced amplitudes on the AC voltages. For instance, if the AC voltage in one of the phases has a considerably lower amplitude than the AC voltages in two of the other phases, the DC voltage will get a second harmonic component which will cause a second harmonic current on the DC side. Due to coupling between the harmonics in the DC current and in the AC currents, the AC currents will get a third harmonic component in the positive-sequence and a fundamental harmonic component in the negative-sequence. With unfavourable impedances in the AC and DC grid this might cause a problem.

c) Effect of direct current modulation:

Even though the AC voltages are perfectly balanced and the firing errors are eliminated through the firing controllers, non-characteristic components in the AC currents may exist. This is due to the coupling between the harmonic components in the DC current and in the AC currents. For example, if for some reason a low order harmonic component in the DC current of order n is generated, this component will be mirrored to the AC side current as harmonic components of orders $n+1$ in the positive system and $n-1$ in the negative system.

d) Effect of asymmetric commutation reactances:

The effect of unequal commutation reactances are odd non-characteristic AC harmonic currents, and even non-characteristic DC harmonic voltages. The size of these depend on the mean of the commutation reactances, the differences in the commutation reactances, the firing angle, and the overlap angle.

Harmonic filters

Figure 2.11 shows an example of an HVDC converter and its filters (there are only filters on the AC side in this figure).

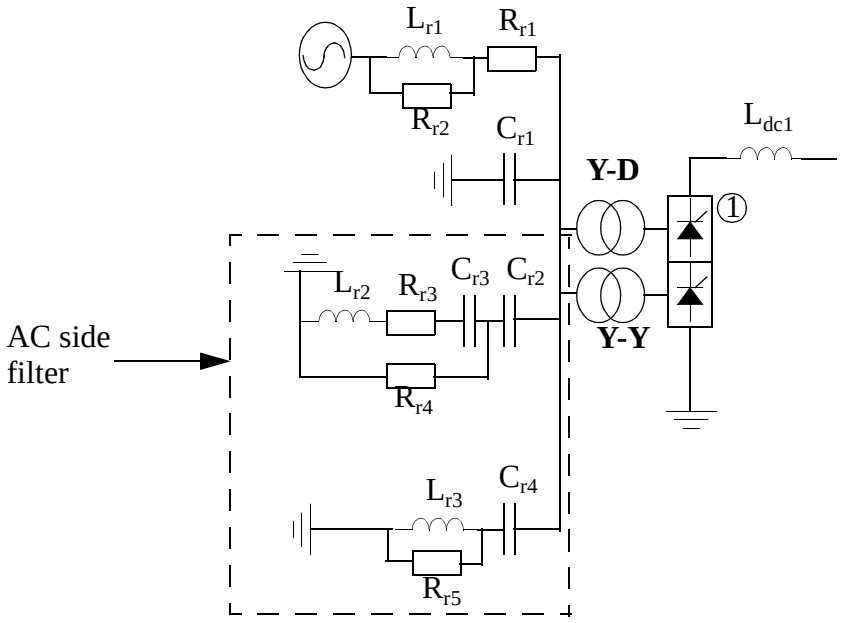


Figure 2.11 Example of an HVDC converter and its filters.

As stated earlier, harmonics may cause extra losses, overheating, and interference with nearby electronic systems. There may also be equipment that is sensitive and should be protected from harmonics. Harmonic filters limit or eliminate the damage harmonic currents or voltages can cause. The idea with harmonic filters is to create a low impedance path to earth for the harmonic currents. In this way they will be prevented from flowing into the AC or DC grid. In addition the AC side filters of an HVDC transmission often have a secondary function. This is to provide reactive power to the HVDC converter [2]. Figure 2.12 shows typical filter configurations and impedance characteristics of filters used in HVDC transmission.

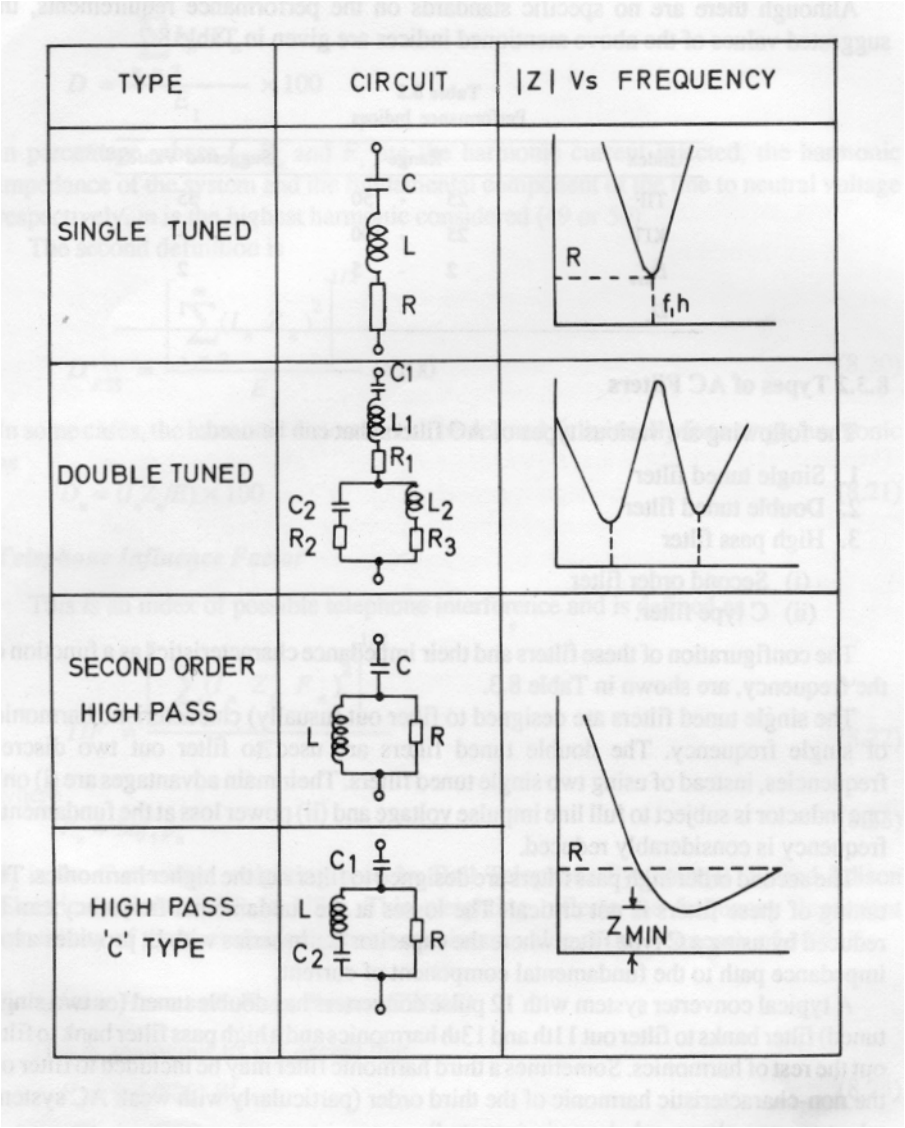


Figure 2.12 Configurations and impedance characteristics of typical filters for HVDC links [7].

The single tuned filter is designed to filter out characteristic harmonics of a single frequency. For instance, when filtering harmonics from a twelve-pulse bridge the single tuned filter may be used to filter out the twelfth harmonic on the DC side.

The double tuned filter is used to filter out two specific frequencies. Reference [7] claims that the double tuned filter has less power loss at the fundamental frequency than two single tuned filters. In addition only one inductor will be subject to full line impulse voltage. The double tuned filter may be used to filter out the eleventh and thirteenth harmonics from a twelve-pulse bridge.

The second order high pass and high pass ‘C’ type filters are both used to filter out higher harmonics. The ‘C’ type filter has less loss at fundamental frequency than the second order high pass filter [7].

The development of power electronic components gives new possibilities in the filtering of

harmonics [8]. An example of this is an active shunt filter [9]. An active shunt filter is a device that actively generate harmonic components of the load current and this way prevent these components to flow in the AC grid. Figure 2.13 shows a simplified circuit diagram of an active shunt filter.

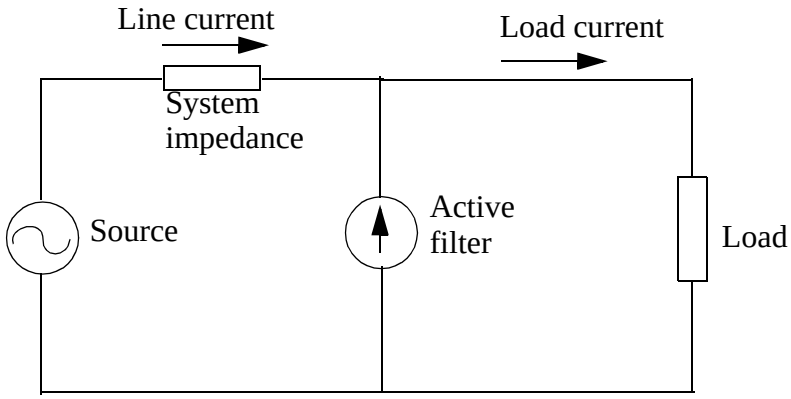


Figure 2.13 Simplified circuit diagram of an active filter that compensates for harmonics in the load current.

Active shunt filters are built up by power electronic devices like GTOs or IGBTs. By measuring the undesired harmonic components in the load current, a current order is generated for the active filter. The current the active filter generates because of this current order will prevent the earlier measured undesired harmonic components in the load from flowing into the AC grid. Compared to passive filters, the active filters have the advantages that they do not cause any parallel resonances with the AC system impedance, nor are they as sensitive to changes in component values as passive filters. Nevertheless, it is necessary to build PWM converters with high VA rating [10] (at least in the case when an HVDC link is the load). Due to the high VA rating required in active filters its switching frequency becomes limited and it is therefore limited how high frequency the active filters are able to compensate for.

A hybrid shunt filter is a combination between an active shunt filter and passive shunt filter. A simplified circuit diagram of a hybrid shunt filter that compensates for harmonics in the load current is shown in Figure 2.14.

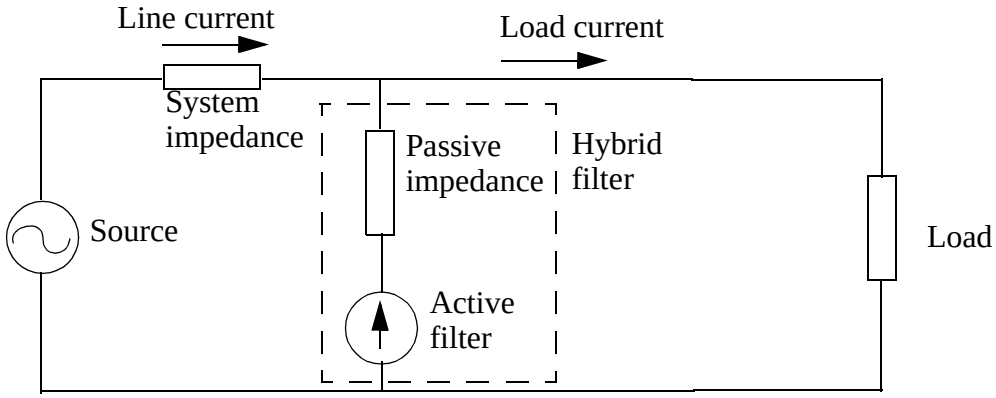


Figure 2.14 Simplified circuit diagram of a hybrid shunt filter that compensates for harmonics in the load current.

The hybrid shunt filter has the same function as the active shunt filter, but it has the advantage that the PWM converter does not have to sustain the voltage level of the AC grid (which might be several hundred kV line-line when the load is an HVDC link). The VA rating of the PWM converter in the hybrid filter becomes much less (typically ten times less) than the VA rating of

the corresponding active filter [9]. This is obtained by controlling the PWM converter such that all the fundamental harmonic voltage drop is across the passive impedance of the hybrid shunt filter. The lower VA rating for the hybrid shunt filter makes it more capable of handling faults and high switching frequencies than a corresponding active shunt filter. By tuning the passive part to have a low impedance for the harmonics in the load currents which it is desirable to compensate for by the hybrid filter, the harmonic voltage across the active part of the hybrid filter is also minimized. This way the rating of the PWM converter is minimized. The component values in the passive part of the hybrid filter might change due to temperature, aging, and other external circumstances. Therefore the PWM converter of the hybrid filter should have some margin in its VA rating. Just like the active shunt filter, the hybrid shunt filter will not cause any resonances in the AC system.

2.3 The HVDC control system

The HVDC control system is designed with a compromise of safe operation of the HVDC scheme and as high power factors for the inverter and rectifier in the HVDC bridges as possible [2]. The control system must also in most cases allow power flow in both directions across the HVDC link. A typical control strategy used for control of HVDC systems is presented now. Much of the theory used in this section is based on [11].

2.3.1 Typical control strategies

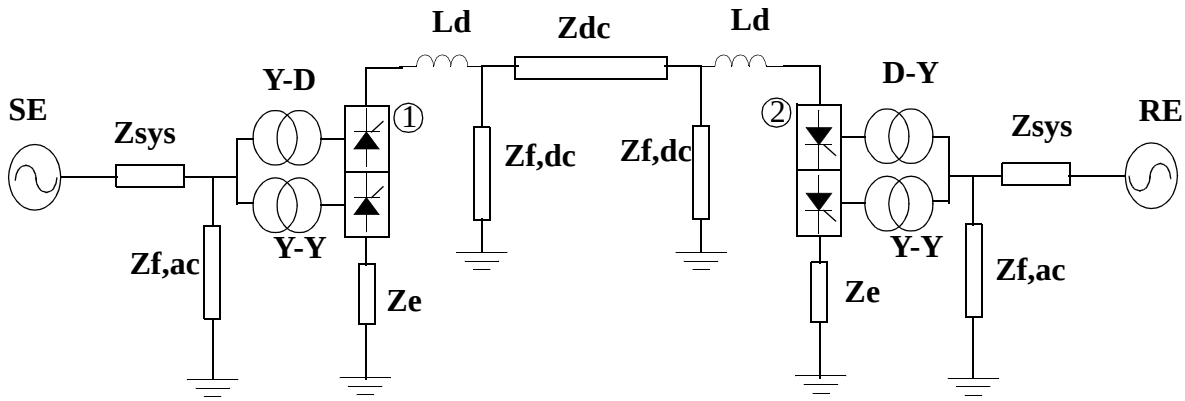


Figure 2.15 Monopolar HVDC Transmission

The average DC voltage V_{dcr} across the twelve-pulse rectifier can be shown to be given by:

$$V_{dcr} = \frac{6\sqrt{2}}{\pi} \cdot V_{llr} \cdot \cos(\alpha_r) - \frac{6X_{sr}}{\pi} I_{ad} = V_{0r} \cdot \cos(\alpha_r) - \frac{6X_{sr}}{\pi} I_{ad} \quad (2.25)$$

V_{llr} is the line-to-line rms voltage applied to each of the rectifier converters.
X_{sr} is the per phase leakage inductance of each of the rectifier converter-transformers referred to their converter side (assumed to be equal for the Y-Y and the Y-D coupled transformers).
α_r is the fire angle of the rectifiers.
I_{ad} is the average DC side current.

The average DC voltage V_{dci} across the twelve-pulse inverter can be shown to be given by:

$$V_{dci} = \frac{6\sqrt{2}}{\pi} \cdot V_{lli} \cdot \cos(\gamma) - \frac{6X_{si}}{\pi} I_{ad} = V_{oi} \cdot \cos(\gamma) - \frac{6X_{si}}{\pi} I_{ad} \quad (2.26)$$

V_{lli} is the line-to-line rms voltage applied to each of the inverter converters.
X_{sr} is the per-phase leakage inductance of each of the inverter converter transformers referred to their converter side (assumed to be equal for the Y-Y and the Y-D coupled transformers).
γ_i is the extinction angle of the inverters.

V_{dcr} and V_{dci} are related by:

$$V_{dcr} = R_{dc} \cdot I_{ad} + V_{dci} \quad (2.27)$$

R_{dc} is the DC side resistance.

It is seen from Equation (2.27) that the size and the direction of the power flow is decided by the difference between V_{dcr} and V_{dci}. Thus, by controlling V_{dcr} and V_{dci} it is possible to obtain a desired power transmission between the rectifier side and the inverter side. If V_{dci} becomes larger than V_{dcr} then the rectifier will be turned into an inverter, and the inverter will be turned into a rectifier. Figure 2.16 shows the converter characteristics due to the control system when power is flowing from station 1 to station 2 in Figure 2.15. If the direction of power flow is from station 2 to station 1 the converter characteristics due to the control system are as shown in Figure 2.17.

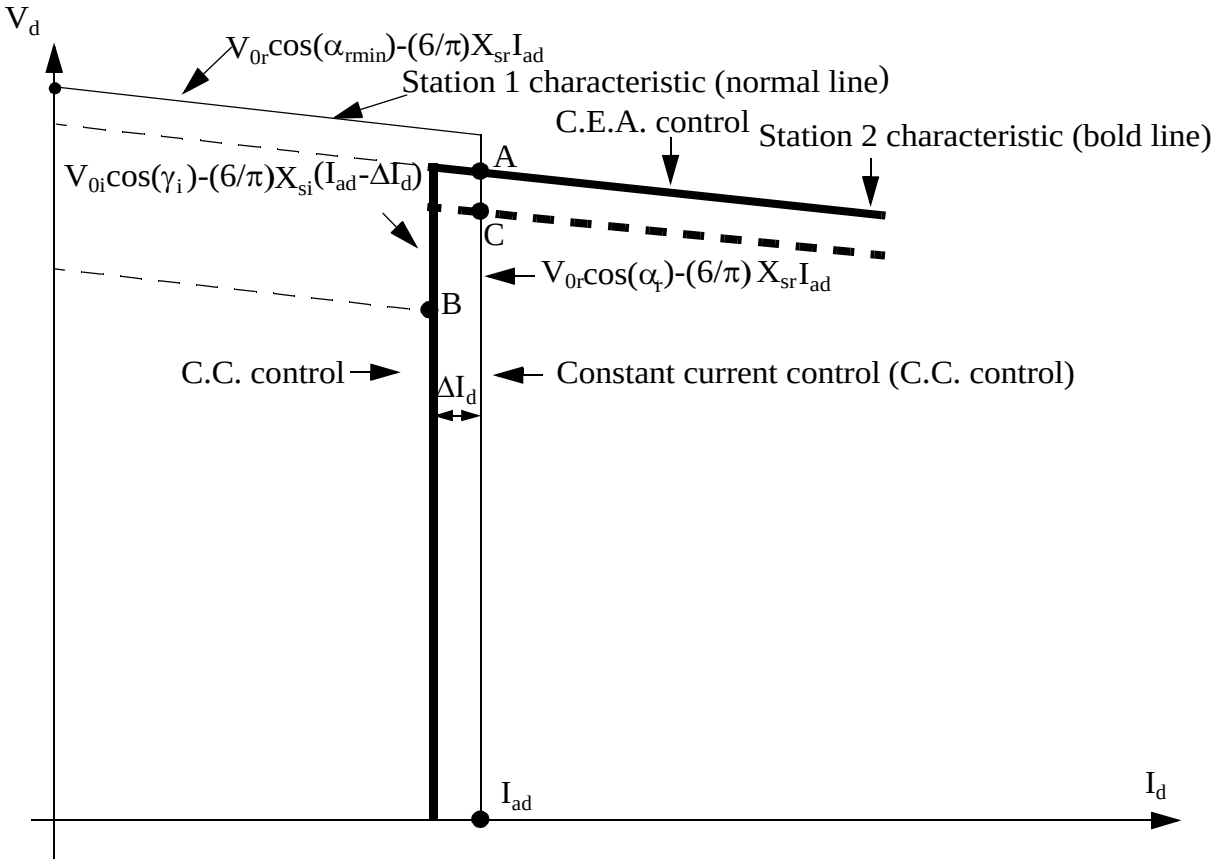


Figure 2.16 Converter characteristics when the power flows from the sending end (SE) to the receiving end (RE)

In Figure 2.16, point A is the operating point both for the inverter and the rectifier. In this case the rectifier is in the constant current control mode, and the inverter is in the constant extinction angle mode. It normally turns out that the reactive power compensation of the HVDC scheme is smallest and that the utilization of the line (or cable) is best in this case [2]. If there is a decrease in the AC side rectifier voltages there will also be a stable operating point between the inverter characteristic and the rectifier characteristic. Point B on Figure 2.16 is an example of this. At point B the inverter is in the constant current (C.C.) control mode, and the rectifier will have the fire angle α_{rmin}. Even if the voltage on the inverter side drops, a stable operating point is ensured. Point C in Figure 2.16 is an example of this. At point C the rectifier will be in its C.C. control mode and have a higher α_r and/or the rectifier AC side voltages will be lower than at point A. The inverter will be in constant extinction angle (C.E.A.) control mode and have the same γ_i as at point A.

If the direction of the power flow is reversed, then the station 1 and station 2 characteristics are changed to the characteristics in Figure 2.17.

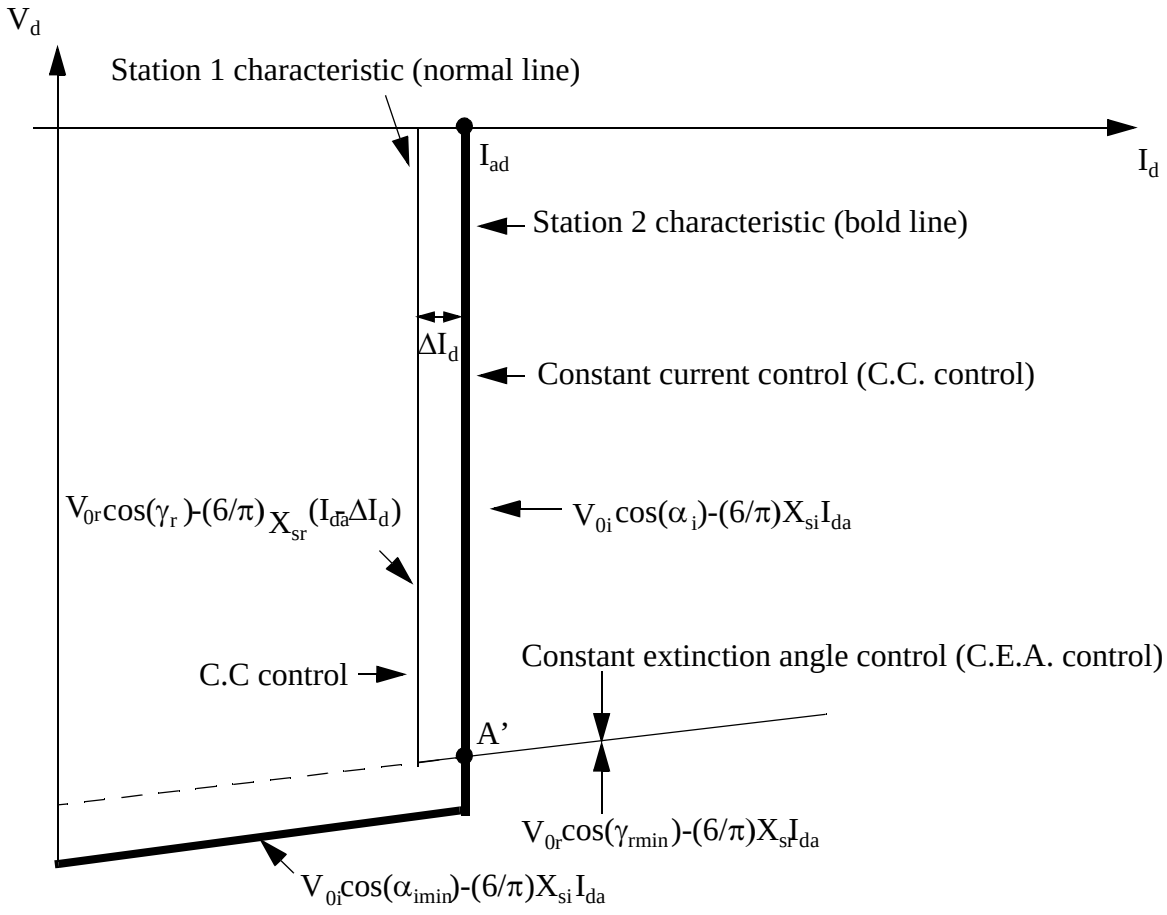


Figure 2.17 Converter characteristics when the power flows from the receiving end (RE) to the sending end (RE)

The operating point at the DC current I_{ad} will now be A'. Station1 is therefore in the C.E.A. control mode, while station 2 is in the C.C. control mode. Similar considerations as above for the characteristics in Figure 2.16 can be done for the characteristics in Figure 2.17.

The rectifier controller (current control)

The block diagram for the rectifier current controller is shown on Figure 2.18.

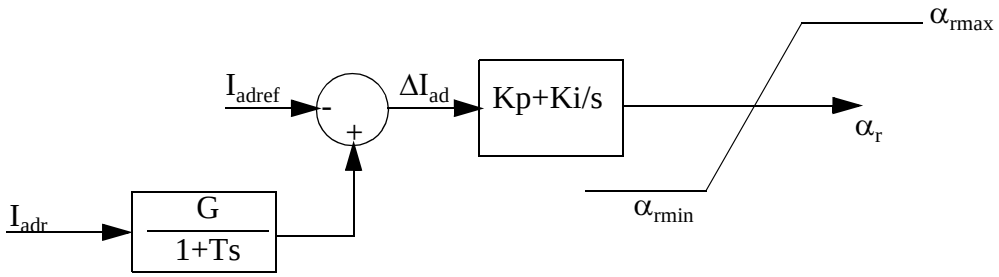


Figure 2.18 Rectifier current controller

I_{adr} is the measured DC side current of the rectifier.

The rectifier fire angle is controlled such that the DC voltage across the rectifier is increased or decreased according to Equation (2.25), and this variation is used to adjust the DC current to its setpoint. If the desired current cannot be obtained for an angle $\alpha_r > \alpha_{rmin}$, the DC current will be limited by Equation (2.25) with $\alpha_r = \alpha_{rmin}$. α_{rmax} limits the minimum power which can be transferred across the DC link in one direction. α_{rmin} is typically chosen to be 5 degrees. This is done so that there is high probability of successfully turning on the valves.

The inverter controller (constant extinction angle control)

The block diagram for the inverter constant extinction angle controller is shown in Figure 2.19.

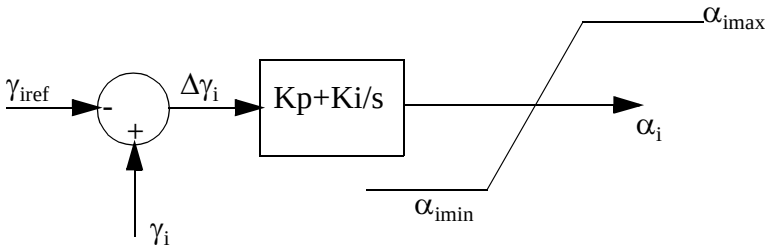


Figure 2.19 Inverter constant extinction angle controller

The inverter fire angle is controlled such that the extinction angle is as small as possible. Since the current I_{ad} is given by the rectifier controller, the extinction angle γ_i of the inverter will be adjusted such that the voltage across the inverter corresponds to the current I_{ad}. The tap changer controller will adjust the DC voltage across the inverter to be within specified limits. Due to the power factor of the inverter it is desirable to have a value of the extinction angle as small as possible. However, the probability of commutation failure increases as γ_i becomes too small. Therefore γ_{imin} is typically chosen in the range 15-18 degrees.

To ensure stable operation if the rectifier AC voltages drop, the inverter controller also has a C.C. control mode. The constant current allows for a degraded mode of operation, like point B in Figure 2.16. For the inverter C.C. controller the current order is typically kept 10 % lower than the current order in the rectifier C.C. controller. The difference in the current settings for the inverter and the rectifier is ΔI_d. How the inverter controller selects between C.C. control mode and C.E.A.control mode, is illustrated in the block diagram in Figure 2.20.

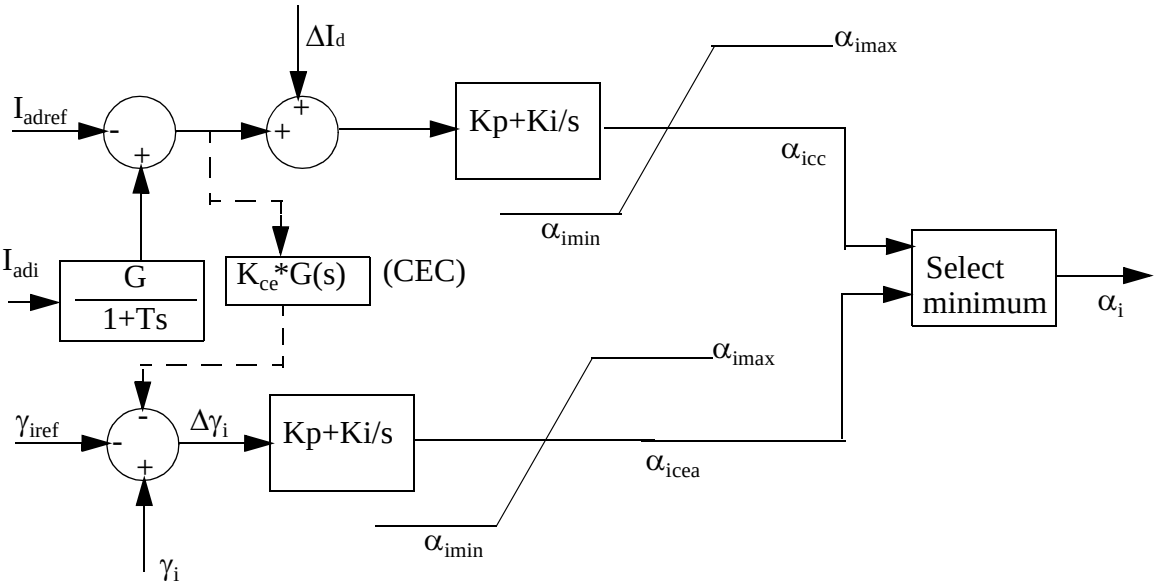


Figure 2.20 Selection between C.C. and C.E.A. control modes for the inverter

I_{adi} is the measured current on the DC side of the inverter.

If $I_{adi} > I_{adiref}$ - ΔId then there is a positive input to the C.C. controller, thus the output will be integrated towards α_{imax}. Therefore the C.E.A. control loop wins and its generated firing angle is used. If the AC side rectifier voltages decreases significantly, the DC current starts to decrease. Eventually this causes the output of the C.C. controller of the inverter to decrease. The fire angle order given by the C.C. controller of the inverter becomes less then the fire angle order given by the C.E.A. controller of the inverter. Thus, the inverter will operate in C.C. control mode. The C.E.C. (Current Error Control) block in Figure 2.20 might be used to give a smoother transition between the C.C. and C.E.A. control modes than on Figure 2.16-17. For the characteristics in Figures 2.16 and 2.17 a small decrease in the rectifier AC side voltages will cause quite a large change in the operating point. By using the C.E.C. a more gradual change in the operating point is possible. This is illustrated in Figure 2.21.

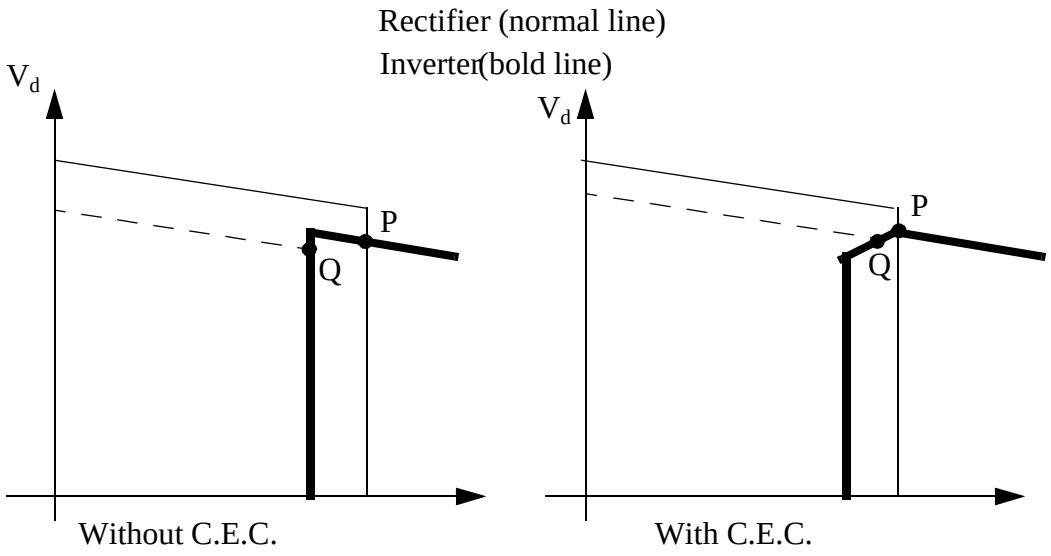


Figure 2.21 The effect of C.E.C. control

Voltage Dependent Current Order Limit (V.D.C.O.L)

Even though the C.E.A. controller is chosen with a minimum extinction angle in the range 15-18 degrees commutation errors may occur (for instance an AC fault on the inverter side causing distorted and reduced commutating voltages). Because of the commutation error, some valves in the inverter may have to carry the rated current longer than they are designed for. This may overheat and destroy the valves. The HVDC-control system can be used to avoid this, and that is done by using the Voltage Dependent Current Order Limit (V.D.C.O.L.) control mode. The overall converter characteristics including C.E.C. and V.D.C.O.L. is shown in Figure 2.22.

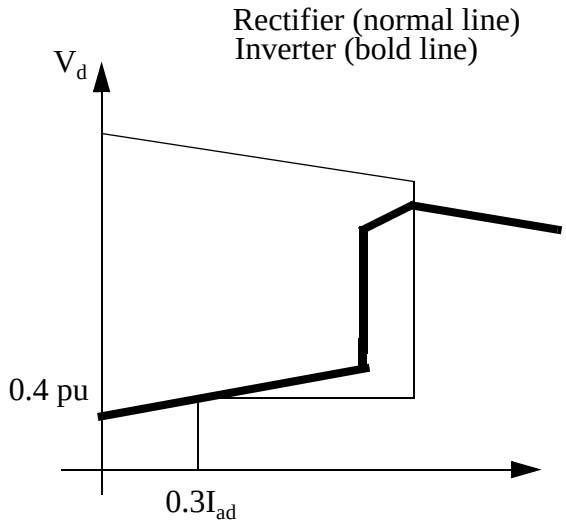


Figure 2.22 Overall converter characteristics

A commutation error will cause a lower DC voltage V_{dcr} on the rectifier side. If V_{dcr} becomes lower than a certain value (typically 40 % of the rated voltage), the rectifier current order is reduced to about 30 % of its rated value. In this way the inverter valves can tolerate the currents flowing through them. The inverter will lower its fire angle such that a new operating point is possible.

Block diagrams showing how the rectifier and inverter controllers can decide if V.D.C.O.L. shall be used or not might be as in Figure 2.23.

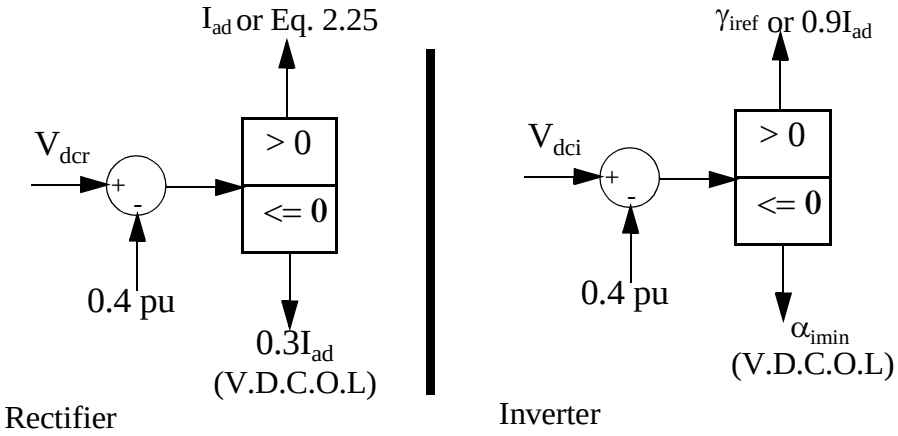


Figure 2.23 Block diagram for selection of V.D.C.O.L.

URN:NBN:no-2111

Tap changing controls

HVDC converters consume reactive power. The lower the rectifier fire angle, the less reactive power does the rectifier demands, and the lower the extinction angle for the inverter is the less reactive power the inverter demands (this is the case if the transferred power is assumed to be constant). To minimize the reactive power demand of the rectifier, the tap changer is controlled such that the rectifier fire angle is not too large. On the other hand, the tap changer control must be controlled such that α_r does not become too small (to have freedom for additional control).

*** Example 2.1

The rectifier in its C.C. control mode has settled to a value of αr=20 degrees in order to maintain the required DC current. To obtain a lower firing angle for the rectifier (and then a better power factor), the tap changer control will decrease the rectifier AC side voltages (see Equation (2.25)). When α_r has reached a tolerance band around 15 degrees the control action of the tap changer stops. If α_r becomes considerable less than 15 degrees, the tap changer control will increase the rectifier AC side voltages.
***

Similar tap changing is carried out at the inverter. However, the criterion for control here is to maintain the rms voltage of a bus in the AC system close to the inverter within a specified tolerance band. In this way load changes in the inverter side AC system have less influence on the power transferred across the DC link.

Firing controls

The firing controls convert the firing angle order demanded by the valve group control system into accurately positioned firing pulses to the valves. One approach to obtain this in a very accurate way is the phase-locked loop (PLL)-based firing system as shown in Figure 2.24.

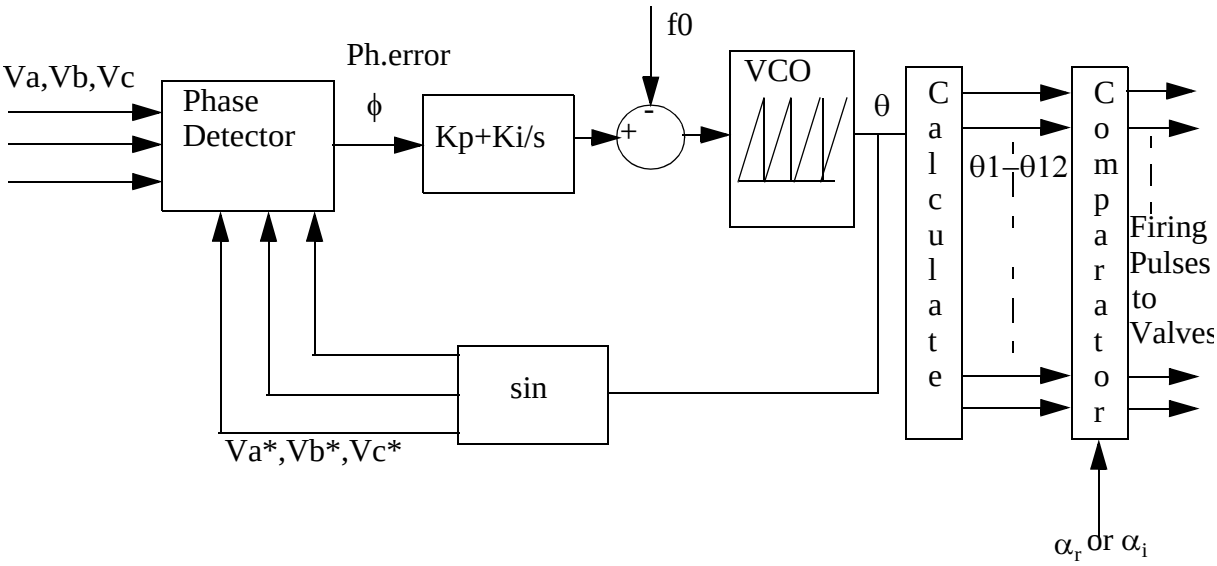


Figure 2.24 Phase-locked loop based firing system

In the phase-locked loop the Voltage Controlled Oscillator (VCO) generates the angle θ. This is done by integrating the signal into the VCO until θ has reached 360 degrees, then θ will be reset to 0 degrees. This process is then repeated. The integration constant in the VCO block must integrate such that if the input is *f0* (the fundamental frequency of the commutating voltages Va,Vb, and Vc), θ is integrated from 0 to 360 degrees in $1/(2\pi f0)$ seconds. θ becomes the time varying part of the phase angle to the three sinusoidal voltages generated in the sin block i.e. Va*,Vb*,Vc*. These three voltages have a phase difference between each other equal to 120 degrees of a signal with frequency *f0* .

The PI controller influences the input into the VCO, such that the positive-sequence of the phase voltages generated in the *sin* block becomes more and more in phase with the positive-sequence of their corresponding commutation voltages. In the end under ideal conditions there will not be any phase difference between Va and Va*, Vb and Vb*, Vc and Vc*.

The instant for firing the individual valves in the HVDC bridge is decided in the comparator. From θ (the output of the PLL) twelve signals θ1-θ12 are generated in the calculate block. They are calculated such that they give appropriate firing angle signals to the valves in the twelve-pulse bridge. At the moment one of the signals θ1-θ12 become larger than the fire angle order (α_r if rectifier operation, α_i if inverter operation) a firing pulse is sent to the valve corresponding to that signal of θ1-θ12 which became larger than the fire angle order. In this way the valves will fire at the right instances.

The overall control diagram

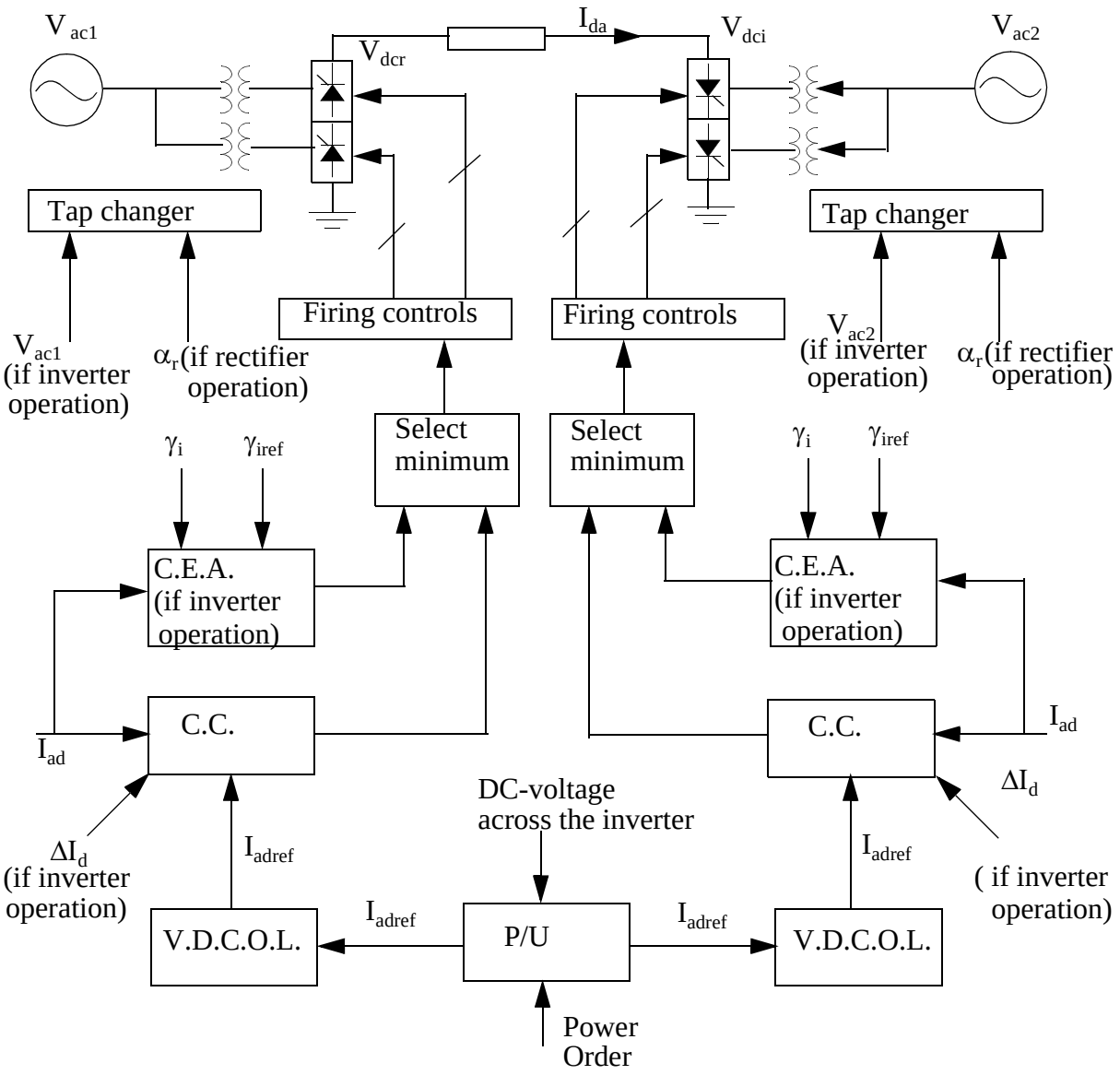


Figure 2.25 Overall control diagram

Figure 2.25 shows the total control system of the HVDC scheme. If the DC line is long, some of the signals in Figure 2.25 must be transferred via a telecommunication link [11]. However, the rapid power control possible in HVDC schemes allows for supplementary control equipment which can be used to damp power swings in the connected AC systems, control sub-synchronous resonances, prevent core saturation instability and so on.

3 Theory about core saturation instability

Core saturation instability is a phenomenon which might occur in the operation of a twelve-pulse HVDC converter [1]. Many factors contribute to its occurrence [1]. One of them is the coupling between the harmonics on the AC and DC sides of the converter. The magnetizing characteristics of the converter transformers also have a significant influence on the phenomenon. Other important contributors to core saturation instability are the impedance seen in the DC network from the converter and the total impedance seen from the commutation bus bar of the converter. The HVDC control system may also contribute to core saturation instability. As a matter of fact this type of instability is considered a rarity without imperfections in the HVDC control system [6]. This chapter gives an overview of the factors that contribute to core saturation instability. In the end these are added together to illustrate core saturation instability.

3.1 Harmonic interaction

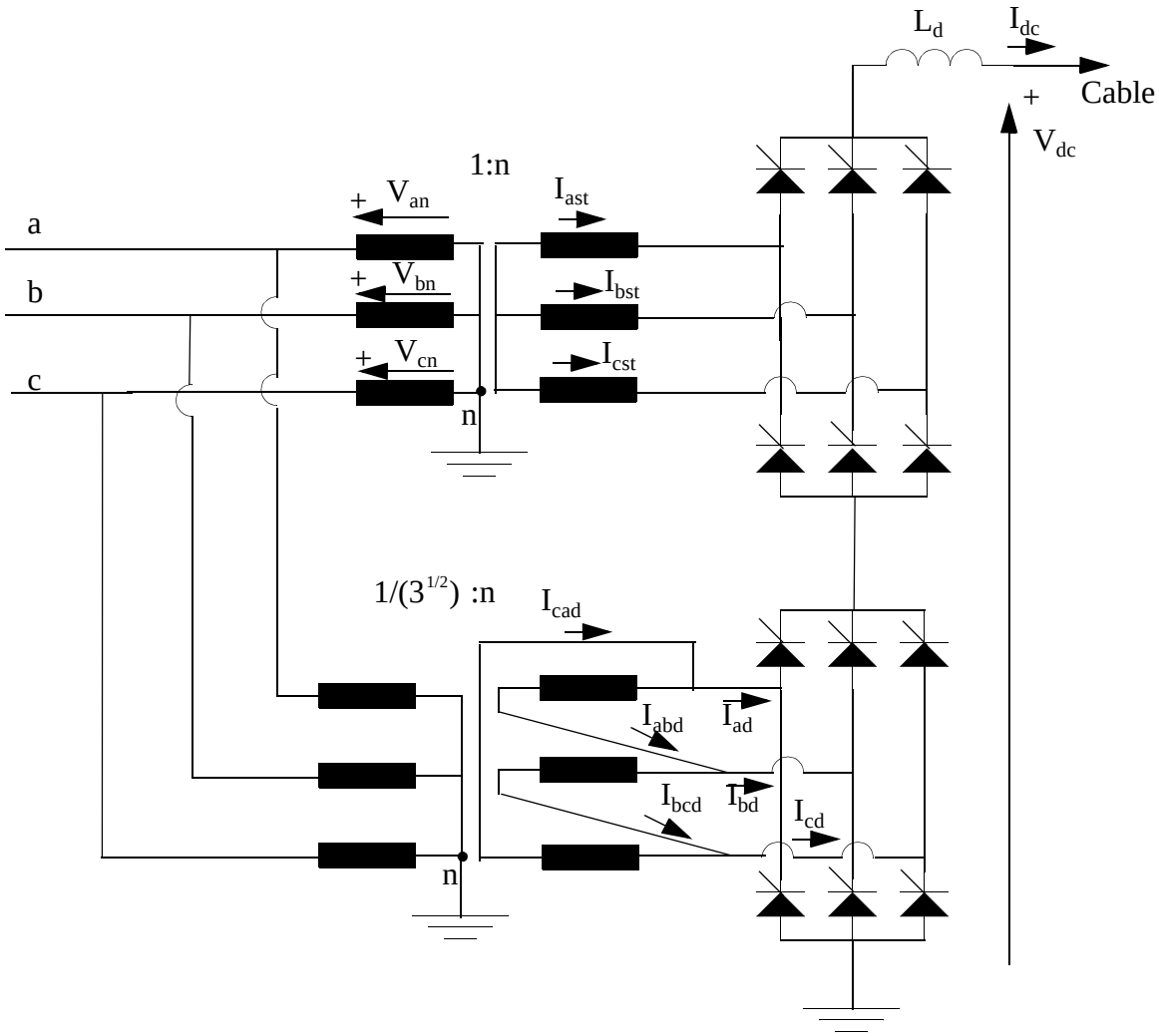


Figure 3.1 Twelve pulse HVDC converter

*** Example 3.1 (relates to Figure 3.1)

It is assumed that the AC voltages V_{an} , V_{bn} , and V_{cn} are perfectly symmetrical and have the frequency 50 Hz. I_{dc} has a perfect DC component and a 50 Hz component which is in phase with the AC voltage V_{an}. The fire angle is 30 degrees, and the commutation angle is assumed to be zero. The transformers are assumed to be ideal and their saturation is ignored. The transformer ratio n is assumed to be one.

To clearly illustrate the currents and voltages that appear under these idealized conditions, the 50 Hz component in the DC current has a peak-to-peak value as large as the value of the DC component in the DC current. The illustrations are made by drawing the currents and voltages by hand. The drawings are shown in Figures 3.2-3.12.

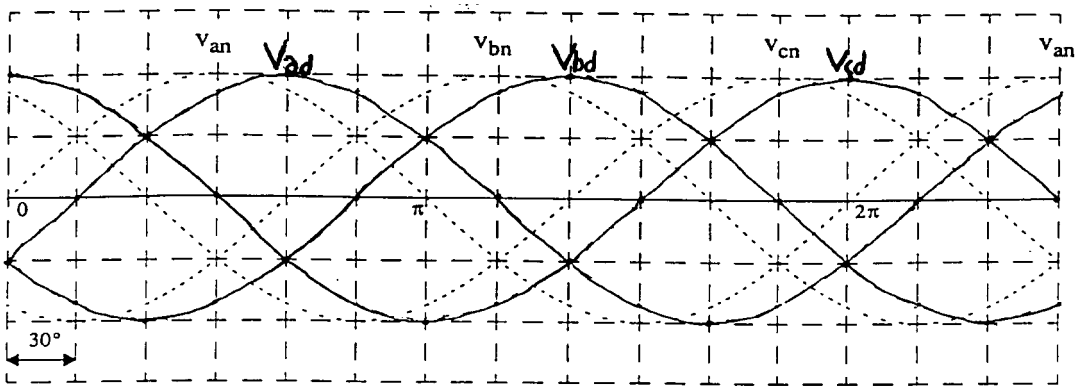


Figure 3.2 V_{an}, V_{bn}, V_{cn}, and the fictitious voltages V_{and}, V_{bnd}, V_{cnd}

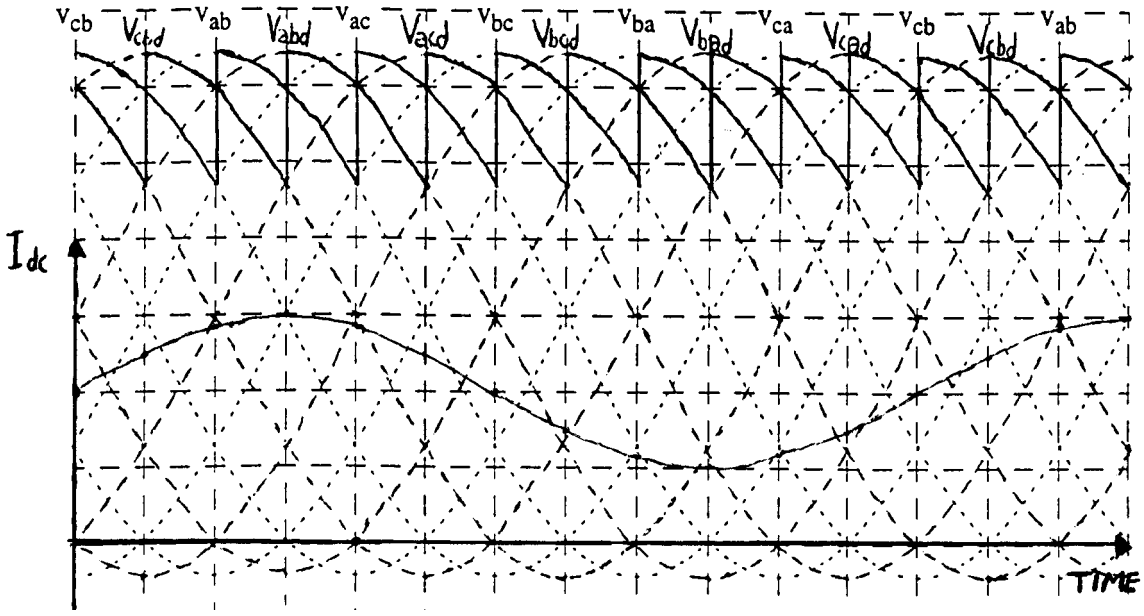


Figure 3.3 I_{dc}, V_{ab}, V_{abd}, V_{ac}, V_{acd}, V_{bc}, V_{bcd}, V_{ba}, V_{bad}, V_{ca}, V_{cad}, V_{cb}, V_{cbd}

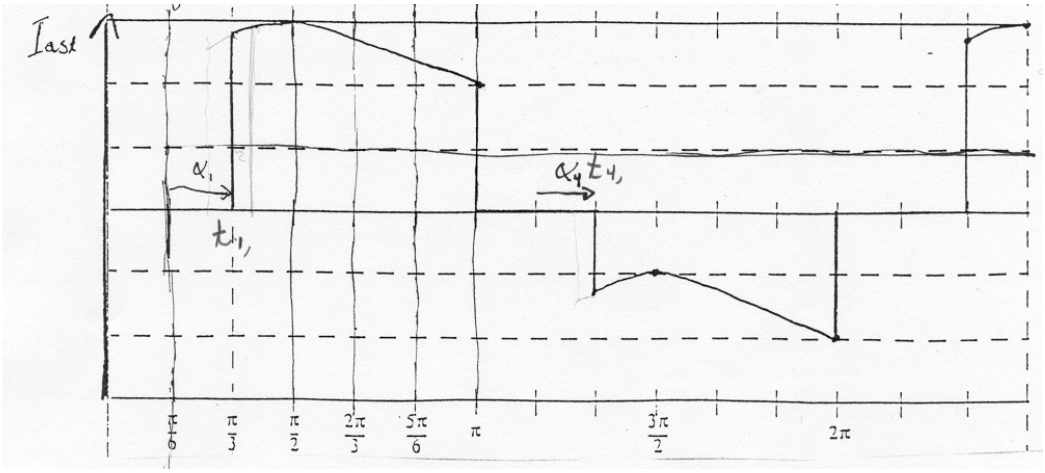


Figure 3.4 I_{ast}

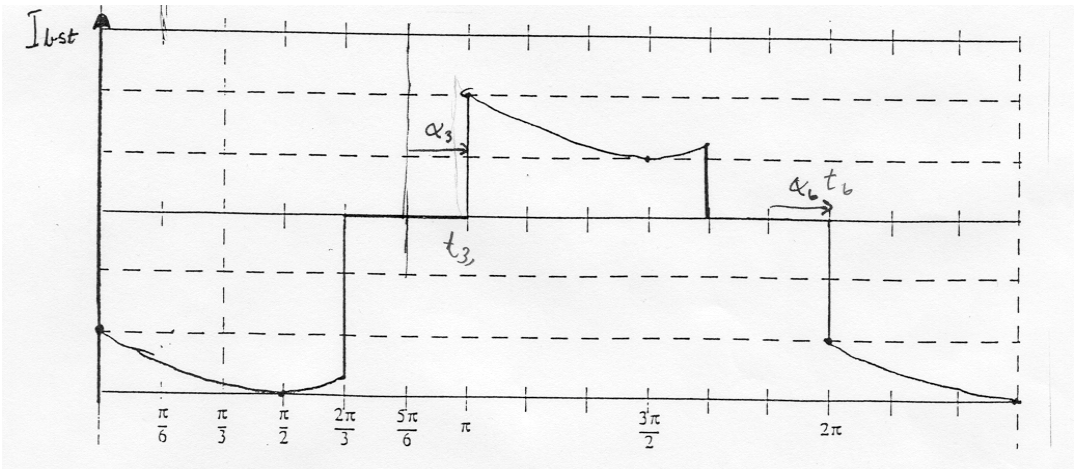


Figure 3.5 I_{bst}

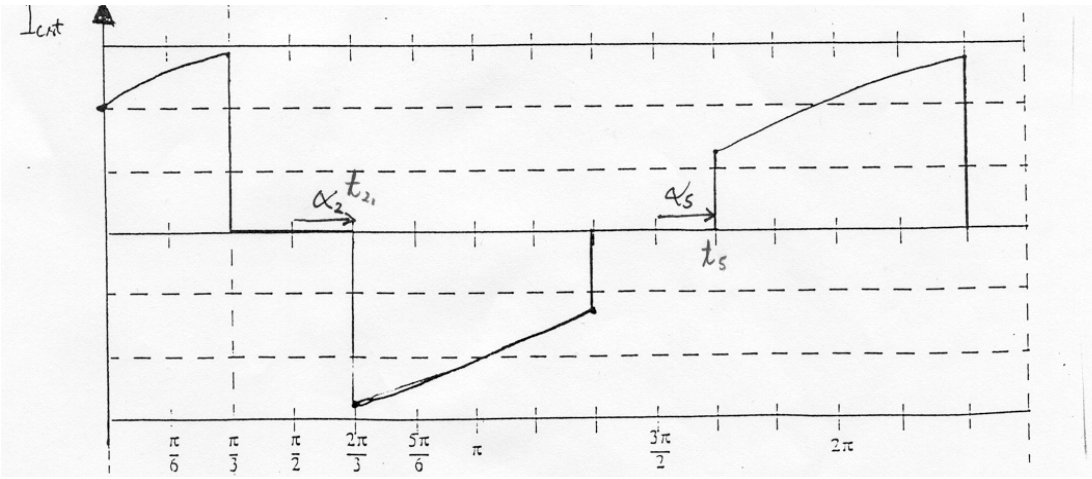


Figure 3.6 I_{cst}

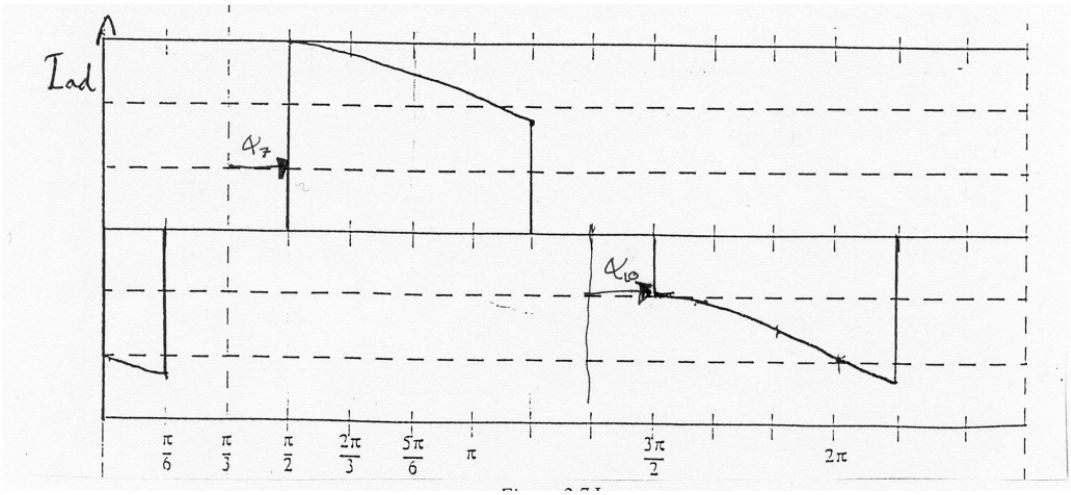


Figure 3.7 I_{ad}

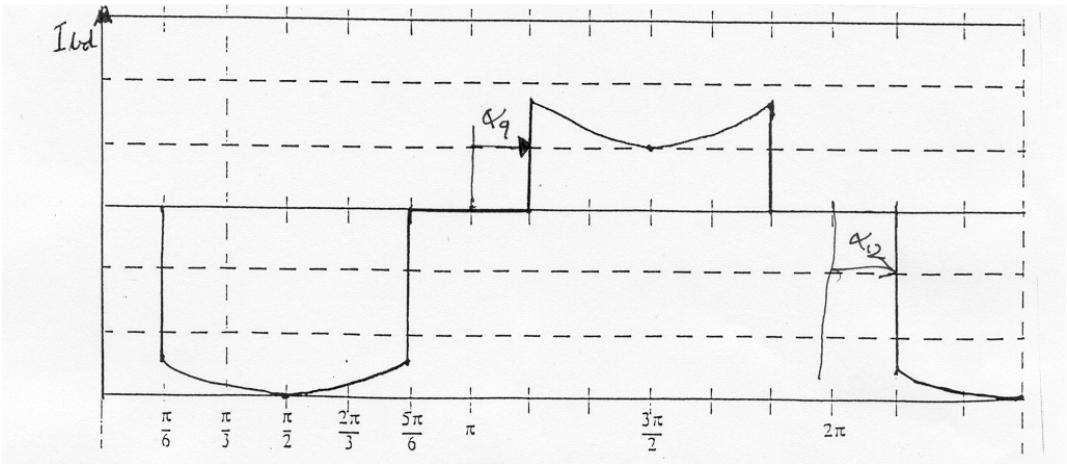


Figure 3.8 I_{bd}

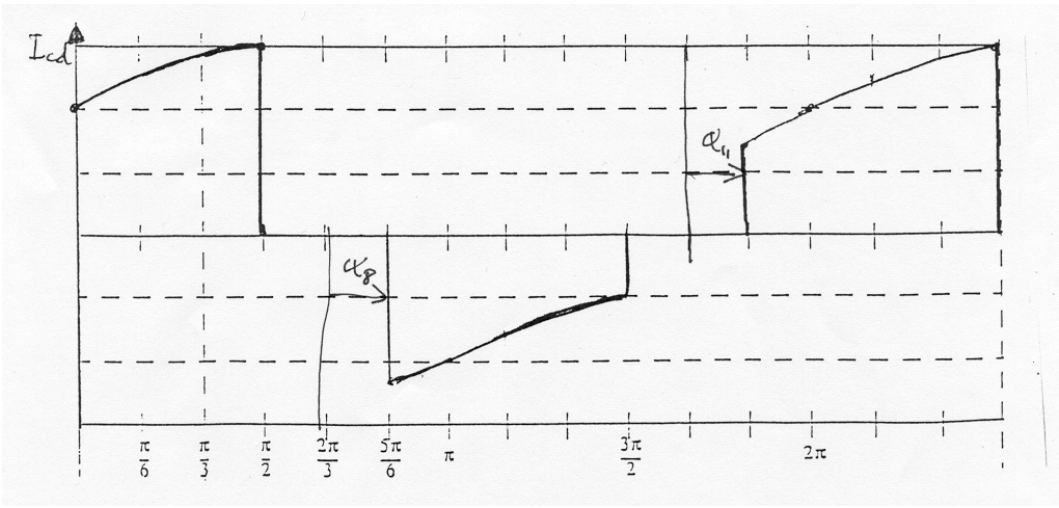


Figure 3.9 I_{cd}

URN:NBN:no-2111

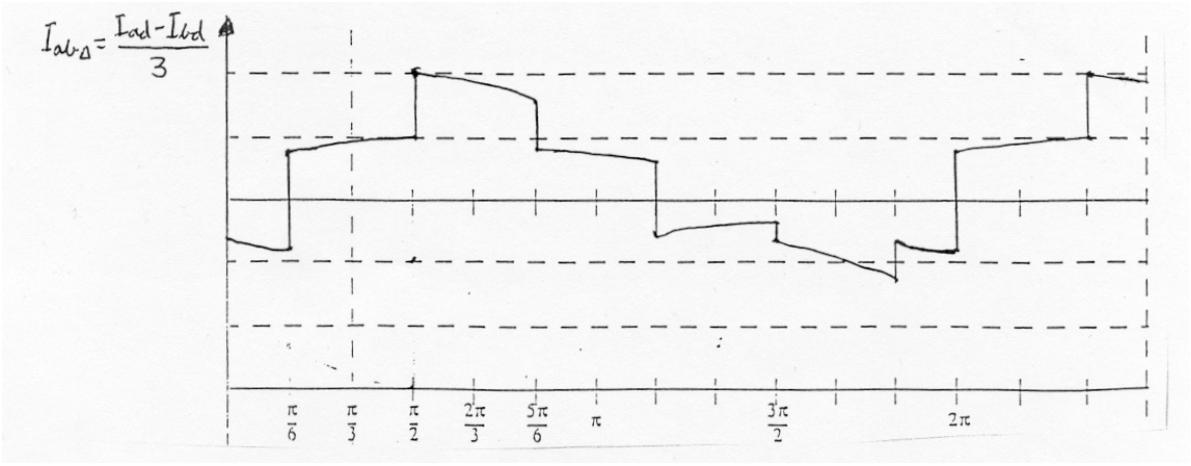


Figure 3.10 I_{abd}

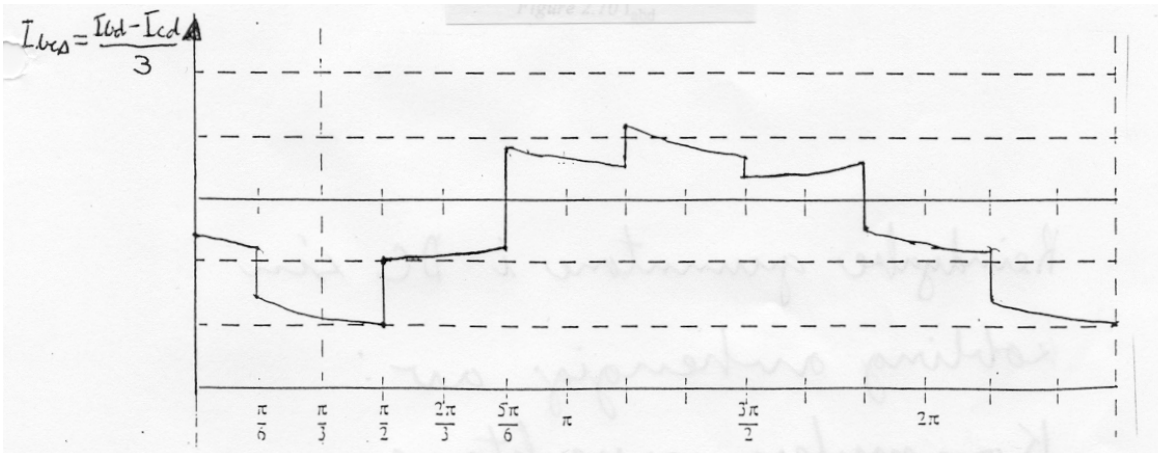


Figure 3.11 I_{bcd}

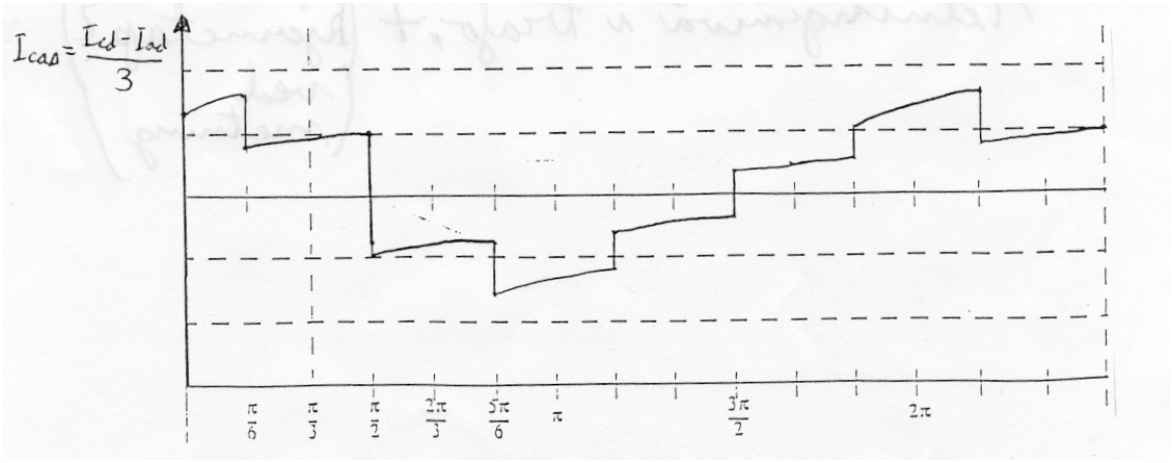


Figure 3.12 I_{cad}

URN:NBN:no-2111

It is seen from Figures 3.4-3.6 that I_{ast} has a positive DC component, I_{bst} has a negative DC component, and I_{cst} has no DC component. It is also clear that the sum of these currents are zero.

Figure 3.7 and 3.9 show that I_{cd} and I_{ad} have positive DC components which are equal in magnitude. The DC component of I_{bd} is negative according to Figure 3.8. It is not obvious from the Figures that the sum of these DC components is zero. However, when analysing the currents flowing in the delta winding (see Figures 3.10-3.12), it becomes clear that the DC components in these currents in sum are zero. The DC components of I_{abd} and I_{bcd} have the same absolute value, but the DC component of I_{abd} has an opposite sign of the DC component I_{bcd}. I_{cad} has no DC component.
***

The example above shows that under ideal conditions a fundamental frequency component in the DC side current will cause DC components with different magnitudes in the AC side currents flowing into the secondary windings of the converter transformers. According to Section 2.2.3 also a positive sequence second harmonic current will flow on the AC side because of the fundamental component in the DC side current. This is not obvious from the example above. However, both the generation of DC components and the positive sequence second harmonic currents on the AC side are essential in the generation of core saturation instability.

3.2 The magnetizing of a transformer

The magnetizing characteristics of converter transformers play an important role in the development of core saturation instability. It is therefore essential in this context to know how the magnetizing characteristics are generated and which parameters that influence the B-H curves during operation of the transformers. To make these considerations less complicated only a one-leg transformer is considered. For background theory to this section see [31].

3.2.1 The B-H curve

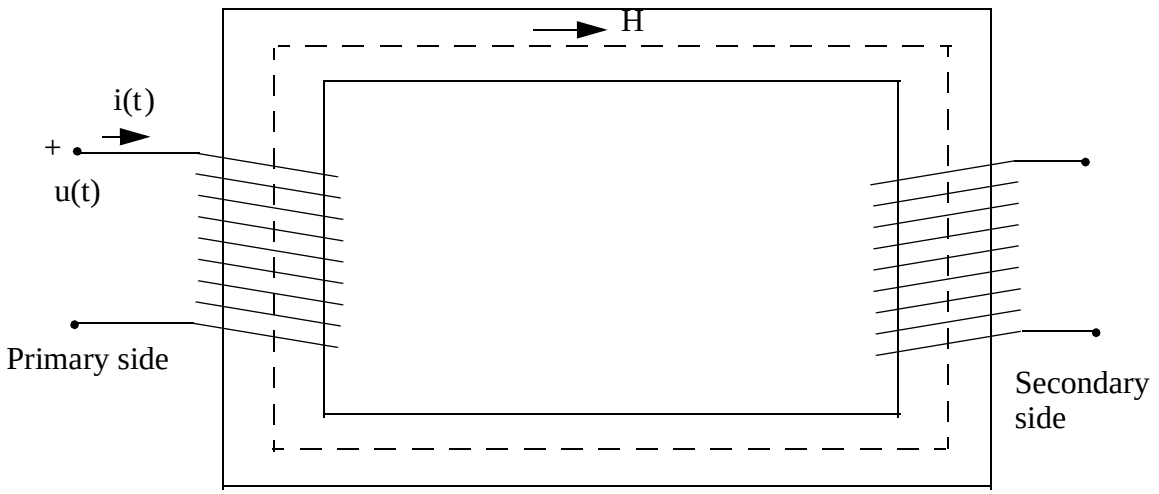


Figure 3.13 An iron core magnetized by the current i(t)

The average iron length is *l*. The cross-section area of the iron core is constant and equals *A*.

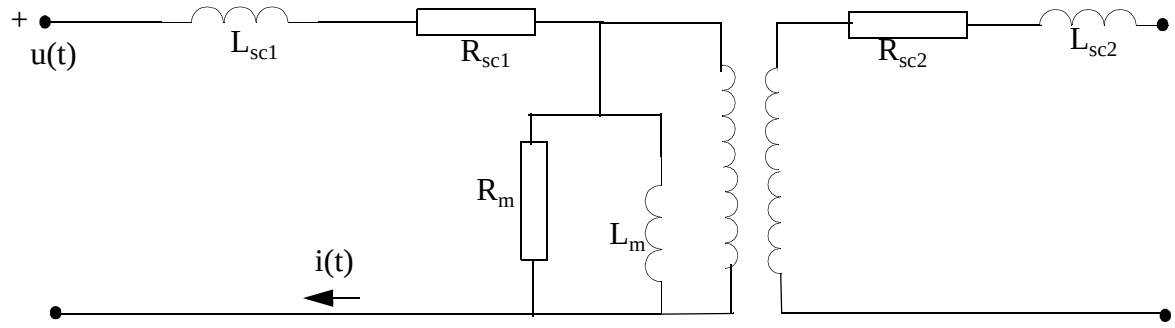


Figure 3.14 Electrical equivalent circuit of the transformer

The leakage inductances L_{sc1} and L_{sc2} are considered to be much less than the magnetizing inductance L_m. During 50 Hz operation the winding resistances R_{sc1} and R_{sc2} are much less $X_1 = 2\pi \cdot 50 \cdot L_{sc1}$ and $X_2 = 2\pi \cdot 50 \cdot L_{sc2}$. The resistance R_m in the magnetizing branch due to eddy currents and hysteresis in the iron is much larger than $X_m = 2\pi \cdot 50 \cdot L_m$ at 50 Hz operation.

Open secondary windings

Because of the current *i(t)* an H-field will be generated inside the iron core. The direction and magnitude of the H-field is given by the direction and magnitude of *i(t)* (the right-hand rule).

$$\oint_l H(t)dl = N \cdot i(t) \Rightarrow H(t) \cdot l = N \cdot i(t) \Rightarrow H(t) = \frac{N \cdot i(t)}{l} \tag{3.1}$$

The magnetic flux $\Phi(t)$ in the iron core has approximately the following relationship with the applied voltage *u(t)*:

$$u(t) = N \cdot \frac{d\Phi}{dt} \tag{3.2}$$

The relationship between the magnetic flux density *B(t)* and the magnet flux $\Phi(t)$:

$$\Phi(t) = B(t) \cdot A \tag{3.3}$$

There is a non-linear relationship between the flux density *B(t)* and the magnetic field *H(t)*. The magnetizing curve of the iron core has a typical characteristic like the one shown in Figure 3.15.

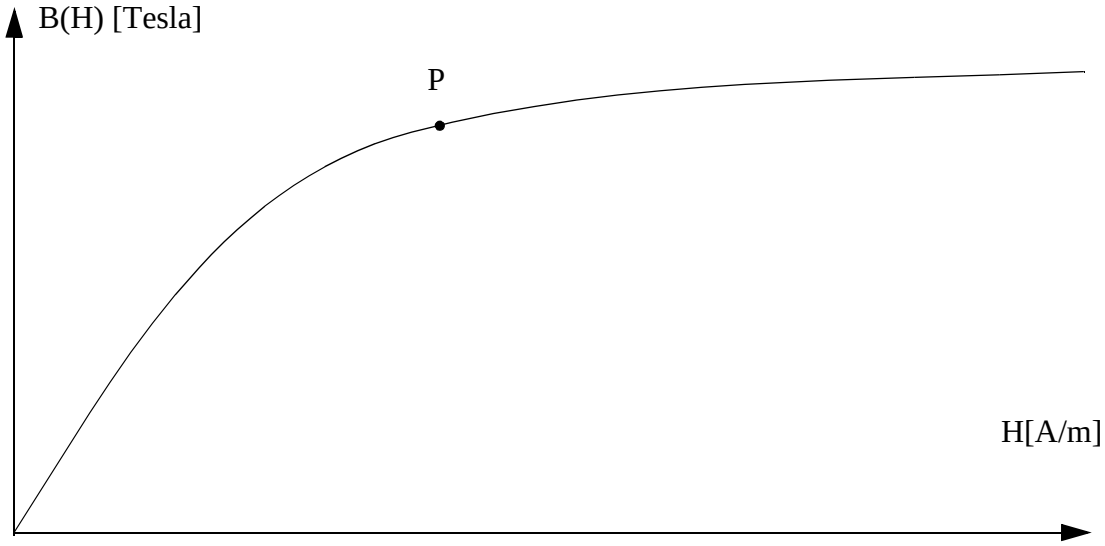


Figure 3.15 Magnetizing curve of the iron core

It is assumed that the applied H-field is increased from zero until it has the value which corresponds to the point P on the saturation curve in Figure 3.15. When decreasing the H-field to zero again the magnetic flux density will not decrease to zero but to a positive value B_r. This is called hysteresis and is the result of how the domain magnetic moments inside the iron core are reoriented when the applied field is removed. If there is a cyclic variation in the applied H-field the B-H hysteresis loop is obtained. A typical B-H hysteresis loop when the applied magnetic field is an AC field is shown in Figure 3.16.

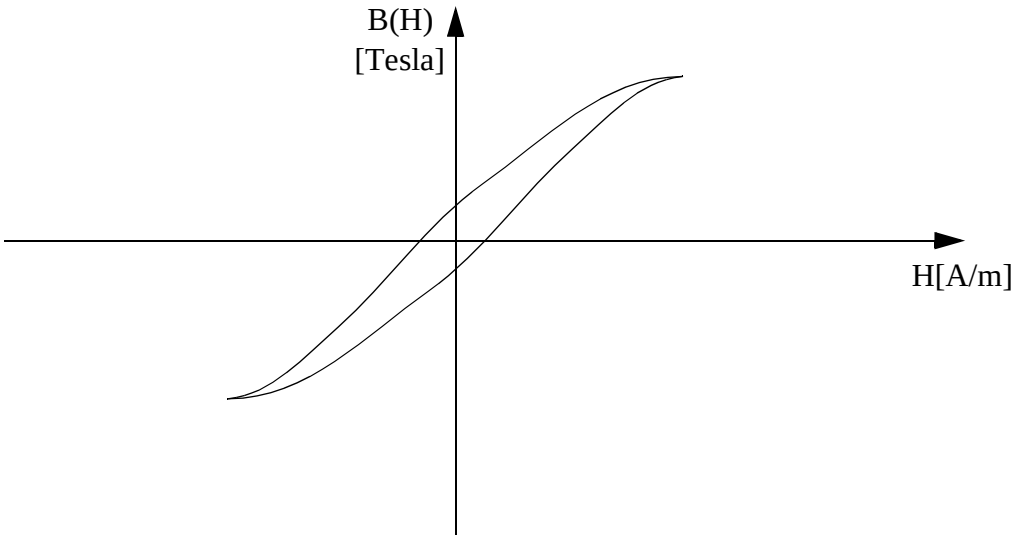


Figure 3.16 Typical hysteresis loop for an iron core when an AC magnetic field is applied

Because of the non-linear B-H loop, the current *i(t)* will not be sinusoidal. It will generate odd harmonics with predominance of the third harmonic. The typical waveform of *i(t)* is shown in Figure 3.17. The fundamental frequency is 50 Hz.

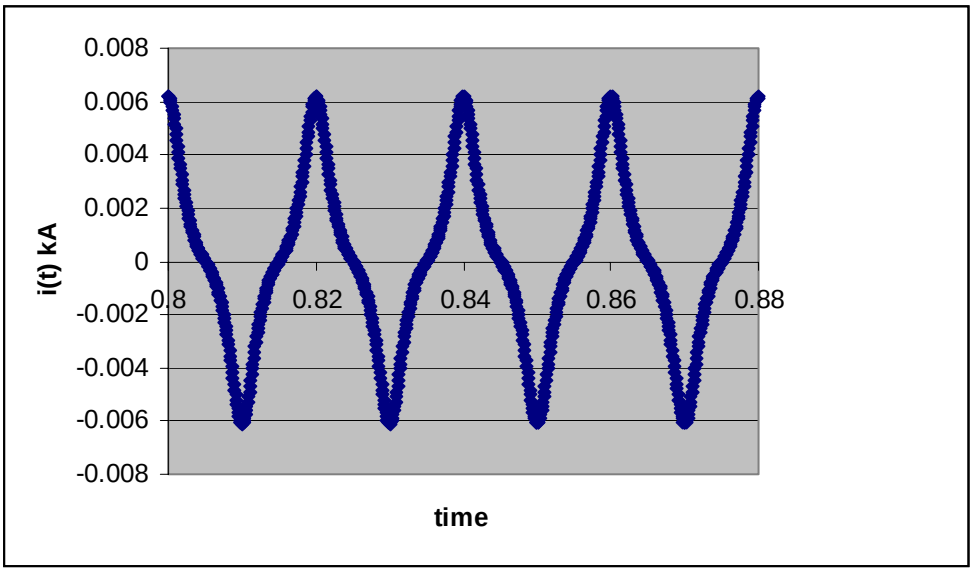


Figure 3.17 Typical waveform of a magnetizing current in a transformer

A DC current source on the secondary winding

The scheme for this is shown in Figure 3.18.

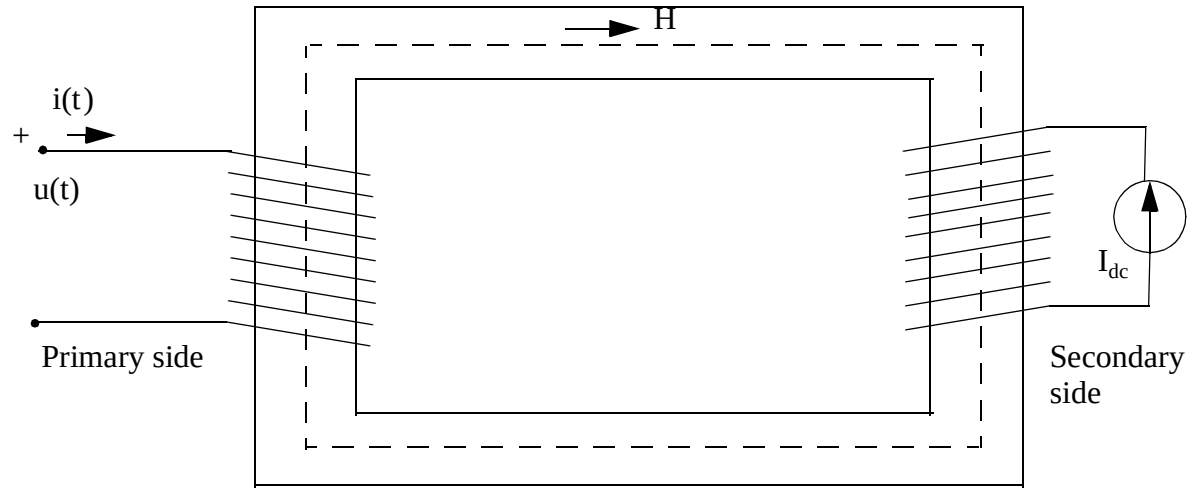


Figure 3.18 An iron core magnetized by the currents i(t) and I_{dc}

The applied H-field will now have a DC component H_{dc}:

$$H_{dc}(t) = \frac{N \cdot I_{dc}}{l} \tag{3.4}$$

The AC component of the H-field:

$$H_{ac}(t) = \frac{N \cdot i(t)}{l} \tag{3.5}$$

URN:NBN:no-2111

The total H-field in the iron core:

$$H(t) = H_{ac}(t) + H_{dc}(t) = \frac{N \cdot i(t)}{l} + \frac{N \cdot I_{dc}}{l} \tag{3.6}$$

In the following reasoning it is assumed for all practical purposes that the current *i(t)* does not influence the voltage *u(t)*.

It is assumed that the voltage *u(t)* on the primary side of the transformer is the same as in the case when the secondary side was open circuited. Then the varying flux in the transformer is the same as in the case of the open circuited secondary side (see Equation (3.2)). This causes the varying B-field in the iron core to be as it was when the secondary side was open circuited (see Equation (3.3)). The DC current I_{dc} causes the flux density to have a DC bias. This can easily be obtained by using the following relationship:

$$B(t) = \mu_0 \cdot \mu_r \cdot H(t) \tag{3.7}$$

μ_0 is the permeability in air ($4\pi \cdot 10^{-7}$ H/m)
μ_r is the relative permeability in iron (typical 5000 in the linear area)

By using Equations (3.6) and (3.7) it is easy to see that the B-field will have one AC and one DC component. When the iron starts to saturate (which means that H(t) becomes large) then μ_r decreases, but Equation (3.7) is still valid. Thus *B(t)* will always have a DC-component when *H(t)* has a DC component.

Since the B-field varies as much as during the open circuit operation and in addition has a DC component the iron core will now be skew magnetized. The DC component of the B-field causes the iron core to be saturated in one half of the fundamental cycle. This is illustrated in Figure 3.19.

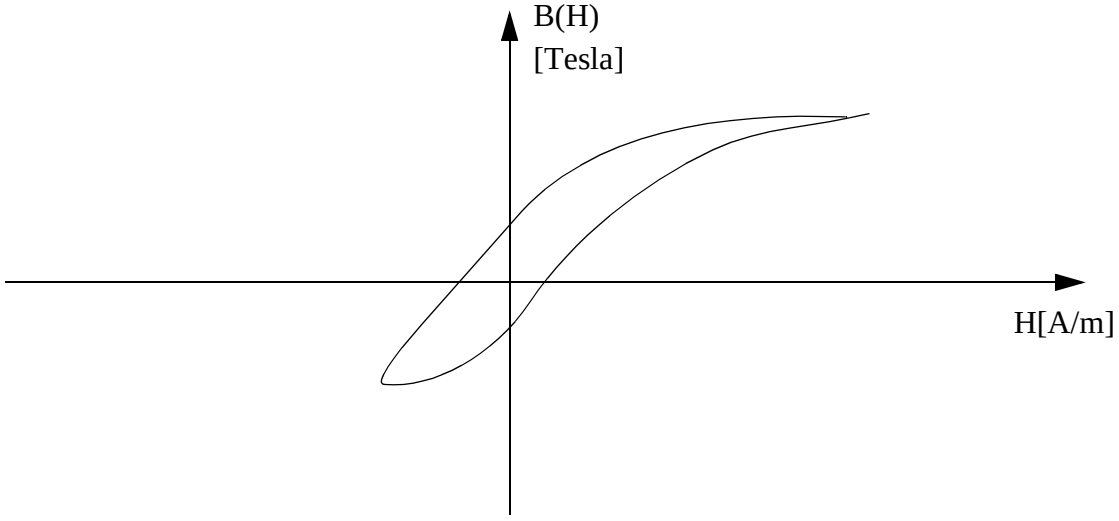


Figure 3.19 B-H loop of a skew magnetized iron core

In the case of a B-H loop as in Figure 3.19, the current *i(t)* typically has a waveform like the one shown in Figure 3.20.

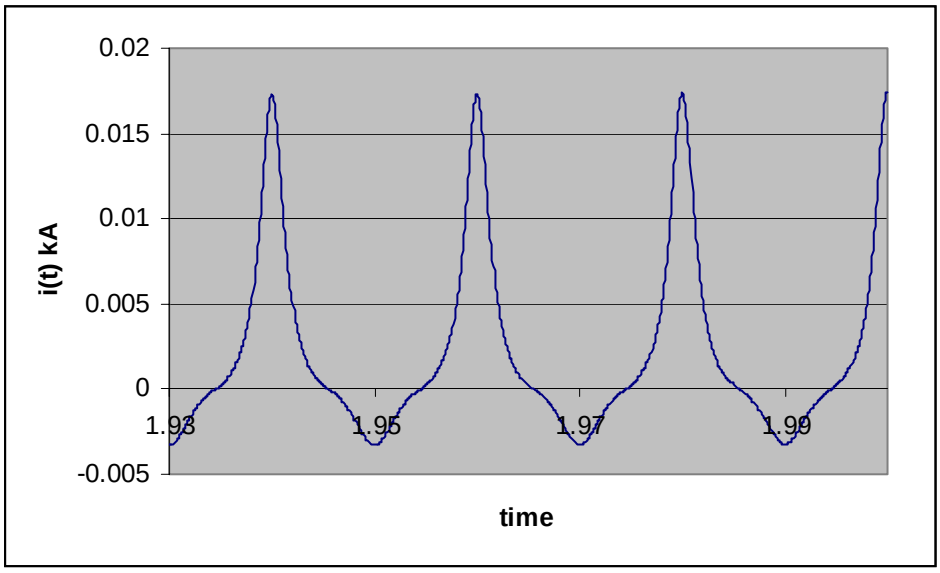


Figure 3.20 Typical waveform of the transformer's magnetizing current in a skew magnetized core

Except for the DC component, the harmonic components in the magnetizing current will be provided from the primary side. The DC component in the magnetizing current is provided from the DC current source on the secondary side. Figure 3.21 is used as a tool to explain this.

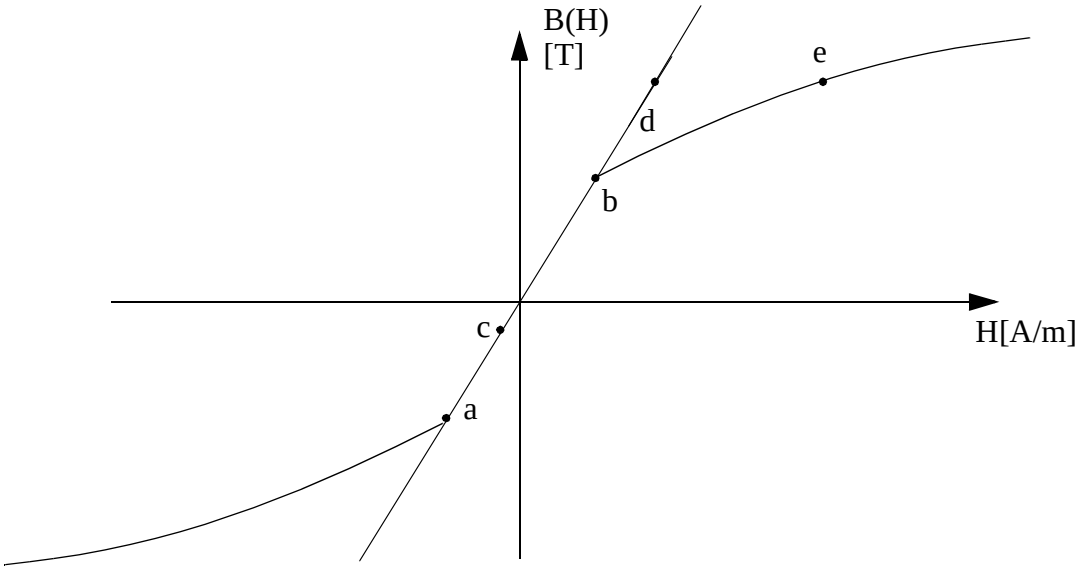


Figure 3.21 Linear and non linear magnetizing curves

Hysteresis is ignored to simplify the explanation, but nevertheless the conclusion would be the same even if hysteresis is not ignored (because the iron core becomes more non-linear when it starts to saturate in both cases). The applied primary side voltage is assumed to be the same whether a DC current exists in the secondary side windings or not.

Linear magnetizing curve

First it is assumed that no DC current is applied on the secondary side of the transformer. Then the B-H loop will start at point a, reach its maximum positive value at point b, and end back at

point a. Because of the linearity of the iron the current i(t) will be sinusoidal.

If a DC current is applied at the secondary side the B-H loop will start at point c, reach its maximum positive value at point d, and end back at point c. i(t) will still be purely sinusoidal.

Non-linear magnetizing curve

If no DC current is applied on the secondary side of the transformer the B-H loop will vary between point a and point b.

If a DC current is applied on the secondary side of the transformer the iron core becomes saturated. The B-H loop will vary between point c and point e. This causes the H-field in the transformer to increase dramatically in one of the half periods, compared to the case with a linear magnetizing curve. Since the H-field is proportional to the magnetizing current there will also be a dramatic increase in the magnetizing current in one of the half periods, compared to the case with a linear magnetizing curve. Therefore the non-linearity in the iron core will cause an increase in the magnetizing current component which is supplied from the primary side of the transformer. This will cause the transformer to be a harmonic current source at the primary side, and harmonic currents of order 2,3,4 .... are generated. The harmonic components in the magnetizing current decrease with increasing order.

3.3 Resonances on the AC and DC sides of an HVDC converter

3.3.1 Parallel resonance

If a circuit has a parallel resonance, then a small current with magnitude I_p and with frequency at or near the parallel resonance frequency will cause a relatively large voltage V_{busa} across the impedance in the circuit. If I_p is applied to the circuit at frequencies that are not near the resonance frequency the voltage V_{busa} will not be particular large.

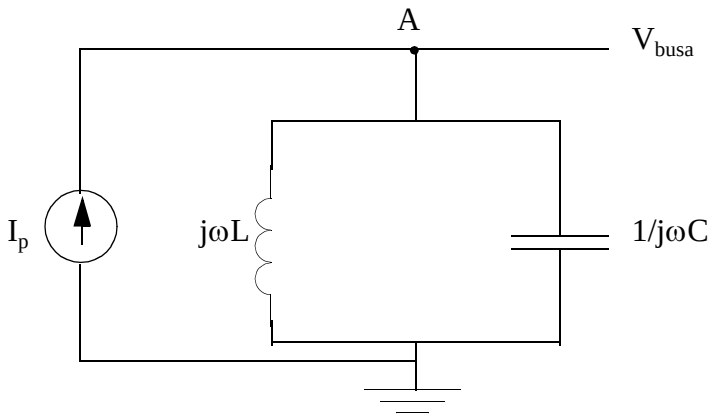


Figure 3.22 Circuit with parallel resonance

The impedance Z_p seen from bus A is given by:

$$Z_p = \frac{L/C}{j\left(\omega L - \left(\frac{1}{\omega C}\right)\right)} \tag{3.8}$$

If the angular frequency ω of the current I_p is $\omega = \omega_n = \frac{1}{\sqrt{LC}}$ then the voltage V_{busa} will become infinity because Z_p will be infinite. In this case the circuit is operated at its resonance frequency ω_n. For I_p having all other frequencies than ω_n, the circuit is not in its parallel resonance condition. Nevertheless for frequencies of I_p near the resonance frequency the circuit will have a very high impedance. In real life both the inductance L and the capacitance C will have a resistive part. This will cause Z_p to not be infinite at the resonance frequency, but the resonance frequency will still be $\omega_n = \frac{1}{\sqrt{LC}}$.

The typical shape of the magnitude of Z_p as a function of frequency is shown on Figure 3.23.

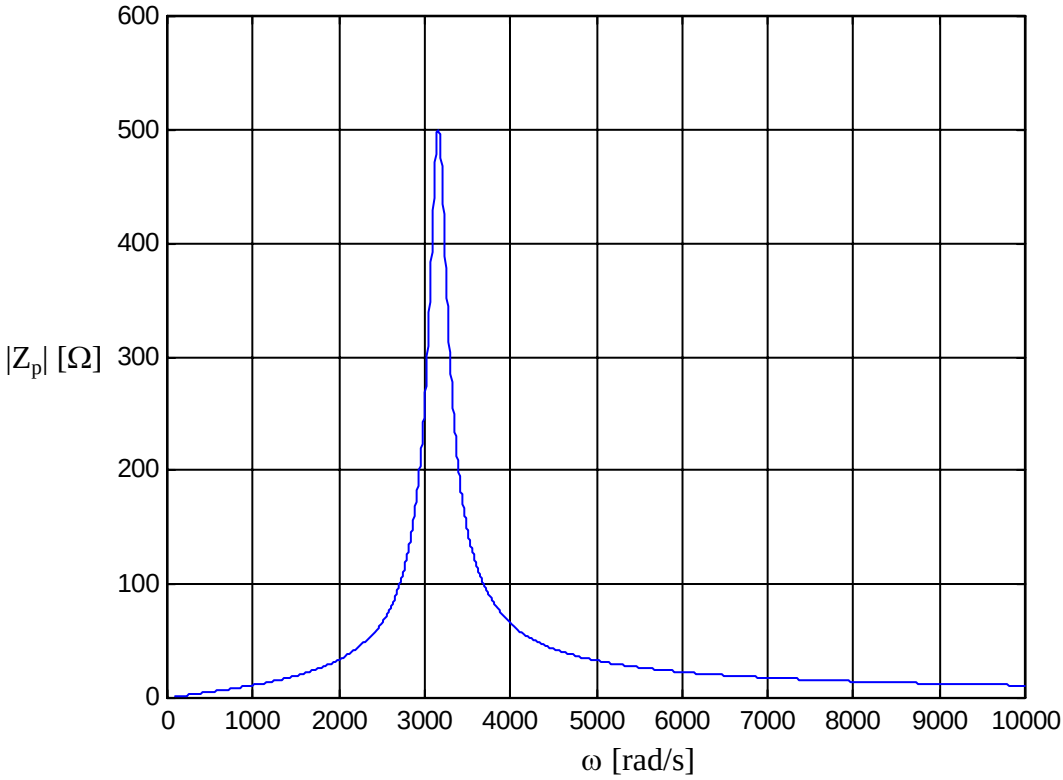


Figure 3.23 Typical shape of the magnitude of Z_p as a function of frequency

It turns out that Z_p is inductive when the frequency is below the resonance frequency, and capacitive when the frequency is above the resonance frequency. At the resonance frequency, Z_p is purely resistive. A typical plot of the phase angle of Z_p as a function of frequency is shown in Figure 3.24. The resistivity in L causes the phase angle to be less than 90 degrees at low frequency (0 degrees at DC).

URN:NBN:no-2111

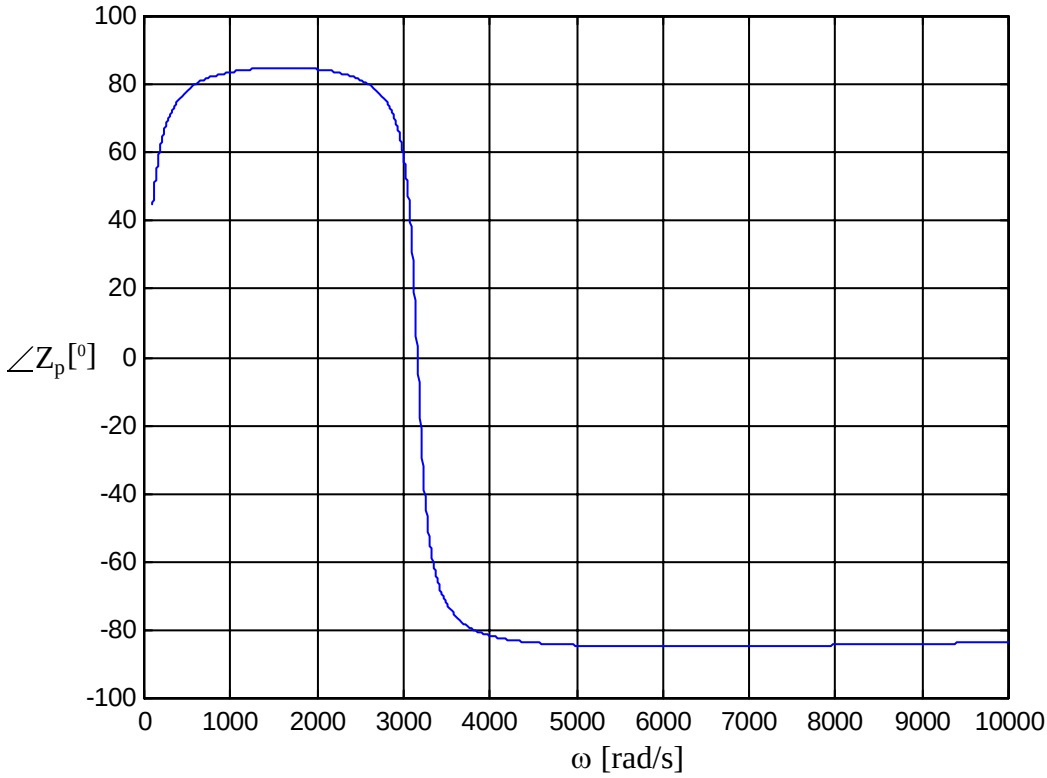


Figure 3.24 Typical shape of the phase angle to Z_p as a function of frequency

3.3.2 Series resonance

If a circuit has a series resonance, then a small voltage with magnitude V_s and with frequency at or near the series resonance frequency will cause a large current to flow compared to when the voltage with magnitude V_s is applied to the circuit at frequencies that are not near the resonance frequency.

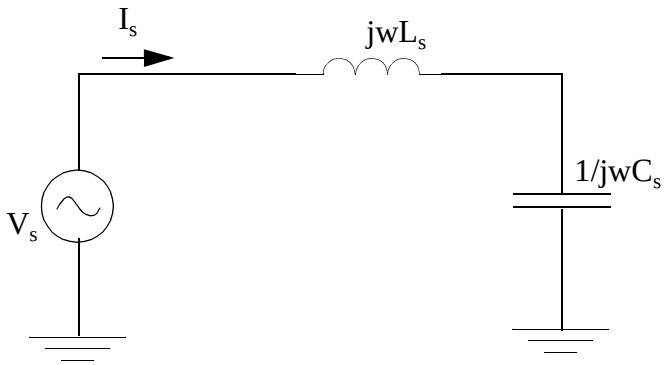


Figure 3.25 Circuit with series resonance

URN:NBN:no-2111

The impedance Z_s seen from the voltage source in Figure 3.25 is:

$$Z_s = j\left(\omega L_s - \frac{1}{\omega C_s}\right) \tag{3.9}$$

If the angular frequency ω of the voltage V_s becomes $\omega = \omega_n = \frac{1}{\sqrt{L_s C_s}}$ then the current I_s becomes infinity and the circuit is said to be operated at its series resonance frequency ω_n. If V_s has a different frequency than ω_n, the circuit is not operated at its series resonance condition. In real life there will also be a resistivity in series with the inductance and capacitance. This will cause the current I_s to be damped (the larger the resistivity is, the more I_s will be damped). Thus I_s will not be infinity at ω_n, but ω_n is still given by $\omega_n = \frac{1}{\sqrt{L_s C_s}}$.

The typical shape of the magnitude of Z_s as a function of ω is shown in Figure 3.26.

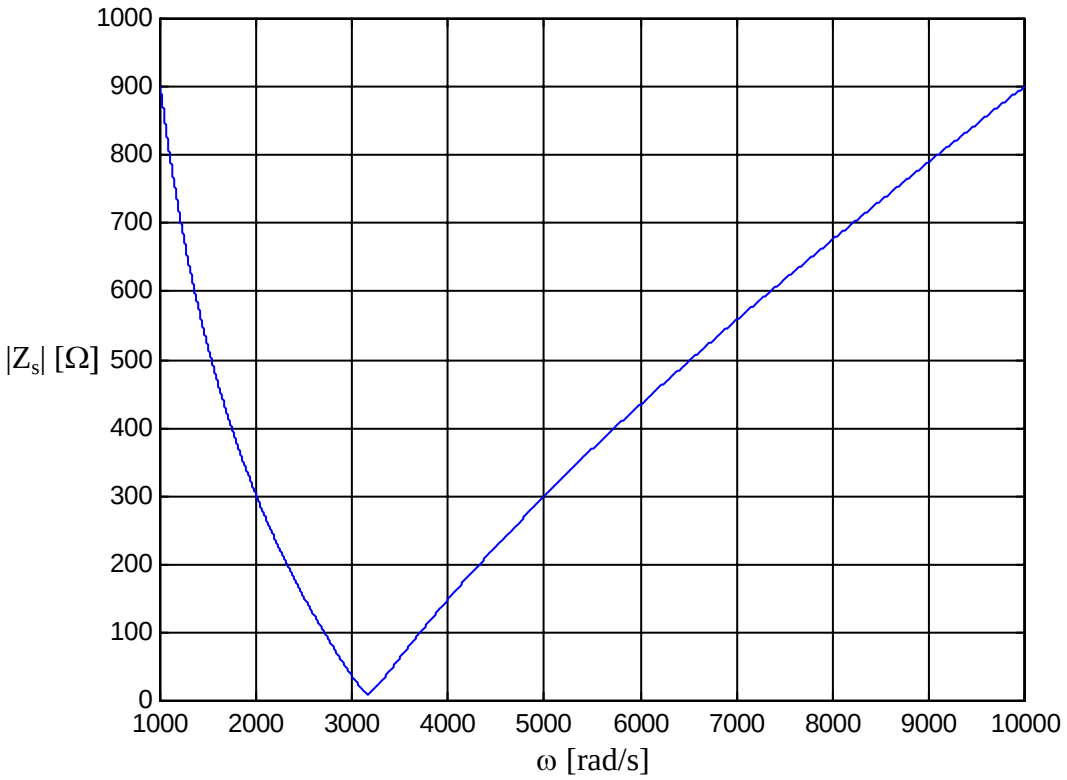


Figure 3.26 Typical shape of the magnitude of Z_s as a function of frequency

For all frequencies below the resonance frequency the impedance of Z_s will be capacitive, and for all frequencies above the resonance frequency the impedance of Z_s will be inductive. At the resonance frequency Z_s is purely resitive. A typical shape of the phase to Z_s as a function of frequency is shown in Figure 3.27.

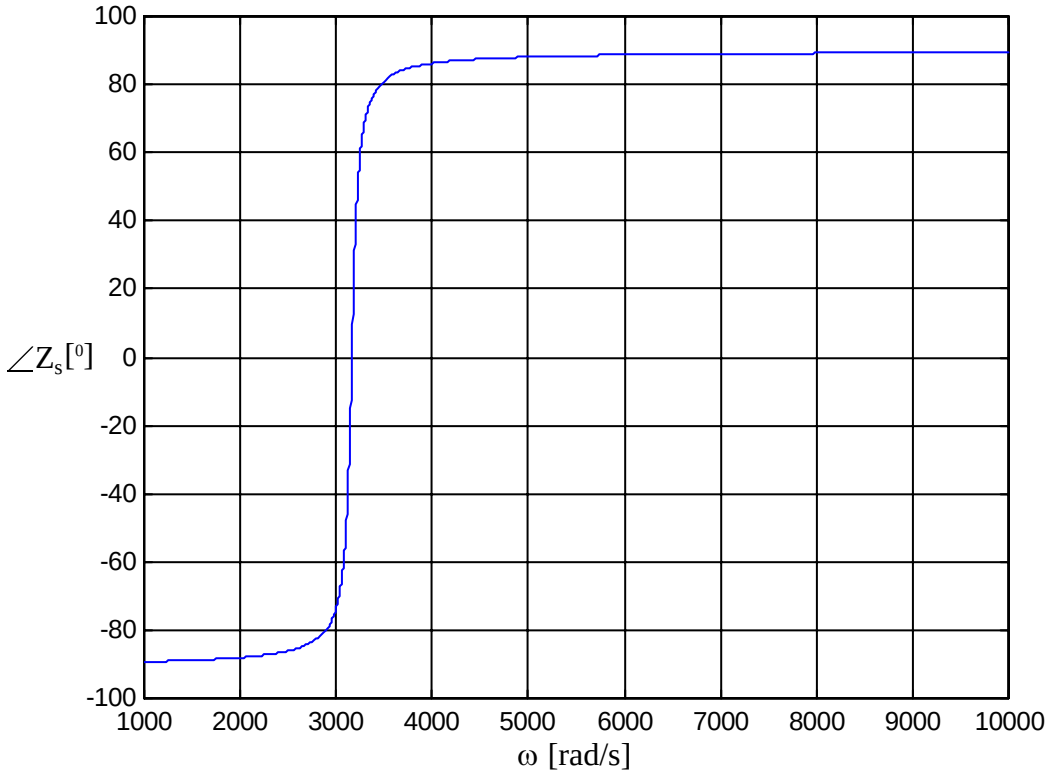


Figure 3.27 Typical shape of the phase to Z_s as a function of frequency

3.4 The HVDC control system

Before the measured current I_{ad} enters the control system in Figure 2.25 it is lowpass filtered to hinder that the harmonic components of it are entering the control system (see Figures 2.18 and 2.20). Nevertheless, the break point on characteristic of the lowpass filter may be higher than the fundamental frequency of the AC networks to ensure satisfying response due to load changes and set point changes. Thus, if there exists a fundamental frequency component in I_{ad} it may enter the control system and create a 50 Hz variation in the fire angle order. Under idealized conditions this will according to Section 2.2.3 generate a fundamental frequency variation in the DC side voltage of the converters. In this way the control system may contribute to the development of core saturation instability.

3.5 Core saturation instability

AC-DC systems with low short-circuit ratios (SCR) [2, p.130] often experience instability in the form of waveform distortion. The low SCR gives an indication of a high AC system impedance, with an inductance which may resonate with compensating capacitors and harmonic filters at the terminal of the HVDC converter. The parallel resonance may be as low as near or at the second harmonic frequency. Under such conditions core saturation instability may develop.

3.5.1 The mechanism of core saturation instability

The mechanism of core-saturation instability can be explained by using the block diagram on Figure 3.28.

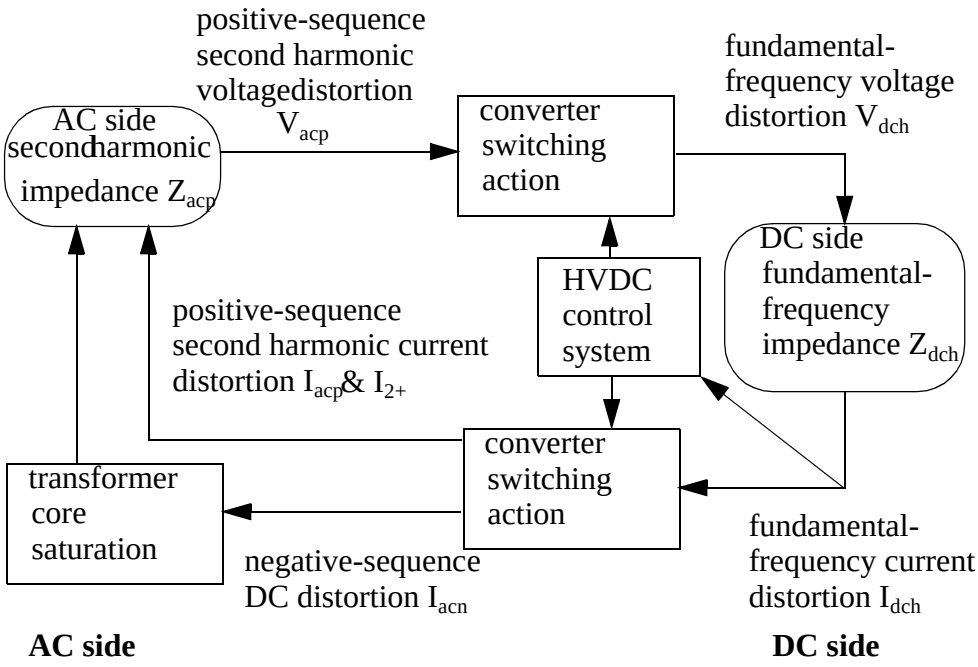


Figure 3.28 Mechanism of core-saturation instability. Based on [12].

If a small-level positive-sequence second harmonic voltage V_{acp} exists on the AC side of the converter, a fundamental frequency voltage V_{dch} will appear on the DC side of the converter due to the converter switching action. A fundamental frequency current I_{dch} will then flow through the DC side impedance. The size of I_{dch} depends on the DC side impedance, if there is a series resonance near fundamental frequency on the DC side a relatively large current I_{dch} will flow even for a small value of $V_{dch.}$ Through the converter switching action the fundamental-frequency DC side current will cause a positive-sequence second harmonic current I_{acp} and a negative-sequence DC current I_{acn} to flow on the AC side. The phase currents corresponding to the negative-sequence DC current I_{acn} can be written as [12, p.182]:

$$I_{adc} = |I_{acn}| \cdot \cos(0 \cdot t + \delta + 0°) \tag{3.10}$$

$$I_{bdc} = |I_{acn}| \cdot \cos(0 \cdot t + \delta + 120°) \tag{3.11}$$

$$I_{cdc} = |I_{acn}| \cdot \cos(0 \cdot t + \delta + 240°) \tag{3.12}$$

δ is dependent on factors such as the fire angle, and the DC and the AC side impedance.

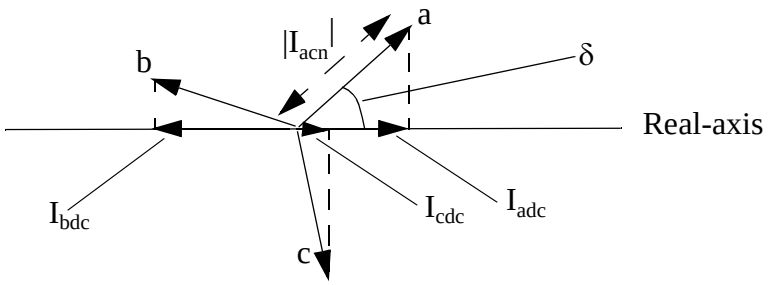


Figure 3.29 The negative-sequence DC produced by the HVDC converter

Because the frequency is zero, the phasors a, b, and c in Figure 3.29 will not rotate. Therefore I_{adc}, I_{bdc}, and I_{cdc} remains different but constant.

The phase currents corresponding to the positive-sequence second harmonic current I_{acp} can be written:

$$I_{a2+} = |I_{acp}| \cdot \cos(2\omega t) \tag{3.13}$$

$$I_{b2+} = |I_{acp}| \cdot \cos(2\omega t + 240°) \tag{3.14}$$

$$I_{c2+} = |I_{acp}| \cdot \cos(2\omega t + 120°) \tag{3.15}$$

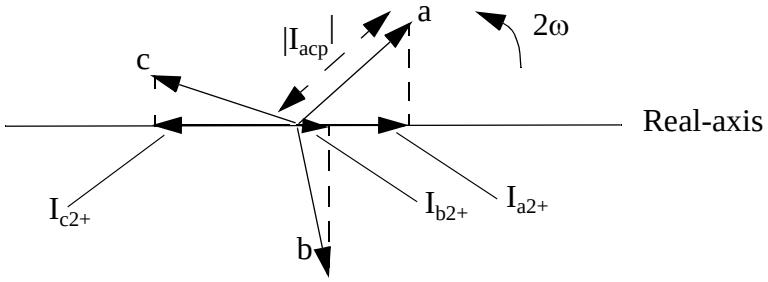


Figure 3.30 The positive-sequence second harmonic produced by the HVDC converter

The phasors a, b, and c in Figure 3.30 will rotate with angular speed 2ω. Therefore I_{a2+}, I_{b2+}, and I_{c2+} will vary sinusoidal between $-I_{acp}$ and I_{acp}.

Due to the dynamics of the instability, the DC side distortion is never exactly at the fundamental frequency [12, p.182]. Thus, the negative-sequence DC current I_{acn} is not true DC but is varying slowly. However, the variation is so slow that the phrase 'negative-sequence DC current' is used. The slow varying currents oriented in a negative-sequence format is referred to as DC currents. The DC currents flowing on the AC side will begin to saturate the converter transformers differently in each phase, resulting in a multitude of harmonic currents in the positive-, negative-, and zero-sequence being generated. This includes the positive-sequence second-harmonic current I_{2+}. This may cause a reinforcement in V_{acp}, especially if the impedance seen from the AC side busbar of the converter has a parallel resonance near the second harmonic frequency. The stability of the system is determined by the following factors:

a) The level of saturation obtained in the transformers due to the DC current magnetization

The more saturated the transformer becomes in the half cycle when it becomes saturated, the more positive-sequence second harmonic current will be generated due to the transformer saturation.

b) The DC side impedance

If the DC side impedance is small at the fundamental frequency, a relatively large fundamental frequency current will flow on the DC side of the converter when a small fundamental frequency voltage is present on the DC side of the converter. The phase angle of the DC side impedance will also influence the stability because the level of the DC current (and second harmonic positive-sequence current) in each phase on the AC side is determined by the phase angle between the fundamental frequency DC side current and the commutation voltages if the fire angle is kept constant.

c) The fire angle

The fire angle will influence the impedance seen from the AC side busbar of the converter. For instance if the thyristors in the converters are blocked or the fire angle is 90 degrees (neglecting the commutation angle) no power will flow from the AC side to the DC side, and thus the converter is seen as an infinite impedance from the AC side busbar. If the fire angle is 0 degrees the power flowing from the AC side to the DC side will have its maximum value, and thus the converter is seen as a finite impedance from the AC side busbar of the converter. In all cases when it flows power between the AC side and the DC side, the converter will seen from the commutation bus act as a finite impedance. Thus, even if the impedance seen into the AC network from the commutation bus has a parallel resonance at the second harmonic frequency, the true impedance seen from the commutation bus does not have a parallel resonance at the second harmonic frequency. In [32] it is shown how the true impedance seen from the commutation bus can be found. The fire angle also influences the level of DC current in each phase on the AC side of the twelve-pulse thyristor bridge. This is because the fire angle determines which part of the fundamental frequency DC side current that will flow in the different phases.

d) The impedance seen from the busbar at the AC side of the converter

If this impedance has a resonance frequency near the second-harmonic frequency and a low damping, a relatively small second harmonic positive-sequence current will cause a relative large second harmonic positive-sequence component in the busbar voltage. The phase angle of the AC side impedance will also influence the sensitivity of the system to core saturation instability because it decides the phase angle to the generated second harmonic voltages, and in this way also influences the phase angle of the fundamental frequency component in the DC side voltage. This will in turn decide the phase angle between the fundamental frequency component in the DC side current and the commutation voltages, and this way also the magnitude of the second harmonic positive-sequence current injected into the AC network and the magnitude of the negative-sequence DC-current injected into the AC network.

e) The control system of the HVDC converter

The DC current is measured and filtered in a lowpass filter that may has its cutoff frequency at such a level that the fundamental frequency component in the DC side current may cause a significant fundamental frequency variation in the fire angle order. In some cases this can contribute to core saturation instability. As a matter of fact it is very unlikely that core saturation instability will occur if not the HVDC controller is contribution to the development of it ([6]).

In points b) and d) it was explained that the characteristics of the AC and DC side impedances decide the level of fundamental harmonic current in the DC side network and the level of positive-sequence second harmonic current and negative-sequence DC current on the AC side. A HVDC rectifier system that is vulnerable to core saturation instability is likely to have the following impedance profile [6]:

- A low and predominantly capacitive DC side impedance at the fundamental frequency with the presence of a series resonance near to but higher than the fundamental frequency.

- A high and predominantly inductive AC side second-harmonic impedance with the presence of a parallel resonance near to but higher than the second harmonic frequency.

- A high AC side resistance near 0 Hz

For the HVDC inverter system that is vulnerable to core saturation instability the following impedance profile is typical according to [6] :

- A low and predominantly inductive DC side impedance at the fundamental frequency with the presence of a series resonance near to but lower than the fundamental frequency.

- A high and predominantly capacitive AC side second harmonic impedance with the presence of a parallel resonance near to but lower than the second harmonic frequency

- A high AC side resistance near 0 Hz

3.5.2 The implications of core saturation instability

When core saturation instability builds up, there will be an increase in the values of the magnetizing currents in the converter transformers. As shown in Section 3.2.1 this will cause an increase in the part of the magnetizing current which is provided by the AC network. Since the sum of the negative-sequence DC currents on the valve side of the converter transformers is zero, the transformer will be asymmetrically magnetized. It is for instance possible that in two of the phases the iron saturates when the voltages across the primary windings in those phases are in the half-cycle they are positive and not in the half-cycle they are negative, while the opposite is the case for the third phase. As a consequence of the asymmetrical magnetization, the currents flowing in the AC network due to the saturation in each phase of the transformer will be asymmetric. Thus there will flow additional positive-sequence, negative-sequence, and zero-sequence currents in the AC network. If the build up of core saturation instability has gone far enough, the size of one of the harmonic components of these zero-sequence currents will be higher than the zero-sequence protection level in the neutral conductor of the AC line feeding

the HVDC converter. This will cause tripping of the line. In other cases the increase in the harmonic components in the magnetizing current can cause filters to become overloaded and this might also cause line tripping by the protection [29]. It is emphasized that even though the fundamental frequency DC side current does not exceed a certain level, the effect of the magnified harmonic components in the magnetizing current may cause tripping due to overloading filters and activation of the zero-sequence protection.

4 Theory about methods to prevent core saturation instability

The focus of this chapter is different initiatives to prevent core saturation instability. These initiatives need to be considered in the light of their cost, their availability, and their influence on other harmonic phenomena or the operating of the HVDC link in general. As described earlier, core saturation instability is a phenomenon which consists of several factors. The way of preventing the phenomenon to occur is to eliminate or suppress one or more of the factors that leads to the phenomenon. In this chapter several ways of doing this are presented. Some of these are later shown by simulations in Chapter 7.

4.1 Stabilizing loop that eliminates the fundamental harmonic in the rectifier's fire angle

A variation with frequency *f* in the fire angle order of a twelve-pulse HVDC bridge causes a switching variation in the DC side voltage with frequency *f*, if *f* is less than six times the switching frequency of the HVDC converter. If *f* is more than six times the switching frequency of HVDC converter, the real fire angle of the HVDC bridge will not have a variation with frequency *f*. This is because of aliasing (see Figure 5.14). In Section 3.5 it was stated that core saturation rarely occurs without the contribution from the HVDC control system. The variation in the fire angle during development of core saturation instability will be close to the fundamental frequency in the AC grid (50 Hz). This is 12 times lower than the switching frequency. Thus, it is possible to use a stabilizing loop from the DC side voltage V_{dc} or current I_{dc} to the fire angle order when dealing with frequencies in the close vicinity of 50 Hz.

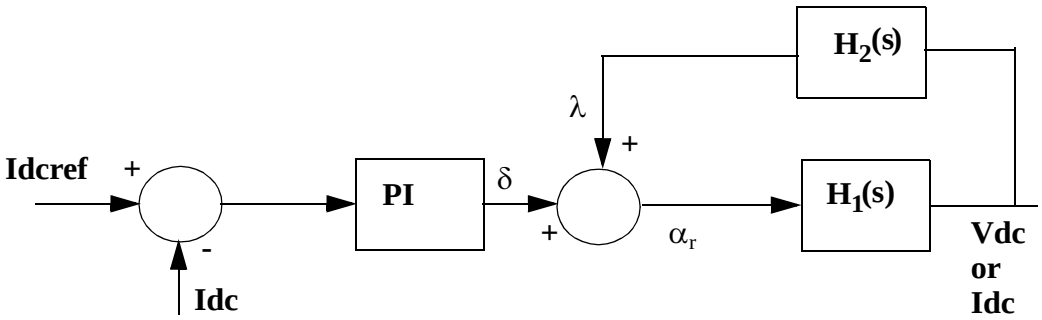


Figure 4.1 The control system of the rectifier included a stabilizing loop from the rectifiers DC side voltage or current to the fire angle order.

The stabilizing loop in Figure 4.1 has the purpose of eliminating the fundamental harmonic in the fire angle α_r. This is a rather inexpensive solution when dealing with core saturation instability since it does not involve new expensive components in the AC or DC grid. $H_1(s)$ at 50 Hz can be expressed as:

$$H_1(j2\pi \cdot 50) = K_1 \cdot e^{j\varphi} \tag{4.1}$$

Now $H_2(s)$ can be developed. The requirements for $H_2(s)$ are:

1) $H_2(s)$ must cause an effective elimination of 50 Hz disturbances in α_r.

2) $H_2(s)$ must not significantly influence the rectifier control system except in a small band around 50 Hz.

To fulfil requirement number 1) $H_2(s)$ at 50 Hz is chosen to be:

$$H_2(j\omega \cdot 50) = K_2 \cdot e^{j(180-\varphi)} = K_2 \cdot e^{j\varphi_2} \tag{4.2}$$

It is assumed that the output of $H_1(s)$ is V_{dc}. Then the transfer function $\frac{V_{dc}}{\delta}(s)$ at 50 Hz will then be:

$$\frac{V_{dc}}{\delta}(j2\pi \cdot 50) = \frac{H_1(j2\pi \cdot 50)}{1 - H_1(j2\pi \cdot 50) \cdot H_2(j2\pi \cdot 50)} = \frac{K_1 e^{j\varphi}}{1 + K_1 \cdot K_2} \tag{4.3}$$

It is clear from Equation (4.3) that K_2 can be chosen such that a 50 Hz variation in the output δ of the rectifier controller gives a much lower 50 Hz variation in V_{dc} than in the case when $H_2(s)$ does not exist. This may have a damping effect on core saturation instability since it diminishes the influence of the control system on the 50 Hz component in V_{dc}. Nevertheless, K_2 must be limited. If not, the feedback loop through $H_2(s)$ might cause harmonic components in V_{dc} to influence α_r and this way disturb the normal operation of the HVDC system. To satisfy both requirements 1) and 2), $H_2(s)$ might be in the form shown in Figure 4.2.

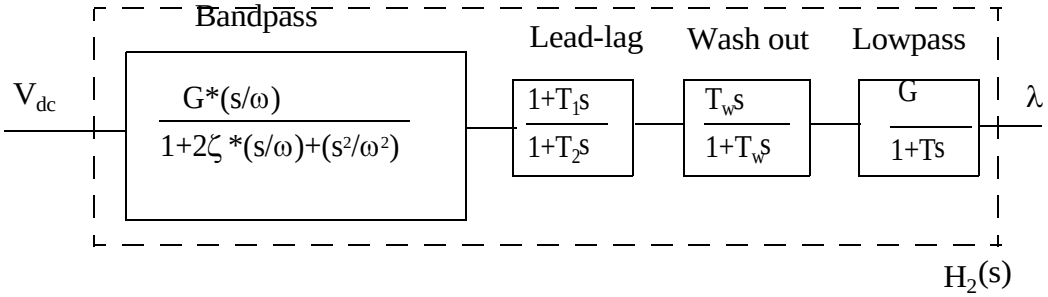


Figure 4.2 Block diagram for $H_2(s)$

If the output of $H_1(s)$ is I_{dc}, the same way of reasoning is used as in the case with V_{dc} as output of $H_1(s)$. $H_2(s)$ will of course be different in this case, since $H_1(s)$ has changed. However $H_2(s)$ may have the same form as in Figure 4.2. In Section 7.3.1 it is shown by simulation how an analog filter in a stabilizing loop from the DC side current to the fire angle order of the rectifier prevents core saturation instability.

A stabilizing loop with similarities to the one in Figure 4.1 was demonstrated in [14]. In this thesis it is investigated whether using an analog filter like $H_2(s)$ in combination with a FFT function like in Figure 4.3 gives a sharper filter in the stabilizing loop than just using $H_2(s)$ alone as in Figure 4.1. The basic idea is that the FFT function makes it possible to separate distinct harmonic components from the input signal. However, this is only the case if the harmonic

components in the input signal are integer multiples of the chosen base frequency of the FFT function (which in this thesis is 50 Hz). As will be shown in Section 5.2 the lowpass Butterworth filters (for instance of order 3 and cutoff frequency 3 Hz) make it possible to decrease the influence from the stabilizing loop on the rectifier control system when inter-harmonics are present in the input signal of the FFT function. Thus, a sharper filter than in Figure 4.1 is obtained. This is advantageous since the influence the stabilizing loop has on α_r is diminished for all frequencies apart from those in a small band around 50 Hz . However, the FFT function must be used wisely in order to avoid undesired side effects. It also turns out that one of the side effects of using the scheme in Figure 4.3 is unavoidable. This side effect causes the combination of the FFT function and the Butterworth filter at the ph50 output to generate undesired frequency components if the input frequency of the FFT function is an inter-harmonic in a small band around 50 Hz. Nevertheless, the stabilizing loop in Figure 4.3 influences the rectifier control system less than the stabilizing loop in Figure 4.1 for all frequencies except those in a small band around 50 Hz. More on this will be presented in Section 5.2. Simulations showed that a stabilizing loop similar to the one in Figure 4.3 managed to prevent core saturation instability. One of the simulations is described in Section 7.3.2.

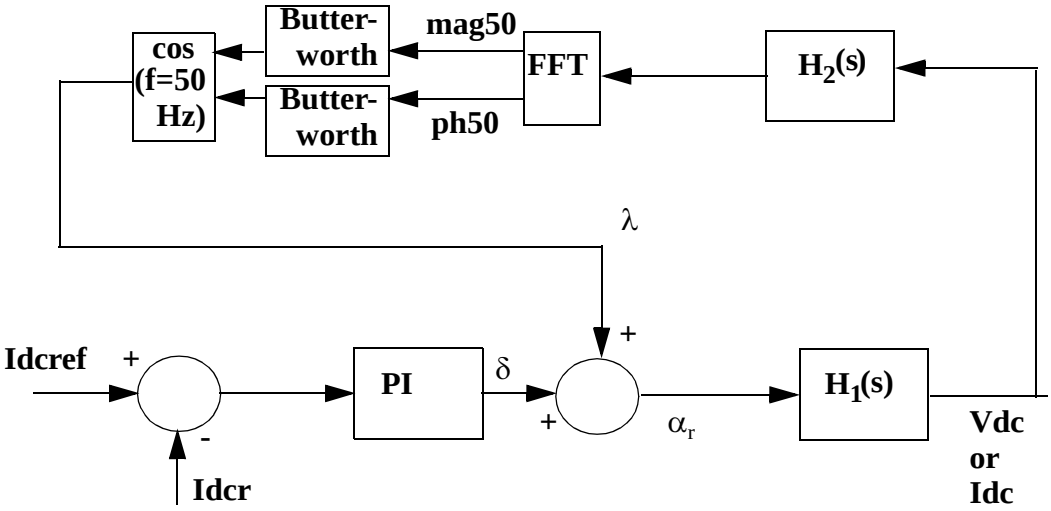


Figure 4.3 A stabilizing loop with an analog bandpass filter and a FFT function in the current control system of the rectifier.

Because it was found in Section 5.2 that the stabilizing loop in Figure 4.3 had a drawback for frequencies in a small band around 50 Hz, an improved stabilizing loop was developed. In this stabilizing loop, which is shown in Figure 4.4, the generation of undesired frequency components due to an inter-harmonic component close to 50 Hz was eliminated. At the same time, the stabilizing loop in Figure 4.4 is significantly sharper than the stabilizing loop in Figure 4.1.

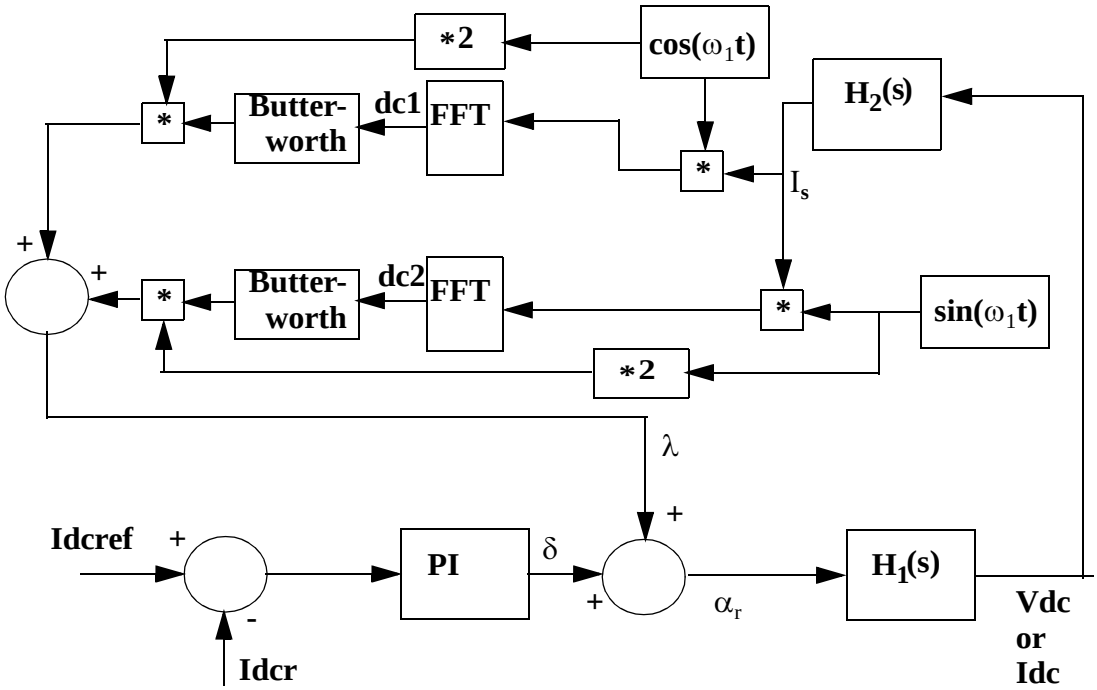


Figure 4.4 A stabilizing loop in the rectifier control system using two FFT functions in combination with an analog filter and sinusoidal functions.

The non-fundamental harmonic components in I_s are significantly smaller compared to the fundamental component in I_s than the non-fundamental components in I_{dc} are compared to the fundamental component in I_{dc}. $H_2(s)$ will also decrease the influence from inter-harmonic components on the harmonic components calculated by the FFT functions. The lowpass Butterworth filters on the output of the FFT blocks causes the desired frequencies that will eliminate core saturation instability to pass through and undesirable effects from sub-harmonics in dc1 and dc2 to be practically spoken eliminated. This matter will now be discussed more fully.

First it is assumed that I_s is given by:

$$I_s = I_0 + I_1 \sin(\omega_1 t + \varphi_1) + I_2 \sin(\omega_2 + \varphi_2) + ... + I_n \sin(\omega_n + \varphi_n) \tag{4.4}$$

ω_1 is $2\pi f_1$, where f_1 is the fundamental frequency component (50 Hz).
ω_n is n times ω_1.
I_n is the magnitude of the nth harmonic component in I_s.
φ_n is the phase angle of the nth harmonic component in I_s.

I_s is multiplied with $\cos(\omega_1 t)$, and the result becomes:

$$\cos(\omega_1 t) \cdot I_s = \cos(\omega_1 t) I_0 + \tag{4.5}$$
$$I_1 \sin(\omega_1 t + \varphi_1) \cos(\omega_1 t) + I_2 \sin(\omega_2 + \varphi_2) \cos(\omega_1 t) + ... + I_n \sin(\omega_n + \varphi_n) \cos(\omega_1 t)$$

Components of type $\cos(\omega_1 t) \cdot \sin(\omega_n t + \varphi_n)$ will have an average value equal to zero over a period of the fundamental frequency if $n \neq 1$. Thus, the dc1 output in Figure 4.4 will be the

average value equal to the average value of $I_1 \sin(\omega_1 t + \varphi_1)\cos(\omega_1 t)$ over a period of the fundamental frequency. It turns out that dc1 becomes:

$$dc1 = \frac{1}{2}\cos(\varphi_1) \tag{4.6}$$

In a similar way as dc1 was found, dc2 can be found. dc2 becomes:

$$dc2 = \frac{1}{2}\sin(\varphi_1) \tag{4.7}$$

λ in Figure 4.4 becomes:

$$\lambda = I_1 \sin(\omega_1 t + \varphi_1) \tag{4.8}$$

This shows that the fundamental frequency component in I_s is the only component that will come all the way through the stabilizing loop.

Next it is assumed that I_s also consists of an inter-harmonic component $I_{int} = I_x \sin((\omega_1 + \Delta\omega)t + \varphi_x)$. First this component is multiplied with $\cos(\omega_1 t)$. This gives:

$$\begin{aligned}\cos(\omega_1 t) \cdot I_{int} = {} & [\cos(\omega_1 t)]^2 \cdot (\sin(\Delta\omega t) \cdot \cos\varphi_x + \cos(\Delta\omega t) \cdot \sin\varphi_x) + \\ & [\cos(\omega_1 t) \cdot \sin(\omega_1 t)] \cdot (\cos(\Delta\omega t) \cdot \cos\varphi_x - \sin(\Delta\omega t) \cdot \sin\varphi_x)\end{aligned} \tag{4.9}$$

From Equation (4.9) it is seen that $\cos(\omega_1 t) \cdot I_{int}$ varies with a fundamental frequency component, a

100 Hz component ($[\cos(\omega_1 t)]^2$) and a component with frequency $\Delta\omega$. If $\Delta\omega$ is small the DC output of the FFT function will vary with frequency $\Delta\omega$ around the average value $\cos(\omega_1 t)I_s$. This is because the DC output of the FFT function is continuously calculated (from 16 to 64 samples every fundamental period). During one fundamental period the component with frequency $\Delta\omega$ has a relatively small change and therefore it appears for the FFT function that the DC value of the input signal is changing. Likewise considerations such as those just made can also be done if I_{int} is multiplied by $\sin(\omega_1 t)$. The lowpass Butterworth filters in Figure 4.4 limit the influence $\Delta\omega$ may have on λ when the frequency of $\Delta\omega$ is relatively high. In this way only frequencies in a small band around 50 Hz influence the overall control system through the stabilizing loop. It is important to allow a bandwidth of a few Hertz in the Butterworth filters in order to get a good response concerning prevention of core saturation instability (remember that the frequency in the DC side current is not exactly 50 Hz when core saturation instability develops).

The FFT function in Figure 4.4 is in reality redundant. It turns out that by simply removing them and only using the lowpass Butterworth filters as shown in Figure 4.5, we get a stabilizing loop with a filter that is just as sharp as in the case where the FFT function was used. Actually, in the work with this thesis it was possible to make the filter even sharper, but then the response time to deal with core saturation instability had to be compromised. Simulations showed that stabilizing loops like in Figures 4.4 and Figure 4.5 managed to prevent core saturation

instability. See Sections 7.3.3 and 7.4.3 for the results of these simulations.

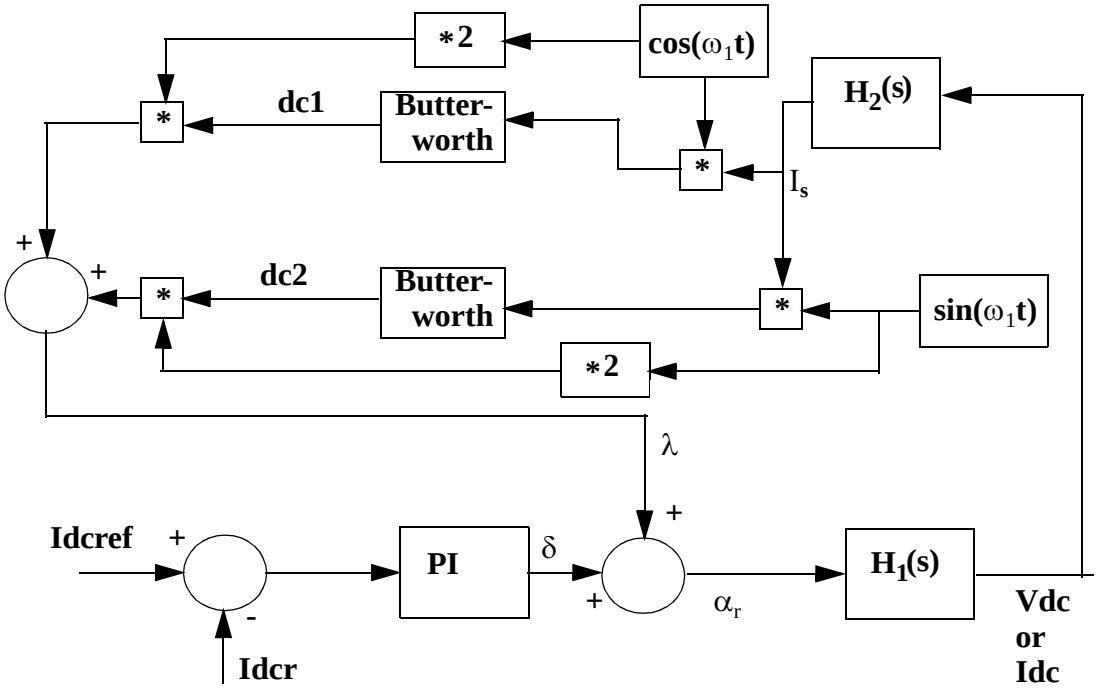


Figure 4.5 A stabilizing loop in the rectifier control system using two sinusoidal functions in combination with an analog filter.

There is reason to believe that the stabilizing loops shown in this section also can be used in other contexts than just preventing core saturation instability. They might be useful in cases where it is desirable to allow only a small band of frequencies to pass through the loop. The loops shown in Figures 4.4 and 4.5 may in some cases be preferred since they will have a significantly smaller gain than the loop shown in Figure 4.1, this is for all frequencies outside the small band it is desirable to pass through the loops. In addition they do not give any undesired side effect like the loop in Figure 4.3. However, there is no guarantee that the system response will become better even though the stabilizing loops in Figures 4.4 or 4.5 are used instead of the loop in Figure 4.1. To illustrate this a signal is considered with a frequency component f_r that is outside the small band of frequencies which the stabilizing loop is designed to operate in. The signal may partially pass through the loop with the analog filter only, and this way it may influence α_r in such a way that the frequency component f_r in V_{dc} or I_{dc} will decrease. This is because this f_r might exist in the output of the PI-controller (since I_{dcr} or V_{dcr} will have a component with frequency f_r) in the rectifier control system and that the contribution from the stabilizing loop with only an analog filter may cause the oscillation at frequency f_r to be decreased. With the stabilizing loops in Figures 4.2, 4.4, and 4.5 the influence at frequency f_r on α_r would to a much higher degree be dependent on the output from the PI controller in the rectifier control system.

Increased sharpness in the stabilizing loop would also have been obtained by simply increasing the order of $H_2(s)$. However, this would also narrow the band where the stabilizing loop is effective. In Sections 7.3.3 and 7.3.4 (see Figures 7.26 and 7.30) it is shown that filters like those used in Figures 4.4 and 4.5 will not narrow this band. Another argument for not increasing the order of $H_2(s)$ is that the stabilizing loop becomes very sensitive if one of the parameters in $H_2(s)$ is changed. Changes in the parameters in the Butterworth filters might influence its bandwidth

a little, but this is not likely to significantly change the transfer function of the stabilizing loop.

4.2 Passive and hybrid filtering on the AC side

Section 4.1 described how to decrease the influence the control system of an HVDC system has on the development of core saturation instability. The focus of this section is how hybrid or passive filtering can change the AC side impedance to prevent core saturation instability. These initiatives are likely to be far more expensive than the initiatives in the control system described in Section 4.1. However, they might be good because they have other properties than just preventing core saturation instability. These are properties like providing reactive power and/or being able to deal with other harmonic phenomena than core saturation instability.

4.2.1 Passive filtering

If single tuned filters (see Figure 2.12) tuned to the second harmonic frequency are placed on the commutation bus of an HVDC converter that is vulnerable for core saturation instability, they provide a low impedance path to earth for the second harmonic components generated by the HVDC load. This will cause the second harmonic voltage on the commutation bus to be relatively low. As seen from Figure 3.28 this will decrease the system's vulnerability for core saturation instability. One of the undesired side effects of passive filters in general is that they might create resonances in the AC grid. This makes filter design a very complex subject that requires accuracy in the modelling of both the harmonic source(s) and AC system configuration [2]. In this thesis, filter design is not the main subject. However, work has focused on how passive filters on the commutation bus may prevent development of core saturation instability. In Section 7.1 this is shown on a modified CIGRE HVDC Benchmark model. With the network configuration used in Section 7.1 the insertion of the single tuned second harmonic filter on the commutation bus of the HVDC rectifier did not generate any dangerous resonances at any integer harmonics.

4.2.2 Hybrid filtering

As stated in Section 2.2 a hybrid shunt filter does not generate any parallel resonances in the AC grid and still creates a low impedance path to earth for desired harmonic currents in the load. If the second harmonic components in the load currents of the HVDC converter is found by measurements, the hybrid filter can be controlled in such a way that it generates these current components. In this way the second harmonic components in the load currents are prevented from flowing in the AC grid. With a low impedance in the passive part of the hybrid filter at the second harmonic frequency the second harmonic voltage at the commutation bus will be relatively low. As stated in Section 4.2.1 this is favourable when it is desirable to avoid core saturation instability. An advantage with the hybrid filter is that its control system can be programmed to pick selected harmonics [28]. In this way the hybrid filter can also be used to deal with other harmonic phenomena. Section 7.2 demonstrate how a hybrid shunt filter can compensate for the second harmonic components in the load currents of an HVDC converter, and this way prevent core saturation instability. This hybrid filter and the control of it are also described in Section 7.2.

4.3 Using a low magnetizing impedance in the converter transformers

When core saturation instability appears, it is normally inconvenient to change converter transformers. This will be too costly. However, it might be valuable when planning an HVDC transmission, to consider how a converter transformer influence on the probability for core saturation instability to occur. This gives the designer a better ability to choose the most convenient converter transformer.

4.3.1 Theoretical background

Consider the coil with the iron core on Figure 4.6.

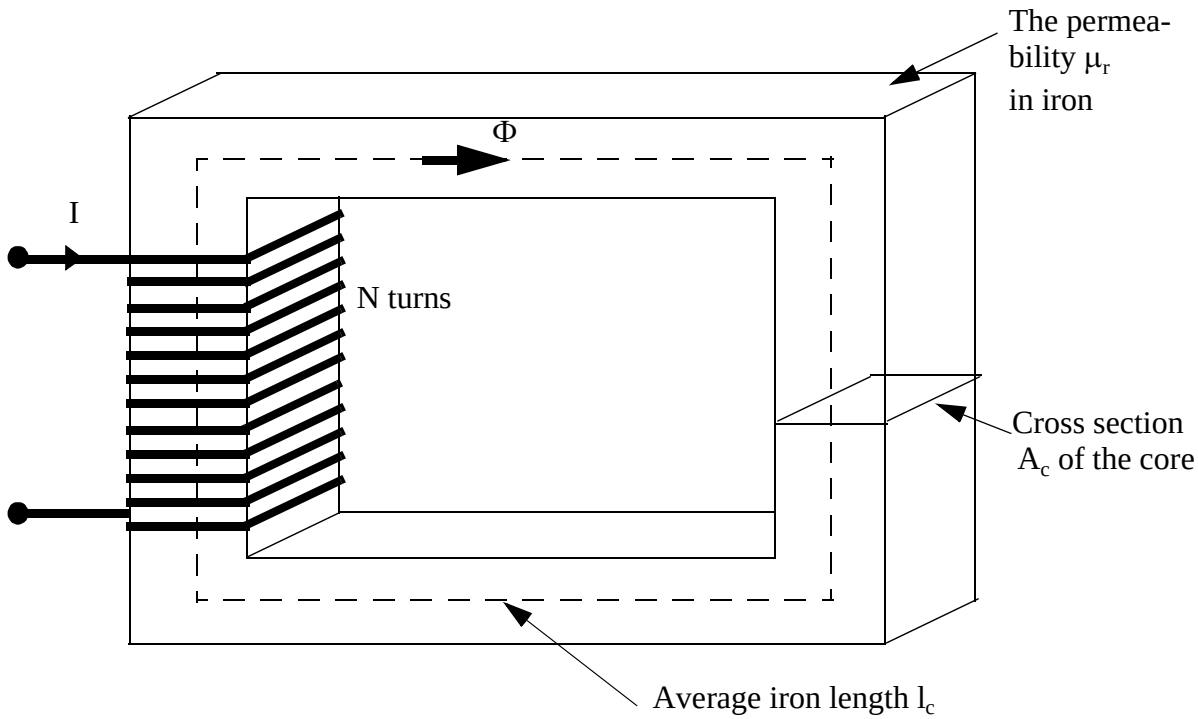


Figure 4.6 Coil with iron core

Ampere's law gives:

$$H_c \cdot l_c = N \cdot I \tag{4.10}$$

The magnetic flux density in the core B_c is given by:

$$B_c = \mu_0 \cdot \mu_r \cdot H_c = \mu_0 \cdot \mu_r \cdot \frac{N \cdot I}{l_c} \tag{4.11}$$

The flux Φ_1 in the iron core becomes:

$$\Phi_1 = B_c \cdot A_c = \mu_0 \cdot \mu_r \cdot \frac{N \cdot I \cdot A_c}{l_c} \tag{4.12}$$

The magnetizing inductance L_{m1} of the coil is given by:

$$L_{m1} = \frac{N \cdot \Phi}{I} = \mu_0 \cdot \mu_r \cdot \frac{N^2 \cdot A_c}{l_c} \tag{4.13}$$

Next the coil on Figure 4.7 is considered:

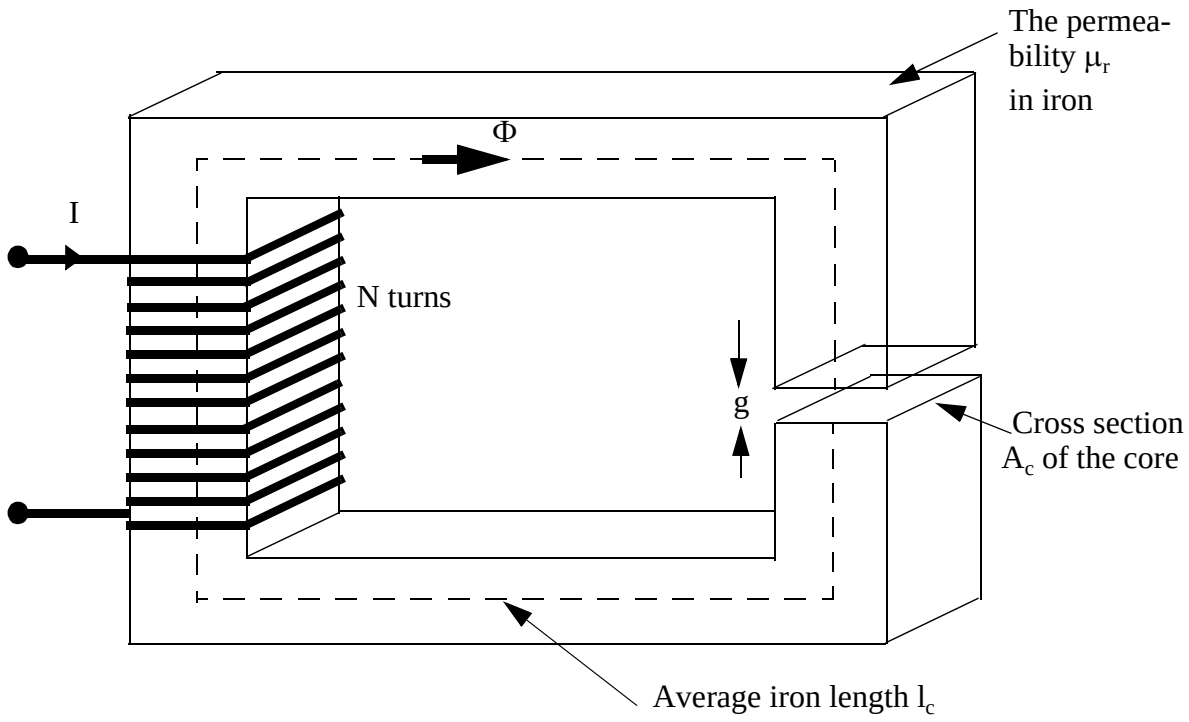


Figure 4.7 Coil with an iron core that contains an air gap

It is assumed that flux in the air gap pass through a cross section A_g which is given by:

$$A_g = 1.1 \cdot A_c \tag{4.14}$$

Applying Ampere's law:

$$H_c \cdot l_c + H_g \cdot g = N \cdot I \tag{4.15}$$

Using the relationship $B = \mu_0 \cdot \mu_r \cdot H$ gives:

$$\frac{B_c}{\mu_0 \cdot \mu_r} \cdot l_c + \frac{B_g}{\mu_0} \cdot g = N \cdot I \tag{4.16}$$

B_c is given by:

$$B_c = \frac{\Phi_2}{A_c} \tag{4.17}$$

B_g is given by:

$$B_g = \frac{\Phi_2}{A_g} = \frac{\Phi_2}{1.1 \cdot A_c} = 0.9091 \cdot B_c \tag{4.18}$$

Using this in Equation (4.16) results in:

$$\frac{B_c}{\mu_0 \cdot \mu_r} \cdot l_c + \frac{0.9091 \cdot B_c}{\mu_0} \cdot g = N \cdot I \tag{4.19}$$

Typical values for μ_r range from 2000 to 80000 for materials used in transformers and rotating machines. Assuming that l_c is not larger than $200 \cdot g$, it is the second part of the left side of Equation (4.19) that mainly contributes to the mmf. A simplification of Equation (4.19) gives:

$$\frac{0.9091 \cdot B_c}{\mu_0} \cdot g = \frac{B_g}{\mu_0} \cdot g = N \cdot I \tag{4.20}$$

This gives the following Equation for the flux Φ:

$$\Phi_2 = \frac{N \cdot I \cdot A_g \cdot \mu_0}{g} \tag{4.21}$$

The magnetizing inductance of the coil will in this case become:

$$L_{m2} = \frac{N^2 \cdot A_g \cdot \mu_0}{g} \tag{4.22}$$

Assuming that μ_r=20000 and that l_c=200g, then the following relation between Φ_1 and Φ_2 is obtained:

$$\frac{\Phi_1}{\Phi_2} = \frac{\mu_0 \cdot \mu_r \cdot \frac{N \cdot I \cdot A_c}{l_c}}{\frac{N \cdot I \cdot A_g \cdot \mu_0}{g}} = 90.9091 \tag{4.23}$$

This means that if the current I=1 A gives a flux Φ_1 that, for instance, is 0.2 Wb, then a current I=90.9091 A is necessary to obtain a flux Φ_2= 0.2 Wb. Furthermore, the flux density B_c will be 1.1 times larger in the case where the air gap is not used than in the case where the air gap is used. As a consequence, the current I needs to be 100 A to achieve the same flux density in the iron core when the air gap is present as when the air gap is not present and I=1 A. To saturate the iron with the air gap present will therefore require a 100 times larger current than saturating the iron when the air gap is not present. This is illustrated in Figure 4.8 by drawing the B-H curve (H is proportional to I) for the case when an air gap is present and for the case when an air gap is not present. The curves are not scaled, but illustrates what is explained previously.

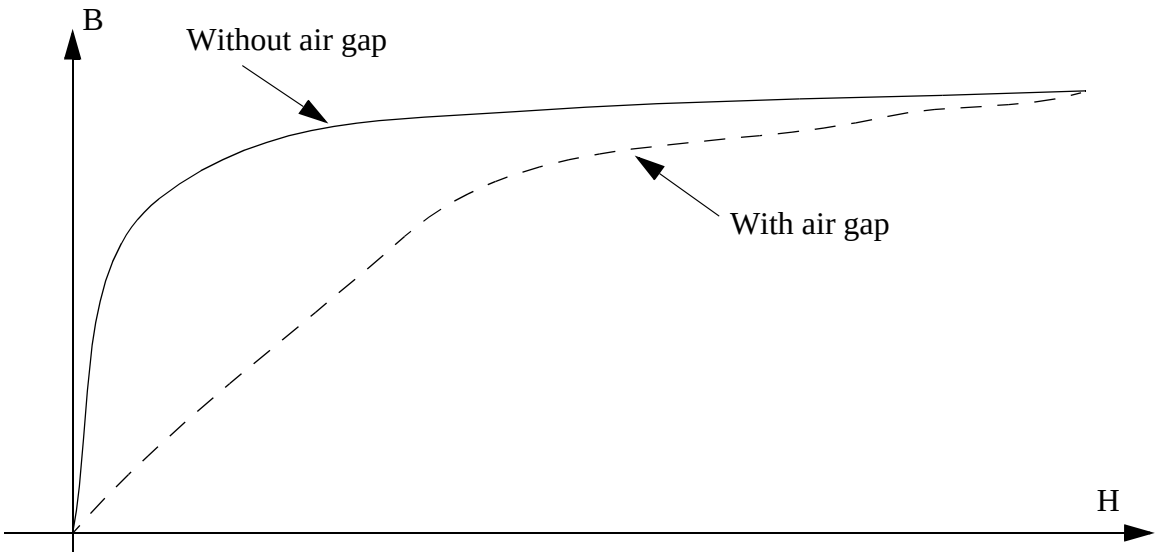


Figure 4.8 Illustration of B-H curves for the coils on Figure 4.6 and 4.7.

The principle that a much larger magnetizing current is required to saturate the iron when a suitable air gap is present can be transferred to three-phase transformers also. Suitable air gaps in these will also cause a much larger magnetizing current to be required to cause the transformer iron to saturate, than in the case when air gaps are not present (this is of course when the air gap is the only difference between two transformers.). The example shown in this section is just written to give a physical understanding of why an air gap may cause a large magnetizing current to be required to saturate the transformer iron. The drawback of using an air gap in the transformer is that it will have higher no load losses than in the case where an air gap is not used. This is because the magnetizing impedance decreases due to the air gap in the transformer. For the case described in in this section, this can be illustrated by calculating L_{m1}/L_{m2}.

$$\frac{L_{m1}}{L_{m2}} = 90.9091 \tag{4.24}$$

The magnetizing impedance will be 90.9091 times larger in the case where the air gap is absent than in the case where the air gap is present.

It should be mentioned that it is unlikely that air gaps have any significant influence on the transformer losses during its rated operation. This is because the magnetizing impedance still will be much larger than the impedance of the transformer load.

The following explains how air gaps in converter transformers might be used to prevent core saturation instability.

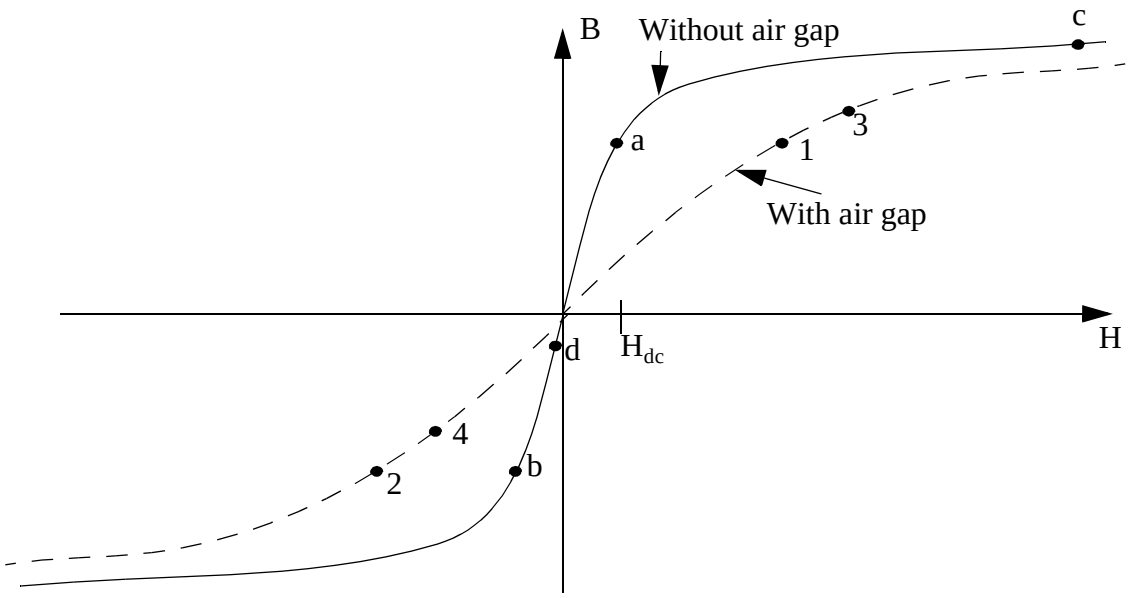


Figure 4.9 Magnetizing curves for two identical transformers with the exception that one of them have air gaps.

In normal operation of the transformer without air gaps, the B-H loop will vary between point a and point b in a cyclic manner. When H_{dc} is present in Figure 4.9 the magnetizing curve will vary between point d and point c, which will cause the transformer to be saturated. This is described in Section 3.2.1. Under unfavourable conditions this can cause core saturation instability to be developed.

If there are air gaps in the converter transformers the magnetizing curve in Figure 4.9 will vary in a cyclic manner between point 1 and point 2. If the transformer becomes DC-magnetized in the same manner as the transformer without air gaps the magnetizing curve in Figure 4.9 will vary between point 3 and point 4 in a cyclic manner. It is easy to see that in this case the transformer is not driven deep into saturation. A much less amount of positive-sequence second harmonic current is produced by the transformer than in the case when the air gaps were absent. It is therefore much more unlikely that core saturation instability will develop in the case when the converter transformers have air gaps.

4.4 A blocking LC filter between the low potential converter and earth on the DC side

The blocking LC filter will be as shown in figure 4.10.

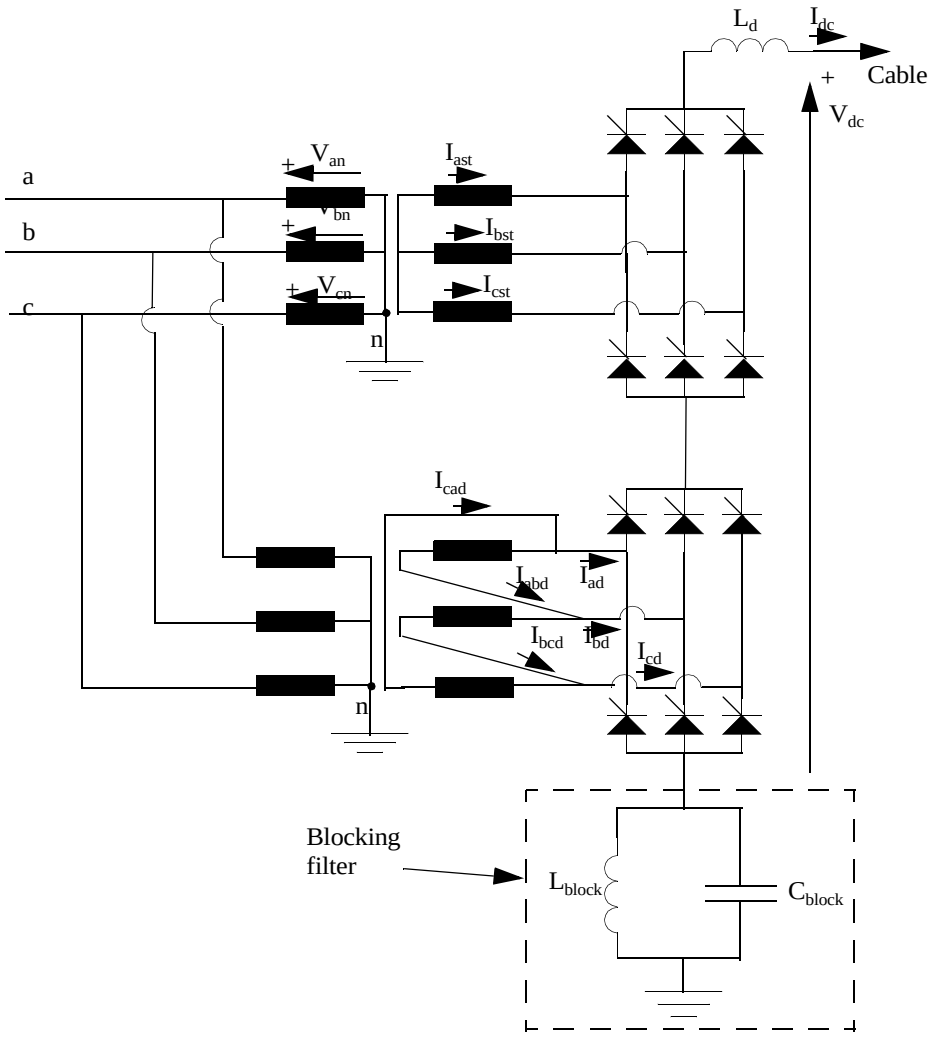


Figure 4.10 HVDC converter with a blocking filter that blocks the fundamental frequency component in the DC side current.

The blocking filter prevents the flow of a fundamental current component on the DC side and allows the DC current component on the DC side to flow through. This will definitely stop any development of core saturation instability. By placing the filter between earth and the low potential converter it does not have to sustain the DC side voltage. However, the filter needs to sustain the DC side current and will therefore have a considerable cost. In Section 7.5 it is shown by simulation how a blocking filter like in Figure 4.10 effectively prevents core saturation instability.

4.5 Series compensated HVDC converters (CCC HVDC converters)

If an HVDC converter is series compensated as in Figure 4.11, the series capacitors will prevent any DC current flowing from the converter to the AC side. However, introducing the commutation capacitors in a conventional HVDC transmission results in higher peak voltage across the valves and increased generation of harmonics [13]. It will also make much of the

shunt compensation redundant. Thus, the cost of inserting the commutation capacitors in a conventional HVDC transmission is very high. Nevertheless, CCC HVDC transmission has many properties that makes it favourable [13]. It prevent core saturation instability, it improves the commutation failure performance, it improves the dynamic stability, it reduces the valve short circuit current, and it reduces the need for shunt compensation. Studies on the CCC HVDC transmission have been performed since the 1950s [15]. The main drawback has been that there has been no economic way to mitigate the transient overvoltages. The development of metal oxide varistors has in the later years increased the interest in concept.

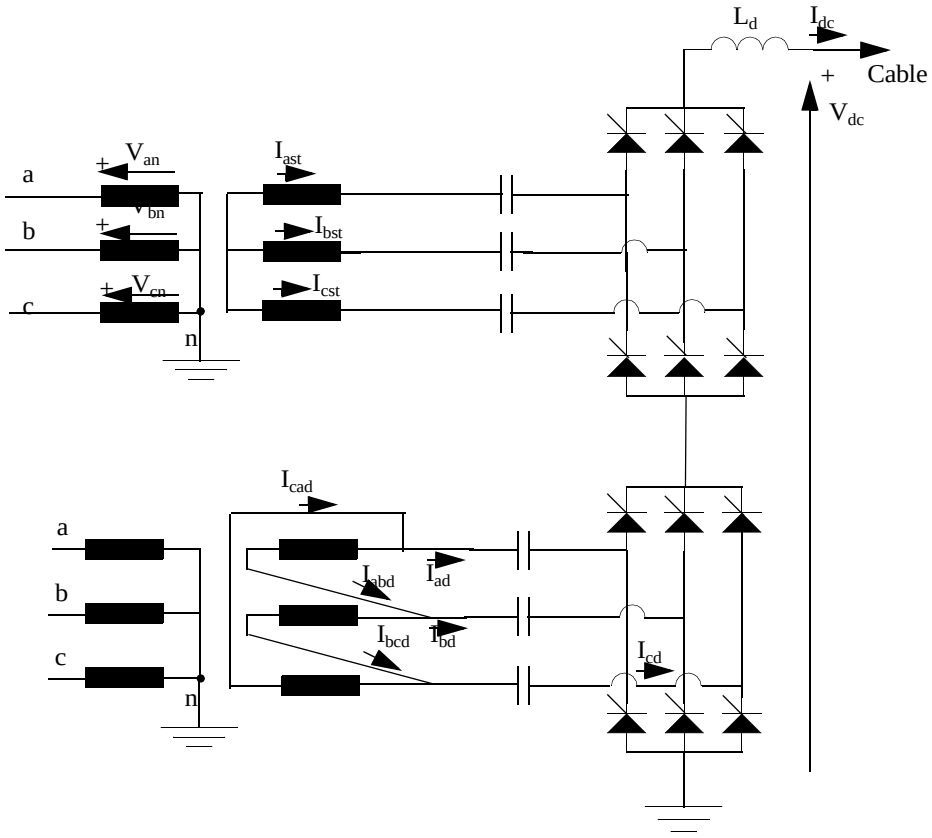


Figure 4.11 Series compensated HVDC converter

4.6 Fire angle modulation based on the DC currents on the secondary side of the converter transformers

In Section 4.1 it was described how a stabilizing loop could be used to eliminate a fundamental frequency variation in the fire angle order of the rectifier control system. A different way to modulate the fire angle order is to use feedback loops from the measured DC currents that are on the secondary side of the converter transformers. The purpose of this is to cause firing instants in such a way that these DC currents are controlled to zero. [33] gives a detailed description on how such fire angle modulation can be implemented.

5 Simulation tools and models

For the simulations described in this thesis the simulation program PSCAD/EMTDC version 3 [16] has been used. PSCAD/EMTDC was developed at Manitoba HVDC Research Centre Inc. and version 3 was released in 1999. PSCAD/EMTDC represents and solves the differential Equations of the entire power system and its controls in the time domain (both electro-magnetic and electro-mechanical systems). PSCAD (Power Systems Computer Aided Design) is the graphical interface between EMTDC (ElectroMagnetic Transients for DC) and the user. In PSCAD users builds their specific circuits and control systems. They can use components from a library or components that they have programmed themselves. The users also defines in PSCAD which signals/measurements that they wants to plot, the time step of the simulation, how many seconds to be simulated, and many other things. EMTDC is the program that does all the calculations on the circuits the users have defined in PSCAD. Manitoba HVDC Centre Inc. claims that PSCAD/EMTDC version 3 is suitable for studies such as:

- Find overvoltages in a power system due to a fault or breaker operation. Transformer non-linearities (i.e. saturation) are a critical factor and are represented. Multiple run facilities are often used to run hundreds of simulations to find the worst case when varying the point on wave of the fault, type of fault, or location of the fault.

- Find overvoltages in a power system due to a lightning strike. This simulation would be performed with very small time steps (nanoseconds).

- Find the harmonics generated by an SVC, HVDC link, STATCOM, machine drive (virtually any power electronic device). Detailed models for thyristors, GTO, IGBT, diodes. are required, as are detailed models of the associated control systems (both analog and digital).

- Find maximum energy in a surge arrester for a given disturbance.

- Tune and design control systems for maximum performance. Multiple run facilities are often used here to automatically adjust gains and time constants.

- Investigate the Sub-Synchronous Resonance (SSR) effect when a machine and multi-mass turbine system interact with series compensated lines or power electronic equipment. Control systems can also be modified to investigate possible SSR mitigating methods.

- Modelling of STATCOM or Voltage Source Converters (and detailed models of their associated controls)

- Study interactions between SVC, HVDC and other non-linear devices.

- Investigate instabilities due to harmonic resonances, controls, etc.

- Investigate the pulsing effects of diesel engines and wind turbines in an electric network.

- Insulation coordination.

- Variable speed drives of various types including cycloconverters and transportation and ship drives.

- Industrial systems including compensation controllers, drives, electric furnaces, filters, etc.
- Feeds to isolated loads.

Time domain analysis is good to use when the aim of the simulation is to analyse harmonics or transients. Therefore PSCAD/EMTDC version 3 should be a suitable tool for simulating a phenomenon such as core saturation instability (as claimed by Manitoba HVDC Research Centre Inc.). Nevertheless, it is important to know how the PSCAD/EMTDC models behave in order to have confidence in the simulated results. This chapter is used to describe the behaviour of important components used in the simulations in this thesis.

5.1 Converter transformer models

It is essential in simulation of core saturation instability to have a good model of the saturation in the converter transformers. In PSCAD/EMTDC version 3 there are two types of transformer models to choose between. In one of the transformer models, saturation is modelled as a current source in parallel with one of the transformer windings. The other transformer model builds on a magnetic model and the saturation curve is defined by the user. In Sections 5.1.1 and 5.1.2 these transformer models are described.

5.1.1 The transformer model with saturation modelled as a current source.

The transformer model described here is constructed from single-phase units. It is assumed that there is a uniform flux throughout the core legs and yokes, and the winding leakage reactances are combined. Core losses are modelled as a resistance in parallel with the each winding. When saturation is included in the modelling the core losses are limited between 0.001 pu and 0.1 pu of the transformer rating. Winding losses must be modelled separately by the user as a resistance in series with each phase of the transformer. The modelling of saturation which is the main focus in this section is illustrated in Figure 5.1.

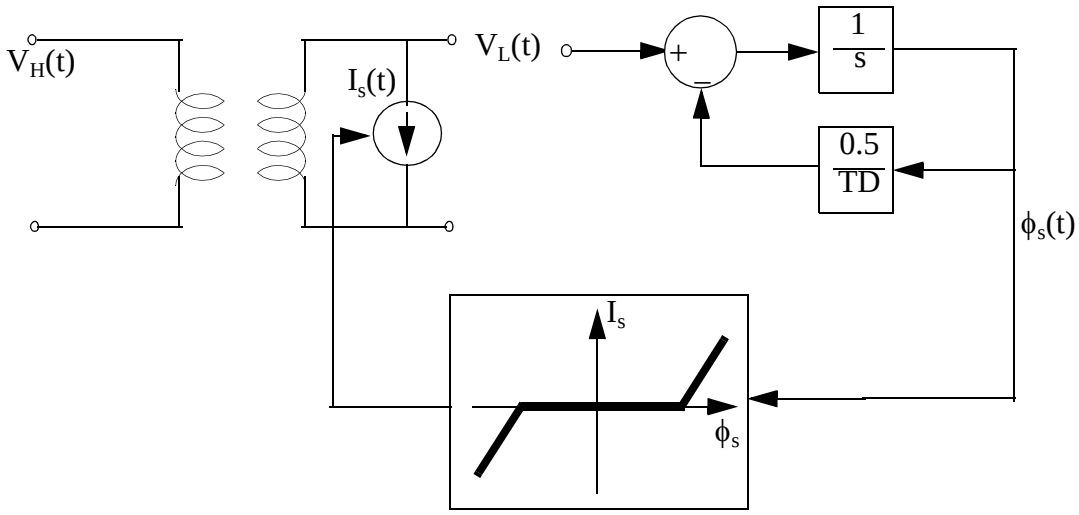


Figure 5.1 One of the saturation models used in PSCAD/EMTDC version 3

The saturation of the transformer is modelled as a current source in parallel with one of the transformer windings. The winding closest to the core is usually selected as it is closest to where the magnetic effects are occurring. In an HVDC converter transformer this is usually the high voltage winding. The voltage on the winding where the saturation is indicated, is measured and converted into pu. The transformer flux is obtained by integrating this pu winding voltage. The magnetizing current is then decided from the magnetizing characteristic of the transformer. The feedback loop including the time constant TD is present to give realistic inrush current decay. In the simulation in this thesis this is not the issue, and therefore TD is chosen to be very large (100 seconds). This provides a more realistic flux since the influence of the feedback loop is very small.

The relationship between $I_s(t)$ and $\phi_s(t)$ is found by a curve fitting algorithm which uses parameters that the user gives as input data in the transformer model. These input data are i) air core reactance (X_{air}), ii) rated magnetizing current (I_m), and iii) knee point voltage (U_{knee}).

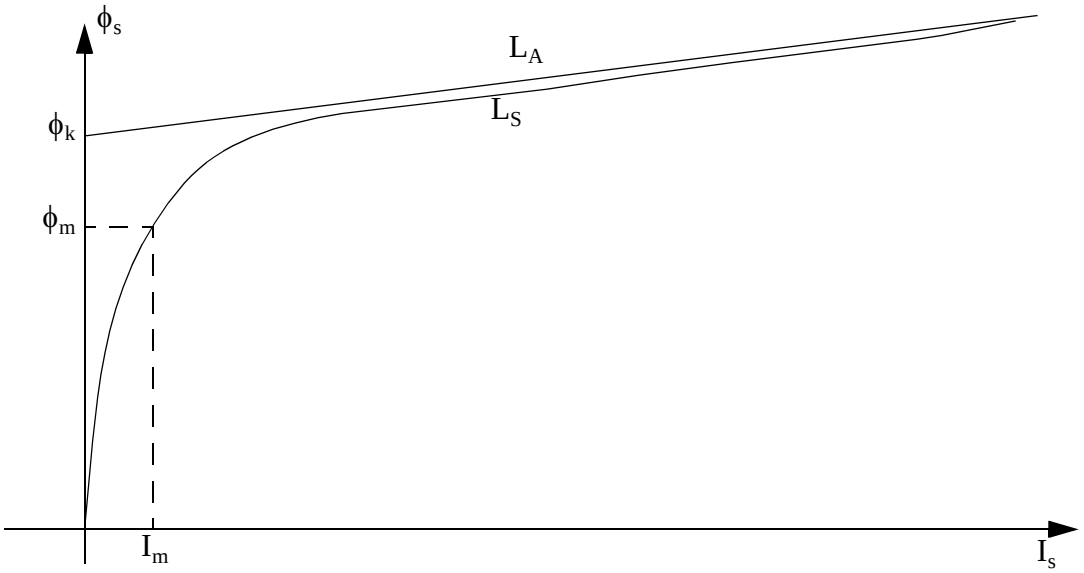


Figure 5.2 Saturation characteristic

ϕ_k corresponds to the flux level when the knee voltage U_{knee} is applied across the winding where the saturation is placed.

ϕ_m is the rated flux.

L_A is the inductance corresponding to the air core reactance.

L_S is the actual non-linear saturating inductance.

I_m is the rated magnetizing current (the magnetizing current when rated voltage is present on the transformer windings and the transformer load is zero).

The relationship between the magnetizing current and magnetizing flux is assumed to be a certain function with convenient parameters (because of the curve fitting algorithm). Due to the uncertainty that exists in true saturation characteristics of a transformer, this way of modelling in many cases may not be unreasonablec. On the other hand this way of modelling causes limitations in which type of magnetizing characteristics it is possible to model.

When simulating with this type of saturation modelling there will be an aspect of accuracy that depends on the length of the time step that is used and the shape of the magnetizing curve[17]. Consider the circuit in Figure 5.3.

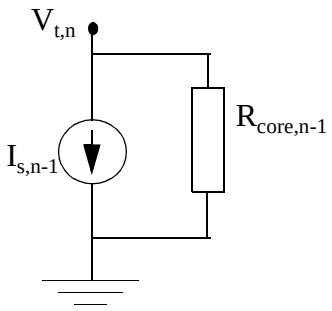


Figure 5.3 Time domain model of transformer saturation

The terminal voltage $V_{t,n}$ at time step n is calculated on the basis of the magnetizing current $I_{s,n-1}$ at time step n-1 and the core loss resistance $R_{core,n-1}$ at time step n-1. When the change in $I_{s,n-1}$ and $R_{core,n-1}$ is small per time step this will have no significant error. However once saturation is reached, the magnetizing current I_s might change significantly from time step to time step, especially if the time step is relatively large. This will cause a considerable error in $V_{t,n}$ which in turn will cause an error in the flux that is used to calculate $I_{s,n}$. The core losses will normally be so small that $R_{core,n-1}$ does not give any significant influence on the error in $V_{t,n}$.

In [18] the transformer model in this section was used in a simulation of core saturation instability where the results closely agreed with the actual system response.

5.1.2 The UMEC transformer model

The general transformer model described in Section 5.1.1 allows only single-phase units and it is also assumed a uniform flux throughout the core legs and yokes. In version 3 of PSCAD/ EMTDC it is, in addition to the model described in Section 5.1.1, included a transformer model based on unified magnetic equivalent-circuit (UMEC) theory. This model permits modelling of single-phase unit transformers, three-limb transformers and five-limb transformers. It does not assume a uniform flux throughout the core legs and yokes, neither does it combine the winding leakage reactances. The UMEC model of a single-phase transformer can be illustrated as in Figure 5.4.

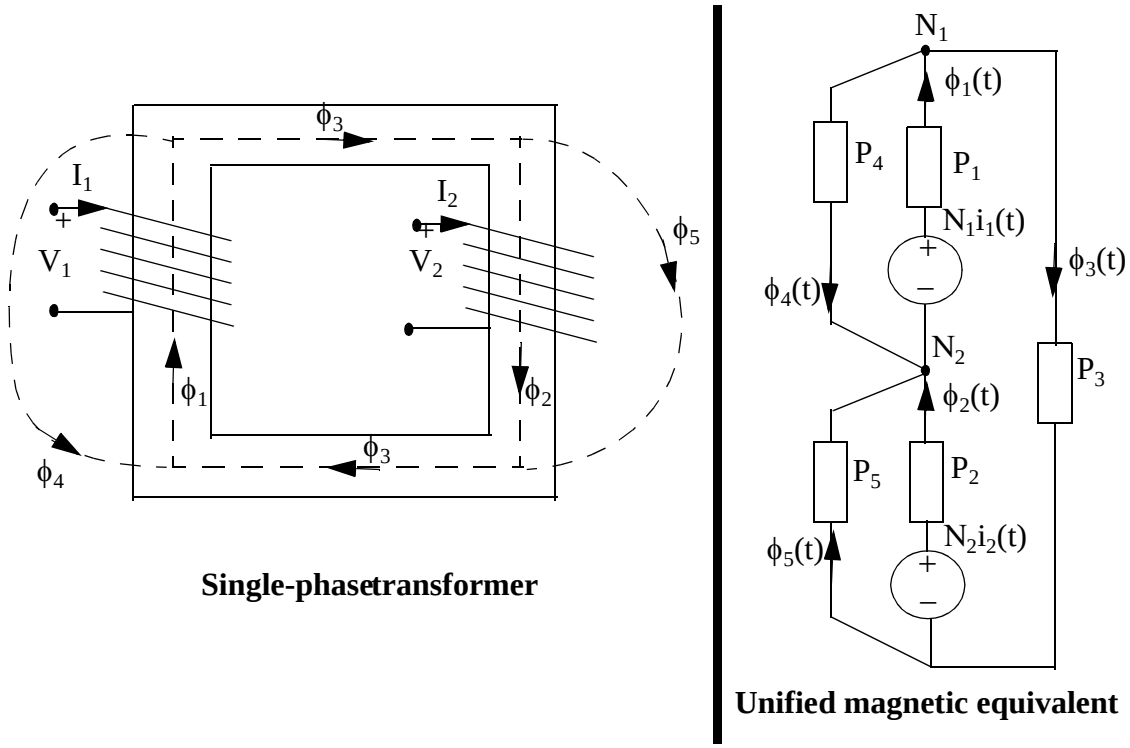


Figure 5.4 UMEC single-phase transformer model

The mmf sources $N_1i_1(t)$ and $N_2i_2(t)$ represent windings 1 and 2. The winding voltages $v_1(t)$ and $v_2(t)$ are used to calculate the winding limb flux $\phi_1(t)$ and $\phi_2(t)$, respectively. The winding limb flux divides between leakage and yoke paths. Therefore, a uniform flux is not assumed. The permeances are calculated on the basis of several factors:

1) An approximation in PSCAD/EMTDC of a user defined saturation curve

2) A user defined leakage reactance (must be equal for all windings)

3) The ratio between the length of the winding limbs and the yokes

4) The ratio between the cross-sectional area in the yokes and the winding limbs.

It is assumed that each winding limb has the same length and cross sectional area, and equivalent for the yokes.

This section does not consider into how these permeances are calculated, it just refers to [6] for more details.

PSCAD/EMTDC version 3 does not give a description on how its available UMEC transformer is implemented. However, according to [6] the branch permeances for the UMEC transformer in PSCAD/EMTDC are calculated on the basis of the flux solution from the previous time step (the leakage permeances are constant so they do not need to be calculated more than once). [6] claims that this still can give acceptable results with simulation steps of the order of 50 μs. Nevertheless, a few simple test cases have been created to find out more about the UMEC transformers saturation model.

Test case 1:

The circuit of test case 1 is shown in Figure 5.5.

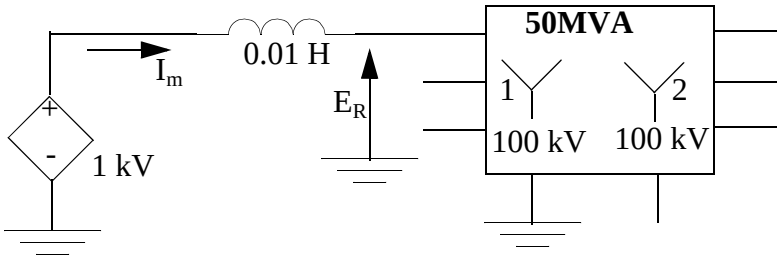


Figure 5.5 Simple test circuit to find properties of the saturation characteristic for the UMEC model in PSCAD/ EMTDC version 3.

The three-phase transformer in Figure 5.5 is built up of three single-phase units. It will therefore not be any interactions between the phases. The transformer data are shown in Tables 5.1 and 5.2.

Table 5.1 Transformer data for the UMEC transformer in Figure 5.5

Rated power S_N	50 MVA
Rated frequency f_N	60 Hz
Leakage inductance	0.1 pu
Tap changer winding ?	No
Saturation enabled ?	Yes
Coupling of winding 1	Y
Rated L-L voltage U_{1N} in winding 1	100 kV(rms)
Coupling of winding 2	Y
Rated L-L voltage U_{2N} in winding 2	100 kV(rms)
Primary neutral earthed ?	Yes
Secondary neutral earthed?	No
Core construction	3 Phase Bank
Ratio yoke/winding-limb length	2.0
Ratio yoke/windin-limb area	1.0

Table 5.2 Magnetizing curve data for the umec transformer in Figure 5.5

Magnetizing current Im (pu)	Magnetizing flux Φm (pu)
0	0
0.01	1.0
0.015	1.05
0.02	1.1
0.025	1.15
0.03	1.2
0.035	1.25
0.04	1.3
0.045	1.35
0.05	1.4

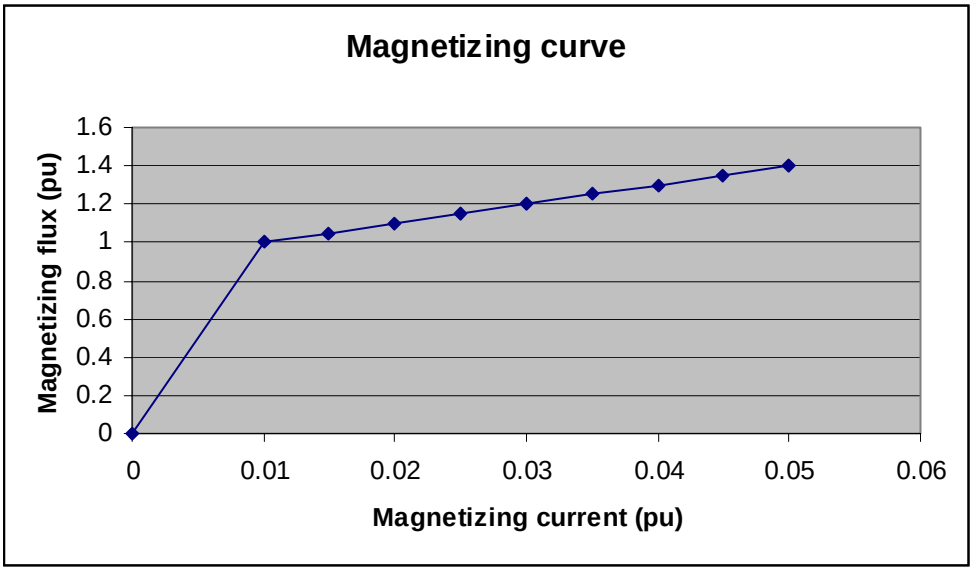


Figure 5.6 The user defined magnetizing curve of the transformer in Figure 5.5.

The peak value of a primary phase voltage U_{fpeak} during rated operation of the transformer:

$$U_{fpeak} = \frac{\sqrt{2}}{\sqrt{3}} U_{1N} \tag{5.1}$$

The rated flux ϕ_{1N} in the transformer becomes (the transformer ratio is 1):

$$\phi_{1N} = \frac{1}{\omega_N} \cdot U_{fpeak} = \frac{1}{2\pi f_N} \cdot U_{fpeak} = 216.5824 \text{ Vs} \tag{5.2}$$

The applied voltage on phase R of the transformer is E_R=1 kV (dc), and the simulation time step Δt used is 100 μs. The increase $\Delta\phi_m$ in the flux ϕ_m per time step becomes:

$$\Delta\phi_m = E_R \cdot \Delta t = 0.1 \text{ Vs} \tag{5.3}$$

In per unit:

$$\Delta\phi_{mpu} = \frac{\Delta\phi_m}{\phi_{1N}} = \frac{0.1}{216.5824} \approx 4.6172 \cdot 10^{-4} \tag{5.4}$$

When ϕ_m=1.0 pu the break point of the magnetizing curve is reached. The corresponding magnetizing current I_m is then 0.01 pu in peak value or if a pure DC current flows I_m=0.01 pu.

The rated current referred to the primary side of the transformer is:

$$I_{1N} = \frac{S_N}{\sqrt{3} \cdot U_{1N}} = 288.6751 \text{ A} \tag{5.5}$$

I_m in the breaking point of the magnetizing curve becomes:

$$I_m = 0.01 \cdot \sqrt{2} \cdot I_{1N} \approx 4.0824829 \text{ A} \tag{5.6}$$

Simulation results are shown in Figure 5.7-5.8. The time step Δt used was 100 μs.

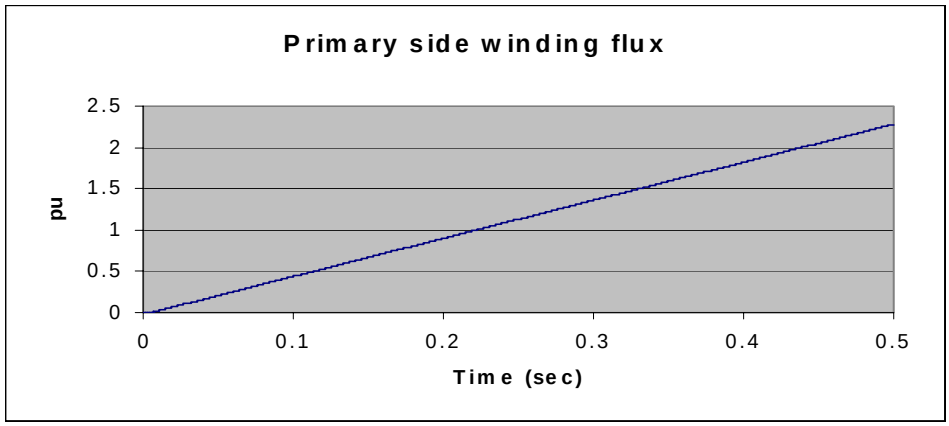


Figure 5.7 The primary side winding flux

URN:NBN:no-2111

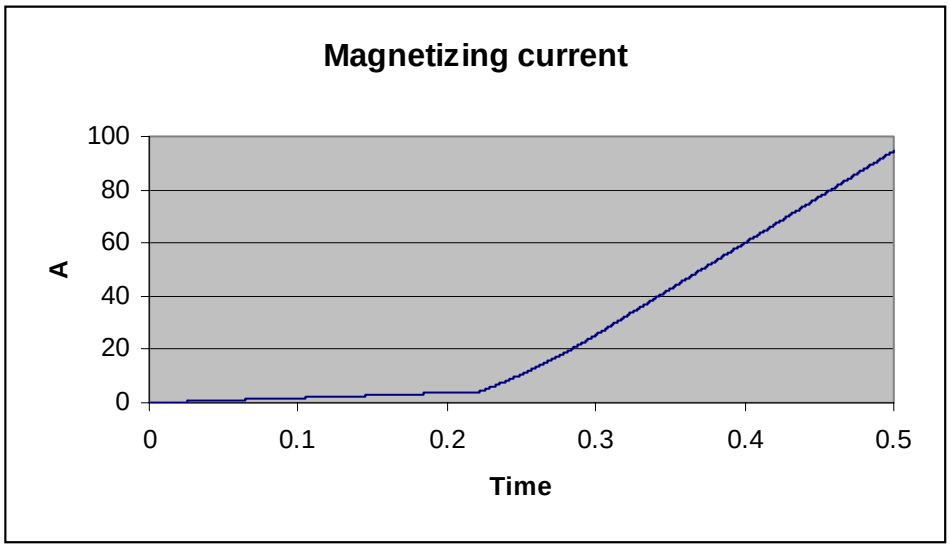


Figure 5.8 The magnetizing current I_m

Figure 5.8 shows that the derivate of the magnetizing current I_m changes when the simulation time is slightly longer than 0.2 seconds. This is because the flux ϕ_m at this instant becomes larger than 1.0 pu and the transformer enters saturation. It is of special interest how the derivate of the magnetizing current changes around the break point on Figure 5.8. This is analysed by means of Tables 5.3-5.5.

Table 5.3 Simulation results

Instant x	x=1	x=2	x=3	x=4	x=5
Time (s)	0.2213	0.2214	0.2215	0.2216	0.2217
$\phi_{m(x)}$ (pu)	0.99850776	0.99896939	0.99943102	0.99989265	1.00035428
$\phi_{my(x)}$ (pu)	0.99809189	0.99855333	0.99901477	0.99947621	0.99993796
$I_{m(x)}$ (A)	4.07491945	4.07680337	4.07868729	4.08057121	4.08245513
$E_{R(x)}$ (Volt)	999.81161	999.81161	999.81161	999.81161	999.81161

Instant x	x=6	x=7	x=8	x=9	x=10
Time (s)	0.2218	0.2219	0.2220	0.2221	0.2222
$\phi_{m(x)}$ (pu)	1.00081576	1.00127674	1.00173746	1.00219818	1.0026589
$\phi_{my(x)}$ (pu)	1.00039865	1.00085845	1.00131697	1.00177549	1.00223402
$I_{m(x)}$ (kA)	4.08977391	4.10569607	4.12729198	4.14884153	4.17039138
$E_{R(x)}$ (Volt)	998.97782	997.83775	997.84307	997.84702	997.84301

URN:NBN:no-2111

$\phi_{m(x)}$ is the primary side winding flux in phase R at time instant x.

$\phi_{my(x)}$ is the yoke flux in the phase R transformer at time instant x.

$I_{m(x)}$ is I_R (see Figure 5.5) at time instant x.

$E_{R(x)}$ is E_R (see Figure 5.5) at time instant x.

The change in the primary side winding flux between time instant x and x+1 is defined as $\Delta\phi_{m(x,x+1)} = \phi_{m(x+1)} - \phi_{m(x)}$.

Table 5.4 The change in ϕ_m between each time instant in Table 5.3

$\Delta\phi_{m(1,2)}$	$\Delta\phi_{m(2,3)}$	$\Delta\phi_{m(3,4)}$	$\Delta\phi_{m(4,5)}$	$\Delta\phi_{m(5,6)}$	$\Delta\phi_{m(6,7)}$
$4.6163 \cdot 10^{-4}$	$4.6163 \cdot 10^{-4}$	$4.6163 \cdot 10^{-4}$	$4.6163 \cdot 10^{-4}$	$4.6148 \cdot 10^{-4}$	$4.6098 \cdot 10^{-4}$

$\Delta\phi_{m(7,8)}$	$\Delta\phi_{m(8,9)}$	$\Delta\phi_{m(9,10)}$
$4.6072 \cdot 10^{-4}$	$4.6072 \cdot 10^{-4}$	$4.6072 \cdot 10^{-4}$

The change in the current on the primary side of the transformer between time instants x and x+1 is defined as $\Delta I_{m(x,x+1)}=I_{m(x+1)} - I_{m(x)}$.

Table 5.5 The change in I_m between each time step in Table 5.3

$\Delta I_{m(1,2)}$	$\Delta I_{m(2,3)}$	$\Delta I_{m(3,4)}$	$\Delta I_{m(4,5)}$	$\Delta I_{m(5,6)}$
$1.88392 \cdot 10^{-3}$	$1.88392 \cdot 10^{-3}$	$1.88392 \cdot 10^{-3}$	$1.88392 \cdot 10^{-3}$	$7.31878 \cdot 10^{-3}$

$\Delta I_{m(6,7)}$	$\Delta I_{m(7,8)}$	$\Delta I_{m(8,9)}$	$\Delta I_{m(9,10)}$
$15.92216 \cdot 10^{-3}$	$21.59591 \cdot 10^{-3}$	$21.54955 \cdot 10^{-3}$	$21.54985 \cdot 10^{-3}$

From Table 5.4 it is seen that the change in flux per time step is almost as in Equation (5.4). The small deviation probably stems from the small voltage drop across the inductance between the source and E_R (see Table 5.3). This deviation becomes larger as the derivate of the magnetizing current increases. The magnetizing flux ϕ_m reaches 1.0 between time instant 4 and 5, but PSCAD/EMTDC version 3 still uses the non-saturated magnetizing inductance from time instant 4 to 5. Thus, if the time step becomes too large there is a possibility that the deviation from the real magnetizing curve causes incorrect simulation results. From $\Delta I_{m(7,8)}$, $\Delta I_{m(8,9)}$, and $\Delta I_{m(9,10)}$ it is clear that when the transformer is in saturation the change in I_m between two time steps will be about $21.55 \cdot 10^{-3}$ A. Before reaching this level of change it takes two time steps.

The level of change in I_m in these two time steps is considerable below $21.55 \cdot 10^{-3}$ A. This will cause PSCAD/EMTDC to miss even more on the user defined saturation characteristic. It should be a matter of concern that it might take almost three time steps before the UMEC model manage to reach the correct level of change in the magnetizing current when a break point on the magnetizing characteristic appears. If the user defines several break points on the magnetizing curve this gives reason for even more concern. This is illustrated in Figure 5.9 (it is assumed that the increase in flux is constant in each time step).

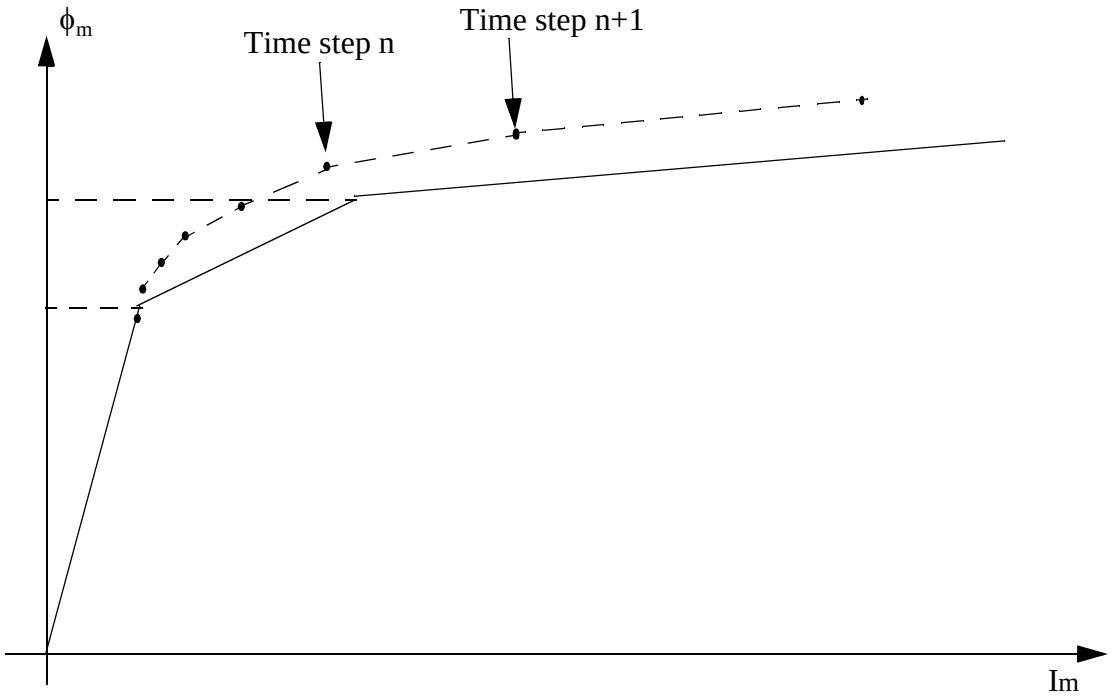


Figure 5.9 User defined magnetizing curve (solid-drawn line) and the magnetizing curve PSCAD/EMTDC will use (dashed line).

Conclusion:

The EMTDC approximation of the user defined saturation curve for the UMEC transformer model might give considerable deviation from the user defined saturation curve, especially if the time step is large. The fact that it might require almost three time steps before the correct magnetizing inductance is achieved when a break point on the magnetizing curve appears should be kept in mind when unexpected simulation results appears. If a simulation of a case where the saturation of transformers is a critical element gives satisfying results, it is a good idea to re-simulate the case with a substantial lower time step. This might be an important of confirming the results and should not be costly.

Test case 2

According to [19] the UMEC transformer does not model hysteresis. Test case 2 was made to verify this statement. The circuit diagram for test case 2 is shown on Figure 5.10.

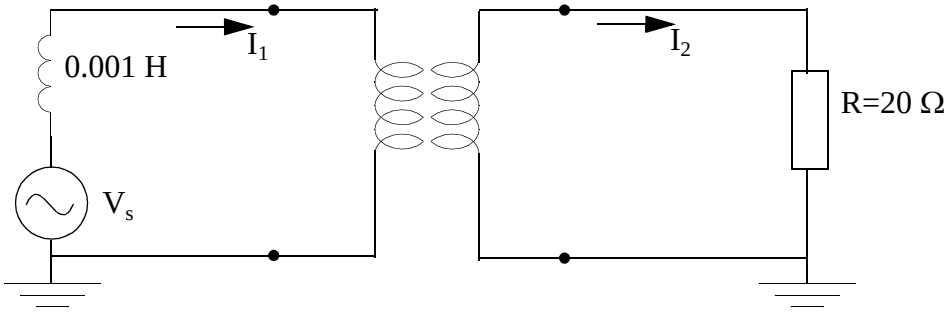


Figure 5.10 Simple test circuit to find properties of the saturation characteristic for the UMEC model in PSCAD/ EMTDC version 3.

Table 5.6 The data for the voltage source in Figure 5.10

Magnitude of voltage V_s	80.710678 kV (rms)
Frequency f_s	60 Hz
Ramp up time	0.05 sec

Table 5.7 The data for the transformer in Figure 5.10

Rated power S_N	50 MVA
Rated frequency f_N	60 Hz
Leakage inductance	0.1 pu
Tap changer winding ?	No
Saturation enabled ?	Yes
Rated L-L voltage U_{1N} in winding 1	70.71068 kV (rms)
Rated L-L voltage U_{2N} in winding 2	70.71068 kV (rms)
Ratio yoke/winding-limb length	2.0
Ratio yoke/winding-limb area	1.0

The transformer in Figure 5.10 has the same magnetizing characteristic as the transformer in test case 1.

The magnetizing current I_m is defined as:

$$I_m = I_1 - I_2 \tag{5.7}$$

The circuit in Figure 5.10 was simulated in PSCAD/EMTDC version 3. The magnetizing curve in Figure 5.11 was obtained in steady state.

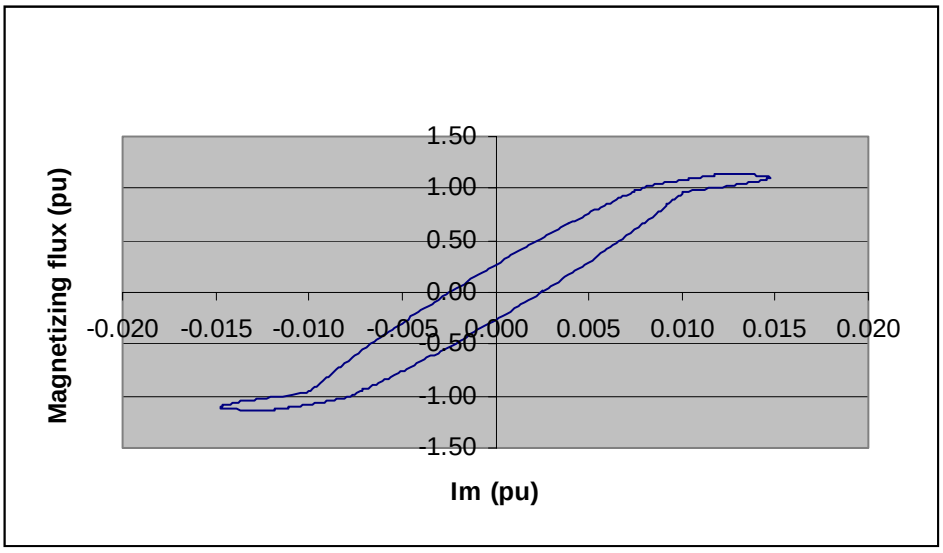


Figure 5.11 Magnetizing curve for the transformer in steady-state operation of the circuit in Figure 5.10

Figure 5.11 shows a clear hysteresis effect. This hysteresis effect may not necessarily give any wrong results. However, what causes this effect is unknown and this causes an uncertainty when using the UMEC model in a simulation.

Conclusion:

Hysteresis seems to be present when using the UMEC transformer model in PSCAD/EMTDC. This is not in correspondence with [19], and the reason for this is unknown. This causes an uncertainty when using the UMEC transformers in simulations.

5.1.3 Conclusion

Despite the new possibilities of the UMEC transformer model it has been shown that there are some uncertainties when using it. It was also observed that the UMEC transformer caused the simulation time to increase significantly. Because of these factors and the fact that the transformer with saturation modelled as a current source earlier has been successful in simulations of core saturation instability, the transformer with saturation modelled as a current source is preferred in the simulations in this thesis.

5.2 The on-line Fast Fourier Transform

The Fast Fourier Transform (FFT) [20] is used to find harmonic components in a signal. This may be useful in many application, for instance if it is desired to control a device in such a way that it directly influences one or more harmonic components in the electric-grid. The advantage of using the FFT is that it works as an infinitely sharp bandpass filter, which causes the controller for the desired harmonic component not to be influenced by any other harmonics. In this way the harmonic controller for the desired harmonic component will not influence the overall system when this component is not present. With an analog bandpass filter this would not necessarily be the case. However, there are pitfalls when using the FFT also. Therefore it is important to know its weaknesses when using it in a simulation in PSCAD/EMTDC. Section 5.2.1 considers the FFT function in PSCAD/EMTDC.

5.2.1 The on-line frequency scanner used in PSCAD/EMTDC

Because of the advantage of being able to find the 50 Hz component in the DC-current when dealing with control methods against core saturation instability the on-line frequency scanner in PSCAD/EMTDC is of special interest. However, this component must be used with care. This section explains why.

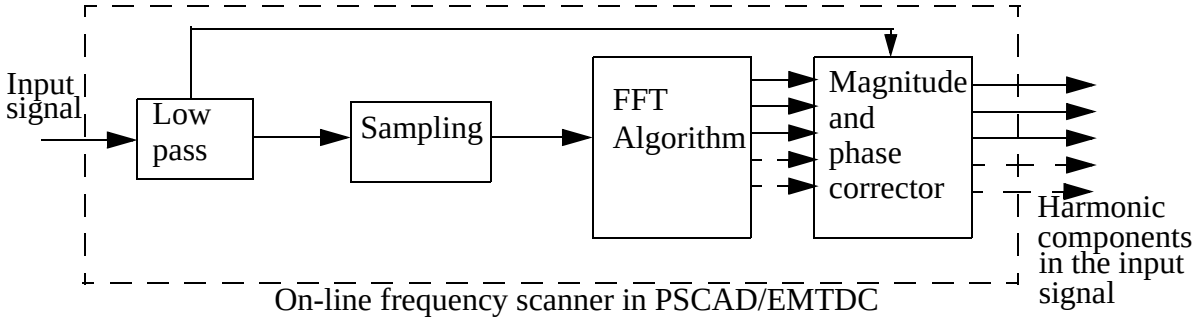


Figure 5.12 The inside of the FFT function in PSCAD/EMTDC

The lowpass filter is a 6th order Butterworth filter with a cutoff frequency depending on the number of harmonics in the output of the per fundamental period. This dependency is shown in Table 5.8. A Butterworth filter of order N with transfer function B(s) will have a magnitude that follows Equation (5.8) [21].

$$|B(j\omega)|^2 = \frac{1}{1 + (j\omega / j\omega_c)^{2N}} \tag{5.8}$$

ω_c is the cutoff frequency of the filter.

From Equation (5.8) it can be found that gain of the filter at the cutoff frequency will be approximately 0.707 or -3.01 dB. This is independent of the order of the filter. However, with a high order filter the gain will drop faster towards zero for frequencies higher than the cutoff frequency and have a flater characteristic for frequencies below the cutoff frequency than a low order filter. This is illustrated in Figure 5.13.

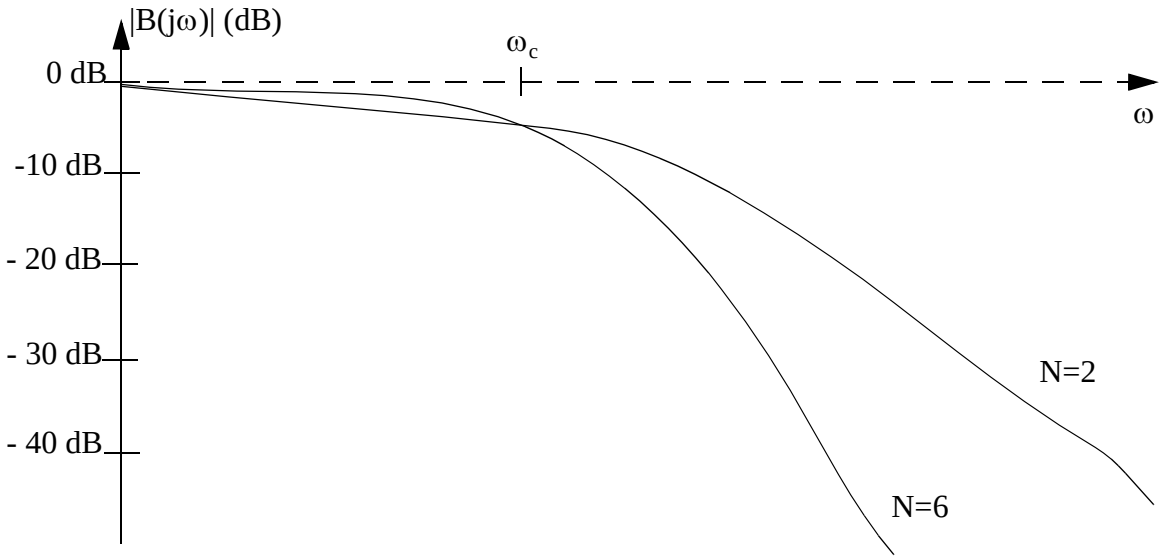


Figure 5.13 Illustration of gain on a logarithmic amplitude scale for Butterworth filters with N=2 and N=6.

This Butterworth filter will hinder aliasing i.e. modulation of low frequency components due to sampling of high frequency components. According to Nyquist's sampling theorem aliasing will occur if the sampling frequency ω_s is less than two times the maximum frequency in the signal ω_m [21]. By using the Butterworth filter the high frequency components of the input signal are suppressed and the effect of aliasing is therefore decreased. An illustration of an aliasing is shown in Figure 5.14. Table 5.8 shows the cutoff frequency of the Butterworth lowpass filter used in PSCAD/EMTDC as a function of the number of harmonics the user wants the FFT function to calculate. In the magnitude and phase corrector block in Figure 5.12 the errors in phase and magnitude caused by the lowpass filter are taken into consideration.

Table 5.8 The cutoff frequency in the Butterworth lowpass filter as a function of the number of harmonics which the FFT function is calculating

Number of harmonics calculated by the FFT function	Cutoff frequency/Fundamental frequency
7	6.75
15	13.5
31	27

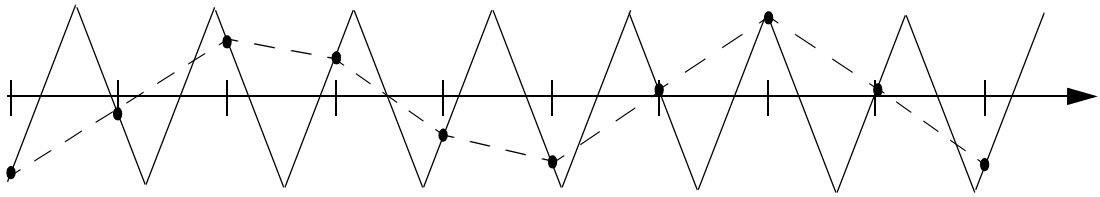
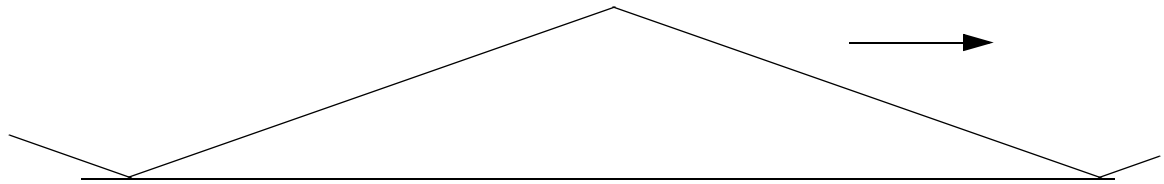


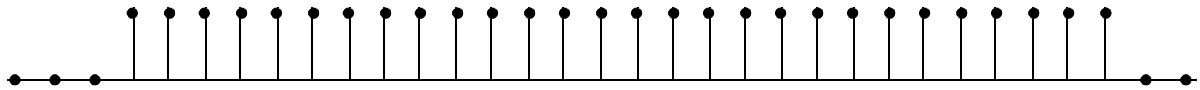
Figure 5.14 The aliasing effect: The original signal (solid line) has a different fundamental frequency than the reconstruction of the original signal (dashed line) which are based on the sampling of the original signal.

URN:NBN:no-2111

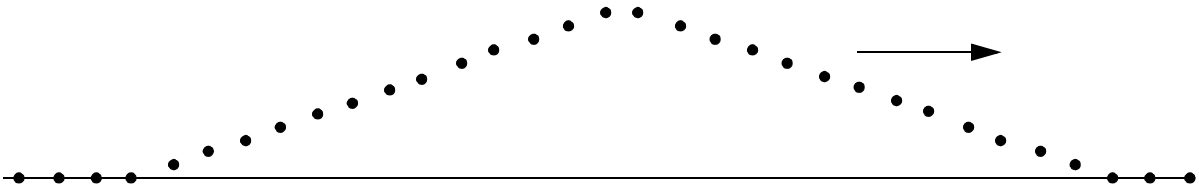
The output of the lowpass Butterworth filter is multiplied by a rectangular window function w[n], as shown in Figure 5.15. This is practically done by writing each sample instant into a buffer. The buffer contains as many values as samples per period (which are automatically defined as in Table 5.9) of the defined base frequency of the on-line frequency scanner. The number of samples per period of the defined base frequency of the on-line frequency scanner is automatically synchronized with this frequency. For instance if the base frequency of the on-line frequency scanner is defined to be 50 Hz (period time 0.02 seconds) and there are 64 samples per period it will be a sampling every $0.02 / 64 = 3.125 \cdot 10^{-4}$ seconds.



a) Output signal from the Butterworth filter



b) Window function w[n]



c) The product of w[n] and the output signal from the window function.
This is the signal the FFT uses to calculate harmonic components.

Figure 5.15 Sampling of the output signal from the Butterworth filter.

The width and the sampling rate of the w[n] is decided by the user-defined fundamental frequency and the number of harmonics the user wants to calculate. PSCAD/EMTDC gives the user three options about how many harmonic components of the input signal the FFT function calculates. In all cases the width of w[n] will be one period of the user-defined fundamental frequency. The connection used in PSCAD/EMTDC between the numbers of harmonics that the user wants to calculate and the sampling rate per period of fundamental frequency is shown in Table 5.9.

Table 5.9 Numbers of harmonics that can be accessed by the FFT function in PSCAD/ EMTDC and the corresponding sampling rate to these.

Number of harmonics the user defines the FFT function to calculate	Samples per period of the fundamental frequency
7	16
15	32
31	64

The FFT function calculates harmonic components at each sampling instance by using the sampled data in the buffer.

*** Example 5.1

Assume the base frequency of the on-line frequency scanner is set to 50 Hz (period time is then 0.02 seconds) and the numbers of harmonics the user defines the FFT to calculate is 31 (samples per period of the base frequency is then 64). At the sampling instance T, the FFT is based on the interval defined by (T-0.02) and (T). At the sampling instance T+0.02/64, the FFT is based on the interval defined by (T-0.02+0.02/64) and (T+0.02/64). In the simulation time steps between the interval defined by (T) and (T+0.02/64) the output of the FFT is based on the interval defined by (T-0.02) and (T).
***

Example 5.1 illustrates a good property with the on-line frequency scanner. It is able to follow changes in the low order harmonic components of the input signal since the FFT will not use values of measured signals that are more delayed than the time between two sampling instances (true if the defined base frequency is for instance 50 or 60 Hz which are typically fundamental frequencies in power systems). The basis function for computation of the phase angles of the harmonic components is a fundamental frequency cosine waveform starting at time=0. This means that all phase angles that the FFT output is relative to this fundamental frequency cosine signal.

An important phenomenon to have in mind when using the FFT is the Gibbs phenomenon [20]. Gibbs phenomenon causes the frequency response of the FFT to have some undesirable oscillations. This is due to the fact that the digital signals used in the FFT have finite length. To achieve an understanding of this, some theory is first presented. First the frequency of discrete signals is considered.

It is assumed that the digital signal has arisen because of sampling of a continuous signal. The time difference between two samples is labelled T. A signal with frequency ω[rad/s] is sampled with a sample time T. The discrete signal which arises will then have a dimensionless frequency Ω given by:

$$\Omega = \omega T \tag{5.9}$$

*** Example 5.2:

A continuous signal contains two frequencies, ω_1=1000 rad/s and ω_2=3000 rad/s. The signal is sampled with sample time T= 0.001 s. The discrete signal that arises will have two dimensionless frequencies. Ω_1 corresponds to ω_1, and Ω_2 corresponds to ω_2.

$$\Omega_1 = 1000 \cdot 0.001 = 1$$

$$\Omega_2 = 3000 \cdot 0.001 = 3$$

***

The ideal frequency response of the FFT is together with its time domain signal is shown in Figure 5.16. Ω_1 corresponds to the highest frequency component which the FFT can find. The impulse response $h_d[n]$ is found by the inverse discrete Fourier transform [20]:

$$h_d[n] = \frac{1}{2\pi} \cdot \int_{2\pi} H_D(\Omega) e^{j\Omega n} d\Omega = \frac{1}{2\pi} \cdot \int_{-\Omega_1}^{\Omega_1} H_D(\Omega) e^{j\Omega n} d\Omega = \frac{1}{n\pi} \sin(n\Omega_1) \tag{5.10}$$

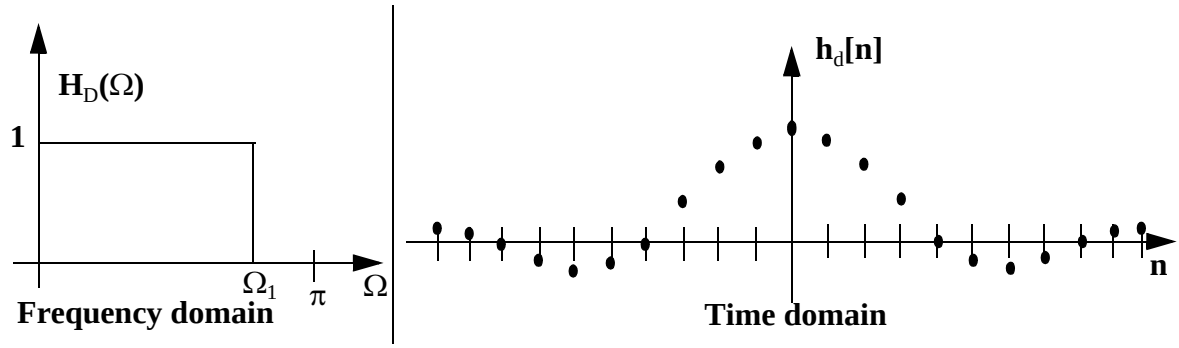


Figure 5.16 The ideal impulse response of the FFT and the corresponding infinite length time domain signal.

A rectangular window function w[n] is given by:

$$w[n] = \begin{pmatrix} 1, & -M \le n \le M \\ 0, & \text{otherwise} \end{pmatrix} \tag{5.11}$$

The frequency domain representation of w[n] can be found from the discrete-time Fourier Transform:

$$W[\Omega] = \sum_{n=-\infty}^{\infty} w[n] e^{-j\Omega n} = \frac{\sin\left[\Omega\left(M + \frac{1}{2}\right)\right]}{\sin\left(\frac{\Omega}{2}\right)} \tag{5.12}$$

The time domain and frequency domain graphs of the signal w[n] typically have the shape as in Figure 5.17.

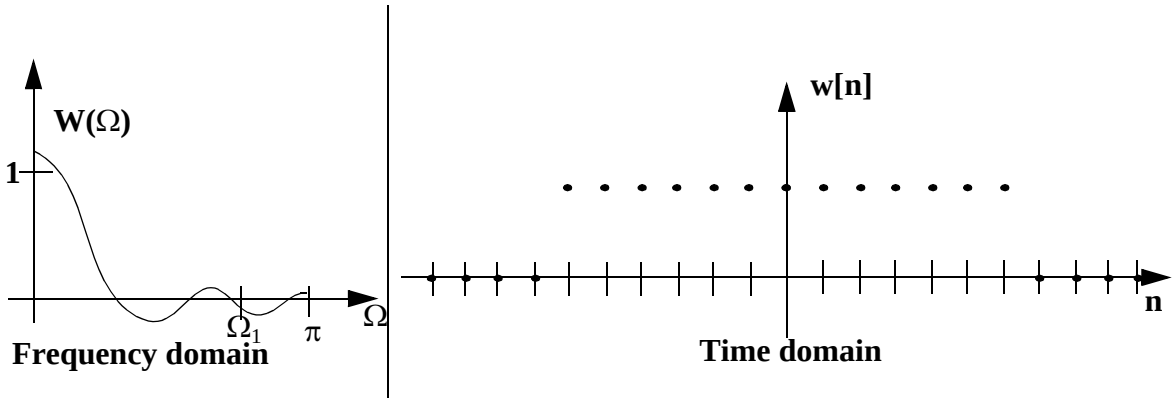


Figure 5.17 A rectangular window and its frequency response

The actual frequency response $H_A(\Omega)$ of the FFT included the window function w[n] is the convolution of $H_D(\Omega)$ and $W(\Omega)$.

$$H_A(\Omega) = H_D(\Omega) \otimes W(\Omega) = \frac{1}{2\pi}\int_{-\pi}^{\pi} H_D(\theta)W(\Omega-\theta)d\theta \qquad (5.13)$$

*** Example 5.3:

Assume the length of the window 2M=4 and that the dimensionless cutoff frequency $\Omega_1 = 2$ rad. From Equation (5.13) $H_A(\Omega)$ is found to be:

$$H_A(\Omega) = \frac{4\cos(0.5\Omega-1)^3\sin(0.5\Omega-1)-4\cos(0.5\Omega-1)^3\sin(0.5\Omega-1)-2}{\pi}$$

By using Maple version 5, $H_A(\Omega)$ was plotted:

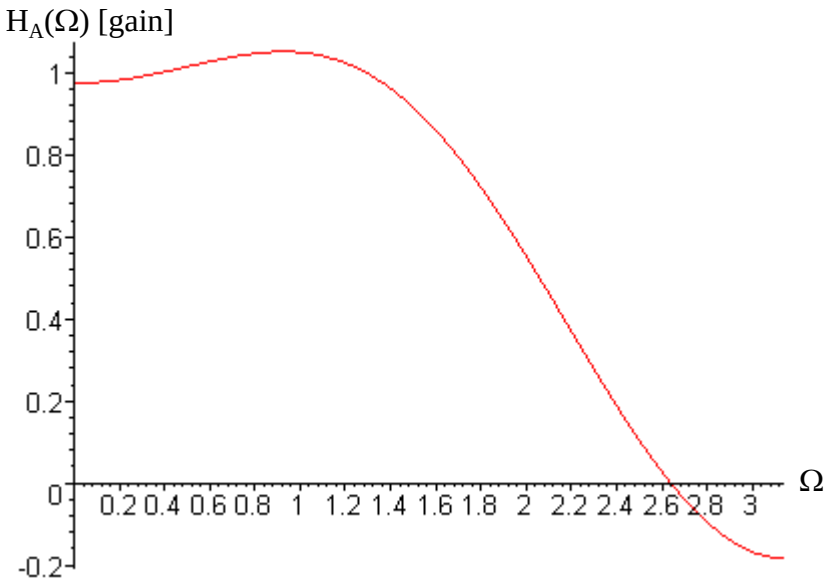


Figure 5.18 $H_A(\Omega)$ when M=2

URN:NBN:no-2111

If the length of the window 2M is increased to 30 then Maple version 5 plots $H_A(\Omega)$ as shown in Figure 5.19:

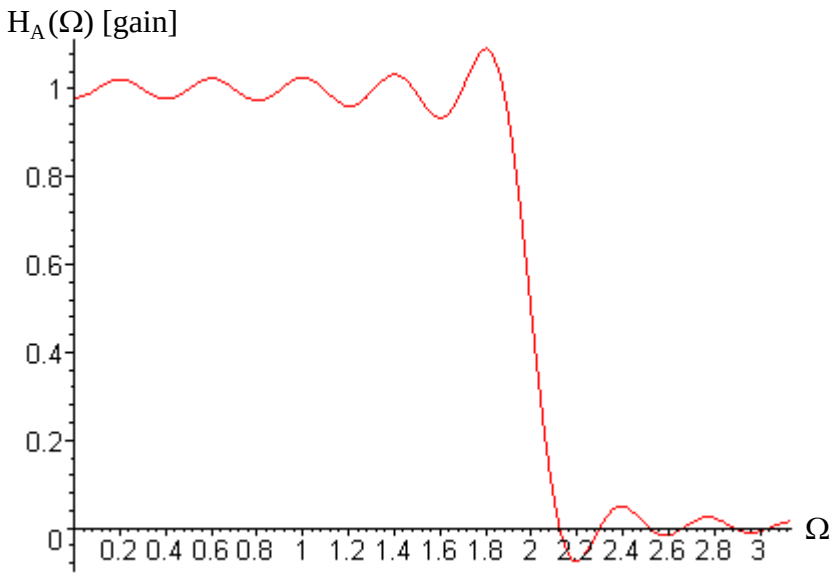


Figure 5.19 $H_A(\Omega)$ when M=15

***

$H_A(\Omega)$ and $h_a[n]$ are typically like illustrated in Figure 5.20.

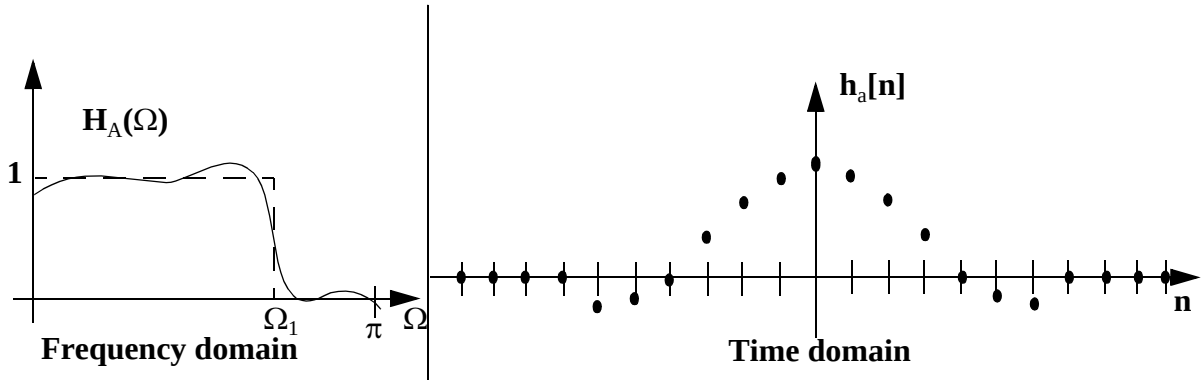


Figure 5.20 Impulse response of the FFT included the window function

The use of the finite length rectangular window corresponds to a direct truncation of the infinte duration impulse response and lead to a solution exhibiting ripples before and after the discontinuity of the ideal frequency response. This is the Gibbs phenomenon. The Gibbs phenomenon causes an error in some of the calculated frequency components in the input signal. The nearer a frequency component is to the discontinuity frequency Ω_1 the larger error is it likely to have. The maximum ripple will according to [20] not be more than around 9 per cent. If the length of the rectangular window is increased the ripples in $H_A(\Omega)$ will bunch more closely around the nominal cutoff frequency Ω_1. However, the ripple magnitudes will not be decreased. Nevertheless, the errors for lower frequency components will practically vanish. This is illustrated in Figure 5.21.

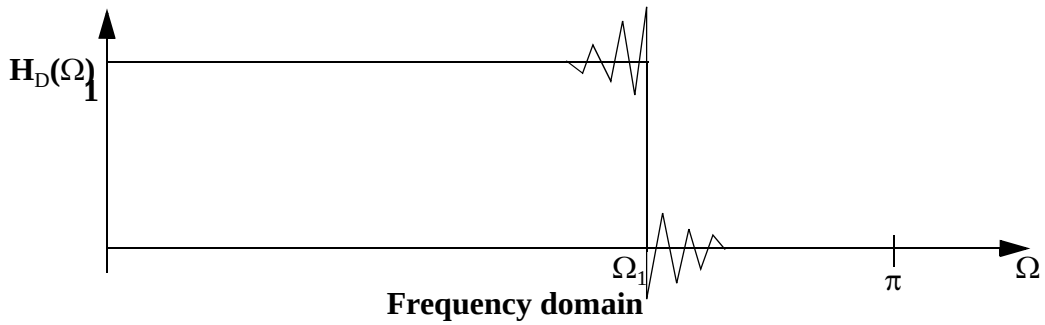


Figure 5.21 Gibbs phenomenon around the point of discontinuity. The length of the rectangular window is long such that Gibbs phenomenon for lower frequencies has vanished.

A good approximation of the lower harmonic components will be obtained if the bandwidth of the on-line frequency scanner is much higher than the fundamental frequency of the signal analysed. This can be obtained by choosing the on-line frequency scanner to calculate as many harmonics it is able to (31 harmonics). The on-line help module in PSCAD/EMTDC version 3 states that Gibbs phenomenon, is usually not a problem with harmonics of the fundamental frequency. This is a result of using rectangular data windows.

Another aspect to be aware of when using the on-line frequency scanner is that inter/sub-harmonics in the input signal of the on-line frequency scanner might cause an error in the calculation of harmonics even during stationary operation of a circuit. The discrete Fourier transform (DFT) of a signal x[n] is given by:

$$X[k] = \sum_{n=0}^{N-1} x[n] \cdot e^{-\left(j \cdot \frac{2\pi kn}{N}\right)} \tag{5.14}$$

N is the number of samples in the sampling interval.
X[k] is the values of the samples on the frequency axis, k=0, 1 ,...., N-1.
x[n] is the sampled signal in the time domain, n=0, 1,...., N-1

To illustrate the DFT Figure 5.22 is considered. Part a) shows the digital signal x[n]. Part b) shows the spectrum of x[n]. This spectrum is continuous with period 2π. Part c) shows the absolute values of the discrete Fourier transform of x[n]. Part d) shows the inverse discrete Fourier transform of X[k].

URN:NBN:no-2111

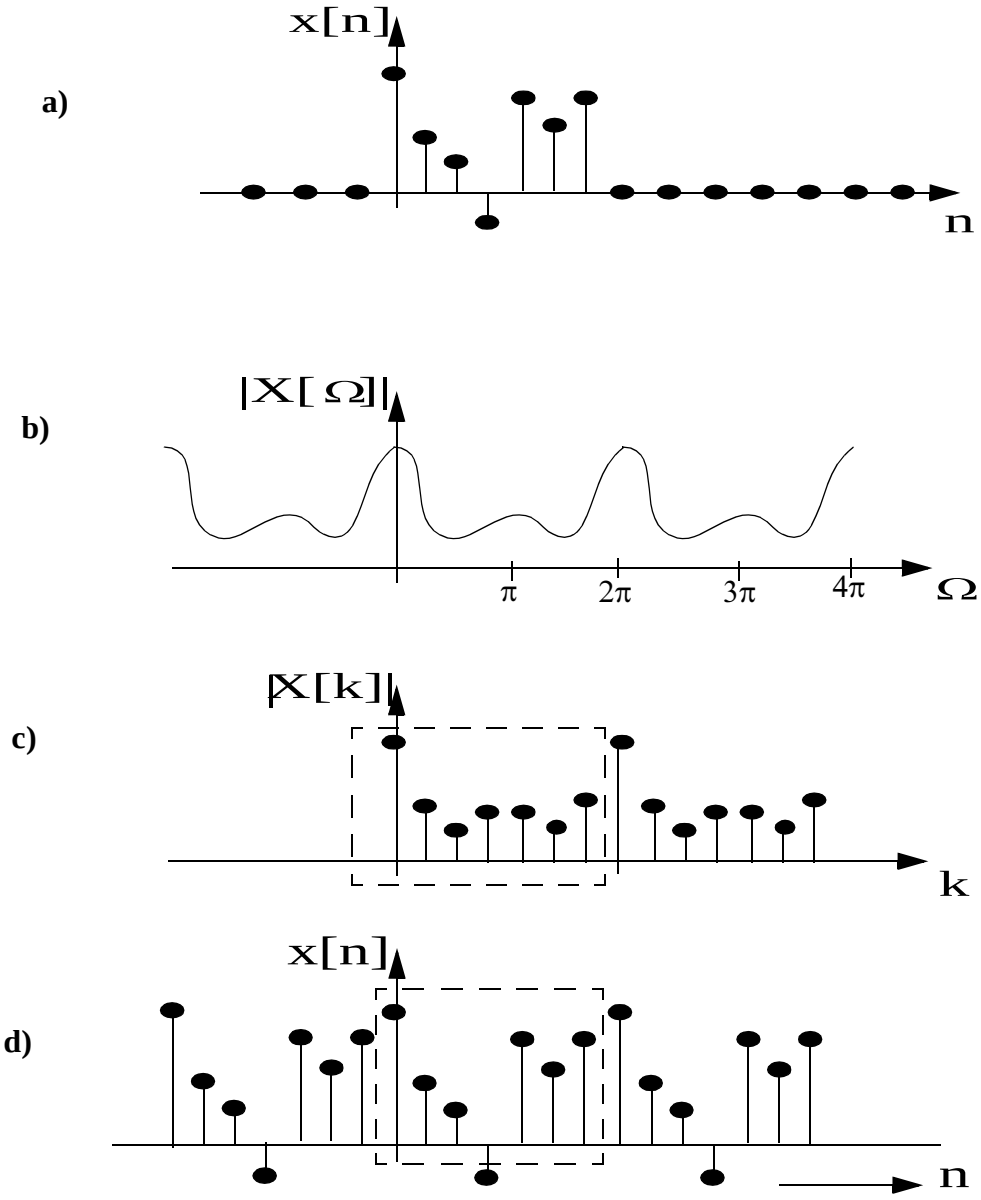


Figure 5.22 Illustration of the DFT

The FFT algorithm is a method that calculates the discrete Fourier transform in a very efficient manner [20]. Thus, the results from the FFT will not differ from the results from the discrete Fourier transform, but the calculation time of the frequency components is much faster with the FFT. From Equation (5.14) it is clear that only the DC component and frequency components which are multiples of $\frac{2\pi}{N}$ are calculated by the FFT. If the user defined base frequency of the on-line frequency scanner is set to 50 Hz, this will correspond to the dimensionless discrete frequency $\frac{2\pi}{N}$. All the other frequencies found by the FFT will correspond to multiples of this frequency. As a consequence if a signal contains frequencies which are not a multiple of the base frequency of the on-line frequency scanner these will not be calculated. However they might influence the frequency components that are calculated and cause errors in the

frequencies that are calculated by the on-line frequency scanner. [21] explains this. It it is assumed that a signal contains one frequency component of order i (i is an integer) and amplitude one (the base frequency of the DFT has order one). The ideal discrete frequency of this signal will then be as in Figure 5.23.

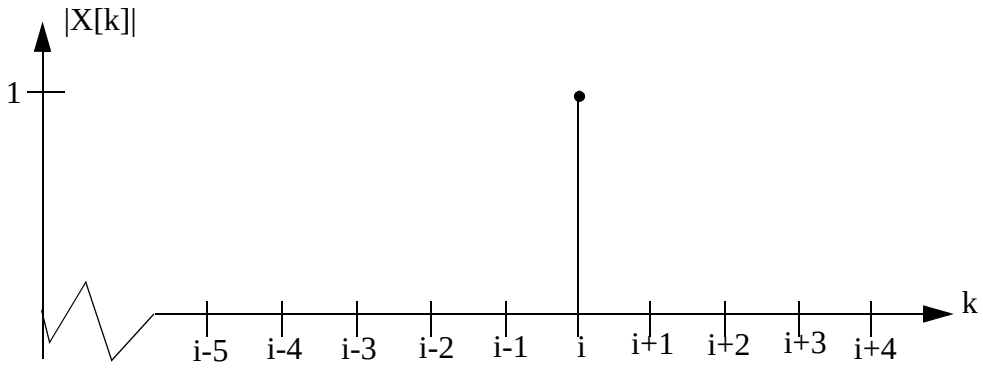


Figure 5.23 The discrete frequency response of a signal with harmonic order i.

If the frequency in the signal with frequency spectrum as in Figure 5.23 changes to a frequency in middle between harmonic order i-1 and i, the discrete frequency response might look as in Figure 5.24.

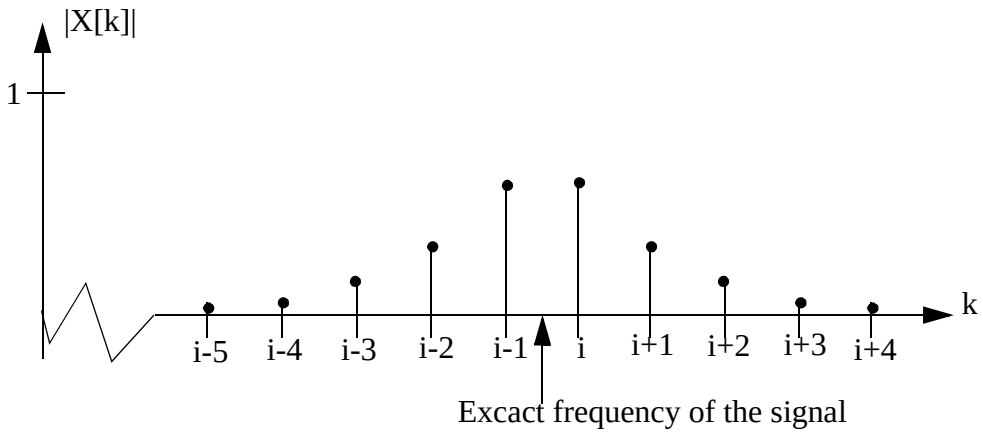


Figure 5.24 The discrete frequency response of a signal with frequency between harmonic order i-1 and i.

A signal with frequency much closer to i in Figure 5.24 would have caused a spectrum like in Figure 5.25.

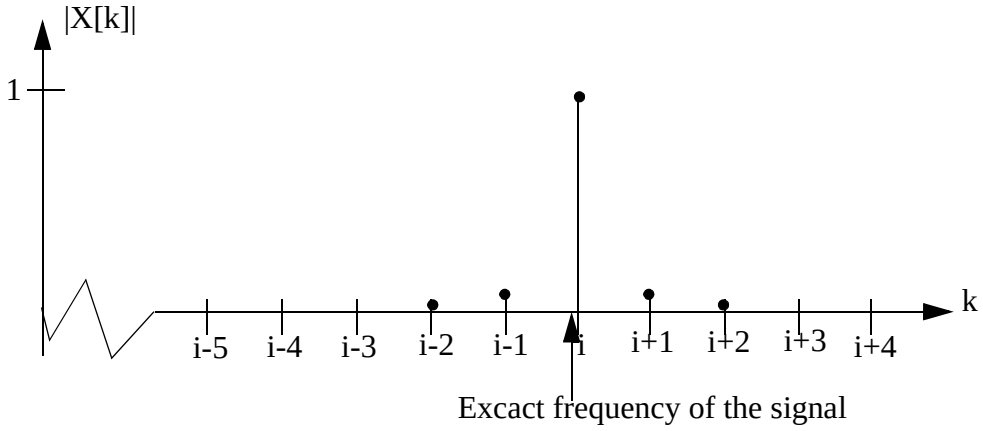


Figure 5.25 The discrete frequency response of a signal with frequency near the harmonic frequency i.

URN:NBN:no-2111

*** Example 5.4

In PSCAD/EMTDC a very simple case was simulated to show the undesired effect inter-harmonics has on the calculations performed by the FFT. The system simulated is shown in Figure 5.26.

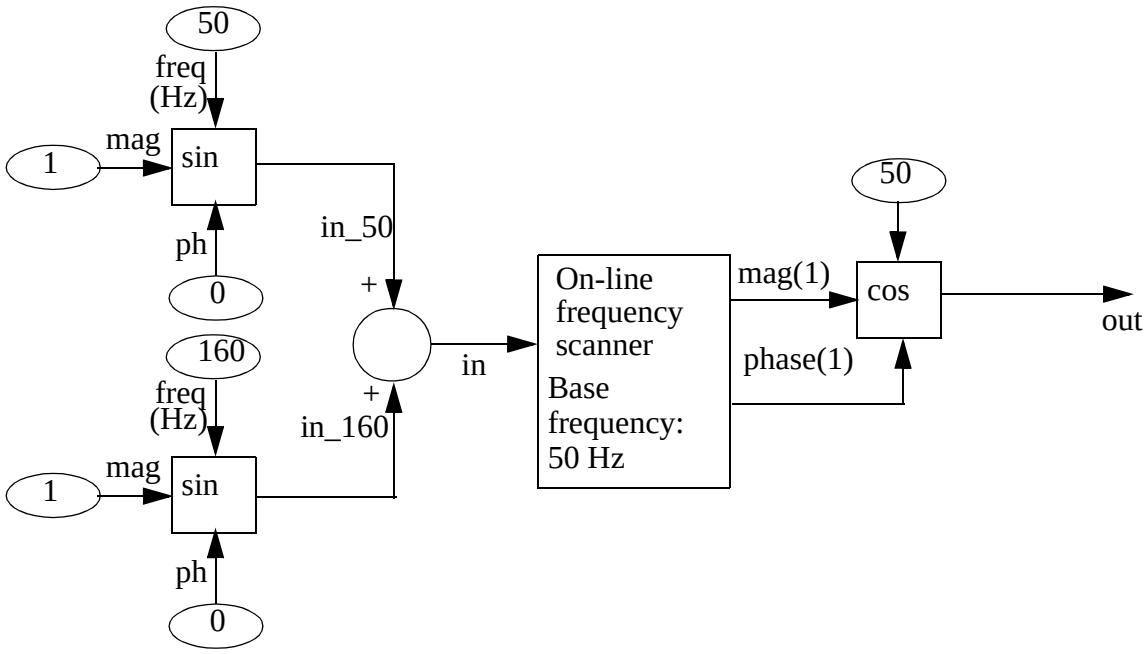


Figure 5.26 System simulated to show the error an inter-harmonic can cause on the output signal of the on-line frequency scanner.

The simulation was performed with 2 μs time step to obtain a very good accuracy. The plot step was 10 μs. The on-line frequency scanner was initiated to calculate 31 harmonic components with a base frequency equal to 50 Hz. Figure 5.27-5.30 show the simulation results.

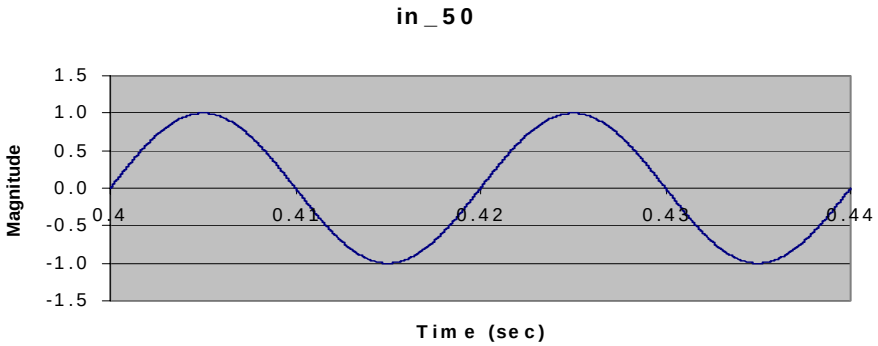


Figure 5.27 The 50 Hz component of the input signal to the on-line frequency scanner.

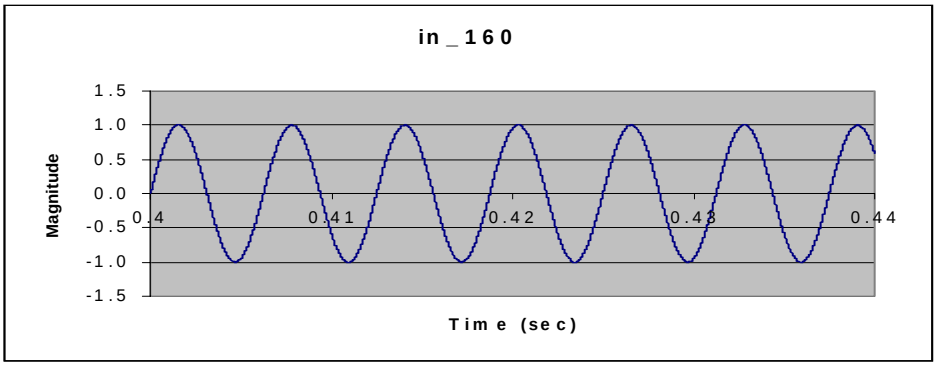


Figure 5.28 The 160 Hz component of the input signal to the on-line frequency scanner.

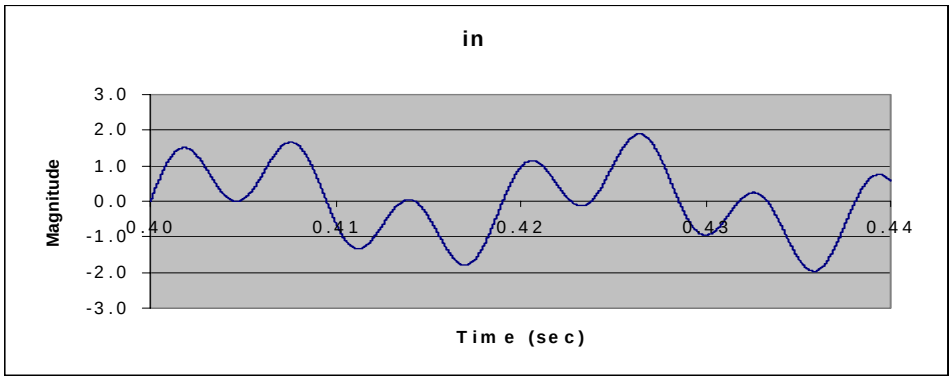


Figure 5.29 The input signal of the on-line frequency scanner.

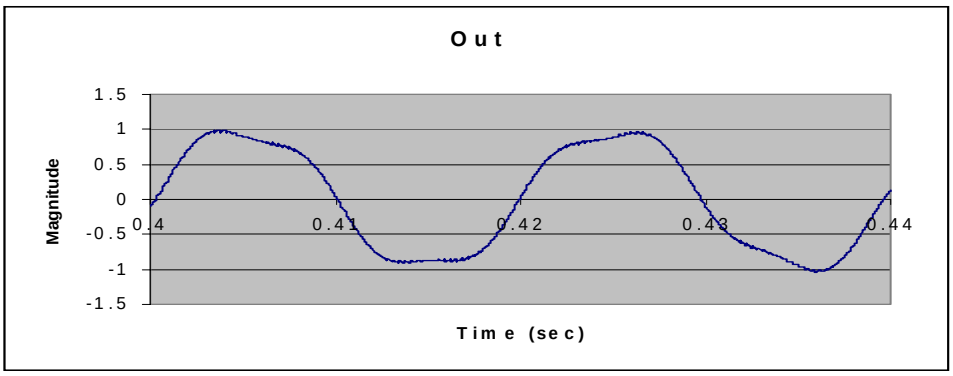


Figure 5.30 The replication based on the output from the on-line frequency scanner of the 50 Hz component in the input signal to the on-line frequency scanner.

***

It is seen from the signal in Figures 5.27 and 5.30 that the FFT does not give a true replication of the magnitude and phase for the 50 Hz component in the input signal. This is due to the inter-harmonic component in the input signal of the on-line frequency scanner.

URN:NBN:no-2111

This inter/sub-harmonic influence on the harmonic components is very important to be aware of when using a FFT in a control system. Undesired noise may cause a sensitive control system to drive a system into instability. Fortunately, the inter/sub-harmonic components are normally much lower than the harmonic components in an HVDC system. At least this will be true for low order harmonics. Thus, the distortion of the Out signal in Figure 5.29 would normally been much less. This fact makes the use of the on-line frequency scanner in an HVDC control system possible. However, it must be used wisely to avoid or decrease the influence of the drawbacks. If it is desirable to use the FFT to find a single frequency component in a signal it is recommended to combine it with an analog bandpass filter tuned to the frequency component that one wants to find. How this is done is shown in Figure 5.31.

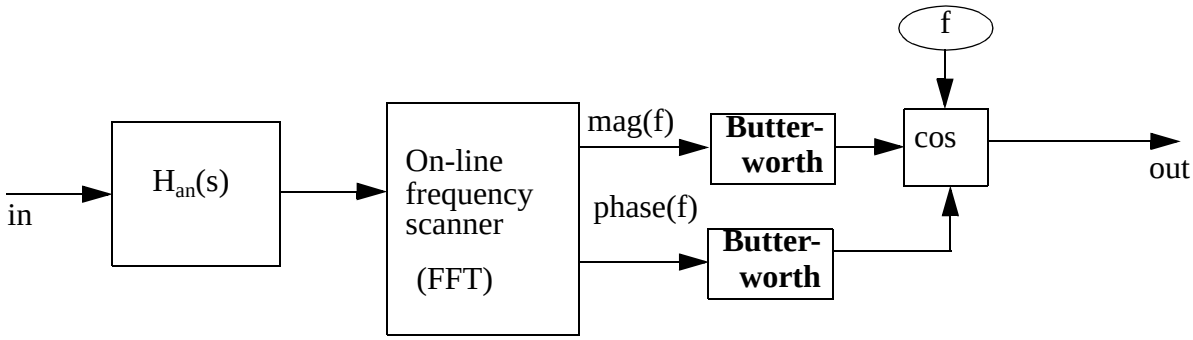


Figure 5.31 Combination between an analog filter and a FFT function. The aim is that the out-signal contains the frequency component with frequency f in the in-signal.

in is the input signal.
out is the output signal.
f is frequency in the input signal that it is desired to find.
$H_{an}(s)$ is the analog bandpass filter tuned to frequency f. $H_{an}(s)$ may have the block diagram as $H_2(s)$ in Figure 4.2.

$H_{an}(s)$ will filter away most of the inter-harmonic content in the input signal in. In this way the errors caused by inter-harmonics in the output of the FFT function are reduced. However, inter-harmonics may still have significant influence on the phase and magnitude output of the on-line frequency scanner. This will especially be the case if the component with frequency f (see Figure 5.31) in the input signal normally is small or zero. The lowpass Butterworth filter on the phase output of the on-line frequency scanner will reduce the influence from the inter-harmonics on the out-signal. An example is used to illustrate how this work.

*** Example 5.5:

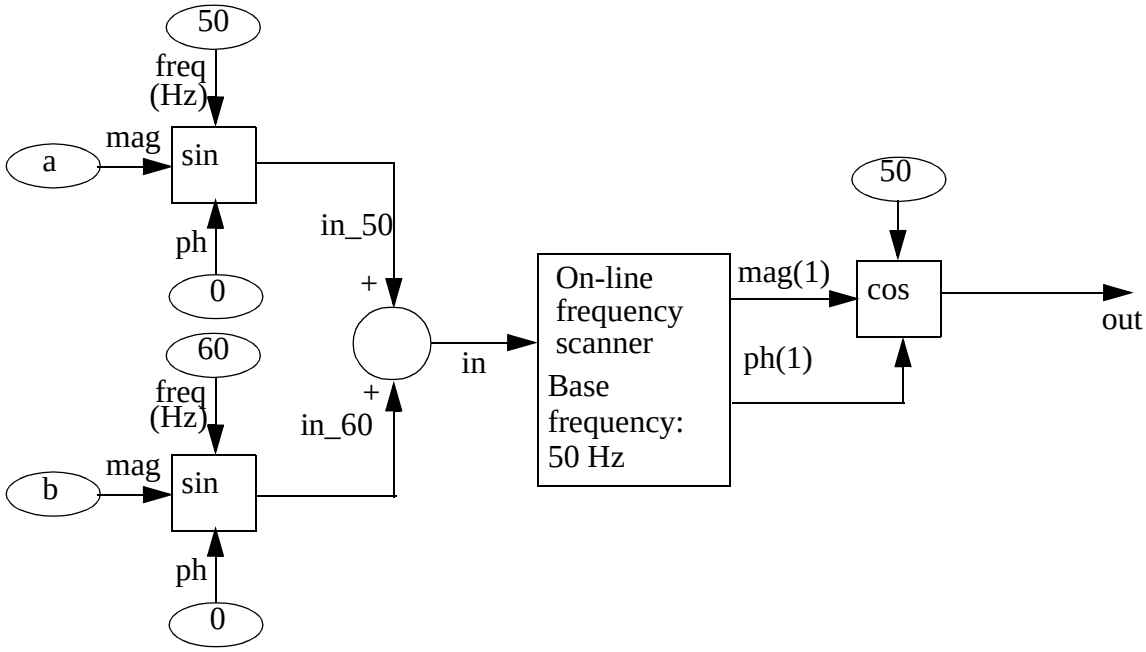


Figure 5.32 System used to simulate how phase and magnitude output is influenced by an inter-harmonic component.

The on-line frequency scanner has base frequency 50 Hz and the outputs from it corresponds to integer multiples of 50 Hz. mag(1) is the calculated magnitude of the 50 Hz component in the input signal of the on-line frequency scanner. ph(1) is the calculated phase of the 50 Hz component in the input signal of the on-line frequency scanner. The system in Figure 5.32 is used for the simulations in cases 1 and 2 below.

Case 1: a=1.0 and b=0.1.

mag (1) and ph(1) are shown in Figure 5.33 and 5.34 respectively.

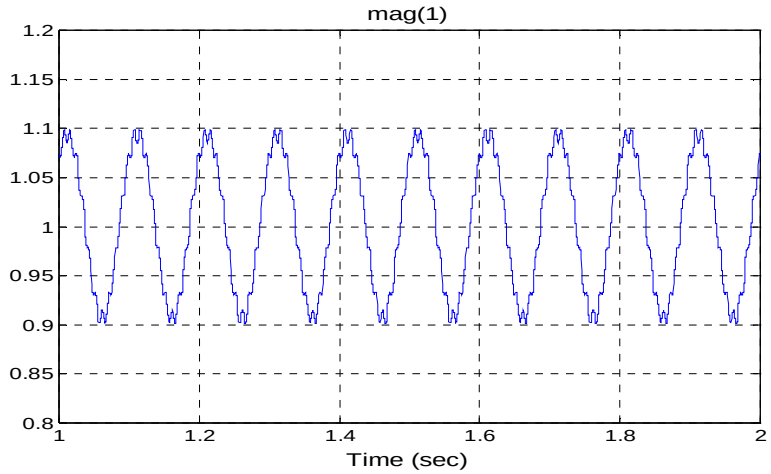


Figure 5.33 mag(1).

URN:NBN:no-2111

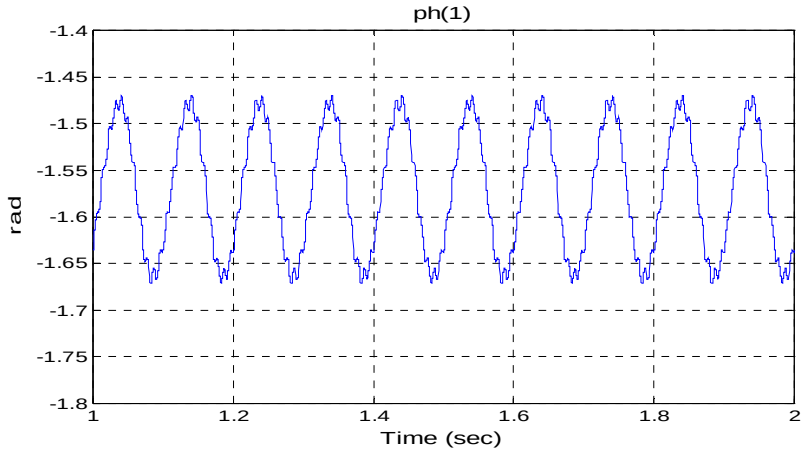


Figure 5.34 ph(1).

Case 2: a=0.1 and b=0.1

mag (1) and ph(1) are shown in Figure 5.35 and 5.36 respectively.

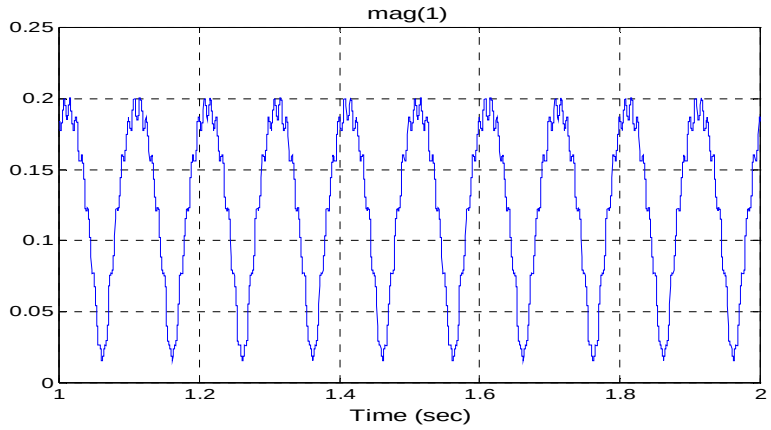


Figure 5.35 mag(1).

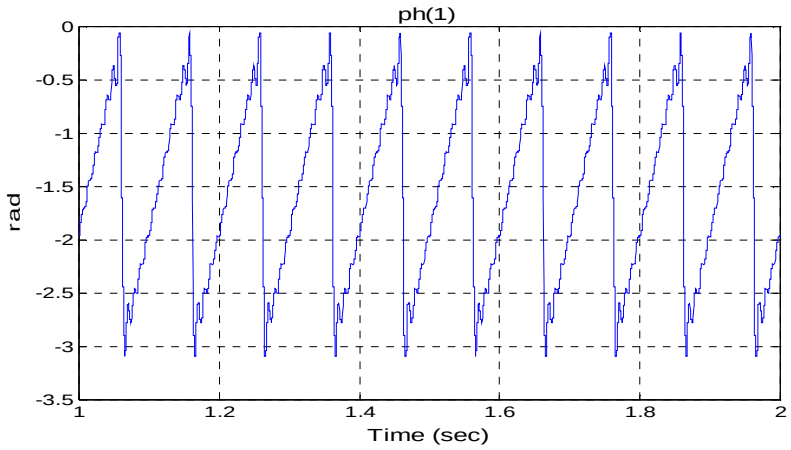


Figure 5.36 ph(1).

It is seen from cases 1 and 2 that when a and b are equal in size the variation in ph(1) becomes much larger than when a is ten times b. mag(1) experience roughly the same variation in both case 1 and 2. It is seen from Figure 5.35 that the DC value of mag(1) is a bit larger than a, this is because the 60 Hz component will influence mag(1). It is also seen from Figure 5.33-5.36 that the 60 Hz component in the input signal of the FFT causes a 10 Hz variation in both ph(1) and mag(1). As a conclusion it can be said that when a is not much larger than b, the mag(1) and ph(1) output may be very wrong. To deal with this problem lowpass Butterworth filters are inserted into the system as in Figure 5.37. The lowpass Butterworth filters have cutoff frequency at 4 Hz and order 3.

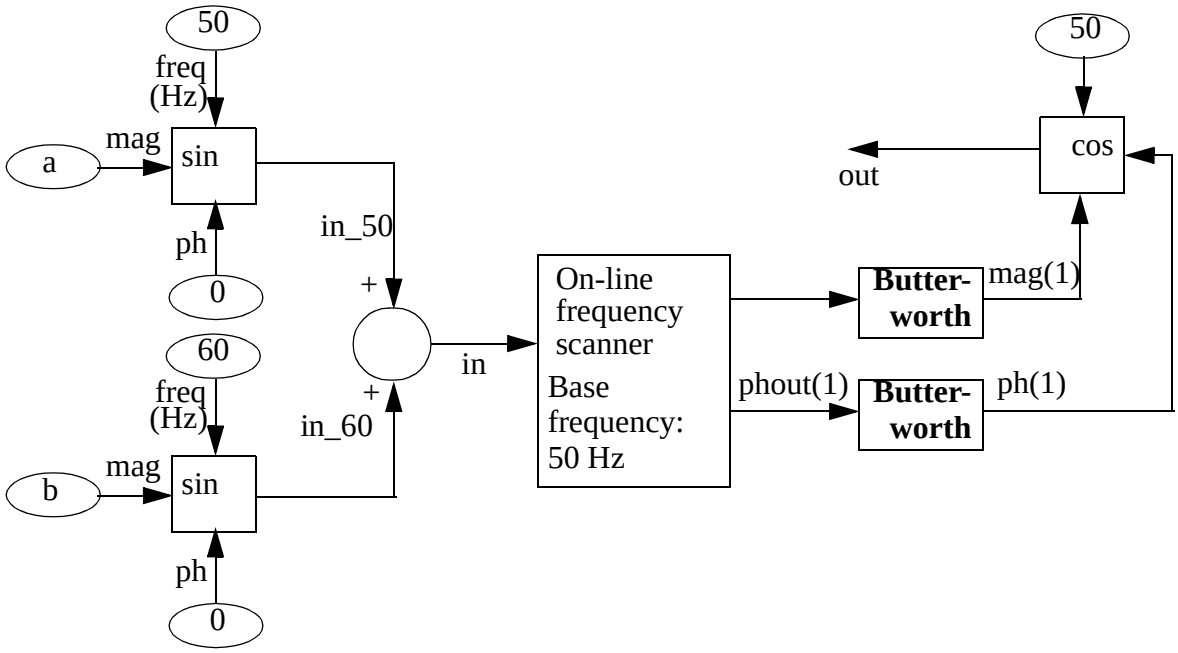


Figure 5.37 Butterworth filters included in the system.

Cases 3 and 4 below build on the system in Figure 5.37.

Case 3: a=1.0 and b=0.1.

mag (1) and ph(1) are shown in Figure 5.38 and 5.39 respectively.

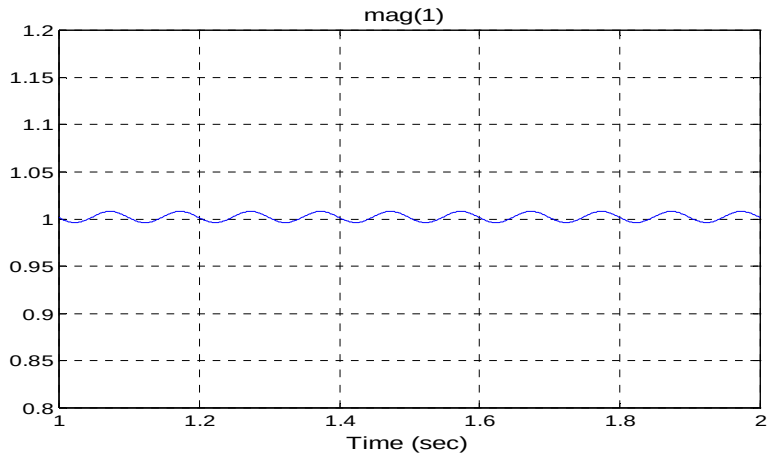


Figure 5.38 mag(1).

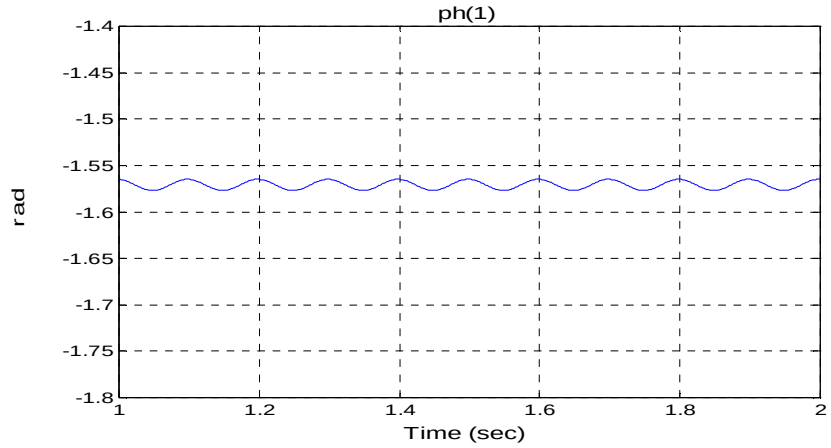


Figure 5.39 ph(1)

Case 4: a=0.1 and b=0.1.

mag (1) and ph(1) are shown in Figure 5.40 and 5.41 respectively.

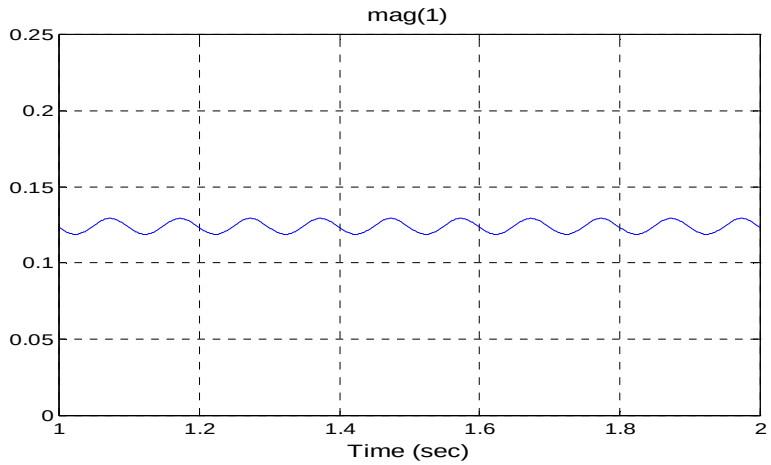


Figure 5.40 mag(1).

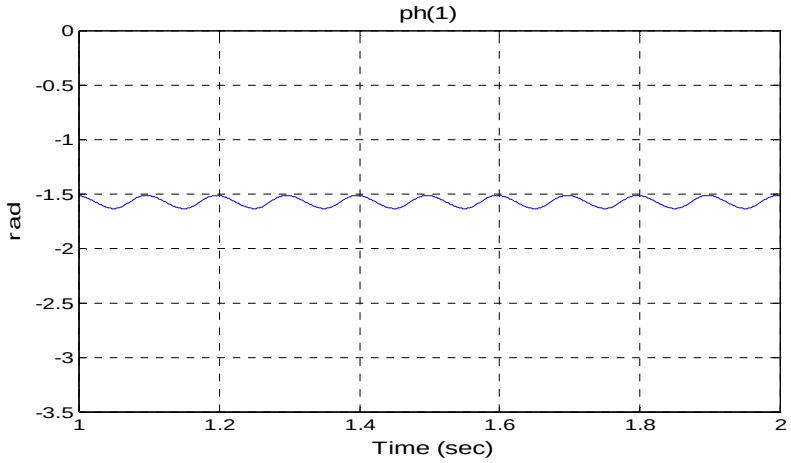


Figure 5.41 ph(1).

Figure 5.38-5.41 shows that the Butterworth filters have worked well. The variation in both mag(1) and ph(1) is much smaller than when the Butterworth filters were not present. This means that the influence of the 60 Hz component in the input signal is significantly decreased. However, from Figure 5.40 it is seen that mag(1) is still larger than a. To deal with this the combination between an analog bandpass filter and the FFT function in Figure 5.31 was used. Cases 5 and 6 demonstrate how this was achieved. The block diagram of the analog filter used for the simulations of cases 5 and 6 is shown in Figure 5.42. The parameters in the filter in Figure 5.42 are shown in Table 5.10.

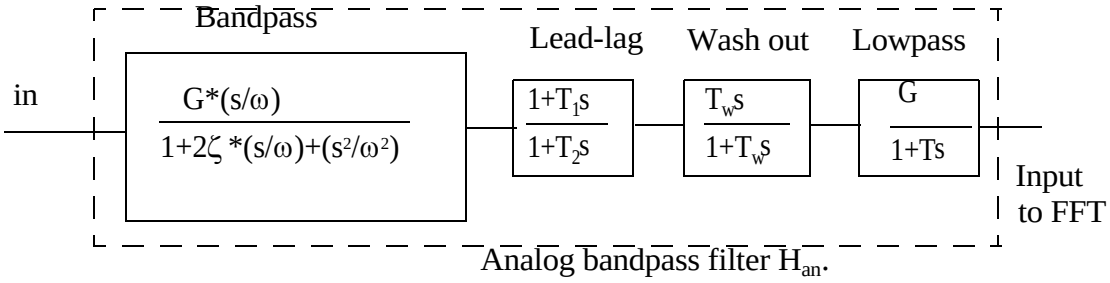


Figure 5.42 Block diagram of analog bandpass filter.

Table 5.10 Data for the analog bandpass filter in Figure 5.42

G	ω (rad/s)	ζ	T_1 (s)	T_2 (ms)	T_w (ms)	T (s)
62.591776	314.1593	0.05	0.0254	6.95	1	2

Case 5: a=1.0 and b=0.1.

mag (1) and ph(1) are shown in Figure 5.43 and 5.44 respectively.

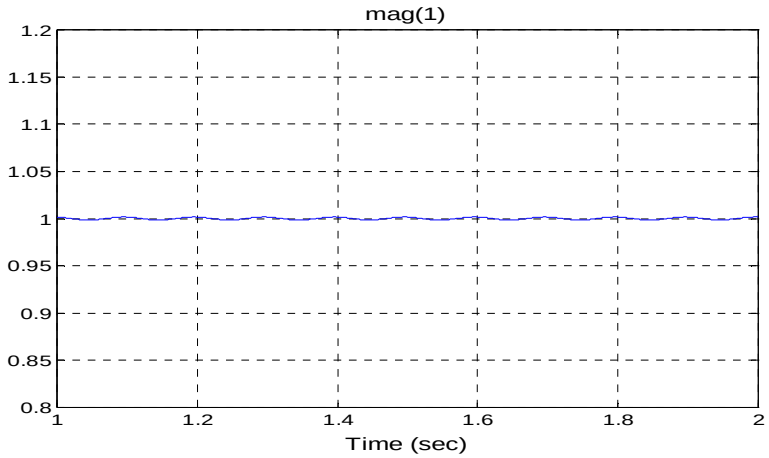


Figure 5.43 mag(1).

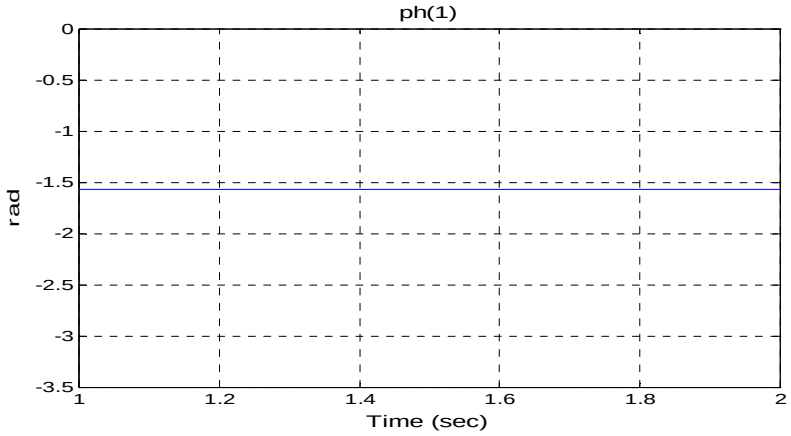


Figure 5.44 ph(1).

Case 6: a=0.1 and b=0.1.

mag (1) and ph(1) are shown in Figure 5.45 and 5.46 respectively.

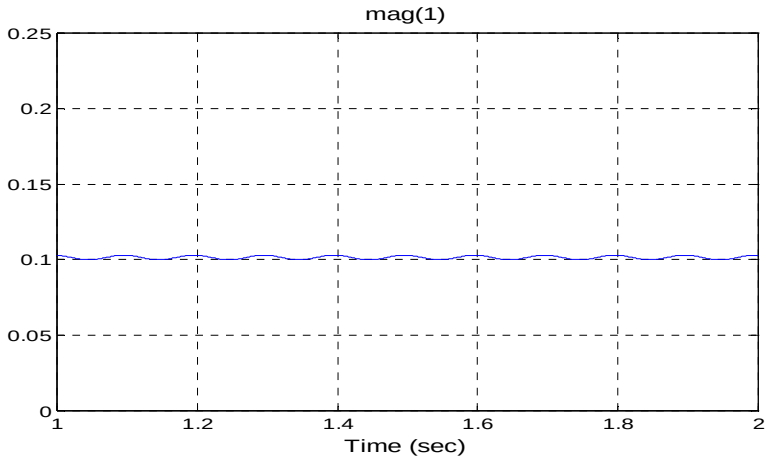


Figure 5.45 mag(1).

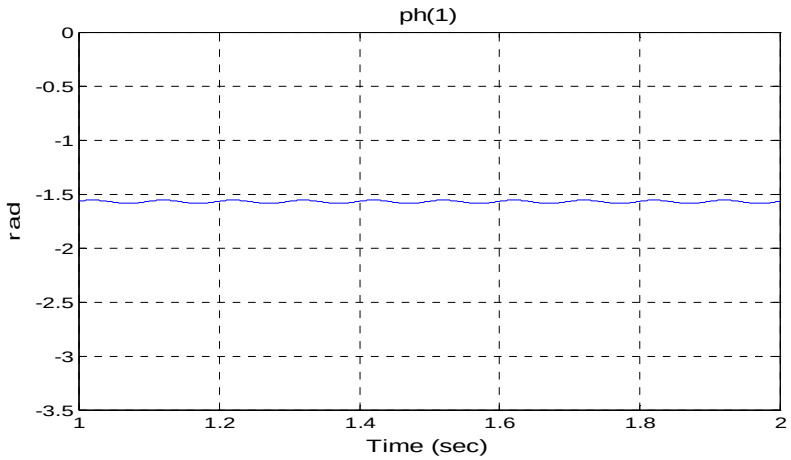


Figure 5.46 ph(1).

***

Despite all the promising results shown in the example just above, there is also a drawback with the configuration in Figure 5.31. This will be illustrated by the example below.

*** Example 5.6:

It is assumed that the same configuration as used in Example 5.5, cases 5 and 6 is used. The only difference is that the input signal a=0.1 and has frequency 53 Hz, while signal b=0.0. The response in the phase output of the online-frequency scanner before it has been filtered by the lowpass Butterworth filter is shown in Figure 5.47 and the response in phase output of the online-frequency scanner after it has been filtered by the lowpass Butterworth filter is shown in Figure 5.48 (see Figure 5.37).

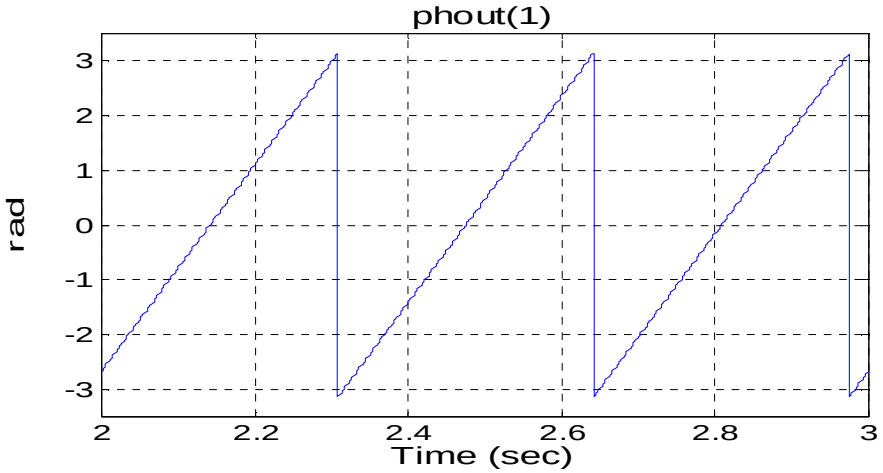


Figure 5.47 phout(1)

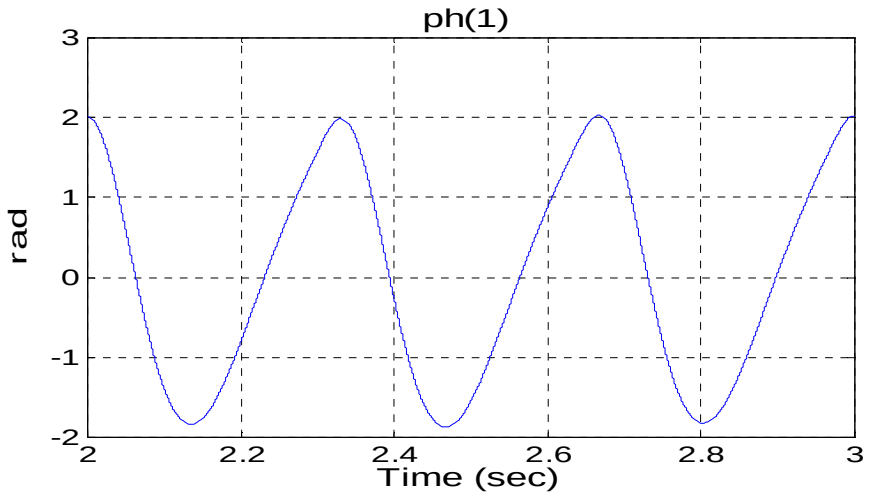


Figure 5.48 ph(1)

From Figures 5.47 and 5.48 it can be seen that ph(1) have different frequency components than phout(1). Thus, the signal out (see Figure 5.37) will contain more frequency components than the signal in. A frequency spectrum of the signal out is shown in Figure 5.49. It is clear that the out signal has many more frequency components than the in signal (which only has a 53 Hz component).

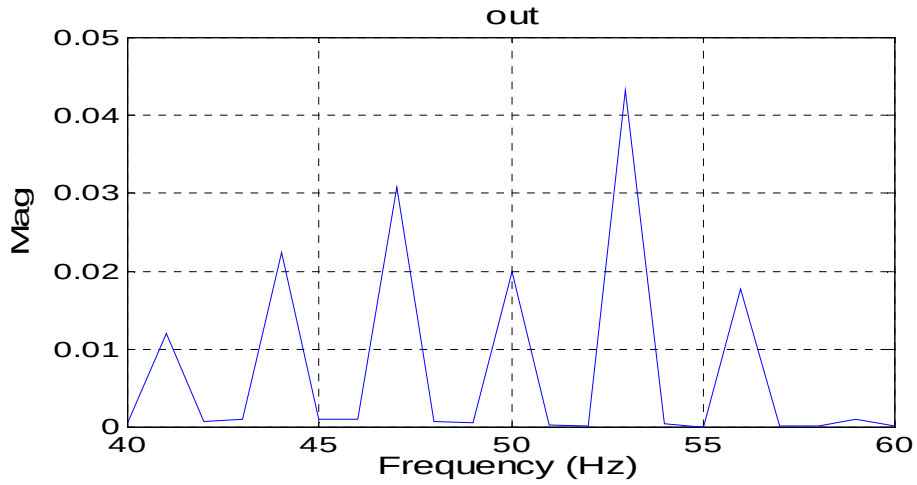


Figure 5.49 out.

If the frequency of the input signal is moved further away from 50 Hz the variation in phout(1) will be filtered by the lowpass Butterworth filter (this is indicated in Example 5.5). Thus, the problem illustrated in this example is only a problem if the input signal has frequencies near 50 Hz.
***

The FFT calculations must in real life be performed by a digital signal processor (DSP). The Texas Instruments DSP TMS320C2000 [23] uses on a 40 MHz processor 0.1888 ms to perform a FFT on 32 samples and 0.2068 ms to perform a FFT^{-1}on 32 samples [24]. The FFT and FFT^{-1} functions used in the simulations in this thesis are performed based on the last 16 samples of the input signal to the FFT function. The input signal of the FFT function is sampled every 1.25 ms. Thus, the FFT functions used in here are possible to perform in real life on the Texas Instrument DSP TMS320C2000.

5.2.2 Conclusions

There are some concerns when using the on-line frequency scanner in PSCAD/EMTDC.

One of the major concerns is that inter-harmonics in the input signal of the on-line frequency scanner might cause errors in calculation of the harmonic components in the input signal. It was shown in section 5.2.1 that if the purpose of the on-line frequency scanner is to find one harmonic component in the input signal, the error in this component due to inter-harmonics can be significantly reduced by first filtering the input signal through an analog bandpass filter tuned to the frequency of the desired harmonic component. It should also be mentioned even though it was not analysed in section 5.2.1 that the influence from the inter-harmonics on the harmonic components calculated by the on-line frequency scanner may be reduced by choosing a low base frequency for the on-line frequency scanner.

Another significant concern was analysed in Example 5.6. However, if the frequency of the input signal of the on-line frequency scanner gradually drifts from 50 Hz towards 53 Hz the on-line frequency scanner will be able to adjust its base frequency. In this way the generation of undesired frequency components in Example 5.6 is avoided. It is much more likely that there

will be a gradually drift from 50 Hz to 53 Hz in the input signal of frequency scanner, than that a 53 Hz compononent suddenly appears in the input signal of the on-line frequency scanner. Thus, the drawback shown by Example 5.6 should not be taken to seriously.

One should be aware of Gibbs phenomenon, especially for the higher order harmonics calculated by the on-line frequency scanner.

5.3 Power electronic components

Power electronic devices are essential in HVDC transmission. It is therefore important that these are modelled in an adequate way to obtain good results when simulating an HVDC system for the purpose of finding harmonics. Switching of power electronic components can for instance be based on an event such as the zero crossing of a voltage. However, such an event may occur between two time steps in a simulation program like PSCAD/EMTDC version 3. This causes the switching to occur in worst case almost one time step later than it should. The result of this may be voltage spikes, non-characteristic harmonics, erroneous numerical interactions between switching devices in close proximity [25]. Sections 5.3.1 and 5.3.2 outlines how the thyristor and the IGBT are modelled in PSCAD/EMTDC version 3, and how the program deals with switching events occurring between two time steps.

5.3.1 The thyristor

The thyristor in PSCAD/EMTDC version 3 is modelled as an off/on resistance, with forward voltage drop and parallel snubber [6].

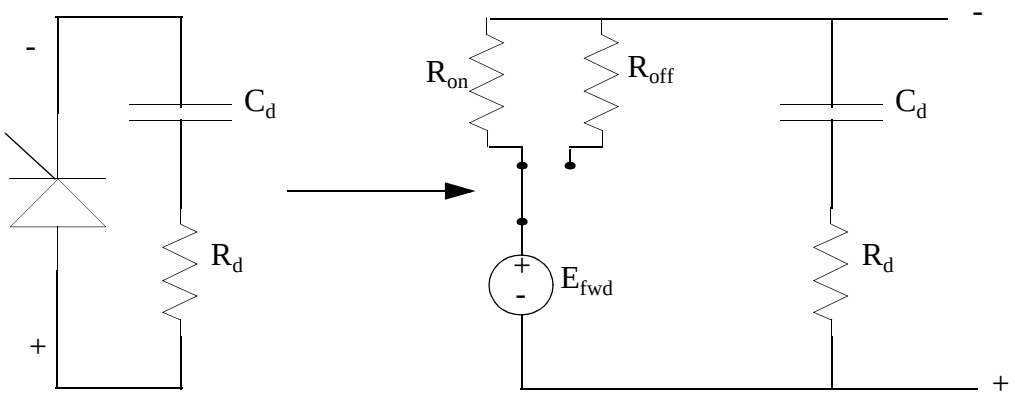


Figure 5.50 Thyristor and snubber equivalent circuit model

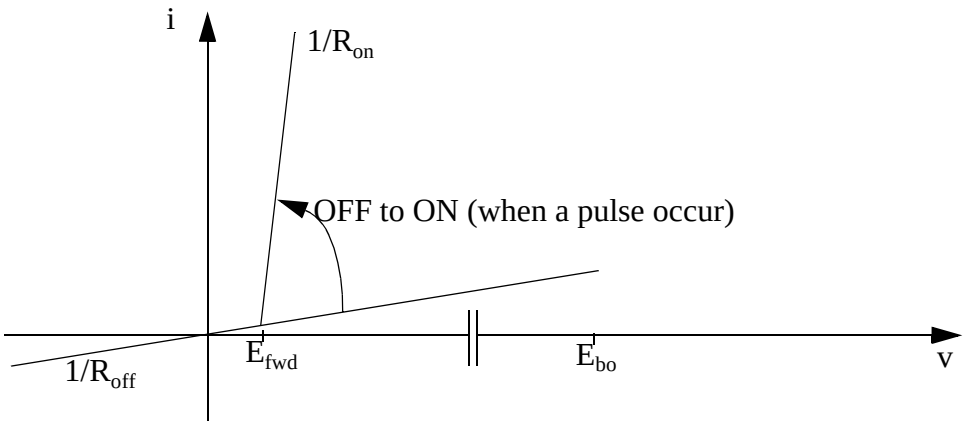


Figure 5.51 v-i characteristic of the thyristor model

The thyristor turned on by a fire pulse at the gate terminal or by the forward breakover voltage. This fire pulse is provided from an external control system. There are three situations that can cause the thyristor to turn on:

- The forward bias voltage is greater than or equal to the forward voltage drop E_{fwd} and the fire pulse parameter IPUL of the thyristor is one. Under this situation the turn on is not interpolated.
- The forward bias voltage is greater than or equal to E_{fwd} and the turn on time (alternative to the fire pulse parameter IPUL) has been reached. In this situation the turn on is interpolated and occur exactly at the right instant.
- The forward bias voltage is greater than or equal to forward breakover voltage. This is an interpolated turn on and occurs exactly at the specified voltage level.

The thyristor will appear as a small resistance R_{on} when in ON state and a large resistor R_{off} when in OFF state. To turn the thyristor off the external power circuit must force the current through it to zero. The turn off is always interpolated and will therefore occur at the correct instance. Also included in the thyristor model is the extinction time (user defined). The thyristor re-fires if the extinction time has not elapsed before the forward voltage rises above E_{fwd} following a turn off even in the absence of a turn on pulse.

As mentioned, to have as accurate results as possible when simulating it is desirable to have the correct turn on time and turn off time of the thyristor. Interpolation is used to achieve this. The interpolation used for the turn off process is described with Figure 5.52 as an aid.

URN:NBN:no-2111

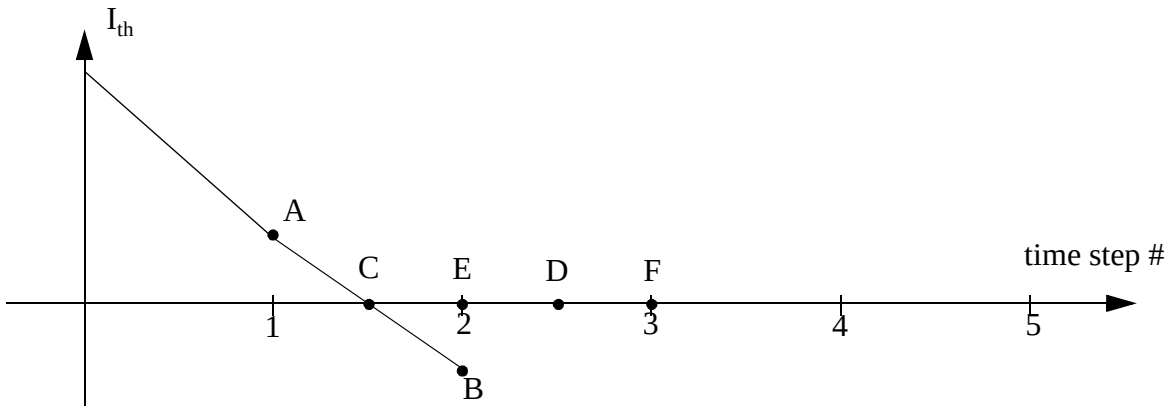


Figure 5.52 Thyristor: interpolated turn off

Between time steps 1 and 2 the thyristor current becomes negative. EMTDC discovers this when it has calculated the circuit solution at time step two. From its check list EMTDC knows that if the thyristor current changes from positive to negative from one time step to the next it must interpolate to the instant of the zero crossing of the thyristor current. When this instant has been found EMTDC calculates the circuit solution at that instant. If no more switchings appear in the circuit between time steps 1 and 2, EMTDC will move one time step ahead and calculate the circuit solution at time D. Then an interpolation is performed and the circuit solution at instant E is found. From this point the simulation proceeds as normal.

The interpolation used for the turn on process is based on the commutation voltage(s) and the fire angle order. As shown in Section 2.3.1 a phase locked loop may be used to find the instant to fire the individual valves in a six-pulse or twelve-pulse HVDC converter. If this instant occurs between two time steps in the simulation the interpolated Thyristor/GTO firing pulses function finds the exact instant of turn on of the thyristor. This instant is sent to the thyristor (in reality it is the time between the time step the fire pulse went to one and the exact time of the turn on of the thyristor) together with the fire pulse. An interpolation is then done to fire the thyristor at the right moment.

5.3.2 The IGBT (or GTO)

The IGBT may be used in voltage source converters. In this thesis a voltage source converter built up by IGBTs was used as a part of a hybrid filter in a simulation. The IGBT can be turned on and off by firing pulses from an external control system applied to the gate terminals. By interpolation the exact turn on and turn off time of the IGBT can be found. This can be used by PSCAD/EMTDC to switch the IGBT at the right instance. If the current through the IGBT crosses zero it will be turned off. In this case interpolation causes the switching instant to be correct. The way of interpolating is as for the turn on and turn off of the thyristor.

The i-v characteristic of the IGBT is shown in Figure 5.53.

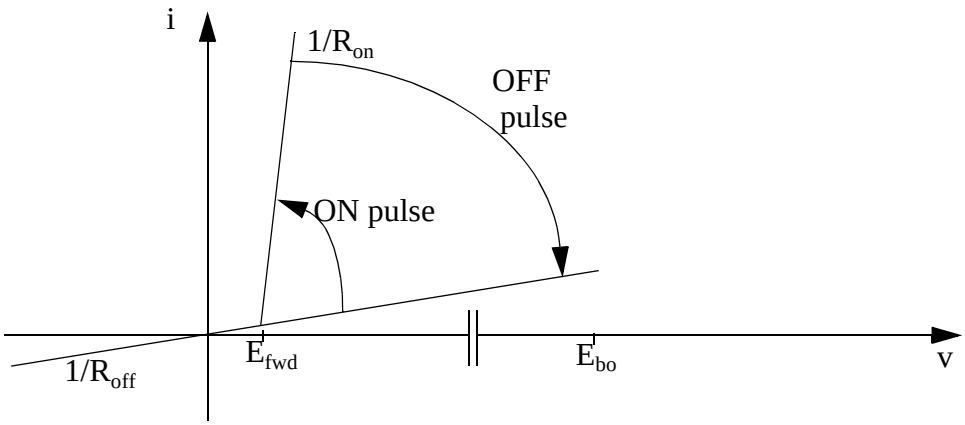


Figure 5.53 v-i characteristic of the IGBT model.

Just like the thyristor, the IGBT is represented by a small resistance R_{on} in on state, and a large resistance R_{off} in off state. In the same manner as for the thyristor the extinction time is included for the IGBT.

URN:NBN:no-2111

6 Simulation of core saturation instability

This chapter demonstrates the simulation of core saturation instability. The model used for simulation of core saturation instability will be the basis of the next chapter when different initiatives to prevent this phenomenon are demonstrated and analysed. The model used to simulate core saturation instability is a modified version of the CIGRE HVDC benchmark model [26]. The modifications of the CIGRE HVDC benchmark model were done to achieve a model with characteristics that caused core saturation instability to develop for a certain disturbance. In Section 6.1 below the CIGRE HVDC benchmark model will be described and results from simulations on this model presented. In Section 6.2 the modified CIGRE HVDC benchmark model will be described and results from simulations on this model are given.

6.1 The CIGRE HVDC benchmark model

The CIGRE HVDC benchmark model consists of an HVDC link connecting two AC-systems. The rated power transferred in the HVDC-link is 1000 MW and the rated current in the DC-link is 2000 A. The control system of the HVDC-link is included in the model. In this thesis, this system allows power flow only in one direction.

6.1.1 Electric system

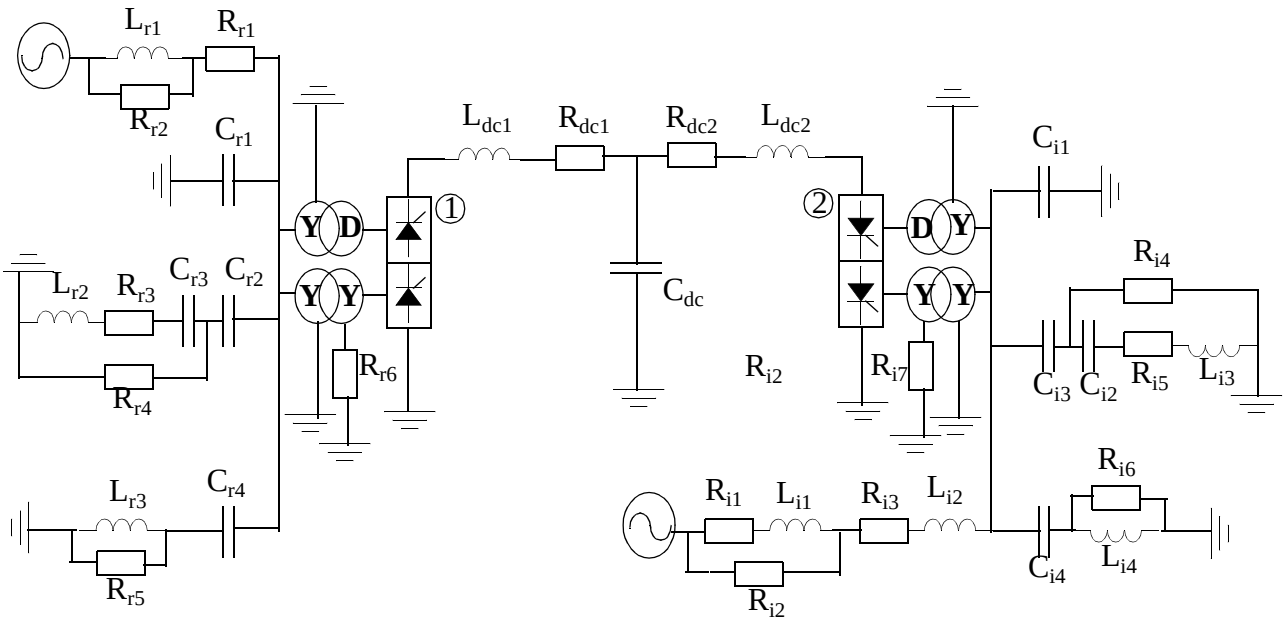


Figure 6.1 One-line diagram of the electric circuit in the CIGRE HVDC benchmark model.

The power flow is from converter 1 to converter 2. In Tables A1.1-A1.16 in Appendix 1 data for the components in Figure 6.1 is given.

6.1.2 Rectifier control system

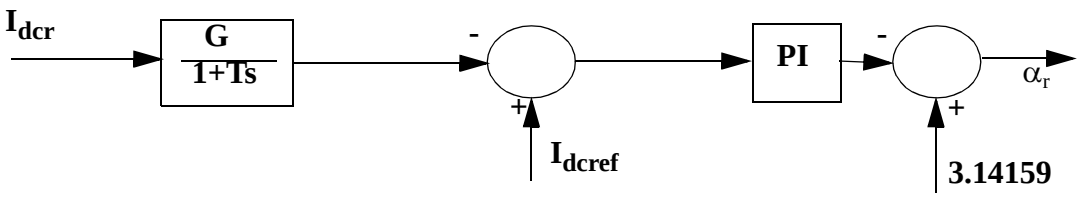


Figure 6.2 The control system for generating the fire angle order α_r

I_{dcr} is the measured current the rectifier injects into the DC side impedance.
I_{dcref} is the current it is desired that the rectifier injects into the DC side impedance. I_{dcref} is generated in the control system of the inverter and is decided by the desired power flow or faults (like commutation errors or short circuits).
α_r is the fire angle order of the rectifier. α_r is compared with triangular signals generated from a phase locked loop to generate fire pulses to the individual valves of the rectifier. The principle of this is shown in Section 2.3.1.

The data of the parameters in the lowpass filter and the PI-controller in Figure 6.2 are given in Tables A1.17 and A1.18 in Appendix 1.

The PI controller in the phase locked loop used to find the right firing instances for the rectifier has gain and integral time as shown in Table A1.19 in Appendix 1.

6.1.3 The inverter control system

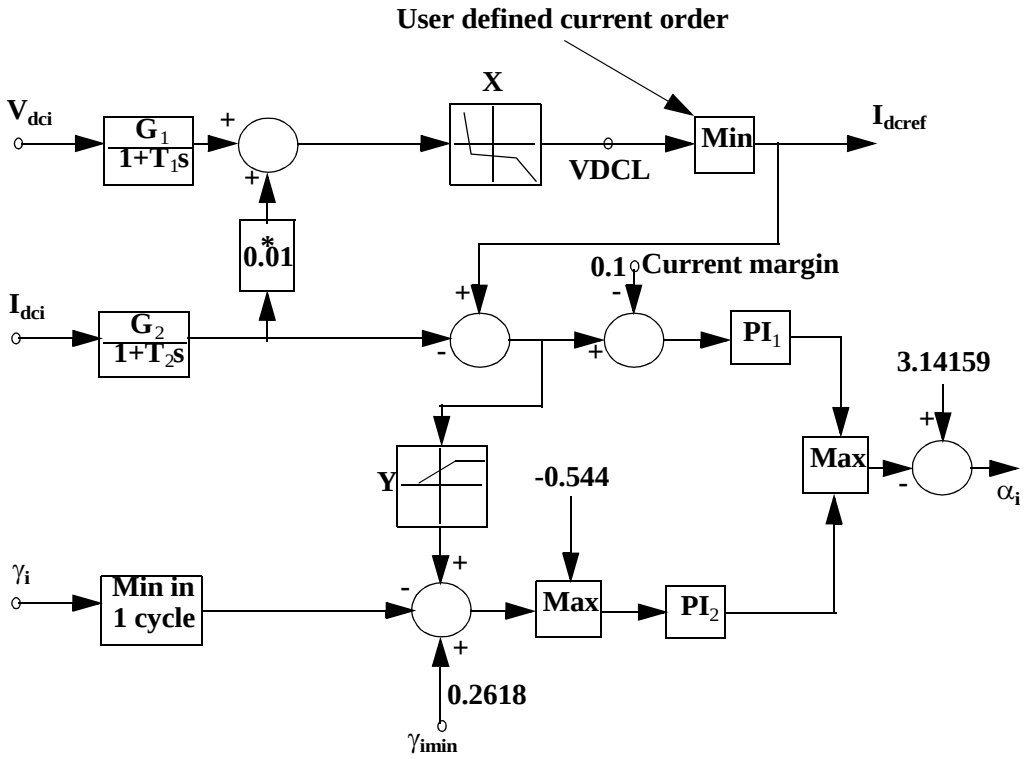


Figure 6.3 The control system for generating the fire angle order α_i for the inverter

V_{dci} is the voltage across the inverter.
I_{dci} is the current flowing from the DC side into the inverter.
γ_i is the measured extinction angle from the inverter after the last commutation.
VDCL is the output of the non-linear function that determines if the control system should operate in Voltage Dependant Current Order Limit (VDCOL).
PI_1 is active if the inverter is in constant current mode.
PI_2 is active if the inverter is in constant extinction angle mode.

The data of the parameters in the lowpass filters and the PI controllers in Figure 6.3 are given in Tables A1.20-A1.23 in Appendix 1.

Data for the non linear functions in Figure 6.3 are given in Tables A1.24 and A1.25 in Appendix 1.

The phase locked loop of the inverter bridge has a PI-controller with data as in Table A1.26 in Appendix 1.

6.1.4 Characteristics of the CIGRE HVDC benchmark model and simulation results

The focus in this section will be on the rectifier side of the CIGRE HVDC benchmark model as it would be redundant to focus on core saturation instability at both the rectifier and inverter sides. It is also unlikely that the phenomenon develops at both ends of the HVDC-link at the same time [6, p.40]. The factors in the CIGRE HVDC benchmark model that have an influence on developing of core saturation instability on the rectifier side will now be analysed. Then the results of a test simulation are presented. In this simulation a relatively large 50 Hz disturbance is superimposed on the fire angle of the rectifier.

Characteristic properties of the CIGRE HVDC benchmark model

Section 3.5.1 states that an HVDC rectifier system that is vulnerable to core saturation instability is likely to have the following impedance profiles:

- A low and predominantly capacitive DC side impedance at the fundamental frequency with the presence of a series resonance near to but higher than the fundamental frequency.

- A high and predominantly inductive AC side second harmonic impedance with the presence of a parallel resonance near to but higher than the second harmonic frequency.

- A high AC side resistance near 0 Hz.

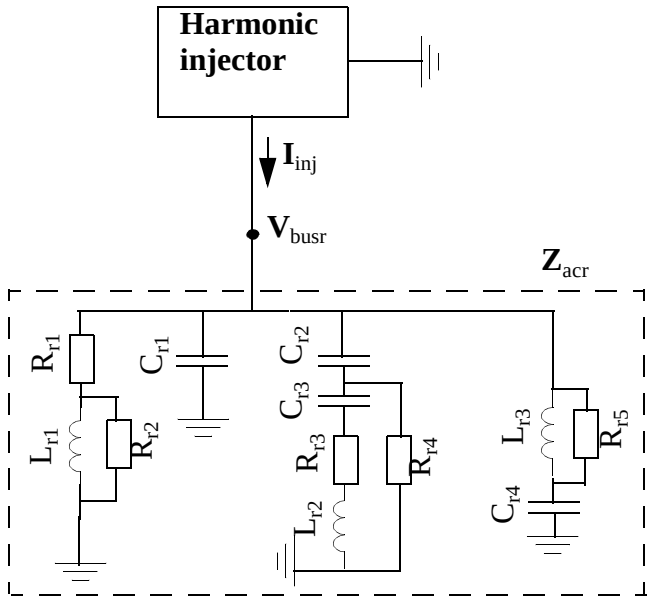
It is seen that a series resonance exists between the smoothing inductor of the rectifier and the capacitance in the DC-link of the CIGRE HVDC benchmark model. The frequency f_0 of this series resonance is found to be:

$$f_0 = \frac{1}{2\pi\sqrt{L_{dc1} \cdot C_{dc}}} \approx 40.4 \text{ Hz} \tag{6.1}$$

For frequencies above f_0 the DC side impedance will be predominantly inductive. This means that the DC side impedance of the rectifier is not typical for an HVDC rectifier system that is vulnerable to core saturation instability.

The AC side resistance of the rectifier at 0 Hz is 3.737 Ω this is relatively high and increases the probability for core saturation instability.

To find the AC side impedance of the rectifier Z_{acr} as a function of frequency a frequency scan was performed. A harmonic current source injected currents with the integer frequencies from 1-200 Hz into Z_{acr}. The response in the voltage V_{busr} across Z_{acr} was measured and this way Z_{acr} for frequencies from 1-200 Hz could be found from Ohm's law. The principle of finding Z_{acr} as a function of frequency is shown in Figure 6.4.



The harmonic injector injects currents at integer frequencies in the range from 1-200 Hz with equal magnitude.

The AC side impedance of the rectifier,Z_{acr} ,is found at each frequency from Ohm's law. This way the impedance profile of Z_{acr} for frequencies from 1-200 Hz can be found.

Figure 6.4 Frequency scanning method used to find the AC side impedance Z_{acr}.

Z_{acr} was found by using the setup in Figure 6.4 for a simulation in PSCAD/EMTDC version 3. Figure 6.5 presents the magnitude of Z_{acr} as a function of frequency and the phase of Z_{acr} is shown in Figure 6.6.

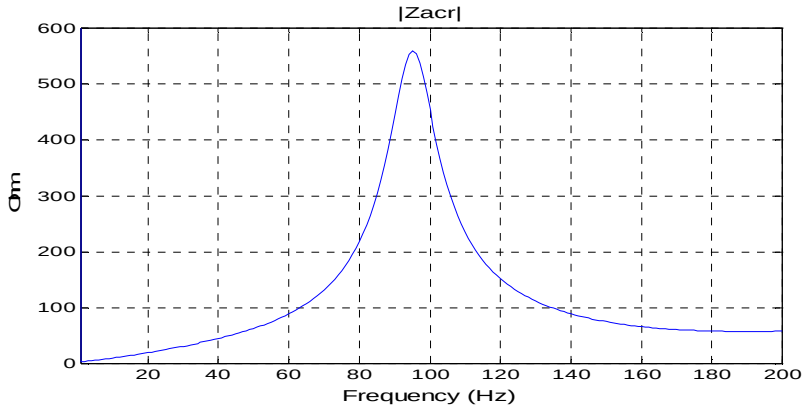


Figure 6.5 The magnitude of the AC side impedance of the rectifier Z_{acr} as a function of frequency

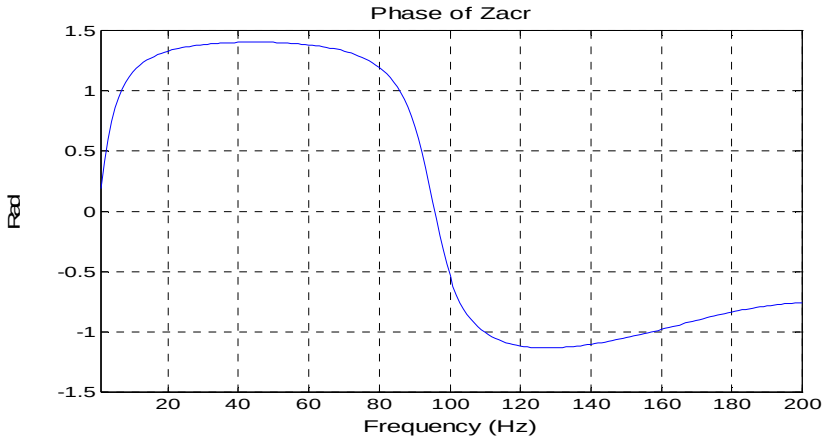


Figure 6.6 The phase of the AC side impedance of the rectifier Z_{acr} as a function of frequency

From Figure 6.5 and 6.6 it is seen that Z_{acr} is capacitive at the second harmonic frequency and that a parallel resonance is present for a frequency slightly lower than 100 Hz (closer investigation shows that the resonance frequency is 95 Hz). Therefore, Z_{acr} is not representing an impedance that is likely to make the rectifier side of the HVDC-link vulnerable to core saturation instability.

As a conclusion it can be said that the impedance profiles in the CIGRE HVDC benchmark model do not make the rectifier side of the HVDC-link vulnerable to core saturation instability.

The magnetizing characteristics of the converter transformers are also essential for the development of core saturation instability. The higher the knee-voltage, the less chance there is to saturate the transformer, and the higher the air core reactance, the less will the peak of the magnetizing current be when the transformer is saturated. The knee-voltage of transformers will typically be in the range from 1.15 to 1.25 pu [25]. In the CIGRE HVDC benchmark model the knee voltage of the rectifier converter transformers is 1.22 pu. Thus, the knee-voltage can still be decreased by 0.07 pu and still be inside the typical range for knee-voltage in transformers. The leakage reactance of the rectifier converter transformers is 0.18 pu. According to [25] the air core reactance can in many cases be considered as about twice the size of the leakage reactance [25]. High voltage converter transformers may have a leakage reactance down to 0.1 pu. Therefore it is also possible to use a significantly lower air core reactance in the converter transformers on the rectifier side in the CIGRE HVDC benchmark model and still have a realistic magnetizing curve. Figure 6.7 shows the magnetizing curve of the rectifier side converter transformers. This curve was found by simulation in PSCAD/EMTDC.

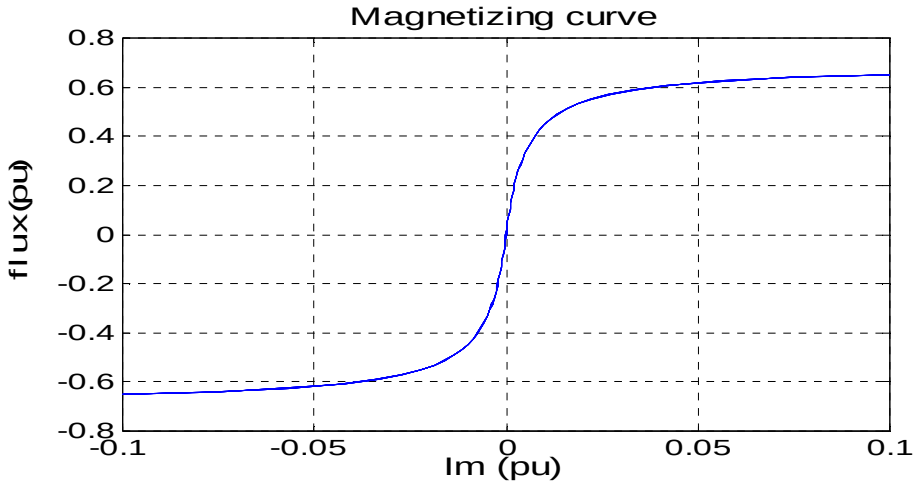


Figure 6.7 The magnetizing curve of the converter transformers on the rectifier side. Im is the magnetizing current in pu.

In Chapter 3 it was stated that core saturation instability rarely develops without the contribution of the HVDC control system. It is the interaction on the rectifier side that is relevant for the development of the phenomenon in this study. Therefore it is sufficient to consider the CC-control system of the rectifier which is shown in Figure 6.2. The magnitude and phase of the transfer function H_{ccr} between I_{dcr} and α_r is shown in Figure 6.8.

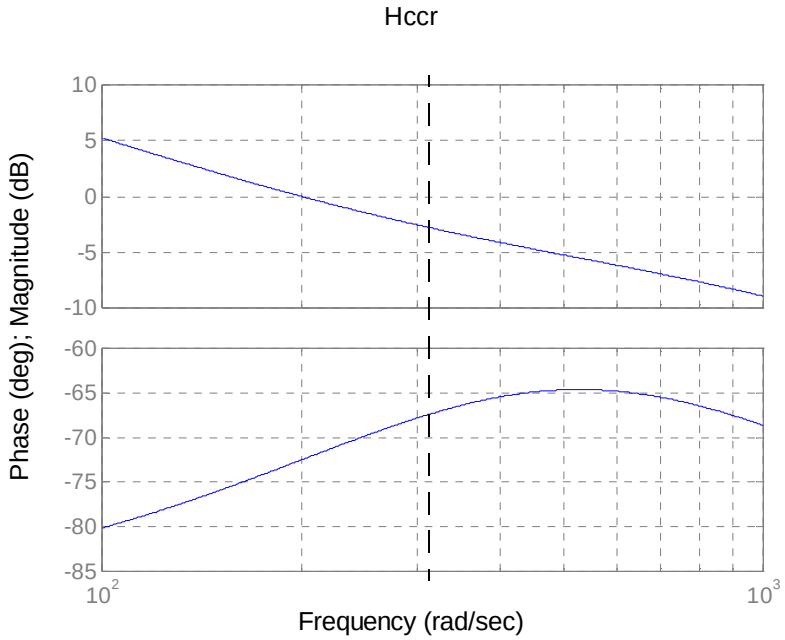


Figure 6.8 Magnitude and phase of H_{ccr} (the transfer function between I_{dcr} and α_r)

The gain of H_{ccr} at 50 Hz is approximately -2.8 dB and the phase of H_{ccr} at 50 Hz is approximately -67.3^0. Increasing the gain of H_{ccr} at 50 Hz will cause 50 Hz variations in the DC side current I_{dcr} to give higher 50 Hz variations in the rectifier fire angle α_r. However, this will not necessarily increase the probability for core saturation instability to occur. The reason is that

the 50 Hz variation in the voltage V_{dcr} on the DC side of the rectifier is not only influenced by the control system but also by the interaction between harmonics on the AC and DC sides of the rectifier. Therefore, the phase of the 50 Hz component in V_{dcr} which is generated by the control system will also be essential for developing of core saturation instability.

Results from the simulated case

After analysing the factors that influence core saturation instability at the rectifier side in the CIGRE HVDC benchmark model it became clear that the system can still be made significantly more vulnerable for the phenomenon. Actually, the system did not have typical characteristics for developing core saturation instability. The simulation described below verified this:

The time step used in the simulations was 10 μs and the plot step was 100 μs. The HVDC-link was initially runned at steady-state near its rated operating point, i.e. the power transfer in the HVDC-link was 1.0 pu (1000 MW). At the steady-state operating point the phase voltages on the rectifier bus were approximately 286 kV(peak). After 2 seconds with the HVDC-link in steady state operation a 50 Hz, 1.75^0 sinusoidal variation was superimposed on the fire angle order of the rectifier. This disturbance was present for 0.5 seconds and then completely removed. The response in the DC side current I_{dcr} of the rectifier side is shown in Figure 6.9 and the 50 Hz component I_{dcr50} of I_{dcr} is shown in Figure 6.10. The fundamental and second harmonic components in the currents of the neutral conductors of the converter transformers are found in appendix 1. If core saturation instability was developing I_{dcr} is expected to have growing 50 Hz oscillations because of the disturbance in the fire angle order of the rectifier. It is seen that I_{dcr} becomes normal again and that I_{dcr50} goes to zero after the disturbance is removed. The results in Appendix 2 shows that the fundamental and second harmonic components of the zero-sequence currents also remain small. This shows that core saturation instability is not developed in this case.

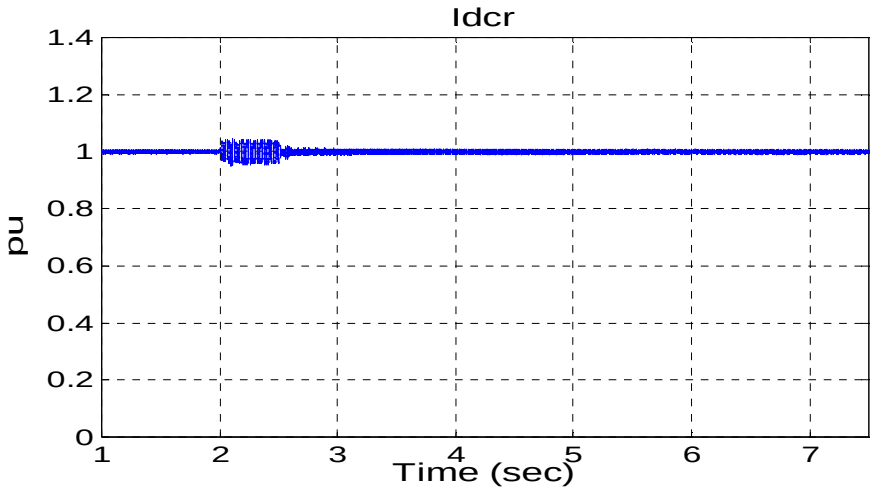


Figure 6.9 I_{dcr}

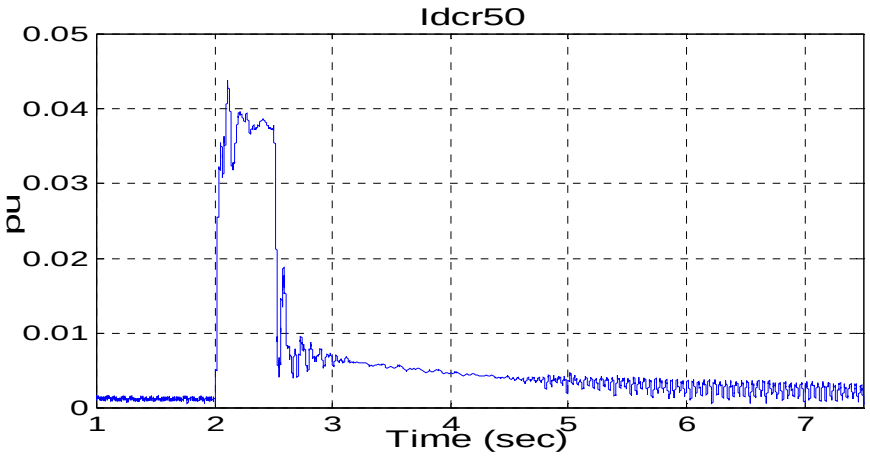


Figure 6.10 I_{dcr50}

6.2 The modified CIGRE HVDC benchmark model

With the CIGRE HVDC benchmark model, core saturation instability was not obtained when applying a relatively large 50 Hz disturbance on the fire angle order of the rectifier. In this section some modifications are made to the CIGRE HVDC benchmark model. With these modifications core saturation instability is developed for the same operation state and disturbance as in Section 6.1.4. This proves that the modified model is much more vulnerable to developing core saturation instability. To modify the impedance profile of the CIGRE HVDC benchmark model in such a way that a worse case is obtained with respect to core saturation instability, a frequency scanning method in [32] is useful. This method was not used this thesis. The modifications made on the CIGRE HVDC benchmark model that are described in this section simply causes an impedance profile of the HVDC rectifier system that according to Section 3.5.1 is likely to be vulnerable for core saturation instability. In addition the magnetizing curves of the rectifier transformers are changed in such a way that these transformers easier will enter deep saturation.

6.2.1 Characteristics of the CIGRE HVDC benchmark model and simulation results

The following modifications were made to the CIGRE HVDC benchmark model to obtain a model that was more vulnerable to core saturation instability (these modifications are based on [6]) :

- The DC side resistances were changed from 2.5 Ω to 1.25 Ω.
- The DC side inductances were changed from 0.5968 H to 0.25 H.
- The DC side capacitance was changed from 26 μF to 38 μF.
- The compensating capacitors on the AC side of the rectifier were reduced from 3.342 μF to 0.6684 μF.

- The leakage reactances in the converter transformers on the rectifier side were reduces from 0.18 pu to 0.12 pu.

- The knee-point voltage of the converter transformers on the rectifier side were reduced from 1.22 pu to 1.15 pu.

- The air core reactances of the converter transformers on the rectifier side were reduced from 0.36 pu to 0.25 pu.

The changes in the DC side impedance changed the frequency f_0 of the series resonance on the DC side. It now became:

$$f_0 = \frac{1}{2\pi\sqrt{L_{dc1} \cdot C_{dc}}} \approx 51.6 \text{ Hz} \tag{6.2}$$

This is as described in the section 6.1.4 increasing the vulnerability to core saturation instability on the rectifier side of the HVDC link.

The AC side resistance of the rectifier at 0 Hz is unchanged, but has, as mentioned earlier, a relatively high value and thus contributes significantly to the development of core saturation instability.

The changes in the compensating capacitors on the AC side of the rectifier gave new impedance characteristics for Z_{acr}. These are shown in Figures 6.11 and 6.12.

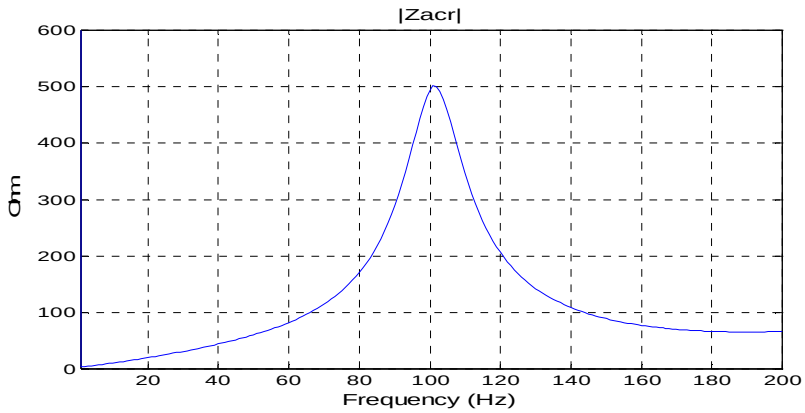


Figure 6.11 The magnitude of the AC side impedance of the rectifier Z_{acr} as a function of frequency

URN:NBN:no-2111

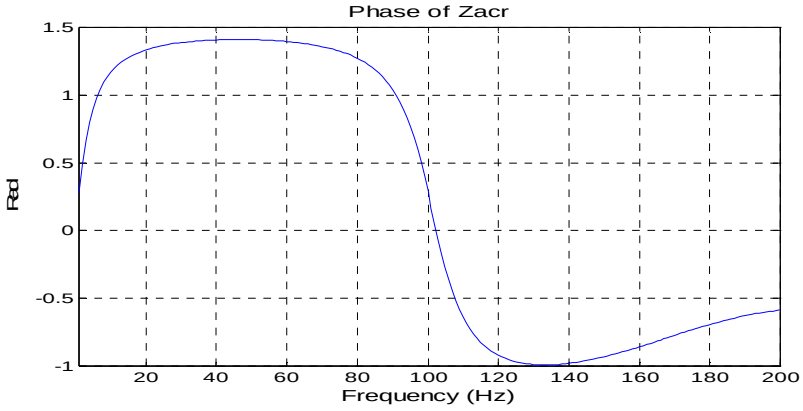


Figure 6.12 The phase of the AC side impedance of the rectifier Z_{acr} as a function of frequency

Figures 6.11 and 6.12 show that Z_{acr} now has a parallel resonance that is just above 100 Hz. This is typical for a rectifier system that is vulnerable to development of core saturation instability. When comparing Z_{acr} in the CIGRE HVDC benchmark model and the modified CIGRE HVDC benchmark model it is clear that the phase and magnitude of Z_{acr} are roughly the same in both models with the exception of frequencies between 70 Hz and 140 Hz. Thus the system response remains practically unchanged at other frequencies than those in the vicinity of 100 Hz.

The conclusion now is that the impedance profiles of the modified CIGRE HVDC benchmark are typical for the development of core saturation instability on the rectifier side.

As mentioned in the beginning of this section parameters in the rectifier transformers were changed to obtain a model that was more sensitive to core saturation instability. The magnetizing curve of the rectifier side transformers in the modified CIGRE HVDC benchmark model is in Figure 6.13 shown together with the magnetizing curve of the rectifier side transformers in the CIGRE HVDC benchmark model.

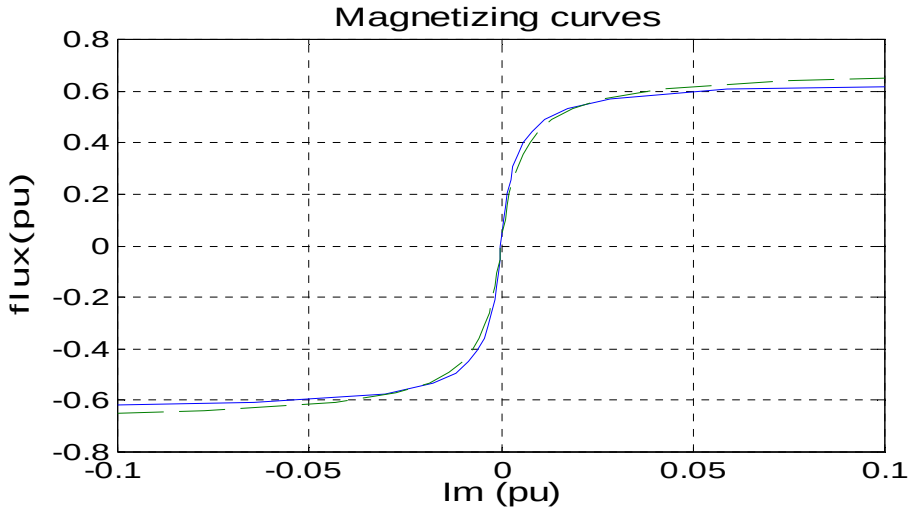


Figure 6.13 The magnetizing curve of the converter transformers on the rectifier side. Im is the magnetizing current in pu. The dashed curve is the magnetizing curve of the rectifier side transformers in the CIGRE HVDC benchmark model. The solid curve is the magnetizing curve of the modified CIGRE HVDC benchmark model.

URN:NBN:no-2111

The magnetizing curves in Figure 6.13 indicates that if an overvoltage is applied on the terminals of the rectifier transformers, the transformers in the modified CIGRE HVDC benchmark model will be more saturated than the transformers in the CIGRE HVDC benchmark model. In addition, a DC component in I_m is likely to cause the rectifier transformers in the modified CIGRE HVDC benchmark model to be significantly more saturated than the rectifier transformers in the CIGRE HVDC benchmark model. Thus, compared to the rectifier transformers in the CIGRE HVDC benchmark model, the rectifier transformers in the modified CIGRE HVDC benchmark model will increase the probability for core saturation instability in an HVDC system.

The control system used in the modified benchmark model is the same as used in the CIGRE HVDC benchmark model.

The same steady-state situation and the same disturbance in the fire angle order for the rectifier bridge as in the simulation with the CIGRE HVDC benchmark model in Section 6.1.4 was simulated with the modified CIGRE HVDC benchmark model. The voltage source on the rectifier was adjusted to obtain equal phase voltages on the commutation bus of the rectifier as in the simulation of the CIGRE HVDC benchmark model i.e. that the line-to-line voltages at the voltage source was adjusted to 393 kV (rms). The DC side current I_{dcr} of rectifier and its 50 Hz component I_{dcr50} is shown in Figures 6.14 and 6.15, respectively. It is observed that core saturation instability now develop. The HVDC-link would of course been disconnected during the build up of the instability. It is expected that harmonic currents in the neutral conductor of the rectifier side converter transformers would have caused the disconnection. The Kristiansand converter station in the Skagerrak HVDC link will be disconnected if the 50 Hz content of the current in the neutral conductor is larger than 25 A or if the 100 Hz content of the current in the same conductor is larger than 78 A [27]. Appendix 3 shows the 50 Hz component of the current I_{0yyr50} in the neutral conductor of the Y-Y coupled converter transformer on the rectifier side. It is clear that the core saturation instability in this case would have caused a quicker disconnection of the HVDC link. In other cases core saturation instability develops slowly or just to a certain degree. This may not cause disconnection because of too large currents in the neutral conductors of the transformers, but heating due to the non-characteristic harmonics that are generated because of the skew magnetized converter transformers may cause disconnections.

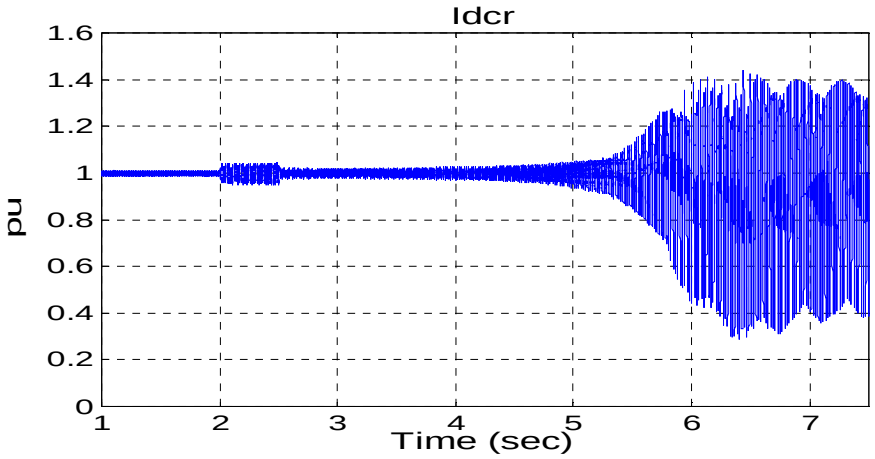


Figure 6.14 I_{dcr}.

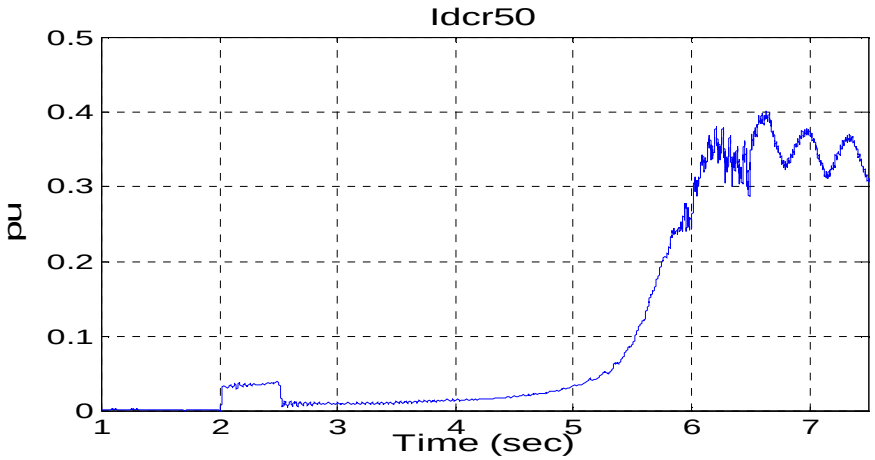


Figure 6.15 I_{dcr50}.

7 Simulation of methods that prevent core saturation instability

In this chapter different initiatives that prevents core saturation instability are tested on the modified CIGRE HVDC benchmark model described in Chapter 6. These initiatives are shown theoretically in Chapter 4. The use of converter transformers with a low magnetizing impedance and the use of CCC converters are not tested since these are methods that must be considered during the design of the HVDC link. The method described in Section 4.6 has been examined thoroughly in [33]. Thus, this method is not tested in this thesis.

Even though the methods are only demonstrated for one disturbance under one operating condition i.e. I_{dcr}=1.0 pu, most of them seem to be valid for the same disturbance or similar disturbances (disturbances where α_{ref} has a different phase angle) at all operating conditions i.e. when I_{dcr} is between 0.4 pu and 1.0 pu. Some additional tuning must be performed on the stabilizing loops that are demonstrated in Sections 7.3.2-7.3.4, since they will only operate satisfactory when I_{dcr} is between about 0.6 pu to 1.0 pu. The reason for this is probably that the phase angles of these loops are considerable different than the phase angle of the tuned stabilizing loop in Section 7.3.1. An alternative to tune the loops described in Sections 7.3.2-7.3.4 is to design additional loops that are active in the cases when I_{dcr} is between 0.4 pu and 0.6 pu. With the method described in [34] the loops in Sections 7.3.3-7.3.4 can be improved by placing PI controllers on the output of the Butterworth filters. With this strategy the stabilizing loops may not need to be tuned in order to operate satisfactory when I_{dcr} is between 0.4 pu and 0.6 pu. Since the tuning problem with the stabilizing loops in Sections 7.3.2-7.3.4 was not focused on before late in the work with this thesis, it has not been enough time to tune them or to go into other methods that would improve them.

7.1 A passive filter on the AC side of the rectifier

As described in Chapter 4, a way to decrease the probability for core saturation is to use a low impedance branch for currents near the second harmonic at the commutation bus of the converter side which is vulnerable to development of the phenomenon. In this case it will be the rectifier side. Despite its drawbacks due to cost and possible undesirable resonances in the AC grid it is a very efficient method to stop core saturation instability. With such a filter inserted into the AC side of the rectifier, the one-line diagram of the AC side impedance becomes as in Figure 7.1.

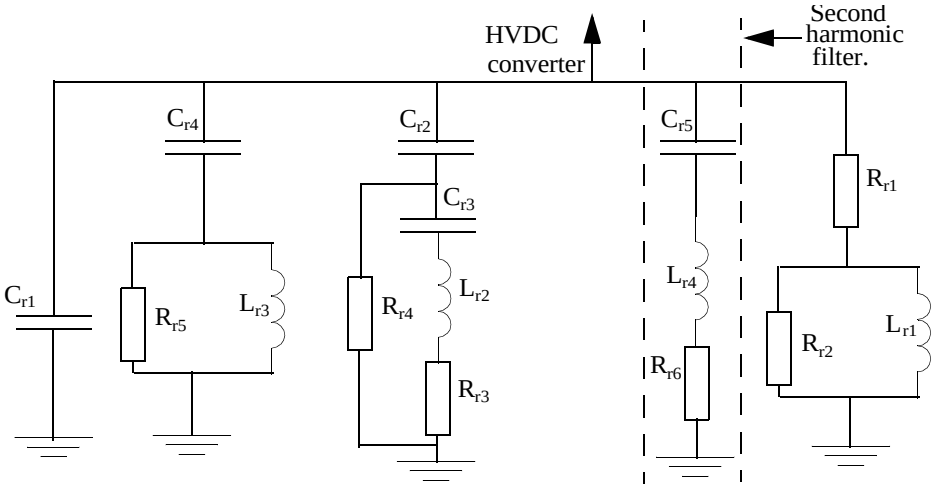


Figure 7.1 The AC side impedance of the rectifier, including a second harmonic filter.

Table 7.1 The values of the components in the second harmonic filter in Figure 2.1.

C_{r5} (μF)	L_{r4} (H)	R_{r6} (Ω)
2.5330	1.0	62.8319

The AC side impedance of the rectifier when second harmonic filter is included has the characteristics as shown in Figures 7.2 and 7.3.

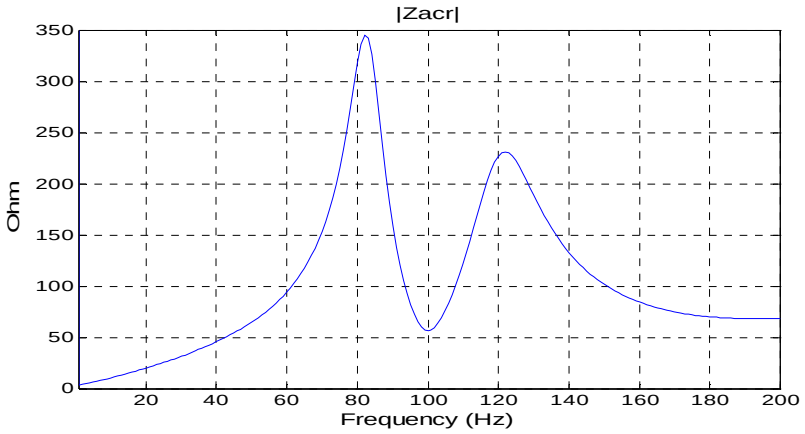


Figure 7.2 The magnitude of the AC side impedance of the rectifier, Z_{acr}, as a function of frequency when the second harmonic filter is included.

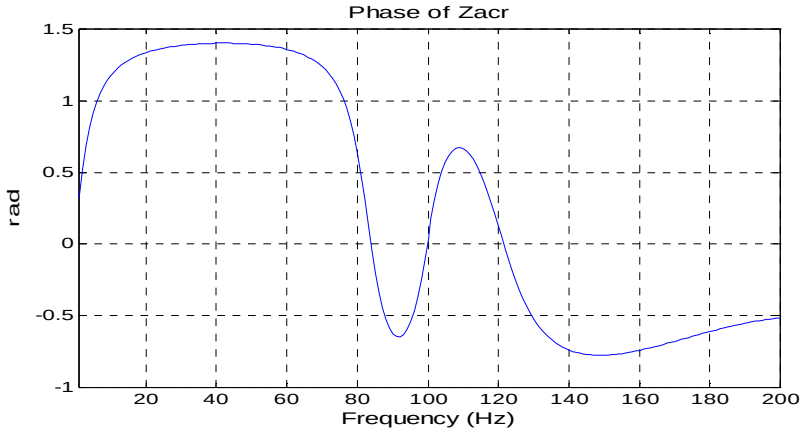


Figure 7.3 The phase of the AC side impedance of the rectifier, Z_{acr}, as a function of frequency when the second harmonic filter is included.

From Figure 7.2 it is seen that the parallel resonance near 100 Hz has disappeared because of the second harmonic filter. Comparing Figures 7.2 and 7.3 with Figure 6.11 and 6.12 also shows that the impedance from 0 to 60 Hz and 150 Hz and up is nearly unchanged despite the inclusion of the second harmonic filter. However, the second harmonic filter generates two parallel resonances. These appear, respectively just above 80 Hz and just above 120 Hz. It is unlikely that significant harmonics at these frequencies would appear in the power system. Nevertheless, it should be kept in mind that in a different coupling situation in the AC grid the second harmonic filter may cause a resonance at an undesirable frequency. This is always a risk when using passive filters, and therefore the use of passive filters should be limited as much as possible.

In the modified CIGRE HVDC benchmark model described in Chapter 6, the AC side impedance was substituted with the AC side impedance in Figure 7.1. Then the same operating situation and the same disturbance which developed core saturation instability on the model in Chapter 6 was simulated. The results of this simulation are shown in Figure 7.4-7.5 and Appendix 4. From these results it is concluded that the second harmonic filter prevents development of core saturation instability.

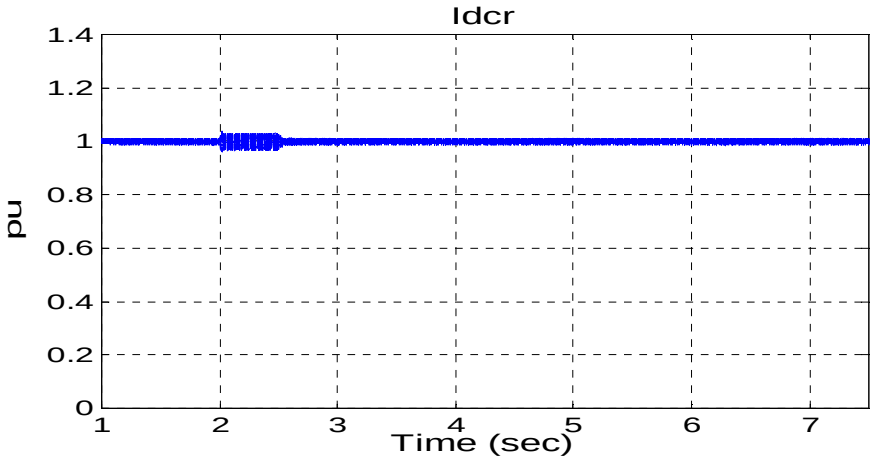


Figure 7.4 I_{dcr}

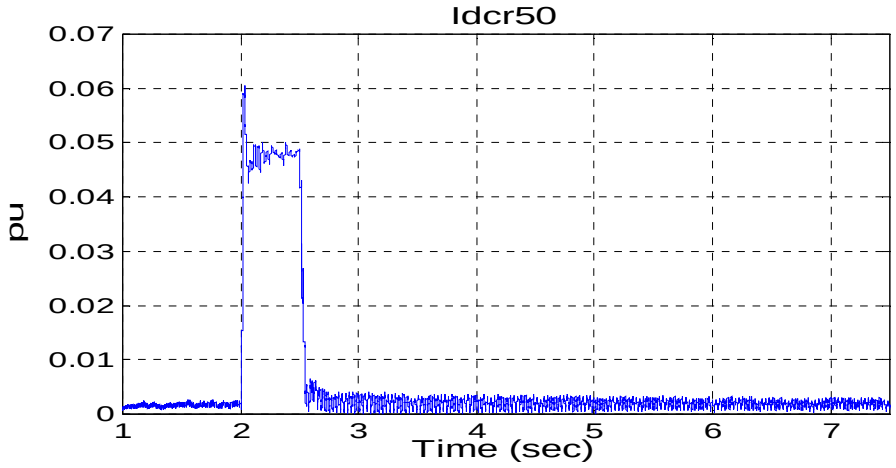


Figure 7.5 I_{dcr50}

7.2 A hybrid shunt filter on the AC side of the rectifier

As stated in Chapter 4 a hybrid shunt filter has the advantage compared to the passive filters that it does not generate any parallel resonanses in the AC grid. However it is more costly since many additional components must be used. In this section it is demonstrated how a hybrid filter can be used to compensate for second harmonic components in the load currents of the rectifier in the modified CIGRE HVDC benchmark model described in Chapter 6. By using the hybrid filter in this manner, the development of core saturation instability is avoided. It is emphasized that it is the principle of using the hybrid filter for avoiding core saturation instability that is focused on in this section. Therefore some simplifications are made. In real life a PWM-converter of the size of the one used in the hybrid filter described in this section would may have required several IBGTs in parallel and/or series to build up one switch, but in this section each switch in the PWM-converter is only built up by one IGBT. Actions in the control system of the hybrid filter to protect it during faults or overcurrents are not modelled since they are not necessary to include in order to show how the hybrid filter can be used to compensate for the second harmonic component in the load current. A simplified circuit diagram of the AC side of the rectifier including the hybrid filter is shown in Figure 7.6.

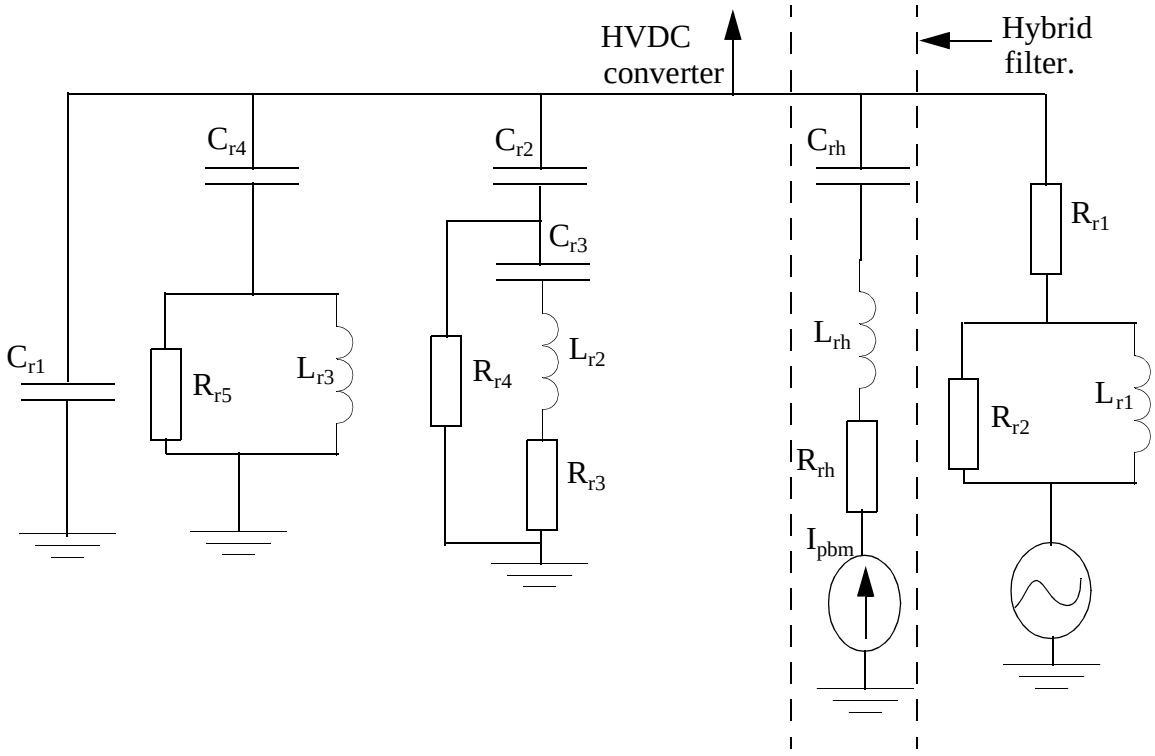


Figure 7.6 Simplified circuit diagram of the AC side impedance of the rectifier, including hybrid filter.

The full circuit diagram of the hybrid filter is shown in Figure 7.7.

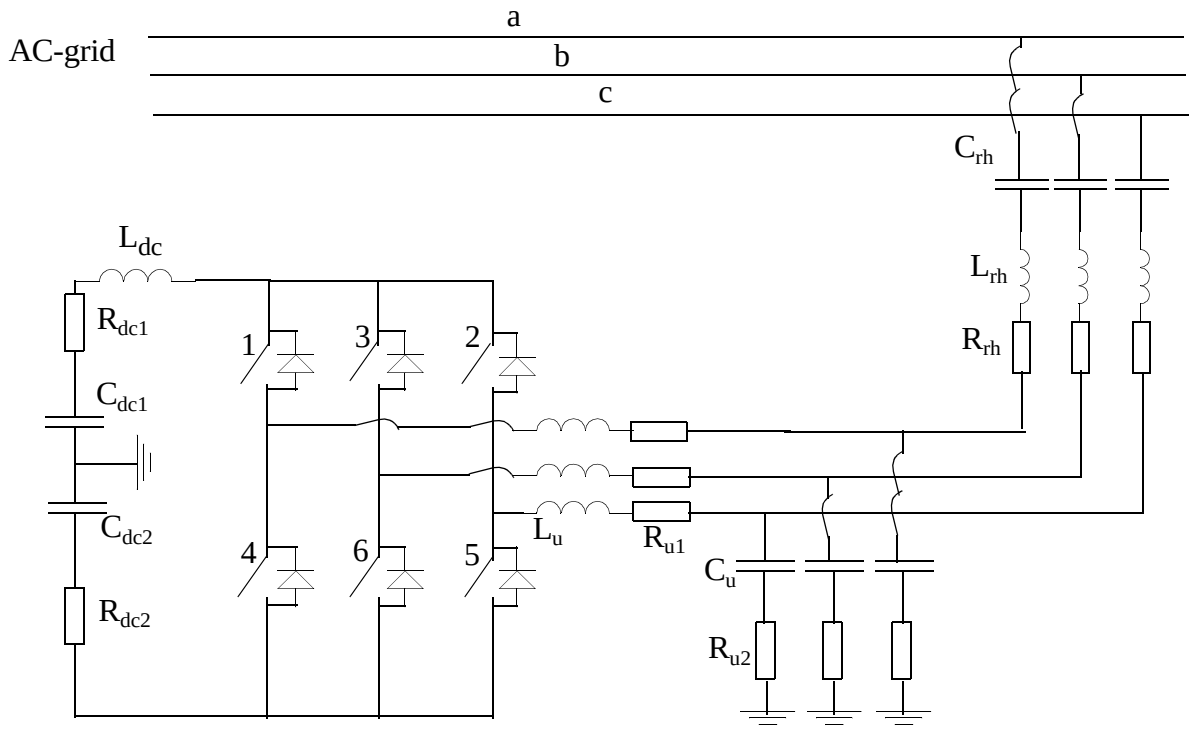


Figure 7.7 Full circuit diagram of the hybrid filter.

The values of the R, L, and C components in Figure 7.7 are shown in Table 7.2-7.4.

Table 7.2 The values of the resistances in Figure 2.7

R_{u1} (Ω)	R_{u2} (Ω)	R_{dc1} (Ω)	R_{dc2} (Ω)	R_{rh} (Ω)
0.02	10	0.01	0.01	61.9319

Table 7.3 The values of the inductances in Figure 2.7

L_{rh} (H)	L_u (H)	L_{dc} (H)
1.1	3.44e-3	1.0e-5

Table 7.4 The values of the capacitances in Figure 2.7

C_{rh} (μF)	C_{dc1} (μF)	C_{dc2} (μF)	C_u (μF)
2.30275	1000	1000	81

The switches in Figure 7.7 are modelled as IGBT transistors. Free-wheel diodes are coupled in anti-parallel with the IGBTs to make it possible for the phase currents to flow both in and out

of the converter. Table 7.5 shows the data for the IGBT switches, and Table 7.6 presents the data for the free-wheel diodes are shown.

Table 7.5 Data for the IGBT switches

On resistance	0.01 Ω
Off resistance	1 MΩ
Forward voltage drop	0.0 kV
Forward breakover voltage	100 MV
Reverse withstand voltage	100 MV
Minimum extinction time	0.0 seconds
Snubber resistance	5000 Ω
Snubber capacitance	0.05 μF

Table 7.6 Data for the free-wheel diodes

On resistance	0.01 Ω
Off resistance	1 MΩ
Forward voltage drop	0.001 kV
Forward breakover voltage	100 MV
Reverse withstand voltage	100 MV
Minimum extinction time	0.0 seconds
Snubber resistance	5000 Ω
Snubber capacitance	0.05 μF

The control system of the hybrid filter is such that it generates a current order for each phase that will ideally provide the second harmonic component of the load current, cause the fundamental harmonic voltage across the terminals of the transformer in the hybrid filter to be near zero, and make sure that the DC side voltage of the PWM-converter stays at its desired value. This current order is compared with the current the hybrid filter injects into the AC grid and the controller causes the difference between these to vanish. Figure 7.8 shows how the current order in one of the phases of the hybrid filter is generated.

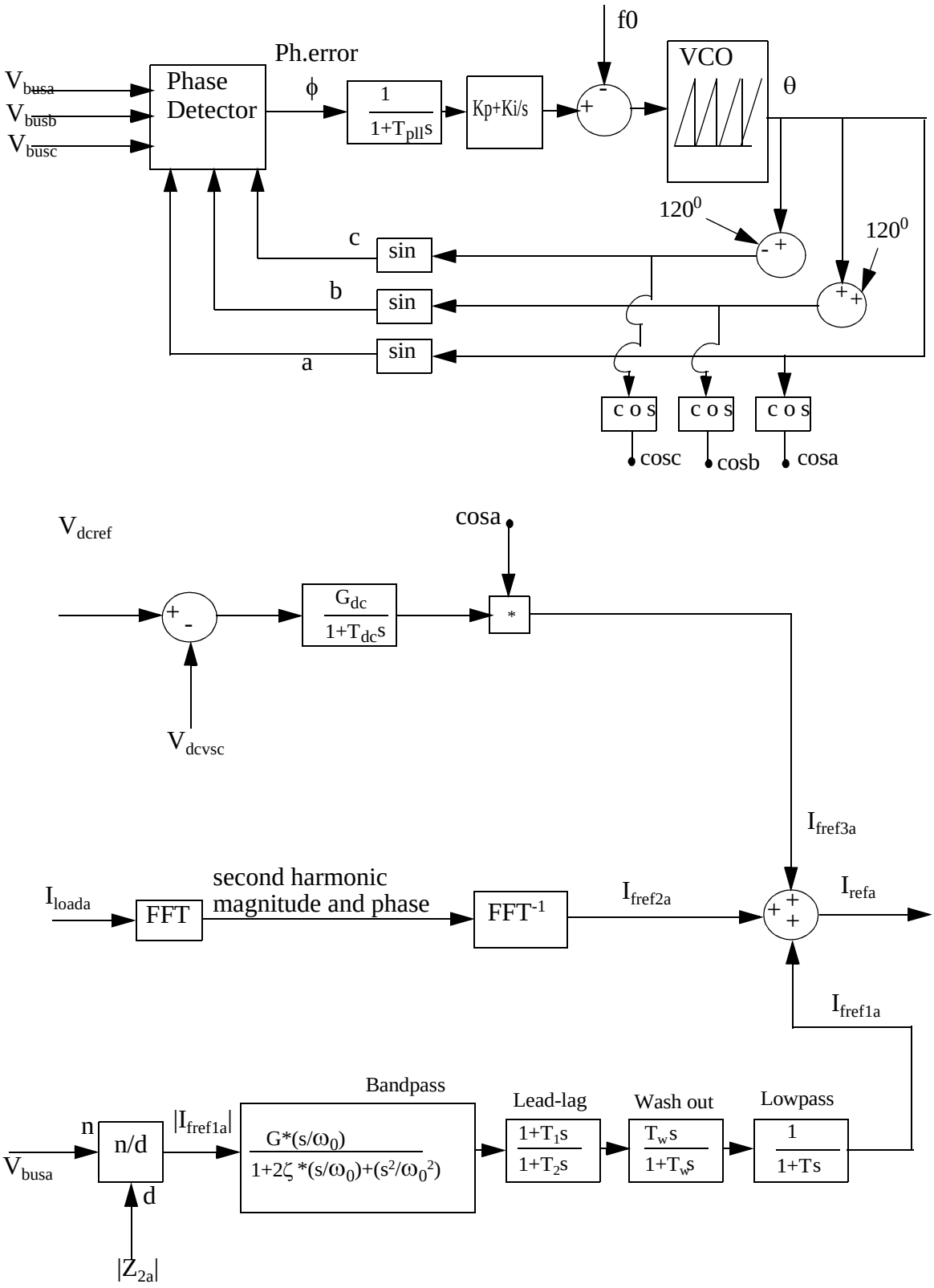


Figure 7.8 Block diagram for generation of the current order in one of the phases of the hybrid filter.

V_{busa} is the measured phase voltage across the hybrid filter in the phase a.
V_{busb} is the measured phase voltage across the hybrid filter in the phase b.
V_{busc} is the measured phase voltage across the hybrid filter in the phase c.

V_{dcref} is the voltage order on the DC side of the PWM converter.
V_{dcvsc} is the measured voltage on the DC side of the PWM converter.
θ is the phase angle of V_{busa}.
f0 is the base frequency of the voltages across the hybrid filter.
cosa is the cosine to the phase angle of V_{busa}.
$|Z_{2a}|$ is absolute value at 50 Hz of the passive impedance consisting of C_{rh}, L_{rh}, and R_{rh} (see Figure 7.7).
I_{loada} is the measured load current for the HVDC converter in the phase a.
I_{fref3a} is the order for the current needed to keep the DC side voltage of the PWM-converter at its ordered value.
I_{fref2a} is the order for the second harmonic component of the current in phase a of the hybrid filter.
I_{fref1a} is the order for the fundamental harmonic component of the current in phase a of the hybrid filter.
I_{refa} is the current order for the hybrid filter in phase a.

Table 7.7 Values to the parameters on Figure 2.8

w0(rad/s)	ζ	G	T_1(ms)	T_2(s)	T_w(μs)	T(s)
314.1593	0.004	17595	2.12	0.033	10	2
$\|Z_{2a}\|(\Omega)$	G_{dc}	T_{dc}(ms)	Kp	Ki	f0 (Hz)	T_{pll}(ms)
1424.845	8.165	1	10	0.02	50	1

The measured load current I_{loada} is passed through a Fast Fourier Transform (FFT) block which returns the phase and magnitude of the second harmonic component of I_{loada}. These components are then passed through the inverse FFT and I_{fref2a} which is the approximate time varying second harmonic in I_{loada} is obtained. This current order enables the hybrid filter to compensate for the second harmonic load current of the HVDC converter in phase a. In this way the second harmonic load current for the HVDC converter in phase a experiences a low impedance. The same control strategy is used for phase b and c, this way the probability of core saturation instability is considerably decreased.

To obtain as low VA-rating on the hybrid filter as possible it is desirable to generate a current in each phase that causes the fundamental harmonic voltage across the output of the PWM converter in the hybrid filter to be zero in all phases. This can roughly be achieved by the configuration used on Figure 7.8. V_{busa} is divided with $|Z_{2a}|$. This will give the absolute value of the current needed to give zero fundamental harmonic voltage across the PWM converter. Since Z_{2a} is roughly capacitive $|I_{fref1a}|$ needs to be phase shifted by almost -90 degrees. This is obtained by the transfer function $H_1(s)$ between $|I_{fref1a}|$ and I_{fref1a} on Figure 1.30. $H_1(s)$ cause the right phase shift at 50 Hz and at the same time they cause all other harmonics in V_{busa} to be suppressed. The impulse response of $H_1(s)$ is shown in Figure 7.9.

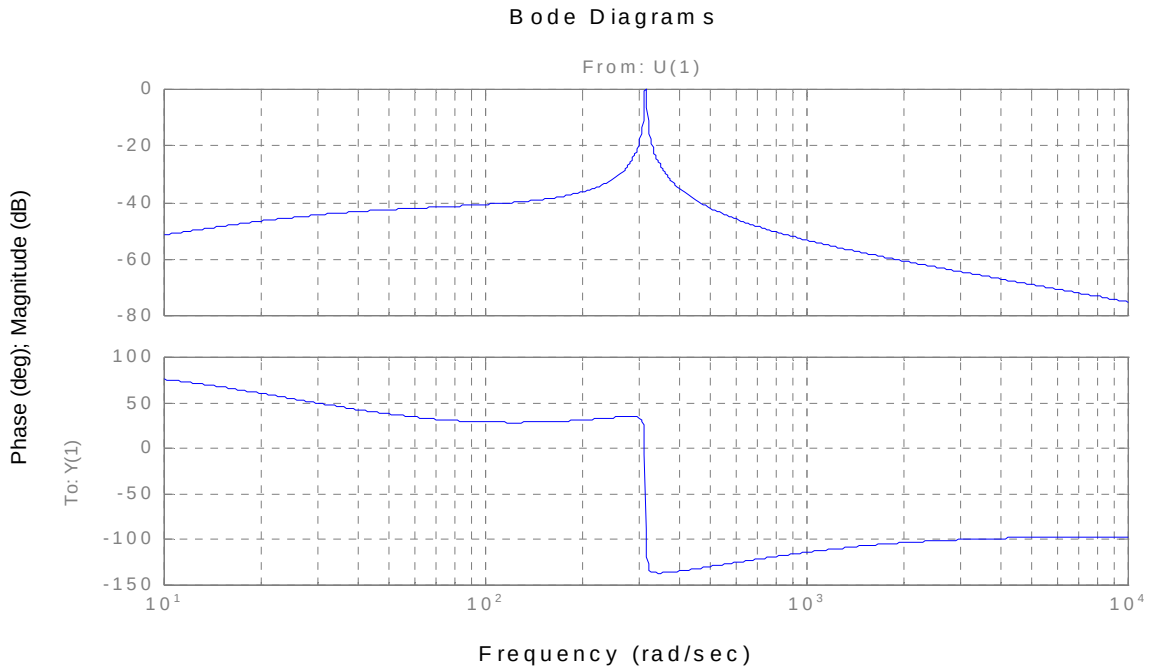


Figure 7.9 The impulse response of $H_1(s)$.

To keep the voltage V_{dcvsc} constant, the PWM converter needs a current component that causes active power to flow from the AC side to the DC side when V_{dcvsc} is less than V_{dcref} and active power to flow from the DC side to the AC side when V_{dcvsc} is larger than V_{dcref}. At 50 Hz the hybrid filter is approximately a capacitance seen from the commutation busbar of the HVDC-converter. The small fundamental voltage that is present across the hybrid filter is approximately 90^0 out of phase with the busbar voltage. Thus, the hybrid filter must generate currents which are 90^0 out of phase with the commutation voltages in each phase in order to exchange active power with the AC grid. To obtain this the phase of each commutation voltage are found by the phase-locked loop in Figure 7.8. These phase angles are shifted 90 degrees and multiplied with the output of the controllers that have the difference between V_{dcvsc} and V_{dcref} as input signal. In this way currents orders for each phase are generated in order to keep V_{dcvsc} constant. In phase a this current order is called I_{fref3a}.

Finally I_{fref1a}, I_{fref2a} and I_{fref3a} are added together and the total current order I_{frefa} for the hybrid filter in phase a is generated. The current orders in phases b and c are generated the same way.

Further on the currents the hybrid filter injects into the AC grid are subtracted from the current orders of the hybrid filters. The differences between these are passed through the controllers of the hybrid filter. The outputs of the controllers are continuously compared with a triangular signal, and the results of these comparisons decide which switches in the hybrid filters are in on state and off states. Figure 7.10 shows the scheme for generating the switching signals in phase a. The same method is used for phases b and c.

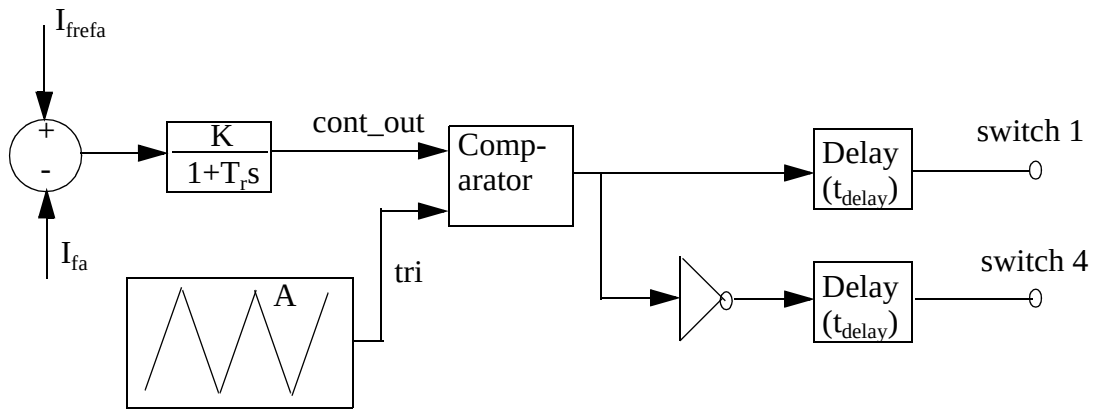


Figure 7.10 Control system for firing of the switches that influence the current in phase a of the hybrid filter.

tri is the output of the triangular signal generator and varies between -5 and 5.
f_{sw} is the frequency of tri.
cont_out is the output of the controller.
K is the gain of the controller.
T_r is a time constant which decides the bandwidth of the controller.
t_{delay} is the turn on delay time of the switches.
A is the amplitude of the triangular signal.

When cont_out is larger than tri the output of the comparator is one. In the opposite case and when outreg equals tri the output of the comparator is zero.

Table 7.8 Values to parameters connected to Figure 1.32

A	K	T_r(μs)	f_{sw}(Hz)	t_{delay}(μs)
5	1	100	1500	5

The hybrid filter was inserted into the modified CIGRE HVDC benchmark described in Chapter 6. The same disturbance and operating condition that caused core saturation instability on the modified CIGRE HVDC benchmark model in Chapter 6 was then simulated. From Figures 7.11 and 7.12 it is seen that core saturation instability was prevented. More simulation results are found in Appendix 5.

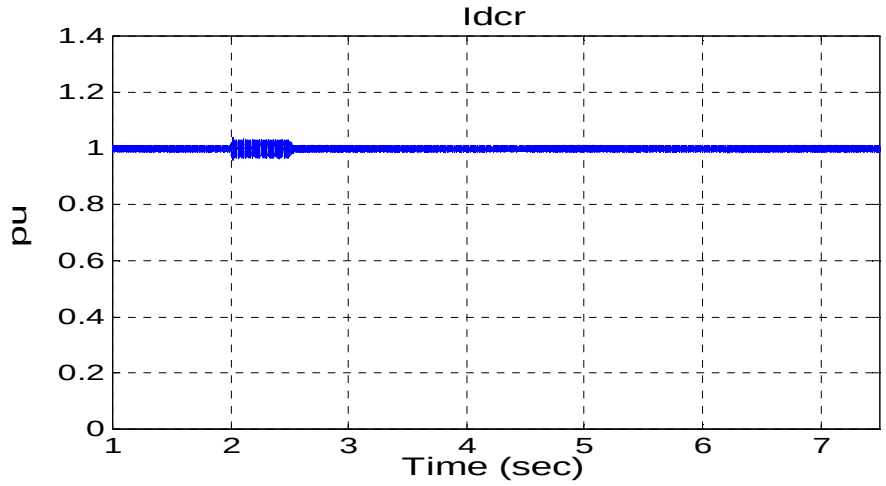


Figure 7.11 I_{dcr}.

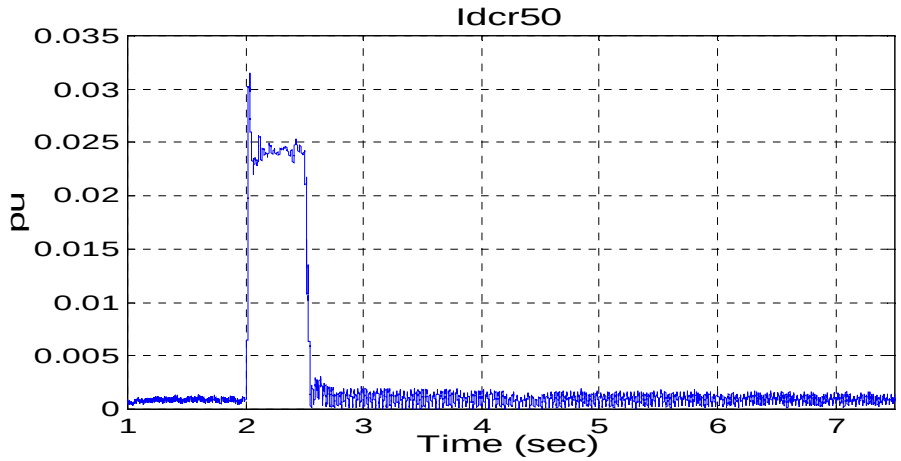


Figure 7.12 I_{dcr50}.

The simulation also showed that the hybrid filter compensated for most of the second harmonic components in the load current drawn by the HVDC link on the rectifier side. As an example of this there is performed an analysis of the current I_{fa} injected by the hybrid filter into the AC grid in phase a together with the load current I_{La} drawn by the HVDC-link in phase a on the rectifier side and the current I_a delivered to the HVDC-link from the AC grid on the rectifier side (see Figure 7.13).

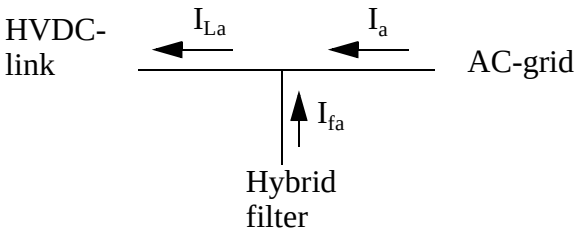


Figure 7.13 Currents involved in analysing the effect of the hybrid filter.

In the time between 2.1 seconds and 2.3 seconds of the simulation time I_{fa}, I_{La}, and I_a were measured. Based on these measurements the frequency spectrum of these currents were found. The reason for choosing the time interval between 2.1 seconds and 2.3 seconds is that the load

currents are expected to have a relative high second harmonic component in this time interval and therefore it is easier to see the effect of the hybrid filter. Table 7.9 shows the second harmonic components found from the frequency spectrum of I_a, I_{La}, and I_{fa}. It is observed that the hybrid filter is effective and prevents much of the second harmonic component of I_{La} to flow into the AC grid.

Table 7.9 Magnitude and phase of the second harmonic component in I_{La}, I_{fa}, I_a

$\lvert I_{La}\rvert$ (A)	$\angle$ I_{La} (rad)	$\lvert I_{fa}\rvert$ (A)	$\angle$ I_{fa} (rad)	$\lvert I_a\rvert$ (A)	$\angle$ I_a (rad)
30.3512	-2.7422	28.4598	-2.6910	2.4177	2.8937

The VA-rating of the hybrid filter is a very important element when considering using a hybrid filter or not. In the case simulated in this section the VA-rating is reasonably low. In Figure 7.14 the measured voltage on the DC side of the PWM-converter V_{dcvsc} is shown and Figure 7.15 shows the current I_{dcvsc} flowing through L_{dc} in Figure 7.7. The maximum power delivered (the maximum value of the product between V_{dcvsc} and I_{dcvsc}) is in this case less than 1 MW. A VA-rating at 1.5 MVA should be secure in this case.

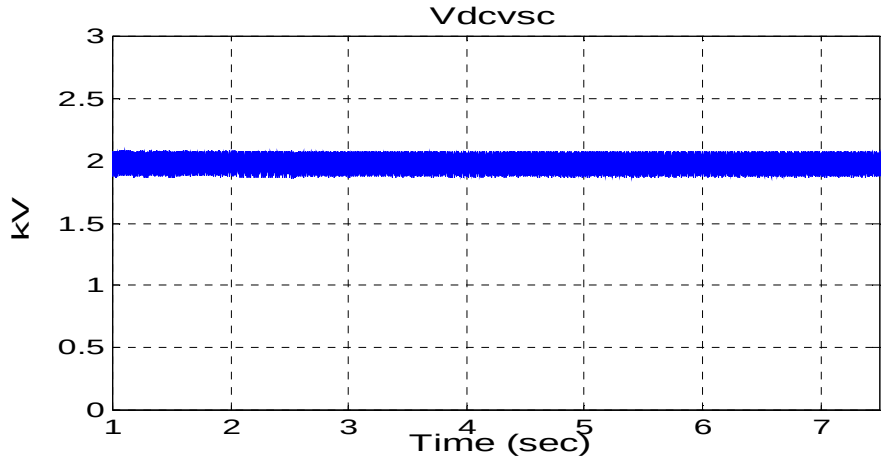


Figure 7.14 V_{dcvsc}.

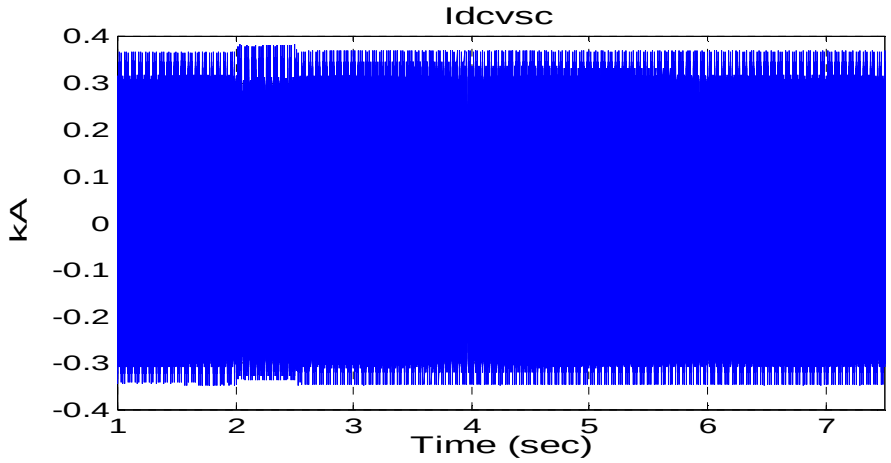


Figure 7.15 I_{dcvsc}.

7.3 Stabilizing feedback loop from the DC side current of the rectifier

As explained in Chapter 4, a stabilizing loop in the control system is an efficient way to stop development of core saturation instability. It is a inexpensive solution and easy to disable or change if it turns out to not function properly in real life. In this section four stabilizing loops from the measured DC side current of the rectifier to the fire angle order of the rectifier are used in the simulations. First in Section 7.3.1, an analog bandpass filter tuned to 50 Hz is used in the stabilizing loop (see Figure 7.16). Secondly in Section 7.3.2, the analog bandpass filter is combined with an FFT function (see Figure 7.20) to obtain a stabilizing loop that compared to the stabilizing loop with only the analog bandpass filter is less influenced by harmonics at other frequencies than in a small band around 50 Hz. This is also the purpose for the stabilizing loops in Sections 7.3.3 and 7.3.4. In Section 7.3.3 the stabilizing loop consists of a filter as shown in Figure 4.4 and in Section 7.3.4 the stabilizing loop consists of a filter as shown in Figure 4.5.

7.3.1 Analog bandpass filter in the stabilizing loop

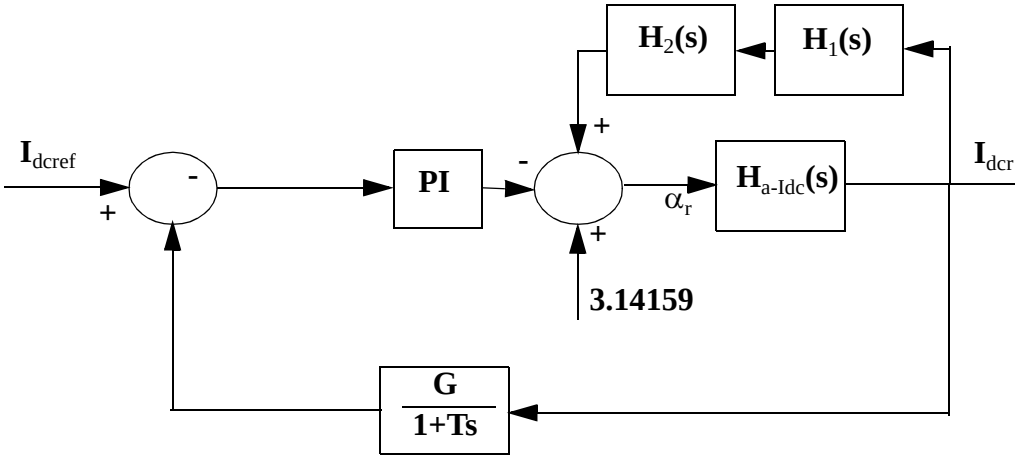


Figure 7.16 A forward loop with an analog bandpass filter in the current control system of the rectifier.

$H_1(s)$ and $H_2(s)$ in Figure 7.16 have the block diagram shown in Figure 7.17.

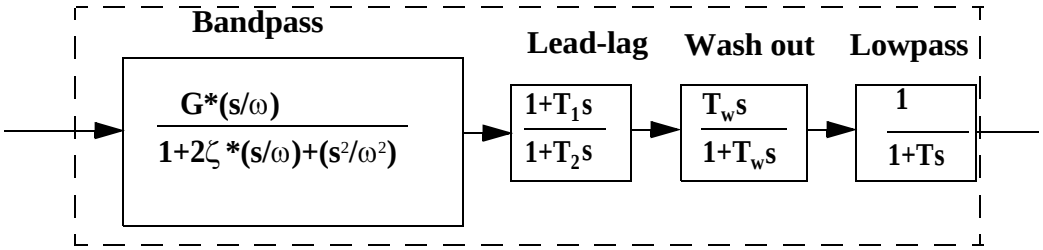


Figure 7.17 Block diagram of the second order bandpass filters in Figure 2.6

The parameters of $H_1(s)$ and $H_2(s)$ in Figure 7.16 are shown in Table 7.10 and 7.11.

Table 7.10 Parameters of $H_1(s)$

G	ζ	T_1 (sec)	T_2 (sec)	T_w (sec)	T (sec)
7	0.05	0.033	0.00395	0.001	2

Table 7.11 Parameters of $H_2(s)$

G	ζ	T_1 (sec)	T_2 (sec)	T_w (sec)	T (sec)
44	0.05	0.033	0.0023	0.001	2

The stabilizing feedback loop in Figure 7.16 was inserted into the modified CIGRE HVDC benchmark model described in Chapter 6. The same disturbance and operating state as in the case where core saturation instability developed in Chapter 6 were then used in a simulation. Results from this simulation are shown in Figures 7.18, 7.19 and Appendix 6. These results shows that the feedback loop prevents core saturation instability.

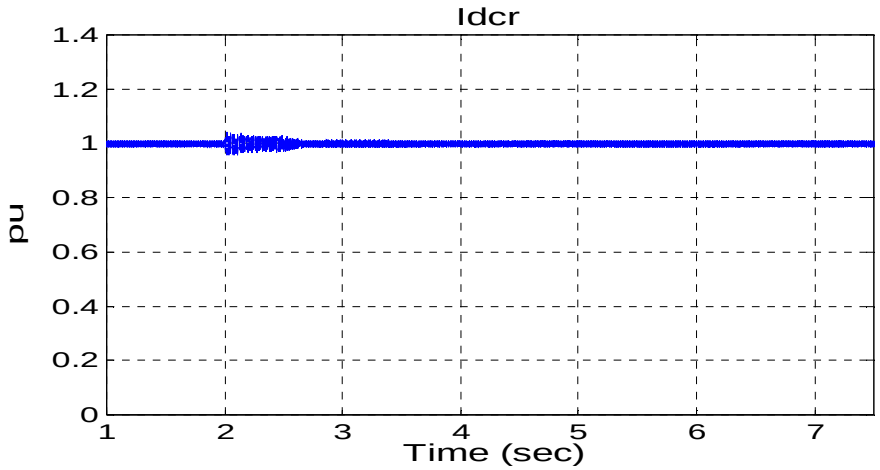


Figure 7.18 I_{dcr}.

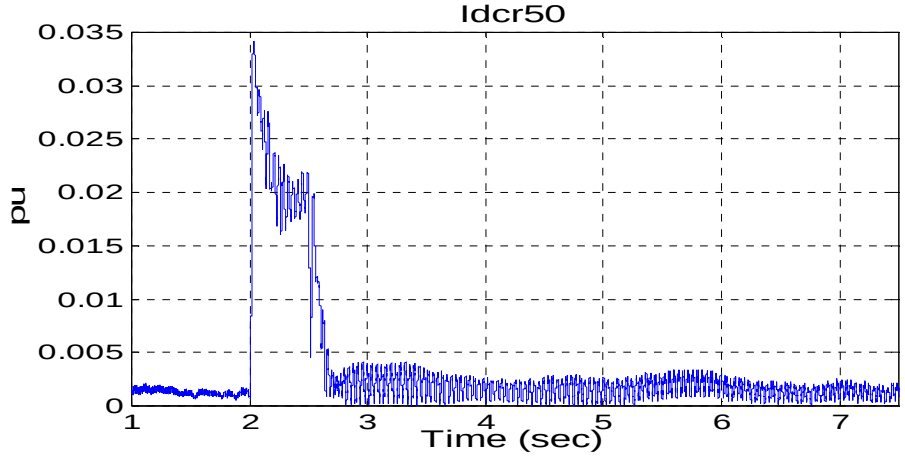


Figure 7.19 I_{dcr50}.

7.3.2 Analog bandpass filter combined with a FFT function in the stabilizing feedback loop

Using an analog bandpass filter in the feedback loop as shown in Figure 7.16 is not without its drawbacks. The most concerning is that it might have a significant influence on the fire angle α_r at undesired frequencies (i.e. the frequencies that are not close to 50 Hz). This might cause the generation of harmonics and in worse case the magnification of harmonics. It is therefore desirable to create a bandpass filter that is sharper than the bandpass filter shown in Figure 7.16. To some degree this can be obtained by using the configuration in Figure 7.20.

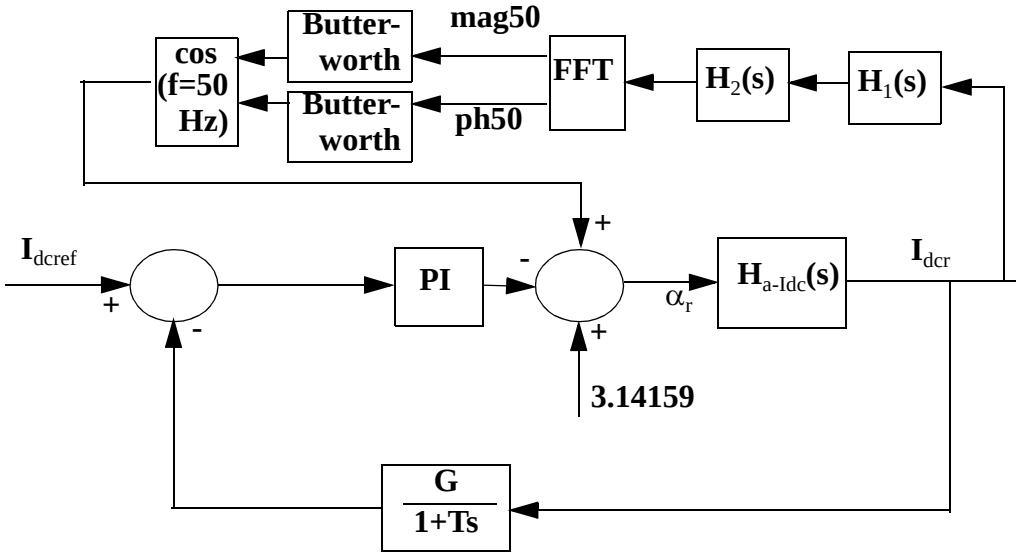


Figure 7.20 A feedback loop from the I_{dcr} to α_r that contains an analog bandpass filter combined with an FFT function.

In Figure 7.20, $H_1(s)$ and $H_2(s)$ are identical with $H_1(s)$ and $H_2(s)$ in Figure 7.16. In Chapter 5 it is described that inter-harmonics in the input signal of the FFT function might cause errors in the calculation of the harmonic components. $H_1(s)$ and $H_2(s)$ cause these errors to significantly decrease. The FFT function has base frequency of 50 Hz and it calculates integer harmonics which are a multiple of 50 Hz up to seven times 50 Hz. The Butterworth filters are lowpass third order with a cutoff frequency 4.0 Hz. If the effect of generating harmonics due to filtering the phase output of the online-frequency scanner (see Example 5.6) is disregarded, the gain and phase of the stabilizing feedback loop becomes like in Figure 7.21 and 7.22 respectively. The gain and the phase for the feedback loop described in Section 7.3.1 are also shown in these Figures. It becomes clear that the FFT function makes the frequency response of the feedback loop sharper. As frequency moves away from 50 Hz the generation of harmonics due to the filtering of the phase output in the FFT function decreases. In Example 5.5 it was seen that the influence on the phase output from a 60 Hz component was small when using an equal Butterworth filter as in this section. Thus, it is seen that the gain of the stabilizing loop at 60 Hz is significantly decreased due to the FTT function and its Butterworth filters. This will also be valid for higher frequencies. The 50 Hz component that is generated due to the 60 Hz input in the FFT function filtering of the phase output will go into a stable loop and decrease with time since the stabilizing loop is tuned to damp out 50 Hz components.

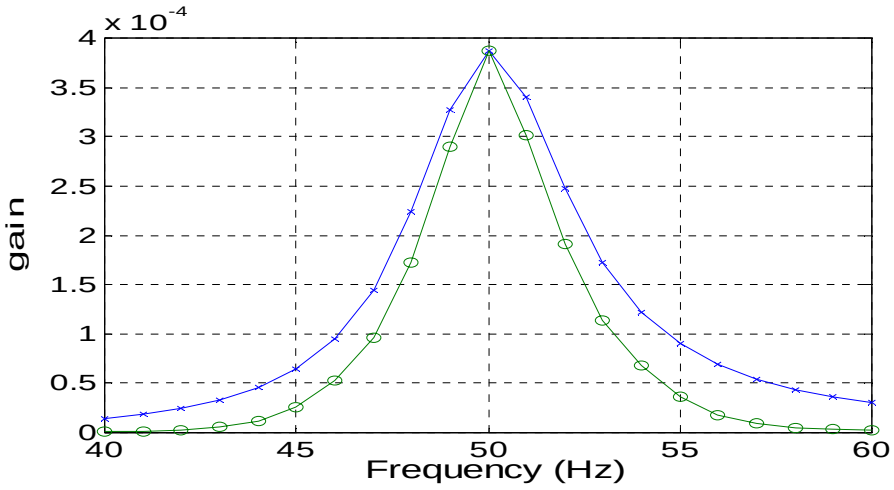


Figure 7.21 The gain of the transfer function in the stabilizing loop.The circled line shows the gain when the FFT function is present and the crossed line shows the gain when the FFT function is absent.

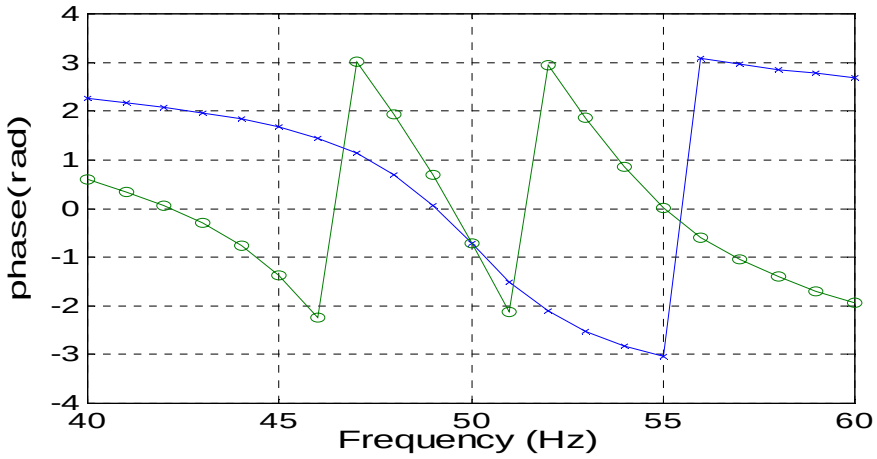


Figure 7.22 The gain of the transfer function in the stabilizing loop.The circled line shows the phase when the FFT function is present and the crossed line shows the phase when the FFT function is absent.

A simulation including the FFT function in the stabilizing loop was performed. The same disturbance and operating state as in the case where core saturation instability developed in Chapter 6 were then used in a simulation. Simulation results are shown in Figures 7.23, 7.24, and Appendix 7. These show that core saturation instability is prevented.

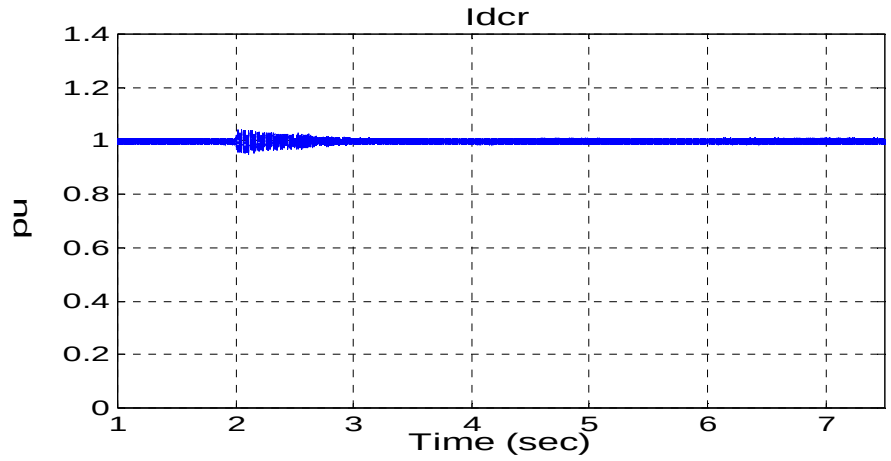


Figure 7.23 I_{dcr}.

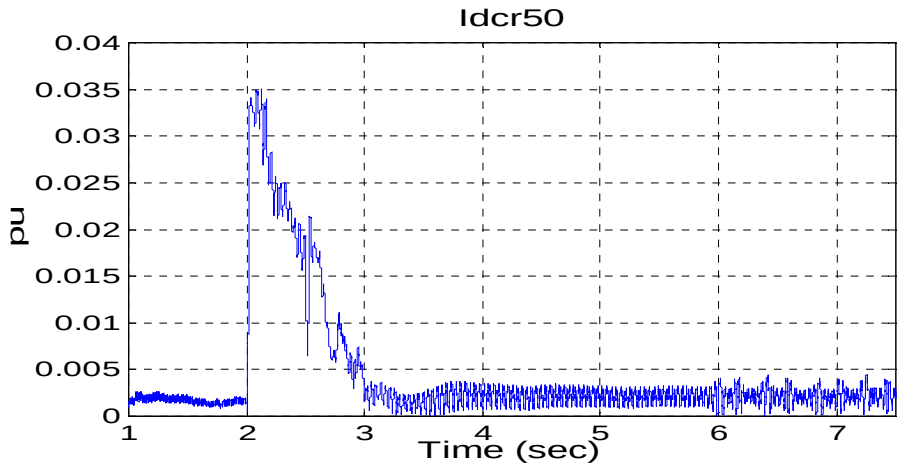


Figure 7.24 I_{dcr50}.

7.3.3 Analog bandpass filter combined with FFT functions and sinusoidal functions in the stabilizing feedback loop

When using the stabilizing loop in Section 7.3.3 there will be a generation of harmonics in the output of the loop if the input contains a frequency component close to 50 Hz. By using the stabilizing loop shown in Figure 7.25 this can be avoided. This loop is explained in Section 4.1. In this section I_{dcr} is chosen as the input to the stabilizing loop. It is also possible to use V_{dcr}, but the principle is still the same.

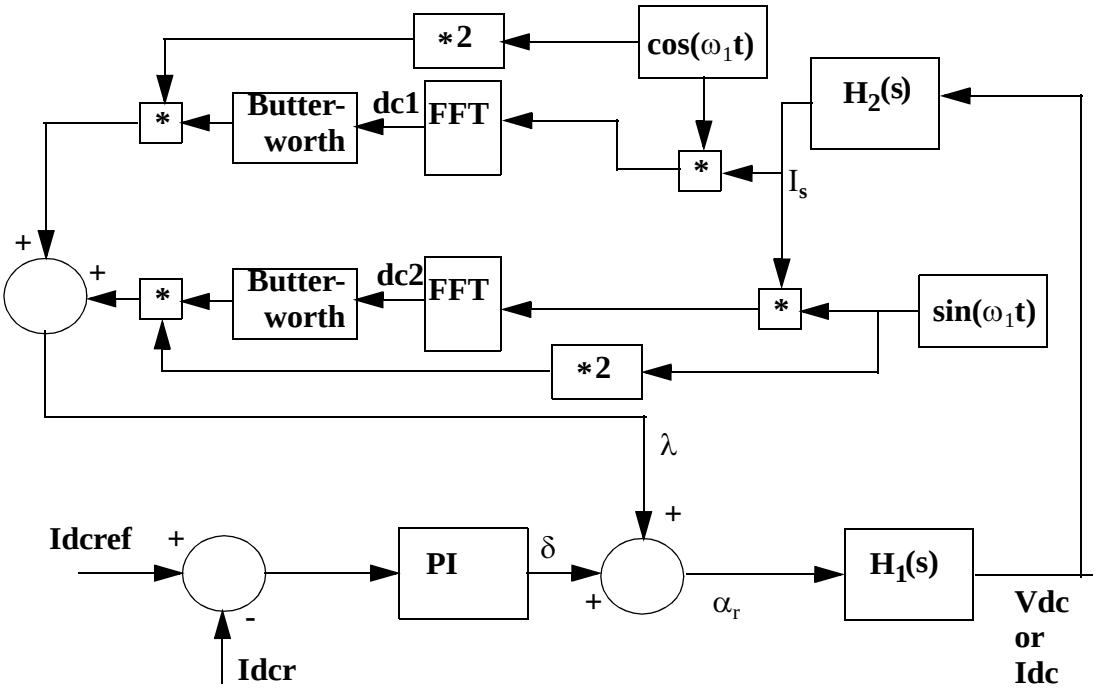


Figure 7.25 A stabilizing loop in the rectifier control system using two FFT functions in combination with an analog filter and sinusoidal functions.

$H_{an}(s)$ is equal to the product of $H_1(s)$ and $H_2(s)$ in Section 7.3.
ω_1 is the fundamental frequency.
dc1 and dc2 are the DC outputs of the FFT blocks.
The Butterworth filters have order 3 and cutoff frequency equal to 3 Hz.

The gain and phase of the stabilizing feedback loop becomes like in Figures 7.26 and 7.27, respectively. The gain and the phase for the feedback loop described in Section 7.3.1 are also shown in these Figures.

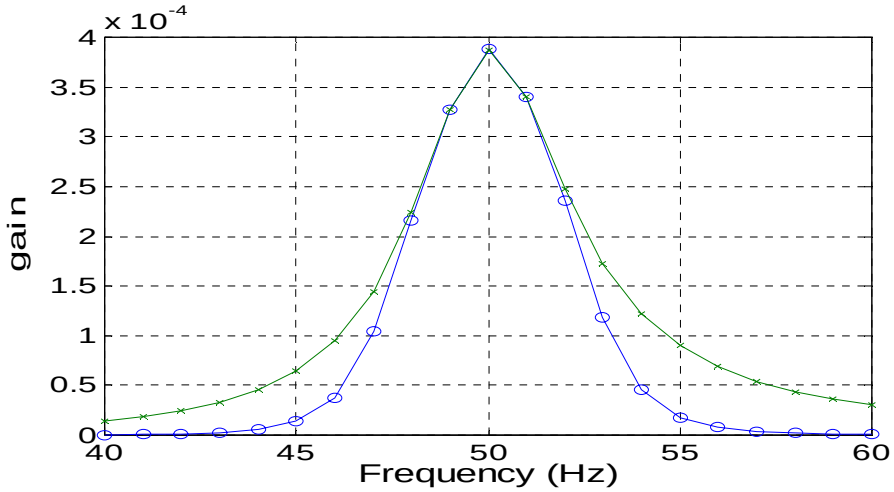


Figure 7.26 The gain of the transfer function in the stabilizing loop.The circled line shows the gain when the loop is as in Figure 7.25 and the crossed line shows the gain of $H_{an}(s)$.

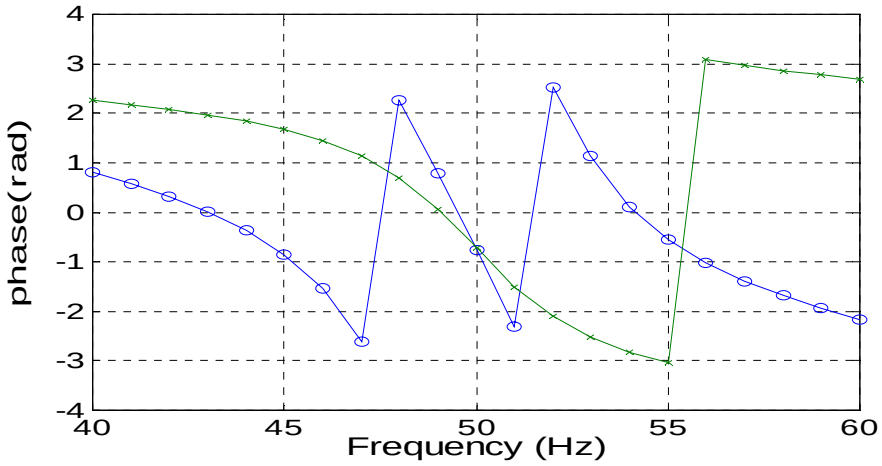


Figure 7.27 The phase of the transfer function in the stabilizing loop.The circled line shows the phase when the is as in Figure 7.25 and the crossed line shows the phase of $H_{an}(s)$.

A simulation was performed with the stabilizing loop described in this section inserted into the modified CIGRE HVDC Benchmark model . The operating state and disturbance was the same as used in the simulations described in Section 6.5. Figures 7.28 and 7.29 shows together with Appendix 8 results of the simulation. They show that the stabilizing loop described in this section is effective in preventing core saturation instability.

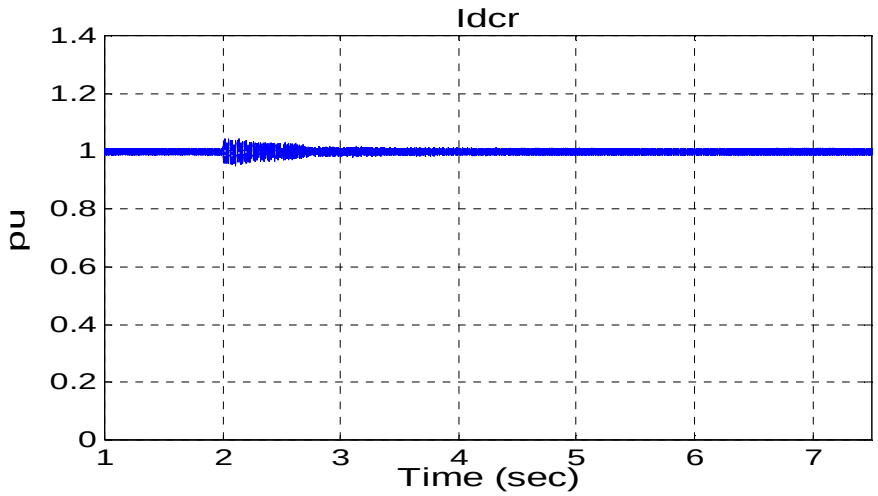


Figure 7.28 I_{dcr}.

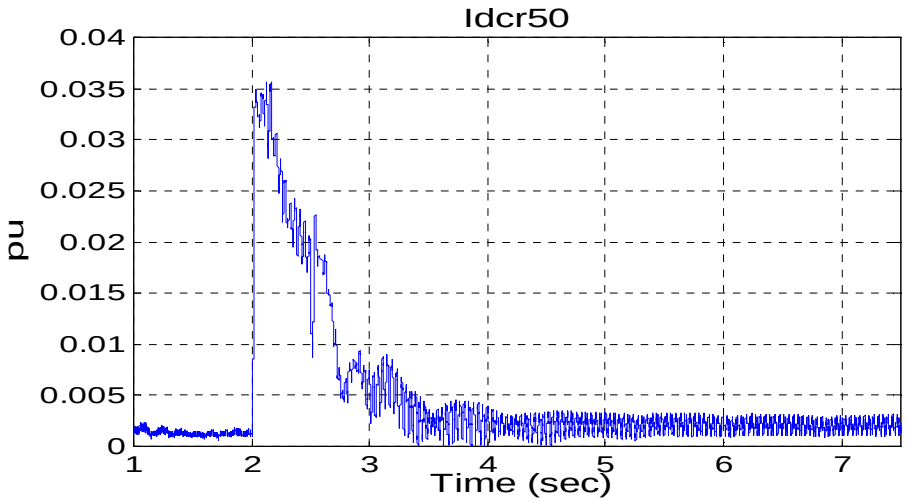


Figure 7.29 I_{dcr50}.

7.3.4 Analog bandpass filter combined with sinusoidal functions in the stabilizing feedback loop

As explained in Section 4.1 the FFT blocks in Figure 7.25 are excessive. In this chapter the same stabilizing loop as in Section 7.3.3 is used, with the exceptions that the FFT functions are removed. This way the block diagram used in the stabilizing loop becomes similar to the one shown in Figure 4.5. The gain and phase of the transfer function of the stabilizing loop used in this chapter are shown in Figure 7.30 and 7.31, respectively. The gain and the phase of the stabilizing loop in Section 7.3.1 are also shown in these Figures.

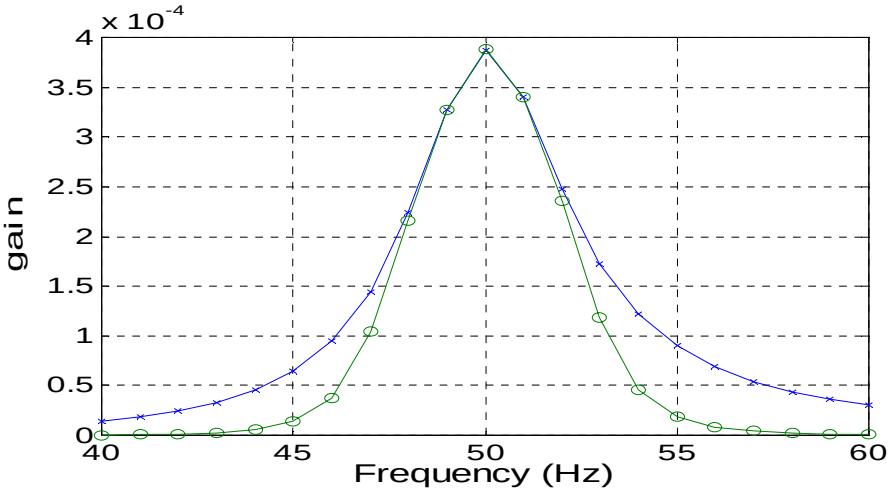


Figure 7.30 The gain of the transfer function in the stabilizing loop.The circled line shows the gain when the loop is as in Figure 4.5 (with $H_2 = H_{an}$ and $H_1 = H_{a\text{-}idc}$) and the crossed line shows the gain of $H_{an}(s)$.

URN:NBN:no-2111

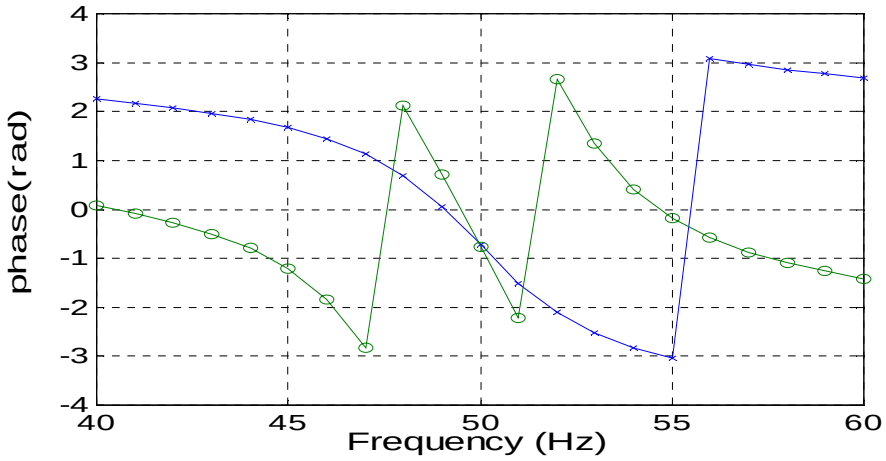


Figure 7.31 The phase of the transfer function in the stabilizing loop.The circled line shows the phase when the loop is as in Figure 4.5 (with $H_2 = H_{an}$ and $H_1 = H_{a\text{-}idc}$) and the crossed line shows the phase of $H_{an}(s)$.

As expected the stabilizing loop described in this section worked well to prevent core saturation instability. The simulation results are shown in Figures 7.32-7.33 and Appendix 9.

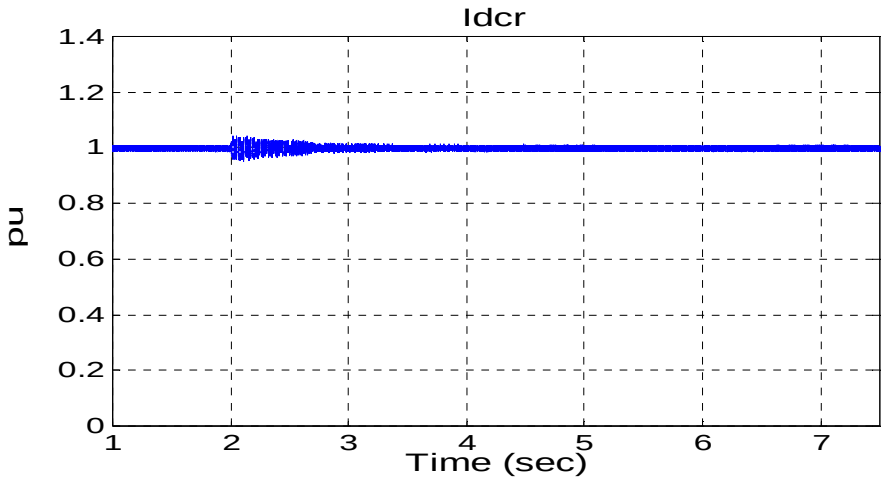


Figure 7.32 I_{dcr}.

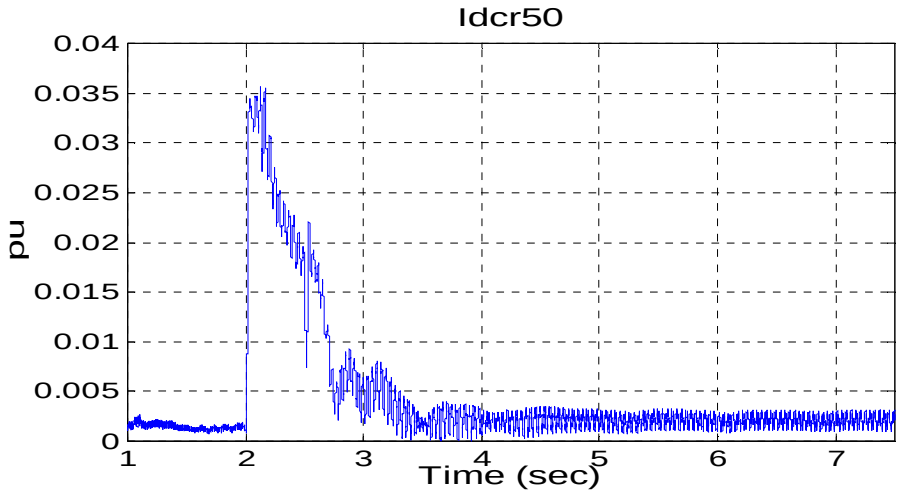


Figure 7.33 I_{dcr50}.

7.4 A blocking LC filter between the low potential converter and earth on the DC side

A blocking LC filter like the one shown in Figure 4.8 was inserted between the low potential converter and earth on the rectifier side in the modified CIGRE HVDC benchmark model from Chapter 6. The LC filter was tuned to 50 Hz and its data is shown in Table 7.14.

Table 7.12 Parameters in the blocking LC filter

R_L (Ω)	R_C (Ω)	L (H)	C (μF)
0.1	0.1	0.5066	20

The same disturbance and operating state as in the case when core saturation instability developed in the modified CIGRE HVDC benchmark model in Chapter 6 were used to demonstrate how effective the blocking LC filter is. The simulation results are shown in Figure 7.33-7.34 and in Appendix 10. They show that the blocking LC filter is a very effective method to prevent core saturation instability.

URN:NBN:no-2111

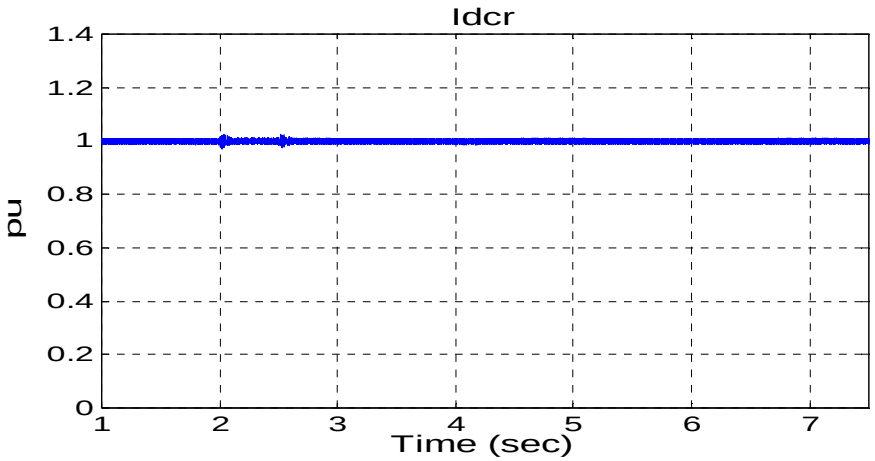


Figure 7.34 I_{dcr}.

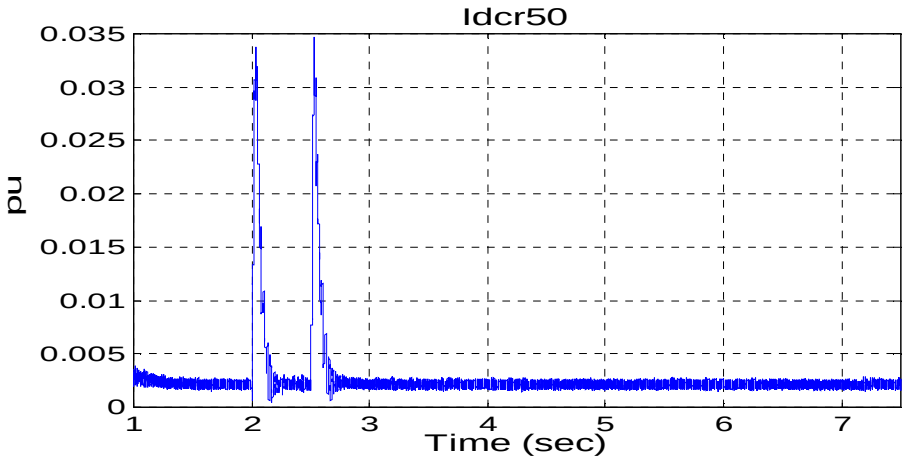


Figure 7.35 I_{dcr50}.

8 Conclusions

Core saturation instability has been successfully simulated on the rectifier side of a modified CIGRE HVDC Benchmark model in PSCAD/EMTDC version 3. The modifications to the original CIGRE HVDC Benchmark model were made to achieve a system that is more vulnerable for developing core saturation instability. The modifications were made on the converter characteristics of the transformers on the rectifier side and the impedances on the AC and DC sides of the rectifier.

The modified CIGRE HVDC Benchmark model where core saturation instability developed were then used as a starting point to demonstrate several initiatives that are preventing the phenomenon. All these demonstrations were done by simulations in PSCAD/EMTDC version 3. The following initiatives were demonstrated:

a) A passive second harmonic filter on the AC side of the converter.

This filter creates a low impedance for currents near the second harmonic at the commutation bus. In this way the second harmonic voltage at the commutation bus becomes low and the damping of core saturation instability is increased. However, it might cause resonances at undesired frequencies when interacting with the AC grid and HVDC link. Component drifting due to agening and temperature might also be a concern. Finally, it is emphazised that the cost of this filter is high.

b) A hybrid shunt filter on the AC side of the converter.

The hybrid shunt filter functions in principle much the same as the second harmonic passive filter. Due to the power electronic components it is however expected to have a higher cost than the passive second harmonic filter. Nevertheless, the hybrid filter does not cause any resonances in the AC network and component drifting are less critical.

c) Stabilizing loops from the measured current on the DC side of the rectifier to the fire angle order of the rectifier.

This is a inexpensive and effective way to stop core saturation instability. However, the stabilizing loop of a pure analog transfer function may have an undesirable influence on the rectifier fire angle at other frequencies than a small band around 50 Hz. By different additional methods such as FFT and/or multiplying a signal in the loop with appropriate sinusoidal functions, this influence can be decreased (see Section 4.1 for the explanation). The simulations showed that both the stabilizing loop with a pure analog transfer function and the stabilizing loops containing additional initiatives effectively prevented core saturation instability. The cases simulated did not show any significant difference between the different stabilizing loop. This is probably because the inter-harmonic components in the DC side current of the rectifier are low. However, some tuning must be performed to optimize the stabilizing loops in Sections 7.3.2-7.3.4. This becomes clear if the current in the DC link is reduced from 1.0 pu to 0.5 pu. A simulation of this is not included in this thesis. This is because it was not paid much attention to the tuning problem before the work with this thesis was in a very late stage.

d) A blocking LC filter between the low voltage potential and earth on the DC side

The LC blocking filter prevents any currents with frequencies in the close vicinity of 50 Hz to flow in the DC link. It has to be rated for the current in the DC link and will be rather costly.

Of the methods mentioned above is, c) is most preferable. It is an inexpensive solution and relatively easy to implement. It is also valuable that the investment risk is low for this solution. In future schemes, active filtering of harmonics on the AC side might be cost effective. Then hybrid filtering might be the preferable one.

Even though it was not the main issue of this thesis, an important finding was how a filter can be made sharper without making it significantly more vulnerable for component drifting. By using Fast Fourier Transform (FFT) and/or multiplications by appropriate sinusoidal signals together with lowpass Butterworth filter this can be achieved.

Using a simulation tool like PSCAD/EMTDC requires care and understanding of the models in the program. As a process in developing the models that were simulated, different components available in PSCAD/EMTDC version 3 were analysed. One of the important conclusions from this was that there are some uncertain factors with the new UMEC transformer model. First of all, the real saturation curve of the UMEC transformer might deviate significantly from the user defined saturation curve. This deviation increases with increasing time step. Secondly, it seems that hysteresis is present in the UMEC model. Even though this may give results that are more in correspondence with real life, this is an undesired uncertainty with the model. The reason is that the UMEC model is said to have no hysteresis effect [19]. The alternative model where the saturation is modelled as a current source in parallel with one of the transformer windings has perviously given satisfactory results in the simulation of core saturation instability [18]. Thus, this model was preferred. It is however important to choose a short time step to get good accuracy.

References

[1] S. Chen, A.R. Wood, J. Arrillaga. A direct frequency domain investigation of the properties of converter transformer core saturation instability. 'AC-DC Power Transmission', 29 April- 3 May, 1996, Conference Publication No. 423, IEE.

[2] J. Arrillaga. HVDC Transmission. The Institution of Electrical Engineers, 1998.

[3] D.A Woodford. HVDC Transmission. Manitoba HVDC Research Centre, 1998.

[4] http://www.abb.com

[5] E. Kreyzig. Advanced Engineering Mathematics, Seventh Edition. John Wiley & Sons. Inc, 1993.

[6] J. Arrillaga, B. Smith. AC-DC Power System Analysis. The Institution of Electrical Engineers, 1998.

[7] K.R. Padiyar. HVDC Power Transmission Systems. Wiley Eastern Limited, New Delhi, 1990.

[8] H. Akagi, H. Fujita. A New Power Line Conditioner for Harmonic Compensation in Power Systems. IEEE Transactions on Power Delivery, Vol 10, No 4, October 1995.

[9] M. Rastogi, N. Mohan, A-A. Edris. Hybrid active filtering of harmonic currents in power systems. IEEE Transactions on Power Delivery, Vol 10, No 4, October 1995.

[10] M. Hernes. Suitability of active and hybrid filters for a 1000 MVA HVDC-system. Technical report from SINTEF Energy Research, Norway, April 1999.

[11] A. Gole. Lecture notes from a course called HVDC Transmission -1 at the University of Manitoba. These notes were earlier available via http://www.ee.umanitoba.ca/~hvdc/ courses.html.

[12] J. Arrillaga et al. Power System Harmonic Analysis. John Wiley & Sons, 1997.

[13] A. Persson, L. Carlsson. New technologies in HVDC converter design. 'AC and DC Power Transmission', 29 April - 3 May 1996, Conference Publication, IEE.

[14] Harmonic effects on HVDC control and performance. Technical report from Manitoba HVDC Research Centre, 1994.

[15] Y. Kazachkov. Fundamentals of a series capacitor commutated HVDC terminal. IEEE Transactions on Power Delivery, Vol 13, No. 4, October 1998.

[16] http://www.pscad.com/main/pscad/pscad_v3/index.html

[17] J.R. Lucas et al. Improved simulation models for current and voltage transformers in relay studies. IEEE Transaction on Power Delivery, Vol 7, No. 1, January 1992.

[18] D.A. Woodford. Validation of digital simulation of DC links. IEEE Transactions on Power Apparatus and Systems, Vol. PAS-104, No. 9, September 1985.

[19] W.G Enright. Transformer models for electromagnetic transient studies with particular reference to HVdc Transmission. A thesis for the degree of Doctorof Philosophy at the University of Canterbury, Christchurch, New Zealand, February 1996.

[20] P.A. Lynn, W. Fuerst. Introductory Digital Signal Processing with Computer Applications. Revised edition, John Wiley & Sons Ltd. 1994.

[21] A.V. Oppenheim et. al. Signals and Systems. Pretince Hall International Editions, 1983.

[22] http://spd.ee.strath.ac.uk

[23] http://dspvillage.ti.com/docs/catalog/dspplatform/dspplatform.jhtml?familyID=110

[24] Jeff Axelrod. TMS320C2000 C-Callable FFT Package. Application report: SPRA354. Texas Instruments Incorporated, 1998. http://www-s.ti.com/sc/psheets/spra354/spra354.pdf

[25] EMTDC- Theory Manual. Manitoba HVDC Centre, 1988.

[26] M. Szechtman et al. First benchmark model for HVDC control studies. Electra, April 1991.

[27] L-E. Juhlin et al. Simulation of harmonic problems in the Kristiansand HVDC station. 13th Power Systems Computation Conference, Proceedings, Vol 2, 1999.

[28] Electrotek Concepts, Inc., Knoxville, Tennessee, USA. Evaluation of Active Filter Design and Performance Using a Detailed EMTP Model. 1994-1995.

[29] J. Arrillaga. HVDC Transmission. Peter Peregrinus Ltd. 1983

[30] J.O Gjerde, K. Uhlen, M. Hernes. HVDC - FACTS State of the art - power system harmonics. Technical report from SINTEF Energy Research, Norway, December 1996.

[31] A.E. Fitzgerald, C. Kingsley, S.D. Umans. Electric Machinery, 5th Edition in SI units. McGraw-Hill International (UK) Limited. Metric Edition 1992

[32] X. Jiang, A.M. Gole. A FREQUENCY SCANNING METHOD FOR THE IDENTIFICATION OF HARMONIC INSTABILITIES IN HVDC SYSTEMS. IEEE Transactions on Power Delivery, Vol. 10, No. 4, October 1995

[33] A.M. Gole, R. Verdolin, E. Kuffel. Firing Angle Modulation for Eliminating Transformer Dc Currents in Coupled Ac-Dc Systems. IEEE Transactions on Power Delivery, Vol. 10, No. 4, October 1995

[34] A.M. Gole, M. Meisingset. An Active Ac Filter for use at Capacitor Commutated HVDC Converters. IEEE Transactions on Power Delivery, Vol 16, No.2, April 2001.

Appendices

URN:NBN:no-2111

URN:NBN:no-2111

Table of contents:

URN:NBN:no-2111

URN:NBN:no-2111

Appendix 1

Data of the CIGRE HVDC benchmark model

Table A1.1: The components in the AC network impedance and the shunt capacitor on the rectifier side of the HVDC link

$R_{r1}(\Omega)$	$R_{r2}(\Omega)$	$L_{r1}(H)$	$C_{r1}(\mu F)$
3.737	2160.633	0.151	3.342

Table A1.2: The components in the second order highpass filter on the rectifier side of the HVDC link

$R_{r5}(\Omega)$	$L_{r3}(H)$	$C_{r4}(\mu F)$
83.32	0.0136	6.685

Table A1.3: The components in the highpass 'C' type filter on the rectifier side of the HVDC link

$R_{r3}(\Omega)$	$R_{r4}(\Omega)$	$L_{r2}(H)$	$C_{r2}(\mu F)$	$C_{r3}(\mu F)$
29.76	261.87	0.1364	6.685	74.28

Table A1.4: The resistance between earth and the neutral point on the secondary side of the Y-Y coupled converter transformer at the rectifier side of the HVDC link

$R_{r6}(M\Omega)$
1.0

Table A1.5: The DC side resistances

$R_{dc1}(\Omega)$	$R_{dc2}(\Omega)$
2.5	2.5

Table A1.6: The DC side inductances

L_{dc1}(H)	L_{dc2}(H)
0.5968	0.5968

Table A1.7: The DC side capacitance

C_{dc}(μF)
26.0

Table A1.8: The components in the AC network impedance and the shunt capacitor on the inverter side of the HVDC link

R_{i1}(Ω)	R_{i2}(Ω)	R_{i3}(Ω)	L_{i1}(H)	L_{i2}(H)	C_{i1}(μF)
0.7406	24.81	0.7406	0.0365	0.0365	7.522

Table A1.9: The components in the second order highpass filter on the inverter side of the HVDC link

R_{i6}(Ω)	L_{i4}(H)	C_{i4}(μF)
37.03	0.0061	15.04

Table A1.10: The components in the highpass 'C' type filter on the inverter side of the HVDC link

R_{i4}(Ω)	R_{i5}(Ω)	L_{i3}(H)	C_{i2}(μF)	C_{i3}(μF)
116.38	13.23	0.0606	167.2	15.04

Table A1.11: The resistance between earth and the neutral point on the secondary side of the Y-Y coupled converter transformer at the inverter side of the HVDC link

R_{i7}(MΩ)
1.0

Table A1.12: The voltage source on the rectifier side

$U_{L\text{-}L,rms}$ (kV)	382.8672
Frequency (Hz)	50
Earthed starpoint ?	yes
Ramp up time (sec)	0.05
Phase shift (^{0})	0.0

Table A1.13: The voltage source on the inverter side

$U_{L\text{-}L,rms}$ (kV)	215.05
Frequency (Hz)	50
Earthed starpoint ?	Yes
Ramp up time (sec)	0.05
Phase shift (^{0})	0.0

Table A1.14: The Y-Y and the Y-D coupled transformers on the rectifier side

Rated power (MVA)	603.73
Rated frequency (Hz)	50
Rated primary side voltage $(kV)_{L\text{-}L,rms}$	345
Rated secondary side voltage $(kV)_{L\text{-}L,rms}$	213.4557
Leakage reactance (pu)	0.18
Air core reactance (pu)	0.36
No load losses (pu)	0.01
Knee voltage (pu)	1.22

Table A1.15: The Y-Y and the Y-D coupled transformers on the inverter side

Rated power (MVA)	591.79
Rated frequency (Hz)	50
Rated primary side voltage $(kV)_{L-L,rms}$	230
Rated secondary side voltage $(kV)_{L-L,rms}$	209.2288
Leakage reactance (pu)	0.18
Air core reactance (pu)	0.36
No load losses (pu)	0.01
Knee voltage (pu)	1.25

Table A1.16: Data for the valves

On resistance (Ω)	0.01
Off resistance (Ω)	1.0E8
Forward voltage drop (kV)	0
Forward breakover voltage (kV)	1.0E5
Reverse withstand voltage (kV)	1.0E5
Minimum extinction time (sec)	0
Snubber resistance (Ω)	5000
Snubber capacitance (μF)	0.05

Table A1.17: The data of the PI-controller in Figure 6.2

T_i (sec)	0.003
K_p (rad/sec)	1.0607
Minimum output (rad)	3.054
Maximum output (rad)	0.52
Initial output (rad)	1.57

Table A1.18: The data of the lowpass filter in figure 6.2

G	0.5
T (sec)	0.0012

Table A1.19: Data for the PI controller in the phase-locked loop of the rectifier bridge

G	25
T_i	0.01

Table A1.20: Data for the lowpass filter that filter V_{dci} in Figure 6.3

G_2	0.5
T_2	0.0012

Table A1.21: Data for the lowpass filter that filter I_{dci} in Figure 6.3

G_2	0.5
T_2	0.0012

Table A1.22: Data for the constant current controller in Figure 6.3

K_{p1} (rad/sec)	0.63
T_{i1} (sec)	0.01524
Minimum output (rad)	1.92
Maximum output (rad)	0.52
Initial output (rad)	1.92

Table A1.23: Data for the constant extinction angle controller in Figure 6.3

K_{p2} (rad/sec)	0.7506

Table A1.23: Data for the constant extinction angle controller in Figure 6.3

T_{i2} (sec)	0.0544
Minimum output (rad)	1.57
Maximum output (rad)	0.52
Initial output (rad)	1.57

Table A1.24: Data for the non-linear function X in Figure 6.3

Lower input threshold	0.4
Lower threshold output	0.55
Upper input threshold	0.9
Upper threshold output	1.0
Gain below lower threshold	0.0
Gain above upper threshold	1.0

Table A1.25: Data for the ramp function Y in Figure 6.3

Start of ramp	0.0
Saturating input	0.1
Saturated output	0.2793

Table A1.26: Data for the PI controller in the phase locked loop of the inverter bridge

K_p	10
T_i	0.02

Appendix 2

Additional simulation results of the case described in Section 6.1

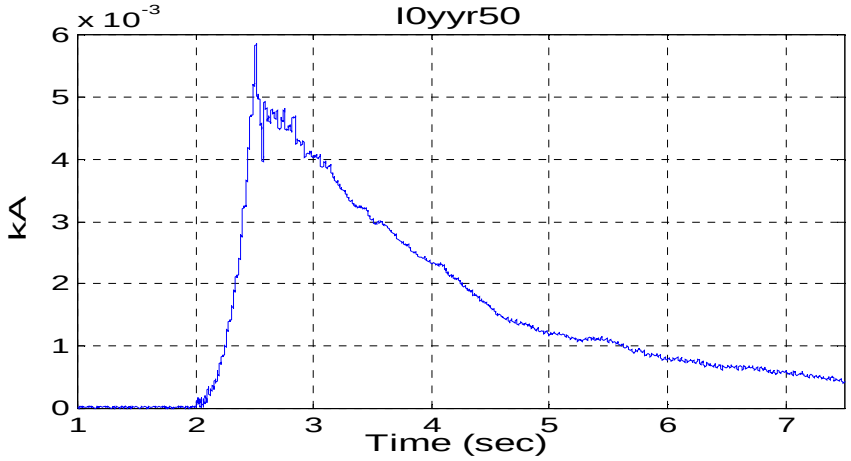


Figure A2.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

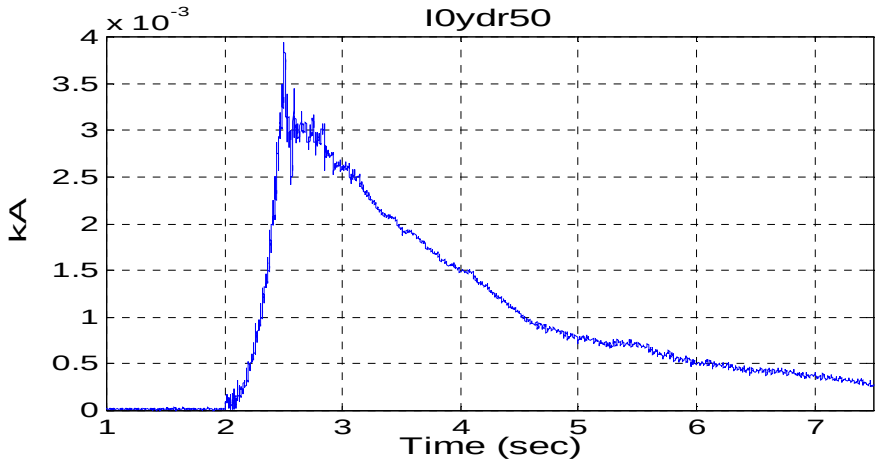


Figure A2.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

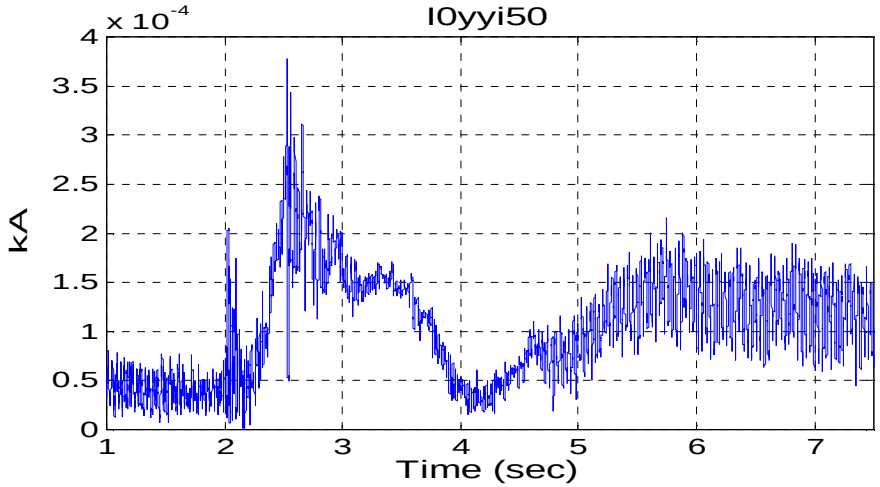


Figure A2.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

URN:NBN:no-2111

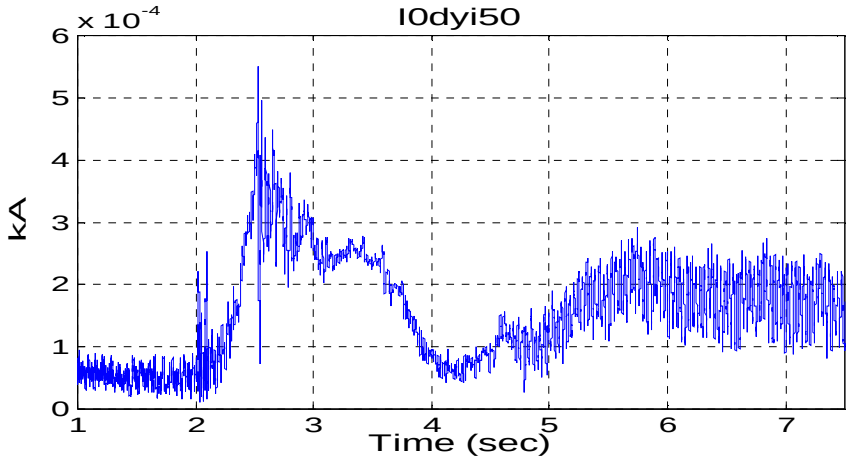


Figure A2.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

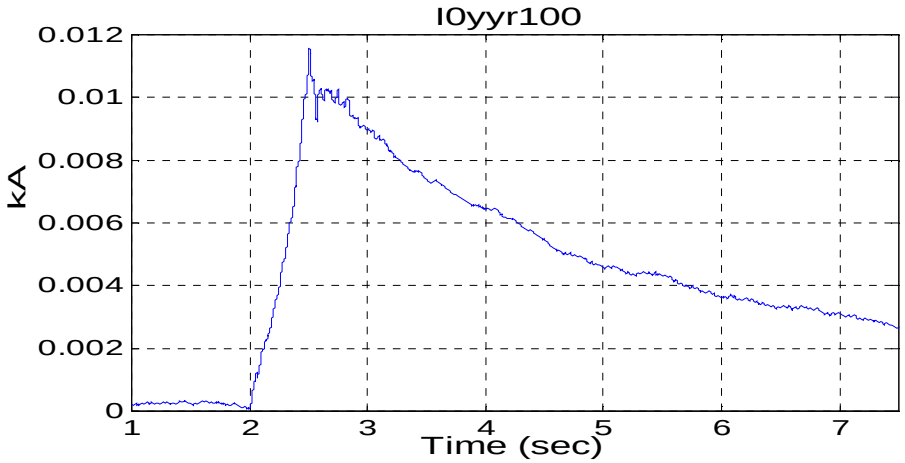


Figure A2.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

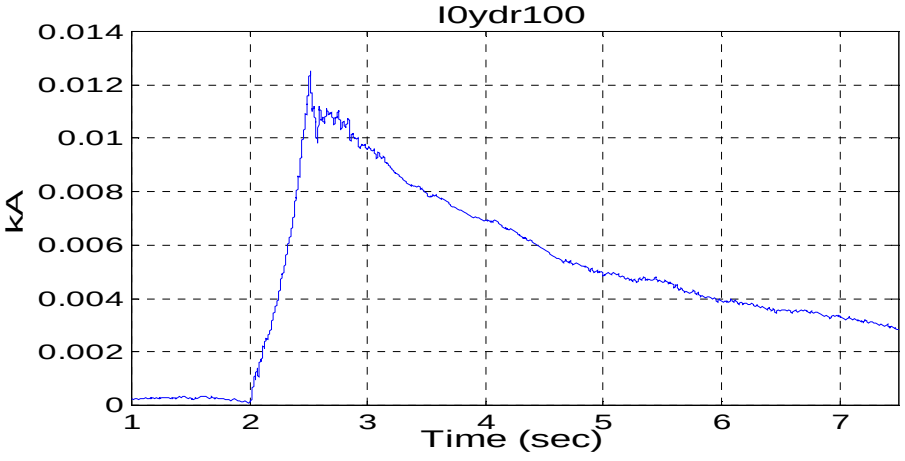


Figure A2.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

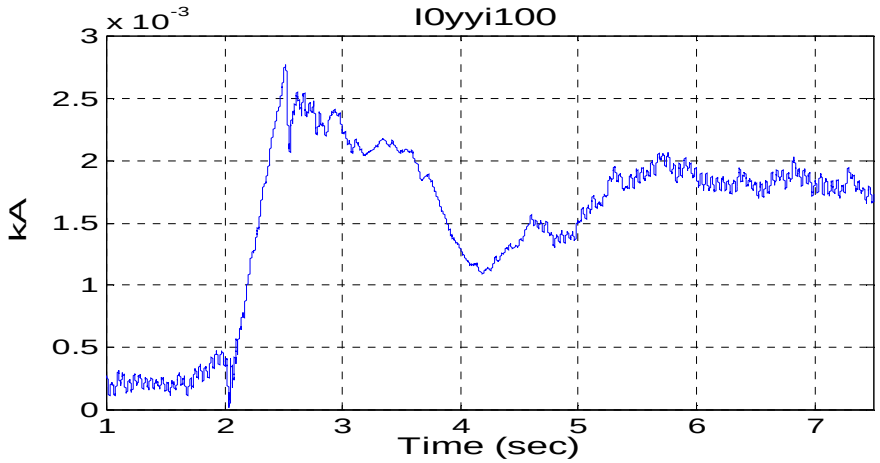


Figure A2.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

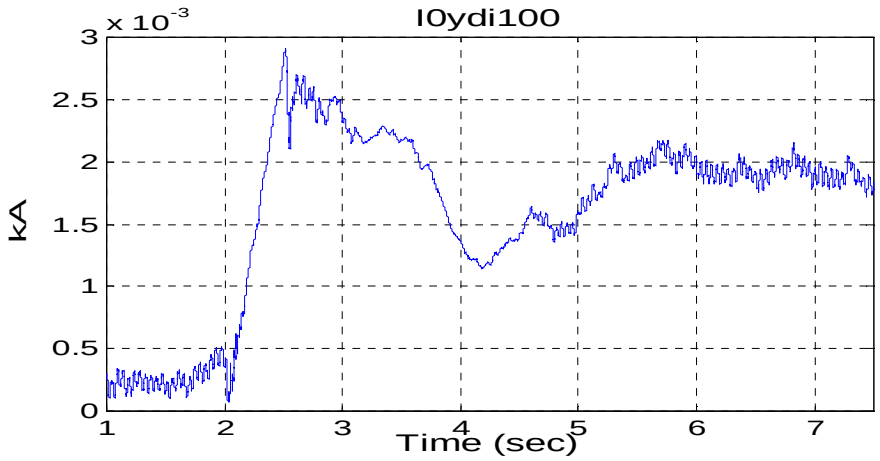


Figure A2.8: The 100 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

Appendix 3

Additional simulation results of the case described in Section 6.2

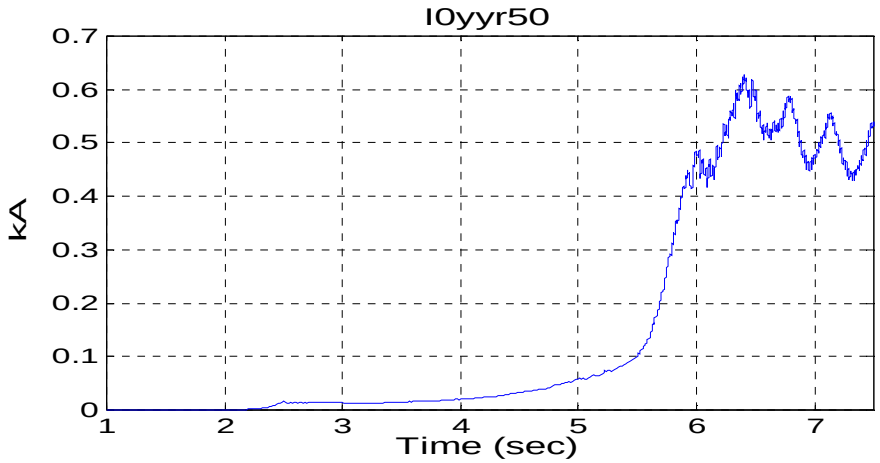


Figure A3.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

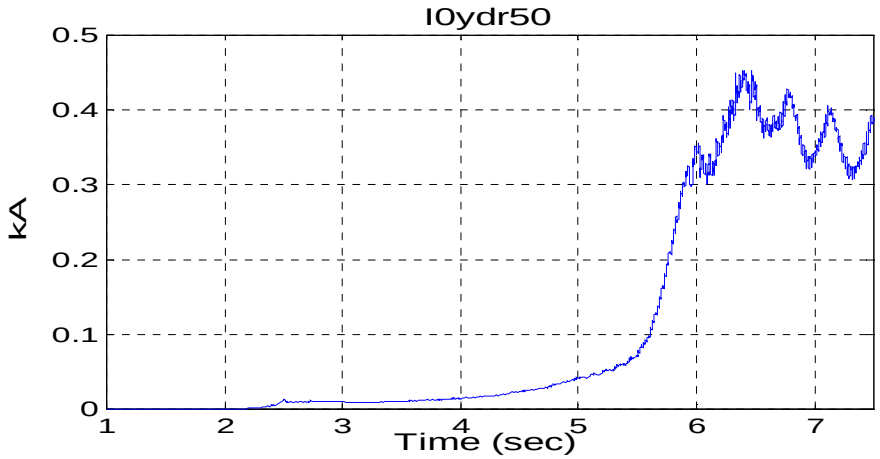


Figure A3.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

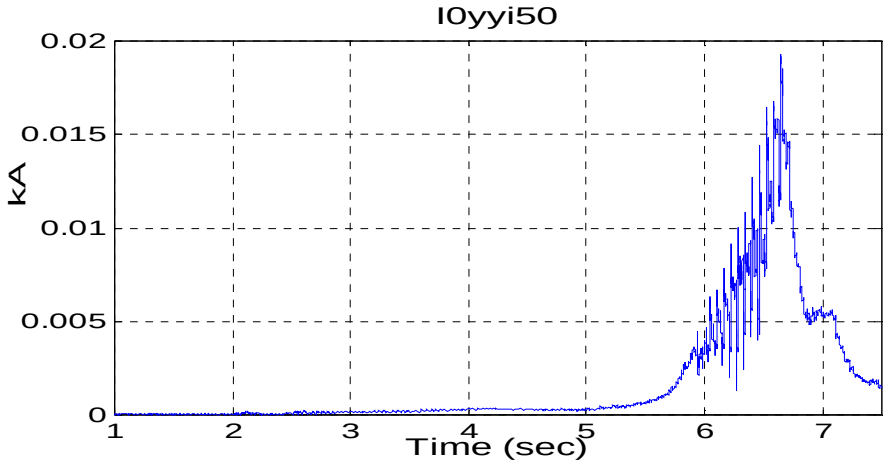


Figure A3.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

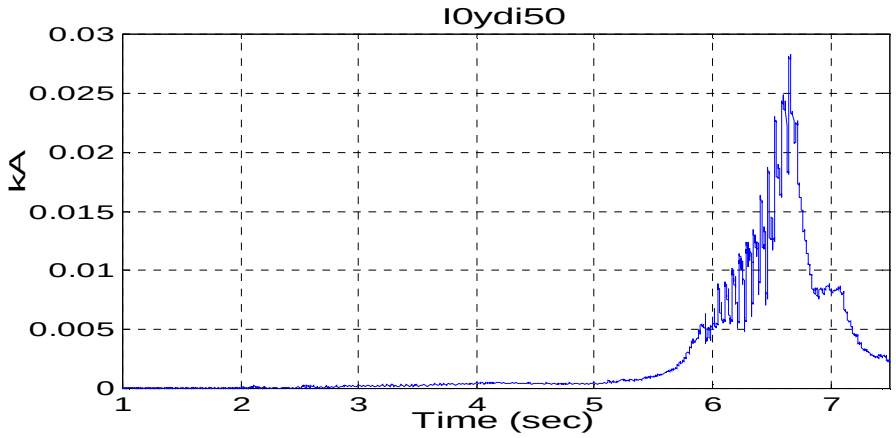


Figure A3.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

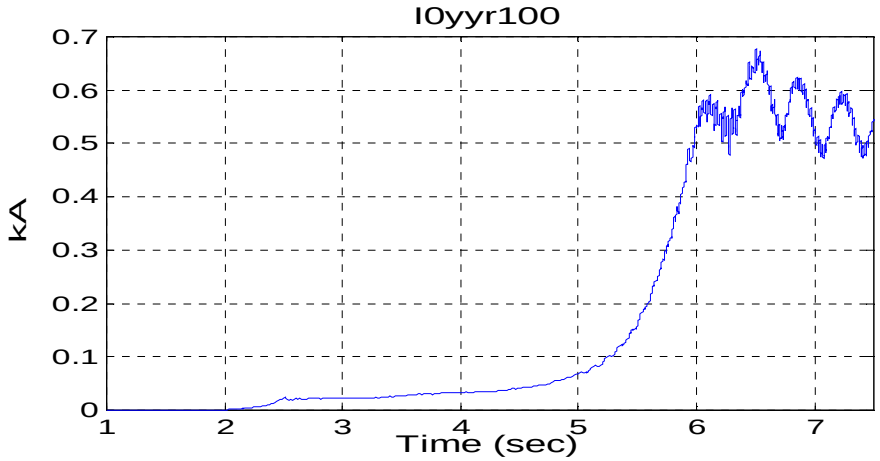


Figure A3.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

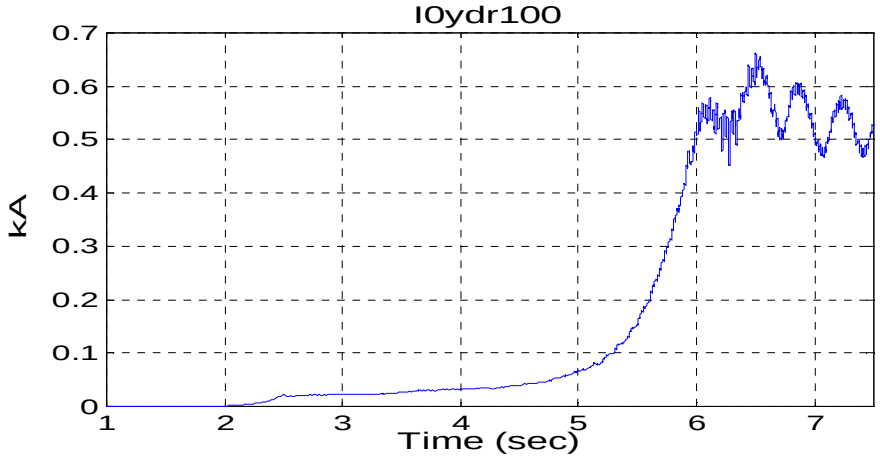


Figure A3.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

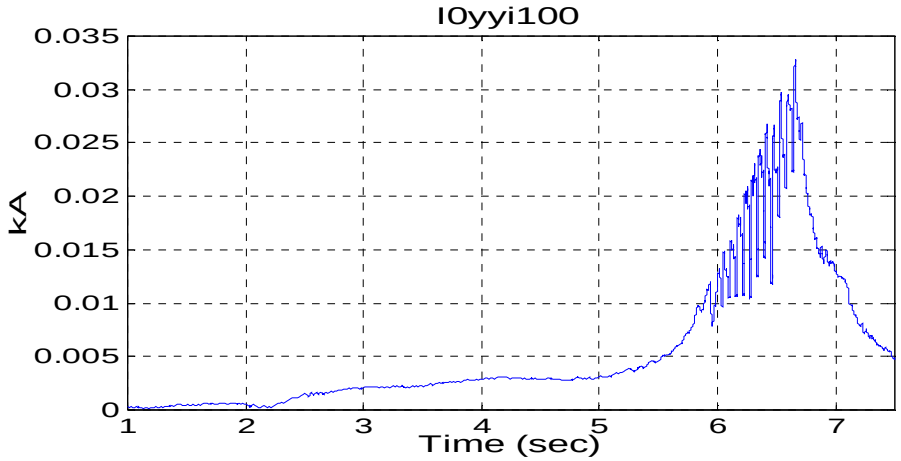


Figure A3.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

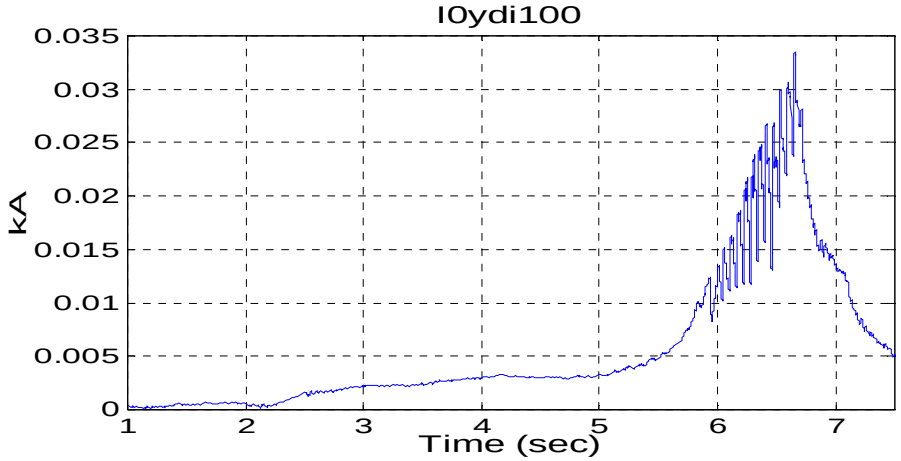


Figure A3.8: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

Appendix 4

Additional simulation results of the case described in Section 7.1

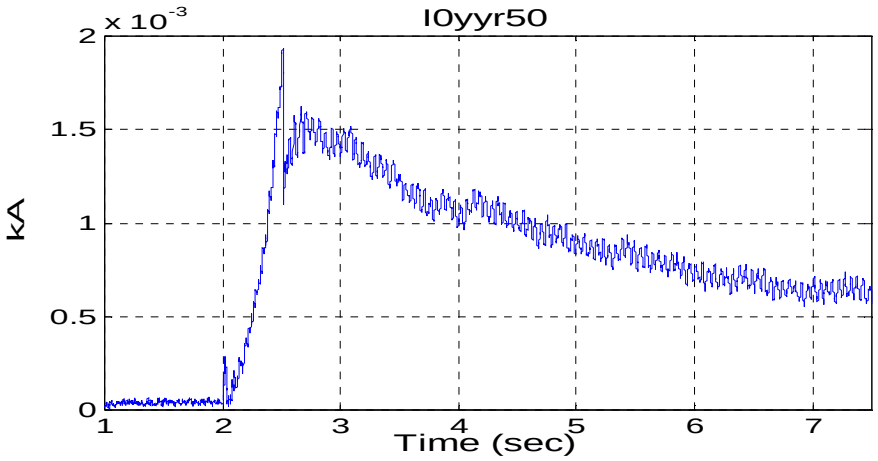


Figure A4.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

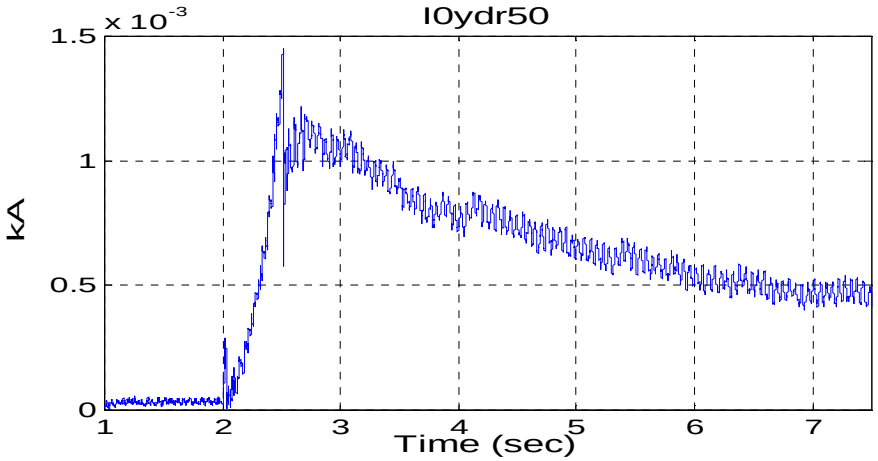


Figure A4.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

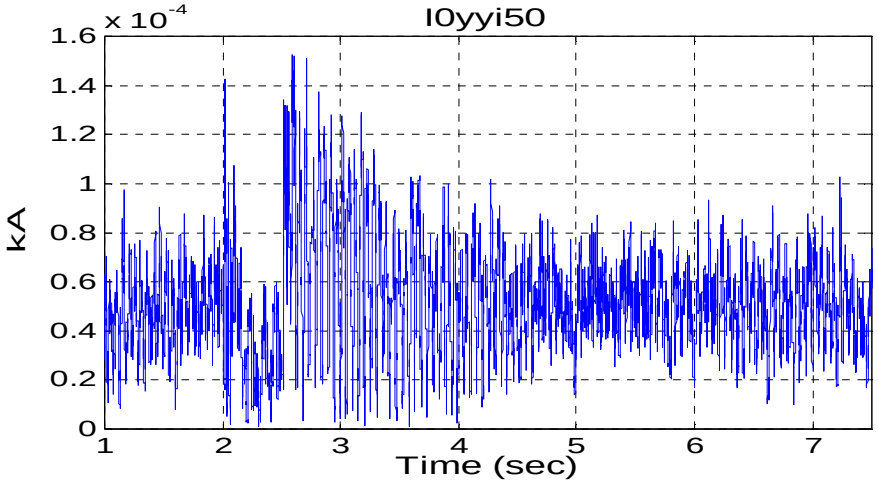


Figure A4.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

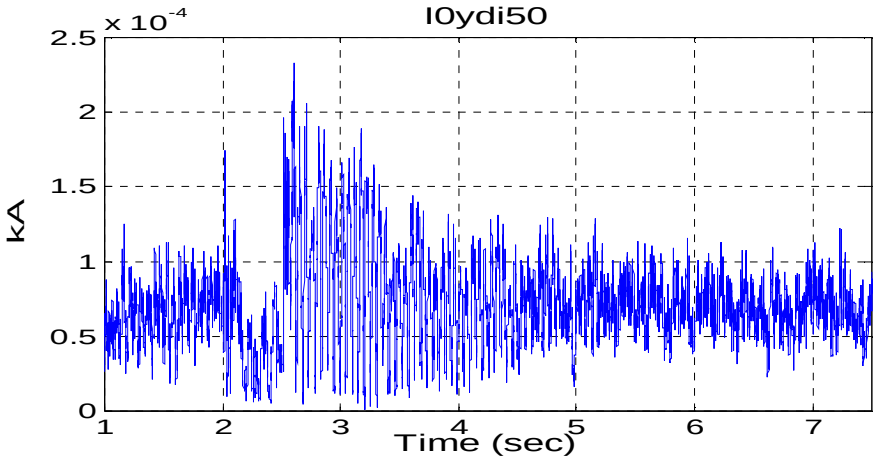


Figure A4.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

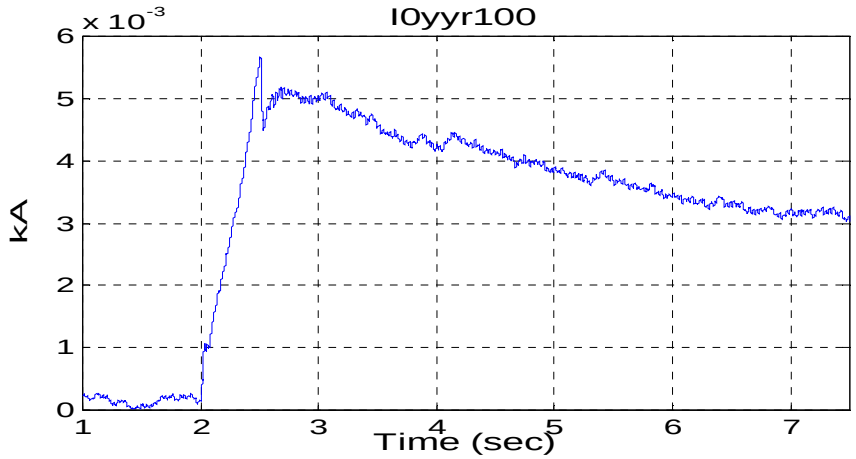


Figure A4.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

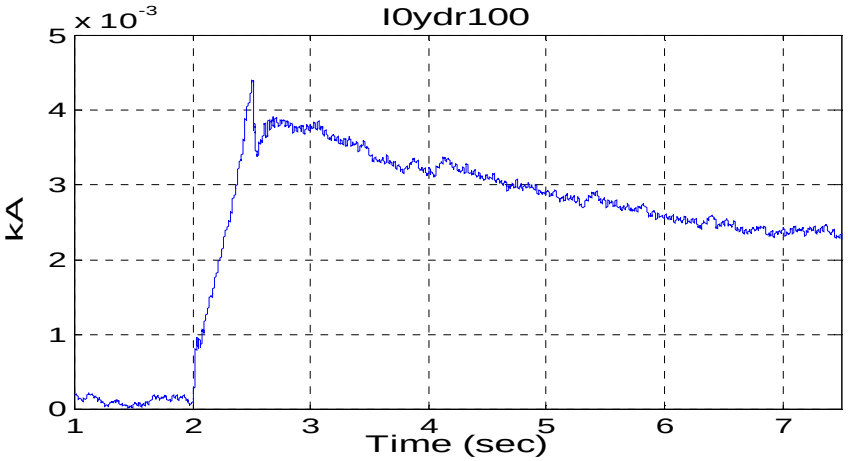


Figure A4.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

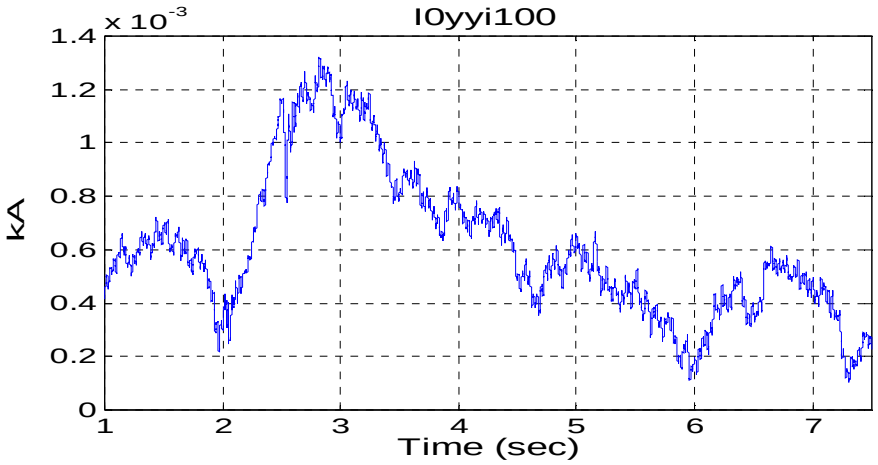


Figure A4.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

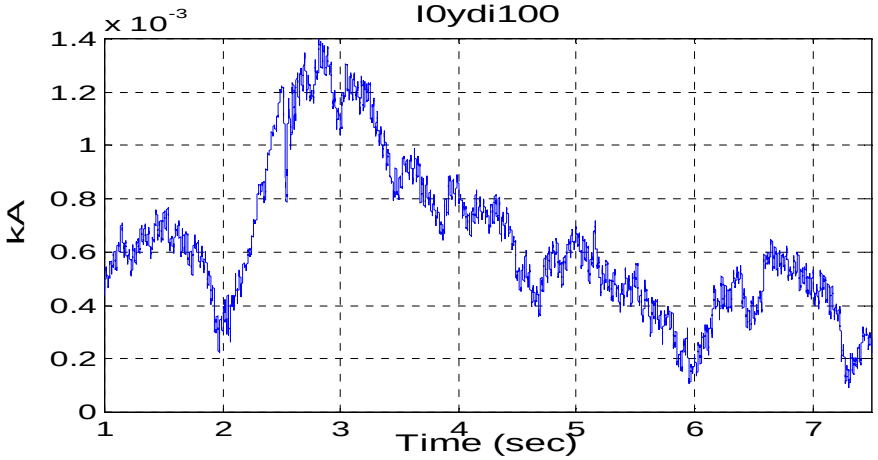


Figure A4.8: The 100 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

Appendix 5

Additional simulation results of the case described in Section 7.2

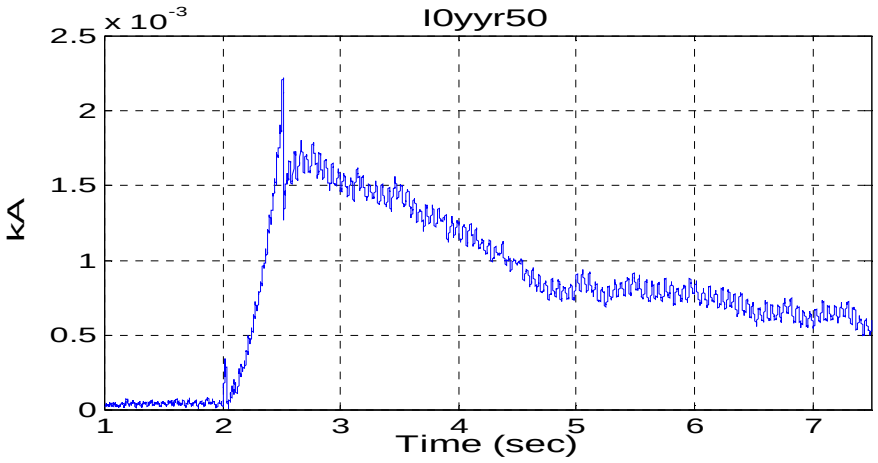


Figure A5.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

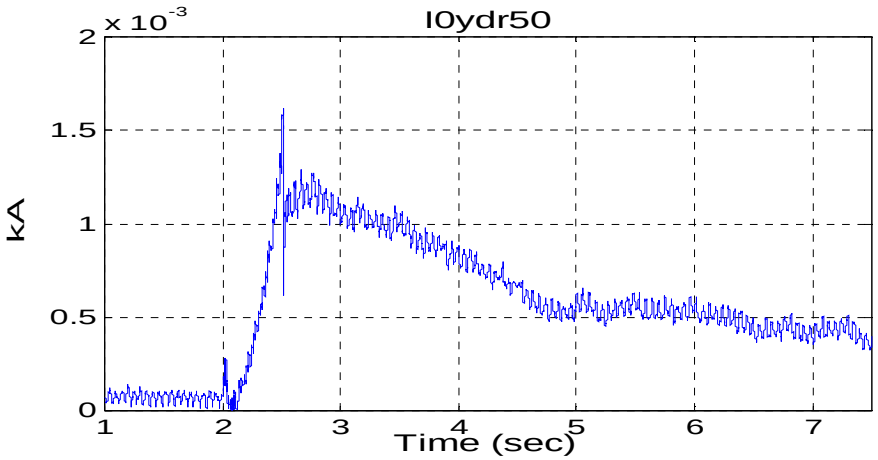


Figure A5.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

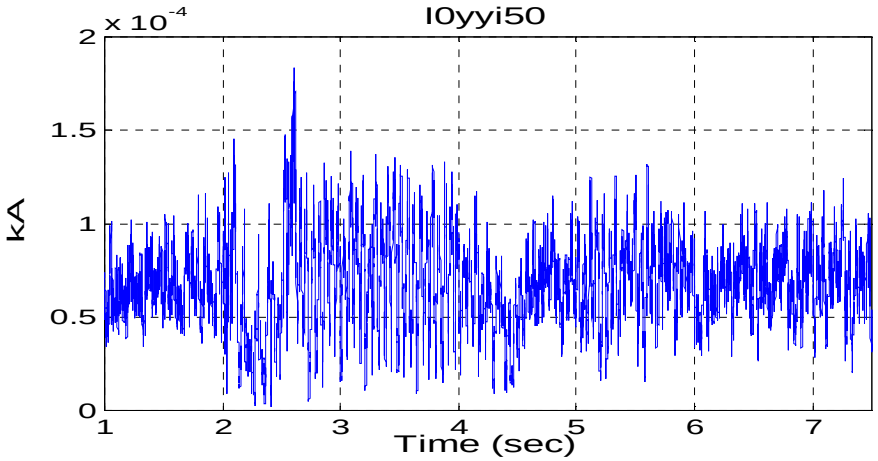


Figure A5.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

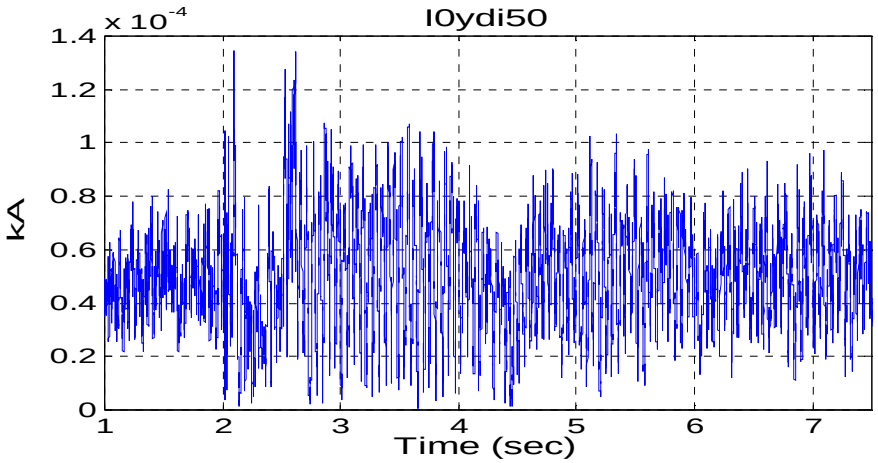


Figure A5.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

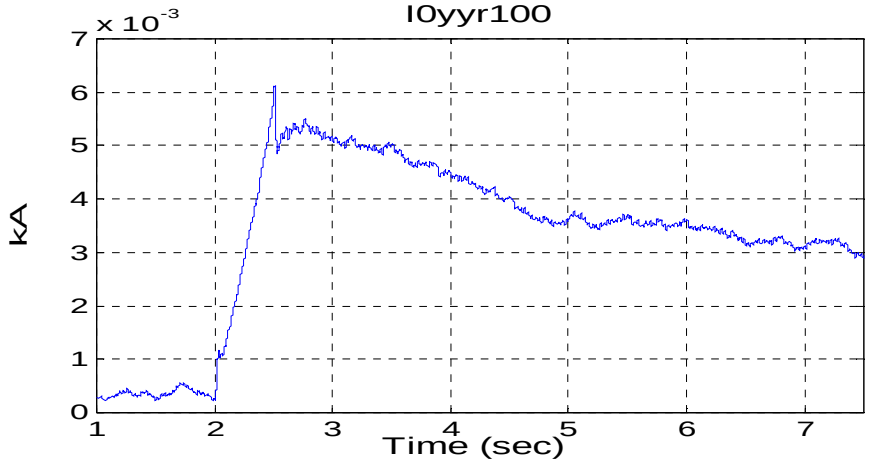


Figure A5.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

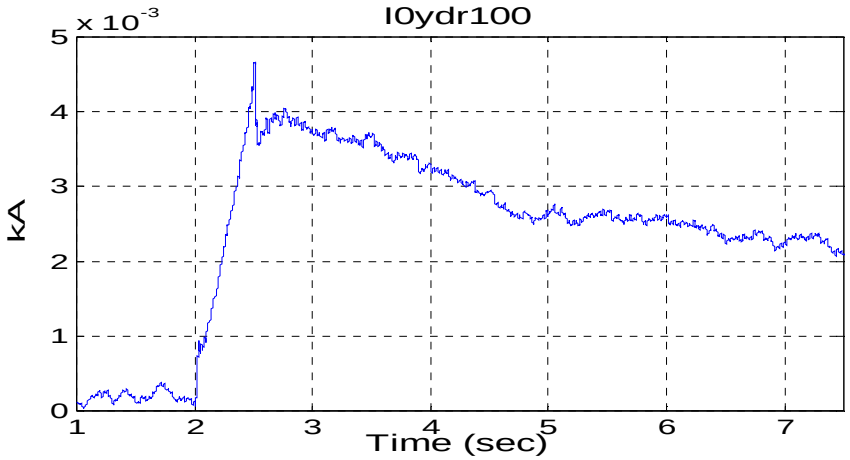


Figure A5.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

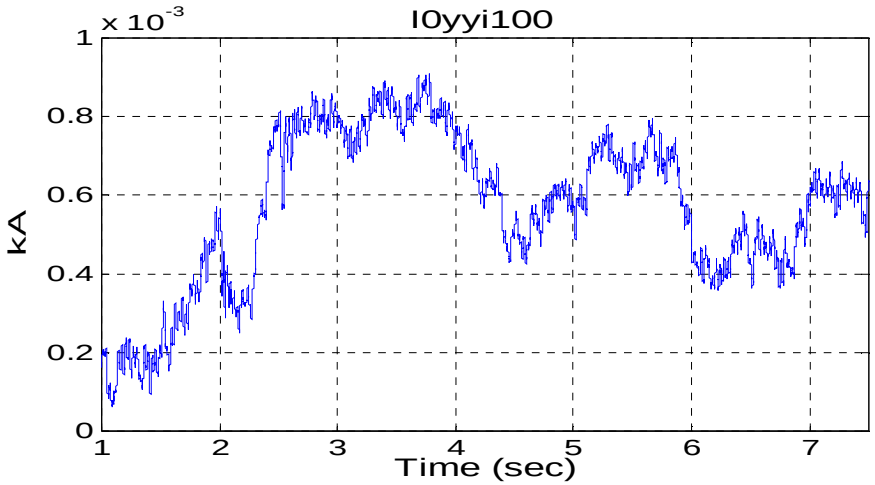


Figure A5.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

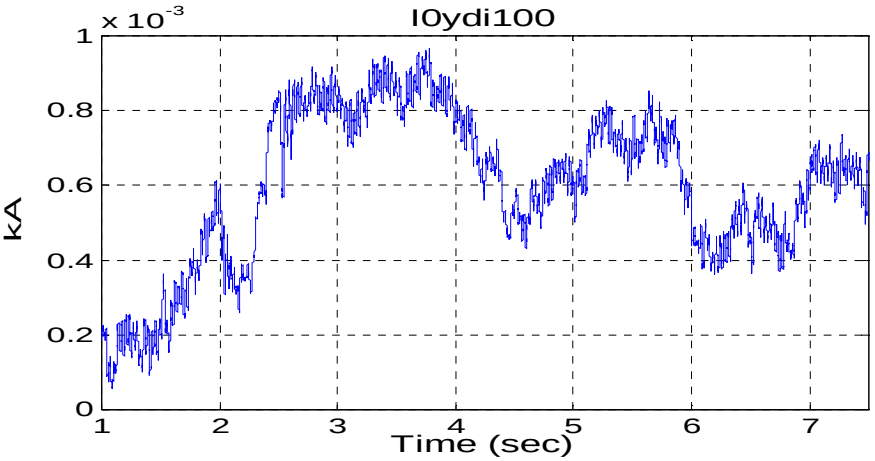


Figure A5.8: The 100 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

Appendix 6

Additional simulation results of the case described in Section 7.3.1

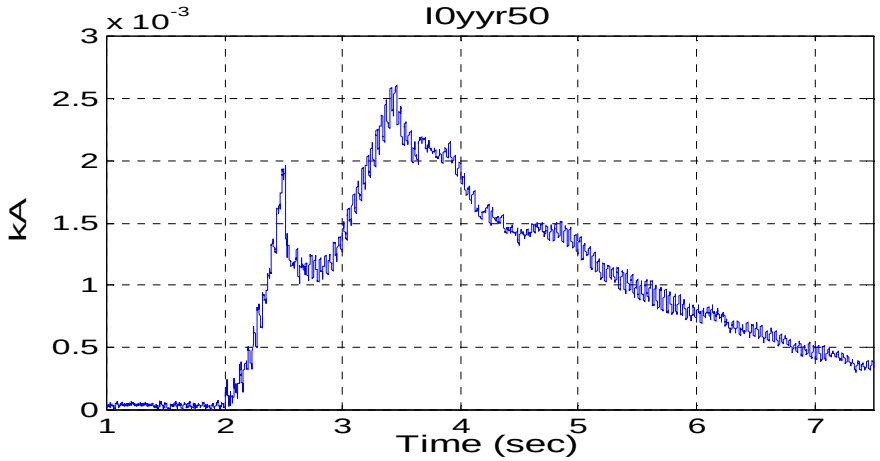


Figure A6.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

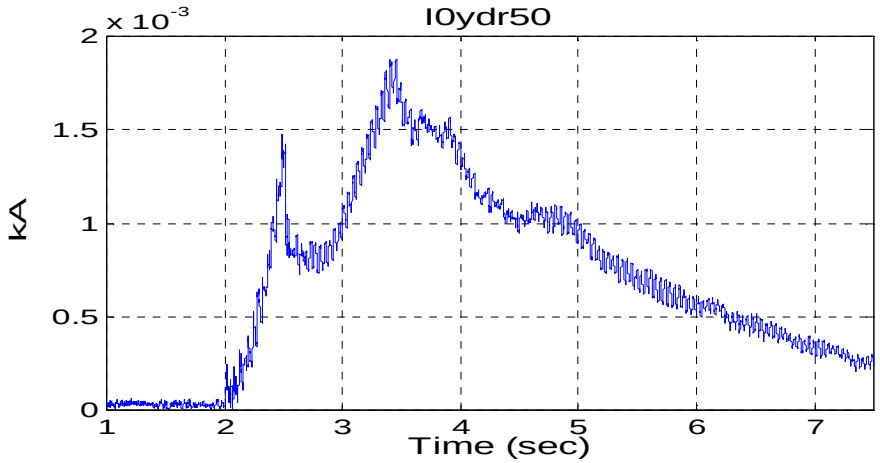


Figure A6.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

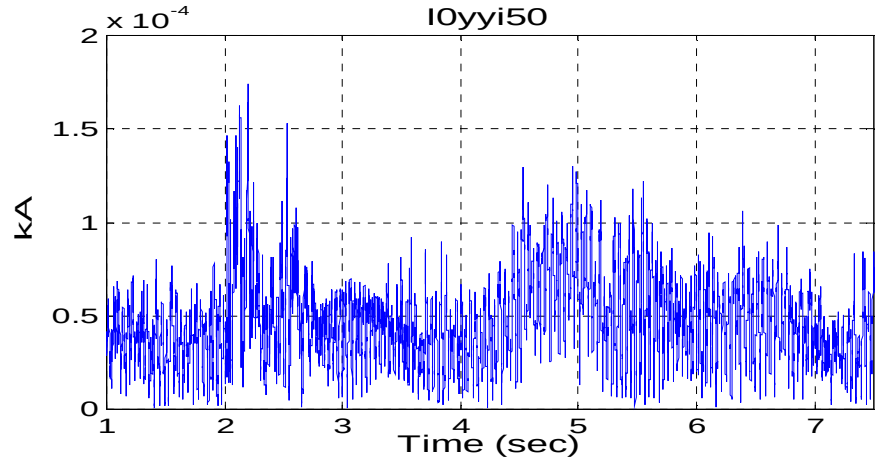


Figure A6.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

URN:NBN:no-2111

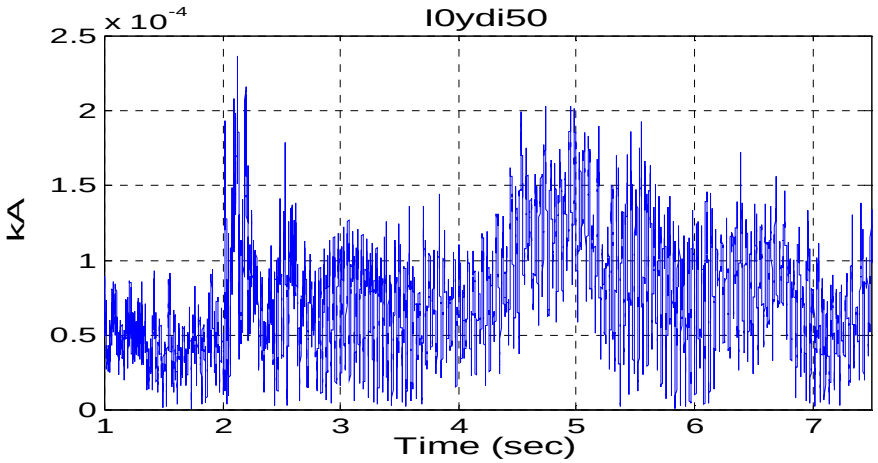


Figure A6.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

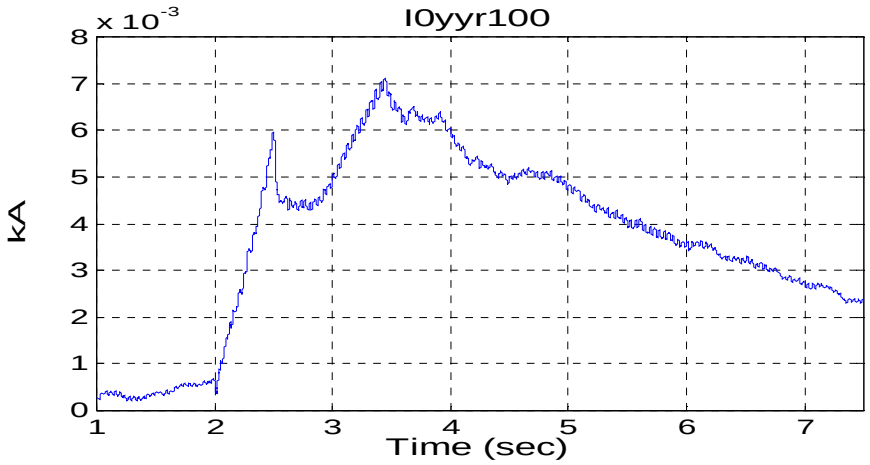


Figure A6.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

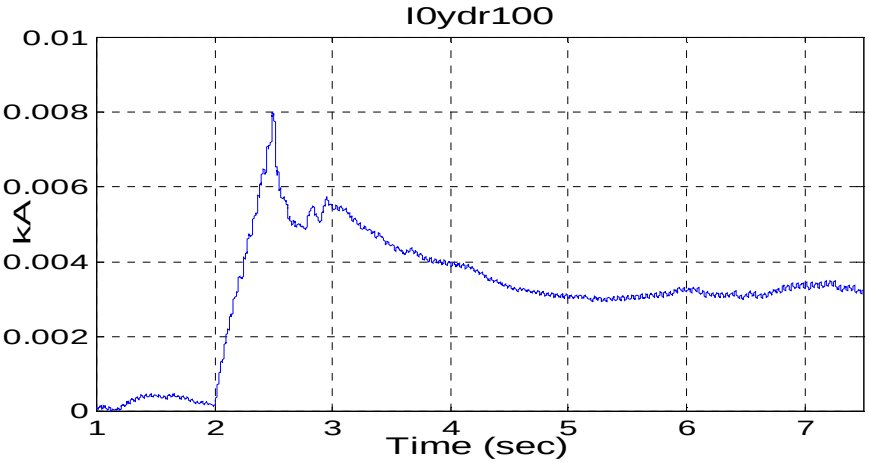


Figure A6.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

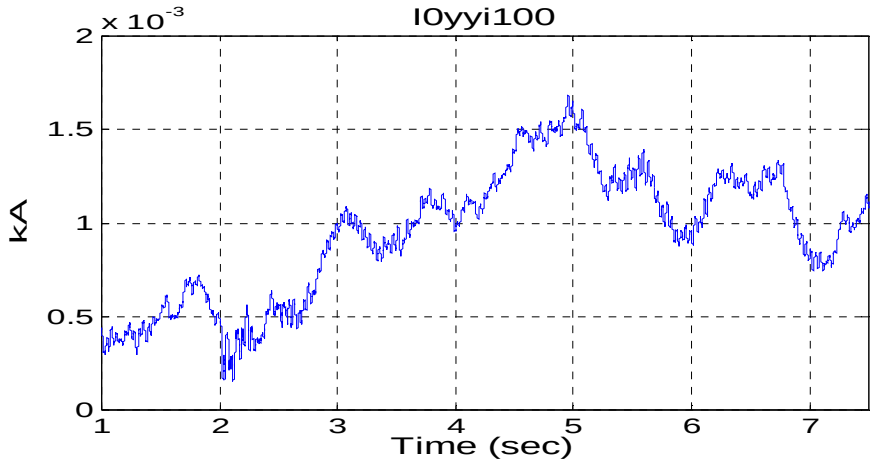


Figure A6.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

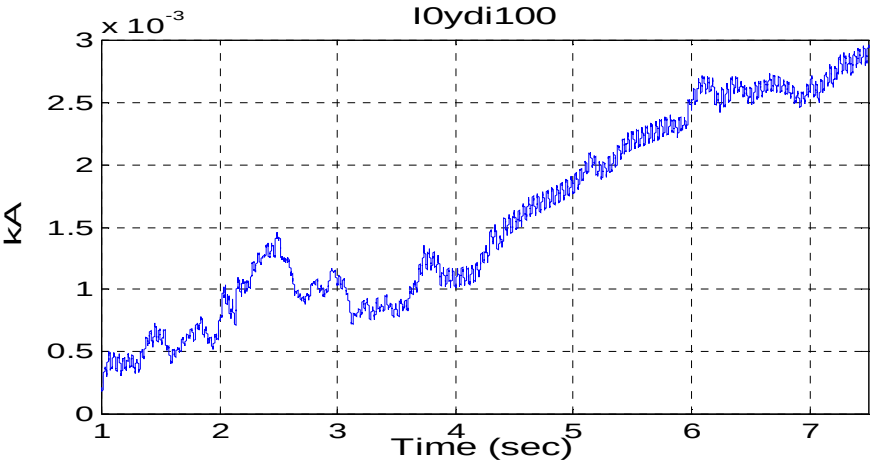


Figure A6.8: The 100 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

Appendix 7

Additional simulation results of the case described in Section 7.3.2

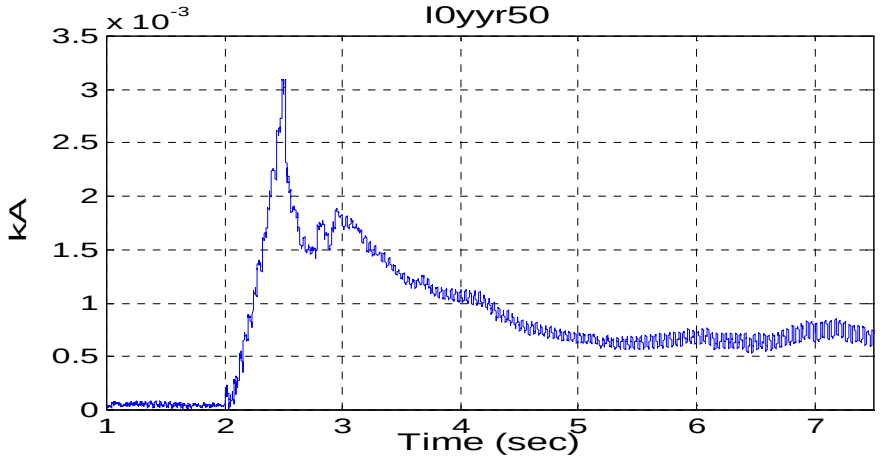


Figure A7.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

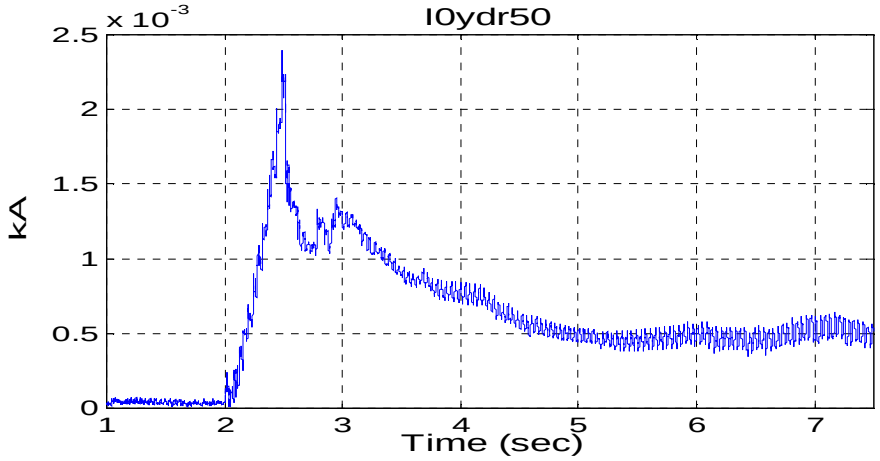


Figure A7.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

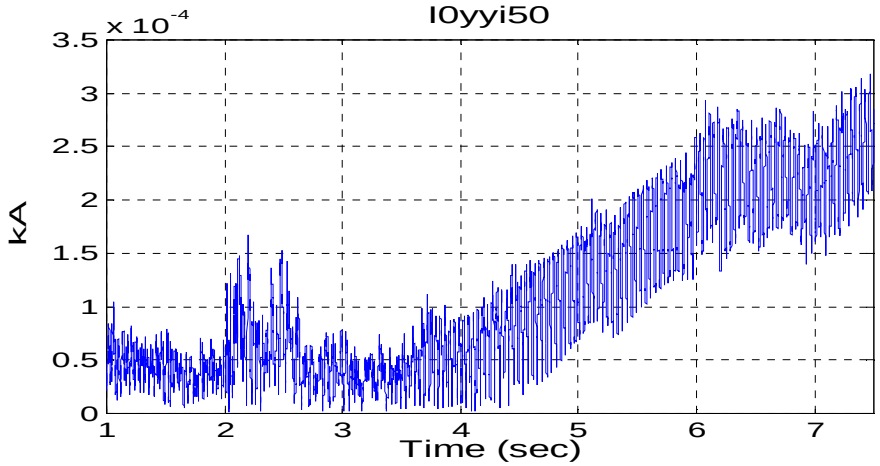


Figure A7.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

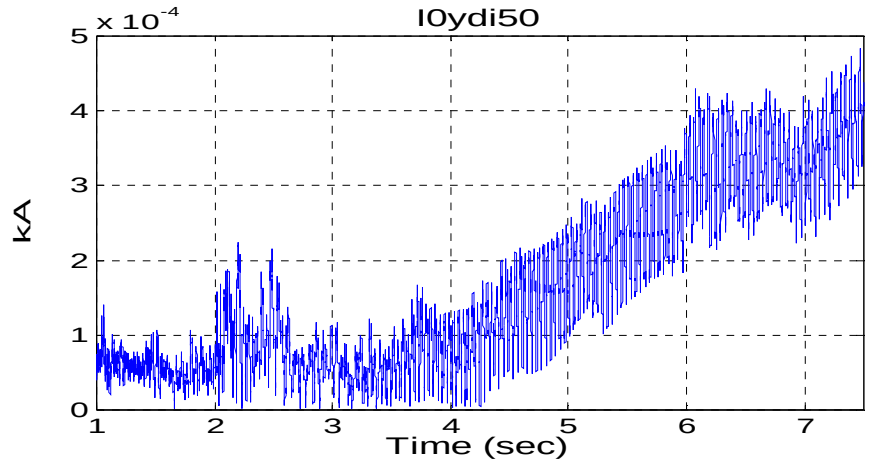


Figure A7.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

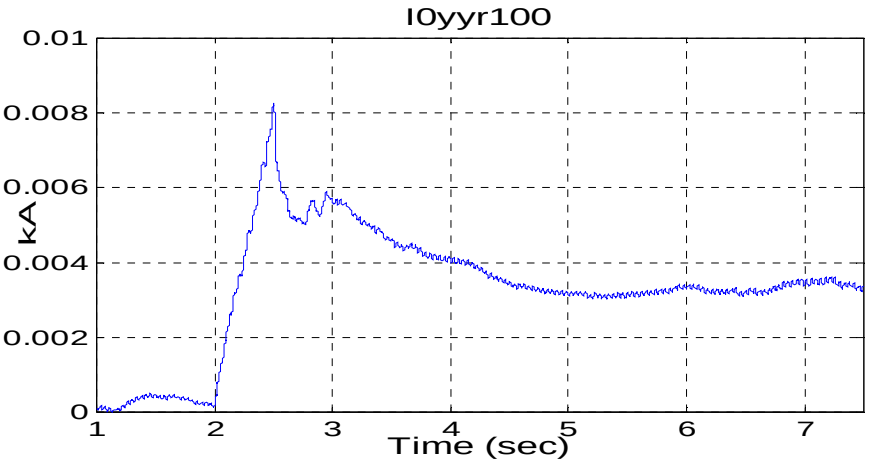


Figure A7.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

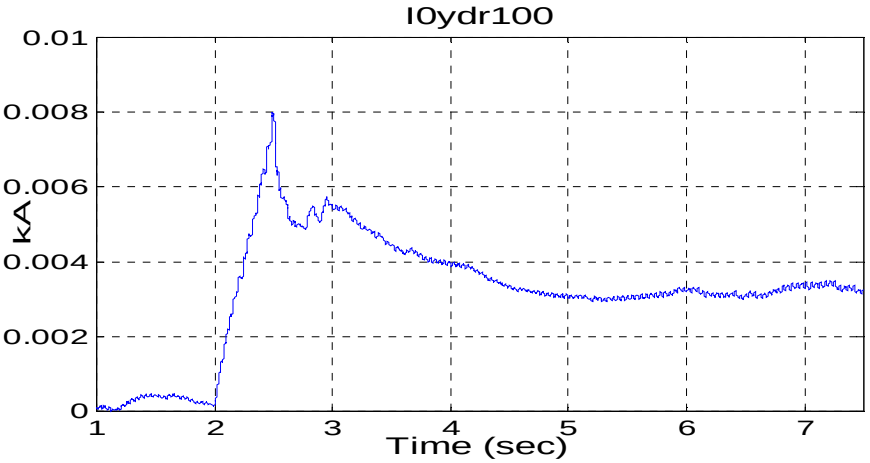


Figure A7.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

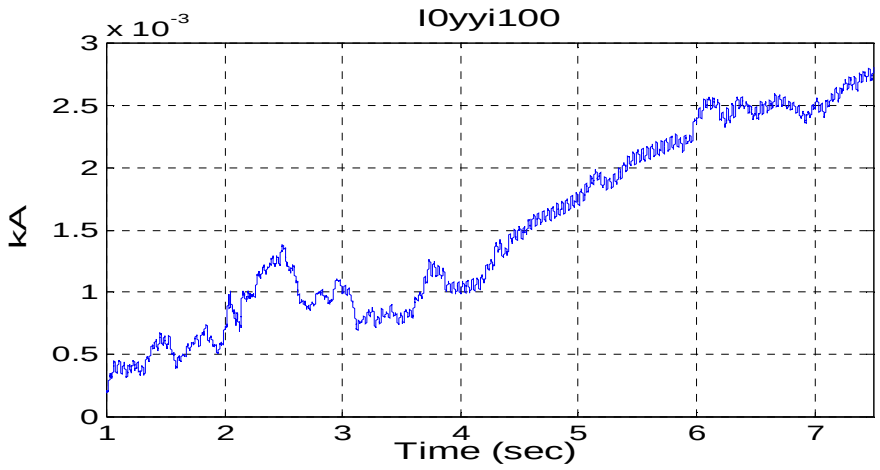


Figure A7.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

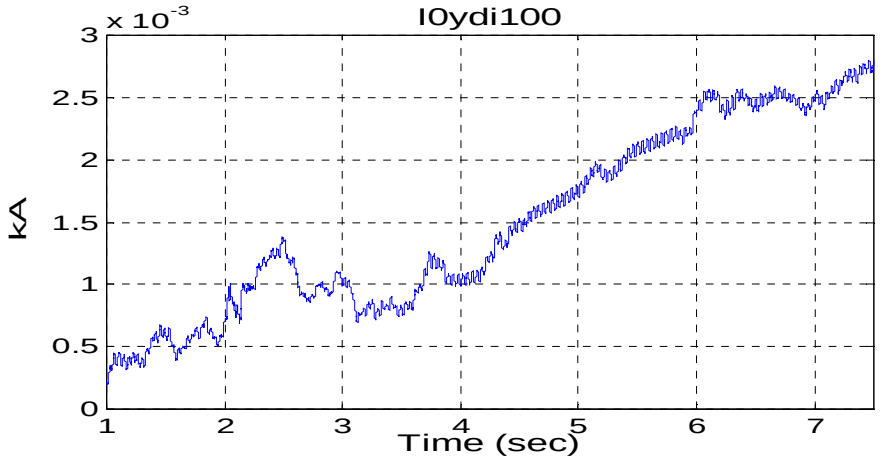


Figure A7.8: The 100 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

Appendix 8

Additional simulation results of the case described in Section 7.3.3

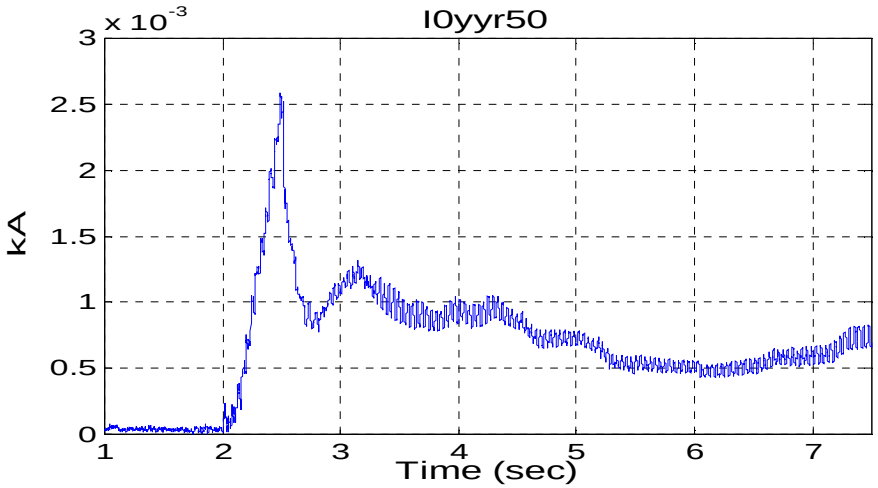


Figure A8.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

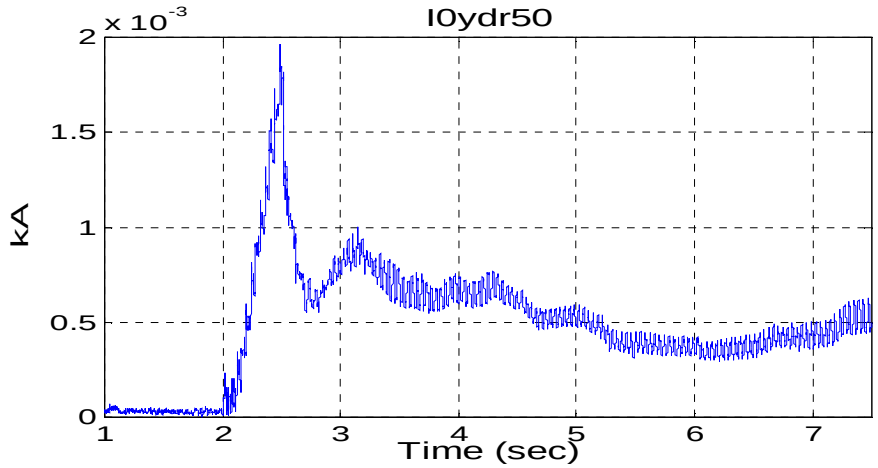


Figure A8.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

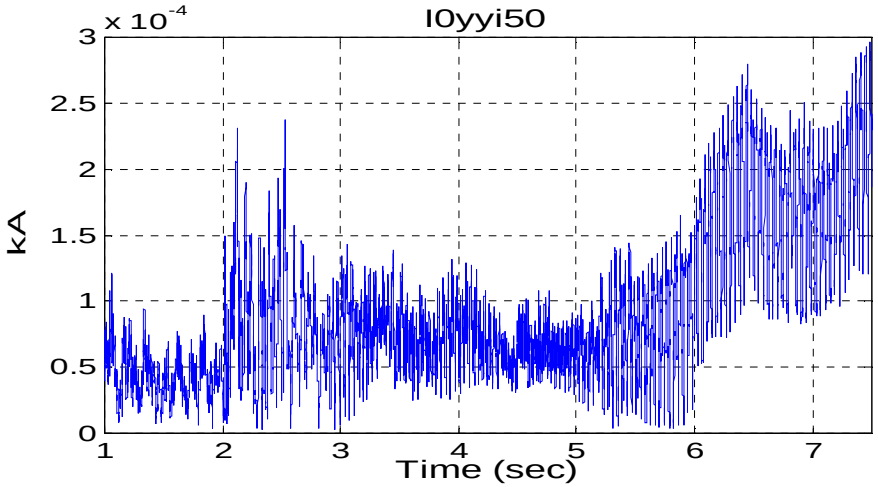


Figure A8.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

URN:NBN:no-2111

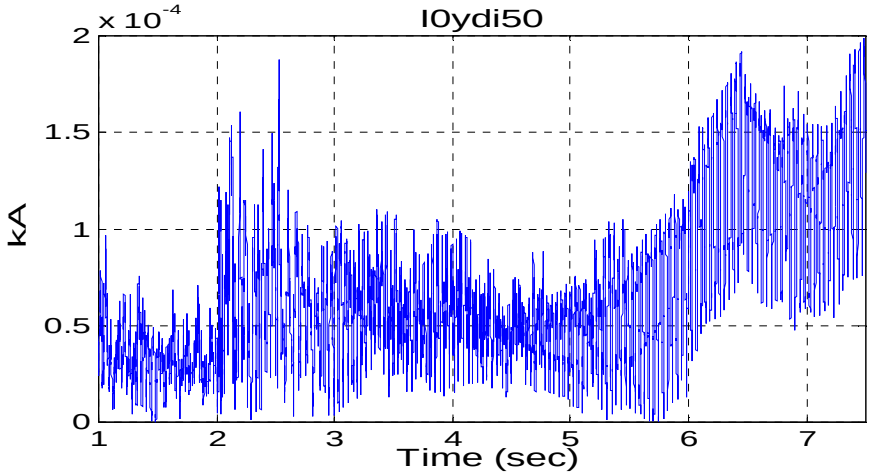


Figure A8.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

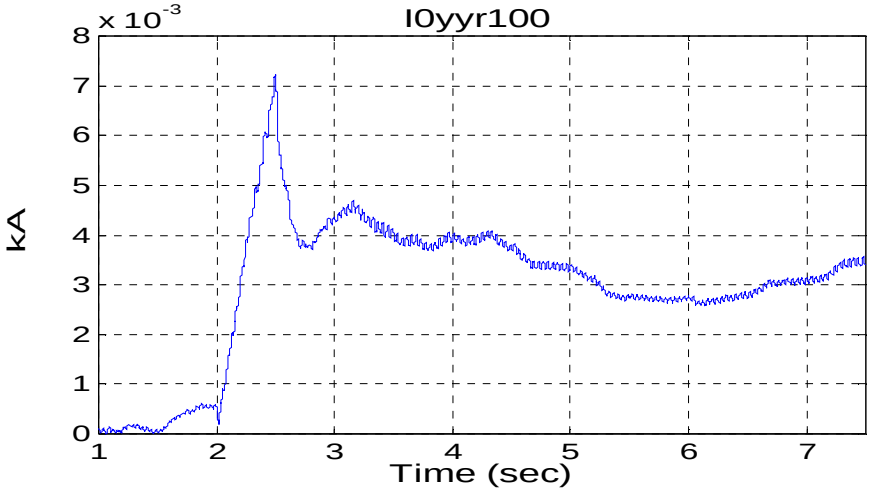


Figure A8.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

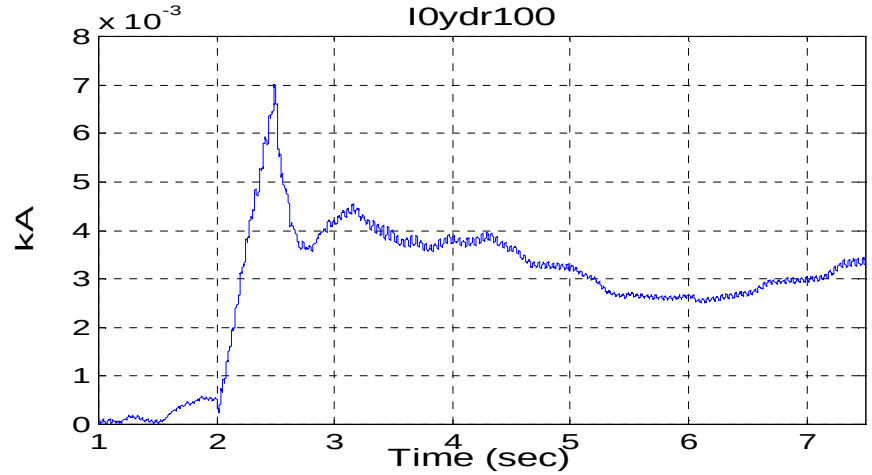


Figure A8.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

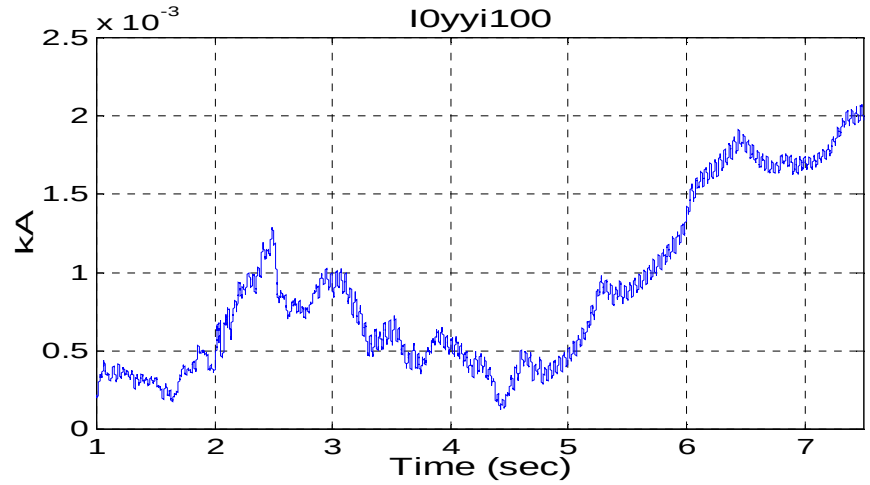


Figure A8.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

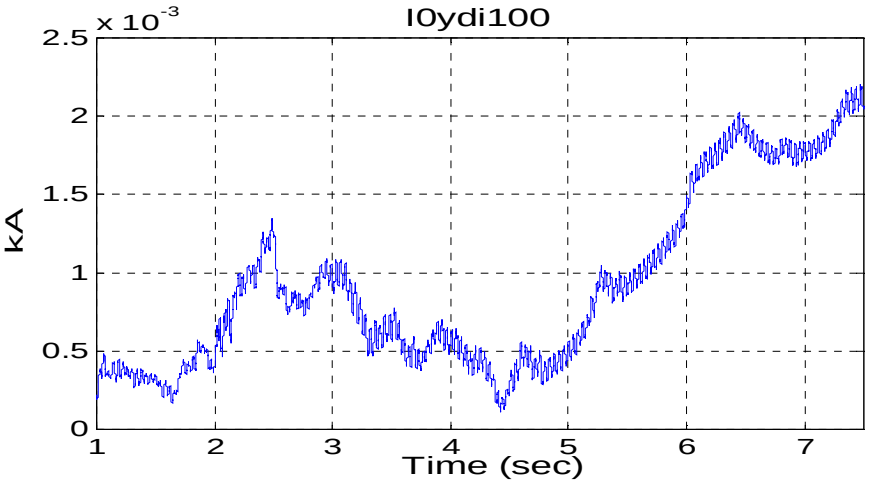


Figure A8.8: The 100 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

Appendix 9

Additional simulation results of the case described in Section 7.3.4

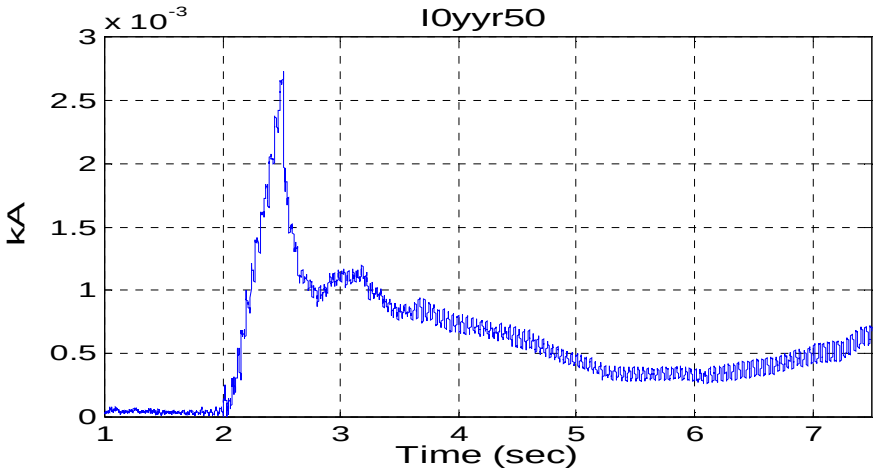


Figure A9.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

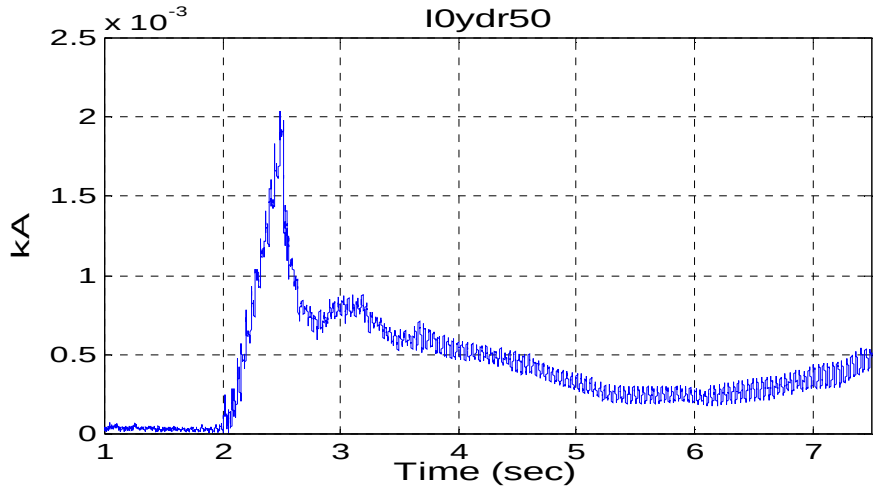


Figure A9.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

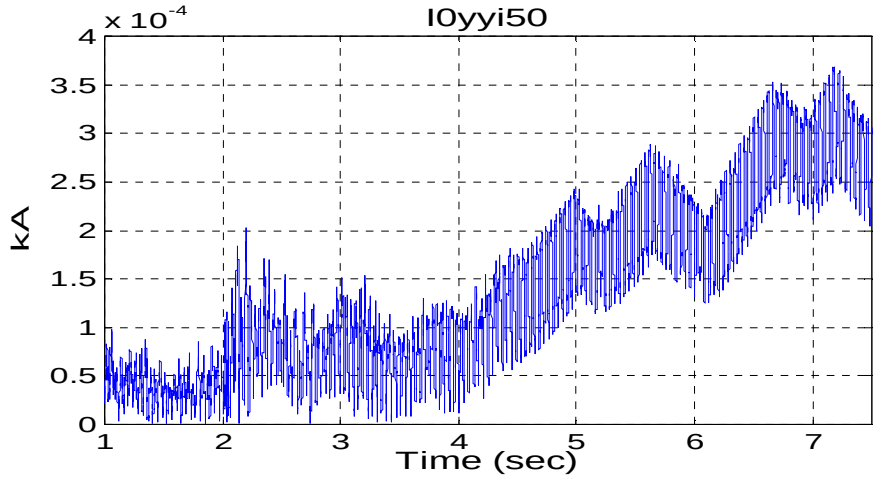


Figure A9.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

URN:NBN:no-2111

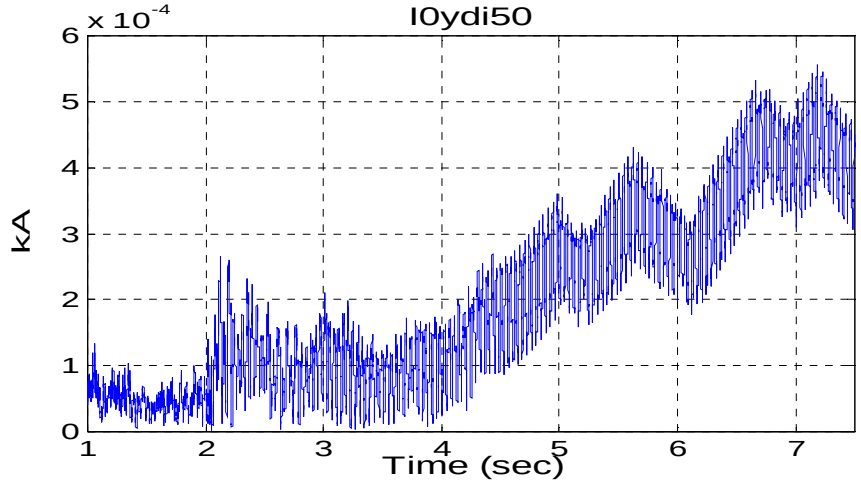


Figure A9.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

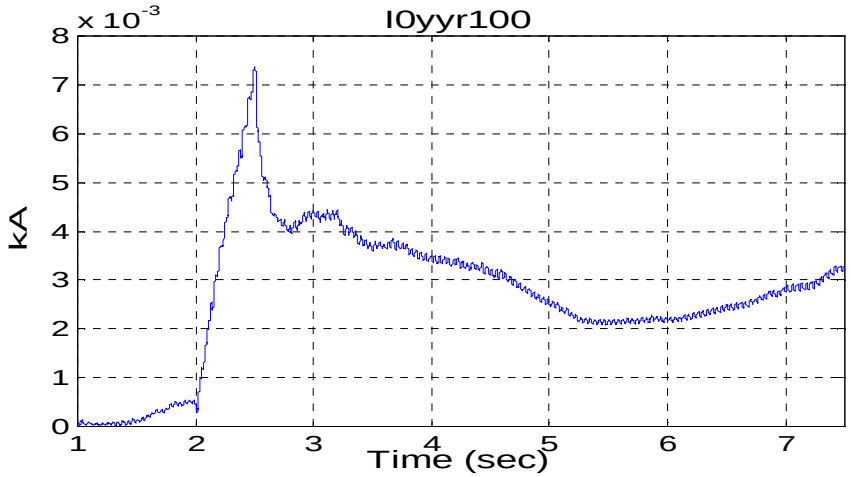


Figure A9.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

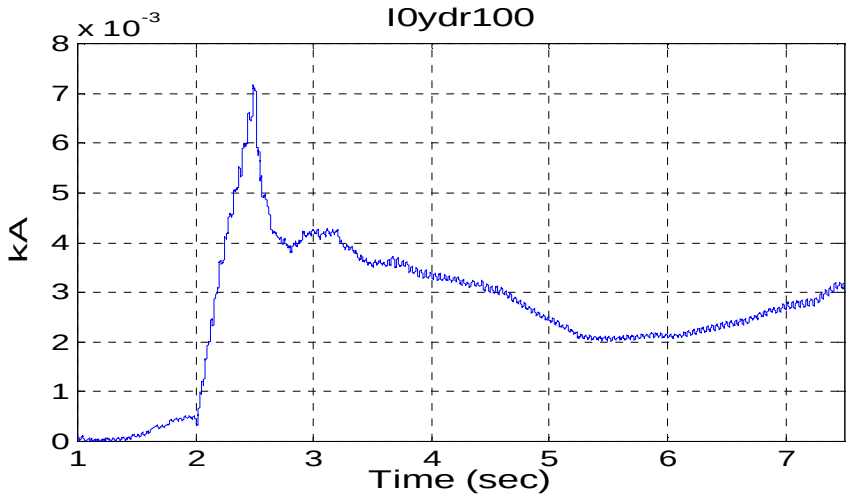


Figure A9.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

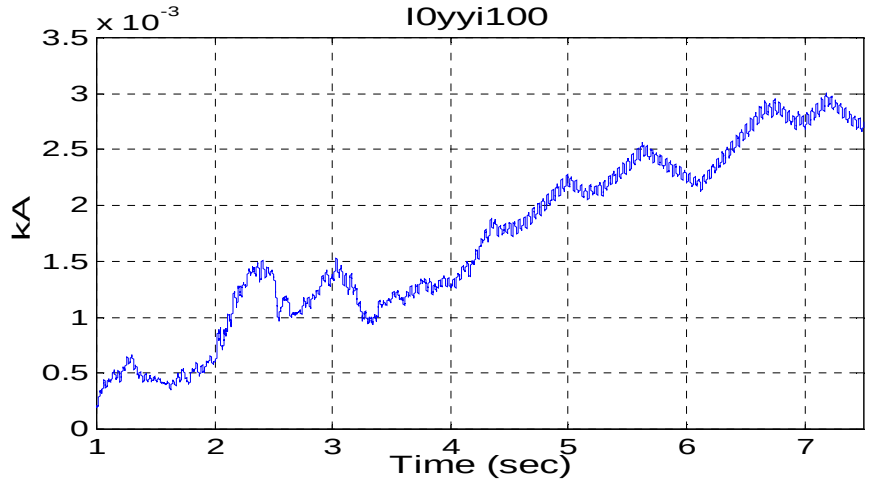


Figure A9.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

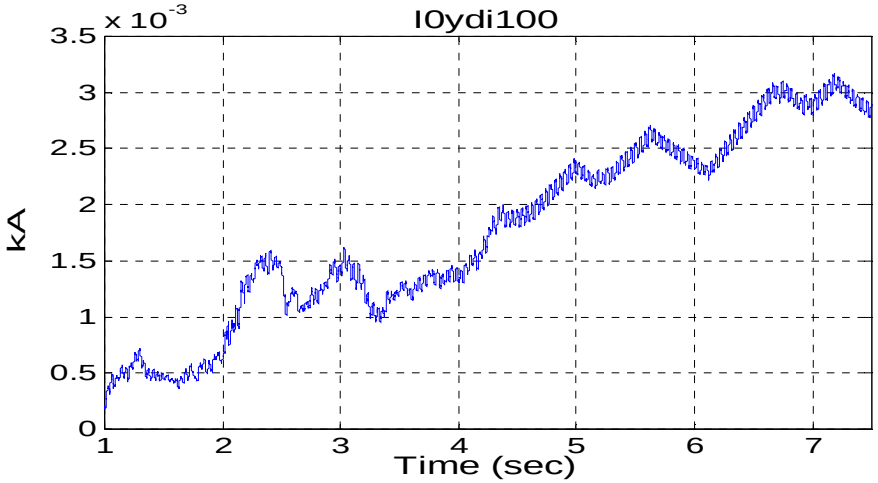


Figure A9.8: The 100 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

Appendix 10

Additional simulation results of the case described in Section 7.5

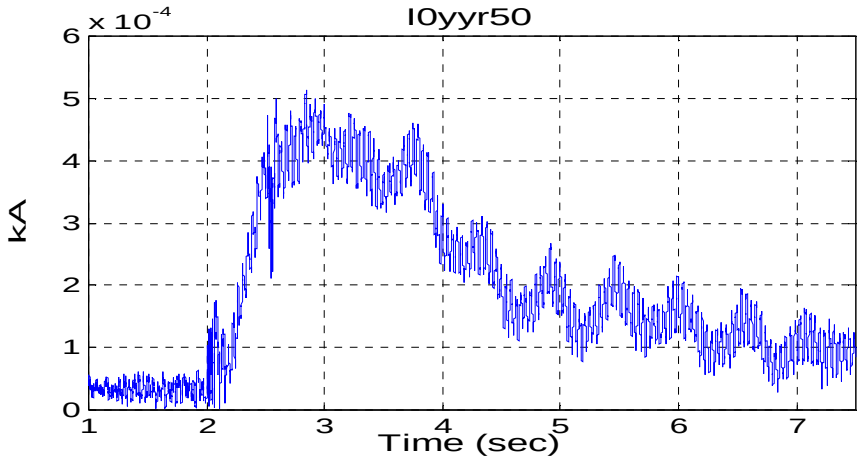


Figure A10.1: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

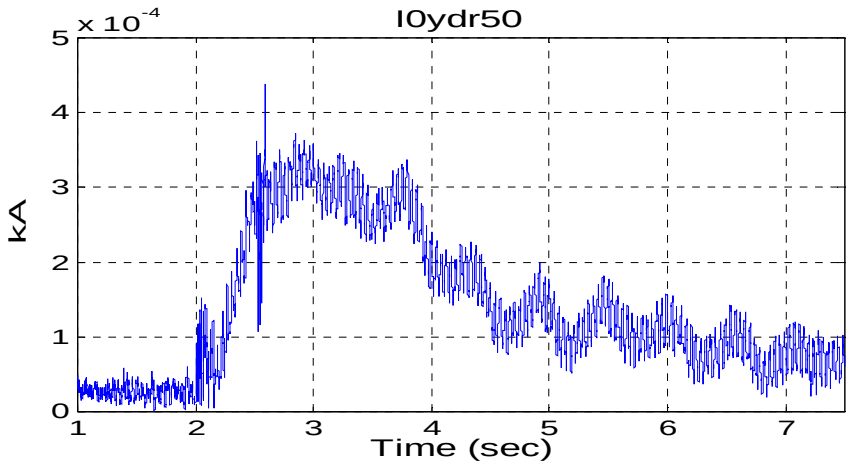


Figure A10.2: The 50 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

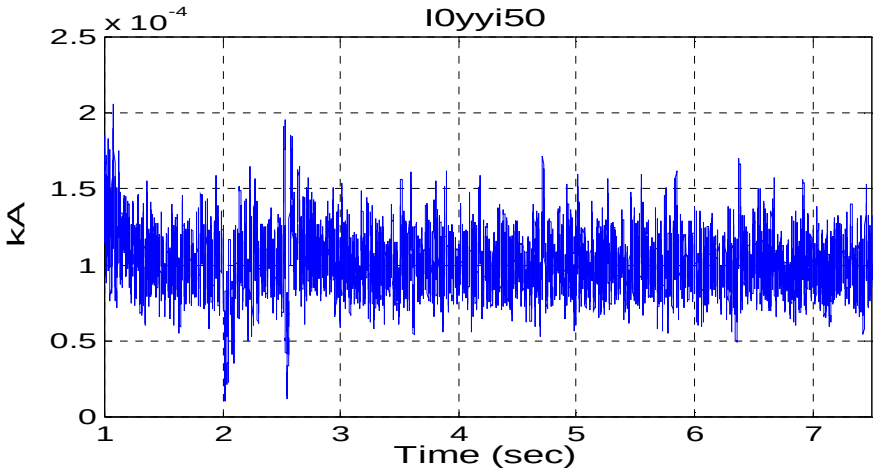


Figure A10.3: The 50 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

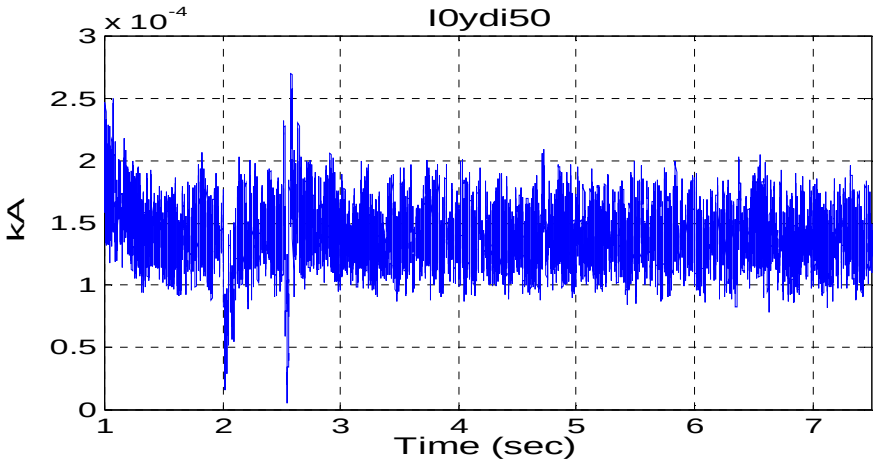


Figure A10.4: The 50 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

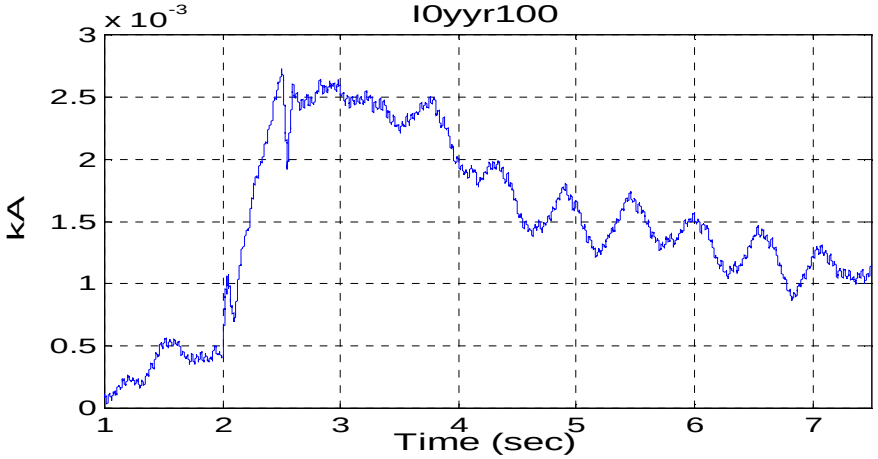


Figure A10.5: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled rectifier transformer.

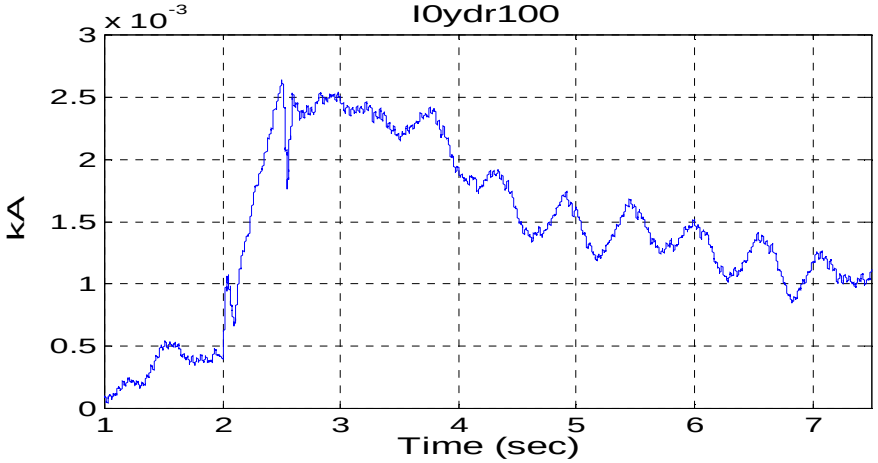


Figure A10.6: The 100 Hz component of the current in the neutral conductor of the Y-D coupled rectifier transformer.

URN:NBN:no-2111

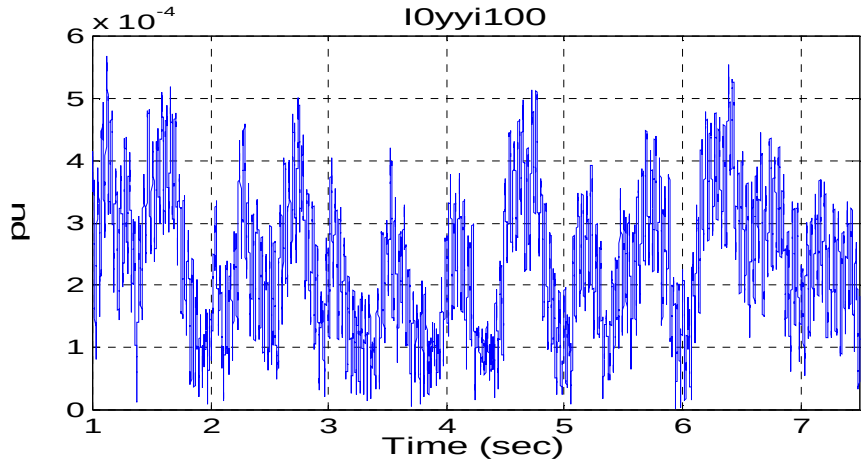


Figure A10.7: The 100 Hz component of the current in the neutral conductor of the Y-Y coupled inverter transformer.

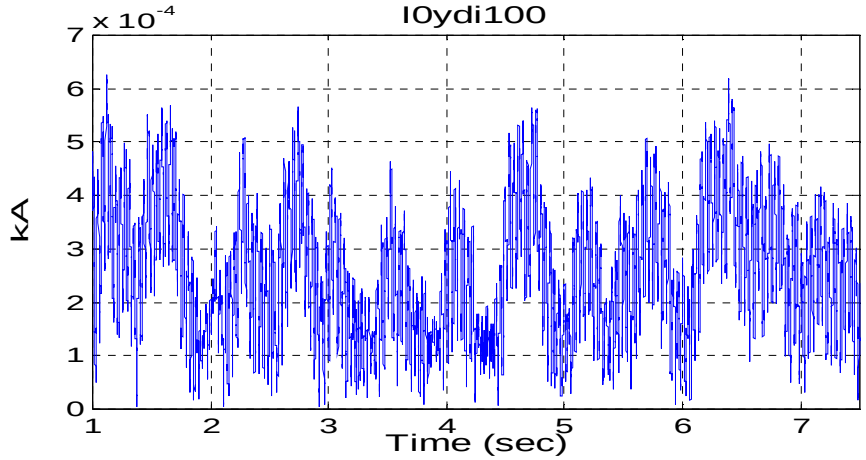


Figure A10.8: The 100 Hz component of the current in the neutral conductor of the Y-D coupled inverter transformer.

Appendix 11

Technical report at NEF (Norwegian electro technical union) technical meeting 2000

TILTAK MOT 2.HARMONISK USTABILITET I HVDC-ANLEGG.

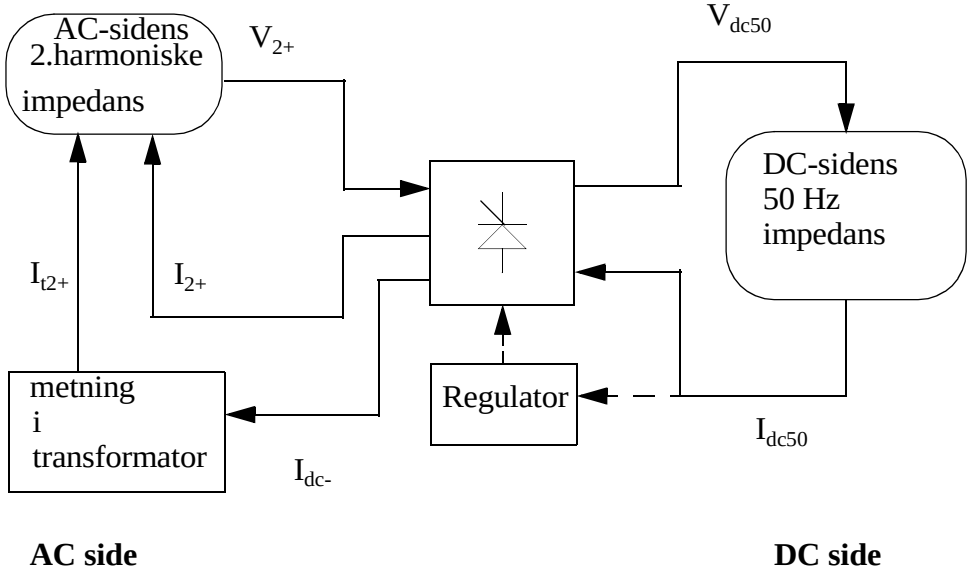
Ian Norheim og Tore Undeland, Inst. for Elkraftteknikk ved NTNU

SAMMENDRAG

2.harmonisk ustabilitet er sannsynlig årsak til noen problemer ved drift av HVDC-systemer [1]. Fenomenet er kompleks og oppstår ved samspill mellom flere ulike hendelser [2]. Omformerenes reguleringssystem, kobling mellom harmoniske på AC- og DC-siden av en HVDC-omformer, resonanser i nettet både på AC- og DC-siden, og metning av omformertransformatorene er faktorer som har betydelig innvirkning på fenomenet. Konsekvenser av 2.harmonisk ustabilitet kan være linjeutkobling pga. store nullsystem strømmer som trigger vern, eller overoppheting av komponenter i kraftsystemet som følge av harmoniske generert av metning i omformertransformatorene [3], [4]. I nærværende rapport er det gitt en forenklet teoretisk beskrivelse av 2.harmonisk ustabilitet. Videre er simuleringer av fenomenet og tiltak mot det beskrevet. Simuleringsprogrammet PSCAD/EMTDC versjon 3 ble benyttet til å utføre disse simuleringene.

1 INTRODUKSJON

2.harmonisk ustabilitet et samspill mellom flere ulike hendelser ved drift av et HVDC-anlegg. Blokkskjematisk kan fenomenet beskrives som på figur 1.



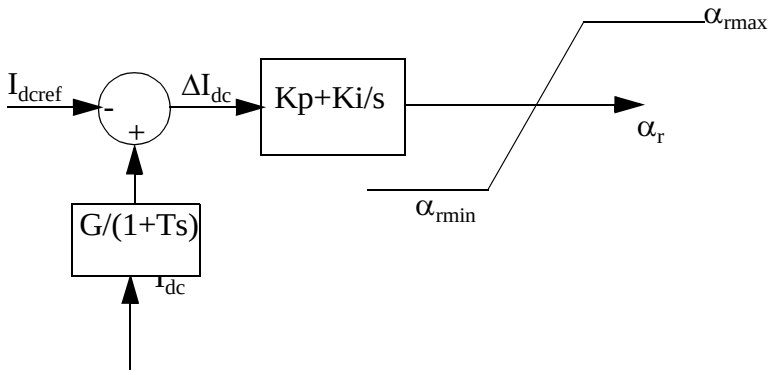
Figur 1.1: Mekanismer som trigger 2.harmonisk ustabilitet

Dersom en liten 2.harmonisk spenning V_{2+} i det positive system finnes på AC-siden av omformeren vil det pga. av svitsjingen oppstå en grunnharmonisk spenning V_{dc50} på DC-siden av omformeren. Gjennom DC-sidens 50 Hz impedans vil det da flyte en grunnharmonisk strøm I_{dc50}. Jo lavere DC-sidens impedans er ved 50 Hz , jo større vil I_{dc50} være. Dvs. at en

serieresonans nær 50 Hz mellom DC-sidens kapasitans mot jord og likeretterens/vekselretterens glattespole vil føre til en relativt høy I_{dc50}.

Pga. omformerens svitsjing vil det nå gå en 2.harmonisk strøm I_{2+} i det positive systemet og en DC-strøm I_{dc-} i det negative system. I_{dc-} sies å være i det negative system da summen av DC-strømmene i de tre fasene på AC-siden er 0, og faserekkefølgen på disse strømmene tilsvarer en faserekkefølge som i det negative system med frekvens lik 0. Disse DC-strømmene vil føre til at omformertransformatorene blir skeivmagnetisert slik at metningsnivået i hver fase er forskjellig. Dette genererer harmoniske av alle orden i både det positive, det negative, og i nullsystemet [4]. Blant disse harmoniske er en komponent i det positive system av orden 2. Dette fører til at to strømkomponenter av orden 2 i det positive system vil bidra til den 2.harmoniske spenningen V_{2+}. I_{2+} oppstår pga. koblingen mellom harmoniske på AC- og DC-siden av omformeren, og I_{t2+} oppstår pga. skeivmagnetiseringen av omformertransformatorene.

V_{2+} vil være avhengig av impedansen disse strømmene møter. Dersom denne har parallellresonans nær 2.harmonisk frekvens vil en liten verdi av summen av I_{2+} og I_{t2+} gi en relativt høy verdi av V_{2+}, og dermed øker sannsynligheten for at V_{2+} skal forsterke seg ved et omløp av blokkskjemaet på figur 1. En faktor som kommer inn ved neste omløp er at omformerenes reguleringssystem påvirker V_{dc50} når det flyter en 50 Hz strøm på DC-siden. Dette er forklart nedenfor for likeretterens strømregulator.

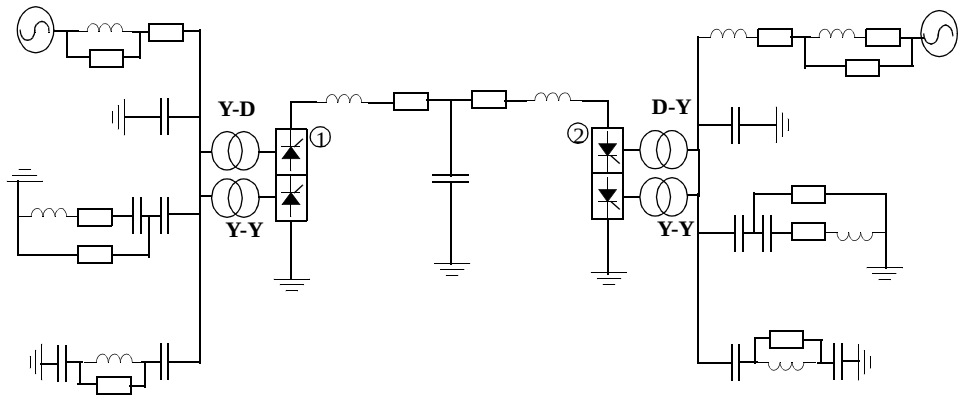


Figur 1.2: Strømregulator til en likeretter

Den målte verdien av strømmen I_{dc} på DC-siden av likeretteren, lavpassfiltreres slik at høyere ordens harmoniske ikke skal påvirke likeretterens tennvinkel α_r. Imidlertid må knekkfrekvensen til lavpassfilteret ikke velges for lav slik at lastendringer og settpunktsendringer blir håndtert tilfredstillende. Dette fører til at en 50 Hz komponent i I_{dc} vil føre til en 50 Hz variasjon i α_r. I følge [2] vil dette gi en 50 Hz komponent i V_{dc}. Under uheldige omstendigheter fører dette til at likeretterens strømregulator er med å forsterke V_{dc50}. Faktisk er det svært uvanlig at 2.harmonisk ustabilitet utvikler seg uten at HVDC-systemets reguleringssystem er involvert [2]. Det er derfor naturlig å utvikle tiltak i reguleringssytemet for å unngå utvikling av 2.harmonisk ustabilitet.

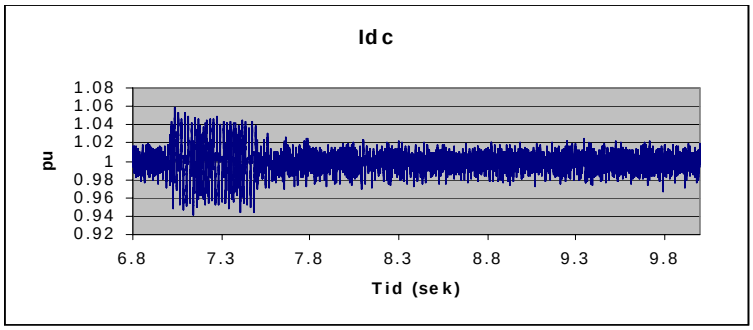
Dersom 2.harmonisk ustabilitet får utvikle seg vil det oppstå store strømmer i nullsystemet pga. den økende skeivmagnetiseringen av omformertransformatorene. Dette vil utløse vern og føre til linjeutkobling og dermed økonomisk tap. Eventuelt kan det skje at fenomenet utvikler seg til en viss grad, men at det er nok demping i det totale system til at det begrenses. Likevel kan tilleggsbidraget av harmoniske føre til utkobling pga. oppheting av filter, transformatorer osv.

2 SIMULERING AV 2.HARMONISK USTABILITET



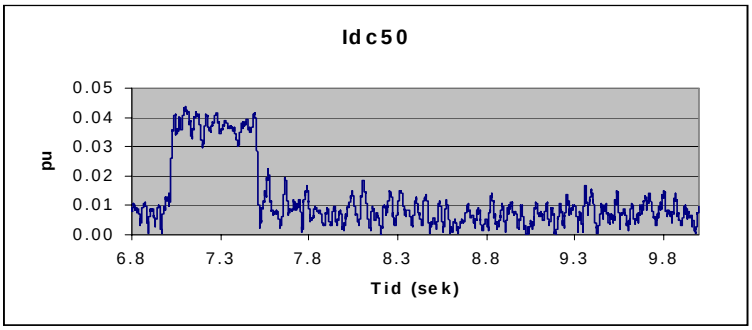
Figur 2.1: Enlinjeskjema av den elektriske kretsen av CIGRE HVDC benchmark modellen

Simuleringene som er beskrevet nedenfor er utført i PSCAD/EMTDC versjon 3 [5]. Grunnlag for simuleringene er CIGRE HVDC benchmark modellen [6]. En 3^0, 50 Hz forstyrrelse i likeretterens tennvinkel ble lagt inn ved stabil merkedrift etter 7 sekund. Denne ble fjernet etter 7.5 sekund. Som figur 4 og 5 viser er det ingen ustabilitet som følge av denne forstyrrelsen. Opprinnelig CIGRE modell er modifisert slik at den er tilpasset lavere reaktiv kompensering i AC-nettet på likerettersiden (svakere nett), annerledes men ikke urimelig magnetiseringskarakteristikk for likerettertransformatorene, serieresonans nær 50 Hz i DC-sidens impedans, og litt høyere forsterkning av 50 Hz komponenter gjennom likeretterens reguleringssystem [2]. Merkeytelsen for HVDC-linken ble imidlertid ikke endret. Ved stabil merkedrift av den modifiserte CIGRE modellen ble det etter 7 sekunder lagt inn en 2^0, 50 Hz forstyrrelse, med samme fase som forstyrrelsen nevnt over, i likeretterens tennvinkel. Denne ble fjernet etter 7.5 sekunder. Det lyktes da å få frem 2.harmonisk ustabilitet. Dette ses på figur 7 der 50 Hz komponenten til DC-strømmen som likeretteren mater inn i DC-nettverket blir svært stor. DC-strømmen på figur 6 er selvsagt helt uakseptabel og ville ført til utkobling av HVDC-systemet.

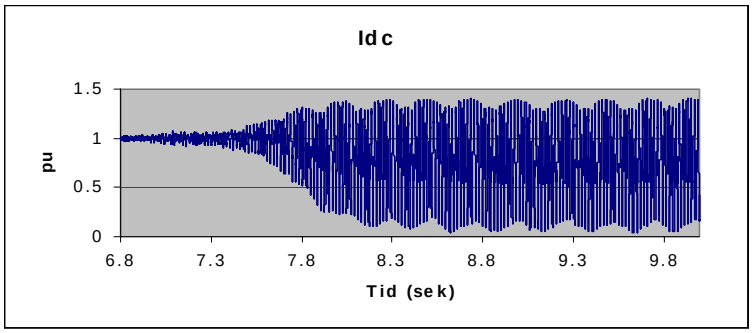


Figur 2.2: Strømmen på DC-siden av likeretteren når CIGRE modellen benyttes i simuleringen.

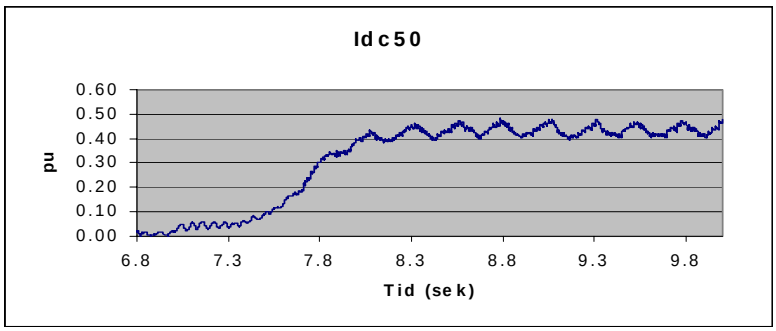
URN:NBN:no-2111



Figur 2.3: 50 Hz komponenten av strømmen på figur 4 (Funnet ved FFT av I_{dc})



Figur 2.4: Strømmen på DC-siden av likeretteren når den modifiserte CIGRE modellen benyttes i simuleringen.



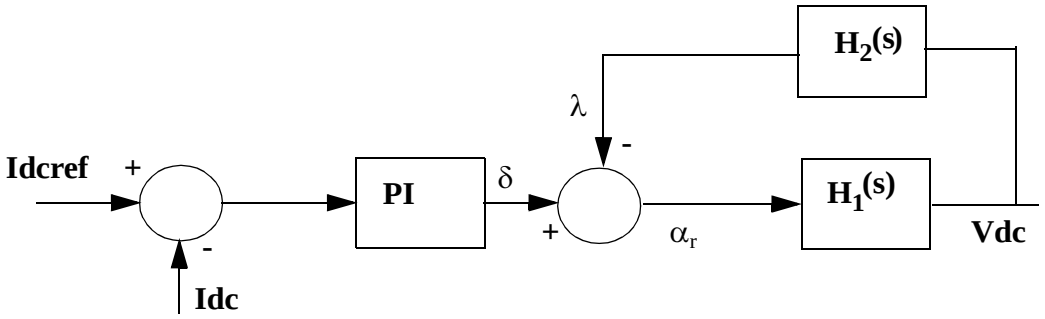
Figur 2.5: 50 Hz komponenten av strømmen på figur 6 (Funnet ved FFT av I_{dc})

3 TILTAK MOT 2.HARMONISK USTABILITET

Som nevnt tidligere er en modifikasjon av HVDC-systemets reguleringssystem et naturlig valg for å undertrykke 2.harmonisk ustabilitet da det er usannsynlig at fenomenet skal oppstå uten reguleringssystemets innvirkning. Dette betyr ikke at det ikke kan brukes andre metoder for å forhindre 2.harmonisk ustabilitet, men disse metodene vil i mange tilfeller utgjøre en mye større kostnad enn en modifikasjon av reguleringssystemet. Derfor velges det kun å betrakte modifikasjoner på HVDC-systemets reguleringssystem i nærværende rapport. De foreslåtte modifikasjoners virkning demonstreres på den modifiserte CIGRE benchmark modellen beskrevet tidligere.

URN:NBN:no-2111

3.1 Metode 1 : Dempetilsats



Figur 3.1: Likeretterens reguleringssystem der dempetilsats er inkludert

Bruken av dempetilsats går ut på å eliminere den grunnharmoniske svingningen i tennvinkelen. Ideen er hentet fra [7], men i nærværende rapport er dempetilsatsen forklart mer grundig. For å få utviklet dempetilsatsen trenger man å finne transferfunksjonen fra α_r til spenningen V_{dc} over likeretteren ved 50 Hz. Da det er ønskelig at dempetilsatsen bare skal være virksom ved 50 Hz er det viktig at den har en smal båndbredde (ellers vil den kunne uønsket påvirke driftstilstanden av HVDC-omformerne). Anta at transferfunksjonen $H_1(s)$ mellom α_r og V_{dc} ved 50 Hz er gitt av:

$$H_1(j2\pi \cdot 50) = K1 \cdot e^{j\varphi} \tag{1}$$

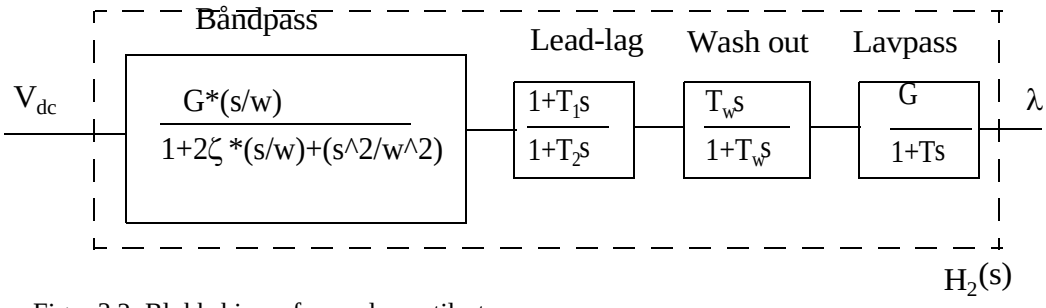
Lar $H_2(s)$ ved 50 Hz være gitt av:

$$H_2(j2\pi \cdot 50) = K2 \cdot e^{-j\varphi} \tag{2}$$

Transferfunsjonen $\frac{V_{dc}}{\delta}(s)$ ved 50 Hz blir da:

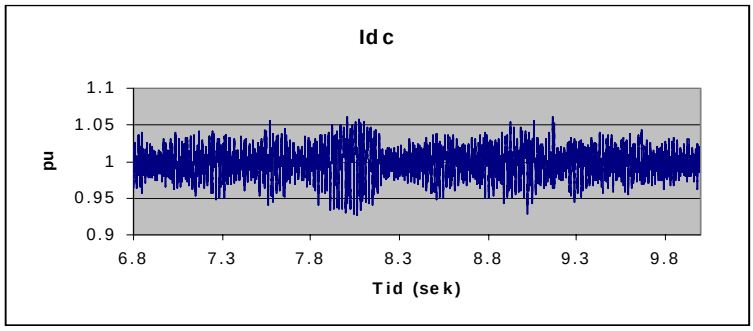
$$\frac{V_{dc}}{\delta}(j2\pi \cdot 50) = \frac{H_1(j2\pi \cdot 50)}{1 + H_1(j2\pi \cdot 50) \cdot H_2(j2\pi \cdot 50)} = \frac{K_1 e^{j\varphi}}{1 + K_1 K_2} \tag{3}$$

Ser at K_2 kan velges slik at 50 Hz variasjonen i δ gir en lav 50 Hz variasjon i V_{dc}. Dempetilsatsen fører altså til at reguleringssystemets påvirkning av 50 Hz variasjonen i V_{dc} reduseres. Dermed reduseres også sannsynligheten for at 2.harmonisk ustabilitet skal oppstå. Imidlertid vil et for høyt valg av K_2 føre til at V_{dc} påvirker α_r gjennom dempetilsatsen ved uønskede frekvenser. Dempetilsatsen kan ha et blokkskjema som på figur 9.

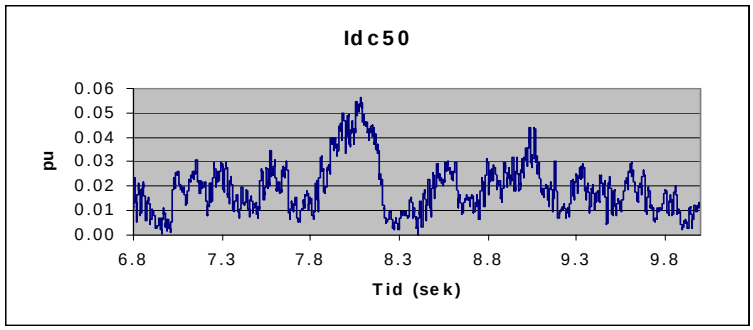


Figur 3.2: Blokkskjema for en dempetilsats

Dempetilsatsen forsterker signaler med frekvenser i et smalt bånd rundt 50 Hz og undertrykker signaler som har frekvenser utenfor dette båndet. En dempetilsats som beskrevet over ble utarbeidet for å undertrykke den harmoniske ustabilitet vist i eksempelet med den modifiserte CIGRE modellen. Dempetilsatsen ble satt inn i modellen og gav følgende resultat for samme forstyrrelse som førte til 2.harmonisk ustabilitet.



Figur 3.3: Strømmen på DC-siden av likeretteren når den modifiserte CIGRE modellen med dempetilsats benyttes i simuleringen.

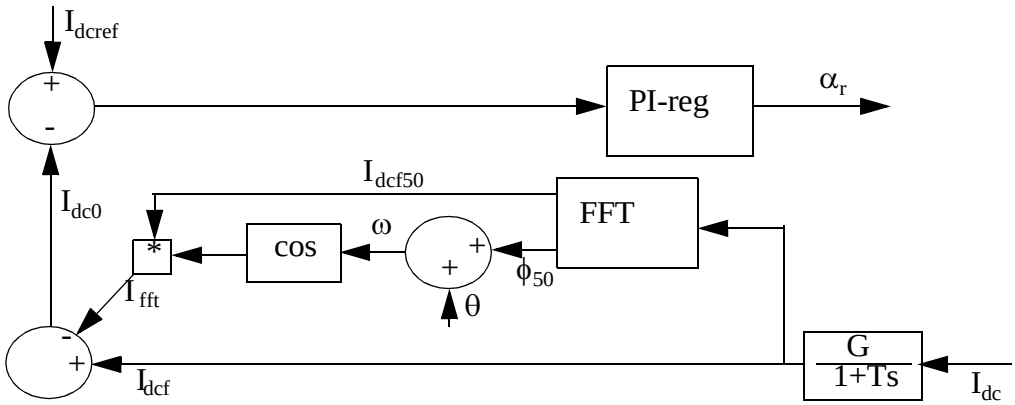


Figur 3.4: 50 Hz komponenten av strømmen på figur 10 (Funnet ved FFT av I_{dc}).

Dempetilsatsen forhindrer effektivt 2.harmonisk ustabilitet.

3.2 Metode 2: Fast Fourier Transform (FFT)

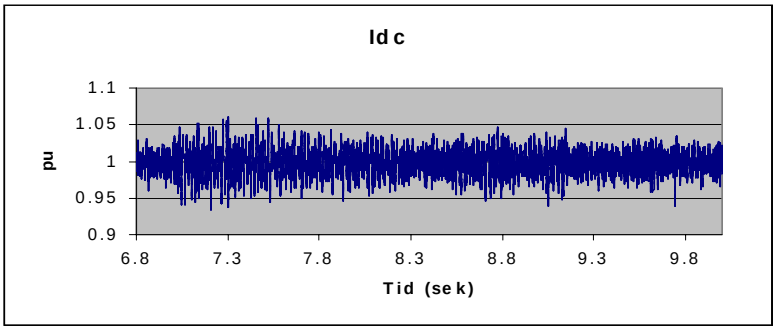
FFT [8], [9] gjør det mulig å bestemme amplituder og fasevinkler til harmoniske komponenter av et signal med en gitt grunnharmonisk frekvens. For å få dette til må signalet først samples (jo høyere harmonisk komponent som ønskes beregnet jo flere samplinger pr. grunnharmoinsk periode må gjennomføres), deretter beregner en mikroprosessor amplituder og fasevinkler til de harmoniske komponentene. Fasevinklene beregnes i forhold til en cosinus funksjon som starter ved tid t=0, har grunnharmonisk frekvens, og vinkel θ. FFT kan være et svært nyttig instrument til å forebygge 2.harmonisk ustabilitet. I dempetilsatsen beskrevet tidligere kunne båndpassfilteret blitt byttet ut med et FFT-filter som kun lot 50 Hz slippe gjennom. I nærværende rapport ses imidlertid på en annerledes anvendelse av et FFT-filter.



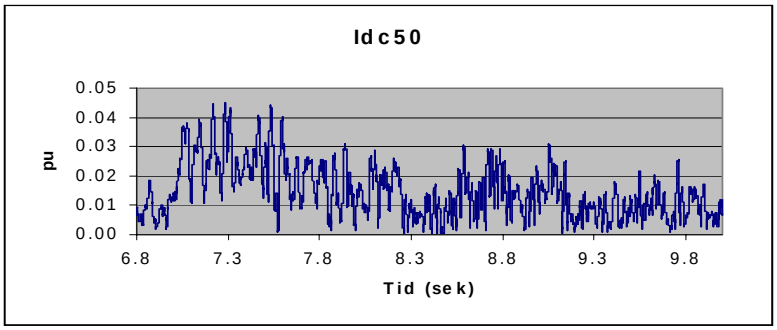
Figur 3.5: Likeretterens reguleringssystem der et Fourier filter er inkludert

Lavpassfilteret på figur 12 hindrer de karakteristiske harmoniske i DC-strømmen (harmoniske av orden 12,24,36,....) å påvirke tennvinkelen α_r. Som nevnt tidligere må ikke knekkfrekvensen på dette filteret velges for lavt. Dette fører til at en betydelig 50 Hz komponent finnes i I_{dcf}. Utsignalet I_{fft} fra Fourier filteret er en tilnærmelse av denne. Ved å trekke I_{fft} fra I_{dcf} vil I_{dc0} nesten ikke ha noe 50 Hz innhold. Dermed blir 50 Hz komponenten i α_r liten og reguleringssystemets ugunstige innflytelse på 2.harmonisk ustabilitet er nesten fjernet.

Et FFT filter som beskrevet over ble benyttet for å forhindre at 2.harmonisk ustabilitet utviklet seg i eksempelet med den modifiserte CIGRE modellen. Forsterkningen til dette filteret ble redusert til $I_{dcf50}/(\sqrt{2})$ da variasjonen i fasevinkelen til 50 Hz komponenten av I_{dcf} skapte interharmoniske som førte til ustabilitet ved bruk av I_{dcf50} som forsterkning. Simuleringsresultater ved bruk av FFT-filteret i den modifiserte CIGRE modellen er vist på figur 13 og 14. Forstyrrelsen er den samme som i eksempelet der 2.harmonisk ustabilitet utviklet seg.



Figur 3.6: Strømmen på DC-siden av likeretteren når den modifiserte CIGRE modellen med FFT-filter benyttes i simuleringen.



Figur 3.7: 50 Hz komponenten av strømmen på figur 13 (Funnet ved FFT av I_{dc}).

FFT-filteret undertrykker 2.harmonisk ustabilitet effektivt.

4 KONKLUSJONER

2.harmonisk ustabilitet er mulig å forhindre ved ulike inngrep i HVDC-systemets reguleringssytem. Imidlertid kan det oppstå andre uønskede harmoniske fenomen ved å gjøre disse inngrepene. Ved bruk av dempetilsatsen kan uønskede frekvenser i likeretterens DC-spenning opprettholdes og forsterkes. FFT-filtrering av DC-strømmen likeretteren injiserer i DC-nettet kan føre til interharmoniske som et resultat av at DC-strømmens fasevinkel ved 50 Hz kan variere. I hvert tilfelle er det derfor viktig å vurdere hvilke tiltak i reguleringssystemet til HVDC-overføringen som er tilstrekkelig for å oppnå tilfredstillende reaksjon mot 2.harmonisk ustabilitet.

LITTERATURREFERANSER

[1] Chen, Wood, Arrilaga
A DIRECT FREQUENCY DOMAIN INVESTIGATION OF THE PROPERTIES OF CONVERTER TRANSFORMER CORE SAT-URATION INSTABILITY.
AC and DC Power Transmission 1996. Conference Publication.

[2] J.Arrillaga, B.Smith
AC-DC power system analysis.
The Institution of Electrical Engineers, London, UK, 1998

[3] P.O. Eide, R. Fredheim, B. Bergdahl, L-E Juhlin, J. Spånberg
Simulation of harmonic problems in the Kristiansand HVDC-station
PSCC 1999- 13th Power Systems Computation Conference Proceedings Volume 2

[4] J. Arrillaga
High Voltage Direct Current Transmission
Pretince-Hall, Inc, 1990

[5] Manitoba HVDC Research Centre
PSCAD EMTDC Version 3 Getting Started Manual, 1998

[6] CIGRE WG 14-02
First benchmark model for HVdc control studies
Electra, April 1991, (135), pp 55-75

[7] MANITOBA HVDC RESEARCH CENTRE
HARMONIC EFFECTS ON HVDC CONTROL AND PERFOR-
MANCE. MAIN REPORT, FEBRUARY 1994

[8] EMTDC manual som følger med PSCAD/EMTDC versjon 3

[9] Electrotek Concepts, Inc., Knoxville, Tennessee, USA
Evaluation of Active Filter Design and Performance Using a Detailed EMTP Model,
1994-1995