Distributed Generation
– Power Electronic Converters, Communication and Control

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Abstract

This thesis tries to explain the changes in the control of power electronic converters that are possible by the use of communication. Many of the renewable energy sources such as photovoltaic panels are geographically dispersed. The power rating per generator is therefore typically low. If this kind of energy source should dominate an electrical grid, the number of generators must be high. There should also be means of controlling this large number of generators simultaneously and safely. The cost of safe communication may be too high compared to the power contribution of a single generator. The Internet offers a low-cost solution, but it cannot guarantee real-time properties. Similarly to the Internet itself, it is shown how communication errors can be detected and handled in a safe manner by the end-system, in this case the generator. The generator can detect a communication timeout, and change control algorithms in order to guard itself and the connected electricity grid. When necessary, it can also disconnect and work as a local standalone power supply. In order to be able to supply all kinds of loads, the generator (in this case an inverter) is primarily voltage controlled. This results in challenges concerning current distortion. The use of feed-forward for cancellation of common grid voltage harmonics is discussed, simulated and measured. An anti-islanding algorithm for voltage controlled inverters is also developed, simulated and measured in this thesis. A DC/DC-converter for optimized connection of a photovoltaic panel is built, exploiting the photovoltaic panel properties to reduce the size and the losses significantly. Although most contributions are connected to details and parts of the system, the interactions between communication and control are emphasized.

Acknowledgements

I think my parents can agree that already from childhood I was busy testing out what I have learned in practice. Both chemistry and electronics were interesting fields. By giving me an electronics set instead of a chemistry set, I guess they hoped to avoid explosions of any kind. Usually I was making less harmful projects, like finding out how to power toy cars by using photovoltaic panels.

It was in the lectures of Professor Roy Nilsen at NTNU that I was first introduced to power electronics and drives. This opened up a new world to me, and I understood that I just had to learn about the programming of microcontrollers and digital signal processors. The four years I have spent on this PhD have been very interesting and educational. I would like to thank Professor Tore Undeland, NTNU for informing me about this PhD scholarship and for being my supervisor the first months. Thanks to Professor Lars Norum, NTNU for being my main supervisor and for helpful support after I was accepted as a PhD student. Help from other PhD students is not only motivating but also important. I will therefore like to thank William Gullviks company ActiveDSP for sharing the DSPcomm program with fellow PhD students free of charge, and for giving a starting point DSP code. Special thanks go to Tore Skjellnes, Pål Andreassen and Guiseppe Guidi for long and helpful discussions. I would also like to thank the Electa group at K.U. Leuven for helpful discussions. I am very grateful for the comments and corrections given by post.doc. Marta Molinas and Professor Tore Undeland.

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1 Introduction

Fossil-fueled thermal electric power plants emit large amounts of CO_2 that affect the climate. One possible solution to reduce CO_2-emissions is substituting fossil fueled plants with renewable energy such as biomass, solar, wind and/or hydropower. Such renewable energy sources are geographically dispersed, and therefore do not have an economy of scale compared to thermal plants. For example, photovoltaic panels can be used as a building cladding, where they do not occupy valuable land area. The surface of one building is however limited, and thus the power of one such generator is small. In addition, often such a generator is close to the consumer. It is thus possible to reduce the capacity of the transmission lines because there is less electricity to transport. The owner of such a generator is often also a power consumer. The owner then avoids any kWh-taxation of the electricity that is internally produced and consumed. Private ownership may therefore encourage demand-side management. For some consumers improving the security of supply is more important than the kWh-cost. Locally owned generators may give a positive contribution in this respect, assuming suitable control is applied. Locally owned generators also encourage generators with little local environmental impact.

Distributed Generation (DG) can be defined as an electric power source connected directly to the distribution network or even on the customer side of the meter [1, 2]. These are often small-scale renewable energy sources, such as photovoltaic panels, biomass or wind turbines. The localization of the DGs can be used beneficially for both the consumer and the producer. Communication and power electronics are the enabling technologies that are necessary to realize many of the possible benefits of DG [3]. A possible communication setup is shown in Figure 1.
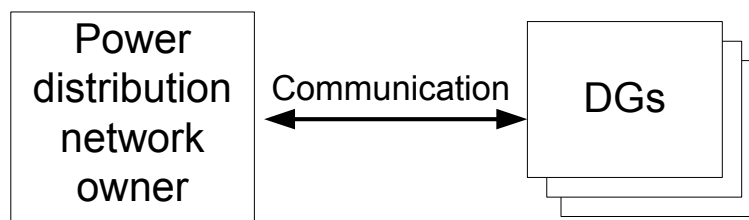
Figure 1: Communication for controlling a large number of Distributed Generation units (DGs).

The network owner and the customer must have a mutual agreement concerning the grid connection [4]. Both parties can be energy producers and energy consumers, depending on the local energy available. Internet communication offers the network owner a low-cost solution to control the local energy production in a way that is beneficial to both parties.

Optimization of the energy production is one of the purposes of information exchange in power systems. It gives the DG owner the possibility to produce energy in the most optimal way. One example is the electricity cost, which varies with time. When using biomass-fired DG only during periods with high energy cost, a DG owner can increase profit margins with regard to fuel cost. The network owner can also use the DGs for peak shaving. Grid reinforcements may be avoided if local energy sources are installed, and if there are communication systems for power management and control.

The internal system of a DG must be designed to meet new requirements introduced by the use of communication. The internal functions range from energy source optimization, to energy storage control, as well as the grid connection. Local energy sources can be divided in dispatchable sources (such as biomass and pump-storage hydropower) and non-dispatchable sources (such as photovoltaic panels and wind power). The latter should be run at full power whenever possible because the fuel cost is zero.

The existing grid requirements prevent the DGs from providing power locally during grid failures. If the grid requirements were modified, the main grid could be separated into smaller islands of active local grids to protect against failures [5]. These could then supply the local grid, and give customers a more reliable power supply compared to the alternative of no local energy sources. The small islands of possibly isolated grids must, however, be able to balance production and consumption of power. This is best done by having some dispatchable energy sources or energy storage. These can then guarantee an adequate amount of power when needed.

An important feature of a power supply system is fault tolerance. Possible fault situations in addition to grid failures are communication failures, which should also be handled in a controlled way. This requires the connected converters functioning safely without communication. Optimization may be lost, but neither people nor machines should be harmed. The DG should also tolerate grid failures and thus avoid interrupting the power supply of the nearest critical load.

The primary energy source can be optimized using digital control. Photovoltaic panels are controlled using Maximum Power Point Tracking (MPPT). Similar methods can be applied for optimizing the speed of wind turbines and even small hydropower turbines. When combined with high efficiency converters, the energy output can be improved. Co-design of the control and the DC/DC-converter hardware may improve the overall efficiency and reduce its size. A schematic representation of the converters in a typical DG with power electronic converters is shown in Figure 2.
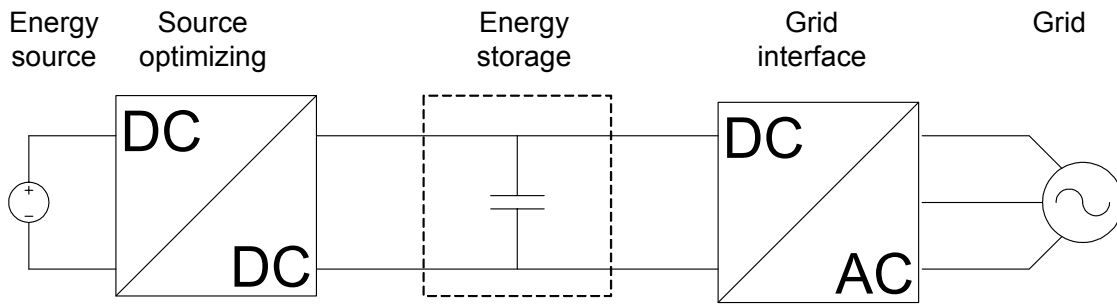
Figure 2: A DG including two power electronic converters with energy storage in between.

A system for grid connection of small-scale renewable energy sources must meet certain requirements from the customer and the network owner. The customer wants an efficient and reliable system at low cost. The network owner has requirements regarding harmonic pollution of the grid, as well as safety measures for equipment and personnel. Requirements vary according to the location of the DGs, even within Norway [4]. The network owner may put too strict grid connection requirements on the local DG owner. A network owner may then effectively block DGs.

The possibility to remotely control various DGs is an improvement. Control of any number of DGs can be achieved using communication. There are various communication possibilities, but using an existing infrastructure supporting point-to-point communication is beneficial. The specific cost of communication per kWh electricity produced must be kept low. This excludes any custom-made infrastructure which may be used in larger generating facilities. The Internet offers possibilities for relatively simple integration of different services into an energy management system. The point-to-point communication offers possibilities of distributed systems. This can share out the processing and communication load within the system, and therefore not overload the network owner. Second, the integration with other information systems, such as the electricity cost, enables more economic electricity production. Failure and status information can be given through a number of channels, ranging from email to real-time protocols.

Reliability is a major concern for an increasing number of customers. Uninterruptible Power Supplies (UPS) are commonly used to avoid undesirable power outages in businesses ranging from hospitals to small offices. Smaller companies relying on computers typically have an UPS to avoid down-time due to grid power outages. A DG can meet the power deficiency of local loads in case of grid failure. This requires, however, voltage control and a means of isolating the critical loads from the grid.

1.1 Contributions

A DG system using control based on Internet communication, digital controllers and a new DC/DC-converter for photovoltaic panels is presented. All these three system components interact, thus it is undesirable to design the parts independently. A laboratory setup has been built, in order to investigate design issues and to test the performance of the system.

An Internet communication system for DG is presented, which has not yet been applied for island detection for DG. The communication may fail, and safe control algorithms make the system soft real-time. If real-time communication errors do not lead to dangerous situations, a system can be called soft real-time.

The soft real-time control can give grid-connected DGs new possibilities to support the local voltage. This can be considered the opposite of the anti-islanding algorithms applied to most of today's DGs. Three different control algorithms, all based on a voltage-controlled AC/DC-converter (inverter), are demonstrated. Basing all these control algorithms on voltage control, the transition between connection states can be done smoothly without interrupting the power to a local critical load. Feed-forward for decoupling of common grid voltage harmonics is tested. An anti-islanding algorithm for a voltage controlled inverter is presented. Such anti-islanding control has not been published by others.

Photovoltaic (PV) panel connected DC/DC-converters is discussed. A known concept is applied to a flyback converter. The concept is to limit the DC/DC-converter voltage control range [6-8]. The DC/DC-converter is then only capable of converting the expected voltage variations during normal operation. It is typically ¼ of the nominal voltage. Given suitable topology, the transistors can switch only a fraction of the voltage or the current from the PV panel. This can give a significant reduction of the size and the losses of the DC/DC-converter, compared to a standard DC/DC-converter. The flyback converter differs from previously published work by being bi-directional, meaning it can step the PV panel voltage both up and down.

A DG system has been implemented in the laboratory. It consists of a controllable DC source representing a PV panel. This feeds energy to a DC/DC-converter. The energy is fed to the DC-link capacitance of a 3-phase inverter, acting as the energy storage. The inverter is connected to the load and/or the electricity grid through an LCL-filter and an electromechanical contactor. A testbench has been developed for testing of islanding detection time and harmonics.

1.2 Outline of the thesis

Chapter 2 describes the requirements of a grid-connected DG with communication. A laboratory setup is presented, which shows how such a system may look in the future. Use of communication may lead to changes the control, especially of the inverter. Some of these possible changes are presented.

Chapter 3 presents the energy source which is a photovoltaic panel. Normally a DC/DC-converter optimizes the photovoltaic panel power output. When there is excess power the control of the DC/DC-converter is important. This chapter presents the concept of limited range voltage control, applied to a flyback-based converter.

Chapter 4 deals with the modeling and simulation of the inverter. A model of the LCL-filter and the grid with some harmonics is presented. The model is the basis of a full state-space observer, which is discretized and designed. The response is simulated in Matlab Simulink, and some measurements are included.

Chapter 5 describes the controllers for the inverter and the DC/DC-converter. All control algorithms are based on a voltage controlled inverter. State feedback is used for damping the LCL-filter resonance. It is designed by pole matching of the feedback loop and a discretized equivalent circuit with virtual resistors. This is seen in relation with feed-forward for grid current THD improvement. A voltage support algorithm is presented, and it is compared to an anti-islanding algorithm developed.

Chapter 6 presents the software framework. Software is a significant part of the laboratory setup. Most of the work presented in this thesis is intended for use in control software.

Chapter 7 presents the system test results and compares this to simulations. The control algorithms are tested and simulated. Communication and grid events causing control algorithm transitions are verified.

Chapters 8, 9 and 10 summarize the discussion. Conclusions are drawn, and further work is suggested.

2 Detailed system description

A DG unit has been designed for the case of feeding power from a photovoltaic panel to a 3-phase electricity grid. The presented solution shows many of the design possibilities, problems and benefits of a DG using communication. The focus is thus on the interface between communication, digital control and power electronic converter design. The system can be divided into two main parts: The energy source using a DC/DC-converter for energy optimization, and the inverter for grid connection. The inverter has a filter as well as electromechanical contactor connected to the grid and a local load.

2.1 Energy optimization

The main purpose of the DC/DC-converter is optimizing the energy output from a photovoltaic (PV) panel, using Maximum Power Point Tracking (MPPT). The converter ensures that the PV panel is operating at optimal voltage under all insolation and temperature conditions. Good conversion efficiency is in this respect essential in order to obtain a net energy gain, minimizing losses. For non-dispatchable energy sources like photovoltaics, the power output can vary from zero power during night to full power during bright and sunny days. The converter must therefore have high efficiency in the whole power range. The European weighted efficiency also given in [9], gives a representative measure of which power levels a PV-connected converter operates:

$$\eta_{euro} = 0.03 \cdot \eta_5 + 0.06 \cdot \eta_{10} + 0.13 \cdot \eta_{20} + 0.1 \cdot \eta_{30} + 0.48 \cdot \eta_{50} + 0.2 \cdot \eta_{100} \qquad (2.1)$$

where η_x is the converter efficiency at x percent of the rated power. The DC/DC-converter control system is shown in Figure 3.
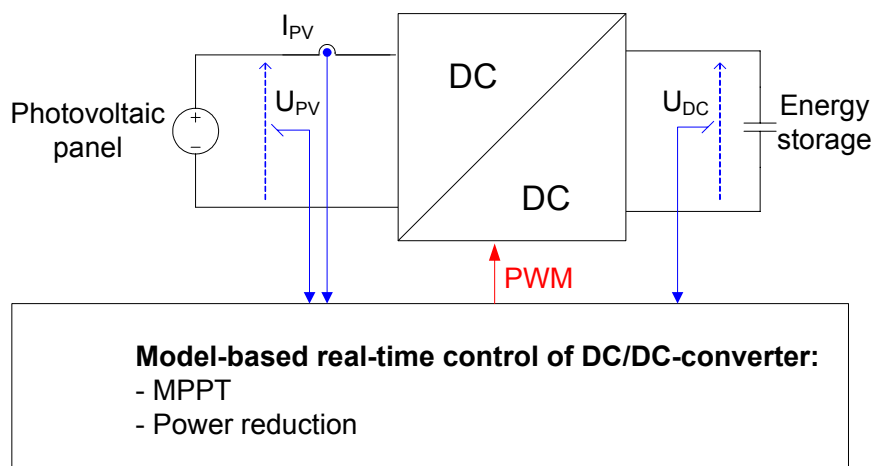
Figure 3: The DC/DC-converter control system.

The DC/DC-converter should be able to handle full energy storage. In this case it reduces the energy source power output. The voltage or current control necessary to reduce the power becomes the dimensioning criteria of the DC/DC-converter. It is thus necessary to control the DC/DC-converter in such a way that it can have a minimal size, and still supply as much energy as accepted by the energy storage. The photovoltaic panel is presented in detail in Chapter 3.

2.2 Grid connection and associated control algorithms

The grid connection circuit diagram is shown in Figure 4.
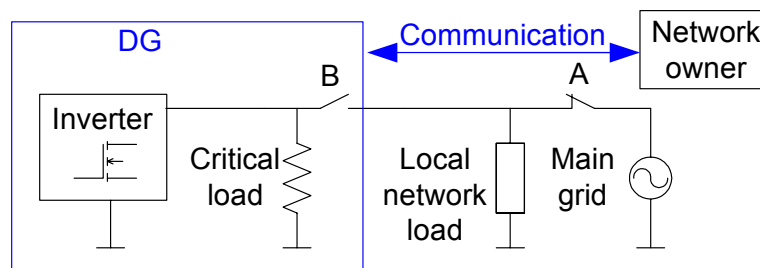
Figure 4: The grid connection circuit diagram.

The circuit breaker A is controlled by the network owner. The DG does not know the state of circuit breaker A explicitly. Circuit breaker B is controlled by the DG, but it may be overridden by the network owner when the communication is operational. There are three relevant connection states as defined in Table 1.

Table 1: The connection states described by circuit breaker states.

Connection state	Circuit breaker state	
	A	**B**
Grid connected	ON	ON
Islanding	OFF	ON
Standalone	Not relevant	OFF

In the grid connected state, all available active power should be fed to the grid. In islanding connection state, the local network may be supplied by the DG when possible and if allowed by the network owner. When standalone the DG has isolated itself from the network, but it can still supply the critical load. These three connection states are related to three different inverter control algorithms. There is not a one-to-one relationship between the connection states and the inverter control algorithms due to the unknown state of circuit breaker A. The inverter can be controlled in one of the three different control algorithms specified in Table 2.

Table 2: The inverter control algorithms in relation with circuit breaker and communication states.

Control algorithm	Circuit breaker state		Communication
	A	**B**	
Anti-islanding	Observable	ON	Not operational
Voltage support	Not observable	ON	Operational
UPS	Not relevant	OFF	Not relevant

Finding the state of circuit breaker A can be done by so-called anti-islanding control of the inverter. An anti-islanding algorithm tries to observe the circuit breaker A state, which is not possible in the voltage support control algorithm. The voltage support control algorithm may on the other hand enable islanding of a grid segment, or support a weak grid by reactive power compensation. The UPS control algorithm supplies a critical load when B is OFF. The three main control algorithms of the inverter are shown in Figure 5.
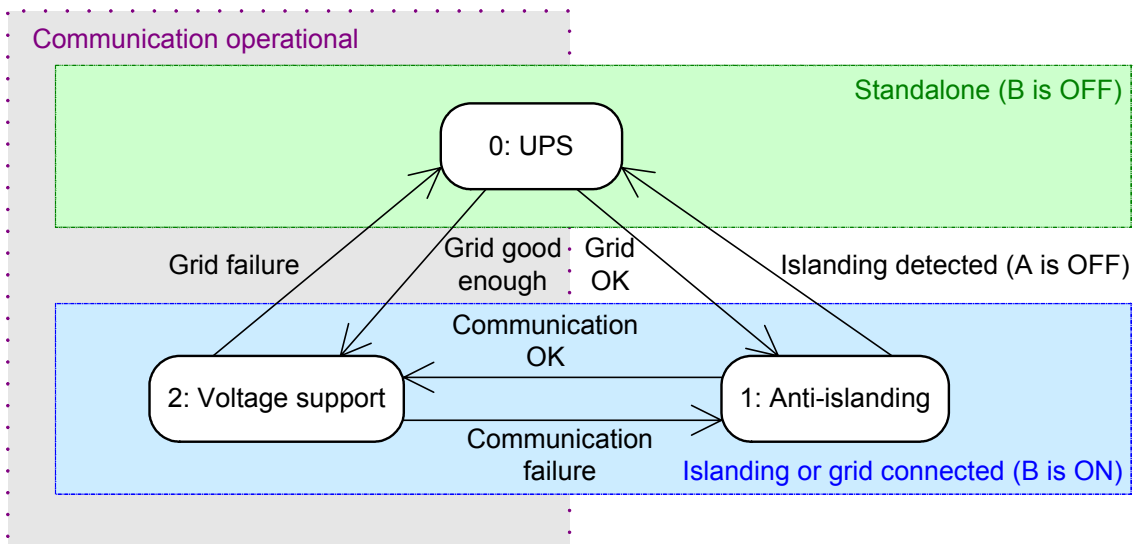
Figure 5: Inverter main control algorithms (rounded boxes) and connection states (squares).

The inverter controls the grid connection. The inverter must meet a number of, and occasionally even contradictory, requirements. One example is that the grid current should be sinusoidal as specified in [10, 11]. When the grid is disconnected the same inverter serves as a power supply for the critical load. This operation requires the voltage to be sinusoidal independently of the current drawn. Voltage control also simplifies transitions between connection states. All three algorithms are therefore based on a voltage controlled inverter, also shown in [12, 13]. The inverter connections are shown in Figure 6.
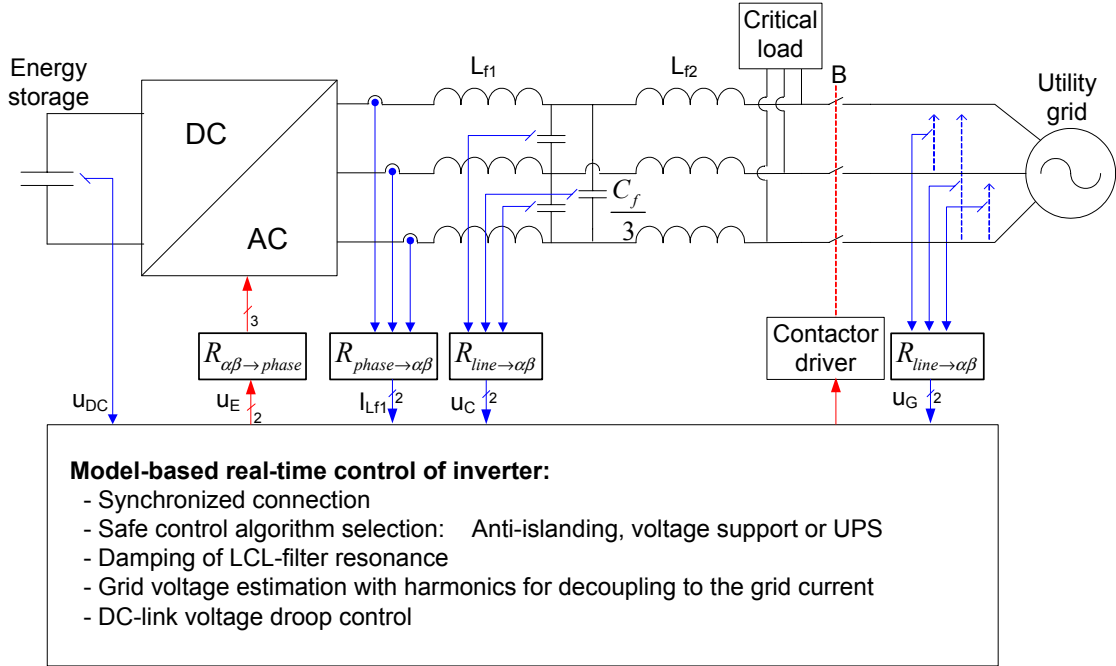
Figure 6: The inverter connections. The neutral connector is not connected (3-wire system).

The grid connection includes a filter which reduces the switching frequency component entering the grid. There are three frequently used alternatives: The purely inductive filter (L-filter), the LC-filter and the LCL-filter. The L-filter requires larger magnetic components compared to the LC or LCL-filter, but it is easier to control (concerning stability). A purely inductive filter however, will not damp any switching frequency if open-circuited. This is often the case in a UPS system. The LCL-filter on the other hand is smaller concerning stored energy, and the different inductors can be optimized for different frequencies. This makes the filter smaller. The main disadvantage of the LCL-filter is its inherent resonance frequency. It is defined by L_{f1} and C_f when the grid is considered open-circuited.

$$f_{0,LCL,OC} = \frac{1}{2 \cdot \pi \sqrt{L_{f1} \cdot C_f}} \tag{2.2}$$

When short-circuited or connected to a stiff voltage source such as the grid, the resonance frequency is given by L_{f1} in parallel with L_{f2} and C_f.

$$f_{0,LCL,SC} = \frac{1}{2 \cdot \pi \sqrt{\dfrac{L_{f1} \cdot L_{f2}}{L_{f1} + L_{f2}} C_f}} \tag{2.3}$$

Damping of this resonance can be accomplished using feedback control of the C_f voltage and inductor currents. The C_f current, which is the difference of the inductor currents, is often used. The voltages and currents are not necessarily measured, but can be estimated using a state-space observer such as the Luenberger observer [14] used in this work. The load-connected inductor in an LCL-filter limits the disturbance frequency, so that it is within the controller bandwidth. In an LC-filter, there are no limits how high the resonance may be. It is thus not guaranteed that the resonance frequency can be damped by a controller for an LC-filter. An LCL-filter also provides a load or grid current less sensitive to filter capacitor voltage errors. The LCL-filter is therefore used in the laboratory setup.

Synchronizing is the responsibility of the inverter controller, which measures the grid voltage, and uses this to adjust its voltage amplitude, frequency and phase. Synchronization can be done using an observer. The use of this observer also offers the possibilities of applying standard design and analysis methods like pole assignment. Both the LCL-filter and the grid voltage can be expressed in state-space form for model-based estimation and prediction used for controlling the inverter. The fast voltage controller is identical for the three different control algorithms. Only the slower power control and some harmonic concerns differ in the two grid-connected control algorithms (anti-islanding and voltage support).

2.2.1 UPS control algorithm

The UPS control algorithm is characterized by sinusoidal reference voltage control. This algorithm is operative when the grid fails. A typical load in this case is a nonlinear load. A 3-phase diode rectifier load shown in Figure 7 gives a representative circuit for a nonlinear load.
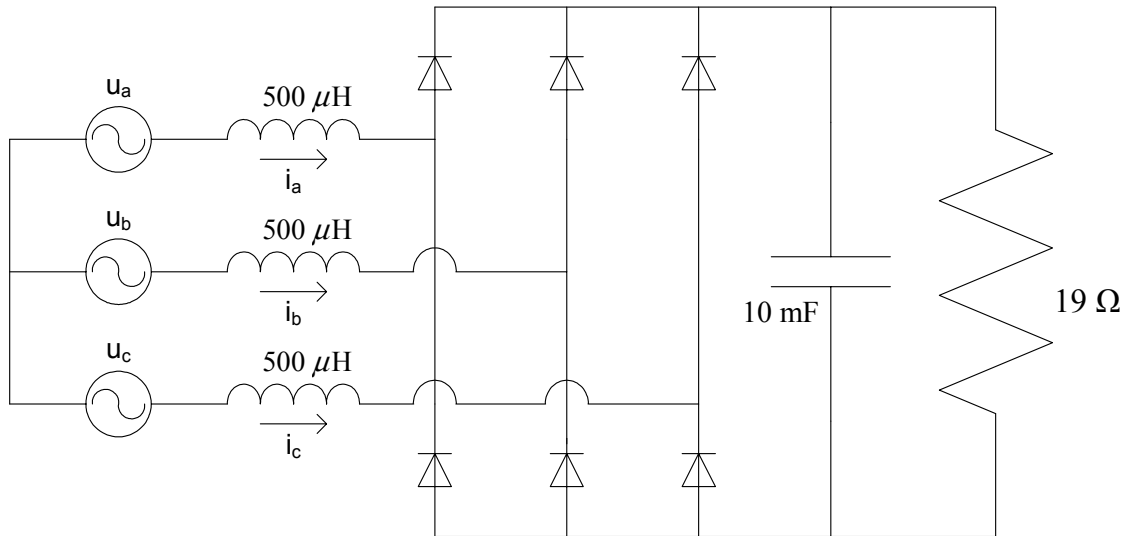
Figure 7: A diode rectifier load representative of electronical loads.

The disadvantage of nonlinear loads is the fact that the current drawn is not sinusoidal as shown in Figure 8.
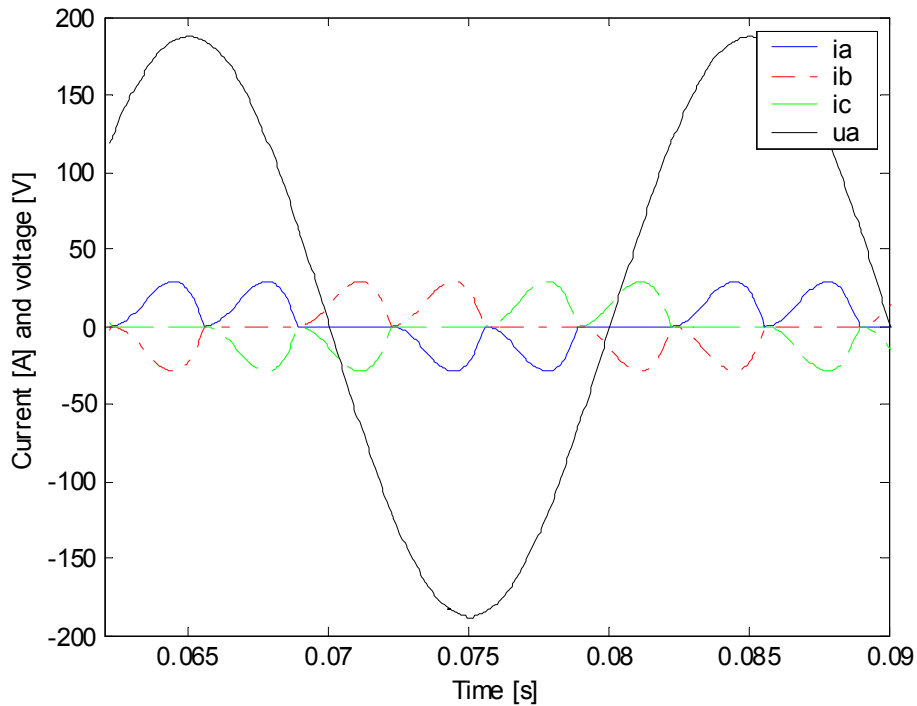
Figure 8: Typical current waveforms of the circuit in Figure 7 (simulation results).

In order to supply a sinusoidal voltage, the inverter cannot be current controlled for this type of load and thus must instead be voltage controlled. The current will have a number of harmonic components. The typical critical load is computers, which are single-phase

loads. This unbalanced diode rectifier load gives a 3rd harmonic in addition to the 5th, 7th and higher frequency components also caused by a balanced diode rectifier load.

2.2.2 Anti-islanding control algorithm

The anti-islanding control algorithm is used when there is a question of unintended islanding anywhere in the connected grid. Such a situation may appear when the locally produced power balances the load, followed by a disconnection event somewhere in the grid. The anti-islanding control algorithm drives the frequency or the amplitude of an eventual grid island out of the main grid tolerances, which indicates a grid island. The DG should then disconnect the grid.

It is important to be able to detect such a situation for personnel safety. The reason for a grid disconnection event is usually a fault. Without this algorithm, an islanding connection state can be hidden. The network owner may believe the disconnected part is not energized. Repair personnel could then be exposed to an electric shock. If a grid island has a phase 180° shifted from the main grid when reconnecting, an effective short-circuit could occur. This may result in damage of equipment or blown fuses. Grid connected distributed power supplies is required to detect an islanding connection state within 2 seconds, as a protection against these two situations [11]. The principle of islanding is shown in Figure 9.
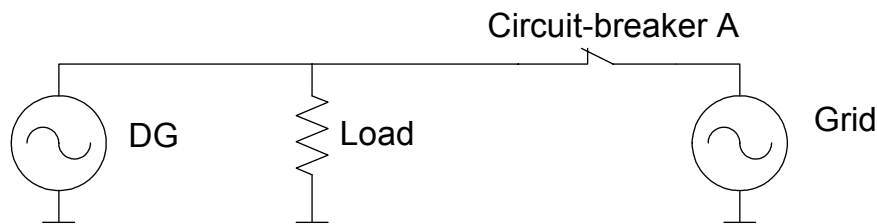
Figure 9: The principle of islanding: If DG production equals the load when the grid is disconnected, they can keep on running forming an island.

This control algorithm is normally grid-connected. The first control aim is to control the grid current to be sinusoidal. The fundamental frequency component can be controlled by applying amplitude and phase shifted voltage compared to the grid voltage. The grid-side inductor current will then be close to sinusoidal. This method is, however, more sensitive to measurement and model errors compared to current control. Compensation of the most common harmonic currents such as 3rd, 5th and 7th can be done using feed-forward of the individual grid voltage harmonics. This improves the current waveform to acceptable levels when using voltage control.

The second control aim is to detect an eventual islanding connection state in the grid. This avoids the risk of a stable island, measured by frequency and voltage. There are many methods for detecting this. Some algorithms such as Sandia Frequency Shift

(SFS), Sandia Voltage Shift (SVS), and Slip Mode frequency Shift (SMS) can detect such a situation reliably [15]. All three algorithms use positive feedback in order to destabilize either the frequency or the voltage amplitude. This drives the frequency or voltage of an eventual island out of predefined tolerances. A stiff grid connection is on the other hand not affected. All known published work is based on current-controlled inverters. One publication relevant to the voltage controlled inverter presented here is anti-islanding algorithms for rotating machinery [16]. A positive feedback anti-islanding algorithm for voltage-controlled inverters will be presented in Chapter 5.

2.2.3 Voltage support control algorithm

In a voltage support control algorithm, the inverter should stabilize both the voltage and the frequency of the grid, regardless whether it is in islanding or grid-connected connection state. The control of the inverter must then be opposite of the anti-islanding control, but similar to the control of larger power production facilities. Such a stabilizing function makes it impossible to distinguish an islanding connection state from a stiff grid connection.

Grid islands are not necessarily a disadvantage, because they can limit failures and thus improve grid voltage reliability. This relies on the ability of the network owner to control the islands. When there is no electrical connection, which is the case for an island, an alternative control method must be based on information from the network owner. The information can ensure the safety of repair personnel and equipment.

The voltage support control algorithm should include the voltage controllability of the UPS control algorithm. For the same reasons as the UPS algorithm, the inverter should be able to supply a non-sinusoidal load current. The voltage support algorithm also acts as a reactive power compensator and active power stabilizer. This balances the production and consumption of both reactive power and active power in islanding connection state (limited by production capacity). When the grid is connected the algorithm helps to stabilize the local voltage by reactive power production. If frequency changes occur, the DG can take part in the active power regulation of the grid. There should be means of controlling differently the various DGs. The network owner should also be able to change the DGs set-points (e.g. AC voltage) and tolerances (e.g. frequency and AC voltage) in real-time. This can be accomplished by using an energy management system.

2.3 Energy management system

In this thesis, the voltage support algorithm is based on voltage control. Internet communication ensures that the network owner always will be able to exit this voltage support algorithm to stop a grid island. In the work of Borle et al. [17], a voltage support algorithm has been applied, but with current control and without the use of communication. A communication system for protection against unintentional islanding

is described by Ropp et al. [18]. However, this is based on power-line communication and it is therefore unavailable during islanding connection state. It does not represent an extra control path, but simply replaces an anti-islanding algorithm in the inverter controller. Pettigrew proposes a system which changes the DG control if communication is lost, in order to detect islanding under all circumstances [19].

On the other hand, Internet cannot guarantee timeliness. It can only support soft real-time systems. In case of communication loss (detected through a timeout), the system fails to a safe control algorithm based on previously received information. For example if both control paths in Figure 10 are broken, the system degrades to UPS control (standalone connection state).

Communications information content:
*Set control algorithm,
set-points (e.g. AC voltage),
tolerances (e.g. voltage and frequency)
and timestamp*

Network
owner

DGs

Electric grid:
*Load sharing using droop
control*
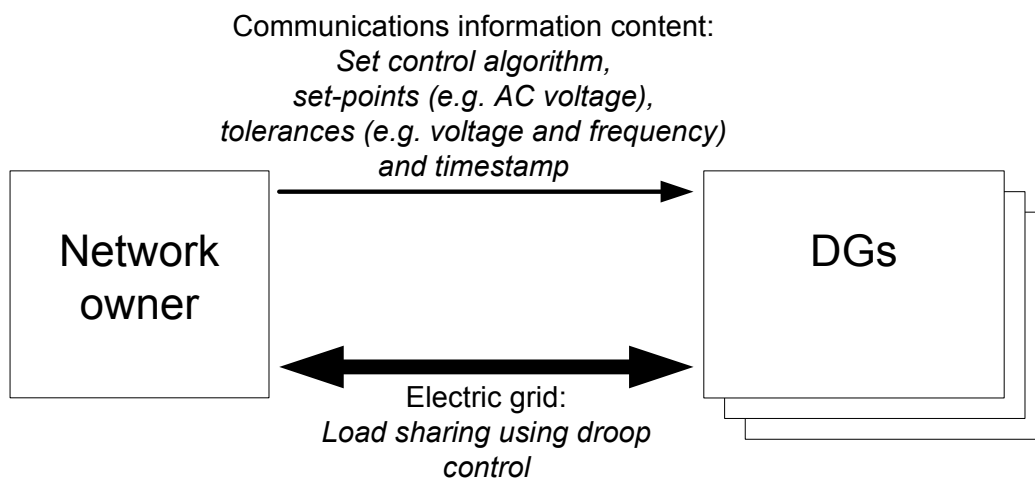
Figure 10: Communication as a method for controlling grid segments independently of the grid.

The energy management system uses communication to control a number of DGs. The design of the communication system is divided in two parts, a local communication bus, and a long-distance Internet communication algorithm. The local communication bus is a CANbus (Controller Area Network bus), connected to the different controllers of a DG. This is connected to the Internet by a DG gateway. It makes it possible to control the DGs externally, for example by the network owner.

2.3.1 Internet protocol

The cost of communication must be kept low. A promising approach is using existing infrastructure, such as the Internet. However, it is neither reliable nor real-time. Fault detection must therefore be placed in the DG. This is similar to the philosophy of the Internet, which has little error correction at the network layer, but compensates this by more advanced error handling in the end-user computers.

The Internet protocol (IP) has disadvantages making it less suitable for power control. It is not real-time because no priority is built in. The reliability during power outages is questionable. A combination of an unreliable communication channel and a fail-safe local control system may be a good choice. The degree of autonomous control in a more general context is discussed by Moslehi et al. [20]. A combination of autonomous DGs with additional functions served by communication is used in this thesis. However, it is important to detect a communication failure. The communication failure detection is done using a heartbeat message with a timestamp. Failure is signaled when the communication system crashes or fails, or in situations when the network owner stops sending these messages. Failure is then detected by the DG through a timeout. The Internet protocol is a network layer protocol in the in the OSI reference model [21] shown in Figure 11.

Application layer
Presentation layer
Session layer
Transport layer
Network layer
Data link layer
Physical layer
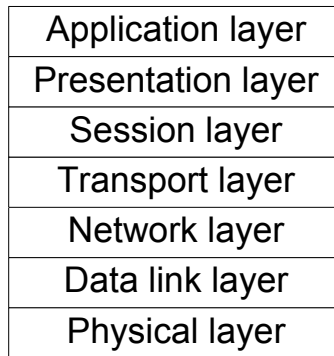
Figure 11: The seven layers of the OSI reference model.

Transport layer communication protocols can be classified into connection-oriented and connection-less protocols. Transmission Control Protocol (TCP) is a connection-oriented protocol, on contrary to the User Datagram Protocol (UDP) which is a connection-less protocol. Both are based on the Internet protocol. A power gateway based on HTTP (TCP/IP), is shown by Mawire [22].

A basic requirement for the communication system for DG is scalability. Communication that includes acknowledges directly faces problems when a large number of DGs are to be controlled. The User Datagram Protocol (UDP) is connection-less, and it does not include acknowledge in any of the phases of the communication. It represents a protocol with less overhead compared to TCP. The destination is addressed simply by the IP address and the port number. It is a best-effort protocol and hence guarantees neither ordering nor delivery. Unlike TCP, the UDP does not have congestion control. This makes it controversial to run high-bandwidth applications like multimedia over UDP [23]. UDP-based protocols are in general sufficient for soft real-time applications. The UDP segment, or transport-layer packet structure is shown in Table 3.

Table 3: The UDP segment structure.

32 bits	
Source port number	Destination port number
Length	Checksum
Application data (message)	

UDP gives the programmer complete control of the information that is transmitted due to its simplicity.

2.3.2 Communication scalability

Scalability is of vital importance for large-scale communication. In order to implement real-time communication, the loading of the master (in this case the network owner) must be taken into consideration. The number of DGs should be possible to increase to several thousands without reaching limits caused by communication bandwidth to the master (network owner). Epidemic algorithms offer this property as described by Demers et al. [24]. They mimic how an epidemic spreads in a population. Flooding is the simplest form of an epidemic algorithm. It can be imagined as flooding water, trying every possible path to the sea. The fastest route determines the convergence time. The end-condition can be given as a fixed number of recursions, or it can be defined by the moment when one message is received twice as shown in Figure 12.

```
RECEIVED_MESSAGE(message w/senders timestamp) {
        If (message newer than last received message) {
                Update local data
                Forward message w/original timestamp to all neighbors
        } else {
                Do nothing
        }
    }
```

Figure 12: Flooding algorithm used in a limited network.

A more advanced epidemic algorithm is gossiping. It mimics how gossip randomly spreads in a population. Vanthournout uses gossiping for scaleable DG communication [25]. This algorithm is not real-time. Flooding has a shorter time delay. It is here demonstrated through practical implementation of a flooding algorithm consisting of one master (network owner) and two slaves (DGs). The flooding algorithm with three slaves (DGs) can be visualized as shown in Figure 13.

DG 2

3

Network
owner

1

DG 1

4 5

2

DG 3

Network
owner

DG 1

DG 2

DG 3

1   $t_1 > t_{prev,DG\ 1}$ $t_{prev,DG\ 1} = t_1$

2   $t_1 > t_{prev,DG\ 3}$ $t_{prev,DG\ 3} = t_1$

3   $t_1 > t_{prev,DG\ 2}$ $t_{prev,DG\ 2} = t_1$

4   $t_1 = t_{prev,DG\ 3}$

5   $t_1 = t_{prev,DG\ 2}$
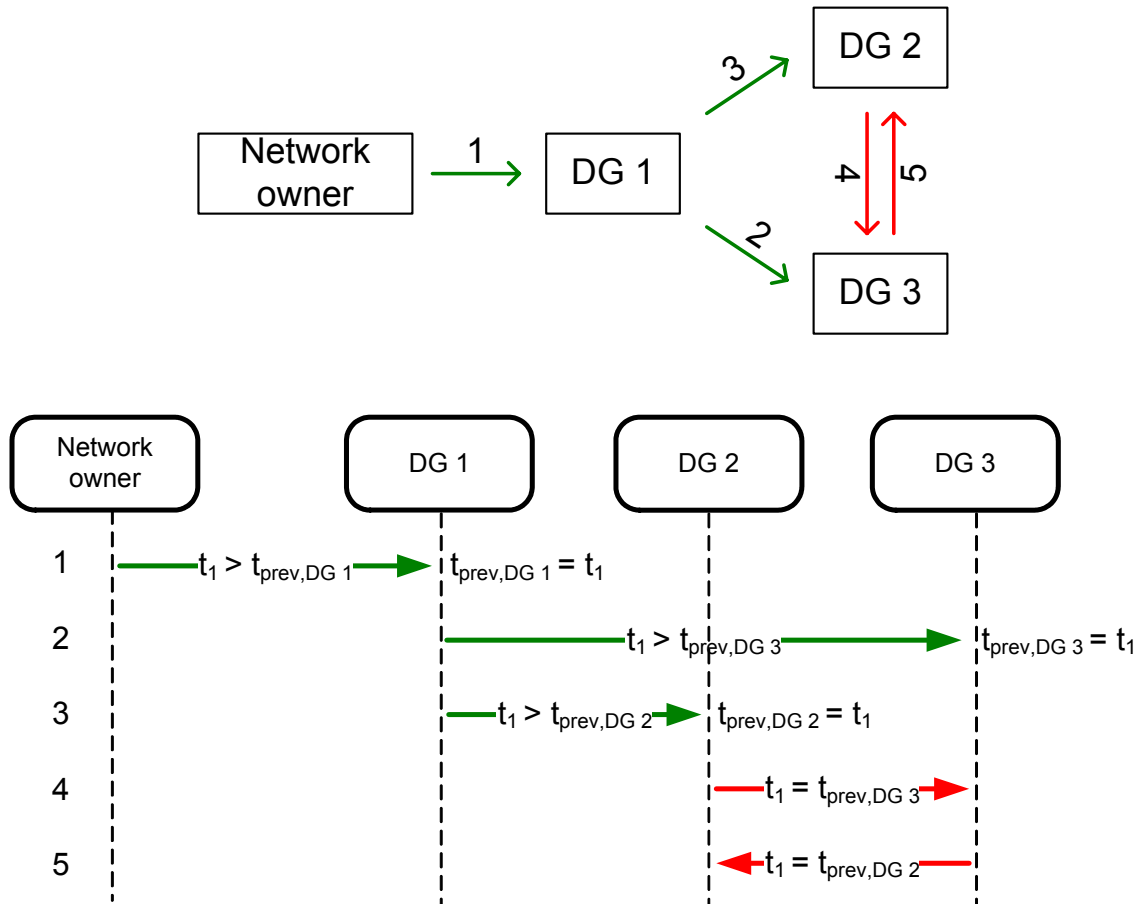
Figure 13: Flooding relies on forwarding of received messages to neighbors until a message has been received twice. This ends the forwarding process. Accepted messages are indicated by green arrows, while red arrows indicate previously received messages.

2.3.3 Monitoring

KWh-metering is perhaps the best driver to communication not only to DG but also to kWh-counters in private homes and in industry in Norway. There are many commercial solutions to this, and standardization is a part of this. Use of communication for monitoring of DG is commercially available. What is needed is mainly a standardization of the data exchange format. An example of such is the ODEL 2.1 XML version presented by Feilberg [26]. The data exchange format used in this thesis is inspired by the ODEL 2.1 XML format.

The monitoring data should be accessible mainly for the owner of the DG. However, it would be beneficial for the network owner also to know both the instantaneous production within one area and type of production (in order to predict the load). A distributed system presented by Vanthournout [25] can be used to get the aggregated production within one area.

2.4 Overall control for safe operation

Power electronic converters require a fast and reliable response time. They must therefore operate safely without the communication operative. Communication status can be used for choosing a safe control algorithm, but the control algorithms themselves can not rely on communication due to timeliness and reliability concerns.

The converter tolerances concerning voltage, current, temperature and other variables depend on the type of power electronic converter. A fail-to-safe-mode control must therefore be implemented, for each converter. For most power electronic components, a safe operating area (SOA) is defined [27]. The different components in a DG system have different safety-critical variables. Table 4 shows some relevant examples.

Table 4: Safety-critical variables.

Standalone inverter	Grid-connected inverter	DC/DC-converter
Temperature DC voltage AC current Driver-level faults	Temperature DC voltage AC current Driver-level faults AC frequency AC voltage Communication (optional)	Temperature Output voltage Input voltage Current Driver-level faults

These safety-critical variables are specified with a minimum and/or a maximum value defining the tolerances. In cases where the variables can be controlled, a tolerance violation should lead to an appropriate change of the control algorithm to avoid further consequences. The tolerance values are defined so that the system is gracefully degradable.

The DC/DC-converter applied in this work can be used in order to illustrate the concept of a gracefully degradable system. If during MPPT the DC/DC-converter looses its load, the energy source must reduce the output power. Otherwise the output voltage may increase out of boundaries. A gracefully degradable system prevents the converter from immediately shutting down, but instead controls the output voltage by switching to a power reduction control algorithm. The list of preferred control algorithms is shown in Table 5.

Table 5: List of preferred control algorithms for the DC/DC-converter.

Preference number	Control algorithm
First priority:	A2: MPPT
Second priority:	A1: Power reduction
Last priority:	A0: Reset (system OFF)

The requirements for the control algorithms in Table 5 can often be ordered in a decision table, as shown in Table 6.

Table 6: Decision table for the DC/DC-converter system control algorithms

Current control algorithm	No output over-voltage	No input over-current	Heat sink temperature OK	No stop system signal	Hexadecimal representation
A0: Reset (OFF)	*0*	*0*	*0*	*0*	*00*
A1: Power reduction	*0*	*0*	*1*	*1*	*C*
A2: MPPT	*1*	*1*	*1*	*1*	*F*
Bit number	*0*	*1*	*2*	*3*	

Voltage and current are connected to the transition between Algorithms A2 and A1. Heat sink temperature is one example of a parameter that can be connected to transitions between Algorithms A1 and A0. This method has been implemented for ensuring safe operation of both converters in the system. Temperature measurements were not implemented in the laboratory setup. For more detailed information, see Chapter 6.

3   Energy source modeling and control

There are a variety of competing technologies as energy sources for DG, such as wind, hydropower, and different fuels such as biogas. In this work, however, photovoltaic (PV) is chosen as the energy source due to its scalability, simplicity and availability. A PV system is easily scaled by the number of PV cells. It has no moving parts, and it is thus reliable. The sun is shining in most places, although the average yearly energy yield varies with latitude and local climate. The technology is promising, but there is a need for cost reduction.

The power output of a photovoltaic panel for a given irradiation and temperature depends on the operating voltage. This voltage can be held fixed, as is most common in battery systems, or it can be varying, which it is for most grid-connected systems. In order to decouple the PV panel voltage and the DC-link voltage of the inverter, a DC/DC-converter is commonly used. The maximum power point (MPP) can then be tracked, using a maximum power point tracking (MPPT) algorithm for optimizing the PV panel operating voltage.

The model of the photovoltaic panel is valuable for the control and choice of DC/DC-converter. Especially during periods with more available PV power than consumed by the load, the control and the choice of DC/DC-converter topology is important. This chapter presents a model of the PV panel. A DC/DC-converter topology is then discussed. The control of this DC/DC-converter is described at the end of Chapter 5.

Silicon is the most common material for photovoltaics. Other materials such as gallium-arsenide (GaAs) give higher efficiency, but the production cost is considerably higher compared to silicon. These materials are often used in space applications and in concentrating PV systems.

3.1 Photovoltaic cells

The photovoltaic cell can be considered as a semiconductor pn-junction. Instead of conducting in the forward-conducting region (forward-conducting diode), one makes use of the reverse space charge region generation current caused by photons, I_{ph}. This gives rise to a current I_{out} flowing in the reverse (blocking) direction of the pn-junction, as shown in Figure 14.
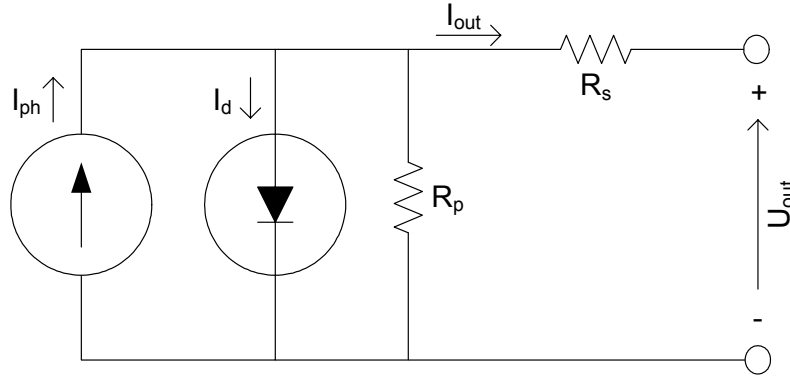
Figure 14: The photovoltaic cell equivalent circuit scheme.

One silicon photovoltaic cell can be modeled according to Equation (3.1) [28]. The last term (the current trough R_p) is added to the original equation to model pn-junction imperfections due to e.g. shunts in the silicon crystal structure.

$$I_{out} = I_{ph} - I_{or} \left[\frac{T}{T_r} \right]^3 \cdot e^{\frac{q_e \cdot E_G}{K \cdot B} \left(\frac{1}{T_r} - \frac{1}{T} \right)} \cdot \left[e^{\frac{q_e \cdot (U_{out} + I_{out} \cdot R_s)}{K \cdot B \cdot T}} - 1 \right] - \frac{U_{out} + I_{out} \cdot R_s}{R_p} \tag{3.1}$$

where:

I_{out} = Photovoltaic cell output current [A]

I_{ph} = Photovoltaic current ($\propto$ irradiance) [A]

I_{or} = Saturation current [A]

T = Solar cell actual temperature [°K]

T_r = Reference temperature (298 [°K])

q_e = Electron charge $= 1.602 \cdot 10^{-19} [coulomb]$

E_G = Silicon band gap (1.1 [eV])

K = Bolzmann's constant $= 1.38 \cdot 10^{-23} \left[\frac{Joule}{°K} \right]$

B = Ideality factor of the diode

R_s = Equivalent series resistance

R_p = Equivalent parallel resistance

The maximum output voltage is given by the diode forward conduction voltage drop (approximately 0.7 V), which for silicon is highly temperature dependent. The IV-characteristic based on Equation (3.1) and estimated parameters specified in Table 7 are shown in Figure 15.

Table 7: Estimated parameters of the PV model

Parameter	Value
I_{ph}	3.36 [A]
I_{or}	$1.91 \cdot 10^{-7}$ [A]
T	382 [ºK]
B	1.55
R_p	$1.84 \cdot 10^{5}$ [Ω]
R_s	9.26 [mΩ]
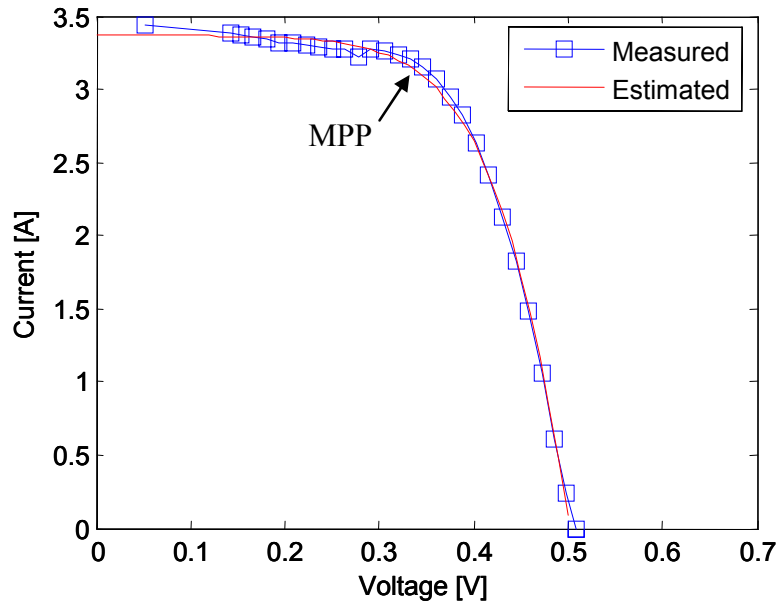
Figure 15: Typical IV-characteristic of a silicon photovoltaic cell. The measurements are scaled from measurements from two series-connected 80 Wp type Photowatt PW 750 PV panels (72 cells). The measurements were taken manually using an IGBT in the active region as an adjustable load.

More advanced methods for modeling PV cells, such as a two-diode model exist. For this work the presented single-diode model is assumed sufficient. Typical temperature- and irradiance dependence is shown in Figure 16 and Figure 17, calculated using Equation (3.1) with the parameters specified in Table 7.
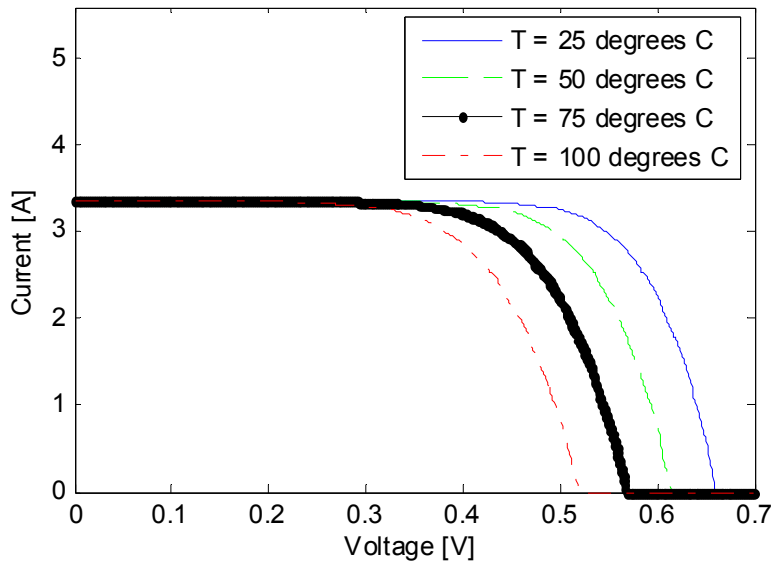
Figure 16: The variation of output current and voltage as a function of the temperature.
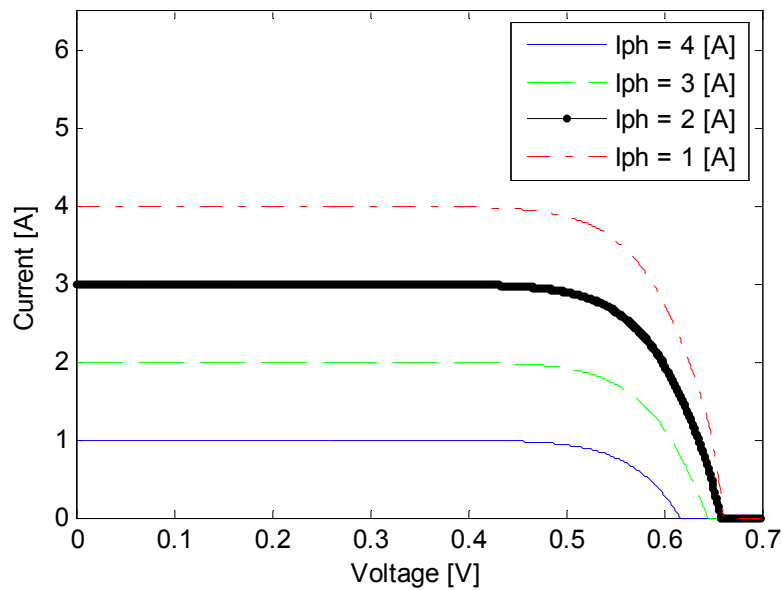
Figure 17: The variation of output current and voltage as a function of I$_{ph}$. The current I$_{ph}$ is approximately proportional with the irradiance.

One can observe that the voltage is approximately inversely proportional to the temperature. The irradiance has some influence on the voltage. However, increased irradiance leads to higher cell temperature. In sum, the irradiance has less influence on the steady-state voltage under normal operating conditions, than Figure 17 indicates.

3.1.1 The photovoltaic panel

A typical photovoltaic panel consists of a number of series-connected photovoltaic cells. A common standard panel for 12 V lead-acid battery charging is 36 cells in series, as shown in Figure 18.
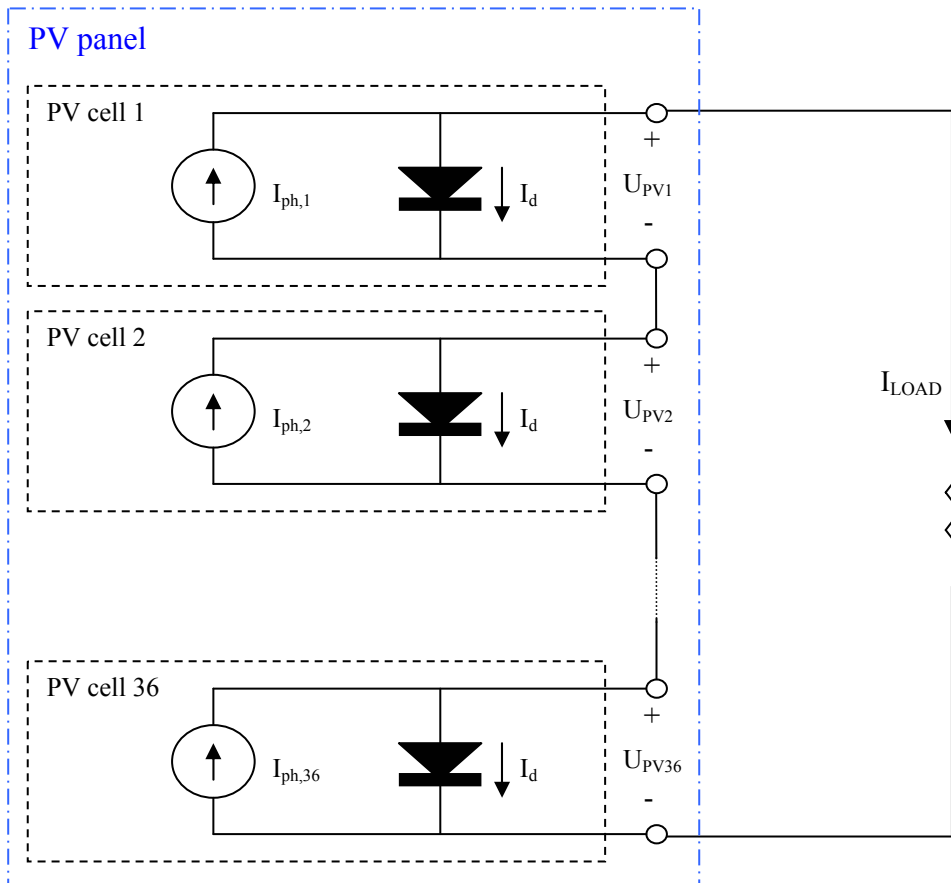
Figure 18: A 36-cell PV panel circuit-scheme representation.

Assuming equal irradiation, temperature and cell parameters a PV panel can be modeled simply by scaling the voltage of a single PV cell. Using the same approach for paralleling, the current can then be multiplied by the number of paralleled strings. These simplifications do not hold for cell inequalities and partial shading of the PV panel.

Bypass diodes are often connected in anti-parallel with the PV cell pn-junction equivalent scheme diode. Bypass diodes are usually not connected over every cell in a PV panel, but instead one diode serves 10-20 PV cells in series. This is sufficient to avoid heat damage of a shadowed cell caused by its absorption of the power produced by the other non-shadowed cells of the series connection. A test setup consisting of two PV panels and a bypass diode per panel (36 cells) is shown in Figure 19.
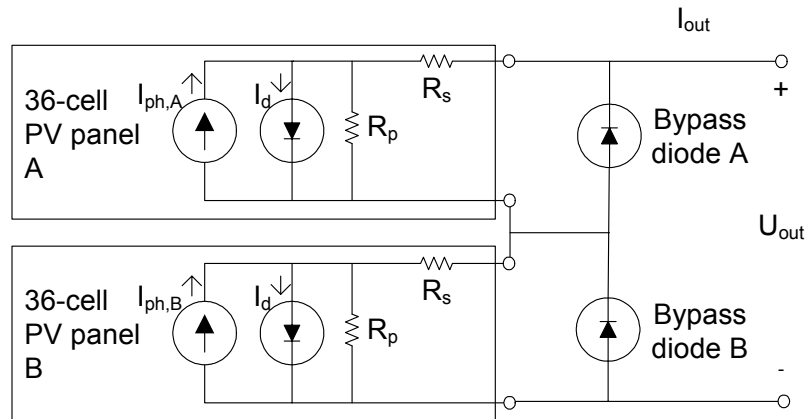
Figure 19: A test setup for testing of bypass diodes in connection with shading of one single cell.

Figure 20 shows how the shading of one cell in one of the PV panels affects the IV-curve of the two series-connected PV panels.

a)
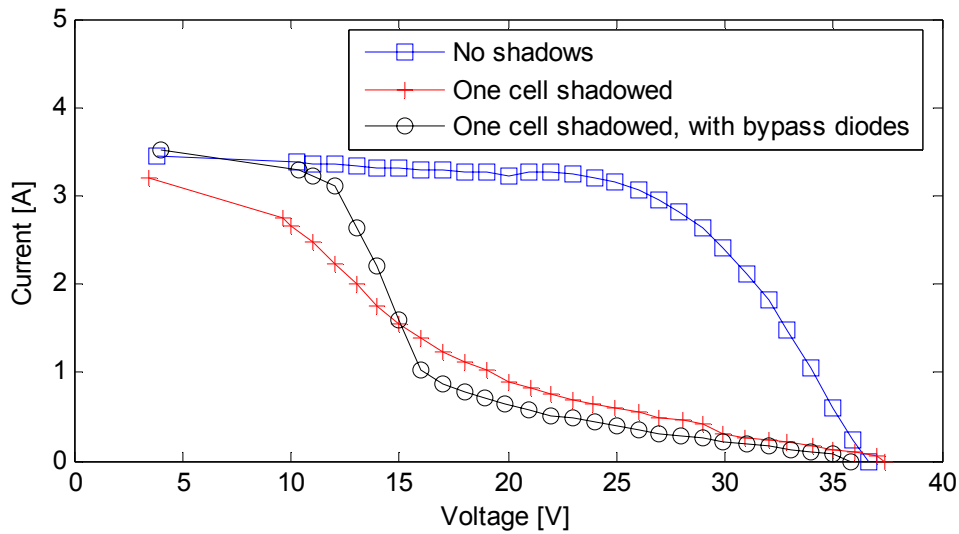
b)
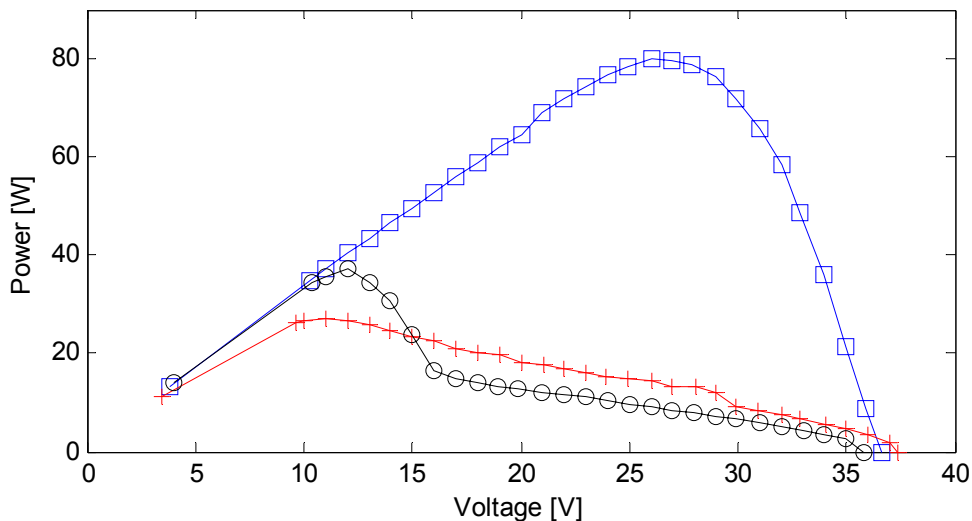
Figure 20: a) Measurements of the shading effect on a photovoltaic panel (2 series-connected 80 Wp type Photowatt PW 750). b) resulting output power.

The combination of blocking or partially conducting cells and conducting bypass diodes makes the IV-curve deviate from the scaled single-cell equivalent. One effect that can be seen due to partial shading is an unexpected large difference in MPP voltage, U_{MPP}, compared to open-circuit voltage, U_{OC}.

Assuming that bypass diodes are applied, the photovoltaic panels can be short- or open-circuited without damaging the panels. Apart from the MPPT algorithm and a method to reduce the panel output power, control of the PV-panel is not needed.

3.2 PV panel voltage control

Control of the PV panel voltage is associated with MPPT and power reduction controllers (output voltage or current limitation). These two purposes are contradictory and only one of these two control algorithms can control the DC/DC-converter at a time. The sizing of the DC/DC-converter is associated with the control of the PV panel voltage.

3.2.1 Converter efficiency

The control of the PV panel voltage is an advantage, but the cost of and losses in the converter needed can, however, offset much of the gain. This is also the case for other systems such as variable-speed turbines compared to fixed-speed turbines (wind or hydropower). Analyzing the physical properties of the photovoltaic panel, converter efficiency and size, one can estimate the gain. The efficiency of a DC/DC-converter is usually significantly lower at partial loading compared to full load, and a converter with less than full power rating is therefore beneficial. This is valid concerning maximum current [29] as well as voltage regulating range [6-8].

3.2.2 MPPT

MPPT can improve the energy output of a PV panel [30]. The gain is however very temperature dependent [31] and depends on DC/DC-converter efficiency [32]. There are two major classes of MPPT algorithms. Having knowledge about the relationship between current and voltage of a given PV panel, one only needs to measure one of the two in order to get sufficient information to perform MPPT. The other class of algorithms, which is used in this work, utilizes the measurements of both current and voltage of the PV panel. The MPPT algorithm then finds the MPP by calculating the output power at different voltages.

Parallel connection of DC/DC-converters with MPPT on the PV panel side, requires communication for MPPT. The connection has been called the team concept by Myrcik and Calais [9]. The other alternative, paralleling on the DC-link side is done for the string converter. The main difference between the two circuit schemes is the string converter does not require communication, while the team concept needs real-time communication for controlling the PV panels in MPPT algorithm. The string converter is compared to the team concept in Figure 21.

a)

b)
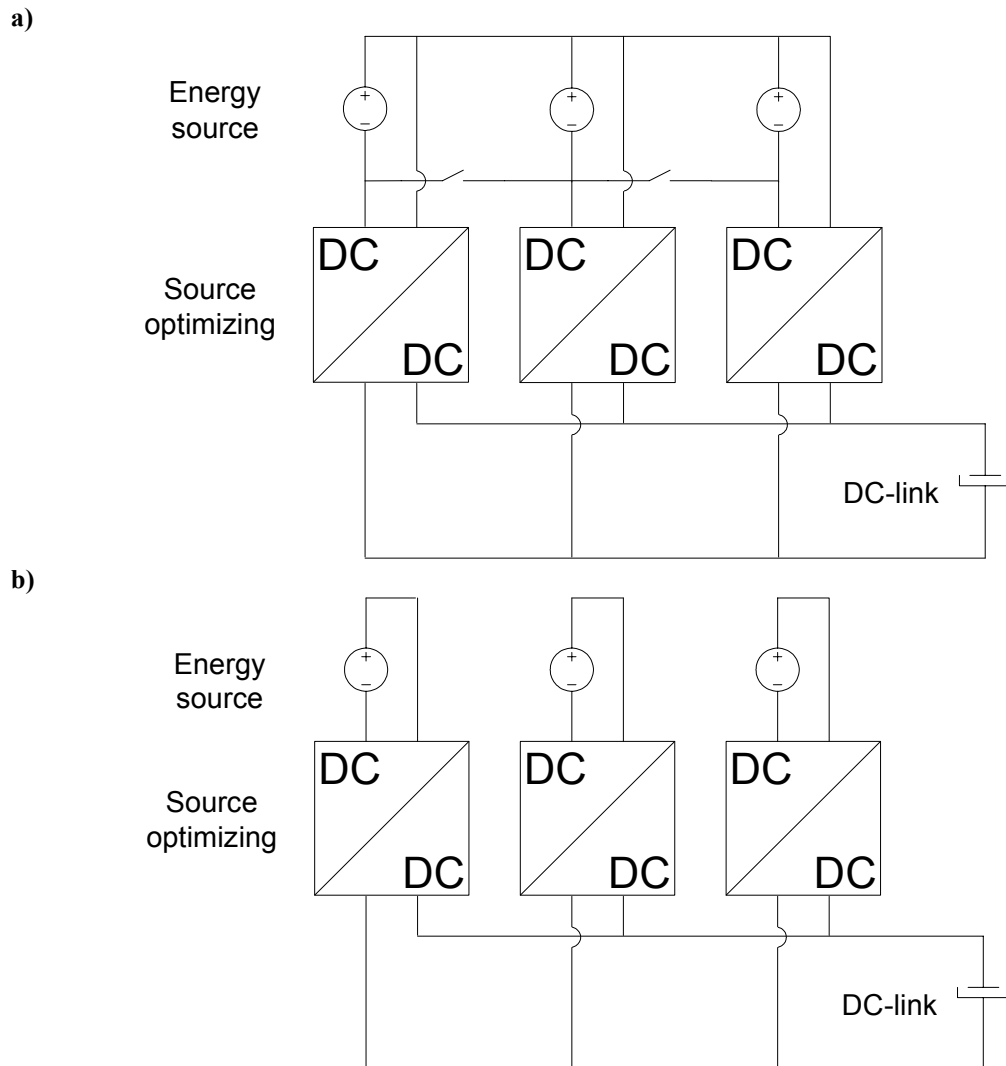
Figure 21: a) The team concept. b) String converters.

The team concept is able to adjust the power level by shutting OFF some of the converters. All active converters except one (controlling the PV voltage) are able to operate at their optimal load point concerning efficiency or other measures. This solution also offers redundancy as one failed converter only reduces the maximum output power of the system, but a failure has no influence on medium power levels. Communication is necessary for selecting the converter to control the PV panel voltage, and for measuring the aggregated power from all the paralleled converters. The rest of the converters are either OFF or current-controlled.

The string converter has gained popularity during the last few years. It is less sensitive to partial shading as the optimum PV panel voltage is tracked independently in the individual strings.

3.2.3 PV panel power reduction

When the PV panel is connected to a DC/DC-converter, control of the panel is vital. The input power from the PV panels must be controlled in order to make the DC/DC-converter work as desired. Most converter topologies (such as boost converter) may output too high voltage or current if not properly controlled. When output power is controlled, the DC/DC-converter is made safe without use of communication. The inverter and the DC/DC-converter both decide the power level through a DC-link droop of 5 %, as shown in Figure 22.
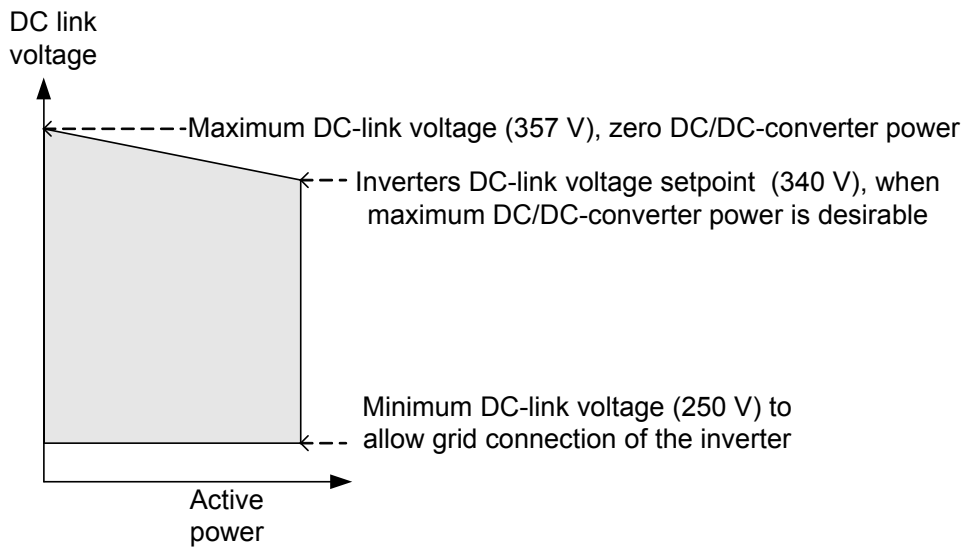
Figure 22: DC voltage droop control of the DC/DC-converter in power reduction control algorithm.

A thorough discussion about DC droop is shown by Karlsson [33]. Gaining control of the output power from the PV panel one needs to look at the connection between voltage and power output from the panel. This is shown in Figure 23.
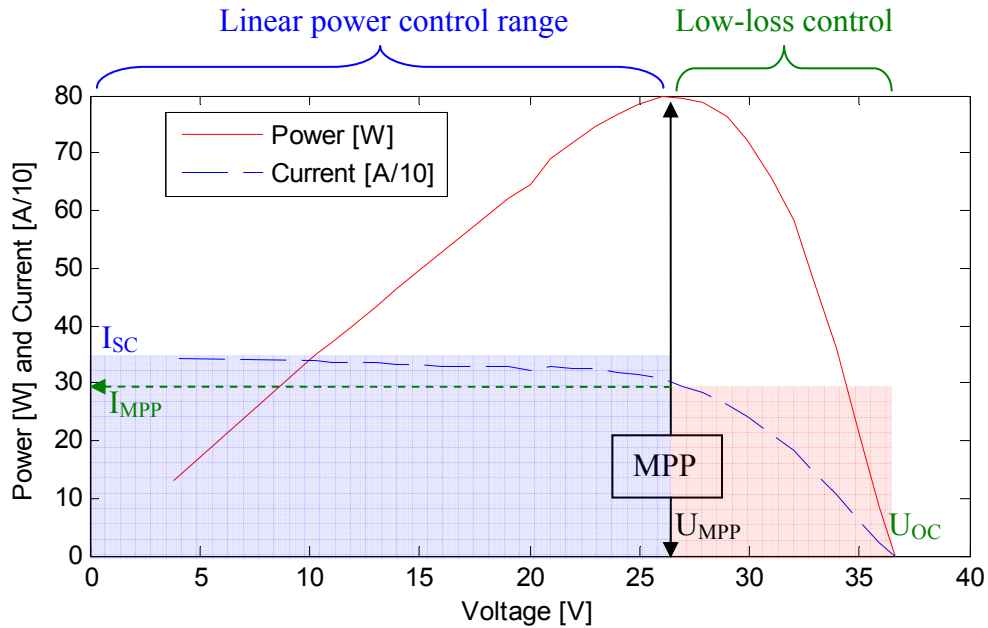
Figure 23: Measured power curve for a 72-cell photovoltaic panel (two series-connected Photowatt PW 750). The colored squares indicate the current- and voltage-rating of the DC/DC-converter. The left, blue square shows the required voltage and current rating when controlling the PV panel voltage from MPP to short-circuit. The right, red square shows the required voltage difference and current rating when controlling the PV panel from MPP to open-circuit.

In order to reduce the power output, two regions of this plot give possible solutions. From a control perspective the most linear part of the curve, from the MPP down to short-circuit current, I_{SC}, may be beneficial. This requires a converter current rating equal to I_{SC} which is higher than the I_{MPP}. This controller does not give limited current (and thus power) rating.

Dimensioning for I_{MPP} is possible if the region from MPP, U_{MPP}, to open-circuit, U_{OC}, is used for power reduction. This makes it possible to reduce the converter rating both concerning maximum current, as well as the maximum input- and output voltage difference. Limited power rating is thus possible.

3.2.4 Series-connected boost converter

The optimal voltage of a photovoltaic panel, U_{MPP}, varies only by a fraction of nominal voltage when the PV panel produces noticeable amounts of power. A voltage variation of only 23 % keeps the voltage at optimum for a temperature span of 75 °C and constant irradiation, assuming the parameters given in Table 7. This makes it possible to decrease the converter losses according to the voltage variation. These losses are then reduced to approximately ¼ of the normal value, which again leads to an increase of the DC/DC-converter efficiency from for example 92 % to 98 %. The low voltage variation also gives the possibility of minimizing the dimensions of the converter to about ¼ of the normal size. This concept for optimal converter design is shown in Figure 24.

Standard converter:
100 % voltage control range
92 % efficiency

η=0.92

Alternative converter:
25 % voltage control range
98 % total efficiency

η=0.92   η=1   η=0.98
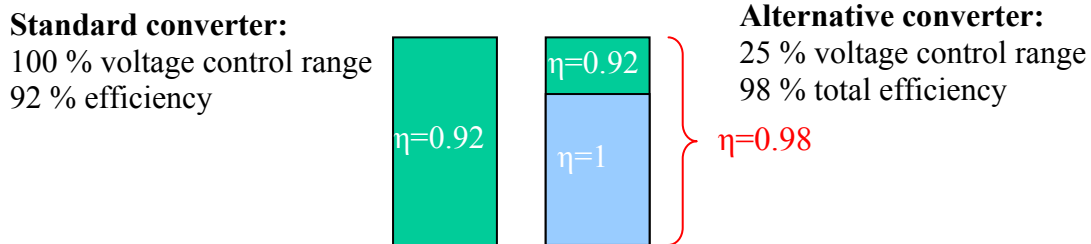
Figure 24: Method of reducing the DC/DC-converter losses.

The method is patented by Beach and Brush [6] for a specific boost topology (Series-Connected Boost Converter, SCBC) and it is also described by Button [7] and Kimnach [8]. A step-down solution for lower voltages than these publications is shown in Figure 25.

+ 0...25 % -

PV panel

DC/DC converter input

DC/DC converter efficiency 92 %

DC/DC converter output

Energy storage
+
-
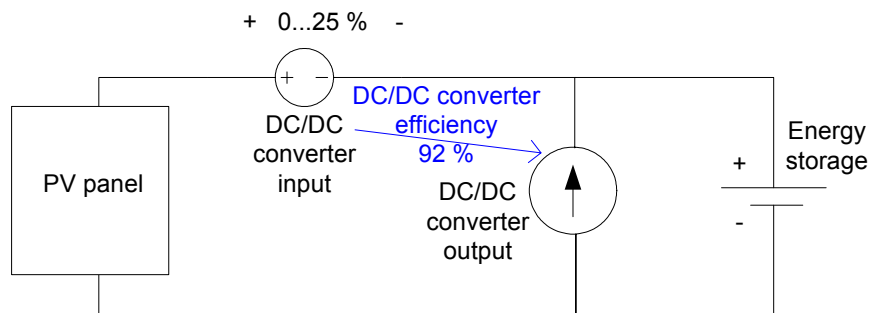
Figure 25: The conceptual circuit scheme of a converter with limited range voltage control

A DC/DC-converter based on a flyback converter with both step-up and step-down capabilities is used in this work. Descriptions of converter topologies can be found in [34].

3.2.5 Series-connected bidirectional flyback converter

The ideal DC/DC-converter circuit for PV panels would be able to transform the voltage both up and down with regard to the output DC-link voltage. A close match between the PV panel output voltage and the DC-link voltage could then be easier to accomplish. Some MPPT methods, which use the open-circuit voltage, need 24 % change between open-circuit voltage and MPP, plus the change due to weather variations. A solution which is close to satisfying these requirements is shown in Figure 26.
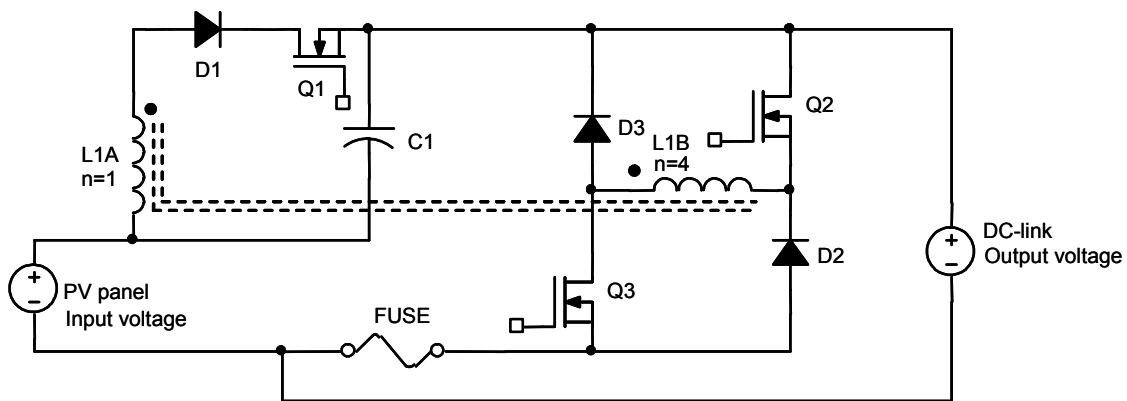
Figure 26: A series-connected bidirectional flyback converter. Inductors L1A and L1B are magnetically connected, with a turns ratio of ¼. Snubbers are not included in the drawing.

To avoid conduction in D2 and D3 when Q1 is ON, the duty cycle is limited to ±45 %. The benefits compared to a standard boost converter, is the fact that the switches Q2 and Q3 carry ¼ of the current. Idealized switching waveforms are shown in Figure 27.
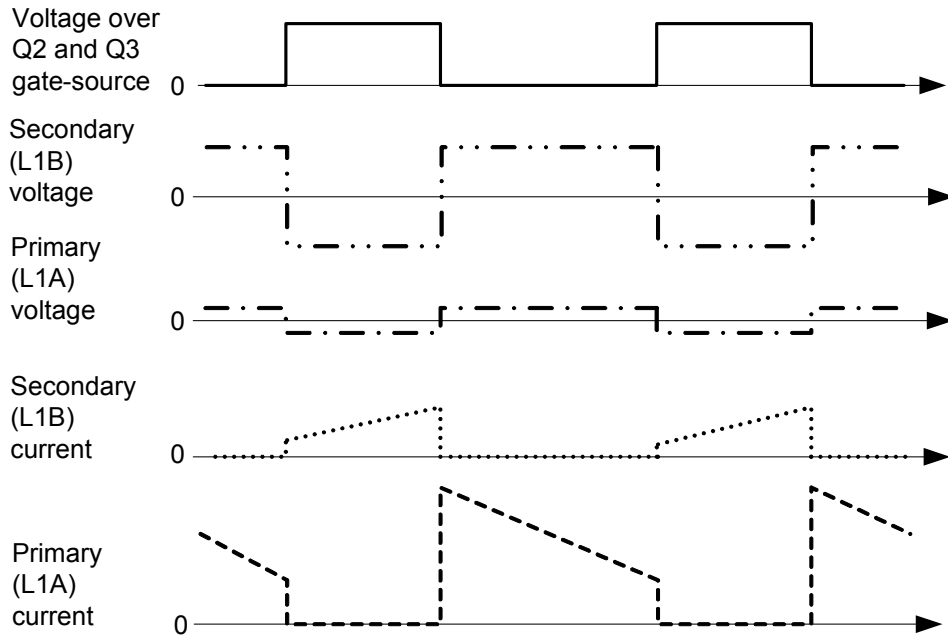
Figure 27: Idealized switching waveforms of the bidirectional flyback converter in boost mode.

The leakage inductance is neglected here, together with the snubbers. The effect of the leakage inductance can be observed on the measured waveforms in Figure 28.
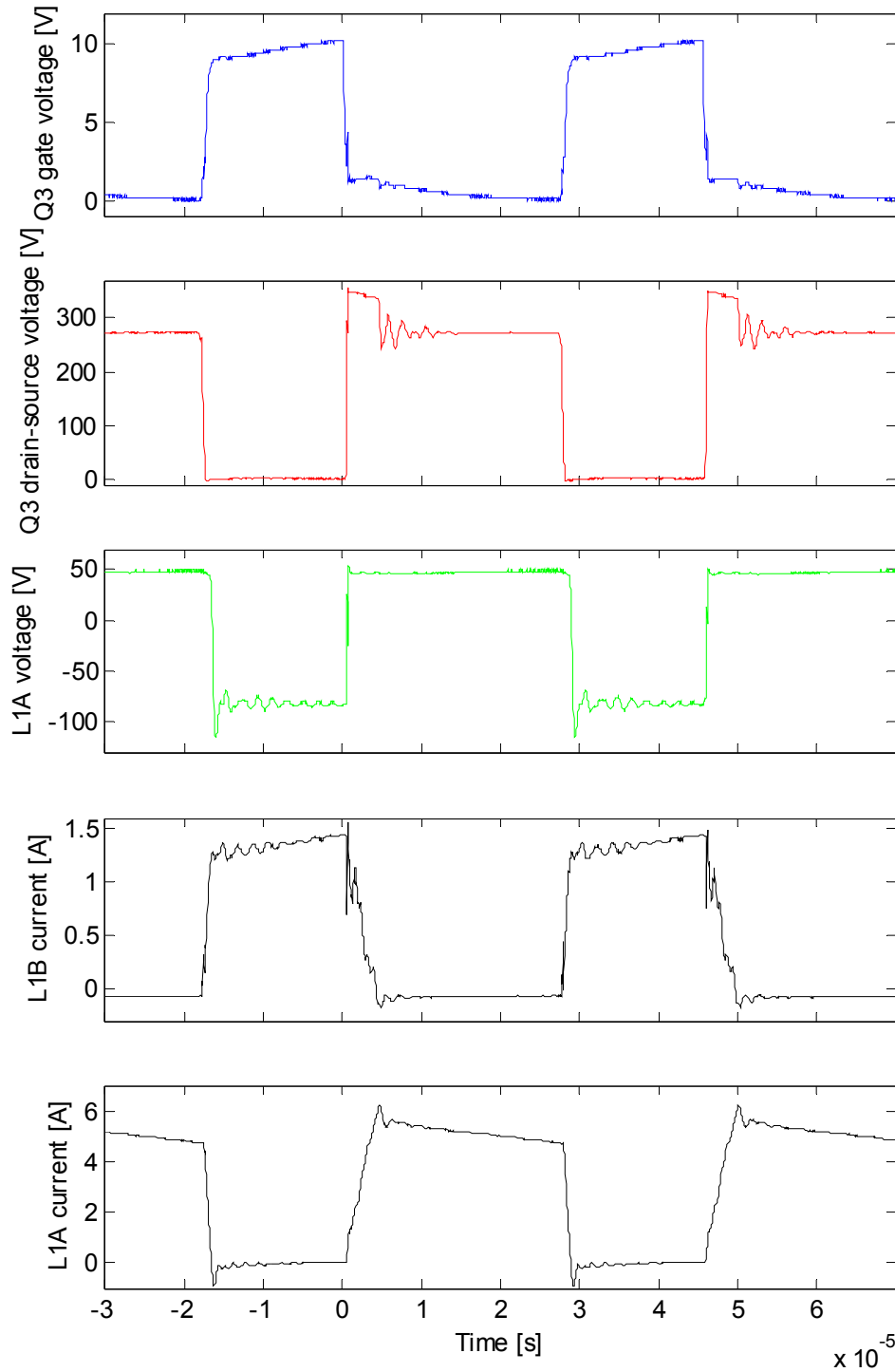
Figure 28: Waveforms recorded at 300 V input and 340 V output. The four upper traces were recorded with 3.4 A input current. The lowest trace was recorded separately with 3.3 A input current. All waveforms were recorded using 16-point averaging.

When coolMOS Q2 and Q3 turn OFF, the leakage inductance energy is freewheeled through diodes D2 and D3. Even though RC-snubbers were used for reduction of ringing, it can still be observed in the waveforms. It can be observed that the switching coolMOS Q2 and Q3 current is less than half the input current. This can reduce the switching loss to less than a standard boost converter, even though there are two switches. The benefit of using limited range voltage control is, however, higher if the input and output voltages are closer.

The extra switch, Q1, makes the DC/DC-converter bidirectional, thus giving the opportunity of having an input voltage higher than the output voltage. Although this switch carries the entire current, the switching voltage is only approximately ½ of the total voltage. The switching losses can therefore be reduced compared to a standard buck converter. The voltage regulating range can therefore be connected to efficiency in a way that can be exploited in PV systems. The DC/DC-converter developed is shown in Figure 29.
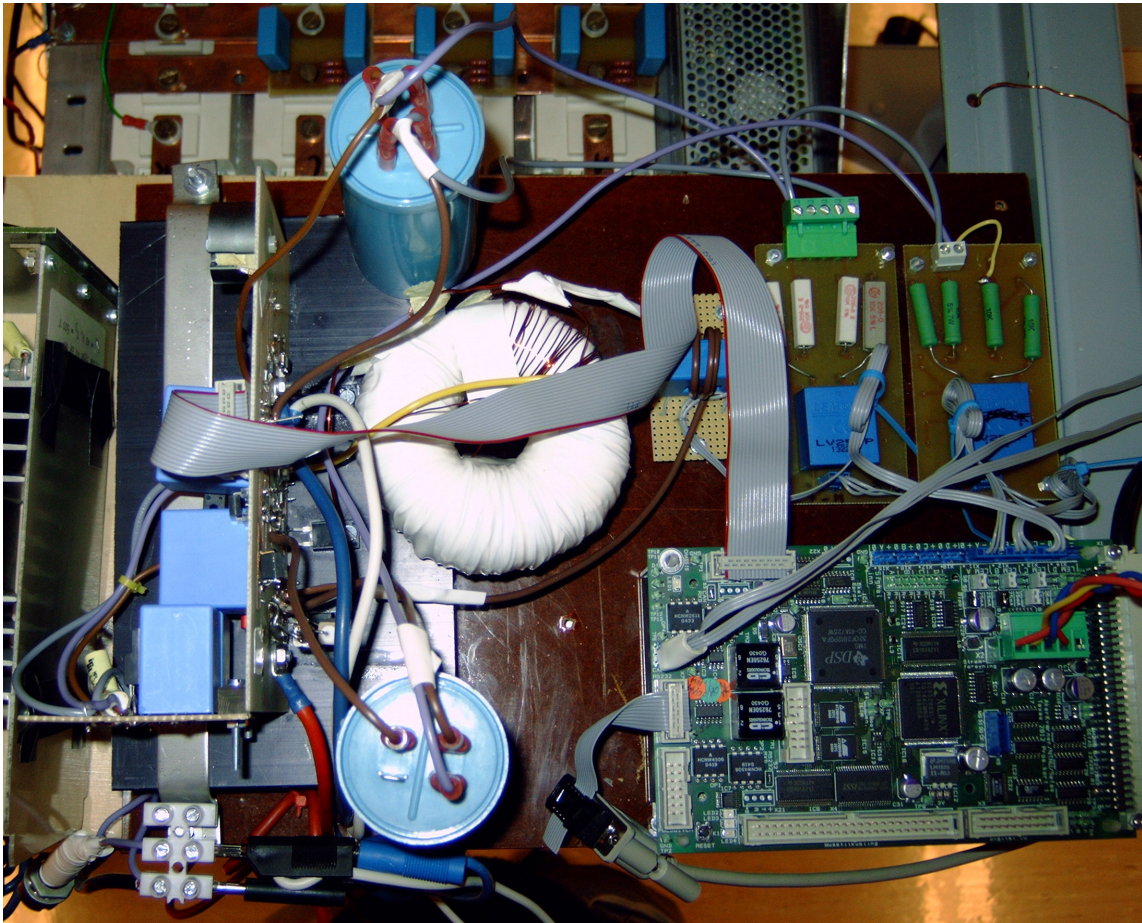
Figure 29: The DC/DC-converter developed for use in the laboratory setup.

3.3 DC/DC-converter discussion

There is an optimal ratio between the DC/DC-converter power rating and the PV panel power rating. The ratio between converter current rating and the PV panel maximum current is connected to the geographical latitude of the PV panel. The optimization is mainly based on a tradeoff between:
1. no-load losses (increases with size),
2. peak power loss due to undersized converter (decreases with size)
3. cost (increases with size).

On the other hand, the voltage control range is connected to:
1. Converter topology
2. The ratio between the PV-panel voltage and the DC-link voltage

The patented series-connected boost converter [6-8] implements the limited range voltage control based on a forward converter. It can only step up the voltage from a PV panel. Other topologies can implement the same principle of limited range voltage control, like the flyback-based topology presented here. It can both step the voltage up and down. The switching action can also be bypassed when not needed, for example when the PV panel optimum voltage equals the DC-link voltage.

Voltage control tradeoff number 2 puts narrow limits on the number of PV cells in series connection. Freedom of scaling is important for building-integrated PV. For small systems with a low number of paralleled strings, the fixed string size may be difficult to scale. On the other hand, for large systems consisting of a high number of paralleled strings, the system can be scaled by the number of parallels. A fixed number of cells in each string then does not represent a major limitation. The limited range voltage control principle is thus best suited for the paralleling of several PV panel strings.

This parallel connection can be done in at least two different ways, as shown in Figure 21. Parallel connection on the PV panel side is one option, called the team concept. Real-time communication is then necessary for MPPT. Parameter inequalities and shading of the PV panel cells give different optimum operating voltages for the paralleled strings. The strings then do not work on their individual maximum power point, reducing the PV panel output unnecessary. The limitation concerning partial shading is believed to be the most important reason why this team concept has not been used more in buildings.

The paralleling of strings with independent DC/DC-converters for each string does not require communication for MPPT. In this case MPPT is possible using only locally measured current and voltage. It is robust concerning inequalities for the different strings due to cell parameter differences and partial shading, because the string voltages are controlled independently. The partial shading losses may be significant for building-integrated PV, but this depends on the specific building.

A system with limited range voltage control may in some designs require maximum system voltage rated semiconductors in order to be safe during startup or unexpected shutdown of parts of the converter system. For example, a short-circuit of the PV panel in the laboratory setup would cause the DC-link voltage to be applied over the normally low-voltage switching transistor, if not properly secured by a diode. Startup of the system when the DC-link voltage is zero, results in the input voltage over this switch. All the switches in the DC/DC-converter are 800 V coolMOS switches, although the maximum expected DC-link voltage is 360 V. The limited range voltage control is thus not connected to the switch voltage rating, but only to the inductors and the thermal management. Using full voltage rated switches reduces the efficiency compared to using low voltage switches. The efficiency still is expected to be significantly higher compared to a standard DC/DC-converter with full range voltage control.

Limiting the voltage control range of a PV-panel connected DC/DC-converter, makes it harder or impossible to detect shaded or damaged PV cells. A standard full voltage regulating range converter can detect unexpected partial shading or damaged PV panel cells, if implemented in software. Such a detection mechanism may be implemented by measuring the complete IV-curve, and look for local maxima. These local maxima are most probably caused by some bypass diodes being activated, shorting some cells above a certain current. In the single-shadowed cell measurement presented here, there is only one global maximum. It is, however, placed unexpectedly far away from the open-circuit voltage. This unexpected location of the MPP can also be used for the detection of PV panel failures. These methods of discovering single cell shadowing or failure are impossible to use reliably for a converter that cannot control the input voltage in the area of the actual MPP. A converter having limited range input voltage control thus cannot detect such situations. The probability of a PV panel failure is small due to the 20 years guarantee of PV panels given by most manufacturers. Unexpected partial shading is difficult to differentiate from expected partial shading due to for example flag poles. The loss of such a measurement method is probably of little significance.

The laboratory setup DC/DC-converter is designed to control the PV panel voltage ±20 % of DC-link voltage. Being able to control in both directions is different from other publications about limited range voltage control. The power supply simulating the PV-panel has a maximum power output of 3 kW. However, the flyback topology does have power limitations. The converter is thus designed for a power output of 1.7 kW, but it was never tested at more than 1.2 kW. For a string of series-connected PV cells, this is a sufficient power output. It was also sufficient for the anti-islanding testing of the DG system.

In order to justify the use of a DC/DC-converter for MPPT, the efficiency must be high. MPPT is most useful where the PV panel voltage varies a lot, which is mainly a result of temperature variance. DC/DC-converters with limited range voltage control can give higher efficiencies and smaller sizes, but they put limitations on the number of series-connected PV cells in each string. In order to avoid large partial shading losses,

independent control of every parallel string is best. The limited range voltage control DC/DC-converter is suitable for this application.

4 Inverter modeling and simulation

The inverter is controlled using an observer. It is a model of the physical process (inverter, LCL-filter and grid). Developing a good model of the inverter including the LCL-filter and the grid is therefore important. This chapter describes the applied mathematical models. The models are developed in the continuous time domain, and then implemented in the discrete time domain.

Due to the dual function of the inverter (both grid-connected and standalone), the filter cannot be an L-filter, so an LCL-filter is chosen. This can handle diode-rectifier load, which cycles between nearly short-circuit and open-circuit during one fundamental frequency period. In order to block the 3rd harmonic current of a symmetric diode rectifier load, the neutral wire is left disconnected. The current DC component is neglected. Also the voltage DC component is neglected because line voltages, not phase voltages, are measured.

A method for cancelling undesirable effects of switching ripple in the measured variables is presented. Based on analog integration it introduces a time delay. This is more clearly defined compared to hall-effect sensors which have a phase shift. This measurement method is used for the fastest dynamics only, which are the LCL-filter measurements. Hall-effect sensors are used for the grid voltage measurements which contain less switching ripple.

All models presented are based on the stationary frame. The models are presented starting from the LCL-filter, and eventually including a 3-phase grid model. Observability is verified, and the discretization method of the model and the observer is presented. Matlab/simulink models are used for verifying the discrete observer.

4.1 Inverter

A grid connected inverter is necessary in all DG including a DC energy source (photovoltaic panels, fuel cells or rectified AC in for example wind turbines). The most common topology is a 2-level voltage source inverter (VSI), as shown in Figure 30.
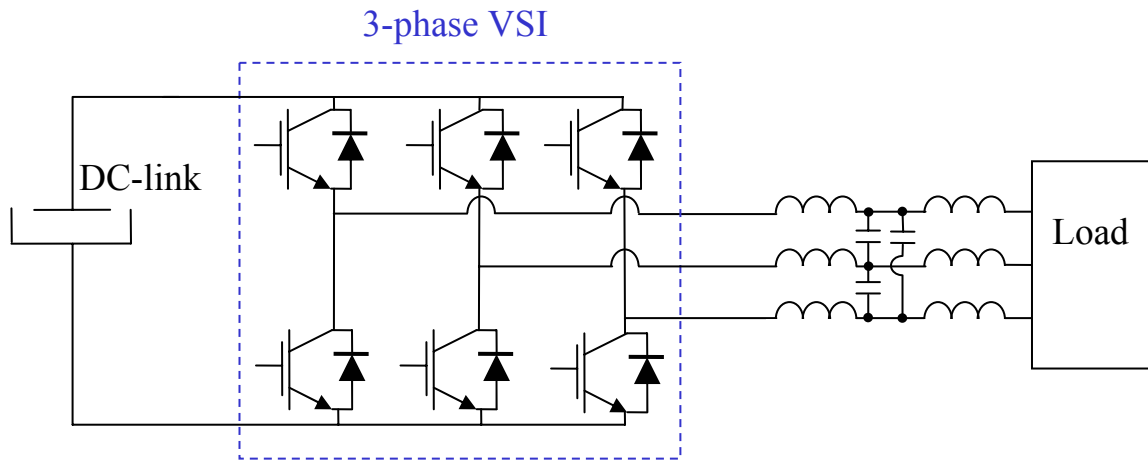
Figure 30: Voltage-source inverter topology with an LCL-filter.

The VSI has many possibilities concerning functionality due to its fast response. Its main objective in this thesis is to run both standalone and grid connected. The VSI is connected to the 3-phase grid without the use of a transformer, but only using an LCL-filter.

4.1.1 LCL-filter

The purpose of the LCL-filter is to block the switching frequency, but pass the 50 Hz component. The inductor closest to the VSI should pass some low-order harmonics (3rd, 5th and 7th) in order to mirror the grid voltage at the filter capacitor. The LCL-filter was designed to supply a diode-rectifier load, which consumes harmonic currents. The filter should not have too large inductors. On the other hand it should be sufficiently large for the 10 kHz digital controller to reject the LCL-filter resonance satisfactorily. The LCL-filter is shown in Figure 31.
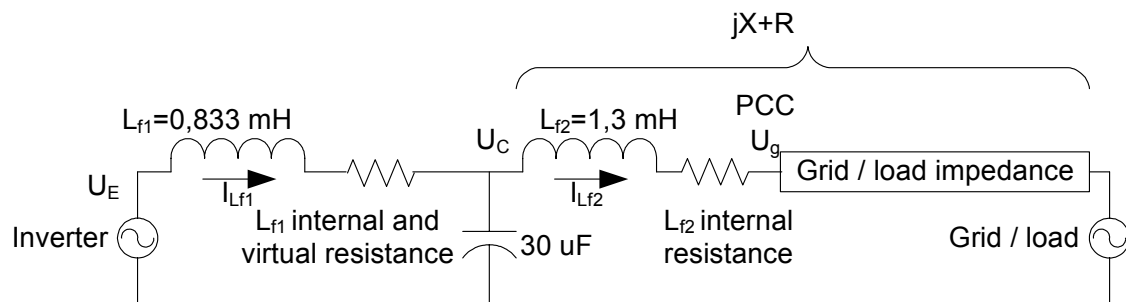
Figure 31: The inverter and the LCL-filter used for grid connection. L_{f1} is 2.47 % in pu, and L_{f2} is 3.85 % in pu. C_f produces 0.1 pu of reactive power under nominal conditions.

The LCL-filter should have low losses, equivalent with a high quality factor Q. The resonance peak must then be damped by the digital controller. In order to do so, the

resonance frequency must be within the bandwidth of the controller. The resonance frequency must be lower than half the sampling frequency, which in this case equals the switching frequency. For open-circuited operation, the LCL-filter resonance frequency is given by

$$f_{0,LCL,OC} = \frac{1}{2 \cdot \pi \sqrt{L_{f1} \cdot C_f}} \tag{4.1}$$

When a stiff voltage source such as the grid is connected, the resonance frequency is influenced by the grid impedance, here assumed equal to L_{f2}:

$$f_{0,LCL,SC} = \frac{1}{2 \cdot \pi \sqrt{\dfrac{L_{f1} \cdot L_{f2}}{L_{f1} + L_{f2}} C_f}} \tag{4.2}$$

The effect of the two inductors, L_{f1} and L_{f2}, on the resonance frequency is that of a parallel connection of the two. The difference in resonance frequency between grid-connected and grid-disconnected mode is low using a large L_{f2}. The inner inductor, L_{f1}, then dominates the resonance frequency.

In this thesis EMI around the switching frequency is neglected, but low-frequency harmonics (3rd, 5th and 7th) are included. The inner inductor, L_{f1}, was chosen equal to 0.833 mH (0.0247 pu), and the grid-connected inductor L_{f2}, was chosen equal to 1.3 mH (0.0385 pu). A low inner inductance can give the filter capacitor voltage fast response. The larger grid-connected inductance limits the high-frequency disturbance from the grid, so that it is within the controller bandwidth. It also gives a current that is less sensitive to filter capacitor voltage errors and hence more sinusoidal grid currents. Choosing a large filter capacitor (0.1 pu) reduces the necessary current-feedback for a given damping ratio in the case of continuous-time state-feedback.

4.1.2 Transient faults < 30 ms

The filter capacitor voltage is subject to control, both every switching cycle (every 0.1 millisecond), and for the reactive power compensation (every millisecond). This filter capacitor voltage may experience fewer disturbances than the grid connection. Whether the critical load experiences grid transient faults, depends on how it is connected to the grid. In the current setup, the grid connection and the critical load share the filter inductor L_{f2}. This gives no protection from transient faults that are faster than the time to disconnect the grid (the electromechanical contactor opening time in this case). On the other hand if the critical load is connected to the filter capacitor either directly or through a separate inductor L_{load}, the fastest grid transients are reduced through the grid connection inductor L_{f2}. This is shown in Figure 32.
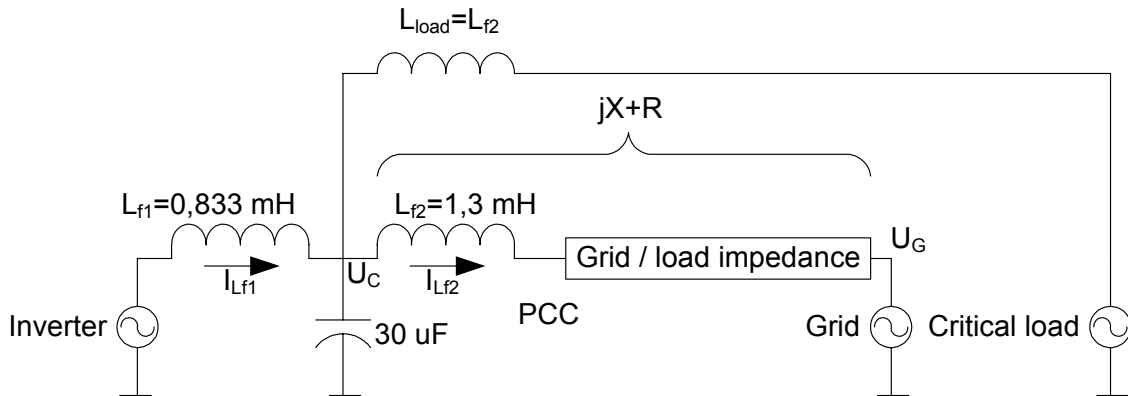
Figure 32: A possible setup that provides better protection of the critical load against transient grid failures than the experimental setup.

4.1.3 Integrating isolation circuit

An integrating measurement card was developed due to a large ripple current through the inductor L_{f1}. Assumingly the ripple current may cause measurement problems using Hall-effect sensors. They have a finite response time, which adds to the timing errors already induced by the ADC conversion time and analog filters. It is also impossible to sample both in the middle of the current triangle waveform and in the middle of the voltage ripple waveform. This is because they are 90º phase shifted as shown in Figure 33.

a)
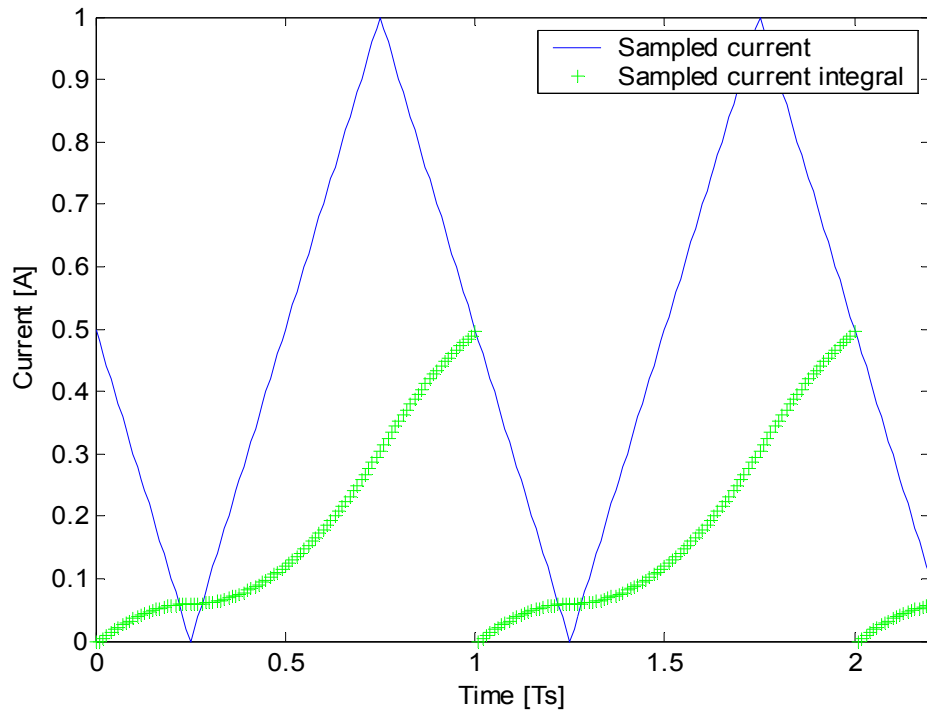
b)
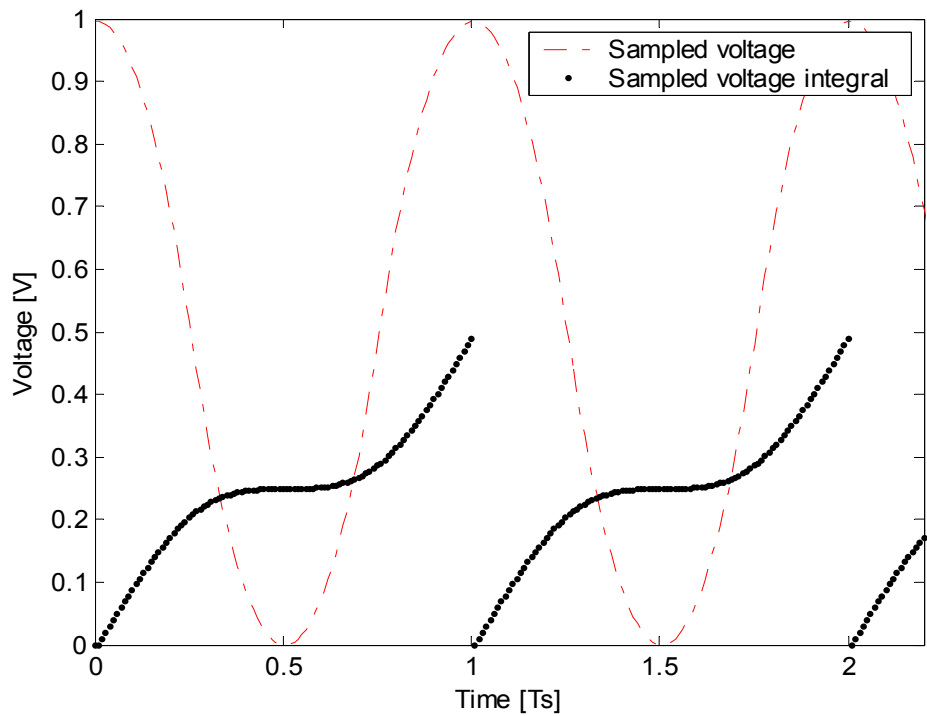
Figure 33: Inductor current (a, blue line) and capacitor voltage (b, red dotted line), both assuming 100% ripple. Using an analog integrator which is reset every switching cycle gives a measurement unaffected by phase. Green crosses are current and black dots are voltage integration, which are sampled and reset every switching cycle.

Integration of the measurement over one switching cycle avoids these phase problems, also described by Mertens and Eckardt [35]. The error otherwise caused by (non-integrating) measurement timing error is shown in Figure 34.
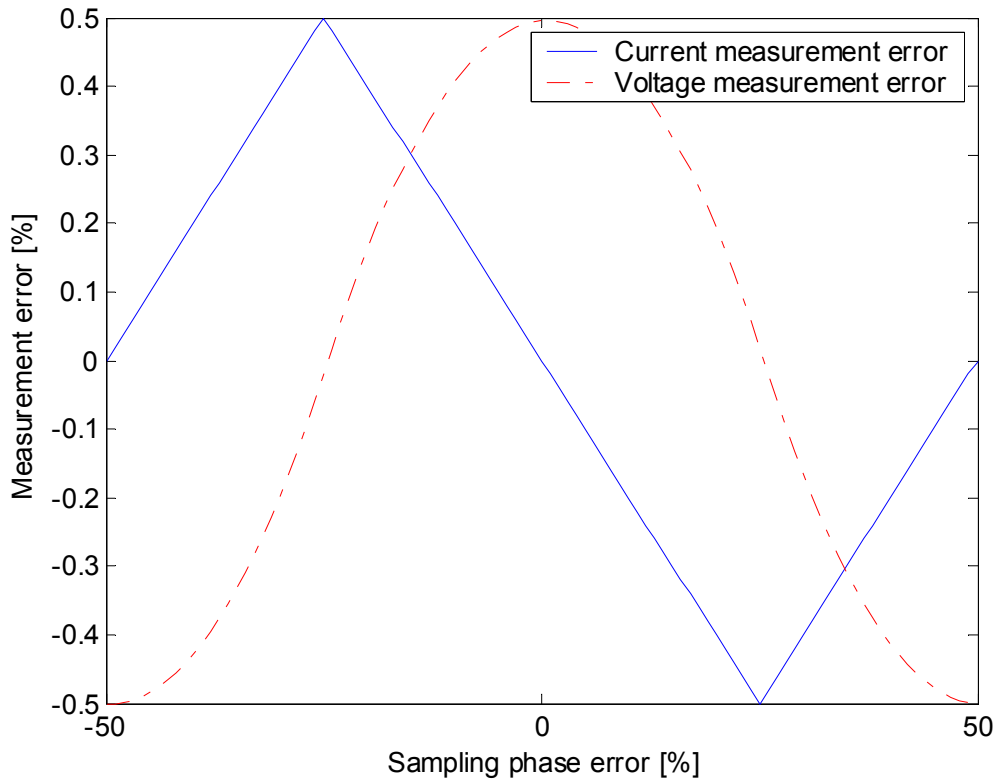
Figure 34: Measurement error caused by timing inaccuracies when not using an integrating measurement.

The integration adds half a sampling period of extra time delay. This is well-defined and thus makes it possible to model more accurately. The linearized optocoupler Siemens IL300 can be used as an ideal current source according to the PV cell model in Chapter 3. Connecting this to a capacitor with a reset circuit gives an integrating isolation circuit, shown in Figure 35.
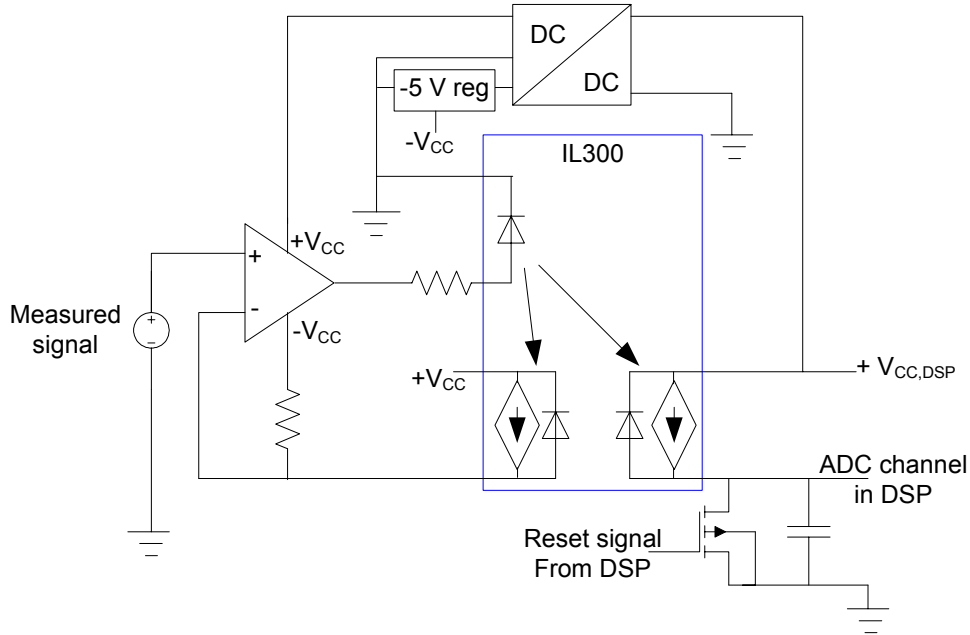
Figure 35: The integrating isolation circuit.

The 2-level 3-phase inverter is a source of common-mode noise. The integrating current measurement circuit had high sensitivity to this noise. A common-mode filter in the form of iron-powder toroids were therefore used to reduce the common-mode current through the LCL-filter.

4.1.4 3-phase transformations

In this work the stationary frame is applied instead of the rotating frame often used (dq0-coordinates). There are two different scaling options of the orthogonal αβ-coordinates: one which conserves the power, and another that conserves the amplitude. The latter is used in this thesis, so that $I_a = I_\alpha$. This simplifies the calibration of the measurements.

The rotation matrices used in order to transform the 3-phase parameters to the orthogonal axes are given in the following text. A thorough description of the rotation matrices can be found in [36], and in Appendix C. Let phase voltage be defined as the vector

$$u_{phase} = \begin{bmatrix} u_a & u_b & u_c \end{bmatrix}^T \tag{4.3}$$

The line voltage is defined as the vector

$$u_{line} = \begin{bmatrix} u_{bc} & u_{ca} & u_{ab} \end{bmatrix}^T \tag{4.4}$$

The stationary frame αβ-coordinates are fixed in orthogonal axis, where α is in phase with the a-phase. The transformation is given as:

$$u_{\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & -\dfrac{1}{2} & -\dfrac{1}{2} \\ 0 & \dfrac{\sqrt{3}}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \cdot u_{phase} \tag{4.5}$$

The voltages in this setup are measured as line voltages. It is therefore necessary to present the transformation between line voltages and the stationary frame:

$$u_{\alpha\beta} = \begin{bmatrix} 0 & -\dfrac{1}{3} & \dfrac{1}{3} \\ \dfrac{2}{3\sqrt{3}} & \dfrac{-1}{3\sqrt{3}} & \dfrac{-1}{3\sqrt{3}} \end{bmatrix} \cdot u_{line} \tag{4.6}$$

Based on this stationary frame model, a state-space representation of the system can be developed.

4.2 LCL-filter and grid voltage model

Developing a model-based state observer and predictor is the aim of this section. First the LCL-filter state-space representation is presented, and then the grid voltage state-space representation is included. Transformation to the discrete time domain is shown, and verified through simulations.

Given an accurate model of the process to be controlled, it is possible to filter measurements according to the physical properties of the process. The models to be presented include the LCL-filter. This has been presented in many publications, for example [37]. The differential equation for the current through the filter inductor L_{f1} is given by the voltage over it, and the internal resistance.

$$\dot{i}_{Lf1} = \frac{u_E - u_C - R_{Lf1} \cdot i_{lf1}}{L_{f1}} \tag{4.7}$$

The differential equation for the current through the filter inductor L_{f2} can be expressed in a similar way

$$\dot{i}_{Lf2} = \frac{u_C - u_g - R_{Lf2} \cdot i_{Lf2}}{L_{f2}} \tag{4.8}$$

The differential equation for the voltage over the filter capacitor C_f is given by the net current flowing into it. Capacitor losses are neglected.

$$\dot{u}_c = \frac{i_{Lf1} - i_{Lf2}}{C_f}$$

(4.9)

The Equations (4.7)-(4.9) can be ordered in a state-space form so that the set of equations can be expressed as:

$$\dot{x}_{LCL} = A_{LCL}x_{LCL} + B_{LCL}u_E$$
$$y_{LCL} = C_{LCL}x_{LCL}$$

(4.10)

where x_{LCL} is the states of the LCL-filter:

$$x_{LCL} = \begin{bmatrix} u_C & i_{Lf1} & i_{Lf2} \end{bmatrix}^T$$

(4.11)

y_{LCL} is the measurement vector:

$$y_{LCL} = \begin{bmatrix} u_C & i_{Lf1} \end{bmatrix}^T$$

(4.12)

A_{LCL} represents the zero input response. B_{LCL} represents the zero state response. C_{LCL} couples the system states x_{LCL} to the measurements y_{LCL}. The system matrices A_{LCL}, B_{LCL} and C_{LCL} are defined as:

$$A_{LCL} = \begin{bmatrix} 0 & \dfrac{1}{C_f} & \dfrac{-1}{C_f} \\ \dfrac{-1}{L_{f1}} & \dfrac{-R_{f1}}{L_{f1}} & 0 \\ \dfrac{1}{L_{f2}} & 0 & \dfrac{-R_{f2}}{L_{f2}} \end{bmatrix}, \quad B_{LCL} = \begin{bmatrix} 0 \\ \dfrac{1}{L_{f1}} \\ 0 \end{bmatrix}, \quad C_{LCL} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

(4.13)

This state-space representation of the LCL-filter is used in a state observer and in simulations. Scaling the model in per unit form is practical for implementation in a DSP. The base voltage is

$$u_{base} = \frac{u_n}{\sqrt{3}} = \frac{230}{\sqrt{3}} = 132.8 \text{ V}$$

(4.14)

All measured AC voltages are divided by this value. The base current is

$$i_{base} = \frac{S_n}{u_n \sqrt{3}} = \frac{5000}{230\sqrt{3}} = 12.55 \text{ A} \tag{4.15}$$

All measured currents are divided by this value. The base impedance is:

$$z_{base} = \frac{u_{base}}{i_{base}} = \frac{132.8}{12.55} = 10.58 \ \Omega \tag{4.16}$$

In per unit scaling the LCL-filter model can be defined as:

$$\dot{x}_{LCL} = A_{LCL,pu} x_{LCL} + B_{LCL,pu} u_E \tag{4.17}$$

The system matrices are then redefined.

$$A_{LCL,pu} = \begin{bmatrix} 0 & \dfrac{1}{C_f z_{base}} & \dfrac{-1}{C_f z_{base}} \\ \dfrac{-z_{base}}{L_{f1}} & \dfrac{-R_{f1}}{L_{f1}} & 0 \\ \dfrac{z_{base}}{L_{f2}} & 0 & \dfrac{-R_{f2}}{L_{f2}} \end{bmatrix}, \quad B_{LCL,pu} = \begin{bmatrix} 0 \\ \dfrac{z_{base}}{L_{f1}} \\ 0 \end{bmatrix} \tag{4.18}$$

This scaled model is used for developing the discrete time domain model used for practical observer and predictor implementation.

4.2.1 Single phase LCL-filter and grid model

The grid phase and amplitude are often measured using a Phase-Locked-Loop (PLL) in addition to voltage measurements. That approach is useful when the rotating frame (dq0) is applied. However, the stationary frame (αβ) is utilized in this work. A grid voltage observer is then more suitable.

The grid observer technique is based on an LC-filter model with the resonance frequency ω_0=314 rad/s. This has been investigated for monitoring purposes by Girgis et al. [38]. The model can be expanded to include imbalanced and harmonically distorted grid conditions. It can also be used for inverter control using Kalman filter, which has been presented by Bolsens et al. [39, 40]. The oscillator has zero stationary error at the resonant frequency. Similar structures have been called a generalized integrator by Yuan et al. [41] and Liserre et al. [42], but applied to current control. A

single-phase version will first be presented. A three phase model will then be studied in the stationary frame with two orthogonal axes. Finally harmonic distortion will be included.

Exploiting the fact that a rotation can be represented as an oscillation, the observer model shown in Figure 36 can be used.
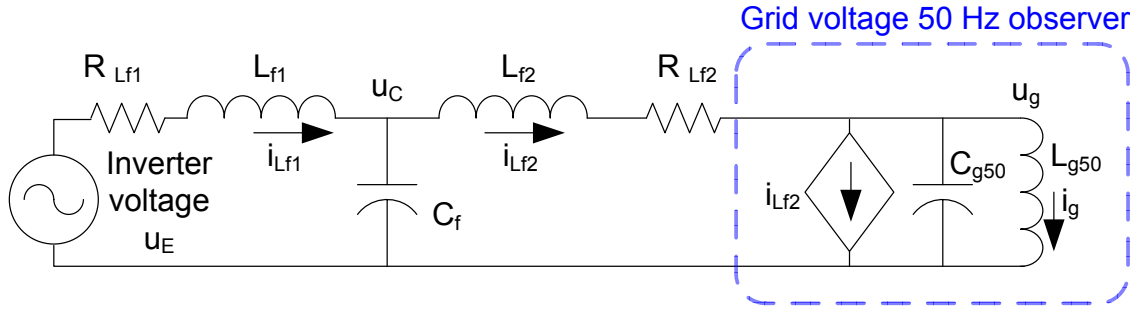
Figure 36: Schematic illustration of the model behind the observer. C_{g50} and L_{g50} are not physical components, but they represent the observer.

The grid is modeled as an LC-filter with $|L_{g50}| = |C_{g50}| = 0.00318$, so that the resonance frequency $\omega_0 = 314$ rad/s. When grid connected, the inverter feeds power to the grid. This is not always true when the system is in UPS algorithm or in voltage support algorithm. The control algorithm should not affect the grid model. Therefore a current controlled source which tracks the current i_{Lf2} is used in the grid model. This gives a grid model that is unaffected by the current fed through L_{f2}. The grid model can be expressed by two coupled differential equations. They give a fully autonomous (not controllable) grid model:

$$\dot{u}_g = \frac{-i_g}{C_{g50}} + \frac{i_{Lf2} - i_{Lf2}}{C_{g50}} \tag{4.19}$$

$$\dot{i}_g = \frac{u_g}{L_{g50}} \tag{4.20}$$

The grid can then be described in state-space form as shown in Equation (4.21):

$$\dot{x}_g = A_g x_g + B_g u_E$$
$$y_g = C_g x_g \tag{4.21}$$

where:

$$x_g = \begin{bmatrix} u_g \\ i_g \end{bmatrix}, \qquad A_g = \begin{bmatrix} 0 & \dfrac{-1}{C_{g50}} \\ \dfrac{1}{L_{g50}} & 0 \end{bmatrix}, \qquad B_g = 0, \qquad C_g = \begin{bmatrix} 1 & 0 \end{bmatrix} \qquad (4.22)$$

The matrix A_g can be rewritten to

$$A_g = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \qquad (4.23)$$

where ω is the system angular frequency (314 rad/s). Now the two parts, the LCL-filter and the grid observer, can be combined in Equation (4.27), using the system matrices (4.25) in the state-space form given in Equation (4.24). The combined system for single-phase must also include the influence of u_g on i_{Lf2} shown also in Equation (4.8).

$$\dot{x}_{1\text{-ph}} = A_{1\text{-ph}} x_{1\text{-ph}} + B_{1\text{-ph}} u_E$$
$$y_{1\text{-ph}} = C_{1\text{-ph}} x_{1\text{-ph}} \qquad (4.24)$$

where:

$$x_{1\text{-ph}} = \begin{bmatrix} x_{LCL} \\ x_g \end{bmatrix}, \quad A_{1\text{-ph}} = \begin{bmatrix} & & 0 & 0 \\ A_{LCL} & & 0 & 0 \\ & & \dfrac{-1}{L_{f2}} & 0 \\ 0 & & A_g \end{bmatrix}, \quad B_{1\text{-ph}} = \begin{bmatrix} B_{LCL} \\ B_g \end{bmatrix}, \quad C_{1\text{-ph}} = \begin{bmatrix} C_{LCL} & 0 \\ 0 & C_g \end{bmatrix} \qquad (4.25)$$

Collecting the terms gives the complete system matrices shown in Equations (4.26)-(4.30). The system states are defined as:

$$x_{1\text{-ph}} = \begin{bmatrix} u_C & i_{Lf1} & i_{Lf2} & u_g & i_g \end{bmatrix}^T \qquad (4.26)$$

The system zero input response matrix is given as:

$$
A_{\text{1-ph}} = \begin{bmatrix} 0 & \dfrac{1}{C_f} & \dfrac{-1}{C_f} & 0 & 0 \\[2mm] \dfrac{-1}{L_{f1}} & \dfrac{-R_{f1}}{L_{f1}} & 0 & 0 & 0 \\[2mm] \dfrac{1}{L_{f2}} & 0 & \dfrac{-R_{f2}}{L_{f2}} & \dfrac{-1}{L_{f2}} & 0 \\[2mm] 0 & 0 & 0 & 0 & -\omega \\[2mm] 0 & 0 & 0 & \omega & 0 \end{bmatrix} \tag{4.27}
$$

The zero state input response is given by:

$$
B_{\text{1-ph}} = \begin{bmatrix} 0 & \dfrac{1}{L_{f1}} & 0 & 0 & 0 \end{bmatrix}^{T} \tag{4.28}
$$

The measurement vector is defined as:

$$
y_{\text{1-ph}} = \begin{bmatrix} u_C & i_{Lf1} & u_g \end{bmatrix}^{T} \tag{4.29}
$$

Not all states are measured, and this is given by:

$$
C_{\text{1-ph}} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \tag{4.30}
$$

The system is observable but not all states are controllable. The inverter is assumed to have a negligible effect on the grid voltage.

4.2.2 Three phase LCL filter model

The single-phase model can easily be expanded to a 3-phase model, where each of the two orthogonal axes is modeled separately. Eventual imbalance as well as both directions of rotation can then be estimated. The number of states of the observer is thus doubled compared to the single-phase case. The system matrices are shown in Equations (4.31)-(4.37). The system can be described in state-space form:

$$\begin{aligned}\dot{x}_{\alpha\beta,LCL} &= A_{\alpha\beta,LCL}x_{\alpha\beta,LCL} + B_{\alpha\beta,LCL}u_{E,\alpha\beta} \\ y_{\alpha\beta,LCL} &= C_{\alpha\beta,LCL}x_{\alpha\beta,LCL}\end{aligned} \tag{4.31}$$

where the state vector is:

$$x_{\alpha\beta,LCL} = \begin{bmatrix} u_{C,\alpha} & u_{C,\beta} & i_{Lf1,\alpha} & i_{Lf1,\beta} & i_{Lf2,\alpha} & i_{Lf2,\beta} \end{bmatrix}^{\mathrm{T}} \tag{4.32}$$

The applied voltage is defined as:

$$u_{E,\alpha\beta} = \begin{bmatrix} u_{E,\alpha} & u_{E,\beta} \end{bmatrix}^{\mathrm{T}} \tag{4.33}$$

The system zero input matrix is given as:

$$A_{\alpha\beta,LCL} = \begin{bmatrix} 0 & 0 & \dfrac{1}{C_f} & 0 & \dfrac{-1}{C_f} & 0 \\[2mm] 0 & 0 & 0 & \dfrac{1}{C_f} & 0 & \dfrac{-1}{C_f} \\[2mm] \dfrac{-1}{L_{f1}} & 0 & \dfrac{-R_{f1}}{L_{f1}} & 0 & 0 & 0 \\[2mm] 0 & \dfrac{-1}{L_{f1}} & 0 & \dfrac{-R_{f1}}{L_{f1}} & 0 & 0 \\[2mm] \dfrac{1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-R_{f2}}{L_{f2}} & 0 \\[2mm] 0 & \dfrac{1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-R_{f2}}{L_{f2}} \end{bmatrix} \tag{4.34}$$

The effect of the applied voltage is given by the matrix:

$$B_{\alpha\beta,LCL} = \begin{bmatrix} 0 & 0 & \dfrac{1}{L_{f1,\alpha}} & 0 & 0 & 0 \\[3mm] 0 & 0 & 0 & \dfrac{1}{L_{f1,\beta}} & 0 & 0 \end{bmatrix}^T \tag{4.35}$$

The measurements are defined as:

$$y_{\alpha\beta,\text{LCL}} = \begin{bmatrix} u_{C,\alpha} & u_{C,\beta} & i_{Lf1,\alpha} & i_{Lf1,\beta} \end{bmatrix}^T \tag{4.36}$$

The states measured are defined by the matrix:

$$C_{\alpha\beta,LCL} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \tag{4.37}$$

A similar expansion can be performed for the grid model.

4.2.3 Three phase grid including 5th and 7th harmonic

The grid voltage is a dominating 50 Hz, but the grid is often polluted by 5th, 7th and higher harmonic components (3-wire 3-phase system). The grid model can include these lowest dominating harmonics. Including these frequency components gives a better tracking of the first harmonic. The main purpose of estimating the grid voltage harmonics is to decouple the most common harmonics from the grid current using feed-forward as described in Chapter 5.

Due to the fact that all variables are represented in a standard state-space form, standard control theory can be applied such as pole assignment. It is a simpler method compared to the Kalman filter of Bolsens et al. [39, 40]. Both methods are based on a stationary frame model. Figure 37 shows a circuit-scheme representation of the grid voltage observer used in this thesis.
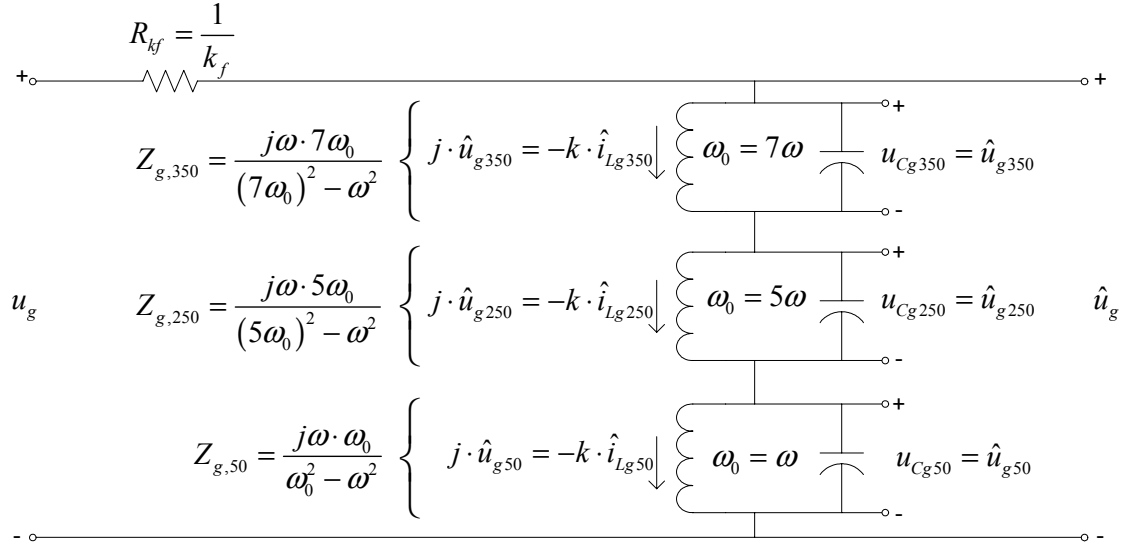
Figure 37: Circuit-scheme representation of the grid voltage observer, including the 5th and 7th harmonics.

The resistance R_{kf} represents the inverse observer feedback gain k_f which in the Figure 37 is equal for the three frequencies in question. However, the observer can have different feedback gains for each frequency in question. As there is no evident reason why different gains should be selected, equal gain for all three frequencies is chosen during the rest of this work. The constant k for extracting the imaginary component of the estimated voltage depends on the scaling of the model. The grid model is not pu scaled, even though the input voltage is scaled. This gives equal amplitudes of the pu currents and voltages. The constant k then equals one.

The correctness of the observer can be shown by calculating the frequency response of the electrical circuit in Figure 37. The estimated voltage for a given frequency can be calculated for the voltage divisor represented by the first harmonic impedance Z_{g50}, the fifth Z_{g250}, the seventh Z_{g350} and the inverse observer feedback gain R_f:

$$\hat{u}_{g50} = \frac{Z_{g50}}{Z_{g50} + Z_{g250} + Z_{g350} + R_f} u_g \tag{4.38}$$

At the resonance frequency when $\omega = \omega_0$, the equivalent impedance Z_{g50} approaches infinity. Hence, the estimated frequency component approaches the grid voltage

$$\hat{u}_{g50} = \lim_{\omega \to \omega_0} \frac{Z_{g50}}{Z_{g50} + Z_{g250} + Z_{g350} + R_f} u_{g,50} = \frac{j\infty}{j\infty + Z_{g250} + Z_{g350} + R_f} u_{g,50} = u_{g,50} \tag{4.39}$$

The influence of one frequency on the others can be shown similarly. For example, the influence of the fundamental component on the fifth harmonic observer can be calculated. The voltage division is applied to the fifth harmonic component:

$$\hat{u}_{g250} = \frac{Z_{g250}}{Z_{g50} + Z_{g250} + Z_{g350} + R_f} u_g \tag{4.40}$$

When only the fundamental component is applied, the impedance Z_{g50} of the fundamental frequency component observer approaches infinity:

$$\hat{u}_{g250} = \lim_{\omega \to \omega_0} \frac{Z_{g250}}{Z_{g50} + Z_{g250} + Z_{g350} + R_f} u_{g,50} = \frac{Z_{g250}}{j\infty + Z_{g250} + Z_{g350} + R_f} u_{g,50} = 0 \tag{4.41}$$

The expression for the fifth harmonic estimation then approaches zero. Thus, there is no stationary coupling between the different harmonics of the continuous-time observer presented. Equation (4.42) shows the grid observer part of the state-space model. Due to its uncontrollability, the B-term is zero, and thus not included in the model.

$$\dot{x}_{gh} = A_{gh} x_{gh}$$
$$y_{gh} = C_{gh} x_{gh} \tag{4.42}$$

The grid observer state vector including fifth and seventh harmonics in both axes is defined as:

$$x_{gh} = \begin{bmatrix} u_{g50,\alpha} & i_{g50,\alpha} & u_{g50,\beta} & i_{g50,\beta} & u_{g250,\alpha} & i_{g250,\alpha} & u_{g250,\beta} & i_{g250,\beta} & u_{g350,\alpha} & i_{g350,\alpha} & u_{g350,\beta} & i_{g350,\beta} \end{bmatrix}^T \tag{4.43}$$

The system matrix is defined as:

$$
A_{gh} =
\begin{bmatrix}
0 & -\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -5\omega & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 5\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -5\omega & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 5\omega & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -7\omega & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 7\omega & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -7\omega \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 7\omega & 0
\end{bmatrix}
\tag{4.44}
$$

(Blocks: 50 Hz voltage model, 250 Hz voltage model, 350 Hz voltage model.)

The grid voltage is the sum of all estimated harmonic voltages:

$$
C_{gh} =
\begin{bmatrix}
1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0
\end{bmatrix}
\tag{4.45}
$$

A matrix for the influence of the grid voltage on the LCL-filter is defined:

$$
A_{gh \to LCL} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\dfrac{-1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 \\
0 & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-1}{L_{f2}} & 0
\end{bmatrix}
\tag{4.46}
$$

Combining the grid model with the LCL-filter model gives the final, 18-state observer:

$$\dot{x} = Ax + Bu_{E,\alpha\beta}$$
$$y = Cx$$

(4.47)

The measurement vector is defined as a combination of the measurements from the LCL-filter and the grid:

$$x = \begin{bmatrix} x_{\alpha\beta,LCL} & x_{gh} \end{bmatrix}^T$$

(4.48)

Applied voltage vector for the two axes is defined as:

$$u_{E,\alpha\beta} = \begin{bmatrix} u_{E,\alpha} & u_{E,\beta} \end{bmatrix}^T$$

(4.49)

The combined system is given as:

$$A = \begin{bmatrix} A_{\alpha\beta,LCL} & A_{gh\rightarrow LCL} \\ 0 & A_{gh} \end{bmatrix}, \quad B = \begin{bmatrix} B_{\alpha\beta,LCL} \\ 0 \end{bmatrix}, \quad C = \begin{bmatrix} C_{\alpha\beta,LCL} & 0 \\ 0 & C_{gh} \end{bmatrix}, \quad D = 0$$

(4.50)

The detailed complete expression is then shown in Equations (4.51)-(4.54). The state vector is defined as:

$$x = \begin{bmatrix} u_{C,\alpha} & u_{C,\beta} & i_{Lf1,\alpha} & i_{Lf1,\beta} & i_{Lf2,\alpha} & i_{Lf2,\beta} & u_{g50,\alpha} & i_{g50,\alpha} & u_{g50,\beta} \\ i_{g50,\beta} & u_{g250,\alpha} & i_{g250,\alpha} & u_{g250,\beta} & i_{g250,\beta} & u_{g350,\alpha} & i_{g350,\alpha} & u_{g350,\beta} & i_{g350,\beta} \end{bmatrix}^T$$

(4.51)

The system matrix is defined as a composite of the LCL-filter and the grid:

$A =$

$$A = \begin{bmatrix}
0 & \dfrac{1}{C_f} & 0 & \dfrac{-1}{C_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \dfrac{1}{C_f} & 0 & \dfrac{-1}{C_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\dfrac{-1}{L_{f1}} & 0 & \dfrac{-R_{f1}}{L_{f1}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \dfrac{-1}{L_{f1}} & 0 & \dfrac{-R_{f1}}{L_{f1}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\dfrac{1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-R_{f2}}{L_{f2}} & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 \\
0 & \dfrac{1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-R_{f2}}{L_{f2}} & 0 & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-1}{L_{f2}} & 0 & 0 & 0 & \dfrac{-1}{L_{f2}} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & \omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -5\omega & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 5\omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -5\omega & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 5\omega & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -7\omega & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 7\omega & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -7\omega \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 7\omega & 0
\end{bmatrix}$$

LCL-filter model (red dashed block). Grid voltage model (blue dashed block): 50 Hz, 250 Hz, 350 Hz sub-blocks.

(4.52)

The applied voltages influence is defined by the matrix B:

$$B = \begin{bmatrix}
0 & 0 & 0 & 0 & \dfrac{1}{L_{f2}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \dfrac{1}{L_{f2}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}^T$$

(4.53)

The measurement matrix defines measurements of filter capacitor voltage, filter inductor currents, and grid voltage for both axes:

$$
C = \begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0
\end{bmatrix}
\tag{4.54}
$$

The presented continuous-time model is described with two independent systems, one for each axis. It does not include the coupling between reactive current in the α-axis and active current in the β-axis, for example. Compensation of such coupling is easier to do in the rotating frame.

4.2.4 Observability

The knowledge of the system dynamics can be exploited in a state-space observer to filter noise, compensate time delays, and to estimate states not measured directly, such as harmonic voltages. The structure of the continuous-time domain observer is shown in Figure 38.
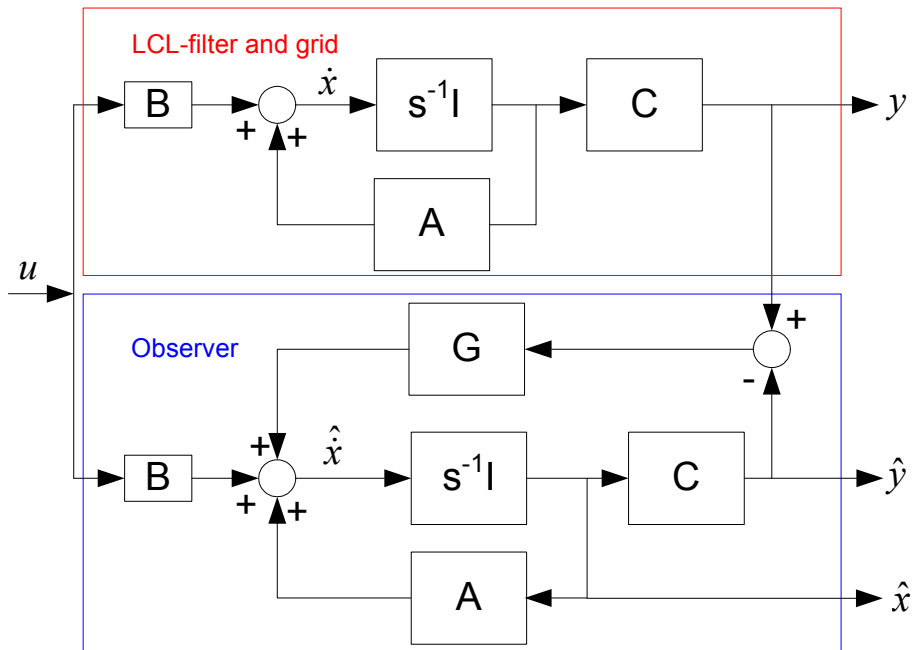
Figure 38: State space observer for the LCL-filter and the grid voltage.

The complete model developed is only useful if it is observable. If there are enough measurements to determine the initial conditions in finite time, the model is observable. Observability can be checked using the rank of the observability matrix defined as [43]:

$$O = \begin{bmatrix} C \\ CA \\ \vdots \\ CA^{n-1} \end{bmatrix} \tag{4.55}$$

where the measurement matrix C and the zero input response matrix A is from the state-space structure presented earlier in this section. If the rank is equal or higher than the number of states n, the system is observable. This definition can also be found in [44]. The system presented here consists of two single-phase models without interactions. The observability can thus be checked only considering one axis. Each of these axes consists of two parts, the LCL-filter and the grid observer. These two parts will first be treated separately, with fewer measurements than used in the laboratory. Even though more measurements were used in the experiments, fewer measurements are assumed to show how few measurements are enough in theory. This section will end by evaluating the observability of the whole system with only one measurement (i_{Lf1}).

The grid voltage observer consists of three oscillators, where the measured voltage is the sum of all three frequency components. The measurement matrix is then:

$$C_{O,g} = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{4.56}$$

A single-axis version of Equation (4.44) is shown in Equation (4.57). The zero-input response matrix $A_{O,g}$ observing first, fifth and seventh harmonic can be written as:

$$A_{O,g} = \begin{bmatrix} 0 & -\omega & 0 & 0 & 0 & 0 \\ \omega & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -5\omega & 0 & 0 \\ 0 & 0 & -5\omega & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -7\omega \\ 0 & 0 & 0 & 0 & -7\omega & 0 \end{bmatrix} \tag{4.57}$$

where $\omega = 314$ rad/s. The observability matrix O_g according to Equation (4.55) is then:

$$O_g = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & -\omega & 0 & -5\omega & 0 & -7\omega \\ -\omega^2 & 0 & -(5\omega)^2 & 0 & -(7\omega)^2 & 0 \\ 0 & \omega^3 & 0 & (5\omega)^3 & 0 & (7\omega)^3 \\ \omega^4 & 0 & (5\omega)^4 & 0 & (7\omega)^4 & 0 \\ 0 & -\omega^5 & 0 & -(5\omega)^5 & 0 & -(7\omega)^5 \end{bmatrix}$$ (4.58)

Rewriting the matrix in reduced echelon form reveals that the matrix has full rank:

$$O_g = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 5 & 0 & 7 \\ 0 & 0 & 1 & 0 & 2 & 0 \\ 0 & 0 & 0 & 1 & 0 & \dfrac{14}{5} \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$ (4.59)

All three harmonic voltages are observable by measuring the grid voltage. The observability of the LCL-filter is guaranteed measuring only the L_{fl} current. This can be shown by analyzing the observability matrix using only this measurement. In that case the measurement matrix is given by:

$$C_{O,LCL} = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix}$$ (4.60)

The system zero-input response matrix $A_{O,LCL}$ is equal to Equation (4.13):

$$A_{O,LCL} = \begin{bmatrix} 0 & \dfrac{1}{C_f} & \dfrac{-1}{C_f} \\ \dfrac{-1}{L_{f1}} & \dfrac{-R_{f1}}{L_{f1}} & 0 \\ \dfrac{1}{L_{f2}} & 0 & \dfrac{-R_{f2}}{L_{f2}} \end{bmatrix}$$ (4.61)

The observability matrix O_{LCL} is according to Equation (4.55):

$$O_{LCL} = \begin{bmatrix} 0 & 1 & 0 \\ \dfrac{-1}{L_{f1}} & \dfrac{-R_{f1}}{L_{f1}} & 0 \\ \dfrac{R_{f1}}{L_{f1}^2} & \dfrac{R_{f1}^2}{L_{f1}^2} - \dfrac{1}{C_f L_{f1}} & \dfrac{1}{C_f L_{f1}} \end{bmatrix} \qquad (4.62)$$

It can be rewritten in the reduced echelon form which has full rank:

$$O_{LCL} = \begin{bmatrix} 1 & R_{f1} & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \qquad (4.63)$$

The LCL-filter is thus observable. Combining the previously two systems, give a 9x9 observability matrix. The only measurement used in this proof, is the inductor L_{f1} current. The measurement matrix is then:

$$C_{1-ph,h} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \qquad (4.64)$$

Due to space limitations, the reduced echelon form is written directly:

$$O_{1-ph,h} = \begin{bmatrix} 1 & R_{f1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 5 & 0 & 7 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & \dfrac{14}{5} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \qquad (4.65)$$

The observability matrix has full rank. The complete system is thus observable with only the inductance L_{f1} current measurement. Also the filter capacitor voltage and the grid voltage are measured, thus representing redundancy and giving better estimates.

4.2.5 Discretization of the observer

The state observer is implemented in a digital signal processor, DSP. The first step towards a discrete time observer is to reduce the number of blocks in the block diagram previously shown in Figure 38. Estimating the measurement y is not necessary. Only the states x are estimated. The zero-input response of the observer can then be represented by the matrix F:

$$F = A - G \cdot C \tag{4.66}$$

The block diagram of the continuous-time observer is shown in Figure 39.
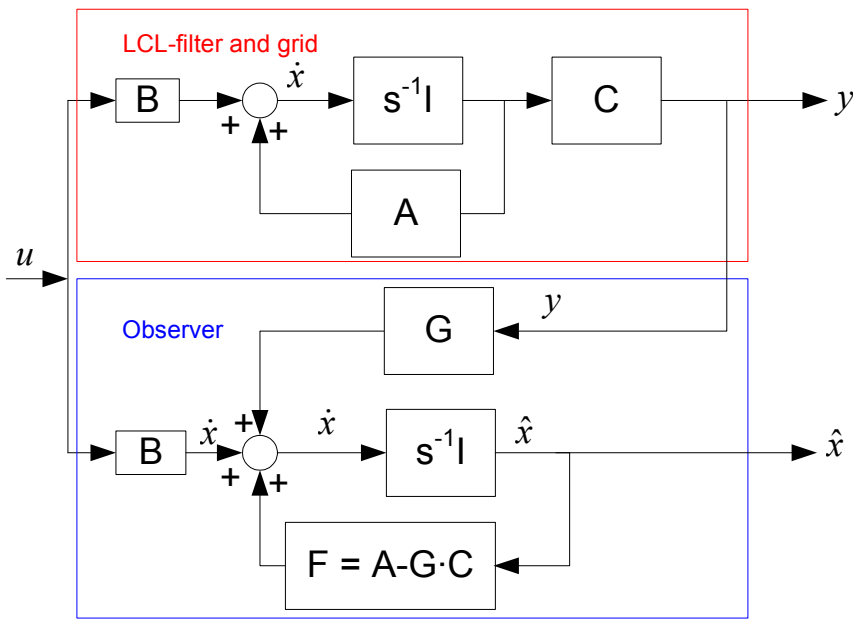
Figure 39: The continuous-time observer for the LCL-filter and the grid voltage.

A discretization method is used in order to make the transition from the time domain. The converter is switching at 10 kHz with the analog to digital converter, ADC, interrupt running synchronously. The discretization step, T_s, is 100 μs. The discrete-time model zero-input response matrix A_D is defined as:

$$A_D = e^{A \cdot T_s} \tag{4.67}$$

Equation (4.67) can be approximated by the infinite series [45]:

$$A_D = e^{A \cdot T_s} \approx 1 + \sum_{n=1}^{n=\infty} \frac{(A \cdot T_s)^n}{n!} \tag{4.68}$$

The 70 first additions are here used in the actual approximation. The zero-state response matrix B can be discretized as follows:

$$B_D = A^{-1} \left(e^{A \cdot T_s} + I \right) B \tag{4.69}$$

Combining Equation (4.69) with Equation (4.67), an infinite series approximation can be expressed for calculation of the discrete zero-state response matrix B_D:

$$B_D = \left\{ \sum_{n=1}^{n=\infty} \frac{A^{n-1} \cdot T_s^{\,n}}{n!} \right\} \cdot B \tag{4.70}$$

The observer can be designed in two different ways. One option is to use the discretized process, and then choose G_D. The observer will then be designed to fit a discrete system. For a real process including sample-and-hold circuits and fast dynamics, this solution guarantees that the separation theorem [46] holds in the discrete time domain.

The other option which does not guarantee the separation theorem, is to first design an observer in the continuous-time domain, including the feedback matrix G. Then the observer is discretized. This option has the benefit of implementing the equivalent circuit of the grid voltage observer previously described. It guarantees zero steady-state coupling between the different harmonics, which the first method does not.

The observer zero-input model is discretized in a similar manner as the discretization of the real process. The zero-input response matrix F is the only difference:

$$F_D = 1 + \sum_{n=1}^{n=\infty} \frac{\left(F \cdot T_s \right)^n}{n!} \tag{4.71}$$

The zero-input observer response is in this case changed:

$$H_D = \left\{ \sum_{n=1}^{n=\infty} \frac{F^{n-1} \cdot T_s^{\,n}}{n!} \right\} \cdot B \tag{4.72}$$

The observer gain is also discretized:

$$G_D = \left\{ \sum_{n=1}^{n=\infty} \frac{F^{n-1} \cdot T_s^{\,n}}{n!} \right\} \cdot G \tag{4.73}$$

The discrete observer is shown in Figure 40.
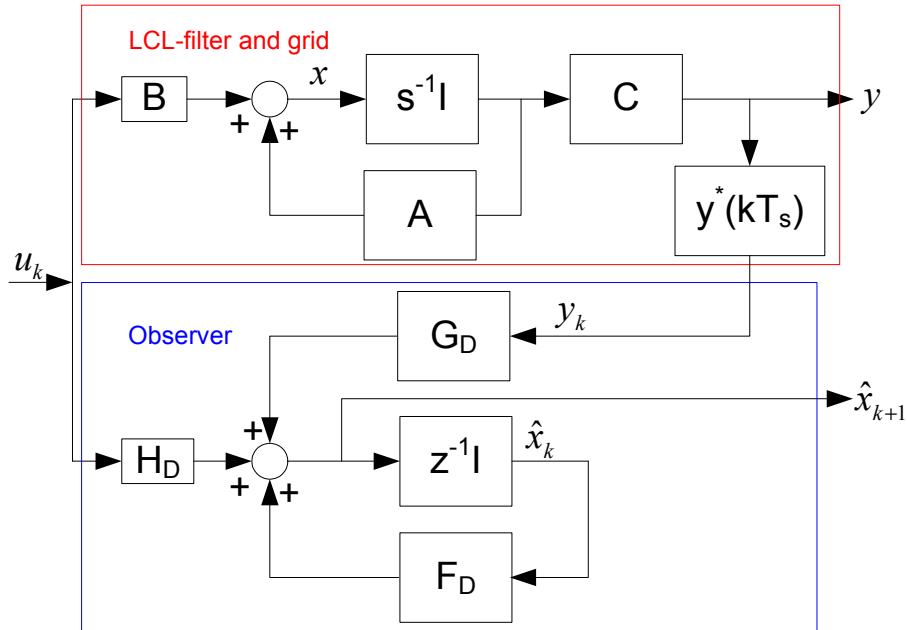
Figure 40: The discrete state-space observer.

4.2.6 Observer pole assignment

The design of the observer can be done in several ways, where the Kalman filter and pole assignment are two well known methods. The Kalman filter takes into account the expected noise. Pole assignment is more basic, but gives a transparent and uncomplicated design. Unlike Kalman filter, this method can be designed to reduce the processing loading of the DSP using intentional sparse matrices. Both methods can be based on a full state-space observer, which can be modeled as shown in Equation (4.74) and in [44]. It is described by:

$$\hat{x}_{k+1} = F_D \cdot \hat{x}_k + H_D \cdot u_k + G_D \cdot y_k \qquad (4.74)$$

The poles of the observer are given by the eigenvalues of the matrix F_D, which can be found by solving Equation (4.75):

$$0 = \left| z \cdot I - F_D \right| \qquad (4.75)$$

F_D is expressed by A, G and C as shown in equation (4.66). It is possible to adjust the different gains in matrix G in order to place the poles in the desired locations. If not specified otherwise, the z-domain pole placement is used throughout this thesis. In order to make the observer converge, all poles are placed inside the unit circle. The complete observer consists of two parts, one concerning the LCL-filter and the other concerning the grid. The LCL-filter observer poles are placed closer to origo, thus obtaining a

relatively fast but noisy response. The grid is a much slower process, so the observer poles can be placed closer to the unity circle. This gives a slower response, but with less noise due to better filtering.

The G-matrix in the continuous time domain is here defined as:

$$
G = \begin{bmatrix}
k_v & 0 & 0 & 0 & 0 & 0 \\
0 & k_v & 0 & 0 & 0 & 0 \\
0 & 0 & k_i & 0 & 0 & 0 \\
0 & 0 & 0 & k_i & 0 & 0 \\
0 & 0 & k_l & 0 & 0 & 0 \\
0 & 0 & 0 & k_l & 0 & 0 \\
0 & 0 & 0 & 0 & k_f & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & k_f \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & k_f & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & k_f \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & k_f & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & k_f \\
0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\tag{4.76}
$$

where the nonzero elements are adjusted in order to place the poles of the observer. This G matrix is then discretized according to Equation (4.73). The discrete G_D matrix could have been defined directly with a similar structure as to G, but the electrical circuit diagram shown in Figure 37 would not be valid in that case. The continuous-time model G-matrix was therefore chosen for the grid part of the observer, and G_D is the discretized version of G. The LCL-filter part of the observer was designed by choosing the discrete G_D directly, due to separation theorem concerns. This is further explained in chapter 5.

4.2.7 Frequency adaptive observer

The grid model presented in Equations (4.21)-(4.23) and shown again here, has a sharp center frequency at $\omega = 314 \, \text{rad/s}$. Expressed in state-space form, the state-space system matrices are given as:

$$x_g = \begin{bmatrix} u_g \\ i_g \end{bmatrix}, \qquad A_g = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}, \qquad B_g = 0, \qquad C_g = \begin{bmatrix} 1 & 0 \end{bmatrix}, \qquad D_g = 0 \qquad (4.77)$$

In some cases, such as islanding connection state, the inverter may experience large grid frequency deviations. An observer based on the model previously presented in Equation (4.77) results in steady-state phase and amplitude error in case of frequency deviations. This makes it unsuitable for operation under islanded situations. The model must therefore be modified in order to track the first harmonic without significant steady-state phase error even when the frequency is varying. The system matrix, A_g, shown in Equation (4.23) should thus change in real-time according to the grid frequency. The discretization for an undamped LC-filter can be written as shown by Girgis [38]:

$$A_{g,D}(\omega_0) = e^{A_g T_s} = \begin{bmatrix} \cos(\omega_0 T_s) & -\dfrac{1}{\omega_0 L}\sin(\omega_0 T_s) \\ \dfrac{1}{\omega_0 C}\sin(\omega_0 T_s) & \cos(\omega_0 T_s) \end{bmatrix} \qquad (4.78)$$

where ω_0 is the center frequency (314 rad/s). A linearization is made possible by calculating $A_{g,D}$ for two different frequencies.

$$A_{\Delta f} = \frac{\Delta A_{g,D}(2\pi \cdot f)}{\Delta f} = A_{g,D}(2\pi \cdot 49.5) - A_{g,D}(2\pi \cdot 50.5) \qquad (4.79)$$

The linearized system can then be expressed as:

$$A_{g,D}(f) = A_{g,50,D} + A_{\Delta f} \cdot (f - f_0) = A_{g,50,D} + \begin{bmatrix} -a & -b \\ b & -a \end{bmatrix} \cdot (f - f_0) \qquad (4.80)$$

The calculated linearization is summarized in Table 8.

Table 8: Frequency dependency of different factors in the discrete $A_{g,D}$-matrix.

Harmonic frequency	a(f-f$_0$)	b(f-f$_0$)
50 Hz	0.0000197 [per Hz] + 0.9995070	0.0006280 [per Hz] + 0.0313948

The frequency is measured by a separate block in the program code, based on the estimated fundamental frequency. The harmonics do not affect the power flow, and hence only the fundamental is adapted.

4.3 Simulations

The observer was simulated under different conditions. It is characterized by the response to a change in the process. Changes in the process both concerning state and parameters are simulated. The simulations in this chapter focus on the uncontrollable states, which are the grid observer states. The main objective is to verify the convergence time and the steady-state errors. Phase and amplitude errors are shown using Matlab/Simulink time domain simulations.

4.3.1 Grid 1st harmonic estimation

The grid observer fundamental frequency is subject to phase changes, amplitude changes and frequency changes. All aspects mentioned are dependent on the grid voltage feedback gain k_f. The simulations are therefore repeated for three different gains, one 50 % lower and another 50 % higher than the selected gain. The grid observer is designed to track the grid voltage slowly in order to filter the grid amplitude and frequency. The grid observer feedback was therefore low compared to the LCL-filter observer.

The main disadvantage of a low observer gain is sensitivity to model errors, in this respect the grid frequency. It is therefore important to make the observer insensitive to frequency errors under steady-state operation. The adaptive grid model described in the previous section is verified by adjusting the grid frequency to 47.6 Hz. A test profile simulates a phase jump, an amplitude change and a frequency change as shown in Figure 41.
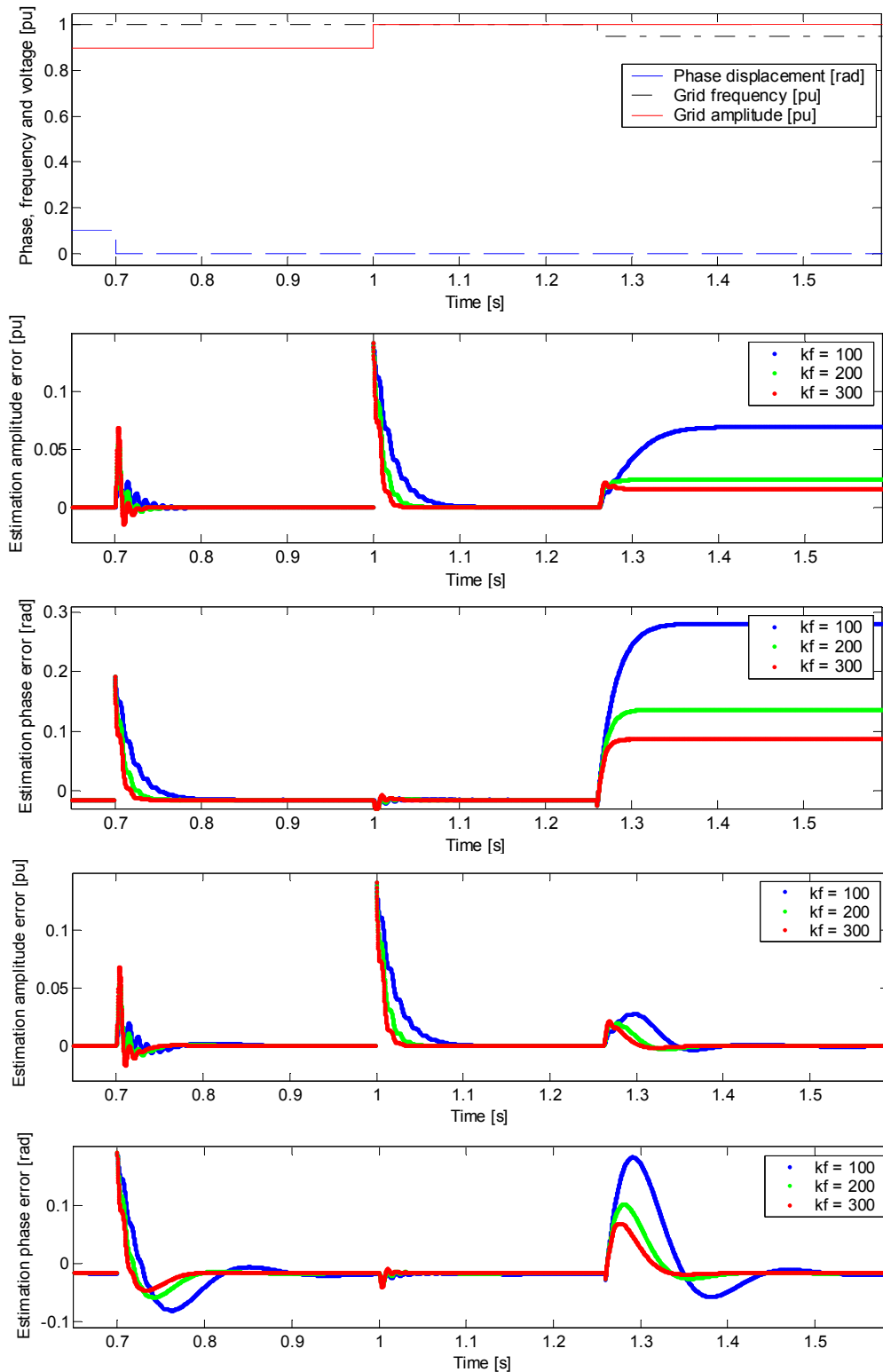
Figure 41: Test profile for simulation of grid voltage observer (upper graph), simple observer response (two middle graphs), and frequency adaptive observer response (two lower graphs).

The simple observer is sensitive to frequency modeling errors as expected. It results in steady-state phase errors and amplitude errors. The grid voltage estimation error affects the estimated LCL-filter variables. The inverter control is based on these potentially erroneous estimates.

Making the state observer frequency adaptive, improves the steady-state performance significantly. Due to the fact that the frequency feedback is based on the estimated states, the observer is included in the transfer function. This may give overshoot, but reduces the steady-state phase error to less than one sampling period T_s (0.0314 rad). The steady-state errors are summarized in Table 9.

Table 9: Fundamental frequency observer steady-state error for 47.6 Hz grid voltage.

k_f	Simple observer		Frequency adaptive observer	
	Fundamental frequency amplitude [pu]	**Fundamental frequency phase [rad]**	**Fundamental frequency amplitude [pu]**	**Fundamental frequency phase [rad]**
100	0.0692	0.281	-0.000307	-0.0194
200	0.0242	0.136	-0.000179	-0.0173
300	0.0154	0.0862	-0.000128	-0.0168

The estimation error is reduced significantly by making the observer frequency adaptive.

4.3.2 Grid 5th and 7th harmonics estimation

The observers for the harmonic voltages have the same structure as the fundamental frequency observer, except no frequency correction is applied. The grid voltage harmonic estimation is only supposed to be active during grid-connected operation. The grid frequency is then fixed within tight limits. Only 50 Hz grid frequency is used in the simulations.

The estimation of the grid 5th and 7th harmonics was tested by injecting a step from 1 % to 10 % fifth harmonic at t = 0.2 s and then a step from 1 % to 10 % seventh harmonic at t = 0.3 s. The results are shown in Figure 42.
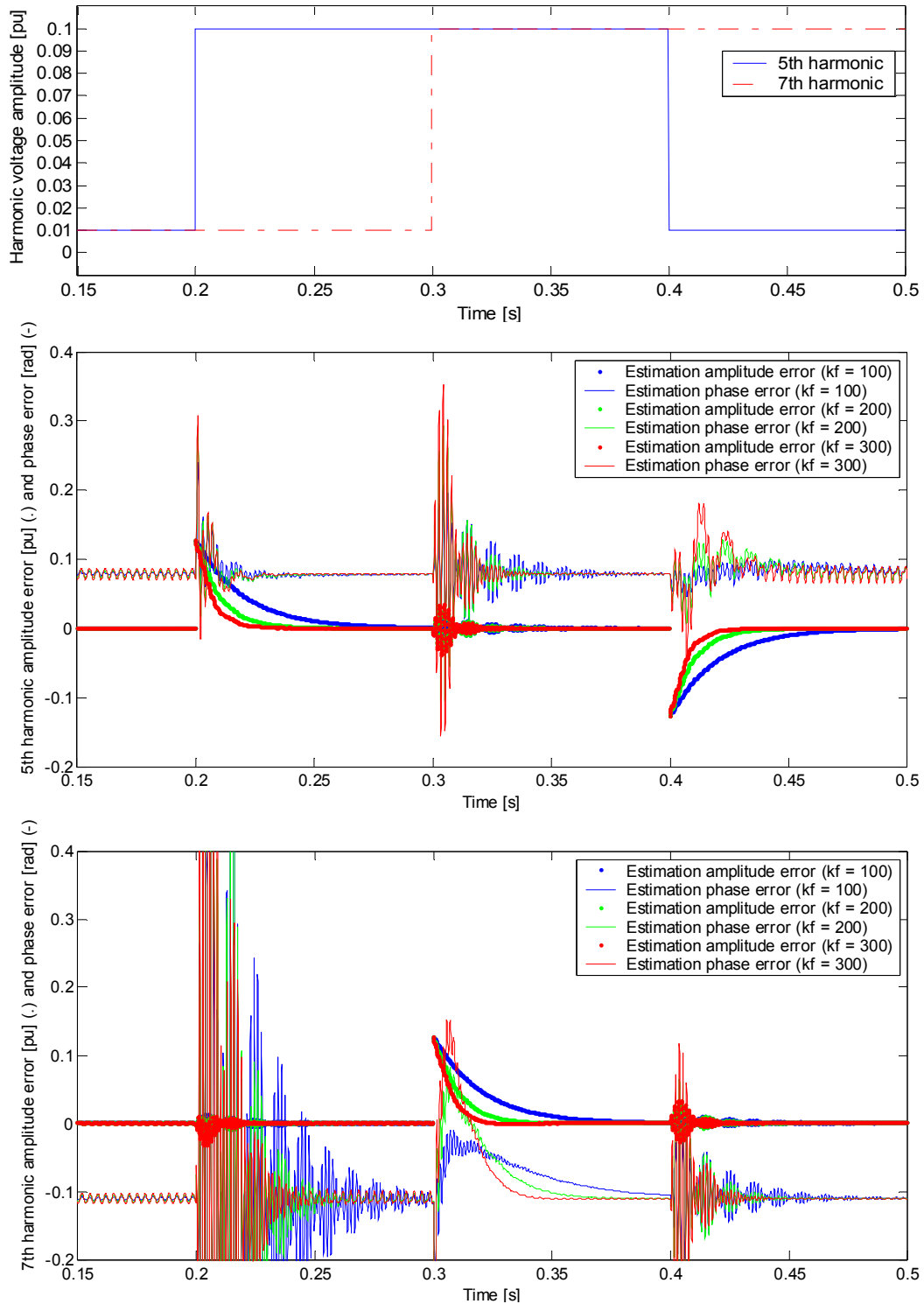
Figure 42: Grid voltage harmonic test profile (upper graph) for 5th (middle graph) and 7th (lower graph) harmonic voltage observers.

The simulation shows steady-state performance within realistic accuracy. The inaccuracy comes from sampling time modeling inaccuracies. The steady-state estimation error caused by a time delay is seen for the fifth and seventh harmonics as previously shown for the fundamental frequency. Measured in radians, the fixed time delay error is proportional to the frequency under consideration. It is less than sampling frequency T_s for both the fifth (0.157 rad) and the seventh (0.2198 rad). The error has an opposite sign for the fifth compared to first and seventh, because it rotates in the opposite direction to these. This is summarized in Table 10.

Table 10: Harmonic estimation error.

5th harmonic phase error	7th harmonic phase error
0.079 [rad]	-0.11 [rad]

The estimation time delay was improved using prediction. It is accurate because the grid is uncontrollable and the estimation gain k_f is low. Transient interactions between the fifth and seventh harmonics observers are seen. The fast step transient of one harmonic is affecting the other harmonic, as a step response has a wide frequency range. The peaks are even larger than for the frequency being estimated, especially the angle. They are not believed to affect the performance of the system because the relative magnitude compared to the first harmonic is small in practical applications.

4.4 Measurements

The observers were tested by applying a step voltage at the measured input of the DG. The inverter was running in UPS algorithm, thus not interacting with the grid observer. The tests were done with a diode rectifier (3 kW) connected in parallel with the grid, in order to worsen the THD. The grid voltage THD was measured using the Labview measurement system, which is independent of the DSP system. The voltage THD is varying, but was measured to 1.084 %. The fifth harmonic was 0.8176 % and the seventh was 0.6796 %. The three different estimated frequencies 50, 250 and 350 Hz are shown in Figure 43.
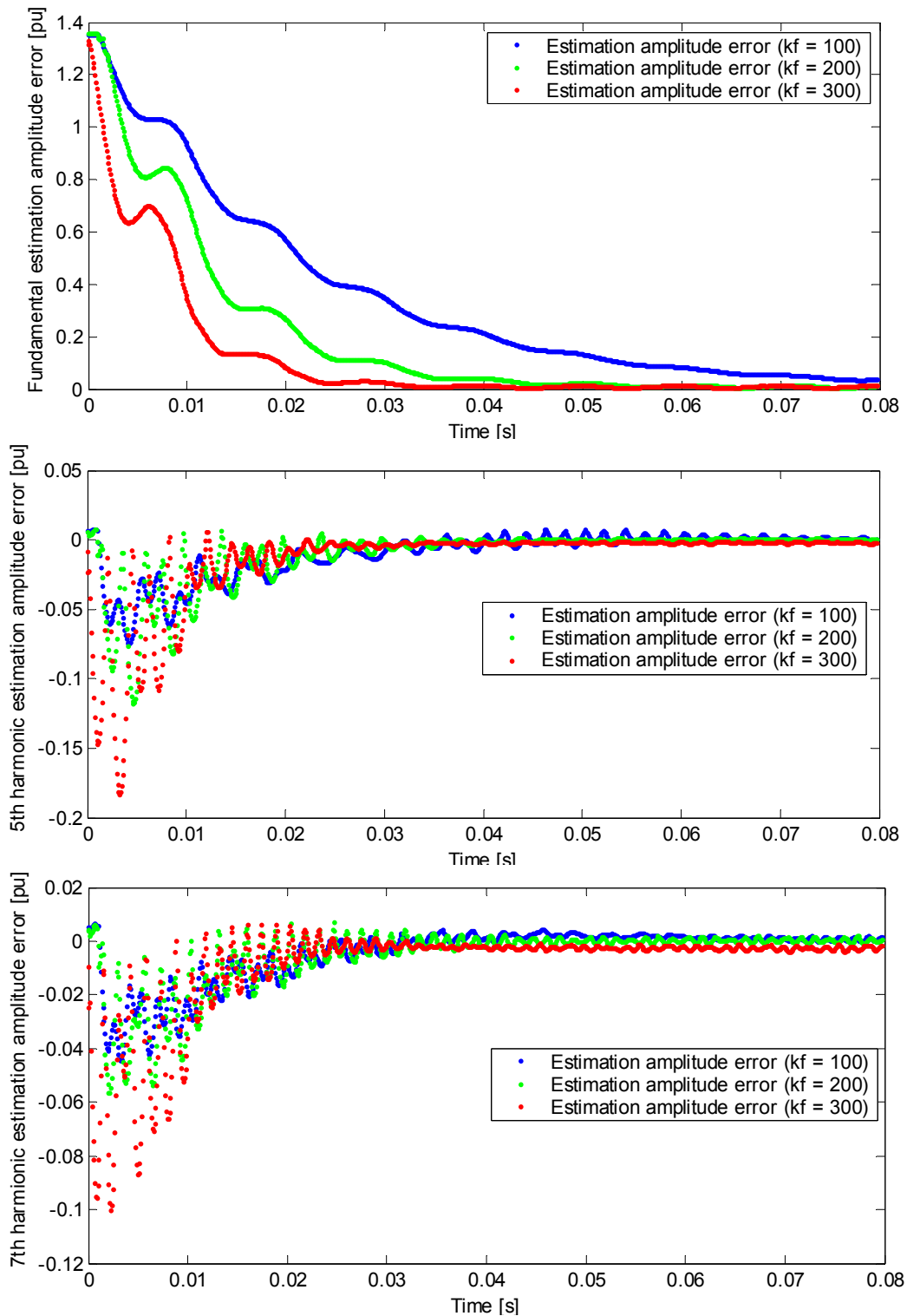
Figure 43: Measured observer response (DSP internal data) to a step voltage.

It is clear that the transient interaction between the different frequency components is large. The interaction seems to be larger with increasing feedback gain. The interaction is also a result of the step voltage which has low THD in this context. The harmonic content is thus much smaller than the fundamental frequency component of the step voltage. The step voltage excites all frequency components of the observer.

The difference between the simulations and the measurements is the fact that all harmonic components are applied simultaneously in the measurements, but not in the simulations. The harmonic observers (which are excited by the step voltage) estimate too large amplitude during the first fundamental frequency period. This is due to the harmonic content of the step voltage. The results are thus as expected.

The harmonic voltage estimation is mainly used for reducing current THD, which is not a transient phenomenon. Thus the steady-state error is more important than the transient behavior. The transient behavior is most important issue concerning fundamental frequency. The observer is part of the transfer function of the entire inverter controller, and especially the power controller including the frequency measurement.

5 Inverter control

There is a variety of options for control mechanisms for grid connected inverters. Ko et al. compare current control, to voltage control and describe the difference in [47]. Current control is most common for DG. There are mainly two reasons for this: Current control makes it easier to meet grid current THD requirements, and the power transistors can be dimensioned more optimal than for voltage control. If no additional control is applied, however, most current controlled inverters tend to produce discontinuous voltage during transitions between grid connected and standalone connection state. Solutions based on current control when grid connected and voltage control in standalone connection state have been shown using thyristors [48]. Fast timing of connection/disconnection events are ensured by the thyristors.

In this work the inverter is voltage controlled both when grid connected and standalone [49]. Voltage control is beneficial for the transitions between different connection states. When using an electromechanical contactor, which is slower than thyristors, voltage control is the best solution in this respect. The risk of power supply interruption to the critical load during connection state transitions is then minimized. A nonlinear load in standalone or islanding connection state requires a voltage controlled inverter in order to supply the distorted current it draws.

Concerning current THD, current controlled inverters are less sensitive to model and measurement errors. This is due to grid voltage harmonics or other non-modelled effects, as well as inverter blanking time. Compared to voltage control, a current controlled inverter can more easily compensate for such errors.

The IEEE grid code standards specify that DGs should feed sinusoidal current to the grid [10, 11]. This can be done by modulating the current as a copy of the voltage waveform, thus making the DG act as a negative resistor. Unfortunately, it also works as a negative damper magnifying oscillations. No problems will occur as long as the DG density is low (enough damping loads close), but serious harmonic voltages can become a problem when the DG density increases. This has been reported by Myrzik [50]. Frequency-selective impedance of the converter as shown in Figure 44, can reduce these problems.
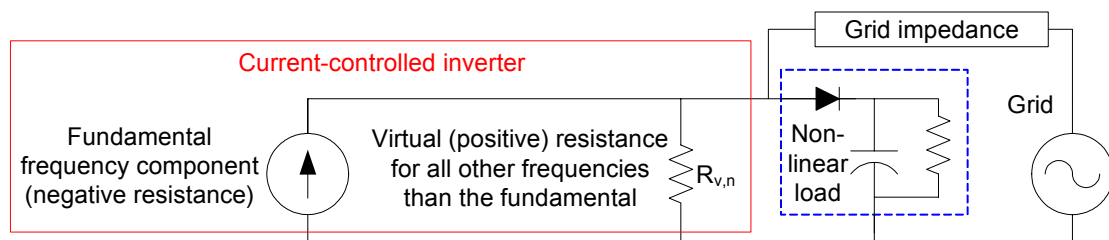

Figure 44: The use of a frequency-selective virtual resistance for grid voltage damping.

The fundamental frequency can be assigned a negative resistance, while the other frequencies up to the bandwidth of the current controller can be assigned a positive resistance $R_{v,n}$. This has been presented by Ryckaert et al. [51]. Such a solution absorbs harmonic current, possibly causing a current THD greater than 5 %. It then reduces the local grid voltage THD. It thus reduces the extra stress harmonics put on equipment such as transformers. Despite the positive impact this has on the grid, it will not comply with grid connection standards. The standards specify limits concerning the current THD, looking upon DG as a negative load. A current-controlled inverter with $R_{v,n}$ close to infinity is a good way to comply with THD requirements. For a voltage-controlled inverter, the thevenin equivalent of Figure 44 is shown in Figure 45.
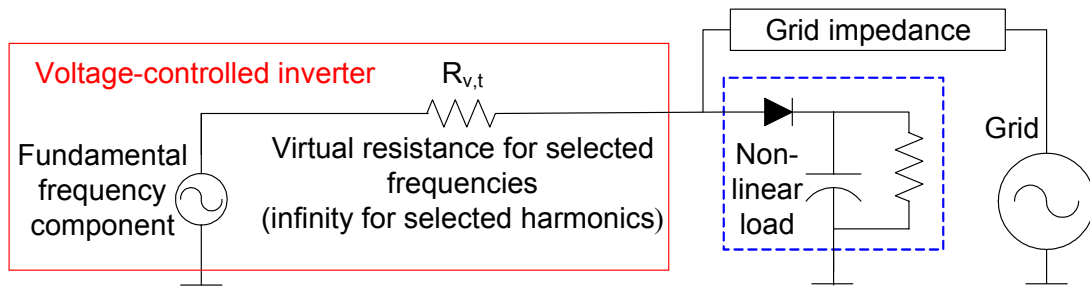
Figure 45: A voltage-controlled inverter with a frequency-selective resistance $R_{v,t}$.

In this work infinite inverter impedance $R_{v,t}$ as seen from the grid can be assigned the third, fifth and seventh harmonics during grid connected operation. The use of an accurate grid voltage observer that includes harmonics makes this possible. Based on feed-forward, the presented methods are applicable to both current-controlled inverters and voltage controlled inverters. A similar method has been described by Bolsens et al. [39, 40].

The grid-connected inverter used in this work also acts as an UPS, thus giving a more complicated control system due to several possible control algorithms. As will be discussed here, this combined role of the inverter requires the filter capacitor voltage to be controlled. The filter capacitor voltage control improves the local load voltage during transitions from one connection state to another. Grid connected voltage controlled inverters are well known in hybrid UPS systems, but not common for DG.

One important task of the digital controllers is the damping of the LCL-filter resonance frequency. The use of inductor current feedback or capacitor current feedback is common. An observer can reduce the number of necessary measurements.

Safety is important and the use of communication to solve the challenges concerning unintentional islanding will be described. The islanding control is closely connected to power control, which is discussed in this chapter. The presented solution is based on filter capacitor voltage control, which differs from most methods presented in the

literature in which current control are applied. A communication algorithm for maintaining the control of intentional grid islands is also presented.

Communication is used *when it is available*, meaning that the system is soft real-time. The purpose of the communication is to allow the network owner to control the DGs. In this case safety is ensured by the network owner, and the inverters can then be controlled in several possible ways. Reactive power compensation, harmonic current reduction and other means of supporting the grid voltage can be enabled when communication is operational. Anti-islanding control algorithm and UPS control algorithm are the possibilities when the communication is down. This is to make sure that the DG will disconnect within a 2 second period after an island connection state is entered, as specified by IEEE standards [10, 11].

5.1 State feedback for LCL-filter resonance damping

State feedback is a control method used for stabilizing systems. It is also used for changing the dynamics. The alternatives to state feedback are different controllers containing internal states such as PI-controllers. For the inverter control in this thesis, the primary purpose is to maintain a stiff filter capacitor voltage. The output voltage should be little affected by the current. Thus low output impedance as seen from the load concerning the fundamental frequency component is desired. Damping of the LCL-filter resonance is the second purpose of the state feedback. State feedback from the system internal states can be measured or estimated. A standard discrete state feedback structure is shown in Figure 46.
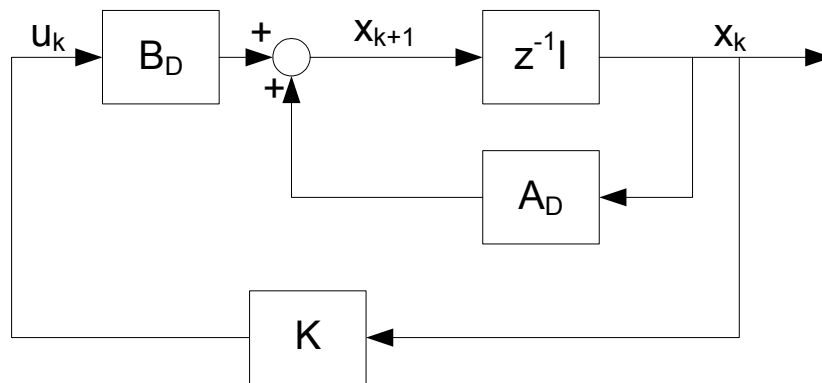
Figure 46: A standard discrete state feedback structure.

State feedback from estimated states is chosen in order to make a simple, noise-immune control system designed by pole assignment. When using state feedback for a voltage controlled inverter it is important to keep the current feedback low in order to avoid a high voltage drop under high load conditions. The filter capacitor voltage should be stiff. This can be solved using capacitor C_f current feedback. The capacitor current can

be either measured or estimated by the difference of the inductor currents through L_{f1} and L_{f2} in Figure 31, which is used here.

According to the separation theorem [14], the eigenvalues of a state-feedback system using estimated states has all the poles of the feedback loop, in addition to the poles of the state space observer. The observer should be faster than the feedback loop. The observer must be designed in the same domain as the controller (either discrete or continuous). The observer and the state feedback can in that case be designed independently. A discrete state-space system can be described as in Figure 46 without state feedback:

$$x_{k+1} = A_D x_k + B_D u_k \tag{5.1}$$

Including the state feedback gain (matrix K), the system is described as:

$$x_{k+1} = \left(A_D + B_D K \right) x_k \tag{5.2}$$

Assuming all state variables are available, the poles of the closed-loop state feedback can be found from the eigenvalues of the matrix $\left(A_D + B_D \cdot K \right)$, which is given by Equation (5.3)

$$0 = \left| z \cdot I - \left(A_D + B_D \cdot K \right) \right| \tag{5.3}$$

The time delay of the controller has significant influence on the controller performance. Methods for cancelling parts of this time delay are thus a benefit. The time delay originates from the isolation measurement circuit and the ADC, as well as the various calculations in the DSP and the PWM module. The time delay is one sampling period T_s for the measurements and calculations. The PWM module adds an additional half sampling period of time delay, which is neglected. An overview of the total time delay is given in Figure 47.
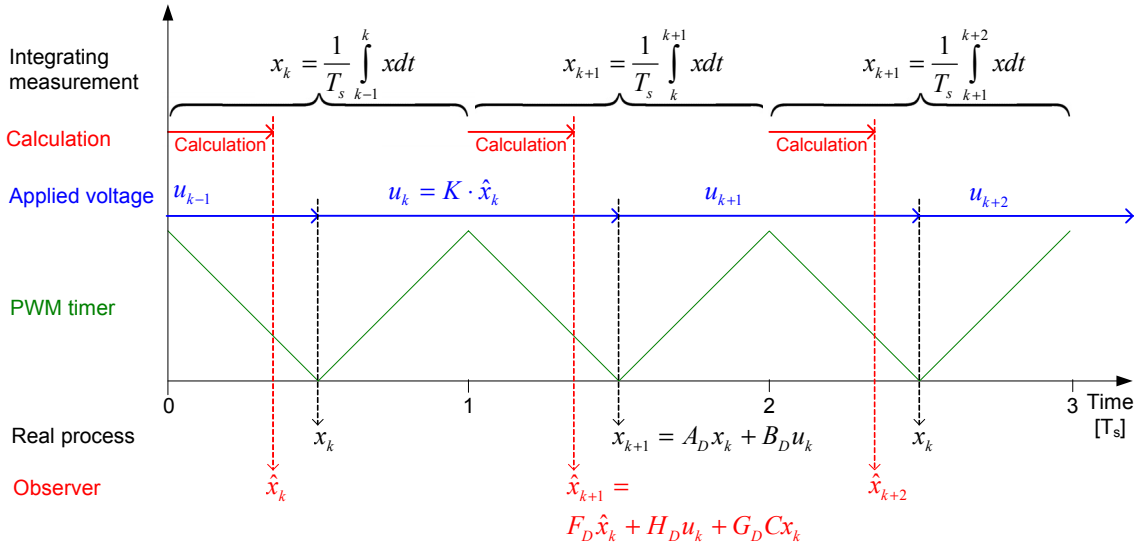
Figure 47: Timing of the inverter control using measurements (x) and estimations ($\hat{x}$) of the states of the LCL-filter.

The time delays of a system can be included in the system model, as is done by Bolsens et al. [39, 40]. In the present work, however, the time delay is cancelled using the discrete model observer directly before the time delay block. This is possible because the observer calculation takes less than ½ T_s. The observer equation is defined as

$$\hat{x}_{k+1} = F_D \cdot \hat{x}_k + H_D \cdot u_k + G_D \cdot y_k \tag{5.4}$$

where $\hat{x}_k$ is used for calculating u_k. This may cancel one sample period T_s time delay. It is possible because $\hat{x}_k$ is available just before the physical system reaches x_k, when u_k must be set.

When designing the filter capacitor C_f voltage controller, only the LCL-filter states are considered. The state feedback gain matrix K is defined as:

$$K = \begin{bmatrix} K_u & 0 & K_{i1} & 0 & K_{i2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_u & 0 & K_{i1} & 0 & K_{i2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{5.5}$$

The controller is designed using the concept of virtual resistors [52, 53]. The feedback gain matrix K is chosen so that the closed-loop system behaves as if virtual resistors ($R_{v,s}$ and $R_{v,p}$) were put in series with the LCL-filter inductors and capacitors. Also the filter capacitor voltage feedback gain $K_{v,u}$ is taken into account. The closed-loop state feedback system can be described with an equivalent circuit-scheme as shown in Figure 48.
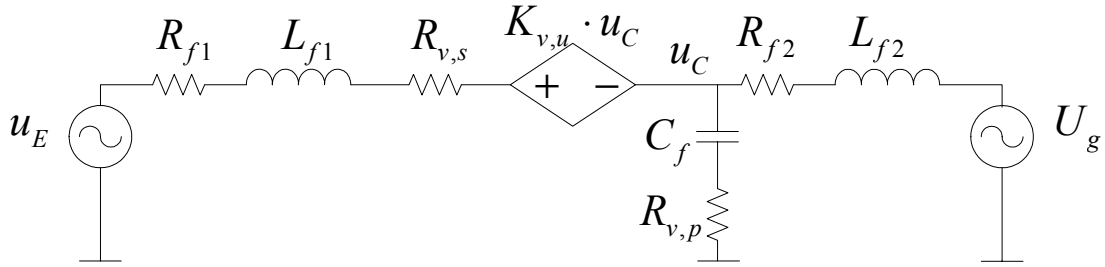
Figure 48: The state feedback equivalent circuit-scheme.

Figure 48 can be described in state-space form by the zero-input response matrix.

$$
A_{LCL,R,pu} = \begin{bmatrix} 0 & \dfrac{1}{C_f z_{base}} & \dfrac{-1}{C_f z_{base}} \\[2ex] \dfrac{-(1+K_{v,u}) \cdot z_{base}}{L_{f1}} & \dfrac{-R_{f1} - R_{v,s} - R_{v,p}}{L_{f1}} & \dfrac{R_{v,p}}{L_{f1}} \\[2ex] \dfrac{z_{base}}{L_{f2}} & \dfrac{-R_{v,p}}{L_{f2}} & \dfrac{-R_{f2} - R_{v,p}}{L_{f2}} \end{bmatrix}
\tag{5.6}
$$

U_g is considered shorted. The zero-state matrix $B_{LCL,pu}$ described in Equation (4.18) is unchanged. By discretizing Equation (5.6), the discrete feedback gain can be found using pole matching. This is done using the function "place.m" in Matlab. First Equation (5.6) is discretized:

$$
A_{D,LCL,R,pu} = 1 + \sum_{n=1}^{n=\infty} \frac{\left(A_{LCL,R,pu} \cdot T_s \right)^n}{n!}
\tag{5.7}
$$

The real LCL-filter is earlier defined in Equation (4.18). The discrete version is called $A_{D,LCL,pu}$. The target is now to find the feedback gain matrix K so that the closed-loop state feedback is equal to the equivalent circuit in Figure 48

$$
A_{D,LCL,R,pu} = A_{D,LCL,pu} + B_{D,LCL,pu} K
\tag{5.8}
$$

The eigenvalues of the circuit with virtual resistors $A_{D,LCL,R,pu}$ is used as a target for the pole placement when calculating the feedback gain matrix K.

$$
eigenvalues \left(A_{D,LCL,R,pu} \right) = eigenvalues \left(A_{D,LCL,pu} + B_{D,LCL,pu} K \right)
\tag{5.9}
$$

If the model is to be correct, the discrete zero state response matrix $B_{D,LCL,R}$ including virtual resistors is different from the system without virtual resistors, $B_{D,LCL}$.

$$B_{D,LCL,R} \neq B_{D,LCL} \tag{5.10}$$

Adding virtual resistors does not change $B_{D,LCL}$ which is physical. It is therefore not modified during the rest of this thesis. This mainly causes the difference of about 2 dB between the equivalent circuit (with virtual resistors) and the real circuit (with discrete state feedback). The difference can be observed below the resonance frequency in Figure 49.
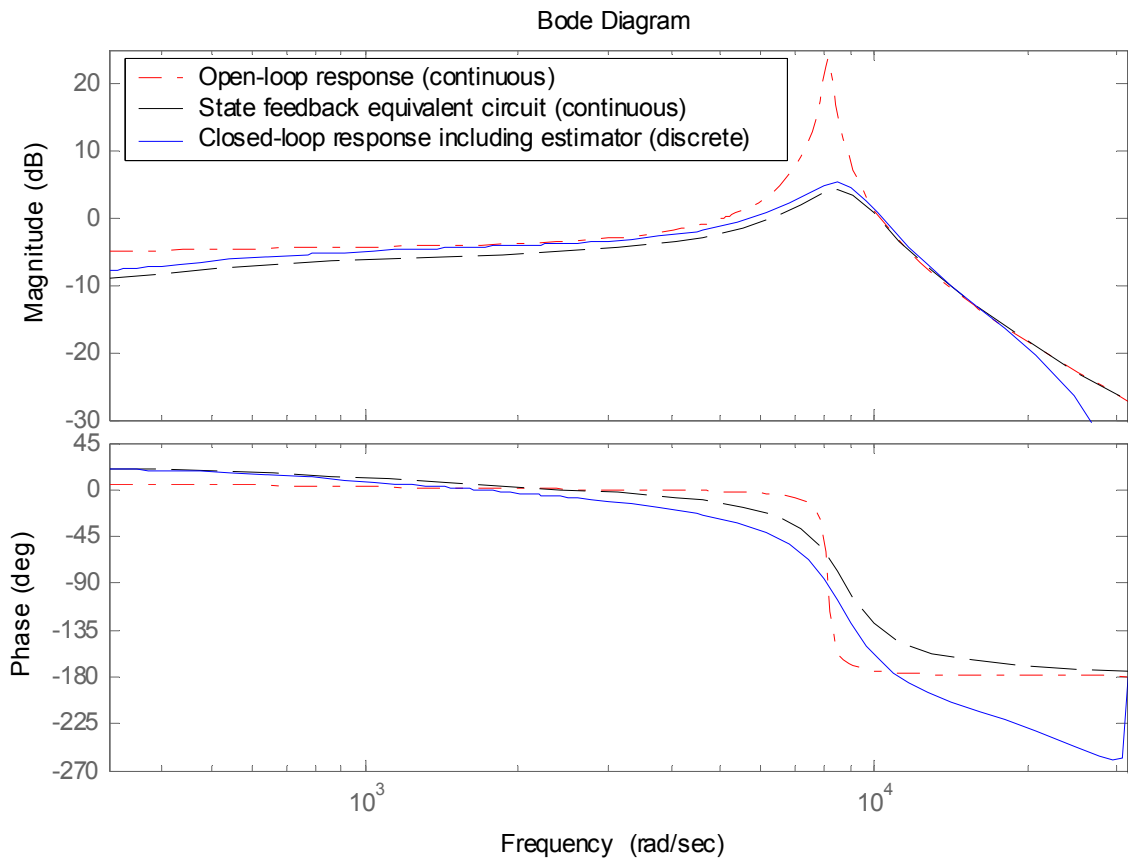
Figure 49: Frequency response of the LCL-filter with and without virtual resistors. The frequency response ranges from 314 rad/s to the nyquist frequency (T_s/2) of 31400 rad/s.

The virtual series resistance $R_{v,s}$ purpose is improved power sharing and oscillation damping. It is low enough to not affect the voltage significantly. The virtual filter capacitor resistor $R_{v,p}$ is chosen so that the system has a closed-loop response with a bandwidth close to the LCL-filter resonance frequency. Bandwidth is here defined as 90º phase of the closed-loop feedback system. The filter should be well damped (by a high bandwidth of the state feedback), but the state feedback should also have a lower

bandwidth than the observer. The observer should filter noise. These three factors gave the choice of state feedback and observer parameters, summarized in Table 11.

Table 11: Inverter state feedback and observer parameters summary.

	Parameter	Value [pu]
Equivalent circuit	Voltage feedback gain	$K_{v,u} = 0.25$
	Series-connected virtual resistance	$R_{v,s} = 0.05$
	Parallel-connected virtual resistance	$R_{v,p} = 0.1$
Controller	Voltage feedback gain	$K_u = -0.0333656$
	L_{f1} current feedback	$K_{i1} = -0.2092426$
	L_{f2} current feedback	$K_{i2} = 0.1682529$
Observer	C_f voltage estimation gain	0.4 (from u_C)
	L_{f1} current estimation gain	0.5 (from i_{Lf1})
	L_{f2} current estimation gain	0.1 (from i_{Lf1} because i_{Lf2} is not measured)

The state feedback is based on the estimated states, not the measured states. The complete state feedback including the observer can be described as a new state-space model:

$$x_{tot,k+1} = A_{tot}x_{tot,k} + B_{tot}u_k \tag{5.11}$$

The state vector now contains both the real process states x, and the estimated states $\hat{x}$.

$$x_{tot} = \begin{bmatrix} x \\ \hat{x} \end{bmatrix} \tag{5.12}$$

The matrix A_{tot} is defined as a combination of the discretized physical process and the observer:

$$A_{tot} = \begin{bmatrix} A_D & B_D K \\ G_D \cdot C & F_D + H_D K \end{bmatrix} \tag{5.13}$$

The matrix B_{tot} is defined as:

$$B_{tot} = \begin{bmatrix} B_D \\ H_D \end{bmatrix} \tag{5.14}$$

The system response can be described by the eigenvalues of A_{tot}, or by the transfer function as shown in Figure 49. The pole placement is shown in Figure 50.
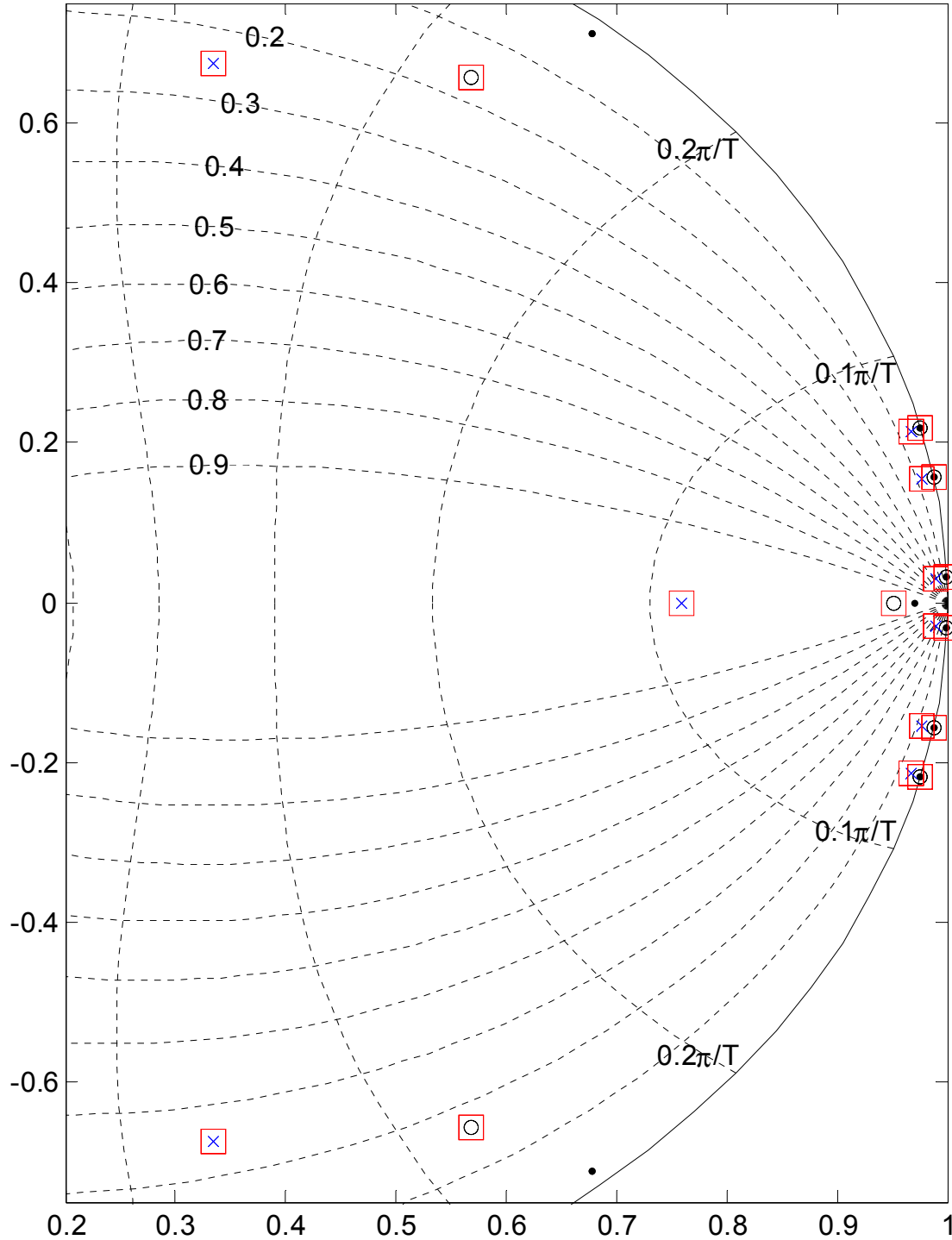

Figure 50: System eigenvalues (.) with state feedback (o), observer poles (x), and estimated state feedback poles (squares).

Due to the sample-and-hold circuits represented by the PWM and the integrating measurement circuit, the physical process is controlled by means of a discrete controller. The use of an equivalent-circuit for the observer represents a continuous-time observer. If the separation theorem should hold, these two cannot be combined.

The observer is therefore designed separately for the slow grid observer and the fast LCL-filter observer. The grid represents a non-controllable oscillator. This means that the grid estimate does not interact with the discrete controller directly. It can therefore be designed as a continuous-time observer which is discretized afterwards.

On the other hand, the LCL-filter is controllable, and also the resonance frequency is close to the bandwidth of the discrete controller. Differences between a continuous-time model and the discrete physical process then become large. If the observer is designed before the discretization (choosing G), the separation theorem will not hold. The observer is therefore designed in the discrete time-domain (choosing G_D). In this case the separation theorem will hold, which is important due to the closeness between the controller bandwidth and the LCL-filter resonance frequency.

The observer thus contains two parts; the grid observer (which is not controllable and thus the discretization does not matter with regard to the separation theorem), and the LCL-filter (which satisfies the separation theorem due to the discrete observer design). The response of the estimated state feedback system is acceptable concerning damping of the resonance peak. There is low steady-state connection between the observed harmonics due to the continuous-time design of the observer. It would have been larger if the grid observer was designed based on a discrete model (choosing G_D).

5.2 Feed-forward for voltage harmonics cancellation

Voltage controlled inverters are especially sensitive to grid voltage harmonic distortion. There is no active correction of the harmonic currents they can cause, which on the other hand current controlled inverters have. An alternative solution is to estimate the most common voltage harmonics. Selected harmonics can be used for feed-forward in the inverter output voltage. The effect of these harmonics on the grid current may then be removed. The distance between the LCL-filter resonance frequency and the different harmonics depends on the harmonic in question. Different gains must therefore be used as compensation for the different harmonics. One procedure is shown in [39]. Here a similar procedure is shown, but it has difficulties to take into account the controller. Therefore a procedure which orthogonalizes the eigenvectors of the system is suggested.

5.2.1 Compensation by inverse transfer function

The aim of the compensation is to have zero grid current I_{Lf2} for a given harmonic. This will be the case if there is zero voltage over the inductor L_{f2}:

$$u_C = u_g \tag{5.15}$$

Assuming the compensation is ideal, no current flows through L_{f2} which means the grid impedance is equal to an open-circuit. This is shown in Figure 51.
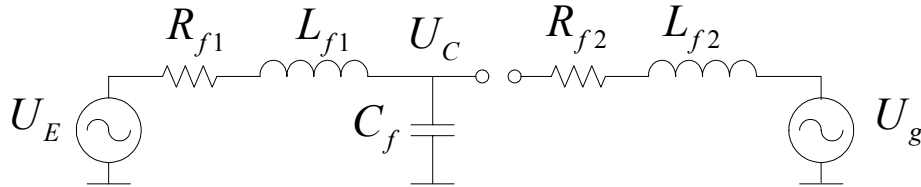
Figure 51: Target equivalent circuit when using feed-forward for harmonic voltage cancellation.

The filter capacitor voltage U_C is in this case independent of the grid impedance (neglecting state feedback):

$$\frac{U_C(s)}{U_E(s)} = TF_{UE \to UC}(s) = \frac{Z_C}{Z_C + Z_{Lf1}} = \frac{1}{s^2 \cdot C_f \cdot L_{f1} + s \cdot C_f \cdot R_{f1} + 1} \tag{5.16}$$

If U_C is to equal U_g for a given frequency, the inverter voltage U_E feed-forward term $FF(s)$ must equal the inverse of Equation (5.16):

$$\frac{U_E}{U_g} = FF(s) = \frac{1}{TF_{UE \to UC}(s)} = 1 + s \cdot C_f \cdot R + s^2 \cdot L_{f1} \cdot C_f \tag{5.17}$$

Combining Equation (5.16) and Equation (5.17) proves the tracking of a given grid harmonic voltage can be unity:

$$\frac{U_C(s)}{U_g(s)} = \frac{U_C(s)}{U_E(s)} \cdot \frac{U_E(s)}{U_g(s)} = TF_{UE \to UC}(s) \cdot FF(s) = TF_{UE \to UC}(s) \cdot \frac{1}{TF_{UE \to UC}(s)} = 1 \tag{5.18}$$

The feed-forward (neglecting the state feedback) can thus be described as

$$FF(s) = 1 + s \cdot C_f \cdot R + s^2 \cdot L_{f1} \cdot C_f \tag{5.19}$$

When assuming an inductor L_{f1} resistance of $R_{f1} = 0.32$ ohm (measured at 1 kHz), the following feed-forward compensation coefficients are given in Table 12.

Table 12: The frequency dependence of the feed-forward compensation.

Frequency [Hz]	Feed-forward compensation coefficient
50	0.997536 + j0.0030144
250	0.9384021 + j0.0150720
350	0.8792682 + j0.0211008

The feed-forward is only used in the anti-islanding control algorithm. When operating in UPS or voltage support algorithm, the voltage should be as close to the fundamental frequency component as possible. The over-harmonics estimates are then set to zero. This improves the voltage THD measured at the LCL filter capacitor, but affect the current THD. Feed-forward of the harmonic voltages thus gives a tradeoff between voltage THD and current THD.

5.2.2 Simulations without state feedback

The feed-forward was simulated in order to verify the benefit by using it. Unrealistically large amounts of 5th and 7th harmonic voltage were injected (10 % 5th and 20 % 7th harmonic). The resulting THD are shown in Figure 52, with no state feedback for LCL-filter damping.
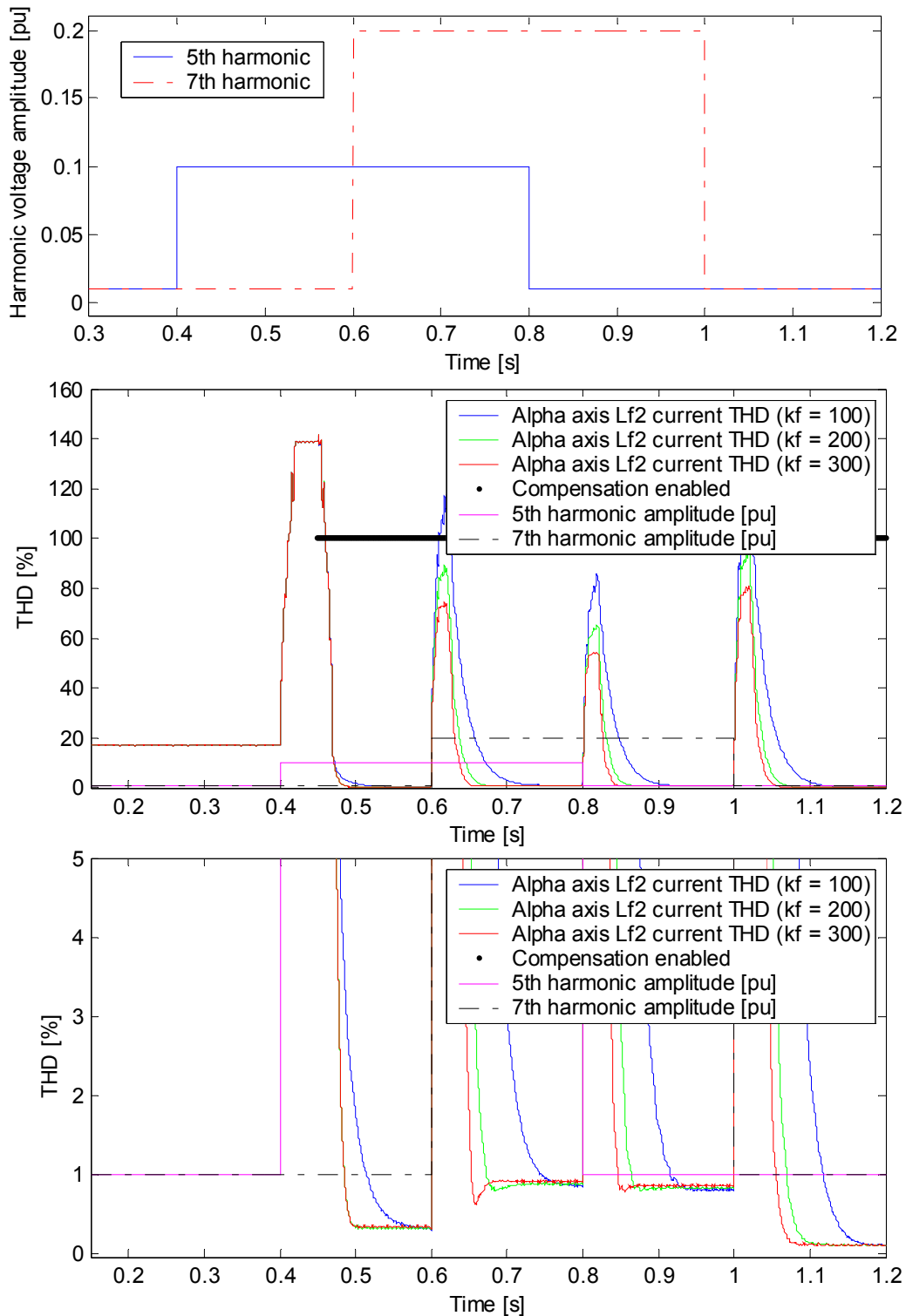
Figure 52: Simulation of harmonic voltage cancellation, enabled from t = 0.45 s. The lower trace is a magnified version. One T$_s$ prediction is used for time delay cancellation. No LCL-filter state feedback is applied.

In order to see the difference of using feed-forward, the alpha axis parameters are shown in Figure 53.
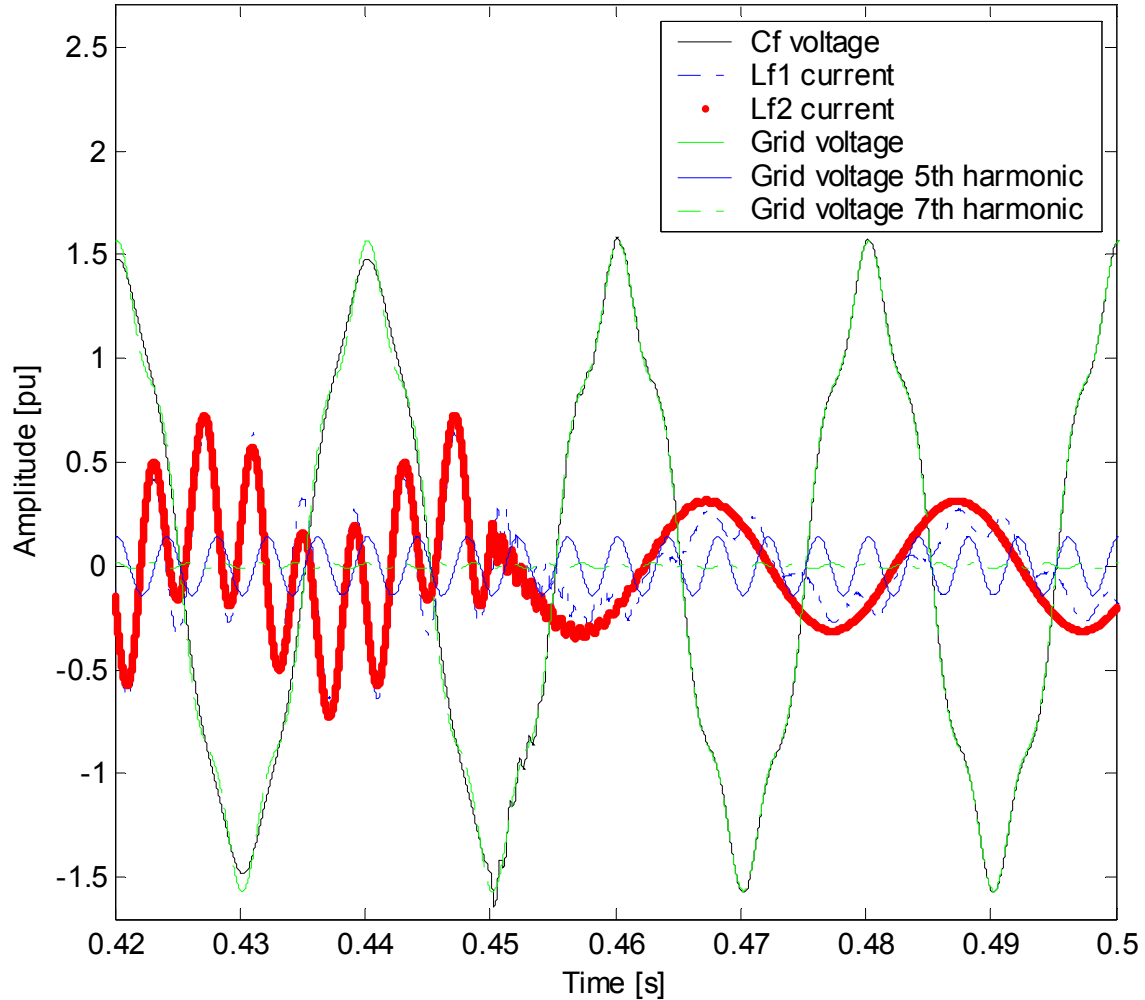
Figure 53: Simulation of the harmonic voltage cancellation, which is enabled at t = 0.45 s.

The simulation shows that the estimated harmonic voltages are cancelled by mirroring the grid voltage harmonic component at the filter capacitor C_f voltage. Harmonic current passes through the inner inductor L_{f1}, but the grid current flowing through L_{f2} is almost sinusoidal.

This harmonic compensation method has its main weakness in the difficulties of including the state feedback when calculating the feed-forward gains. Using the virtual resistors in Figure 48 as if they were physical resistors gives a fair approximation. This requires the state feedback to be designed based on virtual resistors.

5.2.3 Compensation by choice of eigenvectors

A more general calculation method for the feed-forward terms is based on the choice of eigenvectors. A discrete closed-loop state-feedback system can be described by

$$x_{k+1} = \left(A_D + B_D K \right) x_k \tag{5.20}$$

Its eigenvector matrix X can be defined as:

$$\left(A_D + B_D K \right) X = X \Lambda \tag{5.21}$$

where Λ is the eigenvalue diagonal matrix. The eigenvalue assignment algorithm "place.m" in Matlab finds the appropriate gain matrix K for a set of specified eigenvalues. As a part of the algorithm it also maximizes the determinant of X with respect to its columns (with unity-length constraint) [54]. This is equivalent to maximizing the orthogonality of the eigenvectors, or decoupling the different states of the closed-loop system as much as possible.

The Matlab function "place.m" for pole assignment can be applied to the complete equivalent circuit-scheme state-space model including the grid voltage. Since the grid is not controllable, the associated poles cannot change location. On the other hand, the eigenvectors can change. In the resulting state feedback gain vector K, the feed-forward term is appended. The LCL-filter state feedback part, was, however, calculated without including the grid, as shown in the previous section. The grid voltage decoupling does not affect the poles of the system. The decoupling is a by-product of the algorithm, which is not targeted for uncontrollable systems because it is impossible to change pole locations. The main benefit of using this method is that it takes into account the discrete state feedback.

5.2.4 Simulations with state feedback

The two methods for compensation were compared by the use of simulations. The same test sequence was used as in Figure 52, but now the state feedback for LCL-filter resonance damping was added. The continuous-time domain feed-forward is shown in Figure 54. The eigenvector based feed-forward is shown in Figure 55.
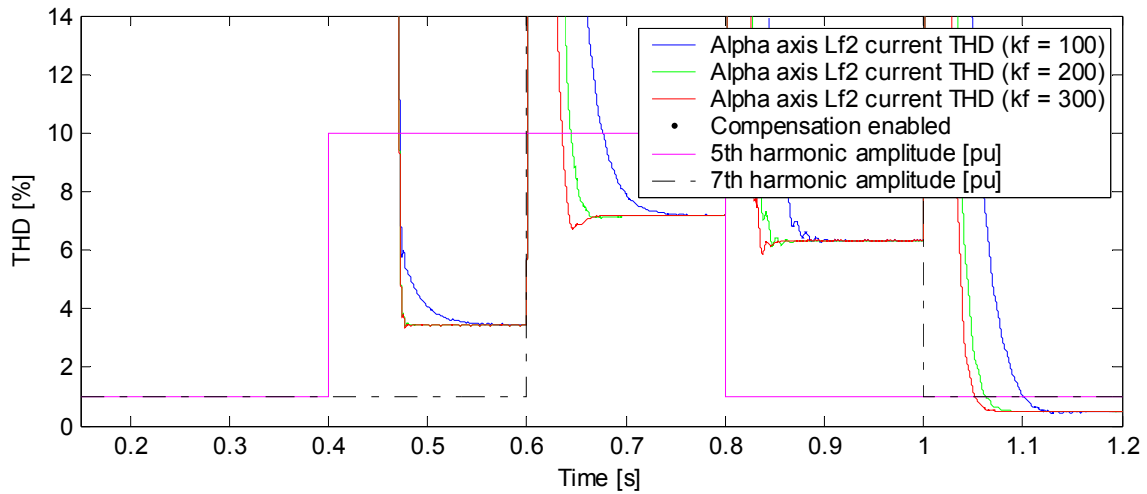
Figure 54: Feed-forward designed using the inverse transfer function including virtual resistors.
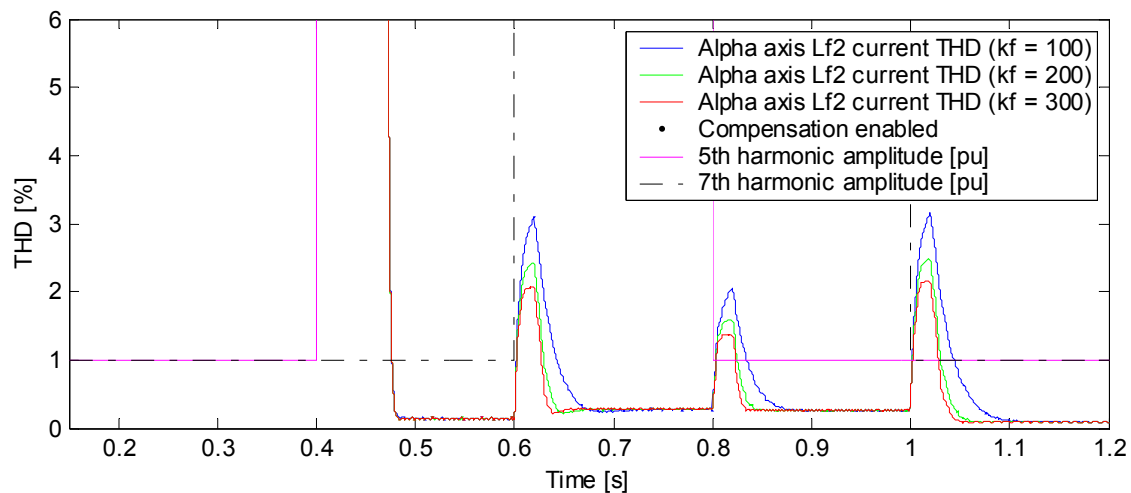
Figure 55: Feed-forward designed using the Matlab function "place.m" for grid voltage decoupling.

There is a remarkably better cancellation of the grid voltage harmonics by the eigenvector feed-forward gains calculation method. Both transient and stationary it produces current THD one order of magnitude less than the inverse transfer function method. The inverse transfer function could have compensated marginally better if the filter capacitor voltage reference was adjusted according to the harmonic content. This was not done, in order to keep an identical simulation environment for the two methods. Still, it is clear that the eigenvector method is best, actually better than the inverse transfer function without state feedback (Figure 52).

5.3 Inverter power control

While the aim of the inverter voltage control method is to produce a sinusoidal voltage (possibly with some harmonics), the inverter power control algorithm controls the power flow to the grid. The power control algorithm works on an order of magnitude slower timescale than the voltage control and includes both voltage support and anti-islanding control algorithms. The cascade control structure shown in Figure 56.
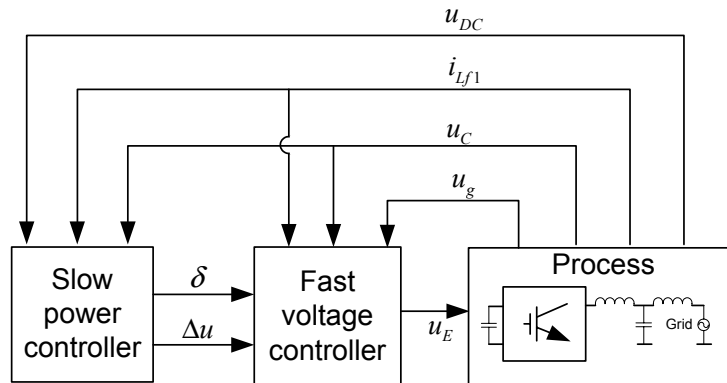
Figure 56: The power controller and the voltage controller connections.

Anti-islanding algorithms based on current-controlled inverters are well known. An overview is given by Bower and Ropp [15]. Du et al. describes anti-islanding algorithms for synchronous generators with band-pass filtering of the parameters P and Q, where reactive power is used for the anti-islanding algorithm [16]. An anti-islanding algorithm that is able to run in a voltage controlled inverter is required in this work. This is shown in [12].

The active power flow is controlled by the current component through the grid inductor, L_{f2}, in phase with the grid voltage. This can either be done by directly controlling the current, i_{Lfl}, or by controlling the voltage phase of U_c. The current through the grid impedance is given by the relationship between the grid voltage and the inverter voltage. The control of this current is based on the phase and amplitude of the voltage difference between the two voltage sources. The grid connection of a DG can be described by the circuit scheme shown in Figure 57
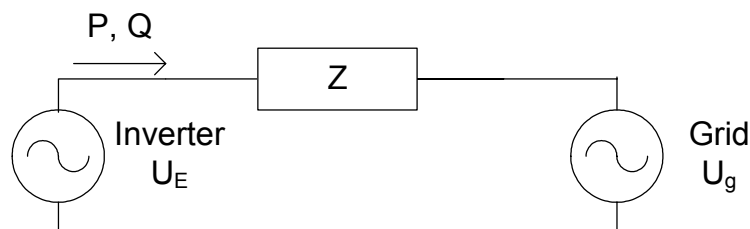
Figure 57: Simplified circuit scheme for the connection of a DG to the grid.

This is a simplified version of the complete circuit scheme including the LCL-filter of the inverter depicted in Figure 58.
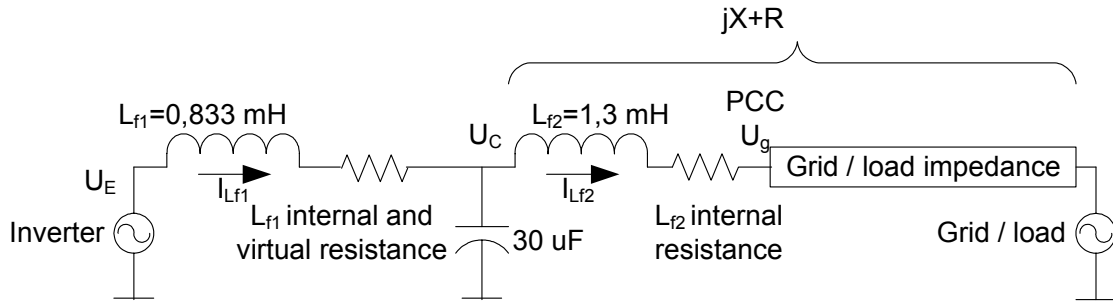
Figure 58: Complete circuit scheme for the connection of DG to the grid, including the LCL-filter.

The active current, I_P, and the reactive power, I_Q, can then be found from the inverter voltage, U_E, and the grid voltage, U_g. This is shown in Figure 59.
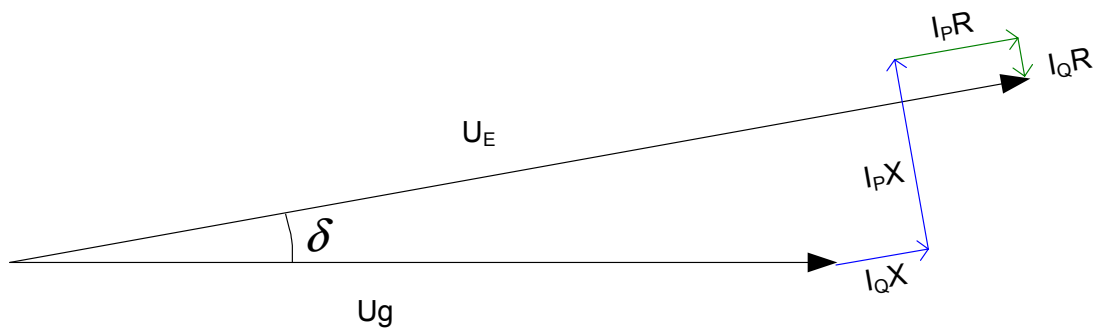
Figure 59: The loading of the inverter as a function of angle and amplitude difference.

The filter capacitor is neglected in the following because it has close to constant reactive power production. Connecting the two voltage sources together gives the following apparent power from the inverter:

$$S = U_E \left(\frac{U_E - U_g}{R + jX} \right)'$$

(5.22)

Separating this into active and reactive power gives the following expressions:

$$P = \frac{R \cdot U_E^2 - R \cdot U_{E,real} U_g + X \cdot U_{E,imag} \cdot U_g}{R^2 + X^2}$$

$$P = \frac{\left\{ R \cdot \left(U_C - \cos(\delta) \cdot U_g \right) + X \cdot \sin(\delta) \cdot U_g \right\} \cdot U_E}{R^2 + X^2}$$

$$Q = \frac{X \cdot U_E^2 - X \cdot U_{E,real} U_g - R \cdot U_{E,imag} \cdot U_G}{R^2 + X^2} \tag{5.23}$$

$$Q = \frac{\left\{ X \cdot \left(U_E - \cos(\delta) \cdot U_g \right) - R \cdot \sin(\delta) \cdot U_g \right\} \cdot U_E}{R^2 + X^2}$$

$U_{E,real}$ denotes the real part of U_E, and $U_{E,imag}$ denotes the imaginary part of U_E. Assuming δ small so that $\sin(\delta) \approx \delta$ and $\cos(\delta) \approx 1$, gives the following approximation:

$$P = \frac{\left\{ R \cdot \left(U_E - U_g \right) + \delta \cdot X \cdot U_g \right\} \cdot U_E}{R^2 + X^2}$$

$$Q = \frac{\left\{ X \cdot \left(U_E - U_g \right) - \delta \cdot R \cdot U_g \right\} \cdot U_E}{R^2 + X^2} \tag{5.24}$$

This can be rewritten as:

$$P = \left(U_E - U_g \right) \frac{R \cdot U_g}{R^2 + X^2} + \frac{\delta \cdot X \cdot U_E \cdot U_g}{R^2 + X^2}$$

$$Q = \left(U_E - U_g \right) \frac{X \cdot U_g}{R^2 + X^2} - \frac{\delta \cdot R \cdot U_E \cdot U_g}{R^2 + X^2} \tag{5.25}$$

The inverse equation gives:

$$\left(U_E - U_g \right) = P \frac{R}{U_g} + Q \frac{X}{U_g}$$

$$\delta = P \frac{X}{U_E \cdot U_g} - Q \frac{R}{U_E \cdot U_g} \tag{5.26}$$

Simplified this is equal to:

$$(U_E - U_G) = I_P R + I_Q X$$

$$\delta = I_P \frac{X}{U_g} - I_Q \frac{R}{U_g} \qquad\qquad (5.27)$$

One can further assume R small, because the L_{f2} is included in the grid impedance. Assuming R << X, indicates that P is given by $\delta \cdot U_E$, and reactive power Q delivered from the inverter is given by $(U_E - U_g)$. In a distribution grid, however, the resistance of the wires may be higher compared to higher voltage grids [55]. Including resistance in the power flow calculation, improves the reactive power step response.

The power flow control is closely connected to the voltage- and frequency control of an eventual island. The standards given by IEEE which specify that a DG should not supply reactive power, will here apply for the anti-islanding control algorithm. This is due to the fact that the reactive power compensation could compromise the ability of the DGs to detect an eventual island. The major difference between voltage support and anti-islanding control in this work is simply the sign of the active power control, as shown in Figure 60.
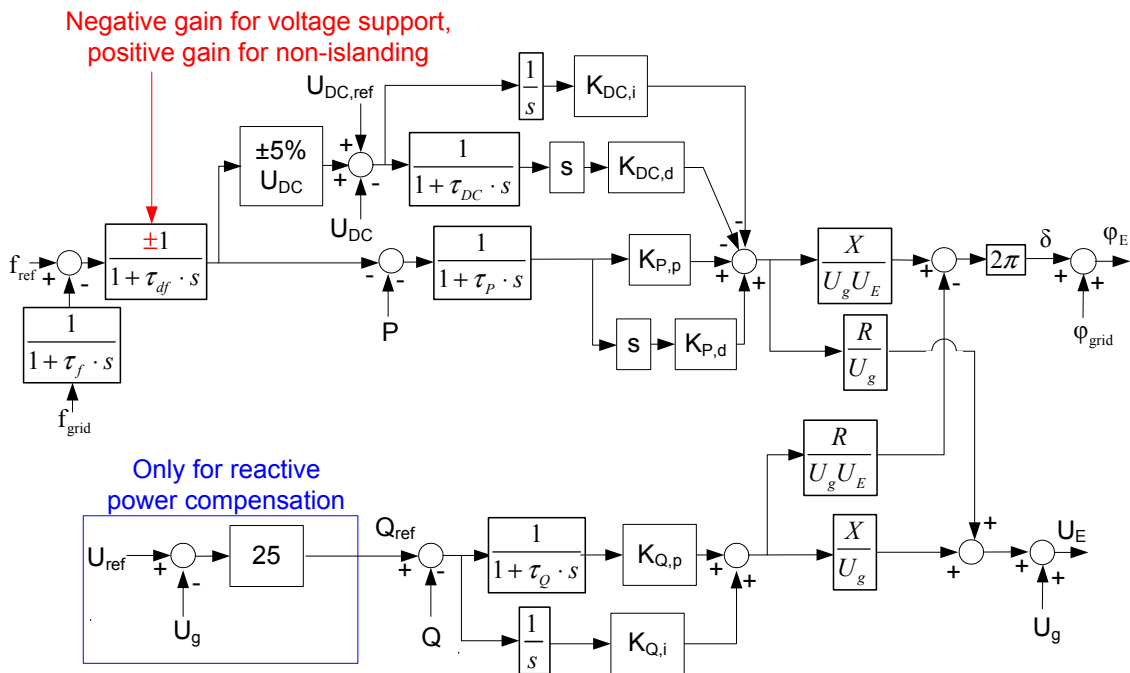
Figure 60: The active and reactive power controllers used, in per unit. The DC power is controlled using a 5 % droop, resulting in a frequency droop of 2 % in steady-state for the active power control.

The parameters used for simulation and laboratory testing are summarized in Table 13.

Table 13: Power controller parameters.

Parameter	Value	Comments
τ_{df}	9.49 ms	Low-pass filter time constant for frequency droop.
τ_f	19.94 ms	Low-pass filter time constant for frequency measurement.
τ_{DC}	19.49 ms	Low-pass filter time constant for DC derivative controller.
τ_P	19.49 ms	Low-pass filter time constant for active power controller.
τ_Q	39.49 ms	Low-pass filter time constant for reactive power controller.
X	0.0632 pu	The two inductances of the LCL-filter, summed.
R	0.0592 pu	The inductors internal resistances, summed.
$K_{DC,i}$	157	DC-link controller integration gain.
$K_{DC,d}$	0.157	DC-link controller derivative gain.
$K_{P,p}$	1.25	Active power controller proportional gain.
$K_{P,d}$	0.00628	Active power controller derivative gain.
$K_{Q,p}$	0.2	Reactive power controller proportional gain.
$K_{Q,i}$	2	Reactive power integrating gain.
P_{nom}	5000 W	Nominal power

5.3.1 Voltage support algorithm

With the emerging use of DG, there have been proposed solutions which form grid islands in order to isolate grid faults. However, the control algorithms used are contrary to the anti-islanding control applied to most DGs today. It is therefore useful to have a closer look at how to intentionally island a part of the grid.

Voltage and frequency droop are commonly used to control reactive power and active power respectively in microgrids. Droop control has been presented by many, for example Lopes et al. [56]. The droop method used in this work is shown in Figure 61 and Figure 62.
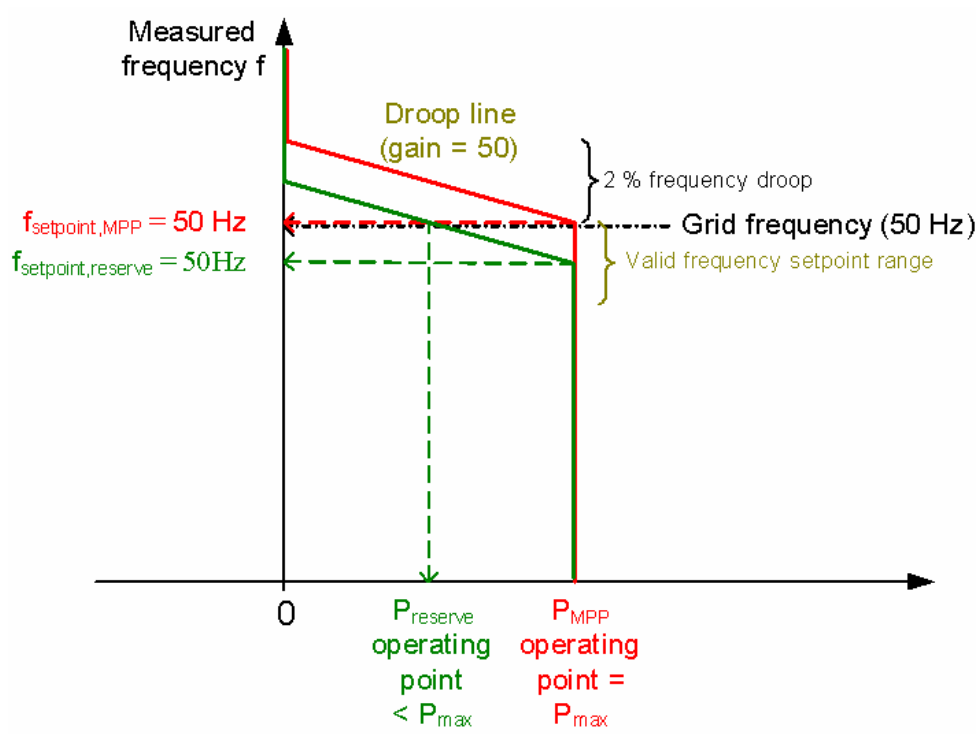
Figure 61: Frequency droop control for voltage support control algorithm.
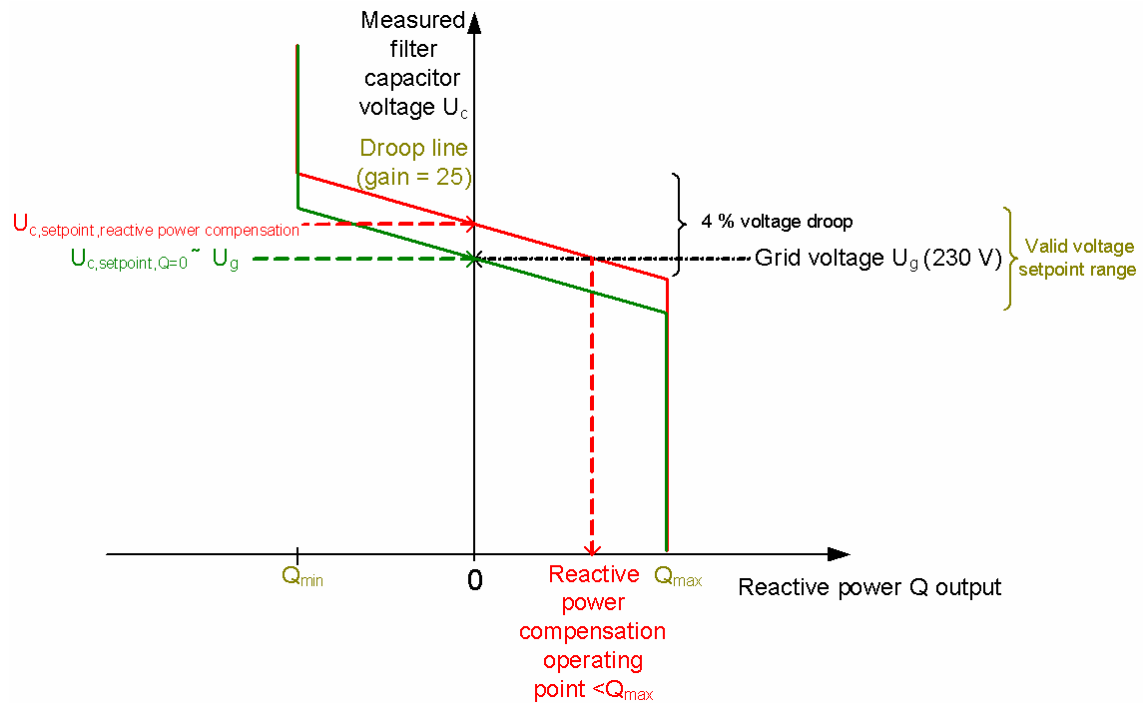
Figure 62: Voltage droop control for voltage support control algorithm.

The voltage support algorithm supports islanded operation. For safety reasons, the network owner should have guaranteed control of an eventual island. This can be achieved by allowing voltage support only when the communication is operative.

5.3.2 Anti-islanding algorithms

According to current standards and recommendations, a DG should disconnect itself from the grid in case of grid failure. The admissible deviations for grid voltage and frequency from nominal values are specified by [10]. The tightest tolerances specified (with longest clearing time) can be visualized as a window of safe operation as shown in Figure 63.
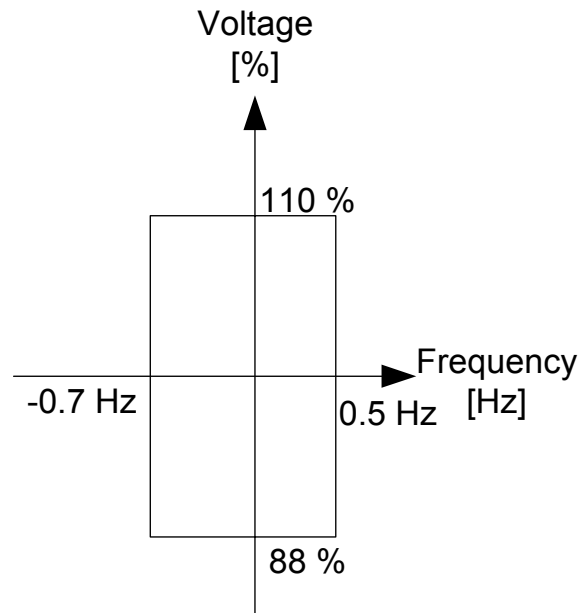
Figure 63: The frequency- and voltage tolerances for the longest clearing time in IEEE 1546 [10].

This window of safe operation gives a guarantee against unintended islanding when the loads do not balance the production. This is the case when there is low DG concentration. As DG becomes the major energy supplier in the electrical grid, this tolerance window alone cannot guard against unintended islanding. A high concentration of DGs may give a situation where loads and production balance. An island may then be stable in spite of the given frequency- and voltage tolerances. Additional methods should be applied to avoid islanding under these circumstances. Several methods for improving the reliability of island detection have been presented:

1. Active sensing of grid impedance changes.
2. Perturbing reactive power Q, and calculating the cross-correlation of Q and rate of change of frequency [57].
3. Grid voltage harmonics, negative sequence amplitude derivatives, phase jumps and rate of change of frequency.
4. Positive feedback for voltage and frequency; making an eventual island unstable.

The first two methods have an inherent limitation concerning scalability. A large number of DGs injecting test signals will dilute the response. At some point the response is impossible to analyze. Group 3 and 4 in these methods can be implemented in a grid with a high concentration of DGs. They are scaleable. Group 3 is based on the fact that the removal of a stiff voltage source will affect several parameters. For example the amplitude of harmonics can be used for detecting islanded operation [58]. The state-space observer used in the presented inverter control measures some harmonics, which can also be used for islanding state detection. Voltage unbalance has also been used for islanding detection [59]. Due to the close dependence of the actual load, this group of methods is not investigated further. Group 4, positive feedback methods, has an inherent follow-the-herd philosophy which is scaleable. The Zone of No Detection (ZND) is among the smallest published.

In order to stabilize a system, negative feedback is used in many applications, including power flow in paralleled inverters. Positive feedback is the opposite of stabilizing a system; it makes an eventual grid island unstable, where a small deviation is amplified. The increasing deviation eventually violates the voltage/frequency tolerances, and the DG will then disconnect itself from the grid. Positive feedback is added to Figure 61 in Figure 64.
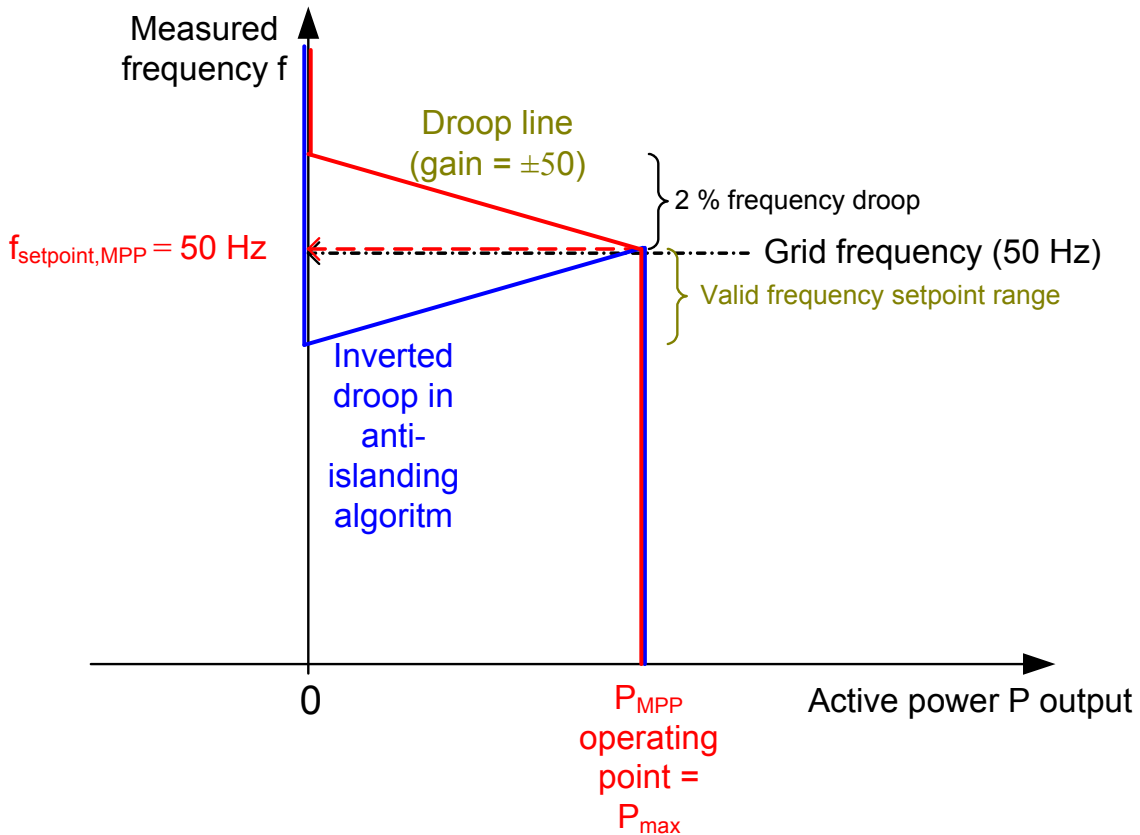
Figure 64: Blue line is the inverse droop control used for positive feedback in the anti-islanding algorithm. Red line indicates droop control for intentional islanding.

The DG can have positive feedback both concerning frequency, and voltage amplitude. This can be implemented for both the rotating frame, and the stationary frame. Band pass filtering is often used in the literature in order to avoid affecting steady-state power control. This was difficult to use in the laboratory setup, probably because the inverter was voltage controlled. According to IEEE standards [10], the reactive power must be close to zero. Positive feedback is then only applied for the frequency. Since the inertia of the load is not known, applying a band-pass filtering may fail for large inertia loads (long time constants).

5.4 DC/DC-converter controller

The DC/DC-converter controller takes part in the active power control of the system, when there is more energy available from the energy source compared to the consumption. As it will be described in Chapter 6, there are three concurrent DC/DC-converter controllers. The most critical controller is the output voltage controller. It reduces the input power in case of excessive power available from the source. The two voltage controllers are identical, but because this situation is most critical, it is the one shown for the pole assignment presented in this chapter.

In order to avoid oscillation between the inductors and capacitors internally in the DC/DC-converter, current feedback is applied. The controller has a state observer and state feedback similar to the inverter voltage controller. Additionally, an integration term is added in order to avoid steady-state errors. The switching frequency is 22 kHz. The sampling, the observer and the controller are synchronized to the switching. Except for the use of Hall-effect sensors, the observer structure is identical to the inverter controller and thus requires no further description.

The controller is designed to be over-damped, in order to not cause oscillations of the DC-link voltage due to interactions with the inverter. The three concurrent controllers use the same state observer. The DC/DC-converter is modeled as a CLC-filter. A voltage source in series with the inductor models the PWM action. The state observer models only the input and output capacitors inside the DC/DC-converter, in addition to the inductor current. This design is based on the worst-case scenario concerning stability, represented by lowest amount of output capacitance. Even though it is not modeled by the observer, the modeling error introduced by connecting to the DC-link capacitance is not problematic.

If the DC-link is not connected, the model equals the physical process. Thus the separation theorem holds, and the estimated state feedback equals direct state feedback. When the DC-link is connected, however, the physical process deviates from the model. The separation theorem is not valid. This gives new poles of the observed state feedback. Due to the fact that the process in this case is slower than the model, and the observer is close to dead-beat, the modeling error does not affect the stability significantly. The pole placement in the situation of a connected DC-link capacitance is shown in Figure 65.
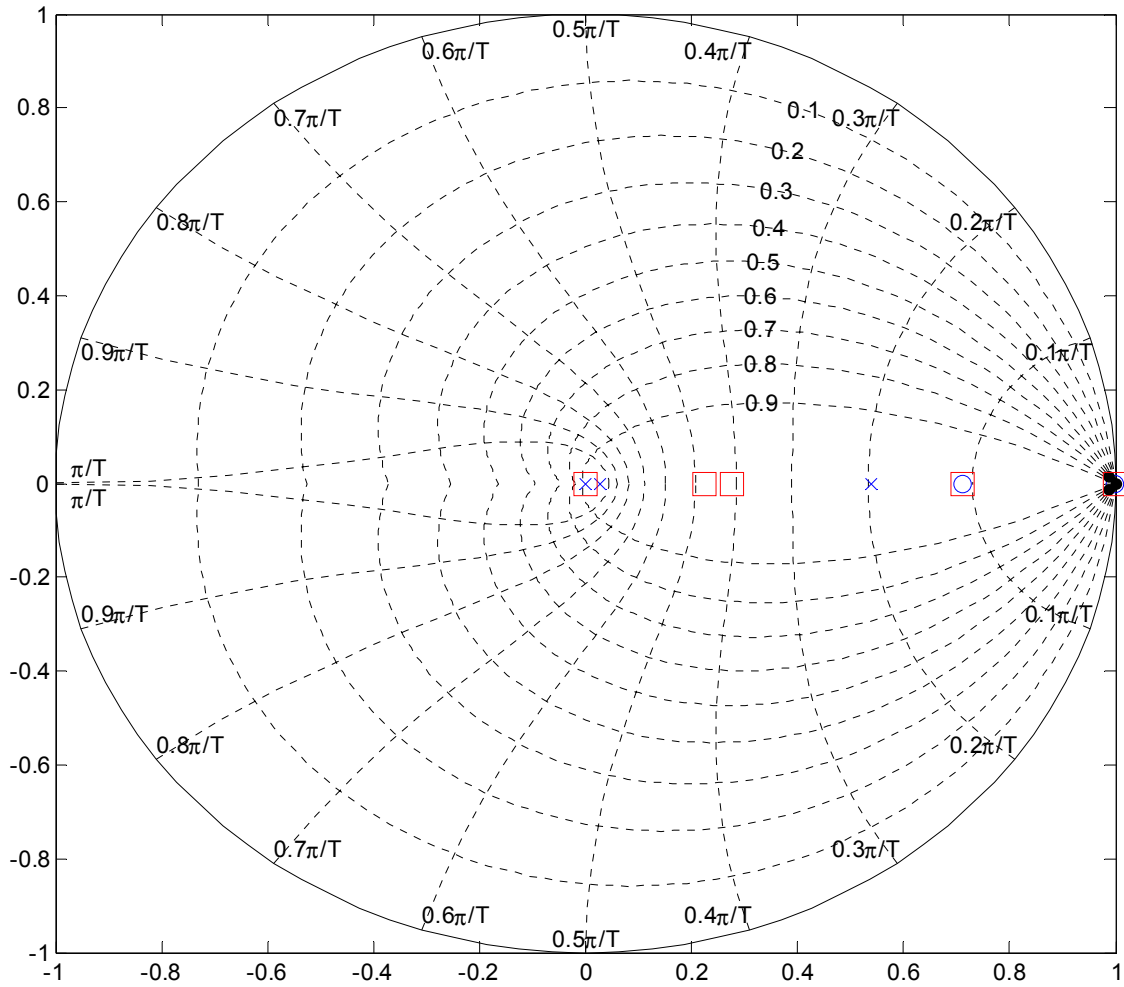
Figure 65: DC/DC-converter poles of the output voltage controller with the DC-link capacitance connected: System poles with feedback (.), observer poles (x) and squares are estimated state feedback poles.

The output voltage is droop controlled. The droop is 5 % referred to the inverter power. This droop helps stabilizing the DC/DC-converter controllers, and it is thus not included in the controller design. The parameters of the DC/DC-converter and the controller are summarized in Table 14.

Table 14: DC/DC-converter and controller parameters.

	Parameter	Value
DC/DC-converter	Converter capacitance	18 μF
	DC-link capacitance	3.3 mF
	Inductance (referred to primary)	2 mH
Controller	Switching frequency	22 kHz
	Current feedback	0.35 pu
	Voltage feedback	0.85 pu
	Integration time constant	47.9 ms
Observer	Current estimation gain	0.95 pu
	Voltage estimation gain	0.46 pu

6 Software

Digital controllers are continuously becoming faster and cheaper. They represent a reconfigurable control option for power electronics. Digital controllers can also be remote adjustable by the use of communication. All controllers described in this thesis are implemented in software, except the IGBT protection (over-current and DC-link voltage). The purpose of this chapter is to describe how the theory from the previous chapters has been implemented. Figure 66 shows the connections of DSPs and computers in the DG laboratory setup.
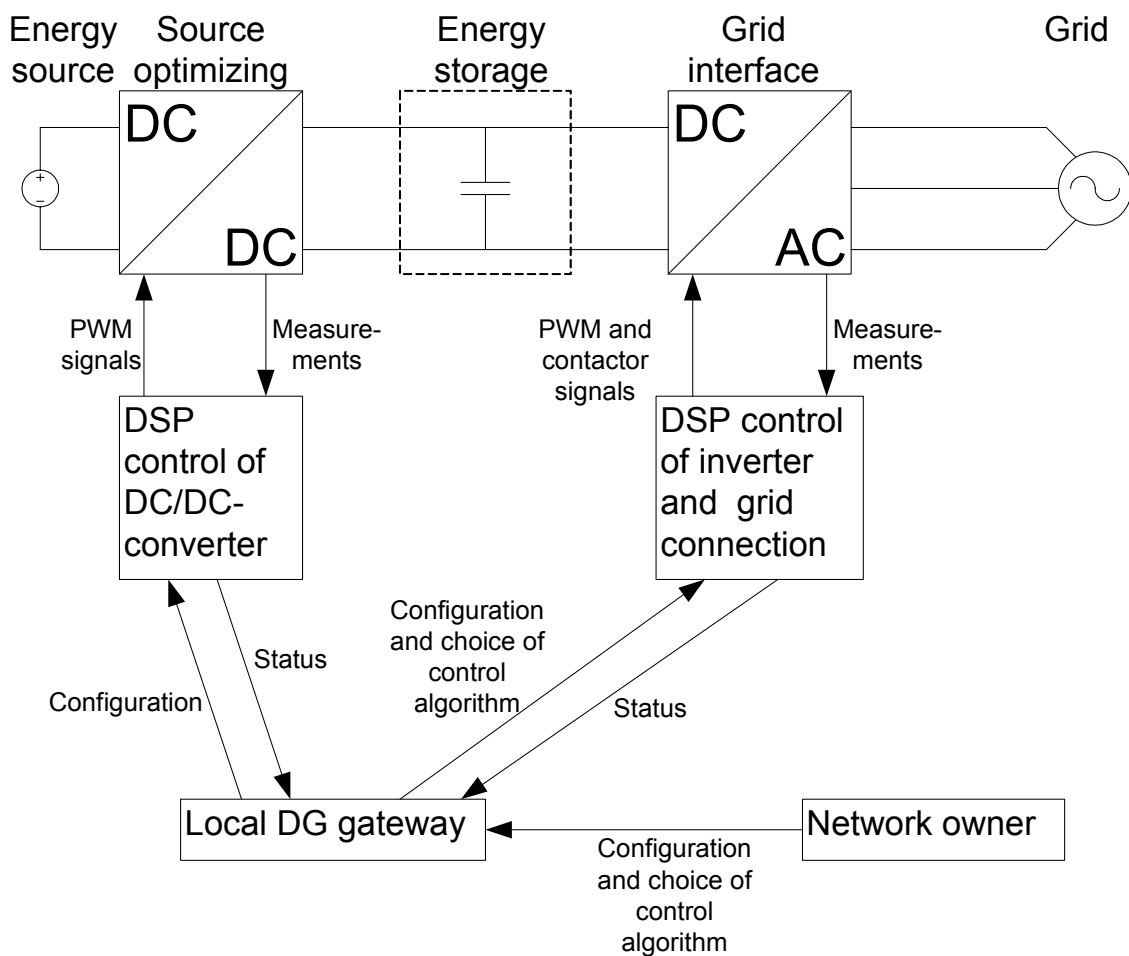
Figure 66: The DSPs and the computers connections in the laboratory setup.

The DG gateway is a standard personal computer acting as an interface between the Internet and the local real-time communication bus based on Modbus/CANbus. It also is programmed to implement the flooding algorithm. If a communication error occurs, it

also takes local actions by commanding a safe control algorithm, which may be anti-islanding algorithm.

6.1 Software framework for controllers

The converter control software which is real-time is programmed in C++. The targets of these programs are two Texas Instrument TMS320F2812 digital signal processors. They are 32-bit fixed-point 150 MHz digital signal processors suitable for power electronics control.

The q-20-format is used when 32 bits are available. This specifies that the 20 least significant bits represents the fractional part of a decimal number. The 12 most significant bits represents the signed integer part. This system can thus represent a number ranging from -2048 to 2047.999999 with an accuracy of 10^{-6}.

The DSPs are programmed to handle the analog-to-digital conversion (ADC), as well as controllers and communication. The two first tasks are hard real-time and must be handled within the time constraints. The DSPs and the local computer use an adapted Modbus for communication. The local control and the communication should be separated. They are therefore represented as two separate processes communicating through a shared memory map suitable for Modbus. Each process has two threads operating in the same memory space, but with different priority and timing. The main software structure is shown in Figure 67.
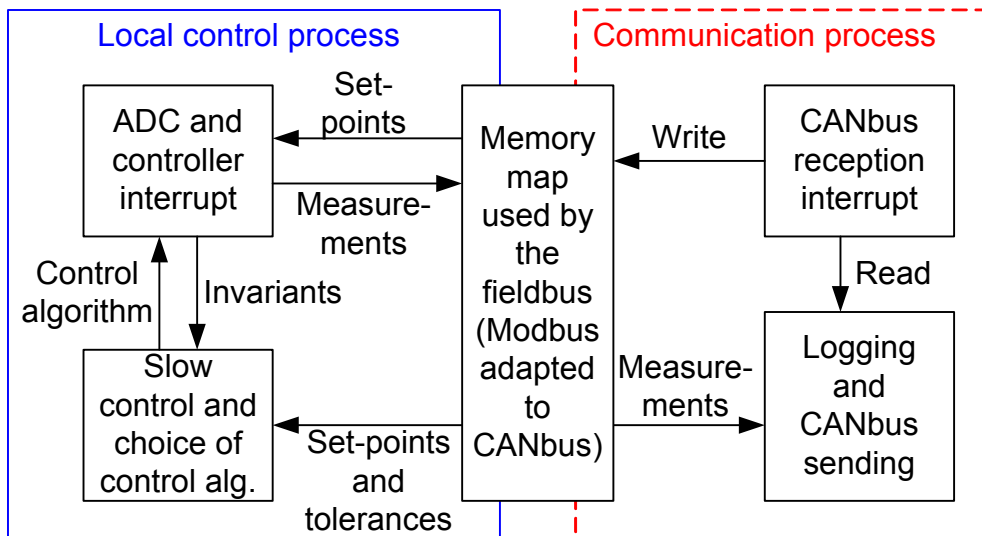
Figure 67: The software framework for the controllers of the inverter and the DC/DC-converter.

The sampling and switching is synchronized using the internal interrupt structure of the DSP. Small timing variations would cause the ADC to be erroneous due to changing integration time. The ADC task therefore has the highest priority. The ADC is directly

followed by the state space observer and the controller calculations. This ensures the lowest time delay possible from measurement to control action. Fault handling concerning fast current limiting is also a task with strict timing constraints. Such functions are therefore also included in this interrupt procedure (ADC and controller task).

The communication is event-driven through a CANbus reception interrupt. This interrupt is however preemptive. If an ADC interrupt occurs, the communication interrupt routine is paused so the ADC interrupt can finish in time. When there is no pending ADC interrupt, the communication interrupt can continue execution. The communication interrupt only handles the reception of messages. The execution of received tasks is left to the next two threads to be described.

In addition to the pure hardware based interrupts, two threads are running cyclically every millisecond, one associated with the local control and the other associated with the communication. The first thread is synchronized to the ADC interrupt but is not a part of it. It mainly handles the choice of safe control algorithms and slow control such as MPPT. It monitors and controls slowly varying parameters such as frequency or PV power. The second cyclical thread handles the further execution of received tasks from the CANbus. The tasks may be for example logging of a couple of parameters for a predefined time. This task is not preempting any interrupts, because it is soft real-time only. A time constraint of one millisecond is sufficient. An example of the real-time schedule of the DSP is shown in Figure 68.
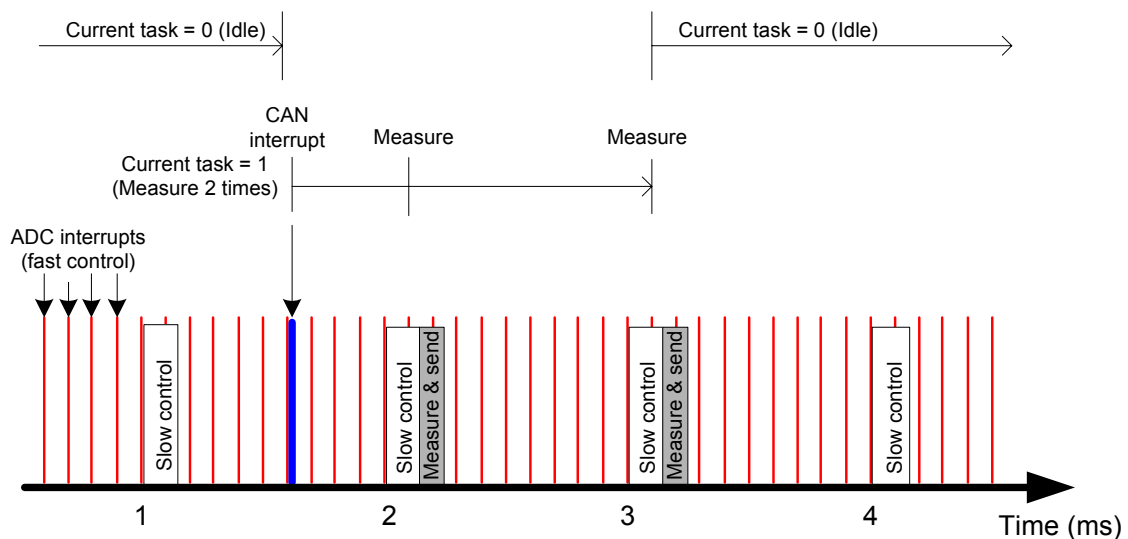
Figure 68: The real-time schedule implemented for the DSP.

For both DSPs, the task priorities are shown in Table 15.

Table 15: DSP program task priorities.

Priority	Task
1	Switching (ADC interrupt)
2	Communication: Preemptive CANbus interrupt
3	Slow control and control algorithm changes
4	Different tasks received by previously received Modbus commands

The presented structure represents a framework for the two converters connected to the CANbus: The DC/DC-converter and the inverter. The local control processes will be described for each of these converters. This will be followed by a description of the local communication process.

6.2 DC/DC-converter controller

The main aim of the DC/DC-converter control is MPPT. This is often based on voltage or current controllers. Voltage control is chosen due to its main dependence on temperature, which is slower varying compared to the current, as described in Chapter 3.

There are three different controllers operating concurrently: The primary controller serves the MPPT by controlling the input voltage. In cases when the load is lower than the production, the output voltage must be limited. This dual role is accomplished using a copy of the previous controller, but applied to the output voltage instead of the input voltage. In order to avoid overloading of the converter, a third input current controller is applied. The controllers are based on state feedback with integration added (0.0479 seconds integration time). The concurrent controllers have the same gains, but there are differences in which voltages are included. The controller commanding highest input voltage (least amount of input power) gains access to the PWM module. The other two controllers saturate. This is equivalent with application of the highest duty cycle of the three as shown in Figure 69.
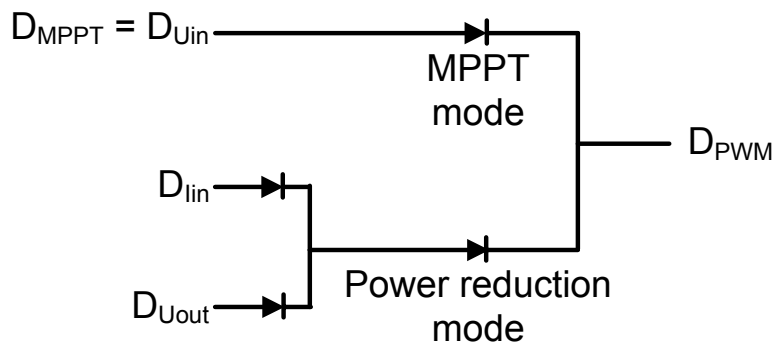
Figure 69: The DC/DC-converter controller choice based on highest duty cycle D.

The duty-cycle from the controllers can range from -0.45 to 0.45. The negative number is defined as step-up action of the converter, while a positive number gives step-down action of the PV panel voltage.

6.2.1 DC/DC-converter safe control algorithms

A standard DC/DC-converter topology for MPPT can have the control algorithms as shown in Figure 70.
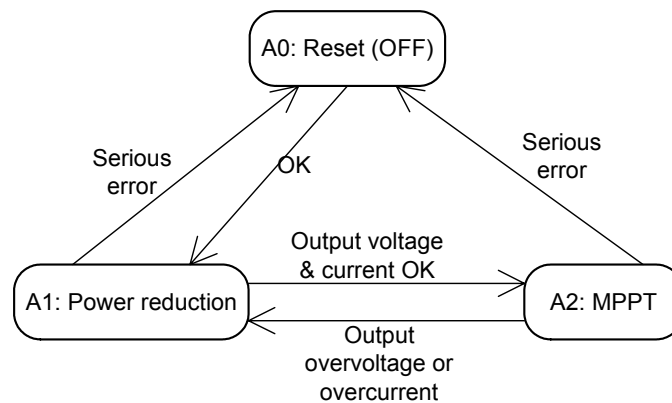
Figure 70: DC/DC converter control algorithms.

The set of control algorithms includes the MPPT algorithm, and the reduced power algorithm, which is necessary not only for reducing the power in UPS or voltage support inverter control algorithm. It is also vital for safety reasons in case the load or grid are disconnected. The most preferred control algorithm is A2: MPPT. The list of prioritized control algorithms is shown in Table 16.

Table 16: Prioritized control algorithms.

Priority number	Control algorithm
First	A2: MPPT
Second	A1: Power reduction
Third	A0: Reset (system OFF)

A decision table can be defined, so that a given control algorithm can only be entered if some specific tolerances are OK. In order to implement Figure 70, one solution is to use a status byte. In the following, "status byte" can also mean a 16-bit or a 32-bit status word. Every bit is associated with a parameter which is TRUE if the parameter is within its tolerances. Related work has been described by Rosin et al. [27] and Polic and Jezernik [60]. The target here is to develop a decision table that defines the required change of control algorithm caused by a tolerance violation. The requirements to change to a given algorithm (control algorithm invariants) can be described by a Boolean

decision table where 1 = required and 0 = not required. This is compared to a status byte where 1 = OK and 0 = not OK. All ones in a requirement byte (a row in the decision table) must be OK in order to enter a control algorithm, or to stay in the present algorithm. This can be expressed as follows:

$$\left(status \wedge DT_{\text{algorithm k}}\right) = DT_{\text{algorithm k}} \tag{6.1}$$

The decision table DT can define most safety-related control algorithm transitions in a single page. It is possible to implement compactly in a digital controller. In Table 17, voltage and current are connected to the transition between algorithms A2 and A1.

Table 17: Decision table for the DC/DC-converter system control algorithms.

Current control algorithm	No output over-voltage	No input over-current	Heat sink temperature OK (not implemented)	No stop system signal	Hexadecimal representation
A0: Reset (OFF)	0	0	0	0	00
A1: Power reduction	0	0	1	1	C
A2: MPPT	1	1	1	1	F
Bit number	0	1	2	3	

The decision table can also be visualized in a commonly used interlock circuit scheme implementing Table 17, shown in Figure 71.
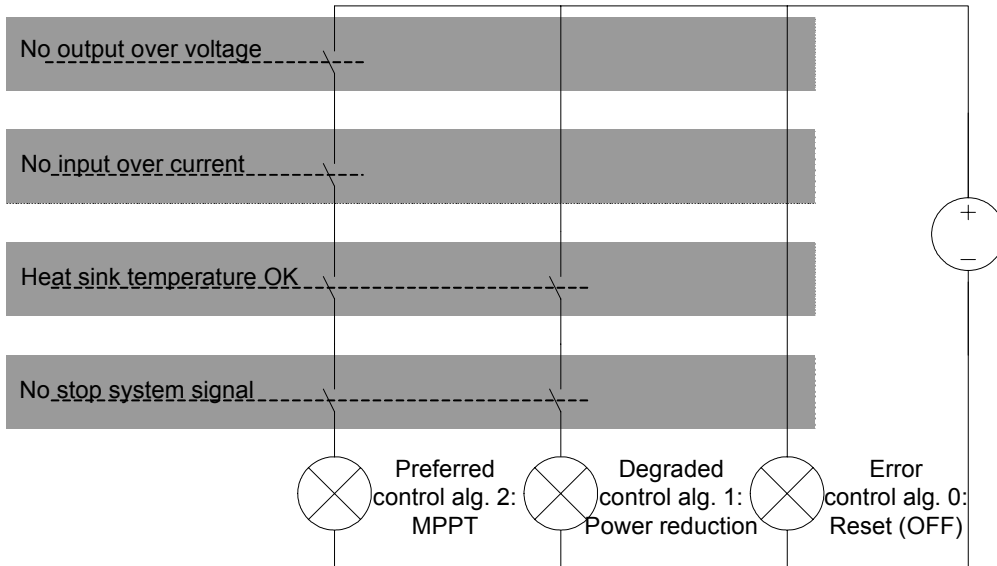
Figure 71: A circuit-scheme representation of Table 17.

The DC/DC-converter used here is the previously presented flyback converter, which is a bit special: It can both step up, or it can step down the input voltage. These two options represent two PWM control algorithms, which are independent of the previously described system control algorithms. A last possibility which can be included in some DC/DC-converters is a bypass. It can be useful in order to avoid switching losses when the PV panel is closely matched to the battery voltage. These PWM related control algorithms represent a level below the system control algorithms in the software hierarchy. The available PWM control algorithms are shown in Figure 72.
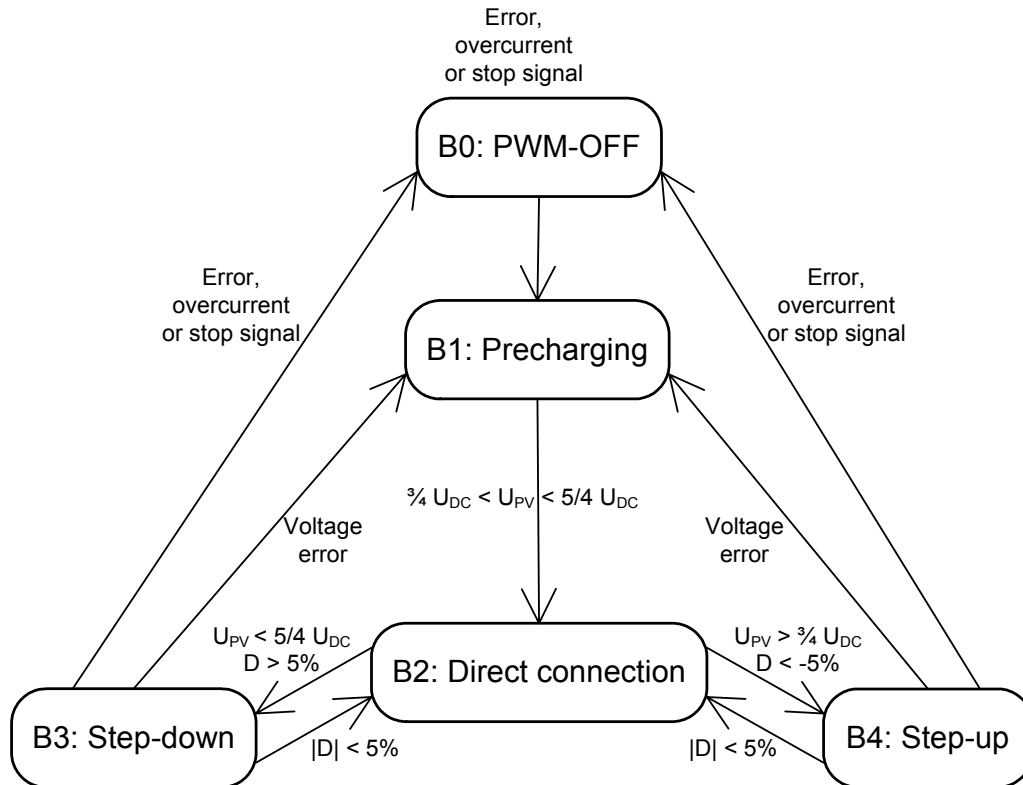
Figure 72: The PWM control algorithms, which are active under system control algorithms A1 and A2 in Figure 70.

The list of preferred PWM control algorithms is shown in Table 18.

Table 18: The prioritized PWM control algorithms.

Priority number	Control algorithm
First	B4: Step-up voltage
Second	B3: Step-down voltage
Third	B2: Direct connection
Fourth	B1: Precharging
Fifth	B0: Reset (PWM OFF)

The PWM control algorithm invariants are defined by the decision table in Table 19.

Table 19: PWM control algorithms decision table, which are active under system algorithms A1 and A2.

Control algorithm	$U_{in} <$ max(5/4 U_{out}, 10)	$U_{in} >$ ¾ U_{out}	D > 5%	D < -5%	No high input over-current	Run PWM	Hexadecimal representation
B0: PWM-OFF	*0*	*0*	*0*	*0*	*0*	*0*	*00*
B1: Precharging	*0*	*1*	*0*	*0*	*1*	*1*	*32*
B2: Direct connection	*1*	*1*	*0*	*0*	*1*	*1*	*33*
B3: Buck	*1*	*0*	*1*	*0*	*1*	*1*	*35*
B4: Boost	*1*	*1*	*0*	*1*	*1*	*1*	*3B*
Bit number	*0*	*1*	*2*	*3*	*4*	*5*	

6.3 Inverter controller

The laboratory setup represents more than one function using the same inverter. This implies mainly increased software complexity. The different control algorithms have some common denominators, but many aspects are also different. All control algorithms are based on the same voltage controller, but the power control methods are different. The control is therefore separated in a common, fast filter capacitor voltage controller (red box in Figure 73), and a changing, slower power controller (blue box shown in Figure 73).
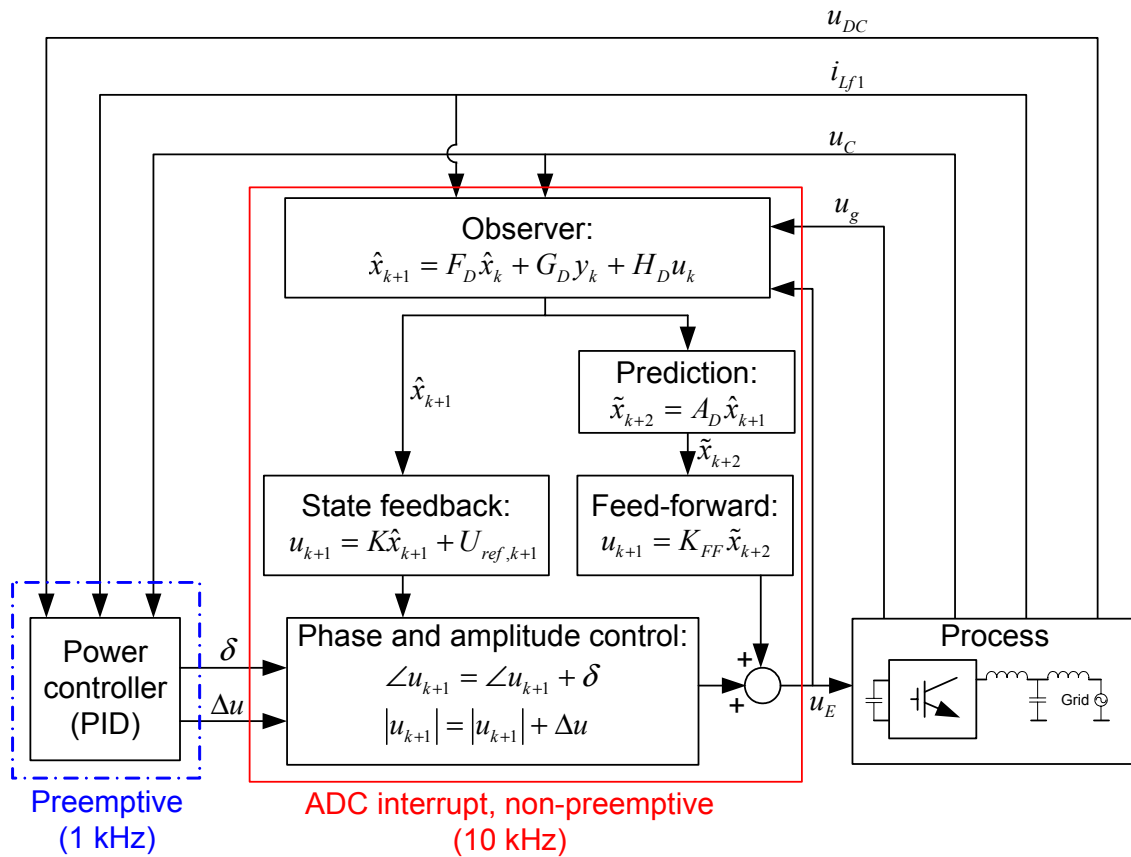
Figure 73: The separation of the voltage controller (Sections 5.1-5.2) and the power controller (Section 5.3).

6.3.1 Inverter safe control algorithms

In addition to LCL-filter control the inverter controller is responsible for the operation of the electromechanical contactor for grid connection. Synchronization and grid fault detection are therefore in the inverter controller domain. This and communication timeout are parts of the decision table for the inverter. The system detects tolerance violations, and changes to a safe control algorithm, as shown in Figure 74, which is identical to Figure 5.
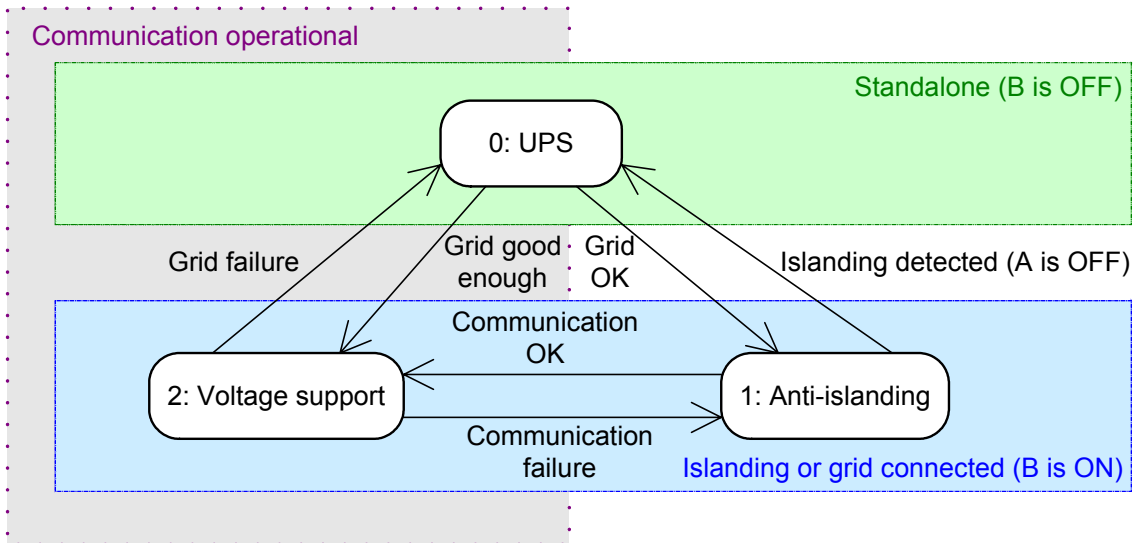
Figure 74: An overview of the main inverter control algorithms.

Besides the parameters of the type previously described, the network owner may want to define a set of tolerances specific for a certain location in the grid. For example when communication is present, (when the network owner has real-time control over the inverter) one set of voltage and frequencies may be defined. If communication fails, it is replaced by a tighter set of tolerances. The two grid-connected control algorithms can be summarized as follows:

2. **Communication OK:**
   Voltage support including reactive power compensation and harmonic voltage reduction are allowed. The voltage and frequency tolerances are wide.

3. **No communication:**
   Anti-islanding control is required. Reactive current and harmonic currents are not allowed and voltage and frequency tolerances are set tight.

Safe operation is first priority. For example the network owner may specify relatively large frequency- and voltage tolerances. This may lead to an undetected island connection state, when communication is lost. Therefore the frequency- and voltage tolerances are defined tighter in the anti-islanding control algorithm (3), in addition to controlling the inverter using an anti-islanding algorithm. This ensures that active power production is not interrupted by temporary communication failures. An island connection state will then always be under the control of the network owner. The inverter has a number of internal control algorithms. The detailed version of Figure 74 including all internal control algorithms of the inverter is shown in Figure 75.
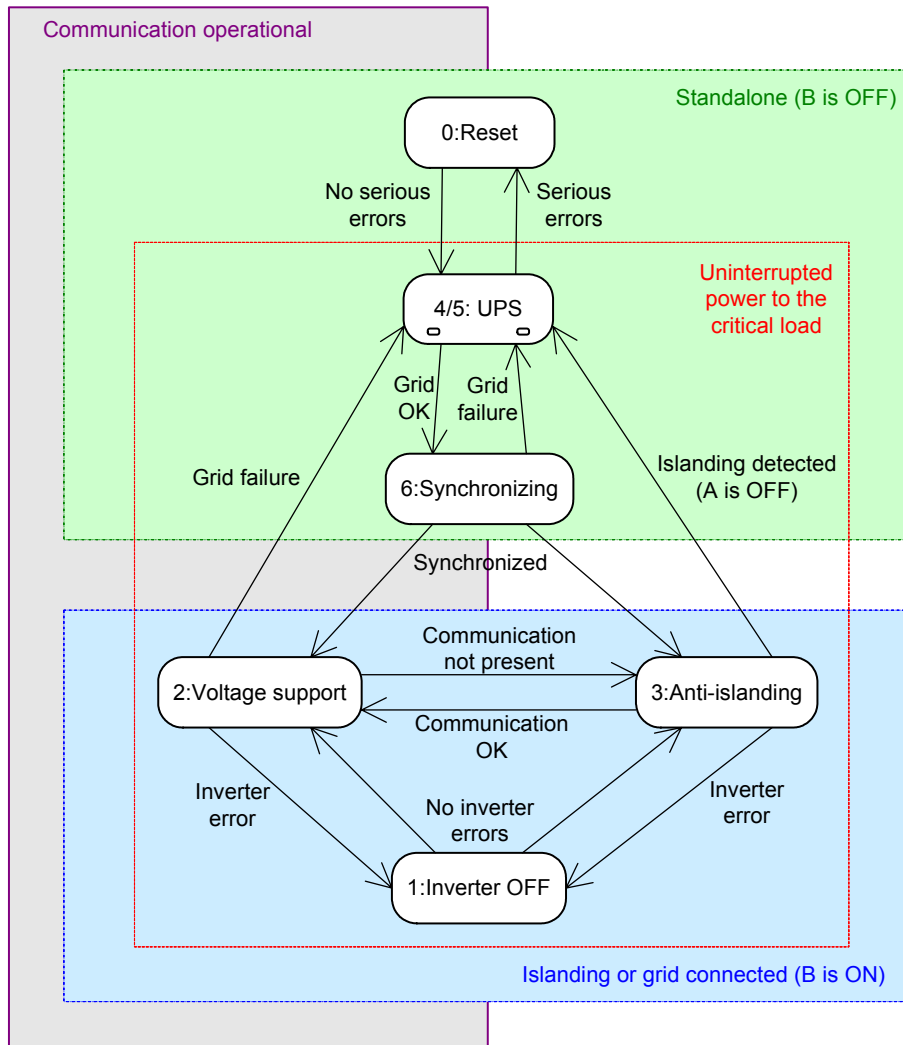
Figure 75: Detailed inverter control algorithms.

The reset (0) represents a fault mode, where the system is safe and dead. In inverter OFF (1), parts of the system can be shut OFF, but the critical load can still be supplied by the grid. When all status bits are OK, the voltage support control algorithm (2) is active, offering all the flexibility available by the inverter (power control and more). If communication fails, the anti-islanding control algorithm (3) offers increased safety against islanding, but reduced flexibility. If the grid fails, or connection is prohibited, the inverter can still supply the local load in UPS control algorithm (4/5). Algorithm 4 has been used as a test mode, and it does not differ from mode 5 concerning the inverter control algorithm. The communication status is the only difference. Phase and amplitude synchronizing in control algorithm 6 is necessary before reconnection to the grid. A decision table defining control algorithm invariants is shown in Table 20.

Table 20: Decision table for a grid-connected inverter with electromechanical contactor.

Control algorithm	AC freq. tight	AC volt. tight	AC volt. broad	DC volt.	AC cur-rent	AC freq. broad	Phase & ampl. diff. OK	Driver level faults	Toler-ances updated	Com-muni-cation OK	DC over volt OK	AC over volt. OK	Grid con-nect OK	Island OK	DC volt. max P	Hexa-decimal repres-entation
0: Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
1: Inverter OFF	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	180D
2: Voltage support	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	3FFC
3: Anti-islanding	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	5DFF
4: UPS w/ com.	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0298
5: UPS w/o com.	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0098
6: Phase and amplitude synch.	1	1	1	1	1	1	0	1	1	0	1	1	0	0	0	0DBF
Bit number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

The decision table must also be supplemented with a priority list of control algorithm transitions, as shown in Table 21.

Table 21: Inverter control algorithms priority list.

Current control algorithm	**Prioritized list of control algorithm transitions (first priority to the left)**
0 (reset and error algorithm)	4, 5, 1, 0
1, 2 & 3 (grid interactive algorithms)	2, 3, 4, 5, 1, 0
4, 5 (UPS algorithms)	6, 4, 5, 1, 0
6 (synchronizing)	2, 3, 6, 4, 5, 1, 0

The presented safe control algorithm transition has no inherent guarantee against one algorithm oscillating against another algorithm. It is quite probable that a control algorithm transition causes a transient. Unless precautions are taken, it may send the system to another control algorithm. This algorithm can potentially send the system back to the first one, and there will be a deadlock situation. It is important to limit how fast a control algorithm transition can happen. It should be slower than these potential oscillations.

One solution is to continuously check for changes in the status byte, even when waiting for an electromechanical contactor to change from ON to OFF or vice versa. This can also lead to a deadlock situation if periodic errors are detected, such as an unbalanced grid voltage would cause. The continuous resetting of the electromechanical contactor time cancellation timer will effectively stop any control algorithm change.

There are some methods that can be used to reduce this problem. One effective solution to the above-mentioned problems is to execute the change from one control algorithm to

another, even if the status byte changes in the mean time. For compensation of the electromechanical contactor time delay, a control algorithm change is required after a predefined time has elapsed. However, the desired algorithm is evaluated every millisecond during this period of time. When this predefined time has elapsed, the algorithm that has been valid for the longest time will become the new control algorithm. Assuming every algorithm transition loop (from one algorithm to another and back again) has a finite transition time, this method addresses the potential transient failure behavior. It also ensures that the maximum algorithm transition time is defined and finite.
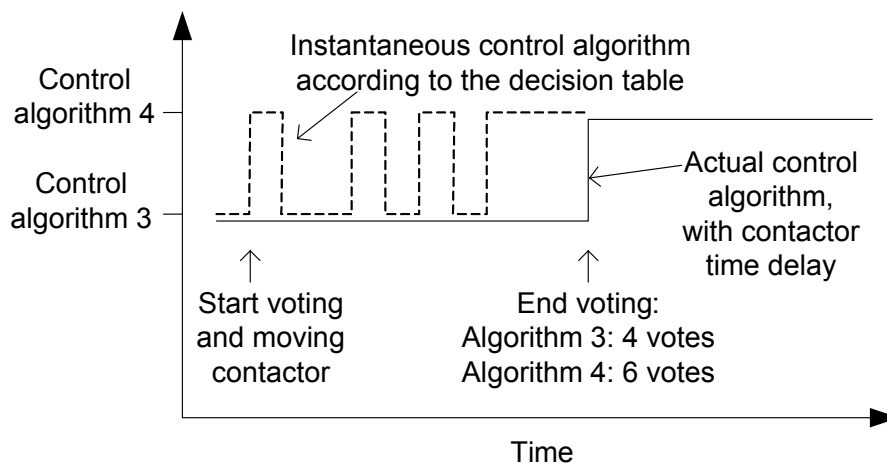
Figure 76: The compensation of the electromechanical contactor time delay using a voting strategy.

The changes in control algorithms are a tradeoff between functionality and safety. It is not as time-critical as ADC interrupt, but it must have a deterministic execution period. This period should be long enough to filter the noisiest relevant parameters sufficiently. It should be short enough to prevent any damage to the hardware. The task must also be guaranteed to finish before the next execution cycle. One millisecond period was chosen as a decent tradeoff.

6.4 Local communication bus

The CANbus can give the converters requests of different kinds: Reading and writing parameters are some of the tasks. The timing of these tasks is not connected to safety. Therefore they are given the lowest priority. The Modbus protocol was chosen due to its simplicity. It is in fact not specified for CANbus. However, an adapted Modbus was implemented so that it better fits the use.

Modbus is based on mapping the different variables in a 16-bit address space. In a simple system as this, the needed address space is below 8 bits. Instead it is often necessary to measure two synchronized parameters, e.g. voltage and current. Therefore two 8-bit address fields were used. Modbus is an old standard, and it is simpler than

other protocols. For example most of the functionality needed can be implemented using only a few commands as shown below:

1. read
2. write
3. request ID
4. report ID

The mapping of the different parameters in a shared memory map is a way of decoupling the protocol and the application. In order to make a reasonable separation of the information, eight main entities were defined as shown in Table 22.

Table 22: The memory map of the CANbus communication protocol.

Addr	Parameters
0-31	Network and transactions
32-63	Tolerances for the decision table
64-95	Set-points for controllers
95-127	Price signals
128-159	Measured variables for metering
160-191	Measured variables for diagnosis
192-223	Measured inverter state-space variables
224-255	DC/DC-converter and energy storage

Measurements, set-points and tolerances were mapped in this way.

6.5 DG gateway software

In order to make a flexible test environment for communication and islanding, computers are used for communication and measurements. They were programmed using the graphical programming language G under Labview 7.1. This is suited for programming communication protocols, test sequences and measurements. This language has the benefits of having predefined modules for communication and measurements. It is also supported by hardware for measurement and communication.

The communication system is divided in a local CANbus based Modbus adaptation, and a global, PC-based Internet communication based on UDP and flooding. There are two computers in the system: The DG gateway computer and the computer connected to the testbench and simulating the network owner (energy management user interface). They communicate over Internet using a UDP-based flooding algorithm. The components of the test setup systems are shown in Figure 77.
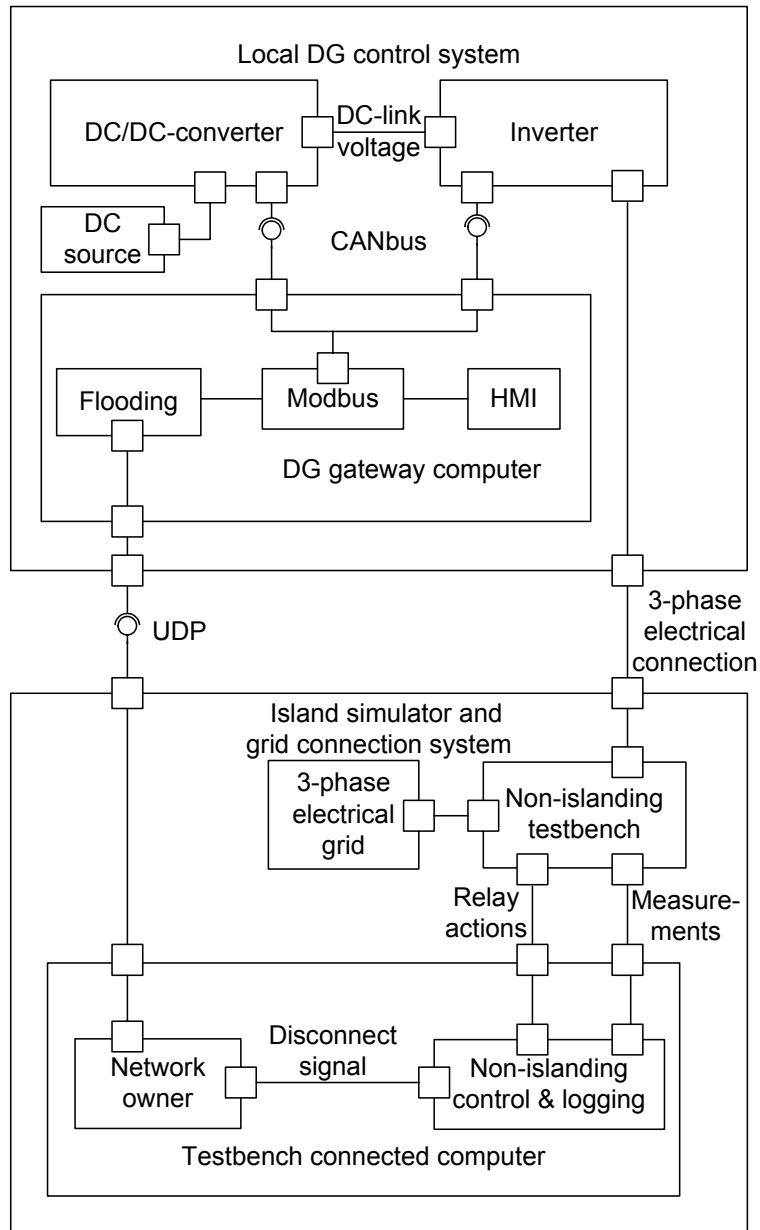
Figure 77: Components of the DG system and the testbench system.

The computers are running on Windows XP. One computer is a 400 MHz standard personal computer with a National Instruments CANbus card, placed near the inverter. The other computer is a National Instruments PXI-chassis for real-time applications. It is, however, used as a non-real-time computer because this was sufficient for the time scale of interest. It controls the testbench, and it also simulates the network owner.

Labview when running under Windows cannot give real-time guarantees. This is not a problem, because the hard real-time requirement represented by the converter

controllers and the electromechanical contactor is handled by the DSP. In any case Internet communication cannot be used in hard real-time systems. Adding a real-time computer to a chain involving non-real time communication would gain little. The system is therefore designed to take proper actions if a timeout occurs.

6.5.1 DG gateway

The DG connected computer acts as a gateway between the Internet (UDP messages), and the CANbus (adapted Modbus messages). A screenshot of the DG gateway is shown in Figure 78.
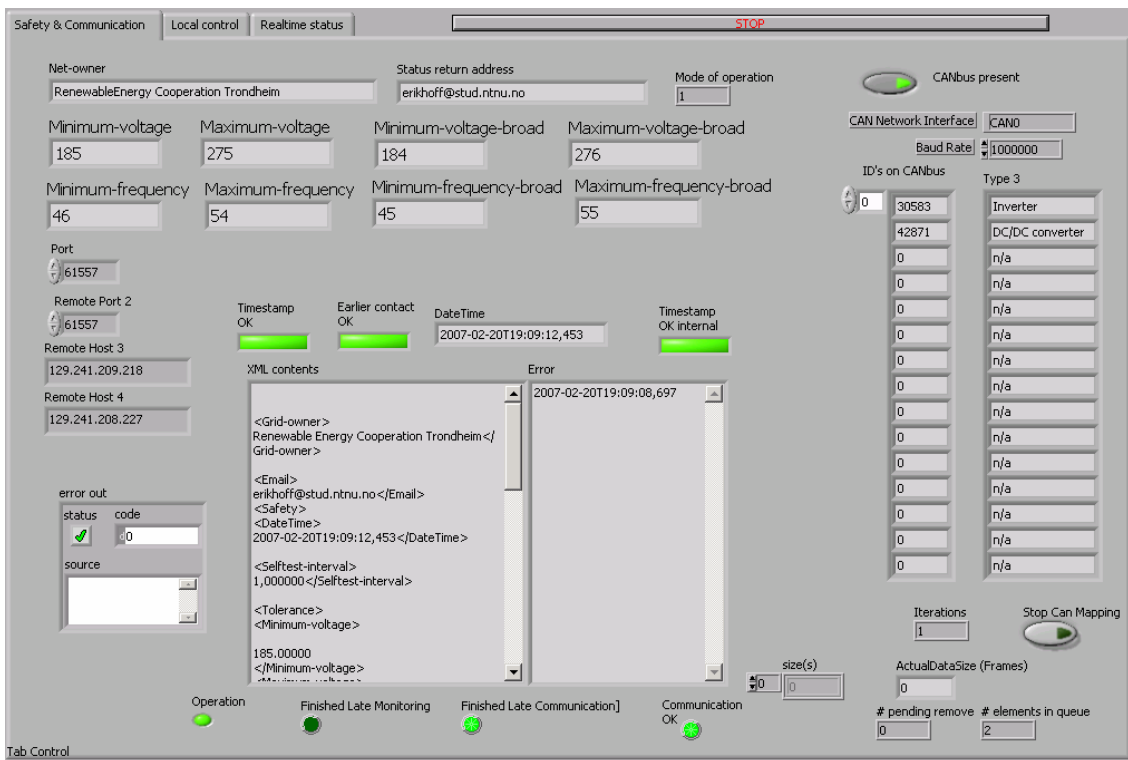
Figure 78: A screenshot from the DG gateway.

The CANbus network is implemented to control up to 16 DSPs independently. The communication is only tested from the computer to two DSPs. In case the Internet communication fails, the DG gateway commands the converters to a safe control algorithm. The CANbus communication task has first priority.

The second purpose of the DG gateway is to forward UDP messages according to the flooding algorithm. It is important to keep this fast.

The local control of the DG has least priority. This is a user interface for configuring the DG locally. Parameters of interest are: DC voltage tolerances, choice of network owner

to communicate with, address for error messages, and so forth. What is desirable here depends on the actual DG. Typically status information should be accessible here. A summary of the priorities are shown in Table 23.

Table 23: DG gateway computer task priorities.

Priority	Task
1	CANbus communication
2	Forwarding of UDP messages as a part of the flooding algorithm
3	Local user interface

The tasks of the DG gateway computer are shown in Figure 79.

1: Modbus / CANbus control:
- Network mapping of connected converters
- Resetting of the converters CANbus timeout
- Writing messages to the CANbus
- Reading measurements from the CANbus
- Execution period: 250 ms

2: Flooding:
- Flooding algorithm
- Timestamp check
- Decide control algorithm
- Execution period: 100 ms

3: HMI:
- Setting local control parameters
- Translating XML to Modbus
- Initiating logging of parameters
- Displaying parameters
- Execution period: 250 ms

Figure 79: The three threads of the DG gateway computer.

The two time-critical threads have a sequential program structure. The Modbus/CANbus thread is shown in Figure 80.
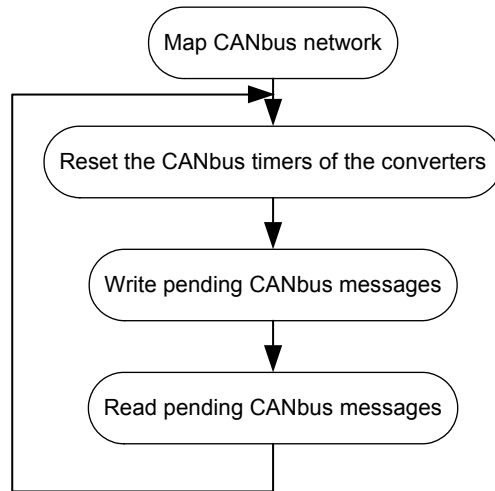
Figure 80: The Modbus/CANbus thread program flow diagram.

The DG gateway thread is shown in Figure 81.
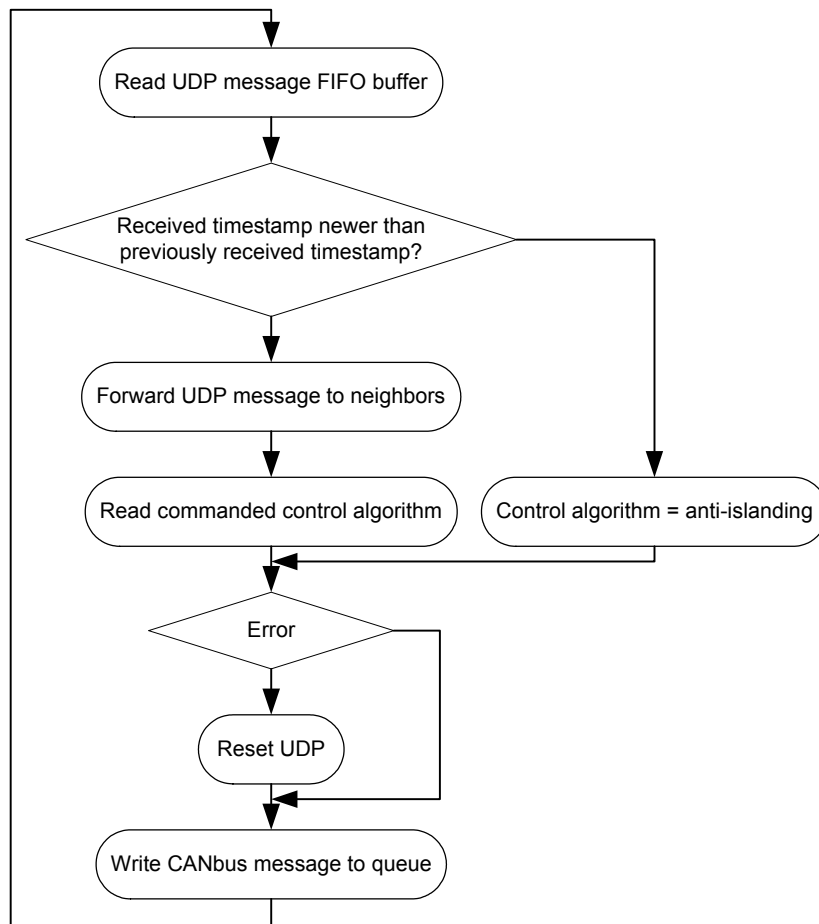
Figure 81: Program flow diagram of the DG gateway thread.

6.5.2 Grid management software

The testbench connected computer has a process simulating the network owner in respect to islanding testing. It sends the periodical heartbeat messages needed for the DG to stay in voltage support algorithm. At the same moment as the testbench opens the grid electromechanical contactor, the sending of these heartbeat messages is also stopped. This gives a test for checking if the direct communication is fast enough. It does not test flooding, and there is reason to believe that flooding would add time to communication timeout detection. How much depends on implementation, distance, network layout, and loading of the communication network. Most of these factors were outside the control of the author. The only laboratory experiments done, verified the functionality. A screenshot of the grid management user interface is shown in Figure 82.
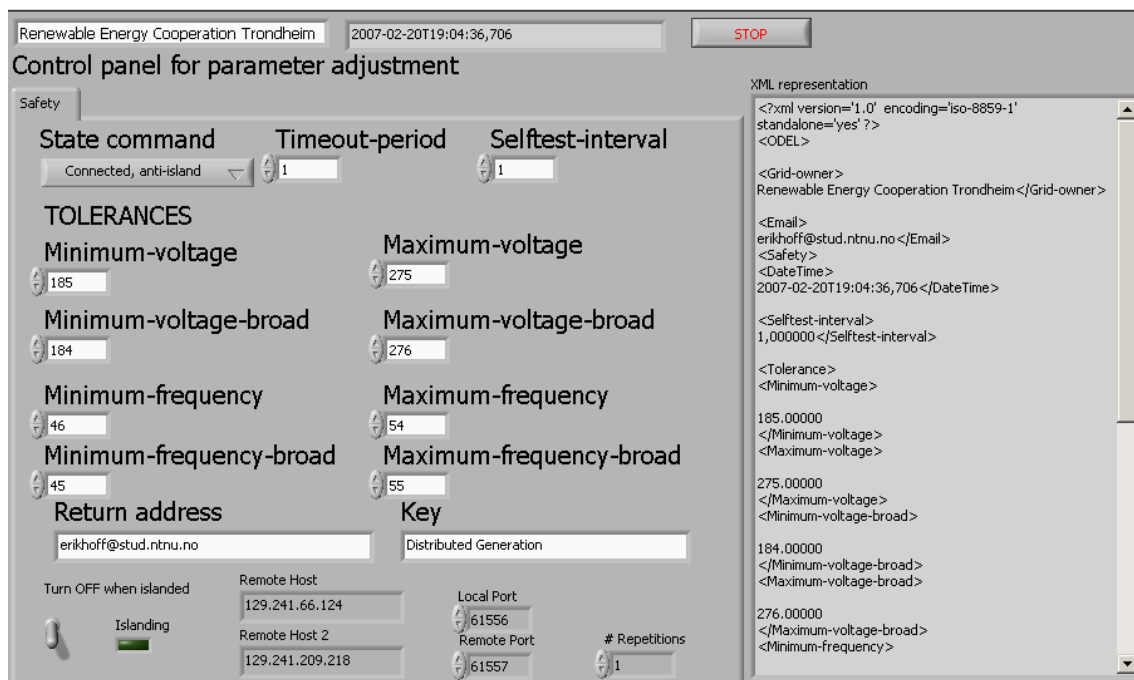
Figure 82: A screenshot of the grid management user interface.

The information including a timestamp is encapsulated in an XML-format. The grid management user interface formats these UDP messages to XML. This gives the possibility to set key parameters such as frequency and voltage tolerances in real-time. It was tested using various computers. It was in the final tests programmed in the testbench computer in order to synchronize measurements and the cease of UDP messages from the network owner. The information included in the XML-messages is show in Figure 83.

```
Network owner
Return email-address
Safety:
        Date and time (ms resolution)
        Selftest-interval
        Tolerance:   Minimum-voltage
                     Maximum-voltage
                     Minimum-voltage-broad
                     Maximum-voltage-broad
                     Minimum-frequency
                     Maximum-frequency
                     Minimum-frequency-broad
                     Maximum-frequency-broad
        Timeout (seconds)
        Key
        Control algorithm
```

Figure 83: The information encapsulated in the XML-format of the UDP-based protocol.

More information could be included, such as set-points. This was not necessary here. A general discussion about the XML format in power systems can be found in [61, 62].

6.6 Communication discussion

The communication system is divided in two communication buses; CANbus for local communication and UDP for wider areas. First the CANbus is discussed, and then the UDP communication is discussed. The section ends with a discussion about error tolerance.

6.6.1 CANbus communication

The CANbus protocol represents a multiple-access network. The bandwidth is limited to 1 Mbit/s or less depending on the acknowledge bit propagation delay. Due to its limited network size, the protocol can meet real-time requirements, under the presumption that all connected devices are designed in order to do so. CANbus is a data link and partially physical layer protocol. An application layer protocol should be build on top of these. A simple application protocol is the Modbus protocol [63]. The Modbus protocol maps the different parameters in a memory map, which can be either read or written. This map separates the main application software and communication. The Modbus is, however, a simple protocol and is not specified for CANbus hardware. An adaptation has therefore been built, hopefully without changing the basic ideas behind the Modbus protocol.

When designing this memory map it was attempted to include the network owner, the DG owner, and the maintainers assumed need for information. Reading and writing to locations in a defined memory map are supported by the Modbus protocol. Other functions such as logging two simultaneous measurements have been added. This could be beneficial for debugging purposes like finding the cause of oscillations. The memory map makes it easy to implement idempotent functions, which is resending to reduce the effect of transient communication errors.

6.6.2 UDP communication

The communication system is based on flooding as a method of forwarding messages. The scalability of this algorithm resides on proper termination of the flooding process. For the system currently presented, the forwarding tables are fixed, which gives a deterministic and possibly an optimal behaviour.

In practical systems, a large effort is required to build the forwarding tables manually. In case of changing network addresses, the effort is even larger. Therefore a more or less automatic method for adding DGs should be employed. The forwarding tables should be dependent on the location in the grid, and the type of DG. For example a biomass-fired DG can control the active power, which could come into use for the network owner. The control could be variable with the type of DG and the location in the network. Such automatically generated forwarding tables would benefit from the use of XML. It simplifies machine readability.

6.6.3 Error tolerance

The communication system presented represents a means of controlling many DG in a master-slave mode. Due to the use of a distributed communication network such as flooding and using resending of messages, it tolerates the loss of some messages without issuing a communication timeout. This is essential in error-prone communication networks.

Control of DG puts constraints on the communication timing. In order to control thousands of DGs simultaneously, the network owner does not need to know how many DGs have not received a specific message. Controlling the majority is more important for real-time control in this context. Explicit acknowledge is thus not necessary. Loss of communication can instead be detected at the receiving end using watchdog timers, as here.

The information offered to the network owner should be limited. A typical electrical grid error will be observed in many locations simultaneously. If all the DGs send an error message simultaneously, the network owner may be overloaded. Distributed algorithms could alleviate this overloading problem. Such algorithms could also offer

the possibility of explicit acknowledge. This could help the network owner to find which DGs are operational.

The distributed communication system based on an epidemic algorithm is vulnerable for non-benign errors, such as attacks. If one computer manages to mimic the network owner, it may gain control over DGs. Possible fixes to this risk may be authorization either by senders network ID, by the use of an authorization code or by ciphering of the entire message. Use of virtual private network (VPN) is another possibility. The use of cryptography was outside the scope of this thesis, as it was not necessary in order to demonstrate the interactions with the power electronic and control parts of the system. Possible attacks must be addressed in a commercial system.

In most distributed systems it is important to keep a consistent state throughout the system. In the system presented this is not necessary. Detection of master (network owner) failure may be false. This is because a DG cannot differentiate between a loss of communication and a master crash. This means that one DG may detect a communication timeout, and order anti-islanding control algorithm. The neighboring DG may not experience the same timeout and continue running in voltage support algorithm. This gives two paralleled inverters counteracting each others frequency-droop. It is important for the frequency tolerances to be tighter in the anti-islanding algorithm compared to the voltage support algorithm. This ensures the inverter in anti-islanding control algorithm disconnects itself before the inverter in voltage support algorithm disconnects. This error selectivity is important to build in due to the possibility of inconsistency in the distributed system state.

7   System simulations and measurements

The performance of the DG system can be characterized from a number of aspects. A key aspect is islanding situation transitions, under different control algorithms. When using the voltage support control algorithm, the inverter should maintain the island frequency and amplitude. However, with the anti-islanding control algorithm, the frequency should be forced out of normal operating tolerances. When the grid is not within tolerances, the system degrades to UPS control algorithm and standalone connection state. This ensures that local high-priority loads such as diode rectifiers are supplied. This chapter will first present the testbench developed. Then, it will present the measurements and simulations.

7.1   Grid connection testbench

In order to test the different anti-islanding algorithms a testbench was developed. The testbench is designed to document non-islanding PV inverter tests according to IEEE standards [11]. Using this testing equipment it is also possible to document grid currents and voltages. The testbench is based on a Labview PXI-chassis for control and measurements. A simplified electrical circuit scheme is shown in Figure 84.
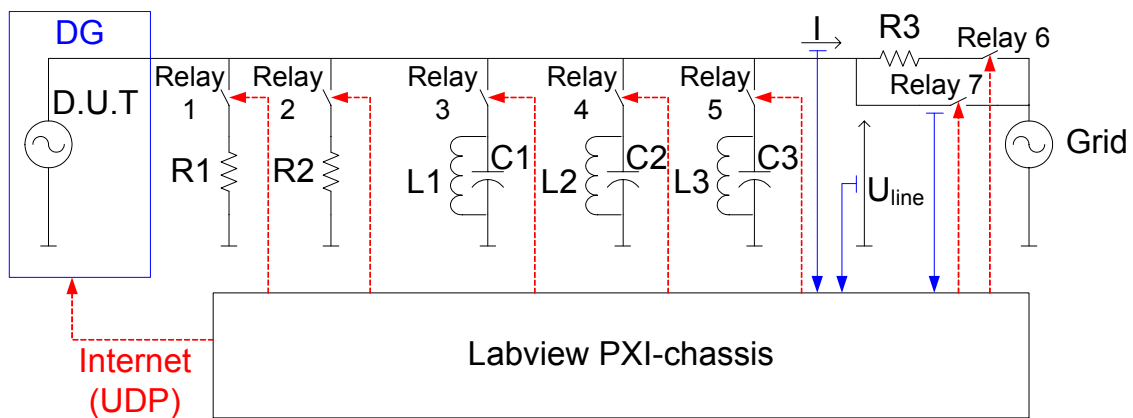
Figure 84: Power circuit of the testbench.

A photo of the testbench and the DG system is shown in Figure 85.
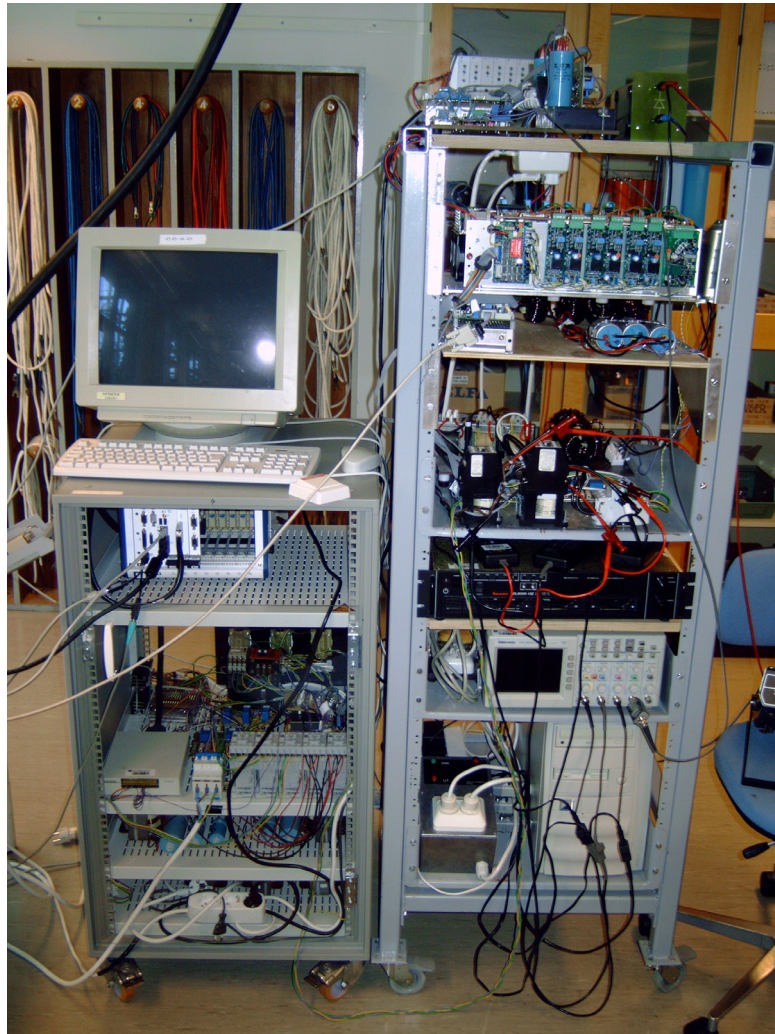
Figure 85: The test bench (left) and the DG setup (right).

The Labview system is a PXI chassis running Windows XP. The system measures power to the grid before grid disconnection, and logging the voltage and the frequency the first 2 seconds after grid disconnection. Additionally it displays current and voltage THD. It provides a user interface for connecting and disconnecting the different parts of the RLC load, in order to change operation conditions. The process for controlling the testbench is sequential. The program flow diagram is shown in Figure 86.
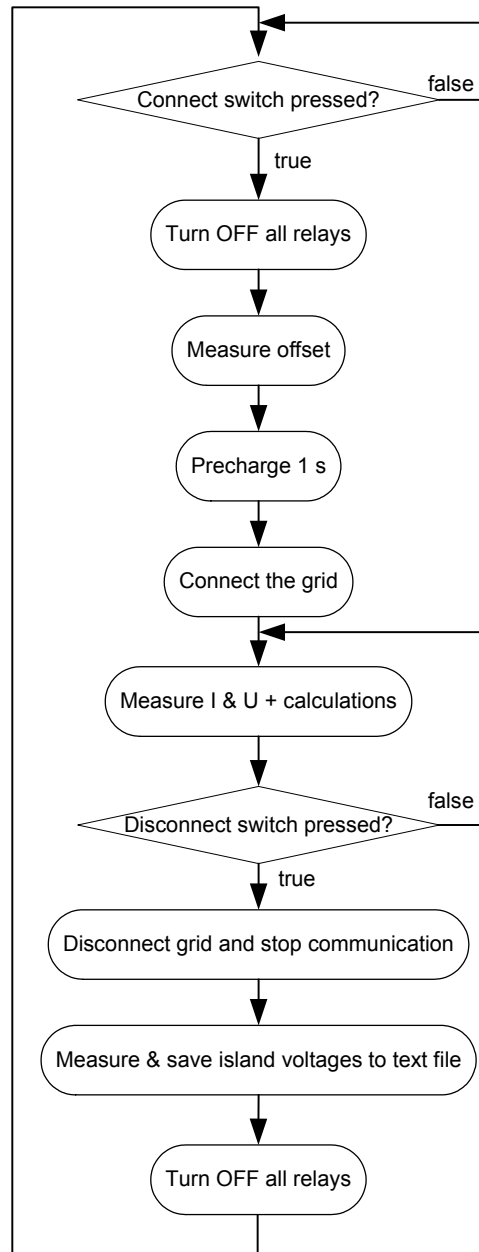
Figure 86: Program flow diagram for the testbench.

The testbench RLC-load is adjustable in steps by connecting different combinations of the components shown in Table 24.

Table 24: Testbench parameters.

Parameter	Value	Connection	Phase equivalent	Delta equivalent
R1	220 Ω	star	220 Ω	660 Ω
R2	110 Ω	star	110 Ω	330 Ω
R3	100 Ω	line	-	-
L1, L2 & L3	483 mH	delta	161 mH	483 mH
Loss per inductor	14.4 W	delta	1221 Ω	3663 Ω
C1	21 μF	delta	62 μF	21 μF
C2	20 μF	delta	60 μF	20 μF
C3	22 μF	delta	64 μF	22 μF

The thevenin equivalent of the testbench is close to a resistor. This means that the power sharing will be slightly different from grid-connected operation, assuming the grid impedance equals an inductance. Active power to the testbench is governed by voltage, while reactive power is mostly frequency dependent. The active power control is limited by the available power from the PV module. The available testbench loads are shown in Figure 87.
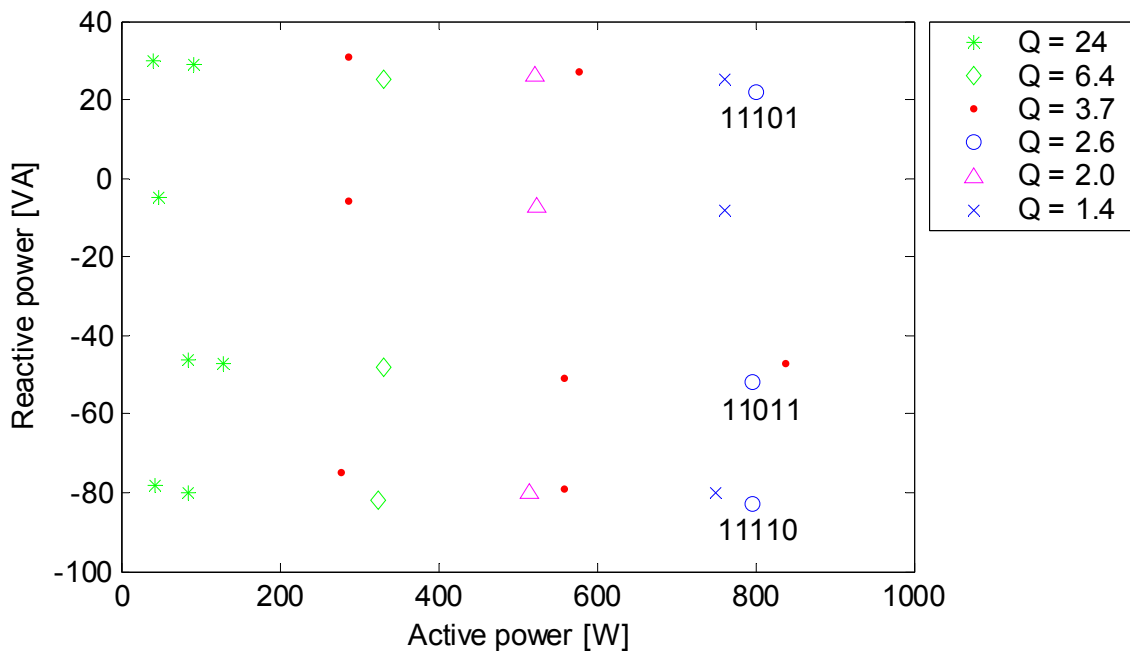
Figure 87: The available loads of the testbench with possibility of variable reactive power.

A quality factor Q below 2.5 means the loads are not relevant for IEEE 929-2000 [11]. The three marked points are the ones used for the testing presented here. The binary number specifies which components are connected. They must be read in connection with Table 25, where the components are specified.

Table 25: The RLC-load connected components specification for Figure 87.

4 (MSB)	3	2	1	0 (LSB)
R1	R2	LC (real)	LC (capacitive)	LC (inductive)

The Q-factor of the load can be calculated as shown in IEEE 929-2000 [11]:

$$Q = R\sqrt{\frac{C}{L}} \qquad (7.1)$$

The resonant frequency of the load was 50 Hz. It can be calculated using the following equation:

$$Q = \frac{1}{2\pi\sqrt{C \cdot L}} \qquad (7.2)$$

The power balance equation of the inverter and the testbench RLC load in islanding connection state can be described as

$$S_{inv} = S_{TB} + S_{Lf2} \qquad (7.3)$$

The right side of Equation (7.3) can be found by calculating the admittance of the testbench. The impedance of the testbench is first calculated:

$$\frac{U_g}{I_{in}} = Z_C(s) = \frac{sL}{s^2LC + s\dfrac{L}{R} + 1} \qquad (7.4)$$

Inserting $s = j\omega$ gives

$$\frac{U_g}{I_{in}} = Z_C(\omega) = \frac{\omega^2 L^2 R - jLR^2\omega\left(\omega^2 LC - 1\right)}{R^2\left(\omega^2 LC - 1\right)^2 + \omega^2 L^2} \qquad (7.5)$$

Inverting Equation (7.5) gives a simpler result, commonly used in anti-islanding analysis of current-controlled inverters:

$$\frac{I_{in}}{U_g} = \frac{1}{Z_C(\omega)} = \frac{1}{R} + j\frac{\omega^2 LC - 1}{\omega L} \qquad (7.6)$$

For the voltage-controlled inverter, the filter inductor must be included. The impedance of the circuit is then:

$$Z_U(\omega) = Z_C(\omega) + Z_{Lf2}(\omega)$$

$$= \frac{s^3 L_{f2} LC + s^2 \left(\dfrac{L_{f2} L}{R} + R_{Lf2} LC \right) + s \left(L_{f2} + L + R_{Lf2} \dfrac{L}{R} \right) + R_{Lf2}}{s^2 LC + s \dfrac{L}{R} + 1} \qquad (7.7)$$

The admittance is the inverted Equation (7.7):

$$\frac{1}{Z_U(\omega)} = \frac{\omega L^2 R - j\left[R^2 \left(LC\omega^2 - 1 \right)\left(LCL_{f2}\omega^2 - L - L_{f2} \right) + L^2 L_{f2}\omega^2 \right]}{\omega \left[R^2 \left(LCL_{f2}\omega^2 - L - L_{f2} \right)^2 + L^2 L_{f2}{}^2 \omega^2 \right]} \qquad (7.8)$$

Separating the real and imaginary parts gives

$$\frac{1}{Z_U(\omega)} = \frac{L^2 R}{R^2 \left(LCL_{f2}\omega^2 - L - L_{f2} \right)^2 + L^2 L_{f2}{}^2 \omega^2}$$

$$- \frac{j\left[R^2 \left(LC\omega^2 - 1 \right)\left(LCL_{f2}\omega^2 - L - L_{f2} \right) + L^2 L_{f2}\omega^2 \right]}{\omega \left[R^2 \left(LCL_{f2}\omega^2 - L - L_{f2} \right)^2 + L^2 L_{f2}{}^2 \omega^2 \right]} \qquad (7.9)$$

The testbench parameters used in Equation (7.9) are summarized in Table 26.

Table 26: Testbench parameters.

Parameter	Value (delta equivalent)
L	241 mH
C	63 μF
L_{f2}	1.3 mH
R_{f2}	0.31 Ω

For the parameters used in the laboratory setup the frequency and voltage dependence of the reactive power is shown in Figure 88.
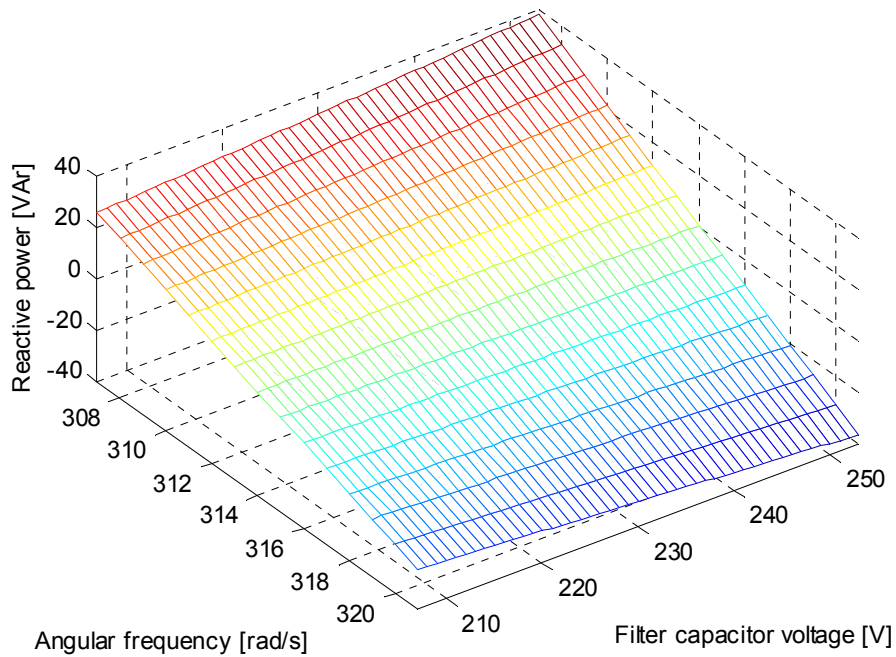
Figure 88: Reactive power consumed by the testbench as a function of angular frequency and voltage.

The active power dependence of frequency and voltage is shown in Figure 89.
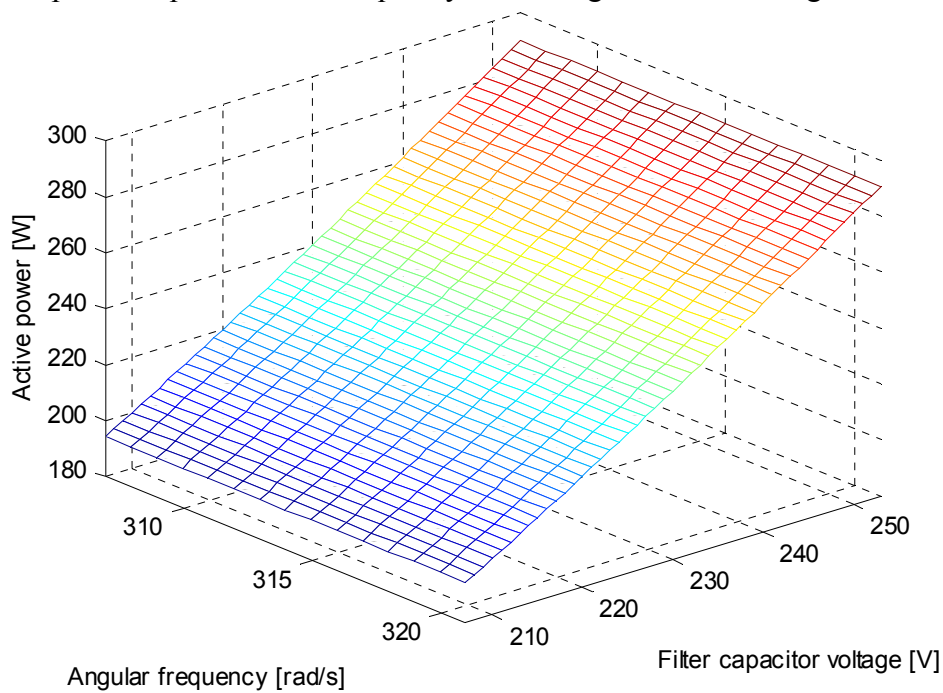
Figure 89: Testbench active power consumption as a function of angular frequency and voltage.

It can be seen from Figure 90 that the frequency of the load will not affect the active power actually consumed.
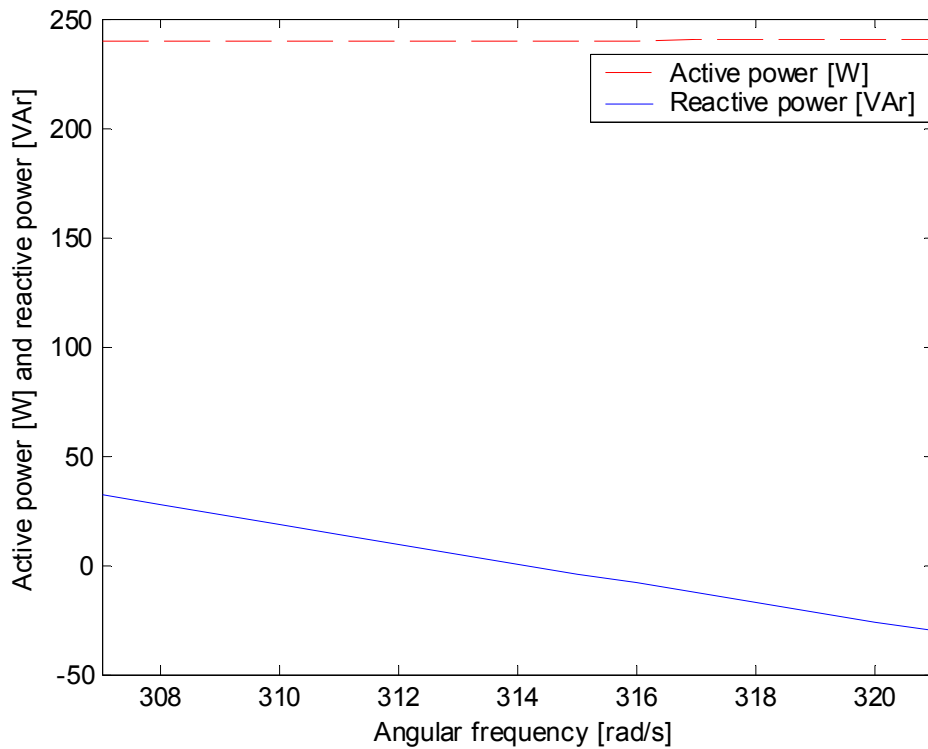
Figure 90: The power consumed by the testbench as a function of the frequency.

The frequency does not affect the testbench active power consumption, which is similar to that of a resistor. A negative droop will be able to stabilize the frequency. A positive droop will on the other hand destabilize the frequency, making it diverge away from a set-point. The power consumption as a function of voltage amplitude is shown in Figure 91.
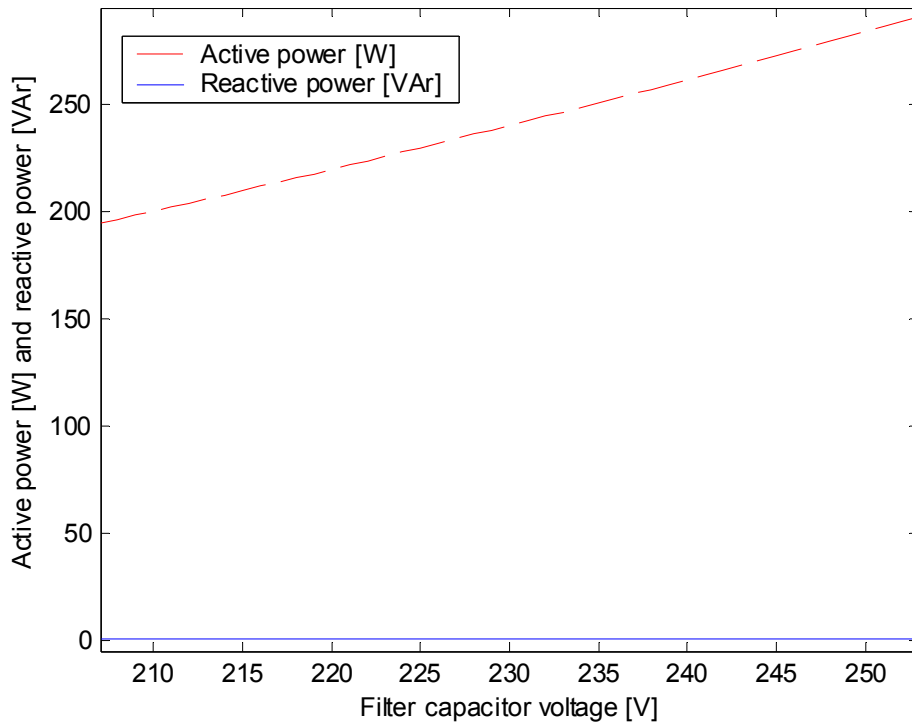
Figure 91: The power consumed by the testbench as a function of the filter capacitor voltage.

A negative reactive power droop responds to a voltage drop by increasing the applied voltage. This will stabilize the active power flow from the inverter to the testbench.

7.2 Voltage support algorithm tests

The voltage support algorithm is able to supply a variety of different loads. The power control is tested using the setup shown in Figure 92.
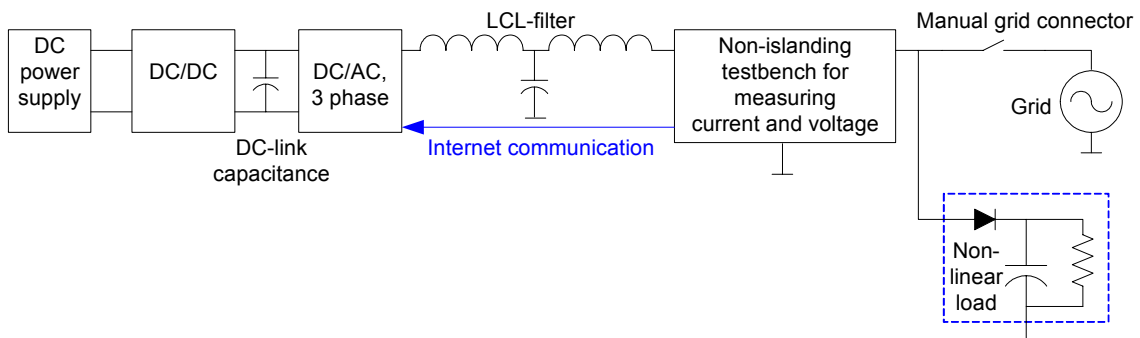
Figure 92: Setup for testing of voltage support algorithm under island connection state. The nonlinear load was only used in one test in islanding connection state shown in Figure 93.

Communication timeout is demonstrated through the transition from voltage support algorithm (2), via anti-islanding algorithm (3) and eventually UPS algorithm (4/5) with a load with a quality factor $Q = 2.6$. The testbench is used for measuring voltages during this transition.

The voltage support control algorithm can be active in grid connected or standalone connection state. The two connection states are not distinguishable by the inverter itself, except through communication. Internal variables of the inverter are shown for a diode rectifier load of 650 W under islanding situation in Figure 93.
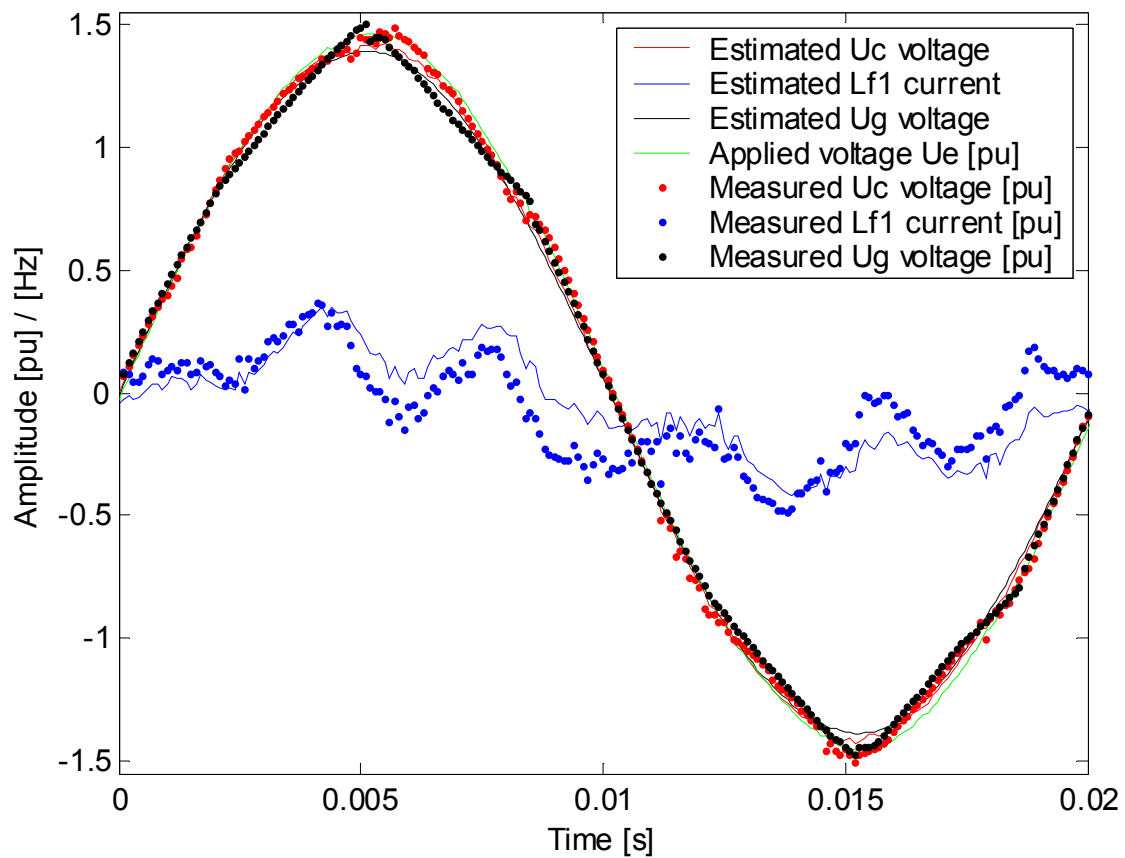
Figure 93: Inverter internal data for a diode rectifier load of 650 W.

The current waveform is highly distorted, as shown in Figure 8. Also the grid voltage is distorted, but little can be done with this when the LCL-filter with state feedback is already designed. A smaller L_{f2} could improve the grid voltage THD. The filter capacitor voltage should also be as sinusoidal as possible. The voltage feedback was chosen low due to noisy measurements. The voltage control in standalone connection state could have been better with a more accurate measurement.

The inverter should supply the load during a step change in load, or equivalently a grid disconnection event. The response to a grid disconnection is shown in Figure 94.
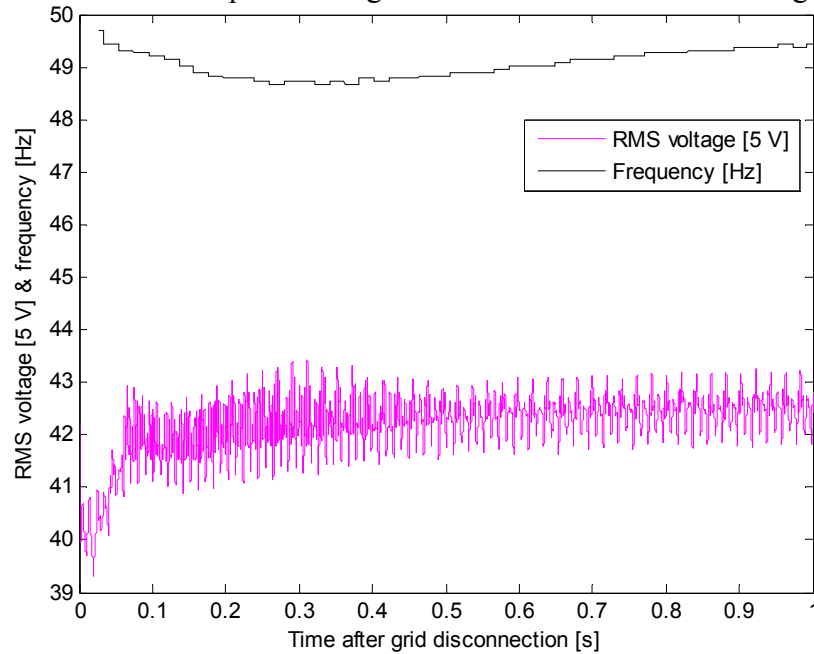
Figure 94: Transition from grid connected to standalone connection state at t = 0 in voltage support control algorithm. The power imbalance before grid disconnection was 816 W and 14 VA.

A simulation of similar conditions is shown in Figure 95.
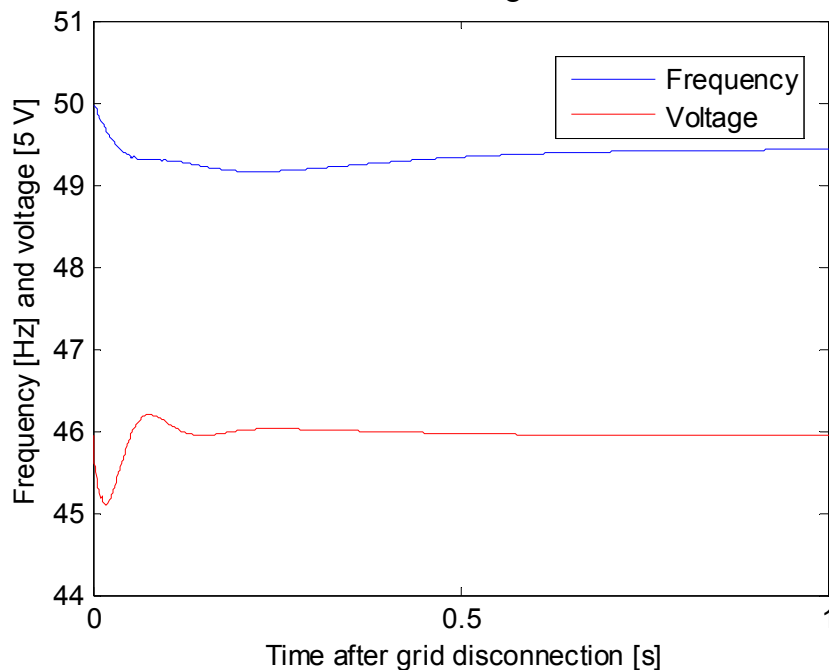
Figure 95: Simulated response of a grid disconnection event under voltage control algorithm. The power to the grid was -154 W and 351 VA.

The simulation and the measured waveforms show similar response. However, the voltage dip in the measurements is larger compared to the simulations. This indicates lower amplitude gain in the laboratory setup compared to simulations. Blanking time may have contributed to this. Also the lack of coupling between the axes in the simulation model may influence the accuracy of the simulation.

When using the voltage support algorithm the minimum and maximum frequency and voltage after a grid disconnection event are of interest. This has been investigated using multiple simulations with different frequency and voltage set-points. The simulation results are shown in Figure 96.
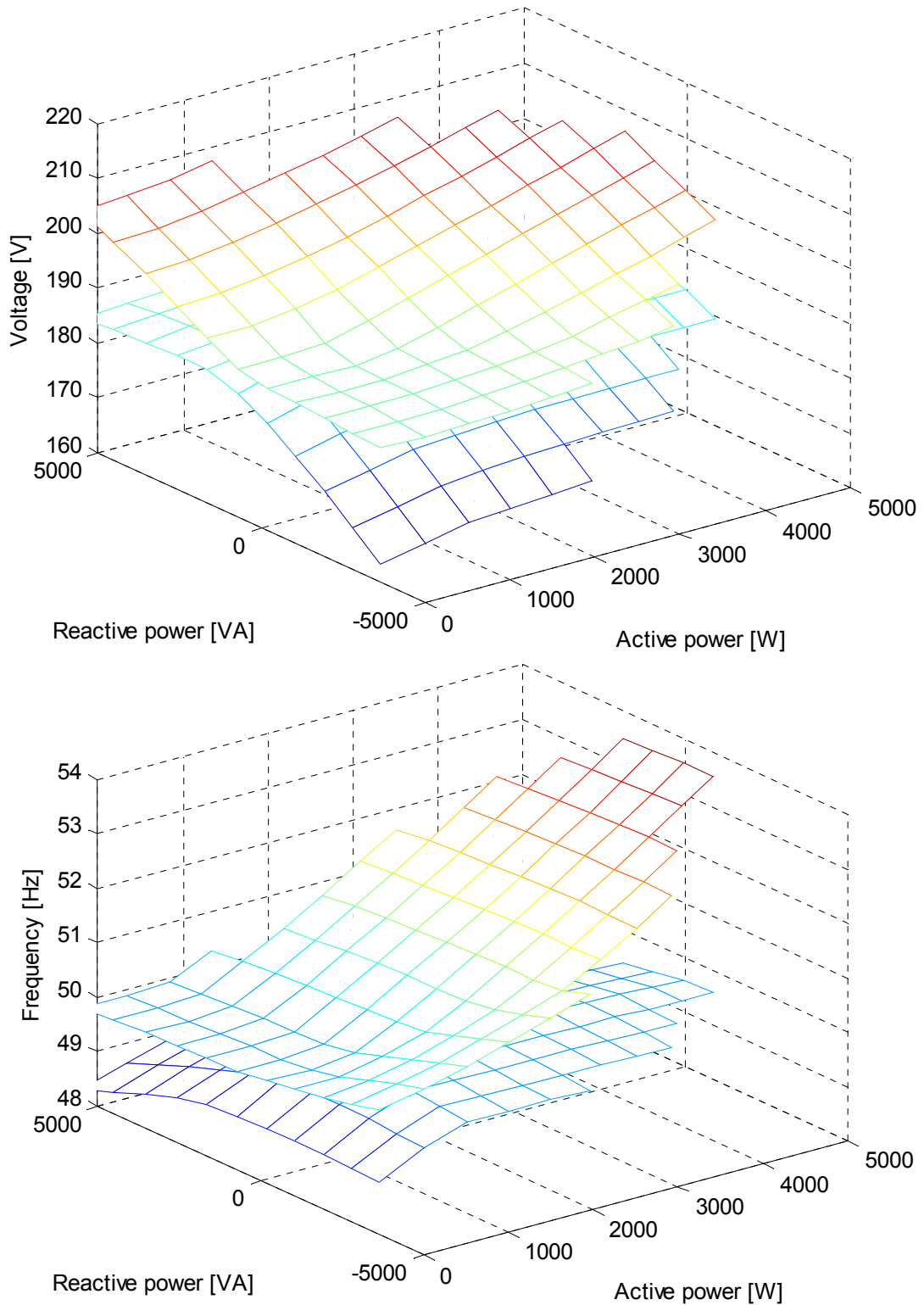
Figure 96: Minimum and maximum voltage and frequency during the transient after a grid disconnection event using the voltage support control algorithm.

Figure 96 shows that the transient voltage is large when there is a large reactive power imbalance. Correspondingly, the frequency transient is large when there is a large active power imbalance before grid disconnection. The large frequency transient in case of active power imbalance is connected to the DC-link available energy and the power controller. The derivative action of the active power controller is mainly causing this transient. This could be designed differently if, for example, a larger DC capacitance was present. The active power controller could then be slower, reducing the transients. This was not done, as the inverter capacitance was already chosen for the laboratory setup. Using the present laboratory setup, other power controller design methods could also have been applied, for example based on dynamic phasors as described by De Brabandere et al. [64].

7.3 Anti-islanding control algorithm tests

When the anti-islanding control algorithm is in steady-state, it is only operating in grid-connected connection state. Current THD is therefore measured. A diode rectifier load can be connected in order to increase the grid voltage THD. The test setup is shown in Figure 97.
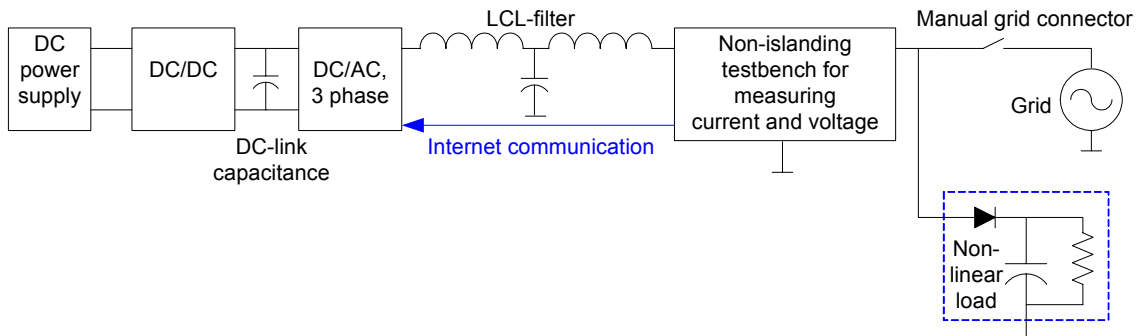
Figure 97: Setup for non-islanding tests. The nonlinear load was used to worsen the grid voltage THD under tests concerning grid current harmonics.

Measurements are done in order to verify the anti-islanding algorithm under different load conditions. Voltages and currents were measured using the testbench. For the anti-islanding control algorithm it is important to document the time to detect islanding connection state. The load quality factor Q was 2.6, and the testbench load was 800 W. This choice maximizes the active power consumed by the testbench. The reactive power is then adjustable in three steps, but only the load closest to unity power factor was used here. The test run with the longest time to islanding detection is shown in Figure 98.
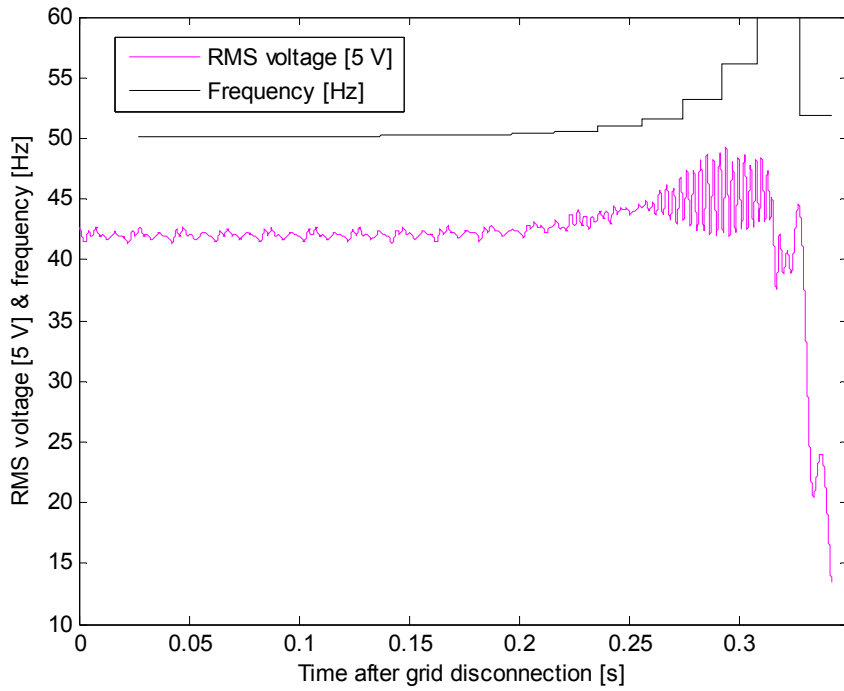
Figure 98: The test run with the longest time to islanding detection. The power imbalance before disconnection was 221 W and 96 VA.

The simulated longest time to islanding detection is shown in Figure 99.
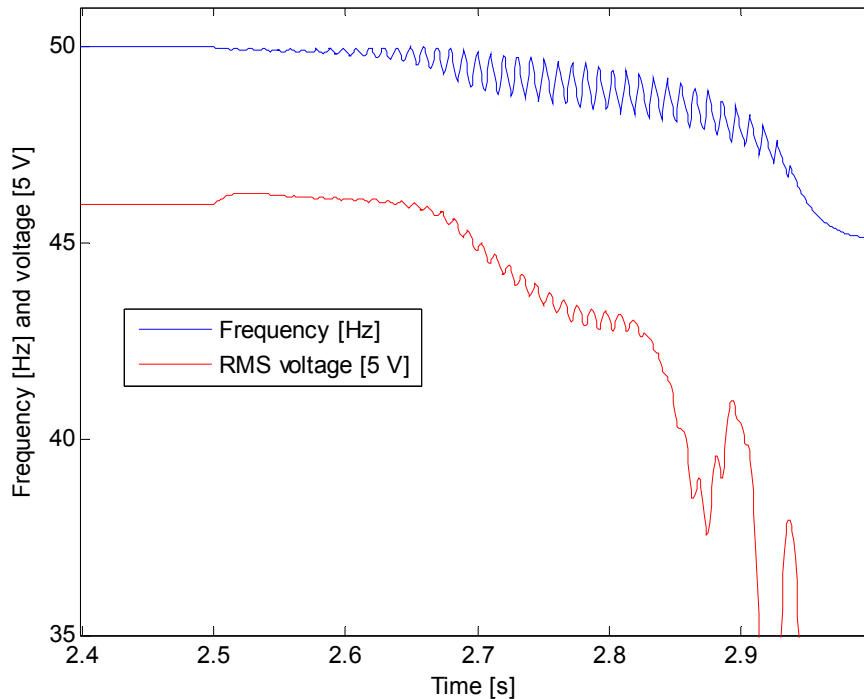
Figure 99: Simulated response to a grid disconnection when in anti-islanding control algorithm. The power from the inverter was 977 W and 329 VA just before disconnection.

It is observed that there are only small frequency changes just after grid disconnection. The frequency is however accelerating when perturbed. The islanding situation is detected here by over-frequency. The frequency limit is set at 46 Hz and 54 Hz, which is wider than what is expected in a practical situation. The tolerances are chosen so wide in order to illustrate the function of the anti-islanding algorithm clearly. The voltage tolerances were chosen equal to 185 V and 275 V. They were chosen so wide in order to clarify the anti-islanding algorithm by having long transients before the inverter disconnects. Measurements of the time needed to detect islanding are summarized for several test runs in Figure 100.
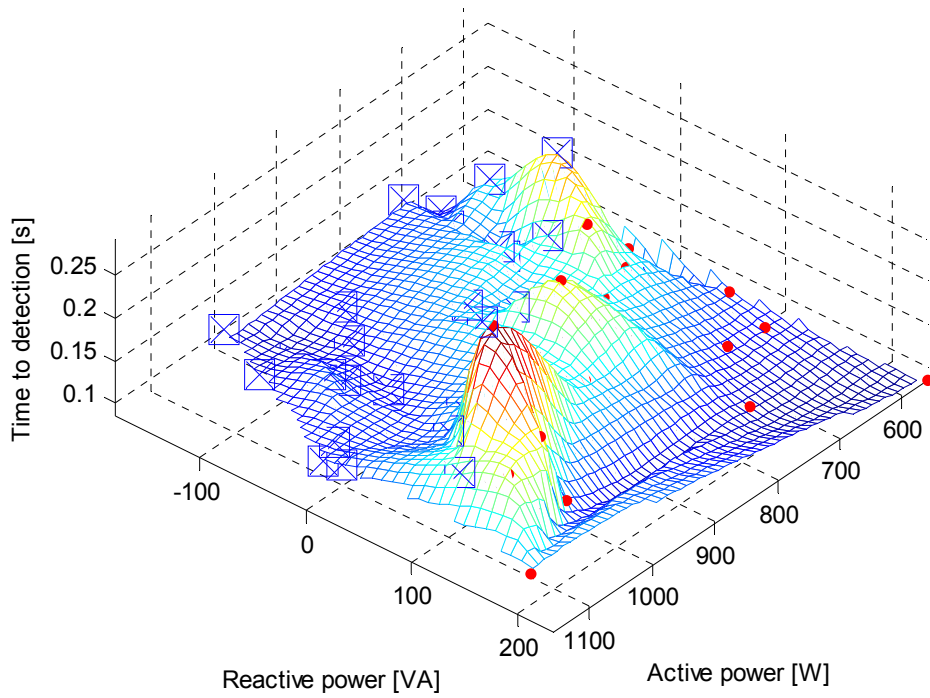
Figure 100: Time to detect an island using an LC-filter with close to 50 Hz resonant frequency. Red dots symbolize over-frequency, while blue crosses/squares are detected through under-frequency.

The simulated time to detect islanding is shown in Figure 101.
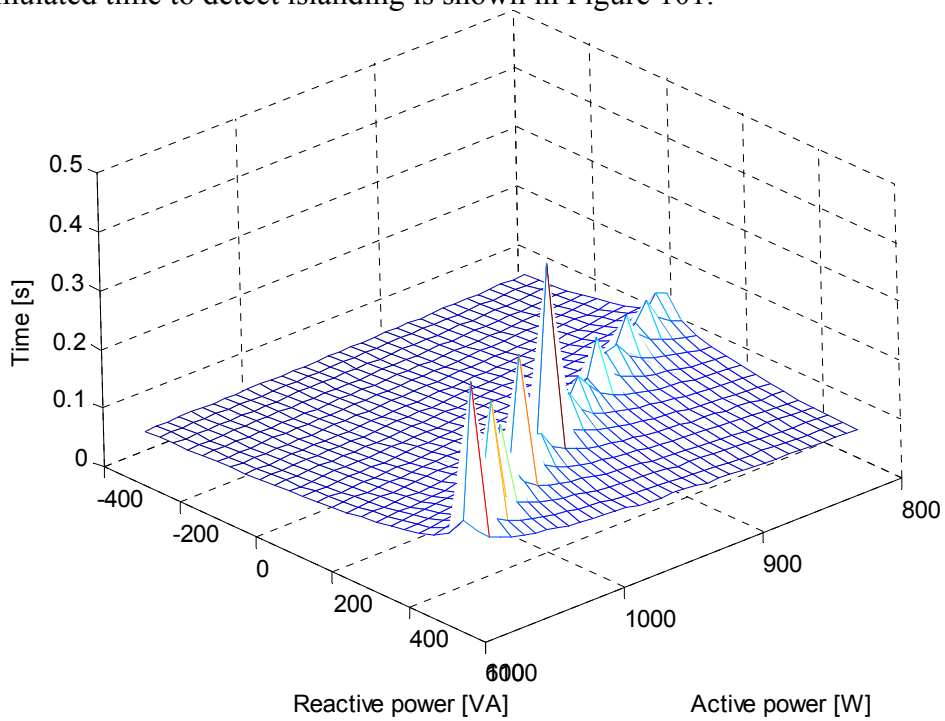
Figure 101: Simulations showing the time to detect an islanding situation when only the frequency is considered.

Figure 100 and Figure 101 show that the islanding situation is always detected. The maximum detection time is at the point where the inverter reactive and active power production is balanced with the power consumption of the testbench (RLC-load). The hill forming a line of longest time to detect an island is a function of active and reactive power. When the inverter tries to maintain non-zero reactive power to the testbench, it adjusts the amplitude of the filter capacitor voltage compared to the testbench. If the inverter produces reactive power, it increases the amplitude and decreases the phase in order to maintain the reactive power after grid disconnection. Due to the resistive characteristic of the testbench, the active power consumption thus increases. This explains the dependency between active and reactive power at the points where the maximum time to detect islanding is observed.

Due to the resistive part of the grid impedance assumed in the power controller, the inverter decreases its phase when commanding more reactive power to produce. This gives an effective decrease in the testbench frequency. The consumed reactive power decreases, thus a stable situation is reached. This is undesirable, but the positive feedback of the frequency assures any situation with a frequency different from 50 Hz is eventually detected.

The islanding situation can be detected from two starting situations: The first possibility already presented is when the inverter is in anti-islanding control algorithm when the grid is disconnected. The variables obtained from the DSP for this case are shown in Figure 102.
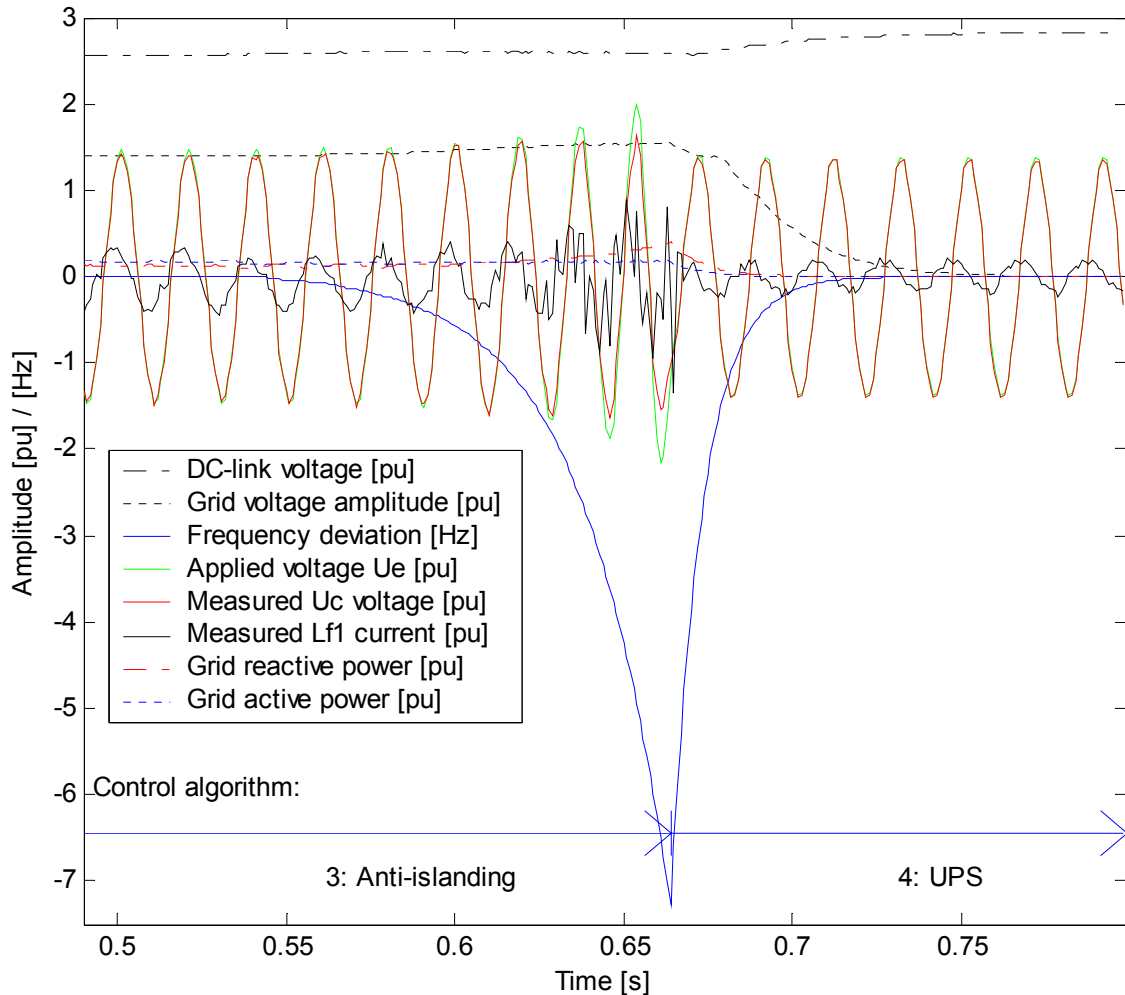
Figure 102: Islanding situation detection, without harmonic voltage compensation.

The other possibility is when the inverter is operating in voltage support control algorithm. The connection to the main grid can then be lost without the inverter noticing it. If a communication timeout then occurs, the inverter enters the anti-islanding control algorithm, in which islanding connection state is detected. A test run of this case is shown in Figure 103.
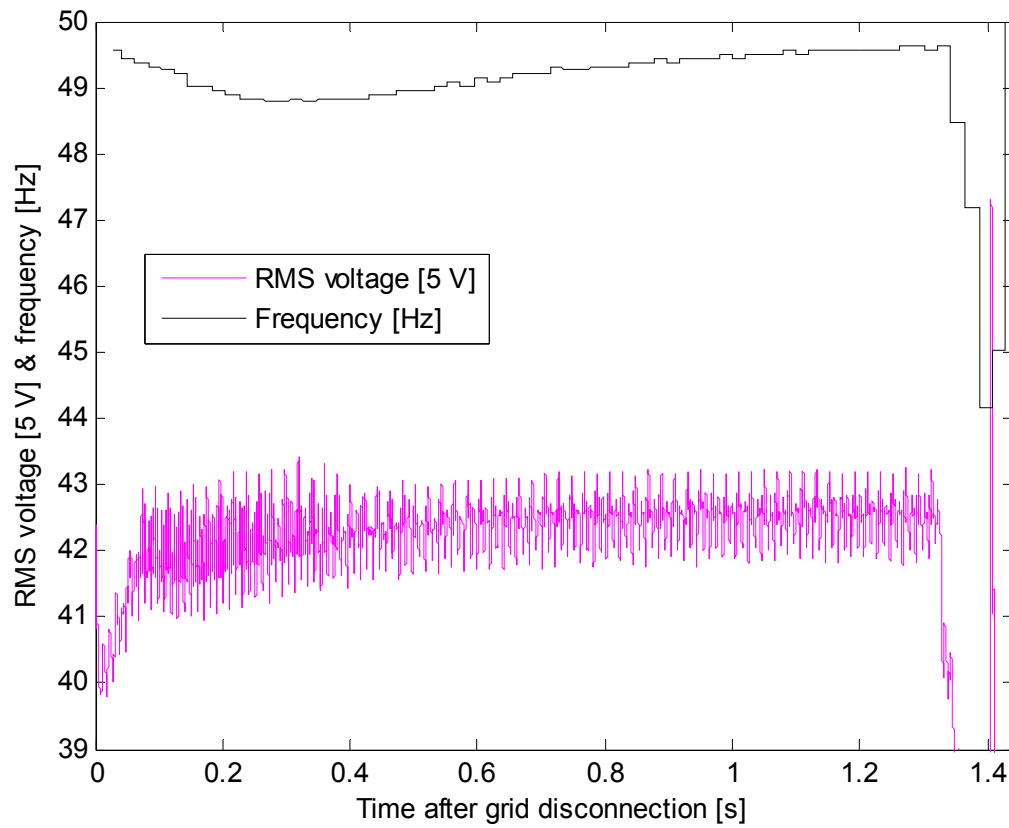
Figure 103: Voltage support algorithm (algorithm 2), until t = 1.3 s, when a communication timeout is detected, and the anti-islanding algorithm is entered. The power imbalance at grid disconnection at t = 0 was 763 W and 142 VA.

The inverter variables obtained from the DSP are shown in Figure 104.
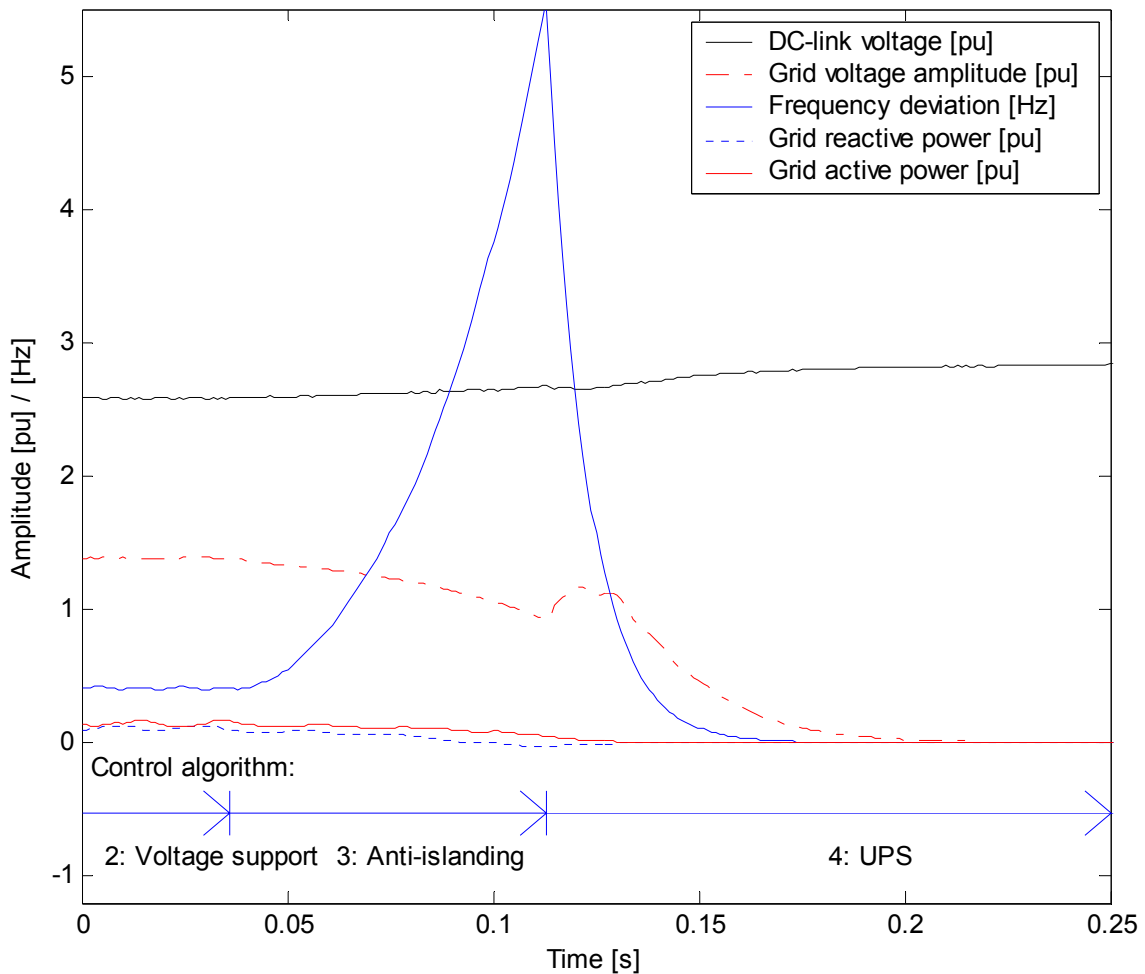
Figure 104: Inverter variables obtained from the DSP.

The effectiveness of the positive frequency feedback is clearly shown. This is also improved by the fact that the nominal frequency DC-link voltage set-point for the inverter changes from 340 V in anti-algorithm (3) to 349 V in voltage support algorithm (2). The primary purpose of this voltage set-point change is to reduce frequency deviations in the voltage support algorithm and islanding state.

7.4 Feed-forward for current THD reduction

When the grid is connected, in the anti-islanding control algorithm, the current THD should be reduced below 5 %. This is challenging for a voltage controlled inverter when the grid voltage is distorted. In order to worsen the THD, a 1.3 kW diode rectifier load was connected in parallel with the grid.

The voltage THD was measured together with the grid current THD. The sampling frequency is 40 kHz, limiting the bandwidth of the THD calculation. The frequencies of

interest are those below half the switching frequency of the inverter. The 40 kHz sampling is thus sufficient. The current THD with and without feed-forward compensation of harmonic voltages are compared in Table 27.

Table 27: Current THD with and without harmonic compensation based on eigenvectors.

	P [W]	Q [VA]	VTHD [%]	ITHD [%]	ITHD, 5th [%]	ITHD,7th [%]
With harmonic compensation	-519	5087	0.87	4.7	3.1	1.4
Without harmonic compensation	-707	5321	0.86	6.2	4.7	2.3

These results were continuously changing due to a changing grid voltage THD. It was, however, a clear benefit to use feed-forward when the inverter was consuming reactive power. Probably due to blanking time effects, the compensation did not show reliable improvement when the inverter was producing reactive power. The simulations presented in Chapter 5 give a better evaluation of the feed-forward.

Third harmonic voltage compensation was added, and a 2.4 kW single-phase diode rectifier was connected in parallel to the grid. Connected between two of the phases it represented an unbalanced nonlinear load. The third harmonic compensation benefit is shown in Table 28.

Table 28: Current THD with and without third harmonic compensation based on eigenvectors.

	P [W]	Q [VA]	VTHD [%]	ITHD [%]	ITHD 3rd [%]	ITHD, 5th [%]	ITHD,7th [%]
With third harmonic compensation	-454	4928	1.00	4.4	1.2	3.2	1.5
Without third harmonic compensation	-450	4891	0.94	4.7	1.6	3.1	1.4

There is a clear benefit in using third harmonic voltage compensation for harmonic voltages caused by an unbalanced nonlinear load. The measurements are, however, varying due to changes in the grid. Therefore there is an uncertainty connected to the benefit magnitude.

7.5 Transients during control algorithm changes

The transition from anti-islanding to UPS control algorithm must happen without the loss of power to the critical load. The transition from voltage support to the anti-islanding algorithm is typically caused by a communication timeout. Entering the anti-

islanding control algorithm eventually leads to the detection of a possible islanding connection state.

When islanded, the feed-forward gives a critical damped feedback system. Due to inaccuracies, it easily becomes unstable in reality. The feed-forward for current THD reduction then acts as a positive feedback mechanism during the grid isolated operation in the laboratory setup. This may reduce the time needed to detect islanding. The harmonic voltages, on the other hand, become unacceptably large. This makes it necessary to limit the maximum estimated voltage distortion used for feed-forward. Harmonic voltage limitation can be done by slowing down the observer, so that it is slower than the time to detect an island. Another option is to limit the maximum harmonic amplitude to compensate. The last option was chosen for the system. This is shown in Figure 105.
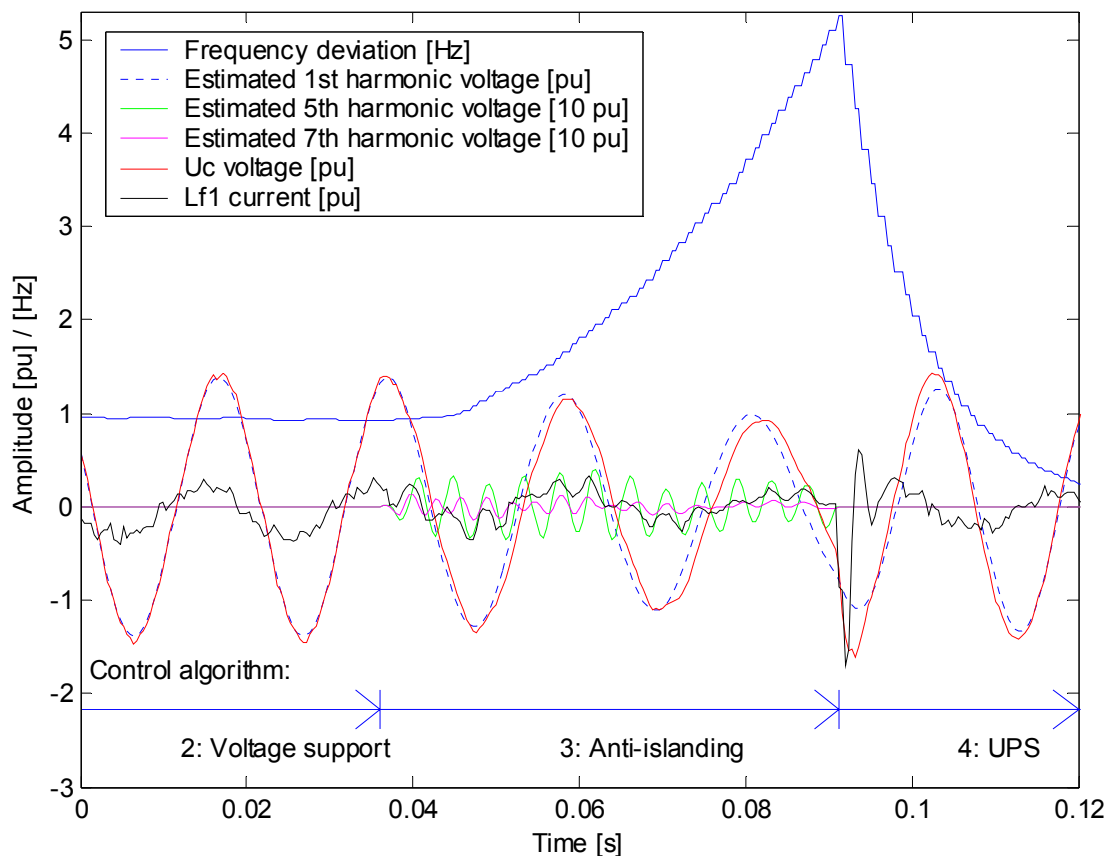
Figure 105: The inverter internal variables when the inverter is in voltage support algorithm, and enters anti-islanding algorithm (with feed-forward) after a communication timeout.

It is observed that the fifth harmonic is amplified, but the seventh harmonic is not causing any problems. The over-harmonic estimators must be limited in amplitude (5 % is used here). If not, they could rise to unacceptable levels during islanded grid operation. Feed-forward for over-harmonic voltage cancellation is in general not useful

in the islanding connection state. The non-islanding tests were run without over-harmonic voltage compensation in order to not disturb the frequency measurements.

8   Discussion of simulations and experiments

The results from simulations and measurements of the inverter control algorithms are now discussed. The inverter voltage controller, representing the fastest control loop is first considered. Then the power controller is discussed in Section 8.2.

8.1 Inverter voltage control discussion

The voltage controlled inverter supplies the critical load even in case of an open-circuit failure of the grid. This is valid when there is enough energy left on the DC-side, and the inverter over-current protection has not limited the output too much. This is different from a converter changing controller algorithm from say current-controlled to voltage-controlled when the grid fails. In this case a power loss easily occurs if the time to isolate the inverter from the grid is not known exactly. The main motivation for using voltage control in all control algorithms was the fact that the fastest control loop does not change. This simplifies the software. In voltage support algorithm, the connection state is unknown. It may be in islanding or grid connected connection state. In the first case the local network may consist of only a diode rectifier. Only a voltage controlled inverter can supply such a load, not a current controlled inverter. Voltage control is thus required in one of the two control algorithms that are normally grid connected.

In a situation where the grid fails to short circuit, a fast disconnection is very important to reduce the power loss to the critical load. For example a thyristor disconnects the grid in maximum 10 ms. This is less than 1/3 of the electromechanical contactor currently used. The added nonlinearity to the net grid impedance introduced by the thyristor could worsen the current THD but damp any LCL-filter oscillations. Short-circuit response was not included in the test setup because the nonlinearity of thyristors was expected to interfere with the harmonic voltage compensation.

The inverter is voltage controlled, but it also has current limitation in software. It shuts the inverter OFF in case a predefined current limit is exceeded, for the protection of the IGBTs. During normal operation the current limit is not exceeded. The sampling frequency is not fast enough for this current limitation to replace the IGBT gate driver level protection. The IGBTs used in the laboratory are oversized. Gate driver level current limitation therefore did not cause any practical problems by interfering with the discrete controllers. In an optimized inverter the current limit of the IGBTs is closer to the nominal grid-connected operating current. In that case a parallel current controller may be beneficial to avoid the driver-level over-current protection to be activated during normal operation. This depends on the ratio between intermediate current rating and continuous current rating of the inverter. In a practical design, it is expected that the maximum current should only be reached in standalone operation and under transient high loads such as starting an asynchronous motor or connecting a diode rectifier. Under such situations action should be taken in order to save the inverter. This can be either

reducing the current, or increasing it in order to blow a fuse. This has been studied by other researchers within the field of UPS, and good commercial solutions exist. It is thus not expected to give problems in an optimized design.

The ratio between maximum transistor current and average operating current is easier to optimize using current control instead of voltage control. When using voltage control, the current limitation should be well above normal operating current. The semiconductor device rating and core saturation of the LCL-filter inductors must be designed with this in mind. These components then become larger compared to a current controlled inverter. Methods to improve this ratio are welcome. For example a concurrent current controller, working as a current limiter, may be one solution.

There is 5 % virtual series resistance in the voltage controller. This represents 5 % current feedback, which helps stabilizing the feedback loop without affecting the output voltage significantly. In standalone connection state, it contributes to damp LCL-filter oscillations. In grid-connected connection state, it adds damping to the power control. Controlling the phase and amplitude of the filter capacitor voltages may seem a bit unpractical compared to directly controlling the grid current. Voltage control is believed to be better for the grid as it simulates a synchronous generator. Thus, it is possible to make such a system of grid-connected inverters voltage controlled. On the other hand a current-controlled inverter may be looked upon as a negative load. It is thus not contributing to adding damping to neither power nor harmonics in the grid in its basic form. If DG should be implemented so that it can dominate an electrical grid, the grid connection standards should to a greater extent look upon DG as generators. Today's grid connection standards specify current THD as if the DG was a load.

A voltage controlled inverter may have problems satisfying the grid current THD limits in practical grids is difficult due to the dominating third, fifth, seventh and higher harmonic voltages caused by for example diode rectifiers. Feed-forward can be used to reduce these harmonics in the grid current, by effectively setting the grid impedance to infinity for selected frequencies. However, the LCL-filter controller interferes with the feed-forward. The virtual resistance is therefore taken into account when calculating the feed-forward gain for the inverse transfer function method. For the eigenvector based method, the discrete state feedback is taken into account when calculating the feed-forward gain. This gives more accurate compensation of the LCL-filter feedback control. The blanking time is on the other hand not compensated for by the controller, and it is expected to interfere with the feed-forward. This interference is changing with the phase of the current. This may explain the different current THD and feed-forward effectiveness under reactive power production and reactive power consumption. Compensation of the blanking time was outside the scope of this work.

Under infinite grid impedance situation, the harmonic compensation is critically stable. In practical applications, however, inaccuracies may make it unstable. This was observed for the fifth harmonic. The feed-forward is only applied in anti-islanding

control algorithm. The islanding connection state is then transient. This transient (less than 0.5 seconds) is enough to excite the harmonic observers. The solution applied in the laboratory was to limit the estimated grid voltage harmonics to 5 % each, which is higher than the level expected in the electrical grid. This gives harmonic voltage compensation when grid-connected, and it does not cause excessive harmonic voltages in the anti-islanding control algorithm and islanding connection state.

8.1.1 Measurement noise

There was a high noise level of the measurements used by the LCL-filter state feedback. This was as expected due to known EMI problems with the inverter used. The use of an analog averaging filter did not reduce the noise problems. It was used despite the noise due to its accurate time delay and its lack of any phase shift effects. The controller structure should be as immune to noise as possible, and the high noise level gave a realistic test condition. The causes of the measurement errors were:

1. Common-mode noise due to a high primary to secondary capacitance of the 1 W DC/DC-converters supplying the galvanic isolation circuit high-voltage side. This connected the DSP +5 V power supply and the high-voltage side through the parasitic capacitance.
2. Interrupt timing errors due to the use of an old version of the debugging program DSPcomm (approximated to 1 %)
3. Generally high ADC-noise level, which is a known weakness of the DSP and the circuit board used.

In a future design of an integrating measurement and isolation circuit, it would be better to have a digital galvanic isolation. Such a solution could be based on a voltage to frequency converting circuit, or an ADC with a serial communication bus. An optocoupler could then represent the galvanic isolation. Such a solution could reduce the common-mode noise problems, compared to the solution used in the laboratory setup which has an analog galvanic isolation circuit.

Three phase measurements for each of the variables of the inverter controller were redundant. Only two phase measurements are sufficient. Due to the high noise ratio it was a benefit to do redundant measurements, as the noise was mostly common-mode, which is cancelled by the αβ-transform when measuring all three phases.

The system is observable by measuring fewer variables than actually done. The filter capacitor voltage measurement is not necessary for the system to be observable. This redundancy reduces the influence of the noise. It also gives better debugging capabilities. No attempts were done to reduce the number of measurements because this has been done previously by other researchers, for example Bolsens et al. [39].

8.1.2 State-space observer and state feedback

The high noise level of the measurements increases the difficulties concerning the inverter control. The state-space observer filtered this, reducing the problems. Its response could be chosen by the use of pole assignment. Having a higher bandwidth than the feedback control, it showed performance as expected, except the fact that no time delay compensation could be observed. The estimated variables tracked the measured variables as expected, but with no phase lead. The reason for this can be model errors.

The inductor L_{f1} was measured, all three phases independently. The common-mode inductance of 38 μH was included in this measurement, giving a sum of 833 μH. As the common-mode filter should not be accounted for, this gives a 4.77 % error and a phase lag in the current estimate. The controller should handle a 5 % modeling error. The state-space observer was held constant at 833 μH. The state-space observer was mainly used for damping the LCL-filter resonance. Due to the above-mentioned problems, the voltage controller had to be slowed down compared to the initial pole assignment, in order to handle full reactive power compensation used in the current THD tests.

The feed-forward of harmonic grid voltages had a positive effect on the grid current THD. For voltage controlled inverters in general a small voltage estimation error otherwise causes a large current error. The electrical grid voltage THD changes continuously. The tests concerning current THD are therefore noisy. Some test runs gave no THD improvement under reactive power production. The measurements indicate the usefulness of this method, but are too uncertain alone to draw a clear conclusion. The simulation results show more accurate results compared to the measurements due to the varying nature of the grid voltage distortion.

The feed-forward gain computed by eigenvector assignment proved to be better than the method based on inverse transfer function. This is due to the fact that the first is designed in the discrete time domain. It thus takes into account discretization errors of the controller to a higher degree than the inverse transfer function method does. For example, the inverse transfer function does not include the inductor L_{f2} current, which is used in the discrete feedback structure, but not in the equivalent circuit. L_{f2} current feedback is thus not compensated properly. Other researchers had more success with the inverse transfer function [39-40]. Placing the eigenvectors as orthogonally as possible makes the pole assignment robust against system perturbations. This is an additional benefit of the feed-forward method based on the "place.m"-function in Matlab used here for eigenvector assignment.

The grid observer is based on a discretized electric circuit diagram of a circuit which is uncontrollable. It is thus not affected by the inverter voltage as modeled. This is however only true in the case when the grid impedance is zero, which is never true in practice. The grid impedance is usually small compared to the LCL-filter. The applied

voltage influence on the measured grid voltage can thus be neglected regarding design of the discrete controller, considering grid connected connection state.

The fact that the grid is modeled as uncontrollable gives the possibility to use prediction in the feed-forward in order to cancel the time delay of the pulse-width modulator. This was used with success both in simulations and in the laboratory setup. The fifth harmonic is rotating in the opposite direction of the first harmonic, and the seventh harmonic rotates in the same direction as the first harmonic. This knowledge was used to find the correct timing of the feed-forward.

The grid voltage observer represents an oscillator, also called a generalized integrator because it has zero steady-state error at the center frequency. Similar oscillator structures are also used in current controllers. They are then called resonant controllers, and they are used to cancel specific frequencies from the current error signal. The difference of the harmonic voltage feed-forward chosen in this thesis and resonant controllers, is mainly the measured parameter. The first requires accurate voltage measurements (or estimations), while the latter requires accurate grid current measurements. Hybrid solutions could be made, such as voltage-controlled first harmonic and current-controlled over-harmonics. However it is simpler to apply the same design and analysis methods to the entire control system. The strength of resonant controllers in current control is assumed better immunity to blanking time effects compared to the feed-forward presented here. Resonant controllers require accurate current measurements, which were not accessible in the laboratory setup. The grid voltage measurement was most accurate, and the harmonic voltage compensation chosen was therefore expected to give best results.

8.2 Inverter power control discussion

The inverter power control controls the phase and the amplitude of the voltage fundamental frequency. The power control is different in voltage support and anti-islanding control algorithm. The anti-islanding algorithm is discussed first then followed by the voltage support algorithm.

8.2.1 Anti-islanding algorithm

Active anti-islanding algorithms are expected to perform better with a high noise level. This is because they need a small perturbation in order to drift in one or the other direction. A high noise level ensures this always happens no matter how well the load is balanced. It has been reported that some inverters using active anti-islanding algorithms fail to detect an island in a low-noise laboratory environment [15]. The non-islanding testing was done with a Q 4 % higher than specified in IEEE 929-2000 [11]. This would in general worsen the time to detect islanding. The maximum time to detect an islanding situation was higher in the simulations (451 ms) compared to the measurements (291

ms). This is as expected because the anti-islanding method applied is excited by noise if the load is balanced.

The line of maximum time to detect an islanding connection state is given by a set of active and reactive power. It is the result of the assumed grid impedance in the power controller. This line shows the same sign of direction in the measurements and the simulations. The direction is different, however. One of the explanations is blanking time. It represents a nonlinearity affecting the actual applied voltage. The power controller part affecting the applied voltage amplitude may therefore have a lower effective gain in the laboratory setup compared to the simulations.

How DGs will interfere with the electrical grid protection equipment is outside the scope of this work. Even so, a few brief aspects are worth pointing out. Especially the automatic reconnection which reconnects a faulted grid after 0.2-15 seconds is one of the functions that may be more difficult or take longer time in case of DGs running in the voltage support algorithm. Assume they can supply the island forming during the time before an automatic reconnection. A disconnection of the DGs will then first happen after a communication timeout has occurred. This timeout may be longer than the automatic reconnection time. Before a timeout and detection of an island, the island frequency may differ significantly from the main grid frequency. This makes the island potentially in opposite phase of the grid at the moment of reconnection. Checking phase and amplitude before reconnection may fix this problem. Using active anti-islanding methods implementing reactive power positive feedback instead of the positive frequency feedback may reduce the frequency deviations during islanding situation. The danger of reconnecting the grid in opposite phase then is reduced.

The island may supply current to the flame arc that the automatic reconnection tries to end. This requires a significant current which may be unrealistic but not impossible in case of power electronic converters. One solution to stop the flame arc may be to apply automatic reconnection not only to the feeder, but also to the DGs under this feeder. This guarantees no voltage to maintain a flame arc, and there is no risk of reconnection in opposite phase to the grid. The speed of the communication timeout is critical. This is manageable by having long enough reconnection time.

8.2.2 Testbench

The IEEE 929-2000 testing of three-phase systems may be easier than single-phase systems due to the fact that the different RLC-filters for the three phases have small parameter differences, resulting in different resonance frequencies. This may cause one phase to transfer energy to another phase. This may result in voltage imbalance, which can excite instabilities in the inverter controller. A faster detection of islanding for 3-phase inverters compared to single-phase inverters is the most likely result. The inverter voltage controller presented here was designed to keep the voltage balanced, regardless of the load. Imbalance is thus not important for the experiments done here.

The thevenin equivalent of the islanding test-bench is capacitive or resistive, depending on the selected load. This seems artificial due to the fact that the grid is mainly reactive. In many grids the load is also dominated by rotating machinery. This may slow down islanding detection time due to the inertia of the rotation. It may require too much energy to change the island frequency fast enough. A frequency increase in, for example, a motor driving a fan leads to increased power consumed by the load. This may balance the increased production of the DG, making an undesirably stable system. For high frequency gains, which is the case for the inverted droop used here, this is however not a problem because the gain is higher than realistic load line derivative of frequency.

An increase in active power may not always be possible, due to the fact that the MPP is tracked. Then, an increase in active power requires energy storage, which is present in the laboratory setup. Additionally the inverter current rating must not be exceeded. This would in most cases not cause a problem due to a higher intermediate rating compared to the nominal rating. An islanding situation should be detected in less than 2 seconds, which is much less than the time constant of typical heat sinks.

8.2.3 Voltage support algorithm

The voltage support is discussed by many researchers, for example [3, 5, 17, 47, 56, 64]. The voltage support algorithm presented here differs from other presented work by having a low frequency gain equivalent with a droop of 2 %. This was necessary in order to be stable when loaded with the test bench LCR-load. It is a target to have a high frequency gain, but it must also be stable. The magnitude of the droop gain commonly applied depends on parameters such as the grid size, load type, energy storage size, the frequency measurement accuracy and the controller structure and design. There is still room for optimizing the power controllers by using alternative controller structures and design methods.

The aim of this work was to outline what a DG may look in the future, given control using communication. This is a wide aim. Optimizing of the individual components was therefore not possible within the time limits.

9 Conclusion

The motivation of this work has been to get the most out of an inverter in a DG by the use of communication. Grid connection standards are discussed, but the work is not limited by them. Still, the safety aspects are maintained. The thesis tries to outline what a DG system may look in the future. A DG system consisting of a PV panel, a DC/DC-converter and an inverter were controlled using the Internet. Power electronic converters were built, and digital control and monitoring were applied. It is shown how the use of communication can improve the control possibilities.

The DC/DC-converter does not need real-time communication if voltage droop is used for output power control. It may, however, be practical to use communication for a few simple tasks such as set-point adjustments and turning the DC/DC-converter ON and OFF. Eventual paralleling of DC/DC-converters should be done on the DC-link side. If, on the other hand, several DC/DC-converters are paralleled on the PV panel side, communication is needed for MPPT.

The PV panel power is best controlled between MPP to open-circuit voltage. First, this gives the maximum DC/DC-converter current equal to I_{MPP} in Figure 23. This is less than the PV-panel short circuit current. Second, the required voltage control range is only a fraction of the PV panel voltage. This has been exploited when designing the DC/DC-converter, reducing the switching voltage or current of the transistors. Even though normally switching at a fraction of the voltage or current, full voltage should be used when selecting the transistor breakdown voltage. This is due to transients and unexpected situations. The efficiency of a DC/DC-converter with limited range voltage control can be significantly higher, and the size can be considerably smaller compared to a standard DC/DC-converter.

The inverter can be controlled in several ways, and three different control algorithms have been developed. All have different frequency control. Reactive power control and harmonics is also handled differently in the three control algorithms.

In islanding connection state the network owner can still maintain control of an island using communication. The grid may consist of several types of loads, such as diode rectifiers. Commonly used current controlled inverters cannot supply such loads. The inverter is therefore required to be voltage controlled. Applying the same voltage controller in all control algorithms simplifies the software design. It also avoids power interruptions during transitions between connection states.

For safety reasons, the inverter should terminate an island if the communication fails. If the grid is not islanded, the inverter should keep on feeding all available power to the grid, regardless of the communication status. Anti-islanding algorithms are commonly used for differentiating a stiff grid connection from an islanding connection state. An

anti-islanding algorithm for voltage controlled inverters has been tested. All previously published work concerning anti-islanding algorithms for inverters is based on current-control. The algorithm developed met the IEEE requirements of disconnecting an island within 2 seconds, including the communication timeout.

The main disadvantage of voltage controlled inverters is sensitivity to grid voltage pollution. Loads like diode rectifiers leads to superimposed harmonic voltages. Compensation methods based on feed-forward have been simulated and tested. The simulations show clear benefits of using a compensation method based on eigenvector assignment. The measurements show benefit, but to a smaller extent due to the presence of other disturbances such as noise and blanking time effects. This is believed to be more a result of uncontrollable factors in the laboratory setup than insufficiency of the compensation method used. The compensation should only be used when there is a grid connection. In an islanding connection state it represents a critically stable feedback loop which in practice may be unstable. Maximum estimated harmonic voltage had to be limited. This is necessary for limiting the harmonic content of the inverter voltage during the short time it takes to detect an islanding connection state.

When a grid error is detected such as islanding connection state, the inverter changes to standalone connection state and UPS control algorithm. It then supplies a local critical load. This may be a diode rectifier. The voltage controller ensures the voltage THD is kept low.

Internet communication was implemented to control the inverter. The DC/DC-converter, on the other hand, was implemented as a slave controlled through the DC-link voltage regarding power. In order to make the Internet communication system scaleable, the distributed communication algorithm flooding was used. This was demonstrated in the laboratory. However, it was beyond the scope of this thesis to measure response time and simulate such a distributed communication system. The basic functionality was implemented. Communication was used as a part of the laboratory testing of the inverter control. A search of the literature revealed that the use of the distributed communication algorithm flooding for islanding control as it is done here is not previously published.

10 Further work

The laboratory setup was designed to show some of the possibilities of using Internet communication for DG. The focus was not to optimize the single parts of the system. The DC/DC-converter design, the inverter integrating measurement card, and the Internet communication software all have room for improvements. Testing the communication system on a real DG would give more realistic test conditions, especially regarding interactions with automatic reconnect in the grid.

The inverter control was not tested during grid short-circuit failure. As this failure mode is most probable in practice, it is a natural test which should be a part of the qualification of a commercial product. How to react to a short-circuit situation would require a more robust current measurement circuit. A thyristor for isolating the grid and the inverter is beneficial in this situation.

In order to improve the transient voltage observed by the critical load, a separate inductor in parallel with L_{f2} would give non-zero grid impedance between the source (inverter) and the grid. The critical load would then be shielded from high-frequency disturbances.

The power controller can be redesigned. Increasing the energy storage would be beneficial. Using better controller design methods, for example based on dynamic phasors, could also improve the system. This could improve the performance measured in frequency and voltage deviations during connection state transitions.

The Internet communication could be implemented using a distributed acknowledge. This could give the network owner a better knowledge about the DG status. The Internet protocol would then not be limited to UDP, but TCP could also give satisfactory response time.

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Appendices

Appendix A: List of abbreviations

Appendix B: List of symbols

Appendix C: 3-phase transformations

Appendix D: List of publications

Appendix A: List of abbreviations

A	Ampere
AC	Alternating Current
ADC	Analog to Digital Converter
CANbus	Controller Area Network bus
DC	Direct Current
DG	Distributed Generation
CRC	Cyclic Redundancy Check
DSP	Digital Signal Processor
DT	Decision Table
DUT	Device Under Test
HMI	Human-Machine Interface
IGBT	Insulated Gate Bipolar Transistor
IP	Internet Protocol
LSB	Least Significant Bit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MSB	Most Significant Bit
ODEL	Object oriented Data model for ELectricity supply
PCC	Point of Common Coupling
PID	Proportional + Integration + Derivative type of controller
PLL	Phase Locked Loop
pu	Per-Unit
PV	Photo Voltaic
PWM	Pulse-Width Modulation
PXI	PCI (Peripheral Component Interconnect) eXtensions for Instrumentation
SCBC	Series-Connected Boost Converter
SFS	Sandia Frequency Shift
SMS	Slip Mode frequency Shift
SOA	Safe Operating Area
SVS	Sandia Voltage Shift
TCP	Transmission Control Protocol
THD	Total Harmonic Distortion
UDP	User Datagram Protocol
UPS	Uninterruptible Power Supply
V	Volts
VPN	Virtual Private Network
VSI	Voltage Source Inverter
XML	eXtensive Markup Language
ZND	Zone of No Detection

Appendix B: List of symbols

α	Stationary frame horizontal axis, parallel with the a-phase
A	State-space representation zero-input response matrix
β	Stationary frame vertical axis
B	Ideality factor of a pn-junction, or State-space representation zero-state response matrix.
C	Capacitor, or State-space representation measurement selection
C_f	Filter capacitor
C_{g50}	Virtual capacitor of a digitally implemented 50 Hz oscillator
C_{g250}	Virtual capacitor of a digitally implemented 250 Hz oscillator
C_{g350}	Virtual capacitor of a digitally implemented 350 Hz oscillator
δ	Phase angle
D_{MPPT}	Duty cycle resulting from MPPT associated input voltage controller
D_{Uin}	Duty cycle resulting from input voltage controller
D_{Uout}	Duty cycle resulting from output voltage controller
D_{PWM}	Duty cycle used to control the DC/DC-converter
dq0	Rotating frame coordinates, with zero component
E_G	Silicon band gap (1,1 [eV])
F	State-space representation observer zero-input response matrix
$f_{0,LCL,OC}$	Open-circuit resonance frequency of an LCL filter
$f_{0,LCL,OC}$	Short-circuit resonance frequency of an LCL filter
G	Observer estimation gain matrix

H_D Discrete observer zero-state response matrix

I   Current

I_{base} Per-unit scaling base current

I_d pn-junction current flowing in the conduction direction of the equivalent circuit diode of a PV cell (it is dominated by diffusion current).

I_{in} Input current

i_{Lf1} Current through inductor L_{f1}

i_{Lf2} Current through inductor L_{f2}

$\hat{i}_{g50}$ Estimated current through virtual inductor L_{g50} of a discrete 50 Hz oscillator.

$\hat{i}_{g250}$ Estimated current through virtual inductor L_{g50} of a discrete 250 Hz oscillator.

$\hat{i}_{g350}$ Estimated current through virtual inductor L_{g50} of a discrete 350 Hz oscillator.

I_{or} Saturation current

I_{out} Output current

I_{ph} Photovoltaic current

K   Bolzmanns constant $= 1.38 \cdot 10^{-23} \left[\dfrac{Joule}{{}^{\circ}K} \right]$, or
state feedback gain matrix

$K_{DC,i}$ DC-link controller integration gain

$K_{DC,d}$ DC-link controller derivative gain.

k_f Grid voltage estimation gain

k_i Inductor L_{f1} current estimation gain

K_{i1}	Discrete controller inductor i_{Lf1} current feedback gain
K_{i2}	Discrete controller inductor i_{Lf2} current feedback gain
$K_{P,p}$	Active power controller proportional gain
$K_{P,d}$	Active power controller derivative gain
$K_{Q,p}$	Reactive power controller proportional gain
$K_{Q,i}$	Reactive power integrating gain
K_u	Discrete controller filter capacitor C_f voltage feedback gain
$K_{v,u}$	Controller equivalent circuit filter capacitor C_f voltage feedback gain
k_l	Inductor L_{f2} current estimation gain
k_v	Filter capacitor C_f voltage estimation gain
K_u	Discrete controller filter capacitor C_f voltage feedback gain
L	Inductor
Λ	Closed-loop system eigenvalue diagonal matrix
L_{f1}	Filter inductor between the transistors and the filter capacitor
L_{f2}	Filter inductor between the filter capacitor and the grid
L_{g50}	Virtual inductor of a digitally implemented 50 Hz oscillator
L_{g250}	Virtual inductor of a digitally implemented 250 Hz oscillator
L_{g350}	Virtual inductor of a digitally implemented 350 Hz oscillator
L_{load}	Inductance connected to the load
η_{euro}	European weighted efficiency
O	Observability matrix
P	Active power

P_{nom} Nominal power

q_e Electron charge $= 1.602 \cdot 10^{-19} \left[coulomb \right]$

Q Reactive power, or
                     LCR-filter quality factor

R Resistance

$R_{v,n}$ Norton-equivalent frequency-selective virtual resistor

$R_{v,s}$ Controller equivalent circuit virtual series resistor

$R_{v,t}$ Thévenin-equivalent frequency-selective virtual resistor

$R_{v,p}$ Controller equivalent circuit virtual parallel resistor

R_{kf} Inverse grid voltage estimation gain k_f

R_{Lf1} Internal resistance of inductor L_{f1} (measured at 1 kHz)

R_{Lf2} Internal resistance of inductor L_{f2} (measured at 50 Hz)

R_p PV cell equivalent circuit shunt resistance caused by Si crystal defects.

R_s PV cell equivalent circuit series resistance caused by the resistance of
                     metal and silicon parts conducting the output current.

S Apparent power

S_{inv} Inverter apparent power

S_{Lf2} Inductor L_{f2} apparent power

S_{TB} Test bench apparent power

T Solar cell actual temperature

τ_{DC} Low-pass filter time constant for DC derivative controller

τ_{df} Low-pass filter time constant for frequency droop

τ_f Low-pass filter time constant for frequency measurement

τ_P	Low-pass filter time constant for active power controller
τ_Q	Low-pass filter time constant for reactive power controller
T_r	Reference temperature
T_s	Sampling and switching period
U	Voltage
u_a	Phase a voltage
$u_{\alpha\beta}$	A vector represented by stationary frame ($\alpha\beta$) voltages
u_{ab}	Line voltage from phase a to phase b
u_b	Phase b voltage
U_{base}	Per-unit scaling base voltage
u_{bc}	Line voltage from phase b to phase c
u_c	Phase c voltage
u_{ca}	Line voltage from phase c to phase a
u_C	Voltage over filter capacitor C_f
u_E	Inverter applied voltage, averaged over one switching period T_s
$u_{E,\alpha\beta}$	Inverter applied voltage vector, averaged over one switching period T_s
u_g	Grid voltage measured at PCC
$\hat{u}_{g50}$	Estimated grid voltage first harmonic
$\hat{u}_{g250}$	Estimated grid voltage fifth harmonic
$\hat{u}_{g350}$	Estimated grid voltage seventh harmonic
U_{MPP}	Maximum Power Point voltage

U_n	Nominal voltage
U_{OC}	Open-Circuit voltage
U_{out}	Output voltage
u_{phase}	A vector represented by phase voltages
u_{line}	A vector represented by line voltages
X	Imaginary part of impedance, or closed-loop system eigenvector matrix
Z	Impedance
Z_C	Testbench impedance assuming current-controlled inverter
Z_{base}	Per-unit scaling base impedance
$Z_{g,50}$	Impedance of a 50 Hz oscillator
$Z_{g,250}$	Impedance of a 250 Hz oscillator
$Z_{g,350}$	Impedance of a 350 Hz oscillator
Z_U	Testbench impedance assuming voltage-controlled inverter
ω	System angular frequency (314 rad/s)
ω_o	Resonance angular frequency

Appendix C: 3-phase transformations

In this work the stationary frame is applied instead of the rotating frame often used (dq0-coordinates). The stationary (αβ-coordinates) frame gives a sufficient model in the UPS/DG context. The rotation matrices used in order to transform the 3-phase parameters to the orthogonal axes (αβ-coordinates) are given in the following text.

Phase voltage is defined as the vector $\begin{bmatrix} u_a & u_b & u_c \end{bmatrix}^T$

The line voltage is defined as the vector $\begin{bmatrix} u_{bc} & u_{ca} & u_{ab} \end{bmatrix}^T$

The product of the rotation matrix $R_{phase \to line}$ and the phase voltage vector gives the line voltages.

$$\begin{bmatrix} u_{bc} \\ u_{ca} \\ u_{ab} \end{bmatrix} = R_{phase \to line} \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \Rightarrow R_{phase \to line} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \quad (A.1)$$

The stationary frame αβ-coordinates are fixed in orthogonal axis, where α is in phase with the a-phase. The rotation matrix $R_{phase \to \alpha\beta}$ is therefore given as:

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\dfrac{1}{2} & -\dfrac{1}{2} \\ 0 & \dfrac{\sqrt{3}}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \Rightarrow R_{phase \to \alpha\beta} = \begin{bmatrix} \dfrac{2}{3} & -\dfrac{1}{3} & -\dfrac{1}{3} \\ 0 & \dfrac{1}{\sqrt{3}} & -\dfrac{1}{\sqrt{3}} \end{bmatrix} \quad (A.2)$$

The inverse equation will then be:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\dfrac{1}{2} & \dfrac{\sqrt{3}}{2} \\ -\dfrac{1}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \Rightarrow R_{\alpha\beta \to phase} = \begin{bmatrix} 1 & 0 \\ -\dfrac{1}{2} & \dfrac{\sqrt{3}}{2} \\ -\dfrac{1}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \quad (A.3)$$

The voltages in this setup are measured as line voltages. It is therefore necessary to find the rotation matrix between line voltages and the stationary frame.

$$\begin{bmatrix} u_{bc} \\ u_{ca} \\ u_{ab} \end{bmatrix} = R_{phase \to line} \cdot R_{\alpha\beta \to phase} \cdot \begin{bmatrix} u_{\alpha} \\ u_{\beta} \end{bmatrix}$$

$$\Rightarrow R_{\alpha\beta \to line} = R_{phase \to line} \cdot R_{\alpha\beta \to phase} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ -\dfrac{1}{2} & \dfrac{\sqrt{3}}{2} \\ -\dfrac{1}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} = \begin{bmatrix} 0 & \sqrt{3} \\ -\dfrac{3}{2} & \dfrac{-\sqrt{3}}{2} \\ \dfrac{3}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \quad (A.4)$$

In order to go from line voltages to the stationary frame, the matrix $R_{\alpha\beta \to line}$ must be inverted. This can be done as follows:

$$u_{line} = R_{\alpha\beta \to line} \cdot u_{\alpha\beta}$$

$$\left(R_{\alpha\beta \to line} \right)^T u_{line} = \left(R_{\alpha\beta \to line} \right)^T R_{\alpha\beta \to line} \cdot u_{\alpha\beta}$$

$$\left\{ \left(R_{\alpha\beta \to line} \right)^T R_{\alpha\beta \to line} \right\}^{-1} \left(R_{\alpha\beta \to line} \right)^T u_{line}$$

$$= \left\{ \left(R_{\alpha\beta \to line} \right)^T R_{\alpha\beta \to line} \right\}^{-1} \left(R_{\alpha\beta \to line} \right)^T R_{\alpha\beta \to line} \cdot u_{\alpha\beta} \quad (A.5)$$

$$\left\{ \left(R_{\alpha\beta \to line} \right)^T R_{\alpha\beta \to line} \right\}^{-1} \left(R_{\alpha\beta \to line} \right)^T u_{line} = I \cdot u_{\alpha\beta}$$

$$u_{\alpha\beta} = \begin{bmatrix} 0 & -\dfrac{1}{3} & \dfrac{1}{3} \\ \dfrac{2}{3\sqrt{3}} & \dfrac{-1}{3\sqrt{3}} & \dfrac{-1}{3\sqrt{3}} \end{bmatrix} \cdot u_{line} \Rightarrow R_{line \to \alpha\beta} = \begin{bmatrix} 0 & -\dfrac{1}{3} & \dfrac{1}{3} \\ \dfrac{2}{3\sqrt{3}} & \dfrac{-1}{3\sqrt{3}} & \dfrac{-1}{3\sqrt{3}} \end{bmatrix}$$

These matrices are, however, only valid for the ideal case. In the setup, the measurement vector is instead defined as $\begin{bmatrix} u_{bc} & u_{ca} & u_{ab} \end{bmatrix}^T$

The rotation matrix

$$R_{ideal \to actual} = \begin{bmatrix} 0 & -1 & 0 \\ 0 & 0 & -1 \\ -1 & 0 & 0 \end{bmatrix} \quad (A.6)$$

can then be used to fit the actual measurements into the above mentioned ideal models:

$$u_{\alpha\beta,actual} = R_{line\to\alpha\beta} \cdot R_{actual\to ideal} = R_{line\to\alpha\beta} \cdot \left(R_{ideal\to actual} \right)^{-1}$$

$$= \begin{bmatrix} 0 & -\dfrac{1}{3} & \dfrac{1}{3} \\ \dfrac{2}{3\sqrt{3}} & \dfrac{-1}{3\sqrt{3}} & \dfrac{-1}{3\sqrt{3}} \end{bmatrix} \begin{bmatrix} 0 & -1 & 0 \\ 0 & 0 & -1 \\ -1 & 0 & 0 \end{bmatrix}^{-1} \cdot u_{line,actual} \qquad (A.7)$$

$$= \begin{bmatrix} \dfrac{1}{3} & -\dfrac{1}{3} & 0 \\ \dfrac{1}{3\sqrt{3}} & \dfrac{1}{3\sqrt{3}} & \dfrac{-2}{3\sqrt{3}} \end{bmatrix} \cdot u_{line,actual}$$

These rotation matrices are thus used to transform the 3-phase line voltages and 3-phase currents to the stationary frame orthogonal coordinates. Based on this stationary frame model, a state-space representation of the system can be developed.

Appendix D: List of publications

Paralleled Three-phase Inverters.
Hoff, Erik; Skjellnes, Tore; Norum, Lars E.
NORPIE 2004; 14.06.2004 - 16.06.2004.

> This paper was a simulation of inverter controllers, based on state feedback.

High Power Linear Electric Machine - made Possible by Gas Springs.
Hoff, Erik; Brennvall, J. E.; Nilssen, Robert; Norum, Lars E.
NORPIE 2004; 14.06.2004 - 16.06.2004.

> The author contributed to this paper by the power electronics, control and laboratory testing of a machine designed by Brennvall and Nilssen. The machine model developed for this paper is the origin of the grid voltage observer model.

Power Electronics Laboratory combined with Digital Regulators.
Hoff, Erik S.; Fuglseth, Thomas Pagaard; Kulka, Arkadiusz; Undeland, Tore M.
EPE 2005; 10.09.2005 - 15.09.2005.

DC-DC-converter for photovoltaic panel charge controller.
Hoff, Erik S.; Andreassen, Pål; Norum, Lars E.
NORPIE 2006; 12.06.2006 - 14.06.2006

> The limited range voltage control concept was here explored in the context of lead-acid battery charging, using a tapped-inductor buck converter.

Development of a computer controlled test bench for long- and short term assessment of power electronics for PV modules.
Midtgård, Ole-Morten; Andersson, Nico; Hoff, Erik S.; Norum, Lars E.; Undeland, Tore M.
PV-SEC 04.09.2006-08.09.2006, Dresden, Germany.

Inverter Control for Distributed Generation. Hoff, Erik S.; Norum, Lars E. IEEE conference proceedings 2006, Portoroz, Slovenia. ISBN 1424401216. 6 s.

Islanding for Distributed Generation. Hoff, Erik S.; Norum, Lars E. Proceedings of the Annual Conference of the IEEE Industrial Electronics Society 2006.

> The two last papers present the inverter control strategy used in this thesis. All the experimental work was done by the author.