Noise Tolerant Voltage-Controlled LC Oscillator Circuits for Deep Submicron VLSI System-on-a-Chip Radio Circuits

by

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Abstract

This thesis studies the problems with maintaining the spectral purity of fully integrated VCO circuits for radio frequency synthesizers in single-chip system designs. LC tank circuit oscillator circuits are shown to convert amplitude variation in the tank circuit voltage into frequency modulation, if voltage dependent capacitances are present in the tank circuit. Since the parasitic capacitances of the gain transistors and the capacitance of the varactor device in a VCO circuit are voltage dependent, any interfering signal, that is able to modulate the amplitude of the VCO tank circuit voltage waveform, is converted to FM sidebands in the output signal spectrum. It is also shown that the AM-FM conversion may be prohibited under some conditons.

A new method for simulating the steady-state voltage waveform of an LC tank circuit oscillator is presented. In this method, one complete oscillation cycle is simulated piecewise, employing the known solution of the damped harmonic motion equation. The voltage-dependent parameters of the equation are updated in the beginning of each segment. The steady state is found by matching the initial conditions and the final conditions of one complete oscillation cycle, using a numerical optimization algorithm. The method avoids finding the solution of the differential equation with variable coefficients.

For minimizing the sensitivity of integrated VCO circuits to the intra-chip noise sources, this work proposes minimizing the AM-FM conversion by designing the VCO in the way that the voltage dependent capacitances of the oscillator core circuit are made to cancel each other's effects on the oscillation frequency at some amplitude level. Experimental results demonstrate 15 dB suppression of the sidebands due to the modulated tail current noise in a negative-G_m spiral inductor PFET VCO circuit. The varactorless prototype circuit is implemented in a 0.35 μm CMOS technology. The measured tuning range of the 3 GHz back gate tuned VCO circuit is 10 %, and the current consumption of the core circuit is 2.5 mA. The phase noise level is -110 dBc at 500 kHz offset frequency.

The last part of this thesis discussses the problems with modeling and characterizing small MOS transistors, and presents characterization of 28 μm wide MOSFSET devices. A new method for extracting the drain and source electrode resistances from the measured Z_{22} response is presented. The response is measured at a constant and very low signal frequency, with $V_{ds} = 0\ V$ and with various gate-source bias voltage values. At low signal frequencies, the equivalent diagram of the MOSFET is dramatically simplified, since all parasitic capacitors of the device may be ignored. Consequently, the number of degrees of freedom in the curve fitting is reduced to only two.

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Contents

Chapter 1

Introduction

During the recent decades, commercially available digital MOSFET integrated circuits (ICs) have developed from relatively simple integrated logic and memory circuits to systems that include tens of millions of transistors on the same chip. Employing digital CMOS technologies, or slightly modified versions of them, complex analog and mixed mode circuits have also been developed. For these reasons, CMOS has been the preferred VLSI (Very Large Scale Integration) semiconductor technology for more than two decades, especially for applications where low power consumption and low production cost, rather than the operation speed, are the main concerns. Due to this wide industrial use, CMOS technologies have also developed in very fast pace, compared to the other mature and widely used IC technologies, like circuits based on NMOS, bipolar, or GaAs transistors.

In addition to increasing the packaging density and the speed of the transistors, and decreasing the power consumption of the chip, the recent trend of semiconductor technology development has been to integrate analog signal processing, radio frequency (RF) circuits, microelectromechanical systems (MEMS), electro-optical, chemical, and biological functions together with digital circuits on the same piece of silicon [1]. For this purpose, the semiconductor technology that is used must also meet the special needs that these other system parts have. Despite of some limitations, CMOS technologies seem to have the potential to play a significant role also with these System-on-a-Chip (SoC) applications, since the production cost in large volumes is lower than with the current date alternatives.

The practical problems and solutions of RF circuits design have traditionally been very different from the digital circuits design issues, since single-chip integration of systems, that employ wireless telecommunications, has not been feasible earlier. Dedicated RF engineers have designed the RF

parts of systems like the mobile telephone. They have had the freedom of using their own design tools and design methods, and employing IC processes that are particularly suitable for RF circuit design. Since the trend of development now is single-chip systems, the RF engineers must use the same semiconductor IC process with the digital circuits designers, which forces the RF designers to tolerate some compromises. In most SoC designs, the digital system parts will cover the majority of the functionality and chip area. Therefore, the transistor properties in most available SoC semiconductor processes are optimized for digital, rather than for RF circuits design. On the other hand, the needs of the digital circuit designers have made the parasitic capacitances and the conductor resistances to decrease, which helps the RF circuit designer's work. Since single-chip system RF designers must use the same IC process as all other designers in the same project, they must accept the limitations that this brings, and try to employ design tools and design methods that the other designer communities have developed.

The well-known limitations of deep-submicron CMOS technologies in RF applications are the low transconductance-per-milliampere of the transistors, the wide statistical spread of the transistor parameters, high level of $1/f$ noise, and lack of good quality passive components, especially inductors [20] [21]. Despite of these limitations, fully integrated CMOS frequency synthesizer circuits, low-noise amplifiers, mixers for wireless telecommunication applications, and complete radio circuits have been demonstrated at least up to 5 GHz carrier frequency [23]. Although other technologies with significantly better RF characteristics, like SiGe BiCMOS, and Silicon-on-Insulator (SoI) have appeared, CMOS probably will remain as a popular choice also in wireless SoC applications, as long as the cost of designing and producing the chip remains cheaper than with the other technlology alternatives.

This thesis studies the problems of integrating the voltage controlled oscillator (VCO) together with the other electronics in a single-chip system. Even though the prototype circuits were fabricated employing a CMOS technology, most of the presented ideas apply to other submicron VLSI technologies, as well. From the RF designers point of view, the VCO and the frequency divider present often the most challenging modules of the phase-locked-loop (PLL) frequency synthesizer. The power consumption of these two blocks limits the available operation time of a battery operated system, since they must be turned on whenever the radio is at least in the listening mode. Together with the VCO buffer amplifier, they are the only functional blocks of the PLL that are running at the full carrier frequency, which makes the circuit design difficult in terms of saving

power and covering the necessary operation frequency range. The other PLL blocks operate at much lower frequencies. Therefore, the design problems with them resemble the problems with designing the baseband analog circuits. Even though the linearity, parameter spread, and high $1/f$ noise level of the transistors are concerns also with these circuits, submicron VLSI technologies have been successfully used for constructing the analog baseband blocks many years before the problems with the fully integrated VCO circuits were solved.

1.1 Intra-chip Noise Coupling in Single Chip Systems

Although many journal papers and books have been published about fully integrated transceiver circuits, the sensitivity of the frequency synthesizer circuits to the intra-chip noise coupling in SoC applications is seldom analyzed in detail [31] [32]. Some works discuss briefly issues like frequency pulling due to the RF power amplifier signal coupling to the frequency synthesizer circuit, or the sensitivity of the circuits to the supply voltage variations. However, the discussion is usually limited to the unwanted signals originating from the other transceiver parts, like the frequency divider or the RF power amplifier. The relative sensitivies of the different parts of the frequency synthesizer circuits are seldom analyzed, the coupling mechanisms are usually not studied in detail, and very few ideas have been presented about reducing the sensitivity, especially against to the substrate noise. However, it is well known that the internal noise coupling is a serious concern in SoC applications, and that frequency synthesizer circuits are sensitive in piciking up noise [18] [48].

Problems with noise coupling between the different intra-chip system parts are getting worse as the transistor dimensions are scaled down and the system complexity is increasing [1] [2]. In a large digital single-chip system, the instantaneous switching current on the chip may be 1000 A. If only 0.1% of this current is injected to the substrate due to the impact ionization current of the NMOS transistors, 1 A of current is distributed to the substrate in some irregular pattern, causing substrate potential variations that are very difficult to predict. Since most of the large systems are programmable, a program update or reconfiguration of a programmable logic block may change this pattern in an unpredictable way, which makes it difficult to predict the worst case substrate noise level.

Even though many modern semiconductor VLSI processes that are intended for integration of such systems, provide various means for isolating circuits

from each other, the most efficient methods may not be available in the process that actually is used. It is also difficult to predict if the available means of isolation will provide sufficient isolation for such sensitive circuits as the VCO. Since the time-to-market is an important factor in developing products, this kind of uncertainties should be minimzied. If extra noise immunity may be achieved by a new circuit design method, it should be adopted, for minimizing the risks in the project and for making reuse of the design easier in the following projects.

The frequency spectrum of the substrate currents is getting wider and harder to predict, as the internal clocking frequencies of the digital circuits will approach the RF carrier frequency, and the software will control large parts of the hardware operations, turning on and shutting down large hardware modules in some unpredictable way, from the hardware designers point of view. The harmonic frequencies of the clock signals easily exceed the RF carrier frequency, and in some unfortunate cases, may match the resonance frequency of some tuned RF circuit. There are also signs that the globally asynchronous locally synchronous (GALS) logic design style will become popular, for alleviating the synchronization problems between the digital modules on the large system chip. This design style relies on local clock signal generation circuits that drive local syncrhonous digital modules. However, if several independent clock generators are running on the same chip at almost the same frequency, and these signals are coupled to the RF synthesizer circuit, the beat frequencies will certaily cause undesired side bands in the frequency synthesizer output spectrum. Even though the signal levels that are coupled from these clock generators to the frequency synthesizer VCO may be small, the resulting spur in the output specrum may still easily exceed the noise level originating from the internal noise sources of VCO gain stage transistors.

1.2 Research Problem

The research problem addressed in this work is to improve the spectral purity of the RF oscillator circuits in single-chip systems, when the other circuits of the system may disturb the oscillators. In the recent literature, the phase noise performance of the integrated VCO circuits has been a central topic of the discussion. However, little attention has been paid to reducing the sensitivity of the oscillators to the intra-chip interference sources. The phase noise spectra of the published fully integrated VCO circuits are measured under conditions where no noise signals in the bias voltage source or in the substrate are present. Usually, no information is

published about the sensitivity of the circuit to the modulation through the supply voltage line, bias sources, or through the substrate. The main goals of this work are to analyze the effects of the interfering signals on the LC tank oscillator output spectrum, and to find methods to reduce the level of undesired sidebands in RF frequency synthesizer circuits, due to the noise coupling to the oscillator circuit.

1.3 Main Contributions

The main contributions of this work are:

- A detailed analysis of the effects of voltage dependent capacitors in LC tank oscillator circuits. The new result of the analysis is that when two different voltage dependent capacitances are present, they can be made to cancel each other's effects on the oscillation period under some conditions. Moreover, it is shown that this effect may be used for suppressing the AM-FM conversion of the oscillator.

- A new method for simulating the steady state voltage waveform of an LC oscillator, when the capacitance and the gain in the circuit depend on the instantaneous signal voltage. The presented method models one complete period of the steady-state waveform in segments, using the local solution of the damped harmonic motion equation inside each segment. The boundry conditions for simulating one complete cycle are found by matching the boundry conditions in the beginning and in the end of the cycle, since the steady-state waveform is known to be periodic. The proposed simulation method avoids finding solutions of differential equations with variable coefficients.

- Use of piecewise sinusoidal waveforms for describing the LC oscillator steady-state voltage waveform, when the loss and the LC product does not remain constant across the steady-state oscillation cycle.

- The experimental work demonstrates that it is possible to design and construct a voltage-controlled LC oscillator circuit that is able to suppress the effects of modulation in the bias sources, without compromising the tuning range, phase noise performance, or the current consumption. The measurements show that the sensitivity of the oscillator to the modulation of the supply current is minimized in the operating point where the FM modulation index is zero. In addition, the measured phase noise level, current consumption, and tuning range are acceptable for existing applications, like Bluetooth.

- The discussion on MOSFET modeling shows that a recently published method for extracting the values of the drain and source electrode resistances is probably incorrect. This thesis presents a new and very simple method for extracting the values of these parameters from the measured Z_{22} response at a low and fixed signal frequency, with various gate-source bias voltages, and $V_{ds} = 0\ V$. In addition, a new method for extracting the substrate network element values is presented. The method takes into account the transconductance of the transistor, when the device is operating in a region where the transconductance is high. The parameter extraction experiment using 28 μm wide MOS transistors produces results that match closely with the expected values for the electrode resistances and transistor parasitic capacitances.

Other significant contributions and new ideas presented in this work are:

- Improving the Q value of the VCO gain transistor drain-bulk capacitors by interleaving the drain fingers of the gain transistor pair. This layout technique creates virtual ground planes very close to the drain finger edges, which will minimize the path of the RF current in the lossy substrate material.

- Using only PMOS transistors in the gain stage of a back gate tuned VCO circuit, in order to maximize the frequency tuning range, and simultaneously to isolate the gain transistors from the substrate in an n-well CMOS process.

- The reciprocal property of the MOSFET, under some bias conditions, is employed for improving the accuracy of the parameters extraction, and for checking the accuracy of the measurement system.

1.4 Thesis Outline

The text is organized in the following way: Chapter 1 introduces the background, motivation, goal, and the contributions of this work. Chapter 2 reviews some central properties of the present-date technology alternatives for SoC designs, and presents some arguments for choosing a technology for designing single-chip systems where an integrated radio interference is desired. Chapter 3 describes some known intra-chip interference coupling mechanisms. This review does not try to list every potential interference

coupling mechanism in single-chip system designs. The purpose of the discussion is to provide the reader the necessary background for understanding the discussion in the later chapeters, and to show that the interference coupling mechanisms need to be carefully analyzed, since the interference coupling problems are different in every design. Chapter 4 discribes how negative-G_m oscillator circuits may pick up disturbing signals and convert them to undesired sidebands in the output signal spectrum. This discussion is based on the classical analog modulation theory. Chapter 5 and Appendix A introduce the the harmonic motion equation. The solution of this equation is then used in the development of the proposed method for finding the steady-state voltage waveform of an LC oscillator in the presence of voltage-dependent capacitances and voltage-dependent gain. Appendix B lists a program example that demonstrates the method. Chapter 6 and Appendix C study the effects of voltage dependent capacitances in the tank circuit. The important new result of this discussion is that if two different types of voltage dependent capacitances are present, it is in some cases possible to find a condition where their effects on the oscillation period cancel out. Chapter 7 presents an experimental oscillator circuit, where the sensitivity of the circuit to the bias current modulation is shown to depend on the bias conditions. It is also shown that in the bias point where the FM modulation index of the oscillator is zero, the sidebands due to the bias supply modulation are suppressed. Chapter 8 presents the MOSFET modeling and parameter extraction method that was developed in the course of this work. This chapter includes a through discussion about the problems in characterizing the RF properties of small MOSFET devices, and presents a new method for extracting the drain and source electrode resistances. The method for extracting the substrate network elements is also new, and it takes into account the transconductance of the transistor when it is operating in a region where the transconductance is high. The results of this device modeling work are not directly used in the discussions on the oscillator circuits. Finally, Chapter 9 presents the conclusions.

Chapter 2

VLSI Processes for SoC Applications

Since the complexity of single-chip systems is increasing in fast pace while the number of engineers working in one project cannot increase much, the future electronics designers must become more productive. Even though the RF parts of the transceiver are not necessarily getting more complex if they are put on the same chip with other circuits, the design work is getting more challenging because of the less-than ideal devices and intra-chip noise coupling problems. In some cases, like single-chip systems that employ multi-band soft radio interface, the work of the RF designers is also getting more difficult because of the demand for increased functionality.

A typical Application Specific Integrated Circuit (ASIC) design group in a company that is dependent on the foundry services that other technology companies sell, has to consider several technical and non-technical issues when choosing the work-horse technology that it will use for most of the design projects. It is usually desireable to pick one technology that is suitable for most projects, in order to gather design experience over a longer time and to develop in-house solutions to frequently appearing design problems. When this technology is not suitable for the design task, it is possible to choose another for one project. However, in this case it is difficult to develop circuits that might fail at the first try. Unfortunately, designing RF circuits often includes this type of risk, since it is for example difficult to simulate the Q value of the passive components or the true level of noise coupling between the circuits. The discussion in the following sections reviews some central properties of the most promising technology alternatives that are suitable for SoC designs with a radio interface.

Many foundries have a selection of process modules that support RF designs, for example a thick top metal layer for spiral inductor designs, and high voltage transistors that help RF power amplifier designs. However, these process modules will probably remain expensive alternatives as long as only some foundry customers use them. Therefore, it is better to design the RF circuits without using these process modules whenever it is possible. To help further the design of the RF parts of single-chip systems, some foundries provide design kits with some characterized RF devices, like spiral inductors.

The traditional problems in using the main stream VLSI processes with RF designs have been the lack of high quality passive components, poor transistor performance in RF circuits, large statistical variation of some important transistor parameters, lack of some process parameters data for simulation models, large parasitic capacitances and resistances, and, especially if high conductivity substrates are used, high RF loss in spiral inductors and intra-chip noise coupling through the conductive substrate. However, the clock frequencies of the digital circuit blocks have increased so much that the digital circuits have started to suffer from the same physical limitations as the RF circuits. Therefore, it seems like some of these old problems are vanishing without much contribution from the RF designer community. Demand from the digital circuit designers has made the parasitic drain capacitances and resistances of the MOSFET devices to decrease. The number of available metal layers has increased from two to at least five, and the conductivity of the topmost metal layers has increased to reduce the RC constant of long digital signal paths. The highly conductive epitaxial wafers in older CMOS processes have been replaced with more resistive bulk wafers, mainly for alleviating the substrate noise coupling problems with mixed-mode designs.

2.1 Technology Choice

The electronics industry that has employed VLSI technologies has largely financed the development of them, and also guided the direction of development by setting the demands for the new generation technologies. Some of this development is the result of the natural interaction between the elecronics industry, the customers, and the technology research laboratories, and some of it is even based on coordinated work between the strong actors of the industry and the research [1] [2]. The demand mainly from the digital circuits designers for increasing speed, increasing single-chip system complexity, and decreasing current consumption has driven the physical dimensions of the transistors and circuits smaller, which also benefits the RF

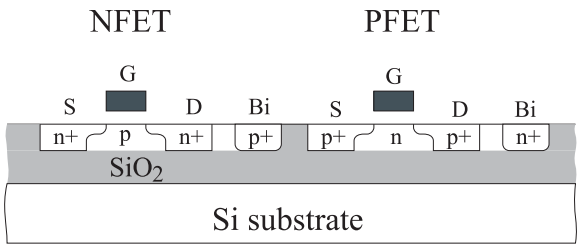
circuit designers. Since the internal clocking frequencies of the high-speed digital VLSI circuits, like computer central processing units, are approaching now the RF frequency bands that are used for wireless communications, the technologies that traditionally were developed mainly for digital use, have got properties that have made also construction of RF circuits possible.

2.1.1 Silicon-on-Insulator

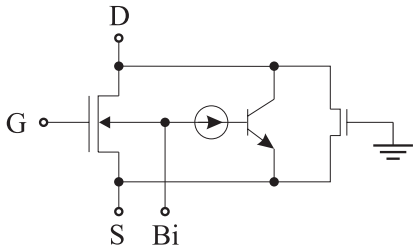
Silicon-on-Insulator (SoI) technologies basically employ standard main stream CMOS design and fabrication methods on an SoI wafer. It seems that after more than three decades of development work they finally are becoming main stream VLSI technologies [3] [4]. Simplified cross sections of typical SoI NFET and PFET devices are shown in Figure 2.1a. The most important difference to the conventional bulk CMOS technologies is that the topmost part of the wafer is a thin crystalline silicon layer that is separated from the substrate with a thin layer of buried silicon dioxide. The transistors are isolated from each other with a silicon dioxide trench.

SoI technologies have some advantages over to the more traditional bulk CMOS technologies, especially in low voltage and low power circuit design, and in high speed digital circuit design. Employing an SoI technology may improve the speed performance of digital logic circuits by approximately 30%, compared to the corresponding bulk CMOS technology [3]. The main reason for this speed improvement is that the drain-bulk capacitance of the traisistor is reduced, since the pn-junction between the drain and the chip substrate is missing. This speed enhanchement can alternatively be traded off, in order to reduce the power consumption of the circuit. Since the SoI transistors are isolated from the substrate, the intra-chip noise coupling through the substrate is very low. Therefore, some of the well-known difficult substrate noise coupling issues are avoided with mixed-mode SoC designs. Moreover, since the buried oxide isolates the devices from each other, it is not necessary to use highly conductive substrate material for preventing the latch-up. Therefore, the RF loss of spiral inductors in SoI circuits may be much lower than with bulk CMOS technologies, where the magnetic field of the inductor tends to induce eddy currents in the highly conducting substrate material [31] [48] [22]. Since the RF loss of the inductors is a major concern in integrated RF circuit design, the possibility of using highly resistive substrate material is very attractive for the RF designer.

Even though the fabrication processes of SoI circuits are very similar to the fabrication of bulk CMOS circuits, the electrical properties of SoI transistors are different from the conventional MOS transistors. If the silicon



(a)



(b)

Figure 2.1: *(a) A schematic cross section of a PD-SoI wafer, showing the NFET and PFET device structures. The local bulk nodes Bi may be connected to some other potential for controlling the threshold voltage of the device. However, in most circuits, the bulk contact is omitted, and the undepleted local bulk material is left floating. (b) An equivalent diagram of a PD-SoI NFET showing the parasitic bipolar transistor and the parasitic NFET. The charge stored into the bulk may activate the bipolar transistor when the SoI MOSFET is switched.*

layer on the top of the buried silicon dioxide insulator layer is thin enough, the regions between the the transistor channels and the buried oxide will be fully depleted when the transistor is operating in the strong inversion (FD-SoI). Consequently, the transistors do not have bulk terminals, that could be used for controlling the potentials under the channels. If the silicon layer is thicker than the depletion layer depth under the transistor channels when the transistors are operating under normal operating conditions, some of the bulk material under the transistor channels remains undepleted. In this case, each transistor has a back gate that can be left floating, connected

to the transistor source, or it may be connected to some active circuit for example for controlling the threshold voltage. These technologies are called partially depleted SoI technologies (PD-SoI).

SoI MOSFET transistors are known to suffer from effects related to self heating, thermal memory effects, and charge storage effects under dynamic operation, which make the circuit simulation and design challenging [5] [6]. Nevertheless, there are proven simulation models for SoI technologies [7], and the many recent commercial SoI digital VLSI circuits demonstrate that SoI technologies are also in practice suitable for designing very complex circuits. It has also been shown that SoI technologies are suitable for designing many microwave circuits [8] [9].

From the RF designers point of view, the presence of the buried insulator under the transistor is not only an advantage, even though it alleviates the noise coupling problems. In all SoI technologies, the transistors are thermally insulated from the substrate by the silicon dioxide isolator layer, making the devices prone to self heating. Therefore, one of the most challenging problems with using SoI technologies in RF transceiver designs is designing the RF power amplifier. Since the transistor parameters are modified due to the self heating effects and the transistors have long thermal time constants, the thermal memory effects will make the design of a low distortion power amplifier difficult.

The laterally doped MOSFET (LDMOSFET) is the RF power transistor device that is available both in conventional bulk CMOS and SoI technologies (Figure 2.2). In the SoI process, the device is insulated by the some hundrids of nanometers thick buried oxide layer, which increases the thermal insulation of the transistor. While the LDMOSFET is a well-proven power device in the conventional CMOS processes, it is difficult to find published experimental works about RF power amplifiers where the signal distortion due to the possible thermal memory effects of the SoI LDMOSFET is studied. Some recent publications show that, in SoI technologies with a thin buried oxide layer, the LDMOSFET RF power transistors perform very well in the terms of the intermodulation distortion, the S-parameters response, and the power added efficiency [10] [11] [12]. However, since neither of these measurements is able to reveal the distortion or the potential data transmission problems due to the thermal memory effects of the power transistor device, it is still unclear if the LDMOSFET is suitable for burst mode or spread spectrum RF power amplifier designs, or for transmitting complicated waveforms, like QAM and OFDM modulated signals. On the other hand, there is published work on complete RF power amplifiers transmitting QPSK modulated signals [13], which indicates that it is possible to

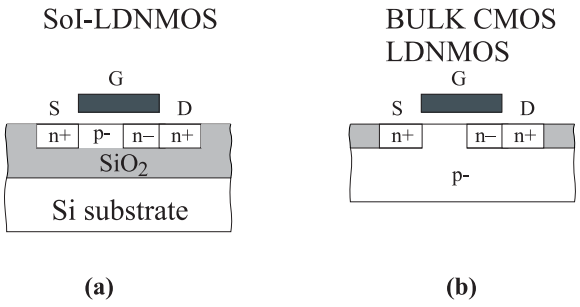


Figure 2.2: *(a) A schematic cross section of an LDMOSFET device in an SoI process. The n-region next to the drain improves the breakdown voltage of the device. (b) The LDMOSFET device in a conventional bulk CMOS process.*

construct working RF power amplifiers at least for simple constant envelope modulated signals.

SoI technologies may soon become the preferred technlogy choice in high-performance digital circuits, and they certainly have many attractive properties for mixed-mode circuit and SoC designs. If SoI becomes an important part of the consumer product market, the price of SoI wafers, and thereafter the price of circuit processing, may become acceptable also for SoC ASIC designs. However, it seems that SoI is not yet a safe choice as a general-purpose technology for SoC designs with RF interface, since it is not yet known if the price will be competitive, compared for example to the conventional CMOS technologies.

2.1.2 SiGe HBT BiCMOS

Since Silicon-Germanium (SiGe) based heterojunction bipolar transistors (HBT) are fabricated on silicon wafers and the processing does not necessarily need high temperatures, it is possible to fabricate them on patterned silicon wafers together with CMOS transistors. In the middle of 1990's, the fabrication methods of SiGe HBTs became mature for the commercial production of SiGe BiCMOS circuits. Soon after this, BiCMOS foundry services, that provide both CMOS transistors for designing digital circuits and SiGe HBT transistors for designing analog and RF circuits on the same chip, became available [14].

The SiGe HBT outperforms the conventional bipolar junction transistor (BJT) in many parametrs that are crucial to the RF circuit designer. The differences between the conventional silicon bipolar transistor and a SiGe HBT is illustrated in Figure 2.3, where the energy band diagrams of both transistor types are shown when the transistors are operating in the active region. The differences between the two appear in the shape of the conduction band shapes. The barrier for the electrons crossing the emitter-base junction is slightly lower for the SiGe transistor, which increases the collector current. Since the emitter regions in the two transistors are identical, the base currents will be roughly equal, and the net result is that the current gain $\beta = I_C/I_B$ of the SiGe transistor is higher [68]. In addition, while the conventional BJT relies entirely on diffusion when the electrons are transported from the emitter to the collector, the gradually changing band gap due to the germanium-doped base region in the SiGe HBT creates an electric field gradient that sweeps the electrons rapidly across the base region. The enhanchement in the electron transport speed improves significantly the f_t of the transistor.

The increased current gain or maximized f_t are usually not the desired final effects, but these properties are traded off for improving the other transistor properties. For example, it is possible to decrease the base resistance by increasing the base region doping level without detoriating the current gain, which results in lower noise figure and higher f_{max}.

Figure 2.4 shows a cross section of an NMOS transistor and an NPN HBT fabricated on the same wafer in a commercial SiGe BiCMOS process. The HBT structure consists of several doped layers, that are not present in the NFET structure. The gradually doped SiGe region in the base layer is usually epitaxially grown on the patterned wafer, before fabricating the metal layers. Since an epitaxial growth or precisely controlled ion implantation of Ge atoms on a patterned wafer is an unavoidable fabrication step of the SiGe HBT transistors, fabricating the SiGe HBT device adds a very different and challenging processing step to the IC fabrication, compared with the plain CMOS transistor fabrication process. In addition, since the CMOS transistor fabrication process must be compatible with the temperature cycles of the HBT fabrication, the CMOS transistor and HBT transistor fabrication processes will always be more or less coupled in the sense that the development of one must take into account the constraints set by the other.

Even though it is possible to use the SiGe BiCMOS process for designing pure CMOS circuits, it is unlikely that it would become profitable often to do so in practice. Even though the SiGe HBT transistors were provided as an additional process module, it seems that designing plain CMOS circuits

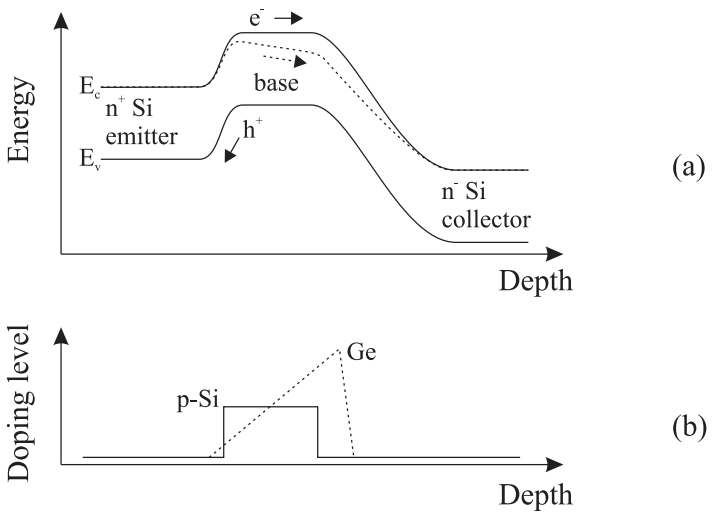


Figure 2.3: *(a) The enery band diagrams of a conventional Si-BJT (solid lines) and a SiGe-HBT (dashed lines), biased in the active operating region. The differences in the conduction band arise from the graded Ge doping of the SiGe-HBT, which gradually reduces the band gap when the electrons traverse from the emitter towards the collector. (b) The doping profile of the p-type dopant in both transistors (solid line), and the graded Ge content of the SiGe HBT (dashed line).*

in this technology will remain more expensive than designing them in a dedicated CMOS process. In addition, since moderate-speed digital circuits do not benefit from the SiGe HBT devices, the user community of SiGe BiCMOS is probably limited to the high-speed digital, mixed-mode, and SoC circuit designers. Therefore, this technology branch will not directly benefit from the large production volumes and technology advancements of the main stream digital circuits.

In designs, where the digital part is very large compared with the RF parts, it may turn out that the performance of the CMOS part of the cheapest available BiCMOS technology is not sufficient from the system design point of view. It seems that the CMOS parts of the SiGe BiCMOS technologies lag one or two generations from the state-of-the-art CMOS technology. In designs with a large digital part, even though in any available SiGe BiCMOS technology the HBTs would provide more than adequate performance for the RF part of the SoC design, for implementing the digital part of the

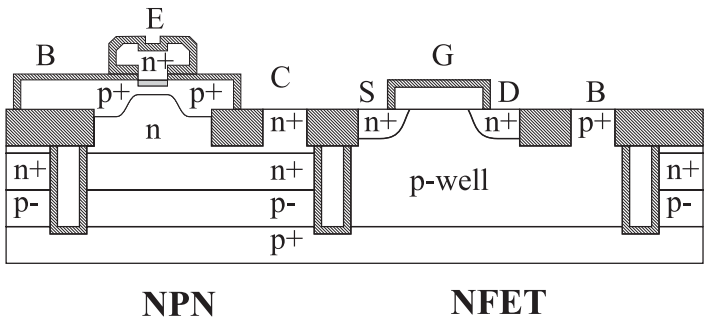


Figure 2.4: *A cross section of a SiGe BiCMOS wafer, showing an NPN heterojunction bipolar transistor and an NFET.*

system the line width may be too coarse with the cheapest alternative. Therefore, the minimum feature size must be chosen according to the digital parts, and the designer may be forced to choose an expensive SiGe BiCMOS process even though the performance of the RF parts would not need it.

Since SiGe BiCMOS technologies were developed from the beginning for mixed-mode and RF circuit designers, the process developers have paid attention to the special problems of these designs, while maintaining the ease of the CMOS digital circuit design. For this reason, a wide range of high-quality passive components for RF designs are available in most commercial SiGe BiCMOS processes, and support for advanced CAD tools for all design phases is usually available. Currently, SiGe HBT BiCMOS is a mature technology for mixed-mode designs and SoC designs with radio interface. The only good reason for avoiding it must be that there is another alternative that is cheaper.

2.1.3 CMOS

Historically, CMOS has been the work horse technology of the commercial main stream digital circuits designer community for more than two decades. The speed performance has improved, since the market has demanded faster-switching circuits, and the income from the sold circuits has financed the development work of the next generation. Even though CMOS processes that are dedicated to analog circuits designs have been available for years, the focus in the process technology development and funding has been in improving the speed and reducing the size and power consumption

of the digital circuits. Therefore, the fastest CMOS technologies have traditionally been tailored for the needs of the digital designers, and the analog designers frequently have even not got sufficient information about some of the important process parameters for designing and simulating analog circuits.

During 1990's, the speed of the CMOS transistors in the state-of-the-art digital processes became so high that it was possible to design RF circuits for the low-GHz region of the frequency spectrum, where many of the wireless and cellular telephone applications operate. Despite of the disussions about the inferior CMOS device physics and too large process parameter variations for robust RF circuit designs, several research groups demonstrated working fully integrated RF circuits that were implemented in the latest digital CMOS technology of the day [21] [25] [26] [27]. A well-known problem was that the high-frequency properties of the available passive components were poor. Especially the spiral inductors suffered from the substrate loss, which was difficult to avoid if the substrate was highly conductive and the field oxide layer was not made very thick. However, innovative work in research laboratories found new solutions at the architectural and circuit design levels, where the MOSFET device physics, highly conductive substrate, and unavoidable process parameter variations were thought to set the limits. Methods were found for compensating the tuned circuits against the process parameter variations, avoiding the bulky IF filters, reducing the power consumption of the circruits that run at the highest frequencies, and dealing with the bad quality factor of the inductors [20] [21] [31] [32]. In the end of 1990's, in addition to the several successful published research works, some companies started to sell highly integrated RF CMOS chips for example for 2.4 GHz ISM band applications.

Today, even though the latest generations of the commercial CMOS technologies still favor the digital circuits designer, it seems that the needs of the RF circuit designers have also got some attention. The focus in the CMOS process development work has shifted from supporting only digital circuit designers to supproting integration of whole systems, including analog electronics and a radio interface. Fortunately, many of the requirements of the RF designer and the VLSI logic circuit designers are very close to each other. Therefore, the current high-end CMOS processes provide highly conducting top metal layers, thick field oxide layers, high capacitance density MIM capacitors, and some foundries even publish measured data about RF devices, like Q values of spiral inductors and MIM capacitors.

One of the old arguments against using CMOS transistors in low-power amplifier designs has been that the transconductance per unit drain current is small. The transistor gain is apparently even worse with deep sub-micron

CMOS transistors, since the charge carrier velocity saturation next to the drain of the saturated transistor makes the transconductance almost bias-independent. The conventional bipolar transistor, and especially the SiGe HBT, provides more gain per consumed milliampere. However, as has been discussed in the recent literature, the transconductance per consumed current as a figure of merit is sometimes misleading, since it does not take into account the linearity of the amplifying device [20]. For example in low-noise amplifier (LNA) designs for wireless and cellular radio systems, the spurious-free dynamic range (SFDR) is a specification that is as important as the gain of the amplifier stage. If the amplifier transistor is non-linear, an undesired strong signal in the LNA input will generate intermodulation products that make the detection of the desired signal impossible. The dominating noise in the received signal in wireless and cellular radio systems often originates from the other users of the same frequency band, rather than from the internal noise sources of the receiver electronics. Therefore, the LNA must tolerate strong signals without generating strong intermodulation distortion components, and the low noise figure of the amplifier transistor turns out to be less important. For these reasons, if the dynamic range per consumed power is used as the figure of merit, the deep sub-micron CMOS transistors turn out to be very useful devices in the low-power LNA design.

Designing a fully integrated RF power amplifier in any existing silicon IC technology has been a well-known problem. Since the RF power transistors dissipate heat, and since the amplifier needs reactive passive devices for matching circuits, it has been difficult to design completely integrated PA stages, especially with CMOS technologies. In addition, since the power amplifier should deliver electric power to the load impedance, the operating voltage of the power amplifier should be relatively high. However,the low breakdown voltage of the modern MOSFET devices prevents often from using a high supply voltage. Nevertheless, successful integrated RF CMOS power amplifiers have been demonstrated [26] [28] [29] [30], even though the power added efficiency (PAE) of the amplifier is usually low. Since in many wireless applications the transmitter does not have to be on for long times, the low efficiency of this stage is not always a serious problem.

Today, all functional blocks of a complete, fully integrable CMOS transceiver have been demonstrated, and a fully integrated wireless LAN receiver chip operating in the 5 GHz band has been published [24]. Since the integration problems of the RF power amplifier should not be more difficult to solve than with the other silicon-based IC technologies, it seems that already the current date CMOS technologies are suitable for designing mixed-mode single-chip systems that employ wireless interface.

2.2 Design Tools

Despite of the intensive development work of mixed-mode circuits simulation tools, some central design phases of complex mixed-mode circuits still rely on the experience and intuition of the development team [17][19][61]. In particular, designing the chip floorplan and supply voltage distribution grids in the way that intra-chip crosstalk is reduced to the "acceptable" level is difficult, since it is difficult to simulate accurately the noise levels and the strength of noise coupling to the victim circuits. There are CAD tools that address some of these problems [18][60], but no widely accepted method that was able to reliably simulate all important intra-chip noise coupling issues exists yet.

The availability of the single-chip system design tools is approximately the same for all the candidate technologies. Hierarchial mixed-mode floorplan design tools, multi-layer routing algorithms, and mixed-mode circuit simulators are available for almost all available SoI, conventional BiCMOS, SiGe BiCMOS, and CMOS technologies. The problem, that the RF and analog circuit designers sometimes face when working with a process that is intended for digital circuits designs, is that the foundry submits only a limited set of simulation parameters for supporting digital circuit designs. In this case, analog and RF circuit designers are left without the information they need for using efficiently the simulation tools they have.

The poor quality factor Q of the integrated spiral inductor was for many years thought to be a major obstacle for complete integration of a high-quality RF synthesizer VCO in any silicon technology that uses moderately or highly doped substrate material. Some research groups have developed tools for predicting the spiral inductor performance, and some groups have even been able to design inductors with excellent Q value when using a CMOS process with highly conductive substrate, based on the results of the electromagnetic simulations [15][16][22]. However, the accuracy of the simplier methods has been questioned [18]. The method that combines an electromagnetic field solver with a layout design tool and an optimization algorithm is shown produce accurate results. However, even though the work of a research group demonstrates that it is possible to obtain excellent results, it is not obvious that ASIC design companies have access to the necessary tools, and are able to use them in a productive way during the intensive product development work. Fortunately, it seems that the lack of the spiral inductor optimization tools has not stopped the development of RF SoC circuits. Several research groups have already demonstrated working single-chip radios operating in advanced radio systems in 2.4 GHz and 5 GHz bands using commercial CMOS processes. Many IC foundries

have recognized the problem of the availability of characterized passive RF devices. Since they can't provide reliable simulation tools, some of them provide a library of characterized inductors and other RF devices.

2.3 Parasitics

The recent trend in silicon-based process technologies development for digital deep sub-micron designs has been that the substrate resistivity has become higher. The reason for this probably is that crosstalk through the conductive substrate is a severe issue in digital systems. The higher substrate resistivity is most welcome for the VCO designer, since one of the largest obstacles for the complete integration of the VCO has been the poor quality factor of the spiral inductor due to the RF loss in the conductive substrate. Since the resistances of the transistor electrodes and the metal conductors have decreased, designing RF circuits in the latest VLSI technologies has become easier than before.

From the CMOS VCO designer's point of view, the large parasitic capacitance per transconductance of the MOSFET and the high RF loss of the inductors are annoying problems. The transistors that are used for providing gain in the VCO circuit, must compensate for the loss in the tank circuit. If the loss is high, the transistor must be large, and the parasitic capacitances associated with the large transistor are also high. After making the necessary compromises, the resulting oscillator circuit tends to have a large capacitor and a small inductor, which reduces the voltage swing across the tank circuit. This tends to result in bad signal-to-noise ratio, and relatively large current consumption. Another well-known problem is that the varactor that is used for tuning the tank circuit must be small, since the large fixed parasitic capacitances of the gain transistors limit the total amount of capacitance in the tank circuit. Therefore, the limited tuning range of the CMOS VCO is often a problem, even if the phase noise problem was solved, for example by a relaxed phase noise system specification.

2.4 Conclusions

The VLSI process technology that is used in the SoC design sets many constraints for the RF transceiver designer. The designer is seldom allowed to pick the technology that best suits the needs of the RF circuits, unless the superior performance of the radio parts is the very reason why the chip could be sold. Instead, the cost and sufficient overall performance of the

complete chip will guide the technology choice. Therefore, the single-chip system RF designer should be able to design RF circuits with any available VLSI technology that allows it.

It seems that the frequency range where mobile communications systems will also in the future work is under 3 GHz, since the signal fading issues are difficult to handle at higher frequencies. The telephone user wants to move around while using the telephone, but it is difficult to maintain the connection between the base station and the telephone, if an object, whose diameter is only some centimeters, may block the signal. Even though it is possible to alleviate some of the fading problems with some kind of diversity scheme, a small telephone is easily completely hidden behind everyday objects [33].

Wireless data transmission systems (like 802.11a,b,d and HIPERLAN) will probably favour higher frequencies, in order to support high data transfer rates. Since the Local Area Network (LAN) users do not have to move while using the system at the highest data transmission rate, since buffering may be used for solving the problems due to short blockages, and since perfect spatial field coverage is usually not necessary, the signal fading issues at high frequencies are easier to solve than with telephony. On the other hand, many of the LAN systems use complicated modulation methods, like like 64-QAM and OFDM. Implementing single-chip radio circuits in these systems is demanding, since linear power amplifier stages and relatively complicated digital signal processing for demodulating and encoding the signal is needed.

For the studies carried out in this work, a relatively new 0.35 μm CMOS process was chosen for the experimental work, for two reasons. Firstly, it was available since it is realtively cheap and the process is widely used. The IC fabrication process is run every six weeks, which makes it possible to submit a design and have it processed without much delay, when it is necessary. This is a very important argument for any product development work: even though the goal is to directly design the final version of the chip, it is often necessary to correct later the errors in the first design without much delay and extra cost. Secondly, this process obviously is suitable for designing RF circuits for operating in the 2.4 GHz ISM band, where several unlicensed applications operate. The process is relatively simple compared with the later generation digital CMOS processes, which probably keeps it a relatively cheap and easily available alternative during the next few years. This technology choice is not considered as the best possible process for solving the given engineering problem, but a good compromise between the price, availability, and performance. A middle-sized ASIC design house might use similar arguments for choosing an IC process for working on

single-chip systems that include a radio interface that works in the 2.4 GHz ISM band, or at a lower frequency.

Chapter 3

Intra-chip Noise Coupling

One of the central problems in most mixed-mode integrated circuit designs is to design the chip in the way that the different functional modules do not disturb each other. Even though crosstalk problems are common in almost all electronics systems designs, putting the different functional blocks on the same chip often makes them more challenging. On the one hand, the signal and supply voltage conductors become much shorter, which will reduce electromagnetic coupling between the circuits. On the other hand, the spacing between the circuit blocks and conductors becomes very small, which may make the direct capacitive and inductive coupling strong. In addition, the substrate of the chip is usually more or less conductive. Unfortunately, the conductive substrate almost never works as a ground plane that helps in shielding the circuits. It usually couples signals between the circuits, and plenty of work in single-chip system designs is usually spent on resolving the substrate noise crosstalk issues.

Several different physical mechanisms are responsible for the crosstalk between circuits that reside on the same chip. Depending on the circuit design, layout design, and the properties of the IC process, some of these mechanisms will be more dominant than the others. In order to minimize the intra-chip interference problems, the members of the mixed-mode circuit designer team should have good understanding of the physics of the noise coupling mechanisms, and the circuit design and layout design techniques that reduce the effects of the interfering signals. This chapter reviews some of the most important coupling mechanisms in single-chip system designs.

3.1 Supply Voltage Noise

One of the obvious sources of interference is the noise in the supply voltage. Since the output impedance of any practical voltage supply is non-zero, the

time-varying current consumption of the circuits will make the available supply voltage to vary. If several circuits share the same voltage supply, the circuits will disturb each other by modulating the supply voltage. All practical circuits will convert the supply voltage variations to output voltage variations. Some well-known circuit techniques, like differential circuit designs and using current sources for biasing the active circuits, are able to improve the power supply rejection ratio (PSRR) of many circuits.

Differential circuit design is an effective way to suppress common-mode noise only when it is possible to make the circuit truly symmetrical and when the circuit operates with low signal levels. Even though it is usually easy to make the transistor layouts symmetrical, it is not always easy to balance the parasitic capacitances of the circuit. Figure 3.1 shows an example where the circuit may have excellent power supply rejection when the interfering signal frequency from the voltage supply line is low. However, if the output load capacitances C_1 and C_2 are unequal and the supply voltage includes transients, the output voltage of the amplifier is disturbed. If the repetition rate of the transients is low, the output voltage noise will also

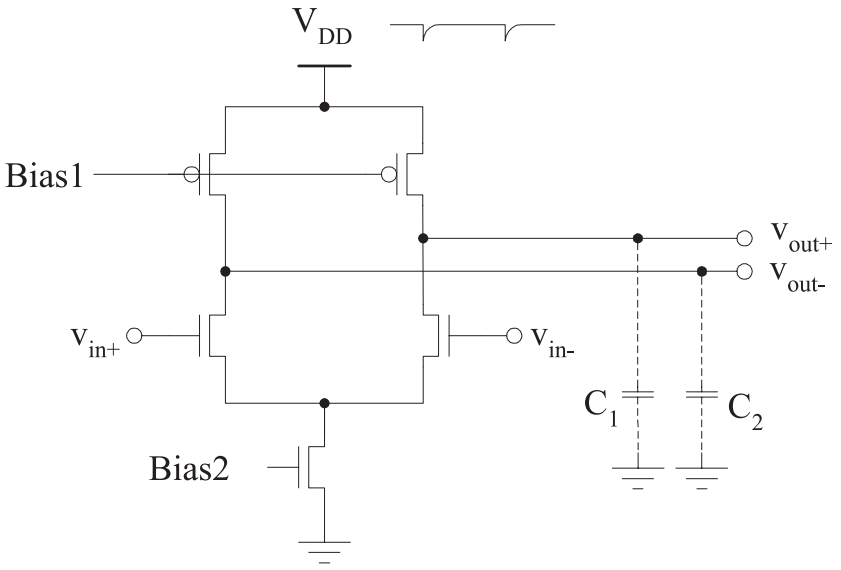


Figure 3.1: *A differential amplifier circuit whose power supply rejection ratio at low frequencies is excellent due to the symmetric circuit construction. A small change in the supply voltage will have the same effect on both output voltages. Since the output signal is defined as the difference of the output voltages, the output signal remains unchanged.*

include low frequency components.

The traditional circuit design techniques for improving the power supply noise rejection usually rely on stacking transistors in the circuit. Since the state-of-the-art VLSI circuits use very low operating voltages, stacking more than three transistors in order to improve the noise tolerance of the circuit is usually not possible. Therefore, the noise coupling through the supply voltage lines is a serious concern in low-voltage SoC designs, and the noise coupling through the supply voltage distribution network should be carefully analyzed when different functional blocks are made to share the same supply voltage source.

3.2 Common Return Path

Figure 3.2 shows another common problem related with the supply voltage source. In this example, the two circuits A and D are known to have excellent power supply rejection ratio. However, the two circuits share the same resistive ground conductor, which carries the power supply return currents of both circuits, and the signal voltage v_s. The time-varying power supply return currents generate a voltage across R_2. Since the signal voltage source is in the same loop with R_2, the noise voltage is summed to the signal

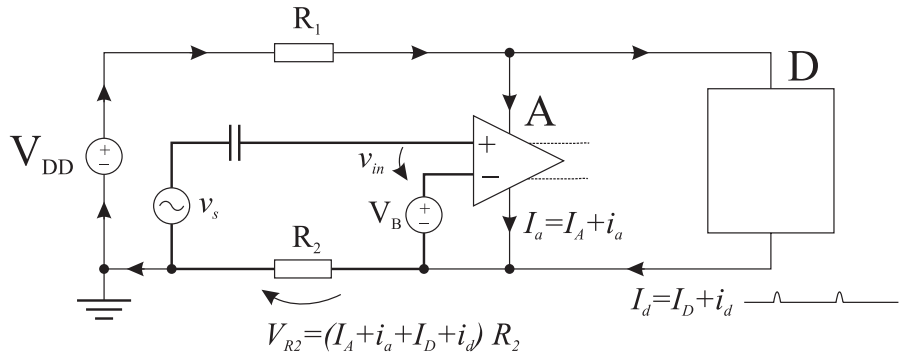


Figure 3.2: *Two circuits sharing the same supply voltage. The voltage loss in the resistive ground conductor R_2 due to the supply currents returning from the two circuits A and D will sum an undesired signal to the input of circuit A. The AC signal in the input of the amplifier A is $v_{in} = v_s + (i_a + i_d)R_2$.*

voltage. The excellent PSRR of the circuits does not help in suppressing this noise, since the noise is summed to the signal outside the circuits. The problem in this case is that the ground return currents are allowed to flow in the same loop with the signal voltage source and the amplifier input. It is interesting to note that the effects of the two noise current components i_a and i_d on the output voltage of circuit A are different. Since i_a is correlated with the input signal of circuit A, the effect of i_a is to increase the harmonic distortion of the circuit. If circuit D is not driven from the same signal source v_s, i_d is not correlated with the output signal of A, and the effect of i_d will appear as an uncorrelated interfering signal.

3.3 Inductive and Capacitive Coupling

The on-chip conductors, that carry large currents, may induce significant image currents to the neighboring conductors and to the conductive substrate, unless the mutual inductance is negligible. Even though the average current in any on-chip conductor is usually low, the peak currents in the supply voltage distributing network of the large on-chip digital blocks may approach several amperes. Obviously, severe intra-chip interference may take place if some of these transient currents are coupled to the signal conductors or to the substrate. Fortunately, it is usually rather easy to avoid significant image currents in the neighboring conductors by sensible layout design. It is more difficult to reduce the effect of the image currents in the substrate, since the distance between the conductor metal and the substrate is fixed. In order to minimize the interference due to the substrate image currents, the length of the conductors carrying large transient currents should be minimized.

Capacitive coupling from conductors that carry large voltage signals to the neighboring high-impedance conductors is another well-known problem with highly integrated circuits. Since the design rules of modern VLSI technologies allow very small conductor spacing, the capacitive coupling between two parallel conductors may be very strong. Therefore, high impedance levels in signal lines should be avoided, and the sensitive signals should be kept short and routed far away from the conductors that carry high-frequency voltage signals or voltage transients.

3.4 Interference Coupling Through the Substrate

Since in SoC applications different functional blocks are integrated on the same piece of semiconductor, electrical signals from the active circuits may

leak to the substrate and couple from the substrate to the other circuits. In addition, the on-chip heat sources may modulate the temperature dependent parameters of the other circuits on the same chip. In analyzing the substrate crosstalk problems, it is useful to discuss the noise source and the victim circuits separately. A typical noise source in an SoC application is a digital block where a large number of gates is switched simultaneously. Other potential on-chip noise sources are analog circuits that handle large currents or high-frequency signals, like RF power amplifiers, clock signal buffer circuits, and large transistors for driving off-chip loads. Typical victims of the substrate noise are the analog circuits that have large gain and process low-level signals, like amplifiers and filters, and circuits that otherwise are easily disturbed, like oscillator circuits.

The level of interference coupling through the substrate depends very much on the electrical properties of the chip substrate material, in addition to the quality of the circuit and layout design [59]. Technologies that employ relatively highly conductive substrate materials, like most CMOS and some BiCMOS technologies, suffer more from the substrate crosstalk effects, since the substrate provides a low-impedance path for the interfering signals. Most competitors of CMOS technologies provide relatively good substrate noise suppression. GaAs technologies use semi-insulating substrate material, which naturally isolates the different circuits from each other. SoI technologies isolate the devices electrically and thermally from the substrate with the silicon oxide layer, which greatly reduces the electrical substrate noise coupling. The thermal isolation of the transistors is known to to generate large local temperature gradients in SoI circuits. However, since the gradients are large only immediately under the power dissipating device, the problems are usually related to the power handling capability of large transistors and distortion due to the potential thermal memory effects, rather than intra-chip crosstalk [6].

The interference coupling through the substrate is usually relatively strong with CMOS and some BiCMOS technologies, since they employ more or less conductive substrate materials. Epitaxial wafers, that are often used with digital CMOS circuits fabrication, use heavily doped substrates that have a thin layer of lightly doped epitaxially grown silicon for fabricating the active devices. The highly conductive wafer material alleviates the latch-up problems with digital CMOS circuits. However, it also provides a low-impedance path between the different circuits, which makes it difficult to isolate the on-chip interference sources from the sensitive circuits. Lightly doped bulk wafers are also sometimes used with CMOS and BiCMOS technologies. Due to the higher substrate resistivity, the noise coupling through the substrate is weaker than with processes that use epitaxial wafers, if the

distance between the source and the victim circuits is large. On the other hand, the same amount of substrate current will change the local substrate potential more close to the source circuit, since the substrate resistance is higher. Finally, some CMOS technologies use triple well isolation for isolating the active devices from the substrate. While this method may reduce the intra-chip noise coupling level, the manufacturing process of triple well isolated CMOS circuits is complicated and expensive compared with the cheapest CMOS technologies. Given that the advantage of CMOS technology over the other technology alternatives is the cheap production cost, triple well isolation probably is not the way to make CMOS competitive in these applications.

3.4.1 Signal Coupling from the On-Chip Interference Source to the Substrate

In addition to the direct signal coupling through the fringing capacitances between the neighboring circuits and through the mutual inductances between the conductors, the on-chip noise sources may disturb the other circuits on the same chip by injecting currents to the substrate. When these currents flow in the resistive substrate material, the local substrate potential of the other circuits is modulated. Depending on the path of the interfering current in the substrate, some regions on the chip may suffer more than the others. If the substrate resistivity is relatively high, the substrate potential variation due to the substrate current will be largest close to the interference source. Correspondingly, the circuits close to the interferer are disturbed more. If the substrate is highly conductive, a current that is coupled to the substrate will change the potential of the substrate by the same amount everywhere on the chip, and moving the the victim circuit further away from the interferer does not decrease the crosstalk.

Several different physical mechanisms may generate currents in the resistive substrate of the chip [63]. The active circuits inject substrate currents through the parasitic capacitances between the active devices and the substrate. Even though the transistor leakage currents to the substrate are usually small, they can increase significantly the subsrtate noise level if a large amount of transistors is active at the same time. Large currents in the on-chip metal conductors may induce significant image currents in the substrate. Ground currents may flow in the substrate between the substrate contacts. In some cases, parasitic surface inversion under the metal conductors that carry high voltages may provide a low-impedance path for interfering singals. However, when the design rules of the process

are followed and the circuit operates within the allowed voltage limits, no conductive paths due to the parasitic inversion should occur.

The leakage currents from the MOSFET drains to the bulk are an important source of substrate noise in deep-submicrometer CMOS technologies. When the transistor operates in the saturation region with a large gate-drain voltage difference, the electric field near the drain is very strong. The strong electric field starts an efficient impact ionization in this region, which generates new electron-hole pairs [58]. While the resulting majority carriers will flow to the transistor channel, the minority carriers will flow to the substrate, generating a substrate noise current that is correlated with the signal in the transitor drain. Even though the substrate current from a single transistor may be very small, large digital blocks where a large amout of transistors switch simultaneously may produce strong substrate currents. The noise currents from the MOSFET drains to the substrate due to the impact ionization is a serious concern for the CMOS VCO desinger, since the noise signal is DC coupled to the substrate. Therefore, significant low-frequency noise currents may be injected to the substrate.

Capacitive signal coupling from the drain to the substrate through the drain-bulk pn-junction is another typical substrate noise source in CMOS technologies. Since the impedance of the pn-junction is high at low frequencies, only high-frequency signals and transients may efficiently couple to the substrate this way. Unfortunately, almost all SoC designs include large blocks of digital circuits and on-chip clock signal buffers, which are able to inject relatively strong current impulses through the drain-bulk capacitors.

3.4.2 Interference Coupling from the Substrate to the Victim Circuit

The local substrate potential variations may disturb the victim circuit by several different physical mechanisms. In most IC technologies, the capacitive coupling from the substrate to the metal conductors is so weak that it is not a major concern considering the substrate noise interference. However, the parasitic capacitances between the devices of the victim circuit and the substrate are usually higher, and are able to couple the high-frequency substrate potential variations and impulse-like noise to interfering currents to the victim circuit.

In CMOS technologies, the parasitic drain-bulk junction capacitance is the most obvious path for the noise signal from the substrate to the victim circuit. However, the parasitic capacitances of other devices, like the bottom plate of an amplifier feedback capacitor or the substrate capacitance

of an integrated resistor in a bias circuit, may be very efficient in picking up the substrate noise. The modulation of the transistor back gate potential is the other important substrate noise coupling mechanism in CMOS circuits. In the simpliest CMOS technologies for digital circuit designs, the NMOS transistors are fabricated directly on the p-type substrate, while the PMOS transistors reside in an n-well. Consequently, the NMOS transistor back gates are directly connected to the substrate, making it impossible to isolate the back gates of the NMOS transistors from the substrate potential fluctuations.

3.4.3 Methods for Reducing the Substrate Noise Couping

Once everything has been done for reducing the amount of injected substrate current at the substrate noise sources, various layout design techniques may be used for controlling the path of the substrate currents. The noise source or the victim circuit may be surrounded with a guard ring, which will collect at least some of the substrate current. Of course, the source and the victim should be placed as far away from each other as possible, but as was discussed, this has little effect if the substrate is highly conductive.

The sensitivity of the victim circuit depends very much on the quality of the circuit design and the layout, in addition to the properties of the IC process. Even though it is not possible to completely remove the parasitic capacitances and thermal coupling between the substrate and the victim circuit, differential circuit design techniques and symmetrical layout design methods may reduce the effects of the coupled noise. A phase-locked loop is able to suppress the noise frequency components that fall inside the loop filter bandwidth. However, these circuit design methods have their limitations, especially when the signal swing in the circuit is large or when the noise signal spectrum contains strong frequency components that the circuit is not designed to handle. For effective suppression of the substrate crosstalk, the substrate noise coupling to the victim circuits must be minimized.

3.4.4 Substrate Noise Analysis Methods

No widely accepted method for modeling and simulating the substrate noise problems exists yet. Many published works on this topic exist, some of which demonstrate promising methods for simulating the substrate crosstalk in some cases [59][60]. There are also commercial design tools that help in analyzing the substrate noise coupling problems in some special cases. A

major problem in simulating the substrate network is that the substrate current flows in three dimensions in the resistive substrate material. Therefore, it must be modeled with a dense three-dimensional resistor network. The amout of nodes in a network that represents the actual problem well becomes very large. Correspondigly, simulating the resistor network with the circuits that may contribute to the substrate noise level takes too much computer power, if conventional circuit simulation techniques are used.

Using a lightly doped substrate is attractive in single-chip systems designs, since it provides better isolation between the on-chip circuits than highly conductive substrates. Unfortunately, the remaining crosstalk is more difficult to simulate, since a full 3-D model for the substrate is needed. Crosstalk in circuits that are fabricated on heavily doped epitaxial substrates is easier to simulate, since the conductive substrate in the simulations may be replaced with one node. Therefore, the number of nodes in the simulation is smaller.

3.5 Conclusions

The discussion shows that it is not easy to design a circuit that could easily be reused with later SoC designs, especially if it is a potential victim circuit. There are many different mechanisms that may couple undesired signals from the interferer circuits to the victim circuits. To minimize the crosstalk, they should be taken into account at all design abstraction levels, not only in the design of the victim circuit. However, information about the substrate noise level, the floorplan, the voltage supply grid structure, and the spectrum of the noise signal in the future designs is not available. If the PSRR and the tolerance of the substrate noise potential fluctuatios are maximized by excessive supply regulation and putting a guard ring around every device, the resulting circuit probably is complex and consumes too much current and is too large for the next generation system design.

Unfortunately, it is difficult to make the intra-chip noise analysis of reusable circuits systematic, since it is difficult to describe the interference coupling strength between the on-chip circuits with with a limited set of clearly defined parameters, and since no widely accepted method for simulating the effects of intra-chip noise coupling exists. As was seen in the previous discussion, the noise coupling strength between the source and the victim circuits depends at least on the interfering signal waveform, the quality of the circuit design, the distance between the two circuits, the signal level in circuits that work in the large-signal region, and the mechanisms that

couple the interfering signal to the substrate and from the substrate to the victim circuit.

In terms of the substrate noise coupling strength, CMOS technologies are the worst among the technology alternatives for implementing single-chip systems. Therefore, the substrate noise is usually considered as one of the most challenging issues in CMOS mixed-mode circuit designs. However, several research groups and commercial companies have already demonstrated fully integrated CMOS single-chip systems that include completely integrated radios for operating in advanced radio systems. Therefore, it looks like once the substrate noise coupling mechanisms are well understood and taken into account in the system design, the performance of many low-cost CMOS technologies is acceptable for these applications.

Chapter 4

Interference Conversion in the VCO

Oscillators, that work under normal operating conditions, are able to translate low-level noise signals in the frequency plane from low frequencies to close to the payload signal frequency, for example by amplitude or frequency modulation. Relatively weak interfering singals, that modulate the VCO core circuit or the bias current circuit, may create sidebands that rise clearly above the phse noise level. If the oscillator tends to injection lock to the interfering signal or to one of its harmonic frequencies, very weak interference may prevent the PLL from locking properly at some frequencies. For these reasons, isolating the oscillator from the on-chip noise sources is often more challenging than solving the noise coupling problems with amplifier and filter circuits.

Even though the noise performance of fully integrated VCO circuits is widely studied in the recent literature, the discussion is usually focused on minimizing the internal phase noise of the circuit, or trading off the phase noise performance against the power consumption. However, in most practical wireless system designs where the VCO is integrated on the same chip with various other circuits, it is likely that the internal noise of the oscillator components is not the only significant noise source that disturbs the VCO circuit. Instead, various signals from the other circuits on the same chip are coupled to the VCO tank circuit, and the spurious signals due to this crosstalk, rather than the internal phase noise floor of the circuit, may determine the adjacent channel noise level [18] [52]. This chapter presents how the spectrum of the frequency synthesizer may be contaminated by interfering signals that are coupled to an LC tank tuned VCO from the other circuits.

4.1 Negative-G_m VCO Circuits

Different variants of the varactor-tuned negative-G_m oscillator are widely used in integrated RF frequency synthesizer VCO circuits, since they are suitable for full integration, have good phase noise properties compared with the other fully integrable oscillator circuits, provide large-swing differential output signals, and are well-known and proven circuits [71]. Some of the popular variants are shown in Figure 4.1. Sometimes the bias current source is placed between the oscillator core circuit and the ground. Various types of varactor devices are used for tuning the oscillating frequency. BiCMOS VCO circuits often employ the circuit of Figure 4.1b, where the NMOS transistors are replaced with NPN transistors, and the base drive signal levels may be adjusted with a capacitor network.

Even though it is possible to start up and run these oscillators with relatively small signal amplitude, it is usually desirable to maximize the tank circuit voltage peak-to-peak amplitude. The signal-to-noise ratio of the output voltage is usually best when the output voltage amplitude is relatively high[1]. If the tank circuit provides sufficiently high drive level for the buffer amplifier stage, the buffer transistors may be made small, since they do not need to provide much voltage gain to produce accetptable signal level for the following circuits. The smaller the buffer transistors are, the less input capacitance they have, and the less they limit the tuning range of the oscillator.

If an integrated spiral inductor is used, a well-known design poblem is to minimize the coupling of the tank circuit energy from the inductor to the substrate, in order to maximize the operating Q of the tank circuit [31] [21]. To compensate for the high RF loss in the spiral inductor, the gain of the core circuit transistors must be sufficiently high. Since MOSFETs provide relatively small transconductance per unit gate width, the gain stage transistors must be made large. However, in addition to increasing the current consumption, this makes the drain-bulk junction capacitances of the gain transistors large, which tends to limit the available frequency tuning range of the oscillator. The narrow available tuning range is a well-known design problem with CMOS VCO circuits. Some designs solve the problem by providing the varactor a wide control voltage range [50]. Sometimes MOS varactors are used instead of pn-diode varactors, since they provide wider

[1] As far as the oscillator operates in the current limited region and the gain transistors are the dominating source of phase noise, increasing the amplitude will increase the SNR. However, if the current source does not stay in the saturation region during the whole oscillation cycle or if the current source is the dominating source of the phase noise, increasing the tail current does not necessarily improve the SNR.

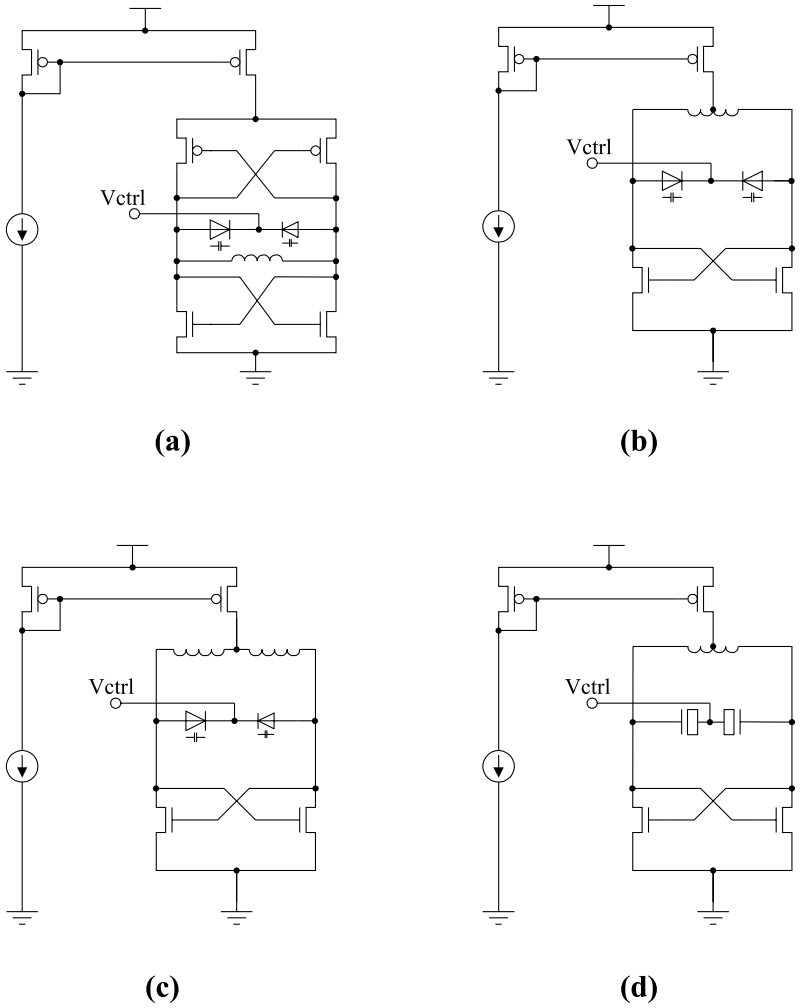


Figure 4.1: *Some popular fully integrated CMOS VCO circuits. (a) A varactor diode tuned CMOS VCO, (b) A varactor diode tuned NFET VCO with a symmetrical center-tapped coil, (c) a varactor diode tuned NFET VCO with two spiral inductors, and (d) a MOS varactor tuned NFET VCO.*

tuning range. To alleviate this tuning range problem, some CMOS process compatible very wide tuning range varactors have been published [34] [36].

Another well-known problem is to maintain the tuning curve of the VCO relatively linear. If the VCO tuning sensitivity varies across the tuning

voltage range, the locking delay of the phase-locked loop will depend on the control voltage [64]. Unfortunately, the varactors that provide the widest tuning range, tend also to be very non-linear [44]. Recently, some creative ideas have been presented for linearizing the tuning curve [34] [37].

The following sections describe how an interfering signal, that is coupled to the VCO circuit, is translated to sidebands in the VCO output signal. The oscillator circuit of Figure 4.1b is used as the example circuit, since it is simple. However, the ideas presented apply to most differential LC tank tuned oscillator circuits.

4.2 Amplitude Modulation

For desrcibing the effects of the varying bias current to the oscillator output signal amplitude, the circuit of Figure 4.1b is studied here. When the signal voltage swing in each NFET drain node is large (say, more than two times the threshold voltage of the transistor), the gain transistors work in the switching mode. As long as the tail current source PFET remains in the saturation region during the complete oscillation cycle, the available tail current will limit the amplitude of the voltage waveform. When one of the gain transistors is off, the other one draws the full tail bias current through the corresponding inductor half. This current flows to the same direction with the current that already is flowing from the tank circuit capacitor through the inductor at this moment, and strengthens the magnetic field of the inductor. Since the tail current is added to the tank circuit current when the magnetic field of the inductor is building up, increasing the tail current will increase the stored energy in the magnetic field. Therefore, increasing the tail current will increase the amplitude of the voltage signal. A typical amplitude versus tail bias current curve is shown in Figure 4.2. Even though the detailed shape of this curve may vary, for most LC oscillators it will increase monotonically across the useful operating region. Therefore, an AC component in the tail current will modulate the amplitude of the oscillator output signal, which will produce undesired sidebands to the oscillator specrum.

The time domain voltage waveform of an amplitude modulated carrier modulated with a sinusoidal signal can be written as

$$s_{AM}(t) = A_c[1 + A_m cos(2\pi f_m t)]cos(2\pi f_c t) \tag{4.1}$$

where A_c=the unmodulated carrier amplitude, A_m=the amplitude of the modulating signal (relative to A_c), f_m= the modulating signal frequency,

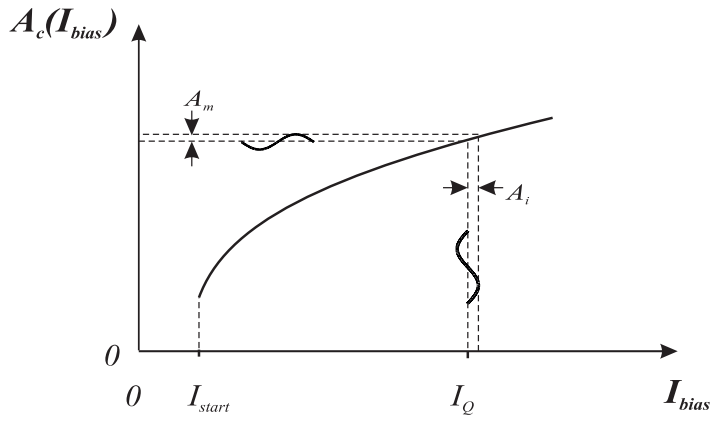


Figure 4.2: *Tank circuit voltage amplitude vs. the tail current in a typical negative-G_m oscillator circuit.*

and f_c=the carrier wave frequency. In order to see the individual spectral components of the signal, this equation can be expanded to

$$\begin{aligned} s_{AM}(t) = A_c\{&cos(2\pi f_c t) \\ &+\frac{A_m}{2}[cos(2\pi f_c t + 2\pi f_m t) \\ &+ \quad cos(2\pi f_c t - 2\pi f_m t)]\ \} \end{aligned} \tag{4.2}$$

which shows that two sidebands appear around the carrier signal due to the amplitude modulation. The power spectrum of this signal is shown in Figure 4.3.

The slope of the curve in Figure 4.2 at the operating tail current value of $I_{bias} = I_Q$ determines how much weak modulation of the tail current modulates the carrier amplitude. If the tail current includes a sinusoidal AC component:

$$I_{bias} = I_Q[1 + A_i sin(2\pi f_m t)] \tag{4.3}$$

and the slope of the amplitude vs. bias current curve at the given operating tail current is

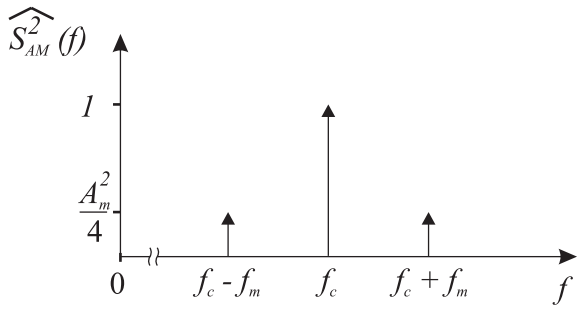


Figure 4.3: *The normalized power spectrum of a sinusoidal carrier that is amplitude modulated with a sinusoidal signal.*

$$k_A = \frac{dA_c}{dI_{bias}} \quad | \; I_{bias} = I_Q \tag{4.4}$$

the amplitude of the modulating signal in the voltage domain is

$$A_m = k_A \; A_i \; I_Q \tag{4.5}$$

Since the relative level of the sideband power to the carrier power (from Equation 4.2) in decibels is

$$P_{sb,dB} = 10 \; log(\frac{A_m^2}{4}) \tag{4.6}$$

we obtain for each AM sideband level as a function of a given tail current I_Q, and a given tail current AC component amplitude A_i

$$P_{sb,dB} = 20 \; log(\frac{k_A \; A_i \; I_Q}{2}) \tag{4.7}$$

For example, if the tail current is 2 mA, the amplitude of the tail bias current AC component is 1% of the tail bias current value, and $k_A = 1V/mA$ (a typical value for a CMOS VCO), the level of the AM sidebands is -100 dBc.

4.3 Frequency Modulation

If a sinusoidal signal modulates the frequency of a sinusoidal carrier, the time domain voltage waveform of the resulting signal can be written as

$$s_{FM}(t) = A_{cFM}\ cos(2\pi f_c t + \beta\ sin(2\pi f_m t)) \tag{4.8}$$

where

$$\beta = \frac{\Delta f}{f_m} \tag{4.9}$$

and A_{cFM}=the carrier amplitude, f_c=the carrier wave frequency, Δf= the peak frequency deviation, and f_m=the modulating signal frequency. The parameter β is called the modulation index. The peak frequency deviation is related to the amplitude of the signal that is the reason for the frequency shift by

$$\Delta f = k_f\ A_i \tag{4.10}$$

where k_f is the sensitivity of the carrier signal frequency to the modulating signal, and A_i is the amplitude of the modulating signal.

If the modulation index is small, we can make the "narrowband FM" approximations

$$cos[\beta sin(2\pi f_m)] \approx 1 \tag{4.11}$$
$$sin[\beta sin(2\pi f_m)] \approx \beta sin(2\pi f_m) \tag{4.12}$$

These approximations hold usually very well in oscillator spurious components analysis, since the interfering signal usually is rather weak, the interesting spurious frequency is in the adjacent channel (f_m is large) and the sensitivity coefficient k_f of a reasonably well designed oscillator circuit is not very large. Using Equations 4.11–4.12 we can expand Equation 4.8 to

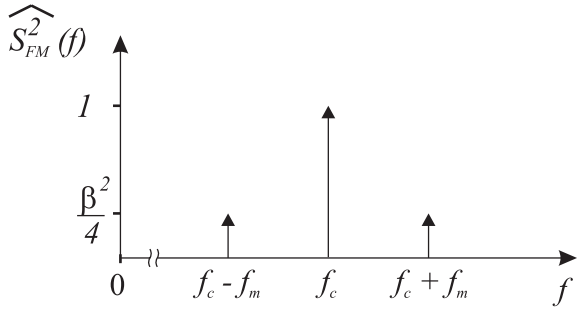


Figure 4.4: *The power spectrum of a sinusoidal carrier that is weakly frequency modulated with a sinusoidal signal.*

$$\begin{aligned} s_{FM}(t) \approx\ & A_{cFM}\{cos(2\pi f_c t) \\ & +\frac{\beta}{2}[cos(2\pi f_c t + 2\pi f_m t) \\ & -\quad cos(2\pi f_c t - 2\pi f_m t)]\ \} \end{aligned} \tag{4.13}$$

The power spectrum of this signal is shown in Figure 4.4. If we set $\beta = A_m$ and compare Equation 4.2 with Equation 4.13, the only difference is the sign of the last cosine term. In this case, the power spectrum of the weakly FM modulated carrier of Equation 4.13 is identical to the power spectrum of the amplitude modulated signal in Figure 4.3.

Combining Equations 4.9, 4.10, and 4.13, we find that the power of each FM sideband relative to the carrier in decibels is

$$p_{sb,FM} \approx 20\ log(\frac{k_f A_i}{2f_m})\ dBc \tag{4.14}$$

Using Equation 4.14 it is possible to calculate the FM sideband level, if the interfering signal and the sensitivity of the VCO are known. For example, if the tail bias current is 2 mA, the amplitude of the tail bias current AC component is 0.1%, or $A_i = 2\ \mu A$, the sensitivity of the oscillating frequency is 15 MHz/mA (a typical number for a varactor diode tuned CMOS VCO), and the frequency of the interfering tail current AC component is 1 MHz, the level of each FM sideband is -36.5 dBc.

Using Equation 4.14, Figure 4.5 plots the relative sideband power level for some interfering sinusoidal signals, as the function of the VCO sensitivity coefficient k_f. The amplitude of the interferer is always $A_i = 1\ \mu A$.

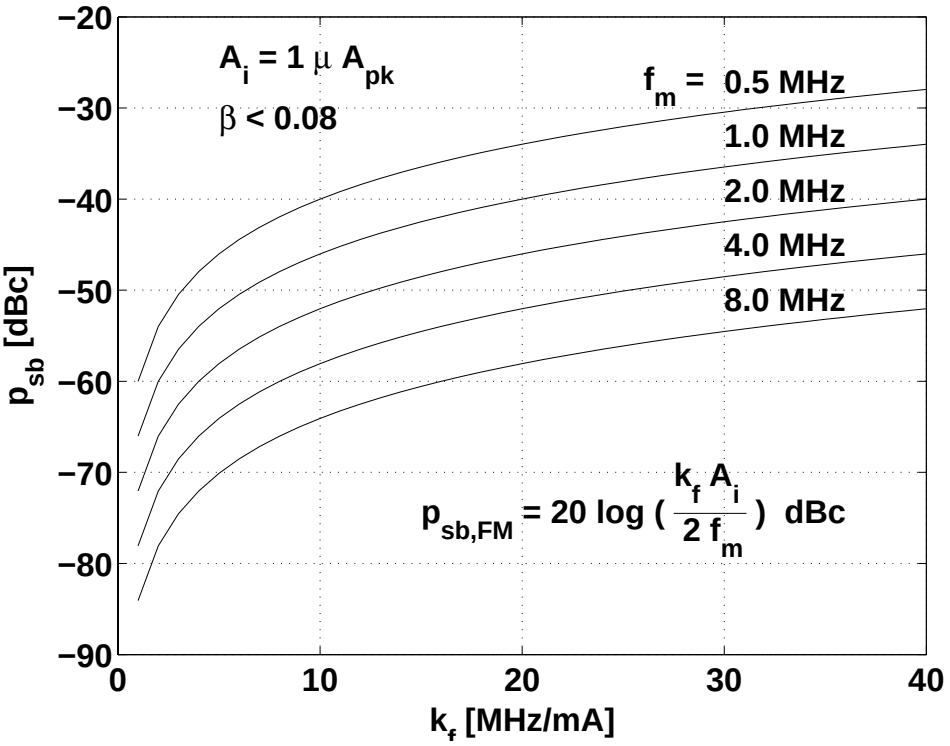


Figure 4.5: *The FM sideband power level due to a weak sinusoidal tail current AC component that modulates the oscillating frequency.*

4.4 Remarks

Since AM and FM produce qualitatively similar power spectra, it is difficult to determine if the sidebands due to an interfering signal in the measured power spectrum of a VCO originate from amplitude modulation or frequency modulation. However, if it is possible to vary the frequency of the interfering signal, it is easy to distinguish between these two mechanisms, since the amplitude of the FM sidebands depends on it, according to Equation 4.13. The level of AM sidebands is independent of the interference frequency.

If pn-junction capacitances or MOS capacitances are present in the oscillator tank circuit, modulation of the tail bias current usually creates FM sidebands that are much stronger than the corresponding AM sidebands.

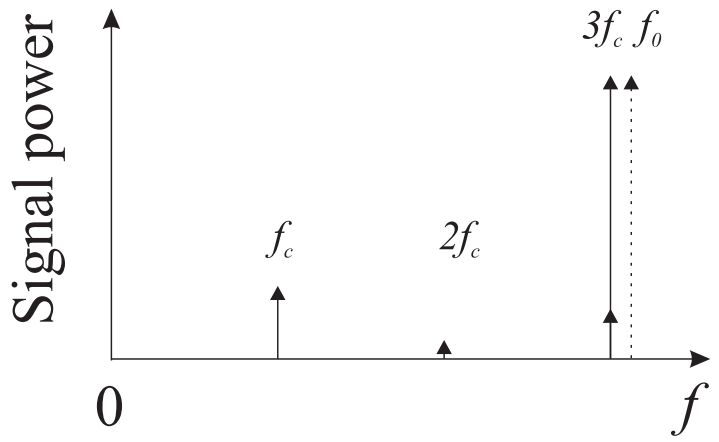


Figure 4.6: *The VCO locking to one of the harmonic frequencies of the on-chip clock signal. f_c is the interfering clock signal frequency, f_o is the desired frequency synthesizer output frequency. The VCO runs most of the time locked to $3f_c$. The frequency jumps back to f_o each time the PLL tries to correct the frequency offset, but since the VCO may lock fast to the interfering clock signal, the spectral line at $3f_c$ may be almost stable.*

Since varactors and many parasitic capacitances in the gain transistors change their capacitance values when the signal voltage in the tank circuit is changing, any unstability in the tail current will modulate the frequency of the oscillator, unless the voltage dependent capacitances can be made to cancel each other.

4.5 Injection Locking

If one of the harmonic or sub-harmonic frequencies of a periodic interfering signal matches closely to the oscillating frequency, the oscillator may injection lock to the interfering signal. In this case, the oscillator changes from an autonomous system to a forced system. If the oscillator is working in a phase locked loop, the result is an unstable frequency that the PLL tries to correct each time the phase comparison is completed. During a new frequency counting operation, the oscillator may lock to the interfering frequency, until the PLL tries to force the oscillator to the correct operating frequency again.

Injection locking is a well-known problem with PLL frequency synthesizers that suffer from signal leakage from the transmitter power amplifier to the VCO. If the PLL is used for generating the carrier frequency and the signal frequency in the power amplifier differs slightly from the carrier because it is modulated, the VCO in the PLL may try to lock to the leaking signal from the power amplifier. This problem may be avoided by choosing the transmitter architecture in the way that the power amplifier and the VCO operate exactly in the same frequency, even when the carrier is modulated. However, considering a general-purpose frequency synthesizer module design, the freedom of choosing the transmitter architecture is not available. For this reason, a general-purpose VCO circuit should be made as immune as possible to injection locking, by decreasing the amount of external AC signal coupling to a negligible level.

4.6 Noise Coupling from the Substrate

Even if the tail current of the oscillator is completely noise-free, there are mechanisms that may couple interfering signals directly from the on-chip noise sources to the oscillator core circuit. It is usually possible to suppress direct capacitive coupling from the other circuits to a negligible level by placing the VCO far away from the interfering signal sources in the chip floorplan, and taking care that conductors that carry potential interfering signals are not routed close to the VCO. However, substrate potential variations may couple DC, low-frequency, and high-frequency signals to the VCO core circuit through the back gates of the gain stage transistors. High-frequency signals and transients originating from swithcing signals may couple in from the substrate through the various parasitic capacitances, mainly through the gain stage transistor and the current mirror output transistor drain-bulk junction capacitors, and the parasitic capacitances from the spiral inductor to the substrate. The buffer transistor parasitic gate-drain capacitances may also couple disturbing signals from the buffer outputs to the VCO core.

4.7 Noise Coupling Inside the VCO Core

Interfering signals, no matter how they were coupled in, will sum undesired currents and voltages to the VCO core circuit branches. If the VCO core is made as symmetrical as possible, most of the interfering signals will appear as common-mode signals. The influence of the resulting common-mode current signals may be analyzed in the same way as interfering current

signals in the tail current, as presented in Sections 4.2–4.4. If the core circuit is perfectly symmetrical, a weak common-mode voltage summed to the oscillator output nodes will not modulate the amplitude of the differential tank circuit signal significantly. However, since it does vary the signal common-mode voltage level, it will lead to frequency modulation if voltage dependent capacitances are present, as described in Section 4.3.

Fortunately, mainly capacitively coupled signals from the substrate or through the buffer transistor gate-drain capacitances might introduce common-mode voltage summation to the oscillator output nodes. Since these parasitic capacitances are very small, the interfering signal frequency must be very high to significantly modulate the common-mode voltage level of the VCO core output nodes. Since the sidebands from a high-frequency modulating signal f_m will suffer from high attenuation (Equations 4.9 and 4.13), the resulting FM sidebands will be very weak, and located very far away from the carrier frequency. However, switching operations with low repetition rate (like DRAM refreshing or data transmission through a serial bus) may couple low-frequency interfering signals to the VCO core through these parasitic capacitances. Since the low frequency components of these signals will generate FM sidebands close to the VCO oscillating frequency, infrequently repeating bursts are a potential source of spurious sidebands in the VCO output spectrum, even if they are coupled to the VCO core as pure common-mode signals.

Some of the interfering signals will couple to the VCO core in the differential mode. Since the device matching is never perfect, and since it is often not possible to construct a perfectly symmetrical circuit, some of the common-mode interference signals are also converted to differential signals, which will directly perturb the differential tank circuit. From the noise analysis point of view, it does not make any difference if the interfering differential signal is coupled to the tank circuit as a current or a voltage mode signal. The final effect of the interfering current or voltage signal is that the phase and the amplitude of the tank circuit voltage waveform are disturbed.

Periodic and random signals that disturb the tank circuit are known to create sidebands to the frequency spectrum of the oscillator, even if the amplitude limiting mechanism was able to suppress the resulting amplitude modulation, and the voltage dependence of the tank circuit capacitance may be ignored [73]. Any interference that is coupled to the tank circuit in the differential mode disturbs the VCO in much the same way as the internal noise sources of the VCO. Therefore, most methods, that are developed for analyzing the phase noise, are suitable for analyzing the effect of this type of external interference. Some recent works on the phase noise properties of oscillator circuits have produced useful analysis methods that

are also suitable for analyzing the effects of periodic disturbing signals on the oscillator spectrum [48] [49].

4.8 Conclusions

There are several different mechanisms that may couple interfering signals to the *LC* tank tuned VCO circuit, and convert them to sidebands. The voltage dependent capacitances of the tank circuit may convert common-mode interfering signals to FM sidebands. The sensitivity to frequency modulation depends on the slope of the frequency-vs-bias current curve in the operating point of the oscillator core circuit. The differential circuit topology of the oscillator does not help in suppressing the FM sidebands that arise from the voltage dependent capacitances of the tank circuit. Otherwise, differential circuit topology and symmetrical circuit layout do improve the inteference tolerance, since the interference coupling to the differential tank circuit is reduced, and the sidebands rising from these signals are suppressed.

Chapter 5

Lossy Tank Circuit Response

The differential equation that describes the dynamics of the ideal LRC tank circuit of Figure 5.1, is known to be the damped harmonic motion equation:

$$C\ddot{E} + \frac{1}{R}\dot{E} + \frac{1}{L}E = 0 \tag{5.1}$$

where $E = E(t)$ is the voltage across the circuit, and $\dot{E}$ and $\ddot{E}$ are the first and second derivatives of $E(t)$. Equation 5.1 is usually deduced considering a one-dimensional mechanical system with a spring, mass, and a dashpot [65], [66], [67]. The circuit of Figure 5.1 is an electrical equivalent of the mechanical system.

The coefficient of $\dot{E}$ is related to the loss in the system. Even though with simple mechanical systems the loss is always positive, this coefficient

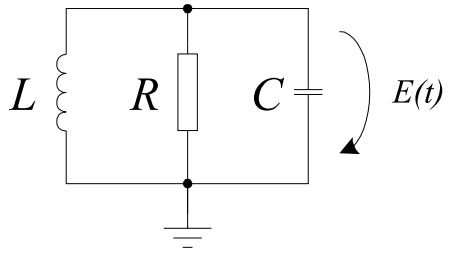


Figure 5.1: *The ideal lossy tank circuit diagram. None of the components is voltage dependent, and no external source is driving the circuit when* $t > 0$.

may also be negative in electrical circuits, if active circuit elements are present. A negative value of R in the circuit of Figure 5.1 implies gain instead of loss. For analyzing electrical circuits, it is necessary to find the solutions of Equation 5.1 for all non-zero values of R. Appendix A deduces the solutions for all relevant initial conditions and parameter values in the following discussion.

5.1 LRC Circuit Response

The response of the LRC circuit of Figure 5.1 depends on the circuit parameters R, L, and C, and the initial conditions. When $\frac{1}{R^2} < \frac{4C}{L}$, the circuit is underdamped and the response is oscillatory. In this case, the particular solution with the given arbitrary initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$ is

$$E(t) = e^{-\alpha t}\{E_0 \cos \omega_u t + \omega_u^{-1}(e_0 + \alpha E_0^2) \sin \omega_u t\} \tag{5.2}$$

where

$$\alpha = \frac{1}{2RC} \tag{5.3}$$

$$\omega_u = \frac{1}{2C}\sqrt{\frac{4C}{L} - \frac{1}{R^2}} \tag{5.4}$$

If $0 < R < \infty$, the circuit dissipates energy. Therefore, the response is an exponentially decaying sinusoidal signal. If $-\infty < R < 0$, the signal in the circuit is amplified, and the response is an exponentially growing sinusoidal signal.

If $\frac{1}{R^2} = \frac{4C}{L}$, the system is critically damped. The particular solution of Equation 5.1 with the given arbitrary initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$ is

$$E(t) = e^{-\alpha t}\{E_0 + (e_0 + \alpha E_0)t\} \tag{5.5}$$

The circuit response is not oscillatory in this case, but depending on the values of the initial conditions, it may assume one peak (local minimum

or local maximum) after $t = 0$. If R is positive, the circuit will dissipate the energy remaining from the initial conditions, and the voltage across the circuit will approach zero when t is approaching ∞. If R is negative, the unbalance originating from the initial conditions is amplified, and the response is unbounded. Depending on the values of the initial conditions, the response may assume one local minimum or maximum after $t = 0$. With large values of t, the response is monotonic, approaching either zero (if $R > 0$) or either ∞ or $-\infty$ (if $R < 0$).

Finally, if $\frac{1}{R^2} > \frac{4C}{L}$, the system is overdamped. The particular solution of Equation 5.1 with the initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$ can be written as

$$E(t) = C_1 e^{(-\alpha+\omega)t} + C_2 e^{(-\alpha-\omega)t} \tag{5.6}$$

where

$$C_1 = E_0 + \frac{1}{2\omega}[E_0(\alpha - \omega) + e_0] \tag{5.7}$$

$$C_2 = -\frac{1}{2\omega}[E_0(\alpha - \omega) + e_0] \tag{5.8}$$

$$\omega = \frac{1}{2C}\sqrt{\frac{1}{R^2} - \frac{4C}{L}} \tag{5.9}$$

Since the exponents in Equation 5.6 are real, no ringing will occur. As in the critically damped case, the response may assume one local minimum or maximum after $t = 0$, but after this the response will decrease or increase monotonically. As in the critically damped case, $\lim_{t\to\infty} E(t) = 0$ when $R > 0$. When $R < 0$, the final value depends on the initial conditions, either $\lim_{t\to\infty} E(t) = \infty$ or $\lim_{t\to\infty} E(t) = -\infty$.

As a special limiting case, when $R = \infty$ or $R = -\infty$, Equation 5.1 is simplified to

$$C\ddot{E} + \frac{1}{L}E = 0 \tag{5.10}$$

The particular solution with the initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$ is

$$E(t) = E_0 \cos \omega_0 t + \frac{e_0}{\omega_0} \sin \omega_0 t \tag{5.11}$$

where

$$\omega_0 = \sqrt{\frac{1}{2LC}} \tag{5.12}$$

The response in this case is a pure sinusoidal signal, whose amplitude and phase depend on the initial conditions.

The equations for the critically damped case and for the condition $1/R = 0$ are physically less interesting, since they represent only boudries between two (more usual) conditions. However, it is later shown that in practical oscillator circuits the coefficient of $\dot{E}$ must change signs at least twice during the steady-state oscillation cycle. Therefore, when the voltage dependence of $1/R$ is taken into account, the oscillator operating conditions will frequently cross this boundry. Similarly, very small variations of $C(E)$ and $R(E)$ may change the system from underdamped to overdamped. Since the numerical precision of simulator programs will limit the accuracy of the calculated response, the critically damped system and the condition $1/R = 0$ will frequently appear in simulations, and Equations 5.5 and 5.11 will sometimes give the best possible approximation of the signal waveform at the current operating condition. For these reasons, Equations 5.5 and 5.11 should be treated in simulator programs as possible responses.

Equations 5.2, 5.5, 5.6, and 5.11 describe the tank circuit response for all meaningful initial conditions and parameter values in the following discussion. In the LC tank oscillator circuits that are studied in this work, the capacitance or the inductance will not assume negative values. However, the gain transistors of the oscillator will make R negative for short time intervals. Of course, no physical system is able to maintain the condition $-\infty < R < 0$ for a long time, since the response is unbounded in this case. However, this condition occurs during every every oscillation cycle in a tank circuit oscillator, when the gain transistors operate in the high-gain region.

5.2 LC Oscillator Steady-state Voltage Waveform

In practical LC oscillator circuits, the value of the inductance does not depend on the signal voltage, if a passive inductor is employed. However, the

tank circuit capacitance C is a function of the instantaneous signal voltage, since the parasitic capacitances of the gain transistors and the capacitance of the varactor are voltage dependent. In addition, the loss term $1/R$ depends on the instantaneous signal voltage in all practical oscillator circuits. When the signal amplitude is low, the gain of the circuit must be high (the loss term $1/R$ must be negative) in order to prevent the oscillator from stopping. The signal amplitude will grow, until some mechanism starts to limit the gain at the peaks of the voltage waveform. If there is no limiter or automatic gain control in the circuit, the the available supply voltage will eventually limit the amplitude. When limiting occurs, the loss term $1/R$ becomes positive during the voltage peaks, and some energy is dissipated during this part of the cycle. After the oscillator has started up, the circuit will automatically find the operating conditions, where the amplitude remains constant. In this steady state, the energy that is dissipated during the parts of the cycle where $1/R$ is positive, is exactly compensated for during the parts of the cycle where $1/R$ is negative. Obviously, when the oscillator is working in the steady state, the loss term $1/R$ assumes both positive and negative values during the cycle.

The voltage-dependent capacitance and loss term will affect the shape and the period of the steady-state voltage waveform. The resulting harmonic frequency components in the output waveform are usually not a problem, since the buffer stage will distort the waveform anyway. However, changes in these parameters will affect the steady-state oscillating frequency.

5.3 Simulating The LC Oscillator Steady State

For modeling the steady-state LC oscillator circuit behavior, it is necessary to take into account the significant voltage-dependent parameters. An equation that models the dynamic behavior of a physical oscillator circuit should at least include the voltage-dependent capacitance and loss terms. A second-order differential equation that takes into account these effects is

$$C(E)\ddot{E} + \frac{1}{R(E)}\dot{E} + \frac{1}{L}E = 0 \tag{5.13}$$

where $C(E)$ and $R(E)$ are the voltage dependent capacitance and resistance, respectively. Since the coefficients of $\ddot{E}(t)$ and $\dot{E}(t)$ are not constant, solving Equation 5.13 is more difficult than finding the solution of the linear homogenious second-order differential equation discussed in section 5.1. If

the analytical expressions for $C(E(t))$ and $R(E(t))$ are known, it is possible to find the solution in many cases. However, it may be impossible to find the analytical solution for some $C(E)$ and $R(E)$, and the most efficient method for finding the solution will anyway depend on which class of functions $C(E(t))$ and $R(E(t))$ include. In order to avoid actually finding an analytical expression for the solution of Equation 5.13, we can approximate the steady-state waveform piecewise using the simple expessions of Section 5.1, and taking into account the changing values of $C(E(t))$ and $R(E(t))$ between each segment.

In practical LC oscillator circuits, the oscillation frequency is approximately known, since the oscillator is designed to oscillate at some given frequency range. Therefore, we can choose an initial time step τ that is much shorter than the estimated oscillation period T_{app}. We choose $\tau = T_{app}/M$, where M is a large integer. We mark the first simulation point with τ_0, and label the time axis with τ_0, τ_1, τ_2, ..., τ_n, τ_{n+1}, ..., as is shown in Figure 5.2. The simulation is started with an arbitary initial guess $E(\tau_0) = E_{init} > 0$, and we set $\dot{E}(\tau_0) = 0$. With these initial conditions, we know that $E(\tau_0)$ represents a local maximum.

Since the time step is small, the values of $C(E)$ and $R(E)$ will not change much during one time step. Therefore, we can assume that they remain

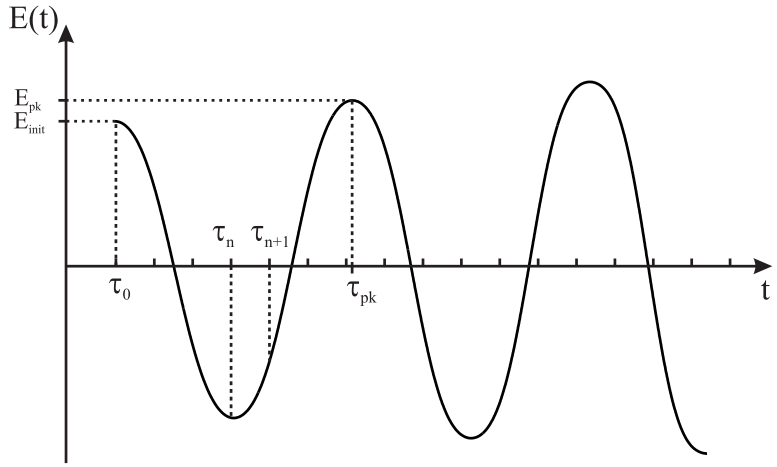


Figure 5.2: *The simulated waveform before the steady-state condition is found. The waveform of $E(t)$ is divided into short segments of length τ, starting from a local maximum of the waveform. The following local maximum $E(t) = E_{pk}$ is searched, and the optimization algorithm must minimize $|E_{pk} - E_{init}|$.*

constant during the current time step, and approximate the response by using the particular solutions of Equation 5.1 that were discussed in Section 5.1. Once the response of segment starting at τ_n is calculated, the values of $E(\tau_{n+1})$ and $\dot{E}(\tau_{n+1})$ are known. These are the initial conditions for calculating the next segment. The values of $C(E)$ and $R(E)$ are updated before the next segment is calculated, based on the current value of $E(t)$ and the $C(E)$ and $R(E)$ data. Before simulating a new segment, we check if the updated set of parameters corresponds to the underdamped, critically damped, or overdamped response, and the correct equation among Equations 5.2, 5.5, 5.6, and 5.11 for simulating the next segment is chosen. The simulation continues until the first local maximum of $E(t) = E(\tau_{pk})$ is found.

Since the initial guess $E(\tau_0)$ was chosen arbitrarly, it is likely that the value of $E(\tau_0) \neq E(\tau_{pk})$. This indicates that the initial conditions did not correspond to the steady-state operation. Since we know that the steady-state solution is periodic, we can resimulate the circuit with different values of $E(\tau_0)$ and search the initial condition that will minimize $|E(\tau_{pk}) - E(\tau_0)|$. Since there is only one variable in the goal function of the search algorithm and since the goal function with any physical set of parameters has only one minimum, most simple optimization algorithms will easily find this condition.

It is possible to improve the speed and the accuracy of the search algorithm

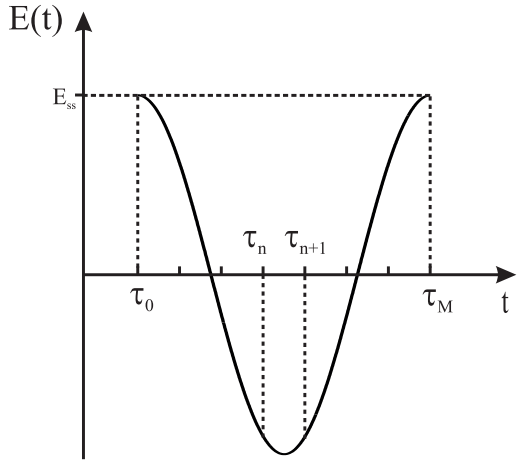


Figure 5.3: *One period of the simulated waveform after the steady state is found. The local maxima are equal, and the period of the signal is an integer multiple of the time step.*

by optimizing the time step during the search. The time step was not initially synchronized with the simulated waveform, but is possible to redefine the time step between each simulation round. After each simulation round we have a new approximation for the oscillation period $T = \tau_{pk} - \tau_0$, and for the next simulation we can use the time step $\tau = T/M$. To speed up the search, a relatively coarse time step may be chosen for the first iterations (for example $M = 100$), in order to find quickly a good initial guess for the following optimization steps.

5.4 Simulation Example

Appendix B shows a Matlab code listing that demonstrates finding the steady-state voltage waveform of an LC oscillator using the method described in Section 5.3. The voltage dependent gain and capacitance data that was used for plotting the example plots is shown in Figure 5.4. The code employs spline interpolation for approximating the values of $C(E)$ and $C(E)$ between the sample points.

In order to demonstrate the method and to verify that the steady-state oscillation period depends on the shapes of the $C(E)$ and $R(E)$ curves, two simulations were run, using slightly different $R(E)$ curves. The results in each case are shown in Table 5.1. The oscillation frequency ω and the Fourier series coefficients are extracted from the simulated steady-state waveform by fitting the truncated Fourier series

$$s(t) = A_0 + \sum_{n=1}^{7} A_n \cos(n\omega t + \Phi_n) \tag{5.14}$$

to the waveform. Finding the Fourier coefficients by fitting rather than using the discrate Fourier transform is a good method in this case, since the period of the final waveform is not necessarily a multiple of the time step.

5.5 Other Methods for Simulating LC Oscillators

Compared with more traditional methods for simulating oscillator circuits, the proposed method has some advantages. Simulating oscillator circuits in Spice simulators in the transient simulation mode is inefficient, since the simulator must simulate until the amplitude level has reached the steady

state with the desired accuracy. Since the simulation time step must be very short and the simulation accuracy must be high, the transient simulations are time consuming and produce large data files. In many simulators it is possible to find faster the final state by storing the final state of a long simulation, and using it as the initial condition for the next simulations. However, for each new set of circuit parameters it is necessary to find

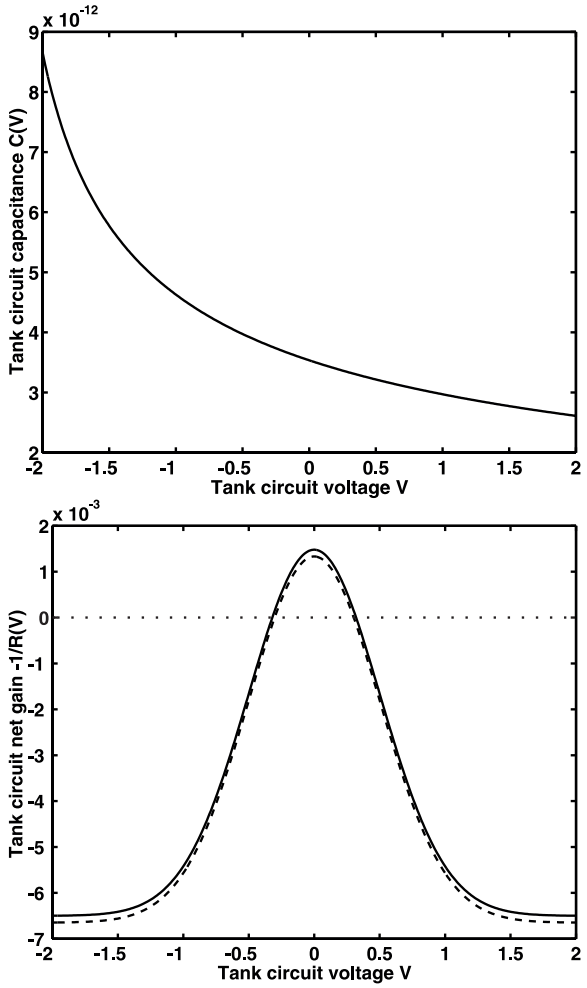


Figure 5.4: *The $C(E)$ and $1/R(E)$ data used in the two example simulations. The same capacitance curve was used in both simulations, but the $1/R(E)$ curve was slightly different . The peak gain in curve A (solid line) is slightly higher than the peak gain in curve B (dashed line).*

Table 5.1: *The steady-state oscillation frequency, the DC component, and the seven first Fourier components extracted from the steady-state waveforms in the two example cases A and B. The oscillation frequency and the level of harmonic components are slightly different in the two cases. In addition to the small differences arising from the numerical precision of the search algorithms, the only difference between the two simulations is the shape of the* $1/R(E)$ *curve.*

	A		B	
F0:	2.19534 GHz		2.17886 GHz	
DC:	0.015 V	-	0.011 V	-
HD1:	0.000 dBc	-0.2^o	0.000 dBc	-0.1^o
HD2:	-35.325 dBc	-0.8^o	-36.740 dBc	-0.0^o
HD3:	-35.973 dBc	11.9^o	-36.278 dBc	11.5^o
HD4:	-50.909 dBc	0.9^o	-52.097 dBc	0.8^o
HD5:	-67.205 dBc	-1.2^o	-68.905 dBc	-2.8^o
HD6:	-81.763 dBc	-15.4^o	-85.522 dBc	-18.7^o
HD7:	-102.119 dBc	-77.4^o	-104.864 dBc	87.6^o

the new steady state by simulating so long that the transient response has completely vanished. Therefore, exploring the parameter space by varying the shapes of $C(V)$ and $R(V)$ curves and resimulating the circuit is very time consuming with traditional analog circuit simulators. The proposed method is searching directly the steady-state solution, which is obtained with relatively little computing power. Some iteration is necessary, since it is necessary to search the solution that matches $E(\tau_M)$ and $\dot{E}(\tau_M)$ with $E(\tau_0)$ and $\dot{E}(\tau_0)$. However, since there is only one degree of freedom and since the goal function has in practice only one clearly defined local minimum, any known search algorithm will converge.

Present-day software tools for behavioral modeling of analog circuits would handle the problem more efficiently than Spice simulators, but they are still specialized and expensive tools that often do not run in a desktop computer. However, it is relatively easy to implement the proposed method with relatively cheap personal computer programming tools that are intented for solving mathematical problems.

5.6 Conclusions

The proposed method for simulating the steady-state voltage waveform is suitable for studying any LC tank circuit oscillator where the tank circuit capacitance and gain depend on the instantaneous signal voltage. It is not necessary to know the analytical expressions for the voltage-dependent parameters. Since the $C(V)$ and $R(V)$ data may be read from a data file, there are no limitations on how the data is generated, and how complicated the functions $C(V)$ and $R(V)$ are. Measurement results, simulation results from analog simulators, or analytic expressions may be used for the $C(V)$ and $R(V)$ data, and for studying the oscillator behavior, the data may be manipulated with other tools, such like a spreadsheet program.

The presented method has some limitations. It assumes that $C(V)$ and $R(V)$ are only functions of the instantaneous signal voltage, which means that the method is not able to take into account non-quasi-static effects. Therefore, care should be taken in interpreting the results if the oscillator is operating close to the transition frequency of the active devices. In addition, it should be taken care that the termination tolerance of the search algorithms is acceptable. Otherwise, the steady-state solution will include properties that arise from the numerical search method, rather than physical properties of the oscillator.

Chapter 6

Voltage Dependent Capacitances

This chapter presents simple piecewise sinusoidal models for analyzing the effects of voltage dependent capacitances in LC tank tuned oscilator circuits. If the tank circuit includes voltage dependent capacitances, the steady state voltage signal waveform of the oscillator will be non-sinusoidal, and the period of the signal will depend on the signal amplitude. The state-of-the-art analog circuit simulator programs are able to predict these effects at least to some extent, if correct capacitance models are used for the simulations. However, constructing a circuit diagram that actually models well the physical circuit and interpreting the results of the simulations is difficult, if the mechanisms behind the amplitude dependent oscillating frequency are not well understood. The model presented here explains why voltage dependent capacitances change the operating frequency of the oscillator, and shows how the polarity of the voltage dependent capacitors and the DC component of the distorted oscillator signal are related to the oscillating frequency.

The modeling approach described in this chapter is intended to give qualitative insight into the effects of the varying signal amplitude on the signal waveform and the oscillation frequency, when the tank circuit of an LC oscillator includes voltage dependent capacitances. Once the circuit has a simple model that describes the most essential effects, it will be easier to inerpret the results from simulations that employ physical device models. The model presented in this chapter employs a very simple model for the voltage dependent capacitor. The capacitance is assumed to change stepwise when the voltage across the capacitor crosses a known threshold value. This assumption allows us to model the tank circuit voltage with

segments of sinusoidal waveforms. This makes the analysis of the waveform simple, and allows us to make some conclusions about the sensitivity of the oscillating frequency to the signal amplitude.

Throughout this chapter it is assumed that the loaded Q value of the tank circuit is high and that it is possible to control the amplitude of the oscillation without detoriating the loaded Q significantly. It is also assumed that the inductor and the capacitors are the only significant sources of phase shift in the circuit. Time constants that rise for example from the redistribution delays of charge carriers in the transistors or capacitors, are ignored.

The effect of the voltage dependent capacitance in the tank circuit is that the factor $\sqrt{LC}$ will depend on the instantaneous signal voltage, which will make the voltage waveform across the tank circuit non-sinusoidal. In addition to introducing harmonic frequency components, this will make the period of the waveform dependent on the signal amplitude. Despite of the simple model for the voltage dependent capacitance, the analysis in this chapter is able to explain how the oscillation period depends on the signal amplitude when voltage dependent capacitances are present. It also shows that if the tank circuit includes several voltage dependent capacitances, they sometimes may be made to cancel each other's effect on the oscillation period, if the signal amplitude can be controlled.

Section 6.1 describes the effects of voltage dependent capcitances in the tank circuit, based on qualitative observations. Sixteen different regions in the parameter space, where voltage dependent capacitances make the oscillation frequency amplitude dependent, are found. Out of these, four different subspaces, where the effects of voltage dependent capacitances on the oscillation period may cancel out, are identified. Section 6.2 clarifies the definition of some of the parameters, and Section 6.3 derives some mathematical relationships between the oscillation period, the signal amplitude, and the parameters associated with the voltage dependent capcitances. Some interesting limiting cases between the regions of the parameter space are discussed in Section 6.5. Finally, the conclusions are presented in Section 6.7.

6.1 Piecewise Sinusoidal Waveform Model

The steady state waveform of the oscillator is approximated in this chapter with a piecewise defined function, where each piece is a segment of a sinusoidal waveform. For this purpose, voltage dependent capacitances are assumed to change stepwise from one value to another, when the voltage

across the capacitor crosses a threshold voltage. At first sight, the stepwise varying capcitor seems to be a poor approximation for the smoothly varying physical voltage dependent capacitances encountered in most physical circuits. Nevertheless, it results in a model that explains the most essential effects of the voltage dependent capacitances in the LC oscillator tank circuit. Despite of the inaccurate nature of the model, it will help in understanding the reasons of the AM-to-FM conversion in the oscillator cirucit.

The oscillator circuit usually includes several different physical voltage dependent mechanisms that simultaneously modify the tank circuit capacitance. For analysis purposes, the mechanisms that contribute to the same direction, may be described with one monotonic voltage dependent capacitance that models the contributions from these mechanisms. If some mechanisms counteract the others, two capacitors with opposing voltage dependencies should be included, in order to model the possible cancellation. For these reasons, the modeling approach presented here employs two voltage dependent capacitances, and is focused on the cases where the cancellation actually may take place.

The circuit diagram of the tank circuit model, that includes voltage dependent capacitances, is shown in Figure 6.1. The total capacitance of the tank circuit is $C_{tank}(V) = C_1(V) + C_2(V)$. We now define a threshold voltage for each capacitor, V_1 for C_1 and V_2 for C_2. These threshold voltages may be either positive or negative but not zero, and their absolute values are assumed to be unequal. Without losing generality, we can set $0 < |V_1| < |V_2|$. Since the two tank circuit capacitors are connected in parallel, it is a matter of definition to call the capacitor with the smaller threshold voltage magnitude as C_1. When the capacitors are named this way, it is not necessary to study the parameter space regions where $|V_1| > |V_2|$. For analyzing the rare special cases, where $|V_1| > |V_2|$, the capacitor names can be interchanged before the analysis. The cases where $|V_1| = |V_2|$ or where at least one of the threshold voltages is zero are special cases that will be discussed separately in Section 6.5.

We can first define $C_{tank}(0) = C_1(0) + C_2(0) \mathrel{\widehat{=}} C_0$, which just states that the total tank circuit capacitance is known at $V = 0\ V$. When the voltage across the tank circuit deviates from zero, moves towards V_1, and crosses it, the capacitance of C_1 will abruptly change to some other value. Therefore, the total tank circuit capacitance will change to $C_{tank}(V_1) = \alpha \cdot C_0$, where α is a positive and real coefficient. When V is then moved towards V_2 and crosses V_2 (independent of if it had to cross V_1 another time), the capacitance of C_2 will change to some other value. Therefore, the total tank circuit capacitance will change to $C_{tank}(V_2) = \beta \cdot C_0$, where β is another positive and real coefficient.

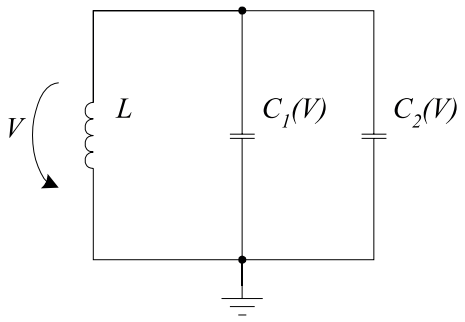


Figure 6.1: *The model for a tank circuit including two counteracting voltage dependent capacitances.*

The parameters α and β indicate how much and to which direction the total tank circuit capacitance deviates from C_0 when V crosses V_1 or V_2. Since the relative change of the total tank circuit capacitance will be the key factor in the following discussion, it is practical to define these parameters in the way that they directly express the relative changes of C_{tank}, rather than the changes of C_1 and C_2 [1].

The four parameters α, β, V_1, and V_2 control the waveform of the piecewise sinusoidal function, when the signal amplitude is changing. To get started with the analysis, it is useful to divide the parameter space in different subspaces, for identifyig the regions where the two voltage dependent capacitances have opposing effects on the oscillating frequency. The interesting two ranges of values that α may assume are $0 < \alpha < 1$ and $\alpha > 1$, since $\alpha = 1$ corresponds to the case where C_1 is not voltage dependent. Therefore, the values of α divide the parameter space in two regions. The value of β must be compared with α, since the ratio α/β will determine to which direction the frequency will change once the circuit is oscillating and A exceeds $|V_2|$. Therefore, the values of β divide the parameter space once more in two regions: $\beta \leq \alpha$ and $\beta \geq \alpha$ (since it is not yet clear if we can ignore the case $\beta = \alpha$, it is included here). It will be possible to choose the signs of V_1 and V_2 in four different ways, which will divide the parameter space two more times by two. Since each of the four parameters divide the parameter space in two regions, the complete parameter space has $2^4 = 16$ different regions where the oscillator waveform is expected to depend on the signal amplitude A. These regions are shown in Figure 6.2.

Since we in the following discussion are interested in the cases where the

[1] Once the nominal values of C_1 and C_2 and their relative changes by the threshold voltage crossings are known, it will be easy to calculate α and β, as is shown in Section 6.2.

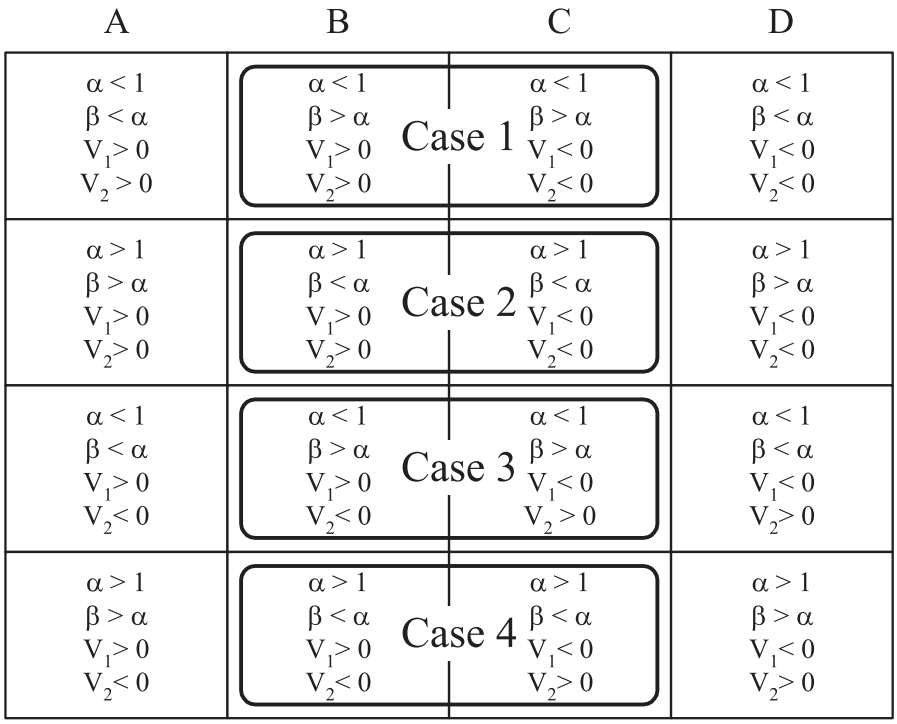


Figure 6.2: *The sixteen regions of the parameter space. The diagram has symmetry about the vertical center line: moving inside the same row from column A to D or from column B to C inverts the signs of V_1 and V_2, which is equivalent to changing the polarity of the signal waveform.*

effects of the two voltage dependent capacitors might cancel out, C_1 and C_2 should have opposing effects on the tank circuit capacitance. This makes the regions where $1 < \alpha \leq \beta$ and $\beta \leq \alpha < 1$ uninteresting. In addition, since in the following analysis it does not matter if the whole signal waveform is turned upside down, the polarity of $V(t)$ is irrelevant. Therefore, instead of analyzing all four combinations of signs of V_1 and V_2, it will be sufficient to study the cases where the signs are equal and where they are unequal, that is, $V_1 \cdot V_2 > 0$ and $V_1 \cdot V_2 < 0$.

Considering these parameter definitions and constraints, we obtain four different subspaces in the parameter space where the effect of the voltage dependent capacitances on the oscillation period may result in complete cancellation, when the signal amplitude A is varied. To simplify the discussion, we name these subspaces as Case 1, Case 2, Case 3, and Case 4, as is shown in Figure 6.2. Each of these cases is now discussed separately.

6.1.1 Case 1: $V_1 \cdot V_2 > 0$, $\alpha < 1$ and $\beta > \alpha$

In this case, the capacitor threshold voltages are either both positive or both negative. It is assumed here that $V_1 < 0$ and $V_2 < 0$, to make the discussion easier. When the voltage across the tank circuit is $V > V_1$, the tank circuit capacitance is $C_{tank}(V) = C_0$. When $V_2 < V < V_1$, the tank circuit capacitance is $C_{tank}(V) = \alpha \cdot C_0$, and when $V < V_2$, the capacitance is $C_{tank}(V) = \beta \cdot C_0$.

We now start up the oscillator and control the steady state amplitude A for example by adjusting the gain of the non-linear amplifier stage. When the amplitude of the waveform is smaller than $|V_1|$, the capacitance of the tank circuit is independent of the voltage: $C_{tank}(V) = C_0$. Therefore, the tank circuit voltage waveform is sinusoidal and the period of the waveform is $T = 2\pi\sqrt{LC_0}$. Since the positive and negative half cycles are half wave symmetrical, the DC component of the waveform is zero. An example of the signal waveform in this case is shown in Figure 6.3. With the given set of parameters, the waveform period[2] is $T = 4.17 \cdot 10^{-10}$ s.

If we now increase the amplitude, the negative peaks of the waveform will eventually cross the threshold level V_1. Since C_1 will temporarily decrease, the factor $\sqrt{LC}$ will decrease from $\sqrt{LC_0}$ to $\sqrt{\alpha \cdot LC_0}$ for the time when the signal voltage is below V_1. This will make the circuit to complete the cycle slightly faster than in the previous case, which means that the frequency of the signal has now increased. The the area limited by the negative half cycle and the t-axis is now slightly smaller than the area between the positive half cycle and the t-axis, which makes the DC component of the waveform positive. The magnitude of this DC component will increase rapidly if the amplitude of the signal is increasing: even if the waveform shape would not change, the difference between the areas limited by the two half cycles would grow. Since the waveform becomes more unsymmetrical when the amplitude is increasing, the DC component will grow faster than proportional to the amplitude. An example of the signal waveform in this case is shown in Figure 6.4. The period is now $T = 3.6 \cdot 10^{-10}$ s. Obviously, the length of the time that the signal spends below V_1 depends on the amplitude of the signal. If A is just slightly larger than $|V_1|$, only a small fraction of the complete cycle is accelerated. Consequently, the increase in the frequency and the magnitude of the DC component will be small. If the amplitude is increased, the signal will spend a larger fraction of the cycle below V_1, and the resulting DC component and increase in the frequency will be larger.

[2]The period in the example cases is calculated using the method that is described in Appendix C.

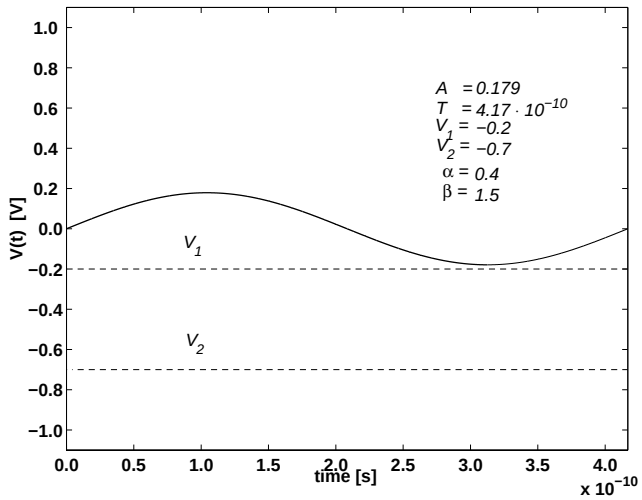


Figure 6.3: *One cycle of the steady state voltage signal waveform, when the signal amplitude does not exceed* $|V_1|$ *(Case 1). Since the tank circuit capacitance remains constant throughout the cycle, the waveform remains undistorted.*

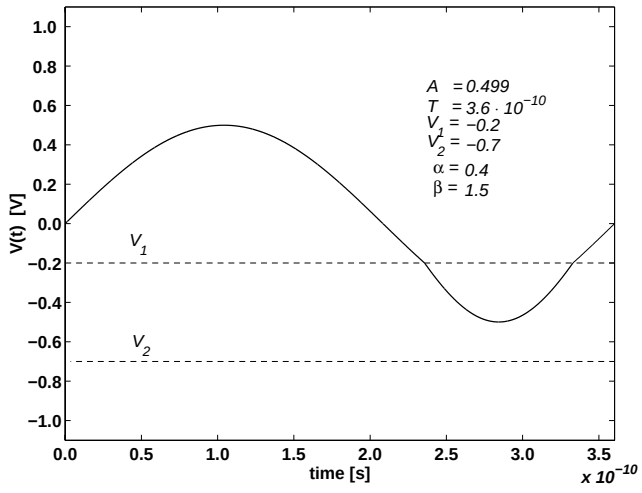


Figure 6.4: *When the signal amplitude is larger than* $|V_1|$*, the negative peak of the waveform will cross the threshold* V_1 *(Case 1). When the voltage remains below* V_1 *the tank circuit capacitance will decrease to* $\alpha \cdot C_0$*. This will speed up the part of the cycle where* $V_2 < V(t) < V_1$*.*

Finally, if we still increase the amplitude, the negative peaks of the signal will eventually cross V_2, as is shown in Figure 6.5. Since the capacitance of C_2 increases abruptly when the signal voltage enters the region where $V(t) < V_2$, the factor $\sqrt{LC}$ will increase from $\sqrt{\alpha \cdot LC_0}$ to $\sqrt{\beta \cdot LC_0}$. Consequently, the signal will complete this part of the cycle slower, making the negative half period longer. The oscillation period of the example oscillator has now increased to $T = 3.82 \cdot 10^{-10}$ s. The area limited by the negative half cycle and the t-axis is now approaching the corresponding area of the positive half cycle, since the increased value of C_2, when $V(t) < |V_2|$, tends to make the negative half cycle wider. Consequently, the magnitude of the DC component starts now to decrease rapidly, when the amplitude is increasing.

The voltage dependencies of C_1 and C_2 (parameters α and β) were chosen in the way that they tend to cancel each other's effects on the oscillation period, when the signal amplitude A is larger than $|V_2|$. Figure 6.6 shows the oscillator waveform when the amplitude is much larger than $|V_2|$. Since the period $T = 4.18 \cdot 10^{-10}$ s is now approximately the same as in Figure 6.3, where the signal was undistorted, we can conclude that the two voltage dependent capacitances now cancel out each other's effects on the length of the oscillation period. The area limited by the negative half cycle and

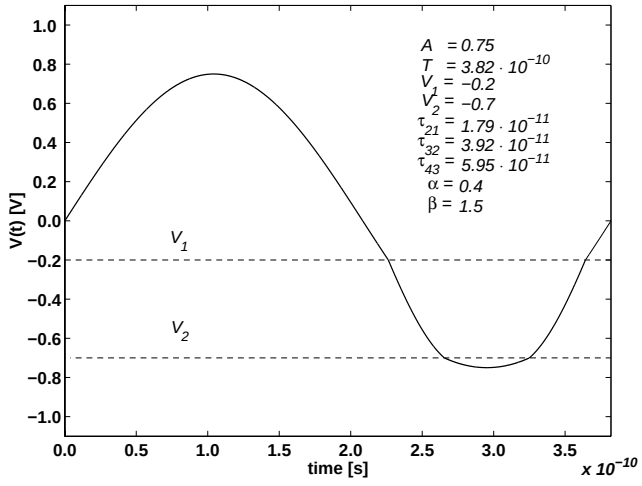


Figure 6.5: *When the signal amplitude exceeds $|V_2|$, the negative peak will also cross the threshold V_2 (Case 1). Since $\beta > 1$, the oscillator will slow down when $V(t) < V_2$.*

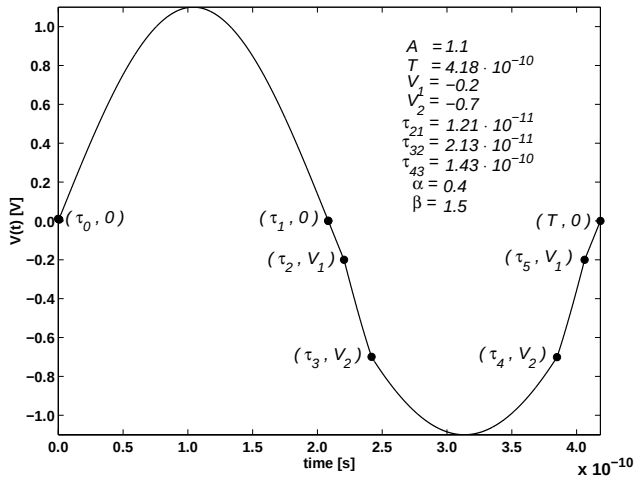


Figure 6.6: *One complete cycle of $V(t)$ in Case 1. The amplitude $A \gg |V_2|$ and the voltage dependent capacitances distort only the negative part of the waveform. When the signal amplitude is much larger than $|V_2|$, the part of the cycle where $V(t) < V_2$ will cover most of the negative half of the cycle.*

the t-axis is now clearly larger than the corresponding area under the positive half cycle, which indicates that the DC component of the waveform is now negative. Increasing the amplitude further would still decrease the frequency and make the DC component more negative, since the part of the cycle where C_2 slows down the circuit would increase, while the two narrow regions, where C_1 speeds up the cycle, would further shrink.

It appears that if we first operate the oscillator with $A \ll |V_1|$ and then increase the amplitude until $A \gg |V_2|$, the operating frequency will first remain constant, then increase, and finally start to decrease. The frequency may decrease back to the original frequency and even further down, depending on the values of the parameters α, β, V_1, and V_2. Correspondingly, the DC component of the waveform will first remain zero, then become positive, reach the maximum, start to decrease, and finally may even become negative. Obviously, there must be some amplitude level at which the frequency-versus-amplitude curve reaches the maximum. The slope of this curve will be zero at this amplitude level, which means that a small change in the amplitude would not change the steady state oscillation frequency, or that the AM-to-FM conversion of the circuit is zero.

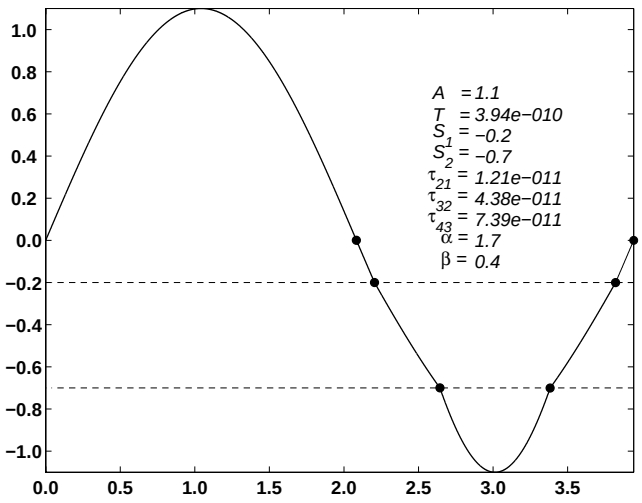


Figure 6.7: *One complete cycle of* $V(t)$ *when* $\alpha > 1$, $\beta < \alpha$, *and* $V_1 \cdot V_2 > 0$ *(Case 2). The signal amplitude is* $A > |V_2|$. *As in Case 1, the voltage dependent capacitances distort only one side of the waveform.*

6.1.2 Case 2: $V_1 \cdot V_2 > 0$, $\alpha > 1$ and $\beta < \alpha$

This case is similar to the previous one in the sense that only one side of the waveform is distorted, when the signal amplitude $A > |V_2|$. As before, we set $V_1 < 0$ and $V_2 < 0$ for the example. When the signal amplitude A increases from $|V_1|$ to $|V_2|$, the period T will now increase and the DC component will become negative, since $\alpha > 1$ and V_1 is negative. When the amplitude is still increasing and the peaks of the signal cross V_2, the period length and the magnitude of the DC component start to decrease. In this case, when the signal amplitude is varied starting from very low level and then increased until $A >> |V_2|$, the operating frequency will first stay constant, then decrease, reach the minimum, and finally start to increase when A exceeds $|V_2|$. The DC component will first remain zero, then become negative, start to increase again, and may even become positive. Clearly, there must exist a minimum in the frequency-vs-amplitude curve at some amplitude level, where the AM-to-FM conversion of the circuit will be very low. An example of the signal waveform in this case with $A > |V_2|$ is shown in Figure 6.7.

6.1.3 Case 3: $V_1 \cdot V_2 < 0$, $\alpha < 1$ and $\beta > \alpha$

This case is different from the previous cases, since one of the threshold voltages is negative while the other one is positive. Therefore, both sides of the waveform will be distorted when the signal amplitude is large. For the example, we choose $V_1 > 0$ and $V_2 < 0$. When $A < |V_1|$, the waveform will be sinusoidal, since neither of the threshold voltages is crossed during the cycle. When $|V_1| < A < |V_2|$, the positive half of the waveform will cross V_1 and will be distorted, while the negative side will remain intact. Since $\alpha < 1$, the positive half cycle will run faster when $V > V_1$. The period length T will decrease, like in Case 1, but the DC component will become negative since it is now the positive half cycle that is getting narrow, compared to the negative half.

When $A > |V_2|$, the situation is quite different from Cases 1 and 2, since both halves of the signal are now distorted. An example of the waveform in this case is shown in Figure 6.8. The positive half cycle accelerates when $V > V_1$, and the negative half cycle slows down when $V < V_2$. Clearly, if β is very large compared to α, the part of the cycle where $V < V_2$ will start to increase the period length when A exceeds $|V_2|$. However, if β

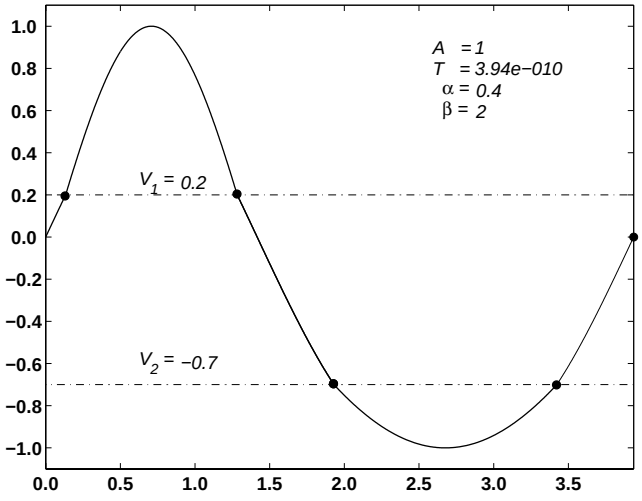


Figure 6.8: *One complete cycle of the oscillator signal waveform when $\alpha < 1$, $\beta > \alpha$, and $V_1 \cdot V_2 < 0$ (Case 3). The signal amplitude $A > |V_2|$. The voltage dependent capacitances distort both positive and negative halves of the cycle.*

is not much larger than α, it is not clear how the period T will change when the amplitude exceeds $|V_2|$. When the amplitude is increasing, the accelerated part of the positive half cycle will cover a larger part of the cycle, but on the other hand, the same thing will happen to the slow part of the negative half cycle. We can conclude that at least if $\beta \gg \alpha$, the frequency-vs-amplitude curve will first remain constant, then increase, reach the maximum, and finally decrease, when the amplitude is varied from $A \ll |V_1|$ to $A \gg |V_2|$. Considering the period length sensitivity to the amplitude, Case 3 seems to be much like Case 1. The DC component of the waveform becomes negative when A exceeds $|V_1|$, and its magnitude will grow rapidly as the amplitude is increasing up to $|V_2|$. However, since in Case 3 one of the voltage dependent capacitors makes one half of the cycle longer while the other capacitor makes the other half shorter, the magnitude of the DC component will continue to grow when the amplitude exceeds $|V_2|$, unlike in Cases 1 and 2.

6.1.4 Case 4: $V_1 \cdot V_2 < 0$, $\alpha > 1$ and $\beta < \alpha$

The difference between Cases 3 and 4 is the relative values of α and β. Since now $\alpha > 1$ the period length will increase when the amplitude hits the region $|V_1| < A < |V_2|$. When A exceeds $|V_2|$, the period will start to decrease, at least if $\beta \ll \alpha$. The magintude of the DC component will be zero as long as $A < |V_1|$. When the amplitude is increasing from $|V_1|$ to $|V_2|$, the DC component will become positive and increase rapidly, and it will continue to increase when A exceeds $|V_2|$.

6.2 Parameters α and β

The parameters α and β express the relative change of the total tank circuit capacitance from $C_{tank}(0)$ to $C_{tank}(V_1)$ and $C_{tank}(V_2)$. Since the relative changes of capacitances C_1 and C_2 are usually the parameters that are available for the analysis, we need to calculate α and β from this information. We can define the nominal values of the capacitors $C_1(V)$ and $C_2(V)$ at $V = 0$ V as

$$C_1(0) \mathrel{\widehat{=}} C_{10}$$
$$C_2(0) \mathrel{\widehat{=}} C_{20}$$

When the voltage across the tank circuit is zero, the total tank circuit capacitance is $C_{tank}(0) \widehat{=} C_0 = C_{10} + C_{20}$. When the voltage across one of the capacitors crosses the threshold voltage associated with this capacitor, we assume that the capacitance of this capacitor changes abruptly by some amount. We can define parameters ζ and ϵ to express these relative changes:

$$C_1(V_1) \widehat{=} \zeta \cdot C_{10}$$
$$C_2(V_2) \widehat{=} \epsilon \cdot C_{20}$$

The parameter α is the relative change of the total tank circuit capacitance when the voltage across the tank circuit has crossed V_1 but not V_2. Since only the value of C_1 deviates from the nominal value, α depends only on the value of ζ. For all four cases of interest we obtain

$$\alpha \widehat{=} \frac{\zeta \cdot C_{10} + C_{20}}{C_{10} + C_{20}} \tag{6.1}$$

The definition of β depends on how $C_1(V)$ and $C_2(V)$ distort the waveform. We want β to express the relative change of the total capacitance when the voltage across the tank circuit is changed from 0 V to V_2. When $V_1 \cdot V_2 > 0$ (Cases 1 and 2), the value of C_1 has already changed from the nominal value C_{10} to $C_1(V_1) = \zeta \cdot C_{10}$ when the voltage across the tank circuit is crossing V_2. Therefore, both ζ and ϵ contribute to the value of β:

$$\beta_V \widehat{=} \frac{\zeta \cdot C_{10} + \epsilon \cdot C_{20}}{C_{10} + C_{20}} \tag{6.2}$$

If $V_1 \cdot V_2 < 0$ (Cases 3 and 4), the value of C_1 is $C_1 = C_{10}$, before and after the tank circuit voltage has crossed V_2. Therefore, the value of β depends only on the value of ϵ:

$$\beta_U \widehat{=} \frac{C_{10} + \epsilon \cdot C_{20}}{C_{10} + C_{20}} \tag{6.3}$$

Since the sign of $V_1 \cdot V_2$ will depend on the circuit topology rather than the process parameter values or the bias conditions, using these two different definitions of β does not make the analysis more complicated.

6.3 Period Length

Up to this point, the discussion on the effects of voltage dependent capacitances on the oscillator signal waveform has been based on rather qualitative arguments and observations. To get more insight, we can deduce some mathematical relationships between the period T, the signal amplitude A, and the parameters C_0, V_1, V_2, α and β. As is shown in Appendix C, the piecewise sinusoidal equation for one complete cycle of the voltage signal waveform for Cases 1 and 2 is

$$V(t) = \begin{cases} A \cdot \sin \frac{t}{\sqrt{LC_0}} & , \tau_0 \le t < \tau_1 \quad (a) \\ A \cdot \sin \frac{t-\hat{\tau_1}}{\sqrt{LC_0}} & , \tau_1 \le t < \tau_2 \quad (b) \\ A \cdot \sin \frac{t-\hat{\tau_2}}{\sqrt{\alpha \cdot LC_0}} & , \tau_2 \le t < \tau_3 \quad (c) \\ A \cdot \sin \frac{t-\hat{\tau_3}}{\sqrt{\beta_V \cdot LC_0}} & , \tau_3 \le t < \tau_4 \quad (d) \\ A \cdot \sin \frac{t-\hat{\tau_4}}{\sqrt{\alpha \cdot LC_0}} & , \tau_4 \le t < \tau_5 \quad (e) \\ A \cdot \sin \frac{t-\hat{\tau_5}}{\sqrt{LC_0}} & , \tau_5 \le t < T \quad (f) \end{cases} \tag{6.4}$$

where τ_1 ... τ_5 are moments when the signal crosses the 0 V, V_1, or V_2 levels, as shown in Figure 6.6. The time delays $\hat{\tau_1}$ ...$\hat{\tau_5}$ select the correct part of the sinusoidal waveform inside each time interval. Within each time interval, $V(t)$ is a segment of a sinusoidal waveform, whose shape is defined by the amplitude A and the argument of the square root.

Correspondingly, the piecewise sinusoidal function for modeling the waveform in Cases 3 and 4 is

$$U(t) = \begin{cases} A \cdot \sin \frac{t}{\sqrt{LC_0}} & , t_0 \le t < t_1 \quad (a) \\ A \cdot \sin \frac{t-\hat{t_1}}{\sqrt{\alpha \cdot LC_0}} & , t_1 \le t < t_2 \quad (b) \\ A \cdot \sin \frac{t-\hat{t_2}}{\sqrt{LC_0}} & , t_2 \le t < t_3 \quad (c) \\ A \cdot \sin \frac{t-\hat{t_3}}{\sqrt{LC_0}} & , t_3 \le t < t_4 \quad (d) \\ A \cdot \sin \frac{t-\hat{t_4}}{\sqrt{\beta_U \cdot LC_0}} & , t_4 \le t < t_5 \quad (e) \\ A \cdot \sin \frac{t-\hat{t_5}}{\sqrt{LC_0}} & , t_5 \le t < T \quad (f) \end{cases} \tag{6.5}$$

In Equations 6.4c–6.4e, 6.5b, and 6.5e, the argument of the square root includes α or β, which will modify the shape of the corresponding segment.

We can define the length of each piece in $V(t)$ as

$$\begin{array}{ll} \tau_{10} \mathrel{\widehat{=}} \tau_1 - \tau_0 & (a) \\ \tau_{21} \mathrel{\widehat{=}} \tau_2 - \tau_1 & (b) \\ \tau_{32} \mathrel{\widehat{=}} \tau_3 - \tau_2 & (c) \\ \tau_{43} \mathrel{\widehat{=}} \tau_4 - \tau_3 & (d) \\ \tau_{54} \mathrel{\widehat{=}} \tau_5 - \tau_4 & (e) \\ \tau_{T5} \mathrel{\widehat{=}} T - \tau_5 & (f) \end{array} \tag{6.6}$$

and the length of each piece in $U(t)$ as

$$\begin{array}{ll} t_{10} \mathrel{\widehat{=}} t_1 - t_0 & (a) \\ t_{21} \mathrel{\widehat{=}} t_2 - t_1 & (b) \\ t_{32} \mathrel{\widehat{=}} t_3 - t_2 & (c) \\ t_{43} \mathrel{\widehat{=}} t_4 - t_3 & (d) \\ t_{54} \mathrel{\widehat{=}} t_5 - t_4 & (e) \\ t_{T5} \mathrel{\widehat{=}} T - t_5 & (f) \end{array} \tag{6.7}$$

The length of the cycle for $V(t)$ is the sum of τ_{10} ... τ_{54} and τ_{T5}, and for $U(t)$ the sum of t_{10} ... t_{54} and t_{T5}. To find out the period of $V(t)$ and $U(t)$, we must first calculate τ_{10} ... τ_{54}, τ_{T5}, t_{10} ... t_{54}, and t_{T5}. Since the shape of each segment is known when the amplitude A and the parameters C_0, V_1, V_2, α, and β are given, it will be easy to calculate the t-coordinates of the points where the segments cross V_1 and V_2. As is shown in Appendix C, the period of $V(t)$, which models Cases 1 and 2, is

$$\begin{aligned} T_V = & \sqrt{LC_0} \cdot \{\pi \cdot (1 + \sqrt{\beta_V}) \\ & +2 \cdot (1 - \sqrt{\alpha}) \cdot P \\ & +2 \cdot (\sqrt{\alpha} - \sqrt{\beta_V}) \cdot Q\} \end{aligned} \tag{6.8}$$

and the period of $U(t)$, which models Cases 3 and 4, is

$$\begin{aligned} T_U = & \sqrt{LC_0} \cdot \{\pi \cdot (\sqrt{\alpha} + \sqrt{\beta_U}) \\ & +2 \cdot (1 - \sqrt{\alpha}) \cdot P \\ & +2 \cdot (1 - \sqrt{\beta_U}) \cdot Q\} \end{aligned} \tag{6.9}$$

where

$$P = \begin{cases} \arcsin \frac{|V_1|}{A} & , A > |V_1| \\ \pi/2 & , 0 < A \leq |V_1| \end{cases} \tag{6.10}$$

and

$$Q = \begin{cases} \arcsin \frac{|V_2|}{A} & , A > |V_2| \\ \pi/2 & , 0 < A \leq |V_2| \end{cases} \tag{6.11}$$

To verify that the qualitative conclusions made in Section 6.1 are correct, we can plot Equations 6.8 and 6.9 with some reasonable set of parameters.

Table 6.1: *The parameters for plotting the $T(A)$ curves in the four example cases.*

Case	C_{10}	C_{20}	L	ζ	ϵ	V_1	V_2
1	1 pF	1 pF	1 nH	0.5	2.0	-0.2 V	-0.8 V
2	1 pF	1 pF	1 nH	2.0	0.5	-0.2 V	-0.8 V
3	1 pF	1 pF	1 nH	0.5	2.0	-0.2 V	0.8 V
4	1 pF	1 pF	1 nH	2.0	0.5	-0.2 V	0.8 V

We may assume that there are two kinds of voltage dependent capacitances available for the oscillator design, and that each capacitance may vary 1:2, depending on the voltage. One of the threshold voltage values is close to the DC level of the signal, while the other one is clearly offset from the operating point level. The value of the inductor is irrelevant as long as it is the same for all examples, since it will only scale the curves in the time domain. Table 6.1 shows the chosen example parameters for the four cases of interest. With these parameters, Case 1 and Case 3 model two oscillator circuits that are similar in every sense but the polarity of C_2. The voltage across the capacitors will vary across the same region $[-A, A]$ in both circuits. The curves in Figure 6.9 show that in both cases the period length first remains constant, then decreases, reaches the minimum, and then starts to increase, as the amplitude is increasing. This corresponds to the conclusions made in Sections 6.1.1 and 6.1.3. The curves $T_V(A)$ and $T_U(A)$ in Figure 6.9 do not overlap for the part where $A > |V_2|$, even though the voltage dependent capacitors tend to cancel each other's effects on the period length in both circuits. The curves diverge when $A > |V_2|$ since in Case 1 capacitors C_1 and C_2 distort the same side of the waveform, while in Case 3 the distorting effects of the capacitors do not overlap. The resulting equations for the period lengths (Equations 6.8 and 6.9) are different.

If the amplitude is let to grow very large, the distorted part of the half cycle will alone determine the length of the corresponding half cycle. For

Cases 1 and 2, the length of the undistorted half cycle is always $\pi\sqrt{LC_0}$ and the length of the distorted half will approach $\pi\sqrt{\beta_V \cdot LC_0}$ when A is very large. Therefore,

$$\begin{aligned}\lim_{A\to\infty} T_V(A) &= \pi\sqrt{LC_0} + \pi\sqrt{\beta_V \cdot LC_0} \\ &= \pi\sqrt{LC_0} + \pi\sqrt{\frac{\zeta \cdot C_{10} + \epsilon \cdot C_{20}}{C_{10} + C_{20}} \cdot LC_0} \qquad (6.12)\end{aligned}$$

Correspondingly in Cases 3 and 4, when A is very large, the length of one of the half cycles will approach $\pi\sqrt{\alpha \cdot LC_0}$ while the other half will approach $\pi\sqrt{\beta_U \cdot LC_0}$. Therefore,

$$\begin{aligned}\lim_{A\to\infty} T_U(A) &= \pi\sqrt{\alpha \cdot LC_0} + \pi\sqrt{\beta_U \cdot LC_0} \\ &= \pi\sqrt{\frac{\zeta \cdot C_{10} + C_{20}}{C_{10} + C_{20}} LC_0} + \pi\sqrt{\frac{C_{10} + \epsilon \cdot C_{20}}{C_{10} + C_{20}} LC_0} \qquad (6.13)\end{aligned}$$

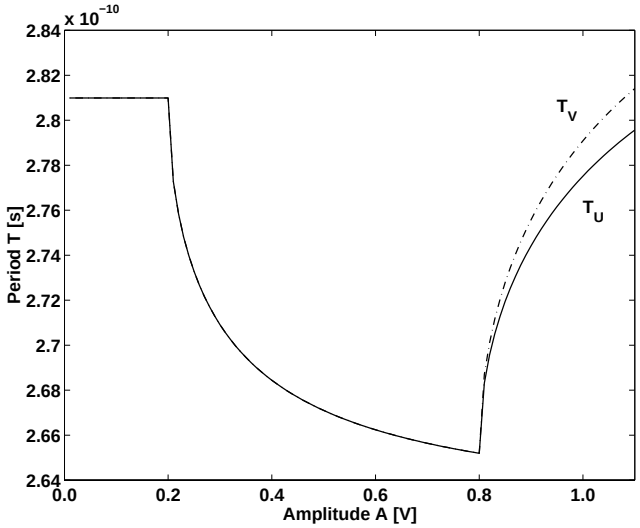


Figure 6.9: *The T-vs-amplitude curves derived from the functions $V(t)$ and $U(t)$ for Cases 1 and 3 with the given set of parameters. The signal swing about the operating point, and all other parameters but the sign of V_2, are identical in the two cases. The resulting period lengths are different when $A > 0.8\ V$.*

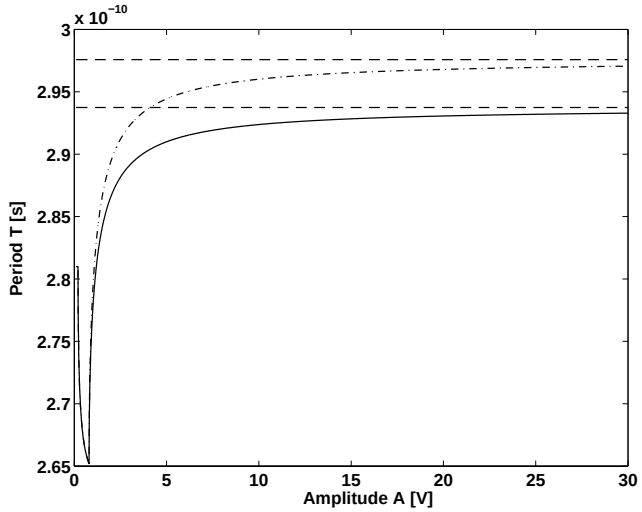


Figure 6.10: *The $T_V(A)$ and $T_U(A)$ curves for Cases 1 and 3 for a wide range of amplitudes. When the signal amplitude is large, the period of each curve is approaching a limiting value.*

These limits for $T_V(A)$ and $T_U(A)$ are also easy to obtain from Equations 6.8 and 6.9. When the amplitude is growing without limits, the values of P and Q will approach zero, since $\lim_{A\to\infty} \arcsin \frac{|V_1|}{A} = 0$ and $\lim_{A\to\infty} \arcsin \frac{|V_2|}{A} = 0$. If we set $P = 0$ and $Q = 0$ in Equations 6.8 and 6.9 and use β_V and β_U from Equations 6.3 and 6.2, we obtain Equations 6.12 and 6.13.

Figure 6.10 plots the curves of Figure 6.9 for a very wide range of A, together with the corresponding limiting values. Clearly, the two curves do not approach the same limiting value, even though the voltage dependent capacitors in both circuits are the same, and the voltage range, that the voltage dependent capacitors sample, is the same. The only difference between the two circuits is the polarity of one of the capacitors.

The curves corresponding to Figures 6.9 and 6.10 may also be plot for Cases 2 and 4 with the parameters of Table 6.1. The conclusions are similar to the conclusions made in Sections 6.1.2 and 6.1.4. In both cases, the period length first remains constant, then increases, reaches the maximum, and starts to decrease when $A > 0.8\ V$. The two curves will not overlap when $A > 0.8\ V$, since Equations (6.8) and (6.9) are different. If $A \gg 0.8\ V$,

the curves will approach the limiting values that can be calculated from Equations 6.12 and 6.13.

6.4 DC Component

In most fully integrated LC oscillator circuits, a dedicated bias current source sets the operating current of the gain stage transistors. A typical example of this is the negative-G_m CMOS oscillator of Figure 6.11a. Due to the symmetry of the circuit, the gain stage transistors find a stable operating point, where the DC current consumption of each transistor equals $I_{bias}/2$, the drain DC voltage of each transistor is $V_D = V_0$, and the signal swings about V_0. If $C_{tank}(V)$ depends only weakly on the voltage, and the Q value of the circuit is high, the signal voltage, referred to the ground, is approximately $V_s(t) \approx V_0 + A \cdot \sin(t/\sqrt{LC_0} + \phi)$. Considering the voltage dependent capacitance $C_{tank}(V_s)$, the signal voltage samples the range $[V_0 - A, V_0 + A]$ of the $C(V)$ curve.

When the distorted waveform was modeled with the piecewise sinusoidal functions $V(t)$ and $U(t)$ in Section 6.1, it was assumed that the signal would swing symmetrically about the same DC voltage level, no matter how the signal was distorted. However, it was also found out that the distorted

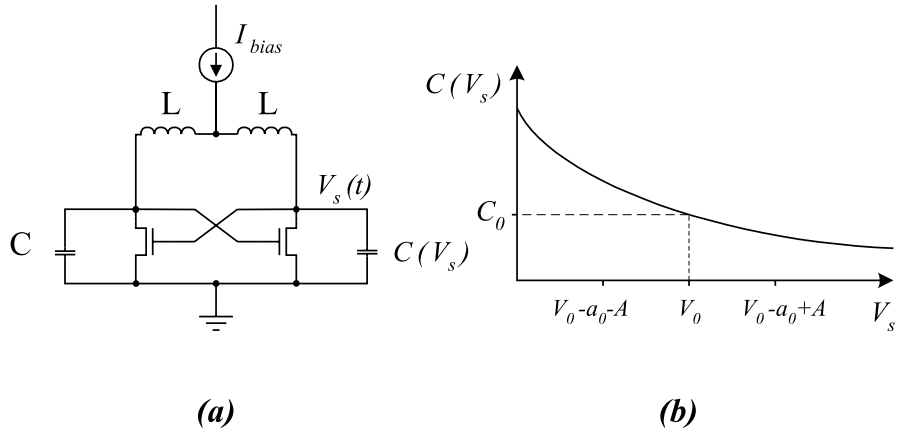


Figure 6.11: *a) A negative-G_m LC oscillator circuit. The right and the left halves of the circuit are symmetrical. b) The $C(V)$ curve of the voltage dependent capacitor.*

signal waveform may include a DC voltage component a_0. In circuits like in Figure 6.11a, the circuit will absorb this DC component by changing the DC voltage level of the signal by a_0 to the opposite direction, so that the current consumption of the gain transistors will match the current of the bias current source. The consequences of this are that the DC level of $V_s(t)$ remains at V_0, but the signal will swing between $V_0 - A - a_0$ and $V_0 + A - a_0$, referred to the ground. An important side effect of this waveform DC level shift is that the signal voltage will now sample a different part of the tank circuit capacitors' $C(V)$ curves than in the low distortion case, even if the signal peak-to-peak swing was the same (Figure 6.11b). Since the capacitance of the tank circuit obviously is coupled with the DC component of the distorted waveform, the steady state signal period will also depend on the DC component of the distorted signal.

To find out how the oscillating frequency is coupled with the DC component of the distorted signal, we can first derive the equations for the DC components of $V(t)$ and $U(t)$ as functions of the signal amplitude, assuming that the signal always swings between $V_0 - A$ and $V_0 + A$. Later, we can use these expressions for deriving the equations for the period length, taking into account the varying DC component.

The DC components of $V(t)$ and $U(t)$ as functions of the amplitude are easy to calculate, since $V(t)$, $U(t)$, T_U, and T_V are known. The DC component in Cases 1 and 2 is

$$a_{0V}(A) = \frac{1}{T_V}\int_0^{T_V} V(t)dt \tag{6.14}$$

and in Cases 3 and 4

$$a_{0U}(A) = \frac{1}{T_U}\int_0^{T_U} U(t)dt \tag{6.15}$$

After solving the integrals of Equations 6.14 and 6.15, we obtain

$$a_{0V}(A) = \frac{2A\sqrt{LC_0}}{T_V}\{G + \sqrt{\alpha}\cdot(H - G) - \sqrt{\beta_V}\cdot H\} \tag{6.16}$$

and

$$a_{0U}(A) = \frac{2A\sqrt{LC_0}}{T_U}\{(H-G) + \sqrt{\alpha}\cdot G - \sqrt{\beta_U}\cdot H\} \tag{6.17}$$

where

$$G = \begin{cases} \cos\arcsin\frac{|V_1|}{A} & , A \geq |V_1| \\ 0 & , 0 < A < |V_1| \end{cases} \tag{6.18}$$

and

$$H = \begin{cases} \cos\arcsin\frac{|V_2|}{A} & , A \geq |V_2| \\ 0 & , 0 < A < |V_2| \end{cases} \tag{6.19}$$

Instead of plotting Equations 6.16 and 6.17 directly, Figure 6.12 plots the DC components normalized to the signal amplitude, using the parameters from Table 6.1. These curves show the DC components relative to the signal swing in each case. The four curves confirm the conclusions that were made in Sections 6.1.1 – 6.1.4. In Case 1, the DC component grows rapidly when the amplitude exceeds $|V_1|$. When A exceeds $|V_2|$, the DC component decreases rapidly and becomes soon negative. In Case 2, the DC component decreases rapidly when A exceeds $|V_1|$, but it does not increase much when A exceeds $|V_2|$. This makes sense, since even though with the parameter values of Table 6.1 the value of C_2 drops by 50% when the signal voltage crosses the threshold value V_2, the value of C_1 is already so high that the change of C_2 does not reduce much the total tank circuit capacitance. In Cases 3 and 4, the magnitude of the DC component is increasing monotonically as the signal amplitude is increasing, as was expected.

Equations 6.8 – 6.11 describe how the period length depends on the amplitude, assuming the signal waveform will sample the range $[V_0 - A, V_0 + A]$ of the capacitor's $C(V)$ curve. However, as was already discussed, the limits of this voltage range will change in a more complicated manner in many practical LC oscillator circuits, since the DC component of the distorted signal will also modify them. To model the effect of the varying DC component, we first realize that moving the DC level of the signal by some amount has the same effect on Equations 6.8 – 6.11 as moving the threshold voltages V_1 and V_2 to the opposite direction by the same amount. Since

the DC component of the distorted oscillator signal is a function of V_1 and V_2 (Equations 6.16 – 6.19), the first problem is to find an equation for solving the DC component when the DC component and the threshold voltages are mutually coupled. Once this is done, we can correct the threshold voltages in Equations 6.10 – 6.11 and calculate the signal period from Equations 6.8 – 6.9.

As was discussed before, in LC oscillator circuits where the bias circuit delivers a constant current to the gain block, the gain stage transistors will find a stable DC operating point with signal DC voltage level V_0. If the distorted signal includes a DC component a_0, it will be absorbed in the circuit. One of the consequences is that the voltage dependent capcitors will sample an asymmetric region about the operating point voltage V_0, which obviously will change the steady state frequency. From our analysis point of view, this DC shift of the waveform is equivalent to shifting V_1 and V_2 by a_0 to the right direction. We can write an implicit equation for the steady state DC component of $V(t)$ by using Equations (6.16), (6.18) and (6.19), but replacing V_1 with $V_1 + a_{0V}$ and V_2 with $V_2 + a_{0V}$ in (6.18) and (6.19). We obtain

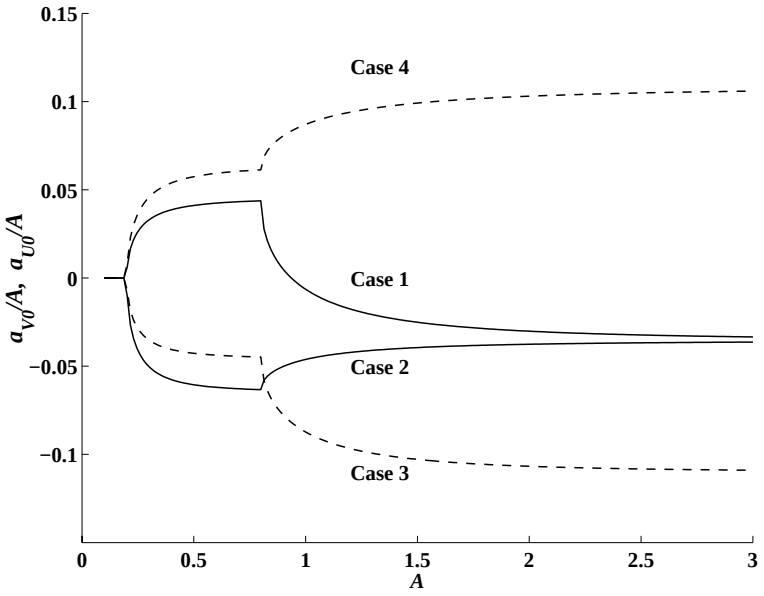


Figure 6.12: *The DC components of $V(t)$ (solid lines) and $U(t)$ (dashed lines), normalized to the signal amplitude.*

$$a'_{0V} = \frac{2A\sqrt{LC_0}}{T'_V}\{G'_V + \sqrt{\alpha}\cdot(H'_V - G'_V) - \sqrt{\beta_V}\cdot H'_V\} \tag{6.20}$$

where

$$G'_V = \begin{cases} \cos\arcsin\frac{|V_1+a'_{0V}|}{A} & , A \geq |V_1 + a'_{0V}| \\ 0 & , 0 < A < |V_1 + a'_{0V}| \end{cases} \tag{6.21}$$

$$H'_V = \begin{cases} \cos\arcsin\frac{|V_2+a'_{0V}|}{A} & , A \geq |V_2 + a'_{0V}| \\ 0 & , 0 < A < |V_2 + a'_{0V}| \end{cases} \tag{6.22}$$

$$\begin{aligned} T'_V = \sqrt{LC_0}\cdot\{&\pi\cdot(1+\sqrt{\beta_V}) \\ &+2\cdot(1-\sqrt{\alpha})\cdot P'_V \\ &+2\cdot(\sqrt{\alpha}-\sqrt{\beta_V})\cdot Q'_V\} \end{aligned} \tag{6.23}$$

$$P'_V = \begin{cases} \arcsin\frac{|V_1+a'_{0V}|}{A} & , A > |V_1 + a'_{0V}| \\ \pi/2 & , 0 < A \leq |V_1 + a'_{0V}| \end{cases} \tag{6.24}$$

and

$$Q'_V = \begin{cases} \arcsin\frac{|V_2+a'_{0V}|}{A} & , A > |V_2 + a'_{0V}| \\ \pi/2 & , 0 < A \leq |V_2 + a'_{0V}| \end{cases} \tag{6.25}$$

Equations (6.20) – (6.25) include all the necessary information for calculating a'_{0V}, but since A and a'_{0V} appear both inside and outside of the arcsin functions, it is difficult to solve for A or a'_{0V} explicitely. However, Equation (6.20) is of the type $a'_{0V} = F_V(A, a'_{0V})$. If A is given a reasonable value, it is possible to solve numerically for a'_{0V} by minimizing the function

$$E_V(A, a'_{0V}) = \{F_V(A, a'_{0V}) - a'_{0V}\}^2 \tag{6.26}$$

For calculating the DC component of $U(t)$ when the circuit is absorbing the DC component of the distorted waveform, we can write an implicit equation by using Equations (6.17), (6.18) and (6.19), but replacing V_1 with V_1+a_{0U} and V_2 with $V_2 + a_{0U}$ in (6.18) and (6.19). As was done with $a'_{0V}(A)$, we can write

$$a'_{0U}(A) = \frac{2A\sqrt{LC_0}}{T'_U}\{(H'_U - G'_U) + \sqrt{\alpha}\cdot G'_U - \sqrt{\beta_U}\cdot H'_U\} \tag{6.27}$$

where

$$G'_U = \begin{cases} \cos\arcsin\frac{|V_1+a'_{0U}|}{A} & , A \geq |V_1 + a'_{0U}| \\ 0 & , 0 < A < |V_1 + a'_{0U}| \end{cases} \tag{6.28}$$

$$H'_U = \begin{cases} \cos\arcsin\frac{|V_2+a'_{0U}|}{A} & , A \geq |V_2 + a'_{0U}| \\ 0 & , 0 < A < |V_2 + a'_{0U}| \end{cases} \tag{6.29}$$

$$\begin{aligned} T'_U = \sqrt{LC_0}\cdot\{&\pi\cdot(\sqrt{\alpha}+\sqrt{\beta_U}) \\ &+2\cdot(1-\sqrt{\alpha})\cdot P'_U \\ &+2\cdot(1-\sqrt{\beta_U})\cdot Q'_U\} \end{aligned} \tag{6.30}$$

$$P'_U = \begin{cases} \arcsin\frac{|V_1+a'_{0U}|}{A} & , A > |V_1 + a'_{0U}| \\ \pi/2 & , 0 < A \leq |V_1 + a'_{0U}| \end{cases} \tag{6.31}$$

and

$$Q'_U = \begin{cases} \arcsin\frac{|V_2+a'_{0U}|}{A} & , A > |V_2 + a'_{0U}| \\ \pi/2 & , 0 < A \leq |V_2 + a'_{0U}| \end{cases} \tag{6.32}$$

Since Equation (6.27) is of the type $a'_{0U} = F_U(A, a'_{0U})$, it is possible to solve numerically for a'_{0U} for a given value of A by minimizing the function

$$E_U(A, a'_{0U}) = \{F_U(A, a'_{0U}) - a'_{0U}\}^2 \tag{6.33}$$

The DC components for the four example cases with the parameters of Table 6.1 were solved with a computer program for a range of values of A. The program employs a numerical algorithm for minimizing $E_V(A, a'_{0V})$ and $E_U(A, a'_{0U})$ for different values of A. The resulting $a'_{0V}(A)$ and $a'_{0U}(A)$ curves, together with the $a_{0V}(A)$ and $a_{0U}(A)$ curves from Figure 6.12, are shown in Figure 6.13. Clearly, the new calculated DC components deviate from the values that were calculated assuming that the signal would always swing between $-A$ and A. However, the difference is not very large, especially in Case 1 and Case 2. In these two cases, the DC component never grows very large, since C_1 and C_2 have opposing effects on the DC component of the distorted waveform when both of them distort the same side of the waveform.

For calculating the period length as a function of the amplitude, we can use Equations (6.8) – (6.9), if we replace P with P'_V or P'_U, and Q with Q'_V or Q'_U. The period length as a function of the amplitude is plotted with

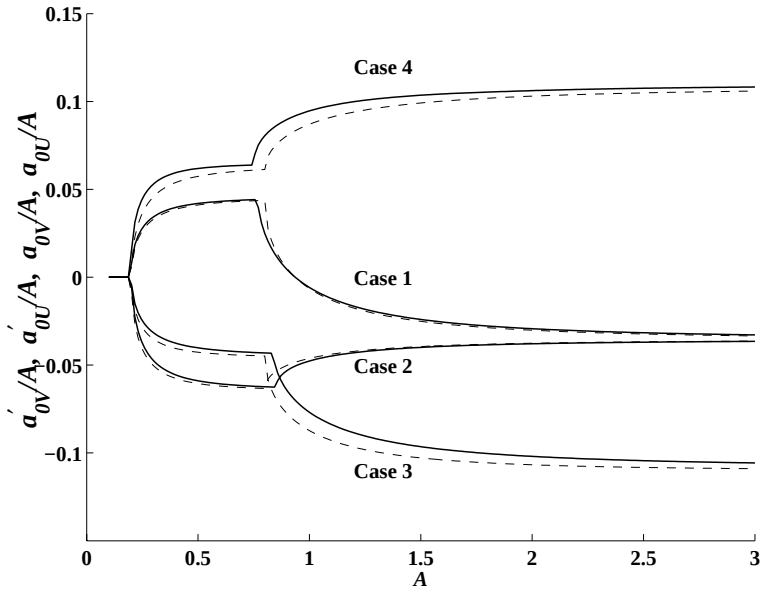


Figure 6.13: *The DC components of $V'(t)$ and $U'(t)$ (solid lines) and $V(t)$ and $U(t)$ (dashed lines) normalized to the signal amplitude.*

solid lines in Figure 6.14 for all the four example cases. For comparison, the dashed lines show the corresponding example curves that were plotted using Equations (6.8) – (6.11), which are the expressions for the period length when the effects of the DC components are ignored. Even though the two sets of curves in Figure 6.14 do not overlap, studying either of them leads to the same qualitative conclusions about the oscillating frequency, when the amplitude is changing. When $A < 0.2\ V$, the frequency does not depend on the amplitude for any of the curves. When A increases from $0.2\ V$ to $0.8\ V$, the oscillating frequency is changing as is expected from the discussion in Sections 6.1.1– 6.1.4. The curves reach the minimum or the maximum when $A \approx 0.8\ V$. When $A \gg 0.8\ V$, each curve seems to approach a limiting value, that is approximately the same for the corresponding curve in the other curve set.

The values of ζ and ϵ were chosen in the previous examples in the way that the waveforms are severely distorted, when the amplitude is large. Nevertheless, since the two sets of curves in Figure 6.14 do not deviate much from each other, it looks like we can use $a_{0V}(A)$ and $a_{0U}(A)$ instead of $a'_{0V}(A)$ and $a'_{0U}(A)$ for calculating the period length of the steady state waveform, when good accuracy of the result is not a concern. Since explicit analytic expressions for $a_{0V}(A)$ and $a_{0U}(A)$ are available, while solving $a'_{0V}(A)$ and $a'_{0U}(A)$ is possible only by numerical methods, it is practical to use Equations (6.8) – (6.11) for qualitative modeling.

6.5 Limits of the Parameter Space

In all examples of this chapter, the parameter values have been selected in the way that they clearly fall inside of one of the interesting parameter space regions. With practical oscillator designs, it may be difficult to guarantee that all fabricated circuits will remain well inside the desired region of the parameter space, since changing the varactor control voltage will change the threshold voltages V_1 and V_2 in VCO circuits, and since the statistical variation of the device parameters will modify the $C(V)$ curves of the tank circuit capacitors. For these reasons, the capacitor model parameters ζ, ϵ, α, β, V_1, and V_2 will be different for each fabricated circuit and varactor bias condition. As long as the values of α, β, and $V_1 \cdot V_2$ remain clearly inside one of the sixteen regions of Figure 6.2, and $|V_1| < |V_2|$, it is possible to approximate the $T(A)$ curve of the physical oscillator circuit with the piecewise sinusoidal models. However, if at least one parameter value falls close to the limit of two regions, these models will probably fail

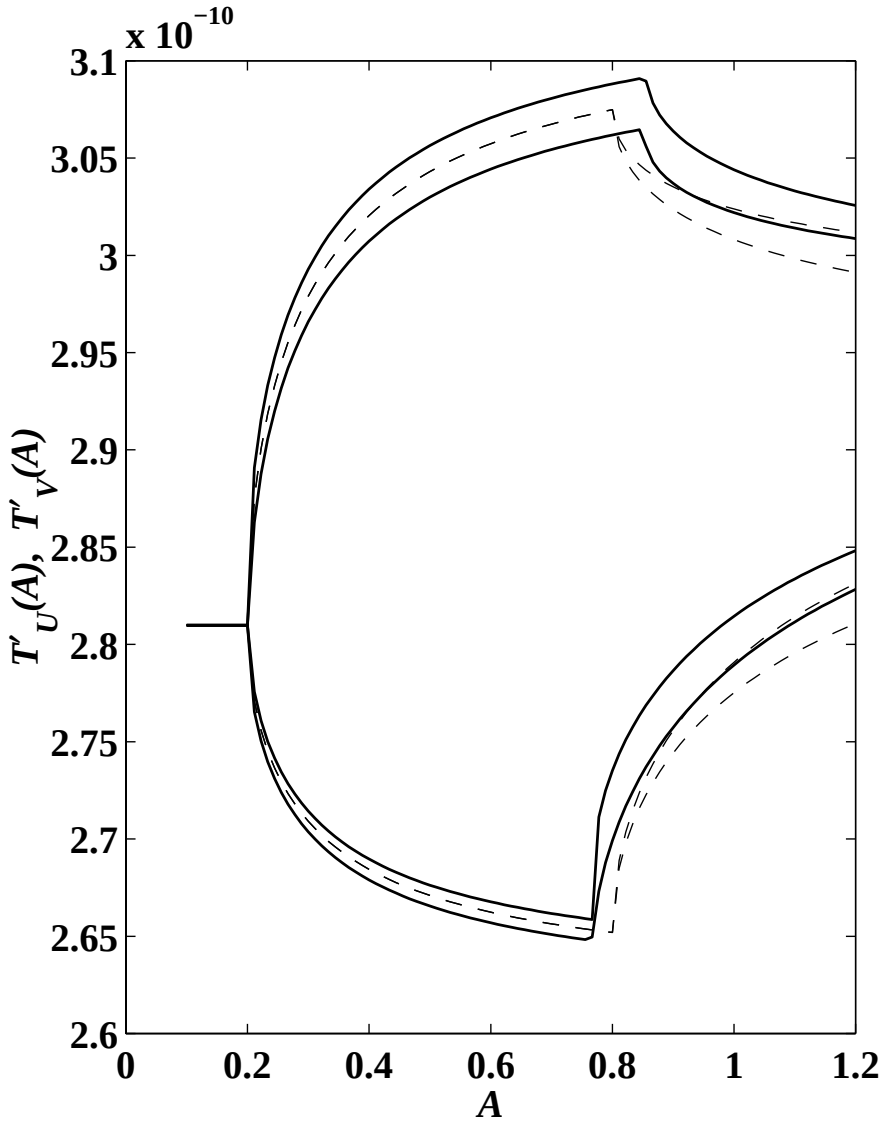


Figure 6.14: *The period length of $V(t)$ and $U(t)$. Solid lines: The effect of the absorbed DC component of the distorted waveform is taken into account. Dashed lines: The period length is calculated assuming that the signal always swings symmetrically about the operating point.*

in predicting the properties of the $T(A)$ curve. Given that the capacitor models are discontinuous, even though the physical voltage dependent capacitances always have continuous $C(V)$ curves, and that the piecewise sinusoidal model ignores the effects of varying gain, we must expect that these models will not predict the $T(A)$ curve of the physical circuit correctly, when for example the values of $|V_1|$ and $|V_2|$ are close to each other. In order to understand how the piecewise sinusoidal models behave close to these limiting parameter values, we can study each limiting case of practical interest separately.

Some parameters of physical oscillator circuits can not approach the theoretical limits of the parameter space at all. The value of ζ or ϵ can not be zero, since any voltage dependent capacitance in a practical oscillator circuit has some fixed parasitic capacitance in parallel. Neither can ζ or ϵ approach infinity, since the finite physical size of the fabricated circuit will always limit the maximum capacitance. Since α, β_V, and β_U depend only on the values of ζ, ϵ, C_{10}, and C_{20}, the values of α, β_V, and β_U are always greater than zero, and finite (Equations 6.1–6.3).

When the parameter space was divided into the sixteen sub-spaces of Figure 6.2, it was assumed that $0 < |V_1| < |V_2|$. If V_1 becomes zero, the effect of C_1 on the waveform will be to make one of the half cycles longer than the other, depending on the value of ζ (Figure 6.15). The period of the waveform will not depend on the amplitude, as long as $A < |V_2|$. Since C_1 does not have any effect on the period length when the amplitude is varied, it can not cancel out the effects of C_2. Therefore, the $T(A)$ curve will not have local minima or maxima, if $V_1 = 0$.

If $|V_1|$ and $|V_2|$ become equal, the resulting effects on the waveform will depend on which side of the waveform the capacitors distort. In Case 1 and Case 2, this condition is the same as setting $V_1 = V_2$. Therefore, it is possible to replace C_1 and C_2 with only one voltage dependent capacitor whose $C(V)$ curve is the sum of the two $C(V)$ curves. Obviously, no cancelling effects can take place, since there is only one voltage dependent capacitor with a monotonic $C(V)$ curve left in the tank ciruit. In Case 3 and Case 4, where the capacitors distort each side of the waveform, we need two voltage dependent capacitors to model the circuit, even if the magnitudes of the threshold voltages are equal. In these cases, Equations 6.9 – 6.11 will hold, but the expression for Q will become equal to P, if we set $|V_2| = |V_1|$. Replacing Q with P in Equation 6.9 and combining all constants, we obtain

$$T_U = T_U(A) = X' + Y' \cdot P \quad \Big|_{|V_1|=|V_2|} \tag{6.34}$$

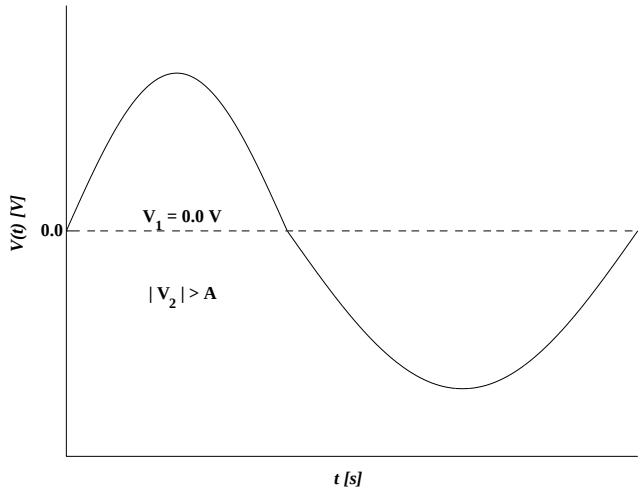


Figure 6.15: *If the threshold voltage $V_1 = 0$ V, and the signal amplitude $A < |V_2|$, the effect of C_1 on the waveform is just to make one of the half cycles longer than the other. The length of the period does not depend on the signal amplitude.*

where X' and Y' are constants, and $P = P(A)$ is the same function as in Equation 6.10. Since $P(A)$ is monotonic, the $T_U(A)$ curve of Equation 6.34 does not have local minima or maxima, when $|V_1| = |V_2|$. In summary, the tank circuit will not have in any of the four interesting parameter regions an amplitude level where the AM-to-FM zero conversion level would be zero, if $|V_1|$ and $|V_2|$ become equal.

In VCO circuits, the tuning voltage will shift the threshold voltage of the tunable capacitance of the tank circuit. In addition, the capacitor threshold voltages of each fabricated circuit will deviate from their nominal values because of the statistical distribution of the device parameters. For these reaons, it may be difficult to design the circuit in the way that the condition $|V_1| < |V_2|$ is always valid. Even if $|V_1|$ turns out to be larger than $|V_2|$, it is possible to analyze the circuit with the same piecewise sinusoidal model, when the capacitor names are interchnged and the parameters ζ, ϵ, α, β_V, and β_U are recalculated to correspond to the new situation. It turns out that if the circuit was designed to operate in one paricular region of the parameter space when $|V_1| < |V_2|$, it starts to operate in another region once the value of $|V_1|$ exceeds $|V_2|$. Even though the $T(A)$ curve might have an AM-to-FM conversion zero level also in this new region, the circuit must move to this new region through the point where $|V_1|$ equals to $|V_2|$. As

was shown above, the circuit is not able to suppress AM-to-FM conversion when $|V_1| = |V_2|$. Therefore, if the oscillator is designed for suppressing AM-to-FM conversion, care should be taken that the circuit will always operate inside the same region of the parameter space in Figure 6.2.

The condition $\alpha = 1$ means that C_1 is voltage independent. The $T(A)$ curve will not have local minima or maxima in this case, since there is only one voltage dependent capacitance with monotonic $C(V)$ curve left in the circuit. It is unlikely that this condition would appear with a practical oscillator design problem: if the voltage dependent part of C_1 is so small that it can be ignored, there is no need to model the circuit with the piecewise sinusoidal models. The values of α and β may be very close to one, if the tank circuit has large fixed parasitic capacitance in parallel with the voltage dependent capacitances. As long as $\alpha \neq 1$ and $\beta \neq 1$ (both C_1 and C_2 have voltage dependent components), it may be possible to find an amplitude level where the AM-to-FM conversion is zero.

If $\beta = \alpha$, the waveforms $V(t)$ and $U(t)$ must be analyzed separately, since the definition of β is different for these two models. For $V(t)$, the condition $\beta_V = \alpha$ means that $\epsilon = 1$, which means that C_2 is not voltage dependent (Equation 6.2). As was discussed earlier, the condition, where one of the capacitors is voltage independent, does not produce minima or maxima in the $T(A)$ curve. For $U(t)$, the condition $\beta_U = \alpha$ means that $\zeta = \epsilon$ (Equation 6.3). Using Equations 6.9–6.11, and setting $\beta_U = \alpha$, we obtain

$$T_U = T_U(A) = A' + B' \cdot (P + Q) \quad | \; _{|\alpha|=|\beta_U|} \tag{6.35}$$

where A' and B' are constants, and $P = P(A)$ and $Q = Q(A)$ are defined in Equations 6.10–6.11. Since $P(A)$ and $Q(A)$ are monotonically decreasing functions, the function $T_U(A)$ of Equation 6.35 is monotonically decreasing, and does not have local minima or maxima. In summary, the voltage dependent capacitances of the tank circuit will not be able to completely eliminate the AM-to-FM conversion when $\beta = \alpha$, since this condition makes the $T(A)$ curves of both piecewise sinusoidal models monotonic.

6.6 Comparison with Simulations

For studying the effects of voltage dependent capacitors in LC oscillator circuits, an ideal oscillator circuit for analog circuit simulations was designed. The schematic diagram of the circuit is shown in Figure 6.16. The simulations are run in an analog circuit simulator program that is able

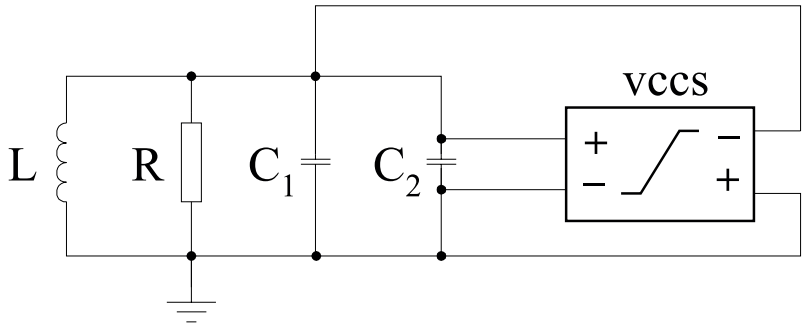


Figure 6.16: *An LC oscillator circuit for simulating the effects of the voltage dependent capacitors C_1 and C_2. The gain stage is an ideal voltage controlled current source with a limiter. The transfer function of the gain stage in the middle of the operating region is linear, and the gain is slightly higher than what is needed to compensate for the loss of the resistor. The clipping levels of the limiter are symmetrical about the zero level and they are adjustable, for controlling the amplitude of the steady state waveform.*

to model the $C(V)$ curves of voltage dependent capacitors with polynomial approximations. The amplitude of the steady state oscillation in the circuit can be set by setting the clipping levels of the limiter circuit in the amplifier block. To find out the steady state oscillation period in the circuit, a transient simulation is run, starting up the simulation with a suitable initial condition. The sinusoidal voltage waveform envelope will first grow exponentially and reach approximately constant amplitude level after a sufficient number of cycles. After the transient response of the circuit has vanished and the waveform has reached the steady state (within reasonable accuracy), the period and the amplitude of the waveform are calculated from the zero crossings of the voltage waveform.

This test circuit is very close to the ideal LC oscillator circuit in every sense but the capacitors, that are voltage dependent. Therefore, any observed effect, that deviates from the ideal LC tank circuit oscillator behavior, must arise either from the presence of the voltage dependent capacitors, or insufficient precision of the simulations. Since it is easy to find out if decreasing the time step or adjusting the simulator numerical precision parameters changes the simulation results, it is relatively easy to find the simulator setup that will produce reliable results, and not consume too much CPU time. Since many analog simulators allow using parameters as the polynomial coefficients, it is easy to run a large number of simulations

with different combinations of voltage dependent capacitors, and to extract the $T(A)$ curves for each combination from the resulting waveforms.

In order to compare the predictions of the piecewise sinusoidal models with the $T(A)$ curves that are extracted from transient simulations of the circuit of Figure 6.16, some example simulations were run with suitable voltage dependent capacitor parameters. The voltage dependent capacitances in the simulator circuit are defined with 10^{th} degree polynomials. The shapes of the capacitor $C(V)$ curves are selected in the way that it is easy to find the parameters V_1, V_2, ζ, and ϵ for the piecewise sinusoidal model of the same circuit. The $C(V)$ curves of C_1 and C_2 for each example case are plotted in Figure 6.17 with solid lines. Overlapping these curves, the $C(V)$ curves of the corresponding piecewise sinusoidal model capacitors are shown with the dashed lines. Figure 6.18 shows the corresponding total tank circuit $C(V)$ curves for each example case. Even though the stepwise varying capacitors model poorly the smooth $C(V)$ curves of the polynomial models, the most essential features of the curves, like the locations of the local extreme points and the capacitance value far away from the discontinuity points, are similar.

Figure 6.19 shows the $T(A)$ curves that were calculated using the piecewise sinusoidal models for the four example cases. For comparison, Figure 6.20 plots the $T(A)$ curves that were extracted from the transient simulations. The curves in these two figures show many similar qualitative features, although some details are clearly different. Of course, the curves of Figure 6.19 are not smooth, since the capacitances are piecewise defined, and include discontinuities. The curves of Figure 6.20 do not overlap each other when the amplitude is small, since the ripples of the polynomial capacitor models make the capacitances to deviate slightly from the target value at 0 V. Both figures predict that for all four cases the circuit will have an AM-to-FM conversion zero when the amplitude level $A \approx 1$ V. After the amplitude has reached the amplitude level $A = 1$ V, the curves for Case 1 and Case 3 (and correspondingly the curves for Case 2 and Case 4) diverge from each other in the same manner in both figures. The parameters of the voltage dependent capacitances for these example simulations were chosen in the way that the only difference between Case 1 and Case 3 (and between Case 2 and Case 4) is the polarity of C_2. Therefore, the diverging $T(A)$ curves in Figure 6.20 confirm the conclusions made earlier in Section 6.3: if the polarity of one of the voltage dependent capacitors is invered in an LC oscillator circuit, the resulting steady state period of the signal may change.

Finally, Figure 6.21 shows how the steady-state oscillation period changes if the polarity of one of the capacitors is changed. Obviously, the oscillation

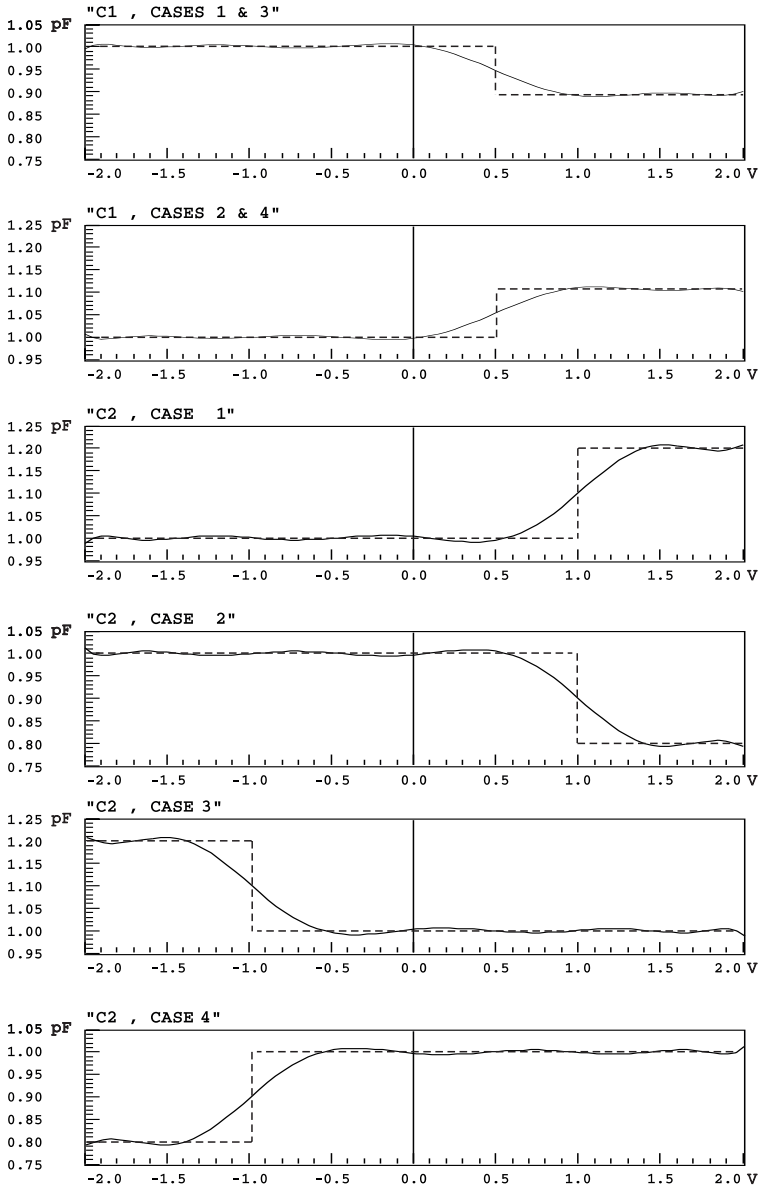


Figure 6.17: *The $C(V)$ curves of the voltage dependent capacitors for the examples.*

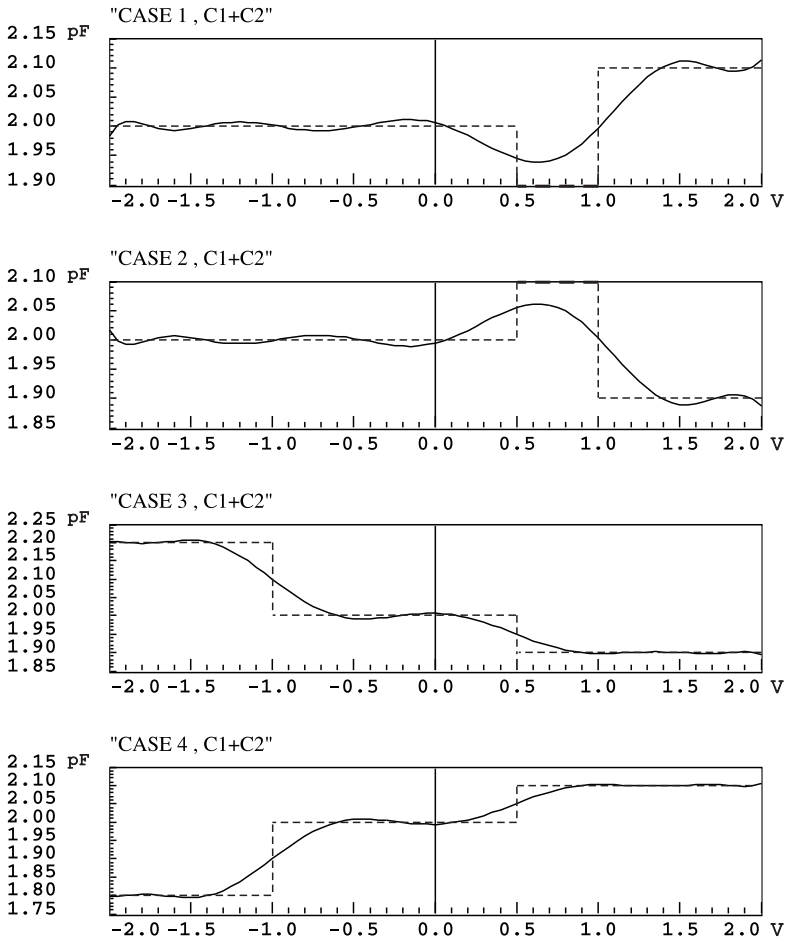


Figure 6.18: *The total tank circuit capacitance in the four example cases.*

period of the LC oscillator depends on the polarity of the voltage-dependent capacitors. Figure 6.22 shows the time domain voltage waveforms in these two cases at one amplitude level. The shapes of the waveforms are clearly different.

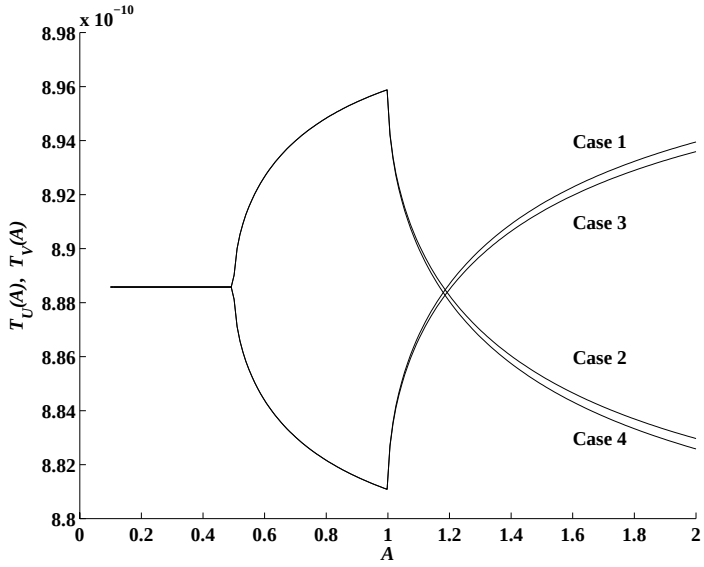


Figure 6.19: *The $T(A)$ curves for the ideal oscillator circuit, predicted with the piecewise sinusoidal models.*

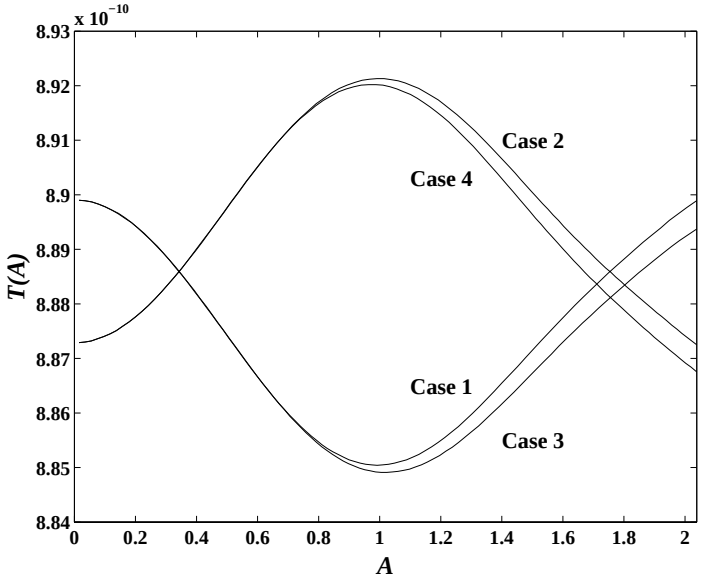


Figure 6.20: *The $T(A)$ curves of the ideal oscillator circuit, calculated from transient simulation results.*

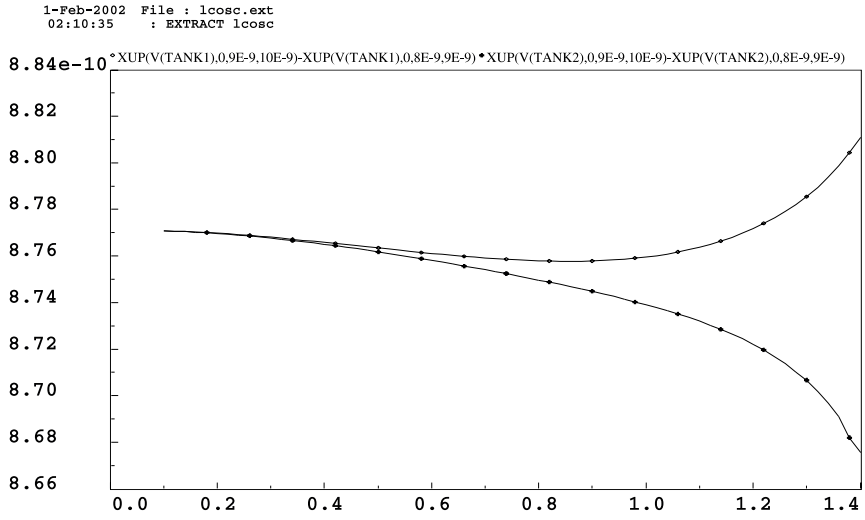


Figure 6.21: *The T-vs-amplitude curves for the LC oscillator circuit with an ideal symmetrically limiting transconductance amplifier and two voltage dependent capacitors. The polarity of C_2 was inverted between the simulations.*

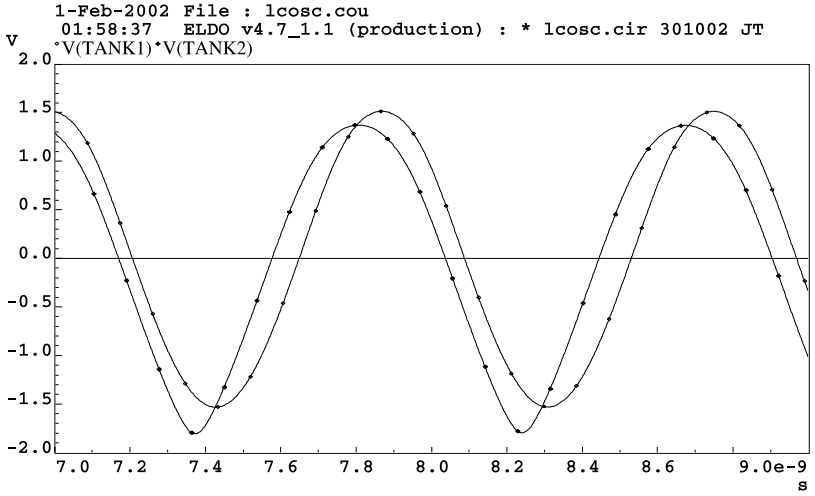


Figure 6.22: *The simulated steady state response of the LC oscillator circuit with an ideal symmetrically limiting transconductance amplifier and two voltage dependent capacitors. The polarity of C_2 was inverted between the two simulations. Otherwise, the simulation conditions are identical. The phase shift between the two curves is not only due to the small difference in the oscillating frequencies, one of the plots is slightly delayed to make the curves easier to read.*

6.7 Conclusions

This chapter studied the behavior of the *LC* oscillator voltage signal waveform, when the tank circuit capacitance consists of two different voltage dependent capacitors. It was found out that these capacitors make the steady state period of the oscillator to depend on the signal amplitude. Moreover, if the voltage dependencies of these capacitors can be selected in the right way, it is possible to find an amplitude level where the AM-to-FM conversion of the circuit will be zero.

Most practical *LC* oscillator circuits include voltage dependent capacitances. Usually, the resulting sensitivity to the bias source modulation is thought to be unavoidable, and the attempts to improve the spectral purity of the oscillator are limited to reducing the noise level of the bias sources. However, the analysis in this chapter indicates that taking into account the voltage dependent capacitances the oscillator might be designed to suppress the spectral impurities that originate from the bias current noise.

Chapter 7

PFET VCO in an n-well Technology

Almost all published fully integrated CMOS VCO circuits employ NMOS transistors in the gain stage for providing the necessary gain in the VCO core. PFETs are often used as the complementery devices with the NFETs, in in order to increase the gain per given bias current [31]. Some authors employ complementary PFET/NFET pairs for making the VCO core voltage waveforms more symmetric, in order to reduce the noise translation from other frequencies close to the oscillating frequency [48]. Even though the PMOS-only gain stage design has appeared in some published papers [51] [53], most published works on fully integrated CMOS VCO circuits seem to include NMOS transistors in the gain stage.

The reason for favouring NMOS transistors in most VCO designs is well-known: because the mobility of electrons is larger than the mobility of holes, NMOS transistors provide larger transconductance per given gate geometry and given drain current than the PMOS transistors in the same technology. Therefore, using NMOS transistors, the gain stage transistors can be made smaller, which reduces the current consumption of the VCO core for a given RF loss and signal swing in the tank circuit. In addition, reducing the gain transistor size reduces the parasitic drain-bulk junction capacitances of the transistors, which helps in obtaining wider tuning range with a varactor tuned VCO circuit. Moreover, NMOS tansistors usually have slightly lower threshold voltage than PMOS transistors in the same technlology, which allows slightly larger signal swing in the VCO core output nodes.

The advantages of using NMOS transistors in the VCO gain stage seem to be so overwhelming that the disadvanteges are seldom discussed. Low-cost digital CMOS processes often provide n-type wells for PMOS transistors,

while the NMOS transistors are fabricated directly on the p-type substrate material. Therefore, the NMOS transistor back gates are DC-coupled to the substrate, and any variation in the substrate potential will drive the back gates of all NMOS transistors. As is discussed in Chapter 4, low-frequency interference coupling from the substrate to the RF frequency synthesizer VCO core circuit may be very troublesome. If the n-well process is optimized for digital use, the suppression of the signals coupled through the back gates usually is considered satisfactory if the noise margins of the digital circuits are maintained. However, since oscillator circuits are much more sensitive in picking up noise, using the NMOS transistors with an n-well process for a VCO design may be difficult.

Even though NMOS transistors provide significantly more gain than the corresponding PMOS devices with the same gate geometry, they also generate more noise. Deep-submicron minimum-length NMOS transistors are noisy when operating in the saturation region, since the hot carriers in the drain region genereate excess noise [58]. The noise level originating from the hot carriers in PMOS transistors is usually very low, since holes do not obtain enough kinetic energy for starting up an efficient impact ionization process in the drain region electric field, even when the transistor is working in the velocity saturation region. In addition, the $1/f$ noise level of NMOS transistors is usually higher (by one order of magnitude or more) than with the PMOS transistors in the same technology and same geometrical dimensions. For these reasons, PMOS transistors are sometimes used when the goal of the design is to maximize the signal-to-noise ratio rather than obtaining the specified gain with the minimum current consumption [53].

Since the goal with the VCO core design optimization should be obtaining sufficient signal-to-noise ratio at a sufficient voltage swing after the buffer transistors, rather than obtaining sufficiently large tank circuit voltage amplitude with the minimum current consumption, it is not obvious that choosing NMOS transistors for providing the gain will automatically result in significantly better performance. Unfortunately, it is difficult to make reliable predictions about the resulting phase noise levels when different gain stage topologies are compared, since the foundries usually do not specify the noise performance parameters of the transistors, especially if the process is intended for digital designs only. It is also difficult to find a published fair experimental comparison where a well-designed PMOS VCO was compared with a well-designed NFET VCO in the same tecnology, taking into account the final SNR, current consumption, and the substrate and power supply noise tolerance of the circuit.

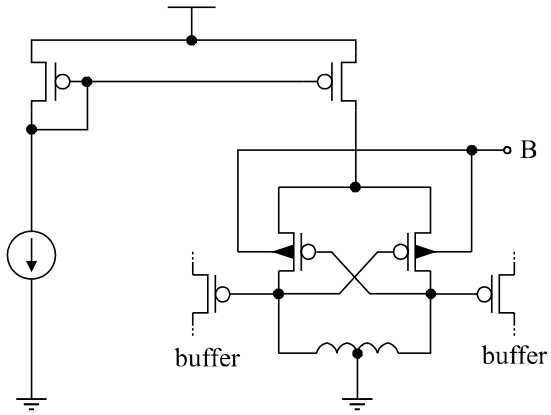


Figure 7.1: *The back gate tuned PFET VCO circuit with the tail current mirror and the buffer transistors.*

7.1 Back Gate Tuned PFET VCO Circuit

The IC process that was available for experimenting during this work, is a 0.35 μm CMOS n-well process, intended for digital and mixed-mode designs. In order to improve the VCO core isolation from the substrate, the VCO circuit studied in this work employs only PMOS transistors in the gain stage and in the current mirror. PMOS transistors are also used in the inputs of the buffer stages, since the DC voltage component of the VCO core voltage signal is 0 V. For driving NMOS transistors, the DC level of the VCO core signal should be shifted above the threshold voltage of the NMOS transistors. Figure 7.1 shows the schematic diagram of the VCO.

Since the PMOS devices provide little gain per given tail current, the gain stage transistors must be made relatively large, which would limit the tuning range of a conventional varactor tuned VCO circuit. However, the drain-bulk junction of the PMOS transistor is the same pn-junction that would be used if a pn-junction varactor was employed for tuning in this circuit. Instead of using a separate diode varactor device, it is possible to use the drain-bulk junctions of the gain stage transistors for tuning the oscillation frequency, if the n-well potential is controlled with an external tuning voltage source [54]. Since the gain transistor drain-bulk junctions become the active tuning elements, the drain fingers may be made as large as desired, without limiting the tuning range of the circuit. Since the conventional NMOS transistors are omitted in the circuit of Figure 7.1, no

other significant parasitic capacitances but the buffer transistor gates and the gain transistor gates are connected in parallel with the tunable capacitor.

The RF loss of the drain-bulk capacitors is a concern, since it is the other significant source of RF loss in the tank circuit, in addition to the spiral inductor substrate loss. The reason for RF loss in the drain-bulk junction capacitor is that the RF current must flow from the drain fingers to a low impedance node in the bulk, when the junction capacitor is charged or discharged during the oscillation cycle. Even though the depletion region under the drain finger has very low losses (since very few charge carriers are present), the capacitor charging current must also flow in the undepleted n-well bulk material, which has high resistivity. A straightforward way to shorten this current path would be to place bulk contacts close to each drain finger. However, as is demonstrated with varactor devices in [62], it is possible to make the RF current path in the n-well much shorter by establishing virtual ground planes next to each drain finger.

The voltage signals in the two gain transistor drain nodes are complementary. If the transistors are fabricated symmetrically inside the same n-well, the potential of the symmetry center of the two transistors with complementary signals must stay constant. This symmetry center looks like a low impedance node to the AC currents flowing from the drain fingers. Moreover, if the drain fingers of the two transistors can be interleaved, a virtual ground plane is established between each drain finger pair, and the RF current path from every drain finger to the low impedance plane in the undepleted bulk material will be very short [56] [57]. Figure 7.2 shows how the gain transistor drains can be laid out to face each other.

7.2 Voltage Dependent Parasitic Capacitances

For analyzing the capacitances of the PFET VCO core circuit, it is instructive to study only one half of the symmetrical gain stage circuit. Figure 7.3 shows a simplified circuit diagram for identifying the most significant voltage dependent capacitances connected to the drain node of transistor M_2. The loaded Q value of the tank circuit is assumed to be high. Therefore, the steady state voltage waveform will be almost sinusoidal: $v_{D,M2} \approx Asin(\omega_0 t + \phi)$. When the tail current is relatively high, the resulting steady state voltage amplitude A is so large that the transistors work in the switching mode (say, $A \approx 2V_{T,PMOS}$). We assume first that the oscillation frequency is so low that the quasi-static approximation holds.

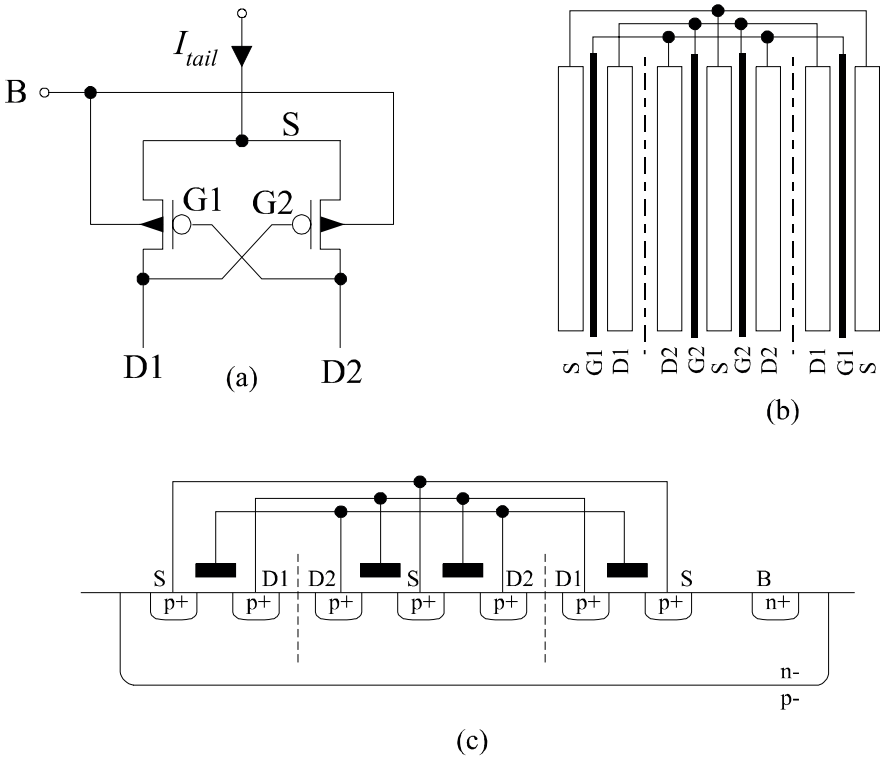


Figure 7.2: *The interleaved PMOS gain transistor pair layout. (a) The schematic diagram of the gain transistor pair. (b) The interleaved gain transistor pair layout. Since the transistor drains are made to face each other, a virtual ground plane is created between each drain finger pair (dashed lines). Since the path of the RF current from a drain finger to a low impedance node in the bulk is everywhere very short, the RF loss of the drain-bulk junction capacitance remains low. (c) The cross section of the gain transistor pair, showing the virtual ground planes (dashed lines) and the bulk contact for the tuning voltage. The bulk n-well is isolated from the substrate with the depletion layer between the n-type well and the p-type substrate.*

Since the size of the gain transistors in this VCO is chosen based on the value of the drain-bulk junction capacitance, rather than obtaining sufficient gain with smallest possible parasitic drain-bulk junction capacitances, the gain transistors are large. Therefore, the transistors provide plenty of gain already when the gate-source voltage only slightly exceeds the thresh-

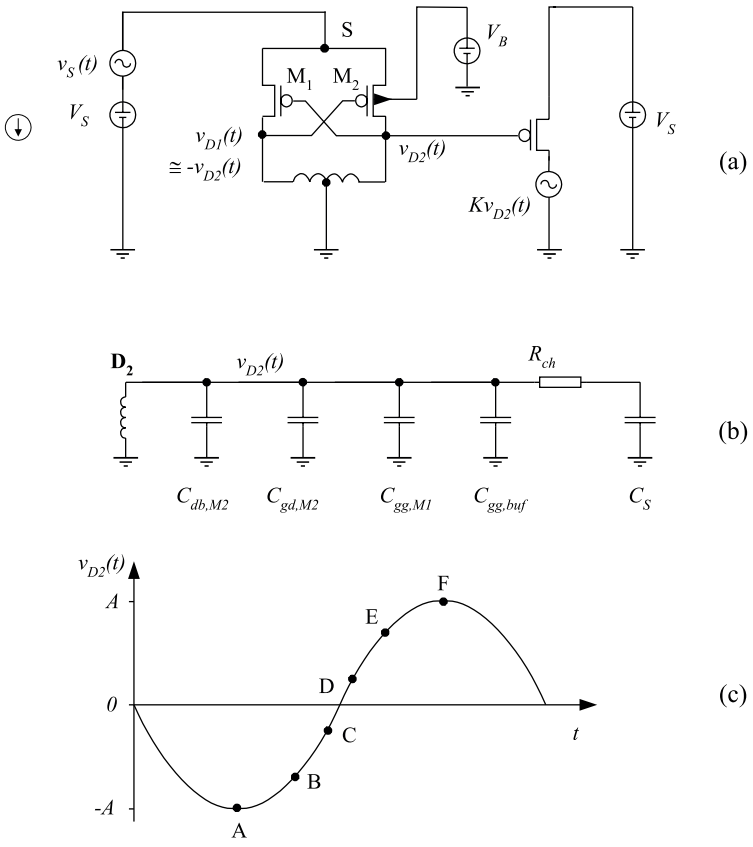


Figure 7.3: *(a) A simplified circuit diagram of the PFET VCO circuit, showing the circuit elements and the voltages determining the instantaneous values of the voltage dependent capacitances in the drain node of* M_2*. (b) The voltage dependent capacitances of the tank circuit in the drain node of* M_2*. (c) Selected points along one cycle of the voltage wavefrm, at which the capacitances* C_i *are estimated.*

old voltage $V_{T,PMOS}$ of the transistor. The steady state DC voltage of the source node will set to $V_S = -V_{T,PMOS} + V_{od}$, where V_{od} is the (positive and relatively small) gate overdrive voltage.

From the discussion in Chapter 5 we can conclude that the instantaneous rate of change of voltage in the drain node of M_2 depends on the factor $(LC)^{-\frac{1}{2}}$, where $C = C_{fix} + \Sigma C_i(v_{D2})$, C_{fix} is the sum of the tank circuit

capacitances that are not voltage dependent, and $C_i(v_{D2})$ are the voltage dependent capacitances in the circuit. Since the inductance L and the fixed capacitance C_{fix} do not depend on the signal voltage, for finding out which way the waveform is distorted, it is sufficient to study how the values of the individual voltage dependent capacitances C_i change during one steady-state oscillation cycle. To obtain qualitative insight, we can estimate the capacitances $C_i(v_{D2})$ at some interesting instantaneous signal voltage values, when the voltage swings from the minimum to the maximum during the oscillation cycle.

The most significant voltage dependent capacitances connected to the drain of M_2 are the drain-bulk junction capacitance $C_{db,M2}$, the gate-drain capacitance $C_{gd,M2}$, the gate capacitance of M_1 (named $C_{gg,M1}$), and the buffer transistor gate capacitance $C_{gg,M3}$. In addition, the capacitances of the source node are connected to the drain node through the channel of the transistor, when it operates in the non-saturation region. Figure 7.3b shows the tank circuit with these elements, and Figure 7.3c shows the points along the oscillation cycle, where the values of the capacitances are evaluated.

In point A, the voltage in the drain node of M_2 is in the minimum, $v_{D2}(t) = -A$ and $v_{D1}(t) = +A$. M_2 is in the cut-off region. Since the channel of M_2 is almost empty of charge carriers, the channel does not contribute significantly to the capancitance of the drain node. The capacitance C_S in the source node is disconnected from the drain of M_2, since the channel resistance $R_{ch,M2}$ is high. Note that M_2 will never enter the accumulation region even if the signal amplitude is high, since M_1 shorts the gate and source of M_2. In this part of the cycle, M_1 operates in the linear region, and its channel potential will follow $v_{D,M1}$. Since the channel voltage is not constant, but $v_{D,M1} \approx -v_{D,M2}$, the capacitance seen from the gate of M_1 to the AC ground will be approximately two times the strong inversion oxide capacitance.

In point B, the drain-source voltage of M_1 becomes so high that M_1 enters the saturation region, and the gate capacitance $C_{gg,M1}$ will slightly drop. Since the channel is now pinched off, the channel potential does not follow the drain voltage anymore, which will further reduce the capacitance seen from the gate terminal.

When the drain voltage of M_2 rises and equals $v_{D2}(t) = -V_{od}$, the gate-source voltage of M_2 equals to the threshold voltage, and M_2 enters the strong inversion region (point C). Since the drain-source voltage at this moment is relatively high, $V_{ds} = V_{TH} + 2V_{od}$, the transistor is in saturation. The holes that build up the channel charge enter the channel from the source. Since the channel is pinched off from the drain side, the buildup of the channel charge does not disturb the drain current.

In point D, $v_{D2}(t)$ reaches the value $v_{D,M2} = V_{od}$. M_1 enters the weak inversion region since the gate-source voltage drops below the threshold voltage. Since the channel charge becomes very small, the gate capacitance of M_1 drops significantly, which will speed up this part of the cycle. M_2 is still in the strong inversion region and in saturation.

When $v_{D2}(t)$ still rises, the drain-source voltage of M_2 drops, and M_2 will eventually enter the non-saturation region (point E). The channel charge of M_2 becomes increasingly dependent on the drain voltage. In addition, when the channel of M_2 is no longer pinched off, the parasitic capacitances of node S are connected to the drain of M_2 through the transistor channel. For these reasons, the value of the tank circuit capacitance has increased again, and this part of the cycle slows down.

Even if C_S is large, it cannot stretch the top of the waveform very much. The gate of M_2 is driven from $v_{D,M1}$, which will switch off the transistor when the gate-source overdrive voltage becomes zero again. Nevertheless, C_2 will slightly postpone this switch-off time moment, and therefore, the parasitic capacitances in the source node will slightly lower the oscillation frequency when the signal amplitude is large.

The drain-bulk junction capacitance $C_{db,M2}$ will reach the maximum value in point A and the minimum value in point E. Even though the pn-junction capacitance does depend on the instantaneous signal voltage, the variation is less abrupt than the variation of the MOSFET intrinsic capacitances. Therefore, it can be first ignored in this qualitative analysis, even though the value of this capacitance is relatively large. The buffer transistor gate capacitances are relatively small, since the buffer transistors are small, compared to the gain transistors. Therefore, they may also be ignored first. The the buffer transistors and the drain-bulk junction capacitances of the gain transistors are easy to include in the simulation test bench.

7.3 Quasi-static Transient Simulations

The circuit of Figure 7.4 was simulated in an analog circuit simulator, employing BSIM3V3-based device models (Eldo Level 53) and process parameters from the 0.35 μm target technology. In order to model the drain and source pn-junction capacitances, the gain transistor finger dimensions were defined according to the interleaved gain stage transistor layout of Figure 7.2 and the design rules of the target process. The simulation test bench starts up the oscillation in the transient simulation mode, simulates until the output voltage waveform has reached the steady state, and extracts the parameters from the last oscillation cycles.

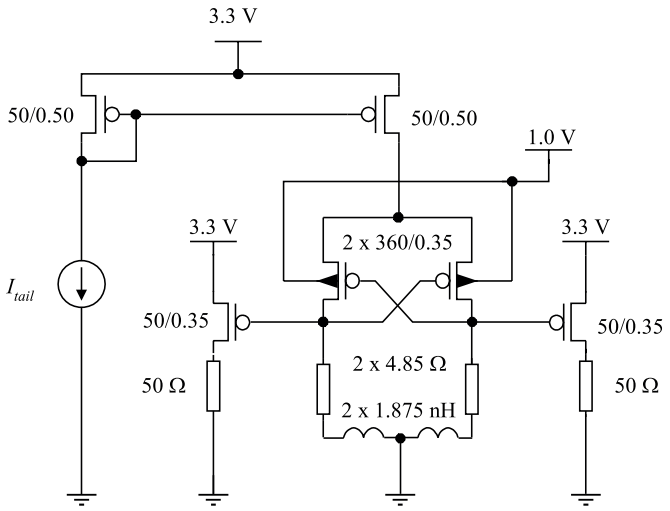


Figure 7.4: *The simulation test bench for extracting the voltage dependent tank circuit capacitances.*

Figure 7.5 plots the steady state voltage waveform $v_{D,M2}(t)$ and the sum of the two dominating voltage dependent capacitances, with two different tail bias current values. In Figure 7.5a, the capacitance drops during the positive peaks of the voltage waveform, since M_1 enters the weak inversion region in this part of the cycle. Consequently, the positive peaks of the voltage waveform have slightly sharper tops than the negative peaks, indicating that the positive peaks of the waveform are accelerated. In Figure 7.5b, the voltage amplitude is larger, and the gain transistors are driven into the non-saturation region during the peaks of the voltage waveform. Consequently, the tank circuit capacitance increases during these peaks. The peaks of the voltage waveform look more round, indicating that the cycle is slowing down during the peaks.

Figure 7.6 plots the simulated steady-state oscillation frequency with different tail bias current values. With small bias currents, the gain transistors switch between the strong and the weak inversion regions, but they remain in saturation. During the voltage peaks, one of the gain transistors is driven into the weak inversion region, where the gate capacitance will decrease, and the cycle is accelerated. If the tail current is increased (but still $I_{tail} < 2.5\ mA$), the fraction of the cycle where one of the gain transistors is in the weak inversion will increase, and the oscillation frequency

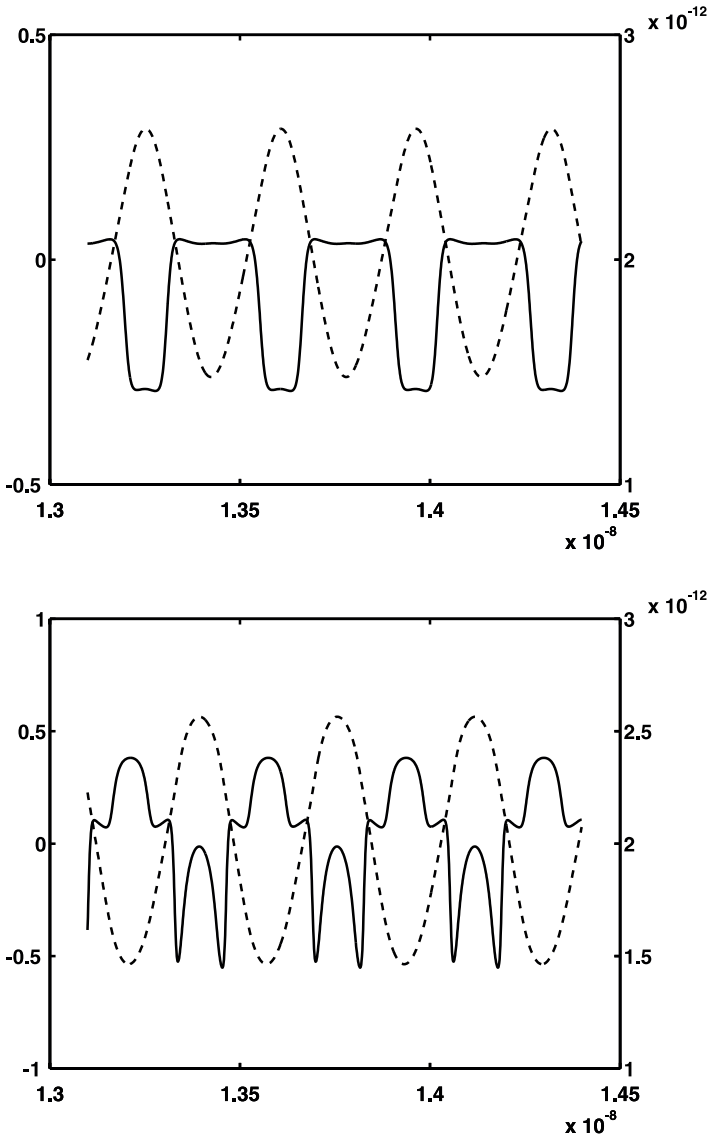


Figure 7.5: *The steady-stage voltage waveform of* $v_{D,M2}(t)$ *(dashed line, left y-axis) and* $C_{db,M2}+2C_{gg,M1}$ *(solid line, right y-axis). (a) With small signal voltage amplitude, the capacitance* $C_{db,M2} + 2C_{gg,M1}$ *drops when* $v_{d,M2}(t)$ *is high, but remains approximately constant elsewhere. The tail current is* $I_{tail} = 1.8\ mA$*. (b) With large signal voltage amplitude, the capacitance increases significantly close to the positive and negative peaks of* $v_{D,M2}(t)$*. The tail current is* $I_{tail} = 4.0\ mA$*.*

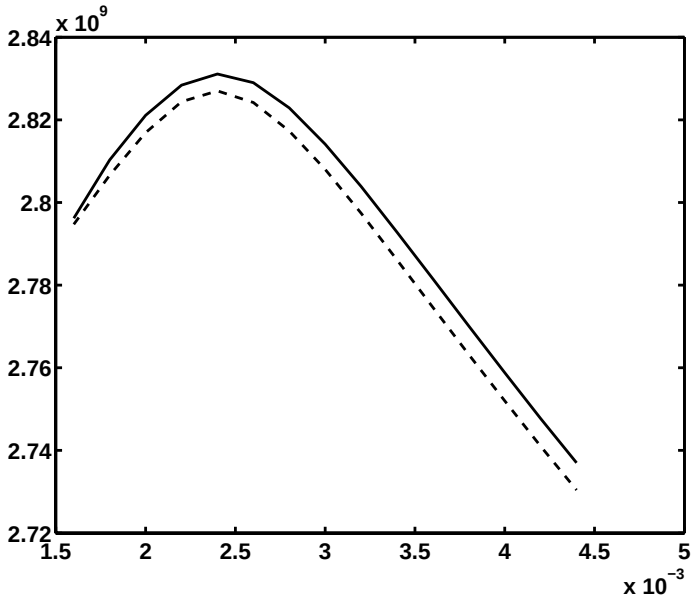


Figure 7.6: *Simulated steady-state oscillation frequency vs. tail bias current. Solid line: no additional capacitance from the gain transistor sources to the ground. Dashed line: a 10 pF capacitor is connected between the gain transistor source node and the ground.*

will increase. With larger tail bias current values ($I_{tail} > 2.5\ mA$), the gain transistors are driven into the non-saturation regions during the voltage waveform peaks. Increasing the bias current even more will increase the fraction of the cycle where the gain transistors are in the non-saturation region, and the oscillation frequency will further decrease.

7.4 Experimental results

A prototype of the back gate tuned PFET VCO circuit was fabricated in a 0.35 μm n-well CMOS technology [57]. A photograph of the prototype circuit is shown in Figure 7.7. The layout was designed for maximum symmetry, in order to suppress common-mode signals conversion to differential-mode signals. A symmetrical center-tapped hollow spiral inductor design was chosen [72]. The gain stage transistors were designed for the minimum distance between the drain finger edges and the virtual ground planes, in

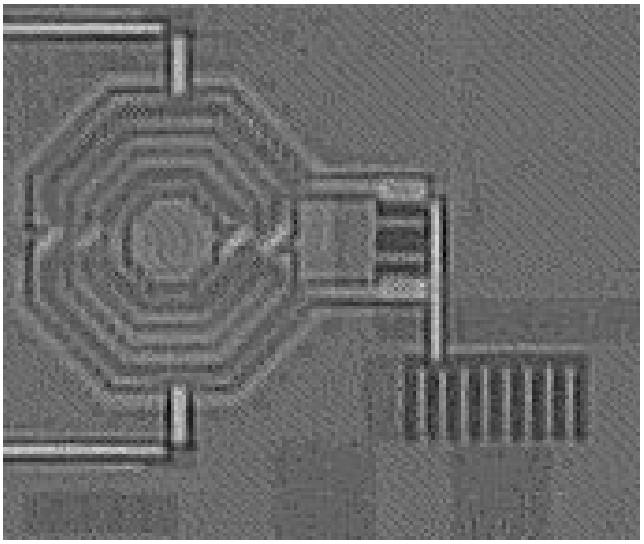


Figure 7.7: *A photograph of the back gate tuned PFET VCO circuit prototype.*

order to maximize the quality factor of the drain-bulk capacitors. Each gain transistor has sixteen 20 μm x 0.35 μm gate fingers and sixteen 20 μm x 1.1 μm drain fingers. The source finger dimensions are 20 μm x 1.1 μm. Since the sources of the two transistors are connected together, neighboring transistor fingers share the source finger between them.

Figure 7.8 shows the measured tuning characteristic of the prototype oscillator. The plot includes the coefficients for a fifth order polynome that was fit to the data, for modeling the VCO in an analog behavioral simulator. The tuning range around the center frequency is $\pm$ 5%, which is relatively large, compared with the other published back gate tuned VCO circuits [54] [55]. However, even though the tuning range is wide enough for covering the frequency band of many practical applications, it is not sufficient for compensating against the arising from the parameter variations of the fabrication process.

The on-chip buffer stages will distort the signal waveform by limiting the amplitude of the buffered voltage signal, when the tank circuit voltage amplitude is high. To avoid this compression during the measurements, the buffer stage supply voltage was grounded during the signal amplitude measurements, and the signal that leaked from the tank circuit through

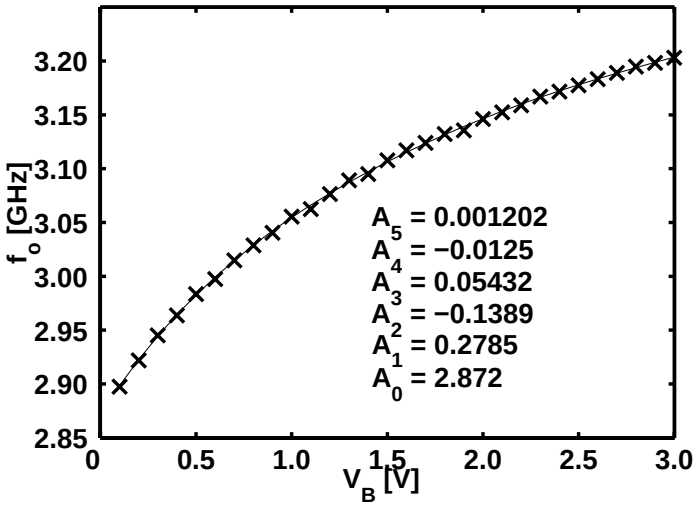


Figure 7.8: *The measured frequency tuning characteristic of the prototype circuit.*

the buffer transistors was amplified with a low-noise amplifier. Figure 7.9a shows the measured signal amplitude with different values of the tail bias current. When the tail bias current exceeds approximately 2.5 mA, the gain transistors work in the switching mode, and the slope of the curve, k_a, is almost constant. With smaller bias currents, the slope of the curve is steeper, but the sensitivity to amplitude modulation is still small ($k_a < 1\ V/mA$).

Figure 7.9b shows the measured oscillating frequency as a function of the tail bias current. The curve is qualitatively very similar to the simulation result of Figure 7.6b, and shows a maximum at $I_{tail} \approx 2.5\ mA$. The measured oscillating frequency is higher than the simulated steady-state frequency at all tail bias currents. Since the oscillation frequency is high, the charge distributions in the transistor channel and in the pn-junctions are not able to follow the quasi-static distributions, which will reduce the capacitances associated with these charges. The estimated parasitic capacitances may also be too large in the simulation test bench.

For the noise spectrum measurements, the signal from one output of the VCO was amplified and connected to the noise measurement system, where it was converted close to 1 GHz using the low-noise oscillator and the mixer of the available phase noise test set. The spectrum of the downconverted

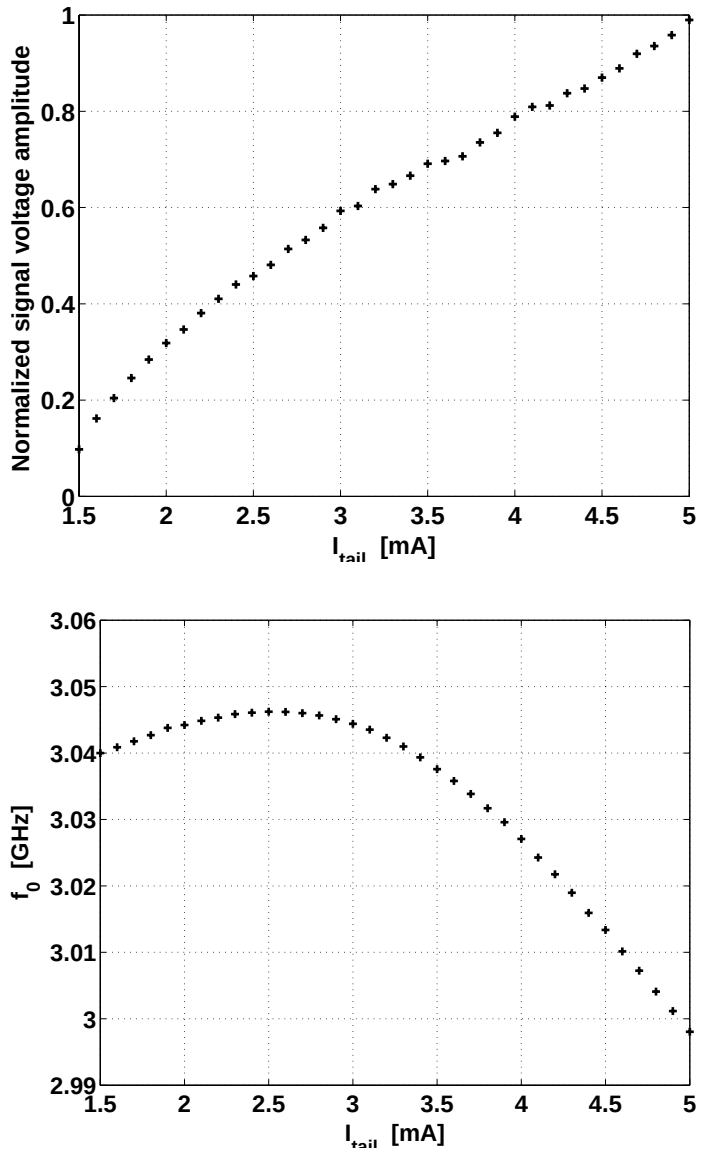


Figure 7.9: *(a) The measured tank circuit voltage signal swing vs. the tail bias current. (b) The measured oscillation frequency vs. tail bias current. The sensitivity of the oscillator to small bias current variations is very small when* $I_{tail} \approx 2.5\ mA$.

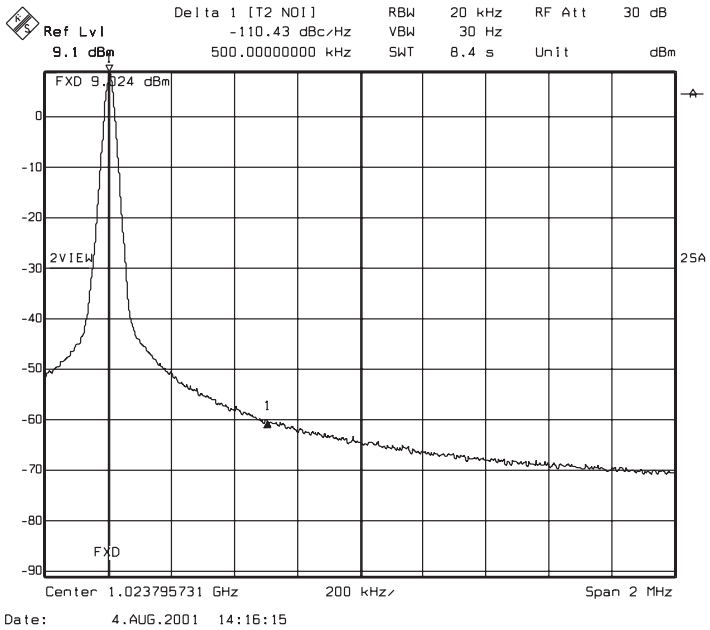


Figure 7.10: *The spectrum of the VCO tank circuit signal. The signal was converted to 1 GHz using an ultra stable reference oscillator.*

signal was measured with a spectrum analyzer. The measured noise spectrum is shown in Figure 7.10. The data includes the contribution from the amplitude noise, since it was not possible to lock the tracking oscillator of the phase noise test system to the VCO signal. The measured phase noise level at 500 kHz offset from the carrier frequency is $-110.43\ dBc/Hz$.

Since the slope of the $f(I_{tail})$ -curve in Figure 7.9b becomes zero at $I_{tail} \approx 2.5\ mA$, it can be expected that the oscillation frequency is insensitive to small tail bias current modulation at this bias current. To verify this, a test setup was built where a weak interfering signal from an external signal source can be summed to the tail bias current or to the supply voltage source, and all other coupling between the modulating signal source and the test chip is suppressed to a negligible level. Figure 7.11 shows the measured spectrum of the prototype oscillator with two different tail bias current values, when a weak square wave current signal is added to the tail current. When the tail current is set to $2.5\ mA$, all sidebands are suppressed, and most of them vanish compleately below the phase noise level of the oscillator.

Finally, Figure 7.12 shows the corresponding spectra when the bias current source is undisturbed, but a low-level square wave voltage is summed to the supply voltage. Also in this case, at $I_{tail} = 2.5\ mA$ the sidebands are strongly suppressed, indicating that the VCO is much less sensitive to the voltage supply noise at this bias current.

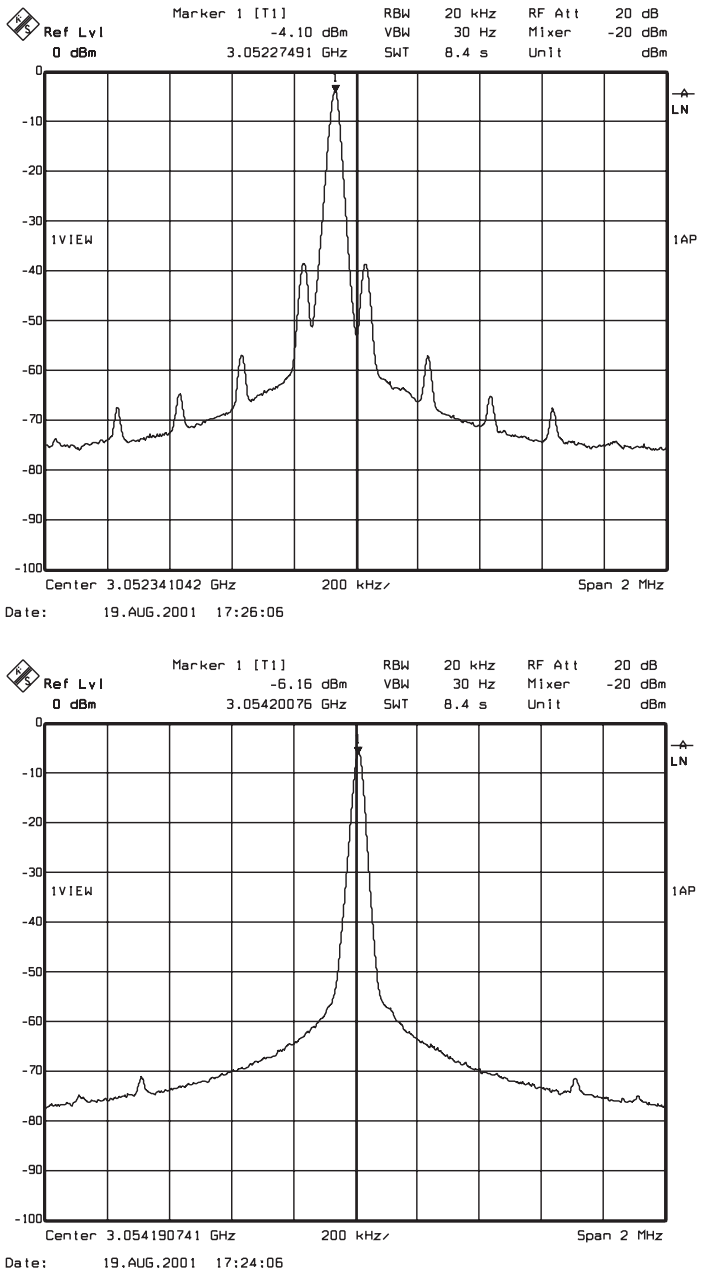


Figure 7.11: *The measured signal spectrum, when a* 1.2 μA_{pp} 100 kHz *square wave (*50% *duty cycle) is added to the tail bias current. (a)* $I_{tail} =$ 3.0 mA*, (b)* $I_{tail} = 2.5$ mA*. Because of the thermal drift of the n-well bias voltage source, the carrier frequency has slightly changed between the measurements.*

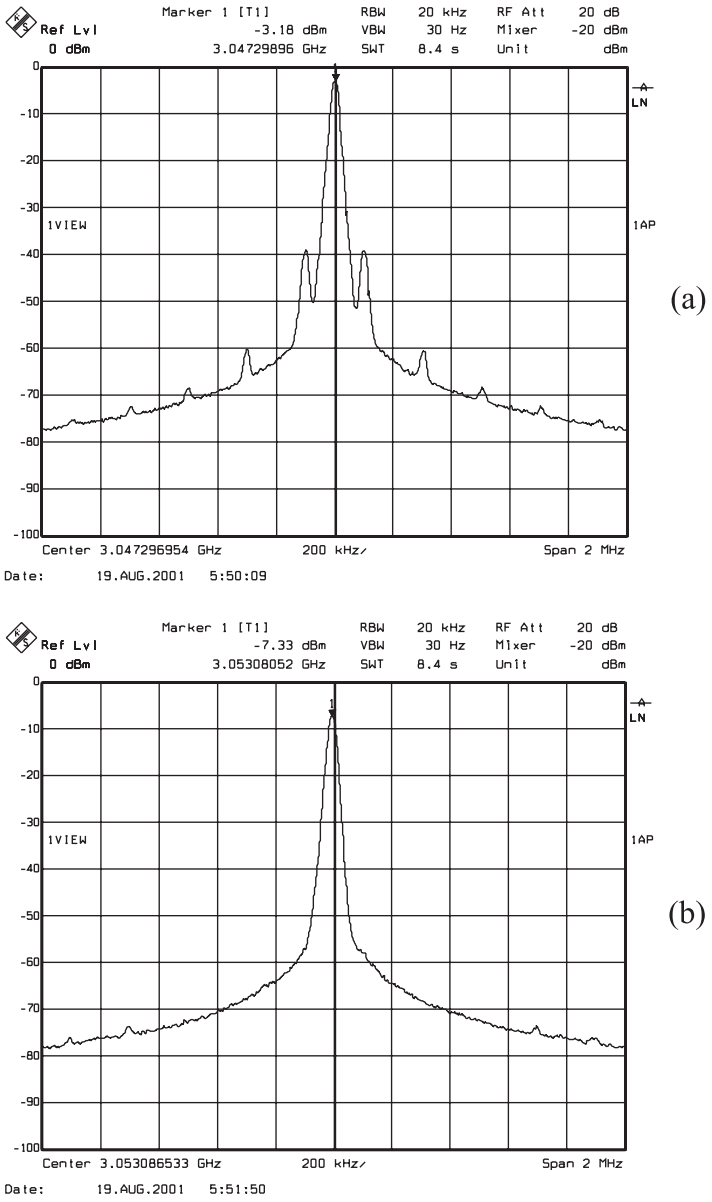


Figure 7.12: *The measured signal spectrum, when a* 20 mV_{pp} 100 kHz *square wave (*50% *duty cycle) is added to the* 3.3 V *supply voltage. (a)* $I_{tail} = 3.0\ mA$*, (b)* $I_{tail} = 2.5\ mA$*. Because of thermal drift, the carrier frequency has slightly changed between the measurements.*

7.5 Conclusions

The experimental results presented in this chapter show that it is possible to construct a fully integrated LC VCO circuit that is able to suppress the effects of bias source modulation. Despite of the unconventional design, no severe performance compromises are involved. The prototype VCO shows good performance in the terms of current consumption, phase noise level, and tunability, in addition to the enhanced interference tolerance. The proposed circuit is able to suppress the AM-FM conversion in the VCO core circuit itself, while most published works, that address the interference tolerance of the negative-G_m VCO, are focused on reducing the amplitude of the modulating signal in the bias source.

Even though it is relatively easy to describe the circuit operation in qualitative terms, it is more difficult to predict accurately the circuit behavior by simulations. According to the S-parameter measurements of the test devices on another test chip, the transition frequency of the minimum-length PMOS transistor in this process is only 9.3 GHz ($V_{DS} = -3.0\ V, V_{GS} = -3,3V$). Since the operating frequency of the prototype oscillator circuit is not much lower, it is obvious that the quasi-static simulations will not produce quantitatively correct results. However, the simulations indicate that the total tank circuit capacitance will drop by a small amount when one of the gain stage transistors is driven into the weak inversion region, and that the tank circuit capacitance will increase again when one of the transistors is driven into the non-saturation region.

The simulations and experimental measurement results show that the proposed CMOS VCO circuit topology provides the necessary voltage dependent capacitances for finding the amplitude level where the AM-FM conversion is minimized, as was presented in Chapter 6. The experimental results confirm that it is easy to find the operating conditions where the sensitivity to the bias current or supply voltage modulation is drastically reduced. Moreover, in this operating point, the phase noise level and the current consumption are acceptable, at least for radio systems with relaxed specifications.

Chapter 8

Characterizing Small MOSFETs

Since sub-micron MOS transistors provide little transconductance per unit gate length, the transisotrs in most MOSFET RF circuits tend to be large in size. Some typical circuits are the low-noise amplifier (LNA), the CMOS commutating switch mixer, the power amplifier, the VCO gain stage transistors, and RF buffer amplifiers. Often very large W/L (say, $W/L > 500$) is necessary to obtain the desired gain or the low channel impedance that is needed for RF signal switching. In order to reduce the gate resistance, the transistor is usually laid out as a multi-finger device. Since it also is easier to characterize large devices, most published works in RF characterization of MOSFET transistors present results from large multi-finger device measurements.

However, there are circuits where the RF response of small MOS transistors is interesting. Some examples of these circuits are the first stages of the frequency divider circuit in a PLL circuit, buffer circuits designed for low input capacitance, and bias circuits that provide the bias current for the RF transistors. Even though bias circuits are designed for providing DC current or DC voltage, the bias circuit transistor that actually is connected to the RF transistor is directly exposed to the RF signal, and will affect the impedance level of this node at high frequencies. Therefore, the output impedance of the bias circuit transistor at radio frequencies is sometimes an important factor that contributes to the RF stage gain and phase response.

It is relatively easy to extract many of the parasitic element values for large MOSFET devices, since most of the parasitic impedances, like the gate-drain capacitance and the gate finger resistance, will make a clear contribution to the measured and de-embedded device response. However,

it is usually difficult to extract the source and the drain contact resistances R_s and R_d with good accuracy with large transistors, since these resistances may even be lower than the contact resistance of the RF probe tip to the pad. Consequently, due to the probe contact resistance instability, especially if the probe pads are made of aluminum, the error in extracting them may be large. The error made in extracting R_s and R_d is seldom a concern with large devices since their values are small, and they contribute little to the overall RF response of the device. However, if the inaccurate results are used for estimating the response of narrow finger devices, the values of values of R_s and R_d must be multiplied by the scaling factor. In this case, the error made when extracting the terminal resistances is greatly amplified, and the resulting model for the narrow finger transistor will be unreliable.

Accurate RF characterization of MOSFET devices is in practice a challenging engineering task, since typical CMOS technologies provide only aluminum for the RF probe pad material. Traditionally, most integrated microwave circuit technologies use gold metallization, which is chemically inert and makes easily good contacts with the RF probe tips. Since aluminum spontaneously reacts with oxygen in the room temperature, the RF pads are always covered with a some nanometers thick aluminum oxide layer. Unfortunately, aluminium oxide is isolating and mechanically very hard. When the RF probe is pressed against the pad, the probe tip metal will penetrate the oxide layer, but it is very difficult to control the area of good galvanic contact. For this reason, the probe-pad contact resistance usually is relatively high, and the stability of the contact resistance is poor. The contact resistance may easily vary from 0.1 Ω to 10 Ω , depending on the length of the probe tip skate, number of touchdowns, how well the mechanical vibrations of the environment are isolated from the measurement setup, and numeruous other factors [45]. Therefore, the issues related to the use of aluminum pads must be carefully studied and taken into account already when the test fixture is designed.

The optimal equivalent circuit topology for modeling the substrate parasitics network depends on the number of transistor fingers, and on the way the bulk contacts and the individual transistor fingers are laid out [38]. Therefore, if the MOSFET RF characterization is carried out using large multi-finger devices, it is difficult to predict the contribution of the substrate network to the Y-parameters of small transistors. Instead, for reliable RF characterization of small MOSFET devices, small transistors should be measured, and the de-embedding and parameters extraction procedures must be designed to tackle with the special problems related with characterizing small devices.

8.0.1 DUT Stability During the S-parameters Measurement

If a large transistor is biased to some operating point where the transconductance is high, it may be difficult to avoid spontaneous oscillation of the transistor, since the test fixture and the RF cables that connect the test fixture to the network analyzer compose resonator circuits. The termination of the probe cables in the S-parameters test set is never perfect, which means that some of the signal, that the transistor has amplified, will reflect back from the test set to the transistor. If, at some frequency, the transistor behaves like a negative resistance that cancels the loss of the reflected signal during the round trip in the probe cable, and the signal phase shift equals to 360 degrees, the transistor will start to oscillate in that frequency. In practical measurement setups, there are also other sources of impedance discontinuities in the RF cables between the S-parameters tester and the RF probes, because of the connector adapters, 90 degree connectors, and bias tees. Although the network analyzer is able to mathematically correct the measurement results for the influence of at least some of these reflections after the Impedance Standard Substrate (ISS) calibration, the calibration does not remove the physical impedance mismatch from the RF cables. Therefore, even if the measurement setup is carefully built and calibrated, the transistor will see undesired transmission line resonators connected to the gate and to the drain, and will oscillate when the transistor gain is high enough to compensate for the round trip loss in one of the cables.

It is sometimes difficult to notice that the transistor is oscillating in the test fixture, since the resulting change in the transistor response is not necessarily dramatic. If a measurement instrument, like a spectrum analyzer, is connected to the system for monitoring this, the reflections from the the extra RF cable that is needed will make the system difficult to calibrate, and reflections from this cable may even become the reason of the circuit instability. However, measuring an oscillating transistor circuit will for sure result in unreliable data for the transistor model parameters extraction. The stimulating RF signal from the network analyzer will at some frequencies injection lock the oscillating transistor, while at the other frequencies the transistor will oscillate freely, or sometimes stop oscillating if the round trip gain drops below unity for some reason. The result would typically be S-parameters data that includes strange discontinuities in the measured S-parameters, especially in the phase data.

In general, large transistors that provide plenty of gain when biased in the saturation region, may suffer from this undesired oscillation in the test fixture. Small devices, that do not provide enough gain for starting up the oscillation, are easier to characterize when the transistor is operating in the high-gain regions.

8.0.2 Problems with Characterizing Small MOSFET Devices

When small MOSFET devices are characterized, some well-known and widely used expressions for calculating the device parasitics do not produce accurate results. For example, for relatively large multi-finger MOSFET devices, the gate resistance is often extracted by biasing the transistor to the linear region and strong inversion, measuring S_{11}, de-embedding the test fixture parasitics, and calculating the gate resistance from [38]

$$R_g\prime \approx \frac{Re\{Y_{11}\}}{(Im\{Y_{11}\})^2} \tag{8.1}$$

It turns out that this equation gives a good approximation of $R_g\prime$ only when the contributions of the channel resistance R_{ds} and the source and drain terminal resistances R_s and R_d to $Re\{Y_{11}\}$ are negligible[1]. Since R_g is proportional to the gate finger width W, while R_d, R_s, and R_{ds} are inversely proportional to W, these conditions will most often not hold for narrow finger devices.

Errors originating from the de-embedding procedure will play an important role when small devices are characterized. The MOSFET device RF response is usually measured in a test fixture that connects the microwave probe to the Device Under Test (DUT). The parasitic impedances of the test fixture are extracted separately, and the measured response of the DUT is corrected for the contributions from the fixture parasitics. The success of this de-embedding procedure depends on the magnitudes of the errors made with the fixture parasitics extraction, and the relative magnitudes of the test fixture parasitics to the DUT parasitic impedances. Since it is not possible to reduce the physical size of the microwave probes very much, the size of the test fixture is more or less fixed, and the contribution from the test fixture parasitics to the measured response of a small MOSFET device will be large. Therefore, the smaller the physical size of the DUT is, the better (more accurate) de-embedding method is needed.

The mechanical construction of the RF probe head and the RF pad pattern planarity in the test fixture may limit the precision of the S-parameters measurement, especially when the pads are made of aluminium. Figure 8.1 illustrates the problem of obtaining good galvanic pad contact with non-planar RF pads and a stiff probe construction. Even though penetrating

[1]The roles of R_s, R_d, and R_{ds} are usually not discussed when Equation 8.1 is deduced, since the contribution of the channel resistance to the distributed gate capacitor impdedance is not included. In addition, for wide gate finger transistors $R_s, R_d << R_g$.

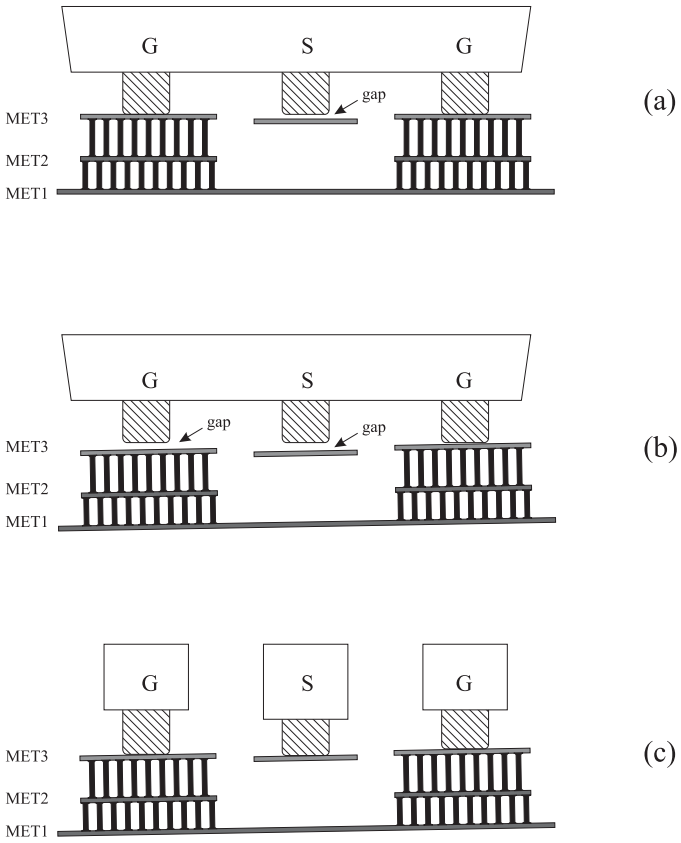


Figure 8.1: *(a) With a stiff probe construction, the middle probe tip does not make a good contact if the middle pad is slightly lower than the other pads, since the ground pads support the whole probe. (b) If the sample is tilted, only one of the three contacts of the solid probe is good. (c) If each probe tip has its own suspension, neither tilt nor non-planar pads affects the contact quality.*

the aluminum oxide layer on the surface of the pad is a known problem with all probe types, air-isolated RF probes with individual suspension for each probe tip are more likely to produce low and repeatable probe contact resistance.

A proper physically based method for extracting the substrate network element impedances is even more important with a small RF MOSFET device

than with a large device, since the value of the parasitic drain-bulk junction capacitance is very small with the small transistor. For this reason, the signal coupling from the transistor drain to the substrate network is weak, and the signal that is reflected back from the substrate network in the S_{22} measurement is very low. With large devices, the contribution of the substrate network to the measured and de-embedded Y_{22} signal may be easy to distinguish, but the corresponding signal from small device measurements easily drowns to the noise, and to the errors made with the network analyzer calibration and the test fixture parasitics de-embedding. It is usually not a good idea to increase the network analyzer signal power level in order to increase the level of the back reflected power, since this would invoke non-linearities in the transistor behavior, and the DUT behavior would no longer correspond to the behavior predicted by the transistor small-signal model[2]. Even if it was possible to increase the signal power, it would not reduce the errors originating from the de-embedding or calibration procedures. Even though it is possible to improve the signal-to-noise ratio (SNR) by averaging the network analyzer measurements, measurements of small transistors will most often suffer from bad SNR, which should be taken into account in the parameters extraction method, especially when extracting the substrate network parasitics.

It is common to extract the values of the substrate network elements by fitting the substrate network model response to the measured Y_{22} data, since it is difficult to extract them directly [41]. However, especially if the SNR is known to be bad, the number of parameters extracted by fitting should be minimized. After the measurements and de-embedding, the Y_{22} data will include noise and errors originating from the de-embedding and network analyzer calibration procedures. The contribution of the substrate network to the Y_{22} signal may not be much stronger than the signal distortion originating from these (random and systematic) errors. If the goal function is given too many degrees of freedom, the curve fitting algorithm will easily find parameter values that make the model network response to match the details that originate from these errors, rather than with the response from the substrate network itself. The result of the curve fitting in this case will be a set of non-physical parameter values. However, the remaining fitting error may still be very small, giving the false indication that the optimization process was successful. If this is allowed to happen, scaling of the resulting parametrized transistor model will result in unpredictable errors, even though the model with the extracted parameter values would match

[2]In contrast, the power level should be increased as much as possible when the de-embedding standards are measured. Since they are passive structures, they will not suffer from non-linearities when the power level is high. Since the data from these measurements are used for processing all DUT measurements data, the SNR should be maximized.

well the measured DUT behavior. For these reasons, one should choose the number of degrees of freedom in the goal function after a careful analysis of the SNR and accuracy of the measurement setup.

With MOSFET devices that have relatively wide gate fingers, reliable extraction of R_s and R_d is difficult, since these resistances tend to be very low compared with the other impedances in the same circuit. For narrow finger devices this is much less of an issue, since the values of R_s and R_d may even exceed the value of R_g. Since the values of R_s and R_d are relatively large for small devices, it is also important to extract them correctly, since these extracted values are also used for extracting some of the other transistor parameters.

Another issue with narrow gate finger devices is that the part of the polysilicon gate that resides outside the diffusion area may make a significant contribution to the total gate-bulk capacitance C_{gb}. The fringing capacitance of the conductors that connect the gate fingers will also increase the parasitic capacitance from the gate node to the bulk. While these components are often negligible with large devices, they should be taken into account when small devices are measured. Since these capacitances are very small, it is difficult to include them into the transistor model and to extract values for them. In this work, these capacitances are treated as another component of the gate-bulk capacitance.

8.1 Modeling the Small-signal MOSFET Operation

Spice-like simulator programs model the transistor behavior with compact models, which means modeling the dominating physical effects with parametrized analytical expressions. Even though the most advanced compact models describe the device behavior very well at moderately high frequencies, their performance is known to be limited at frequencies where the extrinsic parasitics of the transistor significantly contribute to the transistor response [38]. In particular, signal coupling from the drain finger to the substrate will change the output admittance of the transistor, and the gate finger resistance and other resistive components will contribute to the resistive part of the input impedance. Since most well-known compact MOSFET models do not include these effects, they are not reliable when simulating a circuit at high frequencies.

Another known method of simulating the dynamic device behavior is to model the physical transistor structure with a dense two-dimensional or

three-dimensional mesh and solve the charge carrier distribution and the electric field strength numerically in each node, based on the differential equations that relate the electric fields and charge carrier densities. Although this method describes the physics of the device very well, it requires very much CPU power and memory compared with the compact modeling approach, making it unsuitable for large circuit simulations. In addition, it is usually difficult to obtain detailed information about the transistor structures from the foundries, which makes this method difficult to use with circuit designs that employ commercial processing.

The third well-known approach to model the MOSFET high-frequency behavior is to measure the response of test transistors at many different operating conditions, and determine the transistor response in a circuit by using the measured results. The problem with this method is that it needs very much CPU power and memory. Therefore, simulating circuits with may transistors is time-consuming.

The rest of this chapter will discuss modeling the MOSFET in an analog simulator with a compact model and a separate parasitics network. The discussion reveals that when the transistor operates in the linear region, it becomes reciprocal. This property can be used for checking if the model equations are deduced correctly, and it can also be used for improving the accuracy of the parameters extraction. In addition, a new method for characterizing MOS transistors and calculating the parameters a high-frequency MOSFET model is presented.

8.1.1 Modeling the Gate and Channel as a Double Distributed RC Transmission Line

The value of the intrinsic transistor channel resistance is a strong function of the terminal voltages in a MOSFET. If a high frequency signal source is driving the transistor gate, the AC signal current flowing through the gate capacitor has to return to the source and drain electrodes through the channel, which is the bottom electrode of the gate finger capacitor. The AC current flowing in the channel is a manifestation of the charge redistribution in the channel, due to the change in the voltage across the gate finger and the channel. Therefore, the conductivity of the channel will contribute to the real part of the MOSFET input impedance[3]. Even though

[3]Note: The drain current is also flowing through the channel together with the signal current through the gate oxide capacitor. Since the drain current is correlated with the gate-source voltage, knowing the value of the channel sheet resistance alone in the given bias point is not sufficient for calculating the contribution of the channel to the input resistance of the device. In addition to the channel resistance, the transconductance of the device must be taken into account.

the channel resistance is very low under some bias conditions and does not contribute much to the real part of the input impedance during small-signal operation, at low gate overdrive voltages the channel resistance is high, and will significantly slow down the redistribution of the channel charge. A proper model for the input impedance under varying bias conditions, and especially under large-signal operation, must take into account the effect of the varying channel resistance.

Many different methods for modeling the effects of the gate resistance and the other parasitic elements to the input admittance of the transistor under high frequency small-signal operation have been proposed in the literature. Most of the proposed models employ high-frequency equivalent circuit diagrams that describe the transistor parasitics with lumped capacitors and resistors. While most of these methods do take into account the distributed resistance of the polysilicon gate finger, the corresponding distributed RC structure under the gate oxide, consisting of the gate oxide and the transistor channel, is seldom discussed. The contribution from the channel is usually taken into account by assigning the gate resistor an "effective gate resistance" value, that includes also the effect of the transistor channel resistance. The manifestations of this compromise are that the measured gate resistance exceeds the gate finger resistance that is calculated from the polysilicon sheet resistance and the geometry of the gate finger, and that the resistive part of the transistor input impedance does not equal the effective gate resistance under all bias conditions.

The following section desicribes the transistor gate finger – channel structure as a capacitor whose both terminals are resistive plates. This approach helps in understanding the voltage dependency of the transistor input impedance. The discussion shows that the transistor channel may sometimes be the dominant voltage dependent resistive component of the transistor input resistance.

8.1.2 MOSFET Gate Capacitor with Two Resistive Electrodes

The polysilicon gate finger, the gate oxide, and the MOSFET channel resistance together compose a distributed RC transmission line. Figure 8.2a shows a MOSFET under Y_{11} measurement. Figure 8.2b shows the cross section of the transistor along the gate finger. The gate oxide separates the resistive polysilicon gate finger from the conducting transistor channel. Since the AC signal will suffer from voltage drop when the signal current is flowing in the resistive capacitor plate materials, the signal current tends to concentrate on the region closest to the gate contact. Assuming that

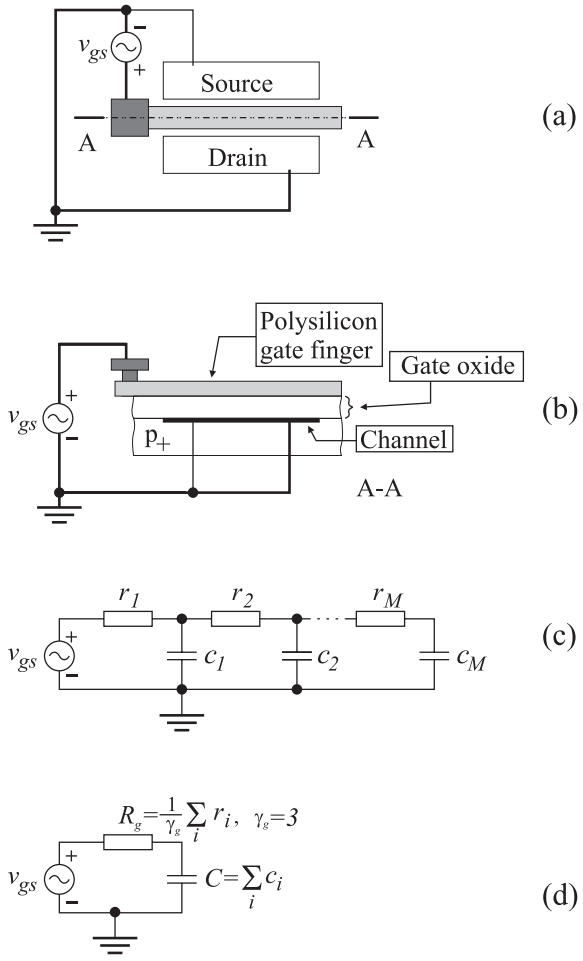


Figure 8.2: *(a) A one-finger MOSFET with one gate contact. The drain and source are AC grounded for the* Y_{11} *measurement. (b) The cross section A–A. The polysilicon gate finger with finite resistivity composes the upper electrode of the distributed capacitor, and the conducting channel under the gate oxide is the bottom electrode. The channel is grounded from both drain and source sides. (c) A lumped element equivalent diagram for modeling the gate RC transmission line, assuming that the transistor channel conductivity is very high, compared with the polysilicon gate. (d) An RC circuit whose input impedance equals to the input impedance of the transistor, when the transistor channel conductivity is high.*

the transistor channel conductivity is much higher than the gate finger conductivity, it is possible to approximate the input impedance of this distributed RC transmission line with the $2M$-element RC network shown in Figure 8.2c, where Σc_i is the total gate oxide capacitance, $r_i = R_g\prime/M$, and $R_g\prime$ is the gate finger resistance calculated from the gate polysilicon sheet resistance and the gate finger dimensions. Moreover, the input impedance of this RC network can be modeled with the two-element RC network of Figure 8.2d. The value of the resistor R_g can be shown to be [42][43]

$$R_g = \frac{1}{\gamma_g}\Sigma r_i \tag{8.2}$$

Here, $\gamma_g = 3$ since only one end of the gate finger is connected to the signal source v_{gs}. Figure 8.3 shows the corresponding distributed RC transmission line for the transistor when both ends of the gate finger are connected to the signal source. Also in this case, if the channel resistance is negligible, we can model the input impedance of the intrinsic transistor with a two-element RC network with R_g given by Equation 8.2, if the value of γ_g is changed to $\gamma_g = 12$.

If the resistivity of the bottom electrode (the transistor channel) is so high that it will make a significant contribution to the real part of the measured input impedance, the signal current distribution in the transistor channel must be taken into account. In this case, the RC networks of Figures 8.2c and 8.3c do not model the distributed gate oxide capacitor correctly. Figure 8.4 shows how the signal current path can be modeled with another, more complicated, RC network in this case. Since the direction of the signal current flow in the transistor channel is perpendicular to the current flow in the gate finger, the resulting signal current distribution problem becomes two-dimensional. Note that if the channel resistor values are set to $r_{dsi,j} = 0\ \Omega$, this network becomes equal to the network of Figure 8.2c, and its input impedance can be calculated with the model of Figure 8.2d, using $\gamma_g = 3$. If the gate finger resistor values are set to $r_{gi} = 0\ \Omega$, the network reduces to the network of Figure 8.5. In this case, the circuit topology corresponds to the equivalent circuit of Figure 8.3c, and the equivalent input impedance of the circuit can be calculated using the model of Figure 8.3d. Figure 8.6 shows the RC circuit that is equivalent with the RC network illustrated on the top of the transistor sketch in Figure 8.4.

The RC network models presented in this section give some important qualitative understanding of the transistor input impedance:

1. The resistance seen in series with the gate capacitor is a sum of two components, the gate polysilicon resistance and the channel resistance. Since

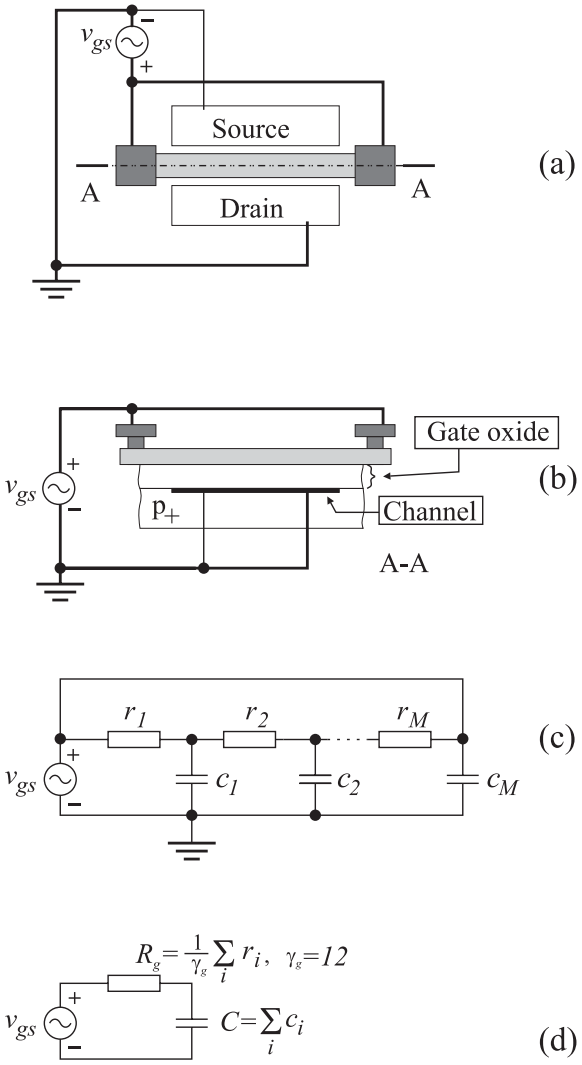


Figure 8.3: *(a) A one-finger MOSFET with two gate contacts. (b) The cross section A–A. Since both ends of the gate finger are contacted to the signal source, only the region in the middle of the gate finger suffers from voltage drop due to the resistivity of the capacitor electrodes. (c) A lumped element equivalent diagram for modeling the gate RC transmission line, assuming that the transistor channel conductivity is very high, compared with the polysilicon gate. (d) An RC circuit whose input impedance equals to the input impedance of the transistor, when the transistor channel conductivity is high.*

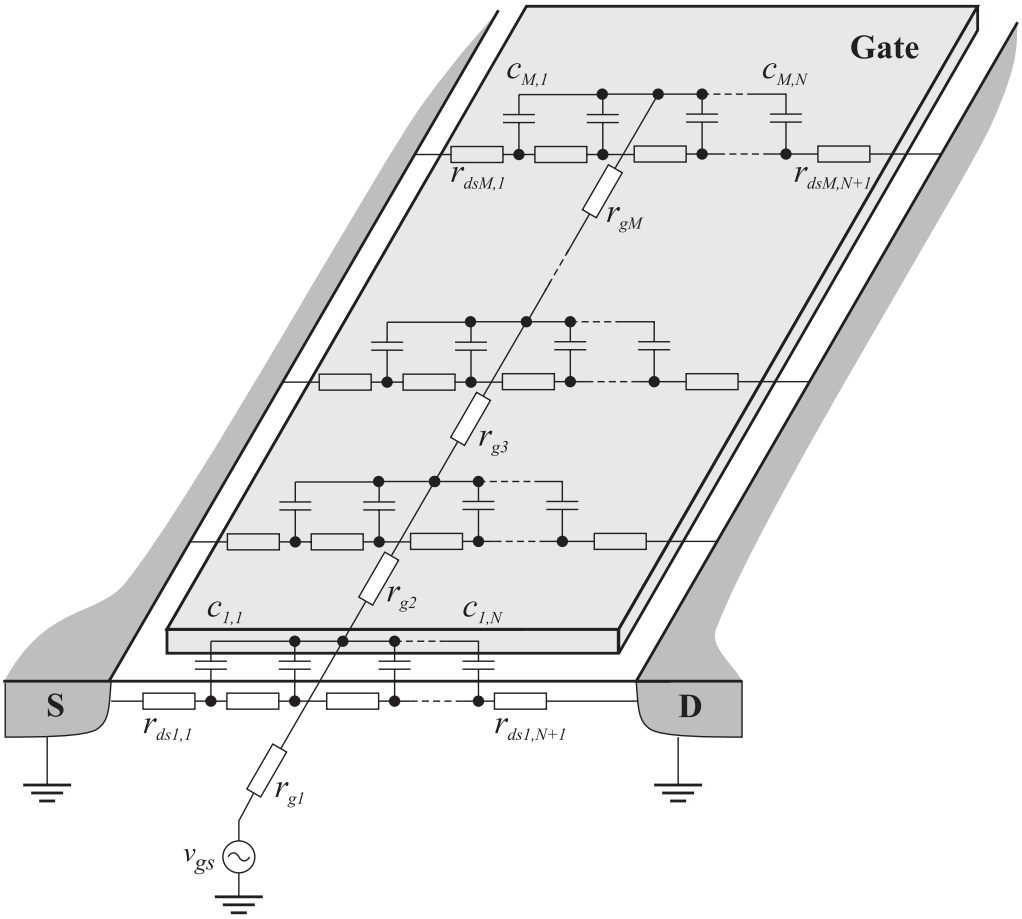


Figure 8.4: *A MOSFET under the Y_{11} measurement. Since, in general, both capacitor plates are resitive, the signal current from the signal source will flow through one distributed resistor above the gate oxide, and through another in the transistor channel. The resistors r_g model the resistance of the polysilicon gate finger, and resistors r_{ds} model the resistance of the transistor channel. The RC network models a transistor whose gate finger has only one contact.*

the channel resistance is a non-linear function of the instantaneous gate-source and the drain-source voltages, the resistive part of Z_{11} depends on them. Since the channel resistance changes over many orders of magnitude when the gate-source voltage is changed from zero to the strong inversion

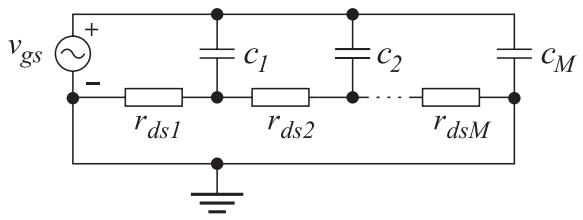


Figure 8.5: *An RC network representing the gate-channel capacitor when the gate finger resistance is equal to zero.*

region, modeling the input resistance with one fixed resistor will produce large errors when simulating the large signal response of the transistor.

2. The voltage drop in the gate finger material is due to the gate AC current only. In the transistor channel, the gate current flows together with the drain current. Therefore, the local channel potential will depend on the transconductance of the device. The voltage gain of the transistor circuit (the value of the drain load impedance) will also contribute to it, since the value of the drain voltage determines if the transitor is in the saturation with a given gate voltage.

3. The transistor gate finger length L is an important parameter contributing to the voltage dependency of the transistor input resistance. If the finger is long, the channel is also long. In this case, the gate polysilicon finger resistance is low, while the channel resistance is high. Consequently, the effect of the channel resistance on the input resistance of the transistor is emphasized.

4. R_{ds} is a strong function of the gate bias voltage. When $V_{ds} = 0\ V$, the transistor channel works as an almost linear voltage controlled resistor, and the channel resistivity is approximately the same everywhere in the transistor channel. In this case, it will be relatively easy to calculate the channel resistance contribution to the real part of the transistor input impedance. When $V_{ds} \neq 0\ V$, the transistor channel resistance is not distributed evenly along the gate length L. Finally, in the saturation region, the channel is even pinched off close to the drain, meaning that a small region of the channel has very high impedance, compared to the other parts of the channel. The non-uniform distribution of the channel charge density in most practical operating conditions of the transistor makes it difficult to calculate the contribution of the channel resistance to the input impedance of the transistor, or to determine the values of r_{ds} in the RC network of Figure 8.6.

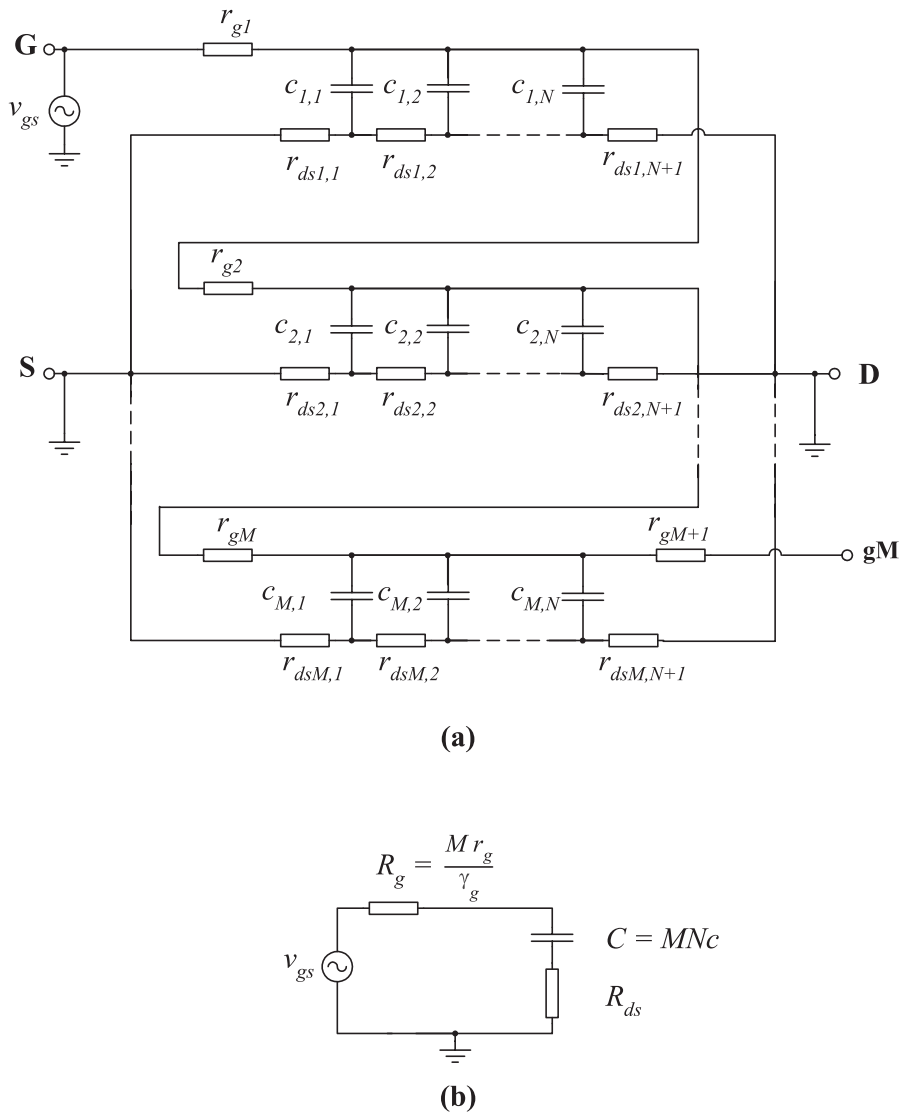


Figure 8.6: *(a) A lumped element RC network for simulating the MOSFET gate capacitor as a double distributed RC transmission line. If both ends of the transistor gate finger are connected to the signal source, node* **gM** *should be connected to node* **G**. *Otherwise,* **gM** *must be left floating. (b) A simple RC circuit for modeling the input impedance of the MOSFET.*

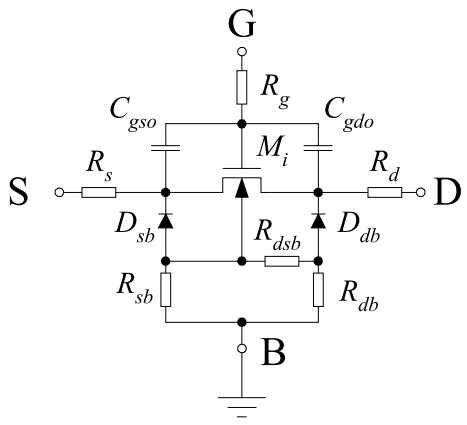


Figure 8.7: *A common approach for modeling the high-frequency behavior of a MOSFET in an analog simulator. The simulator compact model is employed for modeling the intrinsic transistor, and the parasitics of the transistor are modeled separately.*

8.1.3 Quasi-static MOSFET Small Signal Model with External Lumped Parasitics

Figure 8.7 shows a well-known approach for simulating the MOSFET behavior at high frequencies in an analog circuit simulator. The idea is to use an established compact model, such as BSIM3V3 or EKV, for modeling the intrinsic device M_i, and a separate external parasitic devices network for modeling the charge storage effects in the pn-junctions, the other parasitic capacitors, voltage drops in the electrode resistances, and the signal coupling through the substrate. Figure 8.8 shows the corresponding equvalent diagram of the MOSFET in the common source configuration. The circuit includes the necessary intrinsic and extrinsic elements for modeling the circuit of Figure 8.7 under small-signal conditions when the intrinsic device operates under the quasi-static conditions [39] [41].

For extracting the values of the elements in the equivalent diagram of Figure 8.8, it is possible to measure the Y-parameters response of prototype transistors, and fit the element values to the measured response. However, since the number of elements in the circuit is large and the measurements data will include some errors, fitting all varables simultaneously would probably lead to large errors. In order to avoid the problems with simultaneous fitting, it is possible to measure the transistors under special bias conditions, where the values of some of the equivalent circuit elements are negligible. Once some of the element values are solved, it is easier to

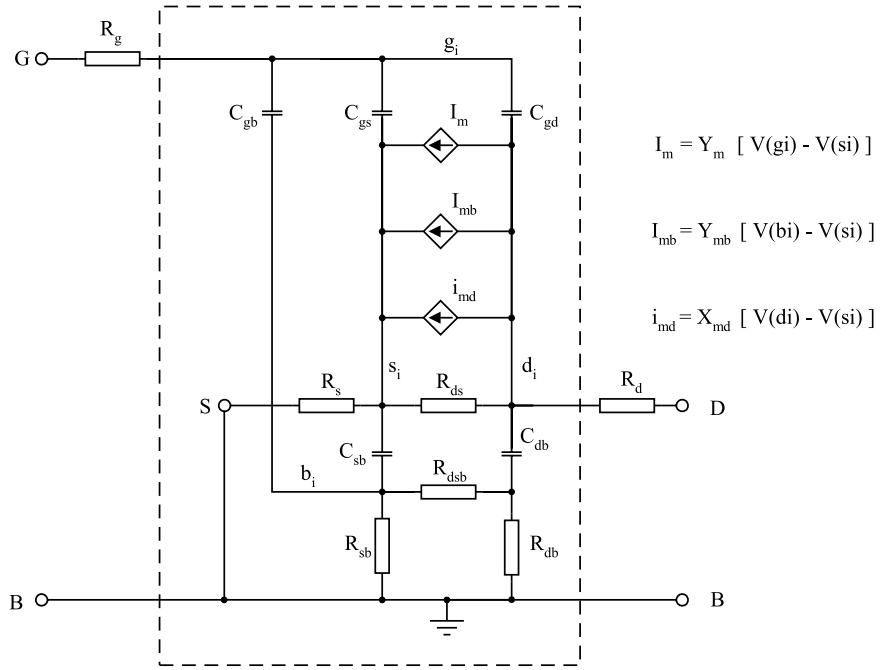


Figure 8.8: *An equivalent diagram for modeling the MOSFET in all operating regions in the common source configuration. The circuit in the dashed-line box is used for the Y_{22} analysis.*

extract the remaining values with acceptable precision.

When the transistor is operating in the linear region ($V_{ds} = 0\ V$) and strong inversion ($V_{gs} \gg V_{th}$), the equivalent diagram of Figure 8.8 can be greatly simplifed. Because of the symmetry, the transadmittances Y_m, Y_{mb}, and X_{md} become zero, and all controlled sources vanish from the equivalent circuit. The remaining network includes only resistors and capacitors, and is therefore reciprocal. In addition, since the drain and the source are in the same potential, the voltage dependent parasitic capacitances and resistances associated with the the source fingers must be equal to the corresponding drain parasitics, if the transistor layout is symmetrical. This symmetry reduces the number of degrees of freedom in the parameters fitting process.

When the transistor is operating in the saturation region and in strong inversion, the value of R_{ds} is high. Therefore, a significant part of the signal in the drain node is coupled through the drain-bulk capacitor to the substrate network, which makes it possible to extract the substrate network

element values. For measuring the Y_{22} parameter, the gate of the transistor is shorted to the ground, which simplifies the equivalent circuit.

Since the simulator user does not have access to the intrinsic transistor model, it is not possible to model the gate-channel capacitor as a MOS capacitor with two resistive electrodes. Instead, the intrinsic gate-channel capacitor is described as the two capacitors C_{gs} and C_{gd} (Figure 8.8), and the resistance associated with the resistive part of the input impedance is described with the equivalent gate resistance R_g. As long as the resistance of the polysilicon gate dominates the real part of the input impedance, it is reasonable to model the input impedance with one fixed resistor. However, if the signal swing is large in the transistor gate or drain, the contribution of the channel resistance should be taken into account, for example by making R_g to depend on the gate-source and gate-drain votages.

8.1.4 Input Capacitance of the Common Source Stage

The circuit of Figure 8.9a shows an equivalent diagram of the MOSFET for the Y_{21} analysis, assuming that the transistor is operating in the linear region and in the strong inversion. This circuit is a simplified version of the equivalent circuit in Figure 8.8. Since the parasitic drain-bulk and source-bulk capacitances are small, we can assume that $|(j\omega C_{sb})^{-1}| \gg R_s$ and $|(j\omega C_{db})^{-1}| \gg R_d$ at frequencies below 10 GHz. Therefore, we can remove all elements that model the substrate network from the circuit of Figure 8.8. All controlled sources vanish due to the symmetry of the transistor in this bias point. The capacitances C_{f1} and C_{f2} represent the capacitances due to the conductors that connect the gate fingers together, and the gate polysilicon that does not overlap the diffusion region. In order to make the analysis simple, we first ignore C_{f1} and C_{f2}, but we keep in mind that they will introduce some error by increasing the input capacitance slightly. Since they are small compared to the other capacitances, the error will not be large.

The circuit of Figure 8.9a, without C_{f1}, C_{f2} and R_{ds}, is often used for modeling the transistor in the Y_{11} measurement. Due to the symmetry of the layout, R_d is equal to R_s, and C_{gs} is equal to C_{gd}. The voltage drop across R_{ds} is zero, and the value of R_{ds} should not contribute to the value of Y_{11}. However, this simplified equiavlent circuit does not take into account that some of the gate AC current will flow in the channel, since the gate-channel capacitor is a distributed device. Therefore, the value of R_{ds} will contribute to the real part of the input impedance. In this work, C_{gs}, C_{gd}, R_g, and R_{ds} are replaced with the RC network of Figure 8.6a, in order to model the distributed gate-channel capacitor. After simplifying

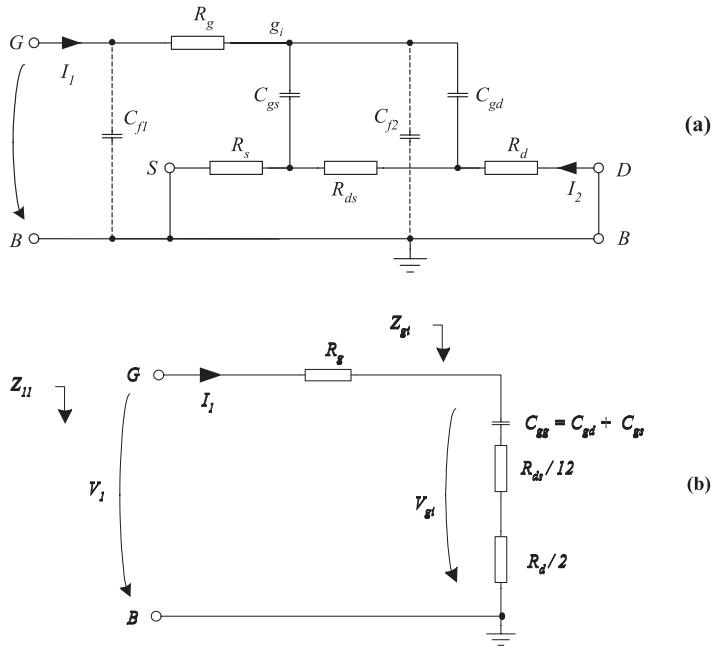


Figure 8.9: *Small signal equivalent diagrams of a MOSFET operating in the linear region and in strong inversion: a) an equivalent diagram for Y_{21} analysis, b) a modified circuit for Y_{11} analysis.*

the RC network using the equivalent circuit of Figure 8.6b, we obtain the equivalent circuit of Figure 8.9b. The input port impedance is

$$Z_{11} = R_g + \frac{R_{ds}}{\gamma_{ds}} + \frac{R_d}{2} - j\frac{1}{\omega C_{gg}} = a + jb, \tag{8.3}$$

where

$$\begin{cases} a = R_g + \frac{R_{ds}}{\gamma_{ds}} + \frac{R_d}{2} \\ b = \frac{-1}{\omega C_{gg}} \\ C_{gg} = 2 \cdot C_{gd} \end{cases} \tag{8.4}$$

and $\gamma_{ds} = 12$, since $V_{ds} = 0\ V$. The input admittance is

$$Y_{11} = \frac{1}{Z_{11}} = \frac{1}{a + jb} = \frac{a - jb}{a^2 + b^2} \tag{8.5}$$

The imaginary part of Y_{11} is

$$Im\{Y_{11}\} = \frac{-b}{a^2+b^2} = \frac{\frac{1}{\omega C_{gg}}}{(R_g + \frac{R_{ds}}{\gamma_{ds}} + \frac{R_d}{2})^2 + \frac{1}{(\omega C_{gg})^2}} \tag{8.6}$$

With typical values of the parasitic resistances and capacitances in short-channel MOSFET devices, with high gate bias voltage, and at frequencies below 10 GHz,

$$(R_g + \frac{R_{ds}}{\gamma_{ds}} + \frac{R_d}{2})^2 \ll \frac{1}{(\omega C_{gg})^2} \quad \Leftrightarrow \quad a^2 \ll b^2 \tag{8.7}$$

which leads to

$$Im\{Y_{11}\} \approx \omega C_{gg} \Leftrightarrow C_{gg} \approx \frac{Im\{Y_{11}\}}{\omega} \tag{8.8}$$

Since in the previous analysis the transistor operates in the strong inversion, the gate-bulk capacitance C_{gb} is very small compared to C_{gs} and C_{gd}. For large transistors, C_{gs} and C_{gd} are much larger than C_{f1} and C_{f2}, and $C_{gg} \approx C_{gs}+C_{gd} \approx C_{ox}$, which is the reason that Equation 8.8 is widely used for extracting the gate oxide capacitance using large transistor structures.

Capacitance C_{gg} represents the total transistor input capacitance, including C_{gd}, C_{gs}, C_{gb}, C_{f1}, and C_{f2}. Since in many circuit analysis problems the total input capacitance of the transistor is the interesting variable, the input capacitance extracted from Equation 8.8 can sometimes be directly used for comparing designed and measured circuit perfomrance. In addition, if reasonable approximations for R_d, R_g, and R_{ds} are available, solving C_{gg} directly from Equation 8.6 will avoid the approximation of Equation 8.7. However, if we want to use the modeling approach of Figure 8.7, it is necessary to assign the total capacitance C_{gg} to the individual values of the equivalent circuit capacitors, which will result in additional errors. Even though the resulting circuit simulator model is suitable for simulating large circuits, it is often questionable if it is necessary to use a compact model -based approach for modeling an RF circuit that includes very few transistors.

From Equation 8.6 we can see that resistances R_g, R_d, and R_{ds} contribute to the extracted value of C_{gg}. The approximation of Equation 8.7 discards

this information, which makes it somewhat unclear if Equation 8.8 gives a good approximation of C_{gg} when the transistor gate finger geometry or the gate bias voltage is changed, or if the low-field mobility of the carriers in the channel is changed. It turns out that the approximation is valid also with transistors that have relatively narrow gate fingers, if the channel resistance R_{ds} is low. Even though R_d will increase when the gate width is decreasing, the value of C_{gg} will decrease by the same factor, and the term $(\omega C_{gg})^{-2}$ will still dominate the denominator of Equation 8.6 for practical small RF transistor designs when $\omega < 2\pi \cdot 10\ GHz$. Increasing the gate length L will increase R_{ds} and it will also increase the oxide capacitance by the same factor. Therefore, if L is increasing, the approximation will fail soon. However, since the channel length of the transistors that are used in MOSFET RF circuits is always close to the minimum length, this usually is not an important issue. Since the the channel resistance R_{ds} is inversely proportional to the low-field mobility, PMOS transistors will violate the approximation easier. Note that with low gate bias voltage the value of R_{ds} alone may become so high that the condition of Equation 8.7 does not hold.

8.1.5 Gate-Drain Capacitance in the Linear Region and Strong Inversion

For extracting the value of C_{gd}, one should employ data that actually represents the AC coupling between the gate and the drain. Even though C_{gd} could be extracted from the equivalent diagram of Figure 8.9b and the measured Y_{11} data, the result would be inaccurate, since the Y_{11} data includes contributions from the unmodeled capacitances C_{f1} and C_{f2}. However, if we use the circuit of Figure 8.9a, model the gate-channel capacitor with the network of Figure 8.6b, and ignore C_{f2}, we can write for the impedance from node g_i to the ground:

$$Z_{gi} = \frac{R_{ds}}{\gamma_{ds}} + \frac{R_d}{2} - j\frac{1}{2\omega C_{gd}} \tag{8.9}$$

The voltage in node g_i is then

$$V_{gi} = V_1 \frac{Z_{gi}}{Z_{gi} + R_g} \tag{8.10}$$

Since the circuit is symmetric, the magnitude of the current I_2 must be 50% of I_1 in the circuit of Figure 8.9b. Therefore,

$$I_2 = -\frac{1}{2}\left(\frac{V_{gi}}{\frac{R_{ds}}{\gamma_{ds}} + R_d - j\frac{1}{\omega C_{gg}}}\right) \tag{8.11}$$

Combining Equations 8.9, 8.10, and 8.11 we obtain

$$Y_{21} = \frac{I_2}{V_1} = \frac{-1}{\frac{2R_{ds}}{\gamma_{ds}} + R_d + 2R_g - j\frac{1}{\omega C_{gd}}} \tag{8.12}$$

The imaginary part of Y_{21} is

$$Im\{Y_{21}\} = \frac{-\frac{1}{\omega C_{gd}}}{(\frac{2R_{ds}}{\gamma_{ds}} + R_d + 2R_g)^2 + \frac{1}{\omega^2 C_{gd}^2}} \tag{8.13}$$

Employing the approximation of Equation 8.7, and then solving for C_{gd}, we obtain

$$C_{gd} \approx -\frac{Im\{Y_{21}\}}{\omega} \tag{8.14}$$

which is a well-known equation for extracting C_{gd}. This expression is often accurate enough in the sense that the error originating from the approximation is small. However, even if the measurements are carried out carefully, the dominating source of error may not be the approximation, but the network analyzer calibration error, external noise signals coupled to the measurement setup, internal noise of the network analyzer electronics, or errors originating from the less-than perfect de-embedding measurements. If the dominating source of error is random in nature, it is possible to improve the accuracy of the extracted value of C_{gd} by employing the fact that the transistor circuit is reciprocal when $V_{ds} = 0\ V$. For this reason, the measured values of Y_{12} and Y_{21} should be equal at all measured frequency points. Any difference between the measured values of Y_{12} and Y_{21} must originate from measurement errors, and the average of Y_{12} and Y_{21} will then be a better estimate for the true Y_{12}, than the measured Y_{12} alone. Therefore, instead of Equation 8.14, the value of C_{gd} may be extracted from

$$C_{gd} \approx -\frac{Im\{Y_{12}\} + Im\{Y_{21}\}}{2\ \omega} \tag{8.15}$$

Equation 8.15 assumes that there are no controlled sources in the equivalent diagram, which is is a reasonable assumption as long as $V_{ds} = 0\ V$. For extracting C_{gd} when $V_{ds} \neq 0\ V$, Equation 8.14 should be used.

8.1.6 Gate-bulk Capacitance

Since the transistor drain-source bias voltage was set to zero in the previous analysis, the transistor is fully symmetrical. Therefore, the gate-source capacitance must equal the gate-drain capacitance. Using Equations 8.8 and 8.15 we can solve the gate-bulk capacitance:

$$C_{gb} \approx C_{gg} - 2C_{gd} \tag{8.16}$$

This value of C_{gb} includes also the contributions from C_{f1} and C_{f2}. The approach taken in this work is to make sure that most of the resulting error, when extracting the parasitic capacitance values, will accumulate to the extracted value of C_{gb}. Comparing the extracted values of C_{gb} and C_{gd} we obtain a coarse indication of the precision of the parameter extraction method. The value of C_{gb} should be positive and much smaller than C_{gd}. Since C_{gb} is very small for a device that operates in the strong inversion, it will be easy to see if the unmodeled fringing capacitances have increased the total input capacitance significantly. Since the exact value of C_{gb} is usually less important when analyzing circuits where the MOSFET operates in the strong inversion, some error in the extracted value of this parameter is acceptable.

8.1.7 Drain and Source Resistances

Considering the equivalent diagram of Figure 8.9b, it is not possible to extract the values of R_d, R_{ds}, and R_g from the measured Z_{11} data. Since the three resistances are in series, it is not possible to distinguish their relative magnitudes. For extracting R_d and R_{ds}, we should use a circuit where R_g is eliminated and the effect of R_{ds} can be separated from R_d. Reference [41] proposes combining the results of Y_{11} and Y_{21} analysis for extracting R_g, R_d, and R_s. Unfortunately, the proposed equations are derived by combining equations that originate from two different equivalent diagrams. A clear sign that the resulting eqations are incorrect is that the equation for extracting R_d includes the nonzero coefficient $|Re\{Y_{21}\} - |Re\{Y_{12}\}|$. However, all networks that were used for deriving the equation are reciprocal, and therefore Y_{12} must always equal to Y_{21}, if the transistor under the current bias conditions can be described with the equivalent diagrams that include only resistors and capacitors. Any difference between the measured Y_{12} and Y_{21} must arise from inprecise measurements or non-zero values of I_m, I_{mb} or i_{md}, rather than the presence of non-zero R_d.

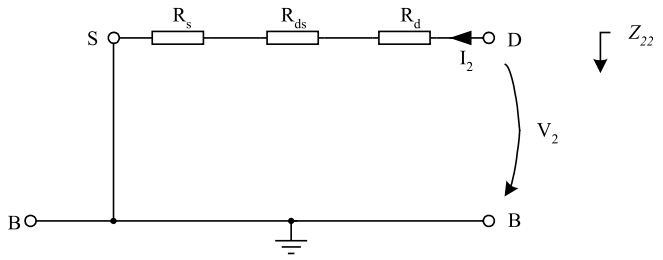


Figure 8.10: *A MOSFET equivalent circuit for the Z_{22} analysis in strong inversion and low operating frequency, with $V_{ds} = 0\ V$. The channel conductance $g_{ds} = 1/R_{ds}$ is proportional to the gate overdrive voltage, while R_s and R_d depend only weakly on the gate voltage.*

This thesis proposes extracting the values of R_d and R_{ds} from the measured Z_{22} data. When the MOSFET operates in the strong inversion and the drain-source voltage is zero, the channel conductance of the intrinsic transistor is high and it is proportional to the gate-source overdrive voltage:

$$g_{ds} = 1/R_{ds} = K(V_{gs} - V_t) \tag{8.17}$$

where $K = \mu C_{ox} W/L$. In addition, the channel resistance is very low compared with the impedances of the capacitances at low frequencies. For the Z_{22} analysis at low frequencies, in the strong inversion, and with $V_{ds} = 0\ V$, the equivalent diagram of Figure 8.8 is simplified to the circuit of Figure 8.10.

While the channel resistance R_{ds} is a strong function of the gate-source overdrive voltage, the terminal resistances R_d and R_s depend rather weakly on the gate voltage. Therefore, we can model the output impdedance of the transistor with

$$Z_{22} = 2R_d + 1/[K(V_{gs} - V_t)] \tag{8.18}$$

By measuring Z_{22} at a low frequency and fitting the data with Equation 8.18 at several different gate voltage values in the strong inversion region, we can extract values for R_d and K. Due to the symmetry of the device, the source

and the drain electrode resistances must be equal, $R_d = R_s$. Since K is now known, it is possible to calculate an estimate for R_{ds} at any gate voltage in the strong inversion and linear operating region. Finally, the difference of the measured Z_{22} response and Equation 8.18 gives an indication of how R_d and R_s depend on the gate voltage.

8.1.8 Gate Resistance

As is discussed in section 8.1.1 and in [40] [41], the resistive transistor channel as a part of the gate RC transmission line introduces an additional resistive component to the input resitance of the MOSFET. Therefore, the MOSFET input resistance R_{gg} does not describe only the effect of the resistive gate finger, but represents all resistive losses of the transistor input impedance.
For extracting the value of R_{gg}, we find the real part of Y_{11} from Equation 8.5:

$$Re\{Y_{11}\} = \frac{a}{a^2 + b^2} \tag{8.19}$$

Using Equations 8.6 and 8.19 we can write

$$\frac{Re\{Y_{11}\}}{(Im\{Y_{11}\})^2} = \frac{a(a^2 + b^2)}{b^2} \approx a = R_g + \frac{R_{ds}}{\gamma_{ds}} + \frac{R_d}{2} \tag{8.20}$$

where Equation 8.7 was used for the approximation. Assuming that

$$\frac{R_{ds}}{\gamma_g} + \frac{R_d}{2} \ll R_g, \tag{8.21}$$

Equation 8.20 reduces to

$$R_g\prime \approx \frac{Re\{Y_{11}\}}{(Im\{Y_{11}\})^2}, \tag{8.22}$$

which is commonly used for extracting the gate finger resistance R_g. However, the condition of Equation 8.21 does not necessarily hold for transistors whose gate fingers are narrow, or if the gate bias voltage is low. Since R_g is proportional to W while R_d is inversely proportional to W, the drain resistance R_d may even exceed R_g for narrow finger transistors, especially if the gate length L is larger than the minimum length that the design rules allow. In order to extract the value of R_g correctly for narrow finger transistors, the values of R_s, R_d, and R_{ds} must be extracted separately, for example with the method proposed in Section 8.1.7. Equation 8.20 may be used then for calculating the value of R_g.

8.1.9 Substrate Network

For extracting the substrate network elements, the transistor should be measured under the conditions where the transistor channel does not shunt the drain-bulk capacitor. When the transistor operates in the saturation region, R_{ds} is high and most of the drain AC current during the Y_{22} measurement will flow through the drain-bulk capacitor, which will excite the substrate network efficiently. Under these conditions, it will be relatively easy to isolate the substrate network contribution to the measured Y_{22} response.

We can use the network of Figure 8.12 for extracting the values for the substrate network elements from the Y_{22} measurement data. This circuit is obtained from the circuit of Figure 8.8 trough several simplification steps, shown in Figure 8.11. First, the values of R_g and R_d are already known from the previous analysis. Therefore, we can calculate the Z parameters of the circuit inside the dashed-line box in Figure 8.8. Next, we calculate the Y_{22} parameter of the circuit inside the box, which is equivalent to shorting the node g_i to the ground. In the saturation region, the reactive part of the intrinsic transistor drain-source impedance is very small, since the drain voltage variations disturb very little the channel charge balance. Therefore, we can model this impedance with R_{ds} alone, and remove the controlled source i_{md} from the circuit.

The remaining network is shown in Figure 8.11a. The intrinsic gate-source voltage controls the current i_m. The intrinsic gate-source voltage is

$$v_{gsi} = V_2 \frac{R_s}{R_s + R_{ds}} \tag{8.23}$$

This voltage is rather small, since $R_{ds} >> R_s$ in the saturation region. However, it should not be neglected, since the transistor is now biased to operate in the region where the transconductance is high. The transistor will multiply the intrinsic gate-source voltage of Equation 8.23 by the transistor transconductance, which results in the drain current component i_m that will increase the output impedance of the transistor. Assuming that no significant phase shift takes place[4], we can replace the controlled source i_m with the negative conductance

$$g_{mx} = \frac{-g_m\, R_s}{R_s + R_{ds}}, \tag{8.24}$$

[4]This is reasonable, since R_s is very small compared to the impedance of C_s in the interesting frequency range.

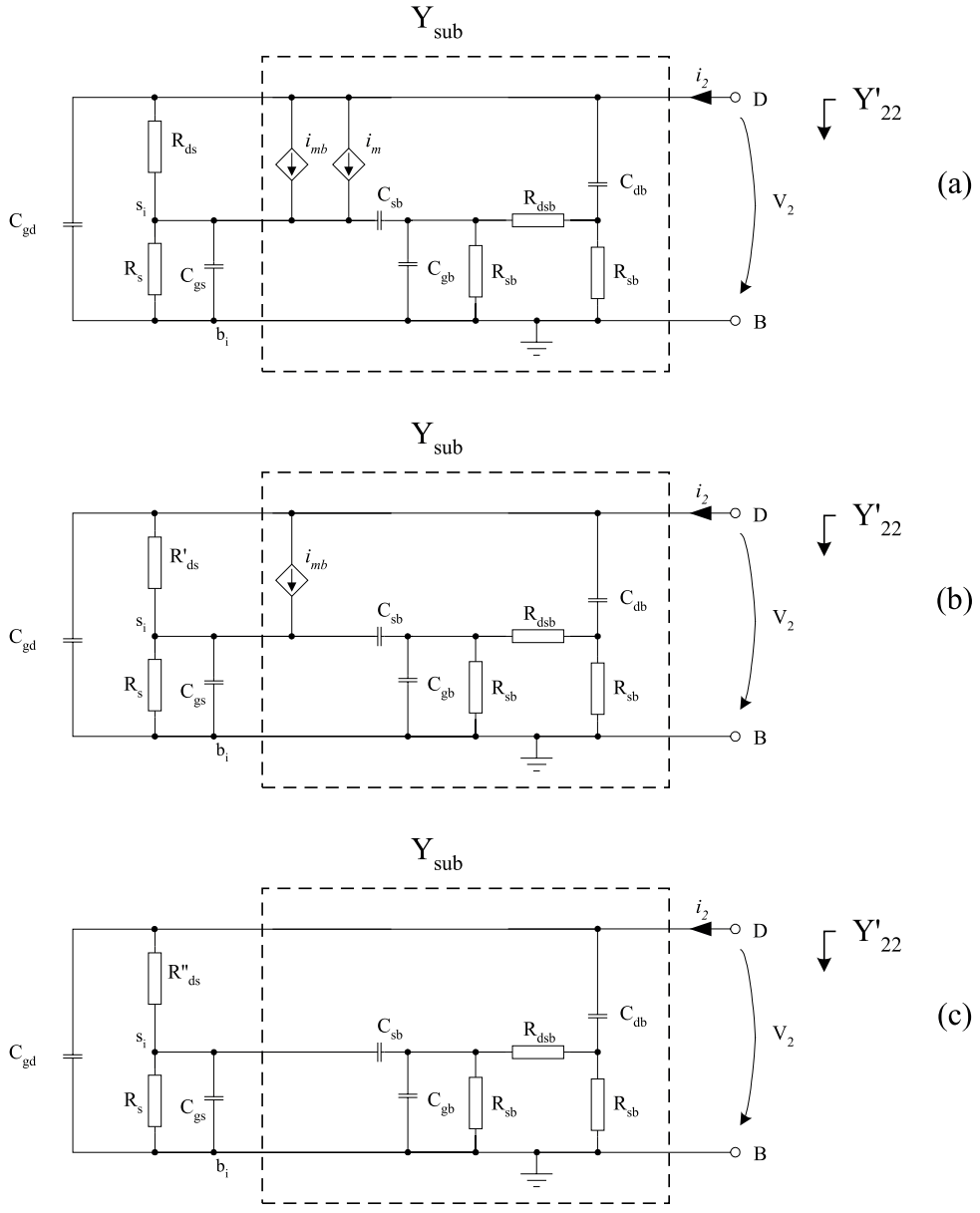


Figure 8.11: *The intermediate steps in simplifying the MOSFET equivalent diagram for extracting the substrate network elements. a) R_d, R_g, and i_{md} are eliminated, b) i_m and R_{ds} are merged to R'_{ds}, c) i_{mb} is removed.*

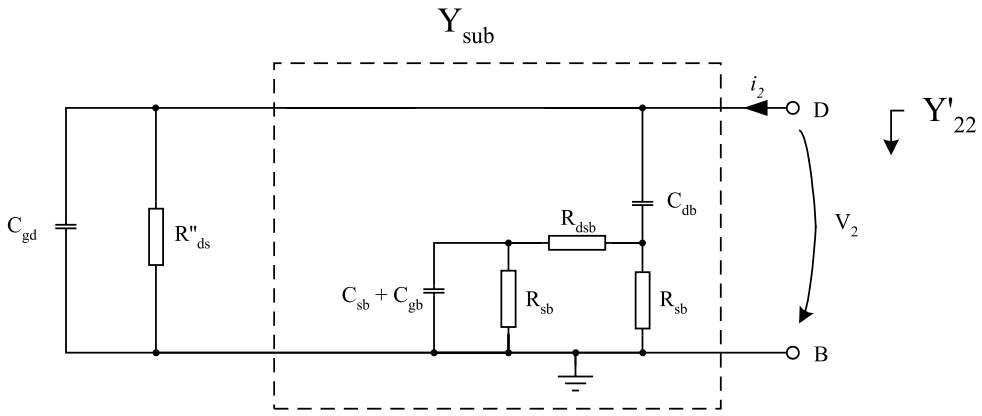


Figure 8.12: *The simplified MOSFET equivalent diagram for extracting the substrate network elements.*

where g_m is the transistor transconductance. In order to further simplify the equivalent diagram of Figure 8.11a, we can combine the effects of g_{mx} and R_{ds} to a single resistance:

$$R'_{ds} = (\frac{1}{R_{ds}} + g_{mx})^{-1} \tag{8.25}$$

This is the value of the intrinsic transistor output resistance that we can extract from a Z_{22} measurement, when the source electrode resistance R_s is non-zero and the transistor operates in a region where $g_m \neq 0$. R'_{ds} is the real part of Z_{22}, measured at a low frequency, when the effects of the electrode resistances R_d and R_s are subtracted:

$$R'_{ds} \approx Re\{Z_{22}\} - R_s - R_d \tag{8.26}$$

A value for the transistor transconductance is obtained from $g_m = Re\{Y_{21}\}$, where Y_{21} is measured at a low frequency. Since R_s is already known, we can now solve R_{ds} by combaning Equations 8.24, 8.25, and 8.26.

Finally, since the gate is grounded and the source is connected to the bulk, the voltage v_{gsi} also controls the current source i_{mb}. Since increasing v_{gsi}

will increase i_{mb}, the effect of this controlled source is to decrease the output impedance of the transistor. Since the controlled sources i_m and i_{mb} are in parallel and they are driven from the same voltage, the effect of i_{mb} can be taken into account in the same way as was done with i_m, by adding another conductance $g_{mbx} = g_{mb}R_s/(R_s + R_{ds})$ inside the parenthesis in Equation 8.25. Unlike with g_m, it is difficult to extract a reliable value for g_{mb}. However, since we already have a value for g_m, it is possible to calculate an estimate for g_{mb} using $g_{mb} = (n-1)g_m$, where n is the slope factor $n = 1 + \frac{\gamma}{2\sqrt{\phi_0+V_P}}$ [41]. However, when the bulk transconductance g_{mb} is known to be much smaller than the small-signal forward transconductance g_m, it is probably not necessary to modify Equation 8.25.

Since the impedance of R_s is much smaller than the impedance of R'_{ds} or C_{gs} at the interesting frequency range, we can now remove R_s and C_{gs} from the circuit by grounding the node s_i. The result is the circuit in Figure 8.12. The value of C_{gd} can be extracted from the imaginary part of Y_{12}. Note that now we cannot use Equation 8.15, since the transistor is not reciprocal in the saturation region. The remaining problem with finding values for the substrate network elements is to fit the Y'_{22} data and the remaining RC circuit response. Since the values of R'_{ds} and C_{gd} are known, the optimization problem includes only four degrees of freedom.

8.1.10 Reliable Parameters Extraction

It is known that all networks, that include only resistors and capacitors, are reciprocal. This is a very useful property for checking that the MOSFET parameter extraction system is working correctly: under all conditions when it is reasonable to model the transistor with a network that includes only capacitors and resistors, the measured Y_{12} and Y_{21} must be equal within the accuracy of the measurement system. For checking that the measurement system and the de-embedding procedure work correctly, a test transistor should be biased with $V_{DS} = 0\ V$, and the measured and de-embedded Y_{12} and Y_{21} data should be plotted on top of each other. If the curves do not seem to overlap perfectly, something must be wrong with the S-parameters measurement setup, de-embedding procecure, the data analysis program, or the bias conditions of the transistor. Since the Y_{12} and Y_{21} data originate from two independent measurements, some random noise on each curve is to be expected. This noise level should correspond to the expected noise level and accuracy of the system. If the curves do not seem to overlap perfectly, the most probable reasons are that the RF probe calibration was not successful, or that the input signal level is too high, biasing the transistor to the active reigon during the signal voltage

peaks. In these cases, is easy to find the reason by measuring the response of another passive device and comparing the results. Finally, when the transistor is biased to operate in a region where gain is expected, the two parameters should become clearly different.

Another good way of checking if the parameter extraction procedure is reliable is to measure Y_{11} under the same bias conditions as with the Y_{12} and Y_{21} measurements, and to extract an approximation of the gate-drain capacitance from the measured Y_{11} data by calculating

$$C\prime_{gd} \approx \frac{Im\{Y_{11}\}}{2\ \omega}, \tag{8.27}$$

Knowing that the capacitance extracted from Y_{11} includes the contributions from the unmodeled capacitances C_{f1} and C_{f2}, the extracted capacitance value $C\prime_{gd}$ should be slightly larger than C_{gd} with all gate bias voltages. Therefore, plotting $C\prime_{gd}$ and C_{gd} as functions of the gate bias voltage on top of each other (when $V_{ds} = 0\ V$) will reveal many errors and inaccuracies in the device parasitics extraction procedures. The difference of these curves, when V_{gs} is well above the transistor threshold voltage, gives an indication of the accumulated error during the extraction process from the S-parameters measurements to the data analysis, and of how much C_{f1} and C_{f2} contribute to the extraction of the parasitic capacitances.

For small transistors that have relatively narrow gate fingers, the value of R_d will be high. Therefore, the contribution of the source and drain parasitic resistances is relatively easy to distinguish from the effects of the disturbing factors. With wide transistor geometries, the extraction of R_d is more difficult, since the value of R_d is much smaller than the impedance level of the measurement system RF cables. In addition, the probe contact resistance may be larger than R_d.

8.2 Experimental Results

For characterizing the RF properties of the devices that would be used later in this work for VCO circuit designs, a test chip was fabricated. Several different test structures were designed, including PMOS and NMOS transistors, diodes, different varactor devices, capacitors, and inductors. Each device resides in a test fixture that connects the device electrically to the RF test probe pads. In addition, the necessary on-chip standards were fabricated on the same chip for de-embedding the test fixture parasitics.

8.2.1 MOSFET Measurement Setup

The ground-shielded test fixtures were designed according to [47], adapting the proposed technique to the available three-metal layer CMOS technology. The source and bulk terminals of the test transistors were connected to the test fixture ground. Since the available RF probes were stiff in construction, it was known that it will be difficult to avoid the contact problems described in Figure 8.1. Therefore, the test fixture GSG pad patterns were designed for the best planarity and mechanical strength, rather than the minimum capacitance between the signal pad and the ground shield. In both ground and signal pad stacks, all three metal layers were present, in order to reduce the height difference between the stacks. The two topmost metal layers in the signal pad were mechanically tied together with a dense via array, in order to improve the mechanical durability of the topmost pad. The only difference between the ground and signal pad stacks is the absent via array between the two lowest metal layers in the signal pad. It turned out that the test fixture design was successful: despite of the unoptimal RF probe construction, the measurement system worked well. Once the RF probe station was isolated from the vibrations of the building and the tilt of the RF probes was carefully aligned, the repeatability of the measurements was good.

Before each new measurement, the RF probes and cables were calibrated using an impedance standard substrate. After the successful probe calibration, the measurements for the test fixture calibration were carried out, using the set of standards that were fabricated on the same chip with the test transistors [47]. The results of these calibration measurements were stored for the following DUT S-parameters de-embedding. The test fixture, that included the test transistor, was measured immediately after the calibration was completed. Only one touchdown was made to the test fixture, in order to minimize the contact resistance instability. The S-parameters of the test device were then measured using a computer-controlled HP8510C network analyzer, and two computer-controlled voltage sources for setting the bias point of the transistor. The gate-source voltage was swept automatically with 50 mV steps trough 0 - 3 V, and the drain-source voltage was swept through 0 - 3.3 V with 100 mV steps. The S-parameters of each test transistor were measured in 201 frequency points in the frequency range 200 MHz-10 GHz. Each measurement result, that was stored, is an average of 16 individual measurements. The goal of the measurements was to measure the DUT with so small voltage steps that the transistor response is known under all possible bias conditions. The data was saved in ASCII format. Even though the resulting data files were large, the format allows read-

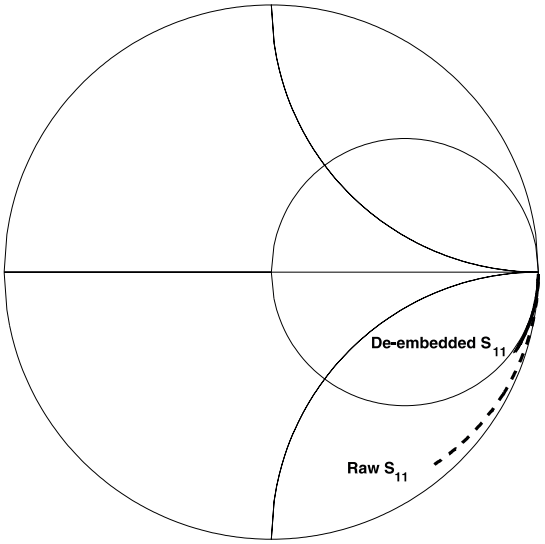


Figure 8.13: *The measured S_{11} data of a 28/0.35 μm NMOS transistor, before (dashed thick line) and after (solid thick line) the de-embedding. The transistor operates in the linear region. The test fixture parasitics clearly dominate the response before the de-embedding.*

ing and analyzing the data in almost any computer platform and writing analysis programs with any programming language.

8.2.2 Parameters Extraction Results

The analysis program was written in Matlab script language. For de-embedding the test fixture parasitics, the method proposed in [46] was used. The advantage of this method is that it models very well the parasitics of the test fixture. Since the test transistors are small and the grounded-shield test fixture has relatively large parasitic capacitances, it is important to de-embed the test fixture parasitics with good precision.

For showing the effect of the test fixture parasitics on the DUT measurements, Figure 8.13 shows the measured S_{11} data of an NMOS transistor before and after the de-embedding. Obviously, the test fixture parasitics change significantly the response. It was found out that the de-embedding procedure together with careful probing and measurements reduced the

effects of the test fixture parasitics to a negligible level, and produced highly repeatable results. The parasitic capacitances calculated from the de-embedded measurements results corresponded well the parasitics that were calculated using the layout geometry and the foundry process parameters data.

Figure 8.14 shows the measured Y_{12} and Y_{21} parameters of an NMOS transistor under two slightly different bias conditions. As is expected, the device is reciprocal when $V_{ds} = 0\,V$. When the drain-source voltage is increased by 100 mV, the Y_{12} and Y_{21} curves do not overlap, since the forward transconductance has increased.

Parasitic Capacitances and Resistances of a Small NMOS Transistor

For verifying the accuracy of the parameters extraction method, the parameters of a small four-finger 28/0.35 μm NMOS transistor were extracted. Figure 8.15 shows some of the extracted capacitance values, when the gate-source voltage is varied and the drain-source voltage is set to zero. C_{gg} and C_{gd} are calculated using Equations 8.8 and 8.15, respectively. The C_{gd} curve at $V_{gs} = 0\ V$ represents the gate-drain edge capacitance when the channel is absent. By subtracting two times this capacitance from C_{gg} we obtain C_{ggi}, which represents the gate-channel capacitance of the intrinsic transistor. For reference, the horizontal dashed lines plot the corresponding gate capacitance calculated from the gate finger geometry and the foundry process parameters data for slow, typical, and fast circuit performance. The value of C_{ggi} is slightly lower than the minimum capacitance calculated using the process parameters data. This result can be expected, since the process parameter for calculating the area capacitance applies only for large gate finger geometries. For the 0.35 μm long gate finger we should expect that the sidewall capacitance will represent most of the gate finger capacitance, and that the calculated area capacitance probably is too large.

C_{gb} is the difference of the total input capacitance and the gate capacitance associated with the channel. As was discussed in Section 8.1.6, C_{gb} represents the gate-bulk capacitance, but includes also the contributions from the unmodeled parasitic capacitances. The extracted value of C_{gb} is small and positive, and it is clearly reducing when the transistor enters the strong inversion region. These are good indications of that the unmodeled parasitic capacitances contribute little to the values of the extracted capacitances, and that the extracted capacitance values must be approximately correct.

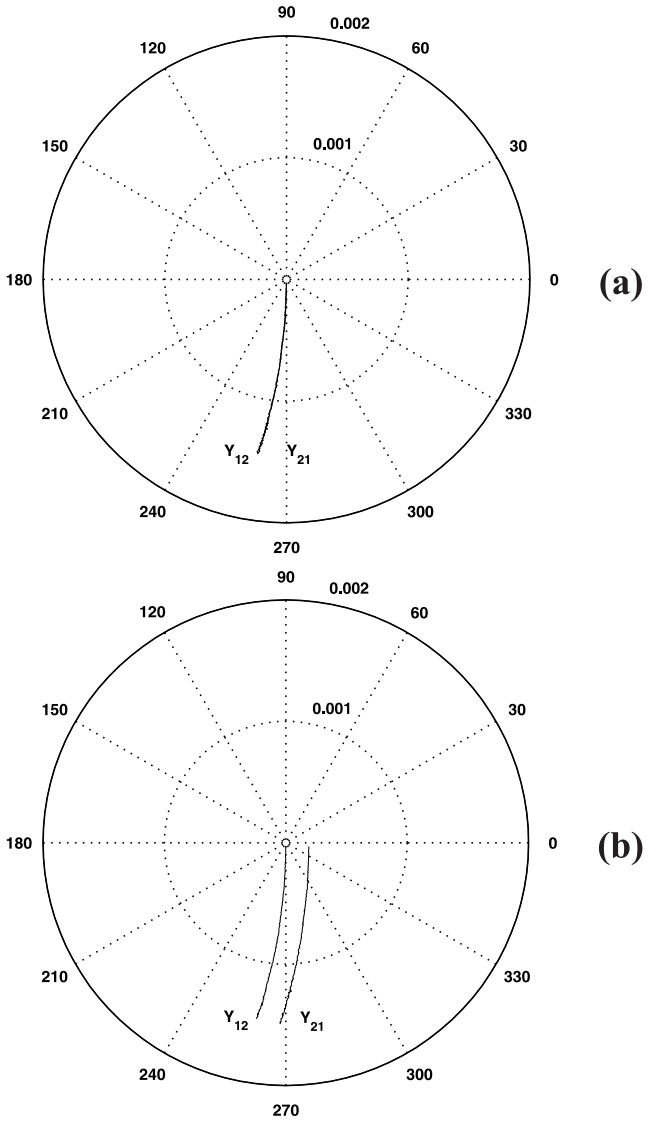


Figure 8.14: *The measured and de-embedded Y_{12} and Y_{21} of a 28/0.35 μm NMOS transistor. The frequency range is 200 MHz - 10 GHz, 201 measured points in each curve. (a) The linear region and strong inversion: $V_{ds} = 0.00\ V$ and $V_{gs} = 3.00\ V$. Considering the accuracy of the measurement system and the de-embedding method, the two curves overlap perfectly. (b) In this plot $V_{ds} = 0.10\ V$ and $V_{gs} = 3.00\ V$. The two curves are clearly separated, since the transistor gain is different in the two directions.*

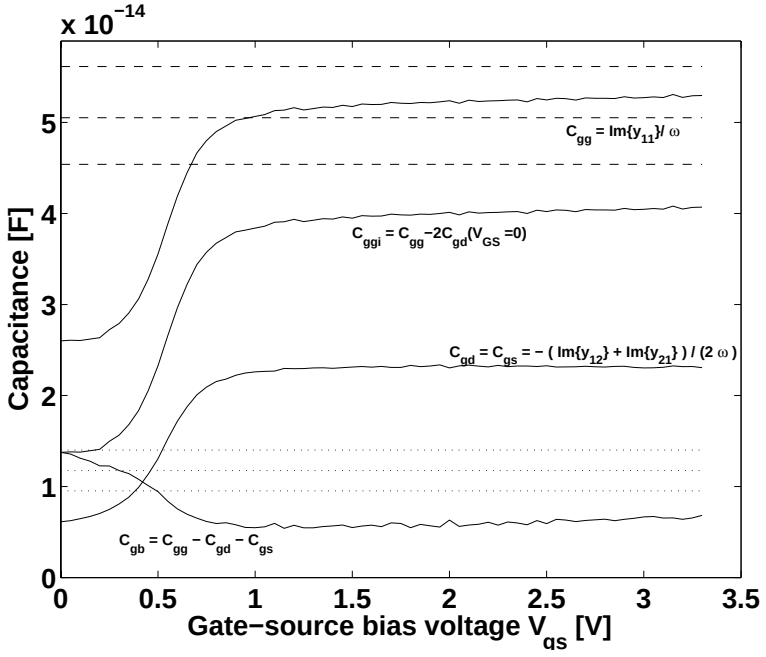


Figure 8.15: *Extracted capacitances for a 28/0.35 μm NMOS transistor. The data is acquired from the measurements at 2.4 GHz frequency. V_{gs} is varied through 0.0-3.3 V, and the drain-source voltage is $V_{ds} = 0.0$ V. The dashed horizontal lines show the simulated gate oxide capacitance, and the dotted horizontal lines the simulated sidewall capacitance between the gate, source and drain.*

For extracting the values of R_s, R_d, and K, Equation 8.18 was fitted to the measured Z_{22} data, as is shown in Figure 8.17. The resulting estimates are $R_d = R_s = 24.05\ \Omega$ and $K = 0.01053$. The value of the threshold voltage V_t is not known precisely, but usually it is not necessary to extract it separately for this purpose. In this experiment, V_t is known from the data that the foundry has measured using test structures that were fabricated on the same wafer as the test chips. If this data is not available, the 'typical' value of V_t from the process parameters data sheet may be used. Since the lowest gate-source voltage that is used in this optimization is more than 1.5 V above the threshold voltage, a small error in the value of V_t is acceptable. The extraction method assumes that the values of R_s and R_d do not depend on the gate-source voltage. This is not completely true, since the lightly-

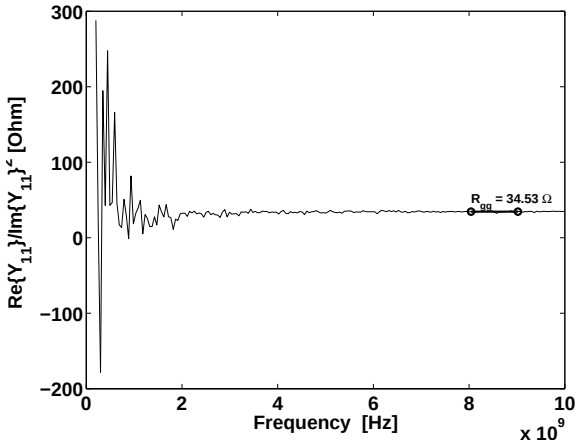


Figure 8.16: *Extracting the input resistance R_{gg} of the four-finger 28/0.35 μm NFET. At frequencies below 2 GHz the plot of $Re\{Y_{11}\}/Im\{Y_{11}\}^2$ is very unstable since $|Im\{Y_{11}\}|$ is not clearly above the measurement system noise level at low frequencies. The solid line is a horizontal line segment that is fitted to the data for extracting R_{gg} at a frequency range where the response is known to be stable.*

doped regions close to the gate finger edges may partially deplete when the gate-source voltage is high. However, since the voltage dependence of these resistances is much weaker than the voltage dependence of the channel conductivity, the resulting error will be small. A good indication of this is that Equation 8.18 fits very well to the Z_{22} data in Figure 8.17, even though the model equation has only two degrees of freedom.

For extracting the equivalent gate finger resistance R_g, Figure 8.16 plots $Re\{Y_{11}\}/Im\{Y_{11}\}^2$, and fits a horizontal line segment to the data for finding the real part of the input impedance. Since R_s and R_d are known, and R_{ds} at $V_{GS} = 3.00\ V$ can be found from the data of Figure 8.17, we can find (using Equation 8.20): $R_g = 34.53\ \Omega - 38/12\ \Omega - 24.05/2\ \Omega = 19.3\ \Omega$. This is the equivalent resistance of the four resistive gate 7/0.35 μm gate fingers in the MOSFET equivalent diagram. Taking into account that each finger has approximately 1 μm of extra polysilicon for contacting the finger to the metal conductor, we can calculate the corresponding equivalent gate finger resistance using the 'typical' and 'slow' process parameters: $R'_{g,typ} = 13.3\ \Omega$ and $R'_{g,slow} = 22.8\ \Omega$. The extracted value, $R_g = 19.3\ \Omega$, falls between these

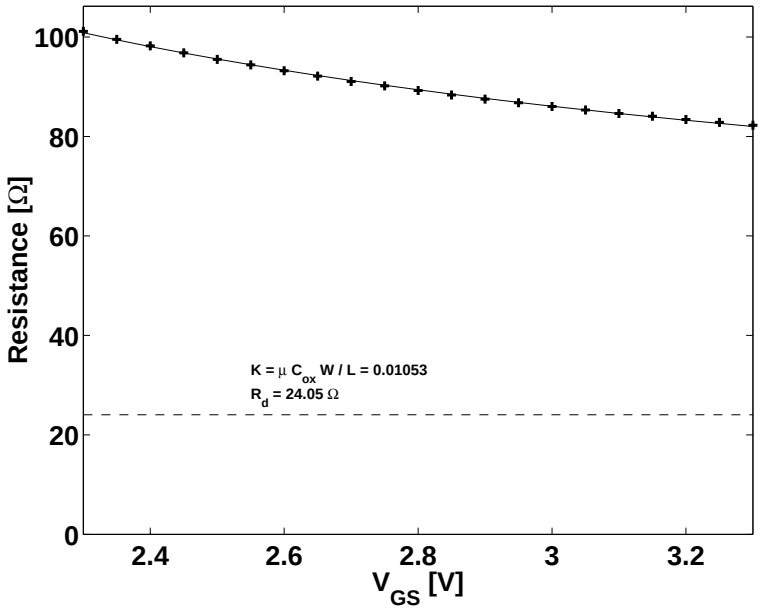


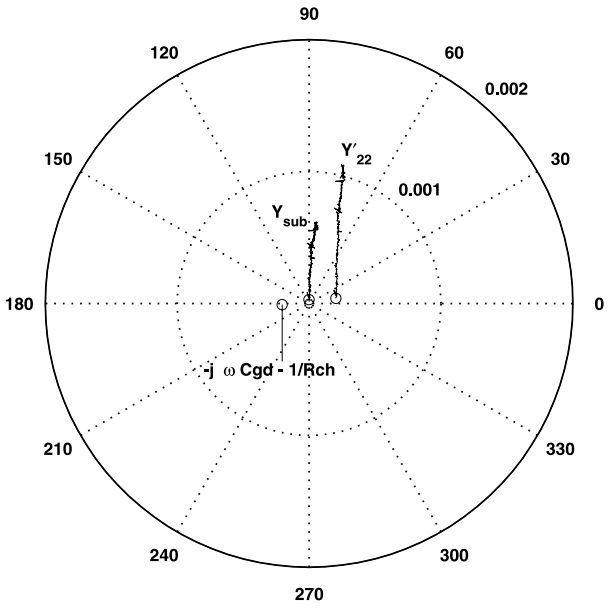
Figure 8.17: *Extracting the value of R_d by fitting the equation $Z_{22} = 2R_d + [K(V_{gs} - V_t)]^{-1}$ (solid thin line) to the measured Z_{22} data (markers). The Z_{22} data was measured at 250 MHz frequency. The dashed line shows the value of R_d that minimizes the error function.*

two predicted values, which confirms that the extracted value is reasonable.

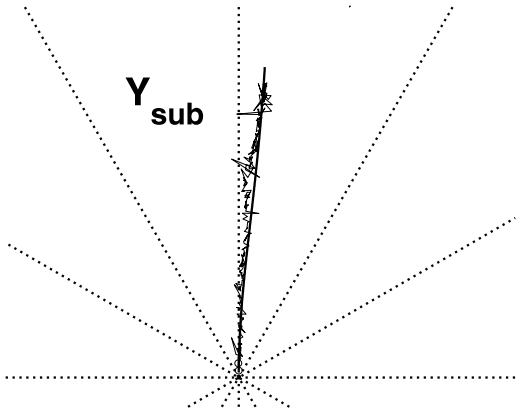
Substrate Network Elements

In order to extract the substrate network element values, the transistor is biased to operate in the saturation region. The Y'_{22} response of the DUT is first calculated from the Z_{22} data, removing the effects of R_g and R_d, and converting the resulting Z parameters to Y parameters. The response of the model of Figure 8.12 is then fit to this Y'_{22} data. For the 28/0.35 μm NMOS transistor, the values $C_{gb} + C_{sb} = 25.2\ fF$, $R_{sb} = 904.1\ \Omega$, $R_{dsb} = 1.0\ \Omega$, and $C_{db} = 14.4\ fF$ were obtained. Note that the value of R_{dsb} is probably too small, indicating that the parameters extraction by curve fitting is error prone, unless the signal-to-noise ratio of the Y_{sub} data is very good.

For clarifying the extraction procedure, Figure 8.18a shows the signals of the circuit in Figure 8.12 in the complex admittance plane. Since the Y'_{22}



(a)



(b)

Figure 8.18: *(a) The signals for extracting the substrate network element values. The transistor operates in the saturation region:* $V_{ds} = 3.00\ V$ *and* $V_{gs} = 3.00\ V$*. (b) A detail of a similar plot after unsuccessful curve fitting. The substrate network model with four degrees of freedom is fitted to the* Y_{sub} *data. The curve does not follow the overall shapes of the data, which is a sign of unreliable results.*

data still includes the contributions of R_{ds} and C_{dg}, these must be removed by subtracting the admittance $j\omega C_{gd} + Y'_{22,LF}$, where $Y'_{22,LF}$ is the output admittance of the network measured at a low frequency. The result is the Y_{sub} curve, which represents the contribution of the substrate parasitics to the transistor output admittance.

For illustrating typical problems with extracting the substrate network element values, the Y_{sub} curve and the fitted response of the substrate network are also shown slightly magnified in Figure 8.18b. The noisy Y_{sub} data carries the available information about the substrate network. In addition to the true substrate network response, this data includes the contributions of the measurement system noise and the errors made with the system calibration and de-embedding. In order to obtain meaningful values for the substrate network elements, these errors must be reduced to the level where fitting a curve with four degrees of freedom to the Y_{sub} data makes sense. The curve drawn with the thick line in Figure 8.18b is a result of curve fitting that was terminated too early. Obviously, the curve does not match the overall shape of the Y_{sub} curve very well. The result of this fitting is parameter values that may be in the right order of magnintude, but are too inaccurate to be used with a scaleable transistor model.

Another problem with extracting the substrate network element values is the accumulated systematic errors in the Y_{sub} data. Even though most of the noise originating from the measurement system electronics is random and can be reduced by averaging, the errors made with the probe and test fixture calibrations tend to be systematic, and are even amplified when the data is de-embedded. Even though the shape of the Y_{sub} curve in Figure 8.18b is approximately correct, the Y_{sub} curve seems first to rise vertically, then to bend to the right, rise vertically again, turn to the right, and finally start rising vertically again, as the frequency is increasing. Obviously, there are more bends in the curve than the circuit of Figure 8.12 is able to explain. The reason for the extra details in the the Y_{sub} curve was found to be a very weak on-chip resonance at approximately 3 GHz during the test fixture calibration measurements[5]. Therefore, all de-embedded results seem to include a small deviation from the expected behavior close to this frequency. Even though the resonance is almost invisible in the test standard S-parameters data, it becomes clearly visible in this curve. The de-embedding procedure tends to amplify the errors made with the calibration, since the de-embedding basically subtracts constant parasitic values

[5]In order to make the test chip layout compact, a test fixture including a spiral inductor was placed next to one of the on-chip calibration standards. This structure probably resonates during the calibration measurement, distorting the calibration data around 3 GHz.

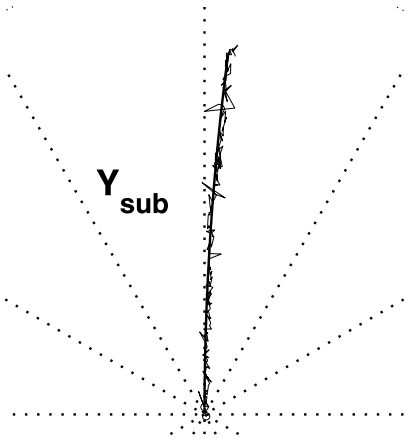


Figure 8.19: *The substrate network signal in the complex admittance plane after a successful calibration and curve fitting. The Y_{sub} data does not contain unexpected bends, and the fitted curve (the thick line) clearly follows the overall shape of the noisy data plot.*

from the distorted raw data. Figure 8.19 shows the substrate network signals when the probe calibration and the on-chip calibration standards measurements were successful. The Y_{sub} data does not contain unexpected bends, and the response of the model network clearly fits the data.

8.3 Conclusions

The proposed parameters extraction method produces meaningful values for the parasitic elements of the analog simulator high-frequency MOSFET model. Only two degrees of freedom are needed for finding the values of R_d and R_s, since they are found by fitting the transistor model response to the measured low-frequency Z_{22} data, varying the gate bias voltage. Most other well-known methods for extracting these parameters employ curve fitting in the frequency plane in a fixed bias point [69] [70]. Since the reactive elements of the transistor equivalent diagram must be taken into account in this case, the number of degrees of freedom in curve fitting becomes higher, which easily leads to inaccurate results.

The test measurements show that it is relatively easy to obtain the necessary resolution for extracting the MOSFET parameters with the proposed method. However, as with any parameters extraction method, the accuracy depends on the contact stability between the RF probe tips and the test fixture pads, and the level of signal coupling between the test fixture and the other on-chip structures that may resonate during the measurements and produce some unexpected side effects. Carrying out the calibration measurements carefully is essential, since the de-embedding procedure will amplify the errors that were made during the calibration measurements. Fortunately, it is easy to reveal many of the error sources by measuring a passive LRC network and checking that the measured response is reciprocal. Once the error sources contributing to the accuracy of the measurement system are eliminated, the parameters extraction method produces a reliable model parameters also for small-sized MOS transistors.

Chapter 9

Conclusions

The recent discussion on fully integrated VCO circuits has been focused on reducing the phase noise level of the oscillator, or minimizing the power consumption of the VCO circuit while keeping the phase noise level at an acceptable level. Even though some papers mention the sensitivity of oscillator circuits to the noise that is coupled from the supply sources, bias sources, or the substrate, few ideas have been presented in reducing the sensitivity of the oscillator circuits. However, given that the SoC RF circuit designer is forced to live with the on-chip interference sources and the limitations of the available technology, the immunity to the on-chip interference sources should be taken as another design goal in VCO designs.

This work shows that the voltage dependent capacitances in the LC tank oscillator circuit play a central role in converting the interference signals into sidebands in the oscillator output spectrum. Moreover, it is shown that it is possible to reduce the sensitivity of the oscillator by taking into account them, and designing the circuit in the way that the AM-FM conversion in the VCO core circuit is minimized. The experimental results show that it is not necessary to severely compromise the traditional figures of merits of LC oscillator circuits. The 3 GHz prototype VCO circuit is able to significantly suppress the bias source modulation, when it is biased to operate in the point where the AM-FM conversion is minimized. In this operating point the current consumption is only 2.5 mA, the phase noise level is -110 dBc/Hz at 500 Hz offset frequency, and the tunability of the oscillating frequency is $\pm$ 5%. Even though the experimental work was carried out using a CMOS process, most of the the presented ideas apply to any LC oscillator circuit that includes voltage dependent capacitances in the tank circuit.

The work on MOSFET modeling and parameter extraction shows how the reciprocal property of a MOSFET device under symmetrical bias conditions may be used for improving the accuracy of some extracted parameter values, and for checking the accuracy of the measurement system and the de-embedding procedure. It also proposes extracting the extrinsic drain and source resistance values from the measured Z_{22} response at a low and fixed signal frequency, by sweeping the gate-source bias voltage. The advantage of this method is that the number of degrees of freedom in the curve fitting is reduced to only two, since the contributions from the parasitic capacitances to Z_{22} may be ignored.

Even though this thesis presents a method for simulating the steady-state voltage waveform of an LC oscillator, it does not provide the VCO designer a method for modeling the voltage dependent capacitances and the RF loss in the tank circuit elements. The discussion on MOSFET modeling shows that modeling the large-signal behavior of the gain transistors, especially the voltage-dependent input and output resistances, may be difficult. The future work should address finding suitable methods for simulating the large-signal behavior of all devices that are connected to the tank circuit, taking into account the non-quasi-static effects.

Appendix A

Damped Harmonic Motion Equation

The linear homogenious differental equation that describes the dynamics of a parallel RLC circuit without external disturbing sources is

$$C\ddot{E} + \frac{1}{R}\dot{E} + \frac{1}{L}E = 0 \tag{A.1}$$

It is called the damped harmonic motion equation, since a similar equation describes the dynamics of a simple one-dimensional mechanical system including a spring, a mass, and a dashpot. It is relatively easy to find the particular solutions for arbitrary initial conditions, using standard methods for solving linear homogenious differential equations.

The auxilary polynomial is

$$P(r) = Cr^2 + \frac{1}{R}r + \frac{1}{L} \tag{A.2}$$

The roots of the auxilary polynomial equation $P(r) = 0$ are

$$r = -\frac{1}{2RC} \pm \frac{1}{2C}\sqrt{\frac{1}{R^2} - \frac{4C}{L}}. \tag{A.3}$$

The form of the solution of Equation A.1 depends on the argument of the square root in Equation A.3.

When $\frac{1}{R^2} < 4\frac{C}{L}$, the system is underdamped. The general solution is

$$E(t) = e^{-\alpha t}\{C_1 \cos \omega_u t + C_2 \sin \omega_u t\} \tag{A.4}$$

where

$$\alpha = \frac{1}{2RC} \tag{A.5}$$
$$\omega_u = \frac{1}{2C}\sqrt{4\frac{C}{L} - \frac{1}{R^2}}$$

For finding the particular solution for the given initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$, we must solve the set

$$E_0 = E(0) = C_1 \tag{A.6}$$
$$e_0 = \dot{E}(0) = -\alpha C_1^2 + \omega_u C_2 \tag{A.7}$$

which gives $C_1 = E_0$ and $C_2 = \omega_u^{-1}(e_0 + \alpha E_0^2)$.

The particular solution for the given initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$ in the underdamped case is then

$$E(t) = e^{-\alpha t}\{E_0 \cos \omega_u t + \omega_u^{-1}(e_0 + \alpha E_0^2) \sin \omega_u t\} \tag{A.8}$$

When $\frac{1}{R^2} = 4\frac{C}{L}$, the system is critically damped. The general solution is

$$E(t) = e^{-\alpha t}\{C_1 + C_2\ t\} \tag{A.9}$$

For finding the particular solution for the initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$, we must solve the set

$$E_0 = E(0) = C_1 \tag{A.10}$$
$$e_0 = \dot{E}(0) = -\alpha C_1 + C_2 \tag{A.11}$$

which gives $C_1 = E_0$ and $C_2 = e_0 + \alpha E_0$. Therefore, the particular solution for the initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$ in the critically damped case is

$$E(t) = e^{-\alpha t}\{E_0 + (e_0 + \alpha E_0)\ t\} \tag{A.12}$$

When $\frac{1}{R^2} > 4\frac{C}{L}$, the system is overdamped. The general solution is

$$E(t) = C_1 e^{(-\alpha+\omega)t} + C_2 e^{(-\alpha-\omega)t} \tag{A.13}$$

where

$$\alpha = \frac{1}{2RC} \tag{A.14}$$

$$\omega = \frac{1}{2C}\sqrt{\frac{1}{R^2} - 4\frac{C}{L}} \tag{A.15}$$

For finding the particular solution with the initial conditions $E(0) = E_0$ and $\dot{E}(0) = e_0$, we solve the set

$$E_0 = E(0) = C_1 + C_2 \tag{A.16}$$

$$e_0 = \dot{E}(0) = -C_1(\alpha - \omega) - C_2(\alpha + \omega) \tag{A.17}$$

which gives $C_1 = E_0 - C_2$ and $C_2 = -\frac{1}{2\omega}[E_0(\alpha - \omega) + e_0]$.

The particular solution in the overdamped case is

$$E(t) = C_1 e^{(-\alpha+\omega)t} + C_2 e^{(-\alpha-\omega)t} \tag{A.18}$$

where

$$C_1 = E_0 + \frac{1}{2\omega}[E_0(\alpha - \omega) + e_0] \tag{A.19}$$

$$C_2 = -\frac{1}{2\omega}[E_0(\alpha - \omega) + e_0] \tag{A.20}$$

Appendix B

Simulating the LC Oscillator Steady State

This Appendix lists an example code for demonstrating the steady-state voltage waveform analysis of an LC oscillator with the method described in Chapter 5. The code supports Matlab v. 6 syntax. Some Matlab Optimization Toolbox functions are also called.

The $C(V)$ and $G(V)$ data are generated with program 'makeCG2.m', which uses analytical expressions for composing the data. The program stores the data in the .csv format. The data file may also be generated by other means, like using an analog simulator or a spreadsheet program.

Running 'LCR_ss.m' will find the steady-state voltage waveform, and extract the oscillation frequency and the harmonic components of the waveform.

```
% makeCG2.m v. 1.0 070103JT
%
% Composes C(V) and G(V) data, and stores it in csv format

clear all; close all;

vout =  [-2:0.01:2]'; % Voltage vector
dd = 9;      % 0=plot on left, 9=plot on right
             % Set to 0 if using only one display

%% COMPOSE THE VOLTAGE DEPENDENT GAIN AND CAPACITANCE CURVES %%
MJ = 0.5;
PB = 1.2;
C0 = 5e-12;
VQ = 1.2;
SIGMA = 0.5;
gpvect1 = (-10E-3)/(SIGMA*sqrt(2*pi)) * ...
          exp( -0.5*(vout/SIGMA).^2 ) + 6.5*1e-3;
gpvect2 = gpvect1 + 0.1*max(-gpvect1);
%Cstep = C0*0.05*(atan(100*(vout+0.2))/(pi/2)-1) ;
Cstep = 0 ;
Cvect = Cstep + C0./(1+(vout+VQ)/PB).^MJ;

dlmwrite('CGdata.csv',[vout Cvect gpvect1 gpvect2],'\t');

figure(1)  % PLOT THE CAPACITANCE DATA
set(1,'Position',smallfig2(dd+1))
plot(vout,Cvect,'Color','k','LineStyle','-','LineWidth',2);
set(gca,'FontSize',16,'FontWeight','demi')
Xlabel('Tank circuit voltage V')
Ylabel('Tank circuit capacitance C(V)')

figure(2) % PLOT THE 1/R DATA
set(2,'Position',smallfig2(dd+2))
plot(vout,-gpvect1,'Color','k','LineStyle','-','LineWidth',2)
hold on
plot(vout,-gpvect2,'Color','k','LineStyle','--','LineWidth',2)
plot(vout, zeros(size(vout)),'Color','k','LineStyle',':')
set(gca,'FontSize',16,'FontWeight','demi')
Xlabel('Tank circuit voltage V')
Ylabel('Tank circuit net gain -1/R(V)')
```

```
% LCR_ss.m v. 1.0 040103JT

clear all; close all; tic
global ti si T M Vout L Cvect Gvect;

L = 2.0e-9;  % Inductance
M = 20;     % M     = # of time steps/period
dd = 0;      % 0=plot on left, 9=plot on right
             % Set to 0 if using only one display

data = dlmread('CGdata.csv');  % Read in the C(V) and G(V) data
%Vout = data(:,1); Cvect = data(:,2); Gvect = data(:,3);
Vout = data(:,1); Cvect = data(:,2); Gvect = data(:,4);

C0     = sum(Cvect)/size(Cvect,1); % A coarse estimate for fixed C
T      = 2*pi*sqrt(L*C0);          % A coarse estimate for the period
GAIN_AREA = sum(Gvect(find(Gvect<0)));
E0 = sqrt(-12*GAIN_AREA);          % First initial guess for E0
fprintf('\nFirst initial guess E(0) = %g\n',E0)
fprintf('                       M = %d\n\n',M)

OPTIONS = FOPTIONS(1);
v0opt=leastsq('search_ss',E0, OPTIONS);

M = 100;     % Decrase step size for better accuracy
fprintf('\nIntermediate result:   E(0) = %g\n',si(1))
fprintf('Decrease time step:         M = %d\n\n',M)
v0opt=leastsq_jt('search_ss',si(1), OPTIONS);
fprintf('\nFinal result:   E(0) = %g\n',si(1))

figure(3)
set(3,'Position',smallfig2(dd+3))
plot(ti,si,'k')
hold on

A0 = si(1);
c = [ (1e-9)*2*pi/T 0  A0    0   0.01*A0  0   0.0001*A0  0  0.00001*A0  ...
      0 0.00001*A0  0 0.00001*A0  0 0.00001*A0  0];
cf=leastsq('harmfit', c);

fit = cf(2) ...                                        % DC
    + cf(3)*cos(1*cf(1)*1e9*ti + cf(4)*pi/180 )...   % OMEGA*1e9
```

```
    + cf(5)*cos(2*cf(1)*1e9*ti + cf(6)*pi/180 )...   % HD2
    + cf(7)*cos(3*cf(1)*1e9*ti + cf(8)*pi/180 )...   % HD3
    + cf(9)*cos(4*cf(1)*1e9*ti + cf(10)*pi/180 )...  % HD4
    + cf(11)*cos(5*cf(1)*1e9*ti + cf(12)*pi/180 )... % HD5
    + cf(13)*cos(6*cf(1)*1e9*ti + cf(14)*pi/180 )... % HD6
    + cf(15)*cos(7*cf(1)*1e9*ti + cf(16)*pi/180 ) ;  % HD7

plot(ti,fit,'r--')

figure(6); set(6,'Position',smallfig2(dd+6)); plot(ti,si-fit)

%%%%%%%%%%%%%%%%%%%%%% ASCII OUTPUT %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
fprintf('\nFrequency domain analysis results:\n\n');
fprintf('F0:  %3.5f GHz \n',cf(1)/(2*pi));
fprintf('DC:  %3.3f V \n',cf(2));
fprintf('HD1:   %3.3f dBc    %3.1f  deg\n',20*log10(cf(3)/cf(3)),cf(4));
fprintf('HD2: %3.3f dBc   %3.1f  deg\n',20*log10(cf(5)/cf(3)),cf(6));
fprintf('HD3: %3.3f dBc   %3.1f  deg\n',20*log10(cf(7)/cf(3)),cf(8));
fprintf('HD4: %3.3f dBc   %3.1f  deg\n',20*log10(cf(9)/cf(3)),cf(10));
fprintf('HD5: %3.3f dBc   %3.1f  deg\n',20*log10(cf(11)/cf(3)),cf(12));
fprintf('HD6: %3.3f dBc   %3.1f  deg\n',20*log10(cf(13)/cf(3)),cf(14));
fprintf('HD7: %3.3f dBc   %3.1f  deg\n',20*log10(cf(15)/cf(3)),cf(16));
fprintf('\n');

toc
```

```
% search_ss.m  v. 1.0   040103JT
%
% Simulates the voltage across a parallel LCR circuit
% starting with the initial conditions
%
%  E(0)=E0 and E'(0)=0  (these correspond a local maximum)
%
% Simulates starting from a local maximum, until the next
% local maximum is found.
%
% Using global variables:
% T     = estimated period length
% M     = # of time steps/period
% L     = Inductance
% Vout  = C(V) and G(V) data definition range
% Cvect = C(V) data vector
% Gvect = G(V) data vector
%
% Input: The initial value of E(0)
%
% Returns the value of the goal function for  minimizing |Einit-Epk|,
% which corresponds to the steady state voltage waveform.

function[d] = search_ss(E0)

global ti si T M Vout L Cvect Gvect;

m      = 1;  % Loop counter
t0     = 0;  % Current time pointer
e0     = 0;  % Set E'(0)=0
ti(1)  = 0;  % Time vector for plotting. Starting from t=0.
si(1)  = E0; % The signal. The first point is the initial condition
dt = T/M;    % Time step

% Simulate E(t) until 1.7 * estimated period
% Interpolate C(V) and G(V) data for better accuracy

while (t0 < 1.7*T)
   s = LCRresp(E0, e0, spline(Vout, Gvect, E0), ...
               L, spline(Vout, Cvect, E0), dt);
   t0       = t0 + dt; % Next time step
   E0       = s(1);    % E(t) in the segment end = next initial cond.
```

```
   e0       = s(2);    % E'(t) in the segment end = next initial cond.
   si(m+1)  = s(1);    % Signal vector for plotting
   ti(m+1)  = m*dt;    % Time vector for plotting
   m        = m+1;     % Increment counter
end

simax = findmax(si);  % Find the local maxima
simin = findmax(-si); % Find the local minima

if (size(simin,1)<2) | (size(simax,1)<2)
   fprintf('\n\nNo local maxima/minima found\n');
   fprintf('Too short initial simulation time or non-oscillatory\n');
   fprintf(' response with the given parameters?\n\n');
   fprintf('Check the plot "The last analyzed waveform"\n\n');
   figure; plot(ti,si); title('The last analyzed waveform')
   drawnow; break
end

% The goal function for minimizing  |Einit-Epk|. NB simax
% is divided by E0 (=simax(1)):
% otherwise, any response with small enough initial
% amplitude will meet the convergence criterium.

d =  10* ( (100*simax(2)/E0) - (100*simax(1)/E0))^4;

break
```

```
% LCRresp.m  v. 1.0  040103 JT
%
% The voltage across a parallel LCR tank circuit (the
% voltage E(t) and its derivative E'(t)) after a given
% time 'dt' from a given initial time point t=0.
% and with the given initial conditions E(0) and E'(0).
% Takes into account the underdamped, critically damped,
% and overdamped conditions.
%
% Input: gp, L, C, dt, E(0) and E'(0).
% gp = 1/R is the parallel conductance of the tank circuit,
% dt is the end time,
% E0=E(0) and e0=E'(0) are the initial conditions
%
% Use:  M = LCRresp(E0, e0, gp, L, C, dt)
%
% where M = [E(dt), E'(dt)]
%

function M = LCRresp(E0, e0, gp, L, C, dt)

ALPHA  = gp/(2*C);
OMEGAu = sqrt(4*C/L-gp^2)/(2*C);
OMEGA  = sqrt(gp^2 - 4*C/L)/(2*C);
emAdt  = exp(-ALPHA*dt);

if (4*C/L-gp^2 > 0)        % underdamped
   c1     = E0;
   c2     = (e0 + ALPHA*(E0^2))/OMEGAu;
   cosOdt = cos(OMEGAu*dt);
   sinOdt = sin(OMEGAu*dt);
   vtf    = emAdt.*( c1 * cosOdt + c2 * sinOdt);
   dvtf   = emAdt*( (OMEGAu*c2 - ALPHA*c1)*cosOdt ...
                   -(OMEGAu*c1 + ALPHA*c2)*sinOdt);

elseif (4*C/L-gp^2 == 0)   % critically damped
   vtf  = emAdt.*( E0 + ( e0 + ALPHA*E0)*dt);
   GAMMA = e0 + ALPHA*E0;
   dvtf = emAdt*( GAMMA - ALPHA*d0 - ALPHA*GAMMA*dt );

else                       % overdamped
   c1     = E0 + (E0*(ALPHA-OMEGA) + e0)/(2*OMEGA);
```

```
   c2     = - (E0*(ALPHA-OMEGA) + e0)/(2*OMEGA);
   vtf    =   c1*exp((-ALPHA+OMEGA)*dt) ...
            + c2*exp((-ALPHA-OMEGA)*dt) ;
   dvtf   =   c1 * (-ALPHA+OMEGA)* exp((-ALPHA+OMEGA)*dt) ...
            + c2 * (-ALPHA-OMEGA)* exp((-ALPHA-OMEGA)*dt) ;
end

M = [vtf dvtf];
```

```
% smallfig2.m v. 1.0  020402JT
%
% Generates position vectors for positioning small figure
% windows. Supports dual display. The input argument is an
% integer 1-18 that selects the position of the window on
% the screen according to pattern
%
%       DISPLAY 1         DISPLAY 2
%
%      1    2    3      10    11    12
%
%      4    5    6      13    14    15
%
%      7    8    9      16    17    18
%
% The return value is a position vector that can be used to
% position an open figure window. The following lines will
% open figure 1 and place it to position 7:
%
%   fig_handle = 1;
%   figure(fig_handle)
%   set(fig_handle,'Position',smallfig(7))
%

function [place] = smallfig2(location)

scrsz = get(0,'ScreenSize');     % get the screen size
d2 =  scrsz(3);                  % display width
lm =  scrsz(3)*0.04;             % set left margin
bm =  scrsz(4)*0.09;             % set bottom margin

width  = scrsz(3) *  0.30;       % width  of one figure window
height = scrsz(4) *  0.16;       % height of one figure window
hsep   = scrsz(3) *  0.03;       % horizontal figure spacing
vsep   = scrsz(4) *  0.14 ;      % vertical figure spacing
```

```
% Position format:
%
% left                bottom             width   height

  figure_positions =  [ ...
  lm                  bm+2*(height+vsep) width   height; ...
  lm+width+hsep       bm+2*(height+vsep) width   height; ...
  lm+2*(width+hsep)   bm+2*(height+vsep) width   height; ...
  lm                  bm+height+vsep     width   height; ...
  lm+width+hsep       bm+height+vsep     width   height; ...
  lm+2*(width+hsep)   bm+height+vsep     width   height; ...
  lm                  bm                 width   height; ...
  lm+width+hsep       bm                 width   height; ...
  lm+2*(width+hsep)   bm                 width   height; ...
  lm+d2                  bm+2*(height+vsep) width   height; ...
  lm+d2+width+hsep       bm+2*(height+vsep) width   height; ...
  lm+d2+2*(width+hsep)   bm+2*(height+vsep) width   height; ...
  lm+d2                  bm+height+vsep     width   height; ...
  lm+d2+width+hsep       bm+height+vsep     width   height; ...
  lm+d2+2*(width+hsep)   bm+height+vsep     width   height; ...
  lm+d2                  bm                 width   height; ...
  lm+d2+width+hsep       bm                 width   height; ...
  lm+d2+2*(width+hsep)   bm                 width   height];

place = figure_positions(location,:);
```

```
% harmfit.m  v.1.0 0600103JT
%
% Calculates the difference of a sample waveform a and
% waveform y, which is a superposition of  cosine waves,
% with real weight coefficients ai and phases pi. The angle
% frequency OMEGA*1e9, the weight coefficients for each harmonic,
% and the phases are given in vector c. OMEGA is scaled by 1e9,
% in order to improve convergence.
%
% Input parameter vector c[] format:
% c[ OMEGA DC  A0    P0   HD2  P2   HD3  P3  HD4  P4  HD5  P5  HD6  P6  HD7  P7]
%
% Phases are in degrees. Zero phase = cosine.


function[y] = difference(c)

global si ti;

y=  si - ( ...
      c(2) ...                                        % DC
    + c(3)*cos(1*c(1)*1e9*ti + c(4)*pi/180 )...   % OMEGA*1e9
    + c(5)*cos(2*c(1)*1e9*ti + c(6)*pi/180 )...   % HD2
    + c(7)*cos(3*c(1)*1e9*ti + c(8)*pi/180 )...   % HD3
    + c(9)*cos(4*c(1)*1e9*ti + c(10)*pi/180 )...  % HD4
    + c(11)*cos(5*c(1)*1e9*ti + c(12)*pi/180 )... % HD5
    + c(13)*cos(6*c(1)*1e9*ti + c(14)*pi/180 )... % HD6
    + c(15)*cos(7*c(1)*1e9*ti + c(16)*pi/180 ) ); % HD7
```

Appendix C

Piecewise Sinusoidal Voltage Waveform Model

This Appendix defines the piecewise sinusoidal periodic functions $V(t)$ and $U(t)$ for approximating the LC oscillator steady state voltage waveform, and derives the necessary equations for calculating the period of $V(t)$ and $U(t)$. As is discussed in Chapter 6, the way the voltage dependent capacitors distort the waveform at large signal levels depends on the sign of $V_1 \cdot V_2$. When $V_1 \cdot V_2 > 0$ and $A > |V_2|$, both voltage dependent capacitances will distort the same (either positive or negative) side of the waveform, while the other side will remain sinusoidal. To model these cases, the piecewise sinusoidal function $V(t)$ is defined. When $V_1 \cdot V_2 < 0$ and $A > |V_2|$, both sides of the waveform will be distorted. To model waveforms that are distorted from both sides, another piecewise sinusoidal function, $U(t)$, is defined. The equations for calculating the periods of $V(t)$ and $U(t)$ may then be derived, since the shape of each segment with the given amplitude A and parameter set (V_1, V_2, α, β) is known.

C.0.1 Cases 1 and 2: Only one side of the waveform is distorted when $A > |V_2|$

Figure C.1 shows one cycle of the piecewise sinusoidal function $V(t)$ and defines the end points of each sinusoidal segment.

We can write the equation for $V(t)$ for one complete cycle as [1]:

[1] It would be possible to define the segments in Equations C.1a and C.1b as one continuous piece. However, for employing the symmetry of the function segments, it is useful to define also the point $(\tau_1, 0)$.

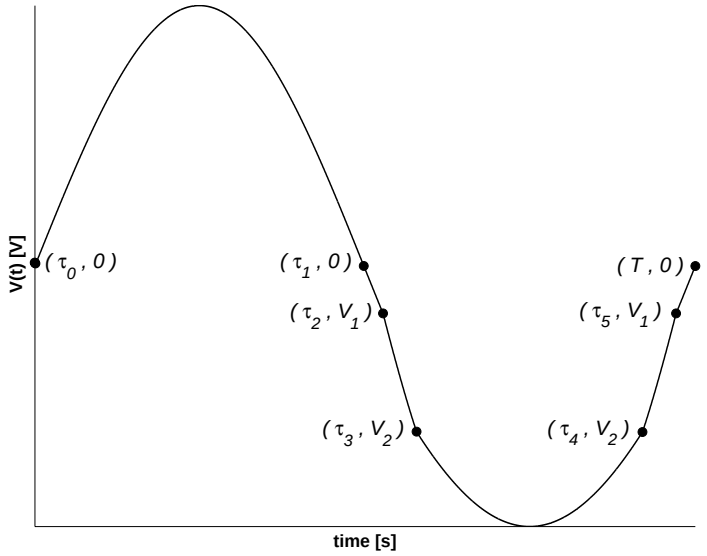


Figure C.1: *One complete cycle of $V(t)$ when $A > |V_2|$. The end points of each sinusoidal segment are marked.*

$$V(t) = \begin{cases} A \cdot \sin \frac{t}{\sqrt{LC_0}} & , \ \tau_0 \leq t < \tau_1 \quad (a) \\ A \cdot \sin \frac{t-\hat{\tau}_1}{\sqrt{LC_0}} & , \ \tau_1 \leq t < \tau_2 \quad (b) \\ A \cdot \sin \frac{t-\hat{\tau}_2}{\sqrt{\alpha \cdot LC_0}} & , \ \tau_2 \leq t < \tau_3 \quad (c) \\ A \cdot \sin \frac{t-\hat{\tau}_3}{\sqrt{\beta_V \cdot LC_0}} & , \ \tau_3 \leq t < \tau_4 \quad (d) \\ A \cdot \sin \frac{t-\hat{\tau}_4}{\sqrt{\alpha \cdot LC_0}} & , \ \tau_4 \leq t < \tau_5 \quad (e) \\ A \cdot \sin \frac{t-\hat{\tau}_5}{\sqrt{LC_0}} & , \ \tau_5 \leq t < T \quad (f) \end{cases} \tag{C.1}$$

For simplicity, the amplitude A is assumed to be the same for all segments. This is reasonable if the tank circuit loaded Q value is high. Strictly speaking, the gain of the oscillator circuit will depend on the voltage in an oscillator that employs the nonlinearity of the gain stage for controlling the amplitude, and therefore, the assumption about constant A is not correct. However, if the RF loss of the circuit is low, the voltage dependent gain of the amplifier will not distort much the waveform. In addition, when we are more interested in the time domain behavior, some error in the amplitude does not matter.

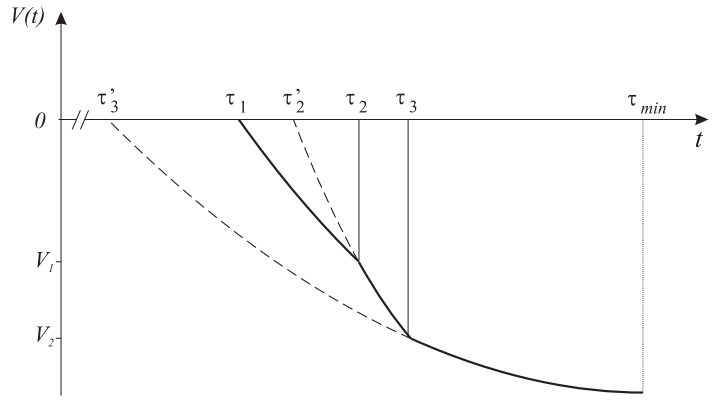


Figure C.2: *A detail of the waveform $V(t)$ (the thick line) for deducing the equations for τ_{21} – τ_{43}. The part after τ_{min} is omitted, since the negative half cycle is symmetrical about τ_{min}.*

The length of the first half cycle for Cases 1 and 2 does not depend on the amplitude of the voltage signal, since only the latter half is distorted. Therefore, we can write directly from Figure C.1:

$$\tau_{10} \widehat{=} \tau_1 - \tau_0 = \pi \cdot \sqrt{L \cdot C_0} \tag{C.2}$$

From Figure C.2 we can deduce the equations for τ_{21}– τ_{43}:

$$\tau_{21} \mathrel{\widehat{=}} \tau_2 - \tau_1 = \sqrt{LC_0} \cdot \arcsin \frac{|V_1|}{A} \tag{C.3}$$

For calculating $\tau_3 - \tau_2$ we first find τ_2' and τ_3:

$$\tau_2' = \tau_2 - \sqrt{\alpha \cdot LC_0} \cdot \arcsin \frac{|V_1|}{A}$$

$$\tau_3 = \tau_2' + \sqrt{\alpha \cdot LC_0} \cdot \arcsin \frac{|V_2|}{A}$$

From the previous two equations we can find $\tau_3 - \tau_2$:

$$\begin{aligned}\tau_{32} \widehat{=} \tau_3 - \tau_2 = & \sqrt{\alpha \cdot LC_0} \cdot \arcsin \frac{|V_2|}{A} \\ & -\sqrt{\alpha \cdot LC_0} \cdot \arcsin \frac{|V_1|}{A}\end{aligned} \tag{C.4}$$

Since the segment from τ_3 to τ_4 is symmetrical about τ_{min}, we obtain

$$\tau_{43} \widehat{=} \tau_4 - \tau_3 = \sqrt{\beta_V \cdot LC_0} \cdot (\pi - 2 \cdot \arcsin \frac{|V_2|}{A}) \tag{C.5}$$

Employing the symmetry of the negative half cycle, we have $\tau_{T5} = \tau_{21}$ and $\tau_{54} = \tau_{32}$. The complete expression for the period of $V(t)$, when $A > |V_2|$, is

$$\begin{aligned}T'_V(V_1, V_2, \alpha, \beta_V, A) &= \tau_{10} + \tau_{21} + \tau_{32} + \tau_{43} + \tau_{54} + \tau_{T5} \\ &= \tau_{10} + 2 \cdot \tau_{21} + 2 \cdot \tau_{32} + \tau_{43} \\ &= \pi \cdot \sqrt{LC_0} \\ &\quad +2 \cdot \sqrt{LC_0} \cdot \arcsin \frac{|V_1|}{A} \\ &\quad +2 \cdot \sqrt{\alpha \cdot LC_0} \cdot \arcsin \frac{|V_2|}{A} \\ &\quad -2 \cdot \sqrt{\alpha \cdot LC_0} \cdot \arcsin \frac{|V_1|}{A} \\ &\quad +\sqrt{\beta_V \cdot LC_0} \cdot (\pi - 2 \cdot \arcsin \frac{|V_2|}{A}) \\ &= \sqrt{LC_0} \cdot \{\pi \cdot (1 + \sqrt{\beta_V}) \\ &\quad +2 \cdot (1 - \sqrt{\alpha}) \cdot \arcsin \frac{|V_1|}{A} \\ &\quad +2 \cdot (\sqrt{\alpha} - \sqrt{\beta_V}) \cdot \arcsin \frac{|V_2|}{A}\}\end{aligned} \tag{C.6}$$

This equation is valid only when $A \geq |V_2|$, since at least one of the arcsin functions is not defined when $A < |V_2|$. However, if the amplitude of the signal in Figure C.1 is adjusted to $A = |V_2|$, points (τ_4, V_2) and (τ_3, V_2) merge, and the time delay τ_{43} is zero. The value of the arcsin function is $\pi/2$, and the lengths of the other time intervals are calculated correctly. For calculating the period of $V(t)$ when $|V_1| < A < |V_2|$, we can replace the $\arcsin \frac{|V_2|}{A}$ factor with a function that assumes the value $\pi/2$ when the arcsin would not be defined. Similarly, if $A = |V_1|$, points (τ_2, V_1) and (τ_5, V_1) merge, τ_{32}, τ_{43}, and τ_{54} are zero, and the value of $\arcsin \frac{|V_1|}{A}$ is $\pi/2$. Therefore, for calculating the period of $V(t)$ with any value of A, we may use the function

$$\begin{aligned} T_V(V_1, V_2, \alpha, \beta_V, A) = \sqrt{LC_0} \cdot \{ & \pi \cdot (1 + \sqrt{\beta_V}) \\ & +2 \cdot (1 - \sqrt{\alpha}) \cdot P \\ & +2 \cdot (\sqrt{\alpha} - \sqrt{\beta_V}) \cdot Q \} \end{aligned}$$

where

$$P = \begin{cases} \arcsin \frac{|V_1|}{A} & , \ A > |V_1| \\ \pi/2 & , \ 0 < A \leq |V_1| \end{cases} \tag{C.7}$$

and

$$Q = \begin{cases} \arcsin \frac{|V_2|}{A} & , \ A > |V_2| \\ \pi/2 & , \ 0 < A \leq |V_2| \end{cases} \tag{C.8}$$

C.0.2 Cases 3 and 4: Both sides of the waveform are distorted when $A > |V_2|$

Figure C.3 shows one cycle of the the periodic piecewise sinusoidal function $U(t)$, and defines the end points of each sinusoidal segment. To make the difference clear from the time coordinate definitions of $V(t)$, notation t_x instead of τ_x is used here for the time coordinates. The equation for one complete cycle is

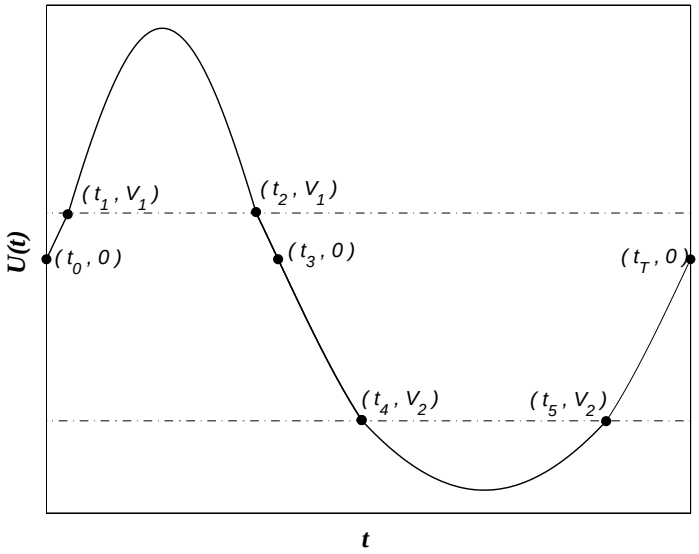


Figure C.3: *One complete cycle of $U(t)$ when $A > |V_2|$, showing the end points of the sinusoidal segments.*

$$U(t) = \begin{cases} A \cdot \sin \frac{t}{\sqrt{LC_0}} & , t_0 \leq t < t_1 \quad (a) \\ A \cdot \sin \frac{t-t_1}{\sqrt{\alpha \cdot LC_0}} & , t_1 \leq t < t_2 \quad (b) \\ A \cdot \sin \frac{t-\hat{t_2}}{\sqrt{LC_0}} & , t_2 \leq t < t_3 \quad (c) \\ A \cdot \sin \frac{t-\hat{t_3}}{\sqrt{LC_0}} & , t_3 \leq t < t_4 \quad (d) \\ A \cdot \sin \frac{t-\hat{t_4}}{\sqrt{\beta_U \cdot LC_0}} & , t_4 \leq t < t_5 \quad (e) \\ A \cdot \sin \frac{t-\hat{t_5}}{\sqrt{LC_0}} & , t_5 \leq t < T \quad (f) \end{cases} \tag{C.9}$$

This time, it is easier to write the equations for t_{10} ... t_{54} and t_{T5}, since each voltage dependent capacitor will distort its own side of the waveform. We can also employ the symmetry of the waveform to find t_{32} and t_{T5}. Using Figure C.3 we obtain the equations

$$t_{10} \hat{=} t_1 - t_0 = \sqrt{LC_0} \cdot \arcsin \frac{|V_1|}{A} \tag{C.10}$$

$$t_{21} \widehat{=} t_2 - t_1 = \sqrt{\alpha \cdot LC_0} \cdot \{\pi - 2 \cdot \arcsin \frac{|V_1|}{A}\} \tag{C.11}$$

$$t_{32} \widehat{=} t_3 - t_2 = t_{10} \tag{C.12}$$

$$t_{43} \widehat{=} t_4 - t_3 = \sqrt{LC_0} \cdot \arcsin \frac{|V_2|}{A} \tag{C.13}$$

$$t_{54} \widehat{=} t_5 - t_4 = \sqrt{\beta_U \cdot LC_0} \cdot \{\pi - 2 \cdot \arcsin \frac{|V_2|}{A}\} \tag{C.14}$$

$$t_{T5} \widehat{=} t_T - t_5 = t_{43} \tag{C.15}$$

The period of $U(t)$ is then

$$\begin{aligned} T'_U(V_1, V_2, \alpha, \beta_U, A) &\widehat{=} t_{10} + t_{21} + t_{32} + t_{43} + t_{54} + t_{T5} \\ &= 2 \cdot t_{10} + t_{21} + 2 \cdot t_{43} + t_{54} \\ &= 2 \cdot \sqrt{LC_0} \cdot \arcsin \frac{|V_1|}{A} \\ &\quad + \sqrt{\alpha \cdot LC_0} \cdot \{\pi - 2 \cdot \arcsin \frac{|V_1|}{A}\} \\ &\quad + 2 \cdot \sqrt{LC_0} \cdot \arcsin \frac{|V_2|}{A} \\ &\quad + \sqrt{\beta_U \cdot LC_0} \cdot \{\pi - 2 \cdot \arcsin \frac{|V_2|}{A}\} \\ &= \sqrt{LC_0} \cdot \{\pi \cdot (\sqrt{\alpha} + \sqrt{\beta_U}) \\ &\quad + 2 \cdot (1 - \sqrt{\alpha}) \cdot \arcsin \frac{|V_1|}{A} \\ &\quad + 2 \cdot (1 - \sqrt{\beta_U}) \cdot \arcsin \frac{|V_2|}{A}\} \end{aligned} \tag{C.16}$$

This expression for the period of $U(t)$ is not defined for $A < V_2$. However, as in the case of $V(t)$, we can replace the arcsin functions with functions P and Q, which are defined for all values of A. For calculating the period of $U(t)$ for any $A > 0$, we can use the function

$$\begin{aligned} T_U(V_1, V_2, \alpha, \beta_U, A) \mathrel{\widehat{=}} & \sqrt{LC_0} \cdot \{\pi \cdot (\sqrt{\alpha} + \sqrt{\beta_U}) \\ & +2 \cdot (1 - \sqrt{\alpha}) \cdot P \\ & +2 \cdot (1 - \sqrt{\beta_U}) \cdot Q\} \end{aligned}$$

where

$$P = \begin{cases} \arcsin \frac{|V_1|}{A} & , \; A > |V_1| \\ \pi/2 & , \; 0 < A \leq |V_1| \end{cases} \tag{C.17}$$

and

$$Q = \begin{cases} \arcsin \frac{|V_2|}{A} & , \; A > |V_2| \\ \pi/2 & , \; 0 < A \leq |V_2| \end{cases} \tag{C.18}$$

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