NTNU

Norwegian University of
Science and Technology

Properties of multicrystalline silicon wafers and case study of PV module viability analysis

Simonas Zickus

Innovative Sustainable Energy Engineering
Submission date: June 2017
Supervisor: Marisa Di Sabatino, IMA

Norwegian University of Science and Technology
Department of Materials Science and Engineering

NTNU – Trondheim
Norwegian University of
Science and Technology

Technical University of Denmark

TMT4915 Master Thesis

Properties of multicrystalline silicon wafers and case study of PV module viability analysis

Student:

Simonas Zickus NTNU-479603; DTU-s152092

Supervisors:

NTNU: Marisa Di Sabatino

DTU: Jacob R. Bowen

Trondheim, Norway

2017

Abstract

Multicrystalline silicon solar cells are becoming a major stream technology. The main reason is the increase of efficiency of solar cells and constant production costs decline. In some countries PV can directly compete with conventional energy generation methods, but in most – incentives are still needed. In this project properties of multicrystalline silicon wafer are described and the relevant experiments are performed. Results show that grain boundary structure is not dependent on the industrial processes, while dislocation density showed a minor improvement. The highest lifetime of wafer minority carriers is observed in the middle of the ingot, while the bottom suffered from the high impurity count. Gettering in most of the ingot had a negative effect on lifetime, but combined with hydrogenation, it out-performed the as-cut case. In addition, simulation of solar power plant was performed for Lithuania, Norway, Germany, Greece, India, China, USA and UAE countries. The main objective was to determine if solar power can compete with conventional electricity generation source, without incentives or feed-in tariffs. Simulation results revealed that Greece and Germany are the best place for solar power generation in private house sector, while Norway and UAE performed the worst.

Acknowledgments

This project would not have been possible without the help of many people. Many thanks to my supervisors Marisa Di Sabatino and Jacob R. Bowen who helped me during all the steps, read and corrected my revisions. Special thanks to Krzysztof Adamczyk, who introduced me to the experimental set-up, helped to understand some of the theoretical principles and consulted during all the experiments. Also, thanks to Birgitte S. Karlsen, who taught me grinding and polishing techniques and to Yingda Yu, who not only introduced me to SEM techniques, but also organized very productive discussions on the relevant topics. And finally, thanks to Gaute Stokkan for participation during the project work meetings and provision of a lot useful insights.

Acronyms

ARC – anti-reflective coating
AC – alternating current
BCC – body centered cubic
CB – conduction band
CI – confidence index
CRT – cathodic ray tube
CSL – coincident site lattice
DC – direct current
EBSD – electron back scatter diffraction
EVA – ethyl vinyl acetate
FCC – face centered cubic
G – gettered
G+H – gettered and hydrogenated
GB – grain boundary
ICx – impurity control, x - ingot number
IPF – inverse pole figure
Mc-Si – multicrystalline silicon
MPPT – maximum power point tracking
OIM – orientation imaging microscopy
PF – pole figure
PL – photoluminescence
PV – photovoltaic
PECVD – plasma-enhanced chemical vapor deposition
RAGB – random angle grain boundary
RES – renewable energy sources
SEM – scanning electron microscope
SoG-Si – solar grade silicon
TW – twin boundary
U – ungeterred
UAE – United Arab Emirates
USA – United States of America
VAT – value added tax
VB – valence band

Table of Contents

1. Introduction

The global solar industry has reached 75 GW installed annual capacity in 2016 with the top leading markets – China, USA, Japan, India and the United Kingdom. – accounting for 80% of installations [1]. This is a 45% increase compared with 2015 of 51 GW installed capacity. Photovoltaic (PV) is as never growing energy source despite this year's low oil and gas prices. The main reasons of solar installation growth are related to its declining production costs, increasing technology efficiency and improving energy demand in Asia. In Europe, the energy policies such as 2020 Energy Strategy (lead by European Commission) also contribute to the growth of renewable energy sources (RES) focusing on 20% RES target of final energy consumption. However, some industry experts believe that global solar market is heading towards a slowdown in 2017, with installed capacity drop of 10%. Specifically, policy turmoil in China, Japan, and the UK is going to hit the overall industry hard — even though the US and India are expected to see the growth [2].

The energy technology is continuously improving and PV market is changing. Currently there are three main types of solar cells in the market: monocrystalline, multicrystalline silicon (Mc-Si) and thin film. In the early 1980s most of solar cells were produced from monocrystalline silicon. Only later, scientists investigated new methods that allow better optimization of production processes and use of multicrystalline structure. Mc-Si solar cells now have higher than 50% share in solar cells market and due to rapid improvement in efficiency and production cost decline, it is believed to stay that way. Thin film solar cells had its ups and downs, but in the past few years market share is decreasing due to the main problem – low lifetime and low efficiency compared to the crystalline solar cells. Additionally, there is a long list of thin film producers, who went bankrupt in the recent years. Therefore, house owners, who are installing these type of modules, are subjected to the higher risk of module warranty service.

Thesis is organized into two main parts. The first part is focused on theory of multicrystalline silicon wafers, production of solar cells, defect mechanisms and description of techniques used in experimental part. The second part is focused on experimental work and is divided into two subparts, which combines research and real project case analysis of solar power plant. In the first subpart, high performance (HP) Mc-Si wafer properties, such as grain boundaries, dislocation density and lifetime of minority carriers, are analyzed. In the second –

solar power plant simulation is performed and solar power viability in different countries is analyzed.

The main goals of the paper are to:

- Describe known defects in and within a crystal in Mc-Si wafers.
- Compare and evaluate grain boundary, dislocation density effects on carrier lifetime in different ingot heights and after different industrial processing steps: as-cut, gettered, gettered and hydrogenated.
- Perform solar power plant simulation and viability analysis in the selected countries and explain the main criteria, which are used to decide whenever to invest or not in the solar power plant.

2. Theory

2.1 Silicon in photovoltaic industry

Silicon as a chemical element is the second (28%) just after oxygen most abundant material in the Earth crust, mostly found as silica (SiO_2) or so-called quartz. Silicon is a IV group metalloid and has properties both from metals and non-metals. The atomic mass is 14 and oxidation states vary from -4 to 4. At room temperature, the silicon density is 2.33 g/cm^3 and melting point - 1414°C.

For solar cell production, very pure silicon is needed since impurities, especially metallic even in small quantities, have a huge impact on solar cell lifetime. Therefore, refining and purification of silicon are crucial techniques in achieving required results. The purification process starts when quartz is reduced in electric arc furnace and directional solidification is the main refining step [3]. In directional solidification, solar grade silicon (SoG-Si) with a purity level of 99.9999% or 6N, is used as a feedstock for multicrystalline silicon Mc-Si ingots.

When silicon is crystallized, and cooled down, the ingot is cut down into smaller bricks. Additionally, due to high impurity content, sides, which have direct contact with the crucible is cut away. Later, ingots are sawed with 100-120 μm thickness diamond plated multi-wire and 150-250 μm thickness wafers are produced. The sawing accounts for roughly 50% loses during the cutting process. In industry, there have been attempts to recycle silicon and use it again, but the industry faces with the main difficulty – decreased efficiency compared to the freshly-grown wafers. Silicon value chain is shown in Figure 1: from quartz to solar cell.

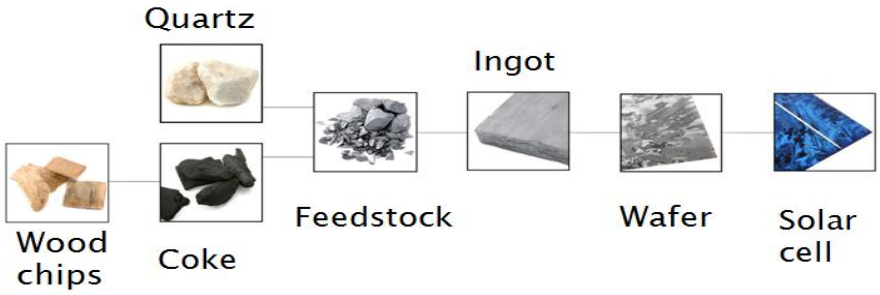


Figure 1. Silicon value chain (*source*: Solar cells lecture slides, picture made by M. Gaal)

2.2 Processes of solar cell fabrication

Multicrystalline silicon wafers undergo a lot of processes before they become solar cells. The steps are described in the order:

- Saw damage removal and etching
- Emitter diffusion and gettering
- Anti-reflective coating
- Screen printing
- Co-firing and hydrogenation
- Edge isolation
- Solar module assembly

2.2.1 Removal of saw damage

Silicon is a brittle metal and is hard to cut it properly without affecting the bulk. For ingot cutting diamond plated wires and various lubricants are used. After sawing, the subsurface damage is around 5-10 μm beneath the wafer's surface and the layer needs to be removed. During the saw damage removal, the surface is etched along the damage in the way to form pyramids. The process is called texturization and is used to trap the light more efficiently [4].

2.2.2 Emitter diffusion

Emitter diffusion is used to create a p-n junction. High resistance thin layer of emitter is deposited on top of the substrate using PECVD method. Additionally, low resistance highly doped emitter is deposited exactly underneath where contact metallization bus bars will be placed to reduce contact resistance [4].

2.2.3 Gettering

During emitter diffusion, a very important step for controlling impurity concentration is performed, called gettering. Gettering is a process, where electrically active metallic impurities such as iron are diffused away to the inactive layer in order to increase the minority carrier lifetime and diffusion length. [5]. In multicrystalline silicon wafers metallic impurities especially tend to decorate the areas with high crystallographic defects such as grain boundaries and dislocation clusters, so naturally gettering is mainly focused to improve these areas.

Gettering can be classified into two categories: intrinsic and extrinsic. In intrinsic gettering interstitial oxygen in the lattice is used to catch and diffuse the metallic precipitates from the bulk of the wafer. In extrinsic gettering an additional stress in the surface is created so that it acts as an active impurity trapping sites for the metallic impurities for the bulk. Impurities tend to agglomerate towards the electrically inactive surface which is less harmful [6]. However, impurities are not only diffused away to the inactive layer, but also new defect mechanisms will form due to re-precipitation. [7]. In the recent study [8] the results show that gettering has a positive effect on carrier lifetime only in the ingot areas with high impurity concentration. High impurity areas are normally the ingot bottom – due to the contact with crucible; and top – due to the metallic impurity segregation. Therefore, in the middle of the ingot, where metallic impurity concentration is low, the positive effect of gettering is offset by the new defect mechanisms and total carrier lifetime is even decreased. The situation is improved by introducing hydrogenation process. During the phosphorous emitter diffusion, the glassy surface will be deposited. For further process, it needs to be etched away.

2.2.4 Anti-reflective coating

Standard silicon reflects more than 30% of the incident sunlight and for solar cells performance it is very important to minimize the reflection as much as possible. After the texturization and anti-reflective coating (ARC) steps, silicon solar cells will reflect less than 5% incident light. In industry, the most used ARC is silicon nitride Si_3N_4 [9]. Normally a thin layer of approximately 70 nm is deposited on the surface of the wafer using PECVD method. A quarter wave interference effect is created, which cancels out the interference of light reflected from the upper and the lower part of ARC. Due to this effect, solar cell color is changed to the dark blue. Additionally, Si_3N_4 ARC acts as a passivation layer for recombination active sites in the surface and in the bulk. [10].

2.2.5 Hydrogenation

Silicon treatment with hydrogen in solar cells has been used widely for some decades. Hydrogen is the smallest known atom and has a high reactivity in silicon lattice with practically all the impurities. Hydrogen can have different charge states: a positive H^+, neutral H^0 or negative H^- charge state [11]. In p-type silicon there are many impurities, which create energy levels close to the middle of the bandgap, and the defects have much bigger impact then they do in n-type silicon solar cell. The main aim of the hydrogenation is to diffuse into the lattice and passivate defects, so that they will not contribute to degradation of solar cell performance anymore. Almost all the defects in p-type silicon will have positive charge, therefore hydrogen charge state is controlled to have neutral or negative charge to allow better reactivity with the defects [12].

2.2.6 Solar module assembly

Prepared solar cells are aligned into rows and connected by metallic pathways. Later, solar cell grids are place on the large plate of glass (in finished module, glass is the front) and cells are encapsulated in ethyl vinyl acetate (EVA), which provides adhesion between cells, top and rear surface. Finally, the frame is added and the module is laminated. Complete module undergoes heat treatments to make sure that EVA is polymerized and module is bonded together. For glass-glass solar module, solar cells are encapsulated into the glass and no metallic frame is needed, therefore, no additional grounding is necessary. Glass-glass standard solar module weighs around 50% more compared to the standard solar module.

2.3 Band gap

Term bandgap is used to describe a pair of atoms, which form a molecule, and their orbitals are arranged in slightly higher and lower energy level than each will have separately [13, Chapter 3.3.1]. In pure silicon, no electron states can exist between the valence band (VB), which corresponds to the lower energy state, and conduction bands (CB), which is the upper energy level. For electron to be promoted from VB to CB, certain minimum amount of energy is needed and that energy is equal to band gap energy. In direct bandgap electron is promoted directly and in indirect – electron needs additional energy due to the moment shift. The required additional energy is supplied by phonons – lattice vibrations [13, Chapter 3.3.4]. In silicon solar cells, the main energy source for electrons are photons. Direct and indirect band gap is shown in the Figure 2.

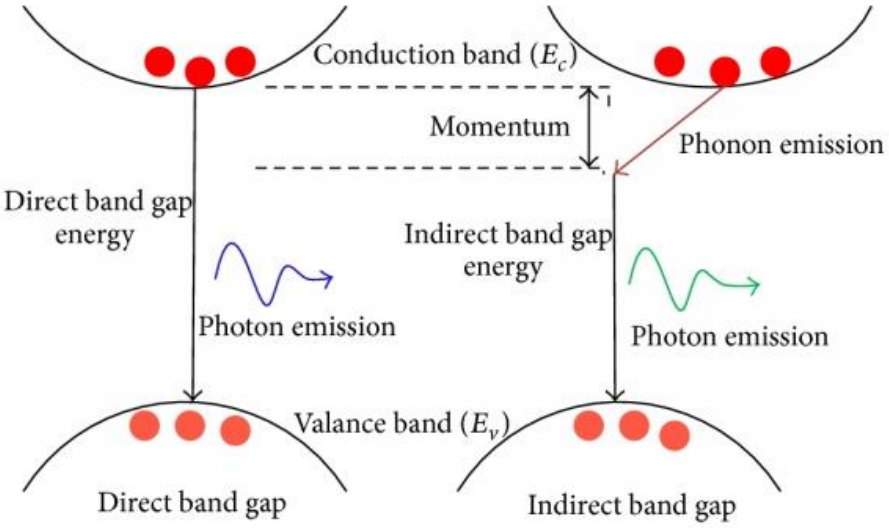


Figure 2. Direct and Indirect band gaps (*source*: [14])

Silicon is an indirect semiconductor and has 33.16% maximum theoretical efficiency at standard conditions according to the calculations made by Shockley and Quesser [15]. The main factors limiting the efficiency are not optimal bandgap width of 1.34 eV and most importantly inability to absorb full light spectrum. resulting in maximum. The maximum efficiency dependence on band gap width is shown in Figure 3.

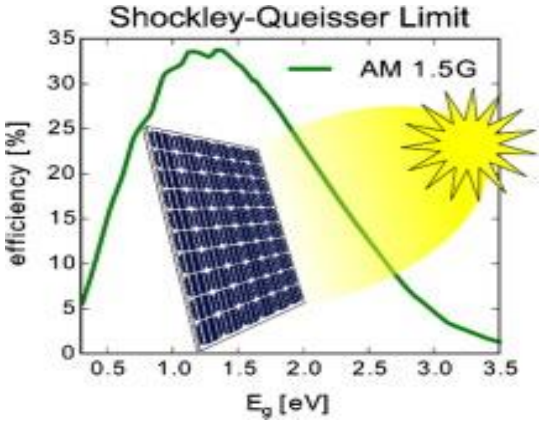


Figure 3. Maximum theoretical efficiency of solar cell (*source*: [16])

There are many materials or combination of materials, which have better properties than silicon, but they all have serious drawbacks: availability, manufacturing and production costs etc. For example, some semiconductors have the band gap values even closer to the theoretical limit such as cadmium tellurium CdTe of 1.49 eV or gallium arsenide GaAs of 1.43 eV. However, production of those materials is significantly more expensive and life time is shorter.

Therefore, silicon as material for solar cells was chosen because of its availability (2nd most abundant material in Earth's crust), appropriate band gap, which is 1.12 eV, giving maximum theoretical efficiency of 31%, low production costs, high durability and long lifetime of at least 30 years.

2.4 Impurities

Impurities in silicon can be separated into two groups: dopants – added voluntarily to improve charge carrier collection and therefore - conduction; and contaminants – introduced unintentionally due to limited production techniques, exposure to environment etc. Contaminants have a negative effect on solar cell performance due to the increased recombination of charge carriers [17]. However, contamination during silicon processing are unavoidable. It includes contamination from the atmosphere: carbon, oxygen, hydrogen and nitrogen are quite difficult to remove; metallic impurities: iron, chromium and titanium, which reduce the diffusion length. Contaminants like nickel, copper do not reduce the diffusion length, but rather affect the recombination rate [18]. Big part of unwanted metallic impurities can be removed by segregation during directional solidification process. Dopants such as Boron or Phosphorous, which are mainly used for p-type and n-type doping respectively, are added to silicon solar cell to improve properties. However, during silicon refining process, they are also treated as contaminants, since they appear in much larger concentrations than needed.

2.5 Doping

In silicon solar cells, doping is used to improve collection of charge carriers. Material is called n-type if dopant is from III group periodic table and have 5 valence electrons, while silicon has 4 valence electrons. In this case doping creates the excess of electrons and Fermi level shifts towards the CB, where Fermi level shows the probability of 50% to find the electron at any given time with certain energy. For p-type doping materials from V group are normally used and doping creates shortage of electron or in other words – holes. In this case Fermi level shifts towards the VB.

2.6 Defects

Atoms in the crystal are arranged in self-repeating three-dimensional patterns, where the unit cell is the smallest building block, which characterizes crystal structure. By repeating it along the axis, crystal lattice is obtained and crystal is constructed by stacking unit cells in

three dimensions. The most common arrangements for atoms are: face-centered cubic (FCC), body-centered cubic (BCC) and close-packed hexagonal. Silicon has a FCC arrangement, where atoms are positioned in a square and in the middle of surface areas [19, Chapter 1].

Perfect crystal configuration is preferred energetically due to minimization of energy needed to maintain the structure, but crystal will always have some flaws, imperfections due to the presence of external forces. Defects can be separated into four categories according to order of the dimension. Zero-dimension point defects appear locally near the single atom. One-dimensional line defects, also called dislocations, appears in the lines, where crystal pattern is changed, due to the misalignment of atoms. Two-dimensional surface defects and three-dimensional volume defects change the pattern of the surface or volume of the crystal accordingly [20, Chapter 4].

2.6.1 Point defects

There are two types of point defects: intrinsic and extrinsic. Intrinsic defects are caused by the removal of local atom or its change in the position, while extrinsic is caused by impurities.

2.6.1.1 Intrinsic defects

Intrinsic defect appears, when the atom is missing in the crystal structure. Absence of the atom is called vacancy. When atom occupies another place, where no atoms should be present, is called self-interstitial.

Self-interstitial defects have unfavorable bonding and are very uncommon. Self-interstitial defect appears because of grain boundary interface – compression forces misplaces or distorts crystal structure and atoms occupy unusual place in the structure. The most common intrinsic defect is vacancy, which accounts for the significant part of crystal defects. Atoms due to solid state diffusion, migrate from one vacant place to another or between the lattices [20, Chapter 4].

2.6.1.2 Extrinsic defects

Extrinsic point defects appear if foreign atoms diffuse into the crystal lattice. As in intrinsic defects, the foreign atoms can occupy interstitial position in the crystal structure and only small size foreign atoms can occupy it. Larger foreign atoms take the vacant place or kick

out the original lattice atoms and take their place [20, Chapter 4]. Vacancy, self-interstitial and substitutional defects are shown below in Figure 4.

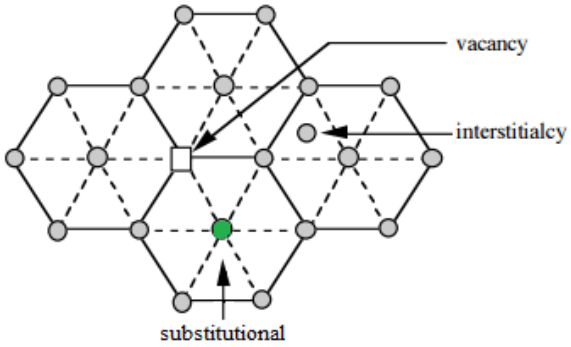


Figure 4. Vacancy, self- interstitial and substitutional defects (*source*: [20, Chapter 4 p.78])

Introducing extrinsic substitutional atoms are widely used in semiconductor materials to control electrical properties such as concentration of charge carriers. The inclusion of foreign atoms to control electrical properties is briefly covered in "Doping" section.

2.6.2 Line defects

Line defects or so-called dislocations appear due to plastic deformation if atomic planes slide over each other. Dislocations mainly forms during the growth of the crystal influencing the structure and in most cases, are unwanted, since they have negative impact on material electrical properties. Two main line defects are edge and screw dislocations [20, Chapter 4].

2.6.2.1 Edge dislocations

Edge dislocations appear if lattice has an extra half plane of atoms inserted and pattern is disturbed. Burgers vector is used to describe the characteristics of dislocation in the material. In the perfect crystal, a rectangle can be drawn with the vector. However, in the presence of dislocations rectangle is not closed and Burgers vector is used to show the missing part, which is needed to complete the circuit in the dislocation area. In edge dislocation Burgers vector is perpendicular to the dislocation line. Edge dislocation is shown in Figure 5 below.

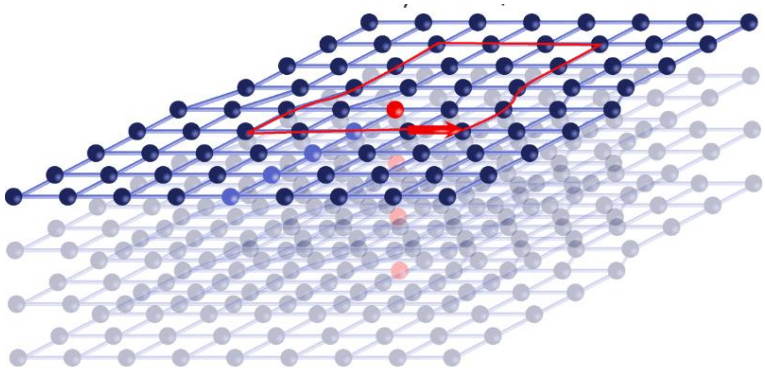


Figure 5. Edge dislocation (*source*: [21])

2.6.2.2 Screw dislocations

Screw dislocations appear if lattice is sheared and offset compared to the other lattice. The name screw dislocation is used, because if drawing rectangle in the crystal lattice, you would end up exactly below the starting point, and the form resembles a screw. In screw dislocations Burgers vector is parallel to the dislocation line. Screw dislocation is shown in Figure 6.

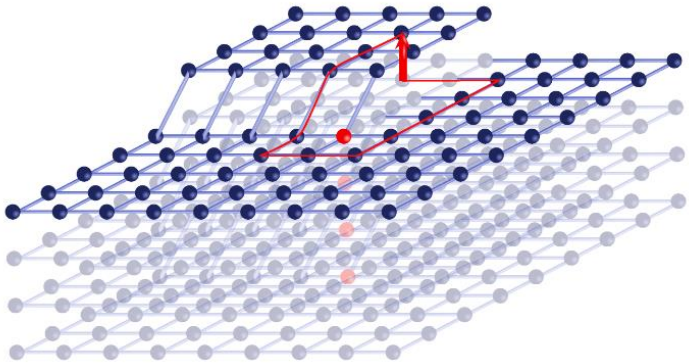


Figure 6. Screw dislocations (*source*: [22])

2.6.3 Two-dimensional defects

Two-dimensional defects in crystal structure can be divided into three groups: free surfaces, interfaces between crystals such as grain boundaries and interfaces within crystals i.e. twin boundary.

2.6.3.1 Free surfaces

Free surface defects appear in the interface between a solid and liquid or vapor phases. It is the area, where liquid or gaseous material starts to solidify. The interface atoms with loose bonds or so called dangling bonds is an attractive place for unwanted smaller atom fills such as oxygen, phosphorous, sulfur [23, Chapter 4].

2.6.3.2 Grain boundaries

The interface between the crystals – is unavoidable in the nature and is called a grain boundary (GB). GB forms, when grains or small crystals are compressed during the crystallization against each other, and it limits crystal growth. Crystals are not perfectly matched against each, there are always misorientation between them, which leaves unfilled gaps, and the GB area is a perfect place for impurity diffusion. Impurities may add additional barrier in the bandgap, which acts as a trap for charge carriers. Additionally, the intermediate band is a perfect place for carrier recombination. If the defect is shallow and close to CB, it traps electrons (acceptors) and if defect is close to VB – holes (donors). Defects close to the center of bandgap are capable of trapping both charge carriers and have the biggest impact on carrier recombination [13, Chapter 8].

GB can be separated into two types depending on misorientation angle: low angle, if misorientation is lower than 15 degrees, and high angle - for 15-180 angles. Grain boundary angle can be calculated by formula:

$$tan\frac{\theta}{2} = \frac{b}{2d} \quad (1)$$

Where: θ - angle of dislocation, b – Burgers vector, d – the spacing of the dislocation array. In the interface atoms accommodate change of the angle and packing become closer when the angle θ decreases leaving less space for possible impurity atoms. Dislocation angle between grains is shown below Figure 7.

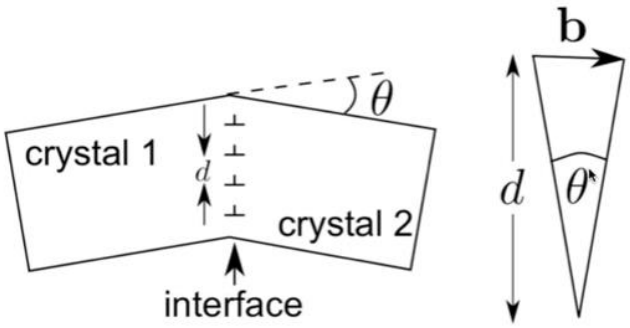


Figure 7. Dislocation angle between grains (*source*: [24])

Coincident site lattice (CSL) is a method used in electron backscatter diffraction (EBSD) analysis as a tool to categorize, monitor or track micro structural changes in GBs [25]. The degree of fit sigma Σ shows the coincidence ratio between two lattices. Total number of the atoms in the GB are calculated and divided by the number of shared atoms between the lattices. For example, if Σ equals to 3, then every third atom is shared, Σ equals to 9 – every ninth, Σ equals to 27 – every twenty seventh and etc. The higher the sigma value, the higher the disorder is between the grains, which means that more space is left for impurity atoms to diffuse in and affect the recombination rate. According to the previous studies of multicrystalline silicon, Σ3 value is between 22% and 64%, Σ9 – between 9% and 12%, and Σ27 – between 3% and 9% of total grain boundaries [26-28]. It is known that impurity contamination has a decisive effect on electrical properties of the material. While Σ3 introduce shallow energy levels in the band gap, Σ9 and Σ27 introduce deep levels in the band gap and accelerates recombination activity of the GB [29].

2.6.3.3 Twins boundaries

Twin boundaries (TB) are a defect within a crystal, which appears in the regions, where crystals undergo plastic deformation and a steady shear. The original crystal structure is mirrored and reflected in a new direction [12, Chapter 1]. TBs containing low-energy are orientated in (111) plane. There is no requirement for broken, disturbed bonds or dislocations; therefore, energy needed to create them is low [30]. High energy twin boundaries are orientated in (221) plane and tend to attract impurities due to precipitation. The difference in simple grain boundary and twin boundary is shown in Figure 8.

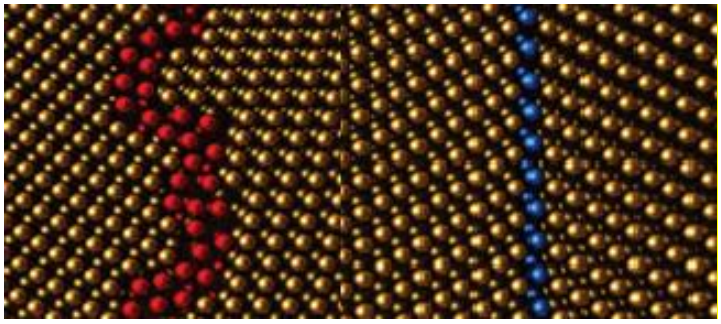


Figure 8. Grain boundary (left) and twin boundary (right) (*source*: [31])

In the multicrystalline silicon twin boundaries correspond to a large fraction of grain boundary defects. The most common is a low-energy Σ3 coherent twin boundary, which has a low impact on carrier recombination; therefore, it is an acceptable defect in photovoltaic silicon. Twin boundaries with higher order of sigma value such as Σ9 and Σ27 are considered as unwanted due to higher recombination activity [32]. However, the most recombination active GB is random angle grain boundary (RAGB).

2.6.3.4 Stacking Faults

Stacking faults is a defect within the crystal and appears locally in the regions, where perfect crystal stacking structure is disturbed. Stacking faults affects the plasticity of crystals they appear in close packed structure with ABC sequence. In FCC structure, there are two main stacking types: intrinsic and extrinsic. In intrinsic part or all the layer is removed (layer C, Figure 10), but the sequence continues further according to the pattern. In extrinsic – a new layer is introduced between the planes (B and C, Figure 10) and the added layers do not belong to the continuous pattern [19, Chapter 1]. The intrinsic and extrinsic defects are shown below in Figure 9.

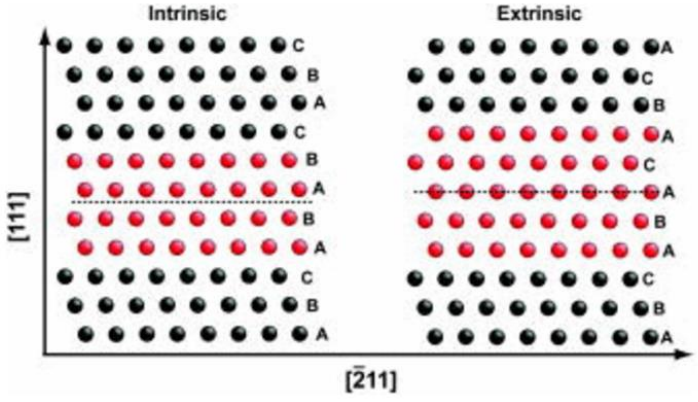


Figure 9. Intrinsic and extrinsic stacking faults (*source*: [33])

2.6.4 Volume defects

Volume defects appear in three-dimensional crystal structures. They can be divided into four groups according to the size and effect: precipitates – a small, part of micron size particles, which increase the strength of the material; dispersants – medium sized particles of 10-100μm intentionally introduced to the structure to enhance electrical or mechanical properties; inclusions – large particles, which entered the structure as a dirt or by precipitation and negatively alters electrical properties; voids – holes in the structure [20, Chapter 4].

2.7 Scanning Electron Microscope

Scanning electron microscope (SEM) consists of the two major components: electron column and control console. Electron column contains an electron gun, condenser lenses, objective lenses, apertures, detectors. The main goal of lenses, apertures in SEM is to control the pathway of electrons going through the evacuated tube. Vacuum of about 10^{-5} lower than the atmospheric is provided in to avoid electron collision with gas molecules, which might influence the pathway. Electron gun generates accelerating voltage of 0.1-30 keV and after focusing, the beam is shot down the column onto the sample. Then specimen scatters electrons, which are collected in the detectors and results are analyzed [34, Chapter 2]. Control console consists of cathodic ray tube (CRT) used for viewing screen, button and knobs for the control of electron beam. The principle scheme of SEM is shown in Figure 10.

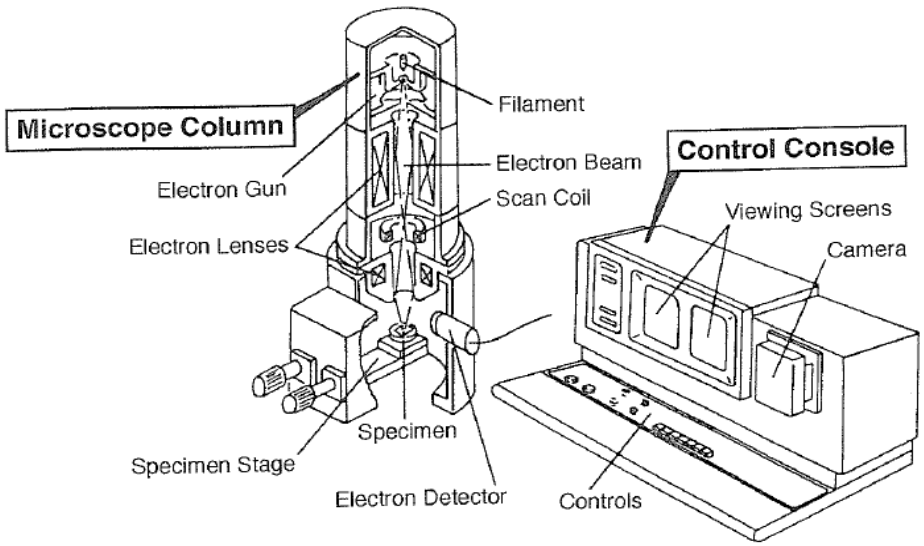


Figure 10. SEM principle scheme (*source*: [34, Chapter 2])

The most common and the least expensive electron gun is tungsten wire. The main disadvantage of this type of electron gun compared to field emission gun, is the resolution and lifetime of the filament. Filament operates at high temperatures between 2000-2700 K and slowly evaporates during the use. Higher temperatures and operation at oversaturation points decrease the lifetime of the tungsten wire significantly, which becomes finer and breaks eventually. Expected lifetime of the wire is up to 100h of operation [34, Chapter 2].

2.8 Electron Backscatter Diffraction

Electron Backscatter Diffraction (EBSD) is a characterization technique used to study the crystalline material diffraction patterns of the backscattered electrons. Kikuchi lines, which are formed by the diffraction pattern, are indexed and crystal orientation is obtained. Lines represent the characteristics and orientation of the diffracting plane. In order to project results in pole figure (PF), inverse pole figure (IPF) or Orientation Imaging Microscopy (OIM), the stereographic projection is employed. In OIM map a color represents a grain orientation defined by IPF [35].

2.9 PV Scan

For dislocation density PV Scan 6000 instrument is used to scan the silicon wafers and provide the maps of dislocation density, grain boundary distribution. Before scanning, selective etching is used in order to strengthen the obtained signal. Sample is immersed into different acids, where grain boundaries and dislocations are etched faster compared to the grain. A point on the sample is illuminated with laser beam and light is reflected. Defects in the surface scatters light more than a grain giving different signal, which is processed and color map is drawn. For dislocations and grain boundaries two different detectors are used.

2.10 Photoluminescence imaging

Photoluminescence imaging (PL) is a technique used widely for PV performance inspection. To obtain minority carrier lifetime estimation, this technique requires metallic contacts, therefore, solar cells must be fully prepared. In PL imaging, silicon solar cell surface is excited and it emits luminescence emission [36]. Camera captures the signal and records values for the exact point. Later PL image can be reconstructed using MATLAB or other software. For PL imaging, wafers were sent to IFE institute in Oslo.

3. Experimental set-up

3.1 Examined materials

The investigated p-type Mc-Si wafers are a part of large research project run by SINTEF, IFE (Institute for Energy Technology) and NTNU (Norwegian University of Science and Technology). A test ingot IC1 contains two sides: quasi-mono and high performance multicrystalline silicon. Quasi-mono part was produced by adding mono silicon seeds in the bed with the goal to influence the crystallization. The main body crystalizes in mono-like structure, while corners have multicrystalline structure. High performance (HP) ingot was produced by adding small size silicon grain layer or so-called incubation layer in the bottom of the bed. Incubation layer limits the growth of the crystals and by adjusting the seed size, the grown crystal size can be controlled. HP process results in higher amount of grain boundaries, but lower dislocation propagation, since it is stopped by the GBs. Crystallization of quasi-mono and HP Mc-Si is shown in Figure 11.

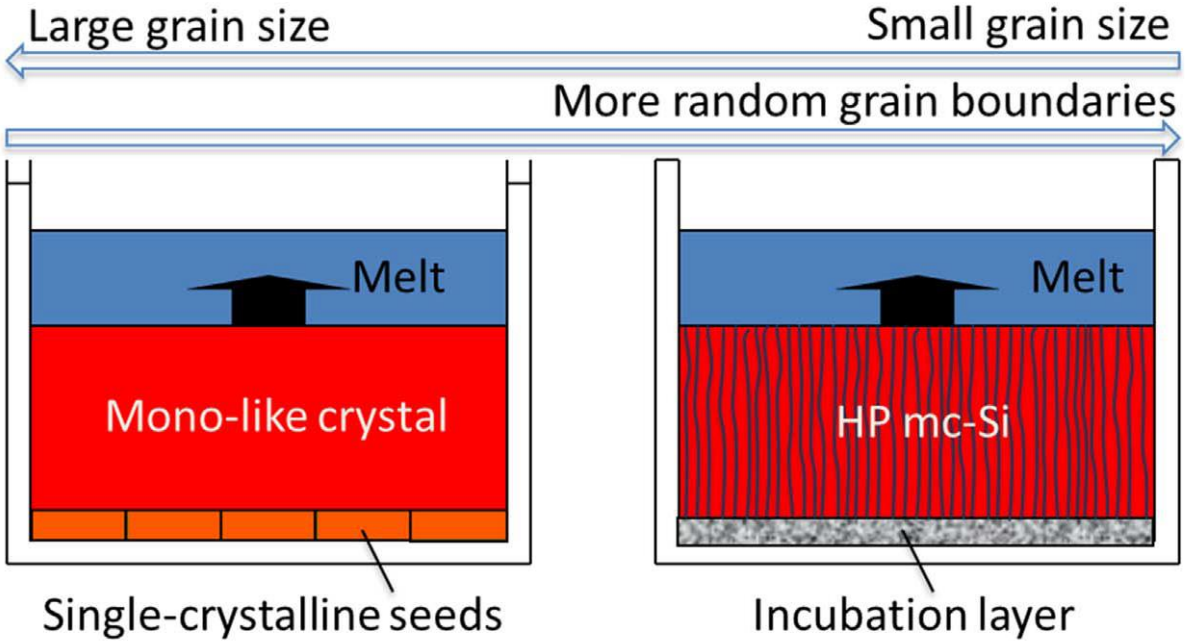


Figure 11. Crystallization of quasi-mono and HP silicon (*source*: [37])

The main task of the experiments is to observe and determine how industrial processes during solar cell fabrication influence defects and how they affect lifetime at different ingot heights. Wafers were produced and provided by SINTEF research institute. Left side of high performance wafer is HP and right – quasi-mono. The ingot was cut into 280 wafers, where

lower numbers corresponds to the lower part of the ingot or closer position to the bottom. The size of the wafers is a standard value of 156×156 mm and average thickness is 200 μm. The main interest is in the first half of the ingot; therefore, wafers were selected accordingly at the positions 10, 40, 70 and 130.

The thermal graph of the ingots IC1, IC4 and IC5 is shown in Figure 12. First, the feedstock was put into crucible and then heated up to the temperature of 1550 C°. After melting of the feedstocks, IC1 ingot was cooled down in 16h, IC4 ingot was cooled down in 12h and ingot IC5 was first annealed at 1200 C° for 6h and then cooled down in 12h. In Figure 12 cross section of the ingot is shown, b – IC1 crystallization profile, c – IC1 comparison with IC4 and IC5 ingots, d – quasi-mono and high-performance ingot after crystallization. In the thesis only IC1 ingot was analyzed.

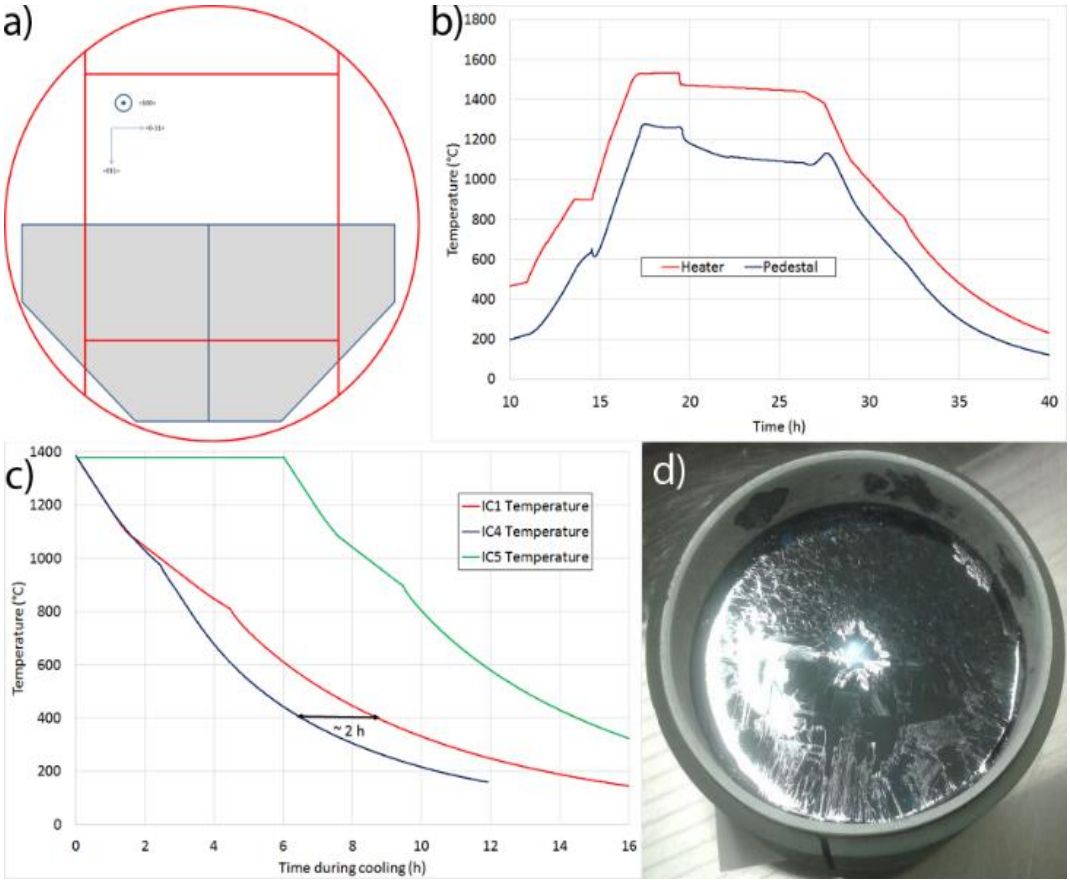


Figure 12. Ingots IC1, IC4 and IC5 crystallization characteristics (source: Presentation "Impurity control workshop" by G. Stokhan)

3.2 Sample preparation

3.2.1 Laser cutting and marking

For further analysis, wafers should be cut into smaller parts. Laser was used to cut the selected wafers into 50x50 mm leaving 6 mm horizontal and vertical segment unused. The wafer cutting grid is shown in Figure 13.

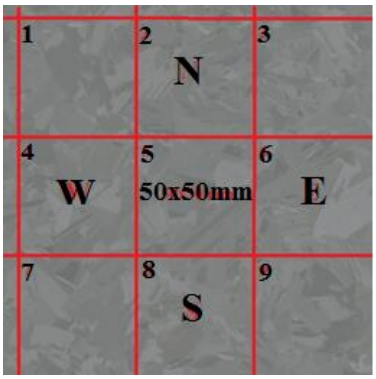


Figure 13. The laser cutting of the wafer into 9 parts

During the laser cutting, wafers were marked and the area of interest was selected. The area was selected according to the previous research of Krzysztof Adamczyk. The size of the area was discussed with the supervisor and agreed to increase when moving to the top of the ingot since grain diameter increases too. Area selection and dimensions are shown in the Figure 14.

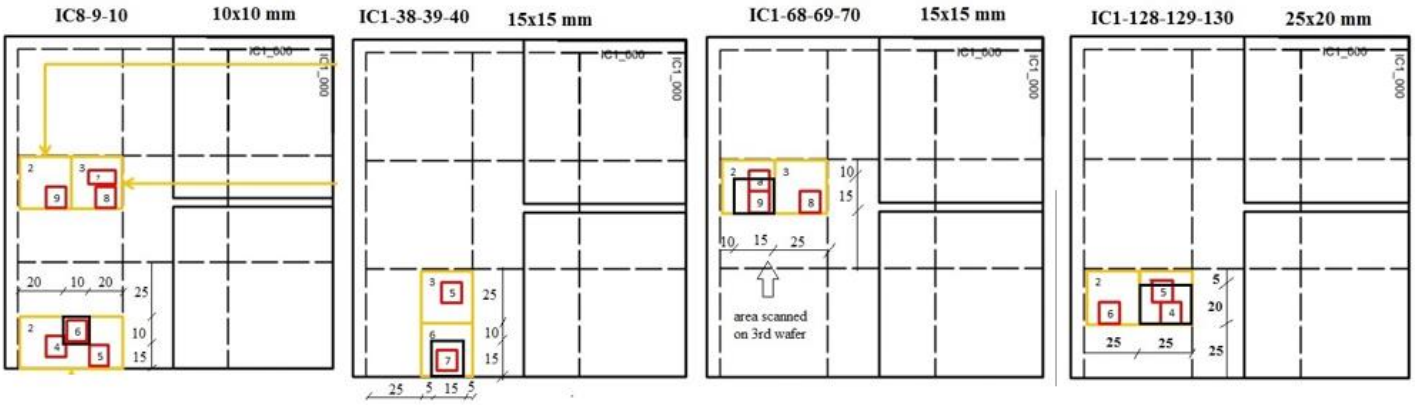


Figure 14. Selected areas for wafer analysis

3.2.2 Grinding and polishing

For further wafer analysis, it is important to polish the sample surface in order to improve the output signal. First, the wafer is grinded with rough grit paper of 1200 for 3min.

Then wafer is polished with 9, 3 and 1 micron particle size paper for 5min each. It is important to remember that during each step of the wafer processing, it is very easy to break it, because the thickness is only 0.2 mm and silicon is very brittle. In collaboration with SINTEF research analyst Gaute Stokhan grinding and polishing manual was prepared. It helps to standardize the procedure and obtain good quality results. Grinding and polishing manual is presented in appendix A.

3.2.3 Electron backscatter diffraction

Even though there are many modern SEM microscopes in the laboratory for EBSD analysis, quite old tungsten wire scanning electron microscope (SEM) was used. It is the only microscope, which offers a moving stage for EBSD combo scan of large areas. Electron beam was set to 20keV, working distance – around 30mm and sample was tilted 62°. When processing data with OIM software, true orientations of the grains was obtained by rotating the sample by -87° around ND axis. EBSD set-up is shown in Figure 15.

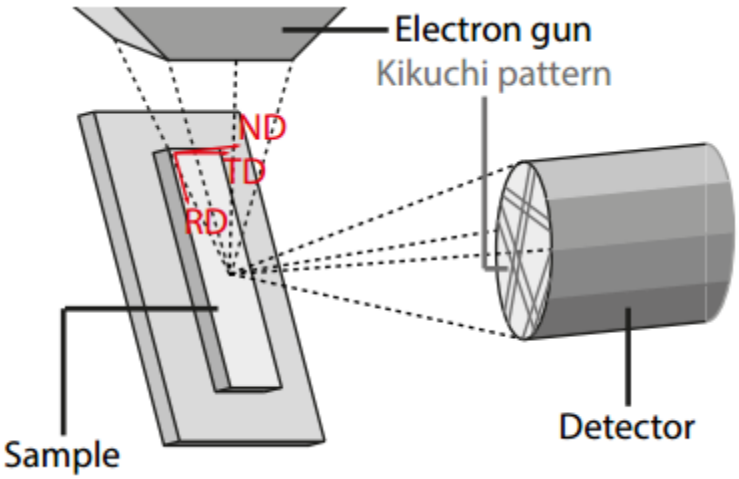


Figure 15. EBSD set-up (source: OIM manual)

The size of the area for EBSD analysis was chosen according to the wafer position in the ingot. During some scans electron beam became unstable and part of the sample data turned to the black line due to changing current and inability to obtain Kikuchi patterns. Additionally, indexing errors due to imprecise calibration arose. These were solved by manually changing beam current to obtain the clear image for the diffraction patterns. Finally, there have been some random magnification changes from 70x to 7000x altering the data set. The problem

appeared only few times and was eliminated by resetting the machine. The unsuccessful EBSD scan is shown in the Figure 16 below.

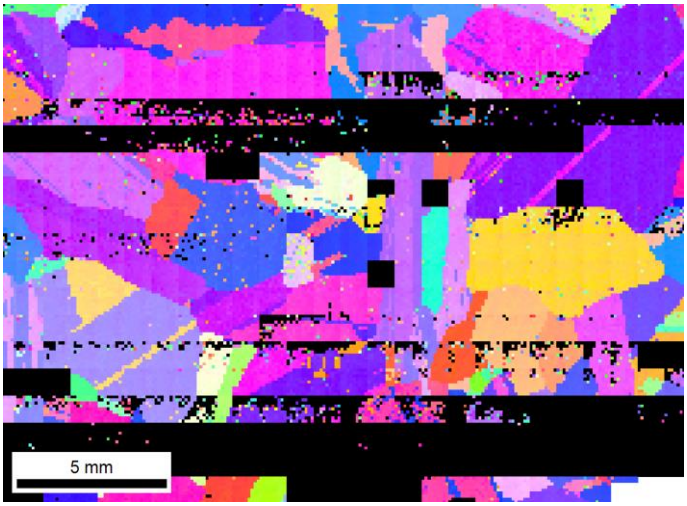


Figure 16. EBSD failed scan

After EBSD scans, mainly different orientation dots appear in the grain. Using OIM software's enhancement methods, the quality of the results is improved. In some cases, part of the data might be lost due to the imperfect algorithms, e.g. twin boundaries might be incorporated into the grain. Firstly, neighbor confidence index (CI) correlation for minimum of 0.1 was set, where in situations, when CI was lower, the neighboring value was taken instead. Secondly, grains were standardized for the minimum of 5 with tolerance angle 5, meaning that smaller grains than 5 pixels and or lower angle of 5 are not treated as a separate grain.

3.2.4 PV Scan

For dislocation density measurements PV Scan 6000 instrument is used. In order to obtain the desired results, wafers must undergo a selective etching procedure. Wafers are immersed in the bath HF acid bath, which etches dislocations faster than grains improving the output signal. After the preparations, wafers are placed on the PV Scan instrument holder and illuminated with a laser beam. The integrating sphere collects the signals from the scattered light. Higher dislocation areas tend to scatter light more, therefore collected signal will be stronger. Scanning speed of 20 mm/s was set by default. Increasing the scan speed might cause unreliable results since integrating sphere might not be able to catch and process all the data. The resolution is 200 µm, which is the step size between the lines shown in the graphs in the results section.

3.2.5 Case study of PV power plant

PV market is growing at the accelerating rates. The market has shifted towards Asia, where China is a major player. However, in most countries PV without subsidies find it hard to compete with conventional fossil fuel electricity generation. In this part of the thesis different countries will be compared and viability analysis will be performed.

The main purpose of this section is to link research analysis with the real-life data and to perform a brief overview of solar industry viability in different countries (I struggled to find any systematic comparison between the countries at the time of writing). In cooperation with solar cell project coordinator company "Saules graza" – the standard sized solar power plant of 5kW was selected. Furthermore, two cases were evaluated: one with standard multicrystalline solar cells used in industry and another – premium class, high durability multicrystalline solar cell. A solar cell system of 5kW PV plant is a standard choice for one family 150 m^2 house with a moderate electricity consumption. It is assumed that the electricity is consumed in the household, while excess is supplied to the grid and bought back later with no additional cost. To check PV viability, no incentives or tariffs for PVs are included. Solar power plant project consists of three main parts: documentation, materials, installation. It is assumed that material price does not differ across the world, while labor-intensive work depends on average country's salary. Lithuania was taken as a starting point with 630 € average salary and others – adjusted accordingly. Labor cost may vary drastically due to the economic differences in society, e.g. income in Norway is distributed quite evenly while in countries like China, USA and especially UAE very cheap labor force can be used. Obtaining exact information about the real project costs in selected countries might give more accurate results, but the reliable data is quite hard to find. For the project inside information of the company "Saules graza" is used for the purpose of this analysis. Project target is rather a single household than company, so value added tax (VAT) is also included in the calculations.

For economic analysis, selected countries are as follows: Norway: capital – Oslo, Lithuania: capital – Vilnius, Greece: capital – Athens, Germany: highly solar power developed region – Bavaria, USA: one of the best place for PV – California, China: capital – Beijing, India: capital – Delhi, United Arab Emirates: one of the biggest PV plants to be built – Dubai. Irradiance for bigger countries may vary drastically, therefore, capitals or major PV industry centers were selected for the analysis.

Solar resource is split unevenly around the world, where Europe gets the lowest average irradiation among all the continents. In Figure 17, the global solar resource is shown.

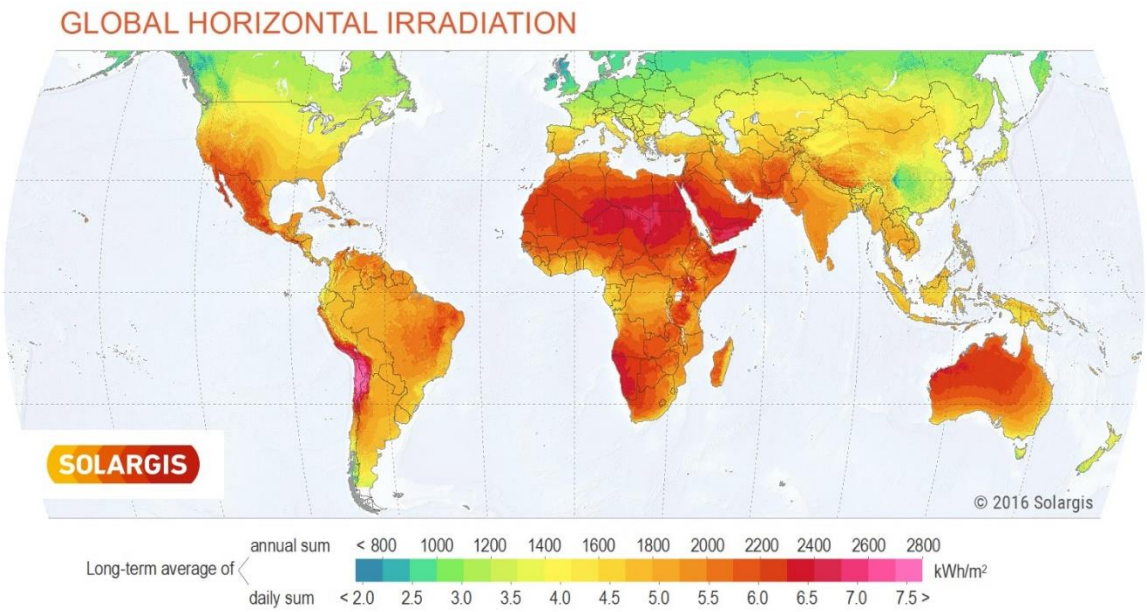


Figure 17. Solar irradiance map (*source*: [38])

Low solar irradiance did not stop Germany for becoming number one country of installed PV back in 2012 with a share of 50% total installed PV. Only later generous feed in-tariffs were cut and installations stabilized. Nowadays when you visit south of Germany, it is hard to find a rooftop not occupied with PV. A picture of a village in South Germany is shown in Figure 18 below.

Figure 18. Solar irradiance map (*source*: [39])

3.2.6 Solar power plant design

For this thesis standard multicrystalline p-type solar cells with a front glass, aluminum alloy frame and plastic rear, which represent majority of the market, are selected. Module has a peak power of 260W with 3% acceptable deviation, dimensions are 1640x992x40 mm (LxWxH) and it has 16% efficiency. Module consists of 60 cells, which are split into 6 strings, and each cell has the dimensions of 156x156 mm. Modules have the efficiency warranty of 25 years that solar module will remain at least 80% of its initial efficiency.

For analysis another high durability premium multicrystalline p-type solar cell, encapsulated in glass from both sides, is selected. The frameless module has a peak power of 260W and is a lot thinner: 1645x986x7.1 (LxWxH). Module has the same number of cells, but surprisingly long warranty of 30 year for 90% of initial efficiency. These solar cells are produced in Lithuania by the company called "Soli Tek". Additionally, company has performed 50-year module test simulations for the PRO module and results showed only 6% degradation. Warranty chart is shown in Figure 19.

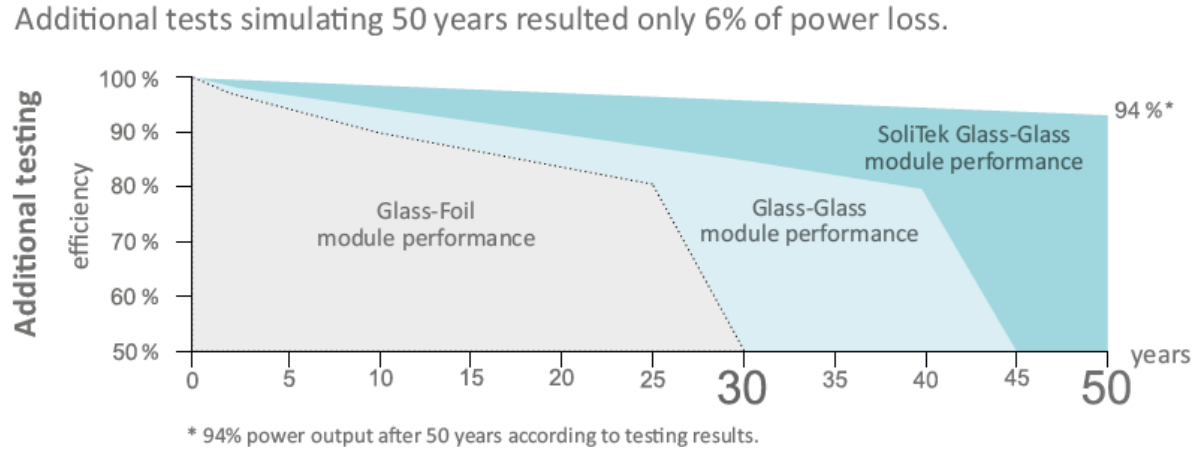


Figure 19. Glass-glass module testing (*source*: [40])

Inverter, which is the weakest part of solar system, has a standard warranty of 5 years, but normally it is operational at least 10-15 years. Simulation lifetime cycle is set to 30 years, so one-time replacement will be included in the calculations. Solar power plants have low to no maintenance; therefore, one time average salary cost is included in the project to cover modules cleaning, wire fixing etc. Solar power plant project, required materials and quantities are shown in the table 1.

Table 1. 5kW solar power plant project

Materials	**Unit price**	**Quantity**	**Total**
PV module SoliTek Standard P60 - 260	150 €	19	2 850 €
Inverter Fronius SYMO 4.5-3-S WLAN WEB three-phase 1MPPT	1 302 €	1	1 302 €
Tile roof mounting system	40 €	19	760 €
Cable 1,0 kV Cu 1x4mm2, MC4 joint	0.8 €	100	80 €
Fronius Smart Meter 50kA-3	239 €	1	239 €
Installation costs			
Installation of the PV system: mounting systems, inverters, modules, cables, monitoring	150 €	5	750 €
Transportation, additional materials	200 €	1	200 €
Documentation costs			
Technical project	400 €	1	400 €
Comissioning of PV plant	200 €	1	200 €
Preparation of documentation	50 €	1	50 €
Total taxes excluded			**6 831 €**
VAT 21%			**1 435 €**
Total			**8 266 €**

The project price with high performance solar cells is 8 955€ with VAT. Soli Tek glass-glass modules are roughly 20% more expensive, at the price of 0.69€/Wp, while standard solar modules is priced at 0.58€/Wp. The main advantage of the glass-glass module is the low degradation rate and long warranty of 30 years and 90% performance. Additionally, module price may vary significantly when installing higher capacity solar power plant and buying more at the reduced price. According to the module trader company "PvXchange", mainstream price for solar module is roughly 0.46€/Wp and is gradually decreasing [41].

Average wage has a direct influence on system total price. The system needs to be mounted, documentation prepared and human hours involved. Assumption is made that parts, which require human involvement are proportional to the average salary after the tax. Electricity price in big countries may vary, but average value was taken according to the 2016 data.

3.2.7 Solar power plant components

In this section project components are explained in detail.

Standard PV module – is the main power plant component, which generates DC current. Standard module has aluminum frame, transparent glass in the front and plastic in the rear. Standard dimensions are 1 m width and 1.6 m length. The standard PV module is shown in Figure 20.

Figure 20. Standard PV module (*source*: "Soli Tek" data sheet)

Glass-glass PV module – essentially it is the same module, but encapsulated into the glass from both sides and has no frame. These modules have higher estimated lifetime and lower performance degradation. Glass-glass PV module is shown in Figure 21.

Figure 21. Glass-glass PV module (*source*: "Soli Tek" data sheet)

Inverter – is another important component in solar power plant. It transforms in solar modules produced DC electricity into AC. At standard conditions, inverters have high conversion efficiency of at least 97%. Converted AC electricity is then used by household or is supplied to the grid. Inverters and modules are connected in strings or in other words – PV modules connected in series. Inverter can have different number of strings, which is in parallel connection with each other. Fronius 4.5-3 S inverter operating voltage is in the range of 300-800 V, which means that dividing the number by 38V – the module open circuit voltage, we get the number of modules that could be connected to one string. In this case the range is 7- 21 modules in one string. Number 3 in inverter name means three-phase inverter and letter S- single maximum power point tracking (MPPT). If inverter with multiple MPPT tracking is used, it allows to connect different amount of PV modules without influencing the output. In example, if single MPPT is used and one string of modules are shaded, it will affect the performance of the rest. Inverter is shown in Figure 22.

Figure 22. Fronius DC to AC inverter (*source*: "Fronius" data sheet)

Mounting system – can be separated into three groups: flat roof, roof with the slope and ground mount (note: some modules can be integrated into the roof, but they are not discussed). The flat roof mount can be used in roofs, where slope does not exceed 5°. Modules are placed into free standing module holders and ballast bricks make sure to hold the system in place against the wind and snow loads. In slope roof, rails are bolted into the roof and specials clamps are used to hold the modules. In ground mount system, massive holders, which are embodied

into the ground with concrete, are used to hold module arrays. Modules placed on the roof do not occupy useful space, however, sometimes it is difficult to orient the modules perfectly to the South direction. Flat roof and roof with the slope mounting system is shown in Figure 23.

Figure 23. Flat roof and slope roof mounting systems (*source*: "Aerocompact" data sheet)

Smart meter – is a device, which allows to monitor solar power plant output using mobile application or dedicated website. Additionally, it shows household electricity consumption and amount of electricity supplied or bought from the grid. "Fronius" solar web application for monitoring solar power plant performance is shown in Figure 24.

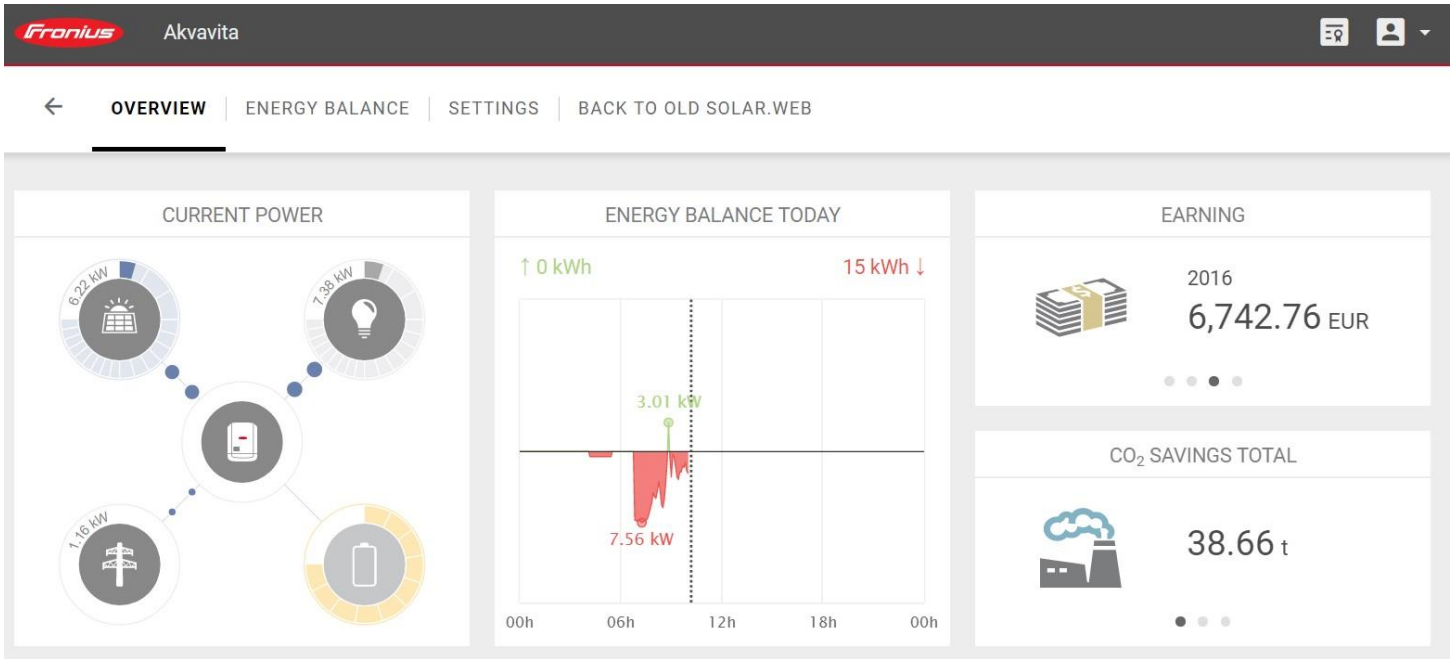


Figure 24. Solar power plant monitoring interface (*source*: "Fronius" solar web)

3.3 Results

3.3.1 Grain boundaries

Four different positions from the standard industrial ingot IC1 are investigated. Each position has three sub-positions, which describes the preparation of the wafer. The lowest number of the group – ungettered or as-cut, middle – gettered, the highest – gettered and hydrogenated. Lower value means that wafer is located closer to the bottom. Position A1 consists of wafers 8-10 with dimensions: 10x10 mm, A2: 38-40 with dimensions: 15x15 mm A3: 68-70 with dimensions: 15x15 mm and A5: 128-130 with dimensions: 25x20 mm. Different dimension size was selected due to the growth of crystal size within the ingot. Additionally, A4 and A6 wafers were produced, but at the time of sample preparation, were not available, therefore, not investigated.

At each step of the investigation, wafers were compared between themselves – to determine how industrial processes affect the structure within the wafer and positions in the ingot. For grain boundary (GB) analysis CSL Σ3, Σ9, Σ27 and random grain boundaries with misorientation angles between 15-180° were selected. Even though low misorientation angle GBs are important to solar cell performance, they cannot be recorded, since higher resolution and smaller step size is needed, which significantly would increase the scan time.

A2 wafer position for wafers 68, 69 and 70 were selected to illustrate the results. All EBSD GB maps are presented in the appendix 2. The results are shown in the figures 25-27 (scale line 5 mm). Color indication according to the effect for lifetime: green – sigma 3, yellow – sigma 9, red – sigma 27, black – random grain boundaries for 15-180 angles.

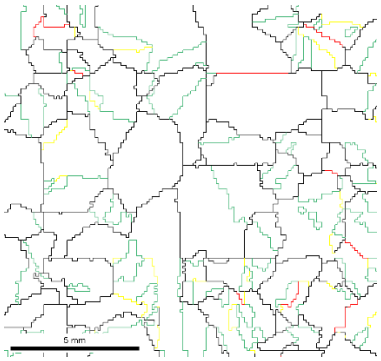


Figure 25. U IC1-68

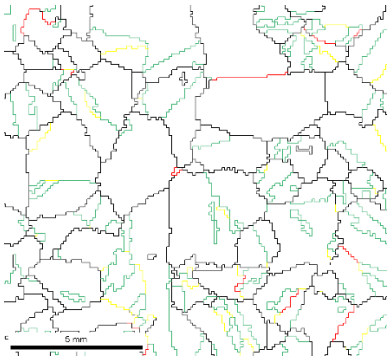


Figure 26. G IC1-69

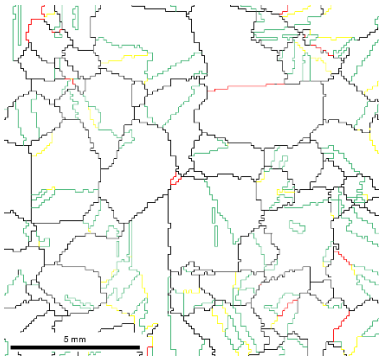


Figure 27. G+H IC1-70

From the results, it is clear, that no change, which might affect the grain boundaries structure during the wafer processing, appear. Additionally, this tendency seems to be true to

all the sub-positions at the same wafer group. However, moving from the bottom to the top of the ingot, the share of random GB slightly decreases while Σ3 increases. Other GB numbers seems to stay stable. For Mc-Si lifetime the most harmful are Σ27 and random angle GB, so lower percentage of these GBs, means higher expected wafer lifetime. The share of GB is shown in the table 2.

Table 2. Wafer grain boundary results

Wafer position	Random angle GB	Σ3	Σ9	Σ27
8	77.5%	18.1%	3.4%	1.0%
9	77.5%	18.7%	2.9%	0.9%
10	78.1%	18.7%	2.8%	0.4%
39	69.1%	25.6%	3.5%	1.8%
40	68.3%	26.7%	3.2%	1.9%
68	68.7%	24.5%	4.4%	2.5%
69	67.1%	26.1%	4.3%	2.5%
70	67.2%	25.7%	5.0%	2.2%
128	68.1%	23.9%	4.2%	3.8%
129	68.0%	24.5%	4.1%	3.4%
130	68.1%	24.6%	3.9%	3.5%

3.3.2 Dislocation density

Dislocation density was measured using PV Scan 6000. Dislocation density results are obtained in the range of 10^4 – 10^6, where lower signal corresponds to the lower value of dislocations. Additionally, values higher than 10^6 were treated as noise, which might have occurred during the sample preparation. In dislocation density maps 1 tick corresponds to 0.2 mm or resolution of 200 µm. Some samples were not polished perfectly due to the holder roughness or other limitations. A3 position wafers are shown in figures 28-30 (color corresponds to the dislocation density intensity).

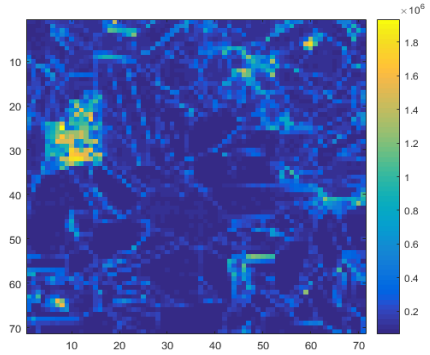


Figure 28. U IC1-68

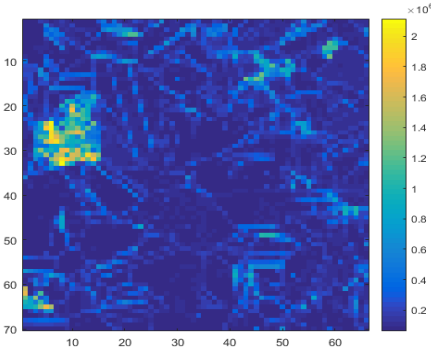


Figure 29. G IC1-69

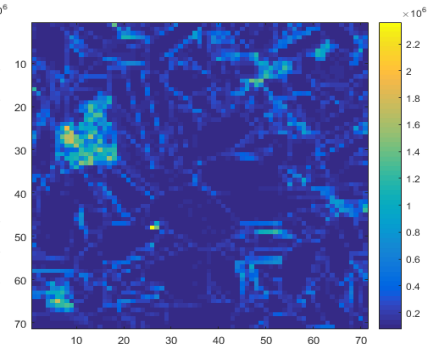


Figure 30. G+H IC1-70

Dislocation clusters can be characterized by position in the wafer: cluster inside the grain (1), cluster inside the twinned grain (2) and cluster inside the multiple grains (3) [42].

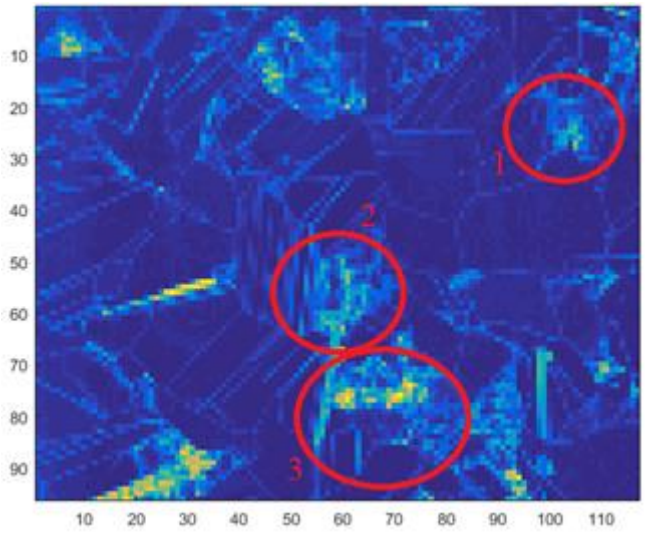


Figure 31. Dislocation density IC1-128

Dislocation density for the range of $10^4 – 10^6$ is shown in Figure 31. Interval $10^5 – 10^6$ corresponds to the highest share of dislocation, therefore, it was split into 5 sub intervals for closer examination. Results are shown in table 3.

Table 3. Dislocation density measurement results

Wafer position	**$5*10^4 – 7.5*10^4$**	**$7.5*10^4 – 1*10^5$**	**$1*10^5 – 2*10^5$**	**$2*10^5 – 4*10^5$**	**$4*10^5 – 6*10^5$**	**$6*10^5 – 8*10^5$**	**$8*10^5 – 1*10^6$**	**$>1*10^6$**
8 U	0.0%	0.0%	2.6%	22.6%	34.1%	24.3%	10.7%	5.7%
10 G+H	0.0%	2.1%	27.3%	26.3%	7.5%	3.3%	1.5%	32.1%
39 G	0.0%	0.1%	18.7%	45.3%	22.0%	7.5%	2.3%	4.1%
40 G+H	0.0%	0.2%	16.8%	33.8%	17.9%	10.6%	5.2%	15.4%
68 U	3.5%	39.0%	30.5%	17.5%	4.2%	2.3%	1.1%	2.0%
69 G	1.6%	45.3%	28.2%	15.2%	4.4%	2.0%	1.2%	2.1%
70 G+H	0.0%	29.1%	44.9%	16.1%	4.9%	2.1%	1.2%	1.8%
128	0.0%	19.8%	53.2%	16.6%	4.8%	2.0%	1.2%	2.3%
129	9.8%	38.4%	31.4%	12.8%	3.2%	2.1%	0.9%	1.5%
130	0.6%	37.1%	40.6%	13.7%	3.2%	1.8%	1.1%	1.9%

During selective etching procedure, wafer 9 and 38 broke down and are not included in the comparison. From the results, it is visible that gettering has a positive effect on dislocation density. After hydrogenation, dislocation density increases again, but the value is still higher compared with the value of ungettered. However, change happens in the small densities and according to the literature, there should be no difference after gettering and hydrogenation

procedures at all. For wafers 8, 10, 39 and 40 significant amount of data falls in the region of $>10^6$, therefore, data is not reliable due to insufficient sample preparation. Additionally, for visual comparison, well prepared results are shown in Figure 32.

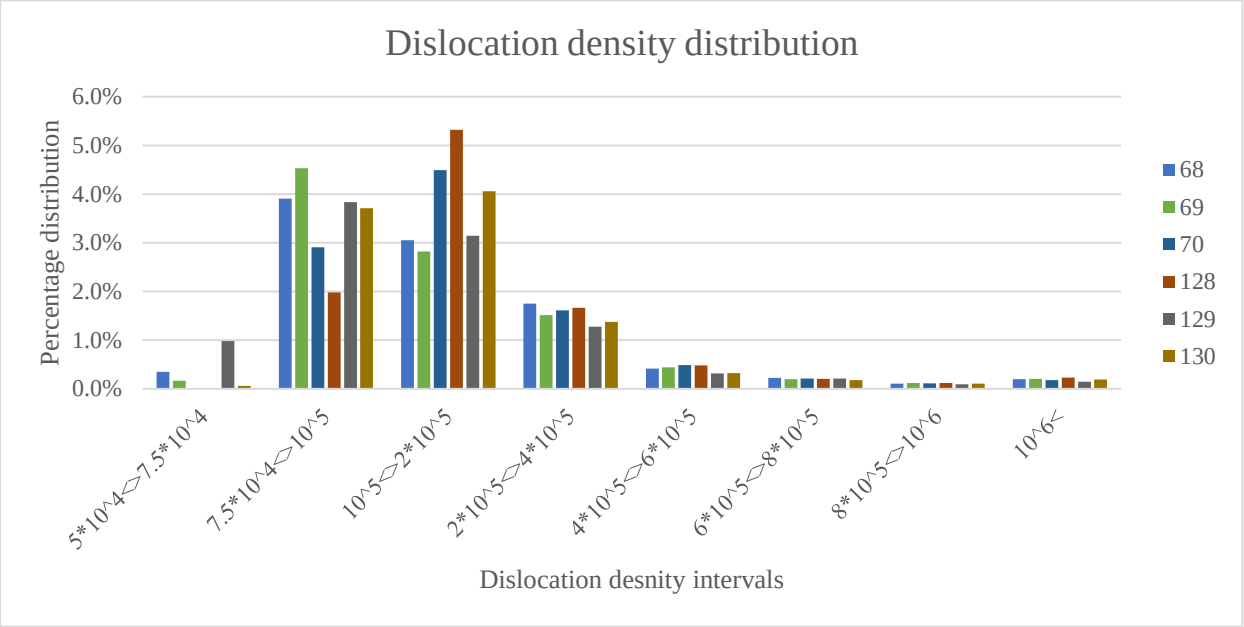


Figure 32. Dislocation density distribution

3.3.3 Lifetime analysis

Raw lifetime data was prepared in Oslo by IFE research institute. In high purity quartz crucible ingot, which was divided into two parts: high performance in the left and quasi-mono in the right, was grown. During lifetime measurements, the resolution of 160 µm was used, but due to non-homogenous structure, the focus was not sharp and it affected image quality. The original wafer lifetime analysis is shown in the Figure 33. HP part is quite inhomogeneous, where the highest lifetime is in the middle of the wafer.

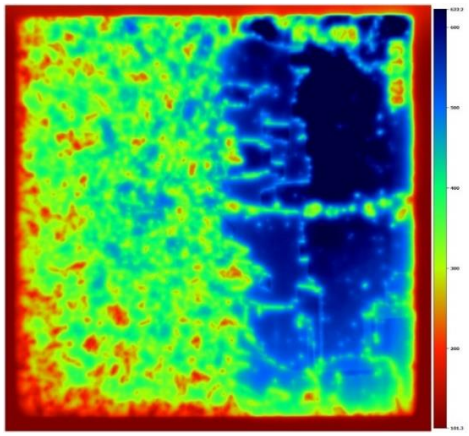


Figure 33. High performance and quasi-mono wafer lifetime

From the lifetime analysis data, areas of selected wafers were calculated and figures plotted. GB maps were fitted on top of the lifetime figures in order to distinguish GB effect on lifetime. Additionally, dislocation density maps are shown for the same reason. Unfortunately, dislocation density scans failed to A1 and A2 wafers due to insufficient sample preparation and wafers IC1-38 and IC1-68 lifetime data was unreadable. Lifetime data, GB and dislocation density maps are shown in figures 34-36.

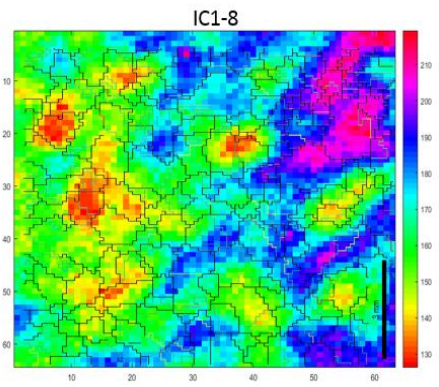


Figure 34. As-cut

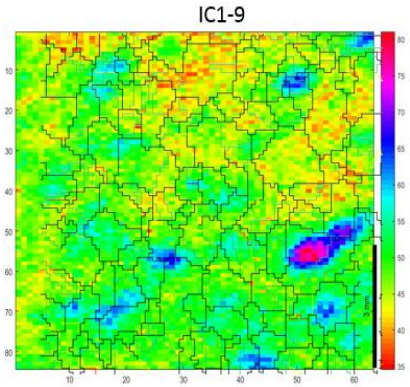


Figure 35. Gettered

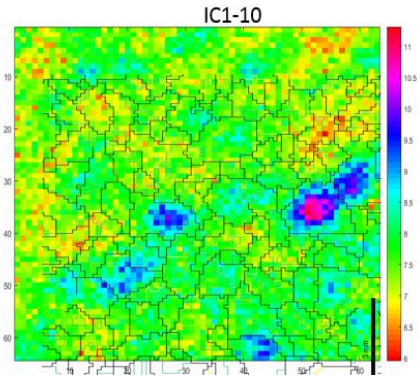


Figure 36. G+H

For A1 wafers lifetime, the resolution of the lens seems to be chosen too low and features are not sharp. Additionally, the comparison between A1 wafers and internal quantum efficiency image prepared by Krzysztof Adamczyk is not possible due to the same reason mentioned above and the fact that small grains change a lot even with the step of few wafers of the ingot. A2 wafer lifetime and adjusted GB maps on top to determine GB influence are shown in figures 37-38.

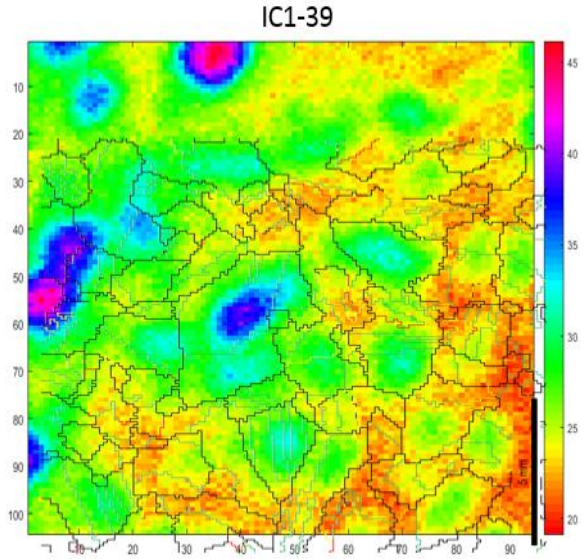


Figure 37. Gettered

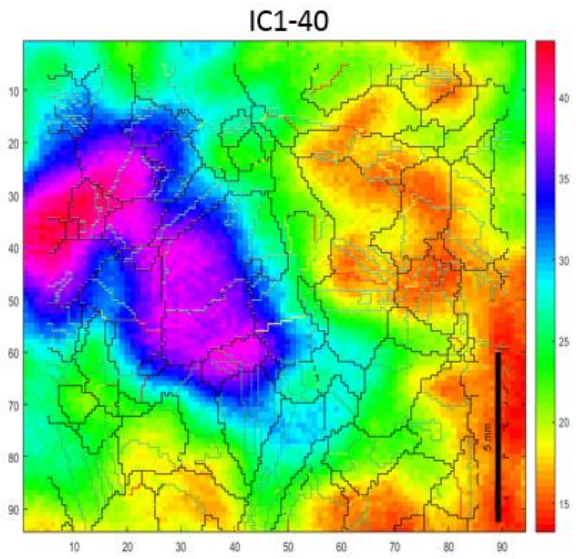


Figure 38. Gettered+Hydrogenated

For A2 wafer lifetime, position 38 failed to present any readable data. The effect of GB on lifetime after gettering is visible and it disappears after hydrogenation. Dislocation density scan failed at A2 wafers due to insufficient preparation. A3 wafer lifetime, adjusted GB maps on top to determine GB influence and dislocation density are shown in figures 39-41.

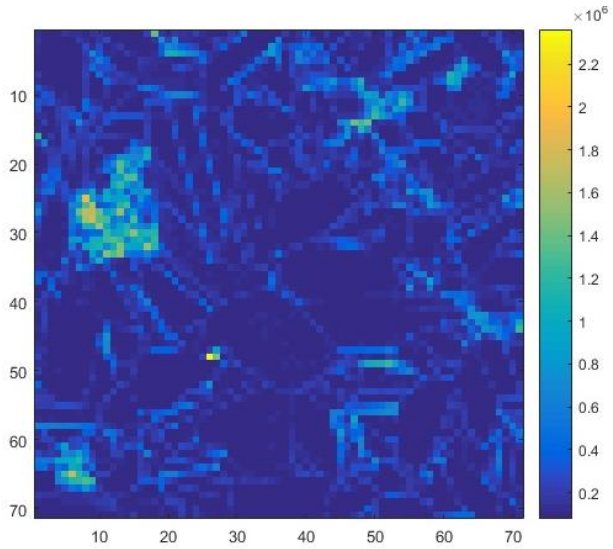
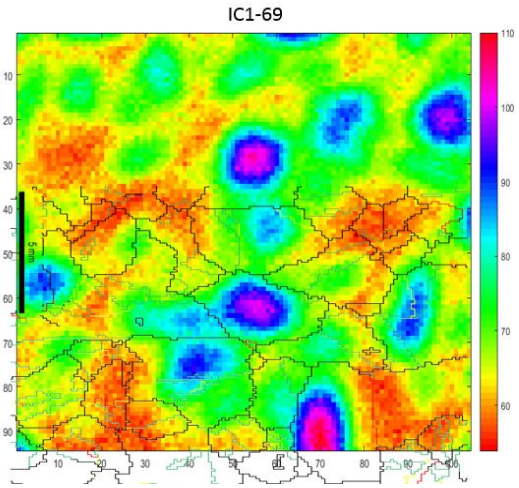


Figure 39. Dislocation density IC1-40



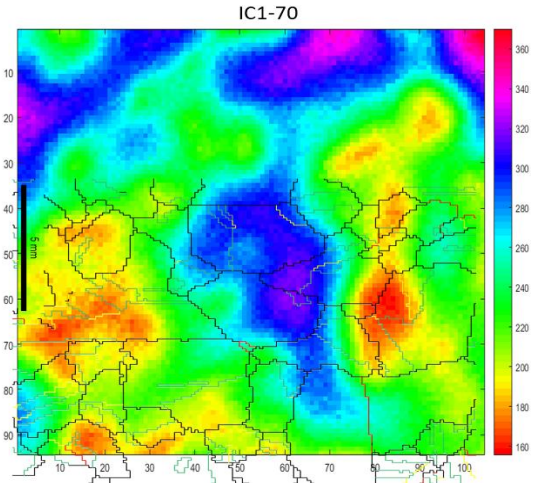
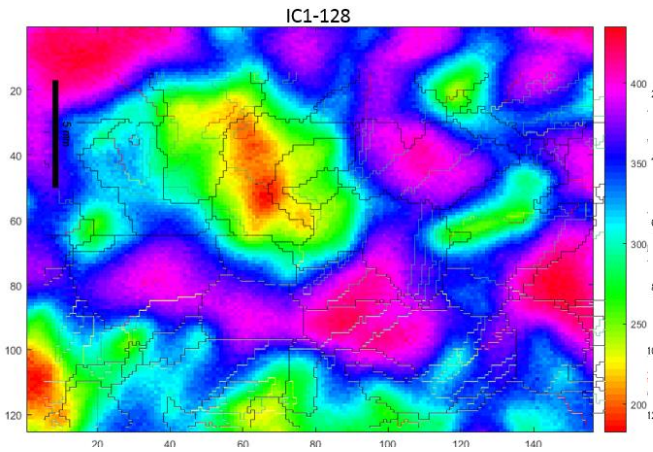


Figure 40. Gettered

Figure 41. Gettered+Hydrogenated

For A3 wafer lifetime, position 68 ungettered wafer again failed to present any readable data. The effect of GB on lifetime after gettering is visible and it disappears after hydrogenation. Industrial processes do not influence dislocation density. A5 wafer lifetime, adjusted GB maps on top to determine GB influence and dislocation density are shown in figures 42-45.



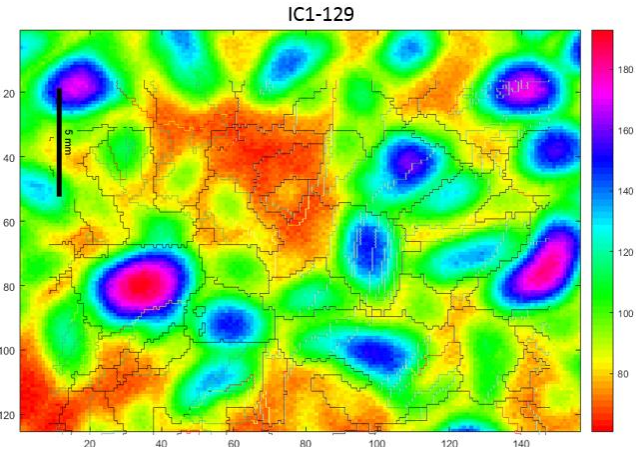
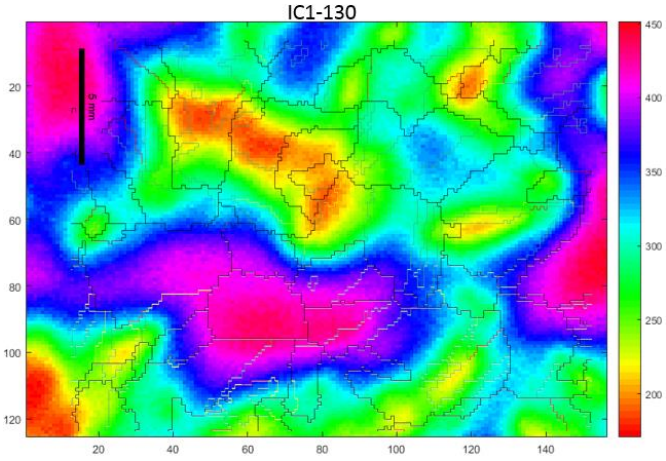


Figure 42. As-cut

Figure 43. Gettered



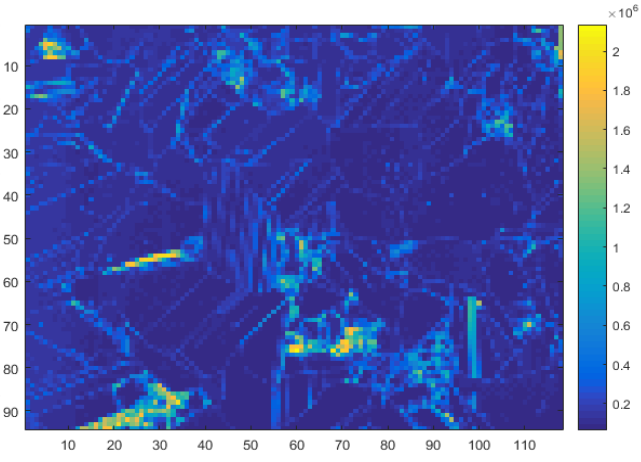


Figure 44. Gettered+Hydrogenated

Figure 45. Dislocation density IC1-128

Ungettered wafer IC1-128 lifetime is a lot higher than expected. For middle ingot position, literature [43] suggests that ungettered wafer lifetime should be the lowest compared to gettered and gettered + hydrogenated. However, the measured values in A5 wafer are similar with C.C. You work on "Effect of Phosphorus Diffusion Gettering and Firing on the Minority Carrier Lifetime in Hybrid Si Wafers". Dislocation density and GB effect on lifetime are the most present for gettered wafers. The results of average lifetime analysis are presented in the Figure 46.

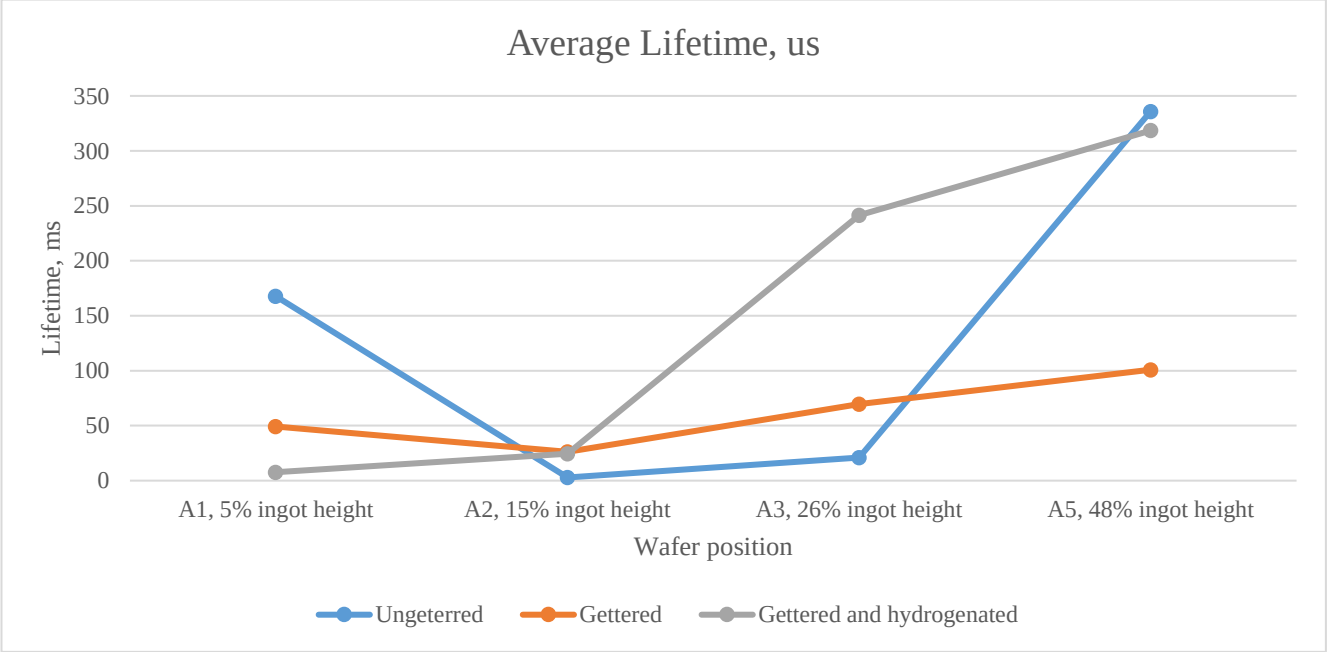


Figure 46. Average lifetime of analyzed wafers

The lifetime of the bottom wafer A1 falls after the industrial processes. It is the expected, since bottom part contains higher amount of impurities compared to middle. A2 and A3 ungettered wafer results were not reliable, therefore, as no was possibility to repeat the measurements, previous results from C.C You work "Impurity control report IC1" were used instead. Minority carrier lifetime is shown in the table 4.

Table 4. Lifetime results

Wafer position	A1, 5% ingot height		A2, 15% ingot height		A3, 26% ingot height		A5, 48% ingot height	
Wafer treatment	Lifetime, µs	STD	Lifetime, µs	STD	Lifetime, µs	STD	Lifetime, µs	STD
Ungeterred	167.9	18.2	2.9*	0.6	21.1*	0.4	335.9	**53.0**
Gettered	48.5	5.3	26.2	3.8	69.6	9.3	100.9	**24.5**
Gettered and hydrogenated	7.7	0.6	24.6	7.3	241.4	**40.6**	318.5	**63.7**

3.3.4 Solar power plant simulation results

Power plant project data was prepared with the collaboration with the solar entrepreneur company "Saulės grąža ". Simulations were performed according to the synthetic weather data related to the city. System price for Lithuania was taken as a starting point and adjusted accordingly for other countries. 5kW system was taken since it covers a small household annual electricity demand. Modules are oriented to the south with the inclination of 30 degrees. The optimal angle for different country may vary slightly. In the Figure 47 is shown the mounting system and mounted modules.

Figure 47. Standard example of 5kW solar module system (*source:* "Saulės grąža" archive)

It is assumed that all the excess electricity is kept in the grid and used later with no additional cost (currently in Lithuania the excess electricity safe-keeping for later use is taxed at 3.5 euro ct/kWh). The project price of 5kW solar power plant is shown in table 5.

Table 5. Summary of solar power plant viability analysis

Country	Average salary after tax **[44]**	Average electricity price, € ct/kWh **[45]**	VAT	5kW modules STANDARD	5kW modules PRO	Annual electricity generation, kWh	Specific production kWh/kWp/year	Maintenance, €	Annual savings, €
Lithuania, Vilnius	630 €	13.0	21%	8 266 €	8 955 €	4 570	925	64 €	530 €
Norway, Oslo	2 883 €	15.2	25%	15 691 €	16 404 €	4 616	934	140 €	562 €
Germany	2 173 €	30.0	19%	12 792 €	13 470 €	5 841	1 182	116 €	1 636 €
Greece, Athens	723 €	18.0	23%	8 693 €	9 394 €	8 077	1 635	68 €	1 386 €
USA, California	2 746 €	15.4	8%	13 181 €	13 797 €	8 323	1 685	135 €	1 148 €
China, Bejiing	816 €	8.4	17%	8 545 €	9 212 €	6 712	1 359	71 €	490 €
India, Delhi	493 €	7.2	14%	7 358 €	8 005 €	8 740	1 769	60 €	571 €
United Arab Emirates, Dubai	3 000 €	5.1	0%	12 850 €	13 420 €	8 243	1 669	143 €	275 €

The biggest system price is expected to be in Norway in both cases. This is mainly due to the high average income and VAT. The highest average salary is recorded in UAE, but currently no VAT is implemented (UAE government has plans on implementing it in the future). In most of the countries there are subsidies for renewable energy development, but as mentioned before, the aim is to compare todays renewable competitiveness and estimate the payback time.

Using PVsyst simulation software, the prognosis of solar power plant yearly production is obtained. The margin of error for the production is not supplied, but it is stated in the program, that the result is the average year of the long-time data analysis.

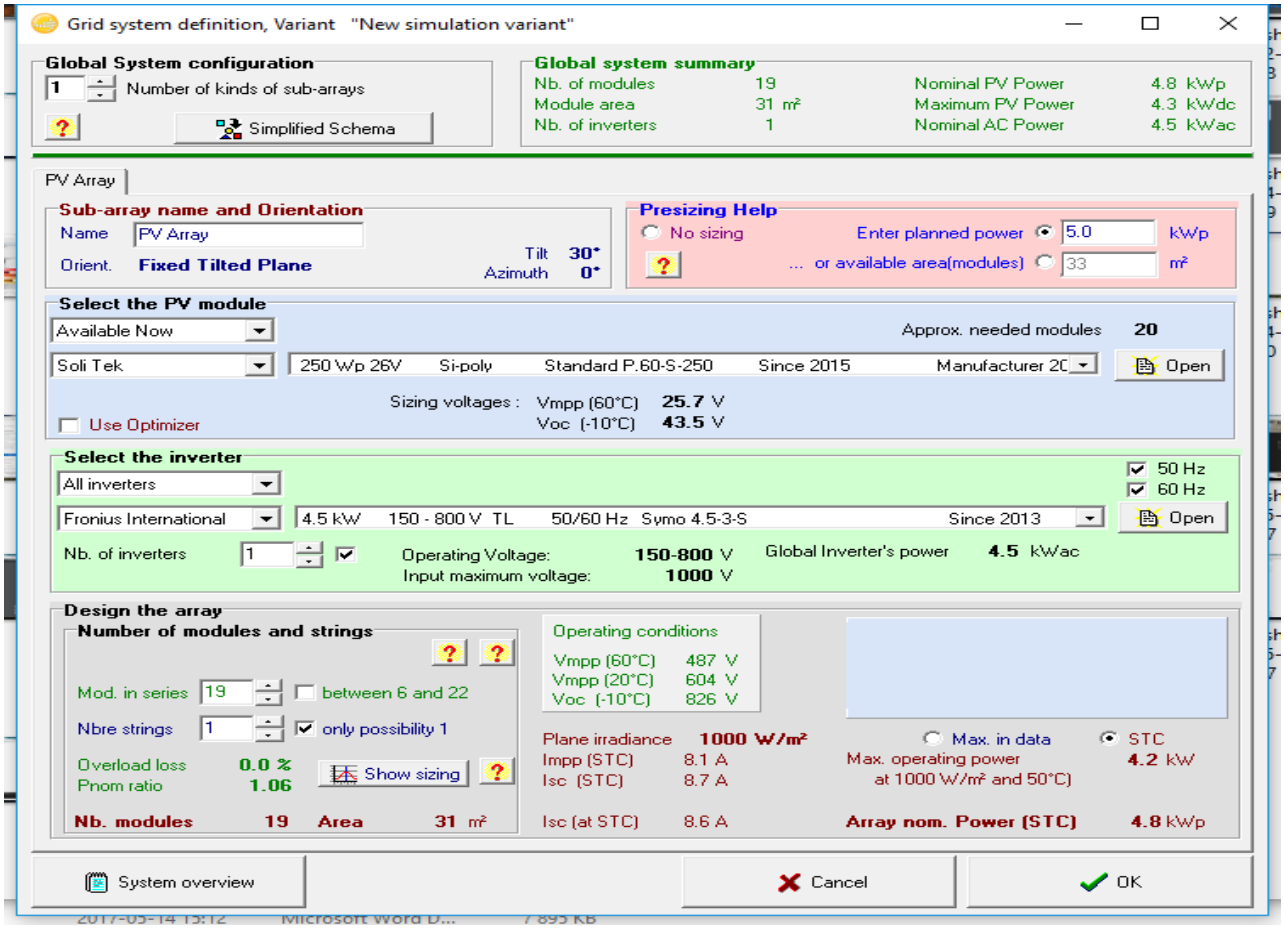


Figure 48. PVsyst design tool for solar power plants

The results show that investigated countries can be divided into two groups: with low solar irradiance – Lithuania, Norway, Germany, China and high solar irradiance – Greece, USA, India, UAE. It is expected that solar system in Lithuania will produce more electricity than in Norway, however, the difference is small even in Norway's favor and might have occurred due to Oslo position close to water, which contributes to higher reflectance. For low

irradiance countries, specific production varies 925-1359 kWh/kWp/year and China has the highest value here.

For high irradiance countries 1635-1769 kWh/kWp/year, India is the leader while USA, UAE and Greece production has close to no difference. The obtained results show the difference of 190% between the lowest and highest countries of solar electricity production. The graphs 42-43 show the annual production in low and high irradiance countries.

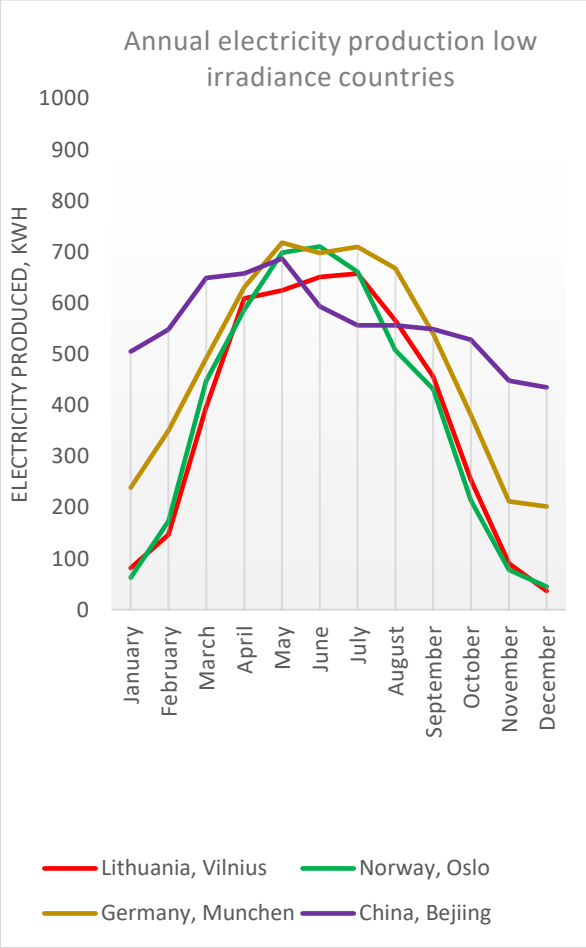


Figure 49. Low irradiance country output

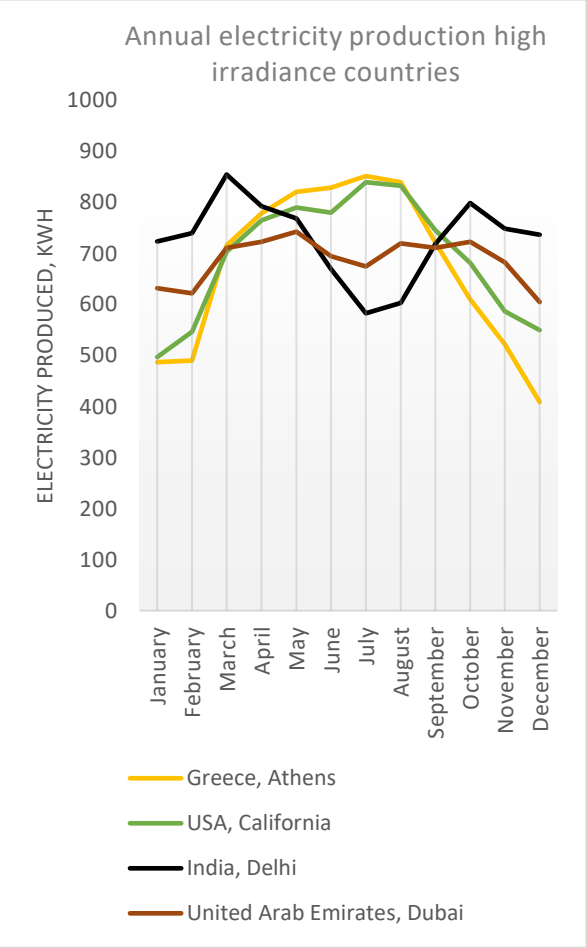


Figure 50. High irradiance country output

In low irradiance graph the clear seasonality for Norway, Lithuania and Germany is visible, while China has a quite constant electricity production throughout the year. This feature can play an important role when designing the optimal share of solar in the countries energy mix, since more stable power source – less connections and energy storage is needed.

In high irradiance country graph, clear seasonality is visible in Greece and USA. In India two peaks are observed – in March and October and during the summer it has the lowest

output. UAE has the most stable conditions of all – the production varies only slightly during all the seasons. The detailed production is shown in the table 6.

Table 6. Summary of monthly output generation

Month/Country	Lithuania, Vilnius	Norway, Oslo	Germany, Munchen	Greece, Athens	USA, California	China, Bejiing	India, Delhi	United Arab Emirates, Dubai
January	82	63	239	487	497	505	724	632
February	147	173	350	490	547	548	740	622
March	397	448	492	716	704	649	855	711
April	609	587	631	779	765	658	793	723
May	625	698	718	821	790	687	769	743
June	651	711	698	829	780	593	670	695
July	658	661	710	852	840	556	583	675
August	565	507	668	840	833	556	603	720
September	456	432	540	722	746	549	719	711
October	254	214	381	610	682	528	799	723
November	91	78	212	522	587	448	749	683
December	37	45	202	409	550	435	737	605
Total, kWh	**4 570**	**4 616**	**5 841**	**8 077**	**8 321**	**6 712**	**8 741**	**8 243**

In Lithuania and Norway there is a significant difference in a production between winter and summer. In the four-month period from November to February, it is produced the same amount of electricity as in one month in the summer. In Germany and Greece, the difference is less obvious – varying from 2 to 3 times for any summer month to winter month. In USA and China, the difference is around 50% and India and UAE has almost stable output throughout the year.

When Mc-Si solar modules installation started to increase exponentially in the beginning of the century, the average life time was expected to be around 20 years. However, time has passed and results show that the real-lifetime might be well above 30 years. Many companies provide warranty of at least 25 years and some go even beyond that. In analysis 30 years were taken as a life cycle. One time inverter change and minor maintenance fee equal to one average salary is applied to the calculations. Standard solar cell degradation is assumed to be 0.5%, when maximum value could be up to 0.7%. After 30 years of operation, modules would retain 86.47% their original efficiency. This might not be true to all the locations, since light induced degradation is expected to be stronger in the countries with higher overall irradiance. The glass-glass Pro model degradation is set to 0.1%. It has the warranty of 30 years for 90% of its initial performance. The module will retain 97% of its initial efficiency. Return

of investment is calculated at the constant electricity price and more real scenario with the 2.5% annual increment. The results are shown in the table 7.

Table 7. Summary of payback time

Country	5kW modules type	**Payback time, years**	NPV after 30 years	**Payback time, +2.5% annual electricity growth, years**	NPV after 30 years
Lithuania, Vilnius	STANDARD	**16.2**	6 525 €	**13.5**	13 857 €
	PRO	**16.9**	6 708 €	**14.2**	14 774 €
Norway, Oslo	STANDARD	**29.9**	5 €	**21.6**	8 532 €
	PRO	**29.4**	218 €	**21.4**	9 717 €
Germany	STANDARD	**8.0**	32 903 €	**7.3**	54 681 €
	PRO	**8.3**	34 918 €	**7.5**	58 741 €
Greece, Athens	STANDARD	**6.3**	30 019 €	**6**	48 147 €
	PRO	**6.8**	31 600 €	**6.3**	51 377 €
USA, California	STANDARD	**11.8**	18 888 €	**10.3**	34 734 €
	PRO	**12.0**	20 162 €	**10.6**	37 589 €
China, Bejiing	STANDARD	**18.0**	5 136 €	**15**	12 033 €
	PRO	**19.0**	5 275 €	**15.6**	12 882 €
India, Delhi	STANDARD	**13.6**	8 583 €	**11.5**	16 385 €
	PRO	**14.1**	8 876 €	**12.1**	17 443 €
United Arab Emirates, Dubai	STANDARD	**53.0**	-5 162 €	**29.5**	-198 €
	PRO	**50.0**	-5 278 €	**30.4**	365 €

Project with the payback time of around 10 years is expected to be attractive choice for the investors. The lowest payback time is reported in Greece, which is 6.3 years and 6 years with the electricity price growth. Few years longer payback time is expected to be in Germany. These two countries are the best place for PV installation from the list of countries under consideration. The main factors in Greece: high irradiance, medium income and quite high electricity price and in Germany: very high electricity price, medium irradiance.

USA California has average payback time, which is quite reasonable value for a long-time investment. Additionally, decreasing price of PV modules and components will make investment even more attractive. Lithuania, China and India are little bit below the traction line. Payback time is quite low varying from 13.6 years to 19 years in standard case. In electricity sensitivity analysis, payback time in India improved to 11.5 years, which is quite reasonable.

Norway due to low irradiance, very high average income and average electricity price is not a promising place for PV development. Only increasing electricity prices, lower PV

project price may improve the situation. However, Norway produces around 90% of its electricity from cheap hydro power plants, therefore, there is not much place for other renewable sources.

Unexpectedly, UAE has a payback time of 50 years due to very low electricity price. After the electricity sensitivity analysis, the payback time improved to 30 years, but it is still the number that will not attract investors. However, the government of UAE understands the importance of sustainable future and have plans to produce 75% electricity from renewable energy source until 2050. The largest ever 800 MW solar power plant is being and will be fully operational in few years [46].

4. Discussion

Grain boundaries and dislocations are the key differences between multicrystalline and monocrystalline silicon solar cells. Existence of these features negatively affect solar cell lifetime. Current research focuses on producing controlled grain size so called high performance solar cells. On one hand, smaller grains form more grain boundaries, where impurities tend to segregate during the growth and increase recombination activity. On the other hand, smaller grain size means lower dislocation density, since the propagation of dislocations are stopped by GB. Additionally, theory states that grain size depends on the position in the ingot. In the beginning of solidification, grains do not have a lot of time to form; therefore, size is small and it increases towards the ingot top.

By limiting the size of the grains, we increase the number of GBs. Random angle grain boundaries play an important role in solar cell performance, since it is the most recombination active GB. In the bottom of the wafer, RAG percentage is the highest of 78% and the share of 68% RAG is stabile in A2, A3 and A5 wafers. This happens mainly due to the smaller grain size in the bottom. CSL indexes Σ3, Σ9, which are the least harmful to the lifetime of the solar cell, are constant throughout the ingot and Σ27 even slightly increases in the A5 wafer. However, increment is too small to draw any conclusions. According to the previous studies of multicrystalline silicon, Σ3 value is between 22% and 64%, Σ9 – between 9% and 12%, and Σ27 – between 3% and 9% of total grain boundaries [26-28]. During the experiments values for Σ3 were obtained in the range of 18-26%, Σ9: 3-5% and Σ27: 1-4%.

From the GB maps, it is visible that solar cell fabrication processes do not influence grain structure due comparingly low up to 1000 °C temperatures, and short exposure time.

However, gettering is performed in temperatures high enough allowing impurities to diffuse towards the inactive part of solar cell. Additionally, the process dissolves impurities, which decorate GBs and allows them to re-precipitate back to the bulk.

Dislocation density for the silicon wafers normally lies in the interval 10^4 – 10^6 dislocations per cm^2. For A3 and A5 wafers, roughly 90% of dislocations lay in $7.5*10^4$ – $4*10^5$ zone with the average value of $1.9*10^5$. The results show dislocation density improvement after the gettering process. According to the literature [47], dislocation density might be improved by isothermal annealing at temperatures above 1250 °C due to dislocation annihilation. However, gettering is performed at temperatures not exceeding 1000 °C, therefore dislocation density should not be affected. Another thing, which might have had the effect on dislocation density improvement, is dissolution of precipitates and impurities to the inactive emitter layer. This micro movement might have caused dislocation motion and stress release. The precise mechanism is still under the discussion among the researchers.

In standard silicon solar cell, minority carrier lifetime after gettering and hydrogenation improves no matter of the wafer position in the ingot. However, in high performance wafers, the gettering and hydrogenation effect differs. The results show no improvement in the bottom (5% relative height position in the ingot) A1 wafer, in contrast, lifetime even decreases more than 20 times from 167.9µs to 7.7µs (lifetime was calculated according to the selected area). This happens mainly because gettering and hydrogenation processes have low impact in high dislocation and high impurity concentration areas. Therefore, average wafer lifetime is not improved, but re-precipitation defect mechanisms are also created. Additionally, it is worth to mention that ungettered IC8 wafer and gettered IC9 wafer have quite high noise level in the sample and due to low resolution, GB were not clearly visible. Furthermore, A1 wafer results contradict with previous studies stating that IC8 and IC9 wafer lifetime should be around 8µs. Overall, IC8 and IC9 wafer lifetime should be measured again to obtain precise results (during the time of writing is was not possible, since lifetime analysis were performed in Oslo and wafers have been further analyzed).

In wafer A2 (15% relative height position) average lifetime is expected to be higher than in wafer A1. However, it decreases from 167.9µs to 2.9µs in ungettered and from 48.5µs to 26.2µs in gettered wafer. It could be explained by the high noise level in wafers IC8 and IC9. Wafer A2 shows overall lifetime improvement from 2.9µs to 24.6µs. Gettering and hydrogenation processes are more efficient since A2 position has lower amount of diffused

impurities from the crucible and surroundings. However, in A2 wafer hydrogenation seems to have low to no effect, since a lot of dislocation clusters are present in the selected area.

In wafer A3 (26% relative height position) lifetime is expected to increase. It is true for all A3 wafers and lifetime increases from 21.1µs to 241.4µs. Hydrogenated wafer has the most uneven lifetime distribution, because areas with high dislocation density are not improved by much, while hydrogenation improves intra-grain areas the most.

In wafer A5 (50% relative height position) average lifetime is the highest. The selected area shows high deviation values even in the ungettered wafer. The fall of lifetime after gettering is interesting. In the middle of the ingot the lowest amount of impurities is present, therefore, industrial processes are not so efficient.

Standard 5kW solar power plant will produce from 4570kWh to 8741kWh depending on the site installed. The lowest value was expected to be in Oslo due to geographical position, but in Vilnius – the production was even lower. In Norway, Lithuania and Germany a big variance in seasons is observed. Varying output between the seasons might become a major obstacle, if deciding to install or not the solar power plant. In grid-connected case, seasonality affects only monthly amount of money saved, but in off-grid – additional conventional power source might be needed as well as higher capacity batteries. In Greece, China, USA, UAE and India production output is stable throughout the year. The most stable output is expected to be in UAE with impressive 18% difference between the lowest and the highest monthly value.

Standard module price is 0.58€/Wp, while glass-glass – 0.69€/Wp. Module costs depends a lot on project size, where price may drop more than 40% for bigger projects. However, glass-glass modules are mostly chosen by private house owners, because it offers longer warranty and better overall performance. Standard modules are chosen for bigger projects, since investment is lower and payback time is faster, even though total net present value (NPV) after 30 years is still lower. Additionally, module price is constantly decreasing, while solar cell efficiency is increasing too. Recently, “Soli Tek” standard multicrystalline solar modules were upgraded from 260W to 270W, which translates to the efficiency increase from 16.0% to 16.6%.

Standard and glass-glass modules have the same solar cell specifications, but production technique differs. Standard solar cell has aluminum frame and plastic back, which is much more likely to deteriorate over time compared to solar cell encapsulated in the glass.

According to the simulation results, standard modules have faster payback time, however, NPV after 30 years is lower. Additionally, people who are willing to invest more and want to have reliable, long lasting power source even for 50 years, glass-glass modules are the way to go.

The fastest payback of solar power plant is expected to be in Greece of 6.3 years with NPV of 30 019 € after 30 years. Greece is the perfect place for PV – quite high electricity price, medium average salary and high irradiation through the year. After the sensitivity analysis with 2.5% electricity price increment, payback time shortens to 6 years and NPV increases by 60%. It shows that electricity price in the country is one of the most important factor while considering solar power plant.

According to the simulation results, Germany is in the 2nd place of solar power plant rating of attractiveness. Return of investment is estimated to be in 8 years and NPV 32 903 €. After the sensitivity analysis, NPV is the highest among the countries and even 22% higher than Greece. Germany cannot offer very high irradiance, but extremely high electricity price, opens viability of solar power in the country.

USA, India and Lithuania and China selected cities have moderate 11.8-18.0 years payback time. It means that solar power in these cities still does not have the possibility to become mainstream generation source without the subsidies and mainly are selected due to the environmental reasons. In Norway, solar power is viable in the remote areas, where no electricity grid is available. Furthermore, the system price will increase roughly two times with the inclusion of batteries, but would be still cheaper than to connect remote mountain house to the grid. The biggest surprise was observed in UAE with the surprising 53 years payback time and negative NPV. It shows that solar power for private house owners is unpractical choice for this high irradiance country, but for huge solar projects situation is completely different. UAE has a goal to shift electricity generation to renewables and huge 800MW solar project is already taking place.

Solar power analysis shows availability of solar plants for private house owners without country subsidies and incentives. According to the results only in Greece and Germany solar power can be mainstream power generation source, while USA, California is just outside 10 years payback mark. The situation might be quite different if subsidies are introduced. Additionally, big solar projects will have better results due to the mass of scale.

5. Conclusions

Defects have a high impact on multicrystalline silicon solar cell performance. It increases recombination activity of charge carriers and, thus, decreases efficiency of solar cell. Dislocations are a disturbance in lattice and it influences negatively electrical properties. In general, GBs have neutral effect in pure silicon. However, impurities are unavoidable and the interface between two grains is the easiest place for impurities to diffuse in.

Grain boundaries have very similar structure throughout the ingot: RAGB – 68%, Σ3 – 25%, Σ9 – 4%, Σ27 – 3%, except for the bottom A1 wafers. It has 10% higher count of the most recombination active RAGBs due to small grain size. Additionally, gettering and hydrogenation do not change GB structure – after these processes the share RAGB and Σ3, Σ9, Σ27 remained the same. The increase of RAGB in HP Mc-Si compared to standardly produced is related to grain size limitation. The effect is higher count of RAGBs, but low dislocation propagation due to small crystal size. From the results, it is visible that RAGB are the most active after gettering process. After hydrogenation RAGB effect on wafer lifetime is decreased due to impurity passivation.

Dislocation clusters can be characterized by position in the wafer: cluster inside the grain, cluster inside the twinned grain and cluster inside the multiple grains. A1 and A2 samples were prepared poorly during polishing step and some of them broke down, therefore, there is no possibility to compare how the dislocation cluster propagated throughout the ingot. In wafer A3 and A5 after gettering there seems to be a minor improvement in dislocation density. However, more simulations should be performed on HP Mc-Si wafers to confirm this result.

Lifetime analysis show that wafer lifetime increases while moving from the bottom to the top. Results agrees with the previous research. However, in as-cut IC8 and IC9 gettered wafers, noise was present and grain boundaries were not clearly visible. In the bottom of the ingot, gettering and hydrogenation have the lowest effect, but the middle part, according to the results, has low effect too. Lifetime in the bottom even degrades due to the amount of impurities present, while gettering creates new defect mechanisms due to re-precipitation. Lifetime in the middle part is not improved by much since impurity level is the lowest there.

According to the case study, the most important factor, which influences the decision whenever to invest or not in solar power plant, is electricity price. Low electricity price will lead to the very long payback time and in opposite, high electricity price will make solar

attractive choice even if project is quite expensive and electricity output from solar plant is mediocre. Other important factors to consider are initial investment cost and solar irradiance characteristics in the country.

Simulation show that the best place for investing in solar power plant is Greece. At status-quo (same electricity price for 30 years) payback time is expected to be 6.3 years and with 2.5% electricity price increment, it diminishes to 6.0 years while using standard modules. Other countries worth attention – Germany and USA, California. The payback time is 8.0 and 11.8 years accordingly. For long term analysis, where 30 years of power plant life cycle is evaluated, the most important parameter is net present value. It is worth to mention, that glass-glass modules have even longer expected lifetime, which is over 50 years. The highest net present value after 30 years is expected to be in Germany 58741 €, Greece 51377 € and USA, California 37589 €. In these three countries solar power is already viable option and can compete with conventional electricity generation sources for the private household sector even without incentives or subsidies. In other countries: Lithuania, India, China, solar power is still quite expensive and government support is needed in order to be attractive choice for household owners. In Norway solar power for grid-connected customers is far away from being competitive. Additionally, country has a huge amount of cheap renewable hydro energy, so there is no need to switch to other source. In Norway, solar power can be a choice for distant mountain house (hytte) owners, where connection to the grid would be too expensive. Additionally, system would require batteries, which will make the project costs substantially higher, but still would probably be the cheapest option. In UAE electricity price for private house owners is so cheap, that solar power has tough time competing with conventional energy sources, even though solar irradiance is very high and stable throughout the year. The country is known for implementing incredible projects and currently one of the biggest solar farm of 800MW is under construction. The project is a part of the plan to produce 75% of renewable energy sources in Dubai.

6. Future work

Future work includes repetition of several failed experiments and additional experiments such as chemical analysis of the wafers: glow discharge mass spectrometry to establish distribution of impurities. Additionally, standardly produced ingot IC1 should be compared with other ingots, produced in the “Impurity Control” project. Working solar module could be built from each of the ingot. Later, HP Mc-Si properties in real conditions could be

tested. Simulation of 30 years real life equivalent could be performed and conclusion drawn. For solar power viability case, each country energy policy could be estimated, electricity price tendencies evaluated and more detailed analysis performed.

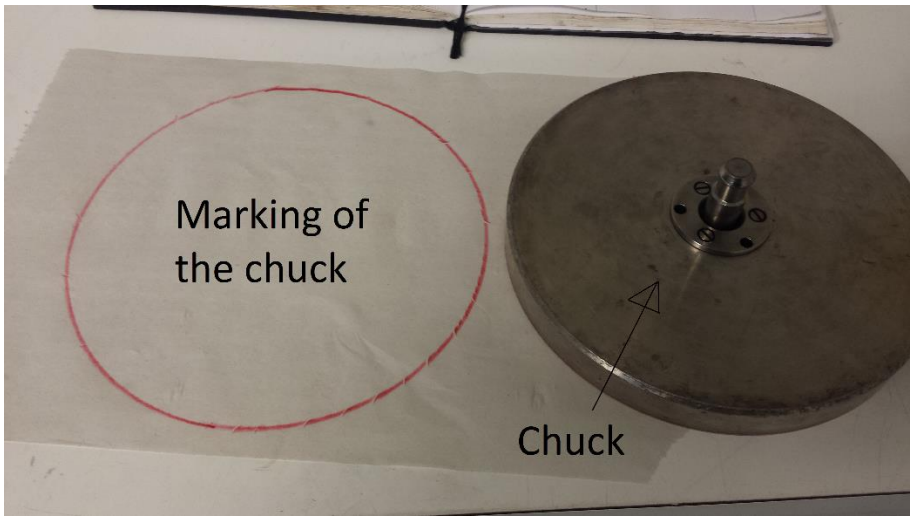
References

1. PV magazine https://www.pv-magazine.com/2017/01/19/pvma-figures-show-75-gw-of-solar-pv-was-installed-in-2016/.
2. Solar market prognosis https://cleantechnica.com/2016/08/03/global-solar-market-install-73-gw-2016-2017-slowdown/ accessed 2016-11-19.
3. Veikko Lindroos "Handbook of Silicon Based MEMS Materials and Technologies" 2010 Chapter 1.1.
4. Tonio Buonassisi lecture on "Wafer Silicon-Based Solar Cells" part II, 2014.
5. J.S. Kang and D.K. Schroder "J. Appl. Phys. 65", 1989 p. 2974-2985.
6. D. Lotfi, E. Hatem "Phosphorus diffusion gettering process of multicrystalline silicon using a sacrificial porous silicon layer", 2012.
7. A. E. Morishige, H. S. Laine, J. Schön, A. Haarahiltunen, J. Hofstetter, C. del Cañizo, M. C. Schubert, H. Savin, and T. Buonassisi, "Appl. Phys." A 120, 2015, p. 1357.
8. K. Adamczyk, G. Stokkan and M. Di Sabatino and others "Grain boundary effect on lifetime in high performance multicrystalline silicon during solar cell processing", 2016.
9. Anti-Reflection coatings http://pveducation.org/pvcdrom/anti-reflection-coatings.
10. SINTEF conference "Anti-reflection coatings for silicon solar cells" https://www.sintef.no/contentassets/a7b420c8e5474cc4880c748a9ebb66a1/daniel-n-wright.pdf.
11. B. J. Hallam, P. G. Hamer and others "Advanced hydrogenation of dislocation clusters and boron-oxygen defects in silicon solar cells", 2015.
12. Pr. Stuart Wenham Lecture "UNSW Advanced Hydrogenation", 2016. https://www.youtube.com/watch?v=FjiDXeIjfis.
13. J.Nelson "The Physics of Solar Cells" 2003.
14. Direct and indirect bandgap semiconductors https://www.researchgate.net/figure/281067517_fig11_Direct-and-indirect-band-gap.
15. Sven Rühle "Tabulated values of the Shockley – Queisser limit for single junction solar cells" 2016.
16. Maximum theoretical efficiency of silicon solar cell http://www.sciencedirect.com/science/article/pii/S0038092X16001110.
17. G. Colleti "Impurities in silicon and their impact on solar cell performance" 2011.
18. G. Colleti "Impact of Metal Contamination in Silicon Solar Cells" 2010.
19. D. Hull, D.J. Bacon "Introduction to Dislocations (Fifth Edition)" 2011 Chapter 1.
20. J.W. Morris, Jr. "Defects in Crystals - Materials Science & Engineering" Chapter 4.
21. Edge dislocations https://inspirehep.net/record/923936/files/edgedislocation.png, accessed 2016-12-05.
22. Screw dislocations https://inspirehep.net/record/923936/files/screwdislocation.png, accessed 2016-12-05.
23. M. A. Meyers, K. K.Chawla "Mechanical Behavior of Materials" 2008 2nd edition Chapter 4.
24. Interfaces and orientation relations, lecture 8 https://www.youtube.com/watch?v=PEoPSC1TS_o.
25. Valerie Randle "The coincidence site lattice and the sigma enigma" 2002.
26. B. Gallien "Analysis of grain orientation in cold crucible continuous casting of photovoltaic Si" 2011 p. 208 – 211.
27. A. Voigt "Grain orientation and grain boundaries in cast multicrystalline silicon, 1998 p. 202 – 206.

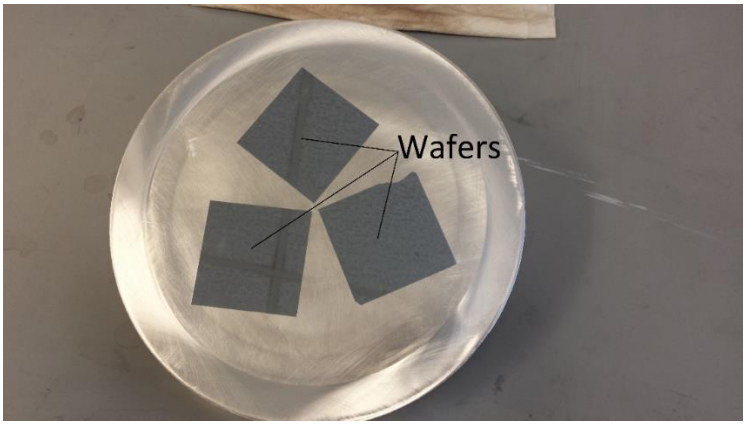
28. A. Autruffe “Influence of pulling rate on multicrystalline silicon ingots” properties, 2014 p. 199 – 203.
29. J. Chen and others “Electron beam induced current study of grain boundaries in multicrystalline silicon” 2004.
30. H. J. Queisser Journal of Electrochemical Society “Properties of Twin Boundaries in Silicon” Vol. 110, No. 1.
31. Journal Science and Technology Review “In Metals Not All Twins Are Identical” issue January/February 2014.
32. V.A. Oliveiraa, B. Mariea, C. Cayrond “Formation mechanism and properties of twinned structures in (111) seeded directionally solidified solar grade silicon” 2016 Vol. 121.
33. Stacking faults https://www.researchgate.net/figure/23801906_fig5_Atomic-configurations-of-intrinsic-and-extrinsic-stacking-faults-in-fcc-Cu-Dashed-lines.
34. S. Goldstein, D. Newbury “Scanning Electron Microscopy and X-ray analysis”, 2003 3rd edition.
35. G. Stokkan, M. Di Sabatino, B. R. Olaisen, R. Søndenå Ø. Dahl “Characterization Techniques for Silicon Solar Cells” 2011.
36. T. Trupke, B/Mitchell and others “Photoluminescence Imaging for Photovoltaic Applications”, 2012.
37. C.W. Lana, A. Lana, C.F. Yanga and others “The emergence of high-performance multi-crystalline silicon in photovoltaics”, 2016.
38. “Solar irradiance world map” http://solargis.com/assets/graphic/free-map/GHI/Solargis-World-GHI-solar-resource-map-en.png.
39. PV farm in Germany, Bavaria https://www.niftyhomestead.com/blog/integrated-solar/.
40. Solar module standard warranty characteristics http://rentechno.ua/en/services/procurement/modules/solitek.html.
41. PV module average price in the market https://www.pv-magazine.com/features/investors/module-price-index/
42. G. Stokhan and others “Study of evolution of dislocation clusters in high performance multicrystalline silicon”, 2014.
43. K. Adamczyk, R. Søndenå, G. Stokkan, Marisa Di Sabatino and others “Grain boundary effect on lifetime in high performance multicrystalline silicon during solar cell processing”, 2016.
44. Average salary https://www.numbeo.com/cost-of-living/country_price_rankings?itemId=105&displayCurrency=EUR.
45. Average electricity price http://www.uscib.org/valueadded-taxes-vat-ud-1676/.
46. Dubai solar power plant https://www.pv-magazine.com/2017/01/17/epc-chosen-and-groundbreaking-set-to-commence-on-800-mw-solar-plant-in-dubai.
47. H. J. Choi, M. I. Bertoni, J. Hofstetter, D. P. Fenning, D. M. Powell, S. Castellanos, and T. Buonassisi “Dislocation Density Reduction During Impurity Gettering in Multicrystalline Silicon”, 2013.

Appendix A. Grinding and polishing manual

1. **Preparing the workplace**. Clean the table, chucks with hot water. Clean polishing pads with water using standard brush for 9 and 3 µm pads and brush named 1 µm for 1 µm polishing pad.
2. **Marking**. Take a paper and make marking of chuck position around. Fold it to get the center point.



3. **Gluing**. Heat up the stove. Use power level 2. First heat the chuck. Use a separate paper between stove and chuck. When chuck is hot enough (when wax melts) take it out and put on the marked paper. Now put the samples on the stove. Use a paper between them. Use transparent wax, which can be washed with hot water. Apply thin layer of wax as little as possible. Remember which side you are going to polish and put wax on the opposite side. Move the chuck away and position wafers on the marked paper. If working with 3 wafers on 1 chuck, try to get the similar angle or in this case 120 angle between the wafers. Now put the chuck on top of the wafers. After few seconds lift the chuck up. The wafers are now stuck. Move wafers slightly round to distribute wax evenly. Finally, put the chuck back on the paper and leave it to cool down. Normally, it takes around 1.5 - 2h, you can use ventilator to speed the cooling.



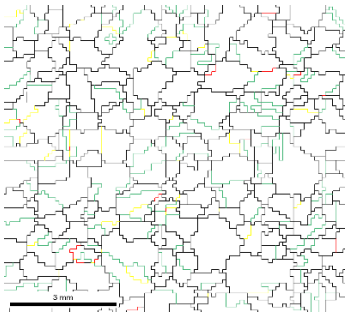
4. **Grinding**. Put a sticky paper first on the grinding machine. Now take a 1200 µm grit paper and put on top of it. Start the water, use as little as possible. Put the chuck on the grinding pad and move it around to let the air bubbles out. Attach chuck to the holder and lift it. Start the grinding machine at 3x100 RPM and start the rotation of the chuck. Push the chuck down. Note: you don't need to hold it. Set the timer for 3min. After it's finished, stop grinding machine and chuck rotation at the same time to avoid shear forces. Detach chuck, slide it all the way, take it out and check for the results. Remove cracked parts of wafer to make sure it will not scratch the rest. Change the grinding paper. For that move the water supply to the side, rotate the grinding machine at high speed to take away water. Change grinding paper. Don't forget to re-attach water supply. Repeat the procedure. Grind 2-3 times according to the samples. Clean the samples with cold water and paper. Dry it with paper.
5. **Polishing**. Attach 9 µm polishing pad on the automatic machine. For the 1st time on all dry pads rotate the pad and add some blue lubricant.

   Settings for 9 µm polishing: program 3, 5min, dosing level 5, suspension level 6. Polish 1-2 times depending on results. After finishing, clean the chuck with cold water and paper, dry it with paper. Don't forget to check the bucket if it's not full of used water. Change polishing pad to 3 µm. Repeat the procedure.

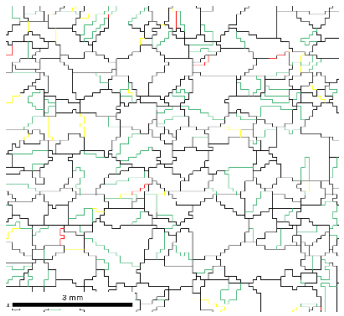
   Settings for 3 µm polishing: program 4, 5min, suspension level 8. Polish 2 times. Clean the chuck again. Change to 1 µm polishing pad. Repeat the procedure.

   Settings for 1 µm polishing: program 5, 3min, suspension level 10. Important: from this step, use gloves. Clean the chuck with cold water and paper.
6. **Unmounting wafers.** Use hot water to heat the chuck and gently slide the wafers from the chuck. Place the wafers in the holder and wash the wax off. Place the wafers vertically to dry off. Clean after yourself. Fill in the book.

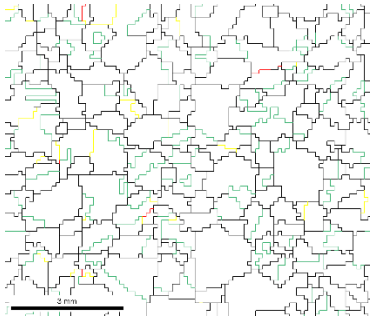
Appendix B. GB maps



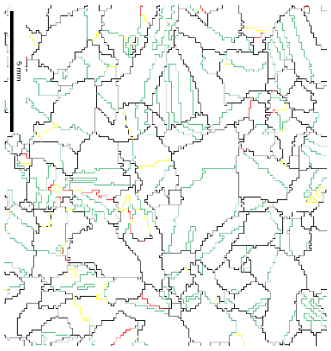
Ungettered IC1-008



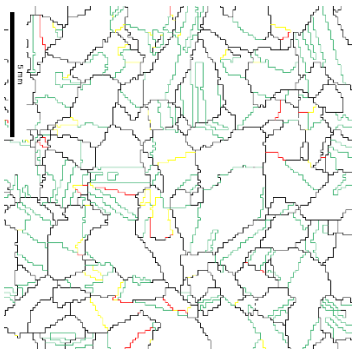
Gettered IC1-009



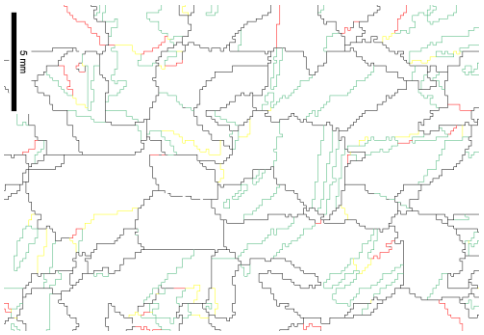
Gettered+Hydrogenated IC1-010



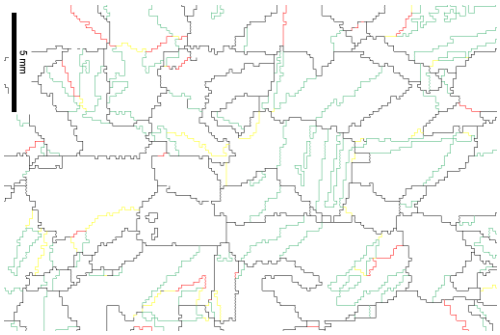
Gettered IC1-039



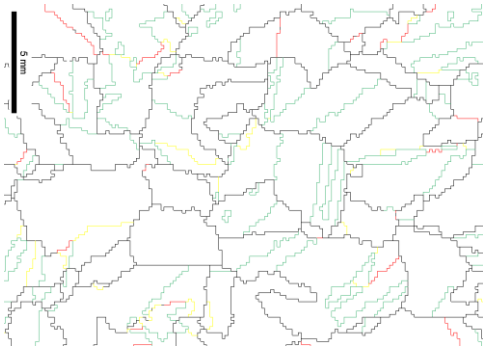
Gettered+Hydrogenated IC1-040



Ungettered IC1-128



Gettered IC1-129



Gettered+Hydrogenated IC1-130

SOLI TEK

Created for energy, designed for YOU

Appendix C. Standard solar module data sheet

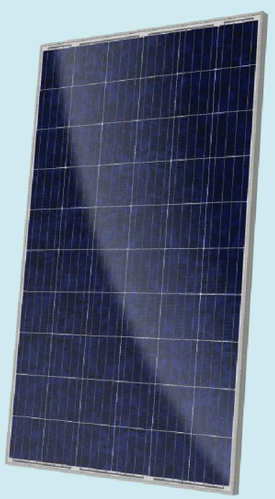
Priedas Nr.3

Soli Tek P60.6 - 250/260

Standard polycrystalline 60 cell module

Soli Tek is the European manufacturer and supplier of PV cells and modules with headquarters and production plant in Vilnius, Lithuania.

The company combines the most sophisticated technologies and over 16 years of manufacturing experience.



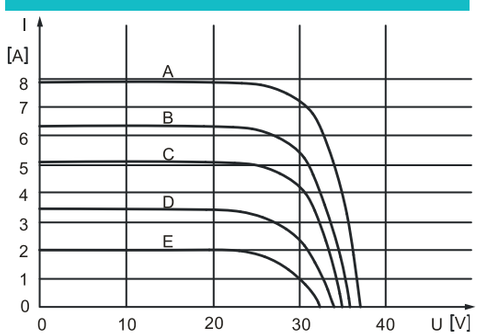
WORKING CONDITIONS

Maximum System Voltage	DC 1000V (TUV)
Operating temperature	-40ºC / +85ºC
Maximum reverse current	15 A
Max. wind load/max. snow load	2400 Pa / 5400 Pa
IP protection level	65
Safety class	II

TEMPERATURE COEFFICIENTS

Voltage temperature coefficient (β)	-0,37 %/K
Current temperature coefficient (α)	+0,06 %/K
Power temperature coefficient (δ)	-0,47 %/K

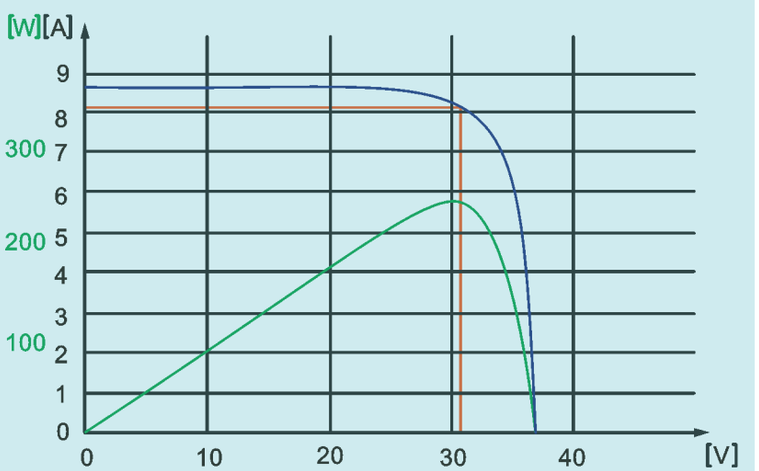
I-V CURVE



A: 1000 W / m² C: 600 W / m² E: 200 W / m²
B: 800 W / m² D: 450 W / m²

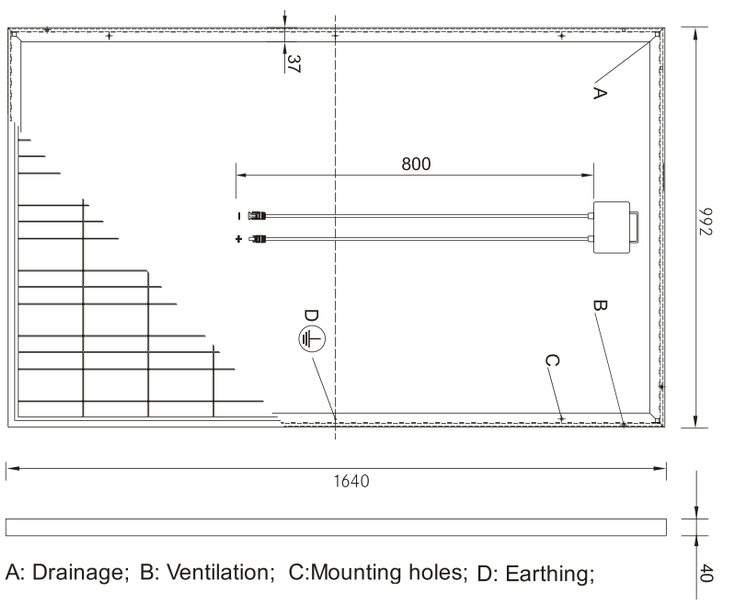
ELECTRICAL PARAMETERS

Type	Soli Tek P60.6–250	Soli Tek P60.6–255	Soli Tek P60.6–260
Maximum Power* (PMPP)	250.1 – 255.0 Wp	255.1 – 260.0 Wp	260.1 – 265.0 Wp
Rated Voltage (VMPP)	31,3 V	31,9 V	32,6 V
Rated Current (IMPP)	8,06 A	8,09 A	8,12 A
Open Circuit Voltage (VOC)	38,4 V	38,5V	38,6 V
Short Circuit Current (ISC)	8,6 A	8,6 A	8,64 A
Power tolerance	0+3 %	0+3 %	0+3 %
NOCT	48,3°C	48,3°C	48,3°C



MECHANICAL PARAMETERS

Cell size	156x156 mm (diagonal: 200 mm)
Number of cells	6x10, three strings in a row
Front side glass	3,2 mm hardened solar glass
Weight	19 kg
Dimensions (L x W x H)	1640 x 992 x 40 (or 42mm)
J-box	Plastic, IP65, ventilated
Cable length	0,8 – 1,1 m
Cable cross section size	4 mm2
Number of diodes	3
Plug-in connection	MC4 or equivalent
Frame	Anodised Al frame
Packing configuration	25 pcs./pallet



A: Drainage; B: Ventilation; C:Mounting holes; D: Earthing;

MADE BY USING RENEWABLE ENERGY
MADE IN EU
LITHUANIA

12 years — GUARANTEE 12 YEARS

90% max output — GUARANTEE 10 YEARS

80% max output — GUARANTEE 25 YEARS

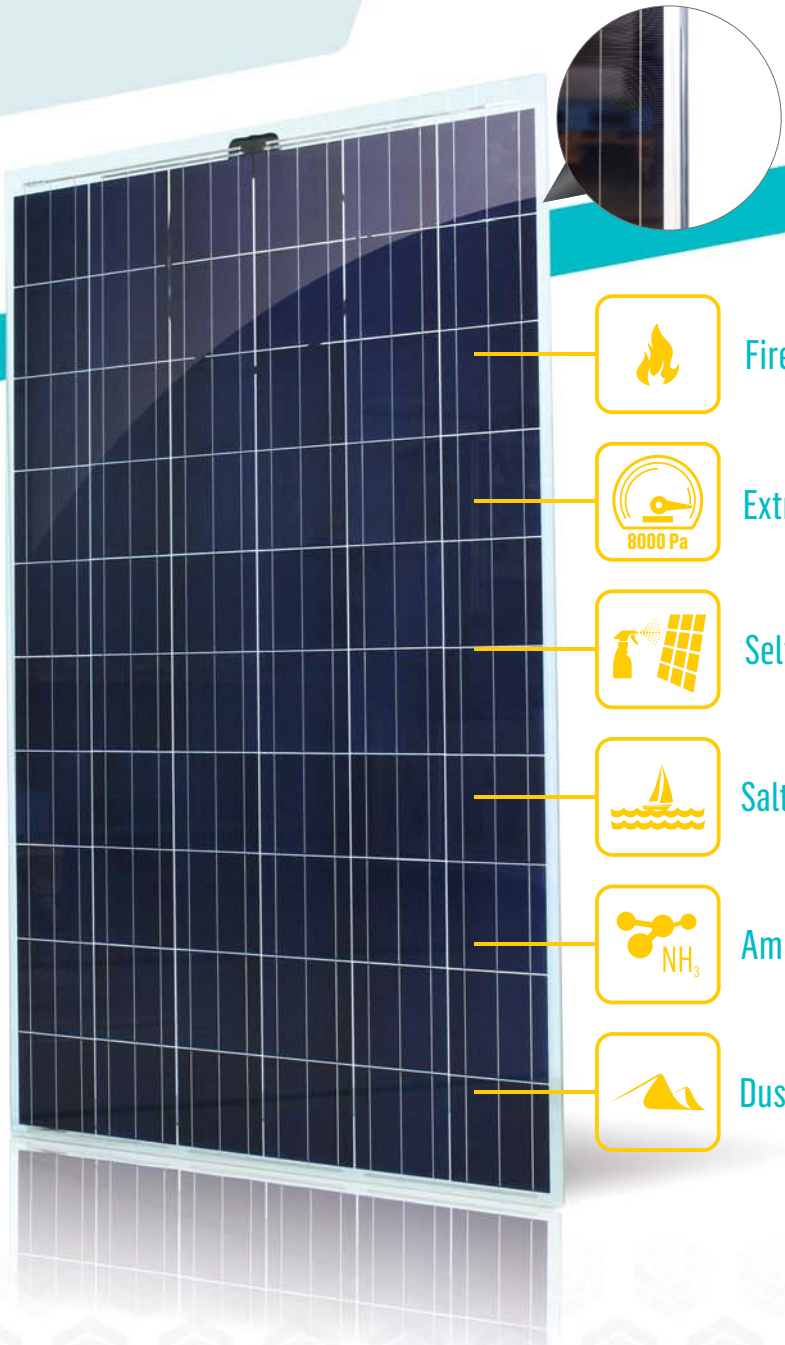
Soli Tek cells Moksliininku str. 6A, Vilnius 08412, Lithuania
Tel: +370 5 263 8774 Fax: +370 5 263 8776 info@solitek.eu www.solitek.eu

Appendix D. Glass-glass solar module datasheet

Solid PRO

Glass/Glass

250/260W



- Fire class A
- Extreme load resistance (8000 Pa)
- Self-cleaning effect
- Salt mist resistance
- Ammonia resistance (NH_3)
- Dust & Sand resistance

PRODUCT WARRANTY 30 YEARS.

EFFICIENCY GUARANTEE 30 YEARS.

POWER GUARANTEE 90% AFTER 30 YEARS.

IEC 61215
IEC 61730
IEC 62716
IEC 61701:2011

PID free

Available with Tigo energy

Available with SOLRIF®

MADE BY USING RENEWABLE ENERGY — MADE IN EU LITHUANIA

SOLITEK MANUFACTURER & SUPPLIER SOLAR GLASS SYSTEMS

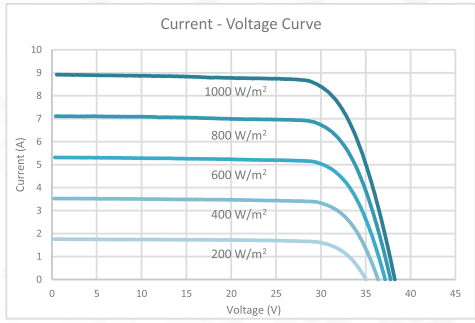
Soli Tek cells Mokslininku str. 6A, Vilnius 08412, Lithuania. Tel: +370 5 263 8774 info@solitek.eu www.solitek.eu

Solid PRO

Glass/Glass

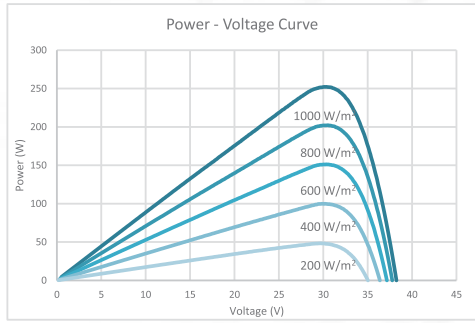
250/260W

Mechanical data	SOLID PRO 250 Wp	SOLID PRO 260 Wp
Dimensions (LxWxH) (mm)	1645x986x7,1	1645x986x7,1
Weight (kg)	27	27
Front / Back glass (mm)	3	3
Cell Type	Poly-crystalline 156x156mm (6 inch)	Poly-crystalline 156x156mm (6 inch)
Cell Orientation	60 cells (6x10)	60 cells (6x10)
Frame	Frameless	Frameless
Junction Box / IP class	TE Connectivity J-box IP67	TE Connectivity J-box IP67
Cable Cross Section Size (mm2)	4	4
Bypass Diodes	3	3
Connector	PV4-S Male/Female	PV4-S Male/Female

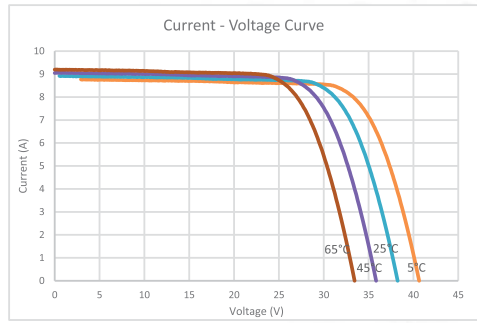


Electrical data (STC*)	SOLID PRO 250 Wp	SOLID PRO 260 Wp
Rated maximum power at STC (Wp)	250.00	260.00
Open Circuit Voltage (Voc/V)	36.23	37.32
Short Circuit Current (Isc/A)	8.86	8.95
Max Power Voltage (Vmp/V)	30.19	31.10
Max Power Current (Imp/A)	8.28	8.36
Max System Voltage (V)	DC 1000V (EU)	DC 1000V (EU)
Max Current (A)	15	15
Operating Temperature	-40~+85C	-40~+85C
Power Tolerance	0/+5W	0/+5W
Safety Class	II	II
Max Static Load (wind/snow) (Pa)	2400/8000	2400/8000

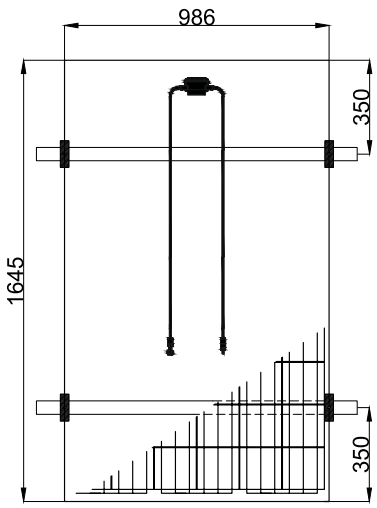
***Under Standard Test Conditions (STC) of irradiance of 1000W/sq. m., spectrum AM 1.5 and cell temperature of 25 C**



Temperature ratings	SOLID PRO 250 Wp	SOLID PRO 260 Wp
Temperature Coefficient of Isc (αIsc)	+0,05%/°C	+0,05%/°C
Temperature Coefficient of Voc (βVoc)	-0,34%/°C	-0,34%/°C
Temperature Coefficient of Pmax (γPmp)	-0,46%/°C	-0,46%/°C
Nominal Operating Cell Temperature	46°C	46°C

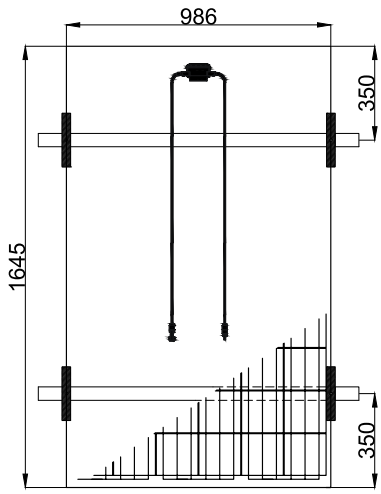


2400/2400 Pa



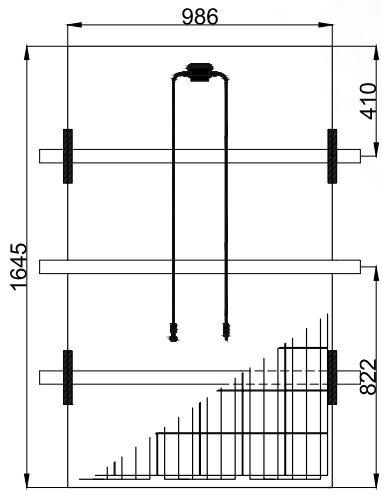
Alumero fixing clamps
END/MID clamps 6.8 100mm

2400/5400 Pa



Alumero fixing clamps
END/MID clamps 6.8 200mm

2400/8000 Pa



Alumero fixing clamps
END/MID clamps 6.8 200mm

Dealer Information

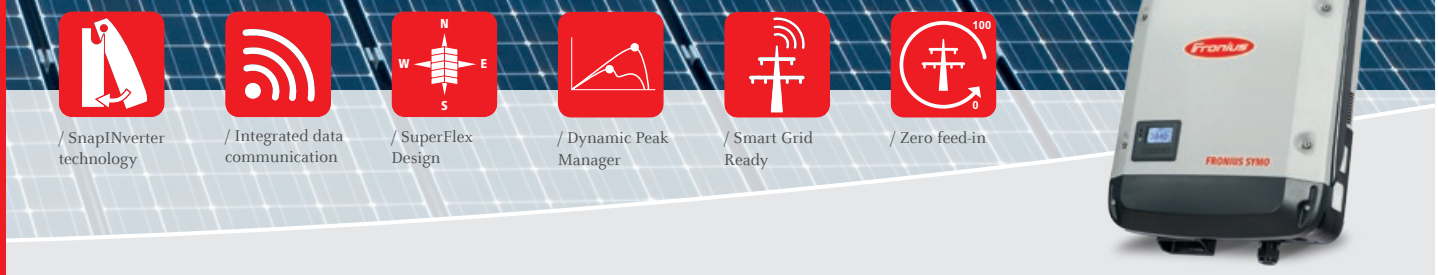
Soli Tek cells Mokslininku str. 6A, Vilnius 08412, Lithuania. Tel: +370 5 263 8774 info@solitek.eu www.solitek.eu

Appendix E. Inverter data sheet

/ Perfect Welding / Solar Energy / Perfect Charging

FRONIUS SYMO

/ Maximum flexibility for the applications of tomorrow.



/ SnapINverter technology

/ Integrated data communication

/ SuperFlex Design

/ Dynamic Peak Manager

/ Smart Grid Ready

/ Zero feed-in

/ With power categories ranging from 3.0 to 20.0 kW, the transformerless Fronius Symo is the three-phase inverter for systems of every size. Owing to the SuperFlex Design, the Fronius Symo is the perfect answer to irregularly shaped or multi-oriented roofs. The standard interface to the internet via WLAN or Ethernet and the ease of integration of third-party components make the Fronius Symo one of the most communicative inverters on the market. Furthermore, the meter interface permits dynamic feed-in management and a clear visualisation of the consumption overview.

TECHNICAL DATA FRONIUS SYMO (3.0-3-S, 3.7-3-S, 4.5-3-S, 3.0-3-M, 3.7-3-M, 4.5-3-M)

INPUT DATA	SYMO 3.0-3-S	SYMO 3.7-3-S	SYMO 4.5-3-S	SYMO 3.0-3-M	SYMO 3.7-3-M	SYMO 4.5-3-M
Number MPP trackers	1			2		
Max. input current ($I_{dc\ max\ 1}$ / $I_{dc\ max\ 2}$ [1])	16.0 A			16.0 A / 16.0 A		
Max. array short circuit current (MPP_1/MPP_2 [1])	24.0 A			24.0 A / 24.0 A		
DC input voltage range ($U_{dc\ min}$ - $U_{dc\ max}$)	150 - 1,000 V					
Feed-in start voltage ($U_{dc\ start}$)	200 V					
Usable MPP voltage range	150 - 800 V					
Number of DC connections	3			2+2		
Max. PV generator output ($P_{dc\ max}$)	6.0 kW_{peak}	7.4 kW_{peak}	9.0 kW_{peak}	6.0 kW_{peak}	7.4 kW_{peak}	9.0 kW_{peak}

OUTPUT DATA	SYMO 3.0-3-S	SYMO 3.7-3-S	SYMO 4.5-3-S	SYMO 3.0-3-M	SYMO 3.7-3-M	SYMO 4.5-3-M
AC nominal output ($P_{ac,r}$)	3,000 W	3,700 W	4,500 W	3,000 W	3,700 W	4,500 W
Max. output power	3,000 VA	3,700 VA	4,500 VA	3,000 VA	3,700 VA	4,500 VA
AC output current ($I_{ac\ nom}$)	4.3 A	5.3 A	6.5 A	4.3 A	5.3 A	6.5 A
Grid connection (voltage range)	3-NPE 400 V / 230 V or 3-NPE 380 V / 220 V (+20 % / -30 %)					
Frequency (Frequency range)	50 Hz / 60 Hz (45 - 65 Hz)					
Total harmonic distortion	< 3 %					
Power factor (cos $\varphi_{ac,r}$)	0.70 - 1 ind. / cap.			0.85 - 1 ind. / cap.		

GENERAL DATA	SYMO 3.0-3-S	SYMO 3.7-3-S	SYMO 4.5-3-S	SYMO 3.0-3-M	SYMO 3.7-3-M	SYMO 4.5-3-M
Dimensions (height x width x depth)	645 x 431 x 204 mm					
Weight	16.0 kg			19.9 kg		
Degree of protection	IP 65					
Protection class	1					
Overvoltage category (DC / AC) [2]	2 / 3					
Night time consumption	< 1 W					
Inverter design	Transformerless					
Cooling	Regulated air cooling					
Installation	Indoor and outdoor installation					
Ambient temperature range	-25 - +60 °C					
Permitted humidity	0 - 100 %					
Max. altitude	2,000 m / 3,400 m (unrestricted / restricted voltage range)					
DC connection technology	3x DC+ and 3x DC- screw terminals 2.5 - 16 mm²			4x DC+ and 4x DC- screw terminals 2.5 - 16mm² [3]		
AC connection technology	5-pole AC screw terminals 2.5 - 16 mm²			5-pole AC screw terminals 2.5 - 16mm² [3]		
Certificates and compliance with standards	ÖVE / ÖNORM E 8001-4-712, DIN V VDE 0126-1-1/A1, VDE AR N 4105, IEC 62109-1/-2, IEC 62116, IEC 61727, AS 3100, AS 4777-2, AS 4777-3, CER 06-190, G83/2, UNE 206007-1, SI 4777 [1], CEI 0-21 [1], NRS 097					

[1] This applies to Fronius Symo 3.0-3-M, 3.7-3-M and 4.5-3-M.
[2] According to IEC 62109-1.
[3] 16 mm² without wire end ferrules. Further information regarding the availability of the inverters in your country can be found at **www.fronius.com.**