

Parasitic capacitances and inductances hindering utilization of the fast switching potential of SiC power modules. Simulation model verified by experiment.

S. Tiwari¹, O.-M. Midtgård¹, T. M. Undeland¹, and R. Lund²

¹Norwegian University of Science and Technology
7491 Trondheim, Norway
subhadra.tiwari@ntnu.no

²Rolls-Royce Marine AS
7041 Trondheim, Norway
richardl@smartmotor.no

Acknowledgments

The authors would like to thank The Research Council of Norway and 6 industry partners who sponsor this project: EFD Induction, Siemens, Eltek, Statkraft, Norwegian Electric Systems, and Vacon.

Keywords

«Silicon Carbide (SiC)», «MOSFET», «Hard switching», «Switching losses», «Simulation», «Hardware», «Parasitics».

Abstract

This paper investigates the switching performances of two state-of-the-art half-bridge SiC MOSFET modules using a standard double pulse test methodology. A deliberate choice of the modules with the same voltage and current ratings, the same packaging, but different stray inductances and capacitances is made in order to give an insight into the influence of parasitics in the switching transients and energy losses. A circuit simulation is performed with varying stray parameters in an LTSpice to illustrate the impact of parasitics in both voltage and current waveforms. Thereafter, a detailed comparison between the two modules is presented at similar dv/dt and di/dt conditions through laboratory measurements. The experimental results confirm the simulation results, giving a clear message that parasitic capacitances and inductances hinder the fast switching potential of SiC power modules. Furthermore, the performance of device with different voltage ratings can be anticipated using this parametric study. Thus, the analysis and understanding of parasitics, and their influence on switching performance is vital in the choice of an appropriate SiC MOSFET module for a particular application. The present paper contributes in this regard.

1 Introduction

SiC MOSFETs have potential to switch extremely fast. For the best utilization of this benefit, it is indispensable to keep both the gate and power loops parasitic (stray inductances and capacitances) as low as possible. Several publications have explained the importance of having lower loop inductances for achieving fast and clean switching of power devices. For instance, the influence of parasitic inductances in the switching circuit are studied for discrete devices, namely, Si IGBT, Si MOSFET, and Si CoolMOS by inserting an external inductor in the loop in [1], [2], and [3] respectively. The same are investigated for SiC modules by deliberately choosing the modules with different package inductances in [4] and the detailed simulations are carried out for extracting the package inductances of SiC modules in [5]. Furthermore, designs of low inductive busbar are addressed in [6, 7, 8].

However, few studies have been conducted regarding the impact of stray capacitances in the switching waveforms. For example, in [9], an external capacitor is connected across the respective terminals of Si

MOSFET for studying such impacts. On the other hand, in this paper, the impact of parasitics are investigated by deliberately choosing SiC MOSFET modules with different stray parameters. The selected modules are APTSM120AM09CD3AG from Microsemi and CAS300M12BM2 from Wolfspeed and are also state-of-the-art devices. They have same voltage (1.2 kV) and current (300 A) ratings, and packaging as well. In particular, this work aims to provide knowledge for anticipating the relative switching performances of commercial power devices with different ratings, which will eventually help in choosing an appropriate device. Indeed, this work also provides a comparison of SiC MOSFET modules against each other, where little research has been performed.

The paper is organized as follows. The short description of methodology and laboratory setup is presented in Section 2. Thereafter, a circuit simulation in an LTSpice is included in Section 3. The main goal of this simulation is to study the influence of stray capacitances in the switching performances, which shows that the switching speed in SiC devices are slower with higher values of stray capacitances. In Section 4, the comparison between the two selected SiC modules are exemplified through laboratory measurements. Most importantly, this comparison illuminates the importance of having low parasitic in the module: both inductances and capacitances in order to reduce the stresses, such as overshoots and switching energy losses. This helps in selecting an appropriate SiC MOSFET module from the several available ones. Finally, the major conclusions are summarized in Section 5.

2 Methodology and laboratory setup

A standard double pulse test methodology is used for evaluating the stresses such as current and voltage overshoots, ringing, dv/dt , di/dt , and switching energy losses in the device under test (DUT). An equivalent circuit with a hard switched arrangement is shown in Fig. 1, where the total stray inductance in a switching loop (L_{stray}) is the sum of L_{dc-bus} , L_{byp} , and L_{module} . L_{module} is the effective stray inductance, which is distributed inside the module, represented by red coils. The current path during the turn-on process is denoted by blue dotted lines, whereas the current loop during the turn-off process is indicated by the green dotted lines.

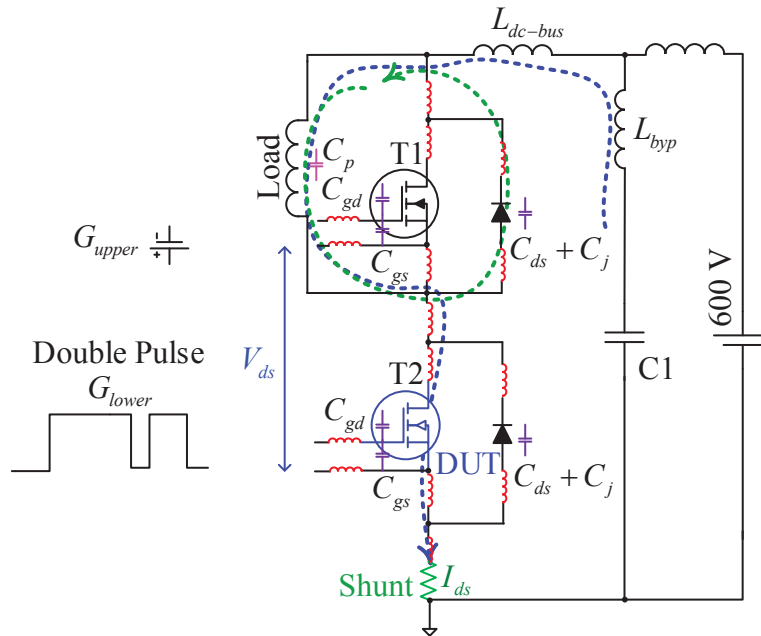


Fig. 1: Circuit diagram illustrating the distribution of L_{module} (in red colour coils) inside SiC module. Current paths show turn-on and turn-off processes in a buck converter during the double pulse test. Upper transistor (T1) is always turned off by applying -5 V in the gate source (G_{upper}) while double pulses are given in the gate source (G_{lower}) of lower transistor (T2) which is also the DUT. Internal capacitors of the SiC MOSFET module are represented by purple colour.

C_{gs} , C_{ds} and C_{gd} are internal capacitors of the MOSFET indicated at various places in the circuit. The values of these capacitors can vary depending on the applied voltage and can be expressed in terms of the datasheet parameters: C_{iss} , C_{oss} , and C_{rss} which are termed as input capacitor, output capacitor and reverse transfer capacitor of the DUT. Likewise, SiC Schottky barrier diode has a junction capacitor denoted by C_j and the load inductor has an inter-winding capacitor of C_p (indicated by pink colour in Fig.1). The internal capacitors denoted by purple colour in the schematic diagram are related to the datasheet parameters as

$$C_{gs} = C_{iss} - C_{rss} \quad (1)$$

$$C_{gd} = C_{rss} \quad (2)$$

$$C_{ds} = C_{oss} - C_{rss} \quad (3)$$

The dc-link is realized with a planar busbar except the termination parts (needed to facilitate the module connection) so that the stray inductance in the switching loop can be kept as low as possible. A current viewing resistor (CVR also called shunt) SSDN - 414 - 01 (400 MHz, 10 mΩ) from T&M research is used for measuring the drain current. The shunt replaces one of the screws in the SiC module as it is mounted directly on the screw terminal. This arrangement decreases the L_{stray} even further as one screw hole is eliminated in the busbar. L_{byp} and L_{dc-bus} are calculated using Ansys Q3D extractor, and is 14 nH in total [6]. The picture illustrating the placement of the shunt in the laboratory setup is shown in Fig. 2. An inductor with a single layer winding is used as the load in order to ensure minimum stray capacitance (C_p) so that the true switching characteristics of MOSFET are reflected. C_p is measured to be 10 pF using impedance analyser (E4990), which is a fairly small value.

High voltage differential probes (THDPO200, 200 MHz) are used for drain voltage (V_{ds}) and gate voltage (V_{gs}) measurements. An isolated gate driver with an adjustable output voltage [10] is used for driving the SiC MOSFETs where the gate voltage is set to 20 V for turn-on and -5 V for turn-off. For keeping the busbar inductances similar, both the modules are chosen with similar screw terminations. All the measurements are evaluated for a dc-link voltage of 600 V and a drain-source current of 300 A.

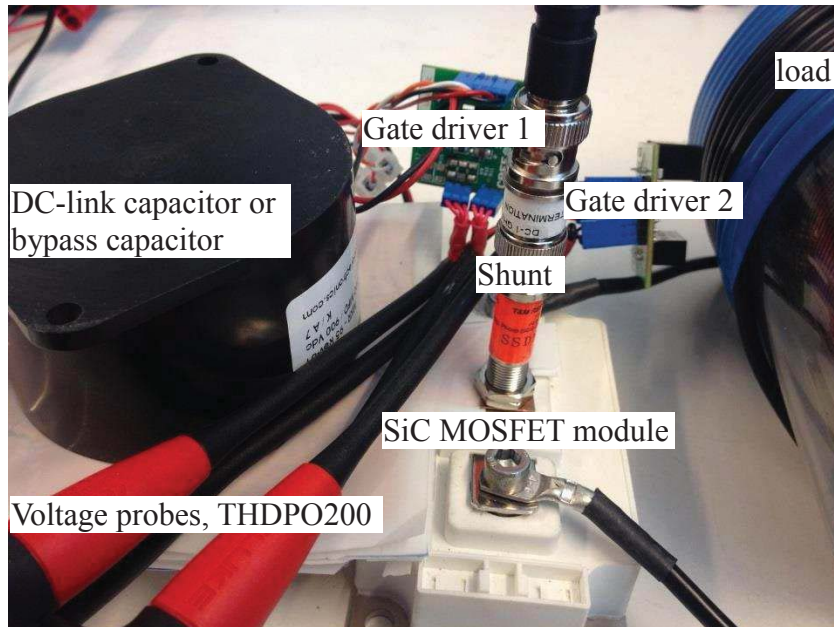


Fig. 2: Hardware setup showing a planar busbar, placement of current shunt instead of a screw, several parallel capacitors in the dc-link to reduce L_{byp} , and to realize an overall low L_{stray} in the switching loop. An inductor with a single layer winding is used as load in order to ensure minimum stray capacitance (measured to be 10 pF using impedance analyser, E4990) so that the true switching characteristics of MOSFET are reflected.

The number of chips, C_{iss} , C_{oss} and C_{rss} of the modules are listed in Table I [11, 12]. Q_c is the capacitive charge of the anti-parallel diode.

Table I: Major differences between the two selected SiC MOSFET modules.

Parameters / Module	CAS300M12BM2 Wolfspeed	APTSM120AM09CD3AG Microsemi
No. of chips \times ($m\Omega$)	6×25	9×80
C_{iss} (nF) @ 600 V	11.7	23
C_{oss} (nF) @ 600 V	2.55	1.1
C_{rss} (nF) @ 600 V	0.07	0.18
Q_c (nC)	3200	1080

3 Analysis of impact of stray capacitances by simulation in LTSpice

A simulation model in LTSpice is used for studying the impact of C_{gs} , C_{ds} , and C_{gd} . An example with C_{gd} connected in the model is shown in Fig. 3. For the other cases: C_{gs} and C_{ds} variations, the capacitors are connected between the respective terminals of the MOSFET. The values are chosen as per the datasheets of the chosen modules, as listed in Table I, and are considered for the case with V_{ds} of 600 V. Although, these capacitors show non-linear variations with V_{ds} , a constant value is taken into account because it is enough for relative performance evaluation. LTSpice model of SiC MOSFET is from Wolfspeed. This section is divided in three subsections. The simulated turn-off and turn-on transients of the currents and voltages in both the gate and drain sides with different C_{gs} , C_{ds} , and C_{gd} are elaborated in Subsection 3.1, Subsection 3.2 and Subsection 3.3 respectively.

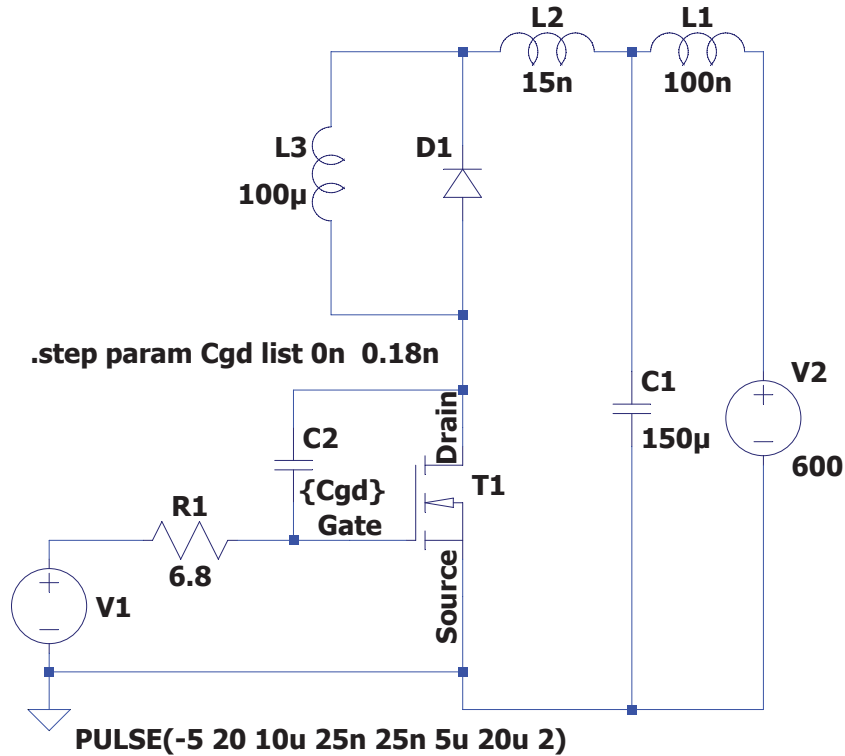
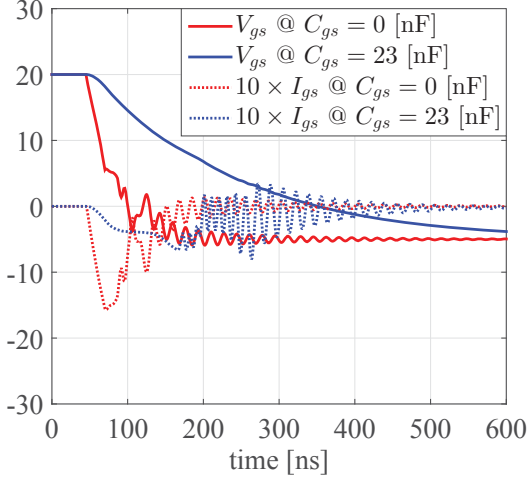


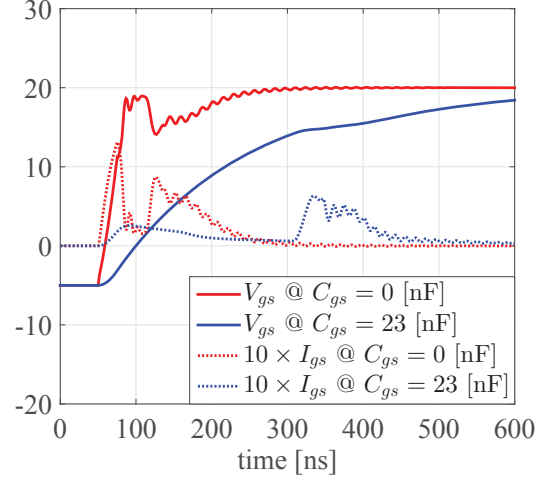
Fig. 3: Simulation model in LTSpice for the study of impact of stray capacitances. For a case with C_{gd} variation, a capacitor is connected between the gate and drain terminals of MOSFET as depicted in the model. For the other cases: C_{gs} and C_{ds} variations, the capacitors are connected between the respective terminals of the MOSFET. The values are chosen as per the datasheets of the modules, as catalogued in Table I, and are taken for the case with V_{ds} of 600 V. Spice model of SiC MOSFET is from Wolfspeed.

3.1 Impact of C_{gs}

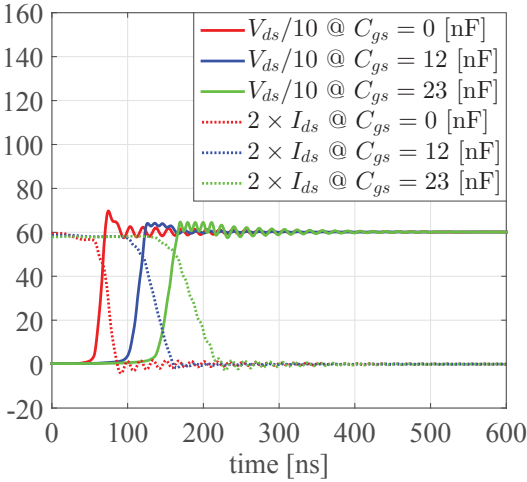
The simulated switching waveforms with varied C_{gs} are illustrated in Fig. 4. With higher values of C_{gs} , the slew rates in gate voltages are reduced significantly, the oscillations are mitigated and the delay times are prolonged, which are evident from Fig. 4 a) and Fig. 4 b). As a consequence, there is decrease of slew rates in drain currents (I_{ds}) as depicted in Fig. 4 c) and Fig. 4 d). Thus, the decreased slew rates and lengthened switching time durations will subsequently increase the switching losses.



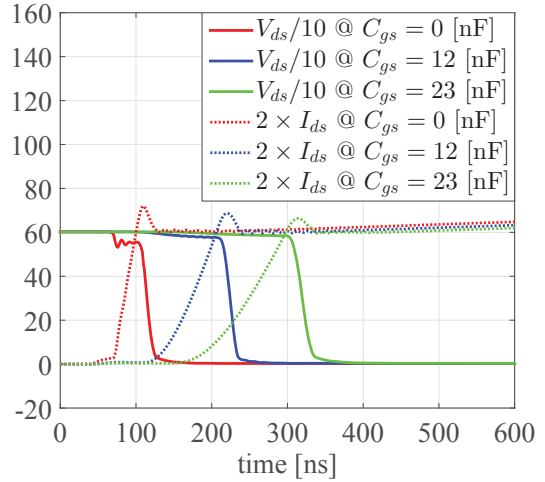
(a) Gate waveforms with different C_{gs} during turn-off.



(b) Gate waveforms with different C_{gs} during turn-on.



(c) Drain waveforms with different C_{gs} during turn-off.

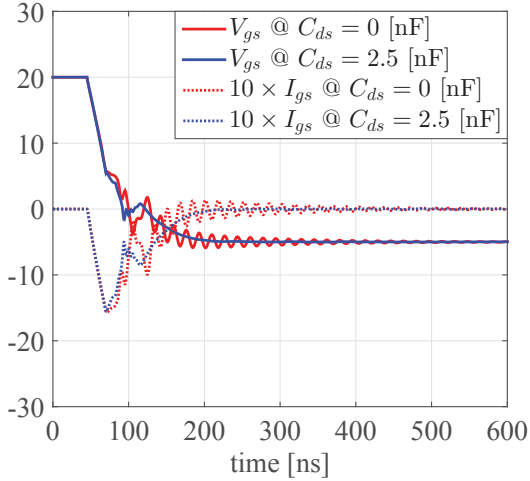


(d) Drain waveforms with different C_{gs} during turn-on.

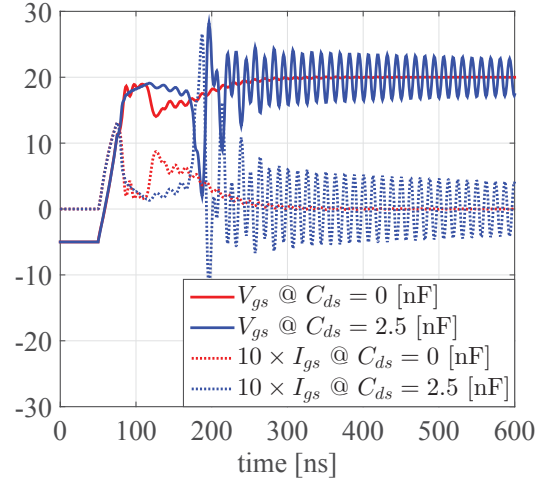
Fig. 4: Impact of different gate-source capacitances on gate and drain waveforms illustrating that these primarily determine the time constant of gate circuit and the slew rates of drain currents. All simulations are performed at drain-source voltage of 600 V and drain-source current of 300 A. V_{ds} are plotted with 10 times lower scale and I_{ds} with 2 times higher scale. Gate current waveforms (I_{gs}) are plotted with 10 times higher scale for better clarity. Chosen values of C_{gs} in the simulation are as per the datasheets of the selected modules, as listed in Table I. The gate resistor is kept constant as in Fig. 3 (6.8 Ω).

3.2 Impact of C_{ds}

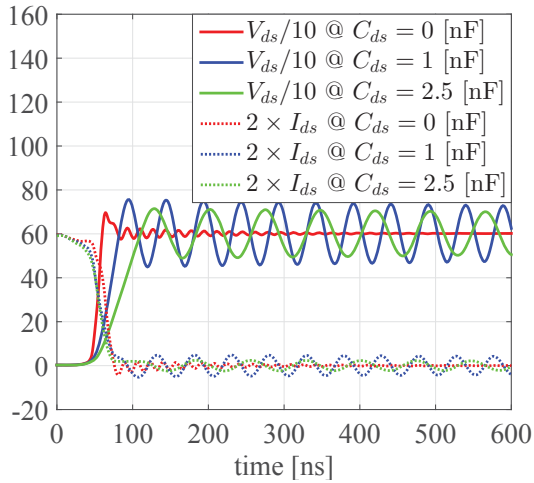
Fig. 5 presents the simulated switching waveforms with varied C_{ds} . Larger the value of C_{ds} , larger is the noise in I_{gs} and V_{gs} waveforms during turn-on, as shown in Fig. 5 b). Furthermore, it is evident from Fig. 5 c) and Fig. 5 d) that the voltage slew rates get slower and frequency of oscillations become smaller with higher values of C_{ds} . Besides, the current slew rates get slightly faster leading to higher current overshoots, as illustrated in Fig. 5 d).



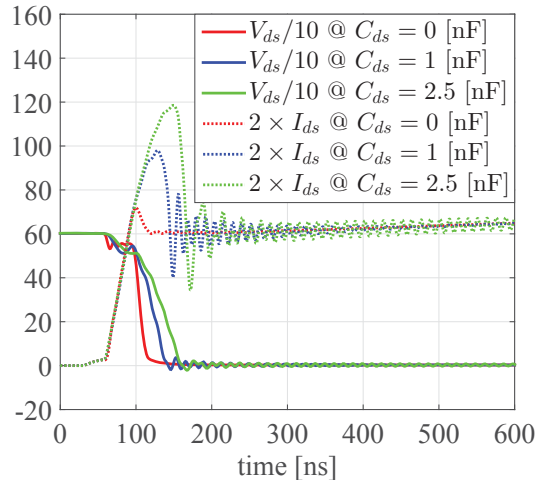
(a) Gate waveforms with different C_{ds} during turn-off.



(b) Gate waveforms with different C_{ds} during turn-on.



(c) Drain waveforms with different C_{ds} during turn-off.



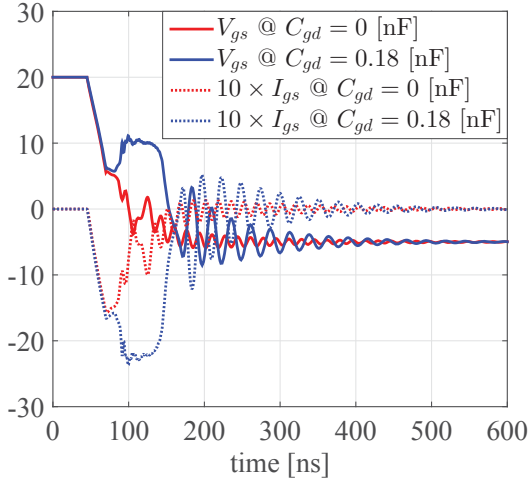
(d) Drain waveforms with different C_{ds} during turn-on.

Fig. 5: Impact of different drain-source capacitances on gate and drain waveforms illustrating that these mainly determine the parasitic ringings and slew rates of drain voltages. All simulations are performed at drain-source voltage of 600 V and drain-source current of 300 A. V_{ds} are plotted with 10 times lower scale and I_{ds} with 2 times higher scale. Gate current waveforms (I_{gs}) are plotted with 10 times higher scale for better clarity. Chosen values of C_{ds} in the simulation are as per the datasheets of the selected modules, as listed in Table I. The gate resistor is kept constant as in Fig. 3 (6.8 Ω).

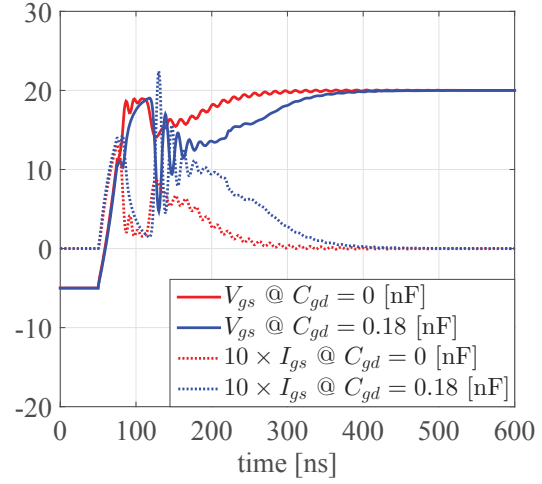
3.3 Impact of C_{gd}

Fig. 6 exemplifies the simulated switching waveforms with varied C_{gd} . It is apparent that both the gate current and voltage waveforms oscillate when C_{gd} increase, which is essentially because of dv/dt related noise coupled to gate side through miller capacitor (C_{gd}). This noise can exceed the threshold voltage limit of SiC MOSFET and cause unwanted turn-on of the device. In addition, it should be noted that the increase in C_{gd} hardly affects the time constant of V_{gs} . Besides, there is visible decrease in slew rates of V_{ds} waveforms, which is clearly shown in Fig. 6 c) and Fig. 6 d). However, the slew rates of I_{ds} are not affected at all, except that during turn-off I_{ds} are delayed a little bit. Thus, the decreased voltage slew rates and delayed current slew rates result in increased switching losses.

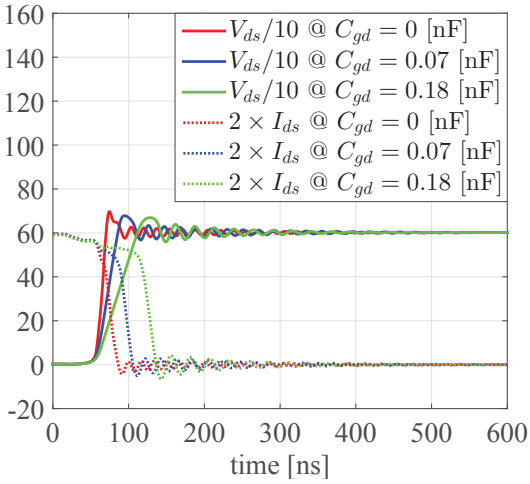
Overall, higher C_{gs} leads to cleaner V_{gs} waveforms; whereas, higher C_{gd} results in noisier ones. Hence, it is not only the absolute value of C_{gd} that endangers MOSFET, instead, it is more precisely related to the ratio of C_{gs}/C_{gd} . Thus, a MOSFET with higher C_{gs}/C_{gd} ratio should be chosen to avoid such turn-on.



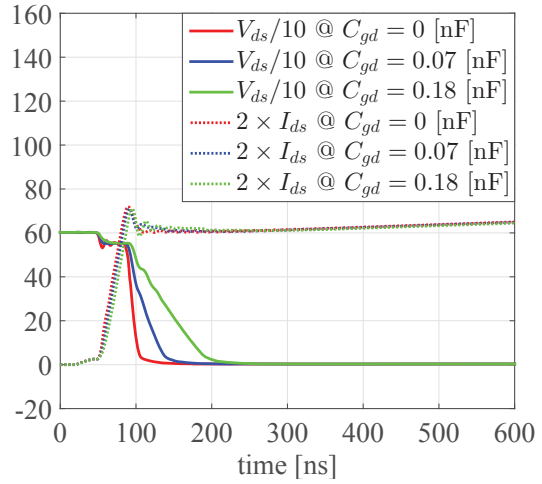
(a) Gate waveforms with different C_{gd} during turn-off.



(b) Gate waveforms with different C_{gd} during turn-on.



(c) Drain waveform with different C_{gd} during turn-off.



(d) Drain waveforms with different C_{gd} during turn-on.

Fig. 6: Impact of different miller capacitances on gate and drain waveforms illustrating that these mainly determine the slew rates of drain voltages. All simulations are performed at drain-source voltage of 600 V and drain-source current of 300 A. V_{ds} are plotted with 10 times lower scale and I_{ds} with 2 times higher scale. Gate current waveforms (I_{gs}) are plotted with 10 times higher scale for better clarity. Chosen values of C_{gd} in the simulation are as per the datasheets of the selected modules, as presented in Table I. The gate resistor is kept constant (6.8Ω as in Fig. 3) throughout the simulation.

Table II: Datasheet readings of SiC MOSFET dies with different voltage ratings: 1.2 kV and 1.7 kV.

Parameters / Die	CPM2-1200-0040B	CPM2-1700-0045B
Voltage rating (kV)	1.2	1.7
Chip size (mm \times mm)	3.10×5.90	4.08×7.35
Thickness (μm)	180 ± 40	380 ± 40
C_{iss} (pF) @ 1000 V	1893	3672
C_{oss} (pF) @ 1000 V	150	171
C_{rss} (pF) @ 1000 V	10	6.7

Looking back in Table I, the input, output and reverse transfer capacitances are different even for the same rated devices. Likewise, Table II shows the datasheet readings of SiC MOSFET dies with two different voltage ratings: 1.2 kV and 1.7 kV, as an example [13, 14]. Areas and thicknesses are different

for these chips and so are the capacitances. The point is that the parasitic capacitances can differ between the devices with same or different voltage ratings. Thus, this parametric study can be utilized to anticipate the relative performance differences in switching waveforms for such devices.

Besides, this simulations also give ideas about the impact of possible externally inserted parasitic capacitances, for instance: addition of a small capacitor or a voltage probe at gate and source; addition of an external anti-parallel diode across the drain and source, as it has a junction capacitance; and placement of the gate driver and module, as it can form a parallel trace between the gate and drain, and thereby form a capacitance across it.

4 Experimental results

In this section, the gate resistance is changed to obtain similar dv/dt and di/dt conditions for the selected modules.

4.1 Similar dv/dt during turn-off

An example of the turn-off switching transients with similar dv/dt in each modules are illustrated in Fig. 7 a) and Fig. 7 b). The frequency of oscillations in both the modules are approximately equal, even though the effective junction capacitance formed by the MOSFET output capacitance and junction capacitance of anti-parallel diode are smaller for Microsemi, indicating the presence of higher L_{module} in the Microsemi compared to the Wolfspeed. Furthermore, for this case, di/dt is smaller for the Microsemi (7.33 A/ns) compared to the Wolfspeed (8.2 A/ns), which is governed mainly by two reasons, first: higher L_{module} , second: higher C_{gs} . The simulation with varying L_{stray} as presented in the previous work [4] supports the former reason and the latter is in accordance with the simulation presented with varying C_{gs} in Subsection 3.1. Smaller voltage overshoot for Microsemi is mainly due to smaller di/dt .

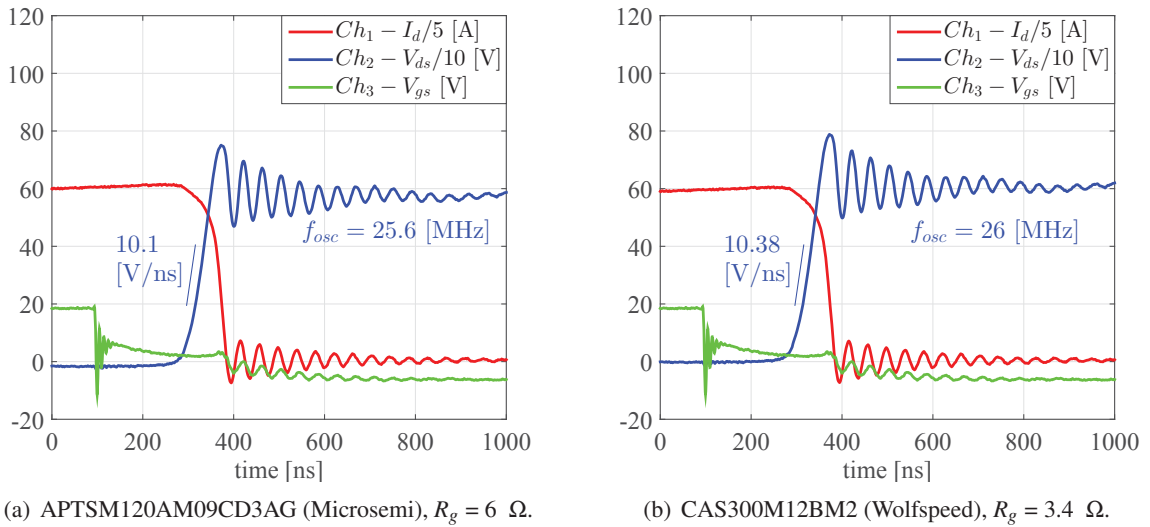


Fig. 7: Turn-off transients of two modules at similar dv/dt during turn-off.

4.2 Similar di/dt during turn-off

Fig. 8 elucidates the turn-off transients of two modules at similar di/dt during turn-off. Higher voltage overshoot in Microsemi clearly refers to the higher L_{module} in it compared to the Wolfspeed module. It is worth mentioning that the V_{ds} of the lower side MOSFET in the half-bridge is measured across the sources of the upper and the lower MOSFETs. If it was measured across the power terminals, the oscillations would be almost invisible.

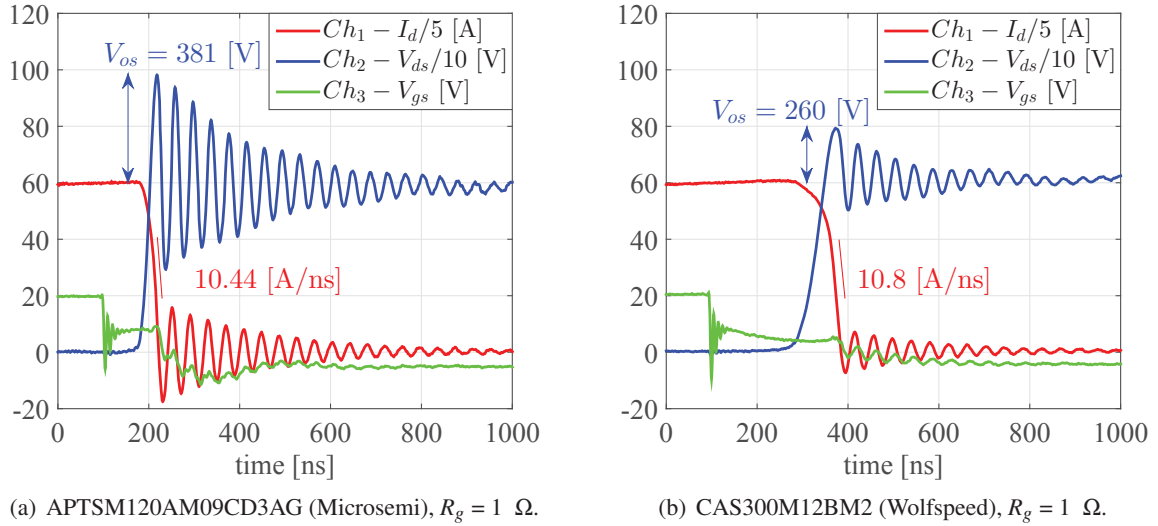


Fig. 8: Turn-off transients of two modules at similar di/dt during turn-off. V_{ds} of the lower side MOSFET in the half-bridge is measured across the sources of the upper and the lower MOSFETs.

4.3 Similar di/dt during turn-on

For the case with similar di/dt during turn-on, the waveforms are shown in Fig. 9 a) and Fig. 9 b). There are series of reasons for current overshoot being smaller in the Microsemi compared to the Wolfspeed. As shown in Table I, Q_c of diode is 0.33 times smaller, C_{iss} is 1.96 times larger, C_{ds} is 0.37 times smaller in the Microsemi compared to the Wolfspeed, which are all favorable for reducing di/dt of the device. This fact also conforms to the simulation presented with varying C_{gs} and C_{ds} in Subsection 3.1 and Subsection 3.2 respectively.

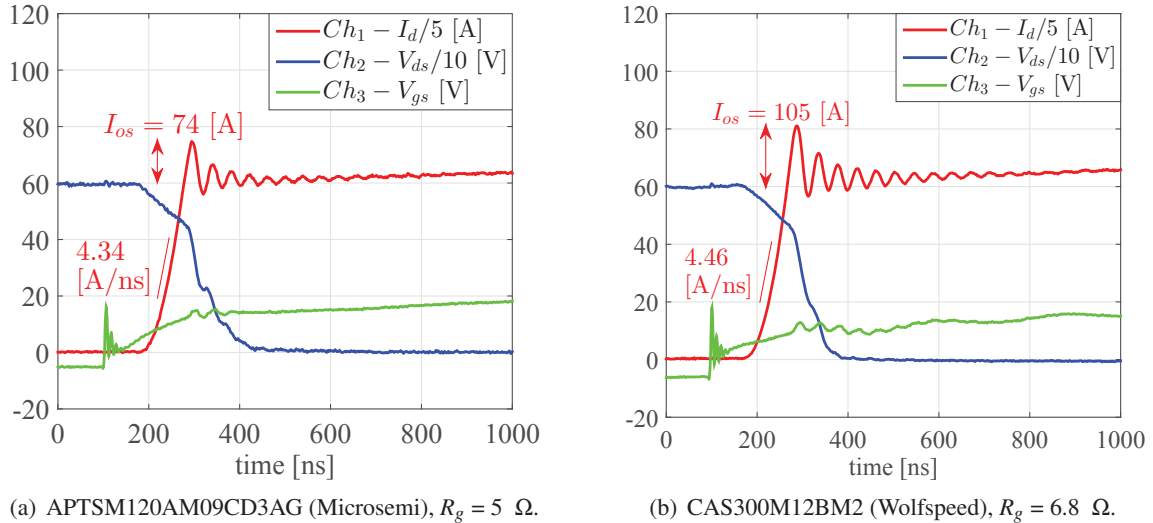


Fig. 9: Turn-on transients of two modules at similar di/dt during turn-on.

Thus, the simulations and experimental results show that the parasitic components of power MOSFETs limit their dynamic performances. In addition, using the information provided in the datasheets of devices (under similar operating conditions), their performances can be predicted. For instance, the conduction figure-of-merit (FOM: $R_{dson} \times Q_g$) and switching FOM ($\sqrt{R_{dson} \times Q_{gd}}$ [15]) are smaller by a factor of 2.55 and 1.27 respectively for CAS300M12BM2 with regard to those of APTSM120AM09CD3AG. A smaller FOM indicates better device performance, i.e., lower device loss.

5 Conclusion

SiC devices have lower threshold voltage and switch extremely fast compared to Si devices. Thus, the switching characteristics of these fast devices are influenced more by both the internal parasitic components and external layouts, and are investigated for two state-of-the-art SiC modules in this paper. The major conclusions from this work are:

- Simulations with varying parasitic capacitances reveal that higher the values, slower the device switches, and are not desirable from an efficiency point of view, particularly for hard-switching applications.
- A closer look into gate waveforms while varying gate-source capacitance show that higher values reduce ringings and maintain the gate loop stability. Conversely, higher gate-drain capacitance together with fast dv/dt can cause unwanted turn-on of the device owing to the fact that dv/dt related noise exceeds the threshold voltage limit of the SiC MOSFET. Overall, it is apparent that not only gate-drain capacitance but the ratio of gate-source to gate-drain capacitance is responsible for the malfunction of the device, and this ratio should be kept high to avoid it.
- Both the simulation and laboratory results illuminate that higher stray parameters hinder utilization of the fast switching potential of SiC power modules, i.e., these parasitics slow down SiC devices, stress them with higher current and voltage overshoots, and higher losses.
- In particular, the comparison of SiC MOSFET modules against each other and the parametric study presented in this work can be utilized to anticipate the relative performance differences between the devices with same or different voltage ratings. Eventually, this provides a guideline to choose an appropriate SiC module.

References

- [1] Y. Shen, J. Jiang, Y. Xiong, Y. Deng, X. He and Z. Zeng, "Parasitic Inductance Effects on the Switching Loss Measurement of Power Semiconductor Devices," 2006 IEEE International Symposium on Industrial Electronics, Montreal, Que., 2006, pp. 847-852.
- [2] J. B. Witcher, "Methodology for Switching Characterization of Power Devices and Modules," Master thesis of Science In Electrical Engineering, Virginia Polytechnic Institute and State University, USA, January 2002.
- [3] Z. Chen, D. Boroyevich and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," The 2010 International Power Electronics Conference - ECCE ASIA -, Sapporo, 2010, pp. 164-169.
- [4] S. Tiwari, O. M. Midtgård and T. M. Undeland, "Experimental performance evaluation of two commercially available, 1.2 kV half-bridge SiC MOSFET modules," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1106-1111.
- [5] Z. Miao, Y. Mao, K. Ngo and W. Kim, "Package influence on the simulated performance of 1.2 kV SiC modules," 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, 2015, pp. 306-311.
- [6] S. Tiwari, O. M. Midtgård and T. M. Undeland, "Design of low inductive busbar for fast switching SiC modules verified by 3D FEM calculations and laboratory measurements," 2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL), Trondheim, 2016, pp. 1-8.
- [7] M. C. Caponet, F. Profumo, R. W. De Doncker and A. Tenconi, "Low stray inductance bus bar design and construction for good EMC performance in power electronic circuits," in IEEE Transactions on Power Electronics, vol. 17, no. 2, pp. 225-231, Mar 2002.
- [8] R. Bayerer and D. Domes, "Power circuit design for clean switching," in Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on, 2010, pp. 1-6.
- [9] J. Wang, H. S. h. Chung and R. T. h. Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," in IEEE Transactions on Power Electronics, vol. 28, no. 1, pp. 573-590, Jan. 2013.
- [10] "SiC MOSFET Isolated Gate Driver," App. Note, CPWR-AN10 Rev. C, Cree, Inc., Durham, NC 27703, 2014.
- [11] "CAS300M12BM2 Datasheet," Cree, Inc., 2014.
- [12] "ATPSM120AM09CD3AG Datasheet," Microsemi, Inc., 2015.
- [13] "CPM2-1200-0040B Datasheet," Wolfspeed, Inc., 2016.
- [14] "CPM2-1700-0045B Datasheet," Wolfspeed, Inc., 2016.
- [15] A. Q. Huang, "New unipolar switching power device figures of merit," in IEEE Electron Device Letters, vol. 25, no. 5, pp. 298-301, May 2004.