Hard and Soft Switching Losses of a SiC MOSFET Module under Realistic Topology and Loading Conditions

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Keywords

≪Silicon Carbide≫, ≪MOSFET≫, ≪Hard switching≫, ≪Soft switching≫, ≪Resonant converter≫, ≪Switching losses≫.

Abstract

This paper investigates the switching performance of a 1.2 kV half-bridge SiC MOSFET module from Sanrex. Unlike in a standard SiC MOSFET module, where the MOSFET and the anti-parallel diode chips are fabricated separately, in the chosen MOSFET module (FCA150XB120), both the MOSFET and the diode are fabricated on a single chip. The device is characterized under both hard and soft switching conditions. For the hard switching characterization, an inductive clamped buck converter is employed, whereas for the soft switching characterization, a resonant half-bridge converter with LC load is used. A comparison of the hard switching loss is performed with the soft switching loss at the same current. This comparison provides insight into the significance of employing an appropriate circuit topology, load and control scheme to reflect the waveforms as in a real application, in order to get a more accurate assessment of the switching losses that will occur. This insight is the main contribution of this paper.

1 Introduction

A superior material performance of SiC over Si enabled the development of high voltage devices even in unipolar technology [1, 2]. SiC MOSFETs are commercially available in the voltage range from 900 V to 1700 V in both discrete form and modules. Newer generation devices are available with some improvements in the older ones. Therefore, before using these devices in an application, it is essential to study their switching and loss performances in detail.

In this paper a 1.2 kV half-bridge SiC MOSFET module, FCA150XB120 from Sanrex [3] is chosen and is characterized under both hard and soft switching conditions. This is a prototype device and has different packaging than a standard commercial module. It has a MOSFET and an anti-parallel diode integrated on a single chip, while in the standard commercial SiC MOSFET module, they are on separate chips. Since the MOSFET and diode are integrated on a single chip, this device is also called DioMOS [4].

In a typical datasheet of a switching device, only the hard switching losses are provided at a certain gate voltage, gate resistance and drain voltage [3, 5, 6, 7]. Furthermore, device manufacturers do not provide information about the switching loop stray inductance and the severity of oscillations during the transients. Higher stray inductance slows down SiC devices, stresses them with higher current and voltage

overshoots, and higher losses [8]. Therefore, it is crucial to make measurements in a real application circuit to acquire a more accurate data for losses.

Besides, the soft switching losses are not included in the datasheet. When the converter switches at very high frequency, these losses are significant; so, it is very important to quantify them in the design phase. The performance of power devices should be evaluated under operating conditions closely resembling those in an actual application in order to obtain realistic data. That is, the circuit topology should be selected such that it incorporates all the possible parasitics in the switching and driver control loops. For instance, a half-bridge configuration is preferred over a chopper as the former accounts all the parasitics. In addition, this will represent most of the converter applications. Moreover, the gate control and the load should be chosen such that the waveforms look as in the real application circuit.

For the measurement of hard switching loss, a widely accepted methodology is a double pulse test in a buck converter with an inductive clamped load which has been used and explained in many publications such as [9, 10]. In this topology, the switch current remains nearly constant over a switching cycle. In the literature, one can find hard switching topologies used for assessment of soft switching loss [11]. Likewise, the soft switching losses of a converter are often calculated using the input from datasheet, which is actually meant for the hard switching case, for example, the characteristic curve of turn-off energy loss as a function of the switching current is used in [12]. Furthermore, a resonant converter is employed with an inductive load in [13] and an LC load in [14]. In the former case, with the inductive load, the switch current has triangular shape, whereas in the latter one with the LC load, the switch current has sinusoidal shape. In a resonant converter, the shape of output voltage and current are square and sine wave respectively, thus in this paper, a resonant converter with the LC load is employed.

The paper is organized as follows. The description of the device under test (DUT) is presented in Section 2. Following this is the comparison of hard switching versus soft switching in Section 3, which covers differences in circuit topology, output waveforms, significance of low inductive busbar, and measuring probe and oscilloscope in separate subsections. The last subsection focuses on the importance of maintaining the probe accuracies; namely, bandwidth and de-skew. It also discusses possible post-processing errors. Section 4 demonstrates the significance of topology through laboratory measurements, which compares the switching losses at different load currents obtained from the two topologies. Finally, Section 5 presents the most important conclusions.

2 Device under test

The concept of SiC DioMOS was proposed in 2011 [4]. Later this device was improved to meet more practical standards for high power switching devices, such as high threshold voltage (V_{gsth}), low on-state resistance (R_{dson}), and low forward voltage drop (V_{FO}) of the channel diode [15]. Table I shows the major differences between the selected SiC module and the standard SiC module (CAS120M12BM2) taken from the manufacturer datasheet [3, 5]. There are three number of chips in FCA150XB120 and six number of chips in CAS120M12BM2. It should be noted that the former has higher V_{gsth} compared to the latter and was realized by making larger SiC depletion capacitance [15]. This is preferable from an application point of view because higher V_{gsth} provides large noise margin enabling stable switching operation.

Table I: Major differences between a 1.2 kV SiC DioMOS and a 1.2 kV standard SiC MOSFET module.

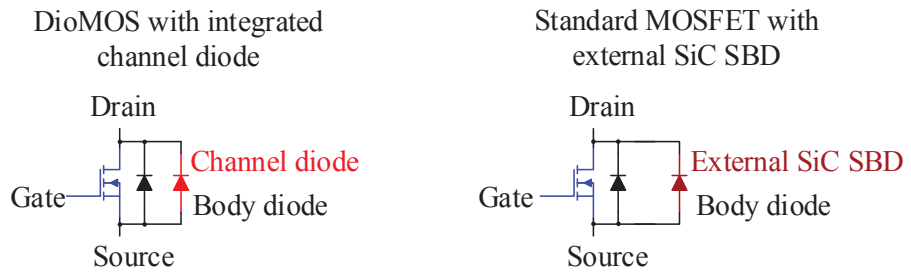
Parameters / Module	DioMOS FCA150XB120, Sanrex	Standard SiC MOSFET CAS120M12BM2, Wolfspeed
No. of chips $\times$ ($m\Omega$)	3×18	6×80
V_{gsth} (V)	4.5	2.6
R_{dson} ($m\Omega$)	5.3 @ I_{ds} = 150 A, V_{gs} = 20 V	13 @ I_{ds} = 120 A, V_{gs} = 20 V
Bonding	Solder	Wire
Package size	$30 \times 93 \times 14$	$62 \times 106 \times 30$

(a) DioMOS module. (b) Standard SiC MOSFET module.

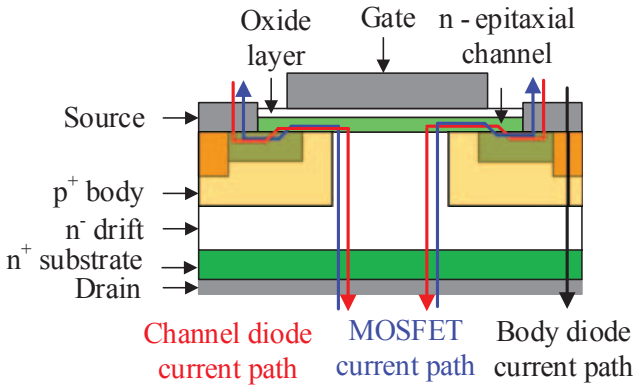
Fig. 1: Photographs of DioMOS and standard SiC MOSFET modules.

Besides, the package size of the former module is smaller than that of the latter module because the external anti-parallel diode chip paired with the MOSFET chip is not necessary [4]. This is essentially due to the fact that the channel diode in DioMOS functions almost similar to SiC SBD. In addition, this will lead to less wiring inductances and eventually higher switching speed in the former device. Fig. 1 shows photographs of the DioMOS and the standard SiC MOSFET modules. The former uses solder bonding technique while the latter uses wire bonding technique.

Fig. 2 a) shows the circuit symbols for DioMOS versus standard SiC MOSFET and Fig. 2 b) illustrates the device cross-section of SiC DioMOS [15]. Compared to the standard vertical power MOSFET, the device structure is mostly similar in DioMOS, the only difference is that the latter consists of an ultrathin and highly doped n - type epitaxial layer and highly doped p^+ - body region. Different possible current paths are shown in Fig. 2 b) where the arrows in blue, red and black colours correspond to MOSFET, channel diode and body diode current paths respectively. The current paths in the DioMOS, namely the MOSFET and body diode current paths, are exactly identical to those in the standard power MOSFET. However, there is an additional current path in the DioMOS which flows through the channel diode.



(a) DioMOS with an integrated channel diode and standard MOSFET with an external SiC SBD. Channel diode of SiC DioMOS functions almost similar to external SiC SBD.



(b) A cross-sectional view of SiC DioMOS with the thin channel layer. It has higher doping concentration of the channel layer and the body region to those of standard SiC MOSFET.

Fig. 2: a) Circuit symbols showing DioMOS versus standard SiC MOSFET. b) A cross-sectional view of SiC DioMOS showing the current paths through MOSFET, channel diode and body diode.

R_{dson} of FCA150XB120 is 5.3 $m\Omega$ at 25 °C and 6.3 $m\Omega$ at 125 °C, i.e., the increase in R_{dson} is smaller compared to that of the typical Si MOSFET. This is caused by the opposite temperature coefficients exhibited by different layers: the channel layer with negative while the combination of drift, JFET and substrate layers with positive, resulting in small positive increase of R_{dson}. It is worth mentioning that in some of the initial publications the overall R_{dson} was shown to be slightly negative up to certain junction temperatures [2, 14, 16] and is mainly due to dominating coefficient of the channel part, while in the latter publications these opposite coefficients were balanced such that the cumulative result gives positive temperature dependence [17]. This is a must for paralleling of devices.

Furthermore, the chip size of FCA150XB120 is larger compared to CAS120M12BM2 resulting in lower conduction loss in the former compared to the latter. Hard switching measurements were performed at similar dv/dt during turn-off for each of these devices and the switching loss was found to be lower in the former module (1.01 mJ) by 13 % compared with the latter module (1.17 mJ). However, di/dt during turn-off was measured to be lower (4 A/ns) in the former compared with the latter (5.4 A/ns), which is primarily because of the larger chip area in the former module giving larger capacitances. It should be noted that while comparing the switching loss, the following parameters were kept equal: gate voltage (+ 20 V and - 5 V), drain voltage (600 V) and drain current (120 A). Similar dv/dt was obtained by adjusting the gate resistance in each module.

3 Hard switching versus soft switching

The differences between the hard switching and the soft switching topologies, the output waveforms, the significance of stray inductance in the switching loops and the accuracy required in measuring probes and oscilloscope are discussed in this section.

3.1 Circuit topology

An appropriate circuit topology, load and control scheme is necessary in order to generate the waveforms as in a real application circuit. Fig. 3 shows a half-bridge circuit in a chopper/buck configuration with an inductive clamped load for measuring hard switching losses. With the inductive load, the current stays nearly constant over a switching cycle. That is, the first turn-off and second turn-on switching transients are at similar current levels which are the key points of interest and are indicated in Fig. 5 a). The details on the measurement procedure is described in [9, 10]. The upper transistor (T1) is always turned off by applying - 5 V in the gate-source while double pulses are given in the lower transistor (T2) which is also the DUT.

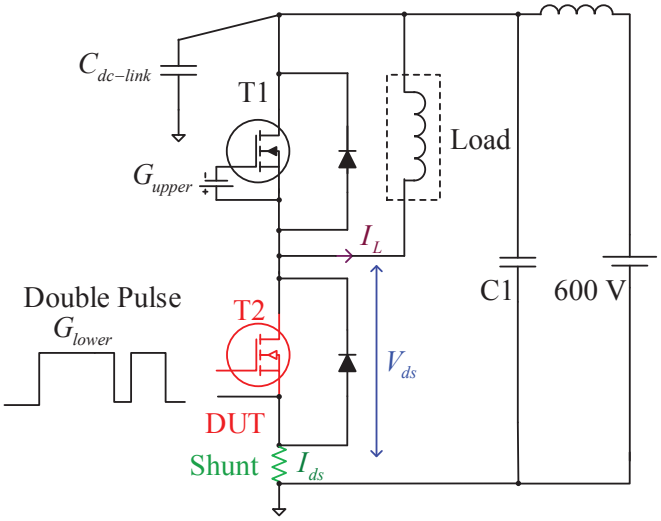


Fig. 3: Circuit diagram for hard switching loss measurement with an inductive clamped load.

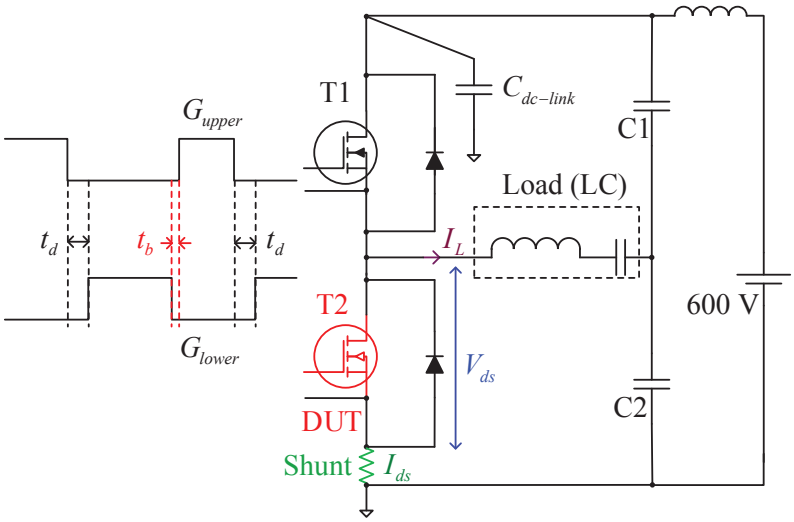
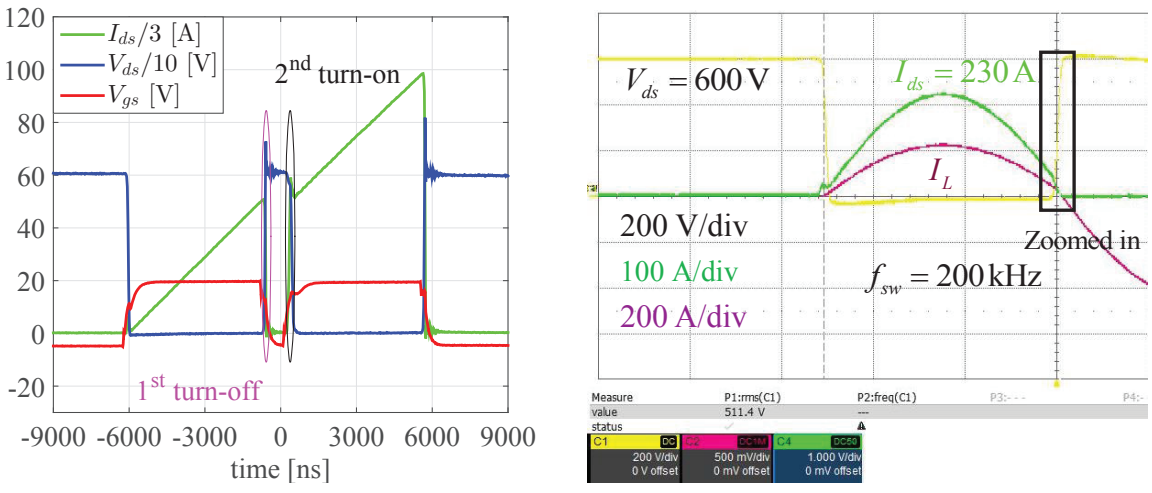


Fig. 4: Circuit diagram for soft switching loss measurement with an LC load and split dc-link capacitors.

Fig. 4 shows a half-bridge resonant circuit with the LC load and split dc-link capacitors for measuring soft switching losses. The upper transistor (T1) is always in on-state except the period where the lower transistor (T2) is in on-state, including some blanking time (t_b) and delay time (t_d). t_b refers to the time interval between the turn-off and turn-on switching of the transistors of the same leg. By adjusting t_b, the switching current can be varied according to the value of interest. The remaining abbreviations used in Fig. 4 are as follows. G_{upper} and G_{lower}: upper and lower gate pulses respectively, $C_{dc-link}$: dc-link capacitor, V_{ds}: drain-source voltage, and I_{ds} and I_L: drain-source and load currents respectively.

3.2 Output waveforms



(a) Waveforms in a hard switching converter.

(b) Waveforms in a soft switching converter.

Fig. 5: Measured waveforms in a hard and a soft switching converter. In the former converter, switching takes place at high current and voltage, whereas that in the latter takes place at low voltage and current. Switching instances, namely first turn-off and second turn-on, are indicated by ellipses in Fig. a), while that is shown by a rectangle in Fig. b).

A sample of a hard switching and a soft switching waveforms at a dc-link voltage of 600 V are depicted in Fig. 5 a) and Fig. 5 b) respectively. For the hard switching, the sample waveform has a current of 150 A, and it is 230 A peak for the soft switching. In a series resonant converter, the output voltage has a square wave and output current has a sine wave pattern as shown in Fig. 5 b) replicating the waveforms as in the real application circuit. In order to achieve higher current, load capacitance (C) was increased

or load inductance (L) was decreased and vice versa, while to acquire a required switching frequency (f_{sw}) the load was adjusted as given by Equation 1.

$$f_{sw} = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

3.3 Significance of low inductive busbar

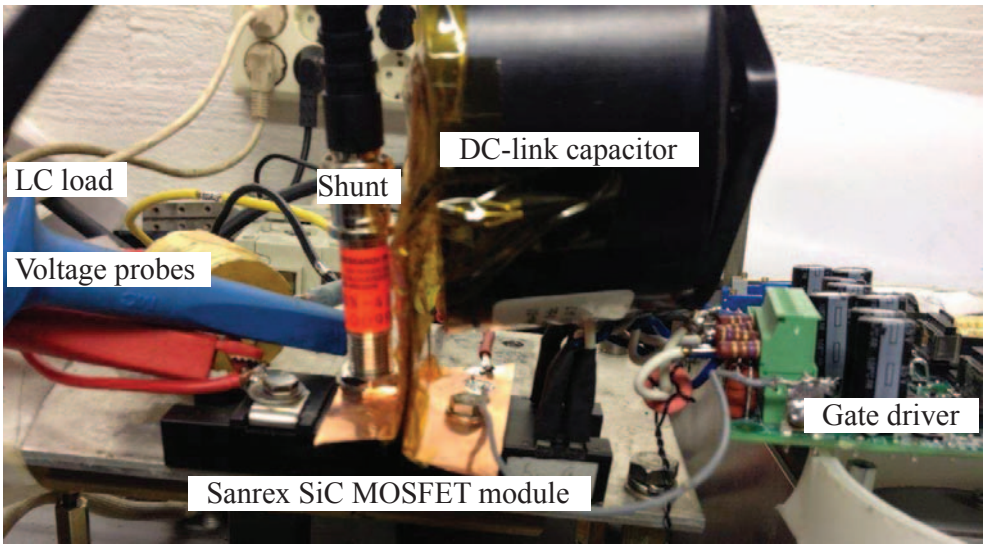


Fig. 6: Laboratory setup with low inductive dc-link. The drain current is measured by a high bandwidth, low inductive shunt, and the drain voltage is measured by a high bandwidth differential probe.

In a hard switched converter, the switching takes place at maximum current and voltage unlike in a soft switched converter where the switching is performed at minimum current and voltage or zero current and zero voltage. Therefore, in the former converter, it is indispensable to maintain the low parasitics in power and gate loop during both the normal operation and short circuit conditions. On the other hand, in the latter converter, during the normal operating conditions, there is no significance of having low stray inductance in the switching loop as the device switches with small di/dt. However, during the short circuit conditions, the current is very high and so is the di/dt. The high di/dt combined with switching loop stray inductance cause high voltage overshoot and ringing resulting in EMI and possible device failure. Hence, it is advisable to maintain lower loop inductances even in a resonant converter.

Thus, in both soft and hard switching cases, the low inductive dc-link connection to the module is adopted. A dc-link is realized with a planar busbar except the termination parts (needed to facilitate the module connection) so that the stray inductance in the switching loop can be kept as low as possible. A current viewing resistor (CVR, also called a shunt resistor) SSDN-414-01 (400 MHz, 10 $m\Omega$) from T & M research [18] is used for measuring the drain current. The CVR replaces one of the screws in the SiC module as it is mounted directly on the screw terminal. The picture illustrating the placement of the CVR in the laboratory setup is shown in Fig. 6. The details of the low inductive measurement setup are described in [19].

3.4 Measuring probe and oscilloscope

3.4.1 Bandwidth

In the datasheet of the chosen device under test (Sanrex SiC MOSFET module), the rise (t_{rise}) and fall times (t_{fall}) of the switching transients are 40 ns and 35 ns respectively. This was for the case with gate resistance (R_g) of 2.5 Ω and V_{gs} of + 20 V / - 5 V [3]. Additionally, the measurements are performed with R_g of 0 Ω and similar gate voltage as in datasheet, which resulted in t_{rise} and t_{fall} in the range of 20 ns. Furthermore, the ringing frequency (f_{osc}) is 30 MHz, as indicated in Fig. 7. Table II shows the bandwidth and rise time of the selected probe and oscilloscope for the measurements.

Table II: Bandwidth and rise time of selected probes and oscilloscope.

Equipments	BW (MHz)	t_{rise} (ns)
Voltage probe (THDPO200, Tektronix)	200	1.8
Current shunt (SSDN - 414 - 01, 10 $m\Omega$, T & M Research)	400	1
Oscilloscope (DPO5104, Tektronix)	1000	0.3

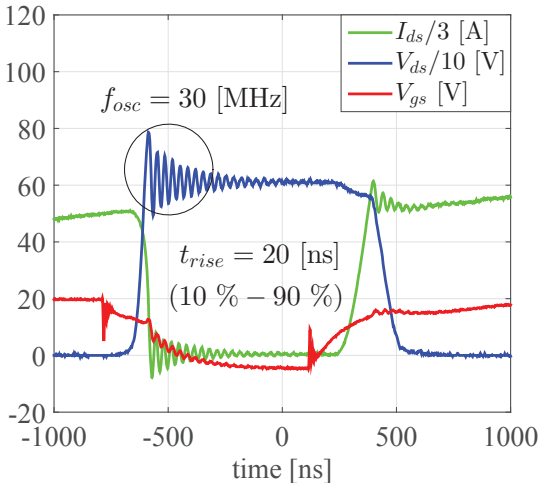


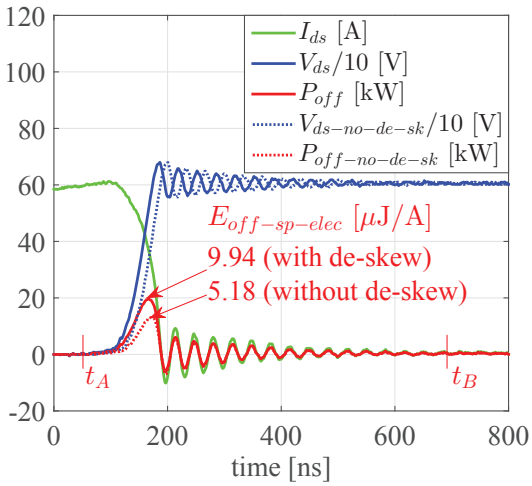
Fig. 7: Zoomed in waveform of Fig. 5 a) to show that the selected probes and oscilloscope are adequate for measuring the switching transients of Sanrex SiC module.

In order to capture the fast rising and falling current and voltage waveforms, the probe and oscilloscope should have adequate bandwidth (BW) or t_{rise}/t_{fall}. If not, the harmonics which are above the cut-off frequency of probe will be filtered out and the measured di/dt and dv/dt will be lower than the real slopes leading to wrong results. In [20], it is recommended to have five times greater BW of the probe and oscilloscope compared to the frequency of the waveform being measured. Since f_{osc} is 30 MHz for Sanrex module, the BW needed is 5 $\times$ 30 = 150 MHz. Moreover, it is also suggested that for accurately tracking t_{rise} and t_{fall} of the waveform, the BW of equipment should satisfy the relation given by Equation 2. Based on these calculations, the chosen equipments prove to be good enough to track the transient waveforms of the selected device.

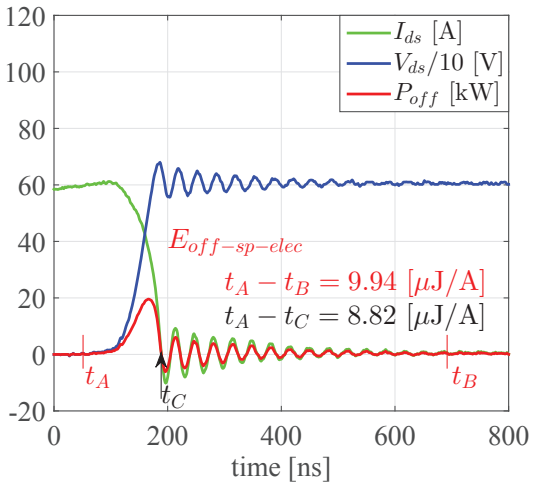
$$BW = 5 \cdot \frac{0.35}{t_{rise}} = 5 \cdot \frac{0.35}{20} = 87.5 \text{ MHz} \tag{2}$$

3.4.2 De-skew

Generally, the datasheet of voltage probe provides information about probe delay which is 14 ns for the selected probe. In order to analyse the influence of the probe delay on the accuracy of measurement, the voltage waveform is de-skewed, i.e., subtracted the probe delay from the originally measured voltage waveform as shown in Fig. 8 a). The originally measured voltage waveform is in dotted blue and the one with de-skewed is indicated by solid blue. As the current waveform is measured by shunt resistor, there is no need to de-skew the current waveform. Thereafter, the current and voltage waveforms are multiplied to obtain the power loss indicated by dotted red for the original and the solid red for the de-skewed. Then, the switching energy loss is calculated for the case with and without probe de-skew. With the former, the specific energy loss ($E_{off-sp-elec}$) is computed to be 9.94 μJ/A, whereas the same with the latter is calculated to be 5.18 μJ/A; lower by a factor of 1.91.



(a) Turn-off transient with and without probe de-skew.



(b) Turn-off transient with different integration time.

Fig. 8: Turn-off transients during hard switching together with the power waveforms. Fig. a) illustrates the influence of probe delay. With 14 ns of voltage probe delay with respect to current measured by shunt, there is significant difference in the computed energy loss. Fig. b) illustrates the influence of integration limits on the power curve. As there is oscillations, the choice of the end of the integration time is not clear. t_A denotes the start of the integration time, while t_B and t_C are two options to select the end of the integration time.

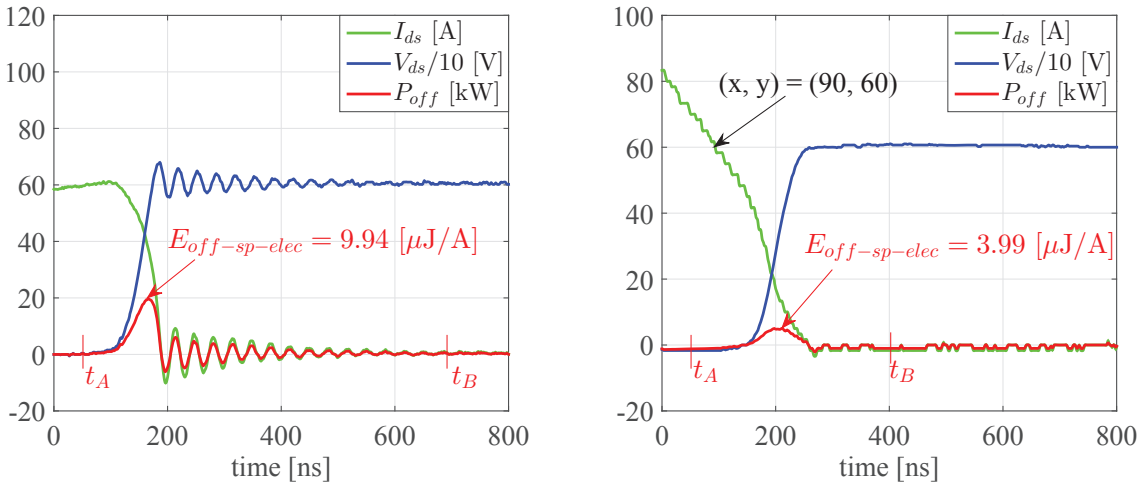
3.4.3 Post processing of measured waveforms

The selection of proper time interval is crucial for integrating the measured power in order to extract the correct switching energy loss, an example of which is illustrated in Fig. 8 b). Both current and voltage waveforms exhibit oscillations at the end of each switching transients and so does the power curves possess. There are two possible integration time limits, first is the initial zero crossing of power curve, indicated by t_C, second is t_B, where the low and high frequency oscillations have decayed. While integrating the power waveform from t_A to t_B, $E_{off-sp-elec}$ is computed to be 9.94 μJ/A, whereas while integrating the power waveform from t_A to t_C, the same is computed to be 8.82 μJ/A; lower by 11.26 %. In this work, the former integration limit where all the oscillations are decayed is considered.

4 Significance of topology through laboratory measurement

As mentioned in the earlier section, the appropriate circuit topology is vital while measuring the switching losses, otherwise, it can give a big difference in losses leading to a wrong sizing of the heatsink and limiting the power of the converter. Fig. 9 shows the example waveforms illustrating the difference between the hard switching and the soft switching. For a fair comparison, these waveforms are recorded at the same load currents (60 A), R_g (2.85 Ω) and V_{gs} (+ 20 V, - 5 V). It is clearly visible that the hard switching waveforms have higher dv/dt, di/dt and ringing compared to the same for the soft switching. In addition, the loss in the former topology is about 2.5 times higher with regard to the loss in the latter.

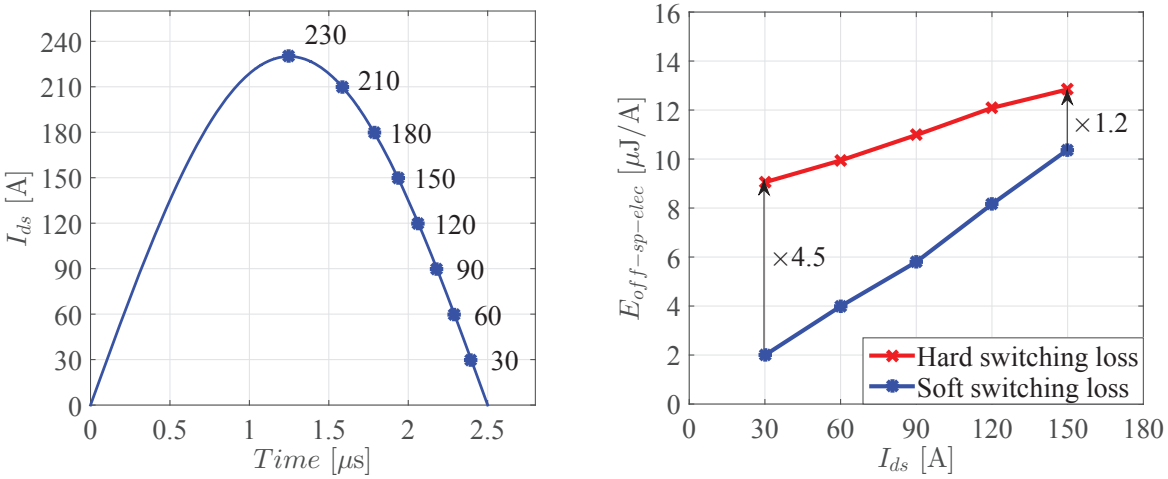
In order to obtain a full overview of switching losses at different current levels, the measurements are repeated and the specific switching energy loss versus load current is plotted in Fig. 10 b). It should be pointed out that the turn-off current for the hard switching case is defined according to the well known double pulse test methodology, where the first turn-off instant is recorded as shown in the previous section by Fig. 5 a). Fig. 10 a) illustrates the definition of turn-off current for the soft switching case where the peak value of load current is fixed at 230 A and the turn-off instants are varied (by adjusting the blanking time) to obtain the current of interest. Furthermore, the switching frequency is set to 200 kHz according to the requirement of application.



(a) Turn-off transient during hard switching.

(b) Turn-off transient during soft switching.

Fig. 9: Illustration of turn-off transients during hard and soft switching conditions at the same load current. Hard switching waveforms have higher dv/dt and di/dt compared to soft switching ones. Besides, the former exhibit oscillations while they are absent in the latter.



(a) Definition of turn-off current during soft switching.

(b) Comparison of the hard and soft switching loss.

Fig. 10: a) Illustration of the turn-off current during soft switching case. The peak value of load current is set at 230 A and the turn-off instants are varied. b) Comparison of the switching loss between the hard and soft switching. Hard switching losses are higher by a factor of 1.2 (150 A) to 4.5 (30 A) depending on the load current.

Measurements show that the hard switching losses are higher by a factor of 1.2 (at I_{ds} of 150 A) to 4.5 (at I_{ds} of 30 A) compared to the soft switching losses, depending on the load current. It should be noted that these losses are plotted for the same driving conditions: same R_g and V_{gs}. Thus, using the hard switching loss for designing the thermal management and estimating the power rating of the soft switching converter leads to significant error as the turn-off switching in the latter takes place at minimum possible current (lower current regions). The difference in losses between the hard and soft switching is more visible towards lower currents than the higher ones, which is mainly because of two reasons. First, at lower current, there is lower dv/dt which causes the output capacitance of MOSFET work better as turn-off snubber compared to higher current. Second, the MOSFET channel is closed for current earlier in the turn-off process with lower dv/dt.

5 Conclusion

The device under test is a prototype device, and therefore only the preliminary datasheet is available. Characterizing the device with an appropriate topology, load and control scheme reflects the waveforms that will occur in a real application circuit, resulting in more accurate assessment of loss. The measured turn-off loss during soft switching is significantly lower compared to the one during hard switching. The turn-off loss during hard switching is higher by a factor of 1.2 (150 A) to 4.5 (30 A) depending on the drain current. As the turn-off in a soft switched converter is aimed towards the lower current region, estimating loss using measurements from hard switched topology leads to much higher errors. Thus, a correct assessment of loss is important, for example, when increasing the power rating of a converter and for thermal design. Additionally, SiC MOSFETs switch very fast, and therefore, loss measurements demand high accuracy of probes and oscilloscopes as well as considerations of all possible errors. Thus, for an accurate evaluation of loss, the adequate bandwidth required for the probes and oscilloscope, adjustments of probe de-skew and possible post-processing errors are considered in this paper.

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