

Growth and Characterization of Silicon Nanowires for Solar Cell Applications

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Declaration

I declare that this work has been performed independently and in accordance with the rules and regulations for examinations at the Norwegian University of Science and Technology, NTNU.

Kai Erik Ekstrøm, Trondheim, July 03, 2011.

Preface

The following master's thesis covers work performed on silicon nanowires during my final specialization in Material Chemistry and Energy Technology, and was provided by the Institute of Materials Science at the Norwegian University of Science and Technology (NTNU) in cooperation with SINTEF Materials and Chemistry as a part of my M.Sc. degree in Industrial Chemistry and Biotechnology.

This work was carried out during spring 2011 as a continuation of the specialization project performed on silicon nanowires during fall 2010. SINTEF Materials and Chemistry provided me with my two supervisors, Senior Researcher Eivind Øvrelid and Research Scientist Øystein Dahl, to whom I want to express my highest appreciation and gratitude. I want to thank them for giving me the opportunity to study and be a part of this new and exciting subject, and for the support and inspiration during long working hours.

Special gratitude also goes to Research Scientist Per Erik Vullum for performing the TEM analysis, Sectional Engineer Espen Rogstad and Chief Engineer Søren Heinze at NTNU Nanolab for all the help given during apparatus and process difficulties.

Last (but not least) I would also like to thank my dear friend Cecilie Sneberg Grøtteland for the time spent proofreading.

Abstract

Si-nanowires are being introduced as an attempt to decrease the high recombination rate present in silicon based thin-film solar cells by employing radial pn-junctions instead of conventional planar pn-junctions. Previous publications have also shown an additional increase in the amount of absorbed light when covering a silicon-substrate in silicon nanowires which may result in a further increase in the total efficiency of a thin-film solar cell.

Successful growth of Si-nanowires has earlier been performed by Chemical Vapour Deposition (CVD), employing gold (Au) as catalytic material. Au is a very stable catalytic material for nanowire growth but Au-residues are unwanted in solar cell applications, and the current experiment has therefore investigated aluminium (Al) as an alternative catalyst material. However, stable Al-catalysed growth has been proven to be difficult and is assumed to be mainly due to rapid oxidation of Al to Al₂O₃. Most of the nanowires were short, tapered and consisted of worm-like structures. Several unsuccessful in-situ NH₃-based cleaning (CVD) processes were attempted. Tin (Sn) was also attempted as a protective coating for the Al-film in order to protect Al from exposure to air during sample transport, without any luck.

As solar cells require both p-doped and n-doped sections in order to form pn-junctions, initial investigations were performed on the effect from the addition of dopant gases (B₂H₆ and PH₃) on nanowire morphology. The addition of B₂H₆ to the gas flow seemed to have much larger effects than PH₃ on the nanowire morphology compared to intrinsic nanowires. Both gases resulted in a continuous reduction in the average nanowire length with increasing *dopant/SiH*₄ ratios, ultimately leading to a complete inhibition of nanowire growth. The highest usable *dopant/SiH*₄ ratios before complete growth-inhibition were found to ~10⁻³ for B₂H₆ and ~10⁻¹ for PH₃. An undesirable tapering effect was also found when adding B₂H₆ to the gas-flow, resulting in radial growth of amorphous silicon on the nanowire walls already at the lowest dopant ratio (~10⁻⁵). This may complicate the use of B₂H₆ as a dopant gas for p-type nanowires. Ignoring the fact that the addition of PH₃ to the gas-flow reduces the nanowire growth rate PH₃ may be assumed to be a good alternative for n-type doping of nanowires as no further effects on the nanowire morphology is observed.

The actual implementation of dopant atoms into the nanowire structure may be determined by measuring the electrical resistivity in the nanowire, and a possible four-contact structure has been designed and partly optimized for this purpose. The contact structure has been designed in three layers where two of them are produced by photolithography while the smallest layer by electron-beam-lithography. Note that the structure has not been finalized because of time limitations. Some optimization of the four nanowire contacts remains as some final lift-off problems appeared, and is assumed to be related to either an incomplete development of the smallest features or an observed resist-bubbling because of high Titanium (Ti) deposition temperature. However, a robust three-point alignment procedure has been investigated and found useful for producing accurate contacts to single nanowires and leads to the conclusion of a promising structure.

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Symbols and Abbreviations

$D_{n/p}$:	Diffusion coefficient of electrons / holes [cm ² /s].
d_{top} :	Diameter on the upper part of the nanowire [cm].
d_{bottom} :	Diameter on the bottom part of the nanowire [cm].
e:	Electron charge [C].
E:	Energy level [eV].
E_c/E_v :	Energy level of conduction/valence band [eV].
E_F :	Fermi level [eV].
E_F^0 :	Standard electrode potential [V].
f_c :	Collection probability.
f(E):	Fermi-Dirac distribution function.
I/I_{AD} :	Current/Current between pt. A and pt. D [A].
$J_{n/p}$:	Current of electrons / holes $[A/cm^2]$.
k:	Boltzmann's constant [eV/K].
l_2 :	Length between inner contacts [cm].
$L_{n/p}$:	Carrier lifetime [s].
L_{nw} :	Nanowire length [cm].
m_n^*/m_p^* :	Effective mass of electron/hole [kg].
n:	Electron-concentration [cm ⁻³].
n_i :	Intrinsic electron concentration $[cm^{-3}]$.
N _A :	Concentration of dopant acceptors [cm ⁻³].
N_D :	Concentration of dopant donors [cm ⁻³].
p:	Hole-concentration [cm ⁻³].
p_{tot} :	Total pressure [Torr].
p_{SiH4} :	SiH ₄ partial pressure [Torr].
q:	Elementary charge [C].
$q\Phi_m/q\Phi_s$:	Work function potential for metal/semiconductor [eV].
<i>q</i> \cears 2:	Electron affinity [eV].
$R/R_C/R_{nw}$:	Resistance/Contact resistance/Nanowire resistance [Ω].
R_{tot} :	Total resistance $[\Omega]$.
<i>r</i> :	Radius [cm].
$r_{tapering}$:	Nanowire tapering ratio.
r _{dopant} /r _{SiH4} :	Dopant-to-SiH ₄ flow rate.
r_{B2H6}/r_{SiH4} :	B ₂ H ₆ -to-SiH ₄ flow rate.
r _{PH3} /r _{SiH4} :	PH ₃ -to-SiH ₄ flow rate.
T:	Temperature [K/°C].
V/V_{BC} :	Voltage/Voltage difference between pt. B and pt. C [V].
V_0 :	Contact potential [V].
<i>W</i> :	Width of depletion region [cm].
$W_{n/p}$:	Penetration with in the n-side / p-side [cm].

$\epsilon/\epsilon_r/\epsilon_0$:Permittivity, relative permittivity, permittivity of free μ_n/μ_p :Mobility of electron/hole [m²/Vs].	
σ : Conductivity [S/m].	
σ_l : Surface tension of a liquid surface [J/m ²].	
σ_s : Surface tension of a solid surface [J/m ²].	
σ_{ls} : Liquid-solid interfacial tension [J/m ²].	
ρ_{nw} : Resistivity of nanowire [Ω -cm].	
τ : Scattering time [s].	
$\tau_{n/p}$: Lifetime of electron / hole [s].	
Al: Aluminium.	
Ar: Argon.	
Au: Gold.	
a-Si: Amorphous silicon.	
B ₂ H ₆ : Diborane.	
c-Si: Crystalline silicon.	
CVD: Chemical Vapour Deposition.	
I-V: Current-Voltage curve.	
H ₂ : Hydrogen.	
LAADF STEM: Low-Angle Annular Dark Field Scanning Tunnelling	g Electron
Microscopy.	
PECVD: Plasma Enhanced Chemical Vapour Deposition.	
PH ₃ : Phosphine.	
SEM: Scanning Electron Microscopy.	
Si: Silicon.	
SiH ₄ : Silane.	
Si-nanowire: Silicon nanowire.	
STEM: Scanning Tunnelling Electron Microscopy.	
TEM: Transmission Electron Microscopy.	
TMB: Trimethylboron.	
VLS: Vapour–Liquid–Solid.	
VSS: Vapour-Solid-Solid.	

1 Introduction

The power consumption on the planet is steadily increasing and because of a limited availability of fossil fuels in combination with a growing awareness on global warming we depend on finding new and preferably renewable energy sources.

Harvesting of solar energy has been promoted as a good and clean alternative for a long time but not without challenges. The price paid per kWh is still too high and it currently cannot match the price for fossil fuels which makes it highly unattractive for the average consumer. Much of today's research therefore focuses on how to reduce the total cost of cell-production and the price paid per kWh in order to make solar energy more competitive to fossil fuels, mainly by increasing the efficiency of the cell.

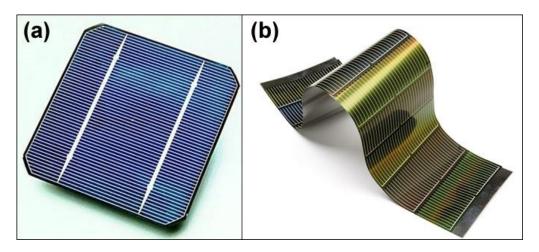


Figure 1.1: A conventional silicon-based solar cell compared to a thin-film solar cell indicating a drastic reduction in thickness (from \sim 250-350 μ m to \sim 1-2 μ m)

A majority of the commercial solar cells available today are based on conventional crystalline silicon (Figure 1.1 (a)). These cells are currently optimized to a thickness of ~250-350 μ m with a conversion-efficiency of approximately 15-20%⁽⁴⁾. The theoretical limit for a conventional crystalline silicon-based solar cell is ~30%⁽⁵⁾. 40-50% of the total cost per finished solar cell module is made up of the amount of silicon-material used in the process, and the potential for cost-reduction is therefore assumed to be large.

Slicing the ingots into thinner wafers causes problems with mechanical handling and large amount of material-losses and a partial solution to this request was the development of the thin-film solar cell (Figure 1.1 (b)).

Thin-film solar cells:

A thin-film solar cell contains only a fraction of the amount of silicon used in a conventional solar cell because of a drastically reduced thickness, but unfortunately such cells suffer from large losses and reduced conversion-efficiency.

Losses may be divided into two main groups; absorption and recombination losses.

i. Absorption losses:

Losses due to incomplete absorption of light increases with reducing cell-thickness; more light goes through thinner cells without absorbing which promotes thicker cells.

ii. Recombination losses:

Losses due to recombination of generated electron-hole pairs. Electrons may diffuse only $\sim 1 \mu m$ in the silicon structure before recombining (for current Si thin-film technology) which leads to high recombination losses for thicker cells.

Because of these opposite effects the currently optimized thickness for a thin-film solar cell has been set to $\sim 2\mu m$ and shows a conversion-efficiency of $\sim 10\%^{(4)}$.

Researchers are currently investigating methods to increase this efficiency by surface modifications, and covering the surface in so-called nanowires is considered to be a promising expansion.

Thin-film solar cells patterned with silicon nanowires:

Better conversion-efficiency for a given cell-thickness will be achieved by reducing either the recombination losses or the absorption losses.

By growing oppositely doped nanowires on a silicon substrate(Figure 1.2 (a)) the necessary pn-junction is retained and in addition the light may now travel and reflect in a forest of nanowires which drastically increases the probability of absorption compared to a clean surface, even compared to a conventional silicon wafer⁽⁶⁾.

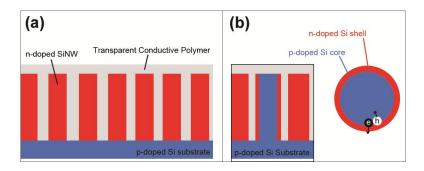


Figure 1.2: Two types of nanowire-usage has mainly been reported in earlier publications; vertical pn-junctions consisting of oppositely doped nanowires than the substrate and radial pn-junctions consisting of two layers of opposite doping.

A further expansion is the introduction of the radial pn-junction (Figure 1.2 (b)) instead of the conventional vertical pn-junction employed in (a).Because of the reduced diameter of this type of pn-junction (~300nm) a reduction in the recombination rate may be expected as the distance the electrons need to travel is reduced to $< 1\mu$ m. Gains in the total solar cell efficiency up to 11% have been reported for diffusion lengths of ~100nm⁽⁷⁾, provided that the trap-density is held to low levels.

A combination of these two modifications may result in a potential low-cost solar cell with a reduced amount of losses compared to more conventional cells which makes this a very interesting alternative for future solar harvesting.

Silicon nanowire growth:

One of the more popular and more investigated methods of growing silicon nanowires is by chemical vapour deposition (CVD). Nanowires grown by CVD employ a vapour-liquid-solid (VLS) growth mechanism where gaseous SiH₄ supplies catalytic droplets with silicon. Gaseous SiH₄ (Si in its vapour phase) added to the chamber diffuses towards and into the liquid catalytic droplets; resulting in supersaturation of the droplets (Si in its liquid phase). In order to re-establish equilibrium concentrations in the liquid droplets excess silicon is crystallised at the liquid-solid interface resulting in axial growth of nanowires (Si in its solid phase). Earlier experiments performed by the author⁽²⁾ (App. G) have employed gold as the catalytic material as it is a very stable material and gives good results. Unfortunately gold will reside both within and on the surface of the nanowires. Gold (Au) is undesirable in solar cells as it is very effective on trapping generated electrons, resulting in a considerable reduction in the cells conversion-efficiency. Aluminium (Al) has shown itself as a capable alternative to gold as it is not very effective on trapping electrons but investigations performed in the current experiments have uncovered other challenges such as oxidation and stability problems.

As solar cells are based on a positively doped p-type region in contact with a negatively doped n-type region the natural next step was to investigate how the addition of dopant gases $(B_2H_6 \text{ and }PH_3)$ influences the nanowire morphology. Because of evident oxidation and stability problems attained for the previous growth with Al as catalytic material this had to be investigated with Au instead. In this case it would also be interesting to investigate the actual implementation of dopant-atoms in the structure, in terms of approximate dopant concentrations and resistivity. This was to be done by four-point electrical measurements of single nanowires but because of time-limitations only a partial measurement-process has been developed.

2 Theory and Literature Review

A basic presentation of silicon nanowires and some of the growth properties will be given in this chapter. More complete theoretical studies of silicon nanowire growth have been done before, and the reader is therefore referred to the earlier reports for more details ^(2, 3). Much of the theory presented here is collected from earlier work and reported literature, and since much of the theory is still in its infancy background literature may be limited in some areas. A morphology study has been reported earlier by the author⁽²⁾ and relevant parts will be summarised in this report for use with new results. The current report is also expanded to cover alternative catalysts to gold and general semiconductor theory needed for exploration of

nanowire doping and electrical measurements.

2.1 Silicon Nanowires

A nanowire may be defined as a nanostructured rodlike crystal or amorphous structure with a diameter of less than 100nm that may attain a length of several micrometres. Structures with larger diameters are often referred to as whiskers. Figure 2.1 shows an illustration (a) and a TEM image (b) of a crystalline silicon nanowire grown on a single-crystal silicon (111) substrate. This report focuses on crystalline nanowires. Crystalline nanowires tend to attain a single-

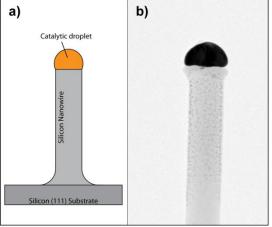


Figure 2.1: (*a*) Illustration of a silicon nanowire. (*b*) TEM image of a silicon nanowire with a solidified catalytic Au-Si particle on top.

crystal silicon structure, and are usually covered in a thin SiO_2 layer resulting from rapid oxidation in air. The droplet on the top of the nanowires is a residue of the catalytic material used for directional growth.

2.2 Growth of Silicon Nanowires

Synthesis of silicon nanowires dates back to the late 1950s⁽³⁾ when R. G. Treuting and S. M. Arnold reported on a successful synthesis of a <111> whisker ⁽⁸⁾ of unknown diameter, and since then several different techniques for nanowire synthesis has been explored⁽³⁾. One of the most successful methods employed for nanowire synthesis is based on Chemical Vapour Deposition (CVD). Nanowires grown by CVD employ a so-called Vapour-Liquid-Solid (VLS) growth mechanism. This mechanism has been the core of silicon nanowire research since Wagner and Ellis⁽⁹⁾ published their proposal in 1964. Since then, a good understanding of the mechanism has been obtained through persistent research, and a good coverage can be found in earlier publications. Previous studies performed by the author mainly covered the general growth mechanism of silicon nanowires and some of its essential properties and variations with growth parameters⁽²⁾. The previous attained knowledge and results has been used as a basis for further exploration of the field and is presented in the current report. A short introduction to the growth mechanism will now be given.

2.2.1 Chemical Vapour Deposition

Chemical Vapour Deposition (CVD) is a process mainly used for deposition of solid thin films on silicon wafer surfaces and other substrates. The substrate is heated to an elevated temperature and exposed to precursor gases which are fed into the reactor. The precursor gases decompose or react with the substrate in production of the desired deposit. The by-products are removed from the reactor through an exhaust. A simplified schematic of a CVD process is illustrated in Figure 2.2.

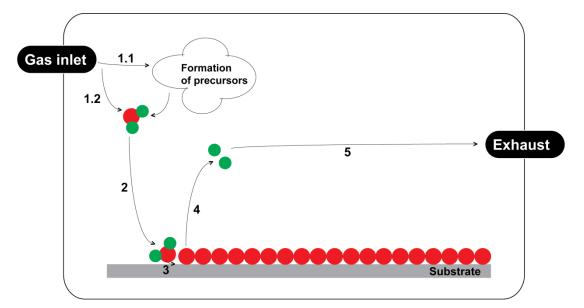


Figure 2.2: A simplified schematic of a CVD process. Precursor gases enters the chamber either directly (1.2) or by gaseous reactions (1.1). Precursor gas molecules diffuse towards the sample surface (2) and adsorbs on the surface (3). The molecule decomposes and releases by-products (4) which are transported out of the chamber (5).

The general steps in a CVD process are summarized as following (Figure 2.2)⁽¹⁰⁾:

- 1) *Precursor formation:* The reactor may be fed with several reactant gases which lead to the formation of the precursor gas through gas-phase reactions (*Step 1.1*), or with the precursor gas directly (*Step 1.2*).
- 2) *Precursor diffusion:* The precursor gas diffuses to the substrate surface (*Step 2*).
- 3) *Film formation:* The precursor molecules adsorb on the substrate surface and the molecules deposit and bond to the rest of the film by surface reactions. The reactions run on energy provided by the heating of the chamber (*Step 3*).
- 4) *By-product desorption:* By-products formed in the previous step desorb from the substrate surface (*Step 4*).
- 5) By product removal: By-products are transported out of the reactor (Step 5).

When used in nanowire growth, the process can be compared and described as a standard CVD process as described over, but the near-surface mechanism described in Figure 2.2 (*Step*

3) differs somewhat from a normal deposition mechanism. This mechanism has been established as the mentioned vapour-liquid-solid (VLS) growth mechanism.

The main difference between the normal film deposition (Figure 2.3 (a)) and nanowire growth (b) mechanism is the necessity of catalytic sites/droplets for the latter. Nanowires will in this case not grow without the presence of catalytic sites as this would favour film growth instead.

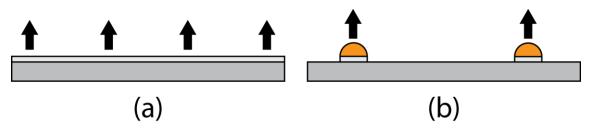


Figure 2.3: In lack of catalytic sites film growth will be favoured (a) but by covering the surface in catalytic droplets the axial growth rate of nanowires will be several magnitudes larger than the growth rate of film resulting in nanowires (b).

2.2.2 Formation of Catalyst Droplets

Catalytic sites or droplets are essential to the Vapour-Liquid-Solid growth mechanism and thus for silicon nanowire growth. A summary of the possible catalytic materials for VLS growth is given in Figure 2.4⁽³⁾, but the most investigated and successful catalytic material is gold and it will therefore serve as the basis for this description.

The melting temperature for pure Au and Si may be found to be 1337K and 1687K

respectively from the Au-Si diagram given in Figure 2.5 (a) ⁽³⁾. By following the liquidus lines one can observe how alloying Au with Si affects the melting point of an Au-Si alloy (The melting point is strongly dependent on the alloy composition and vice versa). In a binary eutectic phase diagram such as for Au-Si, the lowest attainable melting point is at the eutectic point; or the eutectic composition. In the case of

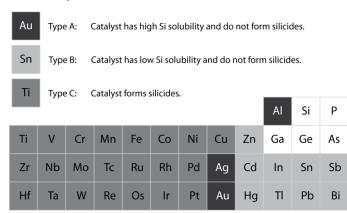


Figure 2.4: Different catalytic materials usable for catalytic nanowire growth as reported by Schmidt et al.⁽³⁾

Au and Si the eutectic composition is given as 18.6 at% Si and 81.4 at% Au which gives an eutectic melting temperature of \sim 636K⁽³⁾. For comparison, the simple binary diagram for Al-Si is given in Figure 2.5 (b) which also shows a prominent reduction in melting temperature by alloying Al with Si (~850K at 12 at% Si and 88 at% Al).

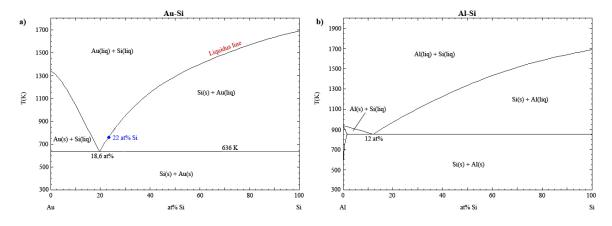


Figure 2.5: The Au-Si phase diagram. The blue dot represents the composition at 500°C and is given by the liquidus line⁽¹⁾ (a). The Al-Si phase diagram for comparison⁽¹⁾ (b).

The main steps in droplet formation are described as following (Figure 2.6):

a) Deposition of catalytic material:

The desired catalytic material (ex. Au) is deposited as a thin-film onto the growth substrate.

b) Material diffusion:

Two materials in contact will start to diffuse into each other. Silicon will start to diffuse from the substrate into the Au-film and opposite. However, most of the Au will remain on the Si-surface (as the solid-solubility of Au in Si is very low, $\sim 10^{-6}$ at% Au at $1000K^{(11)}$) and be saturated on silicon (18.6% at% Si at 636K as noted above) in formation of an Au-Si alloy.

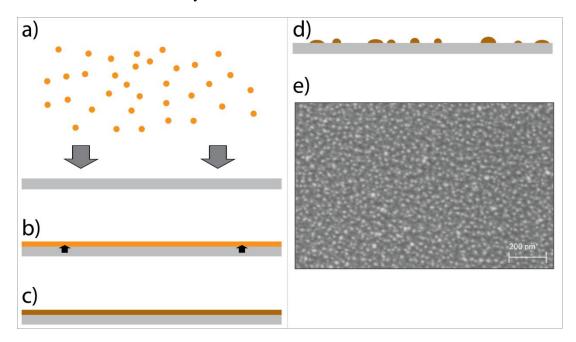


Figure 2.6: Catalytic material is deposited onto a silicon wafer (*a*) resulting in a thin-film of catalytic material. Silicon diffuses into the film (*b*) until the temperature specific equilibrium composition is reached and Au is saturated on Si (*c*). Simultaneously, the melting point of the Au-Si alloy decreases towards saturation which results in a liquid alloy which is stable as droplets (*d*). A SEM image of the Au-droplets after annealing at 500°C (*e*).

As silicon diffuses into the Au-film the melting point will start to decrease in correspondence with the liquidus line given in the Au-Si phase diagram (Figure 2.5 (a)).

c) Saturation of the liquid:

As said, the lowest possible melting point in a binary system is at the eutectic temperature, and is the lower temperature needed to form a liquid Au-Si alloy. The equilibrium composition of the liquid is mainly determined by the surrounding temperature. Since the system in this case consists of an excess of silicon (~275 μ m thick Si-wafer versus 2 nm of Au-film) the liquidus line to the right of the eutectic point (the one closest to pure Si; Figure 2.5 (a)) is used in analysing the composition of the liquid. By heating to an elevated temperature an equilibrium state will be reached when the composition of the liquid alloy has reached the saturation composition at the respective temperature; ex. 22 at% Si and 78 at% Au at 500°C. The composition may be tweaked by respectively changing the ambient temperature.

d) Formation of the droplets:

The reduced melting point results in melting of the Au-Si alloy in formation of the catalytic liquid needed.

Wettability describes the ability of a liquid to stay as a droplet or as a thin-film on a solid surface when brought into contact. The degree of wetting depends on the interface- and surface-forces acting between the liquid, solid and surrounding gas phases, and is given by the contact-angle between the solid surface and the liquid droplet (Figure 2.7 (a)). $\theta=0$ implies perfect wetting (liquid film) while $\theta \rightarrow 180^{\circ}$ implies a continuous decrease in the degree of wetting (increased spherical shape of droplet). The amount of wettability is determined by the forces acting between the liquid and solid phases. In this case of melted metal-catalysts, a continuous liquid film would usually require much more energy to retain because of the large surface-areato-volume ratio. A spherical geometry is therefore much more energy-saving as it has the lowest surface-area-to-volume ratio of all geometries⁽¹²⁾ and is therefore energetically preferred. The spherical shape is maintained by the surface tension existing on the droplet surface (Figure 2.7 (a)). B. Ressel et al⁽¹³⁾ performed experiments on the wettability of Au-Si liquids on Si(111) surfaces and found a contact angle θ of ~43° for the temperature range of 400-650°C. A continuous increase was observed for temperatures exceeding 650°C. In comparison, Au-Si droplets on top of nanowires typically exhibit contact angles of $90-120^{0(14)}$. Three quantities are needed in order to describe a contact-angle configuration for a liquid droplet on a solid surface (Figure 2.7 (a) and (b)):

- σ_l : Surface tension of the liquid droplet.
- σ_s : Surface tension of the solid surface.
- σ_{ls} : Liquid-Solid interfacial tension.

A stable droplet is defined as a droplet which is able to recover its original position if

it slides down one of the sides of the nanowire⁽³⁾. The droplet therefore requires a vertical net force on the part of the droplet sliding downwards which is strong enough to push it back into place. From this, Nebol'sin derived a criterion (Eq. 2.1) which has to be fulfilled in order to attain a stable droplet during growth of nanowires⁽¹⁵⁾:

$$\sigma_l \ge \frac{\sigma_s}{\sqrt{2}} \tag{2.1}$$

This equation indicates that the surface tension of the liquid droplet σ_1 must be larger than the surface tension of the solid surface σ_s divided by $\sqrt{2}$ in order to retain a stable droplet throughout the growth process. If something affects these surface tensions during growth the droplet could become unstable and growth of this nanowire could kink or completely stop.

The Au-Si droplets may vary in size and density, and have been found to mainly depend on the film-thickness of the deposited catalyst material⁽¹⁶⁾. A thicker film (~5nm) was shown to result in larger droplets and a wider size distribution. Careful studies of the surface indicated a prominent surface ripening effect where smaller droplets in the vicinity of larger droplets may diffuse towards and merge with the larger droplets. This happens for small droplets residing within a given distance from the large droplet and forms an empty ring around the large droplets where the smaller droplets have been. The large droplets will therefore become larger and ultimately affect the size distribution. This effect is often referred to as Ostwald ripening⁽¹²⁾ where surface atoms diffuse from smaller droplets to nearby larger droplets. This happens because larger droplets are more energetically stable than smaller droplets⁽¹⁷⁾, and results in the larger droplets growing at the expense of the smaller droplets and the average size and size distribution are naturally affected.

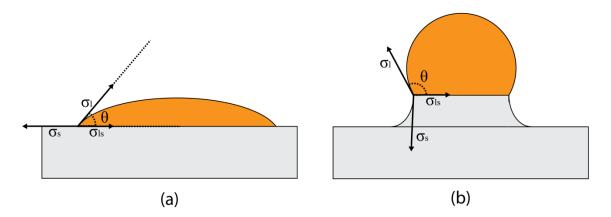


Figure 2.7: A droplet in contact with a surface (*a*) with a contact angle of θ and surface-tension σ_{l} and a liquid-solid interfacial tension σ_{ls} . After initiated growth the contact angle becomes larger and the liquid-solid interfacial tension changes (*b*).

As the film becomes thinner ($\rightarrow \sim 0.2$ nm), the ripening effect gradually disappears, and the droplet sizes become more uniform and the size distribution reduces. Surface ripening is

dependent on the annealing time, where longer annealing times enables more droplets to diffuse over larger distances on the surface. F. Ruffino et al⁽¹⁸⁾ studied this thermal induced self-organization of droplets and was able to successfully manipulate the center-to-center distance and density of the droplets by adjusting the annealing time. Other efforts on controlling the surface ripening have also been done. For example, in order to limit the surface diffusion Westwater et al⁽¹⁹⁾ performed experiments on patterning the silicon surface with SiO₂, as SiO₂-coated areas prevent formation and surface diffusion of the droplets. In this way, some control over the droplet sizes and positions could be gained which is one step farther from the randomness of ripening.

2.2.3 Vapour-Liquid-Solid Growth Mechanism

As described in the previous chapter, catalytic droplets are necessary in order to enable onedimensional VLS growth of silicon nanowires (Figure 2.3). The droplets increase the decomposition and deposition rate of SiH₄ precursor gas by several orders of magnitude compared with uncatalyzed decomposition ^(16, 20). The name of the growth mechanism, Vapour-Liquid-Solid, actually reflects the path of silicon during the growth. An illustration of the whole process is shown in Figure 2.8. Silicon enters the chamber as vapour in the form of gaseous SiH₄ and diffuses towards the Au-Si droplets (*Steps 1-2*). The SiH₄ molecules adsorb (*Step 3*) and decompose (*Step 4*) on the catalytic Au-Si droplets and silicon diffuses into the droplets (*Step 5*) where it gets incorporated into the Au-Si liquid phase. This incorporation disturbs the equilibrium concentration of Si in the liquid and the droplet is now said to be supersaturated on silicon. Because of supersaturation, excess silicon is crystallized at the liquid-solid interface as solid Si in order to re-establish the equilibrium and equilibrium composition. The Si has now been through all the different phases required for Vapour-Liquid-Solid growth.

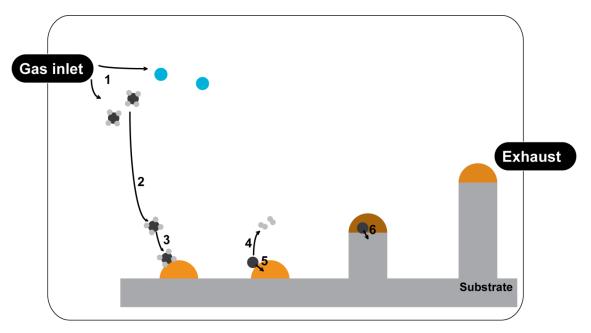


Figure 2.8: An illustration showing the complete VLS growth process from the addition of gas to a complete nanowire. Precursor gases are added to the CVD-chamber (1) and SiH₄ molecules diffuses towards the growth substrate (2). The SiH₄ molecules adsorbs on the Au-Si droplet surface (3) and decomposes into Si(s) and H₂(g) (4). Si diffuses into and supersaturates the Au-Si droplet (5) and in order to re-establish equilibrium composition the Si is crystallised at the liquid-solid interface (6).

The most important steps for catalysed nanowire growth are summarised in Figure 2.8:

- 1. <u>*Precursor feed:*</u> SiH₄ (g) (silane) is fed into the reactor with a possible carrier gas for partial-pressure adjustments.
- 2. <u>Precursor diffusion:</u> Silane diffuses towards the substrate and the catalytic droplet.
- 3. <u>Precursor adsorption</u>: $SiH_4(g)$ adsorbs on the surface of the catalytic droplet.
- 4. <u>*Heterogeneous decomposition:*</u> The adsorbed SiH₄ molecules decomposes on the droplet surface and results in formation of adsorbed Si (s) and the release of H_2 (g) as by-product.
- 5. *Silicon supersaturation:* The decomposed silicon diffuses into and supersaturates the Au-Si droplet.
- 6. <u>Silicon crystallization</u>: Supersaturation pushes the composition of the droplet out of its equilibrium state towards an unstable amount of excess silicon. In order to get rid of this excess silicon and to re-establish the equilibrium state, silicon is crystallised at the easiest interface which in this case is the liquid-solid interface.

Note that uncatalyzed growth is also possible, especially at higher temperatures (See Ch. 2.2.4 for more details). Uncatalyzed growth will not result in nanowire growth but rather result in deposition of silicon on possible silicon surfaces such as the substrate or nanowire walls. However, normal growth-conditions mainly avoid such deposition as the growth-rate of nanowires normally is magnitudes larger than uncatalyzed film-growth⁽³⁾.

Based on earlier studies performed by the author⁽²⁾ a more thorough investigation have been performed on the different transport and reaction processes during growth, and a short description of these studies will now be presented.

2.2.4 Transport and Reaction Processes

Silicon is exposed to several different transport-processes during nanowire growth and the different transport processes are presented in Figure 2.9.

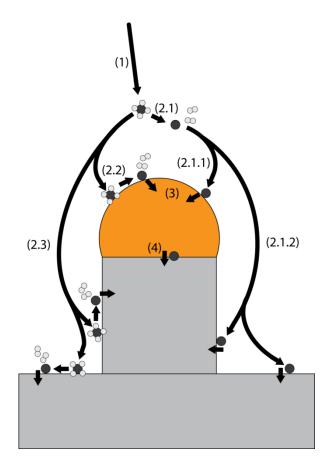


Figure 2.9: When arriving at the sample surface (1) the SiH₄ molecules may either decompose homogeneous into Si(g) and $H_2(g)$ (2.1) or adsorb on one of the surfaces. If adsorbed on the Au-Si droplet the SiH₄ molecule may heterogeneously decompose into Si(s) and $H_2(g)$ (2.2) and the solid Si may then diffuse into and supersaturate the droplet on silicon (3). This may also happen with previously homogeneously decomposed Si(g) (2.1.1). Si(s) will then crystallise at the liquid-solid interface in order to re-establish the equilibrium (4). Alternative routes include decomposition and deposition of Si on nanowire walls and / or substrate ((2.3) and (2.1.2)).

Summary of the steps (Figure 2.9):

• Gas-transport in the chamber (*Step 1*).

There are now three possibilities for the SiH₄ molecule:

- Uncatalyzed homogeneous decomposition of SiH₄ in the gas phase (*Step 2.1*).
 - Adsorption and catalytic growth (*Step 2.1.1*).
 - Adsorption and growth of amorphous or polycrystalline silicon (*Step 2.1.2*).
- Adsorption and catalytic decomposition of SiH₄ on the catalytic droplet (*Step 2.2*).
- Adsorption and uncatalyzed deposition of amorphous or polycrystalline silicon on silicon surfaces (*Step 2.3*).

SiH₄ molecules adsorbed on the Au-Si droplet surface may now continue by the following steps:

- Decomposed silicon sticking to the catalyst droplet may diffuse into the droplet (*Step 3*).
- Crystallisation of silicon at the liquid-solid interface because of supersaturation (*Step* 4).

Closer description of each step (Figure 2.9):

1: Gas transport to droplet-surface:

Mass-transport of SiH₄ to the droplets happens by diffusion, and previous investigations performed on normal uncatalyzed silane pyrolysis have shown that mass-transport of silane at low SiH₄ partial pressures ($\leq 2 Torr$) are not rate-limiting before reaching temperatures above 1050°C⁽²¹⁾. Note that these experiments were performed in a cylindrical quartz reactor which may differ somewhat in geometry from a standard CVD chamber. As growth of Au-catalysed nanowires mostly is performed in the temperature range of 400-500°C and at SiH₄ partial pressures $\leq 2 Torr^{(2, 22, 23)}$ it will still be a fair assumption to reject mass-transport as rate-limiting.

The SiH₄ now have three possibilities; one decomposition possibility (2.1) and two adsorption possibilities (2.2 or 2.3):

 2.1: Homogeneous decomposition of SiH₄: Homogeneous decomposition refers to SiH₄ decomposing in the gas-phase before any interaction with the sample:

$$SiH_4(g) \to Si(g) + 2H_2(g) \tag{2.2}$$

Earlier investigations performed on growth of silicon thin-films^(20, 21) have found that when the SiH₄ partial pressure is held to $\leq 2 Torr$ one may neglect homogeneous decomposition (Eq. 2.2) because of high activation energy. This is an assumption earlier used additionally for silicon nanowire growth⁽²²⁾ and is therefore assumed to also be the case for this experiment. Further analysis of homogeneous decomposition is therefore not performed.

2.2: Adsorption and heterogeneous decomposition of SiH₄ on the catalytic droplet surface: Sticking probability/coefficient $S(\theta)$ is a term used to describe the probability of a given molecule specie to adsorb on a surface and is defined as the adsorption rate divided by the collision rate⁽²⁴⁾. A liquid surface is regarded as an ideal rough surface with sticking coefficient of incoming gaseous silicon molecules of ~1⁽²⁵⁾, which implies a capture of almost all incoming SiH₄ molecules and result in a steady flow of silicon to the surface.

$$SiH_4(g) \rightarrow SiH_4(ads.)$$
 (2.3)

The SiH₄ molecule may now decompose into adsorbed silicon by heterogeneous decomposition⁽²⁰⁾ (Eq. 2.4 and 2.5):

$$SiH_4(ads.) \rightarrow Si(ads.) + H_2(ads.)$$
 (2.4)

$$H_2(ads.) \to H_2(g) \tag{2.5}$$

Activation energies for catalysed heterogeneous decomposition of SiH₄ on Au-Si droplets by assuming Arrhenius behaviour have been reported to vary in an interval of 79 - 92kJ/mol for a temperature range of $450-600^{\circ}C^{(3)}$.

Earlier experiments performed by the author⁽²⁾ have found activation energies varying in an interval of 50 - 137kJ/mol for a temperature range of 400 - 500°C by assuming a thermal activated process (Arrhenius behaviour). These values cannot be directly attributed to the decomposition of SiH₄ as these are values measured for the full growth process. The full growth process from decomposition to crystallisation at the liquid-solid interface is normally said to consist of three steps⁽²⁶⁾:

- i. The incorporation step (Step (2.2) and (3) in Figure 2.9). Covers the decomposition of SiH4 at the Au-Si surface and the diffusion of Si into the Au-Si droplet which leads to a supply of Si at a rate of ρ_{in} .
- *The diffusion step.* Describes the diffusion of silicon through the droplet as a symbol of supersaturation of the Au-Si droplet. This is normally neglected⁽²⁶⁾ because of the assumption of fast diffusion of Si in Au-Si.
- iii. The crystallisation step (Step (4) in Figure 2.9). Covers the crystallisation of Si at the liquid-solid interface at a rate of ρ_{cr} and leads to the growth of a nanowire.

This has proven to be a very complex growthprocess, and based on previous experiments performed by the author one cannot say which of the steps are limiting the growth rate; and therefore not be able to determine which of the steps represents the attained activation energy. It may be assumed that the attained activation energies represent the decomposition of SiH₄ since the values resemble the values reported by others (see beginning of step) and since the diffusion step normally is neglected. One may also ask if the crystallisation step is dependent on temperature and thermally activated. But no conclusions can be set at this point as further investigations are needed in order to separately investigate these steps.

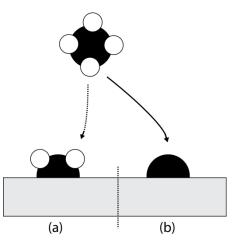


Figure 2.10: A partly decomposed SiH₄ molecule (400-500°C) creating a hydrogenated surface repels new incoming SiH₄-molecules (*a*) while a fully decomposed SiH₄ molecule (~700°C) enables adsorption of new SiH₄ molecules (*b*).

2.3: Adsorption and heterogeneous decomposition of SiH_4 on a silicon surface. There is also a possibility of SiH_4 molecules adsorbing on a solid silicon surface for uncatalyzed growth, but mainly at higher temperatures. It is generally assumed that the sticking factor on a solid silicon surface is several orders of magnitude smaller than on the liquid surface at temperatures usually used for nanowire growth (400°C - $500^{\circ}C$ ^(25, 27). At these temperatures adsorbed SiH₄ is only partly decomposed, and the few SiH₄ molecules that actually stick/adsorb to the solid Si-surface may contain residue hydrogen (Figure 2.10 (a)). This molecule may stay adsorbed to the surface for a while before it is dehydrogenated, and when a SiH₄ molecule now enters the vicinity of the silicon surface it will be completely repelled from the surface because of the apparently hydrogenated surface. On the other hand, at temperatures exceeding 700°C a higher amount of the SiH₄ molecules attain enough energy to release all of their hydrogen atoms after adsorption on the Si-surface (b). In this case dehydrogenated silicon sticks to the surface instead, and since the surface now is not hydrogenated in the same way as for lower temperature the small amount of incoming SiH₄ actually willing to stick may continue to adsorb on the surface. This leads to radial growth of amorphous silicon on the nanowire sidewalls or thin-film growth on the substrate. Higher temperatures may also enable deposition of crystalline silicon thin-film.

Reported activation energies for such heterogeneous silicon decomposition have been reported to:

- ~155kJ/mol for a temperature range of 590 $1050^{\circ}C^{(28)}$.
- ~ 84 kJ/mol for a temperature range of 823 $983^{\circ}C^{(29)}$.
- 3: The next step is the incorporation of the Si-atom into the Au-Si liquid which leads to supersaturation of the droplet. Silicon now goes from an adsorbed gaseous state to an incorporated liquid state. Every silicon-atom diffusing into the Au-Si liquid will disturb the equilibrium of the liquid by pushing the composition towards a higher content of silicon (Figure 2.11; blue arrow), and the droplet will be supersaturated on silicon as long as there is a continuous flow of silicon to the droplet.

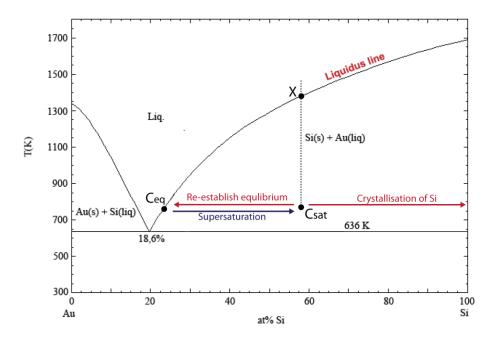


Figure 2.11: Additional flow of silicon to an Au-Si droplet in equilibrium (C_{eq}) will supersaturate the droplet to a saturated composition at C_{sat} (*blue arrow*). In order to re-establish the equilibrium composition the system will crystallise silicon at the liquid-solid surface (*red arrows*).

4: The final step is the crystallization step where silicon goes from its liquid state to its solid state at the easiest interface. Because of an assumedly higher amount of possible nucleation sites along an liquid-solid interface compared to an liquid-gas phase the crystallisation of silicon is assumed to happen at the liquid-solid interface between the catalytic droplet and the silicon surface⁽³⁰⁾.

2.2.5 Nanowire Morphology and Crystallography Based on Earlier Work

Earlier work performed by the author⁽²⁾ mainly consisted of growing silicon nanowires by chemical-vapour-deposition (CVD) and gaining a basic understanding of the employed vapour-liquid-solid (VLS) growth mechanism catalysed by Au-particles. Nanowires were grown at different growth parameters ($400^{\circ}C \le T \le 500^{\circ}C$, $50mTorr \le p_{SiH4} \le 1500mTorr$; Appendix G), and structural characterization of morphological properties such as nanowire diameter, length, direction, crystallinity and defects was performed by Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM). All of the investigated nanowires consisted of a crystalline core covered in a thin (1-2nm) layer of SiO₂ assumedly as a result of post-growth oxidation.

Nanowire diameter:

Earlier reports have shown that the nanowire diameter and distribution mainly depends on the size of the Au-Si droplets formed during heating to a temperature higher than the eutectic temperature^(16, 31). Experiments performed by the author found that a 2nm Au-film resulted in nanowires with a diameter distribution of 10 - 40nm.

No direct dependence on SiH₄ partial pressure or growth temperature was found for the average nanowire diameter other than what was assumed to be an influence by temperature on the surface ripening effects felt on the catalytic droplets, but this is still exposed to frequent discussion in publications and literature^(2, 32-34). Recently, Tan et al⁽²⁵⁾ was unsuccessful in

finding a thermodynamically limit on the minimum nanowire diameter, and suggested that it might be a kinetic limitation, but this has yet to be proven.

Nanowire length and growth rate:

Earlier experiments performed by the author⁽²⁾ indicated a thermally activated growth rate but as presented in Ch. 2.2.4 there are several transport processes which may put a limit on the growth rate of nanowires. The nanowire length / growth rate seemed to follow an approximate Arrhenius behaviour (Eq. 2.6) which is assumed to be dependent on both the growth temperature and SiH₄ partial pressure. The growth temperature supplies the SiH₄ molecules with enough energy to surpass the energetic barriers and a higher partial pressure implies that more SiH₄ atoms collide with the catalytic droplet:

$$a_{rate} = A e^{\frac{-E_{\alpha}}{R_{gas}T}}$$
(2.6)

This relates the growth velocity of the nanowire (a_{rate}) to the activation energy E_{α} , gasconstant R_{gas} , substrate temperature T and pre-exponential factor A.

Earlier reports have indicated a dependence on the Gibbs-Thomson effect which may limit the growth-rate of thinner nanowires^(2, 26) but no Gibbs-Thomson effect was found in the previous experiments performed by the author⁽²⁾ and matches the results attained by Kodambaka et $al^{(14)}$.

Growth direction:

The growth direction of the nanowires seemed to depend on growth temperature, SiH₄ partial pressure and nanowire diameter. The growth temperature and SiH₄ partial pressure was related to the growth velocity and stability of the droplet where nanowires grown at high temperature and partial pressures seemed to prefer a tilted growth direction (<110> and <112>). A combination of high temperature and low partial pressure seemed to result in nanowires preferring a <111> growth-direction perpendicular on Si(111) substrates which was attributed to a high droplet stability and low growth velocity.

There were also indications on that thinner nanowires would prefer a tilted growth direction (<110> and <112>) while thicker nanowires would prefer a perpendicular <111> growth direction in accordance with the previous results presented by Schmidt et al⁽³⁵⁾.

Growth instabilities:

A large amount of the grown nanowires, especially at higher growth velocities seemed to spontaneously kink to alternative directions and was assumed to be a result of instabilities in the catalytic droplets. Two possible causes for such kinking have previously been reported:

- i. *Temperature-gradient*^(36, 37): A sudden change in the temperature of the droplet may cause an unstable contact-angle and the droplet may run down the side-faces of the nanowire, possibly leading to kinks.
- *ii. Growth velocity*⁽³³⁾: Nanowires grown at high SiH₄ partial pressures in combination with low growth temperature (440°C, 500 mTorr) seemed to promote a higher probability of kinking effects than nanowire grown at higher temperatures and lower

partial pressures (520°C, 10 mTorr). This was related to higher droplet stabilities and reduced growth velocities for the latter conditions.

Au-diffusion:

TEM investigations found gold particles on the surface of the grown nanowires up to a given distance from the catalytic particle (~170nm for nanowires grown at 500°C and 1000mTorr; Figure 2.12 (a)). These particles were assumed to come from the catalytic particles by diffusion (b) and have previously been attributed to appear at the end of the growth process during cooling when the SiH₄ valves are closed and the heating is removed⁽³⁸⁾.

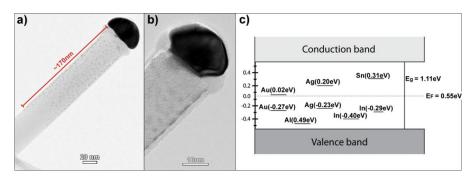


Figure 2.12: Nanowires grown at 500°C and $p_{SiH4} = 1000$ mTorr was covered in diffused Au-particles up to ~170nm from the catalytic droplet (*a*). These particles are assumed to come from the main catalytic particle on top of the nanowire (*b*). Alternative materials with energy-levels farther from the silicon band-gap middle include aluminium (Al), silver (Ag), indium (In) and tin (Sn) (*c*).

2.2.6 Au-catalyst Disadvantages

Despite its robust growth-conditions gold is unwanted in Si-based photovoltaic devices as it may have serious consequences for the efficiency of such devices, and is mainly a result of unfavourable positioning of the energy-levels for Au in the Si band-gap (Figure 2.12 (c)). Energy-levels close to the middle of the band-gap are very good recombination centres⁽³⁹⁾ which drastically reduce the life-time of generated electrons (Ch. 2.4.1).

As previously presented earlier investigations have shown that nanowires grown by Au as catalytic material have a surface covered in Au-particles up to a given distance from the Au-Si particle⁽²⁾ (Ch. 2.2.5). In addition there is a small solid-solubility of Au in Si (max. ~2.0 × $10^{-4} at\% Au$ at ~1280°C⁽⁴⁰⁾). These are probable recombination centres and may drastically harm the efficiency of a potential silicon nanowire base solar-cell. The particles dispersed on the surface of the nanowire (and the main Au-Si catalytic particle on top of the nanowire) could be removed by etching but probably not without harming the underlying structure as gold-removal requires very harsh etching conditions. In addition, such a procedure may be unwanted at large scale productions because of the amount of chemicals needed and the increase in cost and production time and gold contamination should therefore be avoided as far as possible.

Several groups are investigating the mechanisms behind dispersion of Au-particles on the nanowire surface and one has found a dependency on chamber pressure⁽³⁸⁾, but one still faces the problem with removal of the Au-Si catalytic droplet and the solubility of Au in solid Si. Another solution is to employ other catalytic materials which are easier to remove and/or

which do not act as recombination centres, and much of the nanowire research performed today therefore focuses on the use of alternative catalytic materials.

Some alternative catalysts have been investigated and will be presented in the coming chapter.

2.3 Alternative Catalysts

Because of the disadvantages found for Au-catalysed growth a literature study has been performed on some of the alternative catalysts found in Figure 2.4.

2.3.1 Catalyst Basics

Several properties must be considered when assessing the quality of a catalytic material and comparing it with others. The goal is the first property needed to be considered since different goals needs different properties.

Eutectic temperature:

The eutectic temperature is important as it is the lowest temperature where a liquid may form and it therefore also sets the lowest temperature usable for VLS-growth. Higher temperature need higher process temperatures and may limit the usable equipment.

Silicon solubility:

A higher solubility of silicon in the metal reduces the energetic cost of increasing the saturation of the droplet per Si-atom past the equilibrium concentration. Consequently, the Si partial-pressure needed to achieve a given increase in the Si-concentration in the droplet may be lower for liquids with higher equilibrium Si-solubility than for those with lower solubility. It is therefore assumed that higher precursor pressures / SiH₄ partial pressures will be needed for catalyst materials with low Si-solubility to attain respectable growth rates^(2, 41).

Droplet stability:

As indicated by Nebol'sin⁽¹⁵⁾ the stability of the catalytic droplet may also affect the growth conditions for nanowires and possibly fully inhibit growth if the stability is too low, and as presented in Ch. 2.2.2 Nebol'sin developed a criterion for stable growth (Eq. 2.2.1). Schmidt et al⁽³⁾ have reported liquid surface tensions at given temperatures for some of the catalyst metal – silicon alloy systems investigated in this report (Table 2.1). For a solid silicon surface the surface tension σ_s has been reported to 1.20 J/m², and results in a criterion of

$$\sigma_l > \frac{1.20J/m^2}{\sqrt{2}} = 0.85J/m^2 \tag{2.7}$$

in order to achieve a stable catalytic droplet.

Alloy system	Liquid surface tension for alloy system, $\sigma_l^{(3)}$	Temperature
Au-Si (19 at% Si)	1.22 J/m^2	636K
Ag-Si (11 at% Si)	0.92 J/m^2	1108K
Al-Si (12 at% Si)	0.89 J/m^2	850K
In-Si (< 0.01 at% Si)	0.53 J/m^2	700K
Si-Sn (< 0.01 at% Si)	$0.58 \text{ J/m}^{2(15)}$	505K

Table 2.1: Reported liquid surface tensions for respective catalytic alloy systems at the given eutectic composition and temperature⁽³⁾

These values will be discussed in more detail in the coming chapters.

Recombination tendency:

It is known that some metal material may be left behind in the structure as impurities after growth completion. The possible amount may be found from the solid-solubility given in the phase diagram for the respective catalytic system (Table 2.2).

Alloy system	Max. solid-solubility of respective metal in silicon	Temperature
Au-Si	$\sim 2.0 \times 10^{-4} at\% Au^{(40)}$	1280°C
Ag-Si	$\sim 4.0 \times 10^{-4} at\% Ag^{(42)}$	1350°C
Al-Si	$\sim 1.6 \times 10^{-3} at\% Al^{(43)}$	577°C
Si-Sn	$0.1 at\% Sn^{(43)}$	1066°C
In-Si	$5 \times 10^{-3} at\% In^{(44)}$	1300°C

 Table 2.2: Maximum solid-solubility of respective metal in a metal-silicon alloy at a given temperature.

As seen from the table most of the metals have a very low solubility in silicon at the given temperatures, and a further reduction is normally observed when reducing the system temperature. Such low solubilities are normally neglected but for highly sensitive photovoltaic devices even very small amounts may affect the efficiency drastically. As said in Ch. 2.2.6 gold may drastically reduce the photovoltaic efficiency because of unfavourable positioning of the impurity levels in the band-gap of silicon (Figure 2.12 (c)) which ultimately results in increased recombination rate. This chapter also presented earlier investigations which found that Au-particles may cover parts of the nanowire surface and may further reduce the efficiency of photovoltaic devices.

The recombination rate depends on the energy-difference between the impurity-level and the middle of the band gap. An impurity level closer to the middle of the band gap is a much more efficient recombination centre than a level farther from the middle. Use of metals with impurity levels close to the middle of the band gap, so called deep-level traps should therefore be avoided. As noted in the previous chapter, Au have two impurity levels, one which is deep-level. Au contamination may therefore reduce the carrier lifetime and should therefore be avoided.

There are many catalytic alternatives to Au (Figure 2.4) but the structural quality may vary drastically between the catalysts and specific growth regimes designed for each catalyst are needed. This will be illustrated by further presentation of some chosen alternatives; silver

(Ag), indium (In), tin (Sn) and aluminium (Al) which are chosen because of their availability at NTNU Nanolab.

Chemical stability and oxidation:

Additional properties worth mentioning are catalyst removal and oxidation. Chemical stability describes the thermodynamic stability of a chemical system and is related to change in Gibbs energy. An indication of this stability may be found from the standard electrode potential E^0 for the redox equilibrium for the relevant catalyst material. Gold is a very chemically stable element with a very large and positive standard electrode potential; $E_0 = 1.69V$ for $Au^+ + e^- \leftrightarrow Au(s)^{(45)}$. Gold has shown to be very hard to remove and requires harsh chemical treatments which also may attack other parts of the structure. The positive potential also indicates that gold do not oxidize spontaneously at normal conditions which is favourable for nanowire growth as oxides may complicate or fully prevent the growth.

Schmidt et al ⁽³⁾ divided the different catalysts into three groups (Figure 2.4):

i. Type-A catalysts.

Type-A catalysts have simple eutectic phase diagrams with relatively high eutectic solubility of silicon ($\geq 10 \ at\% \ Si$). Catalytic droplets based on these catalytic materials have also been found to generally have high surface tensions. Higher surface tensions have shown to give straighter nanowires with a lower amount of defects such as bending^(3, 41). There are very few Type-A catalysts; only aluminium, gold and silver.

ii. Type-B catalysts.

Type-B catalysts have the same simple eutectic phase diagrams as Type-A catalysts but with much lower eutectic silicon solubility. As the growth velocity has shown to be dependent on solubility these catalysts may result in very low growth rates if not increased to temperatures high above the eutectic. It has also been argued that these catalysts are preferable to use for growth of heterojunctions since the equilibrium composition is quickly re-established after gas cut-off (because of low solubility) and therefore results is more abrupt junctions than catalysts with higher solubility. These catalysts have also been found to generally have a much lower surface tension than Type-A catalysts ^(3, 15, 17) which will result in reduced droplet stability, and growth of straight nanowires may be more difficult with these catalytic materials. Whether it is the low solubility or the low surface tension which causes growth problems is still undecided and needs more investigation⁽³⁾.

iii. Type-C catalysts.

Type-C catalysts forms silicides and have rather complex phase diagrams with several silicide phases and eutectic points. This group contains a large aspect of different catalysts with a vast spectre of properties. It appears to be a trend that nanowires grown via silicide phases have a higher probability of crystallographic defects⁽³⁾. Schmidt et al.⁽³⁾ concludes that type-C catalysts work well for VLS growth at high temperatures and not so well for growth at lower temperature via silicide phases. The

lowest eutectic temperature found for these catalysts is higher than 800°C and is therefore not very attractive for nanowire growth.

In this case two Type-A catalysts (aluminium and silver) and two Type-B catalysts (indium and tin) have been chosen for further investigation, and their phase diagrams are shown in Figure 2.13 (a)-(d) which all are binary eutectic.

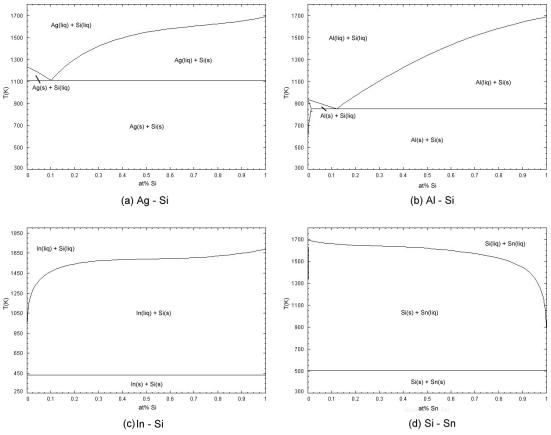


Figure 2.13: The binary phase-diagrams for the catalytic alternatives; Ag-Si (*a*), Al-Si (*b*), In-Si (*c*) and Si-Sn (*d*) systems⁽¹⁾.

2.3.2 Aluminium and Silver (Type-A Catalysts)

<u>Aluminium:</u>

Aluminium is the only non-noble metal with a eutectic Si-solubility (Figure 2.13 (b)) close to that of gold (11 at% Si at 577°C), and ensures reasonable growth rates already at temperature right above the eutectic temperature⁽³⁾. However, the increased eutectic temperature makes Al-catalysed VLS growth less attractive compared to gold. Aluminium catalysed silicon nanowires have been grown at temperatures of 540-900°C without plasma⁽⁴⁶⁻⁴⁸⁾.

The stability of the Al-Si droplet has been reported to be intermediate (Table 2.1) as it is very close to the limit of the criterion given by Nebol'sin⁽¹⁵⁾. This may indicate a more unstable growth compared to gold resulting in a larger degree of instability problems such as bending and kinking.

Al does not induce recombination centres / traps in the silicon band-gap since the single impurity level is very close to the silicon valence band (Figure 2.12 (c)), and simultaneously induces p-type doping of the silicon structure⁽³⁾ which may be advantageous for the production of photovoltaic applications.

The biggest problem with aluminium is the chemical stability as it is quickly oxidised to Al_2O_3 ($E^0 = -1.68V^{(45)}$) in contact with air or water. This problem was investigated by Whang et al.⁽⁴⁶⁾ and by exposing the samples to rapid thermal oxidation before growth one clearly could observe a reduction in the density of nanowires with increasing oxidation temperature. In order to minimize damage done by oxidation, preventive steps have to be taken during the whole processing procedure. One solution might be in situ deposition of aluminium in the CVD chambers as reported by Wang et al⁽⁴⁹⁾. Another solution was given by Ke et al.⁽⁵⁰⁾ who investigated growth at high H₂ and SiH₄ partial pressures. The growth was investigated for temperatures between 450°C and 700°C with reactor pressures between 30 – 600 Torr. Such high partial pressures were found to be effective at reducing problems associated with Al oxidation and nanowire nucleation.

Removal of aluminium is assumed to be easier than compared to gold because of its reduced chemical stability.

Pros:

- High eutectic Si-solubility
- Introduces a single impurity level close to the silicon valence band
- Induces p-type doping
- Assumed to be easier to remove than Au.

Cons:

- Reduced droplet stability compared to Au.
- Increased eutectic temperature compared to Au.
- Large oxidation problems when exposed to air.

Silver:

The Ag-Si phase diagram (Figure 2.13 (a)) has a single eutectic point at 11 at% Si (836°C) which ensures a short saturation time and rapid growth rate compared to Type-B materials^(3, 15). Because of the high solubility it may be assumed that growth may be performed at SiH₄ partial pressures comparable to the ones used for gold catalysed growth. Earlier experiments grew nanowires at partial pressures as low as $p_{SiH4} = 50$ mTorr. On the other hand, silver has a very high eutectic point (838°C) and may be a reason why so few publications cover silver catalysed growth. A high eutectic temperature requires a corresponding high process temperature in order to form catalytic droplets and to enable VLS growth.

The stability of an Ag-Si droplet has been reported to be intermediate by Nebol'sin, and implies that the surface tension for Ag-Si droplet is high enough to grow nanowires but

smaller than Au-Si droplets $(Table 2.1)^{(15)}$. The reduced stability could result in a larger degree of kinking, a general reduction in the amount of straight nanowires and could possibly also affect the growth direction compared to gold-catalysed growth.

The impurity levels formed by silver in the band-gap of silicon is placed a bit farther away from the middle of the band-gap (Figure 2.12 (c)) and hereby results in a reduced recombination rate compared to gold. Note that silver still is a very active recombination center compared to other non-noble alternatives.

Silver has a reduced stability compared to gold and is therefore assumed to be easier to remove after growth⁽⁵¹⁾. The standard electrode potential is reduced compared to gold $(0.80V^{(45)})$ but is still positive, indicating that silver do not oxidize spontaneously at normal conditions and oxidation has not been reported as a major problem in earlier publications.

Pros:

- High eutectic Si-solubility (11 at % Si)
- More favourable placement of impurity levels.
- Reasonable growth rates assumed already at eutectic temperature.
- Assumed to be easier to remove than gold.
- Not exposed to oxidation-problems.

Cons:

- High eutectic temperature (~1000°C) for VLS growth.
- Reduced droplet stability compared to gold.

2.3.3 Indium and Tin (Type-B Catalysts)

Indium:

Indium is a low-solubility catalyst with a eutectic composition of only 0.004 at% Si $(157^{\circ}C)^{(43)}$. The low eutectic temperature makes this a very attractive catalyst, but because of the low eutectic solubility an increased temperature is needed in order to attain respectable growth rates. Plasma-assisted growth has been performed at 200-300°C^{(37, (38)} while normal CVD growth has been performed at a temperature of $600^{\circ}C^{(52)}$. It is assumed that higher SiH₄ partial pressures are needed in order to enable respectable growth rates (Ch. 2.3.1). The resulting nanowires have been reported to be slightly tapered which has been assumed to be a result of evaporation of indium from the droplet because of the low melting temperature⁽⁵²⁾.

The surface tension of an In-Si droplet has reported to be smaller than the necessary value found by Nebol'sin for stable nanowire growth (Table 2.1) and was assumed to be too low for any nanowire growth⁽¹⁵⁾.Later results have shown that indium-catalysed growth is possible and it is assumed that a too low SiH₄ partial pressure was the reason for the unsuccessful growth by Nebol'sin⁽¹⁾ and not the low surface tension. Even if the surface tension do not limit the possibility of growth it definitively affects the growth as indium-catalysed nanowires shows a high degree of instabilities such as bending and kinking^(52, 53).

Indium contaminations results in only a single impurity level in the band-gap of silicon (Figure 2.12 (c)) and is located very close to the valence band of silicon. This indicates that indium is not a very active recombination center and the recombination rate is not largely affected. In addition, because of the close position to the valence band a possible p-type doping will be induced when contaminating/doping the structure with indium. This would be favourable from a process-line standpoint as it reduces the number of processing-steps for photovoltaic devices.

The standard electrode potential for indium is small and negative $(-0.34V^{(45)})$ which indicates that the chemical stability is reduced compared to aluminium and silver as described previously. It is therefore assumed that removal of indium will be easier than of aluminium and silver.

In addition, because of the negative value of potential it may be assumed that tin is exposed to a degree of spontaneous oxidation, but oxidation has not been reported as a major problem in indium catalysed growth which may imply a slow oxidation process.

Pros:

- Low eutectic temperature
- A single impurity level close to the valence band in silicon.
- Indium contaminations may induce p-type doping.
- Assumed to be easier to remove than Au.
- Oxidation does not seem to be a major problem.

Cons:

- Low eutectic Si-solubility (~0.004 at% Si)
- Low droplet stability.
- Higher growth temperatures are needed to attain reasonable growth rate because of the low Si-solubility.

<u>Tin:</u>

Tin is still a relatively unexplored catalytic material for nanowire growth but some research have been performed and it is assumed to be a promising catalyst^(54, 55). It is assumed to hold some of the same properties as for indium because of their similarities in the eutectic diagram, silicon solubility and placement in the periodic table. The eutectic composition of Sn-Si is < 0.01 at% Si (232°C) and places it among other low-solubility catalysts such as indium. Earlier experiments have mainly grown tin-catalysed nanowires by plasma-assisted CVD at temperatures of 300-400°C^(53, 55). Nebol'sin tried tin catalysed nanowire growth but was unsuccessful. The same assumption as earlier presented for indium on low surface tension (Table 2.1) was also performed in this case⁽¹⁵⁾, but as later experiments have shown that tincatalysed growth is feasible one has assumed that a higher SiH₄ partial pressure is needed for normal CVD growth also in this case. The attained nanowires are however assumed to contain a large degree of instabilities such as bending and kinking as presented for indium because of the low droplet stability. Tin contaminations result in two impurity levels in the silicon band-gap, as shown in Figure 2.12 (c). None of these levels are especially close to the band-gap middle and will probably not act as very active recombination centres. The impurity levels will in this case be neutral and not induce p-type doping as with indium.

Tin has a very small negative standard electrode potential of ~-0.14V which indicates a reduced chemical stability compared to silver and gold, and it is therefore assumed that tin may be removed much easier. The negative potential also indicates that tin is exposed to spontaneous oxidation under normal conditions, but since there are found no reports on oxidations problems it is assumed that oxidation of tin is not a major problem, as for indium.

Pros:

- Low eutectic temperature.
- Two approximately neutral impurity levels in the band-gap of silicon.
- Assumed to be easier to remove than Au.
- Oxidation does not seem to be a major problem.

Cons:

- Low solubility of silicon.
- Low droplet stability.
- Higher temperatures are needed in order to attain reasonable growth rates.

From these assessments aluminium is assumed to be the currently best alternative to gold for growth of nanowires for photovoltaic devices as it do not seem to increase the recombination rate and simultaneously induces p-type doping in the structure. Indium seems to result in the same effects and acceptable growth-rates have been attained at temperatures not far from the eutectic temperature of aluminium but because of reduced droplet stability aluminium seems as the better choice. However aluminium is rapidly oxidized in air which may drastically affect the density of morphology of nanowires and preventive steps must be developed / taken.

2.4 Introduction to Semiconductors and Solar Cells

Semiconducting materials are the basis of one of the largest industries today, and are used in a vast amount of different electronic applications. They are also the cornerstone of much of the solid state photovoltaic technology employed today. Many applications, including solar cells, are based on so called pn-junctions and this chapter will give a short introduction to such junctions and their relation to silicon nanowires.

2.4.1 Introduction to Semiconductors and PN-Junctions

Silicon is a semiconductor material having a diamond crystal structure (Figure 2.14) and four valence electrons.

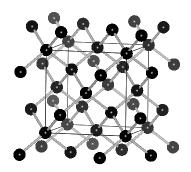


Figure 2.14: The diamond crystal structure employed by Si.

This is a cubic crystal structure consisting of corner-sharing tetrahedral which is a result of sp³ hybridization where 4 atomic orbitals combine to make 4 molecular orbitals with tetrahedral angle between them.

Semiconductors may be separated from metals by their energy-diagram; metals consist of a single partly filled energetic band (Figure 2.15 (a)) while semiconductors have several bands separated by band-gaps (b).

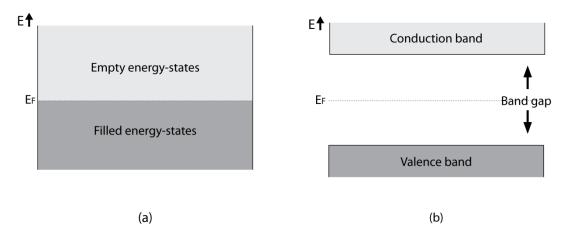


Figure 2.15: (a) Illustrations of the continuous energy-band for metals (*a*) and the discontinuous energy-bands for semiconductors separated by a band-gap (*b*).

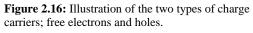
In metals all energy-states up to the Fermi-level E_F are filled with electrons and it requires little energy to excite an electron from its ground state to an empty energy-state above the Fermi-level. This is however not so easy for electrons in a semiconductors structure because of the band-gap. The highest band filled with electrons is called the valence band and all energy-states in this band are completely filled with electrons (at 0K). The next band is the conduction band and is completely empty at 0K as electrons need enough energy to surpass the band-gap in order to excite to this band. The amount of energy needed is determined by the size of the band gap:

- Si ~ 1.11 eV.
- GaAs ~ 1.42 eV.

Conduction:

Conduction in semiconductors depends on the amount of free charge carriers. A charge carrier is an electron which is free to move among the empty energy-states in the conduction band or a hole which is free to move among the filled energy-states in the valence band (Figure 2.16). Charge carriers are mainly divided into two types:

- Conduction band (empty states) Free electron Free hole Valence band (filled states)
- i. *Intrinsic charge carriers:* Charge carriers generated by thermal energy or light-adsorption (Radiative heat); heating the solid to a temperature above 0K.



ii. Extrinsic charge carriers: Charge carriers generated by the addition of dopant atoms to the silicon structure.

A pure semiconductor at T = 0K do not possess any free charge carriers and for a semicoductor to conduct such charge carriers must be generated, and there are mainly two methods to attain charge carriers:

Thermal excitation of electrons (intrinsic charge carriers):

When the temperature is increased to at temperature T > 0K, electrons may start to excite into higher energy-levels. This is called thermal *excitation*, where heat (energy) is absorbed by electrons which get high enough energy to jump to a higher energy-level (Figure 2.17 (a)). If the heat source is removed the electron will fall down to the valence band in a *recombination* process. The probability of finding electrons f(E) (Eq. 2.8) at a given energy-level E follows the Fermi-Dirac distribution:

$$f(E) = \frac{1}{e^{(E-E_F)/kT} + 1}$$
(2.8)

Where *E* is the energy level, E_F the Fermi-level (chemical potential), *k* Boltzmanns constant and *T* the temperature. The probability of finding electrons f(E) at an energy-level *E* increases with increasing temperature *T* (Figure 2.17 (b)).

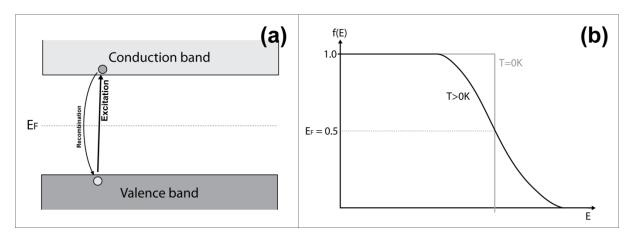


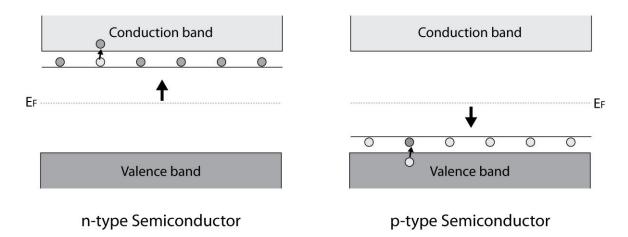
Figure 2.17: By adding enough heat electrons will gain enough energy to excite over the band gap and into the conduction band by an *excitation* process. If the heat source is removed, the electron will fall down to the valence and recombine with a hole in a *recombination* process (a). The probability of finding an electron a given energy-level E is given by f(E) and follows a Fermi-Dirac distribution (b).

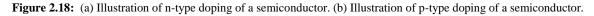
Electrons which excite to the conduction band leaves an empty state, a hole, in the valence band. Both can carry a charge and therefore considered as charge carriers, and the conductivity of the semiconductor depends on both the concetration of electrons in the conduction band and holes in the valence band (Electrons are considered as negative charges while holes as positive charges).

Doping of semiconductors (extrinsic charge carriers):

Another way of generating charge carriers is by doping the semiconductor. Doping may be performed in order to adjust/control the number of charge carriers and hereby the conductivity of the semiconductor. Doped semiconductors are often referred to as extrinsic semiconductors whereas undoped semiconductors are referred to as intrinsic semiconductors.

Doping is performed by adding new material to the existing semiconductor material. In the case of silicon, boron and phosphorus is commonly used. Boron contains one less valence electron compared to silicon and results in p-type doping, while phosphorus contains one extra valence electron and results in n-type doping.





By adding phosphorus to a silicon structure impurity levels are introduced into the silicon band-gap (Figure 2.18 (a)). These impurity levels are filled with electrons and is located very close to the silicon conduction band and the Fermi-level moves upwards because the increased probability of finding electrons at higher energy-levels. Since the energy-difference between the silicon conduction band and the boron impurity levels are very small electrons in the impurity levels need very little energy to excite into the conduction band, and already at room-temperature most of the electrons is assumed to have excited⁽⁵⁶⁾. This increases the amount of free charge carriers in the conduction band and results in an increased conductivity of the seminconductor.

By adding boron to the structure instead (Figure 2.18 (b)) which contains one less electron than silicon, impuity-states filled with holes is formed very close to the valence band. This reduces the Fermi-level in the system. The energy difference between the impurity band and valence band is very small also here and electrons need very little energy to excite from the valence band to the holes in the impurity band. This increases the hole concentration in the valence band and the conductivity of the system is increased.

Charge carrier regimes:

- *Extrinsic regime (Low temperature, T):* At low temperature there is not enough energy to excite intrinsic electrons from the valence band to the conduction band directly, and the concentration of charge carriers mainly dependends on the number of excited extrinsic electrons.
- *Saturation regime (Intermediate temperature, T):* The temperature is now so high that all the electrons from the dopant/impurity level have excited into the conduction band, and has come to a saturation. The temperature is still not high enough to excite electrons from the valence band.
- *Intrinsic regime (High temperature, T):* The temperature is now so high that electrons may start to excite from the valence band to the conduction band. And since the concentration of electrons in the valence band is several magnitudes larger than the concentration in the dopant levels, the total charge carrier concentration is now mainly dependent on the number of excited intrinsic charge carriers.

Mobility and Conductivity⁽⁵⁶⁾:

The mobility of electrons and holes in a semiconductor represents how fast the respective charge-carrier may move through the semiconductor and may be given as the following:

$$\mu_n = \frac{e\tau}{m_n^*} \tag{2.9}$$

$$\mu_p = \frac{e\tau}{m_p^*} \tag{2.10}$$

Where *e* is the electron charge, τ the scattering time and m_n^*/m_p^* the effective mass of an electron/hole.

The effective mass is a collective term on how the structural lattice affects the mass of the electron/hole. The real mass of en electron is defined for a free electron, but since these electrons are trapped in a structure one have to take into account the effect from the surrounding lattice.

The conductivity of a semiconductor (Eq. 2.11) depends on the concentration of chargecarriers in both bands and their mobility, and may be written as following:

$$\sigma = e(n\mu_n + p\mu_p) \tag{2.11}$$

n: Electron concentration in conduction band.

p: Hole concentration in valence band.

All of the properties mentioned above applies to nanowires as to standard solids, it is not before reaching very small dimensions the properties will start to change. Nanowires with diameters less than 10 nm has been shown to endure different quantum effect^(57, 58), but this will not be presented in this report as growth of such small nanowire has not been the focus of this experiment.

PN-Junctions:

As for many other semiconductor devices, solar cells consist of a p-doped part and an n-doped part connected together creating a so-called pn-junction. The formation of such a junction is shown in Figure 2.19 and will be explained in more detail in this chapter.

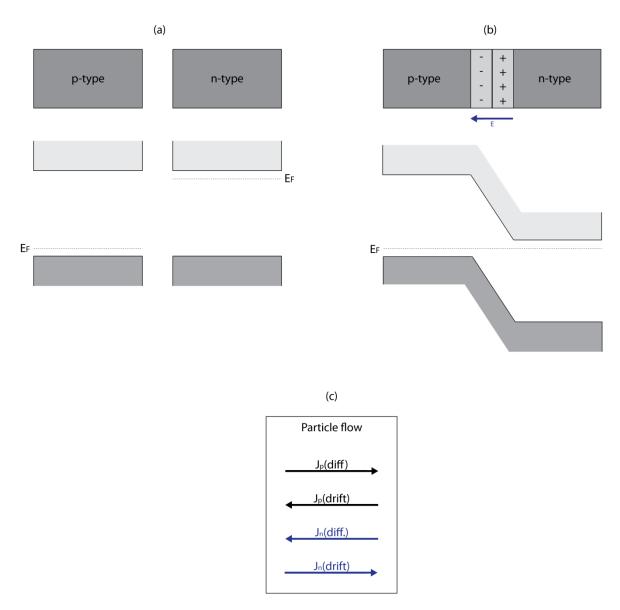


Figure 2.19: Two isolated regions of a p-type and an n-type material in combination with their energy-bands (a). When put together (b) the surplus of electrons in the n-side will start diffusing over into the p-side and vice versa. As this diffusion of majority carriers continues an electric field will start to form over the junction and minority carriers will start drifting in the opposite direction of the junction, ultimately balancing out the diffusion current. The system will now be in equilibrium with two balanced opposite flows of electrons and holes (c).

At this stage, it is important to know the difference between majority and minority carriers. An n-type material is doped in order to increase the electron concentration and electrons are then named the majority carrier while holes are named minority carriers, and oppositely for ptype materials.

When these two materials are connected together, electrons will start to diffuse from the n-type to the p-type $(J_n(diff))$ and holes from the p-type to the n-type $(J_p(diff))$; flow of majority carriers.

This will gradually strip the interface regions of their respective majority carriers and creates an oppositely charged area called the depletion area; depleted of majority carriers. Simultaneously during this depletion process the increasing size of the oppositely charged depletion area results in the build-up of an electrical field E over the junction. This field will initiate a flow of minority carriers over the junction. Electrons will move in opposite direction of the electric field $(J_n(drift))$ while holes will move in the same direction as the electric field $(J_p(drift))$. This flow is called drift-transport of minority carriers and increases with increasing strength of the electric field. These minority-carriers flow in the opposite direction of the majority carriers and electric field will increase in strength until the minority-carrier flow equals the majority-carrier flow for both species and following criterions is fulfilled:

$$J_p(drift) + J_p(diff.) = 0$$
 (2.12)

$$J_n(drift) + J_n(diff) = 0$$
(2.13)

This implies that the electron- and hole-flow is equal in both direction and results in no net current; the system is in equilibrium and continues to be in equilibrium until something disturbs the particle flow. A total of four different particle flows have now been considered, and are summarised in Figure 2.19 (c).

Solar cells:

As presented in the beginning of this chapter, a solar cell is mainly a large pn-junction, as shown in Figure 2.20.

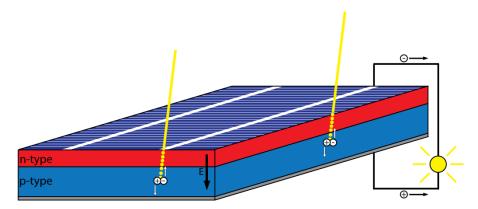


Figure 2.20: A typical solar cell is built up as a previously described pn-junction and connected to an external circuit which transport the carriers back to its origin.

Sunlight is quantified as small energy-packets called photons which are one of the elementary particles. Photons are the basic unit of light and other electromagnetic radiation and their energy may be absorbed by the electrons in the solar cell.

Absorption of a photon adds energy to the silicon structure and may result in an excitation phenomenon where electrons excite to higher energy-levels if the energy of the photon exceeds the band-gap energy of silicon of 1.11 eV.

A basic excitation process is described in Figure 2.21:

- When a photon with an energy exceeding the band-gap energy of 1.11 eV is absorbed by silicon an electron may excite to the conduction band.
- The generated/excited minority electron may diffuse towards the depletion region and electric field while the hole may diffuse in the opposite direction.
- If the electron gets in the vicinity of the electric field within its lifetime the field will pull the electron over to the other side of the junction.
- 4) If the life-time of the electron is too short for successfully reaching the junction the electron will fall down to the valence band and recombine with a hole.

There is now a surplus on electrons in the n-side and holes in the p-side and as this disturbs the equilibrium condition of the system the electron and hole is pushed out into an external circuit as shown in Figure 2.20.

There are two major limiting properties for solar cells:

- i. Recombination of minority-carriers / chargecarriers.
- ii. Light absorption

Recombination of minority carriers⁽³⁹⁾:

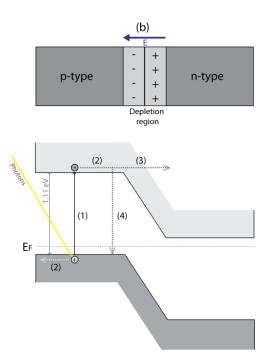


Figure 2.21: An incoming photon with an energy exceeding the band-gap is absorbed by an electron in the p-side valence band. The electron gains enough energy to surpass the band-gap and excites into the conduction band (1) simultanously forming a corresponding hole in the valence band. The electron diffuses towards the electrical field/junction (2) and depending on the lift-time of the electron the electron reaches the junction and drifts over into the n-side (3). Since this disturbs the equilibrium condition the electron is pushed out in an external circuit which leads it back to the p-side. If the life-time is too short the electron will recombine with a hole in the valence band.

Electrons moving through a p-type solid consisting of a large surplus of holes may only stay there for a given amount of time before recombining with a hole (Step 4 in Figure 2.21) (This is also applicable to holes moving through an n-type solid). When recombining the minority carrier is lost and do not contribute to the current output of the cell, and in order to increase the efficiency of the solar cell this recombination rate has to be minimized.

The diffusion length of minority electrons (n) and minority holes (p) depends on the carrier life-time by the following equation:

$$L_{n/p} = \sqrt{D_{n/p} \tau_{n/p}} \tag{2.14}$$

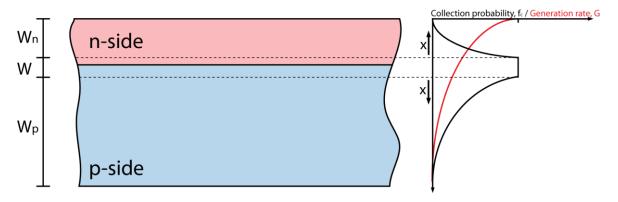
- $L_{n/p}$: Diffusion length of electrons/holes as minority carriers in oppositely doped material.
- $D_{n/p}$: Diffusion coefficient of electrons/holes as minority carriers.
- $\tau_{n/p}$: Lifetime of electrons/holes as minority carriers.

Several steps are taken in order to minimize the recombination rate.

Generation of excited carriers happens at larger rates closer to the surface of the solar cell (Figure 2.22; red curve) and because of this one mainly wants the p-side to be as close to the top of the cell as possible in order to generate as much minority electrons as possible. The width of the n-side W_n is therefore made as thin as possible, but as a good connection is needed with the surface contacts a given minimum width is needed. The n-side is also doped heavily to n+ in order to promote good contact with the surface contact and is why the depletion layer W penetrates farther into the p-side than the n-side (equal amount of charge carriers on each side; Figure 2.22).

The probability that a minority carrier will reach the external circuit and contribute to the total efficiency of the cell is given by the collection probability f_c (Figure 2.22) and may be given by the following equation:

$$f_c = e^{-x/L_{n/p}}$$
(2.15)



x: The distance from the edge of the depletion region.

Figure 2.22: A solar cell consists of a thin n-side (W_n) and a thicker p-side (W_p) with a depletion layer of width W. The depletion layer penetrates deeper into the p-side because of a lower dopant concentration. The generation rate G is higher closer to the surface of the solar cell while the collection probability peaks in the depletion layer.

As seen from this Eq. 2.15 the collection probability depends on both the distance from the depletion region and the diffusion length of the minority carrier. Minority carriers generated farther away from the depletion area / junction have a much lower probability of contributing to the efficiency of the cell as less of them actually reach the junction before recombination.

All of these contributions have to be balanced when optimizing a solar cell:

- Clearly one wants the junction to be as close to the surface as possible because of the higher generation rate, but since one also depends on good contact between the n-side and top contacts one still have to have a given width of the n-side W_n .

- A larger junction width would be preferable but this width depends on the amount of doping performed, and since a high doping is needed in the top n-side the width of the depletion layer is limited.

The width of the junction W at equilibrium state may be found as a function of dopant concentrations added to both sides by the following equations⁽⁵⁶⁾:

$$W = \left[\frac{2\epsilon kT}{q^2} \left(\ln \frac{N_A N_D}{n_i^2}\right) \left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]^{1/2}$$
(2.16)

A normal doping concentration of the top n-side is $N_D \sim 10^{19} cm^{-3}$ for a planar pn-junction employed in a conventional solar cell, and one may plot the junction width as a function of the acceptor dopant concentration in the p-side (N_A ; Figure 2.23).

 $\begin{array}{ll} T = 300K, & \text{Temperature.} \\ k = 1.380 \times 10^{-23} J K^{-1}, & \text{Boltzmann's constant.} \\ \epsilon = \epsilon_r \epsilon_0 & \\ = 11.8 \times (8.85 \times 10^{-14}) & \\ = 1.044 \times 10^{-12} F cm^{-1}, & \text{Permittivity in silicon.} \\ q = 1.602 \times 10^{-19} C, & \text{Elementary charge.} \\ N_D = 10^{-19} cm^{-3}, & \text{Assumed donor doping.} \\ n_i = 1.5 \times 10^{10} cm^{-3}, & \text{Intrinsic carrier-concentration in silicon.} \end{array}$

The penetration into each side of the pn-junction is based on charge neutrality:

- p-side:

$$x_p = \frac{WN_D}{N_A + N_D} \tag{2.17}$$

- n-side:

$$x_n = \frac{WN_A}{N_A + N_D} \tag{2.18}$$

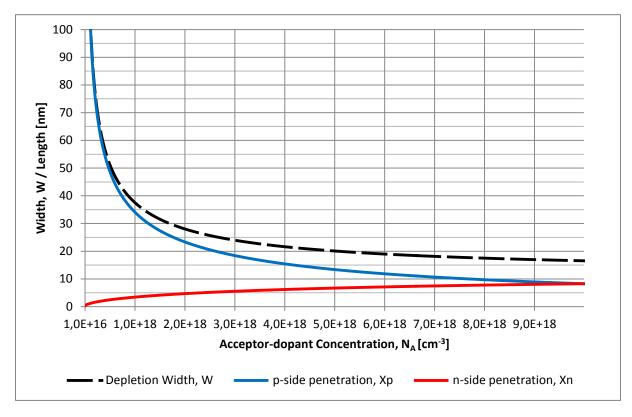


Figure 2.23: The depletion Width W (*black line*), p-side penetration width x_p (*blue line*) and n-side penetration width x_n (*red line*) as a function of acceptor-dopant concentration in the p-side of the junction.

Light absorption:

The amount of light absorbed by the cell depends on the thickness of the cell and normal crystalline silicon cells need a thickness of around ~350nm in order to absorb most of the incoming sun-light $(\sim 100\%)^{(39)}$.

The absorption of light in thin-films depends strongly on the material used as they have a different structure than normal crystalline solar cells described above. Current thin-film technology allows a ~1 μ m thick thin-film to absorb ~100% of the amount of light absorbed by a conventional ~350nm thick silicon solar cell, however most of these cells are based on alternative materials. The light absorption of silicon (amorphous and crystalline) reduces drastically with thickness and a ~2 μ m cell absorbs ~50% of the amount of light absorbed by a ~350 μ m cell^(39, 59).

2.4.2 Silicon Nanowire PN-Junctions

Mainly two types of junctions have been proposed for solar cells based on nanowires; vertical pn-junctions (Figure 2.24 (a)) and radial pn-junctions (Figure 2.24 (b)).

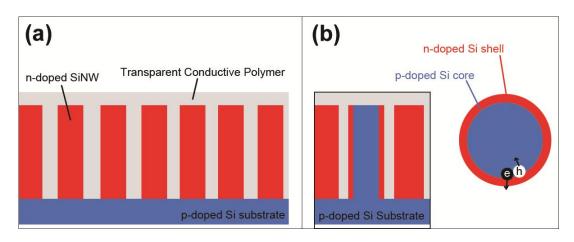


Figure 2.24: Absorption of a solar cell have been improved by covering the substrate with oppositely doped silicon nanowires, while an additional reduction in recombination rate may be achieved by introducing radial pn-junctions.

Light absorption:

The initial introduction of nanowires onto solar cell surfaces was investigated in order to increase the light absorption for thin-film solar cells, and positive results have been published.

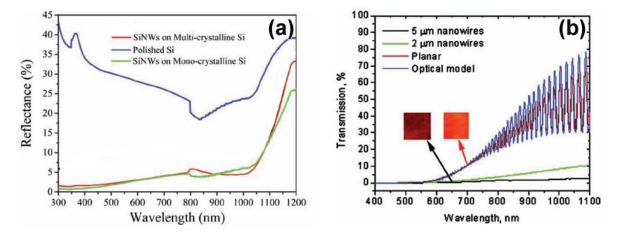


Figure 2.25: A considerable reduction in both reflectance $(a)^{(60)}$ and transmission $(b)^{(61)}$ is observed for a silicon surface when covered in silicon nanowires. Note that these results are attained for nanowires produced by patterned etching in order to investigate how a nanowire patterned surface will affect light-trapping. The latter figure (b) is a result of optical and photocurrent measurements performed on samples of approximately equal thickness. The optical model is generated for a 7.5µm-thin Si-window.

Results by different groups have shown a reduction in both reflectance (Figure 2.25 (a))⁽⁶⁰⁾ and transmission (b)⁽⁶¹⁾ when covering a surface with silicon nanowires which together imply an increased absorption of light by the structure. An increase in optical absorption was confirmed by Th. Stelzner et al, especially at higher wavelengths (Figure 2.26)⁽⁶²⁾.

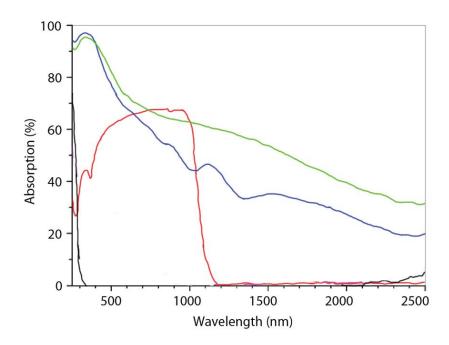


Figure 2.26: Introduction of silicon nanowires on mc-Si (blue line) and glass (green line) substrates shows increased optical absorption compared to a conventional ~375 μ m thick Si wafer (red line). These nanowires have been grown by the same VLS mechanism as employed in this experiment and have an average length of 3 – 6 μ m. The glass substrate has a negligible absorption curve (black)⁽⁶²⁾. Transmission and Reflection spectra were obtained by a UV-vis/NIR spectrometer with a 150nm integrating sphere.

These effects are mainly attributed to the light moving and reflecting between the nanowires, drastically increasing the probability of the light absorbing in the structure. Earlier investigations by Garnet and Yang showed an increase in the path of incident radiation up to a factor of 73 for a surface covered in 5μ m long nanowires compared to a planar surface⁽⁶¹⁾.

Recombination of minority carriers:

By introducing a radial pn-junction (Figure 2.24 (b)) previous experiments have shown a reduction in the recombination tendency of the minority carriers⁽⁷⁾ which is mainly attributed to the reduced diffusion length necessary to reach the depletion region / junction. The diameter of the p-side of the junction is designed to fit the diffusion length of minority electrons, reducing the recombination rate as electrons do not have to diffuse very far. Provided that the trapping density in the depletion region is minimal, large gains in the solar cell efficiency have been observed (up to 11%) for electron diffusion lengths ~100nm⁽⁷⁾.

Dopant addition:

Growth of doped nanowires are preferably done by the addition of additional dopant gases to the growth process. Gaseous diborane (B_2H_6) is used for incorporation of boron-atoms into the structure for p-type doping and gaseous phosphine for incorporation of phosphorus-atoms for n-type doping. It has been shown that the electrical and structural properties of the nanowires are strongly affected by the selection of gases^(3, 63, 64).

In the case of a vertical junction only one dopant-layer is needed, but in order to achieve a radial junction several layers have to be grown. This has been investigated by B. Tian et al⁽⁶⁵⁾ and K. Peng et al⁽⁷⁾ by first growing the p-core by addition of (B_2H_6) to the gas flow at a given temperature and pressure. The shell was then sequentially grown by adding phosphine (PH₃)

to the gas flow at a higher temperature and lower pressure than for the p-core growth, which was done in order to inhibit axial elongation of the silicon nanowire core during shell deposition.

Surface trapping states:

One of the major limitations of employing silicon nanowires is trapping of charge carriers. Nanowires have mainly been found to have a crystalline structure but when exposed to air they are rapidly covered in a thin layer of SiO₂. Because of the large surface-to-volume ratios of nanowires surface properties may have significant influence on the electrical characteristics of the nanowires⁽³⁾, especially the surface between the crystalline core and the SiO₂ layer. Both the SiO₂ layer and Si-SiO₂ interface may contain trapped charges which may affect the band structure of the nanowires in the same way as unwanted contaminations (ex. Au; Ch. 2.2.6); by trapping generated charge-carriers and increasing the recombination rate. It is therefore clear that surface states must be minimized in order to ensure increased solar cell efficiencies. Solutions to this problem mainly aim at increasing the quality of the covering oxide. Adding an annealing step to the processing has proven to reduce the interfacial trap density but the best results is assumed to be attained by replacing the natively formed oxide with a high quality thermal oxide⁽⁶⁶⁾ before the sample is exposed to air.

2.5 Electrical Measurements

In order to determine if the nanowires are successfully doped and get an indication on the amount of implemented dopant atoms in the nanowires one may perform four-point electrical measurements. A principle drawing of a possible four-point measurement method is given with an overview in Figure 2.27 (a) and a more detailed model of the structure in (b).

The contacts are divided into two pairs:

A - D: Used for sending an external current through the nanowire, denoted I_{AD} .

B - C: For measuring the approximate voltage-difference through the nanowire, denoted V_{BC} .

By measuring the voltage-difference for a given current the resistivity of the nanowire is given by

$$\rho_{nw} = \frac{V_{BC}}{I_{AD}} \frac{\pi r^2}{l_2}$$
(2.19)

where πr^2 is given as the area of an assumed circular cross-section of the nanowire, and l_2 is the length between the inner contacts (B-C) excluding the the length buried beneath the electrodes (it is assumed that there is no voltage drop across any single electrode).

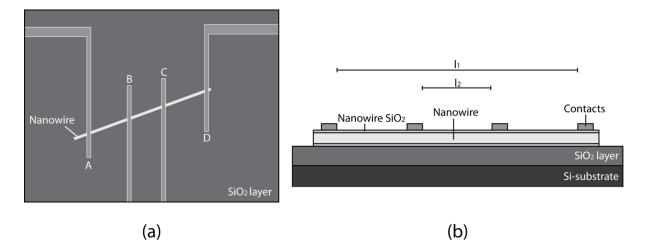


Figure 2.27: An example of a four-point measurement where the Si-substrate is used as a back-gate (a). The cross-section of a contacted nanowire (b).

It is important that the resistance of the voltmeter measuring the voltage-drop is as high as possible in order to force the current to go through the nanowire as current always chooses the easiest route.

For further assessing the measurements one may want to do a voltage sweep and construct an I-V diagram as shown in Figure 2.28. This type of diagram shows the dependence between the measured voltage and the applied current. Note that this diagram depends strongly not only on the nanowire but also on the contacts which will be shown later.

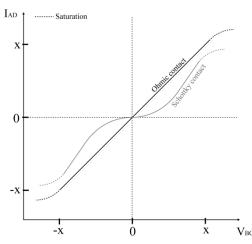


Figure 2.28: Typical I-V curves for Ohmics contacts and Schottky contacts. Ohmic Contacts approximately follow ohms law, giving them a approximately linear I-V curve. Note that most of the bending of the Schottky contacts will disappear when performing four-point measurements.

Eq. 2.19 can only be used to asses the resistivity of the nanowire, on the assumption of a p-type or n-type nanowire. However, it will not confirm

wheter one nanowire is p- or n-type. The determination og p- or n-type must be performed by so-called back-gated measurements of the nanowire in combination with its I-V characteristics.

2.5.1 Back-Gated Measurements

During back-gated measurements a voltage (gate-voltage, V_G) is set over an oxidised (~100-200 SiO₂) Si-substrate in addition to the already mentioned contacts, as shown in Figure 2.29 (a)

A gate-voltage results in a changes in the slope of the recorded I-V curve depending of the type of nanowire doping. Note that it is assumed ohmic contacts in order to attain straight I-V curves, but the same development of the I-V curve is also observed for schottky contacts.

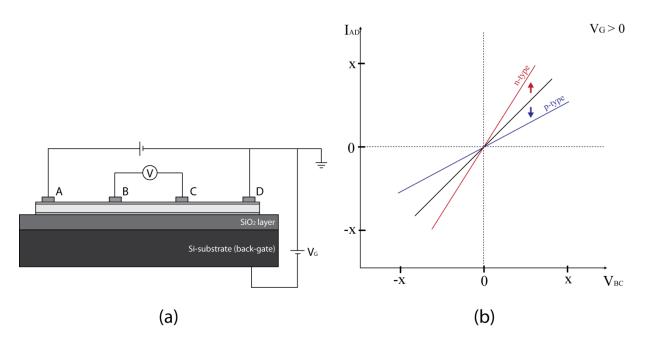


Figure 2.29: An illustrative contacting scheme for back-gated four-point electrical measurements (*a*). The behaviour of the I-V curve with onset of a positive gate-voltage for both n-doped and p-doped nanowires; used to determine if the nanowire is doped or not.

By employing an increasing positive voltage (V_G) to the gate the I-V curves will develop in opposite directions depending on the doping of the nanowire. By applying a positive gate-voltage new electrons will be induced on the other side of the non-conducting oxide / at the nanowire surface and will affect the nanowire in the following way:

- N-type: An n-type nanowire is already doped to contain a surplus of electrons for increased current transport and additional induced electrons will increase this transport even further by making the nanowire more n-type. This will increase the slope of the I-V curve given in Figure 2.29 (b).
- P-Type: A p-type nanowire has been doped to contain a surplus of holes for increased current transport and additional induced electrons will reduce the effective amount of holes in the nanowire making the nanowire less p-type. This will reduce the slope of the I-V curve given in Figure 2.29 (b).

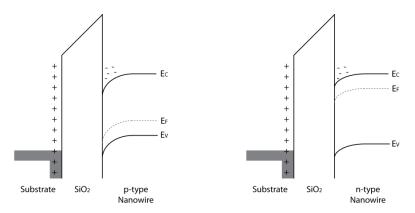


Figure 2.30: An example of an approximated MOS-junction for nanowire measurements. By applying a positive voltage to the gate substrate electrons are induced on the opposite side of the SiO_2 which in this case is a nanowire.

The induction of electrons may be approximated to the same process as of a Metal-Oxide-Semiconductor (MOS) junction in Figure 2.30.

By applying a negative voltage to the gate instead, the opposite will happen; increased current for a p-type nanowire and a reduced current for an n-type nanowire.

Four-point resistivity measurements can normally be used for determining the approximate amount of electrically active p- and n-type carriers in bulk silicon, but as it is expected that the mobility of the carriers in a silicon nanowire is significantly different than in bulk silicon⁽⁶⁴⁾ and this method should therefore not be used. One may therefore only get an indication on the amount of implemented dopant atoms by evaluating the pinch-off voltage.

The pinch-off voltage is the gate-voltage where the nanowire stops conducting and will result in an I-V curve approximately constant at $I_{AD}=0$ for all V_{BC} (horizontal line). A higher pinch-off voltage indicated a higher amount of dopant atoms in the nanowire.

2.5.2 The Contacts

The contacts used for voltage-measurements (B-C) will not be considered in this chapter as they already have been assumed to be negligible. As indicated in Figure 2.28 the I-V curve depends on the contact type established between the nanowire and contacts carrying the current.

There are two types of possible contacts:

- Ohmic contacts
- Schottky contacts

Ohmic contacts:

Ohmic contacts are approximately ideal contacts which allows the same amount of current in both directions, and obey Ohms law;

$$I = \frac{V}{R} \tag{2.20}$$

Completely ohmic contacts have a linear I-V curve as shown in Figure 2.28 but different effects may affect the ohmic quaility of the contact possible decreasing the linearity of the I-V curve. Two criterions exist in order to form ohmic contacts, one for each dopant type:

P-type nanowire: The work function of the semiconductor, Φ_s must be smaller than of the metal Φ_m (Φ_s< Φ_m; Figure 2.31 (a)). The contact is formed by alignment of the Fermi-levels and is performed by electron transfer from the metal to the semiconductor.

Results in a low barrier to hole flow from the metal to the semiconductor which results in an easy flow of holes over the junction even at low voltages.

• *N-type nanowire:* The work function of the metal, Φ_m must be smaller than of the semiconductor, Φ_s ($\Phi_m < \Phi_s$; Figure 2.31 (b)). The contact is formed by alignment of the Fermi-levels and is performed by electron transfer from the semiconductor to the

metal.

Results in a low barrier to electron flow from the metal to the semiconductor which results in an easy flow of electrons over the junction even at low voltages.

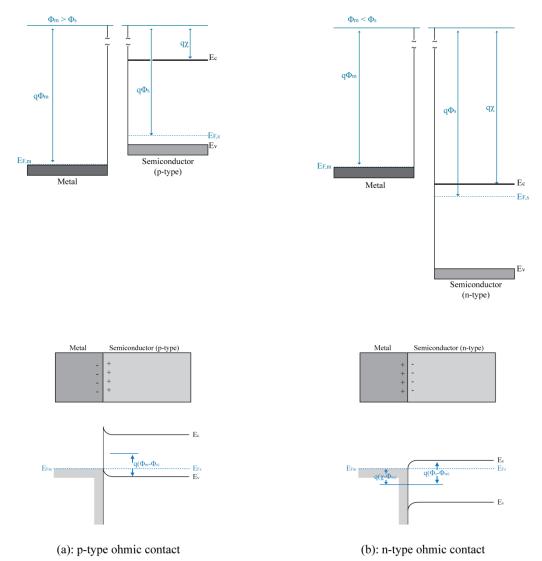


Figure 2.31: (a) Ohmic contact for a p-type semiconductor. (b) Ohmic contact for an n-type semiconductor.

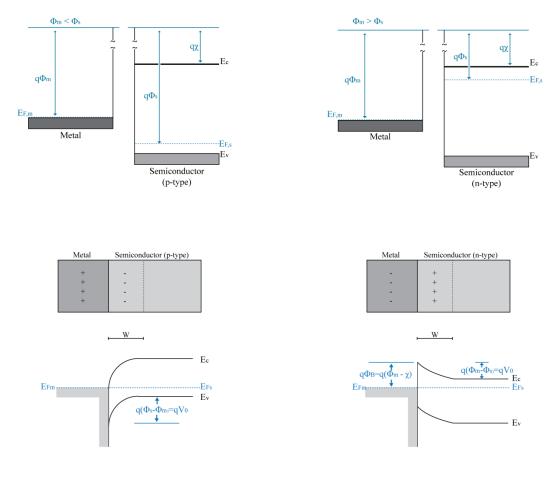
Schottky contact:

Schottky contacts are rectifying with current mainly flowing in one direction because of a large barrier in the other direction. This barrier is a result of the depletion-region formed over the metal-semiconductor junction and a large voltage is needed for particles to pass this barrier in the revese direction.

As for ohmic contacts, two criterions exist in order to form schottky contacts:

P-type nanowire: The work function of the semiconductor, Φ_s must be larger than of the metal Φ_m (Φ_s > Φ_m; Figure 2.32 (a)).

N-type nanowire: The work function of the metal, Φ_m must be larger than of the semiconductor, Φ_s (Φ_m > Φ_s; Figure 2.32 (b)).



(a): p-type schottky barrier

(b): n-type schottky barrier

Figure 2.32: (a) Schottky contact for a p-type semiconductor. (b) Schottky contact for an n-type semiconductor.

Note that since the nanowire is contacted with two oppositely oriented contacts one of the contacts will always be in reverse. This does not affect ohmic contacts which are able to conduct the same amount of current in any direction, but it will limit the Schottky contacts to the reverse saturation current I_0 .

Surface states may lead to Schottky contacts⁽⁵⁶⁾. Surface states appear due to incomplete covalent bonds and other effects which can lead to a charge build-up at the metal-semiconductor junction. One other example is the previously mentioned thin oxide-layer covering the silicon nanowire. Normally, electrons can tunnel through this thin layer (10-20Å), but it is assumed to possibly affect the energetic barrier and the current transport through the junction⁽⁵⁶⁾.

By measuring the resistance between contact A and D (R_{tot}) one may determine the contact resistance (R_c) by using the previously attained nanowire resistivity ρ_{nw} (Eq. 2.5.1). The total resistance in the circuit is a sum of the resistance in the nanowire and the two contacts⁽⁶⁷⁾:

$$R_{tot} = 2R_c + R_{nw} = 2R_c + \frac{\rho_{nw}}{\pi r^2} l_1$$
(2.21)

From this equation the contact resistance may be found to be:

$$R_{c} = \frac{R_{tot} - R_{nw}}{2} = \frac{R_{tot} - \frac{\rho_{nw}}{\pi r^{2}} l_{1}}{2}$$
(2.22)

Ohmic contacts have minimal resistance and are preferred for these types of measurements. Schottky contacts are therefore avoided as far as possible.

Two types of metals have been considered for this project, aluminium and a combination of titanium and gold.

Aluminium:

Aluminium is known to give Schottky-contacts when deposited onto lightly doped / intrinsic silicon without any further treatment.⁽⁶⁸⁾ Since aluminium also works as a p-type dopant for silicon an added annealing step will enable aluminium to diffuse into the silicon forming a heavily doped p^+ -region, and aluminium is known to make an ohmic contact to heavily doped p^+ -doped silicon^(56, 68).

Titanium and Gold:

This is one of the most preferred materials used for making contact^(63, 67, 69, 70). Gold is the major content of the contact and titanium is mainly used to improve the low adhesion between gold and the SiO₂ layer on the substrate surface. Annealing processes have been reported to give nearly ohmic contact with a negligible resistance⁽⁶⁹⁾.

2.6 An Introduction to a Lithographic Process

A lithographic process consists of mainly three parts; a light source (UV-light for photolithography or an electron-beam for electron-beam lithography), a photomask / pattern and a substrate covered in photoresist. A summary of a positive photolithographic process employed in this project is shown in Figure 2.33.

(a) Spin coating and exposure.

The substrate is spin-coated / covered in a polymer-based photoresist which reacts with light and baked at an elevated temperature specific for the photoresist. A photomask is placed above the photoresist and forms a pattern on the photoresist surface. The light source is activated and parts of the photoresist not covered by the photomask are exposed to a given dose of light (exposure dose).

(b) Development.

The sample is soaked in a developing liquid which removes the parts of the photoresist exposed to light.

(c) *Metallization*.

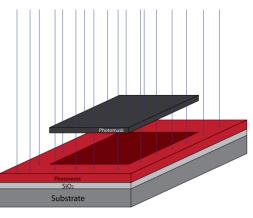
The sample is covered in a metal layer at the desired thickness.

(d) *Lift-off*.

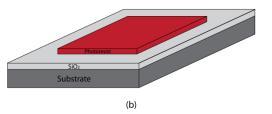
The last step is to soak the sample in acetone which will remove the remaining resist and perform a lift-off of the metal covering the remaining resist. In order to perform a successful lift-off the resist-

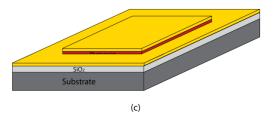
thickness-to-metal-thickness ratio should be ~7:1 in order for the acetone to successfully attack the residing resist.

Note that this explanation mainly covers a standard photolithographic process but may also be applied to electron-beam lithography only with minor changes. Instead of using a UV-light source the resist is designed to react with an electron-beam and instead of using a photomask









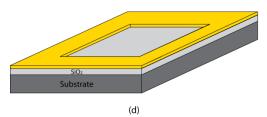


Figure 2.33: A short illustration of a photolithographic process; including exposure (*a*), development (*b*), metallization (*c*) and lift-off (*d*).

a design-file is directly loaded into the electron-beam machine which then moves the electronbeam in the correct pattern.

Some extra notes have to be given for two of the steps in this process:

i. Underdevelopment and overdevelopment (Figure 2.34):

The time the sample is soaked into the developing liquid (step (b); development time) is crucial for the resulting pattern. If the development time is too small the pattern will be underdeveloped resulting in remaining resist-residues in exposed areas. On the other hand, if the development time is too long the pattern will overdevelop resulting in the development liquid etching into unexposed area and destroying the pattern. Great care and thorough investigations should therefore be taken when deciding the best development time.

ii. Successful lift-off.

In order to successfully lift off the metal layer deposited in step (c) above a certain ratio between the photoresist thickness and metal-layer thickness has to be upheld. A general rule is that the photoresist-thickness-to-metal-layer-thickness ratio should be \geq 7: 1 in order to get good lift-off without the use of potential destructive aid (brushing).

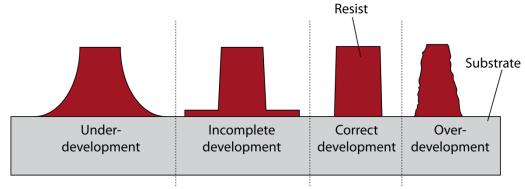


Figure 2.34: The resulting pattern depends on the development time; a too small development time may result in underdevelopment / incomplete development while a too long development time may result in overdevelopment.

3 Experimental

The following chapters will give an overview of the experimental work performed in this project and is divided into several parts:

- *i.* Aluminium Catalysed Growth of Silicon Nanowires (Ch. 3.1). Experiments were performed in order to investigate aluminium as an alternative catalytic material to gold.
- *Growth of Doped Silicon Nanowires (Ch. 3.2).* As solar cells require both positively doped p-type silicon and negatively doped n-type silicon some investigations was performed on the effect from adding dopant gases to the gas-flow on nanowire morphology. This was done with gold as catalytic material because of major oxidation problems when used aluminium as catalytic material.
- Development of a Process for Electrical Measurements of Single Nanowires (Ch. 3.3).
 In order to investigate the actual implementation of dopant atoms into the nanowire structure and not only the morphological effects the development of a four-point probe electrical measurement method was initiated. Because of a limited timeframe this was not finished, but suggestions for further development are given.

3.1 Aluminium Catalysed Growth of Silicon Nanowires

This part of the project employed Si(111) wafers from Siltronix (Table 3.1).

Growth substrates employed.				
Producer:	Siltronix			
Batch:	5578, \$8209			
Process:	Czochralski			
Orientation:	$(111) \pm 0.5^{o}$			
Diameter:	2" (50.8 mm)			
Doping:	P-doped (Boron)			
Resistivity:	< 0.03 Ωcm			
Thickness:	255 – 295 μm			

 Table 3.1: Silicon substrates employed for aluminium-catalysed growth.

3.1.1 Substrate Preparation

In order to remove pre-existing organic and ionic contaminations on the wafer surface the wafers had to be cleaned before further processing and use. The RCA-Clean is a common and well documented cleaning procedure⁽¹⁰⁾ and was chosen as the preferred cleaning method in this experiment., The procedure consists of three immersion steps as shown in Table 3.2.

Step	Name	Chemicals	Immersion time	Properties
1	Standard Clean 1, SC-1	$H_2O/NH_3/H_2O_2$	10 min	Removal of organic
		(5:1:1)		contamination
2	HF etch	5% HF diluted	2 min	Removal of oxide
		in H ₂ O		layer.
3	Standard Clean 2, SC-2	H ₂ O/HCl/H ₂ O ₂	10 min	Removal of ionic
		(5:1:1)		contamination.

Table 3.2: Immersion steps for RCA wafer cleaning.

This cleaning was performed step-wise in batches of 10 wafers at a time. The Standard Clean (SC-1 and SC-2; Table 3.2) solutions were heated to 70°C before immersing the wafers. In

order to cover the whole area of the wafers, 500ml of deionized water was used in combination with 100ml of each required acid/base. The wafers were rinsed in DI water between each step and dried by a N_2 -gun after wafer cleaning (after step 3). This concludes the batch processing of the wafers and further processing is performed on single wafers only.

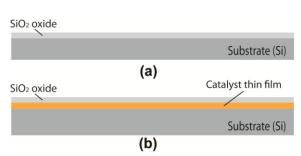


Figure 3.1: Si substrate with an oxidized surface (top). It the case of silicon diffusion through the Au-film, silicon may oxidize on top of the film (bottom).

During this treatment a protective oxide layer

 (SiO_2) will form on the substrate (Figure 3.1 (a)) because of exposure to air. This was left untreated as it protects the wafer during storage and until further processing and was not to be removed before right before catalyst deposition (in the next step).

3.1.2 Catalyst Deposition

The protective oxide had to be removed before catalyst deposition in order to enable contact between the catalyst and the silicon. This was done by immersing the wafer into 5% HF diluted in H_2O for 2 min. The sample was then rinsed in DI-water and dried by a N2-gun. If the water is not repelled from the substrate surface some more etching should be performed until the water is completely repelled.

In order to enable VLS nanowire growth, a thin film of the desired catalyst material had to be deposited on the wafer surface. The deposition was performed in a Pfeiffer Classic 500 E-Beam Evaporator. In this experiment, different types of deposits were deposited:

Deposit 1: 15nm of Aluminium.

Deposit 2: 15nm of Aluminium and 5nm of Tin.

Tin was deposited as an attempt to prevent/minimize oxidation of the aluminium thin-film (Ch. 2.3.2).

The following parameters where used for deposition (Table 3.3) in the E-Beam Evaporator:

Parameter	Aluminium	Tin		
Vacuum	$\sim 10^{-8} Torr$	$\sim 10^{-8} Torr$		
Thickness	~15 <i>nm</i>	$\sim 5nm$		
Current	~41 <i>mA</i>	~47 <i>mA</i>		
Deposition rate	~1.8Å/s	~0.4Å/s		

 Table 3.3: Deposition parameters used for E-Beam Evaporation.

It has been found that some silicon might have diffused through the catalyst thin-film and oxidized as a SiO₂ thin-film on top of the film⁽⁷¹⁾ (Figure 3.1 (bottom)) and should have been etched by $HF^{(2)}$. Since 5% HF also etches away the Al-film in a matter of seconds this step had to be removed. The sample was inserted into the CVD reactor, which was immediately evacuated to vacuum (~10⁻⁷ Torr).

3.1.3 Nanowire Growth

The deposition was performed in a Plasmalab System 100 PECVD chamber by Oxford Instruments (Figure 3.2). Several different growth environments were tried. As aluminium-catalysed growth has not been tried before in this group, some investigation had to be performed in order to find optimal growth conditions for this system. The typical recipes used for growth is described in Table 3.4.

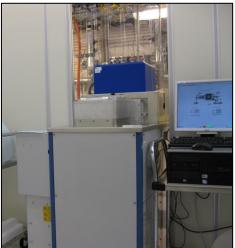


Figure 3.2: Plasmalab System 100 PECVD (Oxford Instruments)

Step	Recipe 1	Recipe 1 Recipe 2		
1	Pump	Pump	Pump	
2	Purge	Purge	Purge	
3	Pump to base	Pump to base	Pump to base	
4	Si deposition	NH ₃	Plasma	
		Cleaning	cleaning	
5	Repeat 3	Repeat 2	Repeat 2	
6	Pump	Pump Pump		
7	Purge Purge		Purge	
8	Loop Loop		Loop	
9	Pump to base	Si deposition	Si deposition	
10	-	Repeat 3	Repeat 3	
11	-	Pump	Pump	
12	-	Purge	Purge	
13	- Loop		Loop	
14	-	Pump to base	Pump to base	

 Table 3.4: Different recipes used in the experiment. Steps between 'Loop' and 'Repeat X' are repeated X times before moving on to the next steps.

The standard chamber cleaning steps are marked in grey in Table 3.4, and have the purpose of cleaning the chamber before and after deposition. The steps marked in white are recipe specific processing steps used for growth. Recipe 1 is the standard recipe earlier used for Aucatalysed growth⁽²⁾, which gave good results. Recipe 2 and 3 are modified versions of this recipe, with additional cleaning steps as an attempt to reduce expected oxidation problems (Ch. 2.3.2) and to improve the growth conditions of aluminium catalysed growth.

A closer look on the cleaning steps:

Two types of cleaning steps are introduced into respectively recipe 2 and 3; a chemical cleaning step ('NH₃ Cleaning' in recipe 2) and a plasma cleaning step ('Plasma cleaning' in recipe 3).

*NH*₃ *Cleaning* (*Recipe 2*):

Gaseous NH_3 (40 sccm) was introduced into the chamber together with N_2 (100 sccm) in order to achieve a NH_3 partial pressure of 200 mTorr. This step ran for 5 minutes at 580°C.

Plasma cleaning (Recipe 3):

This step also introduces 200 mTorr of NH_3 in the chamber as in the previously described cleaning step, but plasma is also activated at a power of 20W. This creates much harsher cleaning environment which may be more effective against Al_2O_3 . This step ran for 5 minutes at 500°C, which is the maximum possible temperature when using plasma in this system.

Si deposition steps:

The wafers where exposed to different parameters during growth, and is described in Table 3.5.

Series	Temp.	Al -	Deposit	0	100	500	1000	1500
	-	cleaning	-	mTorr	mTorr	mTorr	mTorr	mTorr
1	580°C	No clean	15nm Al	-	-	-	013	-
		(Recipe 1)						
2	580°C	NH ₃ clean	15nm Al	021	022	023	024	025
		(Recipe 2)						
3	580°C	Plasma clean	15nm Al	031	-	-	032	-
		(Recipe 3)						
4	580°C	No clean	15nm Al	-	-	041	042	-
		(Recipe 1)	+ 5nm					
			Sn					
5	580°C	NH ₃ clean	15nm Al	-	-	-	051	-
		(Recipe 2)	+ 5nm					
			Sn					
6	580°C	Plasma clean	15nm Al	-	-	-	061	-
		(Recipe 3)						

 Table 3.5: Growth parameters for Al-catalysed growth regimes. The given pressures are for the partial pressure of SiH₄.

In order to get the desired partial pressures SiH_4 was diluted in Ar which is an inert gas. The correct partial pressures for SiH_4 (p_{SiH4}) was set by adjusting the total chamber pressure and the gas-flows (Table 3.6).

SiH ₄ partial pressure	Total chamber pressure	SiH ₄ flow	Ar flow rate
(p _{SiH4})	(p _{tot})	rate	
100 mTorr	1000 mTorr	20 sccm	180 sccm
500 mTorr	1000 mTorr	20 sccm	20 sccm
1000 mTorr	1000 mTorr	40 sccm	-
1500 mTorr	1500 mTorr	40 sccm	-

 Table 3.6: Chamber pressures and gas-flows used for attaining the desired SiH4 partial pressures.

After recipe programming the process was started. In this experiment the samples was grown for 45 minutes each (Si-deposition step).

When the recipe was finished, the loading chamber was vented to air-pressure, and the sample was removed to a storage box. The chamber was now ready for another sample, starting with a 2 min HF-etch before catalyst deposition (end of Ch. 3.1.1).

A short summary of the whole growth process is listed in Table 3.7.

Step	Description					
The fo	The following steps where performed on all wafers simultaneously, as a batch.					
1	RCA Clean, Step SC-2; 10 min. in pre-heated solution + DI Rinse.					
2	5% HF etch; 2 min. + DI Rinse.					
3	RCA Clean, Step SC-1; 10 min. in pre-heated solution + DI Rinse.					
4	Drying of wafers by N ₂ -gun.					
5	Pre-heating of the CVD reactor to parallel specific temperature.					
The ne	xt steps where performed on single wafers only, one by one.					
6	5% HF etch; 2 min. + DI Rinse					
7	Drying of wafer by N ₂ -gun.					
8	Deposition of the catalytic Al-film (15nm) and a possible protective Sn-film (5nm) by					
	e-beam evaporation.					
9	Wafer was put into the CVD loading-chamber and evacuated to low vacuum.					
10	Correct growth parameters where set in the chosen CVD-recipe.					
11	The CVD process was started.					
12	After completed process, the load lock was vented to air and wafer removed.					
These	<i>These steps</i> (6 - 12) <i>where repeated for all wafers in the parallel.</i>					

Table 3.7: A general summary of the whole nanowire growth process.

3.2 Growth of Doped Silicon Nanowires

This part of the project employed silicon substrates from Siltronix, given in Table 3.8.

Gr	owth Substrates #1	Growth Substrates #2		
Producer:	Siltronix	Producer:	Siltronix	
Batch:	5578, \$8209	Batch:	6669, S8667	
Process:	Czochralski	Process:	Czochralski	
Orientation:	$(111) \pm 0.5^{o}$	Orientation:	$(111) \pm 0.5^{o}$	
Diameter:	2" (50.8 mm)	Diameter:	2" (50.8 mm)	
Doping:	P-doped (Boron)	Doping:	P-doped (Boron)	
Resistivity:	$< 0.03 \ \Omega cm$	Resistivity:	1-30 Ωcm	
Thickness:	255 – 295 μm	Thickness:	180-220 μm	

Table 3.8: Substrates used for growth of doped nanowires.

The following gases were employed in this part of the investigation:

3.2.1 Substrate Preparation

The substrates used for growth of doped nanowires were prepared in a similar way as for aluminium catalysed growth (See Ch. 3.1.1). The same three-step wet clean process as described in Table 3.2 where applied also in this case.

3.2.2 Catalyst Deposition

Because of the unpromising results attained for aluminium catalysed growth (Ch. 4.1), this investigation was done with gold as a catalyst instead which earlier have been proven to give good results⁽²⁾. After an initial 2 min HF-etch, gold was deposited by a Cressington 208 HR B sputter coater, which is designed for coating substrates with 1-20 nm thick films. This is much faster than previously used E-Beam deposition (for aluminium deposition; Ch. 3.1.2), and earlier results⁽²⁾ have proven this as a reliable deposition method. It was important to perform the sputtering as fast as possible after etching to prevent unnecessary oxidation of the Siwafer; preferably directly after the HF-etch.

The following parameters where used for the Cressington 208 HR B:

- Mode: Automatic.
- Current: 20 mA.
- Target density: 19.30 (Au).
- Tooling factor: 1.8.
- Film thickness: 2nm.

After catalyst deposition some silicon might have diffused through the Au-layer⁽⁷¹⁾ and oxidized on top of this layer (See Figure 3.1), as noted in Ch. 3.1.2. This possible oxide-layer may be removed by HF without notably affecting the gold layer as Au is more resistant to HF than Al. The sample was dipped into a 5% HF solution for 10 sec and rinsed in DI water before dried by a N_2 -gun.

The sample was then put into the CVD chamber and evacuated to vacuum.

3.2.3 Nanowire Growth

Growth of doped nanowires was performed with the same CVD recipe (Recipe 1) as used for earlier Au-growth investigations (Table 3.4)⁽²⁾ but with minor changes in the gas flows in step 4.

The experiment was designed with constant SiH₄ partial pressure and was set to 100 mTorr at a growth temperature of 500°C (Table 3.6) (as these conditions have been shown to grow approximately vertical (111) oriented nanowires⁽²⁾). 100 mTorr was obtained for intrinsic samples by using the correct SiH₄/Ar ratio from Table 3.6. When dopants were added the flow had to replace some of the Ar flow. The total flow of non-SiH₄ gas should always be 180 sccm.

	Table 3.9: The following samples were set at a growth time of 60 min.								
Sample	р _{SiH4}	Temp.	r_{dopant}/r_{SiH_4}	SiH ₄	Ar flow	PH ₃ /B ₂ H _{6, mix}			
	[mTorr]	[°C]		flow	[sccm]	flow [sccm]			
				[sccm]					
Series 1 (Series 1 (0.1% B_2H_6 dopant gas):								
DB11	100	500	-	20	180	-			
DB12	100	500	-	20	180	-			
DB13	100	500	5.0×10^{-5}	40	358	2			
DB14	100	500	5.0×10^{-4}	20	170	10			
DB15	100	500	5.0×10^{-3}	5	20	25			
DB16	100	500	-	20	180	-			
Series 2 ($(10\% PH_3 do)$	pant gas)							
DP21	100	500	-	20	180	-			
DP22	100	500	-	20	180	-			
DP23	100	500	5.0×10^{-3}	40	358	2			
DP24	100	500	1.0×10^{-2}	20	178	2			
DP25	100	500	1.0×10^{-1}	20	160	20			
DP26	100	500	_	20	180	-			

The samples desired in this investigation are given in Table 3.9.

Table 3.9: The following samples were set at a growth time of 60 min

The recipe was programmed with the correct growth parameters needed for each sample:

- Temperature: 500°C.
- Gas flows: $SiH_4 + Ar (+ PH_3/B_2H_6)$.
- Chamber pressure: 1000 mTorr.
- Growth time (Si-deposition step): 60 min.

The process was started and the samples were exposed to respective gases for 60 minutes; including the pre- and post-cleaning steps the total growth time was about 80 minutes. When the recipe was finished, the loading chamber was vented to air-pressure and the sample was removed to a storage box. The chamber was now ready for another sample, starting with a 2 min HF-etch before catalyst deposition (Ch. 3.2.2).

3.3 Developing a Process for Single-Nanowire Electrical Measurements

In order to be able to measure electrical properties of single nanowires and to give an estimate on the actual implementation of dopant atoms into the nanowire structure, a contact-structure

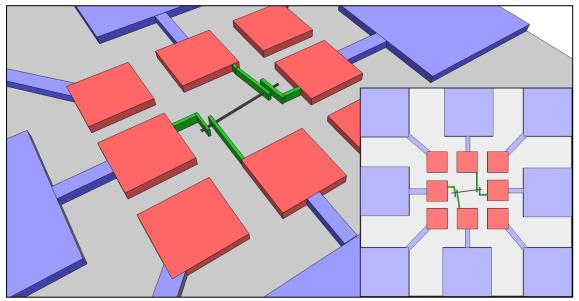


Figure 3.3: An illustration of the desired structure for electrical measurements on single nanowires. A single nanowire (black) was to be dispersed onto an oxidised silicon substrate (gray) and electrically connected through three interconnecting layers of contacts; the inner nanowire contacts (green) produced by electron-beam lithography and the inner contact-pads (red) and outer contact-pads (blue) both made by normal photolithography.

connecting single nanowires to larger contact pads had to be designed and produced. An illustration of the designed structure is given in Figure 3.3 and is divided into different parts separated by colour, and each of these parts needed different processing procedures.

Oxidized substrate (grey):

In order to electrically isolate the dispersed nanowires and to enable back-gated measurement (Ch. 2.5.1) the employed Si-substrates were covered in 200nm of SiO_2 which was predeposited by Chemical Vapour Deposition (Ch. 3.3.2).

The complete contact structure was designed to consist of three interconnecting layers of metal-contacts and each layer was manufactured separately.

Inner contact-pads (red):

The inner contact-pads were the first contacts to be printed on the sample surface after substrate oxidation and the purpose of these contacts was to serve as an intersection between the nanowire contacts (*green*) and outer-contact pads (*blue*). These contacts were made by a standard photolithographic method.

Nanowire contacts (green):

These contacts were designed in order to connect a nanowire to the electrical circuit. As this project focused on four-point measurements four nanowire contacts were needed. As these contacts had to be small (< 1μ m) they had to printed by electron-beam lithography instead of standard photolithography.

Outer contact-pads (blue):

These contacts were designed to serve as main contacts for external probe connections. The contacts were to be made by the same standard photolithography process as used for the inner contact-pads.

Before any contacts could be made, an investigation had to be done on optimizing the lithographic processes. A correct and useable photoresist had to be found for each contact type, and since the resolution and the ability for lift-off strongly depends on the thickness of the photoresist film an optimal photoresist-thickness had to be found. This chapter will therefore cover this lithographic optimization in addition to the design of the lithographic patterns needed for photolithography.

The complete process for developing the contact-structure was designed to follow the following sequence:

- *i.* Designing the necessary lithographic patterns, Ch. 3.3.1. The desired patterns for inner and outer contact-pads were designed and printed onto a photomask.
- *Oxidation of silicon wafers, Ch. 3.3.2.* Silicon wafers were oxidised in order to isolate dispersed nanowires and to enable back-gated measurements.
- *Cutting of silicon wafers into samples, Ch. 3.3.3.*The previously oxidised silicon wafers were cut into samples of smaller sizes.
- *iv.* Formation of the inner contact-pads, Ch. 3.3.4.The inner contacts were printed in an orientation pattern onto the sample by photolithography and the photomask previously ordered.
- *v.* Dispersion of silicon nanowires, Ch. 3.3.5.Silicon nanowires were scraped off the growth-substrate and dispersed on a sample.
- *vi.* Nanowire localisation and pattern-design, Ch. 3.3.6.
 A single nanowire was located and the position was noted in order to design correct nanowire contacts. A contact-pattern was designed in CleWin4 specifically for the chosen nanowire.
- *vii. Formation of the nanowire contacts, Ch. 3.3.6.* The previously designed contact-pattern was printed by electron-beam lithography.
- *viii.* Formation of the outer contact-pads, Ch. 3.3.7.The outer contact-pads designed for probe-contacting were printed by photolithography and the photomask previously ordered.

ix. Sample ready for four-point electrical measurements.
 The sample was now ready for electrical measurements. Note that because of timelimitations a complete structure ready for electrical measurements were not reached.

3.3.1 Designing the Lithographic Patterns

The inner and outer contact pads were to be printed by normal photolithography and therefore needed a photomask. A photomask consists of a glass plate (Figure 3.4 (a)) covered in a thin layer of chromium (b) as chromium is not transparent to UV-light. The mask is normally placed between the light-source and the substrate in a mask-aligner (Ch. 2.6).

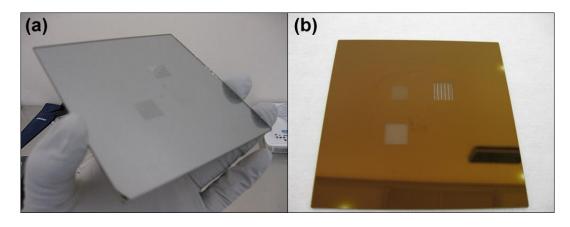


Figure 3.4: The photomask employed in this process. It consists of a glass-based front-side and a chromium-based back-side. Chromium is used as it blocks UV-light.

A photomask may contain several patterns as it can be moved around independently of the substrate. In this case, the patterns shown in Figure 3.5((a) and (b)) were designed separately in CleWin 4; a pattern design software for Windows, and put together onto a 5" photomask as shown in Figure 3.4 (b) (Note that photomask also consists of several patterns not used in this project). The mask was ordered with the designed patterns from The Angstrom Microstructure Laboratory in Uppsala.

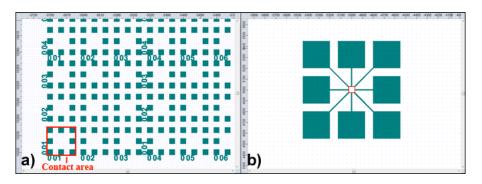


Figure 3.5: The four different patterns designed i CleWin4 for this particular project. (a) A part of the orientation pattern consisting of inner contact-pads. (b) The outer contact-pads. (c) A possible solar cell pattern. (d) Dots for patterned growth of silicon nanowires.

The pattern in Figure 3.5 (a) consists of the inner contact pads and will be printed all over the sample, and will additionally be used as an orientation pattern in order to orientate and to locate nanowires on the sample surface in a microscope. The outer contact pads are given in the pattern in Figure 3.5 (b).

Inner contact-pads / orientation pattern, Figure 3.5 (a):

Note that this design consists of a pattern of inner contact-pads and not only one single contact-area (red square in Figure 3.5 (b)). When the sample gets dispersed with nanowires one must be able to find the exact position of the nanowire desired to contact and this becomes possible with an orientation pattern. This implies that the sample is patterned with the inner-contact-pads *before* the nanowires are dispersed and possibly reduces the chance of finding usable nanowires as they have to be located within a given *Contact Area*. This was however not assumed to become a problem because of the large amount of dispersed nanowires.

A given contact area consists of 8 rectangular contacts and is shown by a red square in Figure 3.5. This square was designed to fit inside the red marked area of the outer contact-pads in design (b). The inner contact pads are designed as $10 \times 10 \mu m$ rectangular contacts, and each contact area has an area of $50 \times 50 \mu m$.

Outer contact pads, Figure 3.5 (b):

As presented in Figure 3.1 these are the contacts used for connecting the electrical probes and are made large enough to be able to accurately position the probes in a light-microscope. The pads are designed as 250 x 250 μ m rectangular contacts and the lines moving into the center are designed to fit accurately into the *Contact Area* defined in (a) and have a diameter of 10 μ m.

3.3.2 Oxidation of Silicon Wafers

In order to achieve back-gated measurements, a \sim 200nm thick SiO₂ layer had to be grown on the wafers. This oxidation was performed in a Plasmalab System 100 PECVD system with the following recipe (Table 3.10):

Table 3.10: SiO ₂ growth recipe.			
Step	Recipe 1		
1	Pump		
2	Purge		
3	Pump to base		
4	SiO ₂ deposition		
5	Repeat 3		
6	Pump		
7	Purge		
8	Loop		
9	Pump to base		

The steps marked in grey are standard cleaning steps necessary for every CVD growth-process.

SiO₂ deposition:

This is the actual deposition step, where a ~200nm thick SiO_2 layer is grown on the whole wafer. The wafer was inserted into the PECVD chamber holding a temperature of 300°C and exposed to the gas-mixture described in Table 3.11 for 4 min.

in the SiO ₂ deposit	ion step (Step 4).
Parameter:	Value:
Chamber temperature	300°C
Chamber pressure	1000 mTorr
Growth time	4 min
Plasma power	20W
Gas mixture	SiH ₄ : 8.5 sccm.
	N ₂ O: 770 sccm.
	N ₂ : 161.5 sccm.

Table 3.11: Parameters used for SiO_2 growth in the SiO₂ deposition step (Step 4).

3.3.3 Cutting of the Wafers into Samples

Each lithographic pattern was designed to fit on a ¹/₄ of a 2" wafer and the wafers were therefore cut into four equal pieces in order to save substrate material and to make the samples fit in the EBL machine. The cutting was performed with a Dynatex DXIII Scriber & Breaker (Figure 3.6 (a)) which is an automatic scribing and breaking tool.

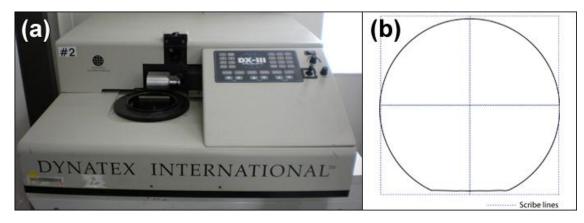


Figure 3.6: (a) Dynatex DXIII Scriber & Breaker used in this project. (b) Scribing lines used in order to break 2" wafers into four separate samples.

By cutting three wafers this way, 12 samples were made. A summary of the procedure is shown in Table 3.12.

Step:	Description:
1	The wafer is placed on a sample holder and put onto the scriber.
2	The scriber is programmed with the correct parameters.
3	X and Y alignment is performed in order to align the wafer for correct scribing.
4	Positions for initial scribe-streets are chosen (Figure 3.6 (b)).
5	The scribing process is started.
6	Breaking is performed with correct parameters.
7	Samples are collected and cleaned in acetone and isopropanol.

Table 3.12: A summary of the scribing and breaking process.

The following parameters were found to correctly scribe and break the wafers into the desired samples (Table 3.13):

Parameter: Value:		Parameter:	Value:	
General parameters:		Break parameters:		
Mode:	Scribe &	Method:	Anvil	
	Break			
Wafer diameter:	60.8 mm	Pressure:	82.7 kPa	
Thickness:	250 µm	Anvil height:	0.4 mm	
Step size:	25.4 mm	Anvil gap:	0.35 mm	
Set Y=X	Yes	Dwell time:	0.1 s	
Scribe para	meters:	Cycle time:	0.2 s	
Method:	Continuous	Alignment p	arameters:	
Impulse bar	0 µm	Theta & First street	Align theta for x axis	
height:			only	
Scribe extension:	76 µm	X-Scribe step	Adjust X	
		compensation		
Scribe force:	1800 cnts	X-Break step	Adjust X	
		compensation		
Scribe angle:	36°	-	-	
Scribe speed	20 mm/s	-	_	
Approach speed	12 mm/s	-	-	
Set Y=X	Yes	-	-	

 Table 3.13: Programmed parameters for scribing and breaking of wafers.

3.3.4 Orientation-Pattern and Inner Contact-Pads

As noted in the previous chapter, the inner contact pads were to be made by standard photolithography. A typical photolithographic process follows the following sequence:

- *i.* Sample cleaning: Cleaning of the sample surface with acetone and isopropanol.
- *ii. Spin-coating and soft-baking:* The sample is spin-coated with the chosen photoresist and baked on a hotplate.
- *iii. Exposure:* Exposure and printing of the pattern onto the resist.
- iv. Development: Removal of unexposed resist.
- *v. Metallization:* Deposition of desired metal onto the sample.
- vi. Lift-off: Removal of remaining resist and metal deposition on top of it.

A more detailed version of the employed processing-steps will now be presented:

<u>Cleaning:</u>

Before any lithographic steps the oxidized sample had to be cleaned and was done by spraying it with acetone and isopropanol before drying it by an N_2 -gun.

Spin-coating:

The sample was put onto a spin-coater and covered in a desired photoresist by using a pipette. The photomask developed for printing this pattern is positive, and a positive photoresist was needed. NTNU Nanolab offered two types of positive photoresists for near-UV exposure, Megaposit SPR700 1.0 and Microposit S1813 G2. It was desired to deposit ~90nm of metal for these contacts and if a minimum ratio between the resist-thickness and metal-thickness of ~7:1 was to be upheld a minimum resist-thickness of 630nm was needed.

By referring to the data-sheets provided for each photoresist and their respective spin-curves (Figure 3.7 (a) and (b)) $^{(72, 73)}$ none of these resist could spin this resist-thickness, but Microposit SPR700 1.0 seemed to be able to spin thinner films than the Microposit S1813 G2. The new resist-thickness was therefore set to ~900nm and Megaposit SPR700 1.0 was chosen as it seemed to be able to spin this thickness at 6000 RPM which was the max-speed of the spin-coater. The effect on the resolution from an increase in photoresist-thickness from 630nm to 900nm is very small for such large features as printed in this part of the project. It was important not to use to much resist, but only as much as needed to cover the substrate. The vacuum was turned on and the spin-coater was programmed with the correct spin-speed, time and acceleration. After spin-coating the sample was soft-baked on a hotplate for 60 sec at 95°C in order to evaporate the solvent in the resist⁽⁷³⁾.

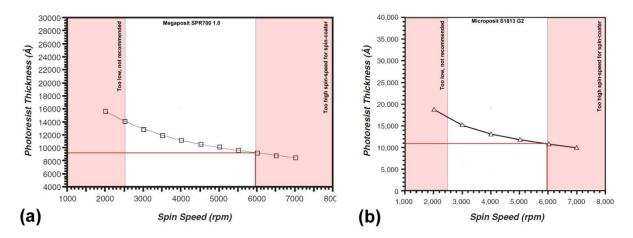


Figure 3.7: The thickness of the spin-coated photoresist is determined by the spin-speed used on the spin-coater. The spincurves for Megaposit SPR700 1.0 and Microposit S1813 G2 is given in figure (a) and (b) respectively.

Exposure, Figure 2.33 (a):

The next step was to expose the sample in a mask-aligner. As this experiment employs positive lithography, the area which is exposed to the incoming UV light will become soluble and possible to remove by a suitable developer. Exposure was performed in an EVG 620 Nanoimprint System which employs a 350-450nm UV light source. The wafer was loaded into the machine which was programmed with the recommended exposure dose which in this case was 125mJ/cm^2 as specified in the SPR700 datasheet⁽⁷³⁾.

Development, Figure 2.33 (b):

In order to remove the exposed resist the sample had to be developed in a suitable developer. MF 26A developer was used for the SPR700 resist. The development time is a crucial factor

in this step, and in order to stop the development and prevent overdevelopment the sample had to be removed from the developer immediately after the development time had been reached and put into a glass of DI water for rinsing. The sample was then dried by a N_2 -gun. The sample was now observed in a light-microscopy for quality-control before metallization.

Metallization, Figure 2.33 (c):

Metallization is the process of depositing the desired metal onto the substrate and was in this case performed in a Pfeiffer Classic 500 E-Beam Evaporator. The sample was inserted into the evaporator which was programmed with the desired metal thickness. Two types of deposits were employed; Al was used alone (90nm) while Au (80nm) was used in combination with Ti (10nm) in order to improve the adhesion of Au.

Lift-off, Figure 2.33 (d):

The last step covers the removal of remaining resist and the metal layer on top of it. This is performed by soaking the sample in acetone as long as necessary. As noted, it is very important to have a correct ratio between the metal and photoresist thickness for lift-off to be successful. The reason for this is that the acetone needs enough room to get to the photoresist and to dissolve it. The sample was then sprayed in isopropanol and dried with a N₂-gun after lift-off and could now be investigated in light-microscopy / scanning electron microscopy for quality-control.

Several samples where produced in order to find the correct parameters to use for the final processing (Table 3.14) which in this case mainly was the development time:

	orientation pattern.					
Sample	Spin speed	Thickness ⁽⁷³⁾	Development	Metal thickness		
	[RPM]	[nm]	time [sec]	(Al or Au + Ti)		
OM01	6500	~900	20	50nm Al		
OM02	6500	~900	15	-		
OM03	6500	~900	10	50nm Al		
OM04	6500	~900	10	-		
OM05	6500	~900	5	-		
OM06	6500	~900	2	90nm Al		
OM07	6500	~900	1	-		
OM08	6500	~900	3	10nm Ti + 80nm		
				Au		

 Table 3.14: The different samples and their employed parameters for determination of the best

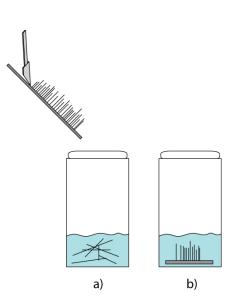
As seen from the table no further testing was performed on the photoresist thickness as the initial lift-off results were acceptable.

3.3.5 Dispersion of Nanowires

Two methods where employed in order to try to disperse and separate nanowires (Figure 3.8):

- i. *Scraping (a):* Nanowires where scraped of the growth substrate directly by a scalpel into a beaker filled with a small amount of isopropanol.
- ii. *Immersion (b):* A small piece of the growth sample is directly immersed into a beaker filled with a small amount of isopropanol.

The beakers were sealed and put into a sonication bath at medium/strong strength at varying lengths of time.



Different samples with different parameters where inserted into the sonication bath (Table 3.15):

Figure 3.8: (a) Scraping of nanowires of substrate into a beaker. (b) Immersion of a small piece of substrate into a beaker.

Sample	Туре	Amount of	Sonication	Sonication
		IPA	length	strength
IM01	Immersion	~1ml	2 min	Medium
IM02	Immersion	~1ml	2 min	Strong
IM03	Immersion	~2ml	5 min	Medium
IM04	Immersion	~2ml	5 min	Strong
IM05	Immersion	~5ml	10 min	Medium
SC01	Scraping	~1ml	2 min	Medium
SC02	Scraping	~1ml	2 min	Strong
SC03	Scraping	~2ml	5 min	Medium
SC04	Scraping	~2ml	5 min	Strong
SC05	Scraping	~5ml	10 min	Medium

 Table 3.15: Different samples tried for nanowire separation and dispersion.

After treatment in sonication bath, a tiny amount of liquid where removed with a pipette and dripped onto a sample prepared with an orientation pattern (Ch. 3.3.4). The sample was then inserted into a SEM in order to look for well separated single nanowires and if these nanowires were to be used for contacting the location of these nanowires was noted and SEM-images taken for further treatment.

3.3.6 Nanowire Contacts

Because of the resolution limit of normal photolithography at approximately $1\mu m^{(10)}$ the nanowire contacts had to be made by electron-beam lithography which is able to produce structures down to nanometer-accuracy. Lithographic testing was performed in order to optimize the following parameters:

- Correct photoresist.
- Correct ratio between photoresist and metal deposit.
- The minimum distance between two initially separated structures.
- Correct exposure dose.
- Correct development time.

Electron Beam lithography employs approximately the same lithographic procedure as described for photolithography (Ch. 3.3.4) but with some minor changes.

Lithographic Procedure:

<u>Cleaning:</u>

Before any lithographic steps the oxidized sample had to be cleaned and was done by spraying it with acetone and isopropanol before drying it by an N_2 -gun.

Spin-coating:

This investigation employed a group of 950PMMA photoresists from MicroChem which is the main photoresist group used for electron-beam lithography at NTNU Nanolab. The following species were investigated:

- PMMA A2 (2% in anisole).
- PMMA A4 (4% in anisole).
- PMMA A7 (7% in anisole).
- PMMA C4 (4% in chlorobenzene).

The PMMA series resists are formulated with two resins of different molecular weight, and the only difference between the PMMA resists is the different compositions of these resins and different solvents. The spin-curves for the resists are given in appendix B.

The sample was put on the spin-coater and spin-coated at the desired parameters:

- Spin-speed: Variable.
- Spin-acceleration: 1000 RPM/sec.
- Spin-time: 45 sec.

This group of photoresists was soft-baked at 180°C for 60 sec on a hotplate⁽⁷⁴⁾.

As presented (Ch. 2.6) a guiding rule states that the ratio between the metal-thickness (t_m) and resist-thickness (t_r) should be at least 7:1 in order to attain successful lift-off.

The desired metal-thickness for the nanowire contacts has been set to \sim 50nm as most of the nanowires grown at the given parameters (2nm Au-film; 1000mTorr SiH₄ and 500°) have a

diameter < 50nm. This implies that a guiding resist-thickness of ~350nm is needed in order to attain successful lift-off.

Exposure:

Exposure was in this case done in a Hitachi 4300 SEM with a Raith 150 E-Beam Lithography System (EBL). As the PMMA family is a series of positive resists, the area which gets exposed by the electron beam will become soluble and removable by a fitting developer (Ch. 2.6). A detailed description of the optimized EBL-procedure employed in this experiment is described in detail in App. A.

Development:

PMMA resists was developed in an M/I 1:3 developer from MicroChem. The time which the sample should be soaked into this developer had to be investigated in order to prevent under/overdevelopment. After the development the sample was soaked in DI water and dried by a N_2 -gun.

Metallization:

The desired metal deposit was deposited onto the sample after development. The ratio between the resist thickness and metal thickness is still very important and had to be investigated. The sample was inserted into a Pfeiffer Classic 500 E-Beam Evaporator which was programmed with the correct parameters. The main deposit was aluminium (Al) but samples was also tested with a combination of titanium (Ti) and gold (Au).

Lift-Off:

Lift-off was performed by soaking the sample in acetone until the metal-layer lifted off.

Samples for initial lift-off testing:

The following samples where set for mainly determining the best resist and metal thicknesses needed for successful lift-off. PMMA A2 was set as the starting point for this investigation, but it was quickly expanded to cover PMMA A4 and PMMA A7.

Although the PMMA A2 resist do not satisfy the guiding $t_r: t_m$ ratio of 7:1 (Figure 4.24 (a)) because of its limited spin-thickness (App. B) some initial testing was performed nevertheless; as it is preferred because of its high resolution.

It is important to notice that the investigation was not performed in the sequence given in Table 3.16 which is only a summary and a more detailed description of the investigation is given in Ch. 4.3.2.

Resist	Samp	Spin	Resulting	Development	Metal
	le	speed ⁽⁷⁴⁾	thickness ⁽⁷⁴⁾	time ⁽⁷⁴⁾	
PMMA A2	A201	1000 RPM	~170nm	30 sec	-
	A202	1200 RPM	~150nm	30 sec	-
	A203	1500 RPM	~110nm	30 sec	Al (50nm)
	A204	1500 RPM	~110nm	30 sec	Ti + Au
					(10 + 40 nm)
	A205	1500 RPM	~110nm	30 sec	Al (50nm)
	A206	1500 RPM	~110nm	30 sec	Al (30nm)
PMMA A4	A401	2000 RPM	~300nm	30 sec	Al (50nm)
	A402	2000 RPM	~300nm	20 sec	Al (50nm)
	A403	2000 RPM	~300nm	20 sec	Al (50nm)
	A404	1500 RPM	~370nm	20 sec	Al (50nm)
	A405	1750 RPM	~340nm	20 sec	Al (50nm)
PMMA A7	A701	2000 RPM	~600nm	30 sec	Al (50nm)

Table 3.16: Initial samples for investigation of optimal parameters for PMMA A2, A4 and A7 resists.

The main patterns used in this part of the investigation are given in Figure 3.9 ((a) and (b)) and was designed in order to simultaneously get an indication on the smallest width of printed features and the smallest distance possible between printed features.

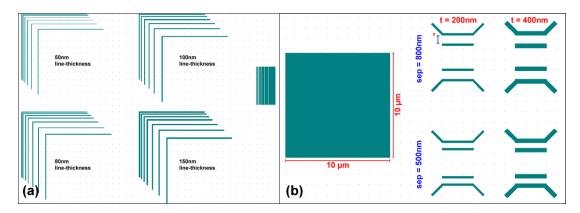


Figure 3.9: The two patterns used in the initial stages of the lithographic investigations. The first pattern (*a*) consists of lines of different thicknesses separated by different distances. The second pattern (*b*) also consists of lines of different thicknesses and separation but also a $10 \times 10 \mu m$ rectangle.

The investigation was mainly done in light-microscopy as it is a quick and reliable method for gaining an overview, but further fine-tuning had to be performed by Scanning Electron Microscopy.

In order to get a simultaneous overview on necessary exposure dose each pattern was written in a matrix on the sample (3×3) and each matrix-element was written at a given exposuredose. The matrix employed in this part of the investigation consisted of the exposure-doses given in Table 3.17.

Matrix	1	2	3
1	$800 \ \mu C/cm^2$	$1200 \ \mu C/cm^2$	$1800 \ \mu C/cm^2$
2	$400 \ \mu C/cm^2$	$600 \ \mu C/cm^2$	$900 \mu\text{C/cm}^2$
3	$200 \ \mu C/cm^2$	$300 \ \mu C/cm^2$	$450 \ \mu C/cm^2$

 Table 3.17: Initial exposure-dose matrix for PMMA A4 samples.

Samples for development time testing:

Further investigations were performed on finding the correct development time for the chosen PMMA A4 resist (Table 3.18). The chosen film thickness is based on the results attained in previous lift-off investigation (Ch. 4.3.2).

Table 3.18: Samples used to determine the optimal development time for the PMMA A4 res

Sample	Spin speed	Development time	Exposure dose interval
A406	1750 RPM	15 sec	$200 - 1800 \ \mu C/cm^2$
A407	1750 RPM	5 sec	$200 - 1800 \ \mu C/cm^2$
A408	1750 RPM	3 sec	$200 - 1800 \ \mu C/cm^2$

These samples employed the same patterns as previously used for lift-off testing (Figure 3.9).

Samples for exposure dose and minimum feature size testing (PMMA A4):

After determining the correct development time further investigations had to be done in order to find the correct exposure dose for the chosen PMMA A4 resist (Table 3.19). After finding the correct exposure dose a more detailed investigation could be performed on the minimum feature size as development and exposure now had been optimized. These samples used a new pattern designed as a four.-point contacting structure especially for a $\sim 2\mu m$ nanowire (Figure 3.10).

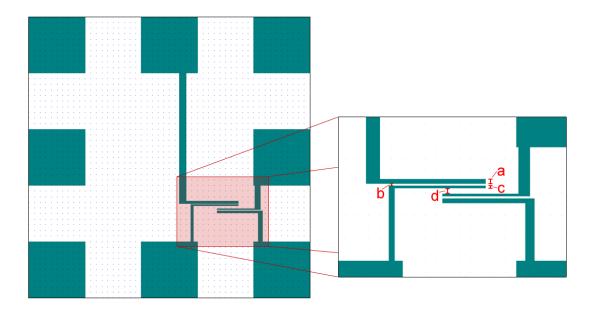


Figure 3.10: A final pattern used for the PMMA A4 and C4 resists. This will resemble a four-point contacting structure to a $\sim 2\mu m$ long nanowire.

Table 3.1	9: Samples set for dete	ermining the optimal exposure-	dose for the PMMA A4 resist.
Sample	Spin speed ⁽⁷⁴⁾	Development time ⁽⁷⁴⁾	Exposure dose interval
a = 400n	m, b = 200nm, c	= 200nm, d = 400nm (R)	Figure 3.10)
A409	1750 RPM	3 sec	$50 - 198 \ \mu C/cm^2$
A410	1750 RPM	3 sec	$50 - 198 \ \mu C/cm^2$
A411	1750 RPM	3 sec	$50 \mu\text{C/cm}^2$
A412	1750 RPM	3 sec	$10 - 50 \ \mu C/cm^2$
A413	1750 RPM	3 sec	$10 - 50 \ \mu C/cm^2$
A414	1750 RPM	3 sec	$15 - 23 \ \mu C/cm^2$

The samples were prepared based on earlier results for spin-speeds and development times.

Initial testing for the PMMA C4 resists:

Because of the problems attained with PMMA A4, some new samples were set with PMMA C4 instead (Table 3.20). C4 is approximately the same resist as A4 but with a different solvent.

Sample	Spin-speed	Resulting	Development	Exposure dose
		thickness	time	
C401	3000 RPM	~500nm	20 sec	$20 - 360 \mu C/cm^2$
C402	3000 RPM	~500nm	20 sec	$20 - 360 \mu C/cm^2$
C403	3000 RPM	~500nm	20 sec	$20 - 360 \mu C/cm^2$
C404	3000 RPM	~500nm	20 sec	$100 - 150 \mu C/cm^2$
C405	3000 RPM	~500nm	20 sec	$100 - 150 \mu C/cm^2$
C406	3000 RPM	~500nm	20 sec	$100 - 150 \mu C/cm^2$
C407	3000 RPM	~500nm	20 sec	100μ C/cm ²

Table 3.20: Samples set in order to determine the best parameters for the PMMA C4 resist.

3.3.7 Outer Contact Pads

The same photolithographic procedure used for the inner contact pads (Ch. 3.3.4) was also applicable to the outer contact pads, and the same parameters attained from lithographic investigation for the inner contacts was therefore used in this case.

3.4 Characterization Methods

3.4.1 Scanning Electron Microscopy

This project used two different Scanning Electron Microscopes (SEMs); one for observing nanowires (Zeiss Ultra, 55 Limited Edition FE-SEM) and one for observing the lithographic patterns (Hitachi 4300 SEM). The Hitachi SEM was used because of simplicity and higher availability, but since sample-tilting is not possible in this SEM silicon nanowire had to be observed in the Zeiss Ultra instead.

Zeiss Ultra, 55 Limited	Edition FE-SEM	Hitachi 4300 SEM		
Acceleration Voltage:	2 - 5 kV	Acceleration Voltage:	10 - 20 kV	
Aperture Size:	30 µm	Condenser Lens:	10 - 13	
Working Distance:	2 - 5 mm.	Working Distance:	7 mm.	
Tilt Angle:	0 - 90°	Tilt Angle:	0 °	

Table 3.21: Parameters used for observing samples in the different SEMs.

3.4.2 Transmission Electron Microscopy

Inspection by Transmission Electron Microscopy (TEM) was performed by Per Erik Vullum (SINTEF) on a selection of doped nanowires in order to further examine the crystallinity and structure. Nanowires were scraped off the sample-substrate with a scalpel onto a copper-grid covered in a lacey carbon-film and investigated in a JEOL JEM 2010F (FEG-TEM) with a resolution up to ~2Å at a voltage of 200kV.

Several techniques were employed:

- *i. Normal bright field imaging.* Gives Z-contrast which may be used to separate heavier elements from lighter elements.
- *Low-Angle Annular Dark Field Scanning Tunnelling Electron Microscopy (LAADF STEM) imaging.* Also gives Z-contrast but heavier elements lighten up while lighter elements remain dark.
- *Energy Dispersive X-ray Spectroscopy.* Was employed in order to determine chemical composition of selected nanowires but this was unsuccessful because of a build-up of carbon contaminations on the surface due to surface-hydrocarbons.

4 Results and Discussion

The project was divided into three parts:

- *Growth of aluminium catalysed silicon nanowires.* The first part of the project consisted of investigating aluminium as a possible alternative to gold as catalytic material for growth of silicon nanowires. Different growth conditions were applied in order to determine the best parameters.
- Doping of the nanowires by employing B_2H_6 and PH_3 as dopant gases. The nanowires attained in the first part were supposed to be further investigated by the addition of p-type and n-type dopants from gaseous precursors (B_2H_6 and PH_3 respectively), but because of major growth problems by using aluminium as catalyst this part was performed by employing gold as catalytic material instead.
- *Developing a lithographic method for making contacts to a single nanowire.* A preliminary lithographic method for four-point contacting of single nanowires has been investigated and proposed. These contacts may ultimately be used for back-gated 4-point electrical measurements in order to determine the effects from adding dopants to the nanowire structure.

4.1 Aluminium Catalysed Growth of Silicon Nanowires

Aluminium catalysed growth have proven to be difficult with major differences in the attained results. A summary of the results is shown in Table 4.1 in order to give an overview over the varying results attained over several different parameter changes. The results will be discussed in comparison with earlier attained results for gold catalysed growth⁽²⁾.

Table 4.1: Samples set for the investigation of aluminium catalysed nanowire growth.								
Series	Τ/	Recipe	Catalytic	0	100	500	1000	1500
	р _{SiH4}	(Table	material	mTorr	mTorr	mTorr	mTorr	mTorr
		3.4)						
1	580°C	No Clean	15nm Al	-	-	-	011 /	-
		(Recipe 1)					012	
G	rowth of n	anowires was	attained for p	$p_{SiH4} = 10$	000 mT o	rr. Large	empty ar	eas
				inate.				
2	580°C	NH ₃ Clean	15nm Al	-	021	022	023	024
		(Recipe 2)						
All sa	mples con	ntained nanow	vires, but no d	ifference l	between ti	hem was f	^c ound. It s	eemed
t	hat the sa	mples had a h	nigher amount	of empty	areas con	npared to	Parallel	1.
3	580°C	Plasma	15nm Al	031	-	-	032 /	-
		Clean					033	
		(Recipe 3)						
Al-drop	Al-droplets could not be found in sample 031, neither any nanowire growth in sample 032.							
It was also found that plasma would not activate at a NH_3 partial pressure of 200mTorr								
and was increased to 1000mTorr for sample 033.								
4	580°C	No Clean	15nm Al +	-	-	041	042	-
		(Recipe 1)	5nm Sn					

able 4.1: Samples set for the investigation of aluminium catalysed nanowire growth.

The	The surface is covered in large bright particles which are assumed to be Sn-particles.							
	Very little nanowire growth is observed.							
5	580°C	580° C NH ₃ Clean 15nm Al + 051 -						
		(Recipe 2)	5nm Sn					
Lar	Large bright particles were found on the surface but no nanowire growth. It may be							
	assumed that the bright particles are Sn-particles.							

The starting point for this investigation was a plain growth method without any extra cleaning steps added. The recipe was the exact same recipe

(Recipe 1; Table 3.4) as used for Au-catalysed growth in earlier experiments by the author⁽²⁾. A comparison of Al-catalysed (580°C) growth and Au-catalysed ⁽²⁾(400°C) growth performed right above the respective eutectic temperatures at 1000 mTorr SiH₄ partial pressure is shown in Figure 4.1 (*a*) and (*b*) respectively. Several differences may be observed from this figure.

- The nanowires appear to be thicker on the Al catalysed samples.
- The density of nanowires is drastically reduced.
- A more pronounced tapering effect is represented on the Al catalysed sample.
- A higher degree of instability results in wormy structures for Al-catalysed growth.

The crystallinity has yet to be confirmed.

4.1.1 Nanowire Diameter

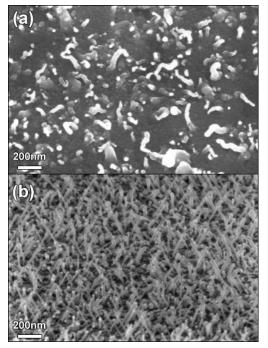


Figure 4.1: Comparison of Al-catalysed growth at 580°C (*a*) and Au-catalysed growth (*b*) at 400°C, both at $p_{SiH4} = 1000$ mTorr.

As presented in the theory (Ch. 2.2.5) both the average nanowire diameter and sizedistribution has been shown to mainly depend on the thickness of the deposited catalytic film, with a thicker film leading to an increase in both due to Ostwald ripening. The current experiment employed a 15nm thick Al-film and resulted in an average diameter of ~40nm +/-12nm. The average diameter for the previously grown Au-catalysed nanowires⁽²⁾ (Figure 4.1 *(bottom)*) was measured to ~19nm +/- 5nm for a 2nm thick Au-film. Because of the prominent tapering of Al-catalysed nanowires the measurements were performed on the bottom part of the nanowires, close to the foot. By comparing two different materials (Au and Al) one could assume that different material properties may affect the Ostwald ripening effect in different ways but is assumed to be small.

Tapering:

As presented, a prominent tapering effect is observed with a smaller nanowire-diameter on the top of the nanowire compare to at the foot of the nanowire. This is an effect which has not been observed for Au-catalysed nanowires in earlier experiments performed by the author⁽²⁾.

The measured tapering-ratio is measured as $r_{tapering} = d_{bottom} - d_{top}/L_{nw}$ where d_{bottom} is the diameter at the foot of the nanowire, d_{top} is the diameter at the top of the nanowire and L_{nw} is the length of the nanowire. The average tapering-ratio was found to $r_{tapering} \approx 0.05 + 0.02$.

There are mainly two reported reasons for nanowire tapering:

- Reduction in catalyst droplet diameter during growth⁽⁷⁵⁾.
- Radial growth of amorphous silicon⁽⁷⁶⁾.

In order to confirm the presence of one or both of these effects the samples should be investigated by high-resolution transmission electron microscopy (TEM). This has not been performed and no further confirmation can therefore be done but assumptions can be made.

Reduction in the catalyst droplet has mainly been reported to be a result of either loss of catalytic material on the nanowire walls or evaporation of the catalytic droplet. The reduced droplet stability may imply a loss of catalytic material on the nanowire walls during growth as observed for Au (Ch. 2.2.6), but there have currently not been any reports on Al-particles on the nanowire surface.

Evaporation of catalytic material may be estimated from the vapour pressure of the respective material. The vapour pressure of Al is reported to an interval of $3.06 \times 10^{-10} - 5.08 \times 10^{-6} Pa^{(77)}$ for a temperature-interval of 520 - 720°C. This is a very low vapour pressure and evaporation of Al is assumed to be negligible. In comparison, Au has a vapour pressure of $\sim 3.72 \times 10^{-8} Pad^{(77)}$ at 1000K.

Another possibility is radial growth of amorphous silicon on the nanowire walls as presented for Au in Ch. 2.2.4. The radial growth rate of nanowires is normally magnitudes lower than the axial growth rate and is under normal conditions (< ~700°C without any additional dopant gases) assumed to be small. Compared to earlier growth of Au-catalysed nanowires⁽²⁾ (400 – 500°C) Al-catalysed growth require much higher growth temperatures (\geq 580°C) and an increased radial growth is therefore possible, resulting in the observed tapering-effect. Earlier investigations by Wang et al⁽⁴⁹⁾ found a clear dependency on growth temperature at even lower temperatures (<500°C) and attributed this to an increase in radial growth rate. However, note that these experiments were performed beneath the eutectic temperature of Al-Si and the growth therefore proceeded via a solid Al-particle (VSS growth) instead of a liquid Al-Si droplet (VLS).

It is however in this case assumed that the tapering effect is a result of radial growth of amorphous silicon because of an increased temperature, but this should be complemented with high-resolution TEM images. The addition of H_2 to the gas-flow during growth has earlier been shown as a possible solution to reduce the amount of tapering of nanowires⁽⁴⁷⁾ and should be investigated.

4.1.2 Density of Nanowires and Oxidation Problems

There may be several reasons why the density of nanowires is reduced compared to Aucatalysed nanowires.

- Ripening effects.
- Oxidation of aluminium.
- Oxidation of silicon substrate.

Ripening effects:

As presented in Ch. 2.2.2, a melted catalytic film agglomerates into droplets which are exposed to ripening effects. Longer annealing times may result in the large droplets collecting a larger amount of smaller droplets which again results in the large droplets getting respectively larger and the density respectively smaller.

Two samples were grown, one without any extra annealing steps added between catalyst deposition and growth (011) and one with a one hour annealing step in-between (012). No clear evidence could be found for increased ripening effect for AL004 as no clear difference in density was found and ripening is therefore assumed to be a minor/negligible effect.

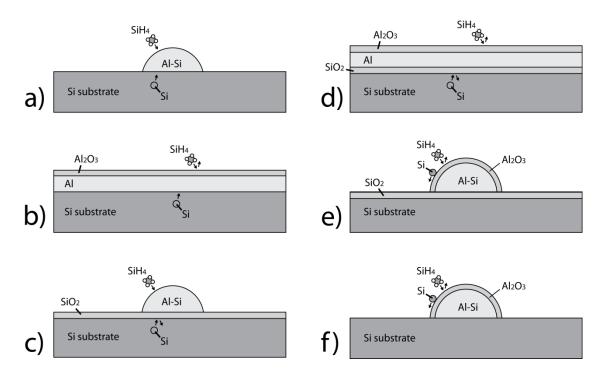


Figure 4.2: The oxidation possibilities during aluminium catalysed growth are many. The desired result is shown for comparison in (*a*). Both the Al-film (*b*) and Si-surface (*c*) are exposed to oxidation but both of them still allows Si-saturation of the Al-film thorugh one of the two interfaces (from the Si-substrate and SiH₄-feed respectively); and formation of the required Al-Si catalytic liquid may still be possible. However, if both of the interfaces are closed of by oxides (*d*) the Al-film cannot be saturated with silicon and the formation of Al-Si droplets become difficult. By assuming succesful droplet-formation the interfaces may still oxidize (*e*) and (*f*) and growth is inhbited by the Al₂O₃ layer preveting SiH₄-feed.

Oxidation of aluminium and silicon:

Both silicon and aluminium is exposed to oxidation in air or other oxygen-containing atmospheres, either partially or fully.

- Aluminium oxidises rapidly and a 3-5nm thick layer of Al₂O₃ is almost instantaneously formed and has been reported as a major problem in nanowire growth⁽³⁾.
- By etching silicon with hydrofluoric acid (HF) the substrate-surface becomes active and susceptible for oxygen and oxidation.

Earlier experiments⁽²⁾ performed with gold as catalytic material employed a 15 min time-limit on the time used from the final HF-etch to the sample had to be in a evacuated PECVD chamber, which was done in order to minimise oxidation of the silicon substrate surface. These experiments employed a sputter-coater to deposit 2nm of Au-film and used only 2 minutes to do so. In the current experiment Al had to be deposited by an E-Beam evaporator which results in a drastically increase in processing time. The processing sequence is summarised as following (Table 3.7; Steps 6 - 12):

- i. Si-sample is etched in 5% HF (Start).
- ii. Transport of Si-sample into E-Beam Evaporator (~1min).
- iii. E-Beam procedure (25-30min).
 - a. E-Beam preparations (Pump-down and Target heating) (10-15min).
 - b. Aluminium deposition (~5min).
 - c. E-Beam cool-down, pump-down and removal (~5 min).
- iv. Transport of sample from the E-Beam to the PECVD chamber ($\sim 1 \text{ min}$).
- v. Evacuation of the CVD chamber (*End*).

A total Al-deposition time of ~30min must be expected when depositing Al and oxidation problems are therefore a large concern. Oxidation of the Si-surface is assumed to mainly be a possible problem when directly in contact with air i.e. before deposition of the Al-film.

All of the steps mentioned above are possible surrounding for oxidation, even when placed in a vacuum the sample may be exposed to some oxygen (E-Beam and CVD chamber). Previous experiments⁽³⁾ have shown that vacuum chambers should hold a maximum base-pressure of $\sim 10^{-9}$ in order to get good results with Al as catalytic material, but one still faces the problems with the transport of the samples in air, ex. between the E-Beam and CVD chamber. Some of the oxidation possibilities during growth are presented in Figure 4.2 (a) – (f).

Several methods were explored in order to possibly minimise the amount of surface oxidation problems, mainly by adding cleaning steps to the CVD-procedure. Note that the pump and purge steps added between the cleaning steps and the silicon deposition steps may affect the process in the different direction towards an increase in oxidation because of a longer annealing time before introduction of precursor gas.

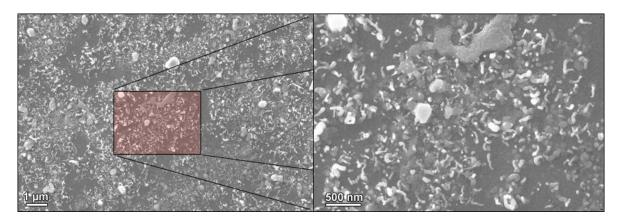


Figure 4.3: Initial aluminium catalysed growth without any added cleaning steps resulted in a low density of highly unstable nanowires (Sample 011).

Oxidation prevention:

As an attempt to limit/minimize probable oxidation problems (Figure 4.3), some additional cleaning steps were added to the standard recipe (Table 3.4).

 NH_3 Cleaning: Series 2 was grown with an added a NH₃ cleaning step to the recipe (Recipe 2) as a try to etch some of the assumed oxide on the sample. A general result observed from the introduction of NH₃ is large dark areas (Figure 4.4 (*a*) and (*b*)) lacking both catalytic particles and nanowires. This may imply either that the catalytic particles have been fully etched by the NH₃ or a complete coverage in either Al₂O₃ or SiO₂.

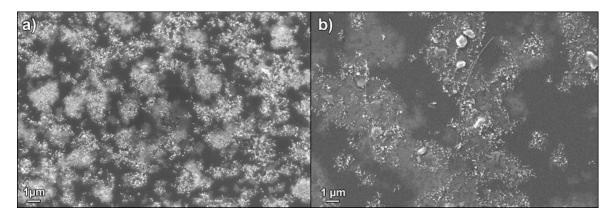


Figure 4.4: Adding a NH3 cleaning-step to the process seemed to reduce the nanowire density even further, here shown for sample 023 (*a*) and 024 (*b*).

 NH_3 -plasma Cleaning: The next series (Series 3) was pre-cleaned by using a 20W NH₃plasma (Recipe 3). As observed from the SEM images in Figure 4.5 most of the surface seems to be completely clean of both nanowires and catalytic particles (a), some small areas however seem to contain catalytic particles but with minimal growth of nanowires (b). Note that independent investigations performed by the supervisor showed that plasma would not activate before a $p_{NH3} = 1000$ mTorr but because of the drastically changes observed it was assumed that plasma was activated in this case. In this case one may also assume either a complete cleaning of the surface or the growth of an oxide-film covering the catalytic droplets. Because of the pores observed in Figure 4.5 (a) one may assume a fully covering oxide.

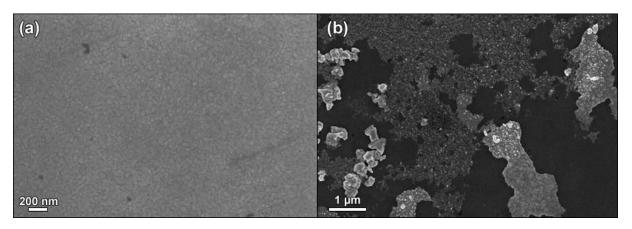


Figure 4.5: By enabling plasma at 20W (sample 032 most of the surface seemed to be clean of catalytic particles and nanowires (*a*), however, some areas was found to contain catalytic particles but with very low amount of nanowires (*b*).

The increased oxidation observed in the previous two cases may also be due to the added pumping and purging steps between the NH_3 Cleaning step and Si-deposition step (Table 3.4; recipe 2 and 3). These steps were added in order to clean the chamber for NH_3 residues before Si-deposition, but may lead to further oxidation of the sample because of the increased time spent in the chamber and the necessity of these steps may be questioned.

Protective Sn-coating: Sn was explored as a protective coating for aluminium (Figure 4.6) as

it more resistant towards oxidation compared to Al (Ch. 2.3.3). It also has a low melting point and is therefore assumed not to block access for SiH_4 to the Al-Si liquid.

The solid solubility of Sn in Al is negligible at room temperature and in combination with



Figure 4.6: An illustration of the proposed protective Sn-coating for the Al-film.

the low time exposed to air it is assumed that no alloying of Al with Sn will happen during transfer to the CVD chamber.

After heating in the CVD chamber Sn will probably start to interact with the other materials in the system (Al and Si), and instead of having an Al-Si liquid one will probably have an Al-Si-Sn liquid which is assumed to alter the growth conditions. From the ternary phase diagram the following equilibrium composition is found for the liquid at $580^{\circ}C^{(78)}$:

- 6 at% Si.
- 38 at% Sn.
- 56 at% Al.

The Si-solubility is reduced compared to an Al-Si liquid but increased compared to a Si-Sn liquid which also have been shown to catalyse growth of nanowires (Ch. 2.3.3).

As seen from Figure 4.7 no nanowire growth was observed for this system. Both samples shown in this figure (Sample 042 (a) and 051 (b)) seem to have a rough surface with bright particles dispersed all over the surface with minimal nanowire growth.

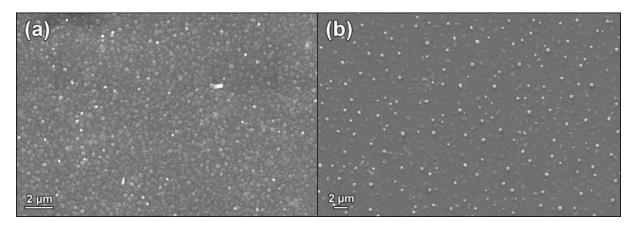


Figure 4.7: The addition of a Sn-layer covering the Al-film resulted in dispersed particles all over the surface. If these particles are pure Sn or is alloyed with Si and/or Al is unknown. Sample 042 is given in (*a*) 051 in (*b*).

Reasons for the lacking nanowire growth may be many, but because of the relatively high solubility of Sn in the Al-Si catalytic droplet one may expect the growth-rate reduces (Ch. 2.3.3) and a possible solution may therefore simply be to increase the growth time.

The prevention of oxidation and improvement of the growth conditions have all in all been unsuccessful with all of the added cleaning procedures resulting in reduced density of nanowires and other procedures may be more suitable for this goal. A possibly better alternative was proposed by J. M. Redwing⁽⁴⁷⁾ et al which found that high SiH₄ and H₂ partial pressures effectively reduced oxidation problems, and was attributed to the H₂-gas passivating the substrate- and nanowire-surface (a surface covered in hydrogen is not available to oxidation; Figure 2.10).

4.1.3 Nanowire Length

By comparing the lengths for Al-catalysed nanowires attained in this experiment with lengths attained for gold catalysed nanowires in earlier experiments performed by the author⁽²⁾, a drastic reduction in the average length is observed at approximately constant growth temperature.

Sample 011 ($p_{SiH4} = 1000$ mTorr for 45 min) was grown right above the eutectic point for the Al-Si alloy (580°C) and is compared with two Au-catalysed samples grown in earlier experiments by the author⁽²⁾ (Table 4.2):

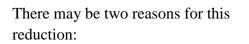
- $p_{SiH4} = 1000mTorr$ for 15 min directly above the eutectic point for the Au-Si alloy (400°C).
- $p_{SiH4} = 1000$ mTorr for 15 min at 500°C.

 Table 4.2: Previously attained Au-catalysed nanowire lengths compared to currently attained

 Al-catalysed nanowire lengths.

	Au (400°C)	Au (500°C)	Al (580°C)	
1000 mTorr	175 +/- 62nm	3900 +/- 450 nm	300 +/- 103nm	

Compared to the Au-Si sample grown at approximately the same temperature $(500^{\circ}C)$ as the Al-Si sample $(580^{\circ}C)$, a reduction in nanowire length is observed. In addition, what is assumed to be Aucontaminations on the Al-sample (Figure 4.8) resulting from contaminations in the E-Beam chamber shows a nanowire length of ~15µm.



- Increased eutectic temperature.
- Oxidation of catalytic droplet.

Increased eutectic temperature:

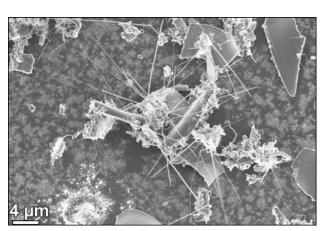


Figure 4.8: Au-contaminations on an ordinary Al-catalysed sample (Sample 011).

As the eutectic temperature for the Al-Si (~580°C) system is higher than for the Au-Si (~360°C) system, a higher growth temperature is needed to completely melt the alloy. It may therefore be more correct to compare the Al-catalysed sample with the corresponding Au-catalysed sample grown (400°C) close to its respective eutectic temperature. The lengths are then comparable between the two systems. Note that it is more difficult to correctly measure the Al-catalysed nanowires because of the large degree of bending of the nanowires.

Another possibility for the difference in growth rate is the difference in activation energy between the Au-Si and Al-Si catalytic materials. As described in Ch. 2.2.4 nanowire growth is assumed to be a thermal activated process with a given activation energy. The possible rate-limiting steps for the growth-rate have in this case been assumed to be one of the following:

- i. Decomposition of SiH₄ on the catalytic droplet.
- ii. Diffusion of Si in the catalytic droplet.
- iii. Crystallisation of solid Si at the liquid-solid interface.

Each step may vary depending on the composition and material-content of the droplet. Diffusion may still be assumed to be negligible and not rate-limiting but both the decomposition of SiH₄ and crystallisation may depend strongly on the catalytic material.

Step (iii): Step (iii) has previously been found to depend on the supersaturation of the droplet (3, 26).

By comparing the lengths of the nanowires grown at approximately constant temperature (Au at 500°C and Al at 580°C) the Au-catalysed nanowires are much longer. This may be a result of the higher solubility of silicon in the Au-droplet compared to the Al-droplet at this temperature and it is normally assumed⁽³⁾ that catalytic materials with higher solubility of silicon result in higher growth rates.

However, by comparing the lengths of the nanowires grown at approximately respective eutectic temperatures (Au at 400°C and Al at 580°C) instead the average nanowire length is larger for Al than for Au. This may imply that since the Si-solubility is smaller in the Al-droplet than in the Au-droplet a smaller amount of silicon is needed to supersaturate the Al-droplet to the same amount of supersaturation as for the Au-droplet which may lead to a higher growth-velocity for Al-catalysed nanowires.

Step (i): The activation energy for step (i) has earlier been described for an Au-Si droplet but has not been found for an Al-Si droplet, but a possible increase in activation energy may reduce the growth-rate at constant temperature if the step is limiting.

As noted before this is a very complex system and a more detailed investigation of the three possible rate-limiting steps mentioned above is needed.

Oxidation of catalytic droplet:

Because of the previously described oxidation-problems the droplets may be covered in an Al_2O_3 layer during growth (Figure 4.2 (*f*)) which would block further feed of SiH₄ and effectively inhibit further growth. Incoming SiH₄ molecules may therefore deposit on the nanowire walls instead contributing to the radial growth rate instead.

It is in this case assumed that a combination of all these possibilities is the reason for the observed reduction in nanowire length compared to the Au-Si system (at constant temperature). In order to increase the growth-rate of Al-catalysed nanowires higher growth-temperatures are needed but because of a 600°C temperature-limit on the CVD chamber employed this must be investigated in an alternative chamber.

4.1.4 Bending and Instabilities of Nanowires

As seen in Figure 4.1 (top) aluminium catalysed growth is exposed to large instabilities and bending assumed to be a result of instabilities in the catalytic droplet. This is assumed to be a result of the intermediate surface-tension of the Al-Si droplet (Table 2.1).

Earlier reports have shown that a reduced growth-rate may increase the stability of the droplet as a lower growth rate results in the droplet getting more time to stabilise between each crystallised Si-atom.

In order to promote Al as an effective catalyst for nanowire growth a better control of the instabilities is needed in order to get straight nanowires, and more investigation is needed. One possible solution was a combination of high SiH₄ and H₂ partial pressure ($p_{SiH4} \sim 54$ Torr at a total chamber pressure of ~600 Torr; 10% SiH₄ in H₂) which seemed to stabilize the growth and additionally minimize the oxidation problems⁽⁴⁷⁾. However, the experiment employed nanowires with diameters in the range of 100-400nm and large droplet diameters hold a much higher stability than the smaller droplets employed in the current experiment (~40nm). The increased nanowire growth may therefore be a result of a combination of H₂-gas passivating the silicon surfaces and larger catalytic droplets.

4.2 Growth of Doped Nanowires

The next step was to introduce dopant atoms into the Al-catalysed nanowires, but because of the bad results attained for Al-catalysed growth this investigation had to be performed on Aucatalysed growth instead. Investigations were performed on the structural changes observed for different flows of dopant-gases (B_2H_6 and PH_3) and comparing them to intrinsic samples grown without dopant-gases. Note that the actual implementation of the dopant atoms into the nanowire structure has to be confirmed by electrical resistivity measurements (Ch. 2.5). Each series started and ended with an intrinsic sample in order to check for possible residues affecting growth after removal of the dopant-gases.

Previous experiments performed on intrinsic growth:

Previous experiments performed by the author⁽²⁾ found that the nanowire morphology strongly depended on the growth-temperature and SiH₄ partial pressure. A combination of high growth-temperature (500°C) and low SiH₄ partial pressure (100mTorr) seemed to result in a preference for a <111>-growth direction for nanowires grown on Si(111) substrates (Figure 4.9 (a)), and was confirmed by TEM-investigations (b). These growth-parameters were chosen to act as a basis for the dopant-investigations performed in the current experiment beause of the preference for a <111>-growth direction easily distinguishable from other possible growth directions.

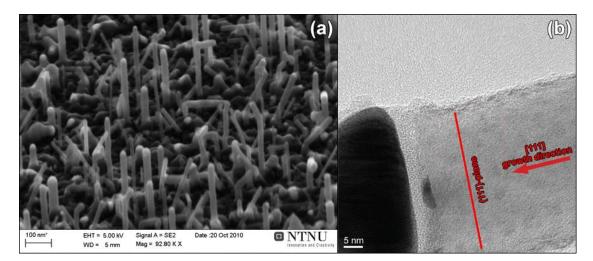


Figure 4.9: Previously grown Au-catalysed nanowires seemed to prefer a <111>-growth direction when grown at high temperatures (500°C) and low SiH₄ partial pressures (100mTorr) on Si(111) substrates (*a*). TEM-analysis confirmed the assumed <111>-direction (*b*).

An average length of 206 +/- 64nm was attained at a growth time of 15 min, resulting in a growth rate of approximately 0.23nm/s (T = 500° C, $p_{SiH4} = 100$ mTorr).

4.2.1 Intrinsic Nanowire Growth and Chamber Contamination

Each series started with intrinsic samples grown at the same growth conditions as previously described but the previously attained results and morphology⁽²⁾ proved to be difficult to replicated during the current experiments. It was assumed that the nanowires would attain the same morphology as attained in previous experiments described above, but this was not the case for any of the samples. Examples of the attained intrinsic morphology are given as sample DB12 and DP22 in Figure 4.10.

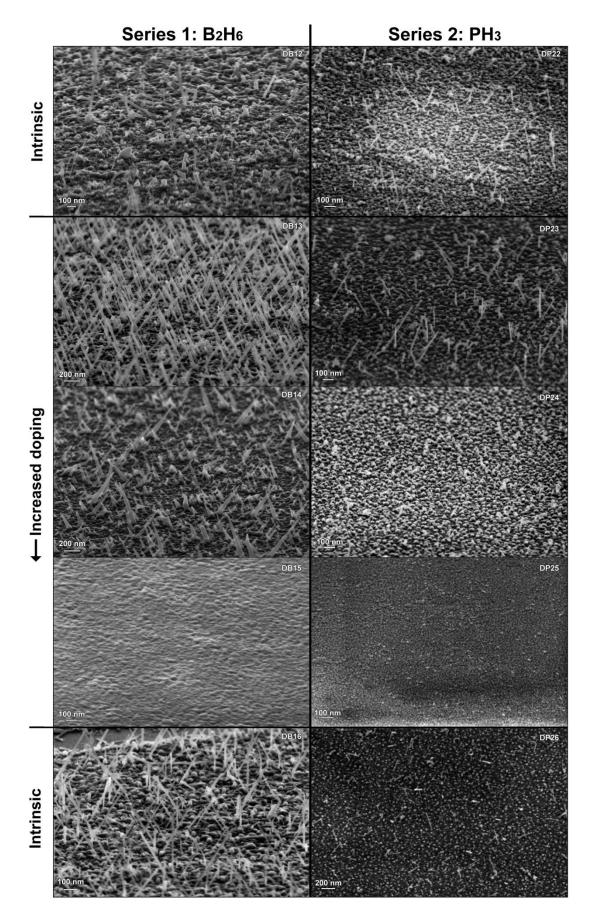


Figure 4.10: Each series started and ended with an intrinsic sample in order to check for possible residues in the chamber after each series. The samples are grown with increasing dopant-ratios downwards in the figure.

Several intrinsic samples were grown but with varying results; even cases of no growth at all were observed. In one case an average nanowire length of $\sim 1-2\mu m$ was attained but because of problems with the following doped samples this series was discontinued.

It is assumed that a combination of newly installed dopant gases and work performed by others in-between this work may inflict with the nanowire growth conditions and cause the instabilities observed for the initial intrinsic samples.

A partial solution to the attained growth instabilities was to perform a plasma-cleaning of the CVD-chamber before any nanowire growth, which indicates a possible contamination problem. There were also indications on better growth-reproducibility if the chambertemperature was increased to the desired growth temperature (500°C) a day in advance of growth in order to degas/purge any residues in the chamber. Contaminations in the chamber are therefore assumed to be the main reason for the observed growth instabilities. Growth following this preparation-procedure seemed to have an approximately stabilized nanowire length between the undoped samples and the average nanowire length was measured to ~244 +/- 138nm and \sim 293 +/- 113nm for sample DB12 and DP22 for a growth time of 60 min. Compared to the nanowires attained at earlier experiments $(\sim 206 + /- 64 \text{nm for } 15 \text{ min})^{(2)}$ the current samples still show a major reduction in nanowire growth rate. J. Kikkawa et al reported on what seemed to be a reduction in the growth velocity during growth, and was assumed to be a result of the increasing distance between the substrate and the catalytic Au-Si droplet possibly reducing the effective temperature felt by the droplet⁽⁷⁹⁾. This is however assumed to not be the reason for why nanowires are limited to a length of ~250-300nm in this experiment since some test-samples have successfully been grown with nanowire lengths of \sim 1µm at the same growth-parameters. It may therefore be assumed that the length-limitations observed also may be a result of a partly successful chamber clean, resulting in possible contamination-residues in the chamber (Figure 4.11) during growth.

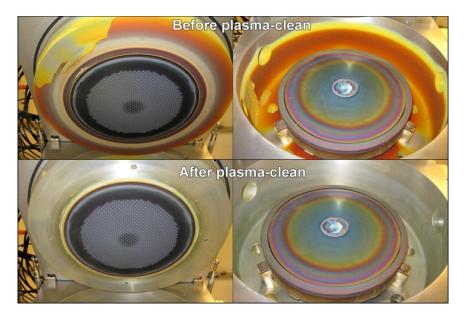


Figure 4.11: Growth problems were assumed to be related to chamber contaminations (top). After a plasma-clean of the chamber the growth conditions improved but some contaminations seemed to reside in the chamber (bottom) further resulting in possible growth problems. Note that a clean chamber is completely metallic gray,

Even if the precautions are taken and cleaning steps are added to the process there are still uncertainties related to the contamination level of the chamber. The chamber is cleaned every week with an occasional wet cleaning every month. Residues are found on regular basis, some may simply be dried off while some must be etched. Possible sources of contamination are process gases and samples introduced into the chamber and are mainly assumed to react with the sample-material in two ways:

- i. Solid material in the form of dust may deposit on and contaminate the sample-surface directly.
- ii. Solid material deposited on the chamber-wall in earlier processes may start to evaporate as a result of increased temperature. Contaminations with low vapour pressure have a higher probability of evaporation.

Both may result in material being deposited onto the catalytic droplet (Figure 4.12). If the contamination is soluble in the Au-Si liquid it may diffuse into the droplet at change the properties of the liquid and possibly changing the growth-properties of the droplet.

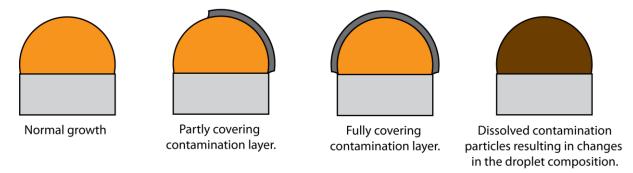


Figure 4.12: Illustrations of possible contaminations in the chamber compared to normal growth. Mainly two possibilities are shown; adsorbed material on the catalytic droplet or a changed composition of the droplet, depending on the solubility of the contamination in the catalytic liquid.

On the other hand, if the contamination is insoluble in the Au-Si liquid it may instead form a partly or fully covering contamination-layer surrounding the Au-Si droplet possibly limiting the supply of SiH₄ to the droplet. These effects may not only affect the length of the nanowires but also the density of nanowires as some of the catalytic droplets may have been affected already before the introduction of SiH₄ into the chamber.

Note that oxygen-containing residues may also release oxygen into the chamber, ultimately resulting in additional oxidation-issues.

The following differences in chamber usage have been logged since the previous experiments performed by the author⁽²⁾:

- i. Growth of carbon nanotubes.
- ii. Instalment and usage of gaseous PH_3 and B_2H_6 .
 - A research covering growth of carbon nanotubes has been started. Employing carbon-containing gases in deposition processes could leave carbon-residues in the chamber in the form of graphite or other carbon-containing species.

After the plasma-etching performed before the B_2H_6 -series one could still observe some contamination which may be related to carbon residues because of its black colour (Figure 4.11). Carbon may as earlier presented be assumed to affect the nanowire droplet in two possible ways:

- *a. Incorporation into the Au-Si droplet:* An Au-Si-C tertiary phase diagram has not been found but by assessing the respective binary diagrams for Au-C and C-Si one finds that the solubility of C is negligible in both at 500°C⁽⁴³⁾. It is therefore assumed that the solubility of C in an Au-Si liquid is negligible.
- b. Covering the catalytic droplet: There is also a possibility that graphite residues could cover the catalytic Au-Si droplets and reduce the number of possible adsorption locations. Normally it may be assumed that adsorption of SiH₄ molecules is not rate-limiting in the growth of nanowires, but if the area exposed to the SiH₄ gas becomes small enough this might change. A reduction in exposed surface-area of the droplet implies a lower area used for SiH₄- adsorption, and one may assume that a smaller amount of SiH₄ molecules are adsorbed on the surface hereby becoming the rate-limiting step. This corresponds to a reduction in the previous presented sticking probability.
- *c.* Evaporation of carbon: Another possibility is a reaction between evaporated carbon contaminants (graphite) and SiH₄ in formation of SiC but this is not assumed to happen because decomposition of graphite requires much higher temperatures than applicable to this chamber. The vapour pressure of graphite (1 Pa at 2775°C) is much lower than for gold (1 Pa at 1373°C)⁽⁸⁰⁾ and evaporation of graphite into gaseous carbon is therefore not expected.

2. The instalment and usage of dopant gases (PH_3 and B_2H_6).

Boron and phosphorus are other possible contaminants and is mainly assumed to be a result of the newly instalment and usage of PH_3 and B_2H_6 gases in the chamber. Most of the deposited material shown in Figure 4.11 is assumed to be mainly silicon-based possibly containing PH_3 - and B_2H_6 -based residues. This silicon-material is mainly assumed to be amorphous and porous because of the low temperatures usually employed in this chamber (300-500°C) and a porous material may adsorb much more gas than a non-porous material. Gaseous contaminations may then reside longer in the chamber when covered in deposited porous contaminations.

The vapour pressure of boron (1 Pa at 2075°C) is much lower than for gold⁽⁸⁰⁾ and evaporation of possible boron residues is not assumed to happen. On the other hand, the vapour pressure of phosphorus is much higher. As phosphorus may be deposited at temperatures above 250°C it may reside in the chamber as red phosphorus one of the four allotropes of phosphorus⁽⁸⁰⁾. Red phosphorus has a vapour pressure of 1Pa at 182°C but quickly increases to 100kPa at 431°C and evaporation is plausible⁽⁸⁰⁾.

Gaseous B_2H_6 and PH_3 however may possible reside in the chamber for a while after deposition even if cleaning/purging steps are added between the samples. This might possibly affect samples grown within a limited time-frame of each other. F. Jansen et $al^{(81)}$ performed experiments on dopant gas contaminations by growing Si-films with B_2H_6 and PH_3 as dopant gases in a given sequence and comparing the measured activation energies for electrical conductivity with intrinsic values. Based on the activation energies it was found that gaseous B_2H_6 could reside for several hours inside the chamber after closing the gas flow by adsorption on the chamber walls; normal intrinsic values was not achieved before the next day. By using PH_3 instead, intrinsic values were restored within one hour. Cross-contamination between samples, especially by using B_2H_6 is therefore highly likely when growing samples within a short time-frame, as in the current experiment. A solution to this may be to introduce longer purging steps or increasing the time between each sample, but may not be ideal for experiments working on a time scale comparable to a production facility.

The chamber had been free of gaseous B_2H_6 several days before growth of the first intrinsic sample (DB12) and the plasma-clean had also been performed. The temperature had also been increased to 500°C the day before to degas/purge the chamber for potential residues. Therefore one assumes that there was no B_2H_6 residing in the chamber during intrinsic growth (DB12).

Sampl	r_{dopant}	Average	Average	Average	Average			
e	r _{SiH4}	length	diameter	diameter (top)	tapering			
			(foot)		ratio			
Boron doping $(0.1\% B_2H_6 dopant gas)$:								
DB12	0	365 +/- 120nm	15 +/- 6 nm	15 +/- 6 nm	0			
DB13	5.0×10^{-5}	336 +/- 122nm	25 +/- 4 nm	15 +/- 4 nm	0.03 +/- 0.01			
DB14	5.0×10^{-4}	250 +/- 134nm	47 +/- 12 nm	13 +/- 4 nm	0.16 +/- 0.05			
DB15	5.0×10^{-3}	-	-	-	-			
DB16	0	268 +/- 102nm	12 +/- 2nm	12 +/- 2 nm	0			
Phospho	orus doping (1	0% PH3 dopant g	as):					
DP22	0	293 +/- 113nm	16 +/- 3 nm	16 +/-3 nm	0			
DP23	5.0×10^{-3}	230 +/- 101nm	13 +/- 3 nm	11 +/- 3 nm	0.006 +/-			
					0.008			
DP24	1.0×10^{-2}	72 +/- 17nm	15 +/- 3 nm	15 +/- 3 nm	0			
DP25	1.0×10^{-1}	-	-	_	-			
DP26	0	278 +/- 75nm	15 +/- 3 nm	15 +/- 3 nm	0			

Table 4.3: Resulting properties for nanowires grown at addition of dopant gases.

Table 4.3 displays the results attained for this part of the project. Note that it was not possible to reduce the dopant gas flow to below 2sccm for any of the two dopant-gases which in combination with a maximum SiH_4 flow of 50 sccm put a lower limitation on the possible

dopant versus silane ratios (r_{dopant}/r_{SiH4}) . Each series will be discussed separately but some

uncertainties should be expected when comparing results across series because of the observed variations in intrinsic results.

4.2.2 Boron Doping

From the SEM-images taken at different dopant-flows (Figure 4.10) and Table 4.3 the following properties may be observed:

- Reduction in nanowire length at increasing boron-flows.
- The increasing diameter at the foot of the nanowire and the increasing tapering ratio at increasing boron-flows.
- The reduction in nanowire density at higher dopant flows.
- The preference for tilted growth directions.

Nanowire length:

As earlier observed by L. Pan et al⁽⁷⁵⁾ and S-J Whang et al⁽⁷⁶⁾ a reduction in average nanowire lengths is observed for higher boron flows and may be assumed to be a result of adsorption of B_2H_6 on the catalytic droplets. The sticking coefficient of the Au-Si droplet earlier has been assumed to be ~1 (Ch. 2.2.4) and there is a high probability that B_2H_6 molecules may adsorb on the droplet in addition to the SiH₄ molecules. The solubility of B in the Au-Si liquid is assumed to be negligible at the given growth temperature ($500^{\circ}C$)⁽⁷⁶⁾ and the droplet may not be a very good catalyst for B_2H_6 decomposition, which may result in the B_2H_6 molecule occupying an adsorption-location (Figure 4.13) on the surface for a given time before desorbing. A continuous supply of B_2H_6 molecules on the Au-Si droplet surface, and will assumedly result in a reduced feed of Si to the droplet ultimately leading to a reduction in the axial growth-rate of the nanowire. An increased dopant-flow is assumed to result in more B_2H_6 adsorbing on the Au-Si droplet thereby blocking more adsorption-states on the droplet surface and ultimately resulting in shorter nanowires. The highest possible dopant ratios before complete inhibition were found to be ~ $10^{-4} - 10^{-3}$.

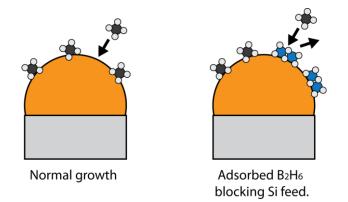


Figure 4.13: B_2H_6 adsorbed on the Au-Si droplet surface preventing full access to SiH₄ may reduce the growth rate compared to normal growth.

The final intrinsic sample has an average nanowire length comparable to the previous grown boron-doped nanowires. Earlier investigation performed Jansen et al⁽⁸¹⁾ showed that gaseous B_2H_6 could reside in the CVD-chamber up to 24 hours after use by adsorbing on the chamber-wall. A continuous desorption of B_2H_6 molecules from the chamber-wall would therefore possibly affect samples processed in the chamber during this time. Since the samples in the boron-series are grown at intervals of one hour it is assumed that some B_2H_6 resides in the

chamber affecting the growth rate of the final intrinsic sample (DB16). The apparent preference for a tilted (discussed later) growth direction observed in the final intrinsic sample is also a strong indication on B_2H_6 residues in the chamber.

Nanowire diameter and tapering effect: As observed from the attained results (Table 4.3) a tapering effect becomes noticeable already at low dopant flows. The tapering ratio is defined as the diameter difference between the bottom and the top of the nanowire divided by the

length of the nanowire.

Mainly two possibilities have been discussed for this diameter difference in earlier publications:

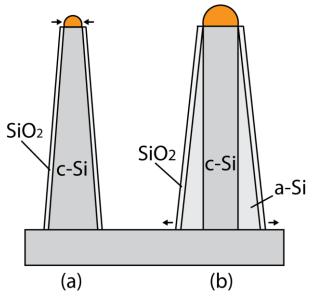


Figure 4.14: Two reported possibilities for nanowire tapering. A reduction in the catalytic droplet (a) or radial growth of silicon on the nanowire walls (b).

- 1. Continuous loss of Au from the Au-Si droplet ⁽⁷⁵⁾ (Figure 4.14 (a)).
- 2. Increased radial deposition of Si on the nanowire wall^(76, 82) (Figure 4.14 (b)).

L. Pan et al⁽⁷⁵⁾ observed that nanowires grown at increased B_2H_6 partial pressures suffered from a loss of Au from the Au-Si droplets because of an assumed instability at the liquid-solid interface, ultimately consuming the whole droplet and preventing further axial growth. Since the nanowire diameter has been found to mainly depend on the diameter⁽²⁾ of the Au-Si catalytic droplet a continuous reduction in Au-Si volume would imply a reduction in the nanowire diameter resulting in the observed tapering effect (Figure 4.14 (a)).

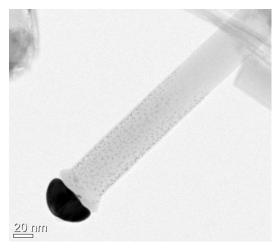


Figure 4.15: Earlier TEM-analysis⁽²⁾ revealed Auparticles diffusing from the main Au-Si droplet on top of intrinsic nanowires down the walls of the nanowire.

In the current experiment most of the nanowires observed seem to still have the catalytic droplet intact, either implying growth termination before fully consumption of droplet or growth without any major loss of catalytic material. Earlier investigations performed by the author⁽²⁾ have found that the loss of Au from the catalytic Au-Si droplets is a prominent effect also observed for undoped nanowires (Figure 4.15) and therefore is not a unique feature only found for boron-doped nanowires as implied by L. Pan et al^(38, 75).

Measurements performed on the top part of the nanowires (Table 4.3) show that the average top diameter for every sample corresponds approximately to the constant diameter measured for intrinsic nanowires in sample DB12 and is a strong indication of radial deposition instead of Au-loss. TEM analysis was performed on tapered nanowires grown on sample DB14 (Figure 4.16 (a)) which confirmed this assumption; all the observed tapered nanowires consisted of an approximately crystalline core with constant diameter covered in a tapered amorphous Si-layer (b).

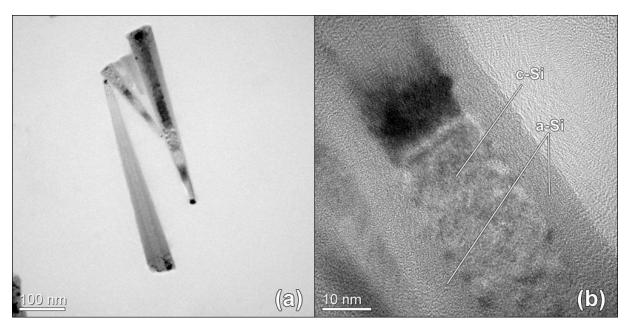


Figure 4.16: TEM-analysis performed on nanowires grown DB14 confirmed the tapering effect (*a*) and indicated a crystalline core of constant diameter covered in a linearly increasing a-Si layer (downwards; (*b*))

The tapered amorphous layer has earlier been reported to be a result of increased deposition of non-catalysed Si on the nanowire wall⁽⁷⁶⁾ when adding B₂H₆ to the gas-flow. F. C. Eversteyn and B. H. Put⁽²⁸⁾ found that the growth-rate of uncatalyzed deposition of polysilicon thin-films from SiH₄ increased with a factor of 2 by adding B₂H₆ to the gas-flow (~680°C), and related it to a reduction in the activation energy for heterogeneous SiH₄ decomposition from ~154kJ/mol to ~29kJ/mol (T < 620°C). C-Y Meng et al⁽⁸²⁾ proposed that a gaseous reaction between SiH₄ and B₂H₆ was the reason for the increased radial deposition rate, forming a SiH₄-BH₃ complex which easily decompose into SiH₃ and BH₃ radicals, and may be the reason for the reduction in activation energy observed by Eversteyn and Put.

The increasing tapering ratio observed for increasing boron-flows is assumed to be a result of more B_2H_6 reacting with SiH₄ assumedly increasing the radial deposition rate. An apparent saturation in the tapering ratio is also observable from Table 4.3 which may be a result of a

limited reaction-rate between SiH_4 and B_2H_6 or a limited deposition/adsorption rate onto solid-silicon at the given temperature.

Reduction in nanowire density:

When the gas ratio reaches a value $\sim 5.0 \times 10^{-3}$ the observed nanowire density is drastically reduced. Apparently most of the catalytic droplets also seem to have vanished from the sample-surface. With basis in the previously mentioned it is assumed that the uncatalyzed deposition rate has exceeded the catalysed nanowire growth rate for most of the nanowires, resulting in film-growth and ultimately covering un-incubated catalytic droplets in solid silicon and preventing growth.

Preference for a tilted growth-direction:

As previously presented, earlier experiments performed by the author showed that intrinsic nanowires grown at the same SiH₄ partial pressure and temperature as used in the current experiment (500°C, $p_{SiH4} = 1000$ mTorr), preferred a <111> growth direction perpendicular to the surface on Si(111) substrates⁽²⁾. Even if there is no clear evidence for a <111> growth direction for the undoped / intrinsic nanowires grown in the current experiment the boron-doped nanowires however, show a clear preference for a tilted <110> growth direction (Figure 4.10). This was supported by TEM-analysis performed on a selection of nanowires taken from the DB14 sample (Figure 4.17).

Schmidt et al⁽³⁵⁾ concluded wit that the growth direction is mainly determined by nanowire surface energetics which in this case consists of two contributions(Figure 2.7 (*b*)):

- 1. Surface tension on the edges of the nanowire, σ_s .
- 2. Liquid-Solid interfacial tension between the nanowire and the Au-Si droplet, σ_{ls} .

It was argued that due to different scaling of these different energetic contributions, thin nanowires (< 20nm) tend to choose a <110> growth direction which provides energetically favourable side-faces while thick nanowires (> ~40nm) tend to choose a <111> growth direction which minimizes the liquid-solid interfacial tension. A transition region was observable at a diameter-interval of 20-40nm.

The earlier grown intrinsic nanowires had

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Figure 4.17: All investigated nanowires grew in the <110>- growth direction.

an average nanowire diameter of $\sim 25 \text{nm}^{(2)}$ in the middle of the transition region, but the droplet was assumedly further stabilized because of the low growth rate further increasing the preference for a <111> growth direction. The currently grown doped nanowires however,

have an average nanowire diameter of ~15nm which is in the thin-region of the above statement and may be an explanation of the observed preference for a <110> growth direction.

Caution is generally to be taken when assessing growth of nanowires as it is a vastly complex system. Earlier reports have shown that the growth rate is assumed to have an effect on the droplet stability and may also affect the preferred growth direction for nanowires⁽⁸³⁻⁸⁵⁾. It has also been shown that contaminations such as carbon⁽⁸⁶⁾ and boron⁽⁸⁷⁾ may affect the relative free energies of the silicon surfaces and induce faceting of the nanowire walls (alternating $\{111\}$ and $\{110\}$), thus also possibly affecting the equilibrium state and growth direction.

It is clear that the chosen growth direction is a result of the system wanting to minimize the surface-energies of the nanowire surface, but because of what is assumed to be contamination problems complicates the research even further and it is hard to make definitive conclusions on this matter. Trends in growth directions for doped nanowires are still an unexplored area, and require further research first by eliminating contamination uncertainties.

Dispersion of Au-particles:

As previously described for intrinsic nanowires (Figure 4.15) dispersion of Au-particles was also found on the wall of tapered nanowires in the current experiment (Figure 4.18).

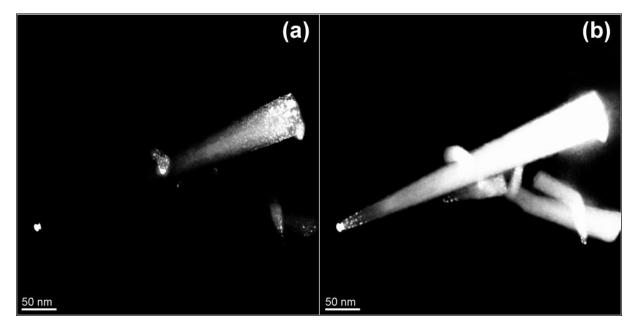


Figure 4.18: LAADF STEM imaging revealed diffuse Au-particles at both the bottom (*a*) and top (*b*) of the tapered nanowire.

The Au-particles observed on top of the top part of nanowire (Figure 4.18 (b)) are assumed to come from the diffusion of Au-particles from the catalytic droplets (Figure 4.19 (a)) onto the nanowire wall during growth ^(2, 38). The Au-particles on the bottom (a) on the other hand, are not assumed to come from the catalytic droplet on top of the nanowire and is based on two reasons:

i. The lack of dispersed Au-particles in the middle part of the nanowire. A continuous loss of Au during growth would have left Au-particles along the whole

axial length of the nanowire, but this is assumed not to be the case because of the discontinuity in Au-particles on the nanowire surface between the top- and bottom-part of the nanowire.

ii. The Au-particles seem to cover the whole radial size of the nanowire and not only the crystalline core.

If the diffusion of Au happens during the axial growth of crystalline silicon it is assumed that the Au-particles either would induce branching of the nanowire or get covered in amorphous silicon because of radial growth of amorphous silicon. But since no branching is observed and the Au-particles seem to cover the whole diameter of the nanowire it is assumed that the formation happens at the end of the growth procedure.

Based on this it is assumed that diffusion of Au happens after nanowire growth and implies that it happens during the final purging steps (~20 min) after SiH₄ cut-off when the temperature is still high enough (500°C) to promote elevated diffusion-rates⁽³⁸⁾.

iii. Reduced diffusion-length compared to earlier investigations on intrinsic nanowires. The Au-particles on the top of the investigated nanowires seem to have diffused ~35nm from the main catalyst particle. In comparison, earlier experiments performed by the author on intrinsic nanowires showed an average diffusion length of ~170nm (Figure 4.15)⁽²⁾. By assuming that the diffusion from the Au-Si droplet happens during the final purging-procedure (after completed growth) one may assume an approximately constant diffusion-time for all samples (as the purging time is held constant for all experiments) and implies a lower diffusion rate for the gold particles in this experiment compared to earlier. This may be a result of the Au-particles diffusing on an amorphous surface (in this case) instead of a crystalline surface (as earlier), and supports the assessments performed above. This has earlier been confirmed for nanowires covered in SiO₂⁽⁸⁵⁾ which also is an amorphous structure.

The Au-particles on the bottom of Figure 4.18 (b) is therefore assumed to come from Audroplets residing on the Si-surface (Figure 4.19 (b)) after finished growth. The reason why this in this case only is observed on heavily tapered nanowires and not on intrinsic nanowires is assumed to be a result of the recused growth-density. Compared to earlier intrinsic growth⁽²⁾ the nanowire density on the investigated sample (DB14) is drastically reduced which implies larger residing deposits of Au on the sample surface, allowing diffusion of Au-onto the nanowire walls.

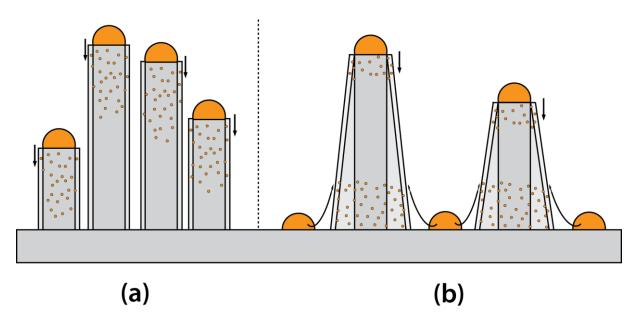


Figure 4.19: It is assumed that because of the high density of grown nanowires there are minimal amounts of Au-residues left on the Si-substrate at intrinsic growth and therefore only the top of the nanowire is covered in gold particles (*a*). In comparison, because of the lower density of grown nanowires for sample DB14 it is assumed that more Au-droplets reside on the Si-surface and the gold particles observed on the bottom of the nanowires is assumed to come from these residing Au-droplets by diffusion (*b*).

4.2.3 Phosphorus Doping

As observed in Figure 4.10, PH_3 does not seem to affect the nanowire growth to the same extent as B_2H_6 . The following properties can be observed from the SEM images:

- A reduction in average nanowire length at increasing dopant flows.
- An approximately constant nanowire diameter with no apparent tapering effect.
- A generally low density of nanowires compared to boron and intrinsic doping.

It was known that boron was used in the chamber the day before, but by comparing the first intrinsic sample (DP22) with the last sample in the boron series (DB16) one can assume that the chamber is approximately free of boron residues.

Nanowire length:

A continuous reduction is observed in the average nanowire length with increasing PH₃ dopant ratio. A reason for this effect is the possible deposition of phosphorus on the catalytic droplet as earlier pointed out for B₂H₆ (Figure 4.13), possibly reducing the number of adsorption sites and making the Si-transport to the droplet surface rate-limiting^(70, 87). The reduction in length is much more abrupt for PH₃ than for B₂H₆ and may be additionally attributed to a simultaneous "poisoning" effect for phosphine. Earlier reports performed on conventional CVD of silicon have shown that the addition of PH₃ to the gas-flow effectively "poisons" the silicon surface and drastically reduces Si growth^(28, 88) which in this case also may be related to nanowire growth. The maximum dopant ratio possible before growth is completely inhibited seems to be $\sim 10^{-2} - 10^{-1}$ (Table 4.3) which is in agreement with earlier experiments⁽⁷⁰⁾.

Reduction in nanowire density:

As also observed for B₂H₆-doping a reduction in nanowire density is observed for PH₃-doping

at increasing dopant-flows, but it seems that the reduction may be attributed to two different processes. As earlier presented B_2H_6 increases the deposition-rate of amorphous silicon and the catalytic particles are assumed to be covered in this amorphous material at a faster rate than their own growth-rate (DB15). PH₃ catalytic droplets however, seem to be present even at high dopant-flows (DP25) indicating a blocking-process possibly related to the same "poisoning" effect of phosphine as previously mentioned.

This may be related to nanowire growth by assuming a reduction in the amount of nucleated catalytic droplets because of nearby adsorbed P-atoms on either the Si-surface of Au-Si droplets, effectively reducing the density of incubated droplets.

As PH₃ blocks Si-growth on the Si-surface the catalytic droplets will still be visible without any covering silicon.

No observed tapering effect:

No radial growth / tapering was observed by the addition of PH_3 to the gas-flow as earlier found by other research groups ^(64, 70). The reason for this is assumed to be the same as previously presented; PH_3 added to the gas-flow effectively blocks the adsorption of SiH₄ and deposition of Si on silicon-surfaces (Si-substrate and nanowire walls) and will prevent any uncatalyzed radial growth of the nanowires.

4.2.4 Summary and Solar Cell Specifics

This chapter has mainly covered the effects on the nanowire morphology from adding dopantgases to the gas flow. It has been difficult to replicate the intrinsic morphology attained in previous experiments⁽²⁾ for the given growth-conditions ($T = 500^{\circ}C$, $p_{SiH4} = 100mTorr$) assumingly because of chamber contaminations. However, a stable growth-regime was found after performing a plasma-clean of the chamber and was used to investigate the effect from different flows of B_2H_6 and PH_3 added to the growth-conditions mentioned above. Both addition of B_2H_6 and PH_3 seems to reduce the attained length/growth rate of the nanowires assumedly because of blocking of SiH_4 adsorption-sites; reducing the feed of Si to the catalytic droplets. However, the effect seems to be more prominent for PH_3 because of a simultaneous "poisoning" effect of the surface.

The addition of B_2H_6 seems to promote radial growth of a-Si on the nanowire walls because of a lowering of the activation energy needed for Si-deposition on a silicon surface, and is assumed to be a result of a gaseous reaction between SiH₄ and B₂H₆. The nanowire still contains a crystalline core, but is covered in an amorphous layer.

The same reaction is assumed to be the reason for an observed reduction in the nanowire density at higher B_2H_6 -ratios; where the deposition-rate of silicon on the substrate surface becomes higher than the axial growth-rate of nanowires. Radial growth is not observed when adding PH₃ to the gas flow assumedly because of the same blocking-effect as mentioned before; reducing the deposition of Si on a silicon-surface to a negligible rate.

 B_2H_6 seems to be unfavourable at higher dopant-flows because of the observed taperingeffect. The amorphous layer formed may have large implications on the electrical behaviour of the nanowire⁽⁷⁰⁾ and should be prevented. Previous investigations have found TMB to be a worthy alternative^(63, 64) as it seems to not increase the deposition-rate of a-Si and induce tapering as with B_2H_6 . Another alternative procedure was presented by S-J Whang⁽⁷⁶⁾ where successful incorporation of B-atoms into the structure was achieved by a post-synthesis in situ plasma B_2H_6 doping process. A clear preference for a tilted growth direction was also observed, mainly the <011>-direction.

 PH_3 on the other does not seem to affect the nanowire growth to the same extent as B_2H_6 . Tapering is not observed but a drastic reduction in nanowire length and a generally low density is observed for increasing PH_3 -rates and is attributed to the adsorption and "poisoning"-effect of P-atoms on both the Au-Si droplet and Si-surfaces. Nucleation seem to be completely inhibited at a PH_3 -ratio of ~ 10^{-2} , in agreement with experiments earlier performed by Schmid et $al^{(70)}$. However, PH_3 is still considered by many as the best alternative for n-type doping of nanowires⁽³⁾.

Solar Cell Specifics:

Today solar cells are designed with a very small n-side (Ch. 2.4.1) in order to maximize the solar cell efficiency, and in order to keep this n-side small and promote low sheet-resistivity it is usually doped as high as possible $(N_D \sim 10^{19} \text{ cm}^{-3})^{(39, 59)}$. By setting this as the desired concentration for phosphorus doping of the n-side in a solar cell pn-junction (Figure 2.22) one may find the width of the depletion region (*W*) as a function of the concentration for boron doping (*N_A*) of the p-side of the pn-junction, as shown in Figure 2.23.

This figure covers a segment of the depletion-width assumed to be representative for nanowires. As an example, a typical ~40nm thick nanowire may hold a maximum depletion width of ~20nm and requires a p-side dopant concentration (N_A) of ~5.0 × 10¹⁸ cm⁻³.

The n-side: Earlier experiments performed by Schmidt et al⁽⁷⁰⁾ found that the upper PH₃-to-SiH₄ ratio limit of 10^{-2} earlier presented (Ch. 4.2.3) corresponds to a phosphorus dopant concentration of ~ 10^{20} cm⁻³. A concentration of 10^{19} cm⁻³ therefore seems plausible but because of the low growth-rate attained at these dopant gas ratios an increased growth-time is expected.

The p-side: Earlier experiments by Pan et al⁽⁷⁵⁾ have shown that a B_2H_6 -to-SiH₄ ratio interval of $\sim 4.0 \times 10^{-6} - 1.4 \times 10^{-2}$ corresponds to a boron dopant concentration interval of $\sim 10^{18} - 10^{19} cm^{-3}$ respectively. However, the current experiment has found that a nanowire tapering effect becomes noticeable already at dopant-ratios of $\sim 5.0 \times 10^{-5}$ (DB13) and the required boron dopant ratio may therefore not be reached without expecting nanowire tapering. A possible solution will therefore be to reduce the required p-side dopant-concentration (N_A) enabling the use of lower dopant gas ratios but will again require thicker nanowires because of the increase in necessary depletion width (Figure 2.23).

4.3 Lithographic Preparations for Electrical Measurements

In order to successfully make single nanowire contacts a thorough preparation and investigation had to be performed in order to find the correct lithographic parameters and to attain good results. The report focuses on developing a complete lithographic method for nanowire contacting and the investigated parts will first be reported separately and finally presented together as a complete process. The following lithographic steps had to be investigated:

- i. Printing of the Orientation-Pattern / Inner Contact Pads (*Ch. 4.3.1*).
- ii. Printing of the Outer Contact Pads (*Ch. 4.3.2*).
- iii. Printing of the Nanowire Contacts (*Ch. 4.3.3*).
- iv. Dispersion of nanowires on the sample (Ch. 4.3.5).

Please see Figure 3.3 for definitions of the different contacts.

4.3.1 Orientation-Pattern and Inner Contact Pads

In order to be able to orientate on the sample surface (Ch. 3.3.2) in a microscope an orientation pattern is needed. Additionally this pattern also consists of the so-called *Inner Contact-Pads;* bridging the main *Outer contacts* with the small *Nanowire Contacts*.

Megaposit SPR700 1.0 was chosen as the preferred resist and may be spin-coated at 6000 RPM in order to attain the desired film-thickness of ~900nm.

In order to attain good results the following parameters had to be tuned (Ch. 2.6):

- *i.* Resist-to-metal-thickness ratio: In order to attain successful lift-off.
- ii. Development time: In order to attain a good high-resolution pattern.
- iii. *Exposure dose:* A too high / low exposure dose will result in overexposure/underexposure of the resist, resulting in the same effects as for underdevelopment/overdevelopment.

The initial sample (OM01) was set with parameters assumed to give lift-off (a ratio of resist to metal higher than 7:1); with a spin-speed of 6000 RPM and a metal-thickness of 50nm Al. The 20 sec development time was chosen only as an initial point for further investigation. Lift-off was successful for this sample but 20 sec of development caused a large amount of overdevelopment (Figure 4.20 (a)) and further investigations therefore had to focus on optimising the development time.

Optimisation of the development time:

The development time was reduced to 15 and 10 sec (for OM02 and OM03 respectively) which displayed a general increase in pattern accuracy and resolution (Figure 4.20 (b)) because of less overdevelopment (Ch. 2.6).

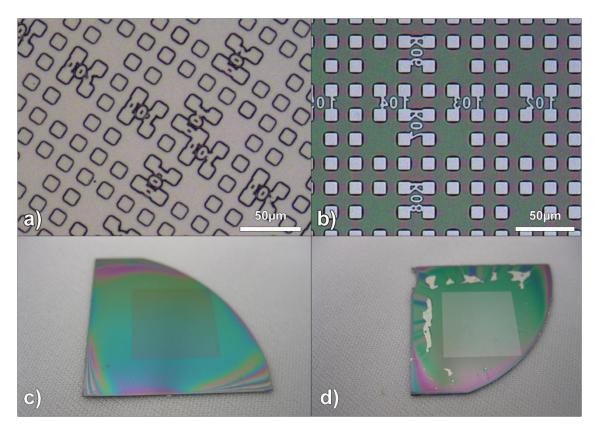


Figure 4.20: (*Light microscopy imaging; before metallization*) Printed patterns attained for OM01 (*a*) and OM03 (*b*). An increase in pattern accuracy and resolution is observed by reduction in the development time from 20 sec to 10 sec. An example of a printed orientation pattern before (*c*) and after lift-off (*d*) with an Al-deposit.

A full-size photo of the samples before and after lift-off with Al-deposit is shown in Figure 4.20 (c) and (d) respectively.

All later attempts to replicate the previously attained results for OM03 failed and resulted in very bad patterns (Figure 4.21 (a)). A solution to this problem was to further reduce the development time. Tests were performed at 5, 2 and 1 sec development (OM5, OM6 and OM7 respectively) with best results attained for 5 and 2 sec. The optimised development time was therefore set to ~3 sec (OM08; Figure 4.21 (b)).

Later reports from NTNU Nanolab showed that one of the hot-plates used in this experiment suffered from a problem with the thermostat, resulting in a temperature of $\sim 25^{\circ}$ C higher than indicated by the thermometer. Since the amount of evaporated solvent and internal stresses in the photoresist depends on the temperature and time used in the soft-bake step, this could change the necessary parameters for later processing steps, such as for exposure and development. It is known that this part of the experiment employed the mentioned hot-plate in combination with others, but no notes were taken on which sample used which hot-plate. This hot-plate was later fixed, but further hot-plate usage was monitored more closely and mostly kept to one hot-plate. All the proceeding samples used in this experiment employed a development time of 3 sec, but because of the problems with the hot-plate it may be assumed that later tries to replicate these samples may need a completely different development time.

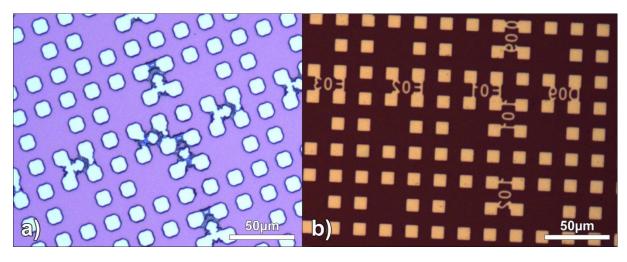


Figure 4.21: (*Light microscopy imaging*) Unsuccessful replicas of OM03 resulted in pattern shown in (*a; before metallization*), possibly because of a problem with one of the hot-plates. Further reduction in development time resulted in better patterns, as shown in (*b; after lift-off*).

Optimization of the metal-deposit thickness:

Some of the samples got a metal-deposit during the resist-investigation (Table 3.14) in order to do a simultaneous investigation on the desired metal thickness. This was assumed to be an applicable method since lift-off mainly depends on the ratio between the resist and metal thickness and since the resist thickness was held constant at all samples.

The first two metal deposited samples (OM01 and OM03) got deposited 50nm of aluminium, and lift-off proceeded readily for both samples as assumed. The next deposit (OM06) was therefore increased to the desired thickness of 90nm, which also gave successful lift-off, but with the support of a brush. Using a brush was in this case not destructive to the pattern and resulted in good patterns.

Aluminium proved to be difficult to use as orientation-pattern material because of low contrast-difference when used together with silicon in Scanning Electron Microscopy, and made scanning speeds higher than speeds used for image-capturing very difficult. The long scanning-time at these speeds makes it unusable for orientation purposes.

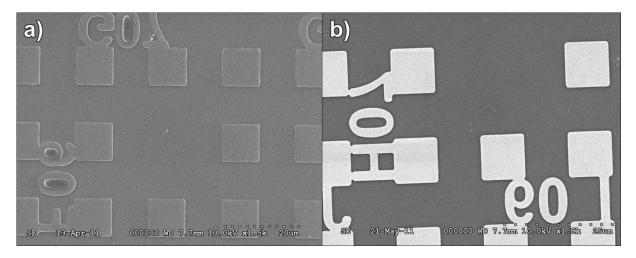


Figure 4.22: (*Scanning Electron Microscopy*) Contrast difference between inner contact-pads samples metallized with Al (*a*; *after lift-off*) and Au (*b*; *after lift-off*).

The reason for this low contrast-difference is the similarity in atomic structure; Aluminium is next to silicon in the periodic table which implies an almost similar atomic mass and density. Aluminium will send approximately the same amount of secondary electrons as silicon back to the detector and will therefore look almost identical (Figure 4.22 (a)). In order to make the orientation usable at higher scanning speeds and speed up the process gold was investigated as an alternative to aluminium. Gold has a much higher atomic number than aluminium and displays a higher contrast to silicon (Figure 4.22 (b)), and lift-off was successfully performed

for the gold structure; with 10nm Ti and 80nm Au (OM08). Titanium is used to increase the adhesion between gold and silicon. Gold do not oxidise under normal conditions in contrast to aluminium which almost instantly forms a thin (2-3nm) surface-layer of Al_2O_3 , and will therefore be a better material to use for multi-layer contacting as oxides between the layers may inflict on the transport properties of the contacts (contacts which is desired to be Ohmic may become Schottky contacts instead; Ch. 2.5.2). Based on these results gold was

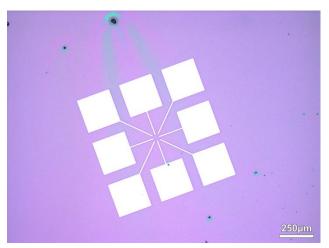


Figure 4.23: (*Light microscopy imaging; after lift-off*) Attained pattern for outer contact-pads with the same parameters optimized for the inner contact-pads (Ch. 4.3.1).

ultimately chosen as the desired metal used in orientation patterning. In order to maintain compatibility between the different contacts the outer contacts and nanowire contacts was ultimately also tested with gold as contact material.

Optimization of the exposure dose:

As good results was attained for the initial exposure dose of 125mJ/cm² no further optimization was necessary.

This concludes the lithographic investigation performed on the inner contact-pads, and a summary of the chosen parameters for this step is as following:

	Photoresist: Photoresist spin speed:	Megaposit SPR700 1.0. 6000 RPM @ 45 - 60 sec.
	1 1	~900nm.
-	Sizing energy:	125mJ/cm^2 .
-	Development time:	~3 sec.
-	Metal deposit:	90nm Al or 10nm Ti + 80nm Au.
		(Ti + Au are preferred for increased contrast
		between the orientation structure and the silicon
		structure).
-	Development time:	 125mJ/cm². ~3 sec. 90nm Al or 10nm Ti + 80nm Au. (Ti + Au are preferred for increased contrast between the orientation structure and the silicon

4.3.2 Outer Contact Pads

The outer contact pads were to use the same lithographic parameters as found for the orientation-pattern. The pattern shown in Figure 4.23 is attained with the same finalised parameters as used for the *Inner Contact Pads* (Ch. 4.3.1). Lift-off was successful with both metal deposits as earlier employed for the inner contact-pads.

4.3.3 Nanowire Contacts

This step mainly covers the determination of desired resist and its parameters for making the *Nanowire Contacts* by electron-beam lithography.

Note that the acceleration voltage for the Scanning Electron Microscopy was initially set to 10kV in this part of the investigation.

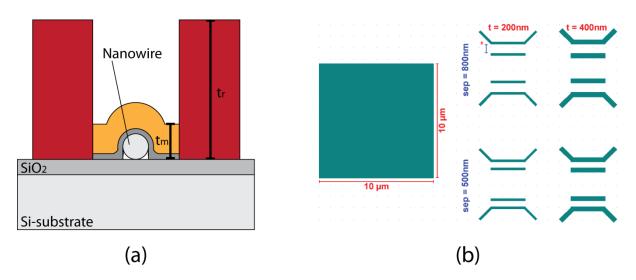


Figure 4.24: Illustration of the necessary photoresist-thickness-to-metal-thickness ratio (~7:1). (b) The pattern used for initial PMMA A2 samples (*a*). The pattern consists of 200nm and 400nm thick lines which are separated by 800nm and 500nm and an additional $10x10\mu$ m rectangle (*b*).

PMMA A2:

PMMA A2 has the smallest film-thickness possible for the 950PMMA series (App. B (a)) and since a smaller film-thickness implies a higher resolution⁽¹⁰⁾ on the printed pattern some initial testing was performed on this resist. The PMMA A2 samples were mainly written with the pattern shown in Figure 4.24 (b) by EBL (App. A.2).

The first step is to determine the necessary resist-thickness needed (Figure 4.24 (a)) in order to attain successful lift-off, and the development time was therefore temporarily set to a constant value of 30 sec.

Film-uniformity: The initial samples (A201, A202 and A203) were coated with different film-thicknesses (~170nm, ~150nm and ~110nm respectively). Note that these resist thicknesses are far under the guiding thickness of ~350nm and that all of the samples are spun at speeds lower than the recommended limit in order to get thickness as thick and close as possible.

Samples A201 and A202 employed speeds of 1000 RPM and 1200 which resulted in uneven films because of excessive vibrations in the spin-coater and could therefore not be used. A203 was spun at 1500 RPM which gave good films and was chosen as a basis for further research (Figure 4.25 (a)) as this seemed to be the thickest resist-thickness possible in combination with good and even films.

Lift-off: Several lift-off attempts were performed on 50nm metal-thickness (Al and the Ti + Au combination) but success was only attained when brushing relatively hard with a brush. Using a brush is not an ideal procedure as it easily destroys smaller structures (ex. A203 in Figure 4.25 (b)) and could possibly destroy the nanowires supposed to be contacted. The metal-thickness was reduced to 30nm (~4:1) and left for lift-off in acetone for 72 hours but brushing was still needed in order to perform successful lift-off (A206).

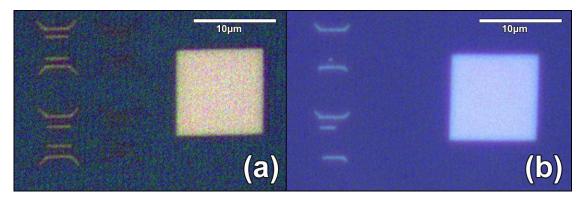


Figure 4.25: (*Light microscopy imaging*) Sample A203 before (*a*) and after (*b*) metal deposit (dosage of 200µC/cm²). Lift-off was supported by brushing, which destroyed a large part of the smaller features.

The results showed that the PMMA A2 resist cannot be used in this case because of its limited thickness possibilities at good film uniformities. Alternative and thicker photoresist had therefore to be investigated.

Further assessments of alternative photoresists (PMMA A4 and A7):

The thicker PMMA A4 (~200 -300nm) and A7 (~400-600nm) resists were therefore to be investigated. The first series consisted of the following samples and employed the pattern given in Figure 4.26:

- A401 (PMMA A4): 2000 RPM resulting in ~300nm of resist.
- A701 (PMMA A7): 2000 RPM resulting in ~600nm of resist.

The samples were written with the desired

pattern by EBL, developed and deposited with 50nm of Al (Table 3.16). Lift-off was successful for all samples and resists without

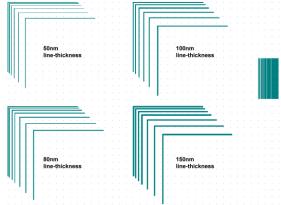


Figure 4.26: Alternative pattern used for PMMA A4 investigations.

the use of a brush and other factors had to be assessed in order to determine the preferred photoresist to use.

Because of the small sizes of the contacts a high resolution is needed and a guiding rule is that thinner photoresist results in higher resolution. Since A4 and A7 practically is the same resist, only diluted to respectively 4% and 7% in order to get different thickness-intervals A4 is chosen over A7 as it may be spun to a thickness closer to the desired resist-thickness. Better separation of lines and a more rectangular rectangle is observed for the PMMA A4 sample in Figure 4.27 (a) compared to for PMMA A7 (b) and indicates a better resolution for the A4 resist (dosage of 200μ C/cm²).

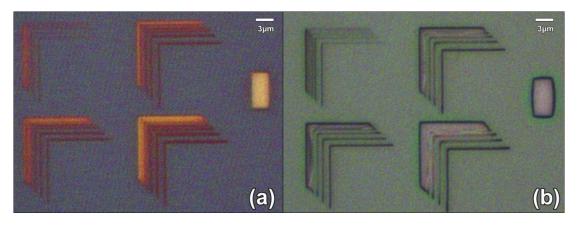


Figure 4.27: (*Light microscopy imaging; before metallization*) A401 based on PMMA A4 (a) compared to A701 based on PMMA A7 (b) for a dosage of 200μC/cm². Complete dosage-matrix is given in App. C.

PMMA A4:

The resist thickness could now be increased beyond the limit for PMMA 2. Two initial samples (A402 and A403) where coated with a 300nm film and with still a constant development time. Both of them consisted of equally good patterns printed with very little differences. It seems that the resolution attained for PMMA A4 (Sample A402) is comparable to the resolution attained for PMMA A2 (Sample A205) for the given feature-sizes, as shown in Figure 4.28 ((a) and (b)).

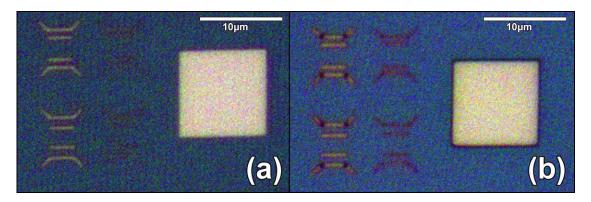


Figure 4.28: (*Light microscopy imaging; before metallization*) Attained pattern for samples A205 based on PMMA A2 (a) compared to A402 based on PMMA A4 (b) for a dosage of 200μC/cm². Complete dosage-matrix given in App. D.

Lift-off was problematic for some of the samples coated with 300nm resists and it was decided to increase the resist thickness. Two samples were set with an increased resist

thickness (A404 and A405) which both showed good lift-off. Note that both of the spinspeeds is lower than the recommendation-limit (App. B) but this was assumed to be okay since a good film-uniformity was observed for both the cases. Note that PMMA A7 at a maximum spin-speed could also have been used in order to attain a 400nm thick film, but it is neither recommended to spin a photoresist at its maximum spin-speed. PMMA A4 was therefore chosen over PMMA A7 as a compromise as it showed to give stable films at the given spin-speeds.

The temporary spin-parameters for nanowire contacting were therefore set to:

- Photoresist:
- Photoresist spin speed:
- Resulting photoresist thickness:
- Metal deposit:

MicroChem 950 PMMA A4 1500 - 1750 RPM @ 45 sec. ~370 - 340nm. 50nm for Al or 5nm Ti + 45nm Au (Dependent on the material used for the *Outer Contact Pads*).

Two parameters still remained to be investigated, the development time and the exposure dose which both strongly influence the resolution of the printed pattern.

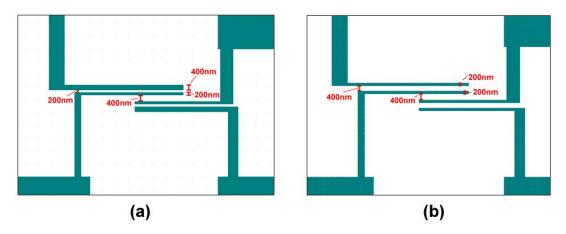


Figure 4.29: Patterns designed for a hypothetical ~ 2μ m long nanowire used for investigations of the PMMA A4 and C4 resists; Pattern 1 (*a*) and Pattern 2 (*b*).

Development time (Table 3.18): Two initial samples were printed with 15 and 5 sec development time (A406 and A407 respectively), and successful development were observed for both. Some overdevelopment was still observed for 5 sec and another sample was therefore set with 3 sec development (A408). This sample did not show any signs of further reducing the overdevelopment, and since the development time already is critically low it could instead be a result of overexposure. The development time was therefore set to a temporary constant value of 3 sec while investigating the exposure dose.

Exposure dose (Table 3.19): The influence of the exposure dose on the pattern is very clear by comparing the different matrixelements in appendix C (a). The smaller lines look to be well separated for doses lower than 400 μ C/cm² but the best result seems to be for a dose-interval of 200-300 μ C/cm² especially by looking at the large rectangle, which should be as rectangular as possible. Further investigations were therefore performed on exposure doses around 200 μ C/cm². Most of the investigations performed up until now have mainly been performed by light-

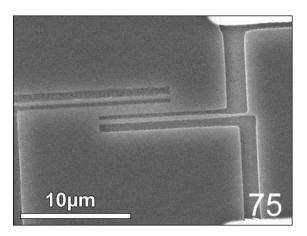


Figure 4.30: (*Scanning electron microscopy; before metallization*) The best pattern attained for Pattern 1 on sample A409 with a exposure dose of \sim 75µC/cm².

microscopy because of microscope-availability and the necessity of a quick assessment to get a coarse overview of the patterns.

From now on however the small feature sizes required Scanning Electron Microscopy imaging in order to be more accurately analysed.

Two version of a new four-contact pattern (Figure 4.29) were designed especially to resemble a nanowire contact-structure for a ~2 μ m long nanowire. The initial sample (A409) was written with a matrix of the pattern in Figure 4.29 covering a dose-interval of 50 – 230 μ C/cm² (Figure E.1). The best pattern was attained for an exposure dose of ~75 μ C/cm² (Figure 4.30). As observed in the figure there is a reduced distance between the two contacts in the 90°-bend which may cause problems for later lift-off procedures.

The same matrix was repeated the next day with the same parameters (A410) as for A409 but with different results. This time all doses resulted in the lines growing together, even at the lowest dosage of 50μ C/cm² indicating some stability issues. A new sample (A411) was printed with both patterns presented in Figure 4.29 ((a) and (b)) in order to investigate this apparent stability issue.

The resulting patterns are shown in Figure 4.31 ((a) and (b)) which shows overexposure in both cases. As none of the patterns were successful in reproducing the result attained in sample A409 it might just have been a one-time coincidence and further reduction in exposure dose was performed in order to find a solution to this problem.

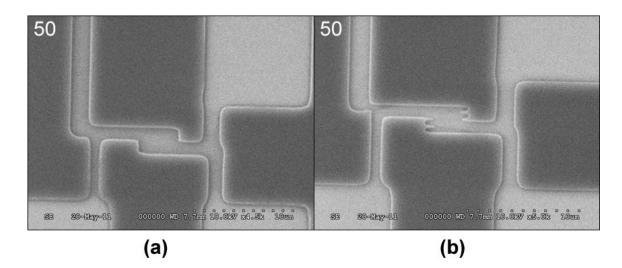


Figure 4.31: (Scanning electron microscopy; before metallization) The patterns (Pattern 1 in (a) and Pattern 2 in (b)) attained for sample A411 at a dosage of 50μ C/cm² showed a large degree of overexposure.

The same two patterns as used for sample A411 (Figure 4.31) were written onto a new sample (A412), but with a matrix covering a dosage-interval of $10 - 50\mu$ C/cm².

The new results showed that the best pattern now was attainable at a dosage of $\sim 20\mu$ C/cm² for both patterns (Figure 4.32). Both matrixes are fully presented for both patterns in Figure E.2 and Figure E.3 and by comparing the patterns attained for both patterns at 25μ C/cm² obvious stability issues still exist.

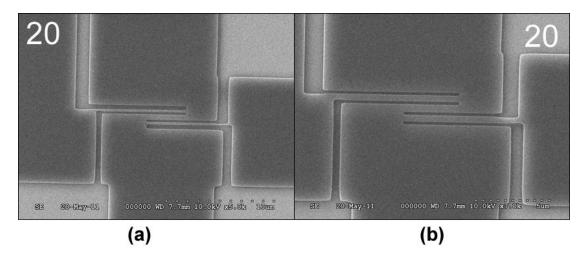


Figure 4.32: (*Scanning electron microscopy; before metallization*) A reduction to 20μ C/cm² for sample A412 resulted in good patterns for both patterns (Pattern 1 in (*a*) and Pattern 2 in (*b*).

In order to check the stability of the dosage a new sample was printed with the same patterns and the same dose-interval (A413). All patterns at all exposure doses showed a critical

overexposure with lines growing together. The stability issue was again confirmed by setting a last sample (A414; Figure 4.14) with a dosageinterval of $15-23\mu$ C/cm². The best pattern was now found at a dosage of 15μ C/cm² as shown in Figure 4.33.

Apparently there are large stability issues in the exposure dose needed for the PMMA A4 resist. It is noteworthy that the exposure dose to attain good patterns is much lower than the

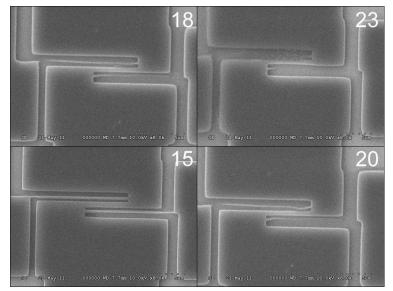


Figure 4.33: (*Scanning electron microscopy; before metallization*) Sample A414 was written with Pattern 1 in a dosage-interval of $15-23 \mu C/cm^2$.

recommended dosage-interval of 50-500 μ C/cm^{2(74).} The necessary development time of ~5 sec is also remarkably low compared to the standard recommended development time of 30 sec⁽⁷⁴⁾. Other research groups at NTNU Nanolab performing experiments with the PMMA A4 have reported good results at much larger development times and exposure doses (20 -30 sec for 400 μ C/cm²).

Mainly two possible reasons for the observed instabilities have been found:

- Old resist.
- Low acceleration voltage.

Old resist: Photoresist have an expiry date but may normally be used up to one year after this date, or until problems start to arise. The photoresist used was found to be several months overdue which could be the reason for the observed problems.

Low acceleration voltage: Another possible reason for the problems is the choice of acceleration voltage which may be too low. It has later been found that the recommended acceleration voltage for this type of EBL-resist is within an interval of $20-50 \text{kV}^{(74)}$. Electrons have a wavelength so small that diffraction no longer may define the lithographic resolution. The resolution is instead limited by optical aberrations and scattering of electrons from the resist and substrate, and is commonly referred to as proximity effects. A. van de Kraats⁽⁸⁹⁾ performed experiments on these limitations and found that this proximity effect may cause a widening of the exposed region because of the electrons from the beam interacting with the structure of the resist and substrate. This would expose resist which normally should not be exposed, and ultimately result in small features growing together as observed in this experiment. It was concluded that one should prefer to use as high electron beam energy /

acceleration voltage as possible when doing electron beam lithography as long as care was taken not to expose the resist to excessive heating.

Based on this, the acceleration voltage was increased from 10kV to a minimum of 20kV to prevent possible proximity effects and observe if this eliminates the observed instabilities in the exposure dose.

Several new PMMA A4 samples were attempted but new problems with the film-stability arose. During spin-coating no stable photoresist-film could be attained even at spin-speeds in the recommended interval of the spin-curve and strengthens the possibility of old resist. The PMMA A4 resist was therefore rejected and replaced with a newer PMMA C4 which is the same photoresist only with chlorobenzene as solvent. PMMA A7 was also an alternative but since it had been mixed from the same precursors as the PMMA A4 and had the same expiry date this resist was also rejected.

Final investigations employing PMMA C4 resist:

PMMA C4 is not able to get as thin resist-thicknesses as PMMA A4 and was spin-coated to a thickness of 500nm.

Exposure dose: The initial sample (C401) was printed with a matrix covering the dosageinterval of $20 - 360\mu$ C/cm² and an increased development time of 20 sec. An increased acceleration voltage of 20kV was used from now on. The resulting matrix for both patterns is shown in Appendix F (Figure F.1 and Figure F.2) and the best patterns were attained for a dosage of ~80 μ C/cm² (Figure 4.34 (a) and (b)).

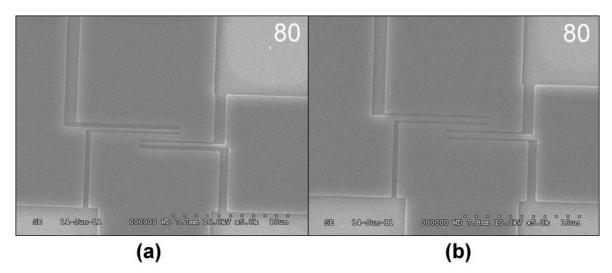


Figure 4.34: (*Scanning electron microscopy; before metallization*) The best initial patterns attained for the PMMA C4 resist (sample C401) was written with a exposure dose of $\sim 80 \mu$ C/cm² (Pattern 1 in (*a*) and Pattern 2 in (*b*)).

As seen from the appendix and Pattern 2 (Figure F.2) has a higher threshold on the degree of overdevelopment compared to Pattern 1 (Figure F.1). Pattern 2 may be used with doses $\leq 180\mu C/cm^2$ before the lines get to close to each other while Pattern 1 may only be used with doses $\sim 80\mu C/cm^2$. Later samples (C402 and C403) showed that these results are replicable but a dose $\geq 100\mu C/cm^2$ should be preferred because of possible underexposure of the pattern. Both patterns were found usable up to a dose of $150\mu C/cm^2$ which therefore is

selected as the desired dosage. Note that because some overdevelopment must be expected Pattern 1 is not ideal as the contacts seem to be too close, and a minimum distance between the contacts should therefore be set to 400nm as in Pattern 2.

Compared to PMMA A4 the PMMA C4 shows a more common behaviour. A development time of ~20 sec is a commonly used time and is easier to maintain constant compared to a development time of ~3sec. The exposure dose for PMMA C4 is also improved to a dose of ~ 100μ C/cm² which is within the recommended dosage for this type of resist. Summarised, PMMA C4 seems to be more stable than PMMA A4 with more commonly used values for the development time and exposure dose and the problems attained with PMMA A4 may therefore be linked to a possibly bad/old resist. Further investigation was not performed on the acceleration voltage and was set to a recommended value of 20kV in order to prevent possible proximity-issues.

Lift-off and Resist-bubbling: Some final lift-off investigations were performed on the PMMA C4 resist. 5nm of Ti and 45nm of Au was deposited by E-Beam Evaporator as before. Normal procedure is to fasten the sample to a Si-wafer (100mm in diameter) with carbon-tape and insert the Si-wafer into a standard steel-based E-Beam sample-holder before insertion into the chamber. After deposition all samples looked like the one in Figure 4.35 (*a*) showing bubbling of the resist. This effect arises when the sample gets too hot and is in most cases a result of low thermal conductivity of the carbon-tape and/or the Si-wafer. Lift-off was possible but with hard brushing and most of the printed structure was destroyed in the process.

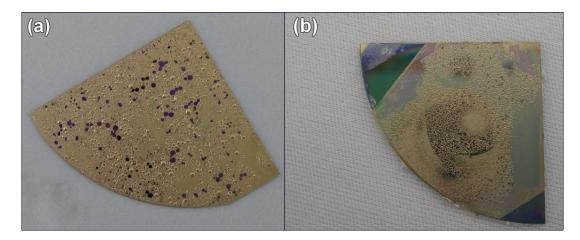


Figure 4.35: Samples deposited with Ti + Au in the E-Beam Evaporator were exposed to resist-bubbling assumedly because of the high temperature needed to deposit titanium (*a*). By replacing the standard adhesive carbon-tape with Mung II SiO₂ thermal paste and the Si-plate with a Cu-plate better results were attained (*b*).Note that the blank areas in (*b*) comes from tape holding the sample in place on the plate.

Two possible solutions were attempted in order to improve the thermal conductivity:

- i. Replace the carbon-tape with a thermal SiO₂-based paste, Mung II.
- ii. Replace the 100mm Si-wafer with a copper-plate (Cu).

The first sample (C404) was tested only by replacing the carbon-tape with Mung II which resulted in an easier lift-off but brushing was still necessary and the resist still bubbled. The next sample (C405) was tested with both (i) and (ii) which resulted in much less bubbling (Figure 4.35 (b)) and lift-off proceeded readily within minutes without the use of a brush. Heating therefore seems to drastically affect the final product by bubbling of the resist and results show that precautions should be taken in order to increase the transport of heat away from the sample.

Some testing was also performed on aluminium at standard conditions which resulted in good films without any resist-bubbling at all, and is assumed to be a result of a cooler chamber. The heat is assumed to mainly come from the heating of the metal-targets in order to evaporate the necessary amount of metal for deposition. In order to evaporate aluminium a temperature of 821°C (for a vacuum of 10⁻⁶ Torr) is needed while gold and titanium needs 807°C and 1235°C respectively⁽⁹⁰⁾. The increased temperature needed for titanium may be the reason for the resist-bubbling experienced for the Ti-Au deposit.

Final thoughts on the development-time: After lift-off some discontinuities were found in the metal-contacts (Figure 4.36 (a) and (b)). Because of the soft and circular characteristics of the discontinuities this is assumed to be a result of underdevelopment where some resist still remained in the pattern during lift-off. These resist-residues will result in lifting off excess metal from the pattern and typically result in the observed patterns attained. Further investigations should therefore include investigating a possible increase in development time. This effect may also be a problem resulting from the resist-bubbling but since larger features do not seem to have the same problems it is more likely that it is due to underdevelopment in the smaller features of the pattern. Smaller areas are harder to penetrate for the development-liquid and may require more time than larger areas. A possible solution to this may be to stir the sample during development.

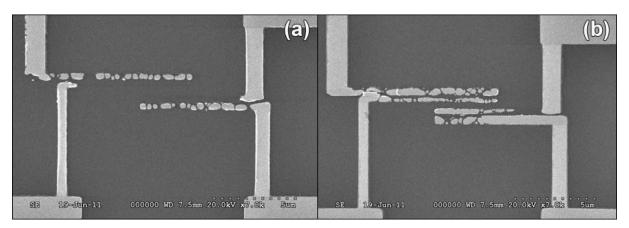


Figure 4.36: (*Scanning electron microscopy; after lift-off*) After lift-off much of the contacts disappeared ((*a*) and (*b*)). Because of the roundness of the remaining structure this was assumed to be a result of either underdevelopment or the experienced bubbling of the resist.

Final thought on the EBL writing-parameters:

During final investigations (C406) the pattern-quality seemed to strongly depend on the writing-parameters chosen by the EBL-machine. Up until now the only parameters set by the user in the EBL-software is the measured *beam-current* and the desired *exposure dose* while

automatically calculating the last parameters in the software (Table 4.4). These automatically calculated parameters include the *step-sizes* and *dwell time* of the beam (App. A.2). What was observed when printing both patterns on the same sample was the different *step-size* and *dwell time* automatically chosen for the two patterns even if the dosage was the same for both (Figure 4.37). Both of the patterns shown in Figure 4.37 should equal the patterns shown in Figure 4.34 but as this was not the case this had to be investigated. A significant difference was found in the mentioned parameters for the pattern in Figure 4.37 compared to the other patterns written at 100μ C/cm²:

Sample	C401		C406		C407	
Pattern	Pattern 1	Pattern 2	Pattern 1	Pattern 2	Pattern 2	
Beam Current	0,0401nA	0,0401nA	0,0401nA	0,0401nA	0,0399nA	
Area Dose	100μC/cm ²	100μC/cm ²	100μC/cm ²	100μC/cm ²	$100 \mu C / cm^2$	
Step Size	0,006µm	0,006µm	0,006µm	0,02µm	0,006µm	
Dwell Time	0,000898 <i>ms</i>	0,000898 <i>ms</i>	0,000898 <i>ms</i>	0,009977 <i>ms</i>	0,000902 <i>ms</i>	

Table 4.4: Employed writing parameters for sample C401, C406 and C407.

The parameters are calculated by the following equation:

$$Area \ Dose = \frac{Beam \ Current \ \times \ Dwell \ Time}{Step \ Size^2}$$

By setting the Area Dose and Beam Current to constant values as for both patterns on sample C401 and C406 the following equation must be fulfilled:

$$100 \frac{\mu C}{cm^2} = 0,0401 \, nA \times \frac{Dwell \, Time}{Step \, Size^2}$$

All patterns on these samples (C401 and C406) fulfil this criterion with their respective *stepsize* and *dwell time* values even if pattern 2 on C406 has completely different values than the other patterns (Table 4.4).

A new sample was printed (C407; Table 4.4) only with pattern 2 and manually setting the Step Size instead of calculating it automatically (the *dwell time* was still automatically calculated) and the pattern was successfully printed to resemble the pattern Figure 4.34 (b) indicating a dependency on the *step size* which should be set to a maximum value of 0.006μ m in future experiments. These are surprising results as both of the step-sizes (0.006μ m and 0.02μ m) are considerably smaller than the smallest contact-diameter in Pattern 1 of 200nm (Figure 4.29 (a)).

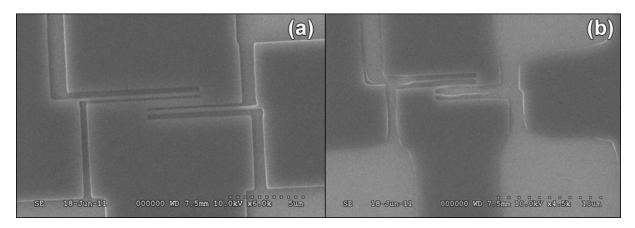


Figure 4.37: (*Scanning electron microscopy; before metallization*) Attained patterns for Pattern 1 (a) and Pattern 2 (b) on sample C406. Pattern 1 employed a step-size of 0.006μ m while Pattern 2 employed a step-size of 0.02μ m.

Finalized parameters:

Several resists have been tried but the best results were attained with the PMMA C4 resist. A resist-thickness of 500nm is recommended in order to get good lift-off with a total of 50nm metal-thickness. It was also found that the ability to successfully lift-off and the degree of resist-bubbling of a Ti + Au deposit strongly depended on the thermal conductivity of the components used in inserting the sample into the E-Beam evaporator for metal deposition. This was not observed for aluminium deposits.

The best results were attained by replacing the standard Si-plate and adhesive carbon tape with a copper-based Cu-plate and Mung II thermal paste; both with higher thermal conductivity.

The following EBL writing-parameters have shown to give best patterns for 500nm of PMMA C4:

- SEM acceleration voltage: 20kV.
- Exposure dose: $\sim 100 \mu C/cm^2$.
- Step size: 0.006 μm.

The development time has currently been set to 20 sec but further investigations are needed on determining a better time in order to attain better structure-continuity after lift-off. If it is desirable to not increase the development time further because of possible overdevelopment, an alternative approach of stirring the sample during development may also be investigated. The smallest distance between the contacts should be set to 400nm for these parameters but may assumedly be reduced if further high-resolution optimization of the parameters is performed.

4.3.4 Alignment of Nanowire Contacts

Positioning of the pattern for *Nanowire Contacts* is a very important process as the contacts must be placed correctly in contact with pre-dispersed nanowires. Samples were pre-written with orientation patterns and test-patterns were written by EBL both with two-point and three-point alignment. The alignment procedures are performed in the EBL software. An origin is defined on the sample and the patterns should ideally be written correctly at a given two-coordinate (u, v) distance from this origin with a correct orientation. The pattern used in this

testing is given in Figure 4.38 (a) has a dimension of $50\mu m$ time $50\mu m$ and is designed to fit perfectly with the squares building up the orientation-pattern in (b).

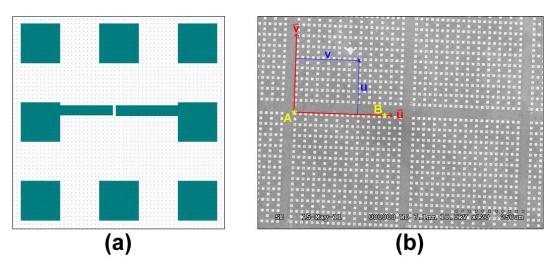


Figure 4.38: The pattern used for this investigation is given in (*a*). The origin of the UV-coordinate system is defined by the chosen Pt. A in the SEM, and the u-direction is determined by an additional Pt. B (*b*).

Two point alignment:

A two-point aligned UV-coordinate system is mainly defined by two parameters in the EBLsoftware, an origin (u=0, v=0; Pt. A in Figure 4.38 (b)) and the direction of the u-axis \vec{u} which is defined by defining a second point (Pt. B in Figure 4.38 (b)).

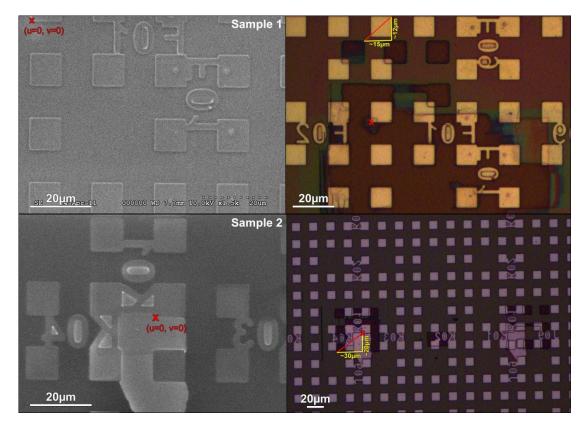


Figure 4.39: Two initial samples were written with the pattern given in Figure 4.38 in a two-alignment procedure. Both of them were supposed to be written with their lower left corner in the red 'X', but the offset was very large and is indicated by red and yellow lines. SEM images to the left, (*before EBL-printing*) and light microscopy images to the right (*after EBL-printing*).

The v-axis \vec{v} will be automatically set to 90[°] on the u-direction. The desired position of the pattern to be written may now be determined by entering the desired UV-coordinate.

Two different samples were printed in order to investigate the usability of two-point alignment (Figure 4.39). The origin of the UV-coordinate system (u=0, v=0) has been defined by a red cross in each sample and the lower left corner of the test pattern should be positioned exactly at this origin. But as shown from the figure this is not the case. The total pattern mismatch is shown as a red line and the u- and v- components of the mismatch are shown as yellow lines. The variations in the mismatch seem to be large and uncontrollable and are not usable for accurate positioning of *Nanowire Contacts*.

A more accurate three-point alignment procedure is therefore needed.

Three-point alignment:

A three-point alignment procedure consists of the previously described two-point alignment (Figure 4.40 (a)) in addition to defining three new points used for alignment (b).

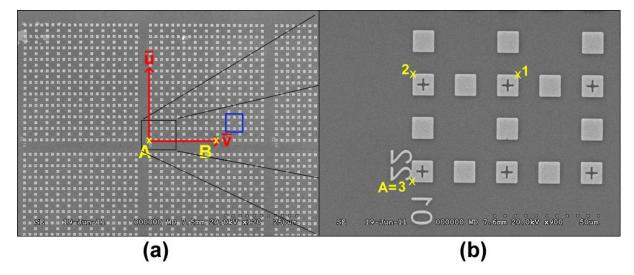


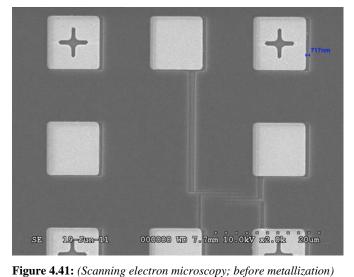
Figure 4.40: A three-point alignment procedure was initiated with a standard two-point alignment procedure (a). The next step was to define three points uniquely for the three-point alignment procedure which scales the pattern given in Figure 4.38 to the correct size (determined by Pt. 1, 2 and 3) (b).

The three added points increases the accuracy of the alignment by defining the size of the pattern onto the sample. Even if the pattern is designed as $50\mu m$ times $50\mu m$ in the UV-coordinate system it still has to be adapted to the XY-coordinate system and scaled to the correct size. The three numbers corresponds to three of the corners in the pattern in Figure 4.38 (a).

A test-pattern was to be written with the final parameters found in Ch. 4.3.3 and placed in the blue square shown in Figure 4.40 (a). The distance from the origin was in this case $u=320\mu m$ and $v=40\mu m$, but because the centre of the pattern is designed to be in $u=25\mu m$ and $v=25\mu m$ (in the design file) as mentioned in Ch. A.2 another 25 μm had to be added to both of the directions, giving $u=345\mu m$ and $v=65\mu m$ for correct placement (Figure 4.41). A small deviation (~717nm) may still be observed in the u-direction which was mainly due to uncontrollable drift-problems of the electron-beam. Three-point alignment seems to be a more accurate alignment method and should therefore be preferred for experiments demanding

accurate placements of the pattern. Some deviations may still be observed in some cases

because of possible drift-issues with the electron beam. This drift has been related to the beam-blanker which is used to blank the beam in order to not expose the sample. It is not recommended to disable the beamblanker for novice users as this would expose everything observed in the SEM and possibly destroying the pattern, and should only be done by experienced users. An alternative is to degauss the beam but it only leads to a minor improvement in some cases.



The accuracy of the placement of the pattern was much higher than for two-point alignment, only with a offset of 717nm in u-direction. This offset was mainly attributed to drift in the SEM electron-gun.

4.3.5 Dispersion of Nanowires

Nanowires tend to lump together when

physically removed from the growth-substrate (Figure 4.42 (a)). In order to improve the probabiblity of finding separate nanowires usable for contacting (Figure 4.42 (b) two methods were employed. The experimental methods are more closely described in Ch. 3.3.5.

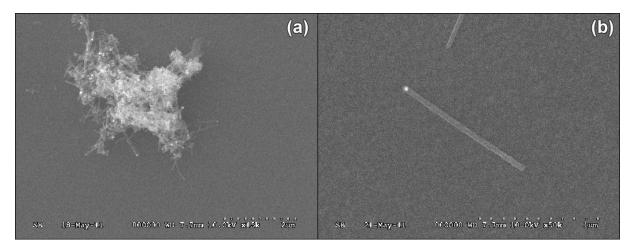


Figure 4.42: Dispersed nanowires mainly collect into big lumps, as shown in (a). Some nanowires could be singled out (b) by a ultrasonic treatment, but lumping was still a widespread phenomenon.

<u>Ultrasound treatment of samples immersed in isopropanol:</u>

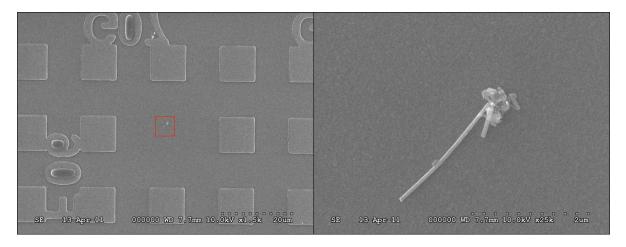
Several samples was put into a sealed beaker with a variable amount of isopropanol and sonicated at variable strength and time. A droplet was transferred from the beaker to the sample and put into a light microscope / scanning electron microscope for observations. None of the immersed samples showed any dispersion of nanowires; no nanowires were found at all. This indicates that the nanowires may be too strongly bound to the growth substrate and cannot be removed by simple treatment in a sonication bath.

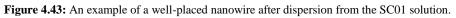
<u>Ultrasound treatment of nanowires scraped of the samples:</u>

By employing a harsher removal method, as scraping with a scalpel, nanowires where successfully removed from the growth substrate and diluted in isopropanol. Nanowires still tend to cluster together because of the forces acting at such small dimensions. An example of a nanowire well-placed for contacting is shown in Figure 4.43.

Possible problems for later contacting-procedures:

- Short nanowire.
- Lumping in one of the ends of the nanowire.





Nanowire length: This is not a very long nanowire ($\sim 2\mu m$), and even if the previous lithographic preparations successfully developed a pattern fitting to a $\sim 2\mu m$ nanowire problems may still arise, mainly because of the drifting-issues observed for the electron-beam during contact alignment (Ch. 4.3.4). Other problems may arise during lift-off because of too closely placed contacts and a contact-separation of at least 400nm should be maintained, but preferably higher. Longer nanowires (> $\sim 3-4\mu m$) should therefore be preferred for contacting.

Lumping: As scraping is a very harsh removal method, the possibility of damaging the nanowire is very high. In this case, the damaged part has collected together in a lump at one side of the nanowire and may create problems for the contacting procedure as one does not know the height and direction of the different components in the lump and could both affect the exposure of the area and/or deposition of either resist or metal. One does also know that it is more difficult to perform lift-off in more crowded areas. A possible solution might have been to make the respective contact larger in diameter so it would cover the whole lump, but this would in this case cover a too large part of the total nanowire length of the already short nanowire.

4.4 Proposal for Final Procedure for Nanowire Contacting

By employing the previous optimizations (Ch. 3.3 and 4.3) a complete procedure for single nanowire contacting may be proposed. Note that a complete structure was not achieved in this project because of time limitations, but enough information has been collected in order to propose a partial contacting procedure.

Step 1: Wafer oxidation and cutting (Figure 4.44).

A 200nm SiO₂-layer is deposited onto the silicon wafer (Ch. 3.3.2) in order to enable backgated electrical measurements. This experiment has deposited the SiO₂-layer by chemical vapour deposition but this can also be performed by thermal oxidation of the wafer if a higher quality oxide is needed. The wafer may then be cut into several smaller samples (Ch. 3.3.3).

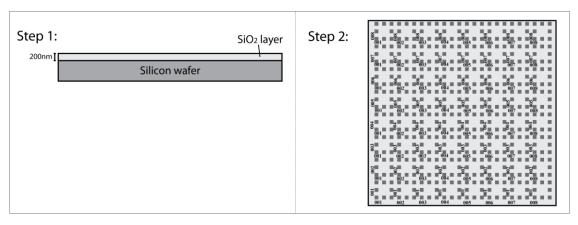


Figure 4.44: (*Step 1*) consists of oxidising the silicon wafer with 200nm of SiO_2 and cutting of the wafer into samples. (*Step 2*) consists of patterning the sample with the neccessary orientation pattern and inner contact-pads.

Step 2: Printing of orientation pattern and inner contact pads (Figure 4.44).

In order to locate and note the position of well-placed nanowires an orientation pattern is needed. This orientation pattern consists of a repeating pattern of the inner-contact pads used for contacting (Ch. 3.3).

The printing of this pattern has been optimized to the following parameters (Ch. 4.3.1):

- Photoresist: Megaposit SPR700 1.0.
- Spin-speed: 6000 RPM @ 45 60sec (~900nm film-thickness).
- Exposure dose: 125mJ/cm^2 .
- Development time: ~3sec.
- Metal deposit: 10nm Ti + 80nm Au (alternatively 90nm Al).

Step 3: Dispersion of silicon nanowires (Figure 4.45).

Removal of silicon nanowires has been shown to be successful by scraping them off the growth-sample with a scalpel (Ch. 3.3.5) into a glass filled with 1-5ml of isopropanol. The glass may then be inserted into an ultrasonic bath and sonicated at medium strength for ~2-5min. A pipette is used to transfer a couple of drops of solution onto the sample surface which is then left to dry in air.

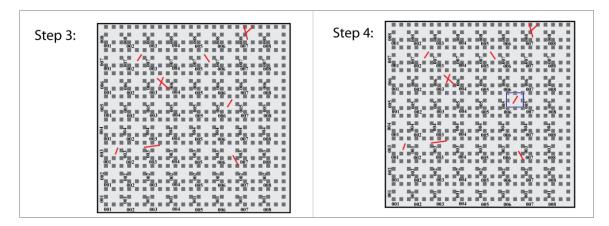
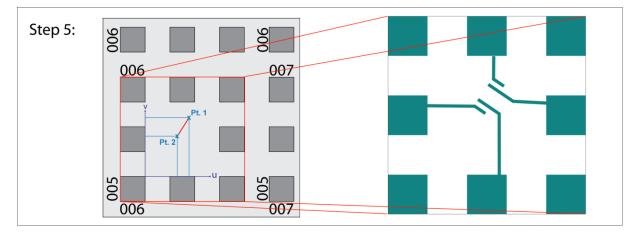
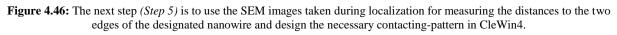


Figure 4.45: (Step 3) consists of dispesing nanowires on the sample while (Step 4) covers the localization of well-placed nanowires.

Step 4: Localization of single well-placed nanowires (Figure 4.45).

Scanning Electron Microscopy (SEM) is employed in order to locate well-placed silicon nanowires. Good SEM images should be taken in order to get a location with high accuracy.





Step 5: Positioning and design of nanowire contact pattern (Figure 4.46).

Positions of the two end-points of the nanowire are noted from high-resolution SEM-images and are used as a basis for designing the printed pattern in CleWin4. The minimum distance between two contacts has been found to ~400nm (Ch. 4.3.3), and further optimizations are needed in order to reduce this distance.

Step 6: Printing of nanowire contact pattern (Figure 4.47).

The nanowire pattern previously designed in CleWin4 is written by Electron Beam Lithography (EBL) with the following parameters (Ch. 3.3.6):

-	Photoresist:	MicroChem 950PMMA C4.
-	Spin-speed:	3000 RPM @ 45 - 60 sec (~500nm film-thickness).
-	SEM Acceleration voltage:	20kV.
-	Exposure dose:	$\sim 100 \mu C/cm^2 @ 20 kV (2000 mJ/cm^2).$
-	Writing step size:	0,006µm

- Development time: ~20sec.
- Metal deposit: 5nm Ti + 45nm Au (alternatively 50nm Al)

A robust three-point alignment procedure has been optimized for correct placement the nanowire contacts relatively to the relevant nanowire (Ch. 4.3.4). This procedure is described in detail in App. A.

Note that in order to reduce bubbling of the resist (Ch. 4.3.3) because of the high temperature needed for deposition titanium it is recommended to use Mung II thermal paste instead of carbon tape and a Cu-plate instead of a Si-plate.

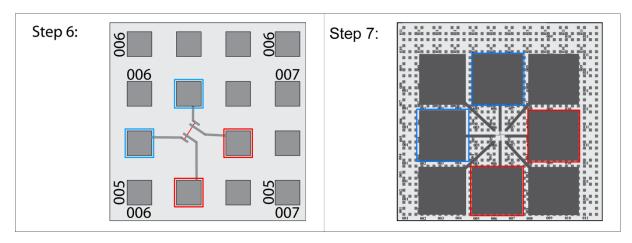


Figure 4.47: The pattern is then written by EBL at the desired writing parameters at the correct location (Step 5). The last step (Step 7) covers the printing of the final outer-contact pads. Corresponding contacts are linked by a color-frame (*red and blue*).

Step 7: Printing of outer contact-pads (Figure 4.47).

The outer contact pads are assumed to be writeable with the same parameters as used for the inner contact-pads (Ch. 4.3.2).

- Photoresist: Megaposit SPR700 1.0.
- Spin-speed: 6000 RPM @ 45 60sec (~900nm film-thickness).
- Exposure dose: 125mJ/cm^2 .
- Development time: ~3sec.
- Metal deposit: 10nm Ti + 80nm Au (alternatively 90nm Al).

Proposal for future electrical measurements (Figure 4.48):

A complete structure has currently not been attained because of time limitations. However, after attaining a complete structure the sample may be used together with a four-point probe system to determine the electrical properties of the sample (Ch. 2.5), as shown in Figure 4.48. The placement of the probes is normally performed by the support of a light microscope because of the small size of the contacts ($250 \times 250 \mu m$).

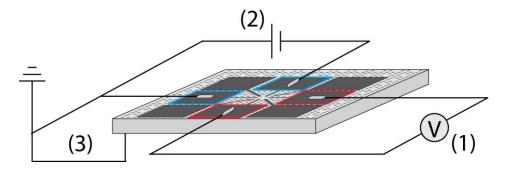


Figure 4.48: Proposed contacting method. The voltage is measured over the inner nanowire contacts by connecting a voltmeter to the respective outer contact-pads (1), see Figure 4.47. The current is sent through the outer nanowire contacts by connecting a current-source to the respective outer contact-pads (2). Back-gated measurements are enabled by onset of a voltage on the back-side of the silicon substrate (3).

The voltage may be measured at the inner nanowire contacts (1; Figure 4.48) by a voltmeter while a steady current is sent through the outer nanowire contacts (2; Figure 4.48). I-V curves may then be found at different gate voltages and the behaviour may be used to determine the effective doping of the nanowires (Ch. 2.5).

5 Conclusion

Al-catalysed nanowires have been successfully grown but unfortunately showed comprehensive stability-problems featuring short (~300 +/- 103nm), tapered and worm-like structures. The instabilities are assumed to be a result of oxidation of both the aluminium catalyst and the silicon substrate because of long preparation-times and repeated exposure to air. Several unsuccessful attempts on reducing oxidation problems with both Sn-based protective coatings and in-situ cleaning (CVD) have been investigated, but have mainly resulted in reduced growth densities. Aluminium is still considered as a good alternative to gold but solutions to the oxidation-problems must be found in order to attain stable growth and to promote aluminium as a viable catalyst for nanowire-based solar cells. Further focus should therefore be given on minimizing the time exposed to air and other oxygen-containing environments during processing. Reduced oxidation may also be attained by employing deposition chambers with ultra-high vacuums (~10⁻⁹Torr). Further research on protective Sn-coatings at longer annealing and growth times, and in-situ cleaning/passivation by the use of gaseous H₂ may also be relevant in order to reduce the amount of oxides.

Because of the instabilities attained for Al-catalysed nanowires, investigations covering the addition of dopant-gases were performed with gold as catalytic material instead. Previous intrinsic growth-conditions were not successfully attained assumedly because of chamber contaminations, but clear effects from adding B₂H₆ and PH₃ to the gas-flows were found nevertheless. Both gases resulted in a continuous reduction in the average nanowire length at increasing dopant ratios, ultimately leading to a complete inhibition of nanowire growth at dopant ratios of $\sim 10^{-3}$ for B₂H₆ and $\sim 10^{-1}$ for PH₃. Both limitations are related to dopantmolecules adsorbing on the catalytic droplets, effectively reducing the number of available adsorption states for SiH₄. A considerable increase in nanowire tapering was observed for increasing B₂H₆/SiH₄ ratios and was found to be a result of radial deposition of a-Si on the nanowire walls during growth. At a B_2H_6/SiH_4 ratio of ~10⁻³ the sample was completely covered in a-Si as a result of the a-Si growth-rate exceeding the one-dimensional growth rate of nanowires, an effect not found for PH₃. B_2H_6 –doped nanowires also seem to prefer a <110>-growth direction instead of the earlier reported <111> direction for intrinsic nanowires. The nanowires are covered in Au-particles both on the top and bottom part which is assumed to come from catalytic droplets. The observed tapering effect may implicate the use of gaseous B_2H_6 as a doping alternative for p-type nanowires as a-Si is assumed to have large implications on the electrical behaviour of nanowires, and alternative dopant-methods such as TMB or post-doping should be investigated. PH₃ on the other hand, seem to be a good alternative for n-type nanowires but an effort should be put on improving the growth rate at higher dopant ratios.

A lithographic method for developing a structure for electrical measurements of silicon nanowires has been proposed. Current optimizations have resulted in a promising Au-based four-point contact-structure, developed by a combination of photolithography and electronbeam lithography. A solid three-point alignment method for aligning the nanowire contacts relatively to single nanowires has also been found. However, some final tuning of the development time and resist-bubbling is needed in order to get a successful lift-off of the four nanowire contacts. Further research may cover combining all the three layers into one single structure and performing some initial resistivity measurements for assessing the quality of the structure. The current SiO₂-layer (CVD) may also need to be replaced with a high quality thermal oxide instead.

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A An Optimized EBL Procedure for Nanowire Contacting

This chapter describes the final optimized Electron-Beam Lithography process used for printing nanowire contacts onto the substrate and is designed to be convenient to follow for the reader. Because of instabilities and proximity issues observed at a SEM acceleration voltage of 10kV (Ch. 4.3.3) the final procedure employs an acceleration voltage of 20kV. This process uses two different types of software simultaneously, the Hitachi S-4300E SEM software and the Raith ELPHY software.

A.1 Sample preparations

The sample has previously gone through the following preparations before this step:

- 1) Oxidized with \sim 200nm of SiO₂.
- 2) Cleaned in acetone and isopropanol.
- 3) Printed with an orientation pattern.
- 4) Dispersed with nanowires.
- 5) A single nanowire has been located on the sample and the position has been noted.
- 6) A GDS-pattern file has been made for the needed contacts to this nanowire.
- 7) Spin-coated with PMMA resist and softbaked.

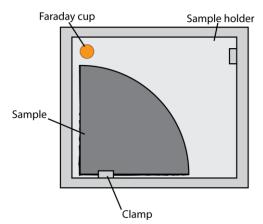


Figure A.1: An illustration of the sample holder and the placement of a sample cut into ¹/₄ of a 2" wafer. The clamps are used to fasten the sample while the Faraday cup is used to measure the beam-current.

The sample (in this case a quarter of a 4" Si-wafer) is inserted into the EBL sample holder (Figure A.1) which is inserted into the Hitachi SEM. The chamber is evacuated and the acceleration voltage is turned on. Remember to check if the blanker is on in order to deflect the beam from not hitting the sample and exposing unwanted areas.

Measuring the current:

In order to get the correct exposure dose the beam current has to be measured. This is done by moving the stage to the Faraday cup by using the preconfigured position in ELPHY (*Stage Control* > *Positions;* Figure A.2). This predefined position centers the beam in the middle of

the faraday cup. Zoom to maximum magnification and measure the beam-current by using the externally current measurement tool. Turn it on, set it to 'pA' and wait for 1-2 min before reading the current. Turn it off and return to the ELPHY software.

A.2 EBL printing

Initial focusing and corrections:

Use the edge of the faraday cup for initial focusing and beam alignment. Beam alignment consists of correcting for beam

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		Faraday Cup Sample spots WF-origo	on holder		<u>E</u> dit				
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Figure A.2: The stage control used for preprogrammed positioning of the stage.

alignment and beam astigmatism, and the necessary tools may be accessed by choosing *Operate* > *Alignment* in the SEM software.

Move the beam to the printed orientation pattern but remember to stay far away from the areas dispersed with nanowires wanted to be contacted. Some more focusing and beam alignment may be required because of the smaller feature sizes and the height difference between the faraday cup and the sample.

Focusing on the resist:

In order to get a correct result the beam must be focused on the resist and not on the structure beneath. This is done by burning a contamination dot on the resist and using it for focusing. Use the *Analyser* toolbar; click on *burn dot* and wait for about 10 sec before stopping the burning process (SEM software). A dot should now appear in the SEM view, as shown in Figure A.3 (a). Try to focus as good as possible on this dot in order to focus on the resist, then burn a new dot to see if the quality of the dot is improved. If the dot instead looks elongated as in Figure A.3 (b) some more astigmatism correction needs to be done. Adjust the astigmatism until the dot is circular and do some focusing. Burn a new dot to see

possible improvement and repeat this procedure as many times as necessary to attain a good circular contamination dot.

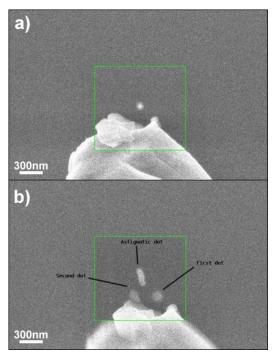


Figure A.3: A correctly burned contamination dot without astigmatism (*a*). An example of a dot burned with non-corrected astigmatism (*b*).

It is important to not change the focus after this step.

Initial coordinate setup:

A coordinate system now needs to be defined. This is done in the vicinity of the relevant nanowire so be very careful when moving the stage around not exposing areas which is not supposed to be exposed. As an example; a nanowire is placed within the green rectangle shown in Figure A.4 and the temporary origin (u=0, v=0) is chosen to be located in point A in the same figure.

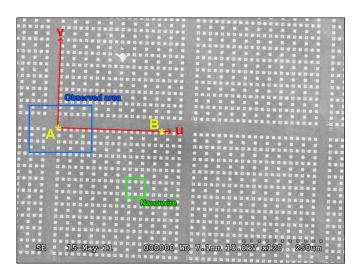


Figure A.4: The UV-coordinate system is set by defining the origin (Pt. A) and the U-axis (Pt. A to Pt. B). In this case the nanowire is located in the green rectangle and in order to not expose resist in its vicinity the *Observation Area* should be small (blue rectangle).

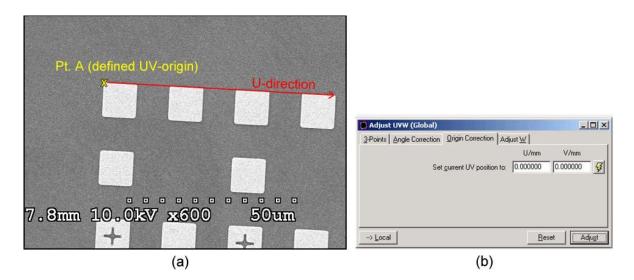


Figure A.5: A closer look on the desired origin point (*a*) (Corresponds to Pt. A in Figure A.4). The origin is set by moving the stage to the desired position and by clicking Adjust in Adjust UVW > Origin Correction (*b*).

Remember to use a magnification so that not the area around the nanowire gets exposed (~5000 X) before moving to the area (ex. blue rectangle in Figure A.4). The origin is defined by moving the stage so that the beam is centered in the upper left corner of the contact (Figure A.5 (a)) and clicking *Adjust* in *Adjust UVW* > *Origin Correction* (Figure A.5 (b)). The UV-Origin is now be set to this position.

The next step is to define the U-direction, and is done via *Adjust UVW* > *Angle Correction* (Figure A.6 (a)). Point 1 is defined in the origin (Pt. A) by clicking Read in Angle Correction. Move the stage to the left (the image moves to the right) and follow the top of the contact-row to the end of the contact-block (point B in Figure A.4) and define point 2 by clicking *Read*. It is important to stay on top of the contact-row (Figure A.5 (a)) in order to get the correct u-direction. Click *Adjust* when both points have been read. Note that the V-direction will automatically be defined as 90°C on the manually defined U-direction.

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3-Points Angle Correction Drigin Correction Adjust W	Name	Mag. + Size/µm		
X/mm Y/mm 1 1 Read 3.687235 24.423876 3 Calculated angle: 0.57*	100 x, 1000.0 μm 500 x, 200.0 μm	100 1000.000 500 200.000		
2 Pa Read 13.687235 24.523876 3	1000 x, 50.0 μm 2000 x, 50.0 μm 4000 x, 25.0 μm 100000 x, 1.0 μm	1000 50.000 2000 50.000 4000 25.000 100000 1.000		
> Local				
(a)	(b)			

Figure A.6: The U-direction is defined by two points in XY-coordinates (*a*) (Pt. A and Pt. B). The write-field is set to the desired magnification and size; in this case 1000X and 50μ m respectively (*b*).

Write-field alignment:

The next step is to perform a write-field alignment procedure. In this case a write field of 50µm at a magnification of 1000X is used since each contact-area is defined as 50 x 50 µm (Ch. 3.3.1). Move the stage so that the beam is centered in one of the crosses in the orientation pattern and zoom in for correct placement of the beam (ex. the lower left in Figure A.5 (a)). Go to *Microscope Control* in the ELPHY software and right click on the *1000X*, *50µm* write-field and click *Set* as shown in Figure A.6 (b). The SEM will now readjust itself to these parameters. In order to align the write-field, go to Scan Manager and select *Align Write Field Procedures* > *Manual*, right click on one of the predefined procedures and choose *Scan Properties* from the menu (Figure A.7 (a)).

Scan properties		Scan properties
Name: 100 um WF	F · Manual ALW/F 5 um marks	Name: 100 um WF - Manual ALWF 5 um marks
Main Mark proc Scan description Field size: Main direction: Scan size: Step size: No of points: Point average: Aright Average: Average count:	redue Advanced Post Processing 100.000 µm C U S 0000 µm 0.0100 µm 0.0100 µm 0.0100 µm 0.0100 µm 0.0100 µm 0.0100 µm 1 Soo 1 1	Main Mark procedure Advanced Post Processing Align WF procedure Iterations: Iterations: Mark sequence: Iterations: Iterations: U V Placement: 30.000 µm 30.000 µm Click for automatic mode
	Cancel OK	Cancel (b)

Figure A.7: The scan properties are set by manually choosing the desired *Scan size* and automatically calculating the *Step size* (*a*). Note that the *No. of points* and *point average* must be set to 512 and 16 respectively. The placement of the write-field during alignment may be done automatically (*b*).

Two parameters under *Main* must be set to a value constant for all scanning procedures:

- No. of points: 512
- Point average: 16

The *Placement* field under the *Mark procedure* tab (Figure A.7 (b)) is set to automatic mode by clicking the X-like button to the right of the U-box.

There are only two fields to change between every write-field alignment procedure; *scan size* and *step size*. Scan size is manually set while the step size is calculated automatically after entering a value for scan size by clicking the calculator to the right of the field.

The first alignment method uses *a scan size* half of the write-field, in this case a value of 25μ m is entered. Click the calculator to the right of the *Step size* in order to calculate the value automatically and confirm by clicking *OK*.

Right click on the edited write-field procedure and click *Enter*. The alignment procedure will now run and scan an image. After completion of the image-scan the software will ask for the user to place the center of the blue cross in the middle of the chosen point for write-field alignment (in this case in the middle of the pattern-cross).

- Click and hold the CTRL button.
- Click and hold the left mouse button simultaneously as the CTRL button.

- Move the blue cursor into the middle off the chosen pattern-cross.
- Release the left mouse button.
- Release the CTRL button.

A new alignment-point has now been made, and the user can proceed by clicking *Continue* in the *Macro execution paused*... box. This has to be done two more times for each write-field procedure; a total of three times.

The same write-field procedure should be repeated for two more runs (with reduced scan size). Edit the scan-size and step size for the same procedure used previous. The first run should be done with a scan-size of $15\mu m$ and the last one with a scan-size of $10\mu m$.

A total of three write-field alignment runs should now have been performed:

- 1) Scan size: 25µm.
- 2) Scan size: 15µm.
- 3) Scan size: 10µm.

3-point alignment:

In order to get an accurate placement of the contacts a 3-point alignment must be done. This requires the design file to be loaded into the ELPHY software and is done by going to the *Design Manager* and loading the respective design file. Right click on the respective pattern in *GDSII Database* and open in in *GDSII Editor*.

Define three marks by using the flags in the Toolbox as shown in Figure A.8 (a). In this case the marks are defined as following:

- 1) u = 50.0, v = 50.0
- 2) u = 0.0, v = 50.0
- 3) u = 0.0, v = 0.0

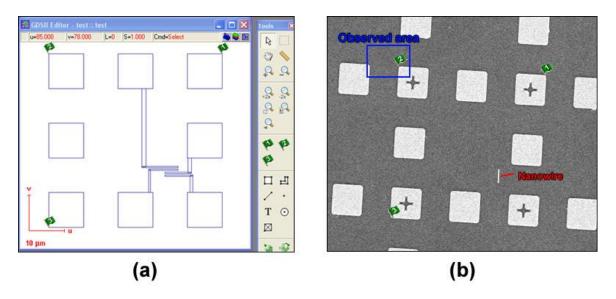


Figure A.8: In order to get the correct aspect ratio of the design onto the pattern three points are defined both in the designed pattern (a) and on the substrate (b). Note that if this is done in the vicinity of the nanowire contact area a very small observation area should be used (high magnification; (b)).

After these marks have been put onto the design, they also have to be defined on the actual structure as shown in Figure A.8 (b). Move the beam carefully towards the area of the nanowire, and when closing in zoom in to a magnification level small enough to not expose too much of the surrounding area (ex. \sim 8000X – 10000X as shown as the blue rectangle in Figure A.8 (b)).

Center the beam in the upper left corner of the contact where flag 2 is going to be located (see Figure A.8 (b)) and open the *Adjust UV* > *3-Points* window (Figure A.9 (a)). The three UV-points may here be defined in the XY-coordinate system used by the sample holder in order to orientate on the sample.

		(a)		12					(b)	
_→ <u>L</u> ocal				<u>R</u> eset	Adju	u <u>s</u> t		<u></u>	ear	<u>S</u> tart
E 3 🕅 Read	0.000000	0.000000	3 0.0000	000 0.001	0000	Ş		w j	mm	Position absolute relative
	0.000000	0.000000	 0.0000			G		U: V:	mm mm	© UVW C XYZT
□1 👖 Read	0.000000	0.000000	3 0.0000	000 0.00	0000	\$	STOP		Destination	Base
	X/mm	Y/mm	U/i	mm V	//mm		🚟 Stage C			
3-Points Angle C	correction 0	gin Correction	1							
🖲 Adjust UV (Glo	obal)									

Figure A.9: A three-point alignment is performed by defining the XY-coordinates of the three points in an UV coordinate system (*a*). During this procedure the stage should not be moved manually but rather automatically by entering the desired coordinates in the *Stage Control* window (*b*).

Use the following procedure to define the points on the sample.

- 1) As the beam already is centered in the position for Flag 2, click the Flag 2 button the *3-Points* view. In necessary, correct the U and V value to u = 0.0 and v = 50.0.
- 2) Click on *Read* next to the Flag 2 button to read the relevant X/Y position.
 (Do not manually move the stage before reading the XY coordinate in order to correct the position to the corner of the relevant contact, this will be corrected in a later step).
- 3) Check the checkbox to the left of the Flag 2 button.
- 4) *Put the blanker on.* Use the *Stage Control* (Figure A.9 (b)) to move the stage to where Flag 3 is going to be. This is done by entering u = 0, v = -50.0, checking *Base > UVW*, checking *Position > Relative* and clicking *Start*.
- 5) Turn the blanker off. Click on the Flag 3 button in the *3-Points* tab and adjust the value to u = 0.0 and v = 0.0 if necessary.
- 6) Click *Read* next to the Flag 3 button to read the relevant X/Y position. (*Do not manually move the stage before reading the XY coordinate*).

- 7) Check the checkbox to the left of the Flag 3 button.
- 8) *Put the blanker on.* Use the Stage Control (Figure A.9 (b)) to move the stage to the where Flag 1 is going to be. This is done by entering u = 50.0, v = 50.0, checking *Base* > *UVW*, checking *Position* > *Relative* and clicking *Start*.
- 9) Turn the blanker off. Click on the Flag 1 button in the *3-Points* tab and adjust the value to u = 50.0 and v = 0.0 if necessary.
- 10) Click *Read* next to the Flag 1 button to read the relevant X/Y position. (*Do not manually move the stage before reading the XY coordinate*).
- 11) Check the checkbox to the left of the Flag 1 button.
- 12) Click Adjust.

The 3-points are now defined, but some corrections still have to be performed.

Adjusting the UV-points:

Make sure the blanker is on. The UV-points defined in the 3-point alignment still have to be tuned. In the *Scan Manager* click *Adjust UV Procedures* > *Manual* and right click on one of the predefined procedures. Enable and write the correct UV-coordinates for each of the three alignment points as given above. Set the *scan size* to $10\mu m$ and click *OK*. Right click on the procedure and click *Scan*. A scan similar to the one for write-field alignment will now be performed, but holding down the CTRL simultaneously with the left mouse button will now be used to tune the three alignment-points instead. The procedure is identical as for write-field alignment and will not be further explained. Run this procedure also for $5\mu m$ and $2\mu m$ by editing the procedure and clicking *Scan*.

Final write-field alignment:

Make sure the blanker is on. A final writefield alignment has to be performed. Go to the origin by using the *Stage Control* (u = 0, v = 0). Remember to check the *UVW* and Absolute checkboxes. Use the same writefield procedure as before, but start at 10µm scan size and reduce to $5\mu m$ and $2\mu m$. Remember, this write-field alignment is performed in the origin and not by moving the stage manually to a pattern-cross. The write-field is then aligned according to the bottom and left edge of the contact defining the origin. Moving the stage manually will destroy earlier alignment procedures and one has to start all over. Alternatively one may move the stage to a pattern-cross farther

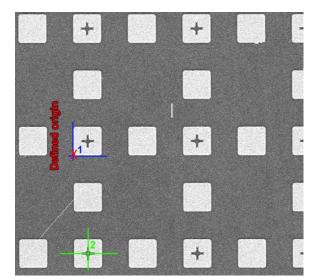


Figure A.10: Final write-field alignment is performed at a feature with clear edges, either at a corner (1) or in a cross (2).

away from the relevant nanowire contacts by using the *Stage Control*. In this case the write-field is aligned according to the center of the pattern-cross as before.

Both of the write-field possibilities are summarized in Figure A.10. Possibility 1 is performed in the defined origin, by using the blue lines as alignment-lines.

The other possibility (Possibility 2) is to move the stage by *Stage Control*. By knowing that the contacts are $10\mu m \times 10\mu m$ and separated by the same values the needed values for the *Scan Control* may be calculated. In this case the pattern-cross is $5\mu m$ in positive u-direction of the origin and $35\mu m$ in negative v-direction. By filling out these u and v values in the *Stage Control* and checking the *UVW* and *Absolute* checkboxes one should place the beam in the respective pattern-cross.

After performing this alignment procedure with $10\mu m$, $5\mu m$ and $2\mu m$ scan-sizes one can move on to the exposure of the sample.

(Note that one may have to perform the final UV-point alignment and write-field alignment several times before getting the best result. Use the Stage Control to move to u = 0 and v = 0and check for deviations from the desired origin. If there is a deviation a new set of UV and write-field alignments should be performed. Do this until the deviation is negligible. Remember to do this at increased magnification at ~8000X in order not to unnecessary expose resist.)

Exposure:

Open up a new *Position List* from the *File* menu. Drag the pattern from the *GDSII Database* to the *Position List*. Right click on the pattern in the position list and click *Properties*.

Verify that the *Working Area* is set from 0 - 50 μ m in both directions. In this case, set the *Position* to $u = v = 25\mu$ m. Choose the layers wanted to print, in this case only Layer 0 is available and chosen.

(Note that the extra $25\mu m$ added to the u and v coordinates is a result from how the design was made. When the example pattern (Figure A.8) was designed in CleWin it was designed with the lower left corner of the pattern in the software-origin (CleWin4). The middle of the pattern will therefore be located at $u=v=25\mu m$ since the pattern have a size of $50 \times 50\mu m$. However, the EBL-software uses the middle of the pattern when placing the pattern on the sample which in this case will result in a displacement of $25\mu m$ in both directions. The solution to this will be to design the pattern with the middle of the pattern in the origin of CleWin4.)

Click *Calculator* in order to set exposure parameters, and set the following parameters:

- Enter the *Beam Current* as read in the beginning of the EBL procedure.
- Check *Equal steps* in the *Area tab* and set the step-sizes to the desired value.
- In the same tab, define the desired *Area dose*.
- Automatically calculate the *Area Dwell Time*.
- Do exactly the same under the *Line* and *Curved Elements* tabs.
- Click OK.

Right click on the relevant pattern in the *Position List* and click *Scan*. The pattern will now be scanned.

<u>Remove the sample:</u>

When the scanning is complete, turn off the acceleration voltage, move the sample holder to the exchange position by using the predefined position in Stage *Control* > *Position*. Unload the sample into the load-lock, vent the load-lock and remove the sample.

The sample is now ready for development. The resulting pattern after development by using the PMMA C4 resist is located in Figure 4.41.

B 950PMMA and Copolymer Spin-Curves

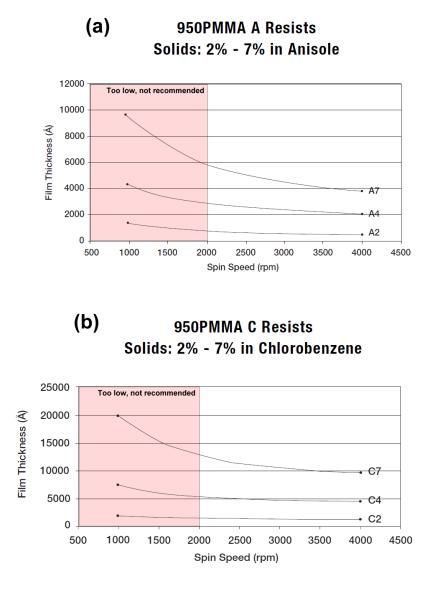
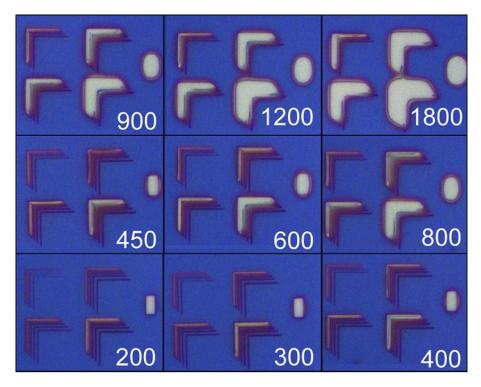
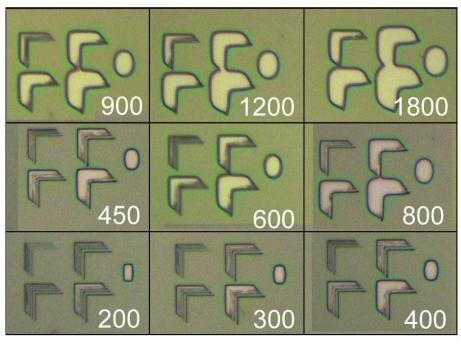


Figure B.1: Spin-curves for 950PMMA A (a) and C (b) resists.

C Dosage-check for PMMA A4 and PMMA 7



(a) PMMA A4



(b) PMMA A7

Figure C.1: Initial dosage-comparison for the PMMA A4 (*a*) and PMMA A7 (*b*) resists. The numbers indicate the dosage in μ C/cm².

D Dosage-Matrix for PMMA A2 and PMMA A4

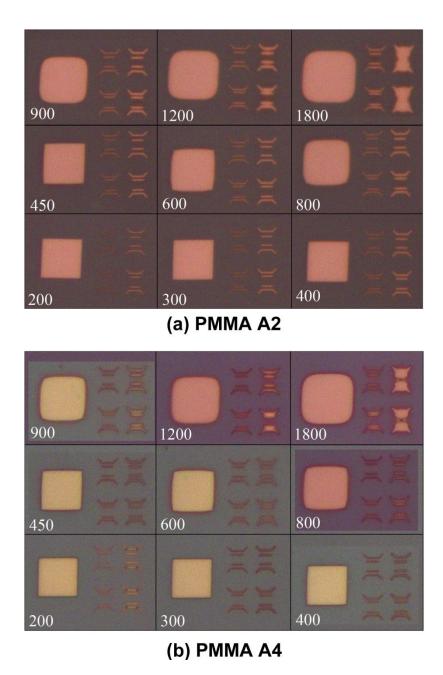


Figure D.1: Initial dosage-comparison for the PMMA A2 (*a*) and PMMA A4 (*b*) resists. The numbers indicate the dosage in μ C/cm².

E Exposure-dose investigation for PMMA A4

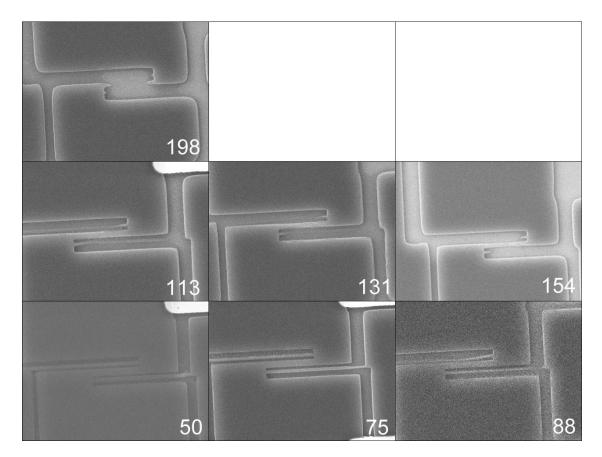


Figure E.1: Closer investigations on the dosage for the PMMA A4 resist, performed by Scanning Electron Microscopy. The numbers indicate the dosage in μ C/cm².

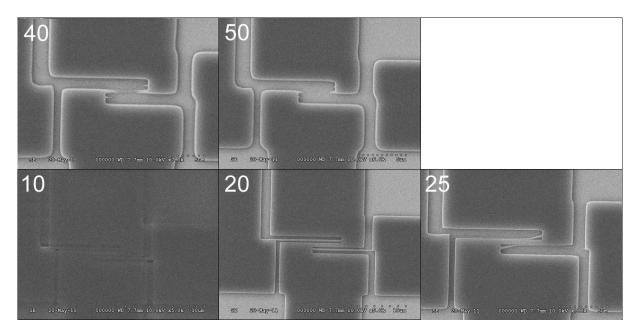


Figure E.2: Narrowing of the dosage-interval for further investigations of the PMMA A4 resist. The numbers indicate the dosage in μ C/cm².

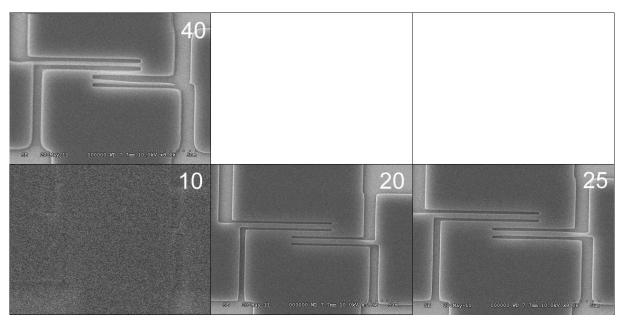


Figure E.3: Further narrowing of the dosage-interval for further investigations of the PMMA A4 resist. The numbers indicate the dosage in μ C/cm².

F Initial dosage-testing for PMMA C4

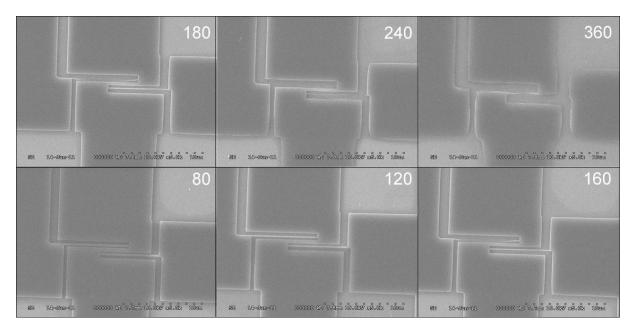


Figure F.1: Initial dosage test for the PMMA C4 resist (Pattern 1). The numbers indicate the dosage in μ C/cm².

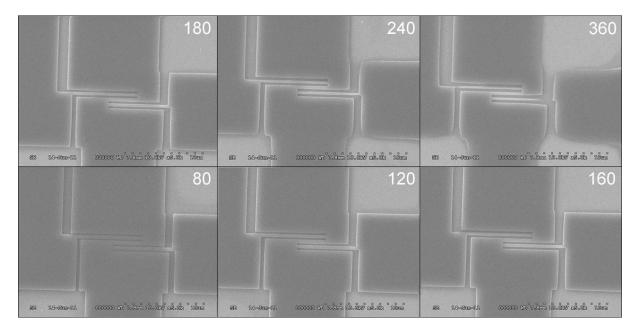


Figure F.2: Initial dosage test for the PMMA C4 resist (Pattern 2). The numbers indicate the dosage in μ C/cm².

G Earlier attained nanowire morphologies

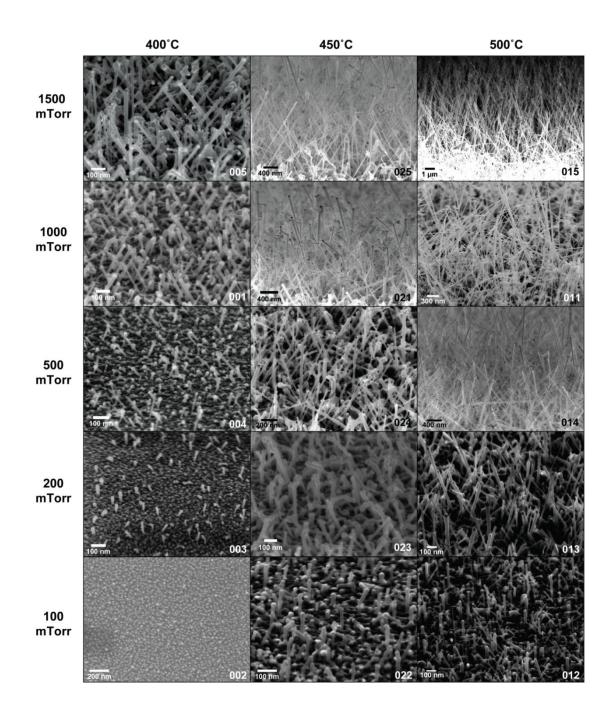


Figure G.1: Nanowires attained at different growth-temperatures and SiH₄ partial pressures in previous experiments⁽²⁾.