Experimental Study on Fast-Switching Series-Connected SiC MOSFETs

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Abstract

This paper presents an experimental study on series-connection of Silicon Carbide MOSFETs. The switching performance of two series-connected SiC MOSFETs rated at 1200 V and having on-state resistances of 80 mΩ was tested using a double-pulse test circuit at blocking voltages up to 1 kV DC and currents up to 50 A. The design and experimental validation of a suitable double-pulse test setup and gate drive circuits are also shown. Moreover, the impact of additional DRC snubbers ensuring an equal voltage sharing among the series-connected transistors is also investigated.

Introduction

After the successful introduction of 1200-V class Silicon Carbide (SiC) power semiconductor devices, the next step from the manufacturers is to expand the blocking voltage capabilities towards higher voltage levels. Indeed, SiC power transistors and diodes with blocking voltages exceeding 10 kV have been recently demonstrated [1]-[3], not only with respect to the device structures and characteristics, but also in terms of operating in power electronics converters [4],[5]. The high voltage (HV) SiC power devices can be found beneficial in a variety of power electronic applications, such as transmission and distribution systems, large motor drives, pulsed-power systems and electrification of subsea operations [6]. In particular, HV SiC power semiconductors will enable significantly higher efficiencies when employed in high-power electronic converters for HV direct current (HVDC) transmission systems. The modular multilevel converter counts as an example, where efficiencies well-above 99.8% are expected using HV SiC junction-field-effect transistors (JFETs) [7]. The expansion of distributed electric power generation, either onshore or offshore, has resulted in the investigation of more flexible and efficient medium voltage (MV) distribution grids [8]. MVDC distribution grids are also expected to electrify on-board and subsea loads in medium and large-scale vessels [9]-[10]. The heart of MVDC distribution grids is high-power and MV power electronic converters. MV power electronic converters, such as solid-state transformers, will play a crucial role in the future DC grids and especially in the establishment of MVDC distribution grids. If SiC power semiconductors are employed in such systems, several advantages over the state-of-the-art Silicon counterparts can be itemized. Apart from the lower power

losses, higher operating temperatures and higher power densities [11], SiC technology enables higher blocking voltages per single chip than state-of-the-art Silicon devices. This is associated with lower number of series-connected SiC power devices in order to meet the blocking voltage requirements, and thus facilitates a lower circuit complexity. A great impact on system performance of high-power MV traction converters or MV DC collector grids in wind or PV farms is also anticipated by utilizing SiC technology. This impact of HV SiC device is expected to be even more significant than the potential gains of SiC in the LV application areas. Regardless of the advantageous expected performance of HV SiC power devices, there are still a few remaining challenges that must be properly addressed. Weak parameters of new devices (e.g. high voltage drop), lack of suitable gate drivers that enable fast switching and HV isolation and circuit layouts designs with sufficient HV isolation are listed as crucial challenges when employing HV SiC power devices [1]. Moreover, the cost of new technology may be predicted to be considerably large. Last, but not least, the current ratings of the available HV SiC power devices are not sufficiently high in order to build high-power converters. A solution to these issues is the series connection of low voltage (1200 V or 1700 V) SiC transistors in order to design high-voltage power switches [12]-[16]. The first expected advantage may be the low cost of LV SiC transistors, which have experienced a serious price drop during the last years [17]. Furthermore, it is very likely that the on-state voltage drop of the series connected LV SiC transistors will be lower than in high-voltage device with similar chip size (i.e. similar current ratings) [16].

In this paper series-connection of 1200-V class SiC MOSFETs is presented under the assumption that the gate resistors, switching speeds and, finally, switching energies per transistors should be kept on the same level as for the LV designs. Double pulse test circuit and gate driver have been designed in order to experimentally validate the performance of two 1200-V series-connected transistors at a blocking voltage up to 1 kV. It is shown, that mismatches in the MOSFETs parameters and gate drive circuits can count as a serious design problem and additional snubber circuits have to be employed.

Main challenges of series-connected SiC MOSFETs

The electrical and thermal performances of series-connected SiC MOSFETs are not trivial, but several issues arise which must be properly solved. These issues are related either to the design of the power or gate drive circuits or to the parameters of the power semiconductor devices.

Variations in stray inductances between the series-connected SiC MOSFETs contribute to the uneven distribution of the transient blocking voltages. Therefore, the power circuit layout must be designed in a symmetrical way by considering equal stray inductances between the devices. On top of this, the design of the gate drive circuit is also very challenging. In particular, a sufficient HV isolation between the gate driver supplies for the individual series-connected SiC MOSFETs must be ensured. This can be feasible by supplying the individual gate drive circuits using high frequency transformers (T/F) with a sufficient HV isolation. However, as shown in [16], designing such a T/F results in increasing leakage inductances which also influence the switching performance of the MOSFETs. Possible variations in the leakage inductances might cause mismatches in the switching speeds of the individual series-connected MOSFETs. In addition to this, short propagation delays among the individual drivers might significantly influence the switching process of the series-connected SiC devices (expected switching times <50 ns). Nevertheless, in Silicon IGBTs such a challenge is usually of minor interest due to the longer anticipated switching times (~600 ns) [17].

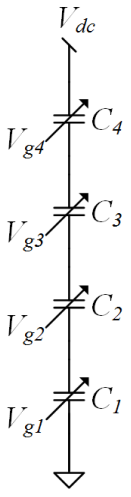


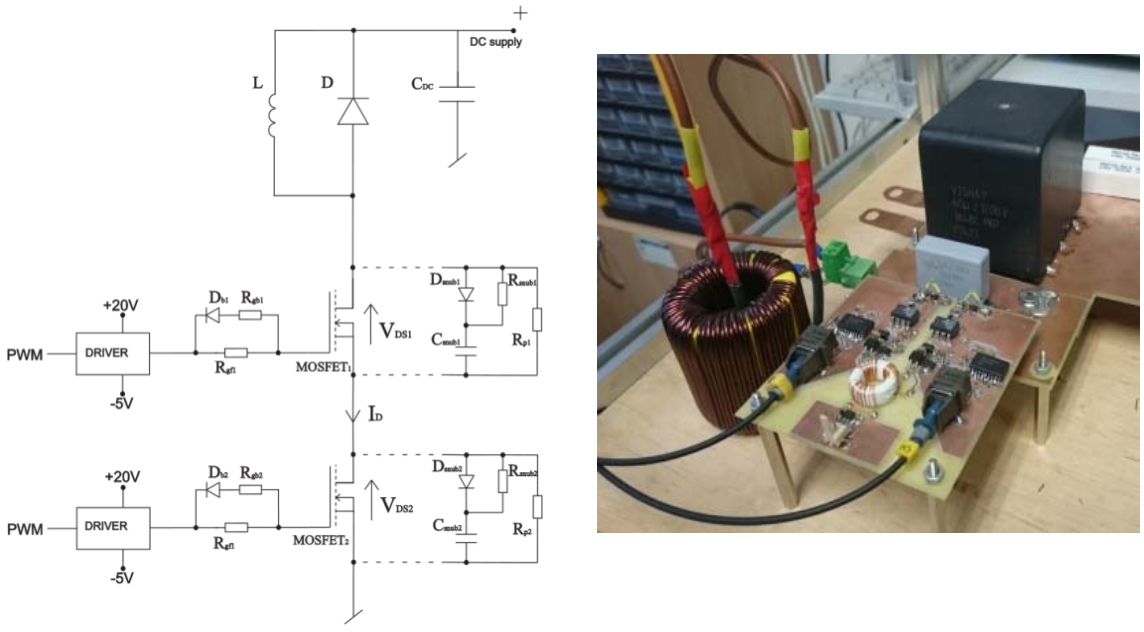
Fig. 1: Series-connected transistors modeled as voltage-controlled capacitors.

Last but not least, the potential spread in the device parameters should also be considered. More specifically, blocking voltage mismatches may be anticipated due to variations in the input capacitance (i.e. stray capacitance) of the series-connected transistors.

The individual series-connected MOSFETs can be modeled as series-connected voltage-controlled capacitors (corresponding to the individual input capacitances), as shown in Fig. 1. By assuming that the individual drive circuits operate with exactly the same switching speed and propagation delays, it is clear that during the switching process the highest *dV/dt* will be observed for the SiC MOSFET having the lowest input capacitance. Hence, this specific transistor will turn-off faster compared to the rest of series-connected devices. However, there is a more severe problem anticipated in such a situation. The turn-off process of the current, which flows through the series-connected transistors, completely depends on the stray capacitance that is fully charged first. The most crucial question here is associated with the blocking voltage of this specific transistor. Assuming that the rest of the series-connected transistors might not be fully turned-off (fully charged stray capacitances) at this time point, the blocking voltages across them will be significantly lower than the blocking voltage appears across the first-turned-off transistor.

Test setup & gate drivers

All tests presented in this paper were performed according to the double pulse procedure, which is usually applied to verify the switching performance of power devices. The test setup (Fig. 2) was designed to experimentally investigate the switching performance of two series-connected SiC MOSFETs. That circuit layout would simulate the process of current switching between the diode and the MOSFETs in order to test its dynamic parameters. High voltage capacitor (60 µF/1200 V) served as DC-link for the PCB with the semiconductor devices (SiC MOSFETs: 2xC2M0080120D and SiC Schottky: C3D25170H). Additionally, an inductor (100 µH/80 A) was applied between the middle point and the positive supply pole. Moreover, special discharging circuit with resistors and a controlled IGBT was also added to speed up the energy dissipation from the main DC capacitor. Additional, fast capacitors (1 µF/1000 V) were also connected across the TO-247 devices in order to improve the switching performance. The designed circuit is also suitable to employ snubber circuits in parallel to SiC MOSFETs, as marked in Fig. 2a. The PCB of the power circuit was designed taking into account the influence of the parasitic inductances. In particular, the design target was to minimize the stray inductances and to keep a symmetry on the power circuit layout between the series-connected transistors. Finally, the test circuit is able to operate at 1 kV DC/80 A. The signals for the MOSFET gate driver and the discharging circuit were provided by a special-designed control PCB with a microcontroller and opto-transmitters. Table I summarizes the parameters of the test circuit.



(a) (b)

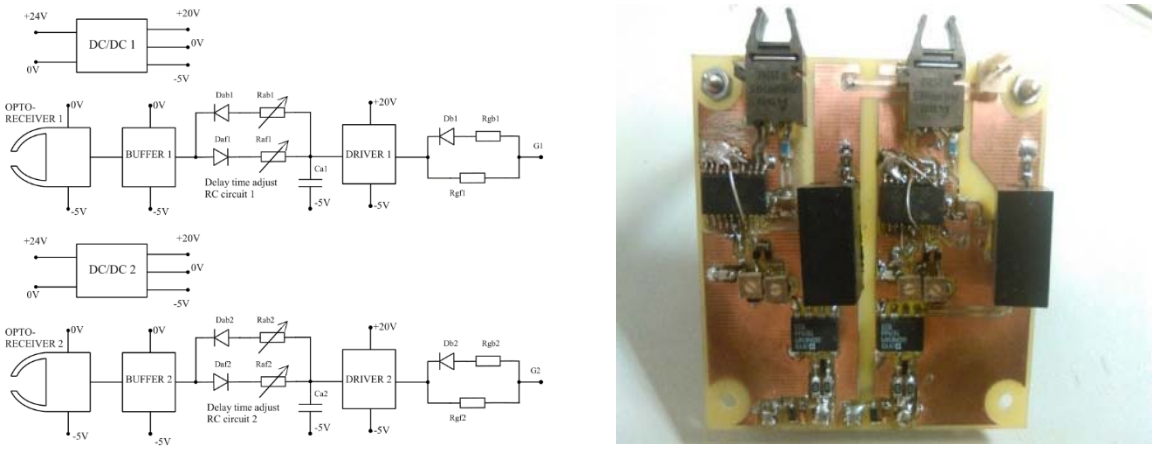
Fig. 2: Schematic diagram (a) and photo (b) of the double-pulse circuit with two series-connected SiC MOSFETs

Table I Parameters of the test circuit

Element	Manufacturer	Part No	Parameters
SiC MOSFETs	Wolfspeed	C2M0080120D	1200V/36A
SiC Schottky	Wolfspeed	C3D25170H	1700V/26A
DC-link Capacitor	Vishay	MKP1848C66012JY5	1200V/60μF
Fast Capacitor	WIMA	FKP1O141007K	1000V/1μF
Inductor	Feryster	-	80A/100μH

Gate driver with adjustable delays

A schematic diagram of the first version of the gate driver is shown in Fig. 3a. It contains a special RC circuit that is connected between the opto-receiver and the power stage of the driver (IXDD614) in order to adjust the delays in the control circuits. Both the upper and lower drivers were supplied by Murata MGJ2D242005SC isolated DC/DC converters. A picture of the gate driver with adjustable delays prototype is shown in Fig. 3b.

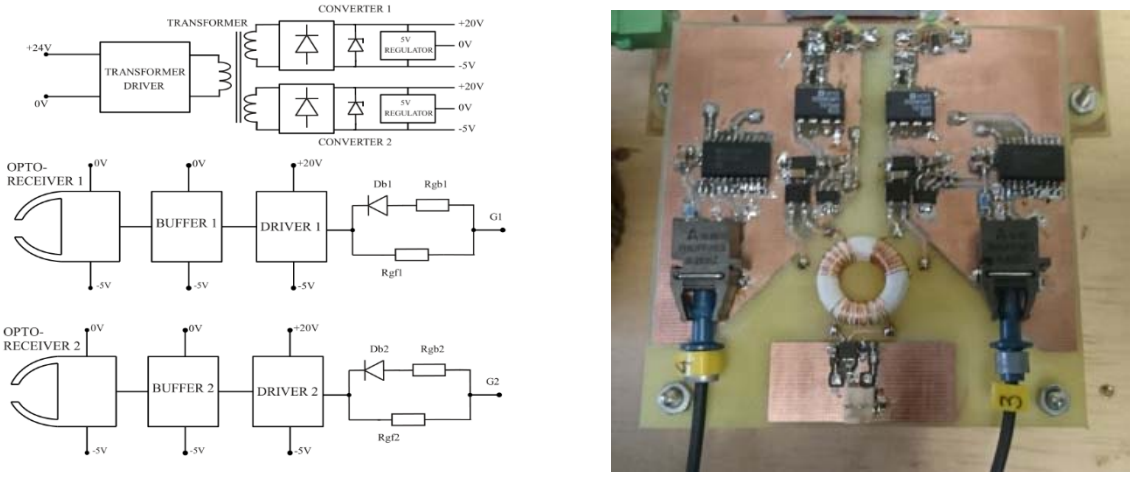


(a) (b)

Fig. 3: Schematic diagram (a) and photo (b) of the gate driver with adjustable delays

Gate driver with reduced inter-winding capacitance

The second version of the driver was designed without using any special RC circuits, but it was supplied from a special isolated DC/DC converter. In particular, the power to the gate driver is provided through a HV isolation T/F as shown in the schematic diagram in Fig. 4a. The HV isolation T/F is supplied by a high-frequency square waveform (supplied by MAX13256) on the primary winding and supplies two floating rectified voltages across the two secondary windings. It must be noted that the inter-winding capacitance of the transformer is approximately 4 nF. A photo of the lab prototype of the second gate driver concept is shown in Fig. 4b.



(a) (b)

Fig. 4: Schematic diagram (a) and photo (b) of the gate driver with reduced inter-winding capacitance

Power consumption of the gate driver during continuous operation

The second version of the driver was tested in order to analyze the power consumption with a continuous PWM operation and in a state without any control signal. In order to measure the current, a precise ammeter was connected between the 24 V DC power supply and the driver. The range of the pulse frequency during the experiment was changed starting at 1 kHz up to 50 kHz, which resulted in a driver current fluctuating between 85 mA and 105 mA. Thus, the anticipated power consumption was varying from 2.15 W up to 2.5 W, as illustrated in Fig. 5. It reveals that the majority of the power consumption is due to the steady-state losses, which are found to be slightly above 1 W per driver channel (loss in the DC/DC converter and linear regulators). Frequency-dependent losses caused by recharging of the MOSFETs gates are rather on the low level due to the low values of the gate charge. The test also included heat measurement of the PCB and its components throughout the whole process with a maximum point temperature never exceeding 75°C.

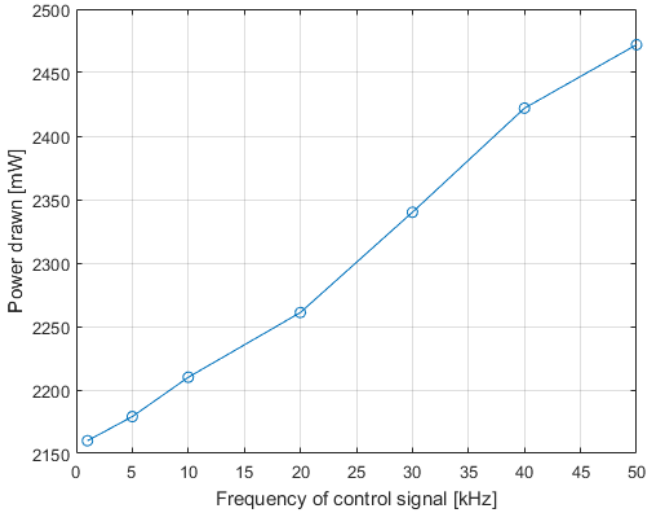
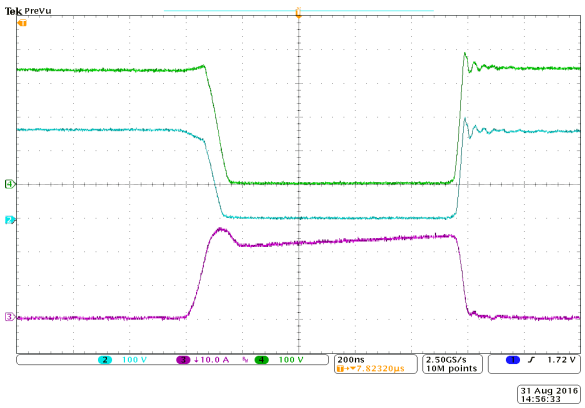


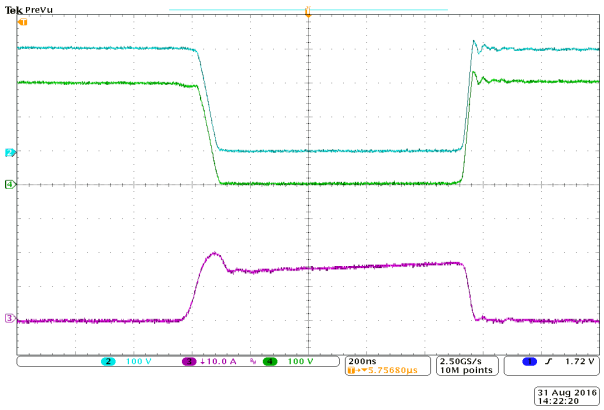
Fig. 5: Power drawn by the drivers from 24 V DC supply as a function of the control signal frequency.

Experiments with adjustable delays

In the next step, a gate driver with adjustable delays has been applied to control two series-connected SiC MOSFETs under the double-pulse procedure. In the first test, with the RC circuit bypassed, a serious mismatch in the drain-source voltage level was observed due to the differences in the device parameters of SiC MOSFETs and in drive circuit parameters – see Fig. 6a. The difference between the drain-source voltages in the steady-state is around 80 V (test performed at 600 V DC voltage). For the second experiment, the additional RC circuits were included between the opto-receiver and gate driver in order to adjust the delay times. After the modification of the gate driver delays almost ideal voltage sharing between the two transistors could be observed (Fig. 6b). The performed test shows the importance of the time delays in the control circuitry when fast SiC MOSFETs are connected in series. However, the time tuning requires manual changes in the gate driver circuit and is problematic in practice, especially with more than two series-connected SiC MOSFETs.



(a)



(b)

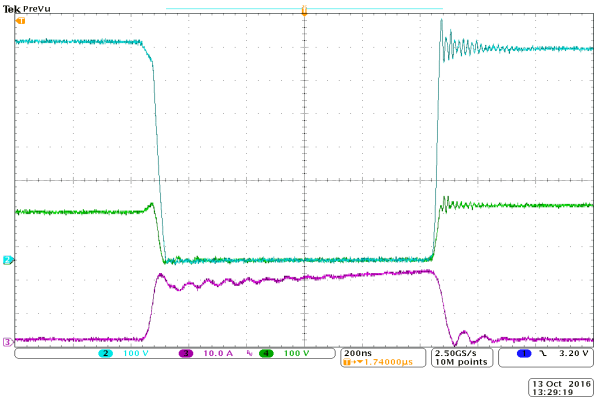
Fig. 6: Oscillograms showing the switching performance of the two series-connected SiC MOSFETs: without RC circuits (a) with tuned RC circuit (b) - from the top drain-source voltage of the upper and lower transistor (100 V/div) and drain current (10 A/div), time scale 200 ns/div.

Experiments with a snubber circuit

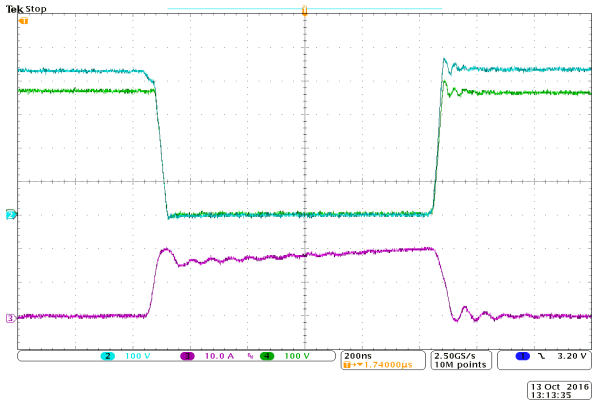
An adjustment of the gate drivers time delays is a solution, which should not be considered in practice. Therefore, some additional efforts are required to balance the voltage sharing. A solution where an additional snubber circuit is connected to each transistor seems to be more realistic. The idea was presented in [19]-[20] for IGBTs and also investigated for SiC MOSFETs in [13]-[15]. Those DRC circuits (Fig. 2) would equalize the drain-source voltages between the MOSFETs and minimize the influence of different switching times by means of additional parallel capacitance, exceeding the output capacitance of the devices. Obviously, this comes at the price of additional energy losses in snubbers,

but due to the voltage balancing effects on turn-on and turn-off switching process, the outcome is positive and total losses are reduced.

Fig. 7 shows a comparison of the switching processes obtained with the second version of the gate driver (Fig. 4) without and with an additional snubber circuit (diode UF4007, Rp=50 kΩ, Rs=10 Ω, Cs=680 pF) performed at 800 V DC voltage. It can be seen that without the snubber, voltage mismatches achieve critical values and cause a situation, where only one MOSFET blocks most of the voltage. This behavior is caused by devices and control circuit mismatches, which become important when devices are switched in tens of nanoseconds. Such a behavior may end up with one transistor overheating or even being destroyed due to parameters surpassing the transistor nominal values. The difference in switching energies, determined in Fig. 8a, is severe - the top MOSFET takes around 4-times more energy. Switching energies, as shown in Fig. 8a, are slightly higher for a circuit with a snubber, but the voltage mismatches on MOSFETs are again on the acceptable level. Thus, additional losses (around 100 µJ) must be accepted in circuits with series-connected transistors. Various values of snubber capacitances were tested - see results in Fig. 9. The higher the capacitances are, the lower is the imbalance. Moreover, it also slows down the switching times of transistors, which slightly affects the energy loss. Including both factors, the total losses are slightly higher for higher snubber capacitance (Fig. 8b).



(a)



(b)

Fig. 7: Oscillograms showing the switching performance without (a) and with a snubber circuit (b) -from the top drain-source voltage of the upper and lower transistor (100 V/div) and drain current (10 A/div), time scale 200 ns/div.

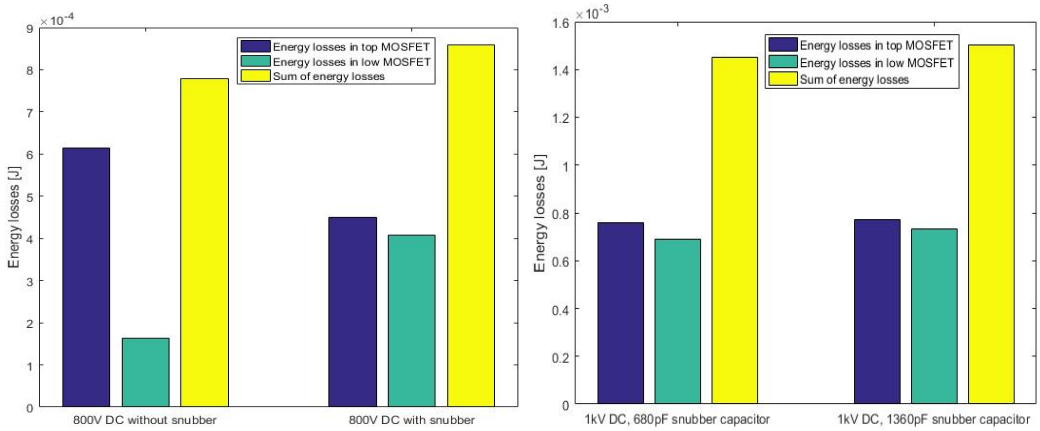
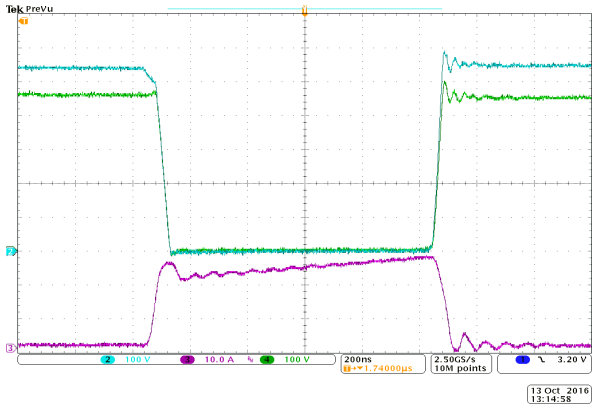
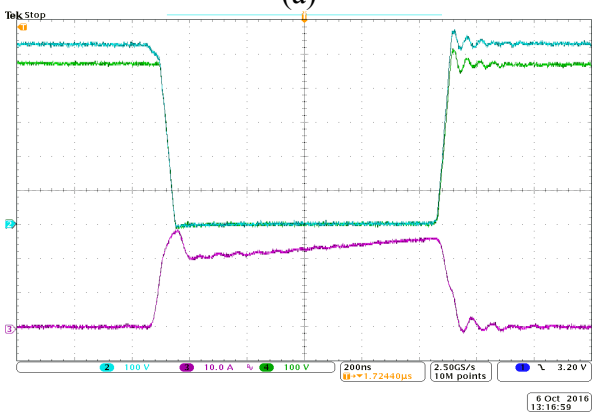


Fig. 8 Comparison of the switching energies: with and without snubber at 800 V DC (left) and with two different snubbers at 1 kV DC (right).



(a)



(b)

Fig. 9: Oscillograms showing the switching performance of the series-connected SiC MOSFETs using two different snubber capacitors: 680 pF (a) and 1360 pF (b) at 1 kV DC. - from the top drain-source voltage of the upper and lower transistor (100 V/div) and drain current (10 A/div), time scale 200 ns/div

Conclusion

Series connection of the SiC MOSFETs may be an interesting solution in medium voltage applications. However, there are several challenges to be addressed, especially when high switching speeds are anticipated. At first, the power circuit layout, including the supply system, must be carefully designed to avoid mismatches in parasitic inductances. Then, the gate drive circuitries must also be identical in order to avoid time delays. Nevertheless, this condition is very hard to fulfill if the switching times counted in tens of nanoseconds are taken into consideration. Actually, in a real system some delay between control signals of the series-connected devices will always occur and it is rather difficult to employ time matching systems such a presented in the paper. In addition to this, potential mismatches in the device parameters (i.e. devices input capacitances) will also exist in practice. That is why, an additional snubber circuits discussed in the paper seems to be an interesting solution. It has been shown that by using snubber circuits, the voltage imbalances are reduced to reasonable level at a cost of slightly reduced switching times and increased power loss, which seems to be on acceptable levels.

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