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Electrical Characterization of Silicon Cores from Glass-Cladded Fibres

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Condensed Matter Physics
Submission date: May 2014
Supervisor: Ursula Gibson, IFY

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"If I could explain it to the average person, it wouldn't have been worth the Nobel Prize"

-Richard Feynman

NORWEGIAN UNIVERSITY OF SCIENCE AND TECHNOLOGY

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Abstract

Department of Physics

Master of Science in Condensed Matter Physics

Semiconductor core fibres represent an emerging technology with potential applications in many areas, including photovoltaics and optical transmission. Recent advances in fibre manufacturing techniques has allowed long, continuous silicon core fibres to be produced in commercial draw towers. The effect of the molten core fibre fabrication method on the electrical properties of silicon cores from glass-clad fibres have been studied. Fibres with core diameters ranging from 60 to 300 µm were produced using a CaO interface modifier between the core and cladding. Five silicon material types with increasing phosphorus doping levels were analysed before and after the drawing process using four point probe technique, supplemented with microscopy and compositional analysis. Novel techniques for preparing and measuring fibre samples were developed, which is suitable for a range of fibre diameters. Cores produced from lightly doped materials showed a large increase in conductivity, while cores produced from a relatively highly doped material showed a small decrease in conductivity. The results suggest that the manufacturing process has introduced significant amount of impurities to the silicon core, which corresponds to additional charge carriers.

Preface

This master's thesis was written during the fall of 2013 to the spring of 2014 and submitted in partial fulfilment towards a master's degree in physics at the Norwegian University of Science and Technology, NTNU. The experimental work was performed at the Department of Physics and at the Department of Material Science and Engineering. The work was carried out under supervision of Professor Ursula Gibson.

I would like to thank those who devoted their time to assist me throughout my time at NTNU; Fredrik Martinsen, who is equally as persistent and stubborn as I with the development of preparation methods; the staff at the NTNU Nanolab for being such a valuable resource throughout my project; Eric Karhu for not only his help with laboratory equipment but also his interesting conversations about science, politics, and life in general. Special thanks to Andrew Dibbs and Erlend Nordstrand for creating a solid foundation for fibre fabrication and my supervisor, Ursula Gibson for the help, direction, and overall enthusiasm.

This thesis includes a thorough coverage of the introduction, background, and methods sections in hopes that future students and those unfamiliar with fibre production may use this information for their benefit in their professional lives or simply for their curiosity.

Trondheim, May 2014

Kyle Andrew Lapointe

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List of Abbreviations and Constants

4PP	4 Point Probe
BSE	Back Scattered Electron
CVD	Chemical Vapour Deposition
CZ	Czochralski
DI	Deionized Water
e-beam	Electron beam
EFOG	Etched Fibre-on-Glass
EGS	Electronic Grade Silicon
FOS	Fibre-on-Silicon
IC	Integrated Circuit
ID	Inner Diameter
I-V	Current-Voltage
MEMS	Micro-electromechanical Systems
MFP	Mean Free Path
MGS	Metallurgical Grade Silicon
MOF	Micro-structured Optical Fibre
NREL	National Renewable Energy Laboratory
NTNU	Norwegian University of Science and Technology
OD	Outer Diameter
PPB	Parts per billion
PPM;	Parts per million
PV	Photovoltaic
PVD	Physical Vapour Deposition
RPM	Revolutions per minute
SC Si	Single Crystal Silicon
SE	Secondary electron
SEM-EDS	Scanning Electron Microscope-Electron Dispersive Spectroscopy
SOI	Silicon-on-insulator

1. Introduction

1.1. Brief history of Silicon

Silicon has become synonymous with the photovoltaic (PV) and electronic industries, yet this association has only been a relatively recent development. Silicon's rise in commercial use has its roots in the rapid industrial expansion in the 1950s, entwined with the production of iron/steel for commercial and military purposes [1]. Along with chromium, manganese, and nickel, silicon became increasingly popular in the late 1800s as it was observed that one, can in part, gain control over many material properties by using alloying agents including strength, toughness, ductility, and corrosion; silicon has a positive effect in steel as it decreases the stability of carbides [2]. Due to the natural abundance of silicon present in its oxide form, silica (SiO_2), it was once known as the "poor man's alloying agent" [1]. During this time, there was a strong drive to lower manufacturing costs and create more efficient processes to purify silicon for various metallurgical purposes. Once it became readily available, other uses and effects were discovered, for instance it became known that silicon as an alloying element reduced magnetic hysteresis losses in steel [1].

Silicon's popularity in the electronics industry arose from its semiconducting characteristics. Its ability to rectify current in a diode, leading to the creation of one of most important devices for modern day electronics in 1954: the solid-state transistor. Silicon has had a substantial impact on the PV industry as it serves as a substrate for conventional PV cells as well as other integrated circuit (IC) electronics, such as in computer processers. These types of uses require ultra-pure silicon with impurities in the single ppb range in order to these devices to function efficiently. For IC applications, a purity or (99.9999999%) or otherwise known as 9N (9 nines) is common and usually referred to as electronic-grade silicon (EGS). In addition, silicon is normally manufactured in large single crystals. These requirements are a result from the high sensitivity of electrical properties and ever decreasing dimensions of devices: Intel currently incorporates 22nm gate lengths (~100 Si atoms) in their Ivy-bridge processors, emphasising the importance of purity [3]. Production of EGS

silicon is relatively energy intensive and costly, therefore only used for applications that require precision control. Though still relatively pure, a slightly lower purity silicon usually around 6-7N is used in PV industries, referred to as Solar-grade silicon (SGS). The reduction of purity is attributed to the low benefit to cost ratio of employing ultra-pure silicon. Silicon used in both industries is produced using the similar methods through a number of refining steps starting with silica, otherwise known as 'sand'. It has since spurred a technological advancement in the production methods of high quality silicon, namely the *Siemens Process*, *Czochralski,* and *Float zone* growth methods, which has lowered the cost considerable compared to 20 years ago. Silicon demand has risen exponentially over the last 10 years, however, it can be shown that the majority of silicon is still used in the metallurgical industry [1].

1.2. Motivation and Scope

The past hundred years has represented a golden-age in advancement of our understanding of light and many of its intrinsic properties, spawning entirely new applications. Optical fibres have transformed the many technological areas including communication, electronics, medicine, and of course optics. Optical fibres act as the communication backbone of the planet, providing a framework for the internet, telephone, and other telecommunication services. They represent the most efficient commercialized method to transmit light over long distances; a typical loss for commercially available fibres is on the order of 0.1dB/km [4]. Many niche applications have evolved as well, for instance, optical fibres are routinely used in lasers and sensors. Fibres can be manufactured from a variety of elements and materials, which can be found as exotic combinations of elements or relatively simple commonly found materials. The majority of optical fibres used today are silica based fibres and thus have become a well-established technology.

The development of solar and electronic industries has triggered an enormous leap in usage and applications of silicon. There is always interest to improve our understanding of materials and more importantly, the depth of applications they can be used for. Silicon's dominating role in conventional PV and electronics markets'

suggest it will remain a well-used material for some time. Improved manufacturing methods have steadily decreased the cost of high purity silicon.

Silicon core fibres have recently come into the scientific spotlight, spawning interest in research from groups across the world. The economic suitability and transmission properties of silicon in the mid-infrared (IR) spectral range has sparked interest in the biomedical, and energy industries where they may be used for power delivery, infrared sensors, and high frequency waveguide structures [5]. Due to their small dimensions, these fibres has spurred entirely new research into crystal growth. There has been a large effort in recent years to develop alternatives to conventional silicon solar technology in order to reduce the cost per kW. There is current interest in application of fibres in renewable energy. Radial PN junctions in the form of wide-array solar cells have sparked interest as an alternative technology for photovoltaics (PV) due to a reduced cost of manufacturing and high absorbance cross section [6]. Silicon based fibres radial PN junctions may have many advantages over conventional silicon solar cells, yet represent a largely unexplored area. Currently effort is being put into improving the manufacturing process of such fibres, wires, and rods. There have been recent advancements in the semiconductor core fibres manufacturing methods used that have produced record low loses of ~ 5dB/cm [7]. Recent exploration into various new geometries of silicon, such as bundled fibres may lead to new commercial applications.

However, little is known about the how fibre production process affects the electrical properties from the starting material to the fibre, which is extremely important in most applications, especially PV. This work explores the molten core method of silicon-core fibre production using the alkaline interface modifier CaO. This work carries on from previously established work by Andrew Dibbs and Erlend Nordstrand who laid a solid foundation in silicon core fibre production [8]. This investigation focuses on the electrical properties of manufactured fibres in effort to determine and clarify effects the production method has on the material Carrier diffusion length greatly contributes to the efficacy of PV and is strongly dependant on the resistivity.

Starting materials comprised of sectioned, single-crystal Si ingots manufactured using the CZ pulling process with varying levels of phosphorus doping are studied by using a specialized preparation process in order to characterize fibres using a custom-built four point probe (4PP). In addition, characterization of the fibres by SEM-EDS and

optical microscopy supplement the 4PP results. The results are compiled into a comparison of electrical properties before and after the pulling process.

2. Background

This section includes a detailed literature review on relevant topics related to the production of silicon core fibres and background to procedures used in this work.

2.1. Silicon

The work presented involves the production and characterization of silicon core fibres. Approximately 27% of the Earth's crust is composed of silicon, found in its oxide form SiO_2. Its abundance has lead it to become one of the most widely used materials the semiconductor industry and as a natural consequence, one of the most researched. As a semiconductor, it displays properties of a both a conductor and an insulator depending on an external stimulus, such as light or an electric field. Its tetravalent nature mimics the behaviour of carbon, but at a substantially less reactive level. Silicon is very reactive with oxygen and will spontaneously produce a thin natural oxide layer approximately 2 nm in thickness [1]. Like water, silicon shows a positive thermal expansion coefficient upon solidification, which is roughly equal to 9% by volume [9]. This can cause difficulty in applications with phase changes from liquid to solid, such as in producing silicon based fibres.

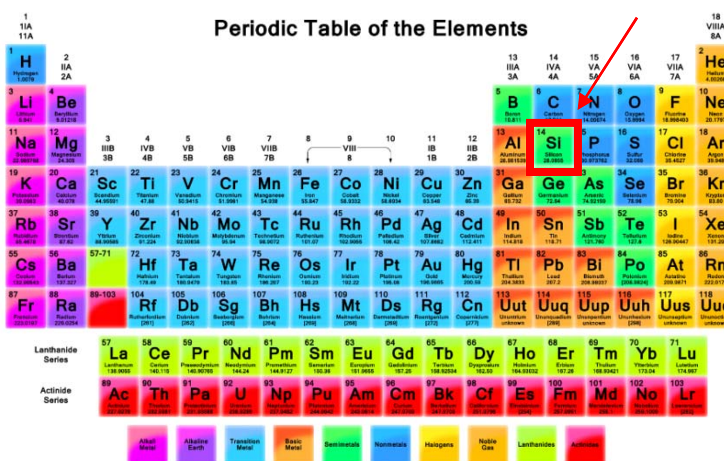


Figure 2.1: Periodic table of elements emphasizing silicon, modified from [10].

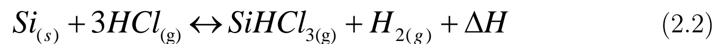
2.1.1. Silicon Production

The silicon refining process is one of the major contributors and silicon's commercial success. The refining process is responsible for achieving many of silicon's material properties, such as conductivity. The starting material for metallurgical grade silicon (MGS) and electronic grade silicon (EGS) is silica (SiO_2). Pure MGS is produced industrially by the reduction of silicon dioxide by carbon electrodes in large arc furnaces; the overall reaction being [11]:

$$SiO_{2(s)} + 2C_{(s)} \leftrightarrow Si_{(s)} + 2CO_{(g)} \tag{2.1}$$

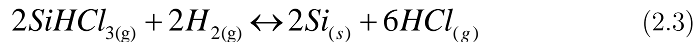
Equation (2.1) is referred to as the Carbothermic process. In reality, there are many by-products including SiO, SiC, CO2, and micro- SiO_2, which reduces the overall yield and increases the complexity of the process. This process is highly energy intensive and requires approx. 11-13MWh per metric ton of MGS silicon [11]. The product of this reaction is still too impure to use in electronic applications and is roughly 98% silicon by this stage.

The Siemens Process is most widely used to further refine silicon into high purity from MGS. In this process, MGS silicon is crushed into small pieces and reacted with HCl to produce Trichlorosilane ($SiHCl_{3(g)}$), following the reaction [12]:



$$Si_{(s)} + 3HCl_{(g)} \leftrightarrow SiHCl_{3(g)} + H_{2(g)} + \Delta H \tag{2.2}$$

Trichlorosilane is then reduced by the addition of hydrogen gas.



$$2SiHCl_{3(g)} + 2H_{2(g)} \leftrightarrow 2Si_{(s)} + 6HCl_{(g)} \tag{2.3}$$

The silicon product from equation (2.3) is very pure, reaching 9N purity. This represents a carbon contamination of less than 2 ppm and less than 1 ppb of group III and IV elements, which are critical doping elements for silicon. Figure 2.2 is a schematic of a conventional Siemens reactor for production of high grade silicon. There are other types of reactors using a modified Siemens process, such as fluidized bed reactor (FBR), which runs as a continuous process rather than a batch process.

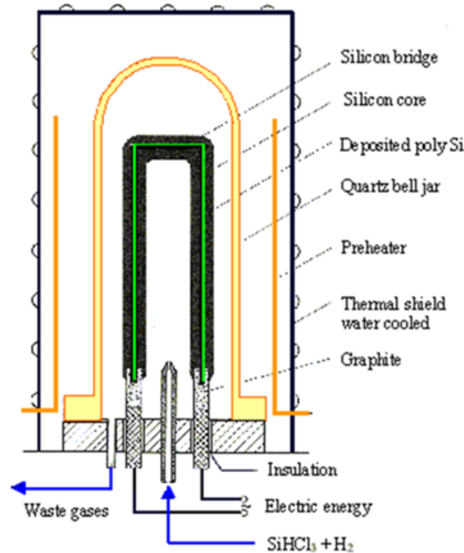


Figure 2.2: Schematic of Bell jar Siemens reactor. EGS silicon is 'grown' on the U-shaped bridge inside the reactor [13].

The end stage of this process produces high grade poly silicon EGS. For many applications that require monocrystalline silicon, one more step is involved. The most common way to produce single crystal (SC) silicon on a commercial scale is the *Czochralski method* [12]. This method involved melting down fragments of EGS, and solidify the liquid silicon into a preferred crystal orientation. The method uses a 'seed' crystal of SC silicon with the desired orientation. While rotating, the seed is dipped into the Si melt and slowly pulled upwards. Liquid Si is pulled upwards with the seed by surface tension forming a thin layer, which can transfer heat away. Solid Si nucleates onto the seed with the same orientation. The temperature, pull rate, rotational speed, and surrounding atmosphere are carefully controlled in order to ensure the Si solidifies as desired. This process can produce relatively large ingot diameters, exceeding 30cm [12]. The process is sensitive to impurity contamination from the diffusion of impurities from the refractory crucible, usually made of silicon nitride. Oxygen is unwanted as it reacts with metallic impurities. In addition, nonhomogeneous distribution of desired impurities such as group III and V elements is also a concern. Doping is usually achieved by mixing in the correct ratio of dopant material into the Si before the CZ process [12]. Over the years doping has been subjective in nature, changing in nomenclature. In order to clarify, dopant nomenclature in this work will follow Table 2.1.

Table 2.1: Dopant nomenclature for Silicon [12].

Dopant	Type	Concentration ($atoms/cm^3$) $< 10^{14}$ Very lightly doped	$10^{14} - 10^{16}$ Lightly doped	$10^{16} - 10^{19}$ Doped	$> 10^{19}$ Heavily doped
V	n	n^{--}	n^{-}	n	n^{+}
III	p	p^{--}	p^{-}	p	p^{+}

2.1.2. Silicon: The Material

Most of silicon's properties and behaviours can be better understood from an overview of its atomic behaviour. All crystalline solids exhibit an ordered structure of atoms. The smallest repeating unit volume of atoms is referred to as a unit cell. Pure silicon arranges itself in a diamond-cubic crystal structure, which as its name suggests is the same structure as carbon based diamond. It can be visualized as two interpenetrating face-centred cubic (FCC) lattices with the second lattice shifted $\left(\frac{1}{4},\frac{1}{4},\frac{1}{4}\right)$ relative to the first: See Figure 2.3. Its structure is a result of the sp^3 hybridization of electron orbitals, allowing bonding with 4 atoms.

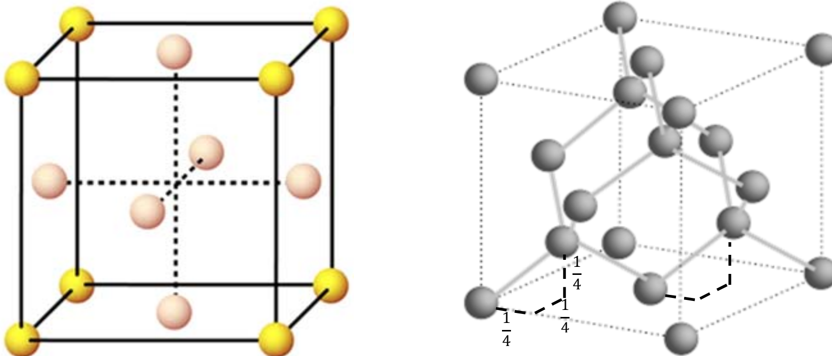


Figure 2.3: *Left)* Standard FCC unit cell. Atoms are present on the corners and faces of the cubic cell [14] *Right)* Silicon diamond-cubic lattice. Easily visualized by $\left(\frac{1}{4},\frac{1}{4},\frac{1}{4}\right)$ [15] transformation from an FCC cell.

Silicon's structure is highly symmetric being cubic in nature and displays a high degree of mechanical anisotropy, easily cleaving along the (100) plane. The atomic structure differs with regards to sp^3 orbital orientations, leading to electrical

anisotropy. Most BCC and FCC based materials will show at least some anisotropy due to differences in atomic packing. For example, the electrical conductivity and etching of silicon with potassium hydroxide significantly differs between the (100), (111), and (110) crystal planes.

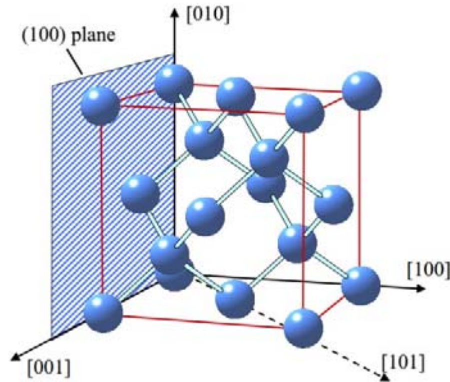


Figure 2.4: Illustration of (100) crystal plane and select directions in the diamond cubic lattice [16].

The above is only valid in a monocrystalline structure. In reality, it is quite difficult to produce SC silicon. Only under highly controlled processes such as in CZ pulling will silicon solidify into a single crystal structure. Due to thermodynamic and kinetic considerations, silicon will preferably solidify (like all other crystalline materials) into in a local ordered, but randomly oriented domains called grains. Heterogeneous nucleation requires less energy to initiate compared to homogeneous nucleation and is more likely to begin on surrounding walls and inclusions, essentially any liquid-solid interfaces. This process begins simultaneously at different places in the melt, forming small ‘seeds’ distributed around the melt. The solidification interfaces expand in different orientations forming regions of varying crystalline orientation, such a material is referred to as polycrystalline. These grains have a large impact on mechanical and electrical properties of the material. Grain boundaries are relatively high energy regions due to mismatch of atomic lattice; the atomic spacing is strained relative to their equilibrium positions. Boundaries create extra resistance for electrons, acting as a high energy barrier. Fractures are more likely to occur at the grain boundaries as well. Figure 2.5 highlights the development of a polycrystalline material.

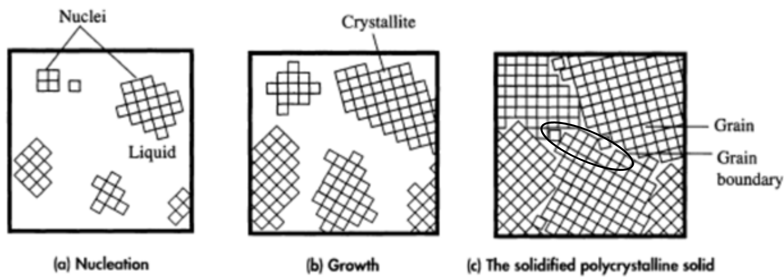


Figure 2.5: Schematic of solidification of a liquid into a polycrystalline structure from initial nuclei to crystalline structure. Grain boundaries occur at the interfaces of misaligned crystals. Time progression (a)-(b)-(c) [17].

Band Theory is an important tool to distinguish a semiconductor's electronic band structure and is critical to the understanding of semiconductors electronic properties. This fundamental property can only be realized when examining electronic properties at the atomic level using quantum theory. As electrons are fermions and obey the *Pauli Exclusion Principle,* in which each electron in an orbital around the atom's nucleus is at a unique energy level. Considering a one atom case, the orbitals exist at distinct quanta of energy. In the case of many close packed atoms, as in a crystal, orbitals begin to overlap and interact with surrounding atoms creating new energy states. A 'band' is formed from the continuity of allowable energy states of atoms' electrons over a range of energy. An example of this effect is illustrated in Figure 2.6: r=∞ implies an isolate atom, while r=a_0 represents a solid with atoms at its equilibrium spacing

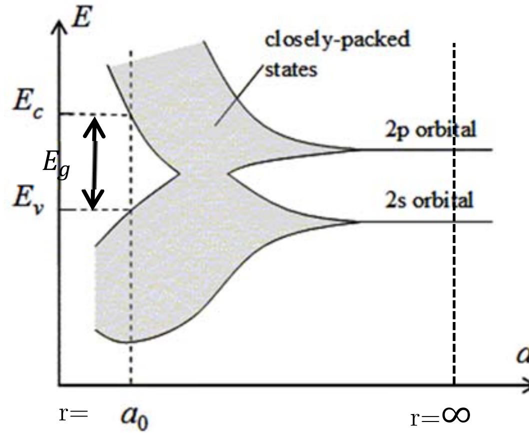


Figure 2.6: Illustration showing formation of bands in a semiconductor w.r.t. atomic distance. Grey areas are continuous energy levels, while the white areas are forbidden. The creation of a bandgap due to a discontinuity in energy levels, denoted by E_g. Modified from [18].

Semiconductors and insulators display a forbidden zone: an energy range where electrons cannot exist. This zone is referred to as a bandgap gap in energy level creating distinct bands. The bandgap is represented as a relative difference from the highest occupied molecular orbital, otherwise known as the valence band (VB) edge, and the lowest unoccupied molecular orbital, otherwise known as the conduction band (CB) edge, denoted as E_V and E_C respectively. In a general sense, the difference between the semiconductors and insulators is the size of the bandgap. Exact definitions are contested, but for simplicity an insulator is usually defined as a material with a bandgap greater than 3.3 eV [2]. However, this value is arbitrary as some 'semiconductors' display a bandgap of over 3eV, for example ZnO and ZnS. Metals do not have this gap in energy and thus usually display conducting properties.

A materials bandgap is responsible for many of its electrical and optical properties. In simple terms, an external stimulus, such as an incoming photon with an energy equal to the bandgap will excite an electron in the VB to the CB. This process leaves behind an empty bond, seen as positively charged charge pseudo-particle, called a 'hole'. An excitation of the electron though the bandgap is said to create an electron/hole (e^-/h^+) pair. Once in the CB, an electron is free to move in the material in a delocalized state, this is the key to transforming a semiconductor into a conducting state. Electronic bands fluctuate relative to the direction in

momentum space denoted by k. In technical terms, k is related to the Fourier transform of crystal spatial domain into the frequency domain. Silicon's electronic band structure is displayed in Figure 2.7.

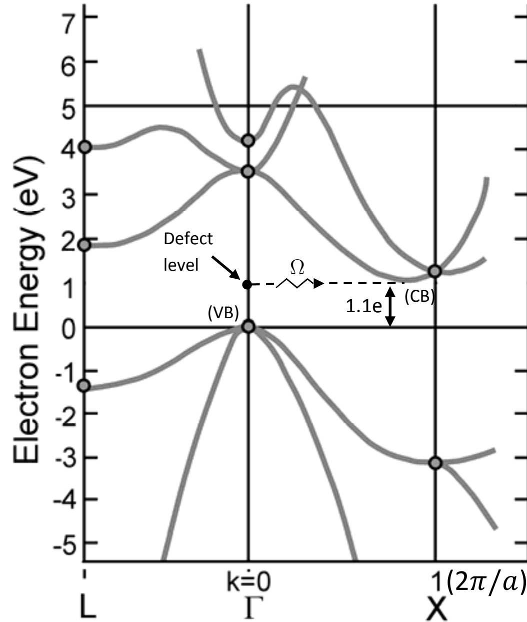


Figure 2.7: Electronic band structure of silicon E(k), marked by Brillouin zone directions. Energy is relative to the top of the VB. Excitation is assisted by a defect level and phonon (Ω). Data from [19].

Silicon is an indirect bandgap semiconductor, that is, the VB and CB edges do not lay in the same k-space. An excitation of an electron requires an assistance of a phonon to transfer momentum in k-space for the electron to reach the CB. A phonon is a quantum of lattice vibration. For simplicity, silicon's band structure is usually given without k dependency when not directly referring to k dependence of energy such as in Figure 2.8. Silicon's bandgap is generally reported as ~1.1eV corresponding to a wavelength of 1.13μm (infrared). The associated between energy and photon wavelength is given by:

$$E(\lambda) = \frac{hc}{\lambda} = hv \tag{2.4}$$

Where h is Plank's constant ($6.62607x10^{-34}Js$), c is the speed of light in vacuum ($2.99792x10^{8}m/s$), and λ is the wavelength of the photon.

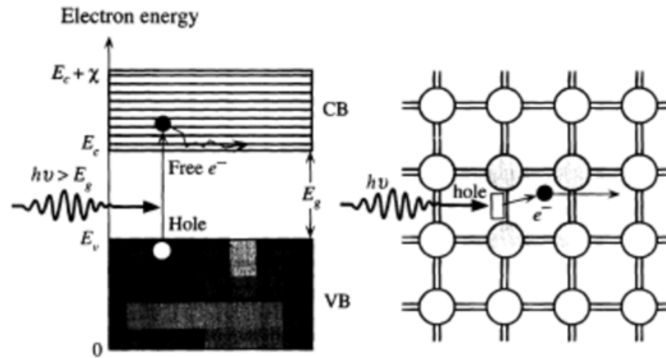


Figure 2.8: Excitation of an electron from the VB to CB from a photon with $E > E_g$, showing the creation of an e^-/h^+ pair [17].

Semiconductors electrical properties are highly sensitive to doping, that is intentionally mixing in impurity atoms into the lattice to produce changes in the quantity of charge carriers i.e. electrons or holes. With the knowledge of doping levels one can estimate the electrical behaviour of a semiconductor, and vice versa. Impurities have a relative difference of electrons in their valence shell, producing local changes to the electronic structure of the host semiconductor by adding or removing an electron to the semiconductor's lattice. For an example, arsenic contains five valence electrons, 1 more compared to silicon's 4 valence electrons. When arsenic is introduced into the silicon lattice, it binds to Si, but the extra electron is loosely bound to the As atom. This final material is referred to as n-type while As is a donor atom. Oppositely, boron contains 3 valence electrons. When it binds to silicon, the fewer amount of electrons leaves one bond unsatisfied. This absence of a bond is referred to as a hole and carries a positive charge (h^+). The resulting material is classified as p-type and boron as an acceptor atom. Both of these particles are loosely bound to their host and thermal energy is usually sufficient free these particles by causing an excitation. An illustration of this effect is shown in Figure 2.9.

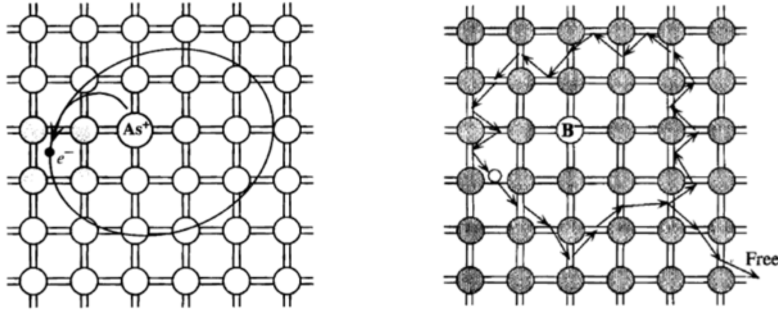


Figure 2.9: *Left)* As dopant in Si crystal producing an extra delocalized electron (e⁻) *Right)* Boron dopant in Si crystal producing a hole (h⁺) [17].

The relationship between temperature and thermal energy (E_T) is given by:

$$E_T = V_T q = k_B T \tag{2.5}$$

Where V_T is the thermal voltage, q is the magnitude of the electronic charge ($1.602x10^{-19}C$), k_B is Boltzmann's constant ($8.617x10^{-5}\ eVK^{-1}$), and T is the temperature in K. For example, the equivalent energy at room temperature (298 K) is ~0.03 eV. Where $1\ \text{eV} = 1.602\text{x}10^{-19}J$. In terms of the electronic band structure, the acceptor and donor atoms lay just above and below the band edges.

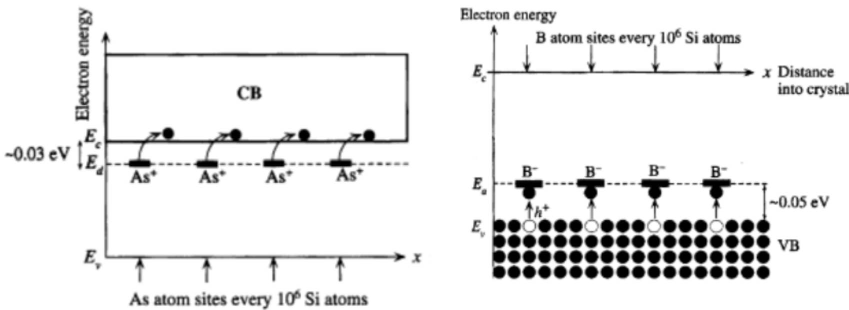


Figure 2.10: Excitation of dopant atoms (As and B) at a concentration of 1ppb in silicon. [17]

The introduction of charge carriers have a large impact on the electronic properties of the semiconductor. Even low concentrations of p- and n-type impurities change the conductivity significantly due to extra charge carriers. The conductivity of the semiconductor depends not just on the amount of the carriers, but also the carrier's

mobility $\mu_{n/h}$, which is a measure of its ability to move through the atomic lattice. Conductivity can be estimated by:

$$\sigma \equiv \frac{1}{\rho} = qn\mu_n + qp\mu_h \tag{2.6}$$

Where ρ is the resistivity, n is the donor concentration, p is the acceptor concentration, $\mu_{n/h}$ represents the mobility of the carrier (usually expressed in cm^2/Vs, and q the unit charge of the carrier. The mobility in turn is can be estimated by its scattering time, and the effective mass. This is treated by the classical Drude model. The carrier mobility is estimated by [17]:

$$\mu_{e/h} = \frac{q\tau_{e/h}}{m^*_{e/h}} \tag{2.7}$$

Where $\tau_{e/h}$ is the mean lifetime before scattering of the carrier and $m^*_{e/h}$ is the effective mass of the carrier (where n/h indicated the carrier type). It is a strange notion that holes have a mass, in this sense mass represents a resistance to acceleration. The positive nuclei within the lattice acts as a force against the positively charged hole, giving it 'mass'. The relationship between impurity concentration and conductivity of silicon has been well documented and experimentally researched. Figure 2.11 shows quantitatively, the relationship between impurity concentration and conductivity of silicon.

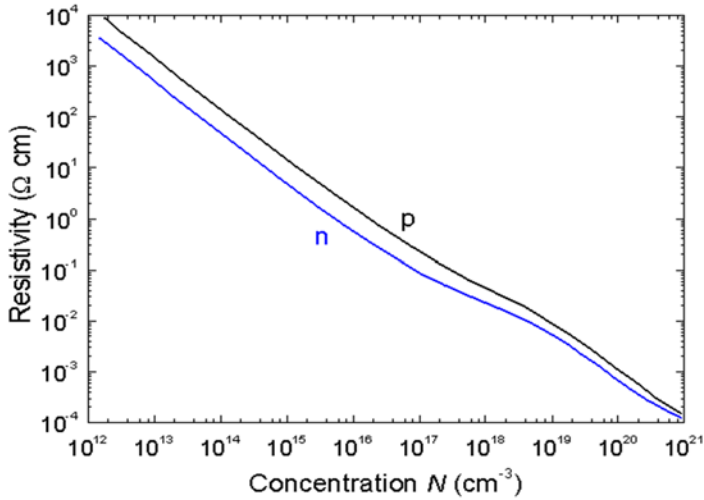


Figure 2.11: Relationship between n and p type impurity concentration and resistivity of silicon showing a general decline in resistivity with increasing donor density [17].

The true effect of grain boundaries on conductivity can be interpreted as energy traps in the band structure. The high energy acts to create energy levels located in the forbidden bandgap that effectively trap electrons in the conduction and valence bands. Overall, this effect reduces the amount of free electrons in the conduction band, which increases resistivity. This effect is realized as a reduction in diffusion length, carrier lifetimes, and carrier mobility. An illustration of the effect of grain boundaries on the band structure is shown in Figure 2.12.

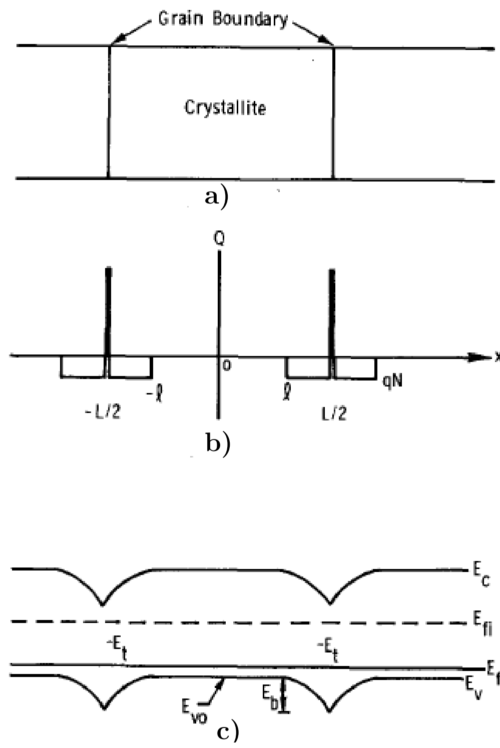


Figure 2.12: *a)* Polycrystalline material with grain boundaries. *b)* Charge distribution in material at grain boundaries. *c)* Resulting energy band structure with energy wells shifted by value E_b, the trap levels are marked by E_t; modified from [20].

It is important to note that the electronic band structure is not as simple as is expressed in this work. For a more detailed treatment of band models and doping, see reference [21]. Table 2.2 is a summary of some important properties of crystalline silicon.

Table 2.2: Summary of important properties of silicon [1, 17].

Property	Value
Density [g/cm^3]	2.32
Bandgap [eV]	1.13
Crystal Structure	Diamond-Cubic
Lattice constant [nm]	0.54305
Melting Temperature [°C]	1417
Intrinsic Resistivity[a] [Ωcm]	$2.3x10^5$
Coefficient of thermal expansion [cm/cmK]	$2.6x10^{-6}$
Thermal Conductivity [$Wm^{-1}K^{-1}$]	150
Index of refraction	1.54

[a] At 300K

2.1.3. Photovoltaics and Silicon's Role

Silicon's role in PV has its roots in the discovery of a PN junction. The PN junction, as it suggests is a junction created between p-type and n-type semiconductor sections. The donors and acceptors of the two sections interact to form a small intrinsic electric field. An incident photon with $E > E_g$ will produce an e^-/h^+ pair, normally this pair's life is short lived recombining immediately releasing heat. However, the electric field inside the PN junction acts to separate the two charge carriers, reducing the probability of recombination. For illustration of this effect see Figure 2.13.

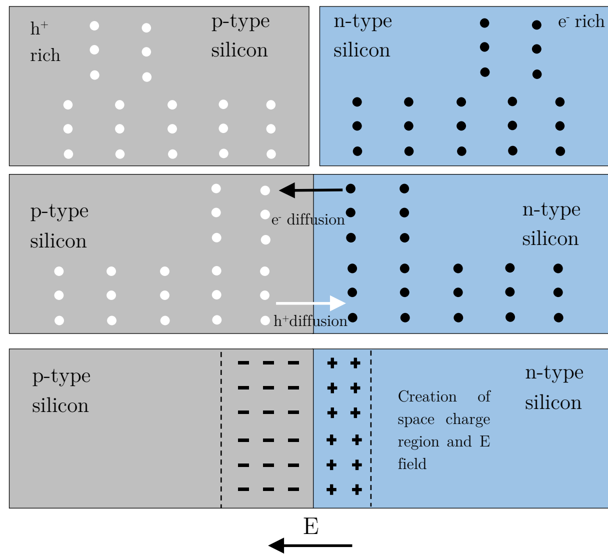


Figure 2.13: Simple PN junction system. Upon contact, electrons from the n-type material diffuse into the p-type due to a concentration gradient. The initially neutral material is now charged near the interface, forming an electric field in opposition to the diffusion flow.

Silicon's bandgap is coincidently suited for the solar spectrum here on earth, which also contributes to silicon's popularity in PV. Conventional silicon based PV has been well established for more than 3 decades. A clear trend indicates efficiency of PV is increasing considerably impart due to an increase in research. Research into improving efficiency, improving product lifetimes, and reducing cost of manufacturing is still ongoing and has explored new geometries and compositions of silicon PV. To date, the record efficiency for a silicon based solar cell is approx. 25% by Amonix achieved using concentrated sunlight. The maximum efficiency of a single junction cell is given by the Shockley–Queisser limit and is around 29% [21]. Figure 2.14 is an excerpt from National Renewable Energy Laboratory (NREL) list of efficiencies for various types of PV from 1995 onwards. It is important to note that the maximum theoretical limit of a solar cell ~86.6%, predicted for a solar cell with an infinite number of junctions [21]: i.e. 86.6% of incoming photon energy is the maximum amount of that could ever be converted into electrical energy. What Figure 2.14 does not show is the cost per kW. Technologies such as multi-junction and metamorphic solar cells has certainly pushed the limits of efficiency in PV, but the majority of a high performance technologies are only realized on a laboratory scale as it is too expensive for commercialization. The motivation to

reduce cost but retain reasonable efficiencies has so far explored primarily high impurity or high defect materials, such as amorphous silicon [22].

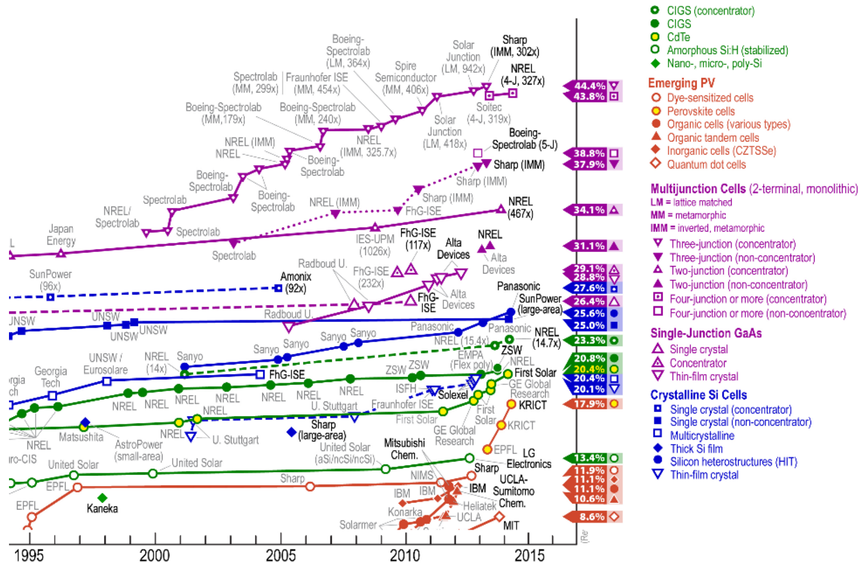


Figure 2.14: List of top efficiencies vs. year for various types PV technology; tabulated by NREL, modified from [23].

By definition efficiency, η is:

$$\eta \equiv \frac{P_{out}}{P_{in}}$$

The physical expression for efficiency of solar cells is [21]:

$$\eta = \frac{V_{oc} \cdot J_{sc} \cdot FF}{P_{in}} \tag{2.8}$$

Where V_{oc} is the open circuit voltage (voltage produced at zero current), J_{sc} is the short circuit current (current at no load), FF is the fill factor, and P_{in} is the radiant power from the sun. The fill factor is a term representing the maximum power that

can be harnessed from a particular system. The current output from a solar cell can be estimated by [21]:

$$J = J_{sc} - J_0 \left[\exp\left(\frac{qV}{K_B T} \right) - 1 \right] \tag{2.9}$$

And the open circuit voltage leads to:

$$V_{oc} = \frac{K_B T}{q} \ln\left[\left(\frac{J_{sc}}{J_0} \right) + 1 \right] \approx \frac{K_B T}{q} \ln\left(\frac{J_{sc}}{J_0} \right) \tag{2.10}$$

Where J_0 is the diode current (assuming an ideal diode). The diffusion length, $L_{n/h}$ (subscript indicating carrier type) is defined as the average length a carrier travels before recombining [6]. Thus, V_{oc}, J_{sc}, and *FF* are influenced heavily by diffusion length of the carriers, the lower diffusion length, the higher recombination rate, both J_{sc}, and V_{oc} drop.

$$L_n = \sqrt{D_n \tau_n} = \sqrt{\left(\frac{K_B T}{q} \mu_n \right) \tau_n} \tag{2.11}$$

Where D_n is the diffusivity constant, estimated by the *Einstein Relation*, μ_n is the electron mobility, and τ_n is the average carrier lifetime. Eq. (2.11) represents diffusion length of electron carriers, holes abide very similarly. J_{sc} can be viewed as the amount of photogenerated current produced across the material. J_{sc} will increase as L_n increases until a limiting point where, L_n becomes larger than the cell thickness, or the optical thickness; Kayes defines the optical thickness as $1/\alpha$, where α is the attenuation coefficient considering the entire solar spectrum [6]. As an arbitrary definition, $t = 1/\alpha$ is when 90% of the incoming light has been absorbed, given by an integration over all wavelengths using *Beer-Lamberts Law*. The optical thickness dictates how thick a material should be in order to absorb the incoming energy of light.

An array of radial PN junction fibres will act as a solar cell and has recently become an idea as an alternative to conventional cells. One major advantage is that the dimensions of the fibres act to reduce the length (x) carriers must travel such that

$x < L_n$. The use of fibres also has the capacity to vastly increase the effective surface area for absorption. Incorporating silicon based materials is an obvious choice due its availability cost and manufacturing technology. Figure 2.15 illustrates the idea using a radial PN junction as a solar cell. However, not much is known of how the manufacturing processes of fibres effect their electrical properties. The majority of research has been on laboratory grown silicon nanowires through a variety of methods such as vapour-liquid-solid, laser ablation, chemical vapour deposition (CVD) and molecular beam epitaxy (MBE), or lithographic methods on SOI wafers, all of which produce high quality single crystal samples [24].

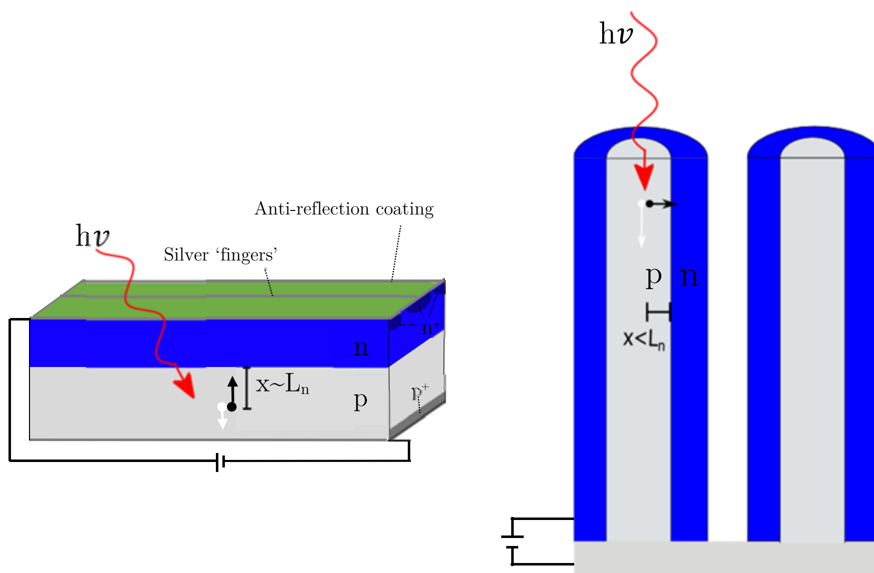


Figure 2.15: *Left)* Conventional silicon based planar solar cell. n^+ and p^+ regions serve to reduce minority carrier surface recombination. Silver fingers collect electrons generated from absorption of light. Anti-reflection coating improves absorption by reducing reflectance of incident light. *Right)* Radial PN junction based solar cell (concept).

2.2. Fibres and Fabrication

Waveguides are one of the major applications of fibres. Waveguides serve as infrastructure for communication around the planet, with most high bandwidth connections facilitated by optical fibres. Optical fibres have also become very useful in many other areas, including sensors, lasers, and lighting. They have advanced our understanding of light and ability to manipulate light. This section will provide a brief overview on optical fibres and current production techniques of semiconductor core fibres.

Fibres are commonly known to be thin multi-layered concentric cylindrical wires. At the simplest level a difference in refractive indexes between the core and layer surrounding the core known as the cladding is responsible for the waveguide effect. A simple fibre illustrating the different layers of components is shown in Figure 2.16.

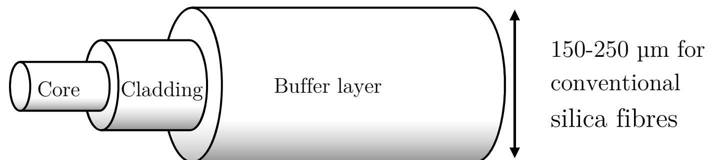


Figure 2.16: Schematic of the different layers within a conventional fibre.

The key mechanism behind the propagation of light in an optical fibre is the relative difference in refractive index. Conventional fibres are almost completely produced from silica due to the commercial availability, established manufacturing processes, and its performance in the mid-IR range [2]. Although complex compositions are used as well depending on the application and wavelength used. Propagation of light is mostly confined to the core although some of the field binds to the cladding. Commercial fibres are protected from weathering and given increased strength by a buffer layer on the outside. Fibres produced as a part of this research do not include a buffer coating.

Semiconductor core fibres share its structural makeup with that of silica optical fibres. Incorporating semiconductors in fibres have only been recently explored and

made possible by constantly improving manufacturing processes of optical fibres. Silicon core fibres have become popular in research after the ability to draw continuous fibres with relatively low attenuation [25]. One advantage of combining semiconductors and optical fibres is the possibility of new integrated electronic optical devices; currently there is a disconnect between the transport and the processing of light. In addition, silicon core fibres may have applications in PV.

2.2.1. Current Techniques

To date focus has been on Si and Ge core optical fibres. Silicon has the potential to define a new class of optical fibres focusing on IR transmission and non-linear optics due its transparency in the mid-IR [25]; research into these fibres have focused on transmission at 1.55µm as it is within the silicon's transmission window. The wavelength appears promising for research with silicon fibres because of the availability of optical components and lasers developed for telecommunications [26]. This section explores methods of silicon core fibre fabrication.

2.2.1.1. Molten Core Drawing

The molten core drawing method is similar to the method used to pull conventional optical fibres. A preform consisting fibre materials scaled to larger dimensions is placed into a furnace. The furnace is heated to around to near the melting temperature of the glass (between 1900°C and 2200°C) [2]. At this point the silica will become soft enough to start stretching under its own weight, known as 'creeping'. When this initial deformation has stretched far enough, the mass at the end is stopped and the heat is turned off. The end is fed through a set of rollers. The rollers enable the pulling force to be changed while controlling the slack. Other equipment consists of a laser measurement system, polymer coater and UV curing stages. The preform is heated again, and when it has reached the correct temperature the rollers being to pull causing a fibre to form. The molten core drawing method is a batch process, limited by the dimensions of preform and conservation of mass. Hundreds of kilometres of fibre can be drawn from a single preform. This pulling method is illustrated in Figure 2.17.

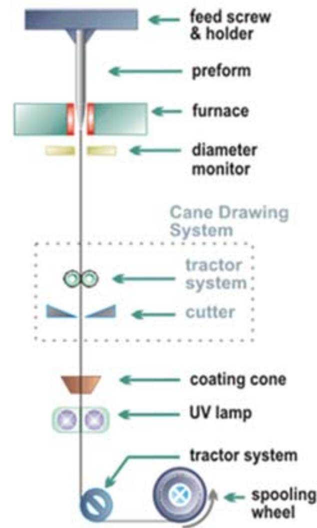


Figure 2.17: Commercial fibre drawing process for conventional silica based fibres. A preform is heated and pulled. The diameter is monitored in-situ by a sensor. The process is continuous and can be tailored to produce fibres of a certain length and diameter [27].

Ballato et al. from Clemson University has developed and progressed research into fabricating solid silicon core optical fibres using the 'molten-core' crucible method; the method is the main method of fibre production for this work. The molten-core method involved placing a poly or monocystalline rod inside the hollow core of a glass rod and drawing while heating the preform. There is nothing fundamentally limiting about this technique in the application of semiconductor cored fibres, however, small dimensional photonic crystals are not possible due to diffusion issues [25]. The production of fibres relies on localized heating of the preform and pulling near the draw temperature. Silicon melts at 1414°C whereas, silica draws at about 1950°C. Theoretically, matching the cladding draw and the core melt temps would alleviate some issues with fibre production that results from the thermal expansion of silicon into the surrounding silica cladding. However, silica remains popular as it is commercially available and has high tensile strength. One benefit of having such a low viscosity melt (large difference in the cladding draw temperature and the core melting temp temperature) is that the core material flows easier, which produces turbulence within the core. It conforms to the shape of the container and can produce good continuity [5]. The oxygen content in the core was found to correlate to core diameter, with greater oxygen content occurring with smaller diameter cores

[5]. The dissolution of cladding into the Si core has been a problem in previous research that has shown relatively high oxygen content in some cases [5, 28]. There is a large negative free energy change corresponding with SiO_2 formation as shown in an Ellingham diagram, which means that silicon oxidizes with a greater driving force than other elements. However, certain oxides (i.e. Ca and Mg) exhibit even lower free energy change. Previous characterization of silicon core fibres show an interesting feature in elemental distribution, a relatively flat profile for each element, whereas a more gradual change in composition would be suspected due to compositional gradients. The homogenization is thought to arise from: [25]

- Turbulent flow during the pull
- Chemical gradient due to the diffusion of oxygen in the cladding
- Thermal gradient from the small size of the heat zone
- Flow induced gradient arising from the pull

Nordstrand et al. has suggested that incorporating a modifying layer at the silica/silicon interface inhibits dissolution the cladding layer and relieves some thermal stress by forming a eutectic between CaO and Si [29]. Mechanical behaviour of fibres produced using this method seem to show improved toughness.

X-ray diffraction on the fibre cores showed a high degree of crystalline and phase purity; crystallinity was estimated to be $>67\%$ for silicon fibres produced by the molten core method [25]. Thermodynamics is thought to govern this process, rather than kinetics to produce the degree of crystallinity found in the core. Small oxygen precipitates should disrupt the solidification process and nucleate different orientations of Si in the core, suggesting that the majority of the core solidified by homogenous nucleation [25]. The molten core method is associated with relatively high growth rates. Growth rates of some crystal growth methods are included for completeness in Table 2.3.

Table 2.3: Relative growth rates for various crystal growth methods [25].

Crystal Growth Technique	Growth Rate	Relative Rate
Hydrothermal	~mm/day	~1
Czochralski	~mm/h	~25
Micro-pull	~mm/min	~1000
Laser-heated pedestal growth (LHPG)	~mm/min	~1500
Molten Core (thick)	~m/min	~1 500 000
Molten Core (thin)	~m/sec	~20 000 000

2.2.1.2. Micro-structured Optical Fibre (MOF)

Work from Penn state and South Hampton University used a silane/helium mix to deposit Si into hollow silica in a pressurized chemical vapour deposition (CVD) process, which creates micro-structured optical fibres (MOF) [25]. Their method produces highly amorphous silicon on the silica boundary. High loses at 50dB/cm at a wavelength of 1550nm were reported for the amorphous sample. However, loses improved with high temperature annealing and larger wavelengths. The lowest loss was around 5dB/cm at 1550nm [25]. The process to create these fibres are complex and difficult, thus it is desirable to employ a less complicated route.

2.2.1.3. Powder-in-Tube Method

Scott et al. has experimented with the powder-in-tube method to produce silicon cored fibres [30]. The powder-in-tube method involves crushing silicon using pestle-and-mortar into small pieces, essentially creating a Si powder and using it as the main source of silicon. The powder is loaded into a hollow silica tube and evacuated prior to pulling to limit Si oxidation. The preform is heated while rotating to produce uniform heating. Once the drawing temperature of ~1600°C was reached, the preform was pulled to produce a fibre. Interestingly, Energy dispersive spectroscopy (EDS) showed that the core was comprised mainly of silicon, with very little oxygen while the cladding consisted of a silicon and oxygen mix [30].

However, the fibre products suffered high losses that are thought to be caused by thermal expansion induced micro-cracks and large grained polycrystallinity along the fibre axis. It showed loses ranging from 4-5.5 dB/cm[30]. Previous work from Dibbs et al. has found that the process incorporates impurities into the fibres, raising the uncertainty of commercial viability [29]. Figure 2.18 shows the pulling method used by Scott et al..

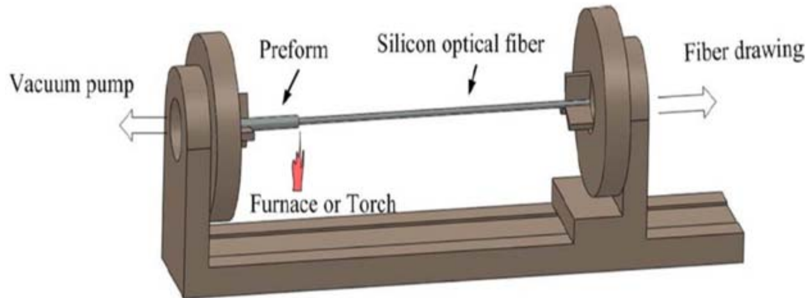


Figure 2.18: Powder-in-Tube method used by Scott et al. A vacuumed preform is heated while rotating and pulled to produce a silicon core fibre [30].

2.3. Metal to Semiconductor Junctions

Ohmic contacts are important in situations where current rectification is undesirable, such as measuring electrical properties of a material. Ohmic constant occurs when the majority carrier is allowed to pass unimpeded through an interfacial region regardless of current direction, i.e., contacts do not limit the current and follow Ohm's law. This is in contrast to rectified, Schottky type contacts that allow a carrier to pass in only one direction, such as in diodes. An Ohmic contact gives a linear I-V relationship regardless of current direction. The only current present during reverse bias in a Schottky contact is due to minority carrier drift. Figure 2.19 shows a qualitative difference between Ohmic and Schottky I-V relationship.

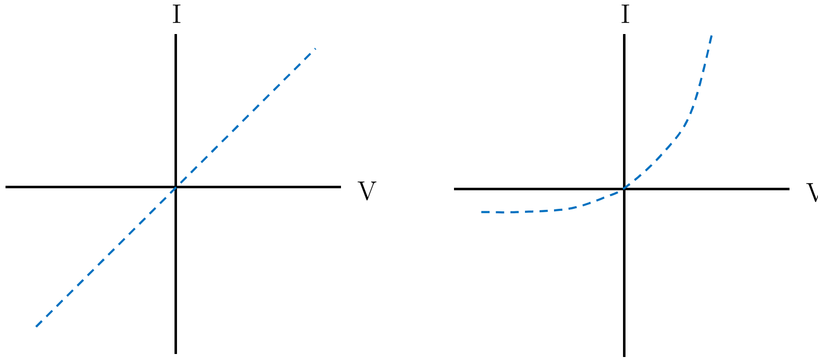


Figure 2.19: *Left)* Ohmic I-V behaviour. *Right)* Schottky I-V behaviour (arbitrary units).

Contacts are extremely important in the context of metal-semiconductor interfaces as there is a mismatch between the Fermi level and carrier bands. When in contact, the valence and conduction bands of the semiconductor will undergo ‘bending’ to achieve potential energy equilibrium with the metal. According to the Schottky model Ohmic contact is formed when there is a zero or negative Schottky barrier height, Φ_B. The model predicts the type of contact between a metal and a semiconductor, which is independent of the semiconductor doping concentration. The Schottky barrier height is defined as the relative difference between the work function of the metal and the work function of the semiconductor. That is [31]:

$$\Phi_B = \Phi_M - \chi_{SC} \tag{2.12}$$

Where Φ_M is the work function of the metal and χ_{SC} is the electron affinity of the semiconductor. (2.12) is commonly known as the Schottky-Mott Rule. Schroder has devised a naming convention for the different contact types according to the Schottky Model [31]:

- Accumulation: $\chi_{SC} > \Phi_M$. Preferred for Ohmic contact
- Neutral: $\chi_{SC} \sim \Phi_M$
- Depletion: $\chi_{SC} < \Phi_M$ preferred for Schottky contacts.

A list of work functions for some common metals is elements is shown in Figure 2.20.

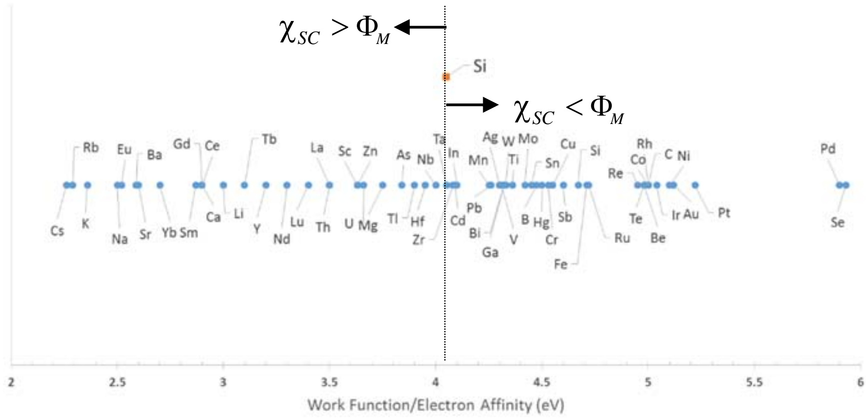


Figure 2.20: Work functions of various metals compared to electron affinity of Si [32].

The effect on conduction and valence bands at a metal/semiconductor interface for and n- and p-type materials assuming accumulation type contact is displayed in Figure 2.21.

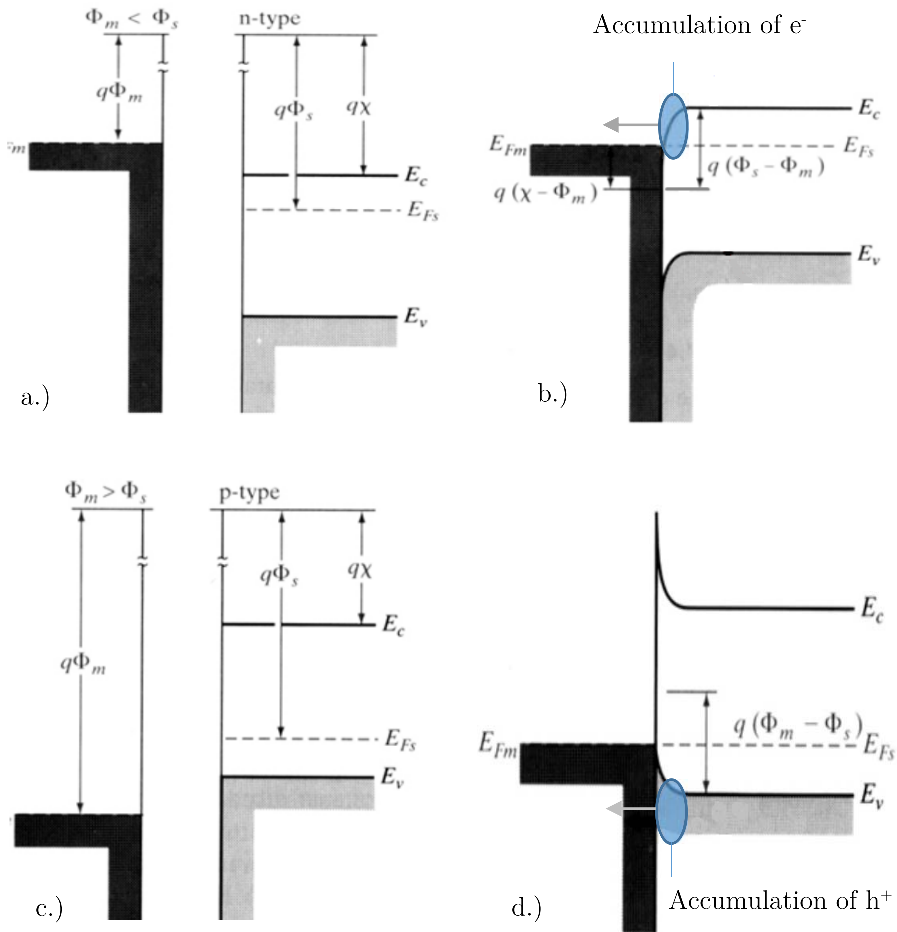


Figure 2.21: Band Diagrams of Ohmic metal-semiconductor contacts a.) n-type (separated) b.) n-type (in contact) c.) p-type (separated) d.) p-type (in contact). Modified from [19].

Upon contact, the electrostatic potential of the semiconductor develops an equilibrium with the metal, which aligns the Fermi level. In both cases, there is an accumulation of the majority carrier near the interface that allows the carrier to cross the boundary. This is because the carrier concentration is higher than that of the bulk, which causes the resistance in the contact region to be low [33]. Thus, there is little or no potential barrier in either direction.

In applications such as resistivity measurements, a potential bias is applied that changes the behaviour of the bands slightly. An application of a potential will bend

the bands towards the potential. An example of positive and negative bias applied to a metal-semiconductor (n-type) is shown in Figure 2.22.

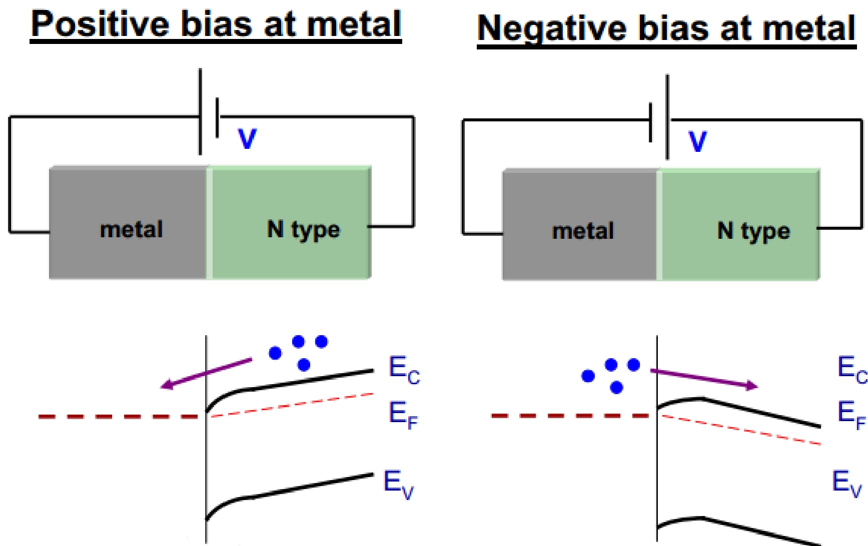


Figure 2.22: Positive and Negative bias of a metal-semiconductor (n-type) junction. A applied potential bends the band edges to form either a depletion or accumulation region for the majority carrier [33].

A positive bias will cause both carriers to easily cross the boundary. However, an application of negative bias will create an electron reservoir at the interface that creates a region of high concentration, which allows the carriers to flow over the boundary due to diffusional energy. The case shown in Figure 2.22 involving an n-type system. The same scenario will be true given a p-type system, however the relationships will be reversed.

The above discussion involves creating accumulation type contacts. In many situations $\Phi_M > \chi_{SC}$, yet an Ohmic contact is still desired. In this situation, a depletion region is formed near the interface. Positive charges from uncompensated donor ions within the semiconductor moves toward negative charges in the metal forming a small electric field near the interface, which bends the bands, forming the depletion region [19]. One practical method to alleviate this issue is by heavy doping

near the semiconductor interface. Φ_B may be positive and still show an Ohmic relationship if, the depletion region is small enough to allow carrier tunnelling. The width of the region is inversely proportional to the donor concentration: $W \propto \frac{1}{\sqrt{N_{D/A}}}$ [33]. Where $N_{D/A}$ is the donor or acceptor concentration. This effect is naturally realized for aluminium contacts deposited on p-type silicon after an high temperature annealing process. The aluminium acts as an acceptor type dopant in silicon, effectively causing a p^+ interfacial layer.

It has been experimentally observed that the barrier height of some semiconductors including Si, Ge, GaAs and other III-V compound materials are largely independent of the metal work function and doping density; however, as stated previously, barrier width does depend on doping density [31]. Interface states are created inside the bandgap of the semiconductor, effectively pinning the Fermi level: Referred to as “Fermi-level pinning” [19]. These types of contacts are generally form depletion type contacts, which means there is a positive Φ_B. It is believed that imperfections at the material surface causing a large increase of surface states, but the true nature of barrier formation is still contested [31]. Depletion contacts are formed on both p- and n-type materials are experimentally determined to be [34]:

$$\Phi_{Bn} \approx \frac{2E_g}{3} \tag{2.13}$$

$$\Phi_{Bp} \approx \frac{E_g}{3} \tag{2.14}$$

E_g represents the band gap of the material. For silicon, $\Phi_{Bn} \approx$ 0.74eV and $\Phi_{Bp} \approx$ 0.37eV.

To complicate things, the true barrier heights have been shown to vary with natural oxide thickness and are dependent on many other factors, such as surface quality. Card et al. showed that the native oxide on silicon pins the Fermi level, effectively lowering Φ_{Bn} to ~0.4eV, low enough to potentially allow tunnelling through the junction [35]; Φ_{Bn} is shown to decrease with increasing oxide thickness (up to 20nm), while Φ_{Bp} has been shown to increase with oxide thickness. This behaviour

was shown for samples that were not heat-treated using a high temperature anneal process. In high temperature anneals, the diffusion of Al into n-type Si caused the barrier height to rise substantially and produce rectifying behaviour [35]. A thorough treatment of aluminium-silicon contacts is given by Card in which he gives current J, as a function of oxide thickness d, temperature T, voltage V, barrier height Φ_B, and tunnelling probability $\Psi^{1/2}$ [35]:

$$J = J_{sat}\left(\exp\left(\frac{qV}{k_B T}\right) - 1\right) \tag{2.15}$$

Where:

$$J_{sat} = AT^2 \exp\left(-\Psi^{1/2} d + \frac{\Phi_B}{k_B T}\right) \tag{2.16}$$

A is the modified Richardson constant (~115 electrons).

There are two ways to create an Ohmic contact between a metal and silicon. Either Φ_B is low (~0.3eV) causing the saturation current to rise, or silicon is heavily doped so that W < 10 nm and is easily tunnelled through [35]. Of course, a material with low resistivity, thermal stability, good adhesion, and a smooth morphology is preferred when making Ohmic contacts for electrical applications. In real-world applications of making contacts, it is difficult to apply theoretical treatments due to its sensitive nature. Typical materials used in industry to create Ohmic contacts with silicon are shown in Table 2.4.

Table 2.4: Commonly used materials for Ohmic contacts in Si [31, 36-39].

n-type Si	p-type Si
Ag	Al*
Ni	Au
Pt*	Pt
Au-Sb	Au-Ga
Al	

*under certain conditions such as high dopant density (>$10^{18} cm^{-3}$) or high temperature anneal.

2.4. Characterization Techniques

2.4.1. Four Point Probe (4PP)

The four point probe (4PP) is a common method to measure electrical impedance in the semiconductor industry. Using a 4-terminal setup, the 4PP can directly measure sheet resistance by measuring a voltage drop across a terminal separation distance. In the 4-terminal mode, a voltage drop is measured by two current neutral terminals held within a collinear and equally spaced active terminals. The benefit of a 4-terminal setup is separation of the current and voltage means there is virtually zero current flowing through the inner sensing electrodes, which limits its contact resistance to virtually zero. A schematic of the 4PP setup is shown in Figure 2.23.

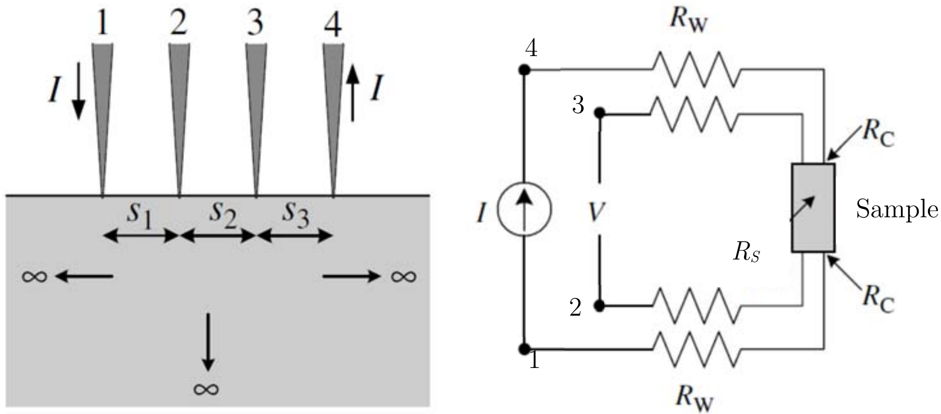


Figure 2.23: *Left)* Diagram of 4-terminal head on a semi-infinite sample illustrating head spacing. *Right)* Equivalent electrical circuitry of a 4PP setup. R_S represents measured resistance, while R_C is the contact resistance on the active current heads [31].

Current, voltage drop, and resistivity are related by Ohm's Law. Given in vector form:

$$\mathbf{J} = \sigma \mathbf{E} \tag{2.17}$$

Where $\mathbf{J}$ represents current density, σ, the conductivity, and $\mathbf{E}$, the field strength.

2.4.1.1. Semi-infinite Samples

Wafers and relatively large samples where the dimensions are large compared to probe spacing are considered semi-infinite samples. The relationship between voltage, current, and resistivity depends highly on the shape of the sample being measured. In the semiconductor industry, wafers and semi-infinite planar samples are popular and 4PP measurements are regularly used to characterize resistivity.

Assuming an isotropic system in (2.17), where $S_1 = S_2 = S_3$, and a semi-infinite sample one can derive that [31]:

$$\int_0^V \mathrm{d}V = \int_0^r \left(\frac{I\rho}{2\pi r^2} \right) \mathrm{d}r$$

$$\rho = 2\pi S \frac{V}{I} \qquad (2.18)$$

Where I represents current, S the electrode spacing, V is the voltage drop, and ρ is the resistivity of the material. Eq. (2.18) assumes a semi-infinite sample size, however, when the sample thickness, t< S , or the electrode placement is an edge, a correction factor, F must be applied. Eq. (2.18) becomes [31]:

$$\rho = 2\pi S \frac{V}{I} \cdot F \qquad (2.19)$$

F has been examined using Carbino sources, Poisson's Equation, Green's Functions and conformal mapping. A detailed derivation of correction factors is given by Weller [40]. F can be written as a product of independent factors.

$$F = F_1 F_2 F_3 \qquad (2.20)$$

F_1 represents a contribution from sample thickness, F_2 the contribution for lateral sample dimensions, and F_3 the placement of probes relative to sample edges. Calculation of the correction cofactors is difficult and their equations usually simplify. This is the case with the sample thickness cofactor, F_1. If $t / s \leq 0.5$, and the sample is on an insulating substrate, F_1 approximates to [31]:

$$F_1 = \frac{t / s}{2 \ln(2)} \qquad (2.21)$$

One can see that in general, this process quickly becomes complex as the sample size decreases, or for oddly shaped samples.

2.4.1.2. Small Cylindrical Samples

For a small cylindrical shaped samples such as fibres, the electrical field can be assumed to be uniform along the longitudinal axis of the cylinder. This assumption leads to a simplified expression relating voltage, current, probe spacing and resistivity.

$$\begin{aligned} E &= -\nabla\Phi(x) \\ &= \frac{-\Delta\Phi(x)}{\mathrm{S}} \end{aligned} \tag{2.22}$$

Where $\Phi(x)$ represents the electric potential, and S represents the probe spacing. Combining (2.22) and (2.17) leads to the expression:

$$V = \left(\frac{\rho S}{\pi r^2}\right) \cdot \mathrm{I} \tag{2.23}$$

Thus the resistivity can be estimated by correlating voltage and current.

2.4.2. Scanning Electron Microscope (SEM)-Energy Dispersive Spectroscopy (EDS)

Scanning electron microscopy (SEM) is imaging technique that uses incident electrons to extract topographical and phase information from a sample's surface. Electrons emitted from an electron gun strike a samples surface. Some incident electrons transfer their energy and cause emission of secondary electrons (SE). Electrons can give a much higher resolution and depth of field compared to using photons as free electrons have much smaller wavelengths. These electrons are captured by a detector to form a topographical image of the surface. However, some incident electrons scatter within sample's crystal structure eventually returning to and ejected from the surface. These electrons are known as backscattered electrons (BSE) and are captured by a detector to form an image showing elemental contrast; heavier elements are more likely to back scatter electrons.

Energy Dispersive Spectroscopy (EDS) or Energy Dispersive X-Ray Spectroscopy (EDX) is a qualitative technique to measure characteristic x-rays emitted from a sample while bombarding it with high energy electrons. The incident electron beam interacts with the electron cloud surrounding an atom, usually providing enough energy to cause an ejection of an inner-shell electron from the sample where the incident energy is greater than the work function of the element. The empty hole left from the ejected electron is then filled by an electron from a higher orbital, releasing characteristic energy equivalent to the drop in energy the electron experiences. This characterization technique is often combined with SEM as it can take advantage of SEM's imaging capabilities.

2.5. Optical Lithography

Optical lithography is a technique used to pattern small features in a photosensitive chemical. It is widely used in the semiconductor industry to manufacture small multilayer devices and micro-electromechanical systems (MEMS). An example of such a device manufactured using optical lithography is shown in Figure 2.24.

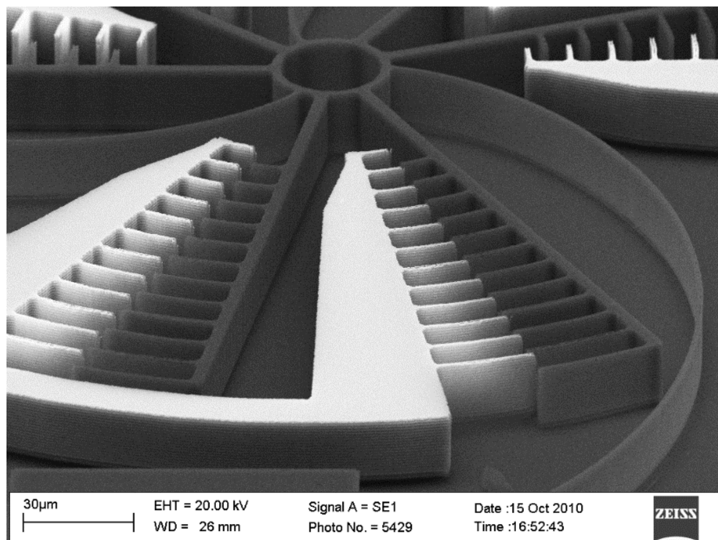


Figure 2.24: SEM image of Archimedes spiral spring MEMS produced using optical lithography and anisotropic etching.

In basic principle Optical Lithography is similar to the developing procedure in photography. Optical Lithography uses light to expose a light-sensitive chemical, which causes changes in its molecular structure to make it either more or less soluble in a developer. The process uses a mask with transparent and opaque areas to limit light exposure in the shape of the required pattern. The photosensitive chemicals are referred to as photoresist and are sensitive to narrow range of wavelengths. There are many types of resist, each finding its niche in a specialized function, but for brevity only Diazoquinone Novalak (DQN) positive resists will be discussed. The DQN resist has 3 components:

- Diazoquinone (DQ) - Photoactive compound
- Novalak Resin (N) - The ‘body’ of the resist
- Solvent - Controls viscosity

The Novalak resin is soluble in alkaline developers however DQ is not, causing the DQN solution to be insoluble in its normal state. Upon exposure to UV light (λ~365nm), DQ absorbs a photon and decomposes to carboxylic acid+$N_{2(g)}$, making the resist soluble in a NaOH based developer. Photoresist is applied to a substrate using spin coating and must be briefly heated after coating to evaporate the solvent. This process is called a “soft-bake”. Oppositely, there are negative type resists in which exposed areas become insoluble in developer. A schematic illustrating lithographic steps to create a pattern on a substrate is shown in Figure 2.25.

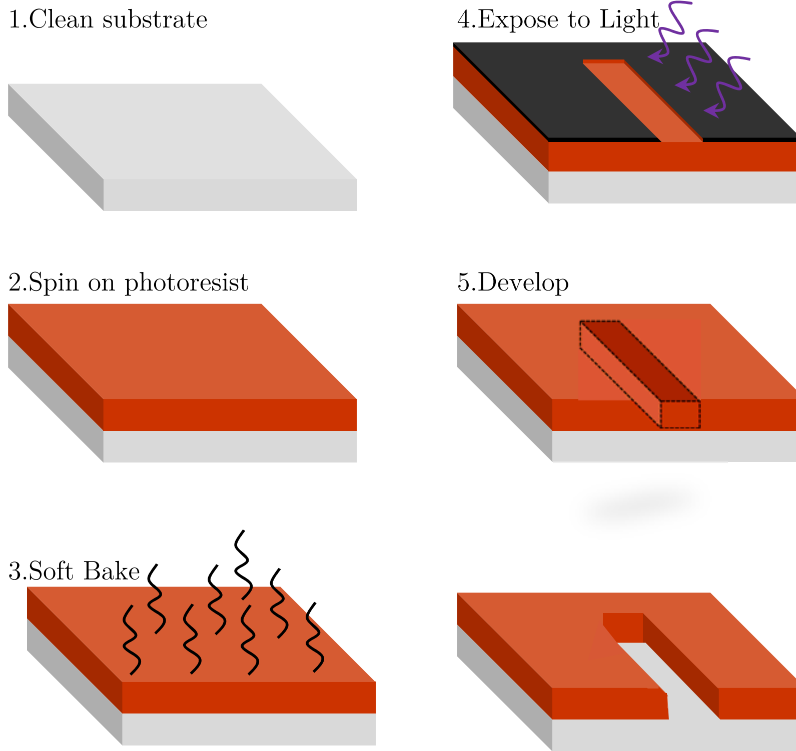


Figure 2.25: Sample lithography patterning process with a positive photoresist. The exposed areas become soluble and are removed by the developer.

Once the pattern is made on a substrate, it is used as a mask for deposition of films or etching. That way one can make complex structures with high aspect ratios such as in the MEMS device in Figure 2.24, which was produced using a deep reactive ion etch. The photoresist can be removed after the subsequent etching or deposition by using an organic solvent, leaving just the desired structure.

2.6. Physical Vapour Deposition (PVD)

This work involved depositing metallic films using different PVD processes, namely sputtering and evaporation. As the name suggests, PVD is a physical process of depositing films onto a substrate, in contrast to CVD techniques, which involves a one or more chemical reactions to grow a film onto a substrate. Film nucleation plays a major role in the structure and properties of deposited films for PVD processes. Nucleation is the initial stage of growth for thin films on a substrate and affects the final structure of the film. Films produced from PVD are not isotropic blocks of material, rather are columnar, nucleating from small seeds at the substrate interface and growing upwards. The density of these films will never be as high as the starting bulk density (range from 90-98%), affecting the electrical and optical properties of the material [41]. A structure zone model proposed by Movchan and Demchishin has classified film microstructure with respect to deposition temperature into three distinct regions. The original structure model is shown in Figure 2.26.

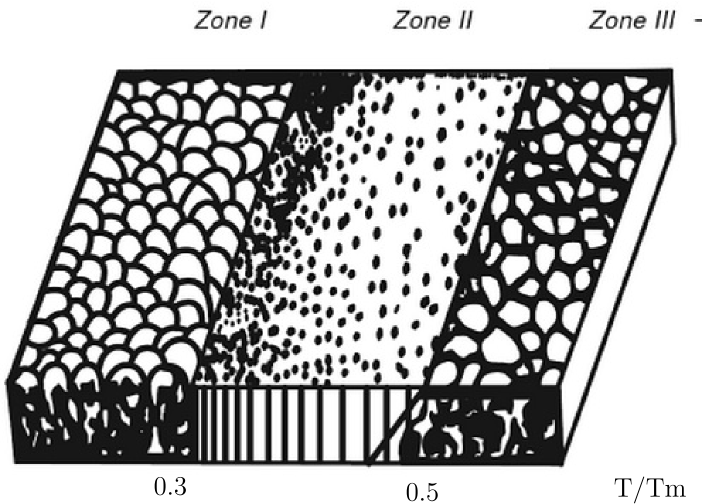


Figure 2.26: Structure zone model according to Movchan and Demchishin as a function of substrate temperature (T) and melting temp (Tm). Zone 1 shows large isotropic grains vertically oriented; Zone 2 is tightly packed columns from improved diffusion; Zone 3 shows isotropic grain structure from annealing. Modified from [42].

2.6.1. Sputtering

Sputtering based PVD involves ejecting atoms from a target material, composed of the depositing material, onto a substrate forming a coating over time. The target atoms are ejected by bombarding the target material with high energy ions in a plasma, usually argon due to its inert nature, cost, and relatively high mass. The ions physically dislodge atoms from the target material and migrate towards a substrate. A region of plasma with high ion density is created by applying a large potential through the argon gas biasing the target material as a cathode; the positive ions are accelerated to energies ranging from 500 to 5 000 eV, enough to knock off (sputter) the target material's atoms [12]. The incoming ion causes a collision cascade, colliding with many times within the materials lattice. Sputtering is advantageous for depositing refractory, conductive materials, and gives the ability to co-deposit complex alloys while maintaining the ability to control many variables of deposition process. For illustrative purposes, a simple schematic of the sputtering process is included in Figure 2.27

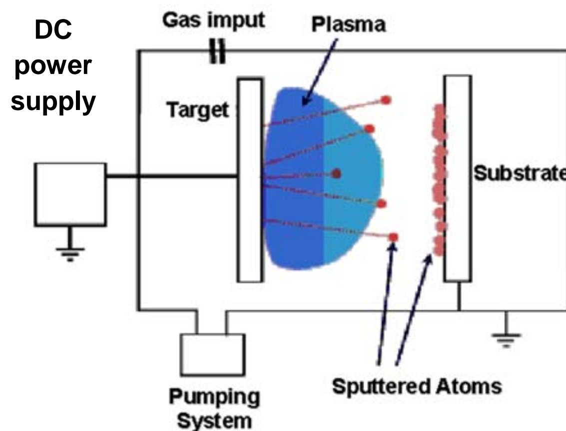


Figure 2.27: Simple schematic of a diode sputter process. Plasma formed from an inert gas (Ar) strikes a target material and ejects atoms. The atoms drift towards and coat the substrate.

The probability of ejecting atoms from the target material is dependent on many factors, such as the operating potential, target material, target purity, pressure

inside the chamber, and incident angle [41]. Sputter systems usually operate wait a gas pressure around 3 mbar creating an angular distribution of sputter atoms. Other target processes include the reflection of the incident ion, ejection of a secondary electron, or implantation of the ion in the target material. The ratio between an incoming ion and a sputtered atom is referred to as the "sputter yield", where a sputter yield of 1 represents an average of 1 ejected atom per incident ion; it is possible for incident ions to eject multiple atoms (sputter yield > 1), especially using high potentials and heavy ions. An illustration of the collision cascade and other target processes are shown in Figure 2.28.

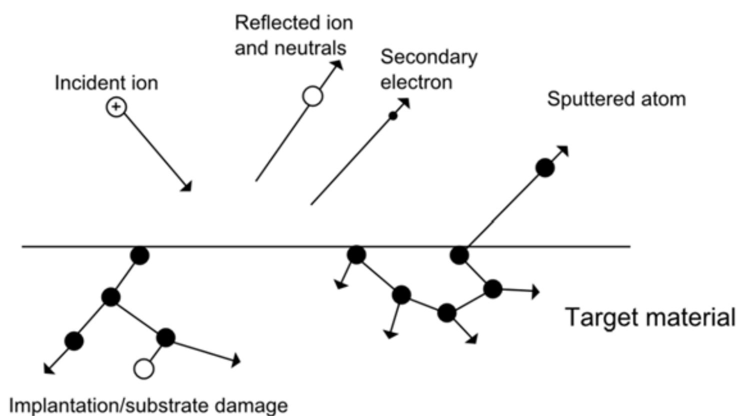


Figure 2.28: Sputter target processes. Incident ions will generate artefacts including secondary electrons and reflected ions, and sputtered atoms.

Overall, reflected ions and neutrals account for ~2% probability per incident ion and secondary electron emissions is ~10% [12].

To increase the ion density near the target material, magnetic fields can confine the electrons in helical paths near the target surface, increasing the amount of ionizing events and thus ion density. This is known as magnetron sputtering and is common in commercial sputter systems due to its higher degree of target utilization. Sputter systems contain multiple magnetron guns oriented within a circular chamber and are angled relative to the substrate. This increases the non-directionality of the process.

2.6.2. Evaporation

Evaporation is relatively simple and early PVD technique. Metal layers were almost solely deposited using evaporation in the early days of the semiconductor industry. However, since the 1970s, sputtering has replaced evaporation for most silicon wafer technologies [12]. In its simplest form, evaporation involves heating a target material until it vaporizes. The vapour flux leaves the melt and travels in a straight trajectory to the cooler substrate, where it condenses and forms a thin layer of solid material. Simple evaporation is accomplished using a target material in a resistive heating element composed of a refractory material with low vapour pressure at the melting point of the target material (thermal evaporation). Other evaporation systems simply pass a high current through the target material to induce vaporization, such as the case with carbon coaters. The evaporation process also requires high vacuum conditions in order to increase the mean free path (MFP) of the evaporated atoms, reducing contamination and increasing process efficiency. A typical evaporation pressure is 10^{-6}torr and below, corresponding to a MFP of ~50m [41]: i.e. the atom will on average travel 50 meters before colliding with another particle. This is in contrast to sputter systems that although require an initial high vacuum, deposit at roughly ~10^{-2}torr (MFP ~50mm). MFP is important as a transfer from viscous to molecular flow regime occurs when the MFP > vacuum system. A simple thermal evaporation scheme illustrating the principle components of an evaporation system is shown in Figure 2.29.

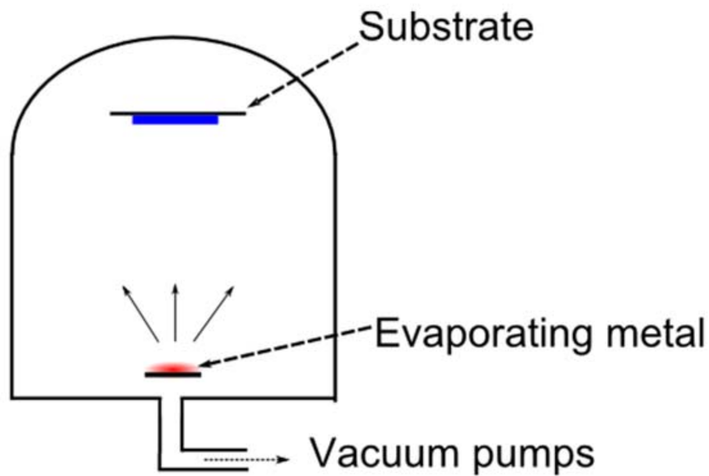


Figure 2.29: Schematic showing simple evaporator system. A resistive heating element causes a sample to melt and evaporate.

Modern evaporation systems commonly employ electron-beam (E-beam) evaporation for more precise control of evaporation rate and increased target utilization. E-beam involves an electrode discharging a beam of electrons at kV potentials, whose path is guided to the target using a magnetic field.

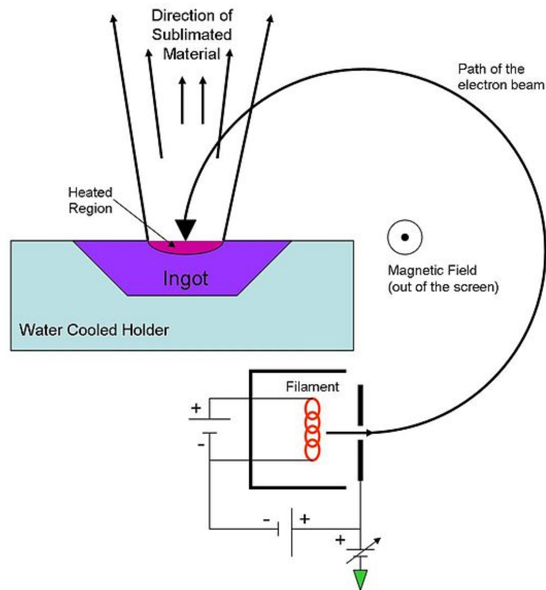


Figure 2.30: Illustration showing the principle of e-beam evaporation. A magnetic field (shown coming out of the screen) bends the electron beam due to the Lorentz force. The electron beam strikes the sample causing heating and evaporation in a confined region [43].

The drawbacks of the evaporation PVD process stems from its limitation of suitable target materials, limited step coverage, and the inability to accurately control compositions of deposited alloys [12]. However, the evaporation is still common and has found niche roles in the research fields that take advantage of these limitations.

3. Methods and Materials

Silicon core fibres were drawn in a quartz tube using the molten core drawing method. Electrical resistivity of 5 SC n-type and intrinsic silicon materials were investigated and compared to resistivity of the fibres. The silicon core fibres were incorporated with a CaO interface modifier. The materials were obtained through a specialized distributer El-Cat from various manufacturers.

Table 3.1: Ingot information specified from the distributer.

Name	Material	Manufacturer	Origin	Resistivity (Ωcm)
D429	Si:P	Prolog Semiconductor	Ukraine	0.130-0.145
O212	Si:P	Cysteco	USA	15-22
E944	Si:P	Pacific Hi-Tech Systems	China	266-336
J895	Si:P	Pacific Hi-Tech Systems	USA	>4 800
3169	Si:i	Pacific Hi-Tech Systems	China	>20 000

3.1. Fibre Fabrication

3.1.1. Coating

Previous work by Dibbs and Nordstrand suggested that an alkaline interface modifier applied to the inner surface of the hollow quartz tube reduced residual stresses in the fibre by forming a small eutectic region at the Si/SiO_2 interface [8, 29]. The coating had little effect on the core composition and improved bending radii. An alkaline coating mixture of $CaO:H_2O$ at a ratio of 1:3 was found to contain suitable viscosity and produce homogenous, consistent coatings [29]. The resulting aqueous mixture of calcium hydroxide allows even coating of the tubes.

$$CaO_{(s)} + H_2O_{(l)} \rightleftharpoons Ca(OH)_{2(aq)} \quad (3.1)$$

Sigma-Aldrich reagent grade (99.9%) CaO was used to make the aqueous coating mixture. CaO powder was mixed with DI water at a ratio of 1:3. The accuracy of this ratio id important as the mixture is sensitive to changes. The preforms were fabricated from hollow quartz tubes with an inner diameter (ID) of 2.2 mm and an outer diameter of 5mm. The tubes ranged in length, but usually were cut to ~25 cm. To coat the tubes, one end was connected to an aspirator while the free end was placed in the aqueous mixture. The aspirator suction force was adjusted to allow the mixture to be drawn up the tube slowly. Afterwards, the coated tubes were placed in a furnace set at 100 °C for a minimum of 72 hours to dry, reducing the hydroxide back to CaO. The thickness and quality of the coating varied slightly from tube to tube, but averaged ~20 µm, which agreed with work from Dibbs and Nordstrand [29]. Over the project, it was necessary to inspect coatings inside the quartz to determine if the coating process was adequate. Measurements from the optical microscope were supported by visually inspecting the transmission of visible light by holding the tube up to a light fixture and looking for contrast. A higher suction force would cause the aqueous solution to start spitting and sputtering through the tube, which produced uneven coatings. An image of a coated quartz tube is shown in Figure 3.1.

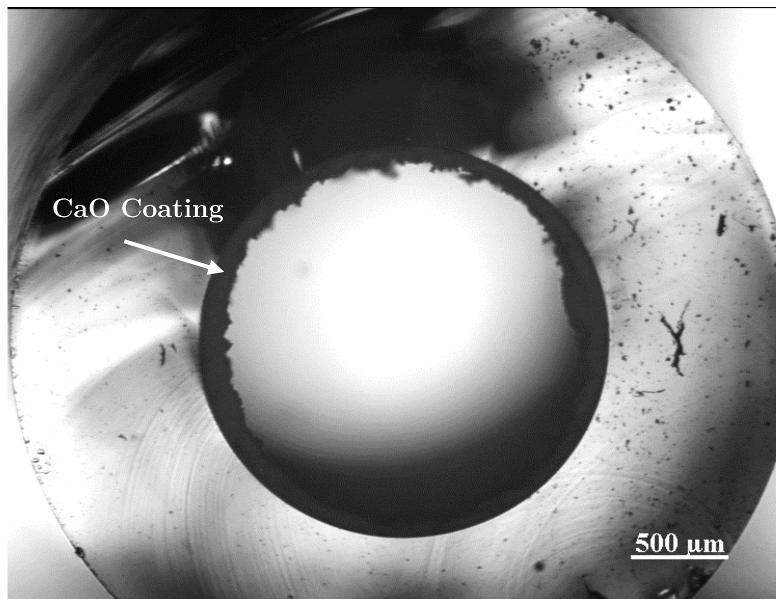


Figure 3.1: Image of CaO coated quartz tube before packing with Si cores.

The stability of the bulk CaO became an issue during the course of the project. CaO will preferentially convert to $CaCO_3$ and Ca(OH) upon contact with CO_2 and H_2O, respectively. CaO powder stored in open atmosphere (within the closed container) seemed to form poor coating after mixing. Elevated amounts of $CaCO_3$ produced very non-uniform coatings due to agglomeration of $CaCO_3$ particles in the mixture and its low solubility in H_2O [44]. Therefore, the bulk CaO powder was stored in sealed, N_2 filled container afterwards.

3.1.2. Preform

The molten-core drawing method was used to produce the fibres discussed in this thesis. Silicon cores were drilled from a bulk single crystal boule and separated into pellets with the diameter 2mm and varying lengths. The silicon cores were cleaned by bathing the cores in 65% nitric acid for 15 minutes, followed by cleaning with de-ionized (DI) water and dried using pressurized N_2 gas. Immediately afterwards, the cores were loaded into coated quartz tubes. The Si cores were loaded into the tube by first pinching off one end of the tube by melting the glass and stacking the cores inside after it had cooled. When loading, no extra force was applied to the cores in order not to scratch the coating when loading. The coating was easily abraded by the cores, one reason why the slightly larger 2.2mm ID tubes were chosen. The loaded tubes were attached vertically to a holding chuck. A diagram of the tube mounting system is shown in Figure 3.2.

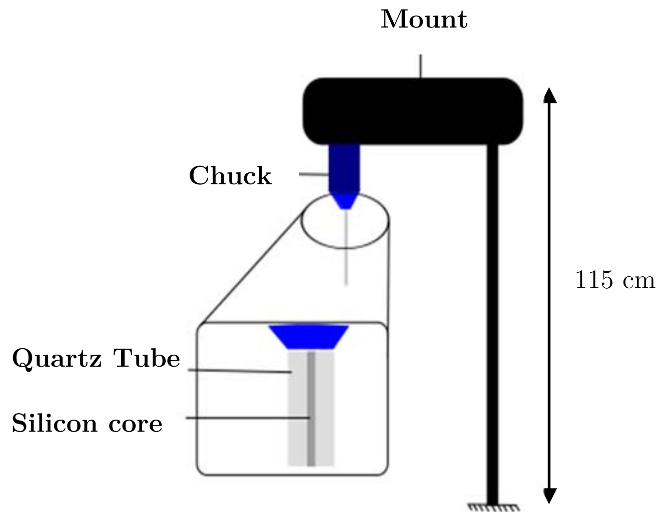


Figure 3.2: Schematic of preform mounting system for pulling (not to scale). The loaded preform is inserted into the chuck and held in place. The mount is composed of a drill press motor and rotates for even heating.

3.1.3. Fibre Drawing

The system was setup in a large fume hood to vent combustion by-products. An oxyacetylene torch was used to heat the preforms for drawing. The oxygen/acetylene ratio was adjusted until the high temperature inner-core of the flame was small and pointed in shape. The preforms were heated until the quartz reached its draw temperature, which is approximately 1925°C [28]. This was estimated by visual inspection of the heated preform while heating as the quartz produced an intense white glow when it became malleable enough to draw. The procedure requires the user to hold the torch near the preform and adjust the distance according to visual clues given by the heated tube. Once a silicon melt region was established and the quartz reached its draw temperature of the glass became a viscous fluid and easily malleable. Applying a little force using stainless steel tongs should create a necking region directly above, this was an additional sign that the tube was ready to be pulled. Pulling the end of the tube rapidly downwards caused the heated zone to neck and form into a thin fibre. The diameter

of the fibre was strongly affected by the pull speed and force, making precise reproducibility of fibres difficult. The pull rates were estimated to be within the range of 1 to 3 m/s. The height of the mounting system limited the length of fibres that can be produced to a maximum of 50cm. After drawing, the fibres were collected and stored; the storage method limited the length of fibres to approximately 7 cm. Figure 3.3 shows a close up of the preform during the heating and drawing process. Due to the thermal conductivity of silicon, the melt zone extending approximately 5 mm above the torch flame.

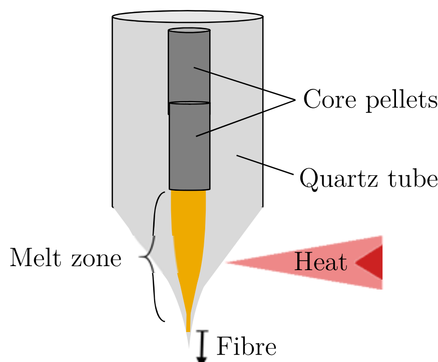


Figure 3.3: Schematic of preform during pulling process. Heat is produced by the oxyacetylene torch. The fibre is drawn from the bottom of the melt zone.

There were some issues with imperfect cores, specifically cores that had fractured slightly during the drilling process. They formed small voids in between cores when stacking. During heating, the air expanded and caused the surrounding quartz tube to burst and in some cases causing liquid silicon to pour out from inside the preform. These were small issues as the silicon would immediately solidify cauterizing the hole in the preform. However, it was noticeable as it reduced the fibre yield considerably as the quartz surrounding the whole fractured forcing approx. 1 cm of preform to be cut off.

3.2. Sample Preparation

3.2.1. Bulk Samples

To reiterate, the starting material consisted of cores drilled from SC-Si ingots with a diameters of 2 or 3 mm. The 3mm cores were not used for fibre fabrication, but due to the limited availability of 2mm cores, the 3mm cores were preferred choice for characterization of starting material. Since the bulk samples were large enough, additional contact leads were not required. Multiple cores exceeding 5mm in length were placed in a small circular epoxy mould, covered with Allied EpoxoFix epoxy and placed aside for a minimum of 12 hours for curing. Once cured, the sample was removed from the mould and ground down to create a planar surface finishing with P4000 SiC grinding paper. In total, 3 separate cores per material were mounted in epoxy for testing. Figure 3.4 shows a planarized bulk sample.

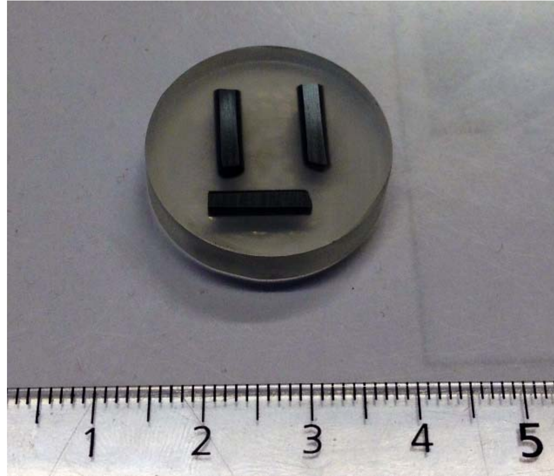
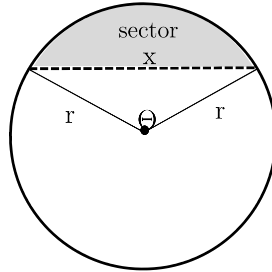


Figure 3.4: Polished 'Bulk' Sample. Bulk cores were mounted in epoxy and ground to reveal a planar surface

Resistance measurements are highly dependent on cross sectional area. The planarized samples represented a small problem as each sample varied in diameter

and ground to a different depth. The cross sectional area was estimated by using simple trigonometry assuming the samples were a near-perfect cylinder.



$$A_{sector} = (\frac{\theta}{2})r^2 - \frac{1}{2}\sin(\theta)r^2$$

$$\theta = \cos^{-1}(1 - \frac{x^2}{2r^2}) \text{ *from Cos Law}$$

$$A_{cross-section} = A_{circle} - A_{sector}$$

$$A_{cross-section} = \pi r^2 - \left[\frac{r^2}{2}\left(\cos^{-1}\left(1-\frac{x^2}{2r^2}\right) - \sin\left(\cos^{-1}\left(1-\frac{x^2}{2r^2}\right)\right)\right)\right] \quad (3.2)$$

Equation (3.2) related the measured value x and radius, r, to the cross sectional area of the cylindrical sample.

3.2.2. Fibre-on-Silicon (FOS) Planarization

The small size of the pulled fibres presented a challenge to characterize. In order to deposit Ohmic contacts to the fibre core, the cladding had to be removed to expose the core underneath. It was thought that it would be significantly easier for future depositions and characterization of the fibre if it was first ground to form a planar surface. The fibre-on-silicon (FOS) technique resembled the preparation of bulk samples, but on a much smaller scale. Fibres were imaged using optical microscope before and after planar polishing to determine the fibre's core diameter and cross sectional area for future resistivity measurements. The fibre was placed flat on a small piece of Si wafer and covered with Epoxobond 110 heat curing epoxy. Si wafers were chosen as a substrate material based on its availability and ease of

cleaving. The substrate was then placed on a hot plate set at 140 °C until the epoxy cured, usually taking 4-5min. Samples were attached a fine polishing holder (referred to as ‘the clock’) by securing the sample to a small stub using heat curing adhesive wax, which attaches into the larger ‘clock’. Not surprisingly, it was quite difficult to polish down a sample accurately to within ±10 µm. An effort was made to polish down approximately 70% of the way using a relatively coarse grit grinding paper (usually 2500 grit), afterwards switching to a fine 4000 grit paper to finish the polish. One issue that arose during the FOS polishing procedure is that the fibre was prone to fracturing. The fibre sample was sensitive to the applied force during the polishing phase. The fractures seem to originate from the cladding and propagated through the fibre in most cases. The fine polish is much less likely to fracture the fibre compared to the coarse polish due to its smaller particle size. Figure 3.5 illustrated the FOS planar polishing procedure.

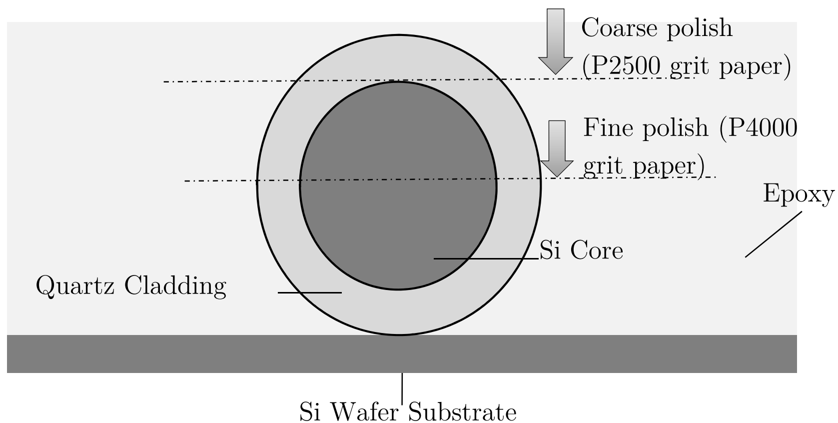


Figure 3.5: Illustration of polishing procedure. Coarse grinding is done until the surface of the core is revealed, then fine grinding paper is used to carefully remove the remaining core material.

The finished product contained an exposed planar surface of the silicon fibre secured in epoxy. Figure 3.6 shows cross-sectional images of the FOS before and after polishing, while Figure 3.7 shows the surface of the FOS sample after polishing.

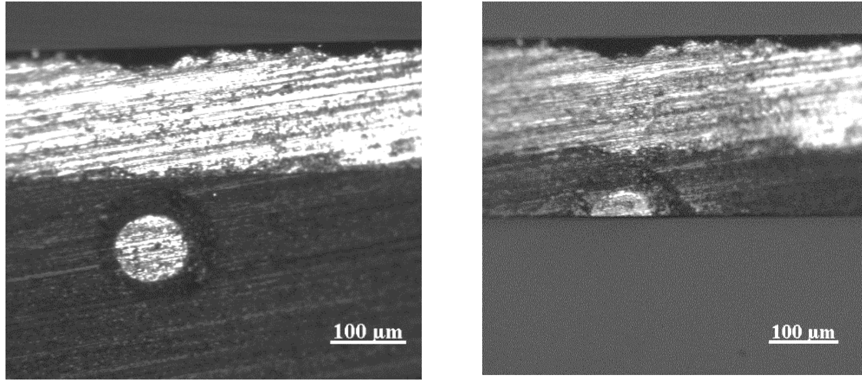


Figure 3.6: *Left)* Before FOS preparation *Right)* After FOS preparation, the fibre was ground to reveal approx. its full diameter.

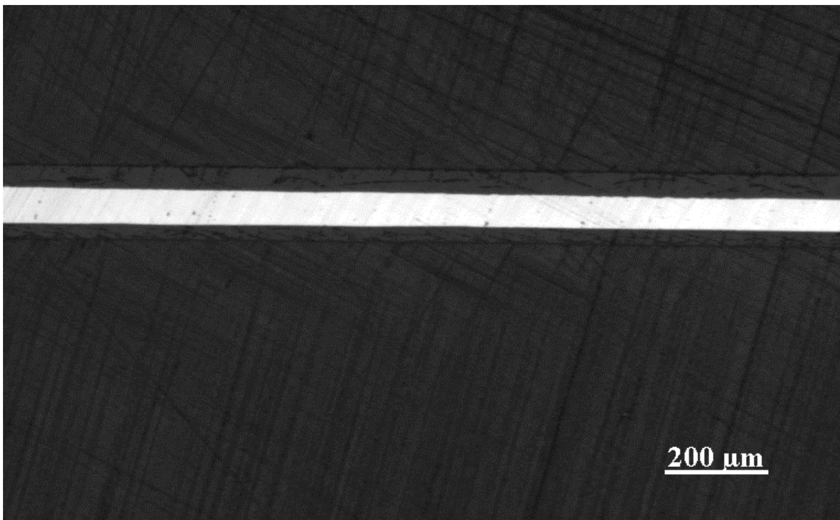


Figure 3.7: FOS Sample surface after polishing. The fibre surface shows grinding streaks but remains un-fractured.

3.2.3. Etched Fibre-on-Glass (EFOG)

As the FOS method requires considerable preparation time, an alternative method to deposit contacts for electrical measurement was developed to measure fibre samples and to test the suitability of contact materials. The etched Fibre on Glass (EFOG) method is a much faster method in terms of turnover time per sample.

Essentially, the method involves removing the silica cladding layer of the fibre using an isotropic hydrofluoric acid (HF) etch then placing the silicon core on a clean glass slide and surrounding the fibre with a thin layer of epoxy. Its success requires the core to rest on the glass substrate surface and allowing surface tension of the epoxy to force the liquid epoxy down the fibre. The key aim of this step is to prevent a shadowing effect by the core during deposition of contacts. The initial procedure involved dropping the fibre carefully onto a small amount of uncured epoxy. The aim of this was to maintain an open surface on top of the fibre, while securing the fibre and provide a good surface for adhesion of contacts. Although this method produced usable results, it was highly inconsistent as it was possible for the fibre to become submerged and in some cases the epoxy did not cure correctly, later affecting the adhesion of the metal contacts. Through a lot of trial and error, the original method was modified to limit the amount of epoxy used, reducing the chance to 'drown' the fibre. It also allowed the majority of metal contacts to be deposited on the glass substrate itself, rather than the epoxy, vastly improving adhesion of the contacts. Detailed steps for this procedure including images are given below:

1. Removed oxide layer by placing fibres in concentrated HF solution (~43% by Vol.). at room temperature for and leaving it in an un-agitated HF solution for 6-8 hours. Once the etch is finished, the fibre cores were thoroughly rinsed with DI water before allowing to dry and placed in a clean glass storage beaker for transportation. It is quite normal for the longer fibres to fracture into many smaller pieces during this step therefore a significant quantity of fibres are needed to ensure success. The fracturing may indicate large residual stresses or even fracturing during the solidification process from thermal expansion mismatches.

2. Epoxobond 110 two-part epoxy was mixed in a ratio of 10:1. A small drop of epoxy (~0.5mL) on a piece of a standard glass microscope slide substrate and spread over a small area to reduce the thickness.

3. The etched fibre was carefully placed on the glass and pushed into the epoxy such that the puddle just covered the tip of the fibre. The surface tension drew the epoxy down the fibre, coating just the sides. This effect is immediate but was allowed to sit for approx. 1 min before curing. The epoxy was cured on a hot plate set at 140° C for approx. 8-10 minutes. The time varied due to the

inconsistent size of the fibres. As simple schematic of cross section of a finished EFOG sample is shown in Figure 3.9 (not to scale), while Figure 3.8 shows a top view of the sample after this stage.

Figure 3.8: Optical microscopy image of EFOG sample after curing showing epoxy encasing the sides of the fibre.

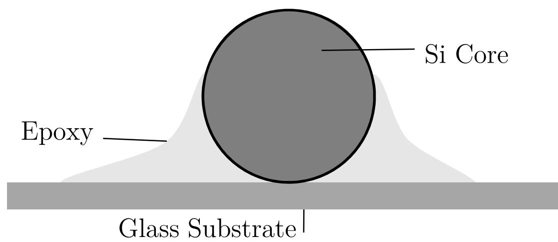


Figure 3.9: Cross section schematic of 'ideal' EFOG sample after step 3.

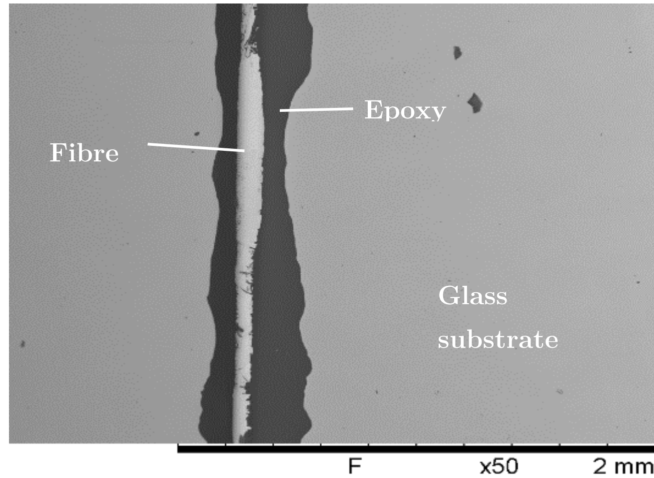


Figure 3.10: Angled BSE image of D429 EFOG fibre indicating fibre surface is exposed.

3.2.4. Lithography

The physical size of the fibre samples limited the ability to directly measure the electrical properties with the 4PP. Also, the potential small cross-sectional area of the fibres lead to upsurge in resistance, which also created issues when measuring using the standard 62.5 mil (1.58mm) probe spacing and the Kiethley power source. To produce viable contacts that will allow the measurement of resistivity similar to that of the starting materials (upwards of 5000 Ωcm) on thin fibres cores that range in diameter from 60-250 µm, we needed to control three major factors:

- Probe Spacing: Lowering probe spacing will reduce the effective resistance. Main issue with high resistivity materials: see (2.23).
- Placement of contacts: The electrical pathway must lead away from the fibre to are area suitable for placement of the 4PP contacts.
- Fibre diameter: increasing the fibre diameter will reduce the overall resistance, allowing a larger current to pass through.

The *finmaskinversted* at NTNU could only machine features at a minimum of ~500 µm, potentially making it problematic solution for measuring small high resistivity fibres (>1000 Ωcm), however it may work for samples with larger cross sectional

areas or lower resistivity fibres (<1000 Ωcm). Conventional optical lithography offers the ability to produce patterned features on the order of a 100 nm, as well as the ability to make complex patterns making it a suitable method to produce a mask for PVD depositions. Conventional masks for photolithography usually are Cr etched patterns on glass made from a relatively complex and expensive electron beam lithography process. Standard masks offer a reusable rigid mask with excellent linearity, smooth surface, and compatible with most mask aligners. They have mainly used for patterning conventional Si wafers in processes that involve multiple patterns and layers. Since the 4PP contacts require relatively large feature sizes, creating an expensive and complex Cr-glass masks to accomplish this task is far in excess of what is needed. Instead, the mask patterns were custom printed onto a transparent Mylar (biaxial oriented PET) by CAD/ART Services[1] for a fraction of the cost and turnover time. Varying the contact spacing between each pattern allowed us to account for variations between pulls such as core diameter due to the incorporation of the human element into the procedure. In total, the mask included five 4PP patterns and twelve Hall patterns. An example of each pattern, highlighting dimensions is included in Figure 3.11 and Figure 3.12.

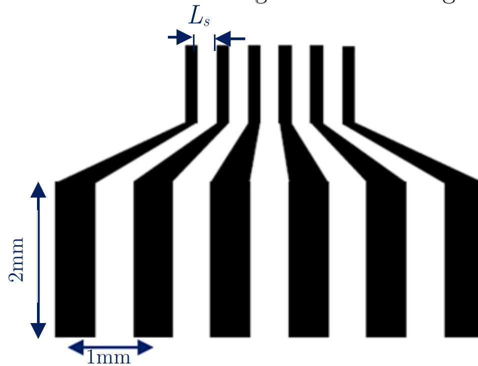


Figure 3.11: Photolithography 4PP mask pattern

[1]CAD/Art Services Inc.
Brandon, Oregon, USA 97411

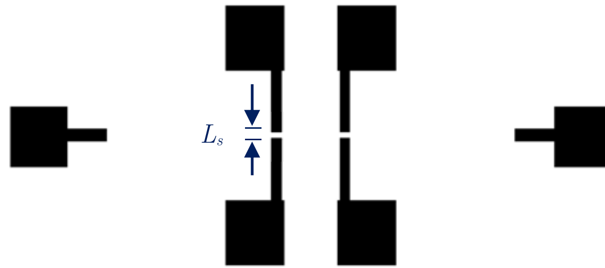


Figure 3.12: Photolithography Hall mask pattern

For simplicity, the black areas in Figure 3.11 and Figure 3.12 represent a transparent section in the mask, while the white spaces in between and surrounding the pattern are opaque; in reality the colour scheme is inversed. Spacing length, L_s varied from 150µm - 1000µm for the 4PP pattern and 80µm - 240µm for the Hall pattern. The purpose of these patterns is to produce a physical mask in a photosensitive photoresist.

Photolithography is highly sensitive to the surface quality. A planarized and uniform sample surface produces higher quality patterns and reduces the complexity of the process. The process is also dependant on many other factors such as, viscosity and thickness of resist, exposure time, surface material, soft baking, post hard baking, and development times just to list a few things. The complete recipes were produced through trial and error over many EFOG and FOS samples. It took considerable time and effort to perfect the lithography procedure as there are many sensitive and essential variables that are required to create a working contact. The most important of which was the surface quality of the epoxy. The finest grinding paper used during the FOS preparation is P4000 grit SiC, corresponding to D_{50} of ~2.5µm and a surface roughness of Ra=20nm [45]. This implies that the surface may contain features around 2.5µm that may be problematic for thin films of photoresist. To fix this issue, a lower RPM spin was used to increase the thickness of the photoresist. Observations of the resist and patterned resist after development shows the coverage was adequate. Furthermore, the Epoxofix epoxy produced very poor homogeneity after the curing process; it was inevitable that small bubbles had formed throughout the epoxy during curing regardless of the mixing technique and adjustments of the ratio between the resin and hardener. Epoxobond 110 delivered

a noticeably better quality epoxy after curing with virtually no bubbles, improving the adhesion of the subsequent deposited resist and metal film. For comparison, two images showing Epoxofix and Epoxobond 110 after the litho-development stage.

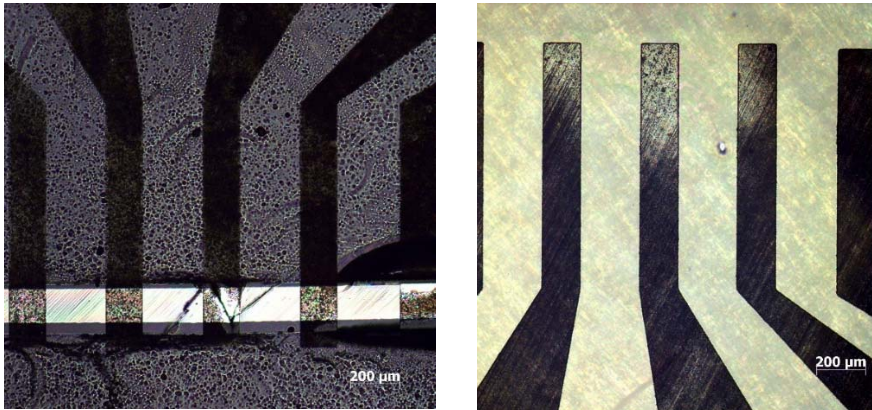


Figure 3.13: *Left)* Development of 4PP pattern on Epoxofix Epoxy *Right)* Development of 4PP pattern on Epoxobond 110 Epoxy. Note the stark contrast between the quality of patterns on the two surfaces.

3.2.4.1. Lithography Procedure FOS Samples

Starting from a planar polished FOS sample. Firstly, the sample was cleaned with 96% Ethanol, rinsed in DI H_2O, and dried using compressed air. The sample was then vacuum mounted onto a spin coater. Approximately 2mL (2 drops) of Shipley SPR 700.1 DQN Positive Photoresist was added to the sample surface using a micro-pipette. Table 3.2 is a recipe designed to for lithography of planar FOS samples.

Table 3.2: Lithography ‘recipe’ for 4PP and Hall patterning of planar FOS samples

Resist	Shipley SPR 700.1
Spin	• RPM: 2000 • Time: 30 sec • Acceleration: 1000RPM/sec^2
Soft Bake	• 95°C for 60 sec*
Exposure (MA6 Aligner)	• Soft exposure mode • E_s of ~220 mJ/cm^2* • Exposure time 40-60 sec (Hg lamp output decreases with time)
Developing (MF-26A)	• Develop for 65 sec in agitated solution at room temperature • Rinse DI water/Dry with compressed N_2

*Soft bake and E_s information given in product sheet for Shipley SPR700[46]

A post-development bake (hardbaking) is usually done for DQN resists to improve durability and adhesion to substrate, typically required for reactive ion etching and other wet etches [41]. This process was not done during the production as hardbaking decreases the solubility of the photoresist in organic solvents, which is used in the NTNU Nanolab for resist removal. Depositions were made using the AJA Sputter Coater and Evaporator. Ag, Cr, and Al were sputtered rather than evaporated due to improved step coverage of sputtering over evaporation. Adhesion of the metal contacts on the epoxy surface was issue throughout the development of the lithography procedure. Silver was originally chosen based on its use in the PV industry as contacts to n-type silicon. However, it was found that depositions made with Ag suffered from adhesion issues. Silver provided almost no adhesion to Epoxofix epoxy, most likely caused by the quality of the epoxy surface. However, proved much more useful on Epoxobond resin. The main issue with Ag arose during the lift-off procedure as inspection of the Ag layer before lift-off showed sufficient uniformity and coverage. An ethanol/IPA solution was substituted for commonly used acetone as a solvent to remove the photoresist after metal deposition. Tests showed the structure of the cured epoxy was attacked and weakened over long exposure to acetone but fared much better in exposure to ethanol and IPA. Lift-off required the use of an ultra-sonic bath to prompt removal of photoresist. Tests on

epoxy alone showed Ag provided sufficient adhesion on epoxy. However, even a low intensity ultra-sonic bath had a high probability of removing the silver film near the fibre on FOS samples. It was determined that silver adhesion to the SiO_2 cladding was the main cause of failed samples. It was also noted that even if the lift-off procedure was successful, exposure to the surrounding atmosphere caused the film to flake off. Figure 3.14 shows an image of an FOS sample after lift-off with removal of Ag film on the cladding.

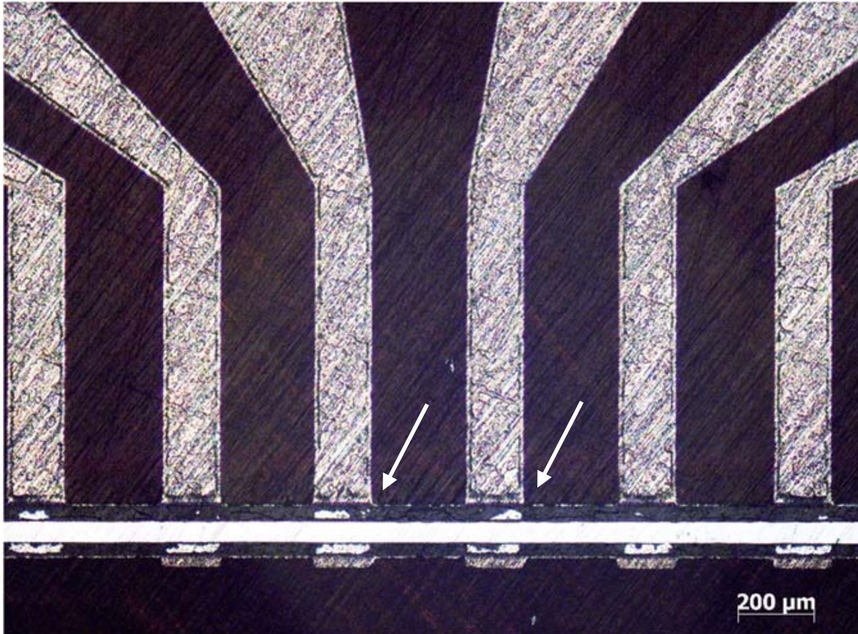


Figure 3.14: Ag pattern on O212 FOS sample after low intensity US lift-off in Ethanol. The Ag layer has been removed from the contact near the fibre.

Reparation of the patterns fingers is possible by applying small drops of silver paste using a precision applicator: a small piece of facial hair glued to the end of a tooth pick. However, it is undesirable due the precision of applying relatively large amounts of Ag around small features.

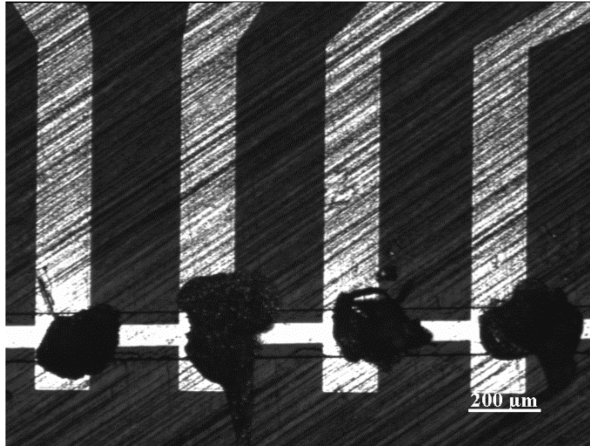


Figure 3.15: Repaired O212 FOS sample with silver paste added to bridge the contact leads with the fibre core.

Depositions with chromium were also attempted but failed as well due to adhesion issues on epoxy. Aluminium was chosen based on its superior adhesion qualities to most materials. Aluminium is highly reactive, which most likely plays a role in its adhesion to the epoxy. Depositions substituting Al for Ag were successful. The figures below are optical microscopy images of FOS samples deposited with Al after lift-off.

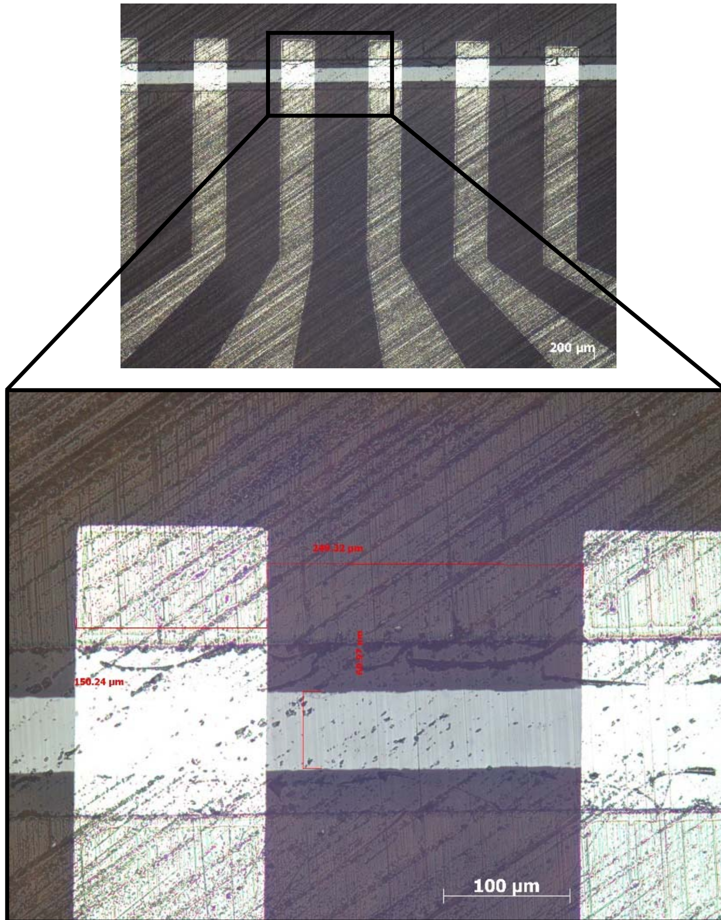


Figure 3.16: O212 FOS sample after lift-off in ethanol.

3.2.4.2. Lithography EFOG

Lithography was performed on EFOG samples to test its suitability for Hall contact measurements and as an alternative method for 4PP contacts on planar FOS samples. Using lithography to pattern photoresist on EFOG samples provided a considerable challenge. The surface consisted of a full fibre core mounted on a glass substrate: feature size equal to approximately the core diameter, which can exceed 80µm. As a general rule, the resist thickness should match the surface roughness: i.e. producing 80µm thick resist layer. Although achievable, this would take

considerable time, effort, and increase the number of steps, heightening the chance of failure.

Approximately, a 10µm layer of AZ4562 positive photoresist was applied to the EFOG samples by spin-coating. The matching developer for this specific resist is AZ351B, an orthoboric acid and sodium salt based developer mixed in a 1:4 ratio with DI H_2O. It was found to produce sufficient coverage over the fibre due the surface tension of the liquid resist; the main requirement for successful contact pattern is a thin layer of resist protecting the fibre. The profile of resist required an extremely large exposure dose due to a build-up of resist near the fibre. The profile illustrating the difference in thickness of photoresist over the EFOG sample is shown in Figure 3.17.

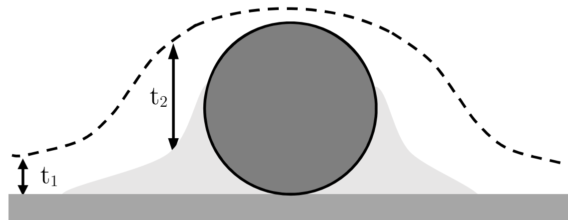


Figure 3.17: Resist profile over EFOG sample

Through trial and error, an exposure of ~3200 mJ/cm^2 was sufficient to expose the entire resist layer. It is important to note that this value is highly dependent on the resist thickness, which is dependent on the diameter of the fibre and spin RPM: 3200 mJ/cm^2 was sufficient on an EFOG sample with a core diameter of ~180 µm and 2000 spin RPM. An example of inadequate exposure of resist, leaving resist scum on the sample after development is shown in Figure 3.18.

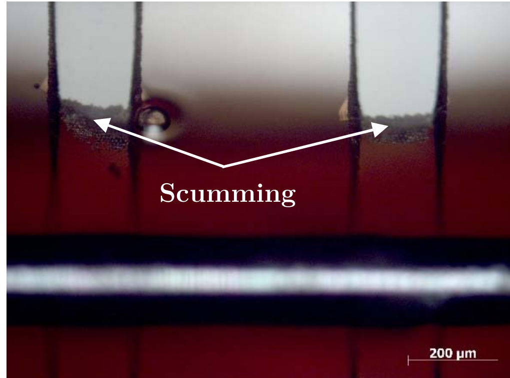


Figure 3.18: Resist scumming on developed EFOG sample indicating unexposed resist.

The recipe below illustrates the parameters used for patterning a fibre sample with a diameter of ~180µm, produced according to the EFOG method. Some of the information in was retrieved from AZ 4500 series product sheet [47].

Table 3.3: Lithography 'recipe' for 4PP and Hall patterning of EFOG samples.

Resist	AZ 4562
Spin	• RPM: 2000 • Time: 20 sec • Acceleration: 1000RPM/sec^2
Dry	• Let dry in atmosphere for ~5min
Soft Bake	• 100°C for 55 sec
Exposure (MA6 Aligner)	• Soft exposure mode • E_s of ~3000 mJ/cm^2**
Developing (AZ351B 1:4 H_2O)	• Develop for ~120 sec in agitated solution at room temperature • Rinse thoroughly with DI H_2O/Dry with compressed N_2

*Highly dependent on resist thickness, longer exposure times necessary for thicker fibres

Figure 3.19 displays images of successful lithography development on EFOG samples. The dark regions surrounding the fibre on the pattern fingers are epoxy.

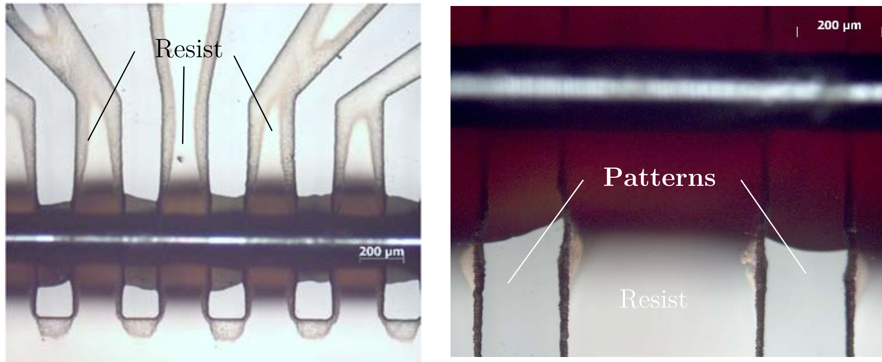


Figure 3.19: Examples of successful development on EFOG samples (note the difference with Figure 3.18)

3.2.5. Deposition

It was necessary to prepare fibre and bulk material samples for comparison. Depositions of all electrical contacts performed using the AJA Sputter + Evaporator in NTNU's Nanolab, shown in Figure 3.20.

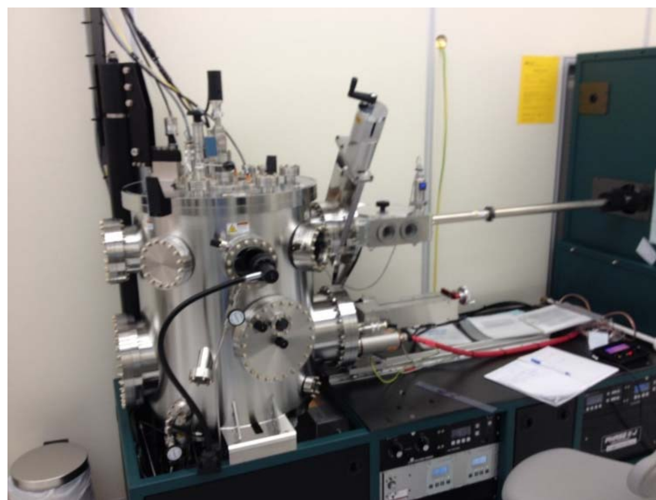


Figure 3.20: AJA Sputter and Evaporator used for depositing contacts

3.2.5.1. Evaporation

In order to create electrical contacts to measure the fibre via 4PP pattern shadowing mask was placed overtop the EFOG sample secured to a substrate holder. The holder was then loaded into the vacuum chamber of the AJA apparatus and pumped down to approx. 10^{-7} torr. Once the parameters were set, the evaporation process was automatically controlled. The e-beam evaporation of Al used a pre-set ‘recipe’ that consisted of heating, ramping, depositing, and cooling stages. The parameters used during the deposition stage were 8.90 kV and 260 mA, resulting in an average deposition rate of 2.0 Å/sec. The AJA system was set to deposit 200 nm Al. The sample stage was set to rotate during the deposition. The shadow mask used for evaporation and a completed EFOG sample are shown in Figure 3.21.

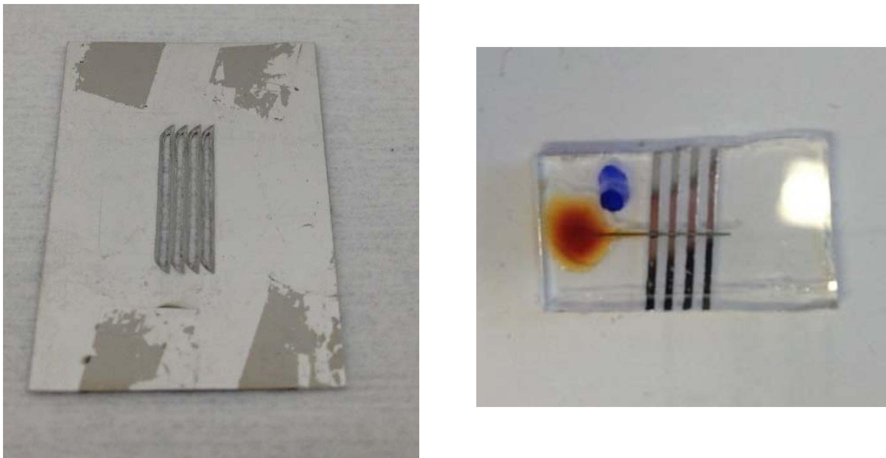


Figure 3.21: *Left)* Shadow mask used for evaporation. *Right)* EFOG sample after e-beam evaporation of Al.

The electrode spacing and fibre diameter were retrieved after deposition by analysing the sample using an optical microscope. Figure 3.22 is an optical microscopy image of an O212 EFOG sample after contact deposition with important dimensions.

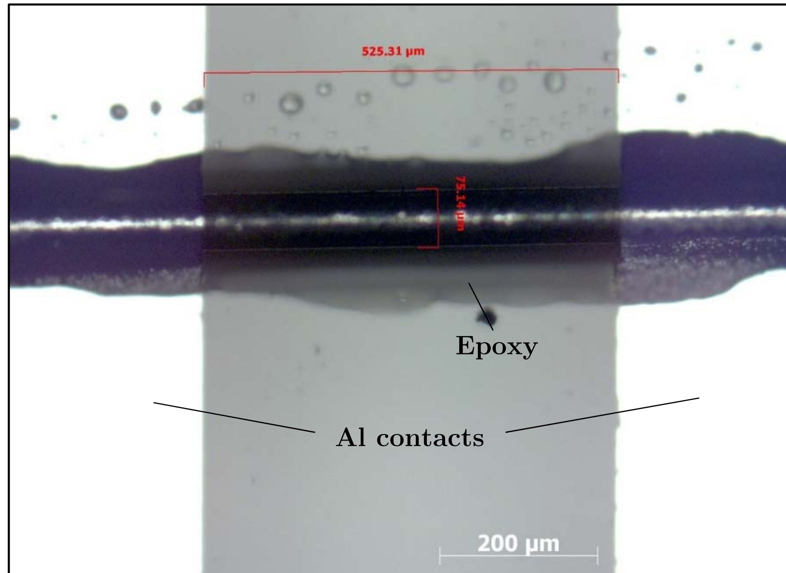


Figure 3.22: Optical microscope image of finished EFOG (O212) sample.

It is important to confirm the fibre is both showing and in contact with deposited Al contacts. Figure 3.23 contains SEM images showing deposited aluminium contacts on an EFOG sample after measuring the conductivity of the fibre with the 4PP (probe marks present in image).

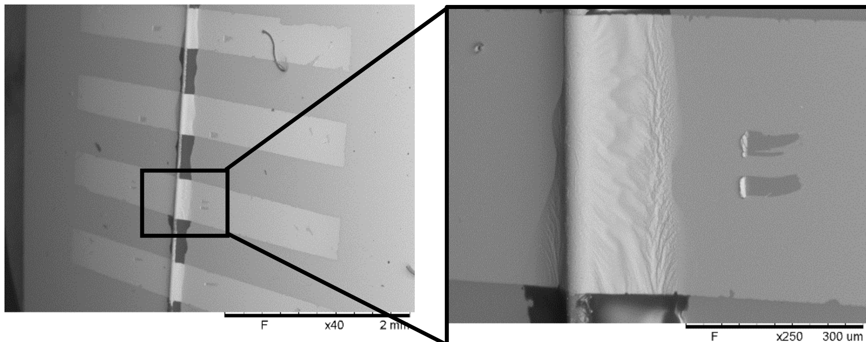


Figure 3.23: SEM images showing deposited Al contacts overtop of an EFOG sample.

3.2.5.2. Sputtering

Sputtering was used to deposit a conductive layer onto FOS and EFOG samples prepared with lithography. The sample was loaded into the AJA system in similar fashion as the e-beam evaporation procedure but without attaching the shadowing mask. The plasma was struck at 30 mtorr argon pressure and 150W DC power. Once the plasma stabilized, the argon pressure was reduced to 3 mtorr Argon pressure and 250W for deposition. After waiting approximately 1 minute, the shutter shielding the sample was opened to begin the deposition process. The parameters produced an average rate of ~5Å/s to deposit a 200nm layer of Al; the sample was rotating during sputtering. Following the deposition, the photoresist was removed by putting the coated sample in low intensity ultra-sonic bath of ethanol for approximately 3 minutes. The lift-off process is relatively fast for thick films of resist. Figure 3.24 displays successful sputter depositions on FOS and EFOG samples using lithography techniques to produce.

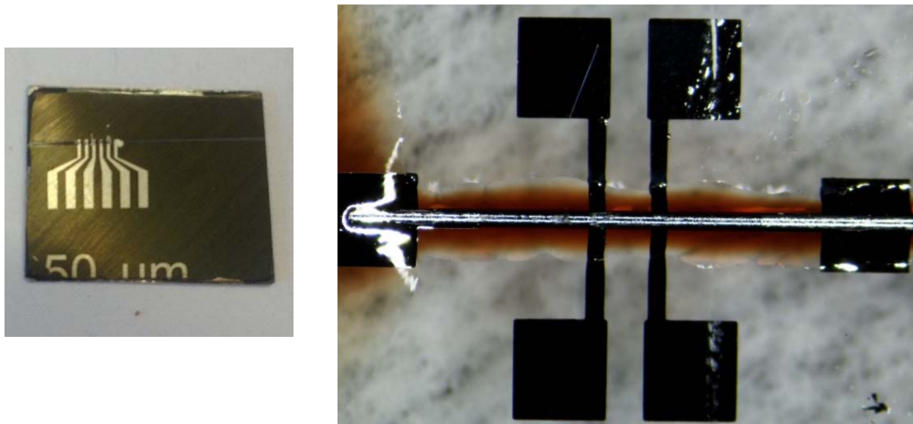


Figure 3.24: *Left)* Successful lift-off of 4PP pattern on FOS sample. *Right)* Successful lift-off of Hall pattern on EFOG sample.

Tests with sputtering lead to uniformity issues with depositions as the mask extends relatively far above the surface of the sample (~1mm). The patterns broaden considerably due to the non-directionality of the sputter process: See Figure 3.25.

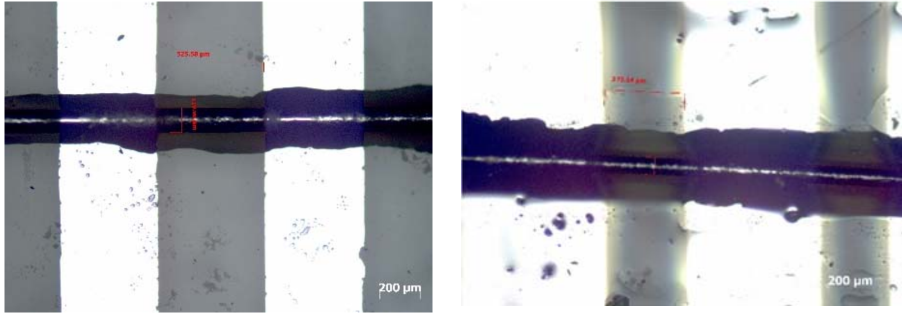


Figure 3.25: *Left)* OM image of 4PP contact patterned with Al using e-beam. *Right)* OM image of 4PP contact patterned with Al using sputtering. The pattern caused a short circuit during measurement.

3.3. Sample Measurement

3.3.1. 4PP

The power source used for the 4PP measurements is limited by its ability to produce a source current and measure a voltage. This data is given by the manufacturer Kiethley and is quoted to be:

Table 3.4: I/O specifications for Kiethley 2420 power supply

Source Current	5.00pA-3.15A
Measure Voltage	1.00µV-63.3V
Source Voltage	5.00µV to 63.0V
Measure Current	100pA to 3.17A

In practice, the minimum step size for a current sweep is 1µA using the Solview. Solview is a Labview program designed for the automatic control of the Kiethley power supply. Preferably, at least 10 measurements should be recorded on a current sweep to reduce uncertainty in the I-V slope. For example, the J895 material was quoted to have a bulk resistivity, $\rho_o > 5000\ \Omega cm$. For an average fibre with a 200µm diameter with a J895 core (assuming there has been negligible change in

resistivity during fabrication), the estimated contact spacing is calculated to be ~120µm in order to allow measurement by the Kiethley source.

3.3.1.1. Bulk Samples

Sample surfaces was cleaned prior to 4PP measurement with laboratory grade ethanol, rinsed with IPA, and dried using compressed air. The exact parameters used varied with material type but for low resistivity materials D429 and O212, the current sweep ranged from -1mA to + 1mA, with step size of 0.1mA. A lower range of -10µA to +10µA, with a step size of 1µA was used for high resistivity materials (E944, J895 and 3169). However, the 3169 cores were intrinsic silicon with a substantially high resistivity (>140000 Ωcm), and produced inconsistent results. The Kiethley power supply was unable to produce measurements within its own limitations.

3.3.1.2. Fibre Samples

The 4PP head was switched out for a custom built head with 1.01 mm probe spacing to match the spacing distance in the physical mask. Combined with the custom made shadowing masks, the actual contact spacing was reduced to 520-570 µm. The range exists due to variation in the relative placement between the shadowing mask and the fibre sample.

Solview contains the option to perform a sweep measurement, taking user input for the start current, end current, and current step size. This option didn't contribute many problems when measuring the bulk samples as the cross sections were relatively large, reducing the voltage for a given current. The fibres varied in resistivity and diameter providing difficulty when measuring; the current sweep mode was limited to a maximum ±2.0 V. The program allowed for a voltage sweep mode raising the limit to ±41 V but results were relatively inconsistent and as there was no current limitation allowed for the possibility of overheating the 4PP electrodes (within the power supplies operating limits). Thus for consistency and

only the current sweep function was used to measure fibres, while performing some tests using the voltage sweep mode. Rarely was it that 2 subsequent fibres produced the same results under the same measuring parameters. However, it was clear that the contacts produced an Ohmic relationship due to the high degree of linearity of current and voltage. Thus the limits of the current sweep were adjusted until the sweep produced a linear relationship over the largest range of current, usually however, it was limited to ±100 µA.

The fibres small dimensions raises the issue of possible current constriction. For metallic contacts made on EFOG samples approximate contact area was 0.02 mm^2 per lead for a fibre with a diameter of 100 µm. The resistance for electrical constriction, R_c of a rectangular area was found experimentally and estimated by the equation [48]:

$$R_c = k\left(\frac{\rho_1 + \rho_2}{S^{0.63}}\right) \tag{3.3}$$

Where $\rho_{1/2}$ is the resistivity of the contact materials expressed in Ωmm, k is a parameter depending on the width of constriction (~0.5), S is the rectangular area in mm^2. Assuming that the fibres resistivity is unchanged from their bulk, and taking the highest resistivity sample, J895 leads to an additional constriction resistance of ~2.5 kΩ for a contact area of 0.02 mm^2. As a comparison, the total measured resistance for a fibre with given dimensions and resistivity would be ~3 MΩ, negating the effect of constriction. The surface of the fibre cores were rough, providing an increased surface area relatively to a smooth cylinder. Through the course of experimentation, it was found that Al contacts produced reproducible Ohmic contacts with the silicon fibre samples while also providing good adhesion to the sample surface.

3.3.2. SEM-EDS

Over the course of project, it was necessary to compare the compositional distribution of the fibres to those previously characterized by Dibbs in order to determine if the quality of the fibres produced were consistent. EDS is a fast and

simple process that produced relatively good qualitative information about the compositional distribution. EDS was completed using a Hitachi TM3000 “table top” SEM with installed back scattered electron (BSE) and EDS detectors. Prior to the analysis the samples were coated with approximately 15nm of carbon using a Cressington 208 Carbon Coater as the samples was on a non-conducting glass substrate. The same preparation procedure was used for SEM imaging. Samples were loaded into the table top SEM and the chamber was pumped down to a reasonable vacuum. Proprietary software provided by Hitachi was used for imaging and EDS analysis.

3.3.3. Anisotropic Etching

The electrical and mechanical properties of a material are sensitive to changes in grain structure. EFOG samples were prepared by lightly polishing the surface with a P4000 grit SiC grinding paper to reveal a planar surface. Once a planar surface was established, the sample was moved to an Fischione Tripod auto-polisher and polished down in sequence with 2µm, 1 µm, 0.5µm, finishing with 0.1µm fine polishing paper. This fine polishing step removed most of the visible scratches under 60X magnification. A combination of KOH, H_2O, and IPA in a 23:63:14 mixture was prepared and heated to 60°C. This etchant mixture is commonly used for anisotropic etching of silicon in the MEMS industry [41]. The key mechanism is the dangling bonds in each crystal plane. The (111) plane is close packed leaving only 1 dangling bond causing the etch rate to be extremely slow. Other planes such as (100) and (110) are more corrugated leaving more open bonds and thus, showing higher etch rates [49]. The sample was placed in the etchant for 2 minutes while gently stirring. Small bubbles of $H_2(g)$ immediately formed at the surface indicating the etching reaction is taking place. After removing the sample from the etchant, it was thoroughly rinsed with DI water and dried with compressed air. Afterwards the sample surfaces were examined using an optical microscope. A table showing etch rates of select crystal planes are given in Table 3.5.

Table 3.5: KOH Etch rates of select crystallographic planes of silicon [49]

Crystallographic Orientation	Etch Rate (~30% KOH) [$\mu m\ min^{-1}$]
(100)	0.797
(111)	0.005
(110)	1.455
(210)	1.561

4. Results

4.1. 4PP

This section provides results from the bulk material and fibres obtained using the 4PP technique to measure resistivity. More information on error calculation can be found in Appendix A.2.

4.1.1. Bulk Samples

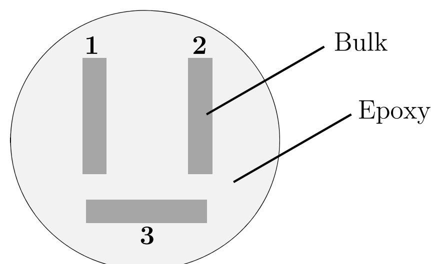


Figure 4.1: Layout of bulk core samples in epoxy

4PP measurements of the bulk samples generally showed a close correlation with the manufacturers provided data. Figure 4.2 displays an I-V curve from a 4PP measurement of the E944 silicon core, representative of the Ohmic I-V relationship produced by non-intrinsic cores. Results from all the core types are tabulated in Table 4.1 including an estimate of uncertainty for the result. Each sample consisted of 3 cores, each core was measured 3 times, creating a total of 9 measurements per material.

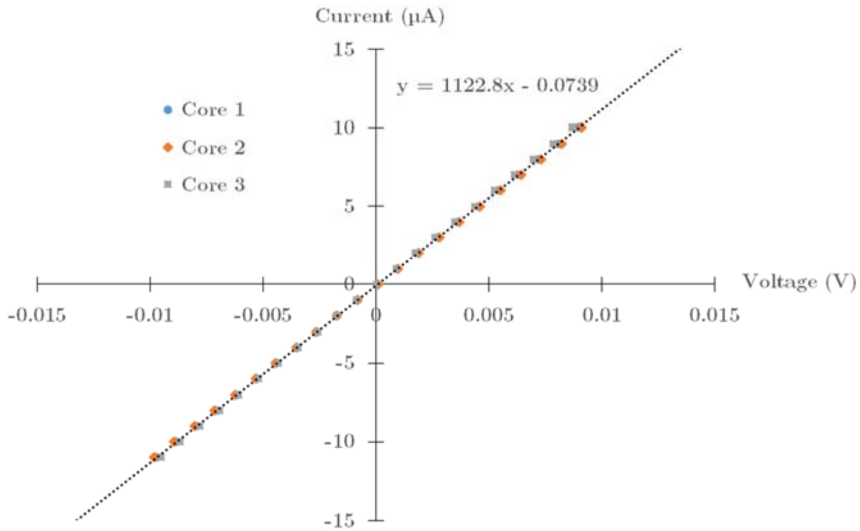


Figure 4.2: IV curve for E944 bulk cores' 1, 2, and 3.

Table 4.1: 4PP results of bulk core measurements for all silicon types.

	D429 Si:P	O212 Si:P	E944 Si:P	J895 Si:P	3169 Si:i
Reported Bulk Resistivity [Ωcm]	0.130-0.145	15-22	266-336	>4800	>20 000
Measured Bulk Resistivity [Ωcm]	0.13	35	373	4310	136 000
Uncertainty [±Ωcm]	0.05	5.2	30	390	11 000
Number of samples measured	3	3	3	3	2
Standard Deviation	0.01	2.1	8.1	156	2200

The high resistivity samples proved difficult to measure and produced inconsistent I-V relationships. The 4PP results did not show an ideal linear relationship between current and voltage but rather distinct sections with a linear relationship at small voltages. The 3169 sample showed very similar IV relationship above ±0.2V, producing the exact same slope in the positive and negative regions of the I-V graph. Figure 4.3 shows the 4PP results for the intrinsic 3169 cores 2 and 3 with extrapolated trend line to illustrate the matching I-V slope; core 1 fractured during

sample preparation such that it could not be measured. The measured slope of 3169 was within range of resistivity of intrinsic silicon well reported in literature [2].

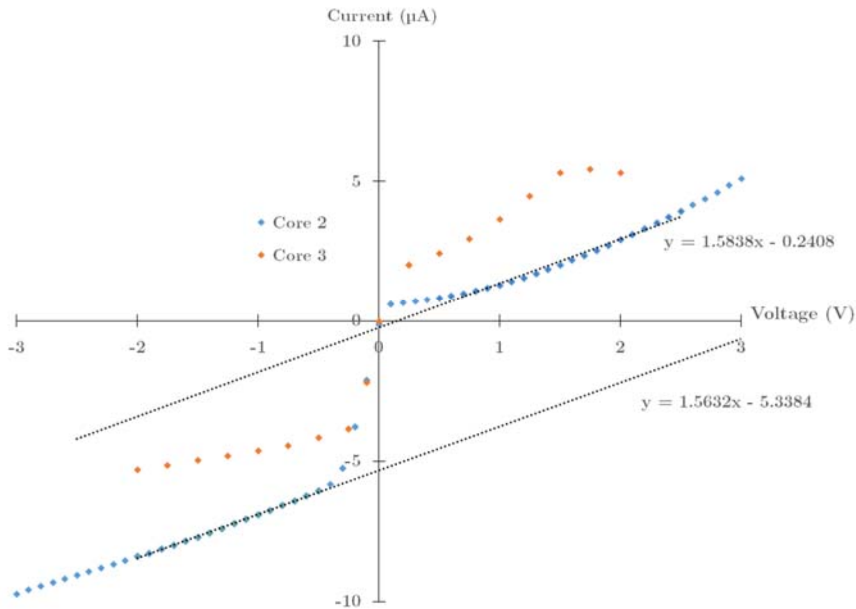


Figure 4.3: 4PP results of intrinsic 3169 bulk material.

4.1.2. Fibre Samples

The fibres proved to be less problematic to measure than hypothesized. Generally, the fibres showed a large decline in resistivity, except material D429, which showed a slight increase. The FOS method for sample preparation produced usable samples that gave identical 4PP results to those produced using EFOG and shadowing mask. Due to time constraints, only one FOS sample was tested. Table 4.2 summarizes the 4PP results of fibre samples, while Figure 4.4 compares the 4PP results of fibres to the starting, bulk material.

Table 4.2: 4PP results from EFOG and FOS fibre samples.

	D429 Si:P	O212 Si:P	E944 Si:P	J895 Si:P	3169 Si:i
Measured Fiber Resistivity [Ωcm]	**0.27**	**11.1**	**11.8**	**270**	**>10 000**
Uncertainty [±Ωcm]	0.13	4.4	5.2	31.0	-
Number of fibres measured	4	5	4	4	3
Standard Deviation	0.06	2.4	2.9	19.0	-
Change from bulk	+107.7%	-68.3%	-96.8%	-93.7%	-

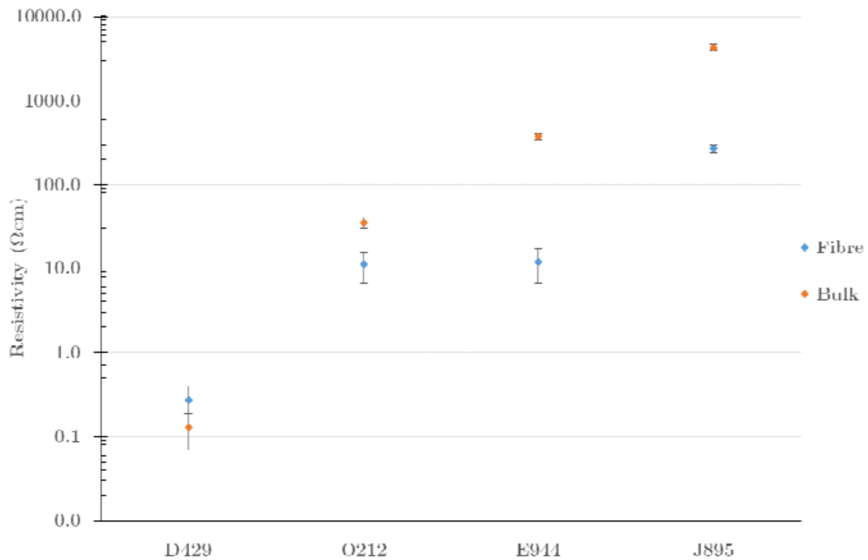


Figure 4.4: Bulk resistivity results plotted against fibre resistivity for doped samples on $\log_{10}$ scale.

The J895 sample had the largest initial resistivity of the n-type materials. Measurements varied in behaviour between samples. Two of the 4 samples showed a discontinuity in I-V near the origin but yielded the same I-V slope on either side of the discontinuity. These slopes were used in the calculation of resistivity. Figure 4.5 shows the I-V behaviour of 2 J895 samples one continuous at the interface, while

the other shows a discontinuity. The difference in the apparent slopes between the fibres is due to dimensional variance.

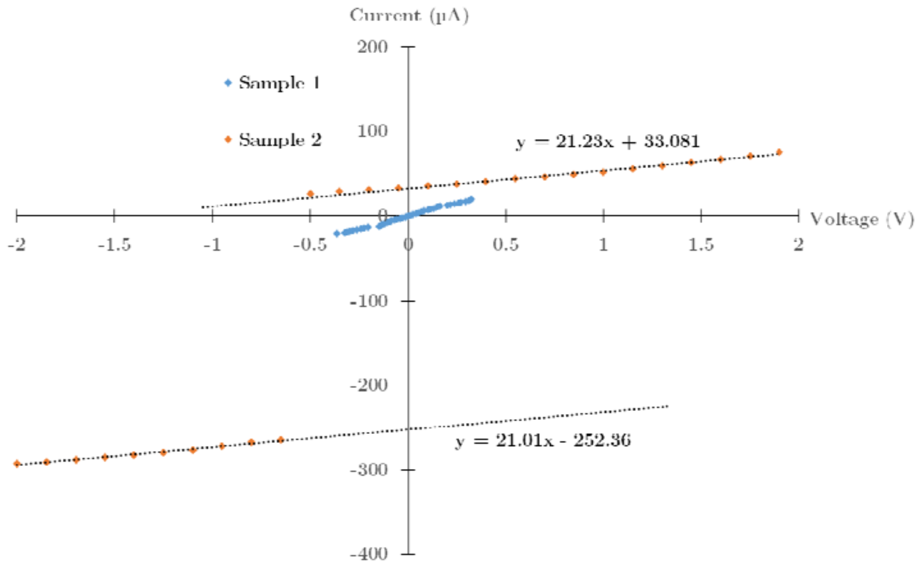


Figure 4.5: 4PP results from EFOG J895 sample 1 and 2 illustrating the discontinuity in I-V in sample 2.

Measurement of material 3169 showed a formation of Schottky contact. Interestingly, it showed a significant photosensitive response further suggesting the formation of a Schottky contact between the Al contacts and the Si fibre. Results from a 4PP current sweep of a 3169 fibre is shown in Figure 4.6. A test of photosensitivity was performed by exposing the sample for the light emitted by an iPhone4S LED flash during a negative bias voltage sweep and shown in Figure 4.7.

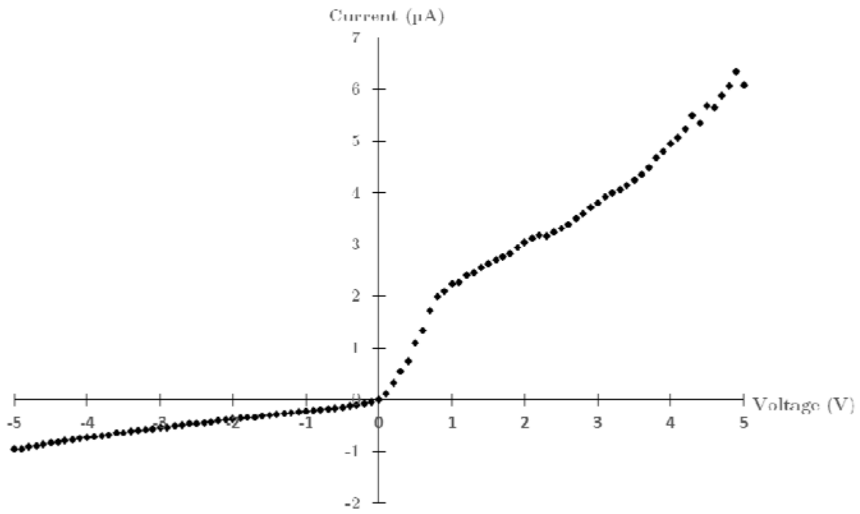


Figure 4.6: Current sweep on 3169 EFOG sample illustrating Schottky style curve

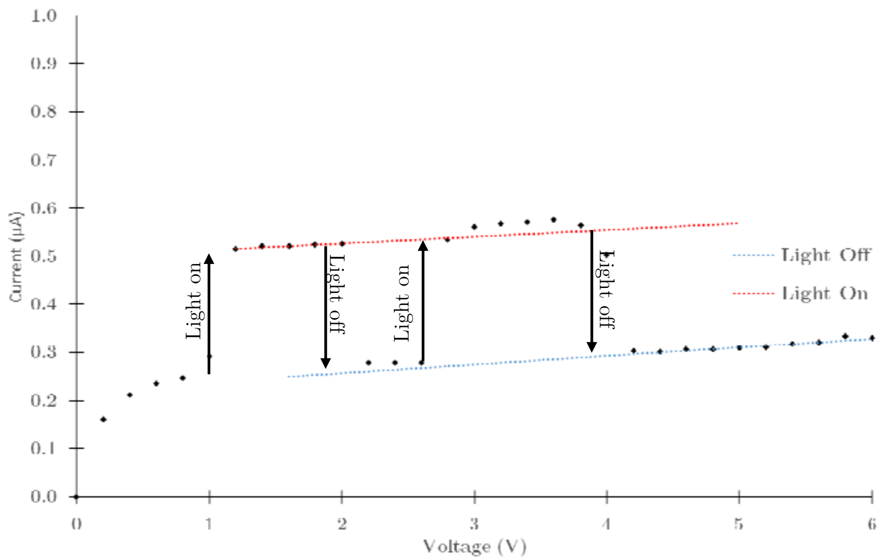


Figure 4.7: Voltage sweep on 3169 EFOG sample illustrating photosensitivity. The lighting test was performed in situ and shows one data set.

4.2. KOH Etching

As grain structure has a strong effect on materials electrical properties. Etching of planar samples with a KOH solution produced a definitive grain structure on the surface. The immediate contrast between grain sections appeared rather quickly, appearing only after a minute of etching in an agitated solution. Samples were left in the etchant for 2 to 3 minutes determining the completeness of the etch by inspecting the results in an optical microscope. In general, the images show very large grains, suggesting high crystallinity. There was no significant difference in grain structure between the types of core used to pull. Optical microscopy images of the etched fibres are displayed in Figure 4.8.

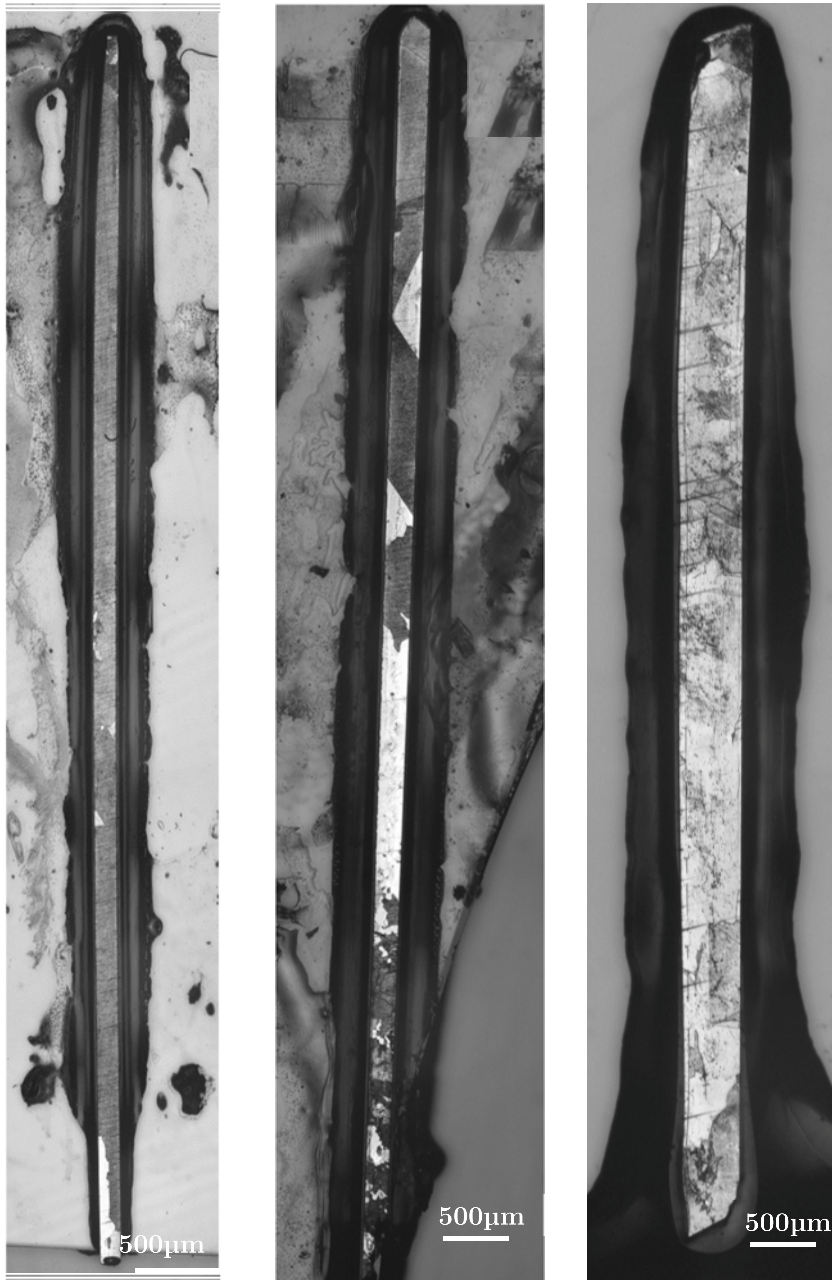


Figure 4.8: *a)* Optical micrograph of EFOG D429 *b)* Optical micrograph of EFOG J895 *c)* Optical micrograph of EFOG 3169. All samples etched with KOH solution for 2 minutes revealing grain structure.

4.3. SEM-EDS Imaging

As this work is similar and a continuation of previous results achieved by Nordstrand. A comparison of these fibres was carried out to those previously pulled by Nordstrand to ensure similar structure and composition. An interfacial layer between the Si core and cladding is apparent and measured to be approximately 4µm in thickness. The interfacial layer is composed mainly of Ca and O. Mapping of aluminium showed a noticeable difference of presence in the core and in the cladding indicating the concentration is above the detection limits of the EDS detector. BSE and EDS results showing elemental distributions in the core of a planar FOS sample are compiled in Figure 4.11. The surface of a fibre core on an EFOG sample is displayed in Figure 4.9 and Figure 4.10.

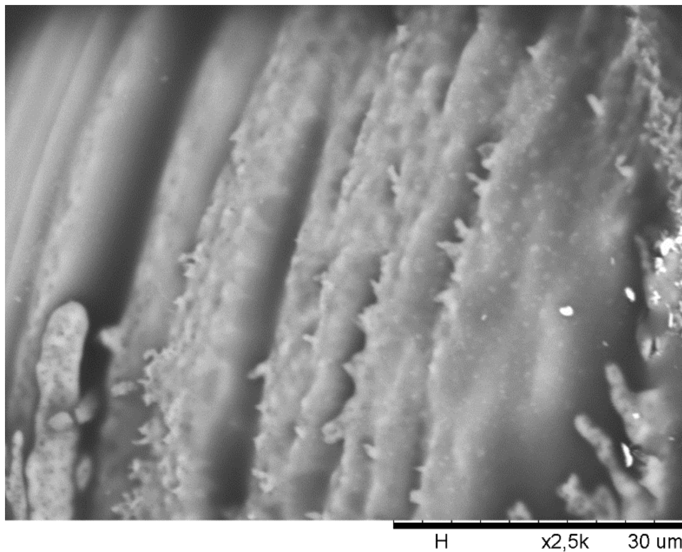


Figure 4.9: SEM image of J895 fibre core surface showing rough and highly irregular surface features.

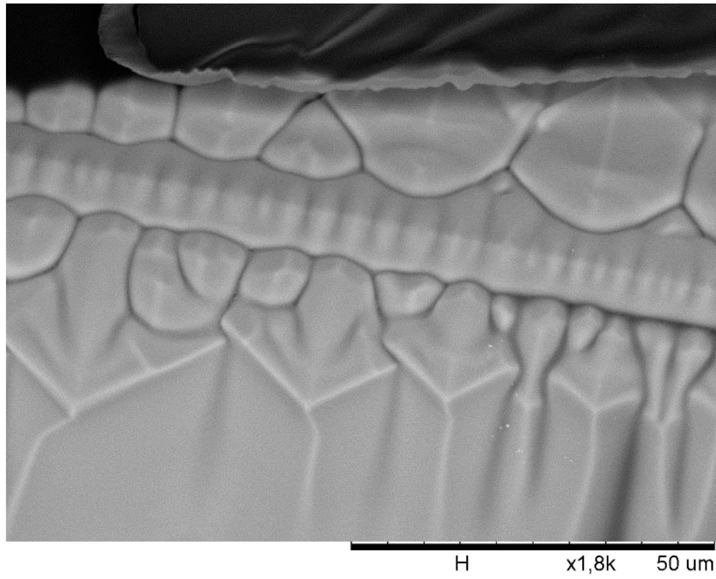


Figure 4.10: SEM image of the longitudinal face of J895 fibre core surface showing smooth dendritic features.

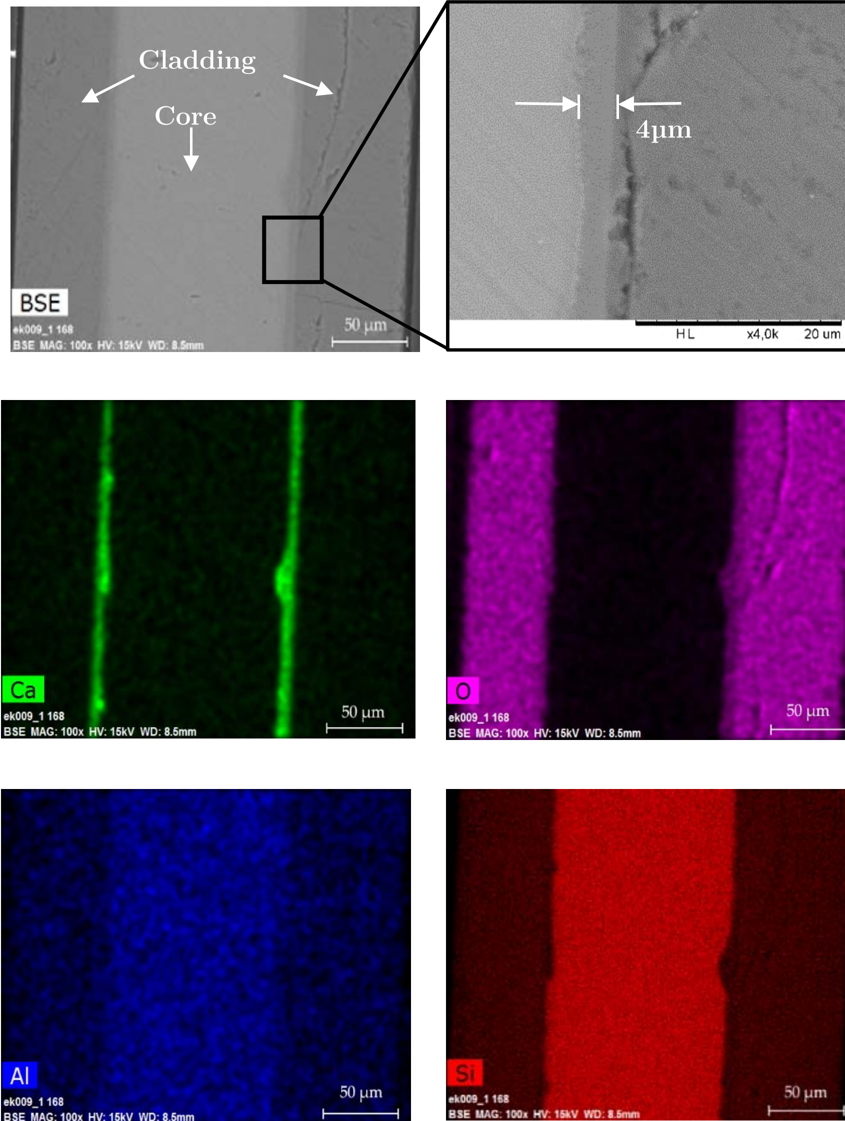


Figure 4.11: SEM-EDS results from O212 FOS fibre highlighting Ca, O, Al, and Si distribution

5. Discussion

5.1. Coating & Fibre Drawing

The CaO coatings on the inside surface of the quartz tubes closely resemble coatings made by Dibbs [29]. It was discovered that CaO powder depreciates over long periods (~6 months), reacting with CO_2 and H_2O in the atmosphere to form unwanted contaminant. The poor quality was noticed quickly as the solution did not produce heat when mixed: eq. (3.1) is exothermic. In addition, the coating was uneven and had agglomerated into large pieces inside the quartz tube after coating further signifying the presence of $CaCO_3$ as it is insoluble in water. A new batch of high-grade CaO powder was ordered and stored in a N_2 filled container to remedy the problem. To reduce exposure of CaO to CO_2, large batches of coatings were prepared to limit the opening of the container. The CaO powder stored in N_2 environment was found to produce good quality coatings after months of storage.

Fibres proved very fragile after etching away the silica cladding. It was quite common for fibres to spontaneously fracture during etching. This indicated that there most likely exists large residual stresses inside the core after pulling. Thermal mismatch between the silicon core and the glass cladding has been well documented to be a major issue in the production of silicon core fibres. Unwanted effects such as fracturing and interfacial imperfections that leads to high attenuation in optical fibres are common [8, 50]. The CaO interface modifier has certainly increased the integrity of the core, yet there still exists significant stresses. The inherent nature of manually drawing the fibres causes reproducibility issues as it is impossible to precisely control the fibre diameter. Variations in the draw speed and angle may account for additional residual stress at the core-cladding interface. Changes in fibre thickness will alter the surface area to volume ratio, which create gradients in stress during solidification. A custom-designed, small scale fibre drawing machine, similar to fibre towers used to commercially produce fibres was built, although time constraints limited the ability to employ it to draw fibres. The drawing machine controls the pull speed, acceleration, and angle to theoretically improve fibre

consistency between pulls. More information on the machine is included in Appendix A.1. Dibbs reported a significant difference in surface roughness of the core for manually drawn fibres and those drawn using a commercial fibre tower [29]. Figure 4.9 and Figure 4.10 show SEM images of the core surface from the same fibre. Dendritic features indicate a fast and unstable solidification front, which is expected from the high cooling rates. The difference in images highlight the large variation in cooling rates and the need to employ a more consistent method to draw fibres.

5.2. Sample Preparation

The FOS planarization process also proved to be success. Fibre surfaces were ground to an adjustable depth with reasonable precision of ±5 µm allowing characterization and contact deposition on planar surfaces. At this stage of preparation, both Epoxofix and Epoxobond 110 type epoxies worked well. Epoxofix epoxy is transparent when cured allowing an easier observation of depth versus the dark red colour of Epoxobond, however this was never a significant issue. Noticeable stresses occurred when using larger amounts of Epoxobond to secure the fibre, bending the substrate in some cases. This made it difficult to achieve an even plane and increased the likelihood of fracturing the core during grinding. Reducing the amount of epoxy used decreased the stress formed by thermal contraction of the epoxy.

Lithography proved to be a suitable technique to make deposition masks on both planar surfaces and surfaces with large features (i.e. EFOG samples). It demonstrated to be a versatile method that is suitable on glass, silicon, and epoxy. Despite this success, it also showed to be very sensitive to the surface quality. The curing process of Epoxofix epoxy produced voids within the bulk of the epoxy, sometimes large enough to botch the entire sample preparation process. Although the resist more or less conformed around these small voids, the chances of failures were heightened due to an uneven distribution of resist after the spin on process: see Figure 3.13. Moreover, PVD of Al, Ag, and Cr were much more likely to fail due to poor adhesion and film distribution over the surface voids. 110 Epoxobond heat curing epoxy provided a much more uniform surface that eliminated most

problems with resist homogeneity and poor PVD film distribution. Al proved superior to other PVD films attempted in terms of overall adhesive characteristics. Both Ag and Cr showed similar qualities on epoxy surface, but were easily removed during the lift-off process, specifically overtop of the fibre cladding: see Figure 3.14. This was an odd behaviour for Cr as it is a common material to manufacture optical lithography masks, which are usually Cr on quartz glass. Although only one Cr sample was tested and the sample preparation may have been responsible for the adhesion failure.

Using lithography to create 4PP and hall patterns on EFOG samples was a large success. Initially it was thought that the large diameter of an EFOG sample would be too extreme and outside the limitations of the process. Nevertheless, a combination of viscous photoresist and large exposure times reliably produced patterns on EFOG cores with diameters >100 µm. It is important to note that there is an upper limit to the size of core that can be patterned. Fresnel diffraction of light through the photomask will broadens the features. In addition, the required exposure time rises exponentially with resist thickness. Although theoretically a gap of 1-2 mm should be possible (based on the photomasks used), the upper limit to the size is estimated to be ~300 µm due to practical issues with the mask aligner. Fresnel diffraction predicts that a gap of 300 µm will widen features ~25 µm: i.e. a vertical gap of 300 µm between the mask and substrate cause 50 µm features to expand to ~75 µm. The minimum feature sizes in the photomasks are 50 µm. Although deposition of Hall contacts were successful, time constraints and apparatus availability limited the ability to perform Hall measurements.

5.3. 4PP

Aluminium contacts produced excellent I-V linearity for samples E944, D429, and O212 indicating high quality Ohmic contacts. Current sweeps ranged from ±100 µA for E944, D429, O212, and J895 fibres made using the EFOG method and produced a linear I-V relationship with a regression R^2 value equal to ~1. This correlated much nicer than was previously expected. Initial attempts at measuring the resistivity of fibres inconsistent and even gave contrasting results. The issue

was narrowed down to the EFOG preparation method and the method was subsequently adjusted. The early method involved gently placing an etched fibre onto a thin layer of epoxy. Consequently, the fibre occasionally drowned in the epoxy or the epoxy surface caused uniformity issues after curing. Nevertheless, altering the preparation method to use less epoxy in a fashion that made preparation more consistent resulted in more consistent 4PP results.

Measurement of J895 fibres was limited to a current sweep of ±100 µA in order to achieve suitable linearity between I and V. The I-V graph, as seen in Figure 4.5, showed a discontinuity in some of the J895 EFOG samples near the origin. There is an abrupt change in voltage before returning to a stable I-V slope seen on either side of ~-0.2 V. The resistivity of the J895 fibres was calculated based on the stable I-V slope shown on either side of this discontinuity. The resistivity in these areas show relatively similar values and are in agreement across different fibre samples, thus the results were taken as resistivity; the average resistivity of the J895 fibres samples were found to be 250 ±35 Ωcm with a standard deviation of 18 Ωcm. The deviations around the origin were present only on certain samples and fluctuated per measurement, suggesting the cause of the effect was the measurement procedure itself. Furthermore, the same type of discontinuity was shown in bulk material 4PP results, indicating the issue is most likely not in the contacts. Stray voltages or thermoelectric voltages from resistive heating may be a possible cause, as the resistivity of J895 bulk material is relatively high at ~5000 Ωcm. The current sweep started at high currents (±100 µA) and moved in 1 µA steps to the other extreme. To rule out this, the current sweep should be modified to start at the origin. Silicon has a relatively high thermal conductivity and should dissipate heat reasonably well. Despite this, any thermoelectric voltage would be small (on the order of uV) and should be negligible in determining the resistivity. Thermoelectric voltages will affect measurement accuracy [51].

There was generally a large decline of resistivity from bulk material to fibre. The decrease in resistivity is much more pronounced in the higher resistivity J895 and E944 starting materials, which showed a decline of ~95% of the original material resistivity. Likewise, O212 showed a resistivity decline by 68% of its original value. Material D429, the highest conductive starting material appears to show a slight increase in resistivity from 0.13 ± 0.05 Ωcm to 0.27 ± 0.13 Ωcm but cannot be proven to be statistically significant as the confidence intervals overlap. In either

case, D429 seems most unaffected by the fibre drawing process, while J895 shows the largest change. The nature of the inconsistency of the drawing process suggests the possibility of a high degree of variation between measurements. However, this was not the case. In general, measurements in each material class were in close agreement. The standard deviation of data for bulk and fibre measurements are shown in Table 4.1 and Table 4.2, respectively.

Conductivity of semiconductors can be estimated by eq. (2.6) and its proportional to dopant concentration. The decreases in J895, E944, and O212 materials suggests the incorporation of additional dopant elements. There are three reasonable explanations for this decrease. Either n-type impurities, incorporated from the drawing process supplemented the existing phosphorus doping; a relatively large amount of p-type impurities were incorporated compensating the phosphorus and transforming the core material to p-type; or a combination of the two. The most likely source of contamination would be the CaO interfacial coating, which was quoted to be 99.9% pure with trace metals accounting for 200-300 ppm. An obvious solution to verify this would be to test fibres made with higher purity CaO and compare to any. It is important to measure trace impurities using a quantifying spectroscopy technique such as inductively coupled plasma spectroscopy, or secondary ion mass spectroscopy. The detection limitations of EDS cannot quantify trace elements. Correlating the change to an increase in n-type dopants while assuming a negligible addition of p-type elements accounts for an addition of approximately 5-15 ppb. In this case, 15 ppb would have a negligible impact on material D429. By contrast, assuming an incorporation of p-type impurities only would require an addition of 20 ppb for the J895 material to 1 ppm for the D429 at least near the core surface. Both assumptions are in the range of possibility. As it is difficult to control the addition and distribution of impurities, such a case would not be beneficial towards PV applications. Impurities can also act as preferential sites for heterogeneous nucleation, which creates additional grain formation.

KOH etching revealed an outline of some grains, but this should not be taken as the total grain structure of the fibre cores. KOH etching only revels contrast between close packed and other ‘less packed’ planes. Grain sizes in fibres seem to be relatively consistent and in agreement with literature [25, 52]. Grain boundaries represent high energy regions acting as high energy defect sites, which act to

increase resistance in materials by trapping carriers. Assuming the reported resistivity increase in D429 is real, the slight increase from 0.13 Ωcm in bulk material to 0.27 Ωcm could be attributed to measurements across grain boundaries. The standard deviation for D429 fibres were relatively large, contributing to its high uncertainty. More measurements of this material type is needed to increase the certainty of the results.

Measurements of 3169 fibres show a clear Schottky type contact: see Figure 4.6. The current was limited in one direction but unrestricted in the other. The 3169 samples also a photosensitive response under negative bias, raising the current approximately 70% compared to dark conditions, shown in Figure 4.7. The photosensitivity suggests there is an increase in charge carriers caused by the absorption of light. The relatively low powered and diffuse iPhone 4S LED (~5W) rules out intrinsic carrier absorption, suggesting the presence of shallow level impurities. Another possibility for the photosensitive behaviour is the injection of carriers from the metal suggesting a Schottky diode [31]. It is important to note that the starting material 3169 is intrinsic silicon. The Schottky nature of 3169 indicates the variance in contact quality. In order for this to occur, one contact would have to behave Ohmic in nature. Metallic contacts to silicon are well known to be extremely sensitive to many factors such as surface roughness, contact layer thickness, and natural oxide thickness. The fact that the core surfaces vary to such a large degree as seen in Figure 4.9 and Figure 4.10 only adds to probability the possibility of different types of contacts, especially for samples with low doping concentration.

6. Conclusion

The effect of the molten core fibre fabrication method on the resistivity of silicon core fibres have been studied. The silicon core fibres were produced using a CaO interface modifier. Five silicon material types with increasing phosphorus doping levels were analysed before and after the drawing process using 4PP, supplemented with microscopy analysis. Measurement involved the development of novel preparation methods for fibre testing. One method involved using photolithography to create specialized 4PP and Hall patterns on epoxy and the other involved using a PVD shadowing mask. Both methods produced usable results.

Based on the results, there was generally a significant decline in resistivity for most material types, where the largest reduction is found in the lowest doped material, J895. The results show a correlation in resistivity change with the material's initial doping level in the bulk material: (increasing in doping)

- The resistivity of the J895 material dropped from 4310±390 Ωcm (bulk) to 250±35 Ωcm (fibre).
- The resistivity of the E944 material dropped from 373±30 Ωcm (bulk) to 11.8±5.2 Ωcm (fibre).
- The resistivity of the O212 material dropped from 35±5 Ωcm (bulk) to 11.1±4.4 Ωcm (fibre).
- The resistivity of the D429 material increased from 0.13±0.05 Ωcm (bulk) to 0.27±0.13 Ωcm (fibre).

It is believed that the correlation suggests that there is an addition of impurities from the fabrication process, most likely from the CaO interface modifier.

Characterization of the fibre core and cladding by SEM and EDS indicate that the quality and consistency of the fibres closely match those reported by Nordstrand and Dibbs [8]. Although the fibres suggest an increase in conductivity for most doping levels, this is only a first order analysis that does not investigate other important electrical characteristic, such as diffusion length or carrier lifetime, which is of special interest in PV applications.

7. Further Work

The two major achievements in this work has been the development of a practical method for electrical measurements of small fibres and discovering the process used to produce the fibres is quite dirty, meaning it incorporates a lot of impurities in the cores. This conclusions was drawn without any direct measurement of impurities in the core due to time constraints. Also, the results on electrical characterization presented are conclusions based on 4PP measurements. It would be wise to employ additional characterization methods to make a more complete picture of the electrical nature of the fibre cores.

Naturally, continuation of this work should include:

- Analysis of impurities in fibre cores through a quantitative compositional analysis method, such as inductively coupled plasma spectroscopy.
- Use a higher purity CaO (≥99.995%) for interface coatings.
- Perform Hall measurements of fibre cores using the developed photolithography procedure to deposit Hall contacts.
- Use electron beam induced current (EBIC) method to measure diffusion length of carriers.
- Utilize the custom built fibre drawing rig in future pulls to increase the precision and consistency of fibre draws.
- Measurement of more fibres per material type.

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A. Appendices

A.1 Fibre Pulling Rig

A custom designed apparatus was built to pull fibres. The machine closely resembled commercial draw towers, but on a smaller scale. One main advantage with this method is that the user's responsibility for creating the force to pull a fibre is limited and instead, relied on the precision of a TMA Zaber Stepper motor. In theory, this method should produce more consistent fibres as the human factor is removed. A labelled image of the custom built fibre rig is shown Figure.A.1. A modified torch head that encompassed the loaded preform was substituted for the welder's torch head use for manual pulling. The machine was assembled and tested, but at the time of writing has not been used to pull fibres.

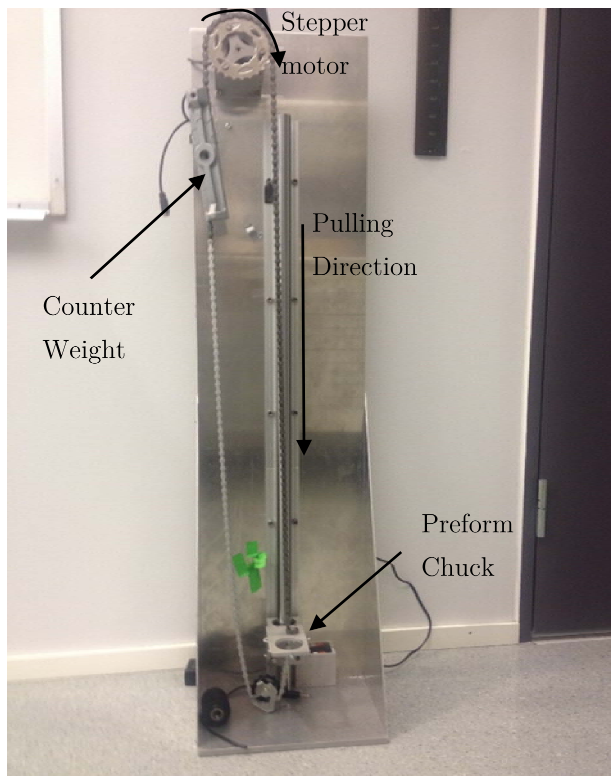

Figure.A.1: Custom built fibre pulling machine powered by stepper motor

A.2 Error Calculations

Error calculations apart of this work were computed using a simplified Gaussian propagation of uncertainties. For example, Ohm's Law:

$$J = \sigma E \tag{B.1}$$

The uncertainty would be estimated by:

$$U_J = \sqrt{\left(\frac{dJ}{dE} U_E\right)^2 + \left(\frac{dJ}{d\sigma} U_\sigma\right)^2} \tag{B.2}$$

Where U_J represents the uncertainty in J. Uncertainty in measurements were taken as half of the smallest unit of measurement. For example, a ruler with 1 mm markings would have a measurement uncertainty of ±0.5 mm.

For values estimated by regression and averages, such as resistivity, the total uncertainty was estimated using eq. (B.2) but adding an additional term including a student 2-tailed T-tests. That is:

$$\pm SD \cdot t_{a,dF} \tag{B.3}$$

Where SD is the standard deviation of the average, and $t_{a,dF}$ is the t-value taken from the t-test table with the required confidence interval (α), and the degrees of freedom of the sample (dF).

Plotting and regression calculations were performed by Microsoft Excel 2013.