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Local Resistivity Measurement on Multicrystalline Silicon

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Masters Thesis Submitted for the Partial Fulfillment of the Requirements for the Degree of Master of Science in Condensed Matter Physics

Supervisor: Prof. Ursula Gibson

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I dedicate this work to my mother who sacrifice her youth to make sure I am were I am.

Mame I know what you did for us is not going to be measured by anything so I just want to say thank you and may God keep you safe and live long to see all your rewards and your labors.

I love you

Abstract

Even though in the past the photovoltaic industry was dominated by single-crystalline silicon this days multi-crystalline silicon is consider to be on of the most promising material for application in low manufacturing cost solar photovoltaic arrays, consequently it has a huge potential to dominate the single-crystalline silicon in the photovoltaic industry in the next decades. However the presence of crystal defects such as dislocation and grain boundaries in multi-crystalline solar cells hugely reducing the conversion efficiency of this material compared to single crystalline silicon solar cell. Hence realizing the widespread utilization of this material will require understanding and control of the effects of this defects on the photovoltaic cell performance. Therefor we will examine the local resistivity of a given multi-crystalline sample in a dark and how it is affected by the presence of grain boundaries and the electrical activity when we cross or with in the grain boundary or twin boundaries. We have measured the resistivity of a number of samples of multi-crystalline silicon using a multi-height four-point probe.

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Chapter 1

Introduction

Solar electricity, also known as photovoltaics (PV), is a technology that uses a semiconductor material to convert suns energy in to electrical power when they are illuminated by photons that has an energy greater than the band gap. While the most widespread ways to produce electrical energy presently presents problems in terms of availability of resources and environmental effects, however, PV is far less concerned by these problems. The source of energy is the sun light, thus essentially infinite, and the most widespread PV technologies are based on silicon that is the second most abundant element in the earth crust [6].

Even though the non renewable energy sources still the main source of energy it is expected the PV solar energy to become a major energy source within this century. The basic working principle of solar cells is the photovoltaic effect that is the absorption of photons, by a semiconductor, which has energy greater than the band gap so that an electron-hole pairs (EHPs) will be created. These EHPs can be separated by the electric field to opposing terminals where they are extracted to perform work in an external circuit.

The most common and old technology of solar cell is the wafer based technology, in which ingots of silicon are cut into thin slices (wafers) that are processed to solar cells and assembled to solar modules. Addressing the high costs of purification of quartz to produce electronic grade silicon, photovoltaic research developed cheaper refining processes compared to microelectronics leading to sub-ppm densities of impurities without a too large decrease of solar cell efficiency. Additionally, the crystallization process was also simplified leading to higher yield and lower price at the expense of having multicrystalline silicon (silicon composed of 0.1 mm to 1 cm sized crystals) instead of singlecrystalline silicon. Multicrystalline silicon (mc-Si) is therefore of major interest for low cost solar cells.

1.1 Motivation

Due to the huge expansion of industries over the past century and a fast growth of developing countries specially in North America and Asia pacific our world was demanding energy more than ever. As a consequence of this the reserved amount of the main energy resources such as coal, oil and gas are decreasing rapidly due to unbalanced exploitation of natural resources to satisfy our need. To prevent major world energy shortages when all the stored energy is depleted we must begin to develop an alternative energy source before it is too late. Even though a lot of work has been done in the past decades to solve this problem, development of a clean energy resources as an alternative to fossil fuels as well as satisfying the great energy demand of the fast growing developing countries still been the most important tasks that we are facing in 21^{st} century.

In this new era, a renewable energy source such as solar energy, wind energy as well as wave energy has a larger role than ever to play. The first thing that will come in to our mind when we think about renewable energy source is the Sun which is the primarily source of all renewable energy. The Sun can supply a vast amount of energy to our Earths surface, on average the Earth can get, about $1.2 \times 10^{17} W$ [5] of solar power of which if we mange to harness a portion of this huge amount of solar energy for sure it would be enough to satisfy the world's hunger for energy.

As we know the high nuclear activity, in the center of the sun, generates a huge amount of electromagnetic radiation. According to the theory of quantum mechanics, this radiation of light is composed of particles called photons. Photons have no mass, but each carries an energy and momentum, which is related to the wavelength of the light.

$$E = \hbar\omega = \frac{hc}{\lambda} \tag{1.1}$$

Even though it is possible to use the solar energy for different purposes the most desirable use of solar energy and the most important to our future is the production of electricity. To harness this huge amount of energy and change it into electricity it needs a technological device that can convert directly the absorbed solar energy into electricity. The most common and important device that we use to transform this solar energy in to electricity is the Photovoltaic solar cell. Solar photovoltaic (PV) directly converts solar energy into electricity using a PV cell made of a semiconductor material.

A PV solar cell is the most promising renewable energy technology of this century. According to international energy agency(IEA) over the period 2000-11, solar PV was the fastest-growing renewable power technology worldwide for example solar electric energy has grown by 20%-25% per year over the past 10 years. Cumulative installed capacity of solar PV reached roughly 65 gigawatts at the end of 2011, up from only 1.5 GW in 2000 and according to solarbuzz, the international solar electric industry generates around 3-4 billion in revenues each year.

The PV industries emerges as the main actor in the area of renewable energy after we saw

a sharp annual growth in the module production recently. In 2003 the PV industry uses more Si wafers than the microelectronics industry [1].

Crystalline silicon PV cells are the most common photovoltaic cells in use today. They are also the earliest successful PV devices. However the high price of the technology, which is the material cost as well as production cost, becomes the main obstacle for large-scale expansion of PV solar cells. However this days PV industries starts to use mc-Si wafers which have a huge potential to conquered the market through a significant reduction in cost in comparison to single crystal Si with a small sacrifice in device performance.There are some reasons when we say that mc-Si will dominate the PV solar cell industry in the future to mention some

- The simplicity and versatility of the casting technique, which can accept silicon feed stock which consider to be a waste in microelectronics industry.
- The electronic quality is comparable to that of single crystal Czochralski(CZ) silicon.
- The carrier lifetime of single crystal CZ silicon is lower than the mc-Si due to the degradation of the P-type CZ Si under the solar cell operating conditions.
- And finally the cost of a CZ wafer is higher than the mc-Si wafer and considering that the efficiency difference is only 1% is not big enough to compensate for the high cost of CZ wafers.

Even though mc-Si becomes popular and reliable PV material in the last few decades its drawbacks remain as challenging as ever, and they need to be solved urgently to keep up with the improved performance levels that are being demanded from solar cells[10].

So the main motivation of this research is to solve this problem by using use mc-Si, which is easily accessible and cheap processing cost for application of low cost PV solar cells. However mc-Si features crystal defects such as dislocations and grain boundaries that gives lower cell efficiency than snglecrystalline cell. So to use this material for application of PV solar cell and increase the efficiency of the cell will require understanding of the effect of crystal defects specifically grain boundary on the performance of the PV solar cell. However the effect of grain boundaries on the properties of the cells are not well understood and looking at the resistivity maps will contribute to our understanding.

1.2 Previous research

This work is a continuation of the work started by Karianne Austad [2] specifically on the resistivity measurement of mc-Si using a four point probe. As it can be seen clearly from her graphs the signal to noise (SNR) was very low, and the step size in probe motion precluded any major conclusions. Therefore this thesis was intended to follow up on results to determine whether the technique could be more useful with improved electronics.

Chapter 2

Background

2.1 Solid Materials

In general solid materials are often divided in to three categories based on their conductivity; insulators, semiconductors and conductors [7]. As shown in figure 2.1 both insulators and conductors have a discrete conductivity values where as semiconductors have a values ranging from close to insulators to almost perfect conductors. This range of conductivity is the most important proprieties of semiconductors which have many application in this electronic world. We will see later in this chapter how this range of conductivity or a change in resistivity of a semiconductor can be achieved.

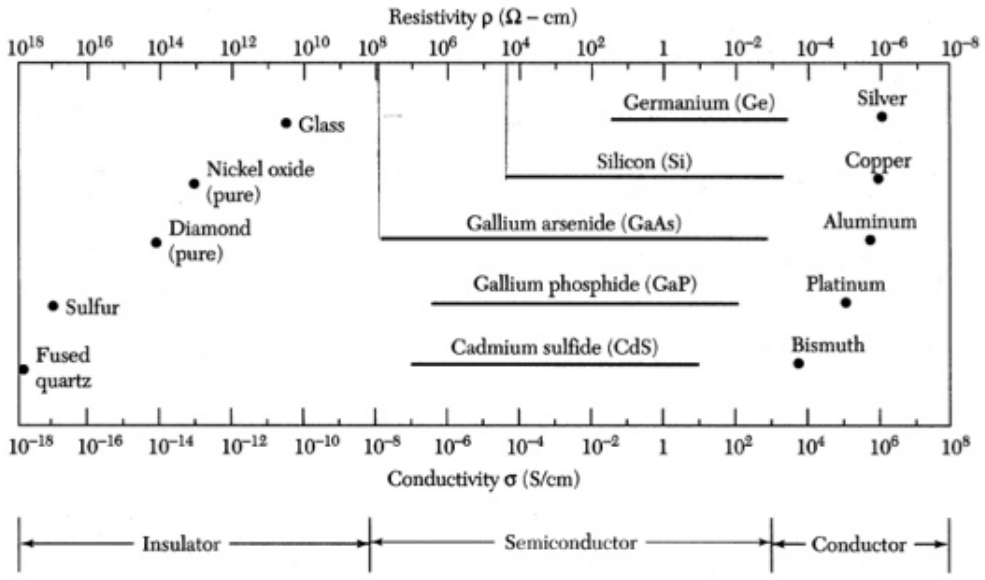

Figure 2.1: Range of conductivity values for some selected insulators, semiconductors and conductors [16].

2.2 Energy Band

As it was mentioned above solid materials categorize in to metals, semiconductors and insulators based on the ability to conduct electricity which is a consequence of a difference in energy band structure of materials so it is a good idea to see first the formation of band structure of solid materials in general.

2.2.1 Band theory of solids

According to quantum theory, "in an isolated atom the electrons surrounding a nucleus are restricted to a certain discrete energy levels in which gaps exist in the energy scale were no energy states are available" [15]. However according to the Pauli exclusion principle, the maximum number of electrons that can occupy the same energy-level is two provided that they have opposite spins. In the case of solids as each isolated atoms are brought together to form a solid the electrons of one atom are very close to the electrons of the nearest neighboring atoms as a result of this their electron wave functions begin to overlap and it appears as the electrons of one atom is occupying the same energy-levels as the corresponding electrons in the neighboring atom [12].

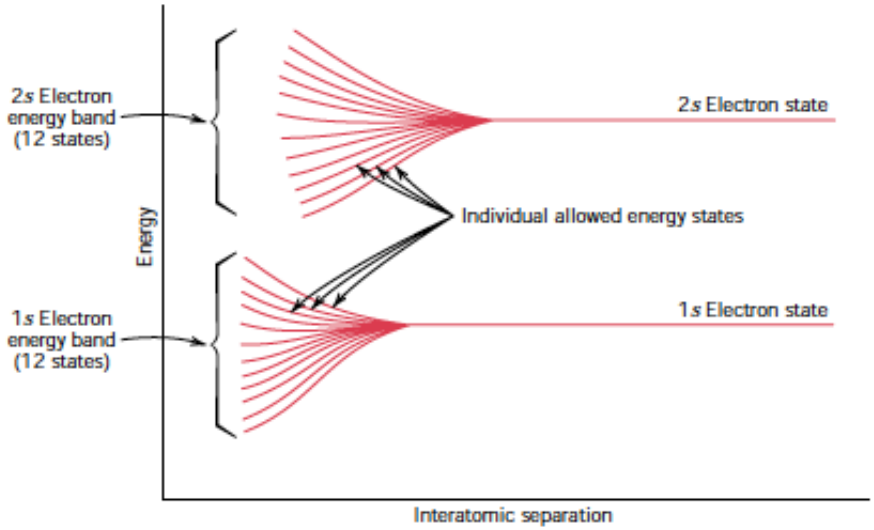

Figure 2.2: Energy splitting of two energy levels for six atoms as a function of the separation of the atoms [9].

However this violates the Pauli exclusion principle so when atoms are brought together to form a solid each distinct allowable energy levels will split, as shown in figure 2.2, in to slightly different energy levels so that no more than two electrons will occupy the same energy level [9].

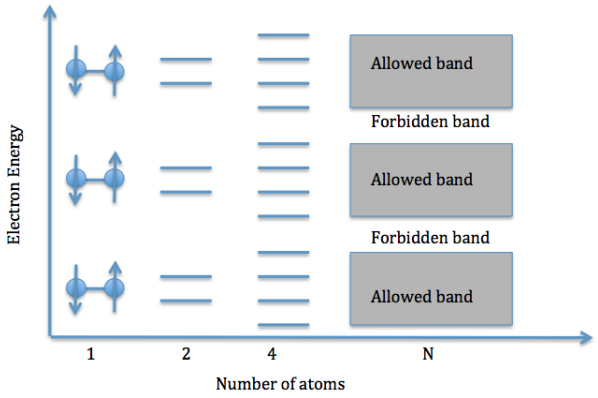

Figure 2.3: The Energy band of Solids.

Because the number of atoms in a crystal is very large the energy difference between each split energy level will be extremely small therefore for large number of atoms we can consider each sets of split energy levels as a continuous level of energy called bands [8] as shown in figure 2.3. The electron energy band structure can be viewed as an overlap between single electron energy states as shown in figure 2.4 which shows how the energy band structure is generated.

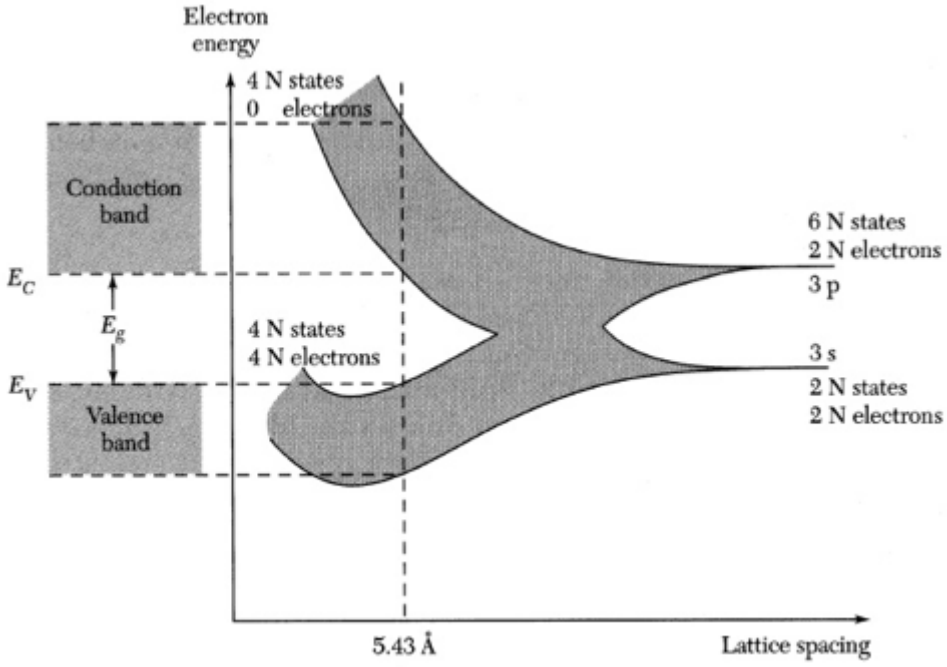

Figure 2.4: Formation of Energy bands as a diamond lattice crystal is formed by bringing isolated silicon atoms together [16].

Each discrete energy levels have come together to form allowed energy bands, which is the valance band (VB) and the conduction band (CB), where electron can be found, and

a forbidden regions between the allowed bands called a band gap energy (E_g), a region were no electron is allowed to be found.

2.2.2 Band gap

A band gap (E_g) is the forbidden regions, between the allowed energy bands, where electrons can not be found. This band gap represents the amount of energy required to knock electrons out of the valence band into the conduction band and allow it to become part of an electrical circuit. The energy required for an electron to jump the band gap can be provided by heat or some form of radiation or from an electric field and is usually expressed in electron volt (eV) (An electron volt is equal to the energy gained by an electron when it passes through a potential of 1 volt in a vacuum) where $1\ \mathrm{eV}$ is equivalent to $1.6 * 10^{-19}$ J. In semiconductor as well as in insulators the energy range is not continuous, as it is in metals, it is been interrupted by an energy gap of width E_g. Table 2.3 shows energy gap value of some semiconductor materials.

For electrons to participate in conduction of electricity, they have to be in the CB. However this can only happen if the electrons in the VB are provided with enough energy from an external source to move from the VB to the conduction band as a result of this the concentration of electrons in the CB as well as the conductivity of the material will increase. In addition to this, there will be a free state in the VB, which results in a less probability of collisions among the remaining electron, which lead to a higher mean kinetic energy of the electrons in the valence band [**?**]. This also contribute to a better conductivity for the material.

As we mentioned before radiation of light is composed of particles called photons. Photons are a packets of light energy. The photon energy of light varies according to the wavelengths of the light as shown in equation 2.1. The entire spectrum of sunlight, from infrared to ultraviolet, covers a range of about $0.5\ \mathrm{eV}$ to about $2.9\ \mathrm{eV}$. For example, red light has an energy of about $1.7\ \mathrm{eV}$, and blue light has an energy of about $2.7\ \mathrm{eV}$. The energy of a photon absorbed by the electron in VB must be at least as great as the band gap energy in ordered for the electron in the CB to be excited. However, photons with more energy than the band gap energy will expend the extra energy as heat when freeing electrons. Most PV cells cannot use the energy of the sunlight because this energy is either below the band gap of the material used or carries excess energy. Typical band gap for semiconductor silicon is $\mathrm{E_g} = 1.1\ \mathrm{eV}$, compared with $5\ \mathrm{eV}$ for diamond, which is an insulator [15].

Energy of light in electron volt (eV) for a given frequency is given by,

$$E = h\nu = \frac{hc}{\lambda} \tag{2.1}$$

where E is energy in electron volts, h is Planks constant, ν is frequency, and c is the speed of light.

2.3 Semiconductors

Semiconductor materials are, as the name implies, a type of materials whose conductivity lies between that conductors and insulators. They have lower conductivity than conductors, but better than insulators. They are general classified in to two, the elementary semiconductors, found in group IV of the periodic table and the compound semiconductors formed by combinations of group III and group V elements [7].

Period	II	III	IV	V	VI
2		B	C	N	O
3	Mg	Al	Si	P	S
4	Zn	Ga	Ge	As	Se
5	Cd	In	Sn	Sb	Te
6	Hg		Pb		

Table 2.1: A portion of the periodic table related to semiconductors.

Table 2.1 shows a portion of the periodic table in which the most common semiconductors are found where as table 2.2 lists some elemental and compound semiconductors.

Elemental semiconductors	
Si	Silicon
Ge	Germanium
Compound semiconductors	
AlP	Aluminum phosphide
AlAs	Aluminum arsenide
GaP	Gallium phosphide
GaAs	Gallium arsenide
InP	Indium phosphide

Table 2.2: A list of some semiconductor materials [7].

Silicon which is an elemental solid state semiconductor is the point of discussion in this work.

2.3.1 Electrical properties of semiconductor

When an isolated atoms are brought together to form a solid various interactions such as ionic, metallic, covalent will occur between neighboring atoms of a solid. The forces of attraction and repulsion between atoms in the bond will be in equilibrium at a proper inter atomic spacing for a given crystal. In the process, important changes occur in the electron energy level configurations, and these changes result in the varied electrical properties of

solids[15]. The electrical properties of a semiconductors can be controlled by two means first we can change it by creating a electron-hole pair using the mechanism thermal excitation as the temperature of the sample increased. Second by adding donors or accepters impurities.

In semiconductors the type of bond is a covalent bond where each atom contributes an electron to share with its neighboring atoms. To understand the fundamental electrical differences between semiconductors, insulators and metals we need to know two important information.

- Understanding of how allowed bands and forbidden bands form when atoms come together to form a solid.
- A band that is completely full of electrons can not participate in electrical conduction.

Since we already saw in the above subsection how an allowed as well as a forbidden bands are formed lets see here how an electron behave in a completely full band specifically in semiconductors. In intrinsic semiconductors (semiconductors which are not doped) the highest allowed energy band below the energy gap and nearly completely filled with electrons at absolute zero ($\mathrm{T} = 0\ \mathrm{K}$) is called valance band(VB) and the next higher allowed energy band above the energy gap, which is nearly empty at $\mathrm{T} = 0\ \mathrm{K}$, is called the conduction band(CB). The VB is the highest filled energy band at $\mathrm{T} = 0\ \mathrm{K}$ and the CB is the first allowed band lying above the VB. For an electron to participate in conduction of electricity the electron should be in the CB therefore, electrons in the VB should gain enough energy, to cross the band gap, from an external stimuli to move in to higher energy state which is CB. However an electron in VB can only be exited to the CB if the energy absorbed by the electron has an energy at least $E_{gain} = E_g$ [12].

Often one speaks of a semiconductor if $\mathrm{E_g} < 3\ \mathrm{eV}$, and of an insulator if $\mathrm{E_g} > 3\ \mathrm{eV}$. Indeed, this crossover value reduces as the temperature is lowered and at $\mathrm{T} = 0\ \mathrm{K}$ all semiconductors are insulators. As shown in table 2.3 at $\mathrm{T} = 300\ \mathrm{K}$, $\mathrm{E_g} - \mathrm{Si} = 1.12\ \mathrm{eV}$, $\mathrm{E_g} - \mathrm{Ge} = 0.66\ \mathrm{eV}$, $\mathrm{E_g} - \mathrm{GaAs} = 1.42\ \mathrm{eV}$, $\mathrm{E_g} - \mathrm{InSb} = 0.17\ \mathrm{eV}$ (narrow gap semiconductor), $\mathrm{E_g} - \mathrm{ZnS} = 3.68\ \mathrm{eV}$ (wide band semiconductor) [15].

Basically intrinsic semiconductors at $\mathrm{T} = 0\ \mathrm{K}$ behaves and have the same band structure as insulators, the only difference is the size of band gap, that is band gap of insulators is much larger than the band gap of semiconductors[15]. As it was mentioned before the energy range for electrons in metals is continuous hence an electron excited by absorbing a photon loses its extra energy easily to the crystal as a lattice collision (phonon). Since any particle prefers to minimize its energy the excited electron will try to return to its initial state, by losing energy as photon or phonon, which is the valance band. Therefore because of metals have a continuous band energy, the life time of the exited electrons is very short (order of $10^{-12}\ \mathrm{s}$) there is no enough time to convert this energy in to electrical energy before it losses its extra energy. On the contrary in semiconductors however, because of the energy gap,the excited electron will need more time to return to a state in the valance band. As a result an electron may stay in the conduction band for about $10^{-3}\ \mathrm{s}$

Semiconductor		Lattice constant Å	Bandgap eV	Band	Mobility ($\mathrm{cm}^2/\mathrm{Vs}$) μ_n	μ_p	Dielectric constant
Element	Ge	5.65	0.66	I	3900	1800	16.2
	Si	5.43	1.12	I	1450	505	11.9
IV-IV	SiC	3.08	2.86	I	300	40	9.66
III-V	AlSb	6.13	1.61	I	200	400	12.0
	GaAs	5.65	1.42	D	9200	320	12.4
	GaP	5.45	2.27	I	160	135	11.1
	GaSb	6.09	0.75	D	3750	680	15.7
	InAs	6.05	0.35	D	33000	450	15.1
	InP	5.86	1.34	D	5900	150	12.6
	InSb	6.47	0.17	D	77000	850	16.8
II-VI	CdS	5.83	2.42	D	340	50	5.4
	CdTe	6.48	1.56	D	1050	100	10.2
	ZnO	4.58	3.35	D	200	180	9.0
	ZnS	5.42	3.68	D	180	10	8.9
IV-VI	PbS	5.93	0.41	I	800	1000	17.0
	PbTe	6.46	0.31	I	6000	4000	30.0

Table 2.3: Some properties of important element and compound semiconductors at $\mathrm{T} = 300$ K [16].

which is comparatively long time than the life time of electrons in metals to convert the excess electron energy in to electrical energy before recombination takes place[17].

2.3.2 Direct and Indirect Semiconductors

Based on the energy band structure semiconductors can be divided in to two classes direct and indirect semiconductors as shown in the Figure 2.5 (a, b) respectively.

Figure 2.5 shows the band structure of semiconductors of allowed energy verses momentum. The minimum amount of energy which will promote an electron from the valence band into the conduction band is called the fundamental band gap, E_g. If the conduction band minimum(CB_{min}) and valence band maximum (VB_{max}) occur at the same value of **k**, then a photon of energy E_g is sufficient to create an electron-hole pair. This type of semiconductor is called a *direct band gap* material shown in figure 2.5a.

Example of *direct band gap* material is: GaAs, GaN

And if the CB_{min} and VB_{max} occur at different values of **k**, a photon with energy E_g is not on its own sufficient to create an electron-hole pair. Promoting an electron from the VB_{max} to the CB_{min} would cause a change in its momentum. Momentum has to be conserved in a crystal, but since photons possess virtually no momentum, that extra

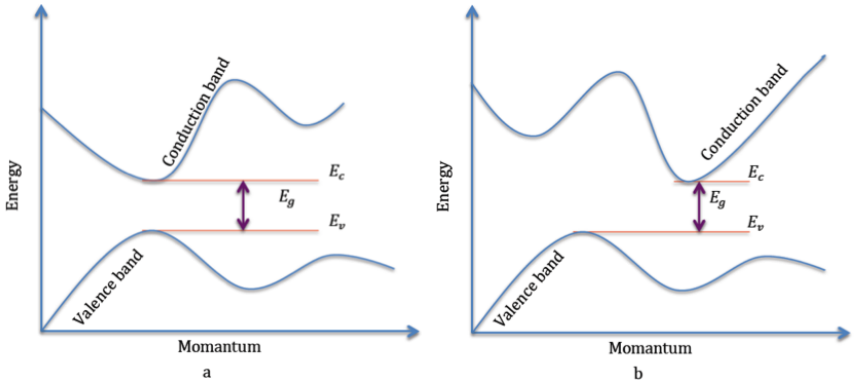

Figure 2.5: The two classes of semiconductors (a) direct energy band gap and (b) indirect band energy gap.

momentum must be supplied by some thing else. Usually it is supplied by a *phonon*-a lattice vibration-of the correct momentum. The phonon gives up its momentum to the electron at the moment of photon absorption so that both energy and momentum are conserved. This type of semiconductor is called an *indirect band gap* material shown in figure 2.5b [18].

Example of *indirect band gap* material is: Ge, Si

As it was mentioned above any particle prefers to minimize its energy so an electron in the conduction band can fall in to an empty state in the valance band by giving off an energy this processes is called recombination we will see later more about this. In direct semiconductors the energy given off as a photon of light is equal to the E_g where as, in the indirect semiconductors it is less than the E_g [20].

Figure 2.6 shows the band structure of the two most important semiconductors Si and GaAs. The valence band maximum in most semiconductors is at **k**=0 point which is denoted by Γ. As we can see from the figure the conduction band minimum for Si is at $k \neq 0$; therefore it is indirect band gap, on the other hand the conduction band minimum and the valance band maximum for GaAs are both at $k = 0$; therefore it is a direct band gap.

2.4 Charge Carriers in semiconductors

Conduction of current in metals is much more easy to visualize than in semiconductors. In the case of semiconductors at $\mathrm{T} = 0$ K has a filled valance and an empty conduction band therefore for conduction to take place an electron-hole pair must first created by thermal excitation by increasing the temperature of the sample. Also we can change the charge carriers concentration by introducing impurities.

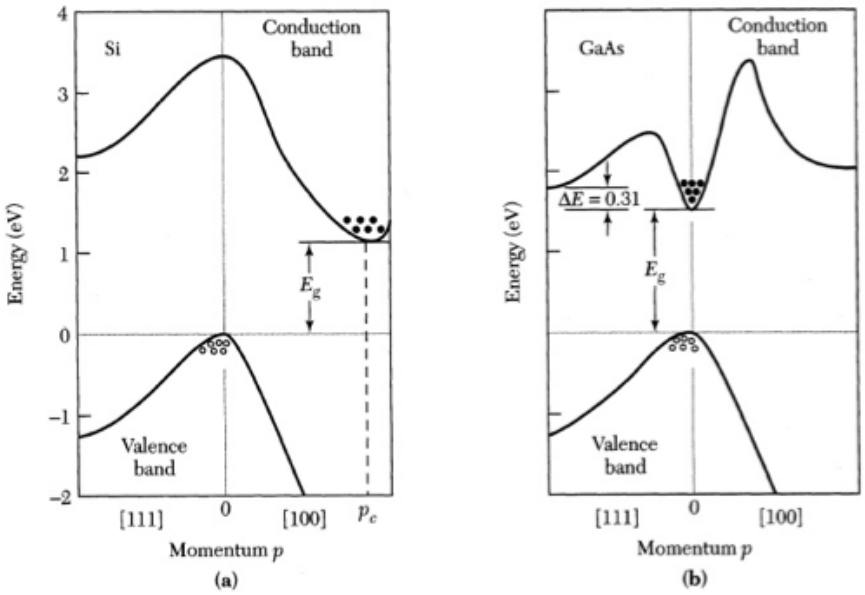

Figure 2.6: Energy band structures of Si and GaAs [16].

2.4.1 Densities of electrons and holes

The number of allowed states per unit volume and energy is given by [18]

$$N(E) = \frac{8\sqrt{2}\pi m_e^{*3/2}}{h^3}\big(E - E_c\big)^{1/2} \tag{2.2}$$

and the probability of occupying this states (equation 2.2) is given by the Fermi-Dirac distribution function as follows

$$f(E) = \frac{1}{1 + \mathrm{e}^{(\mathrm{E}-\mathrm{E_F})/\mathrm{k_B T}}} \tag{2.3}$$

Were $f(E)$ is the maximum energy level occupied by an electron at $\mathrm{T} = 0\ \mathrm{K}$ using the above two equations 2.2 and 2.3 we can calculate the density of electrons in the CB and holes in VB.

The number of electrons in the conduction band per unit volume of the crystal is given by [18]

$$n = \int_{E_c}^{E_{c\ max}} f(E)N(E)dE \tag{2.4}$$

Using the following three assumptions we can find the value for the integration of 2.4

1. Since E_c is $\gg$ than E_F, $f(E)$ for the CB will be $\approx \mathrm{e}^{-(\mathrm{E}-\mathrm{E_F})/\mathrm{k_B T}}$
2. We can replace $E_{c\ max}$ with ∞ and
3. $\int_0^\infty \mathrm{x}^{1/2}\mathrm{e}^{-\mathrm{x}}dx$ is a standard form and is equal to $\sqrt{2}/\pi$

Considering this we get,

$$n = 2\big(\frac{2\pi m_e^* k_B T}{h^2}\big)^{3/2} \mathrm{e}^{(\mathrm{E_F}-\mathrm{E_c})/\mathrm{k_B T}} = N_c \mathrm{e}^{(\mathrm{E_F}-\mathrm{E_c})/\mathrm{k_B T}} \tag{2.5}$$

- Were $N_c = 2\big(\frac{2\pi m_e^* k_B T}{h^2}\big)^{3/2}$ is the effective density of states in the conduction band and is constant for a given temperature. Were m_e^* is an "effective mass" of the electron which incorporates the effect of the periodic force of the lattice atoms, $\mathrm{h} = 6.625 \times 10^{-34}$ Js is Planck's constant, $\mathrm{k_B} = 1.380 \times 10^{-23}$ J/K Boltzmann's constant
- E_c the minimum energy of the conduction band
- E_F is the Fermi energy up to which states are filled
- T is an absolute temperature,
- $k_B T$ is the internal energy

And the total number of holes in the VB per unit volume of the crystal can be calculated similarly with N_v, the effective density of states in the VB. Therefore

$$p = 2\big(\frac{2\pi m_p^* k_B T}{h^2}\big)^{3/2} \mathrm{e}^{-(\mathrm{E_F}-\mathrm{E_v})/\mathrm{k_B T}} = N_v \mathrm{e}^{(\mathrm{E_v}-\mathrm{E_F})/\mathrm{k_B T}} \tag{2.6}$$

2.5 Intrinsic and Extrinsic(doped) semiconductors

Finite conductivity of semiconductors is due to occupied states in CB (conduction electrons) or unoccupied states in VB (holes).

There are two mechanisms to get non-zero concentrations of electrons and holes

1. Thermal excitation of electrons from the VB to the CB
2. Thermal ionization of impurities that provide additional states and can donate (donors) or accept (acceptors) electrons

In the absence of impurities (which is never true) the semiconductor is called intrinsic, otherwise it is called doped. In pure (intrinsic) semiconductors, concentration of conduction electrons, n_e, is equal to the concentration of holes, n_h. This is known as electrical neutrality condition. In doped semiconductors, impurities may be ionized and donors will become positively charged and acceptors become negatively charged [16].

2.5.1 Intrinsic Semiconductors

An intrinsic semiconductor is a perfect crystal with no impurities or lattice defects. At absolute zero temperature there is no charge carriers since the valance band of intrinsic semiconductor is full and the conduction band is empty as shown in the figure 2.7 (left).

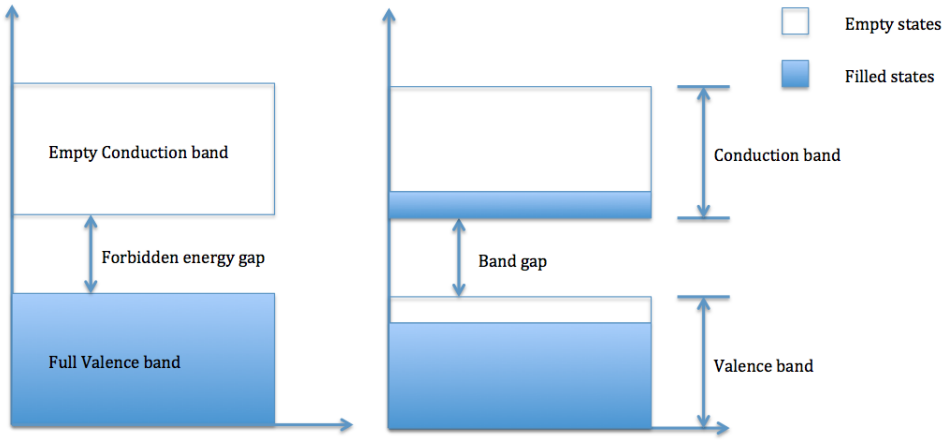

Figure 2.7: Semiconductor energy bands at absolute temperature (left) and at room temperature (right).

The difference in energy between the bottom of the conduction band (E_c) and the top of the valance band (E_v) is called the energy gap (E_g) of the semiconductor and is given by

$$E_g = E_c - E_v \tag{2.7}$$

As it was mentioned above a full band as well as an empty band of a semiconductor can not participate in electrical conduction at absolute temperature. However an electron-hole pairs (EHPs) can be generated when an electron in the VB receive enough thermal energy and excited across the E_g and be available for conduction in CB. As a result of this a unoccupied electron energy state called a hole will be left in the valance band as shown in the Figure 2.7 (right) and it behaves like a positive charge carriers with the same magnitude but opposite sign as the electron [18]. For intrinsic semiconductors the number of electrons in the conduction band must equal the number the number of holes in the valance band because each e^- has given rise to one h^+ and the conduction of current takes place by electrons in the conduction band as well as by holes in the valance band which is the conduction is a bipolar (two carrier). At room temperature Si has a band gap of about 1.1 eV so a valance band electron in Si must gain 1.1 eV or more of energy to be excited to the the conduction band of Si [12].

Since for an intrinsic semiconductors e^- and h^+ created in pairs, the conduction band electron concentration n(electrons/cm^3)is the same as the concentration of holes in the valance band p (holes/cm^3) and they are called an intrinsic carrier concentration usually denoted as n_i.

The concentration of electron-hole pairs n_i will have a certain value for a given temperature [15]. As there is a generation of electron-hole pair there will be also a recombination of electron-hole. Recombination of EHPs takes place when an electron in the conduction band makes a transition to an empty state in the valance band. If a steady state carrier concentration is maintained the recombination of EHPs is at same rate as generation of

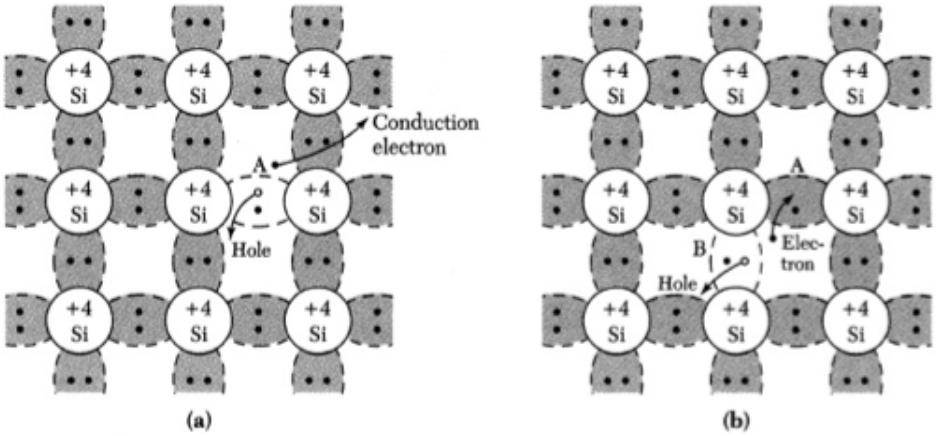

Figure 2.8: The basic representation of intrinsic silicon. (a) A broken bond at position A, resulting in conduction electron and a hole. (b) A broken bond at position B [16].

EHPs is express as follows

$$r_i = g_i \tag{2.8}$$

For an intrinsic semiconductor (semiconductor without any doping atoms), like a pure silicon crystal,

$$n = p = n_i \tag{2.9}$$

As electrons are excited from the valence band into the conduction band a hole which is describe as a missing electron will appear in the valance band. With a small band gap, and high temperatures, there will be a considerably larger amount of electrons in the conduction band, compared to low temperatures, and a large band gap. This is described by low of mass action and the law of mass action can be written as

$$np = n_i^2 \tag{2.10}$$

Substituting the value for n and p from equation 2.5 and 2.6 respectively and considering equation 2.9 we get

$$np = n_i^2 = N_c N_v \mathrm{e}^{(\mathrm{E_v}-\mathrm{E_c})/\mathrm{k_B T}} = N_c N_v \mathrm{e}^{-\mathrm{E_g}/\mathrm{k_B T}} \tag{2.11}$$

Therefor

$$n_i = \sqrt{N_c N_v}\mathrm{e}^{-\mathrm{E_g}/2\mathrm{k_B T}} \tag{2.12}$$

The number of electrons per unit volume (n) in the conduction band and holes in the valence band per unit volume (p) is given by $n = N_c \mathrm{e}^{(\mathrm{E_F}-\mathrm{E_c})/\mathrm{k_B T}}$ and $p = N_v \mathrm{e}^{(\mathrm{E_v}-\mathrm{E_F})/\mathrm{k_B T}}$

from equation 2.5 and 2.6 respectively. And for an idealized case of a pure and perfect crystal n equals p

$$n = p \tag{2.13}$$

now lets substitute n and p in equation 2.13 we get

$$N_c \mathrm{e}^{(\mathrm{E_F}-\mathrm{E_c})/\mathrm{k_B T}} = N_v \mathrm{e}^{(\mathrm{E_v}-\mathrm{E_F})/\mathrm{k_B T}} \tag{2.14}$$

Then $\ln$ of both sides gives us

$$\ln(N_c \mathrm{e}^{(\mathrm{E_F}-\mathrm{E_c})/\mathrm{k_B T}}) = \ln(N_v \mathrm{e}^{(\mathrm{E_v}-\mathrm{E_F})/\mathrm{k_B T}}) \tag{2.15}$$

Expanding equation 2.15 we get

$$\ln(N_c) + \ln(\mathrm{e}^{(\mathrm{E_F}-\mathrm{E_c})/\mathrm{k_B T}}) = \ln(N_v) + \ln(\mathrm{e}^{(\mathrm{E_v}-\mathrm{E_F})/\mathrm{k_B T}}) \tag{2.16}$$

from equation 2.16 we get

$$\ln(N_c) + (E_F - E_c)/k_B T = \ln(N_v) + (E_v - E_F)/k_B T \tag{2.17}$$

from equation 2.17 solving for E_F gives

$$E_F = \frac{E_c + E_v}{2} + \frac{k_B T}{2} \ln(N_v/N_c) = \frac{E_c + E_v}{2} + \frac{3k_B T}{4} \ln\left(m_h^*/m_e^*\right) \tag{2.18}$$

From equation 2.18 we can see that the Fermi level for an intrinsic semiconductor lies close to the mid gap.

2.5.2 Extrinsic Semiconductors

In the above subsection we mention how carriers generated in semiconductors thermally. But it is also possible to create carriers by purposely introducing different concentration of impurities into the crystal to get a range conductivity and this process is called doping [16]. By adding certain atoms of a different type than those constituting the semiconductor itself, it is possible to increase the concentration of electrons in the conduction band without a change on the number of holes in the valence band. For example adding phosphorous into a silicon crystal will result in more electrons in the conduction band, due to phosphor having one more valence electron than silicon. By adding phosphorous this way, one can increased electrons, n, without increasing holes, p. This is called donor doping. If you instead of phosphor, add boron, the material will be acceptor doped. This is due to boron having one less electron in the valence band than silicon, and would result in an extra hole in the valence band of the crystal.

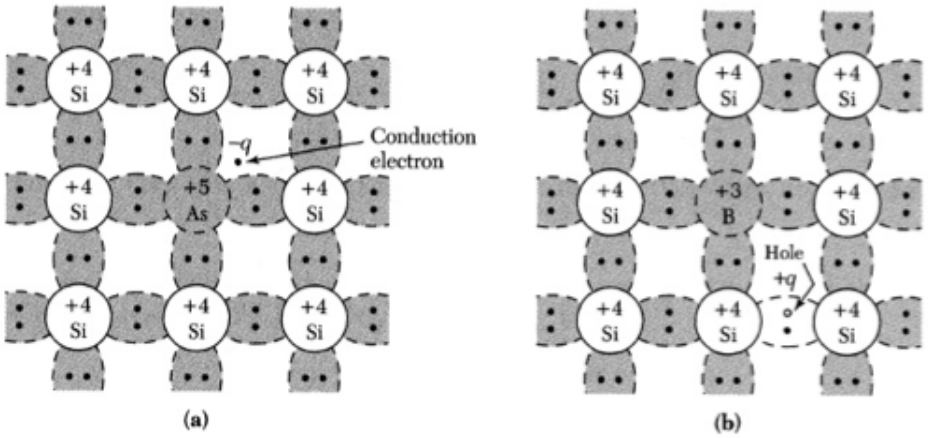

Figure 2.9: The representation of extrinsic silicon for (a) n-type Si with donor atom (arsenic) and (b) p-type Si with acceptor atom (boron) [16].

The density of carriers can be controlled by varying the density of dopants, N_d. If $N_d \gg n_i$ and the donors (n-type material) are fully ionized at room temperature, then

$$n \approx N_d \tag{2.19}$$

and in equilibrium if we substitute 2.19 in to 2.10 we get

$$p = \frac{n_i^2}{N_d} \tag{2.20}$$

And if we substituting N_d for n in equation 2.5 we get

$$N_d = N_c \mathrm{e}^{(\mathrm{E_F}-\mathrm{E_c})/\mathrm{k_B T}} \tag{2.21}$$

Then $\ln$ of both sides

$$\ln(N_d) = \ln(N_c \mathrm{e}^{(\mathrm{E_F}-\mathrm{E_c})/\mathrm{k_B T}}) \tag{2.22}$$

from this we get

$$\ln(N_d) = \ln(N_c) + (E_F - E_c)/k_B T \tag{2.23}$$

$$\ln(N_d) - \ln(N_c) = \ln(N_d/N_c) = (E_F - E_c)/k_B T \tag{2.24}$$

Then from equation 2.24 we get

$$E_F - E_c = k_B T \ln(N_d/N_c) \tag{2.25}$$

Similarly, for material doped with acceptors, where $N_a \gg n_i$ we have

$$p \approx N_a \tag{2.26}$$

and in equilibrium if we substitute 2.26 in to 2.10 we get,

$$n = \frac{n_i^2}{N_a} \tag{2.27}$$

And if we substituting N_a for p in equation 2.6 we get

$$N_a = N_v \mathrm{e}^{(\mathrm{E_v}-\mathrm{E_F})/\mathrm{k_B T}} \tag{2.28}$$

Then $\ln$ of both sides

$$\ln(N_a) = \ln(N_v \mathrm{e}^{(\mathrm{E_v}-\mathrm{E_F})/\mathrm{k_B T}}) \tag{2.29}$$

from this we get

$$\ln(N_a) = \ln(N_v) + (E_v - E_F)/k_B T \tag{2.30}$$

$$\ln(N_a) - \ln(N_v) = \ln(N_a/N_v) = (E_v - E_F)/k_B T \tag{2.31}$$

Then from equation 2.31 we get

$$E_v - E_F = k_B T \ln(N_a/N_v) \tag{2.32}$$

where N_d is donor concentration, and N_a is acceptor concentration. If the equilibrium carrier concentrations n_0 and p_0 of a given material are not the same as the intrinsic carrier concentration n_i when a crystal is doped then the material is said to be extrinsic [20]. From equation 2.25 and 2.32 the Fermi level (E_F) of the semiconductor moves away from the middle towards the CB for n-type and VB for p-type material as the doping concentration increases [18].

2.5.3 n-type and p-type semiconductors

A doped semiconductor is generally called extrinsic [15]. If a semiconductor is doped with a number of donor atoms there will be more electrons than holes and it is called n-type. For acceptor doping it is called p-type semiconductor. The dominating charge carrier in the semiconductor are called majority carriers. The other charge carrier, i.e. holes in the n-type semiconductor and electrons in the p-type semiconductors are called minority carriers. Impurities may affect either band. Donors contribute electrons to the CB or fill holes in the VB. Acceptors remove electrons from the CB or create holes in the VB. We will assume that each impurity atom contributes (removes) exactly one electron. This is known as approximation of fully ionized impurities.

2.5.4 Impurity levels

When impurities are introduce in to a perfect semiconductor, additional levels will be created with in the band gap of the energy band structure. For example am impurities

from column V such as P introduce an energy level called a donor level very near to the CB and it only needs a very little thermal energy to excite these electrons to the conduction band. Therefore at room temperature $n_0 \gg (n_i, p_0)$ for semiconductors doped with a donor atoms. Where as impurities from column III such B introduce impurity levels called acceptor levels near the VB and they are empty at 0 K and it only needs a very little thermal energy to excite electrons from the valance band into the impurity levels leaving behind holes. Therefore at room temperature $p_0 \gg n_0$ for semiconductors doped with a acceptor atoms [15].

2.6 Silicon

The chemical symbol of silicon is Si and it is found in group IV A with an atomic number 14. The name Silicon was first suggested by a Scottish chemist Thomas Thomson (1773-1852) and is originated from the Latin word silex (Flint) and it was isolated for the first time in 1823 by the Swedish chemist Jons Jakob Berzelius. Next to oxygen Silicon is the second must abundant element in the Earth's crust. Its abundance is estimated to be about 27.6 % of the earth's crust. Naturally Si does not occur in its elemental form. It is always found in combination with oxygen as silicon dioxide (SiO_2), often called silica, or with oxygen and various metals in the form of salts of silicic acids, or silicates moreover, many rocks contain quartz crystals. Therefore the availability of high quality and quantities of raw materials of silicon is the main reason for the dominance of silicon in the PV industry [13].

2.6.1 Atomic Structure

All matter is composed of atoms, which are made up three basic particles protons, electrons, and neutrons. The central part of the atom which is the nucleus contains the positively charged protons and the neutral neutrons were as the negatively charged electrons orbit around the nucleus. Since the number of positively charged protons and the negative charged electrons are the same for a given atom the overall charge of an atom is neutral.

As shown in figure 2.10, silicon atom has 14 electrons with with an electronic configuration $[Ne]s^2 3p^2$. Since the outer most shell of Si contains four electrons, Si is a tetra valent element.These four electrons, called valence electrons and play an important role in the photoelectric effect.

Depending on their energy levels electrons orbit at different distances from the nucleus. The less energetic electrons orbit close to the nucleus were as the more energetic electrons orbit farther away from the nucleus. The higher-energy electrons farthest from the nucleus are the ones that bond with neighboring atoms to form solid structures.

From electronic configuration, the outermost valence shell of Si atom has four electrons. So in order the outermost valance shell to be complete (to have a stable set of eight elec-

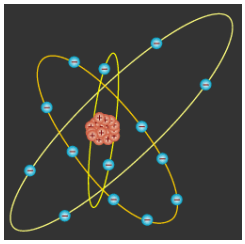

Figure 2.10: Silicon atoms has 14 electrons. The four electrons that orbit the nucleus in the outermost "valence" energy level are shared with other neighboring atoms [14].

trons) or to satisfy the octet rule each Si atom share each of its four valance shell electrons with each of four neighboring atoms by covalent bond, which form the energy state valance band.

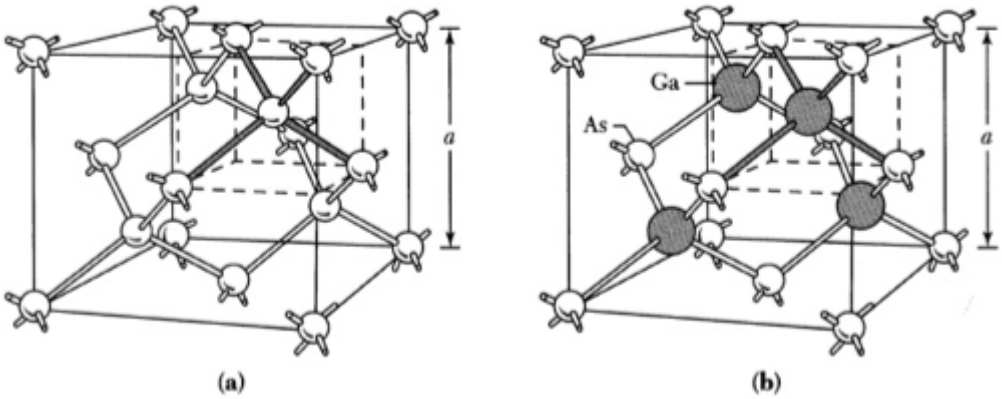

Figure 2.11: (a) Diamond lattice: atom shares each of its four valence electrons with each of four neighboring atoms and (b) Zincblende lattice structure [16]

Si has a diamond lattice structure as shown in figure 2.11a. The diamond structure can be seen as two interpenetrating FCC lattices with one of it displaced from the other one by one-fourth along the diagonal [16].

2.7 Pure Silicon from sand

Even though pure silicon does not exist in nature its raw material in the form of sand, quartzite or silicon dioxide (SiO_2) is abundant almost everywhere [5]. To reduce SiO_2 to metallurgical grade silicon (MG-Si) it must react with coke (coal) in an electric-arc furnace at a very high temperatures ($\sim 1800\ ^{\circ}\mathrm{C}$) according the following reaction [15].

$$SiO_2 + 2C \longrightarrow Si + 2CO \tag{2.33}$$

The overall reaction shown in equation 2.33 looks like a simple one however the actual reaction is far more complex as shown in the figure 2.12 below.

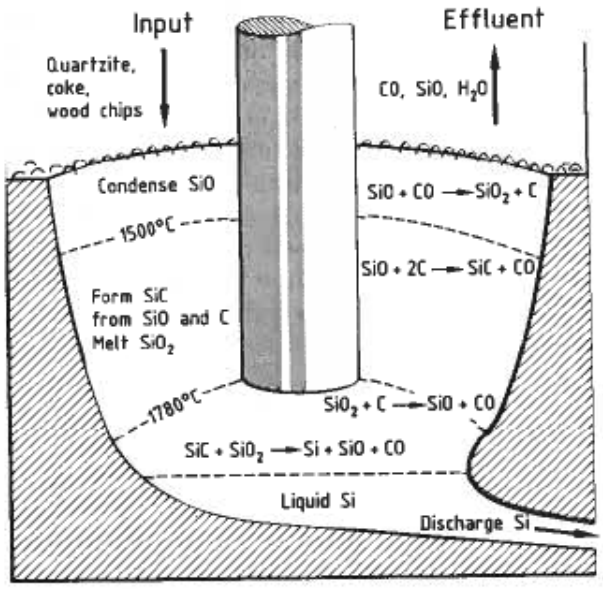

Figure 2.12: Schematic diagram of production of MG-Si using electric arc furnace [13].

This common industrial process produces a MG-Si with purity about $98 - 99\ \%$ which has a number of uses in industries to make special steel and alloys. Even though this process is relatively cheap both in production energy and cost this product contains many impurities which makes the MG-Si level of purity is not sufficient for electronic applications [6].

As it was mentioned before the electrical properties of semiconductor devices are influenced by small percentage of dopant atoms in the crystal this means the number of impurities in the starting material must be less than the amount of dopant in order the device to be built which is the EG-Si must be highly pure. Therefore the MG-Si must be purify further till the impurity level become less than $0.1\ \mathrm{ppma}$ to get a semiconductor (electronic) grade silicon (EG-Si) as follows [15],

$$Si + 3HCl \longrightarrow SiHCl_3 + H_2 \tag{2.34}$$

Then using fractional distillation we can separate the trichlorosilane ($SiHCl_3$) from the other impurities then converted in to a ultra pure EG-Si in solid form by the following reaction [15],

$$SiHCl_3 + H_2 \longrightarrow Si + 3HCl \tag{2.35}$$

The reaction in equation 2.35 is the final solidification step of the conventional purification processes used by semiconductor industry shown in figure 2.13. The most common way to produce a very high quality of Si is by thermal decomposition of saline. The reaction takes place in the presence of a thin $(0.5\ \mathrm{cm})$ seed rod of ultra pure Si heated to about $1100\ ^{\circ}\mathrm{C}$. Therefore when the compound hit the rod they decompose in to an elemental silicon which then deposit by the technique called CVD in to the rod until the desired thickness

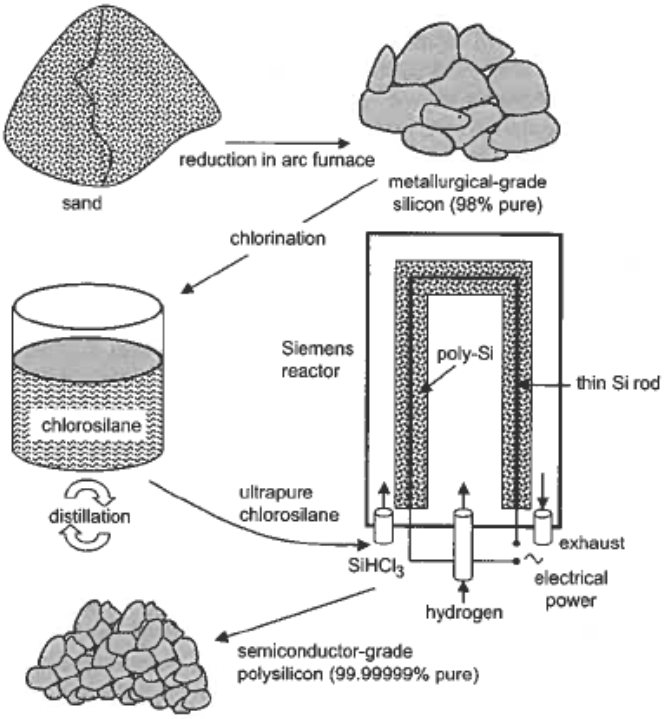

Figure 2.13: The conventional purification process used by the semiconductor industry to get ultrapure Si from sand [5].

is achieved (usually about $12.5\ \mathrm{cm}$ in diameter). The end product of this technique called Siemens process will be a poly-crystalline Si [5].

2.8 Crystalline Semiconductors

The dominant issue of the photovoltaic industry is to fabricate solar cells in large volumes that are both highly efficient and cost-effective. Solid materials are classified into amorphous, or crystalline based on the way the atoms in the solid arranged. When the atoms in the solid are arranged randomly they are called amorphous whereas if the atoms are arranged in a highly ordered structure they are called crystalline.

Furthermore crystalline materials can be classified in to singlecrystalline and multicrystalline. The dominant material used today for the majority of the commercially produced solar cells is the Czochralski-grown crystalline silicon (c-Si) in singlecrystalline and block-cast material in multicrystalline form (mc-Si) [24]. We will see more about this two techniques in the following sections.

2.8.1 Singlecrystalline silicon

As it mention above the end product of the Siemens process is a poly-crystalline which is an aggregate of micro-crystals and no special attention is given to its crystallographic structure besides its purification at this stage. However the progress of solid state device technology has depended not only on the development of device concepts but also on the improvement of quality of the materials from which it is made therefore a specific crystallization techniques are usually applied to get a material with appropriate properties that can be use for production of different semiconductor devices.

Single-crystalline silicon have minimal defects and is of superior quality result in a higher solar-cell efficiencies in comparison to multi-crystalline silicon. Shown in figure 2.14 the Czochralski (CZ) method is the most common crystallization method used by both the microelectronic and PV industries to convert the ultra pure polycrystalline Si (EG-Si) into single crystalline ingot [5].

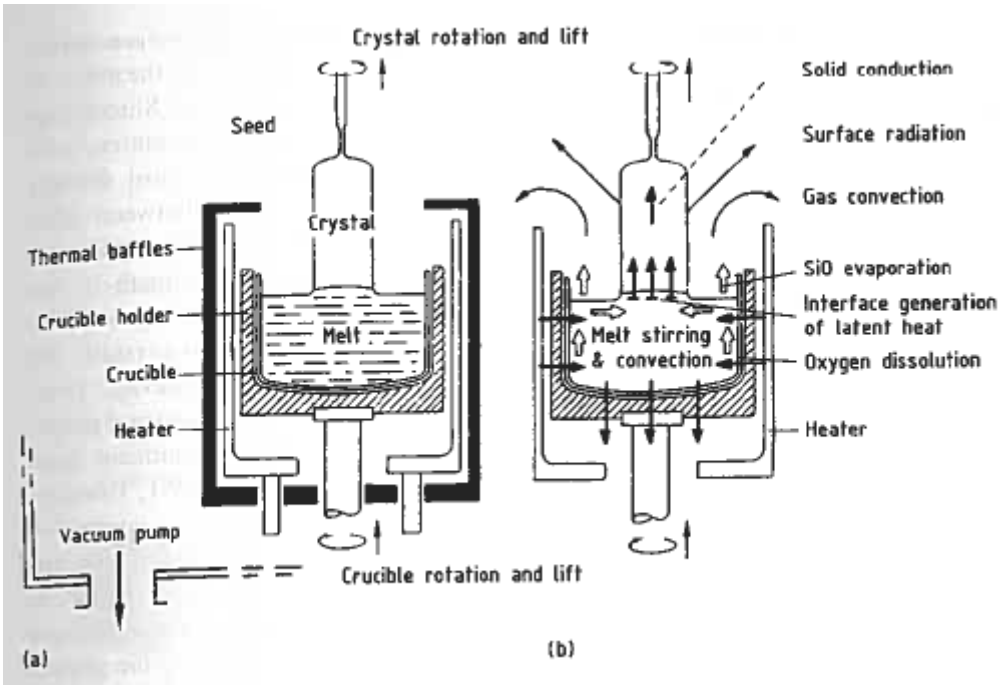

Figure 2.14: The Czochralski silicon crystal puller (a) the component of the hot zone (b) Heat flow(➡) and oxygen transport(⇨) during crystal growth [13].

In the CZ crystal growth, the the ultra-pure MG-Si will be melt with a precise amount of dopant such as P for n-type and B for p-type at about $1414\ ^{\circ}\mathrm{C}$, just above the melting point of Si. A small and thin single-crystal seed mounted in a rotating shaft is used to start the crystallization process [13]. Then the seed will be lowered and make a contact with the melt then pull out very slowly. The temperature will be controlled so that the melt silicon will solidify on the seed according to the crystallographic structure of the seed. The growth rate for CZ method is about $5\ \mathrm{cm/h}$ and the end result typically for

cylindrical ingots are $1\ \mathrm{m}$ long and $20\ \mathrm{cm}$ in diameter [5].

2.8.2 Multicrystalline silicon

Multicrystalline (MC) material consists of multi-grained structure with inclined crystal planes that meet at grain boundaries. The grain size vary for different crystallization techniques but usually it has a size between several millimetres to centimetres.

Even though there exists different techniques for the production of MC-Si the dominating techniques are based on directional solidification which has a cost benefit over Cz single crystalline silicon. The electronic industry only uses single crystalline silicon due to high quality requirements however the PV industries uses both single crystalline and multi-crystalline silicon.

MC-Si besides single crystalline silicon represents the basis of today's photovoltaic technology and it is not going to be far that MC-Si will be the standard material for PV cells. As it was mentioned above at a small cost of efficiencies MC-Si offers advantages over single crystalline silicon with respect to manufacturing costs and feedstock tolerance. Another inherent advantage of MC-Si is the rectangular or square wafer shape yielding a better utilisation of the module area in comparison to the mostly round or pseudosquare single crystalline wafers [24].

Eventhough until recently SC-Si solar cell was dominant in the PV industries, due to the fact that the lower production cost of the multicrystalline silicon ingot compared to single crystalline silicon the production volume of solar cells using multicrystalline silicon has recently exceeded the production volume from single crystalline silicon solar cell however, multicrystalline silicon has a major drawback, the presence of structural defects such as dislocation or grain boundaries [19].

2.9 Crystal Defects

It is impossible to find a defect free crystal. Crystals always contain some kind of lattice defects in their structure, however the density of defects is much higher in multicrystalline materials. If the regular patterns in crystalline materials interrupted by crystallographic defects the crystalline solid is said to be contain defects. Even though most of the time defects are introduce during solidification sometimes defects can be introduce intentionally to change the properties of a given material[11]. Usually lattice defects are categorizes according to their dimensions in to four as follows.

1. Point defects (zero dimensional) such as vacancies and self interstitial
2. Line defects or dislocation (one dimensional) such as edge and screw dislocations

3. Surface defects (two dimensional) such as stacking faults, twin and grain boundaries
4. Volume or bulk defects (three dimensional) such as inclusions and voids

Since our main focus is MC-Si we will only see in the next subsection the most popular defect in MC-Si which is planer defects

2.9.1 Surface defects

Planer defects are form when two homogeneous single crystal regions of different orientation interfaces. Grain boundaries, stacking faults are example of planar defects.

2.9.2 Stacking faults and Twin boundaries

Stacking faults and twin boundaries are produced when a long range stacking sequence is disrupted. staking faults are produce if the change in the stacking sequence is over a few atomic spacing whereas twin boundaries will be form if the change is over many atomic spacings [16].

2.9.3 Grain Boundaries in MC-Si

Even though most of the the defects mention above are found in single crystalline materials generally solids consists a number of crystallites or grains. A MC-Si is a material consisting of many Si grains however each grains are a single crystaline Si. Depending on the cooling rate grains size can range from from nm to mm. Since the orientation of each grains are different from its neighboring when each grains comes together to form a MC-Si a boundary will be form. The transition region where one grain stops and another grain begin is known as grain boundary. As it mentioned above grain boundary is an example of planer defects and is one of the dominant defects in mc-Si which has a great effect in the efficiency of the solar cell [16].

2.10 Resistivity measurement

As it was mentioned in the previous part, materials can be categorized based on different properties. One of these properties is electrical resistivity, which is represented by the Greek letter (ρ), a key physical property of all materials that describes how much the material resists to the flow of electricity (charges). The electrical resistivity of a material is an intrinsic physical property, which is independent of the particular size or shape of the sample [21]. Based on this materials can classified as metals, semiconductors and

insulators. Since metals have a lot of free electrons it has a low resistivity to the flow of electricity. On the contrary semiconductors at 0 K and insulators have a high resistivity to the flow of electricity. However as it was mentioned earlier the valance electrons bonded by covalent bond in semiconductors can be thermally or optically freed (excited) to the conduction band so that this freed electron will contribute to the flow electricity as a consequence the resistivity of the semiconductor will be decreased.

Since the resistivity of different materials varies over a large order of magnitude (over 20) no single technique or instrument can measure resistivity over this wide range therefore we need different instrument or technique to measure the resistivity of a given material [21].

Resistivity of a given material can be measured either using a two-point or a four-point measurement. By making two contact, which is sourcing current through the two probes and measuring the potential deference (voltage) across the two probes, we can measure the resistivity of a given sample and it is called two-point measurement. However if the contact resistance becomes comparable to sample resistance it is preferable to use a four contact called four-point measurement, which separates the current and the voltage contacts.

The advantage of using four probes over two probe is, using four probes eliminates measurement errors due to the probe resistance, the spreading resistance under each probe, and the contact resistance between each metal probe and the semiconductor material [23]. Since the voltmeter has very high impedance there is only very little sense current pass through the voltmeter that is almost all the input current passes through the resister of the material under investigation to the other terminal of the current source.

The resistivity of a given sample can be calculated using

$$\rho = G(\frac{V}{I}) \tag{2.36}$$

were $\frac{V}{I}$ is the resistance of the sample and G is a correction factor dependent on the shape and dimension of the sample as well as the arrangement of electrical contacts [22].

Here we will use the most common way of measuring the resistivity of a semiconductor material which is the four-point collinear probe.

2.10.1 Derivation of resistivity

The resistivity of a material can be obtained by measuring the resistance and physical dimensions of the material, so lets drive the relation between resistance and resistivity of a conductor of cross-sectional area A carrying a current I as shown in figure 2.15.

The current density J in the conductor is given as

$$J = \frac{I}{A} \tag{2.37}$$

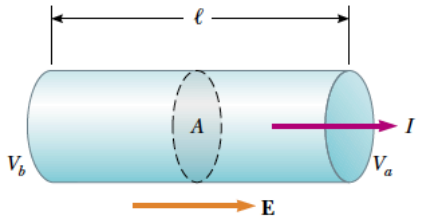

Figure 2.15: A uniform conductor of length l and cross-sectional area A. A potential difference $\Delta V = V_a - V_b$ maintained across the conductor sets up an electric field E, and this field produces a current I that is proportional to the potential difference [25].

However J is proportional to the electric field with a proportionality constant σ called the conductivity of the conductor as follows

$$\mathbf{J} = \sigma \mathbf{E} \tag{2.38}$$

However $\sigma = \rho^{-1}$ were ρ is the resistivity of a material therefore from equation 2.38 we get

$$E = \rho J \tag{2.39}$$

Equation 2.39 is one form of Ohms law. Now consider the uniform conductor shown in figure 2.15. A potential difference $\Delta V = V_a - V_b$ can be calculated as follows

$$\Delta V = V_a - V_b = -\int_a^b \mathbf{E} \cdot ds = E \int_0^l dx = El \tag{2.40}$$

Substituting the value of E from equation 2.39 and the value of J from equation 2.37 in to 2.40 we get

$$\Delta V = l\rho J = l\rho \frac{I}{A} = (\frac{l\rho}{A})I = RI \tag{2.41}$$

were equation 2.41 is another form of Ohms law and R is the resistance along the length l of the conductor and is given by

$$R = \rho \frac{l}{A} \tag{2.42}$$

2.11 Four-Point Collinear Probe Method

As it was mention above for measuring the resistivity of a MC-Si we use a four-point collinear probe. Figure 2.16 shows the schematic of four-point collinear probe measurement technique for measuring the resistivity of a given sample. The four-point collinear probe technique uses four equally spaced in line individually spring loaded probes, were two of the probes used as a current source and current sink while the other two uses to

measure the potential drop across the surface of the sample. Typical values for the tip spacing range from $0.5 - 1.5$ mm.

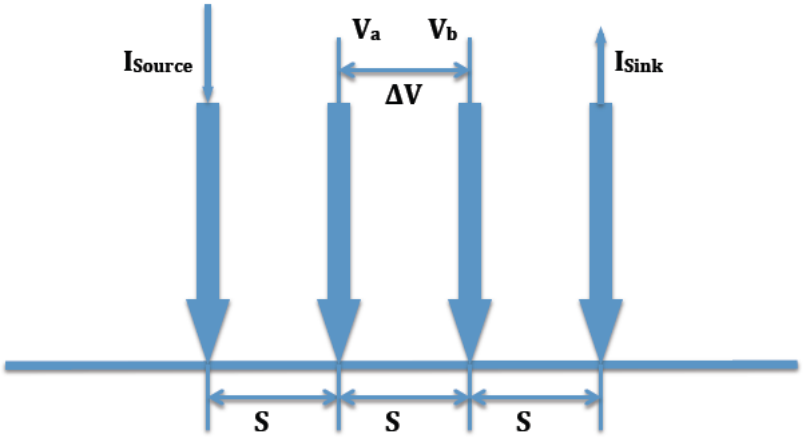

Figure 2.16: In-line four-point probe measurement setup.

Since we are going to use the jandel RM3-AR test unit in combination with the multi-height probe stand for general purpose measurement the system can measure either bulk or thin film specimen, each of which consists of a different expression. With the known current and measured voltage, the resistivity for bulk and thin samples will be calculated as follows,

2.11.1 Bulk Sample

For bulk samples we assume that the metal tip is infinitesimal and the sample being measured is semi-infinite (that is the thickness (t), width and length of the sample are each much greater than the probe spacing (s)). Therefore we can assume the current emanates in a spherical form from the outer probe tips then the resistivity can be calculated as follows,

The differential resistance from equation 2.42 will be

$$dR = \rho\Big(\frac{dx}{A}\Big) \tag{2.43}$$

We carry out the integration between the inner probe tips where the voltage is measured

$$R = \int_s^{2s} \rho\Big(\frac{dx}{2\pi x.x}\Big) = \int_s^{2s} \rho\Big(\frac{dx}{2\pi x^2}\Big) = \frac{\rho}{2\pi}\Big(-\frac{1}{x}\Big)\Big|_s^{2s} = \frac{\rho}{2\pi}\Big(\frac{1}{2s}\Big) \tag{2.44}$$

Due to the superposition of current source and sink at the outer two tips, R = V/2I. Thus, we arrive at the expression for bulk resistivity

$$\rho = 2\pi s\Big(\frac{V}{I}\Big) \tag{2.45}$$

2.11.2 Sheet resistivity for thin sample

Eventhough we use FPP to measure a bulk sample as it was mention before however in the case of microfabrication environment when the thickness (t) of the sample is much less than the tap spacing (s) which is mostly applied for the equation for resistivity can be can be calculated as follows,

For a very thin layer (thickness $t \ll s$) we get current rings instead of spheres. Therefore the expression for the area will be $A = 2\pi x.t$. Then by substituting A in to equation 2.43 and integrating both sides we get

$$R = \int_{s}^{2s} \rho\Big(\frac{dx}{2\pi x.t}\Big) = \frac{\rho}{2\pi t}\int_{s}^{2s}\Big(\frac{dx}{x}\Big) = \frac{\rho}{2\pi t}\Big(\ln x\Big)\Big|_{s}^{2s} = \frac{\rho}{2\pi t}\Big(\ln 2\Big) \tag{2.46}$$

Consequently, for R = V/2I, the sheet resistivity for a thin sheet will be

$$\rho = \frac{\pi t}{\ln 2}\Big(\frac{V}{I}\Big) = \frac{\pi t}{\ln 2}\Big(R\Big) \tag{2.47}$$

Chapter 3

Experimental techniques

3.1 Multi height four point probe

In this experiment we measure the resistivity of a multi-crystalline silicon (MC-Si) samples from different position of the ingot by a four point technique using a Jandel multiheight four point probe which can be use to measure samples of different thickness from wafers to ingots upto 6 inch high. As shown in the figure 3.1a the instrument comprises a $29\ \mathrm{cm}$ deep, $25\ \mathrm{cm}$ wide and $0.8\ \mathrm{cm}$ thick hard anodized aluminum alloy base with a usable area for sample of $25\ \mathrm{cm}$ by $25\ \mathrm{cm}$ and a vertical column of $19\ \mathrm{mm}$ diameter stainless steel column of $20\ \mathrm{cm}$ high screwed to the base which uses to support the probe head raising and lowering mechanism incorporating the vertical slide which carries the probe head, operating lever shaft and micro switch.

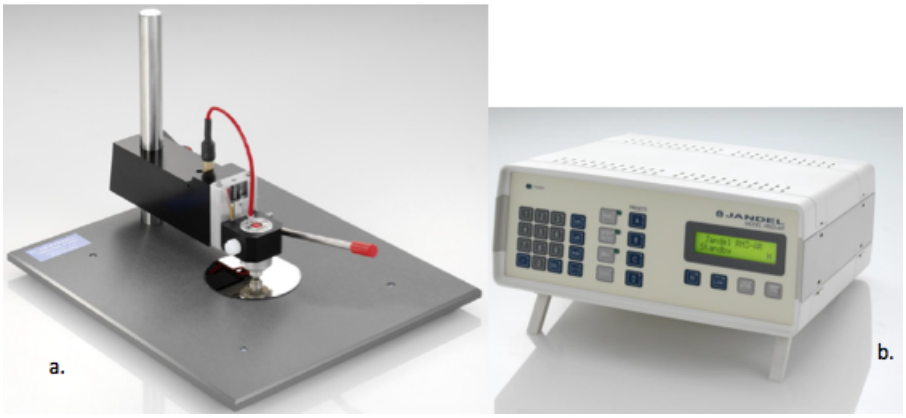

Figure 3.1: Jandel multiheight four point probe

The probe head have a cylindrical shape of $200\ \mathrm{g}$ in size with four pointed in line probes as shown in figure 3.2. The tip radius is $40\ \mu\mathrm{m}$ made from tungsten carbide with spacing

of $s = 1\ mm$ from each other. The probe head are electrically connected to the electronic equipment (RM3-AR) shown in figure 3.1b which supplies a constant DC measuring current and displays the measured output voltage. The RM3-AR test unit shown in figure 3.1b combined both a constant current source and a digital voltmeter and we use it in combination with the multi-height four point probe to measure the resistivity of the sample. The test unit supplies a constant current and measures either the the voltage drop or the sheet resistance of the sample depending on which function we choose.

Figure 3.2: In-line Jandel cylindrical probe head

3.2 Procedure for setting up the instrument

The four-point probe method is the most common way to measure a semiconductor materials resistivity. Two of the probes are used to source current and the other two probes are used to measure voltage. This technique involves bringing four equally spaced probes into contact with the material of unknown resistance. The probe array is usually placed in the center of the material, as shown in figure 3.3.

Before starting taking data we have first to follow the following procedure to setting up the instrument,

- Put the sample to be measured on the stage
- Set the height of the probe head raising and lowering mechanism. To assist this a dummy probe head is used to avoid the risk of breaking the real probe head needles. Make sure its top is in level with the probe head mounting block and clamp the dummy probe head by the red thumb screw on the left of the head mounting block .
- Lower the probe head slide fully using the long lever until the micro-switch operates

- Lower the whole assembly by sliding it down the vertical column until the tip of the dummy probe head touches the sample then then tighten the real clamp to fixed the height.
- Raise the probe head slide using the long lever and unclamp the dummy probe head by the red thumb screw on the left of the head mounting block
- Insert the real probe head and make sure its top is in level with the top of the mounting block
- Attach the connecting lead marked 4PL to the 9-way plug at the rear of the assembly and secure it by the locking screws
- Finally plug the lead in to RM3-AR test unit at the real

3.3 Resistivity measurement

The first step was measuring the the MC-silicon wafer thickness and the dimensions then the resistivity with four-point probe. The samples are $5\ \mathrm{cm}$ by $5\ \mathrm{cm}$ with a thickness $\mathrm{t} = 0.022\ \mathrm{cm}$ MC-Si. Since the spacing of the probes is $\mathrm{s} = 0.1\ \mathrm{cm}$ the ratio of t and s will be $\mathrm{t/s} = 0.22$ which is $t \ll s$ therefore we use the following two equations for our calculation of sheet resistance (R_s in $\Omega/\square$) and resistivity (ρ in $\Omega\ \mathrm{cm}$) of wafers and films.

$$\mathrm{R_s} = \mathrm{R}\left(\frac{\pi}{\ln 2}\right) \approx 4.532 \times \left(\frac{\mathrm{V}}{\mathrm{I}}\right) \tag{3.1}$$

and

$$\rho = \mathrm{R_s} \times \mathrm{t} = 4.532 \times \left(\frac{\mathrm{V}}{\mathrm{I}}\right)\mathrm{t} \tag{3.2}$$

where t is the thickness of the sample in cm, I is the current source supplied by the RM3-AR system unit being passed between the outer probes and V is the voltage measured across the two inner probes.

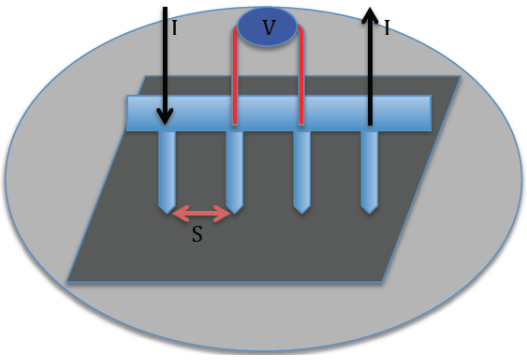

Figure 3.3: Schematic of Four-Point Probe

The sample was put in x or y micrometer translation stage and measurements was taken for each point, with a spacing of $0.1\ \mathrm{mm}$ or $0.2\ \mathrm{mm}$ across each of the samples with the probe pins in parallel or in line with the measured direction both in forward and reverse direction and will fed the data into a personal computer. For every sample we choose an appropriate current range by selecting the auto button by pressing the standby button twice and we use this auto current as a reference and choose current source for our measurement. After we take a measurement we took a microscopic image of the samples to correlate the data taken to the point on the sample

As we know when the FPP make a contact with the sample the contact should be ohmic which is the potential drop across the sample should be directly proportional to the current source which supplied by RM3-AR test unit should be linear which is $V \propto I$ with a proportionality constant R called the resistance of the sample under test. To show this for example for sample R9-Q3-227 we take one point in the sample and take the potential drop in forward and reverse direction for a range of current source then we calculate the average of the potential drop of the forward and reverse. The result of this will be graphed which is the current source verses average potential for each current source to see whether the contact is ohmic.

As it was mention in chapter 2 when we make simple resistance measurements using a two wire we are also including the resistance of the contact point of the wires with the sample. If we assume that the contact resistance is very small comparing to the sample resistance we can ignore it. However when we measure a sample with a very small resistance the contact resistance can be a dominant and have n effect on the resistance of the sample. In such cases it is more advantageous to use four wire which will eliminates measurement errors due to the probe resistance, the spreading resistance under each probe, and the contact resistance between each metal probe and the semiconductor material as shown in the circuit diagram in figure 3.4 [23]. Since the voltmeter has very high impedance there is only very little sense current pass through the voltmeter therefore almost all the input current passes through the resister of the material under investigation to the other terminal of the current source.

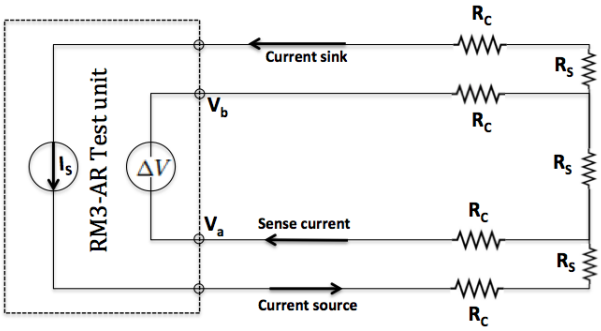

Figure 3.4: The circuit diagram of the multi-height four point probe with RM3-AR test unit

Were I_s is the current source, R_c the contact resistance and R_s the resistance of the sample.

3.4 Procedure for resistivity measurement

After we setting up the instrument we follow the following procedure to measure the resistivity of the sample

- Place the sample under the probe head
- Lower the probe on to the sample
- Switch on the test unit by the switch found on the back of the RM3-AR test unit and will caliber it self and will be in standby
- Press the standby again to choose auto range current source or use the keypad to input a desired current source then press the FWD for the forward and REV button for the reverse current source. Usually up to four commonly used current source can be stored in the A to D preset buttons
- Take the reading of the measured potential both for forward and reverse we should get almost the same result for both direction of current except a negative value for the reverse direction. we can also get the sheet resistance by pressing the $\Omega/\square$ button.
- Multiply the calculated resistance which is $\dfrac{\mathrm{V}}{I}$ from the data by $\frac{\pi}{\ln 2}$ to get the sheet resistance, in $\Omega/\square$, of the sample under measurement or press the $\Omega/\square$ button to get directly the sheet resistance.
- Finally multiply the sheet resistance by the thickness of the sample (t), in cm. This will be the resistivity of the of the sample, in $\Omega\ \mathrm{cm}$

  We use two types of translation when we measure the resistivity. The first one is when the inline pins are in parallel to the direction of motion of the translation stage and the second one is when the inline pins are perpendicular to the direction of motion of the stage.

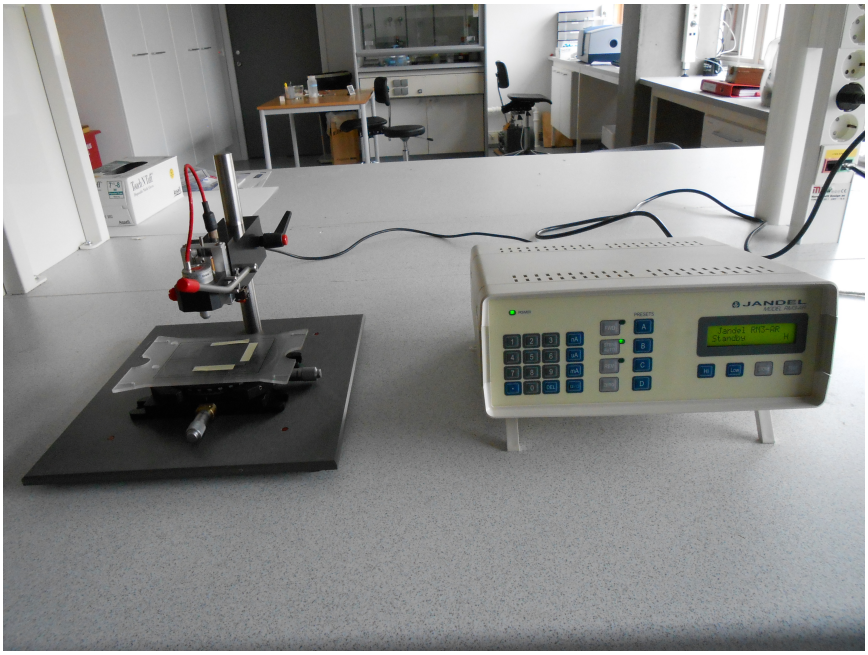

Figure 3.5: Experimental setup with a sample in the translation stage

Chapter 4

Results and discussion

In this chapter we will present the result of the measurements made on the samples using four-point probe in a dark and discuss the results of our findings of the resistivity of the different samples in a graphic form and see how the grain boundaries influences the resistivity of the mc-Si. We measured with translation both $\parallel$ and $\perp$ to the probe array and found at least two distinct behaviors which is a high voltage when a pin is on the grain boundary and an increase in ρ when we approach a different grain. Resistivity measurements have been done on samples from different position of an ingot. The samples that are considered in this experiment are R9-Q3-226, R9-Q3-227, R9-Q3-142, R9-Q3-143, R9-Q3-057, R9-Q3-058.

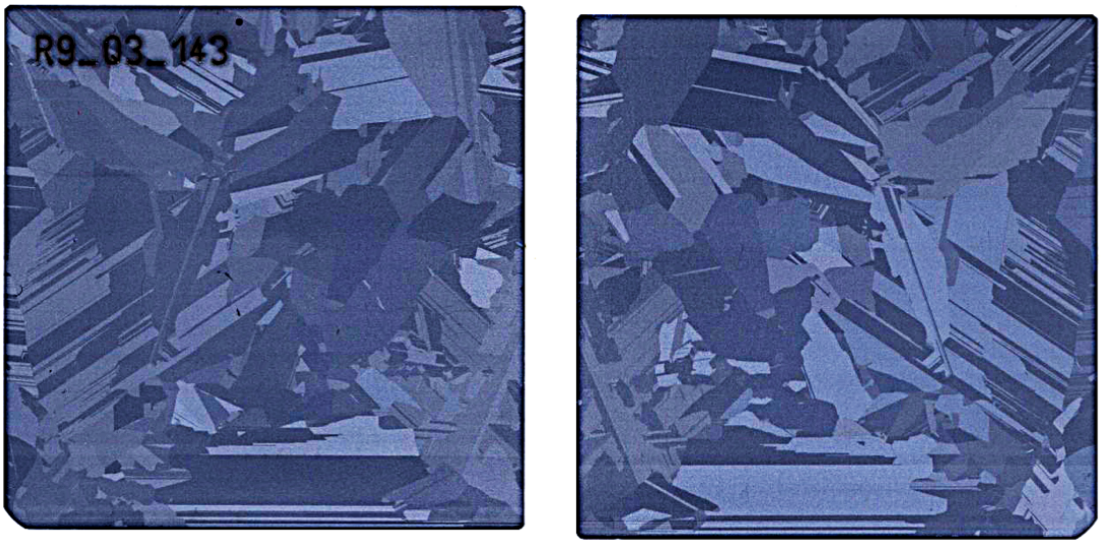

Figure 4.1: The front (left) and back (right) sides of R9-Q3-143 mc-Si sample.

The first step of this experiment was taking a scan of the samples and here we present as an example two of our samples as it can see in figure 4.1 and 4.2 shows the front (left) and back (right) sides R9-Q3-143 and R9-Q3-142 mc-Si samples respectively. Then we took

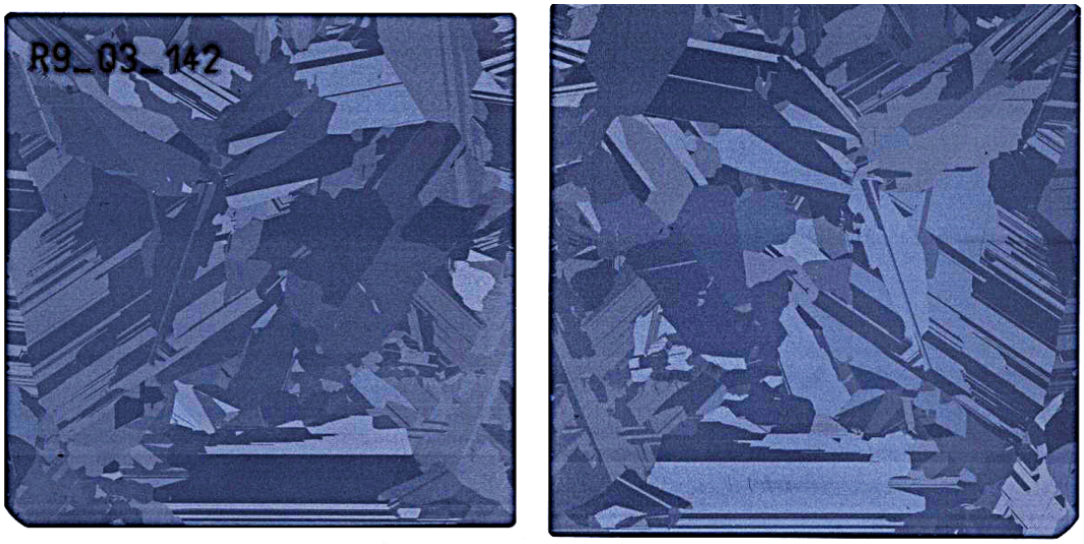

Figure 4.2: The front (left) and back (right) sides of R9-Q3-142 mc-Si sample.

measurements of dimension of the samples. We use a millimeter scale to measure size of the samples. And for all the samples we get the size is 50×50 mm and using digital micrometer we measure the thickness and got the thickness of the samples is 220 μm. Then we use ultrasonic solvent to clean the dirt in the samples.

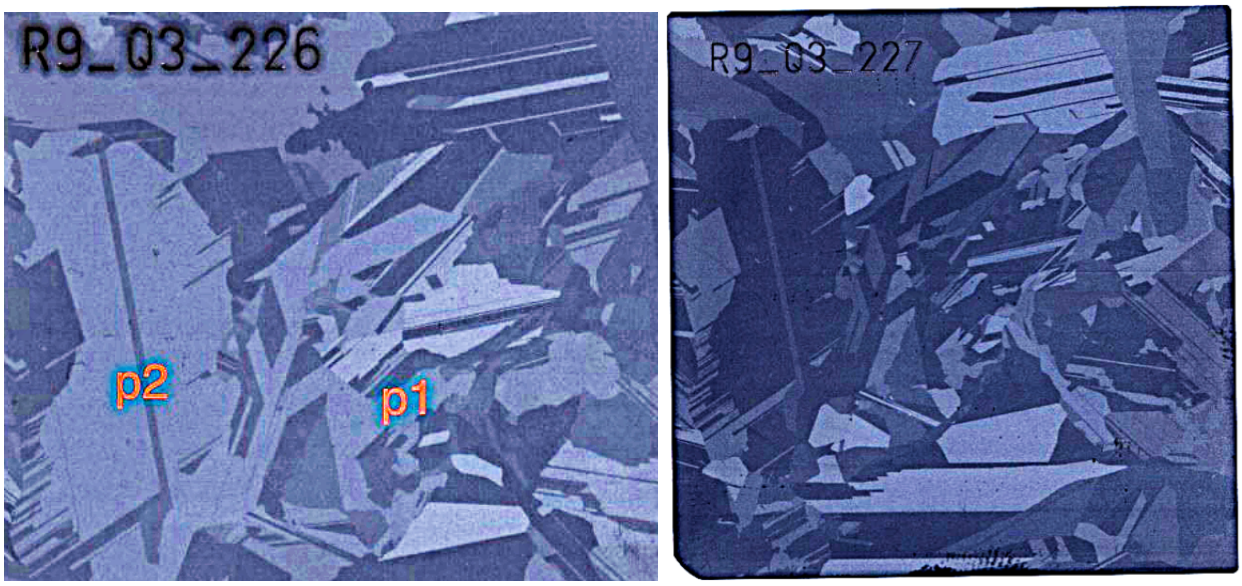

Figure 4.3: The front sides of R9-Q3-226 (left) and R9-Q3-227 (right) mc-Si sample.

Figure 4.3 shows the front sides of R9-Q3-226 (left) and R9-Q3-227 (right) mc-Si sample in which the data was taken for the resistivity measurement. The data for the graph in figure 4.4 was taken using a 4-point probe and DRT-Osciloscope and SM for Multicrystalline Si(R9-Q3-226) for single point which is p_1 shown in figure 4.3 (left) were as the

data for the graph in figure 4.5 was taken from sample R9-Q3-227 shown in figure 4.3 (right) to show whether the contact made between the the tip of the four-point probe and the mc-Si is ohmic [4] and as you can see from the graph the result is linear with an average resistance $4.385\ \Omega$ and $4.276\ \Omega$ respectively. However as you can see from the graph we got more linear for the data taken by the multi-height four-point probe than the data taken using the Model S-301 four-point probe.

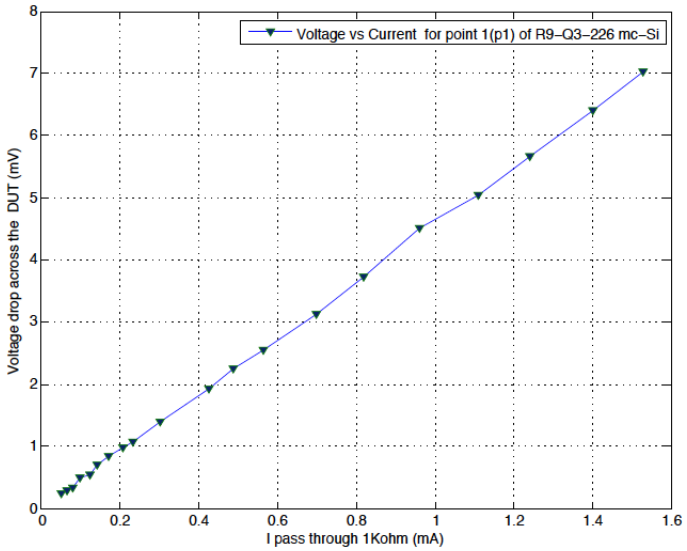

Figure 4.4: Current verses voltage for R9-Q3-226 mc-Si sample taken with S-301 four-point probe

Each samples was placed on the top of x or y stage which we use to locate the relative positions during the measurement. Data was taken across each of the samples with the probe pins either in perpendicular or parallel to the direction of mothion of the samples. The potential drop was measured for a give current source for each point, with a relative spacing of $0.1\ \mathrm{mm}$ or $0.2\ \mathrm{mm}$.

Figure 4.6 shows the resistivity of R9-Q3-227 mc-Si versus relative position when the data was taken when the probe moves parallel to the direction motion of the sample. The data was taken in a space of $0.2\ \mathrm{mm}$ and for each point we took two measurements both in forward (FWD) and reverse (REV) direction with a current source $1\ \mathrm{mA}$ and $2\ \mathrm{mA}$. We got the value potential drop in both directions more or less similar which is as it was expected. After we find the average value of the FWD and REV potential drop we calculated the resistance using equation 2.41 for both current sources by averaging this value we got the average resistance for each point . The resistivity for each point was then determined using equation 2.47 considering the thickness (t) of the sample from table 4.1 in cm. Since the spacing s between the tips of the probe is $1\ \mathrm{mm}$ and the relative position of each point has a spacing of $0.2\ \mathrm{mm}$ the position of the inner probes are at points 6 and 11 as shown by the rectangular box with a tip in figure 4.6. The box indicates the position of the inner pins in the sample corresponding to the first and last points on the graphs.

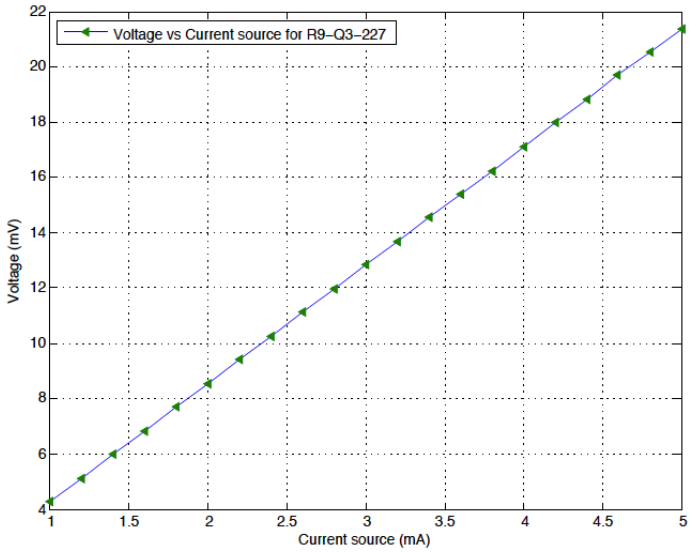

Figure 4.5: Current verses voltage for R9-Q3-227 mc-Si sample taken with Jandel multi-height four-point probe

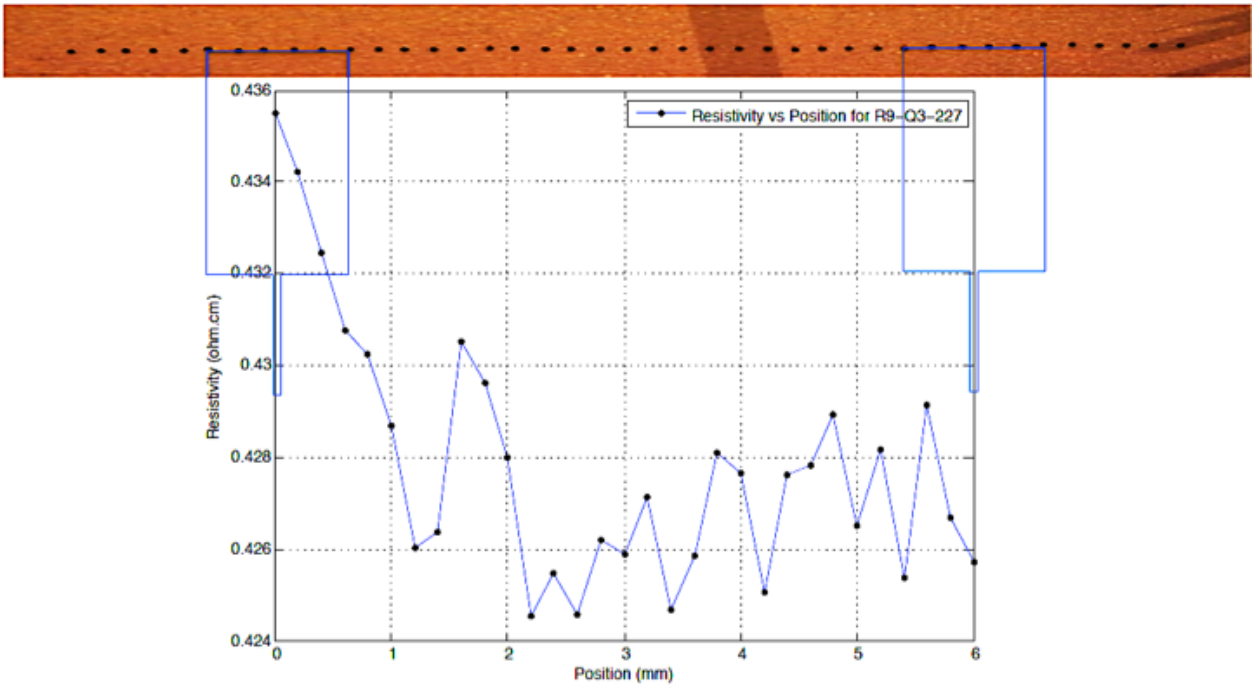

Figure 4.6: Resistivity versus position for R9-Q3-227 mc-Si sample the data was taken in which the direction of translation of the sample is $\parallel$ to the probe array

As it can be seen in figure 4.3 the data for figure 4.6 was taking from two grains separated by a twin boundaries. The data was taken in which the direction of translation of the sample is $\parallel$ to the probe array and as shown in the graph we can see the resistivity starts with a higher resistivity. As it can be seen in appendix figure **??** there is a another grain

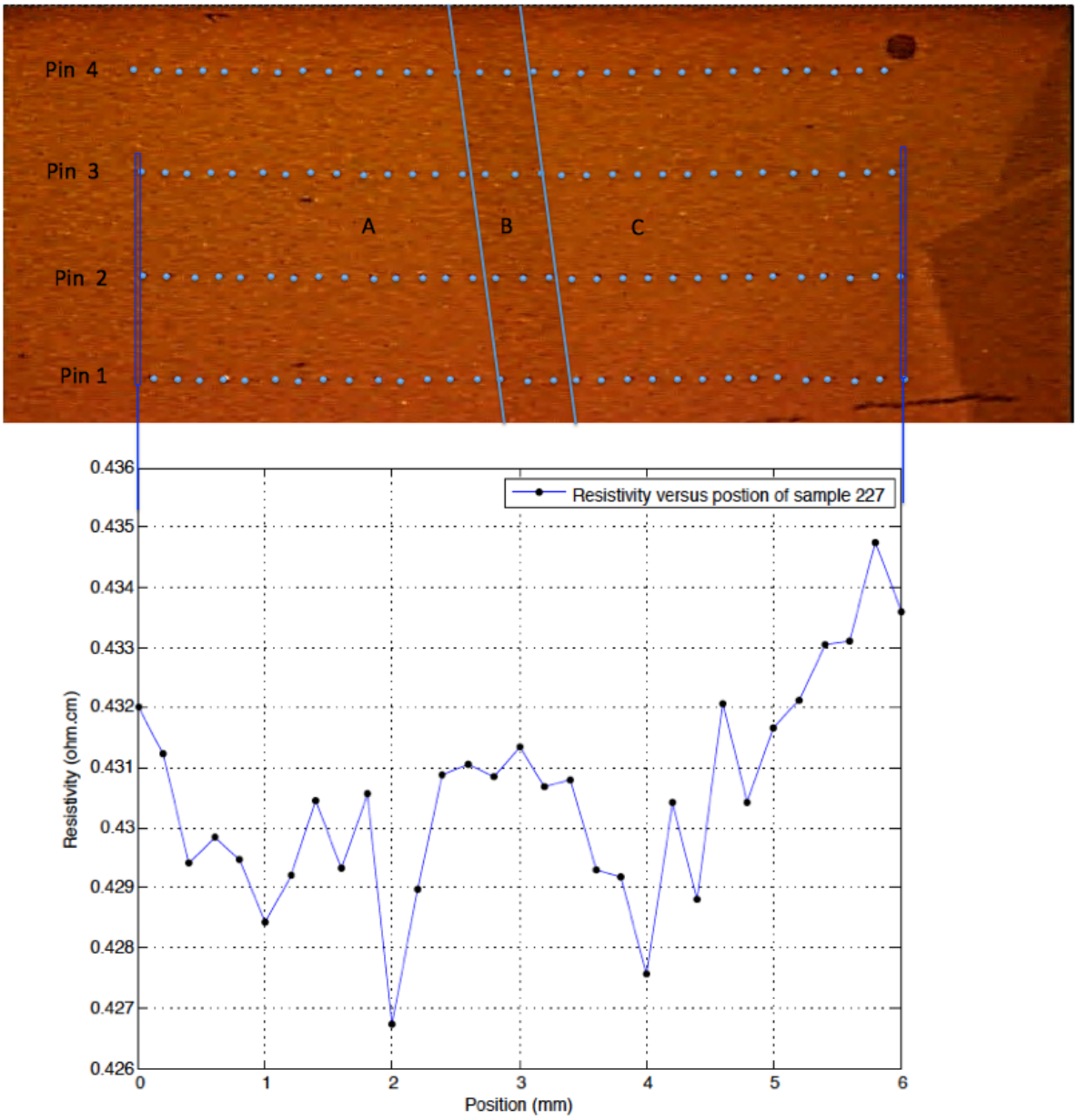

Figure 4.7: Resistivity versus position for R9-Q3-227 mc-Si sample the data was taken in which the direction of translation of the sample is $\perp$ to the probe array

to the left of the area were our data were taken and this could lead to a strain or high dislocation density near the edge which is also consider to be more defect area introduced during the sample cutting process and starts to fall when we go away from the edge until we reach the bulk resistivity of the grain which is around $0.426\ \Omega\,\mathrm{cm}$ at $1.2\ \mathrm{mm}$ relative position. Then when the first pin hit the twin boundary the resistivity increases to about $0.4305\ \Omega\,\mathrm{cm}$ at $1.6\ \mathrm{mm}$. Immediately after the first pin completely pass the twin boundary the resistivity drops to about $0.4248\ \Omega\,\mathrm{cm}$ at $2.2\ \mathrm{mm}$ which shows the twin boundary does not have an effect unless the pin is on the top of the twin boundary. We see an increase in

resistivity from $3.0\ \mathrm{mm}$ to $3.2\ \mathrm{mm}$ when the second pin is inside the twin boundary then decreases to about $0.4248\ \Omega\,\mathrm{cm}$ at $3.4\ \mathrm{mm}$. When the two inner pins are on the opposite side of the twin boundary we saw a decrease in resistivity at $3.4\ \mathrm{mm}$ which shows there is no potential barrier in the twin boundary. The resistivity of the sample increases to about $0.428\ \Omega\,\mathrm{cm}$ at $3.8\ \mathrm{mm}$ when the third pin is inside the twin boundary. After the third pin passes completely the twin boundary which is when all the three pins are on the other side the resistivity decreases to about $0.425\ \Omega\,\mathrm{cm}$ at $4.2\ \mathrm{mm}$ this decrease in resistivity are due to a barrier induced widening of the current path between the inner pins which lead to a voltage drop[3].

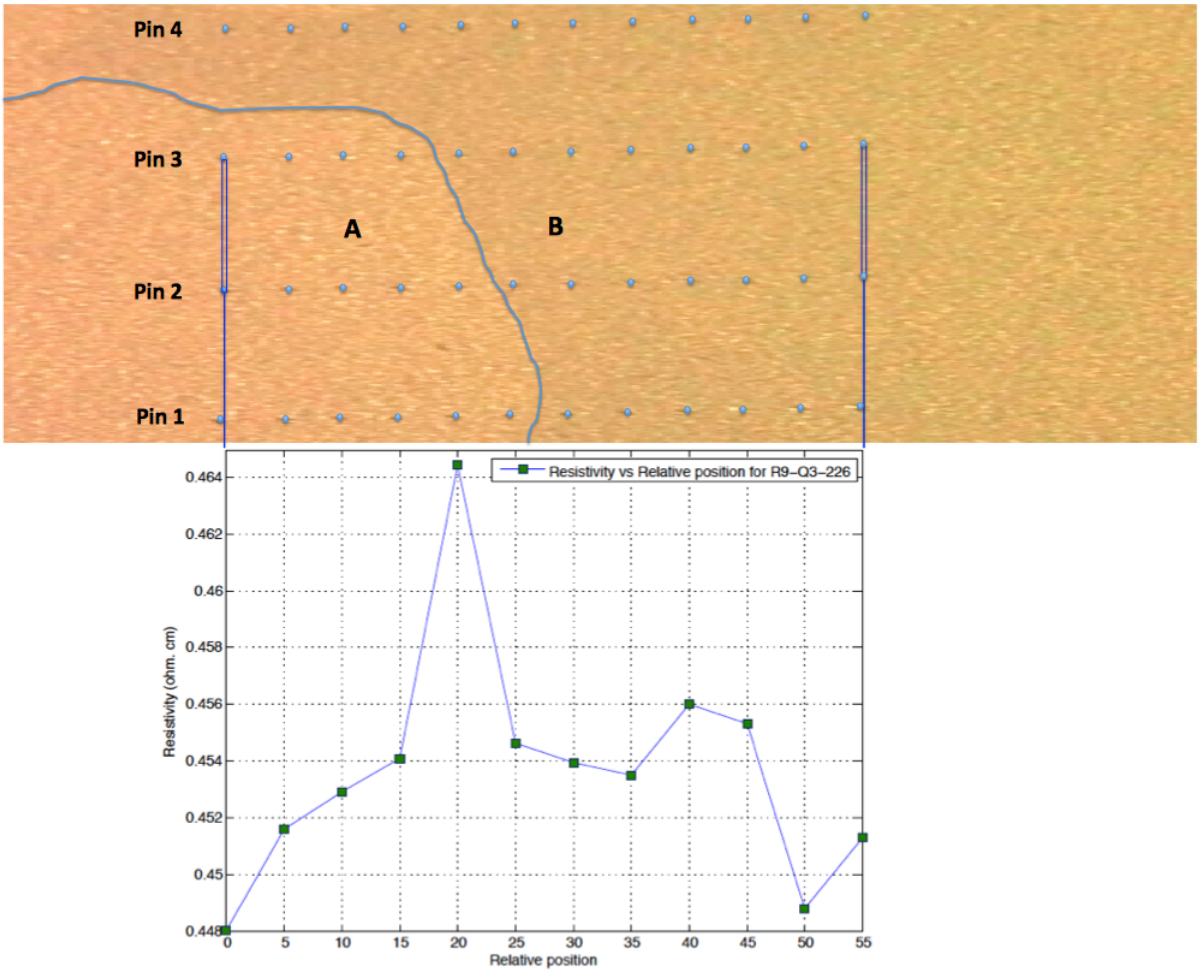

Figure 4.8: Resistivity versus position for R9-Q3-226 mc-Si sample the data was taken in which the direction of translation of the sample is $\perp$ to the probe array

But such kind of measurement which is when the direction of motion of the sample or the stage are in line or parallel to the collinear pins has the following disadvantages

- Pins can put in the same point again and again so it will have an effect on the resistivity for that particular point as it could be damaged by the pins.

- It is more difficult to visualize which points in the graph corresponds to a point in the sample image.

So as shown in figures 4.7, 4.8, 4.9, 4.10 we use a different approach to measure the resistivity to avoid the above mention problems. In this case the direction of motion of the sample or the stage are perpendicular to the collinear pins.

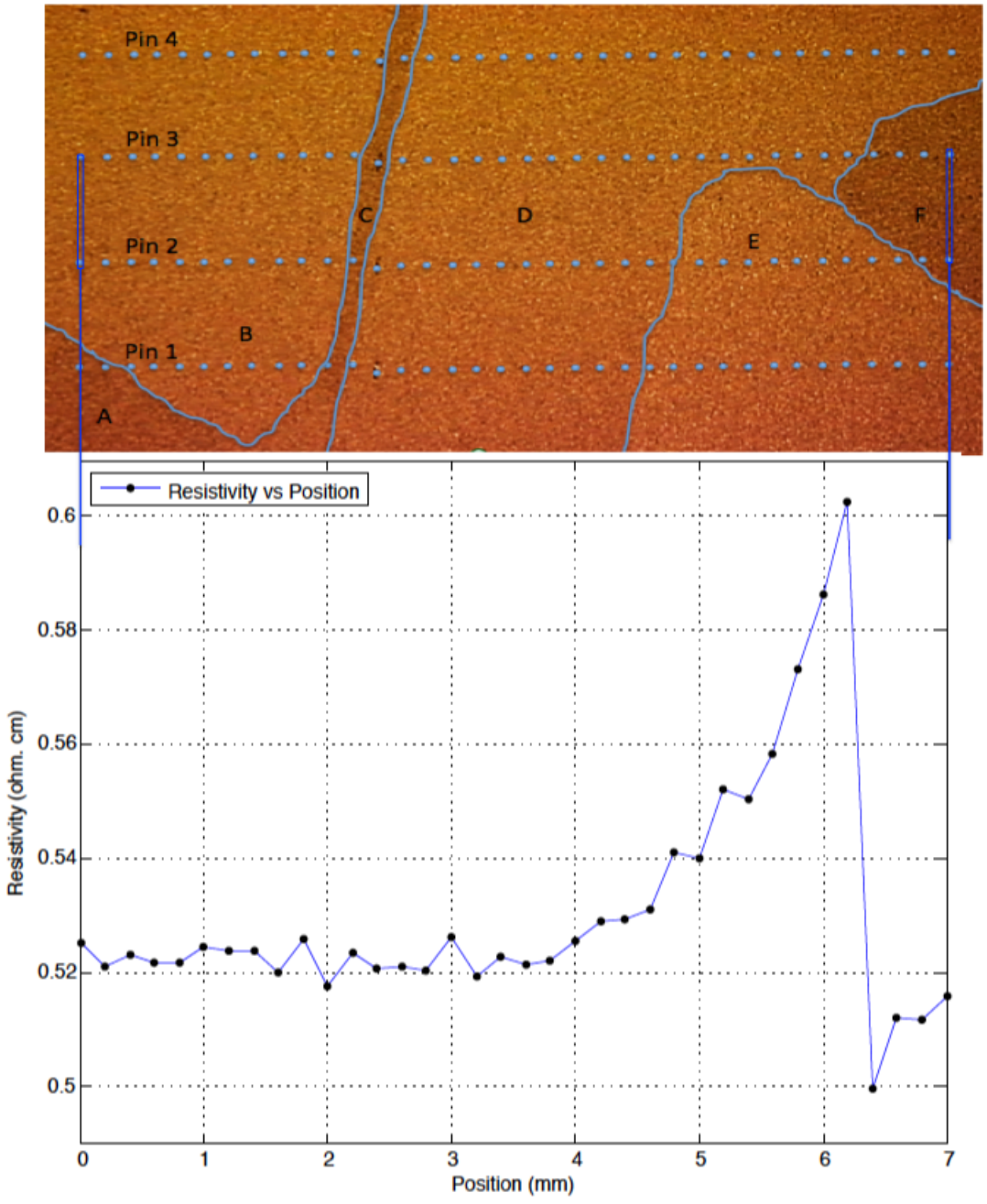

Figure 4.9: Resistivity versus position for sample 143 the data was taken in which the direction of translation of the sample is $\perp$ to the probe array

Figure 4.7 shows the resistivity versus the relative position of R9-Q3-227 mc-Si sample. We again try to see how a twin boundary affects the resistivity of the sample. The resistivity value gradually decreasing when we move away from the high dislocation area near the edge towards area A caused by the strain of the neighboring grain then the resistivity increases when pin 2 and 4 sits on the grain (area B). We found the maximum resistivity value at area B about $0.4314\ \Omega\,\mathrm{cm}$ at position $3.0\ \mathrm{mm}$ when all the pins are with in the grain (area B). Then as the pins emerges from area B to C the resistivity decreases. Finally the resistivity starts to raise to the right possibly due to stress associated high dislocation density when we approaches the grain on the far right. As we can see from the graph there are two points at position $2.0\ \mathrm{mm}$ and position $4.0\ \mathrm{mm}$ which has a lower value than the bulk resistivity and according to Barranco [26] when the measurement is perform parallel to the boundary, the potential difference will be screened by the charge at the GB surface and will give a lower value than the bulk resistivity.

Figure 4.8 also represents the resistivity versus the relative position of R9-Q3-226 mc-Si sample. We choose an area in the sample where two grain boundaries meet and see how its resistivity behave when we cross from one grain to another. Therefore as it can be seen from the graph pins 1, 2 and 3 are in grain A were as pin 4 is in grain B for relative position from 0.0 to 15.0 and it has an average resistivity value around $0.452\ \Omega\,\mathrm{cm}$ then when the pin 3 inters grain B which is when pins 1 and 2 are in grain A and pins 3 and 4 in grain B at relative position 20.0 the resistivity suddenly increases to its maximum value about $0.464\ \Omega\,\mathrm{cm}$ due to grain boundary potential distortions [26]. Immediately after pins 2, 3 and 4 inters grain B the resistivity drops to its bulk resistivity.

Name of the sample	thickness μm	Average resistance Ω	Sheet resistance Ω/□	Resistivity Ω cm
R9-Q3-227	220	4.386	19.88	0.437
R9-Q3-226	220	4.393	19.91	0.438
R9-Q3-143	220	5.187	23.51	0.517
R9-Q3-142	220	5.299	24.02	0.528
R9-Q3-058	220	5.358	24.28	0.534
R9-Q3-057	220	5.361	24.30	0.535

Table 4.1: Average resistivity of a random point in each of the mc-Si samples

A different behavior was observed for sample R9-Q3-143 as shown in figure 4.9. We start at the far left when all three pins which are pins 2, 3, 4 are in grain B where as pin 1 is in grain A with a resistivity around $0.52\ \Omega\,\mathrm{cm}$ but the resistivity is almost constant even when pin 1 crosses the boundary and enters grain A at relative position $0.4\ \mathrm{mm}$ here all the pins are in grain B. As it can see from figure 4.9 the twin boundary does not affect the bulk resistivity when we cross from grain B to D. However the resistivity of the sample starts to raise when pins 1 and 2 approaches grain E possibly due to stress associated high dislocation density between grains D and E. Then after both pins 1 and 2 are in grain E and pins 3 and 4 are in grain D the resistivity is continue to raise. Since pins 2 and 3 are

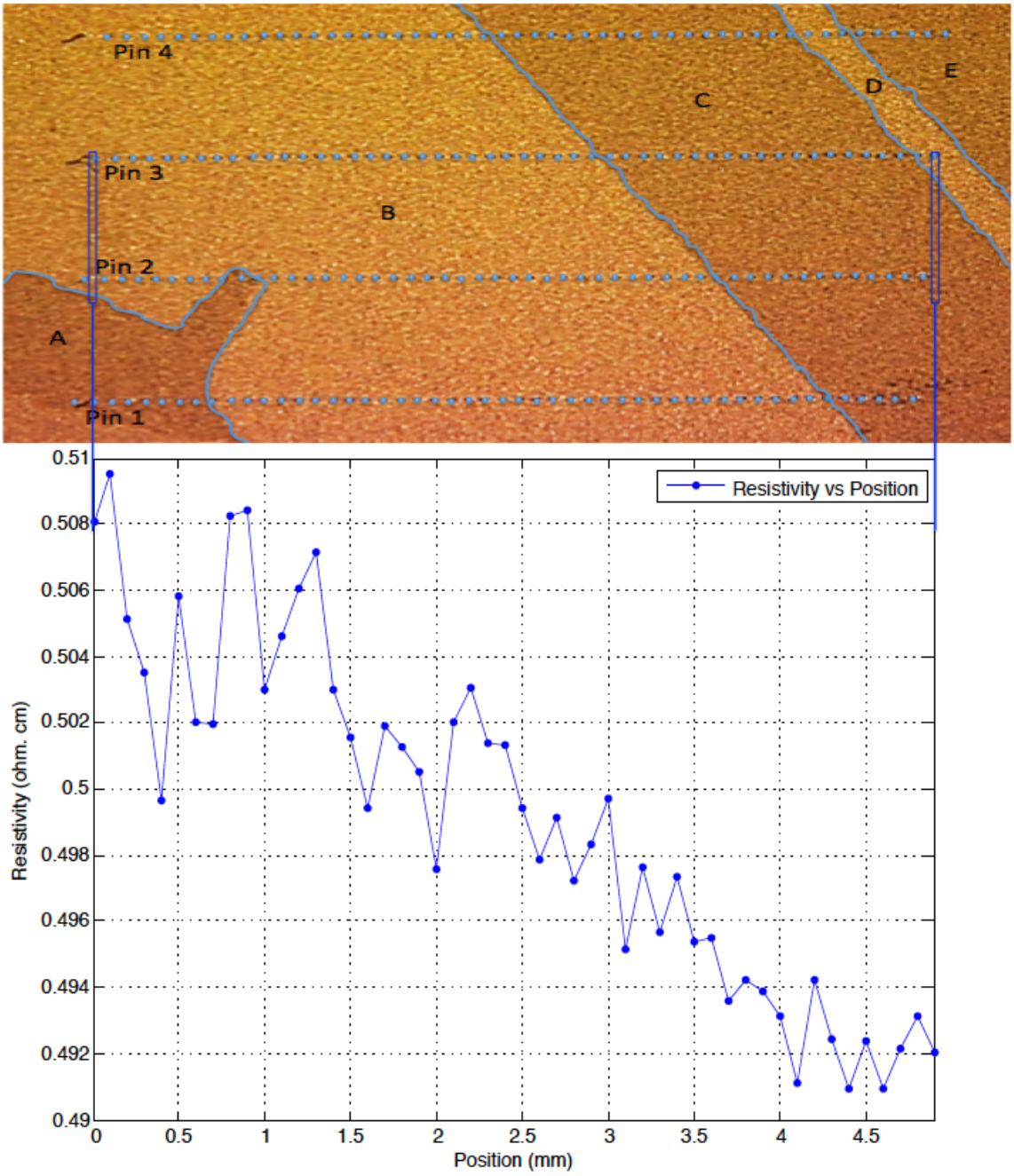

Figure 4.10: Resistivity versus position for sample 143 the data was taken in which the direction of translation of the sample is $\perp$ to the probe array

in different grains grain E and D respectively it is expected the resistivity will increase as this two pins are the responsible ones for measuring the potential drop. This increase in potential difference when the the two inner pins (2 and 3) are due to the potential barrier between two grains [26]. The resistivity even raises further to its maximum value around $0.60\ \Omega\,\mathrm{cm}$ at $6.2\ \mathrm{mm}$ when both pins 2 and 3 approaches grain F which shows this area

has a high dislocation density due to stress between grains E and F for pin 2 and D and F for pin 3. Finally as pin 3 inters grain F the resistivity drops to its minimum value around $0.50\ \Omega\,\mathrm{cm}$ at $6.4\ \mathrm{mm}$ which shows the potential barrier between grains E and F are low.

The date measured for figure 4.10 also taken from sample R9-Q3-143 and the relative position of each point has a spacing of $0.1\ \mathrm{mm}$. As it can be seen in the figure the resistivity value decreases towards the right side. This is like the behavior of figure 4.9, where grain B have a high dislocation density due to stress associated between grains A and B. However there is an increase in resistivity when pin 2 inters from grain B to grain A in this case both the inner pins are on different grains and there will be a potential barrier between the grains. Even though there is small raise in resistivity when the third pin is on the grain boundary at $3.0\ \mathrm{mm}$ the resistivity does not affected much by the grain boundary possibly due to the over starched grains (B and C) decreases the possibility of surface charge shield in the boundary. Finally when both pins 2 and 3 are with in the same grain (C) the resistivity value becomes stable until pin 3 inters grain D and the resistivity starts to raise again.

To see the effect impurity when the sample is taken from different height of the ingot we calculated the the average resistivity of each sample as shown in table 4.1. The table shows us the average resistivity of the samples which are cut from different height of the ingot. It is clearly be seen from the table the resistivity of the samples $\rho_{R9-Q3-227} < \rho_{R9-Q3-143} < \rho_{R9-Q3-057}$ which is the resistivity of the samples vary due to the difference in impurity concentration during solidification.

Finally we have seen that local resistivity measurement give us interesting results related to the grain boundary structure, and this may lead to a better understanding of the defects that reduces the efficiency of mc-Si solar cell.

Chapter 5

Conclusion

To address the high costs of purification and crystallization process, photovoltaic industries should focus on researches to develop cheaper refining processes as well as the crystallization process should also be simplified which will lead to low price multicrystalline silicon solar cell that can substitute the singlecrystalline silicon which usually consumes high energy, therefore, mc-Si have a huge potential for low cost solar cells.

However mc-Si features crystal defects such as dislocations and grain boundaries that gives lower cell efficiency than singlecrystalline cell. The boundaries between grains in mc-Si accumulates electrical active impurities during solidification which affects the performance of the cell by a current drop due to recombination and a voltage drop induced by local fixed charges as well as a result of the reduced current.

For all the samples the dimensions are 50×50 mm with thickness of 220 μm. All the data are measured using the multi-height collinear four-point probe and as you can see in table 4.1 we found out that the resistivity of each of the samples from different height has different resistivity values. Since adjacent wafers fabricated out of the ingots show nearly identical defect structures (grain boundaries and dislocations) their resistivity values are also almost similar. But generally the resistivity of the samples decreases with increasing block height of the samples.

In this work we found out that the resistivity a sample is affected by a grain boundary when the two inner pin are on the opposite side of the boundary the resistivity increases due to a potential barrier build in the boundary. And also we observe that when the pins approaches parallel to the boundary there will be an increase in resistivity due to high level of dislocation near the boundary.

We investigate the electrical activity in dark when we cross the grain and twin boundaries both in parallel and perpendicular to the direction of motion of the stage. According to our result the resistivity of samples varies from grain to grain more importantly we found out that locally each time the pins hits the grain or twin boundaries we see an increase in resistivity which can clearly indicate that there is an accumulation of metallic impurity at defect areas that affects the electrical activity. As shown from the graph We found out

that there is a great correlation between grain structure and the measured resistivity for each sample.

The problem we faced regarding to the measurement technique which is when the direction of translation of the sample is $\|$ to the probe array can be solved by using an x-y stage method mentioned by M. Spitz and S. Rein [3] instead of x or y stage.

Finally the average resistivity of each sample with in a grain of the samples are between $0.4\ \Omega\mathrm{cm}$ to $0.6\ \Omega\mathrm{cm}$ which is a very good value for solar cell fabrication. The table shows us the average resistivity of the samples which are cut from different height of the ingot. It is clearly be seen from the table the resistivity of the samples $\rho_{R9-Q3-227} < \rho_{R9-Q3-143} < \rho_{R9-Q3-057}$ which is the resistivity of the samples vary due to the difference in impurity concentration during solidification.

Suggestions for further work

- Combine structural analysis like electron backscatter diffraction to determine the specific grain orientations would confirm the association of high angle grain boundary with increased resistivity.
- The effect of etching and polishing on resistivity.
- Measurement of laser beam-induced current
- Controlled studies of the doping level and grain boundaries induced resistivity changes.

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Appendix A

Original Images

Here we included for reference the original microscopic images that was taken before it was modified and used in the result and discussion part of this work.

Figure A.1: Original image used in figure 4.6

Figure A.2: Original image used in figure 4.7

Figure A.3: Original image used in figure 4.8

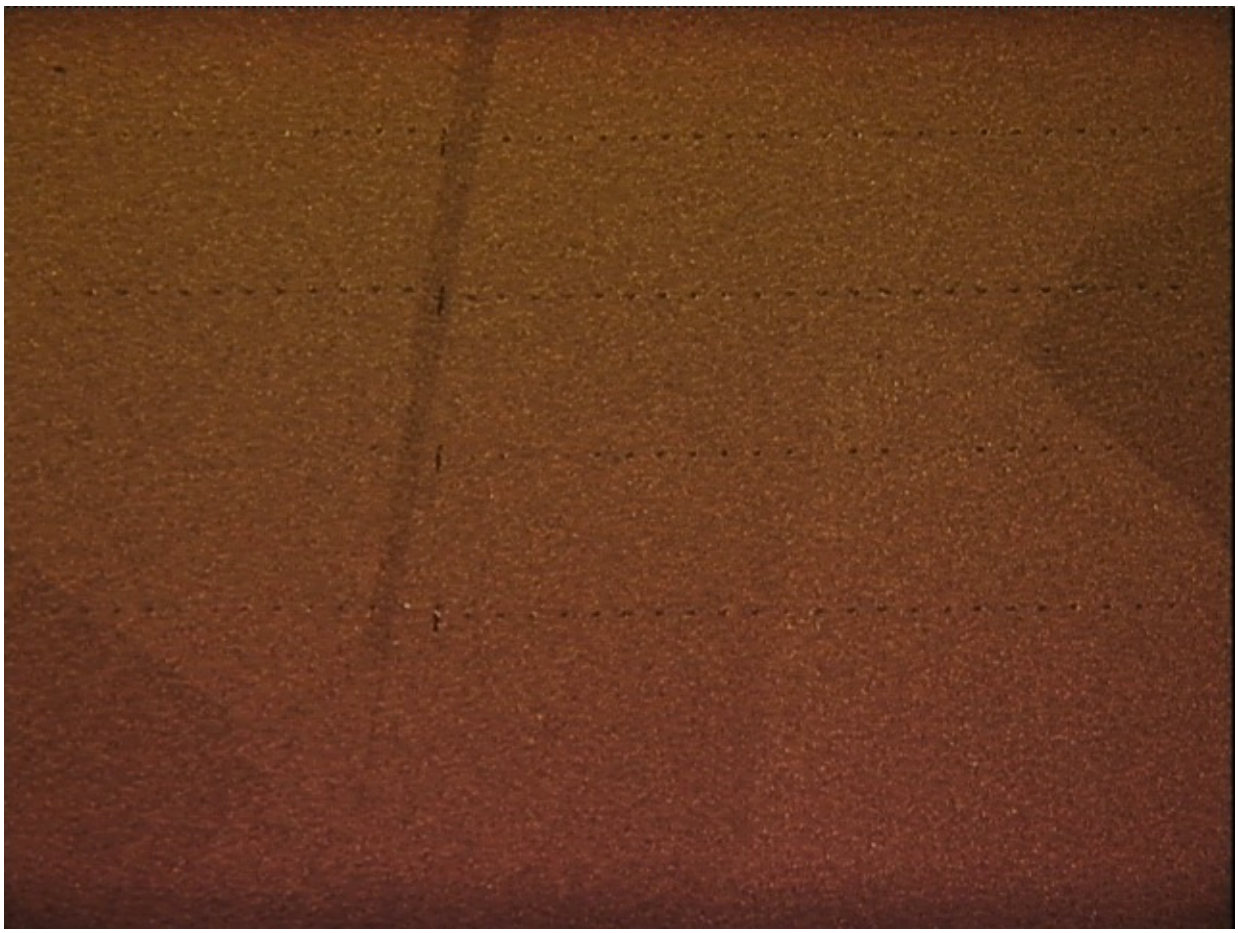

Figure A.4: Original image used in figure 4.9

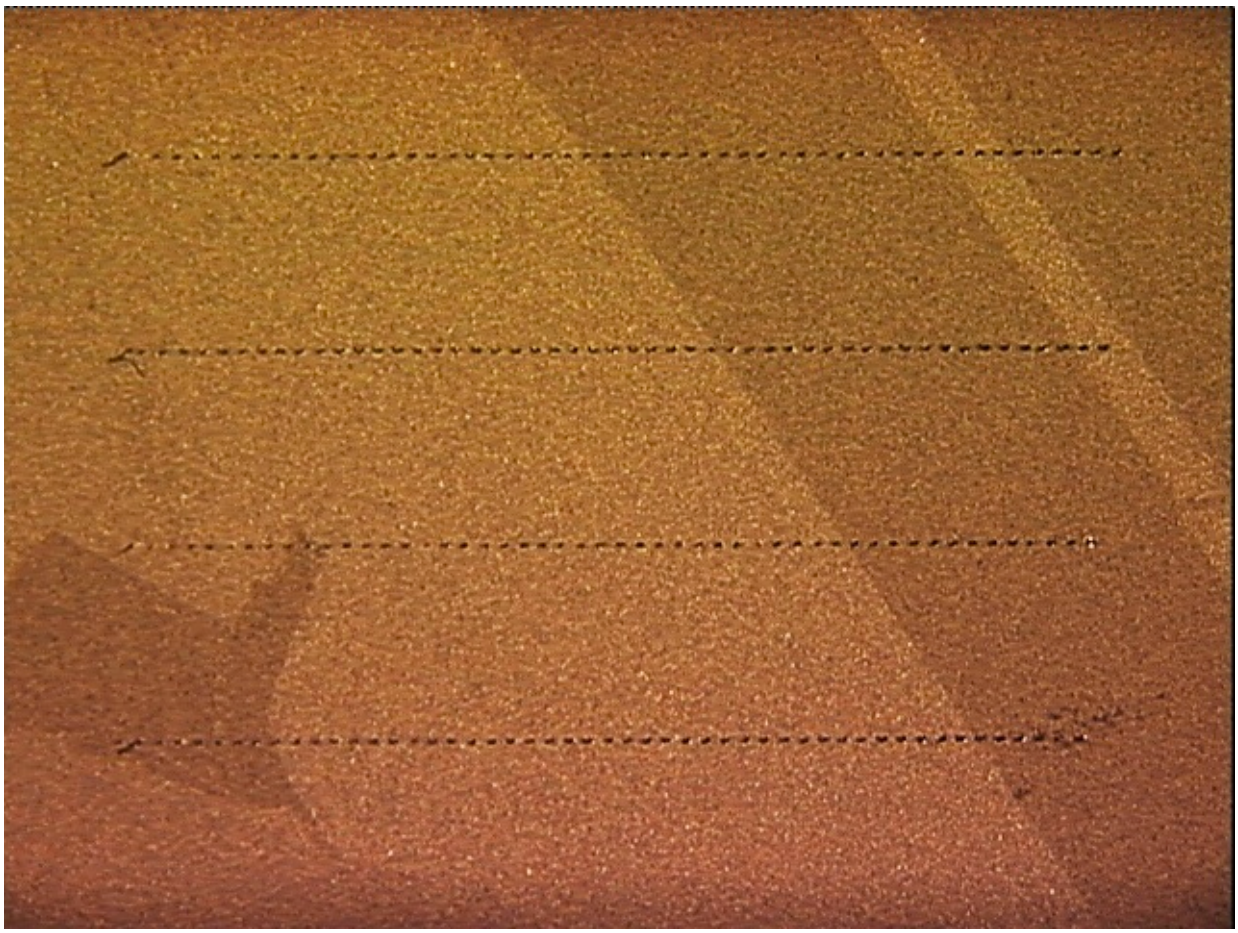

Figure A.5: Original image used in figure 4.10