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Ultra-low power Design of DSRC modulator/demodulator in 28nm FD-SOI

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ABSTRACT

Toll registaration units used in cars today are battery dependent and subject to issues such as battery leakage and false activation. Running the on-board unit with power only from harversted energy from radiofrequency signal from road side units. Creating a circuit which is able to only run on the power harvested requires a circuit which has lower power requirements than today's implementations. Using newer technology nodes and low power design techniques, a battery free energy harvesting solution may be possible.

This thesis presents the design and evaluation of a Reciever/transciever module and a stack-module designed according to the DSRC standard commonly used in road toll registration. Using 65nm CMOS technology and 28nm FDSOI technology has proven to be a significant improvement in terms of power consumption. A minimum current draw of 41 nA for the RX/TX-module and a minimum of 220nA for the stack, both acheived using 28nm FDSOI technology.

Keywords: *Thesis*, *Masters*, *DSRC*, *Ultra-low power*, *sub-threshold*.

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Place: Trondheim

Date: 22/06/2017 **Gunnar Lid**

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List of Terms and Abbreviations

DSRC	Dedicated short range control field
V2I	Vehicle to infrastructure
V2V	Vehicle to vehicle
OBU	On board unit
RSU	Road side unit
CMOS	Complementary metaloxidesemiconductor
FD-SOI	Fully depleted silicon on insulator
MAC	Medium access control
LLC	Logic link control
LPDU	Link layer Protocol Data Unit
MSB	Most significant bit
LSB	Least significant bit

CHAPTER 1

Introduction

The DSRC standard is a widely used standard in electronic toll registration, either for V2I or V2V communication like in Figure 1.1. A part of this standard is a battery powered on-board unit used for identifying users in a toll registration system. The OBU gets it's information signal from road-side units which transmits and receives messages in the 5.8 GHz band[11]. The energy used in transmitting these messages could be exploited in a energy harvesting solution. The power consumption and minimum supply voltage needs to be reduced to make this possible. One of the problems faced in today's DSRC solutions, is the problem of false activation of OBUs caused by devices operating in the same frequency band, causing the batteries to drain. Batteries which will need replacement sooner than planned. The batteries which are commonly produced in lithium ion can be a hazard to the environment and produces toxic waste [4]. A energy harvesting solution, would not have a problem with false activation, as the battery is

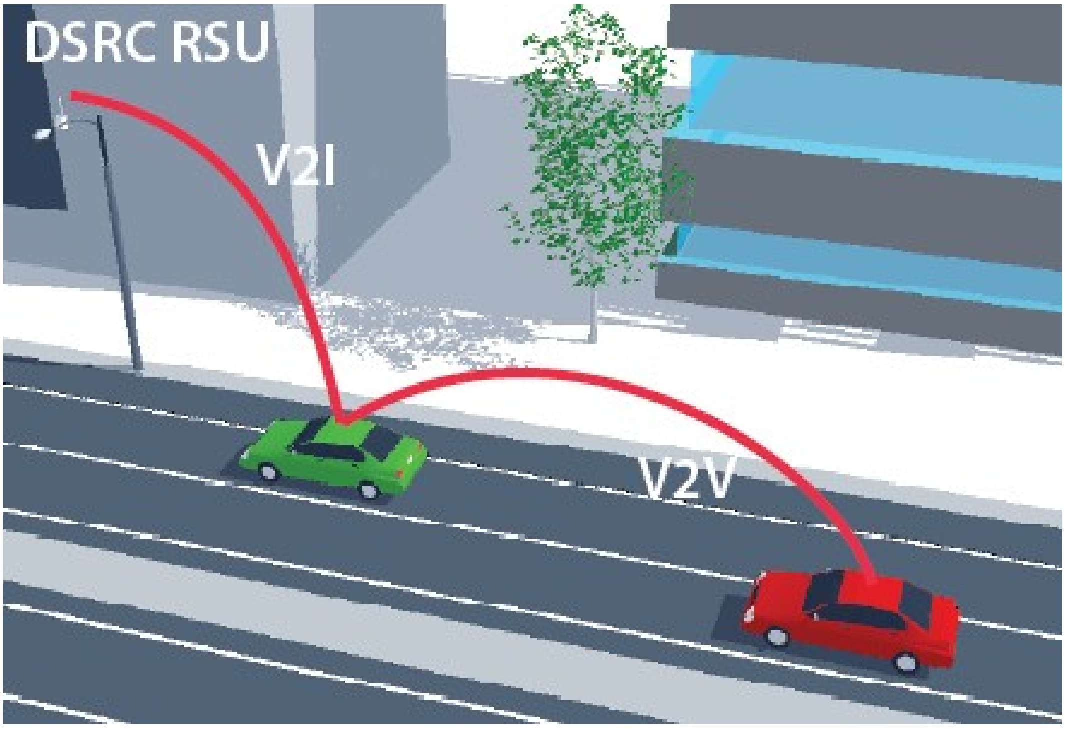

Fig. 1.1 Example of V2I and V2V communication

obsolete when the circuit can run on harvested power only.

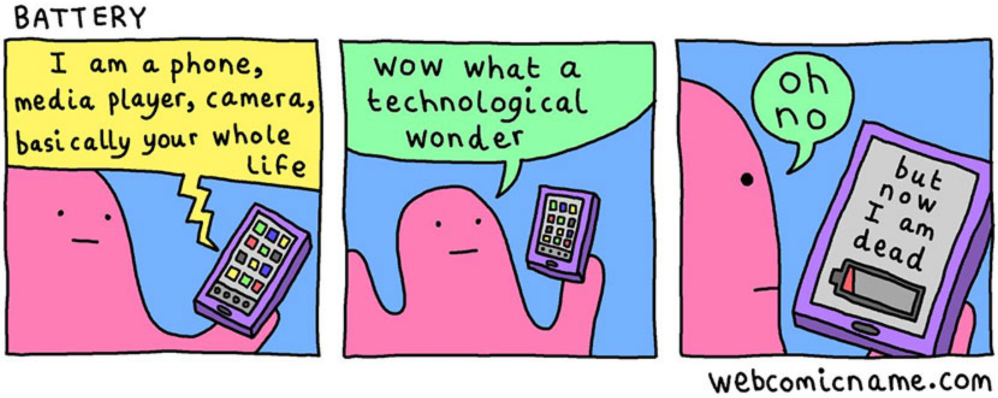
BATTERY
I am a phone, media player, camera, basically your whole life
wow what a technological wonder
oh no
but now I am dead
webcomicname.com

Fig. 1.2 Technology and battery life

To achieve lower power consumption and functional supply voltage, different techniques and technologies has been investigated and tested to see benefits and trade-offs through research.

Using a smaller process node is a recommended move in improving overall circuit performance and lower power consumption [8]. Achieving lower power consumption is the main factor in successfully implementing a energy harvesting solution and are meant to decrease with shrinking process nodes. Using FD-SOI is a promising technology as it allows for lower power consumption and lower operational voltage than bulk CMOS [13]. However, it is not guaranteed to be beneficial to change process node and changing process node introduces a new set of challenges and issues, among them is increased leakage power. This technology may or may not be suitable for a circuit of this size/complexity, and needs to be investigated to be confirmed.

My research has proven it to be beneficial change in regards to power consumption. Using 28nm FDSOI a minimum current draw of 41 nA were measured for the RX/TX-module were found using 200mV supply voltage. The stack measured a minimum current draw of 220nA at 200mV supply voltage. However using this technology is expensive. A battery powered solution with higher power consumption is used today in millions of units worldwide.

Energy harvesting is still not widely implemented and slowly making a arrival in consumer electronics[12]. Fitting an effective antenna in a small appliance is difficult. Having an effective amplifier at extremely low voltages is also a challenge which is outside of reach of this project. These reasons are also the reason why it has not been done before.

A RX/TX-module was designed by my adivsor Snorre Aunet, and implemented on chip using 90nm technology. Magne Værnes did project work were he measured the power consumption of this chip[7].

CHAPTER 2

Theoretical background

In this chapter the theoretical background for understanding this project will be presented.

2.1 Technology types

Two types of technology nodes has been used in this project; **Bulk CMOS** and **FD-SOI**

2.1.1 CMOS

Complementary metal-oxide-semiconductor is commonly used technology when constructing integrated circuits. The two most important characteristics of cmos devices are high noise immunity and low static power consumption. Smaller technology nodes struggles with increasing static leakage, which has become dominant factor in the total power consumption. [3]

2.1.2 FD-SOI

Silicon on insulator technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, to reduce parasitic device capacitance, thus improving overall performance. The main difference in SOI-based devices from conventional silicon-built devices lies in that the silicon junction is above an electrical insulator, typically silicon dioxide or sapphire. The FD in FDSOI stands for fully depleted as the channel is not doped.[13]

2.2 CMOS power dissipation

CMOS transistors has different sources of power dissipation. Each with different sources and high significance.

2.2.1 Dynamic power dissipation

Dynamic power dissipation is power consumed by active inputs. Inputs with AC activity causes capacitances to charge and discharge, which in turn causes the power consumption to increase. The equation for dynamic power dissipation is:

$$P_{switching} = \alpha C_l V_{dd}^2 f$$

Where α is the activity factor, which is the fraction of the circuits that is switching. C_l is the load capacitance, V_{dd} is the supply voltage, and f is the clock frequency[2].
Another factor in the power consumption in CMOS is the short circuit power, expressed by the equation:

$$P_{short-circuit} = I_{sc} * V_{dd}$$

I_{sc} is the short circuit current. Short-circuit current is the current through CMOS that occurs in the input of the switching logic unit. The finite rise and fall time of the input waveform results in a direct current path between V_{dd} and GND which exists for a period of time during switching. More specifically , when $V_{tn} < V_{in} < V_{dd} - |V_{tp}|$ holds for the input voltage, where V_{tp} and V_{tn} is NMOS and PMOS threshold voltages. Under these conditions conductive path will open between V_{dd} and GND since both the NMOS and PMOS devices will be on. To minimize the total short circuit current, it is beneficial to have equal input and output edge times[2].

2.2.2 Static power dissipation

$$P_{leakage} = I_{leakage} * V_{dd}$$

For nanometer devices, the leakage current sources are dominated by **Sub-threshold leakage current** and **Gate-oxide tunneling leakage**. As the process size has shrinked, sub-threshold leakage current has become one of the dominant sources of leakage. The sub-threshold leakage current is the drain-to-source leakage current when the tranistor is in the OFF mode. This happens when V_{GS} is lower than V_{th}, also known as weak inversion mode. The subthreshold current flows due to the diffusion current of the minority carriers in the channel in the MOSFET. Modern devices features low V_{th} which has become a dominant factor in static power consumption. The subthreshold leakage current can be expressed as :

$$I_{d,weak} \propto \exp(\frac{V_{gs}}{n * V_T})$$

where V_T is the temperature voltage derived from

$$V_T = \frac{k * T}{q}$$

As for **Gate Oxide Tunneling Current** the device scaling in the nanometer regime increases short channel effects such as drain induced barrier lowering and V_{th} roll-off. To control the short channel effects, oxide thickness must scale accordingly in each technology generation. This scaling of oxide thickness causes a rise to high electric field resulting in a high direct-tunneling through the transistor gate insulator. The thin oxide layer reduces the width of the energy barrier that separates the gate from the channel, which in turn makes it easier for electrons/holes to tunnel through the insulator layer. For ultrathin oxide MOSFETs the application of the gate voltage is a major contributor for this type of leakage current. The larger the gate voltage, the larger the electric fields generated in the substrate and thus more energy will be given to the carriers in the substrate, thus increasing the risk of tunneling.

Band-to-band tunneling current could also be mentioned, however it is considered to be a neglible source of leakage for technologies above 25nm. [1]

2.3 Clock Gating

To save switching power, a common HDL design technique is the use of clock gating. Clock gating is the principle of adding logic to disable switching in a circuit. It's intention is to stop a clock signal to propagate through a circuit. Switching states in a circuit leads to dynamic power consumption, disabling the clock signal removes the power dissipated by switching and leaves the leakage power as the source of power consumption. The straightforward approach is to use a 2-input AND gate in front of a clock input, with the clock in one input and a select signal in the other input. This can introduce the hazard of glitches which can cause unintentional behavior. A more safe approach is to connect the enable signal to the input of a latch, with a inverted clock signal connected the enable input of the D latch, and one clock signal connected to a 2 input AND gate like in Figure 2.1[5].

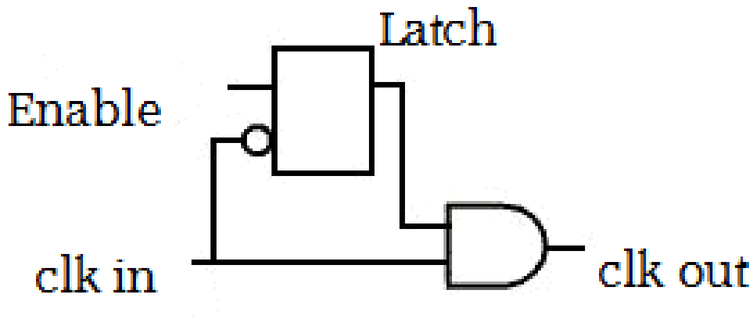

Fig. 2.1 Latched clock gating

2.4 Clock dividers

Different clock dividers are used to get more clock frequencies in a design:

2.4.1 Divide-by-4 module

A divide by 4 module is supposed to to divide a clocked input by 4. In Figure **??** the clock input is divided in 4 and there is clock cycle on the output for each 4 clock cycles on the input.

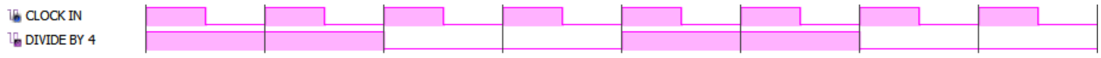

Fig. 2.2 Input and Output waveform of the DIV4-module

2.4.2 Divide-by-3 module

The DIV3 module must divide must turn three clock cycles from input into one clock cycle on the output- Waveform with correct input output relation is in Figure **??**.

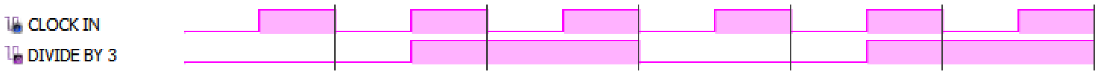

Fig. 2.3 Input and Output waveform of the DIV3-module

2.5 Line coding

The RXTX-module features a different set of line codings which are used and mentioned in this paper. How the encodings work are explained in the following subsections.

2.5.1 Non-Return-to-Zero-Level and Non-Return-to-Zero-Inverted

Non-Return-to-Zero-Level, uses two levels as the signal elements for two binary digits, and appears as raw binary digits without encoding. Most commonly maps binary 1 to logic-level high and binary 0 to logic-level low.
The Non-Return-to-zero-inverted uses the absence or presence of a transition to signify a bit level, where a existing transition signifies 1 and absence of a transition 0[9]. An example of both the NRZ-L and the NRZ-I encoding scheme can be found inFigure 2.4.

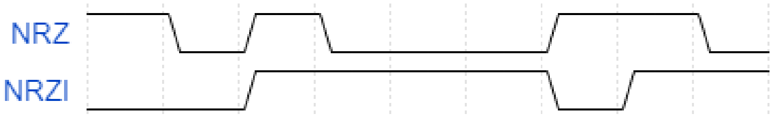

Fig. 2.4 NRZ-L and NRZ-I encoding of the a '10100011' signal

2.5.2 Bi-Phase Space Coding (FM0)

Bi-phase space coding is a digital coding standard which requires one transition per bit time, and an additional transition may appear in the middle of the bit. It has a predictable transition per bit, so a receiver can recover clock information from the data stream[6]. The rules for representing binary values 0 and 1 are:

- Logic 0 are represented with a transition in the center of a bit
- Logic 1 are represented with the absence of transition in the center a bit.

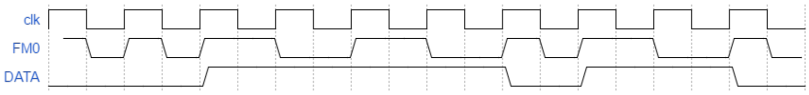

Fig. 2.5 fm0 encoding of the a '0011110110' signal

Since a transition is expected at every bit time, errors in the data stream can be detected through the absence of a expected transition. Example FM0 decoding can be seen in Figure 2.5.

2.5.3 Binary phase-shift keying

Binary phase shift keying is the simplest of the phase-shift keyings (PSK). Two different phases are used in this example;0° and 180°. This modulation is considered the most robust of all phase shift keyings, as it takes maximum noise for the demodulator to reach an incorrect decision. Since it is only able to modulate at 1 bit/symbol.
In Figure 2.6 an example binary phase shift keying is shown, triggered by the toggling off the 'data' signal.

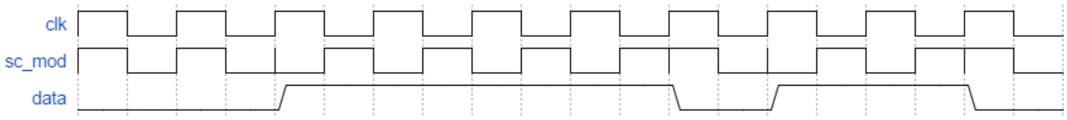

Fig. 2.6 Example of BPSK enabled by the toggling of a signal

2.6 DSRC stack

The DSRC stack is the implementation of the DSRC data link layer, medium access and logical link control [10]. The relevant parts of the DSRC standard will be described here.

2.6.1 Common expressions

A few expressions are used when describing the usage of the DSRC stack.

- **Uplink** The communication channel in which the mobile equipment (i.e. OBU) transmits its information.
- **Downlink** The communication channel in which the fixed equipment (i.e. RSU) transmits its information.
- **Window** Period of time in which the physical medium is allocated to either the mobile or the fixed equipment.
- **Frame** Format in which all the fields are transmitted (Link address field, flag etc.)
- **Mobile equipment** Mobile communication facility capable of recieving information from fixed equipment, transmitting information to fixed equipment is optional.

- **Fixed equipment** Fixed communication facility with one or more downlink channels, and optionally one or more uplink channels.

2.6.2 Transparency

To prevent the detection of a flag between the start and end flags, a zero bit insertion procedure is used as follows: The transmitter inserts a 0 bit following 5 contiguous 1 bits anywhere between the start and end flag. The insertion applies to the contents of the link address the MAC control field, the LDPU and the FCS.
The receiver contiguously monitors the received bit stream. After 5 contiguous 1 bits, the receiver shall inspect the following bit, if it is a 0 bit. The five 1 bits are passed on as data. if the the sixth bit is a 1, the receiver shall inspect the seventh bit, if it is a 0, a valid flag has been raised, if it is a 1. An abort message has been received and the receiving station shall ignore that frame.

2.6.3 Flag

A flag is sent at the beginning and the end of every downlink/(uplink?) frame to determine when a frame begins and ends. The flag is an octet of ”01111110”
A end flag shall not be used as start flag for the next frame.

2.6.4 Link address field

This field carries the Link identifier (LID). The link address either contains a private link address identifier(4 octets). or a multicast LID (1 octet) or a broadcast LID (1 octet).

The LSB of each octet in the link address field is an extension bit.

The **private LID** consists of 28 bits, where the LSB of the first three octets are set to 0, to indicate that a further octet of the link address field follows. The LSB of the fourth octet is 1 to indicate that it is the last octet of the link address field.

2.6.5 MAC control field

The MAC (Medium Access Control) control field is used to:

- indicate whether the frame contains an LPDU (Link layer Protocol Data Unit)
- indicate the transmission direction;
- allocate public and private windows;
- request for private windows;
- specify type of LPDU

All of this is indicated in one octet. The MAC control field is different for the downlink and uplink.

2.6.6 MAC control field downlink

The 7th bit is used to indicate the existence of LPDU. 6th bit (D) identifies bit direction. 5th bit is the medium allocation bit, and allocates a uplink window. The 4th bit shall be used to identify the LPDU as command or response. This is ignored if the LPDU bit is set to 1. The 3rd bit is the MAC sequence bit shall be used to distinguish between first allocation of uplink window and reallocation of window. The rest of the bits are reserved and set to 0.

2.6.7 MAC control field uplink

This is similar to the downlink except the 5th bit is used to request a uplink window. And the 3rd bit is reserved and set to 0.

2.6.8 LPDU

The LPDU consists of a LLC control field (one octet) and information field consisting of N x 8 number of bits, where the upper limit is 128 for public downlink and and private uplink frame, and 9 octets for private uplink windows.

2.6.9 Frame check sequence

Within one frame, there shall be a 16-bit frame check sequence before the end flag for error detection purposes. The contents of the link address field, MAC control field and LPDU shall be included in the calculation of the FCS.
The frame check sequence is compliant with 16-bit frame check sequence as defined in [ISO/IEC 3309] The generated polynomial shall be $X^{16} + X^{12} + X^5 + 1$ and the inital value used is $FFFF_{16}$. '

2.7 Energy Harvesting

Energy harvesting is the process where energy is derived from external sources (e.g. solar power, thermal energy, wind energy, salinity gradients and kinetic energy, aka ambient energy), and captured and stored for small, wireless autonomous devices. I.e. wearable electronics and wireless sensors networks.
The energy harvesters provide a very small amount of power, which in turn can be stored in a capacitor, super capacitor, or battery. Capacitors are used for units with high power spikes, while batteries provide a steady flow of energy and low power leakage.

2.7.1 Ambient-radiation sources

Powering devices with active and/or ubiquitous radio transmitters from power carried in radio frequencies, this can be done with photovoltaic technology, radiofrequency rectenna and optical rectenna technology. Where radiofrequency rectenna technology is considered the most efficient. Also a nantennea has been proposed as a solution to harvest ambient energy.

2.8 Various approaches

Snorre Aunet has done 90 nm implementation of a dsrc encoder/decoder. Magne Værnes did a research on the power performance of the unit, presented in [7]. There is room for improvement by shrinking the process node, shrinking process nodes are known to have lower power consumption.

2.9 DSRC my way

This is a continuation of my project work, as it indicated a promising improvement in the general circuit performance.
This implementations uses 65 nm CMOS and 28nm FD-SOI technology. Clock gating are used to inactivate unused modules and save power. Threshold voltage are adjusted in the transistor to improve the static to total power consumption ratio. The DSRC stack is made to be as minimal as possible and is meant as a exploration of the technology to see how it scales in terms of power consumption and minimal functional supply voltage. It is only able to decode one type of ”message” and give the correct response.

CHAPTER 3

Implementation

The dsrc encoder was first implemented in verilog (HDL) and simulated in Active-HDL with a test bench with normal and special case inputs. Synthesis schematics were explored throughout the design flow. to verify that the circuit would be as intended. When the design was fully verified in HDL, the design was converted to SPICE via YOSYS synthesis tool, with respect to the existing gates in a given 65nm library and the 28nm library. The existing gates in the 65 nm library is NOR, NAND, Full adder, D flip-flop, and inverter (INV). The same gates are available in the 28 nm FDSOI library. Equivalent test benches were used to test the design at SPICE-level. A transistor level simulation can give a close estimation of the designs performance. It also gives the designer the ability to adjust a variety of parameters such as transistor type, threshold- and supply voltage, temperature, capacitance, resistance etc.

3.1 Gate level implementation

This section presents gate-level implementations of cells which were not implemented in the supplied libraries.

3.1.1 2-input Multiplexer

A 2-input multiplexer is implemented with 3 NAND-gates and one INV. Connected as shown in figure Figure 3.1

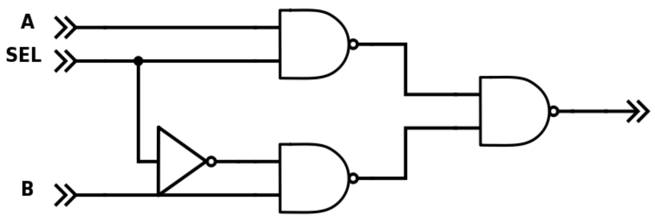

Fig. 3.1 Gate level schematic of the implemented 2-input MUX

Table 3.1 JK flip-flop truth table

J	K	Comment	Q_{next}
0	0	hold state	Q
0	1	reset	0
1	0	set	1
1	1	toggle	$\bar{Q}$

3.1.2 JK flip-flop

JK flip-flop was not part of the standard cell library and had to be implemented with the existing cells in the library. JK flip-flop functionality can be achieved by using three 2-input NAND-gates, one inverter and one d flip-flop, connected like shown in Figure 3.2.

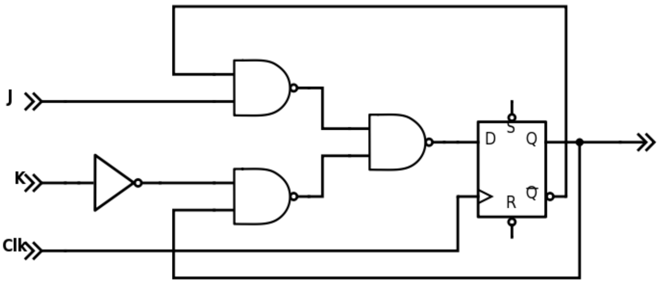

Fig. 3.2 Gate level schematic of the implemented JK flip-flop

3.1.3 Exclusive or-gate

An XOR gate can be implemented with 4 NAND-gates, as shown in Figure 3.3.

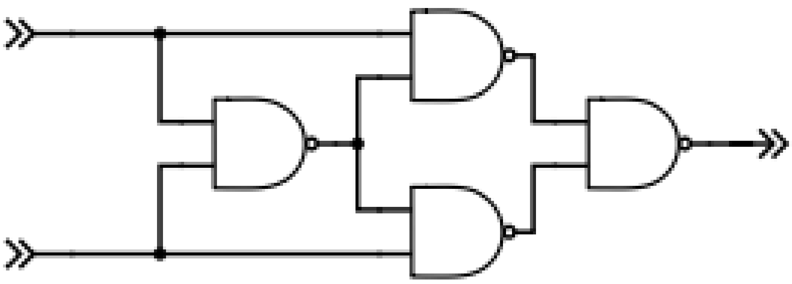

Fig. 3.3 Gate level schematic of the implemented XOR-gate

3.2 RXTX-module

A RXTX-module is used for modulating a received signal or a signal to be transmitted. The received signal is a FM0 encoded signal, and the signal to be transmitted signal is a NRZ encoded signal. The RX-module needs to decode the FM0 signal to NRZ, and the TX-module needs to encode a NRZ signal into a NRZI signal which activates a phase shift on either a 2 MHz or 1.5 MHz sub-carrier.

This module contains a RX-module and a TX-module. The module also contains a divide-by-3 (DIV3) and two divide-by-4 (DIV4) modules. The input clock frequency is at 6MHz, which is needed to achieve the three different internal clock frequencies of 500 kHz, 1.5 MHz, and 2 MHz.

The architecture of the module is shown in figure Figure 3.4. The input clock (6 MHz) is connected to the the combined divide-by-3 and divide-by-4 module. The output of the divide-by-3 module (2 MHz) is connected to the separate divide-by-4 module which outputs a 500kHz clock signal. The 500kHz clock signal is connected to a clock output and used to run external modules such as the DSRC stack. The 500kHz clock signal is connected to the JK-flip-flop in the tx-module and to the clock input of the RX-module to sample the data signal from **DIN** and **MODIN**. The divide-by-3 and divide-by-4 module is connected to a multiplexer connected to the XOR-gate in the TX-module. The **sc_select** signal is used to select sub-carrier. The **TX_EN** signal is connected to the a latched clock gate in front of the clock inputs of the TX-module and the RX-module, with the purpose to disable the modules when they are not in use.

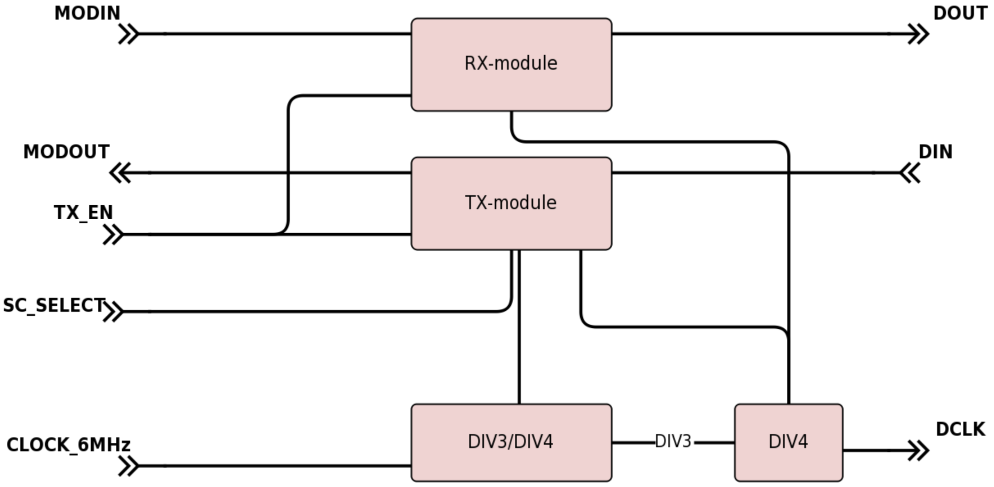

Fig. 3.4 Architecture of the complete module

- MODIN is the input for the encoded FM0 data stream.

- DIN is the input of the raw binary data to be encoded and phase shifted.
- DOUT is the decoded FM0 data
- MODOUT is the phase shifted sub-carrier signal.
- DCLK is a 500 kHz clock used for synchronization.
- SEL is a select signal to select sub-carrier.

3.2.1 Divide-by-4 module

Consisting of two d flip-flops, this design is a straightforward implementation.The first DFF samples the input clock signal, which has it's Q output connected to the D input of the other DFF. The $\bar{Q}$ of the first DFF is connected to the D input of the first DFF, thus toggling it's output each second clock cycle, thus dividing the clock input by 2. The second DFF is connected in a similar manner, with the $\bar{Q}$ connected to it's D input and Q connected to output. As a DFF connected to itself works as a divide by 2 circuit, two divide-by-2 circuits creates a divide-by-4 circuit. The implemented circuit is shown in Figure 3.5.

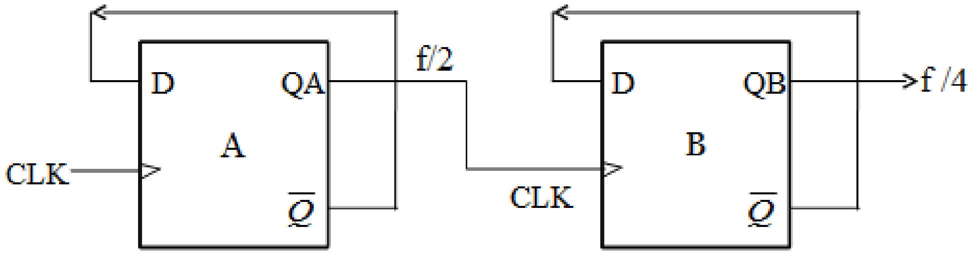

Fig. 3.5 Divide by 3 module

3.2.2 Divide-by-3 module

The Divide-by-3 divides the input clock by 3. The DIV3 module logic consists of 3 flip-flops, one NAND-gate, one NOR-gate and four inverters. The module divides the input clock by 3 with a 50% duty cycle. The DIV3-module can be seen in Figure 3.6 As seen in Figure 3.6 the clock signal is inverted and drives the last D flip-flop, the other two clock signals drive the two other D flip-flops. The time domain of the two left-most D flip-flops can be divided into three phases; a is zero, b is zero, and both are zero. When both are zero, the c signal is set to one, and the left most D flip-flop samples one and a is set to one, the middle D flip-flop samples a and b is set to one. Now B is one for a half clock cycle until it is switched to zero, and the DIV3 output is one.

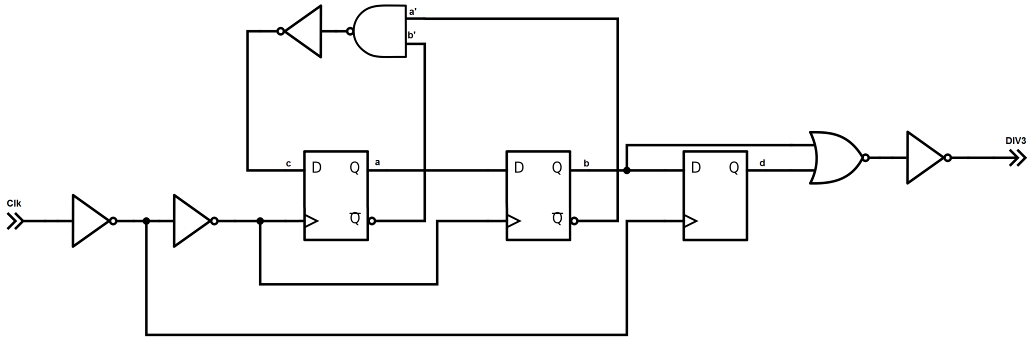

Fig. 3.6 Divide by 3 module

3.2.3 TX-module

The TX-module consists as seen in Figure 3.7 of a JK flip-flop and an xor gate. The circuit modulates a NRZ signal into a NRZI BPSK signal. The sub-carrier can be 2 or 1.5 MHz.

First the circuit turns a NRZ signal into a NRZI signal, the NRZI signal indicates a logic ’1’ by a toggling of it’s signal, this can be achieved by connecting a NRZ signal to both the J and K input of the JK flip flop like the one seen in Figure 3.2. A logic 1 at both inputs toggles the output and a logic 0 keeps the output stable as seen in Table 3.1.

The NRZI signal is connected to one of the inputs of the xor-gate. While the other input of the xor-gate is a clock signal which is 2/1.5 MHz depending on if the ’sel’ signal is 1 or 0 in the div3 or div4 module. The xor-gate output is the circuit output which is a NRZI BPSK signal. The implemented xor-gate is shown in Figure 3.3

Not shown is a latched clock gate like in Figure 2.1. Where the clock inputs are connected to separate latches and the TX_EN signal connected to the enable input of the latch. This was done to simplify the circuit diagram for readability. This was left out of Figure 3.7, to simplify the figure.

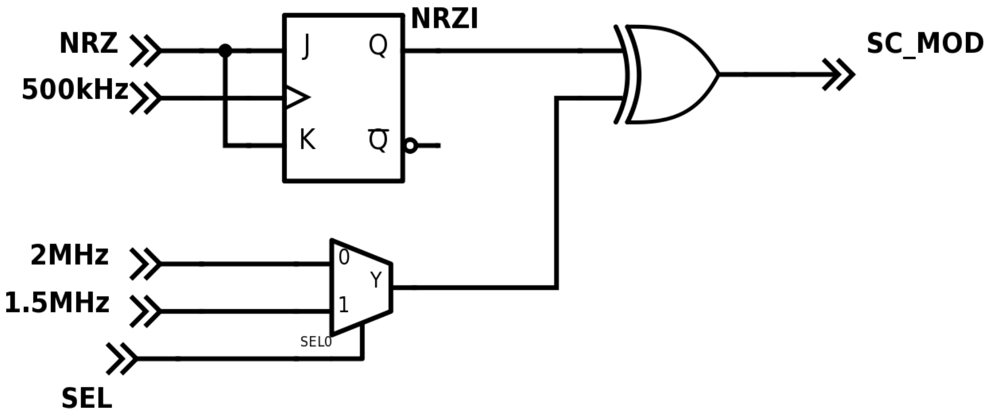

Fig. 3.7 Schematic of the TX-module

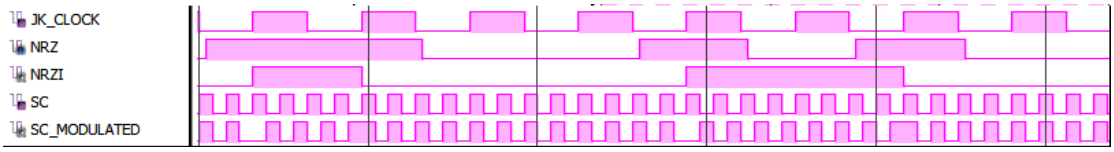

Fig. 3.8 Input and Output waveform of the TX-module

3.2.4 RX-module

The RX module seen in Figure 3.9 takes a FM0 encoded signal and decodes it to NRZ encoding. The RX-module consists of four D flip-flops, and a XOR-gate. The XOR gate checks if the signal from the first D flip-flop has been changed since the last time step. If the signal has changed, the NRZ output will be set to 1, if not it will be 0. The xor-gate has been implemented like in Figure 3.3

A latched clock gate seen in Figure 2.1 is not shown in the figure. Input clock is connected to the clock input of the latch, and TX_EN is connected to the enable input of the D latch. This part was left out of Figure 3.9 to ease understandability of the figure.

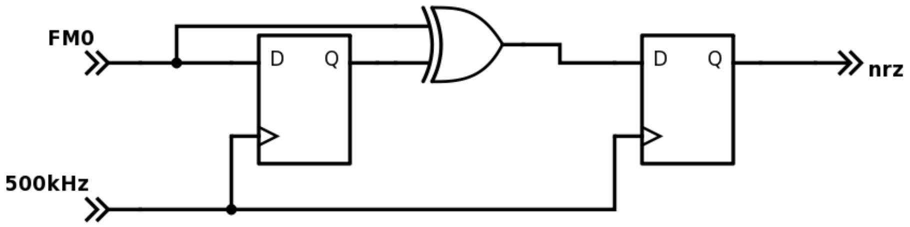

Fig. 3.9 HDL schematic of the RX-module

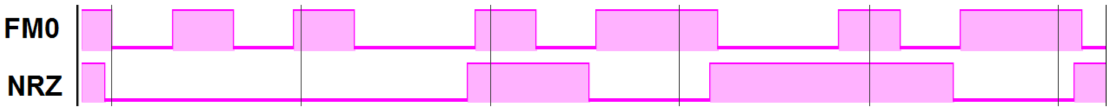

Fig. 3.10 Input and Output waveform of the RX-module

3.2.5 Selective clock gating

Clock gating could also be applied to the clock dividers. However, as both the RX-module and the TX-module both requires a 500kHz clock signal, both the DIV3 module and the standalone DIV4 module needs to be active at all times as they are required for generating a 500kHz clock. The DIV4-module in the combined DIV3/DIV4-module could have a clock gate, but would a area to a already small module. Also the RX and TX-module would not be used simultaneously in a real-world application as the unit is not meant to send and receive messages simoultanously.

3.3 DSRC stack

This section describes the implementation and the design choices for the DSRC stack. The DSRC stack is able to a handle a single downlink+uplink use case. Both downlink and uplink are according to the given standard[10]. The module has been divided into three parts; flag detection/bit stuffing, downlink buffer check, and uplink buffer. The flag detection/ bit stuffing unit detects whether the incoming frame is a flag, while also monitoring for stuffed 0 bits. The downlink buffer check consists of a FIFO buffer and a logic circuit which checks if the values of the fifos are correct, if they are correct a done signal gets sent to the uplink buffer. The uplink buffer consists of a fifo buffer which is connected to a multiplexer, when the pulse propagates through the fifo, the different values connected to the mux gets selected and outputs the correct uplink message.

The downlink and uplink frame is according to the layer 2 standard. This was done to get a prototype with behavior more similar to a real world DSRC product. The different fields of the frames are explained in section 2.6 The Downlink test frame consists of a flag, Private Link identifier, MAC control address and frame check sequence explained in. The uplink test frame consists of a similar frame, with a different Private link address field.

The architecture of the dsrc stack is shown in figure Figure 3.11. The flag check module and the downlink buffer check is synthesized from verilog, while the uplink buffer was written in spectre. This was done since the synthesis tool (yosys) created circuit with very long paths, thus creating timing issues. Writing the circuit in spectre gives the designer full control over the circuit design, which was beneficial.

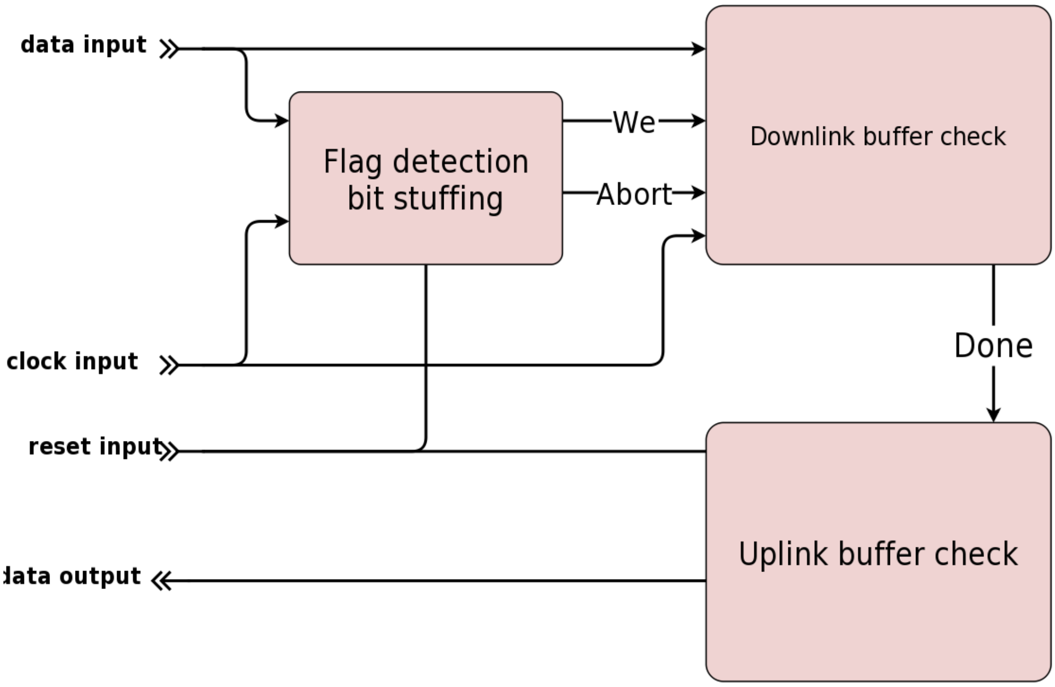

Fig. 3.11 Architecture of the DSRC stack

3.3.1 Frame check/ stuffed bit detection

The frame check basically implements the transparency part mentioned in subsection 2.6.2. A counter is used to count the number of sequential 1 bits, if a frame consists of ”01111110”, a 0 bit followed by 6 consecutive 1 bits and a 0 bit, a flag has been raised, this inverts the flag bit. If the 5 consecutive 1 bits has been received and a 0 bit is received, the 0 bit is not written to the downlink fifo buffer. If 7 consecutive 1 bits are received, a abort signal is raised and the downlink buffer is reset to all 0’s. Seen in figure Figure 3.12 is the state machine diagram of the described frame check/ stuffed bit detection. State1 and State 2 are simple counters for the 4 first consecutive 1 bits, if there is a 0 bit at the data input. The ”onescounter” is set to 0 as the stream of consecutive 1 bits is interrupted. If the data input is 1 the onescounter is incremented by 1. State3 and state4 are used when the ”onescounter” is equal to 5, if the data input is 0, the state is set to state3 and the write enbable signal is set to zero as this is the stuffed bit used for data transparency. If the data input is 1, the state is set to state4, where the next state is either state5 or state6. If the data input is 0, a flag has been transmitted, the flag bit is then inverted and the ”onescounter” is set to zero. If the data input is 1, a abort signal has been raised, and the downlink buffer is meant to be reset.

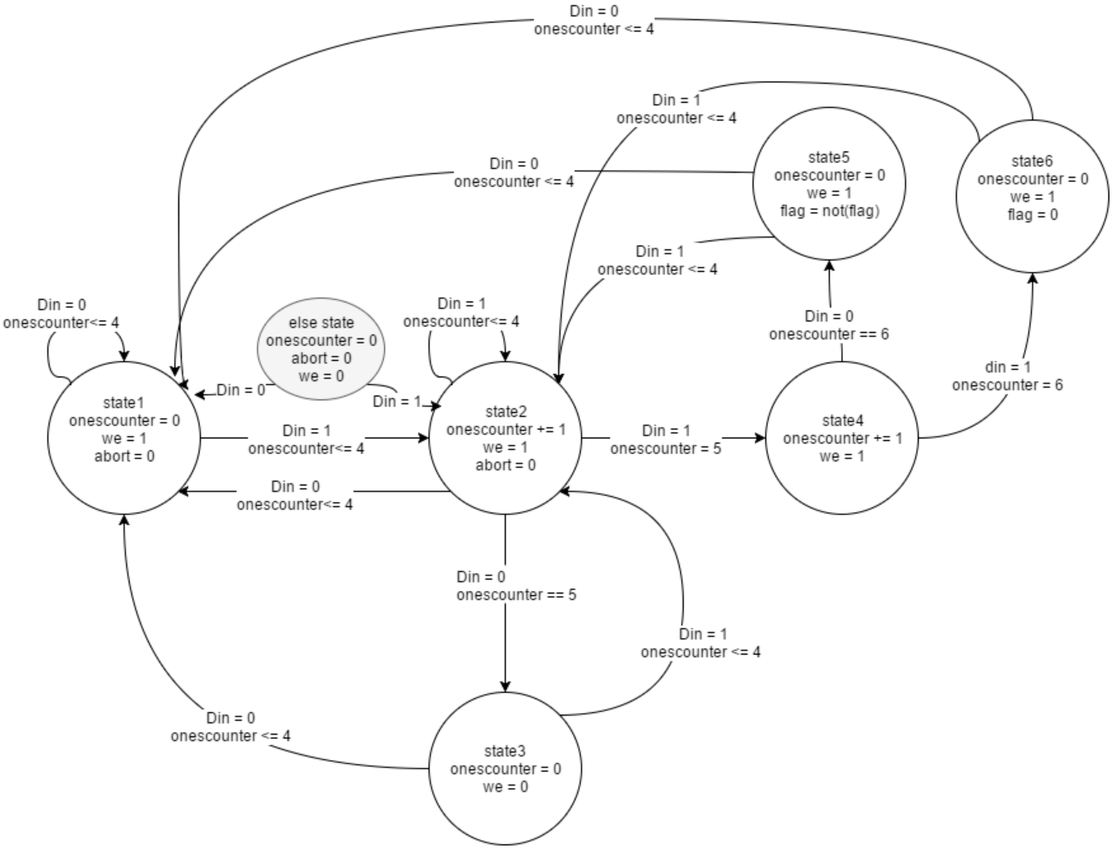

Fig. 3.12 Implemented state machine module, and bit stuffing detection

3.3.2 Downlink buffer check

The downlink buffer consists of a FIFO of 64 DFFs connected in series. As seen in Figure 3.13, the dotted DFF is meant to indicate the rest of the not shown DFFs.

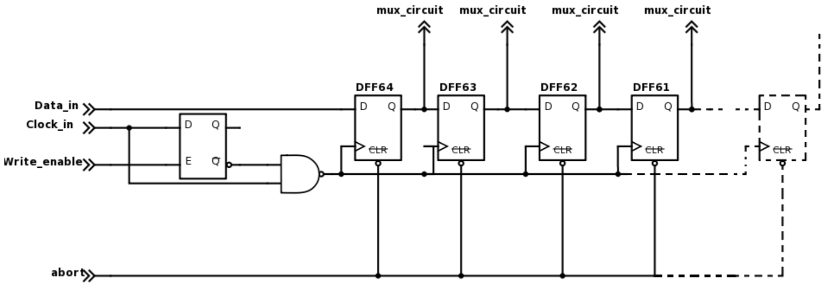

Fig. 3.13 Downlink fifo buffer

The FIFO features a clocked D latch at the clock input of the fifo shown in Figure 3.13. This is used to disable the data input to be written to the FIFO buffer. The ”we” signal from the flag detection module is connected to the enable port of the d latch. The abort signal from the flag detection unit is connected to the the DFFs reset input. Each D flip flop output are connected to the multiplexer shown in Figure 3.14. When the value stored in the fifo buffer is correct, a done signal will be raised for one clock cycle, as the value stored in the FIFO will only be correct for one clock cycle, as the value will be shifted the next clock cycle.

The multiplexer in Figure 3.14 does not show the whole multiplexer as it is too big to view on A4 paper. The inputs of the NAND and NOR-gates which appear unconnected with dotted lines are connected similarly as the NOR gates at the bottom of the figure. The red box also shows the logic of the not seen parts. As can be seen in Figure 3.14, the mux consists of 7 levels, and is one of the longer paths in stack.

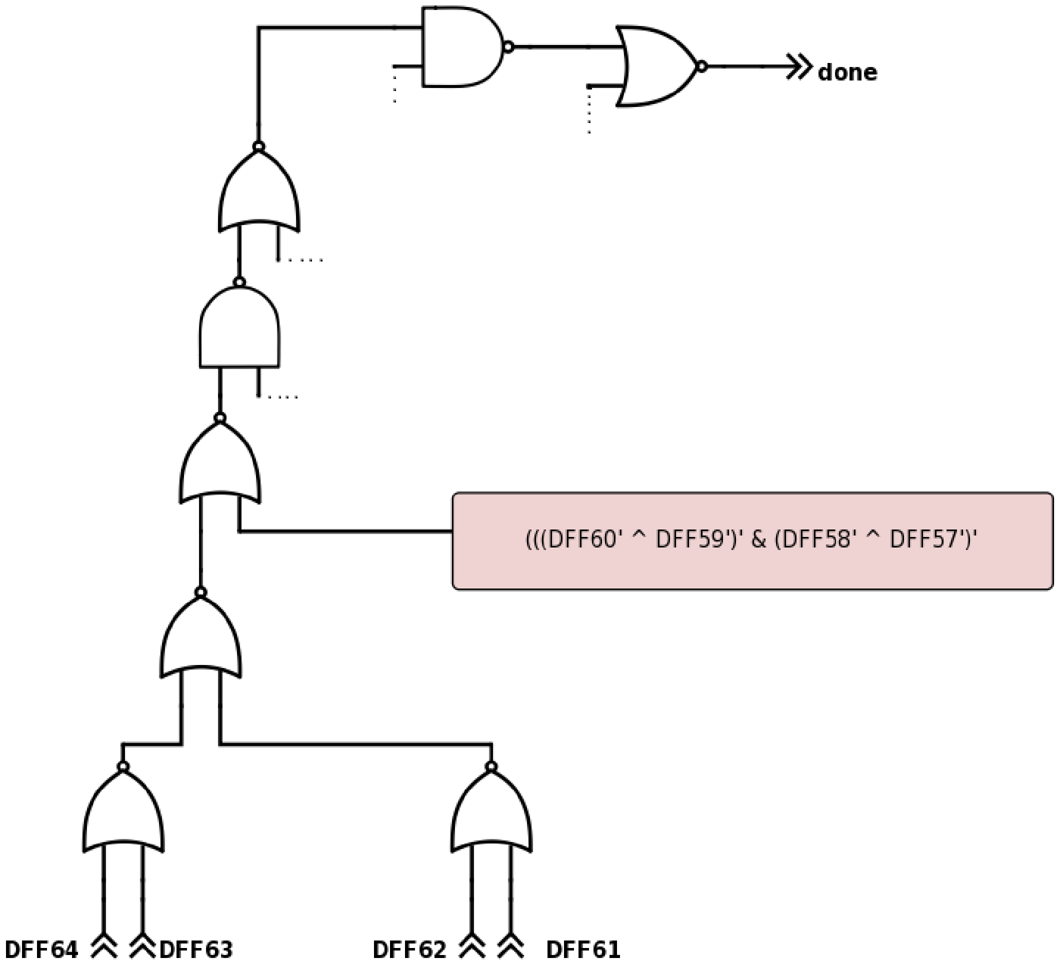

Fig. 3.14 Downlink multiplexer

3.3.3 Uplink buffer

Similarly to the downlink buffer check, the uplink buffer module consists of a fifo of DFF connected in series. and a multiplexer circuit. This is used in a different manner. As a done pulse with the duration of one clock cycle is meant to start the process of sending a uplink frame, as the pulse propagates through the fifo and cycles through the inputs of the multiplexer circuit.

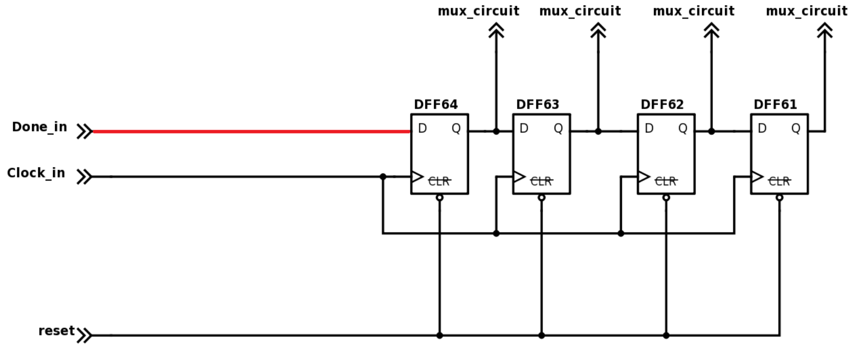

Fig. 3.15 Clock cycle 0 in the fifo

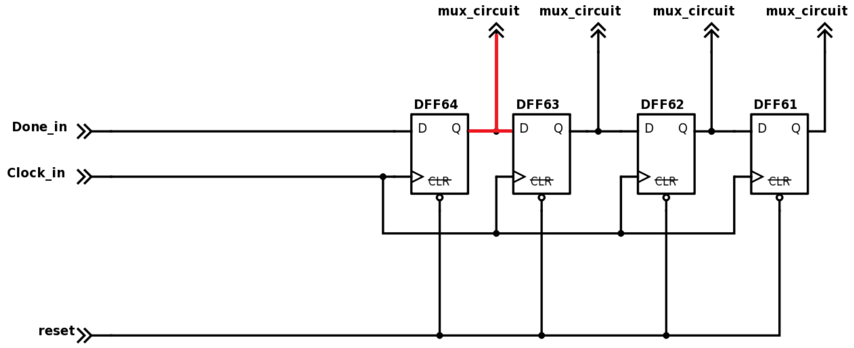

Fig. 3.16 Clock cycle 1 in the fifo

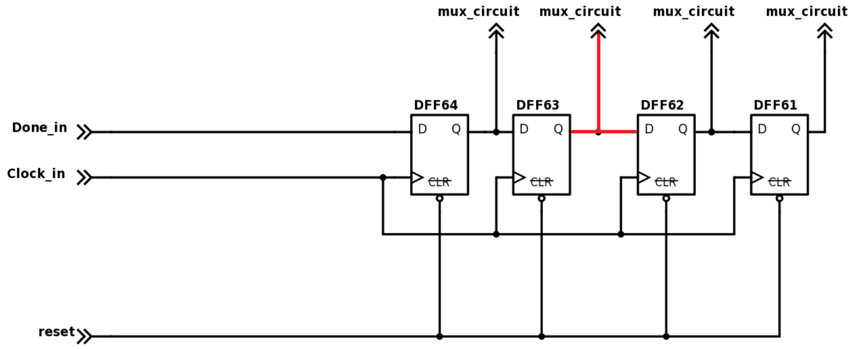

Fig. 3.17 Clock cycle 2 in the fifo

The Done pulse from the downlink buffer will propagate through the fifo buffer as shown in Figure 3.15, Figure 3.16, and Figure 3.17 while they enable all the ports of the multiplexer sequentially, resulting in a output of a given uplink frame. The fifo buffer used for the uplink buffer does not feature clock gating like in the downlink buffer. The ”manually” written multiplexer is connected to either supply voltage or ground, depending on what the appropriate value are and to the outputs of the fifo buffer as seen in Figure 3.18. The inputs that appear unconnected are connected in a symmetrical manner to the not shown part of the fifo buffer.

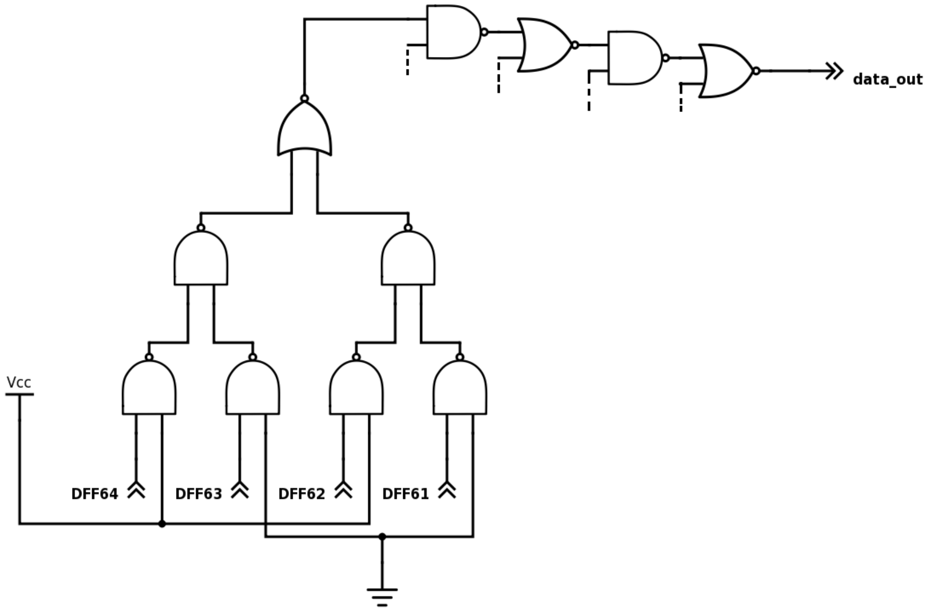

Fig. 3.18 Uplink multiplexer design

3.3.4 Compability

The stack and RX/TX-module are supposed to be connected. The purpose is that the RX/TX-module receives a moduleted signal which it decodes into NRZ signal, which the stack can receive. When the stack outputs a uplink frame, the RX/TX-module converts the NRZ signal from the stack into NRZI shift BPSK data. They have been tested seperately as the results of power consumption are best evaluated by themselves.

3.4 Tools

The following software tools were used for the design and simulation during this project work.

3.4.1 Active-HDL student edition

Active-HDL is a popular tool for design, simulation, project management, and debugging of HDL-designs. With support for both VERILOG and VHDL. The student edition is available at no cost for students, with a limited set of features. Synthesis is not included in student edition.
This tool was chosen due to it's availability and accelerated waveform viewer.

3.4.2 Yosys open synthesis tool

Yosys is a open source command-line framework for VERILOG RTL synthesis. Among it's features:

- Processing of synthesizable VERILOG-designs
- Built-in formal methods for property checking and equivalence
- Converting VERILOG to BLIF / EDIF / BTOR / simple RTL VERILOG / SPICE / etc.
- Mapping ASIC standard cell libraries

This tool was chosen as it was the only free synthesis tool found, with desired functionality.

3.4.3 Cadence Spectre Circuit Simulator

Spectre is a high-performance simulation tool which provides accurate SPICE-level simulation for analog, radio frequency and mixed-signal circuits. With other cadence tools it delivers transistor-level analysis in multiple domains.
This tool is a part of a cadence package installed at NTNU's servers. As it is a high performance tool in analog simulation, it was a clear choice.

3.4.4 Cadence Virtuoso Analog Design Environment

Virtuoso is tool for design and simulation tool for analog design. It gives the user to a accelerated debug process using a variety of built-in analog analysis tools.
This tool is also part of a Cadence package at NTNU's servers, and works great in combination with Spectre.

CHAPTER 4

Results

The implemented design was partly written in verilog and spectre, and simulated in spectre circuit simulator. This is a good approach in finding the characteristics of the circuits, as spectre is a powerful professional tool within circuit simulation. This was also the best available tools at the university, which my co-advisor Trond Ytterdal knew well.

The test benches used in the following simulations were also used by Magne Værnes in his characterization of a similar RX/TX-module implemented in 90nm. The test benches covers typical, special and edge cases and are meant to verify desired functionality. All modules are verified separately to ensure full functional coverage. As ultra low power is focus of this project, the circuit is tested at variable voltages to find the minimal functional voltage.

Test benches were made in spectre. For the power consumption analysis special case input causing maximal switching were used to give worst case power consumption. All modules are active during simulation to find worst case power consumption.

For the stack a typical case input was used. The Figure 4.1 shows the shape of the test bench vector.

Flag	Link Address Field	MAC Control Field	LPDU	Frame Check Sequence	Flag

Fig. 4.1 Input frame test bench used for the stack

4.1 Module verification

Here, all modules will be presented separately to show that all modules are verified.

4.1.1 Divide-by-4 module

The Divide-by 4 is fully functional at 120mV. This is with a clock input of 6MHz, which is the maximum clock frequency in this circuit.

The simulation waveform in Figure 4.2 at 140 mV appears without any glitches or issues as clock skew. 140 mV is lower than the minimum functional voltage of the RXTX-unit.

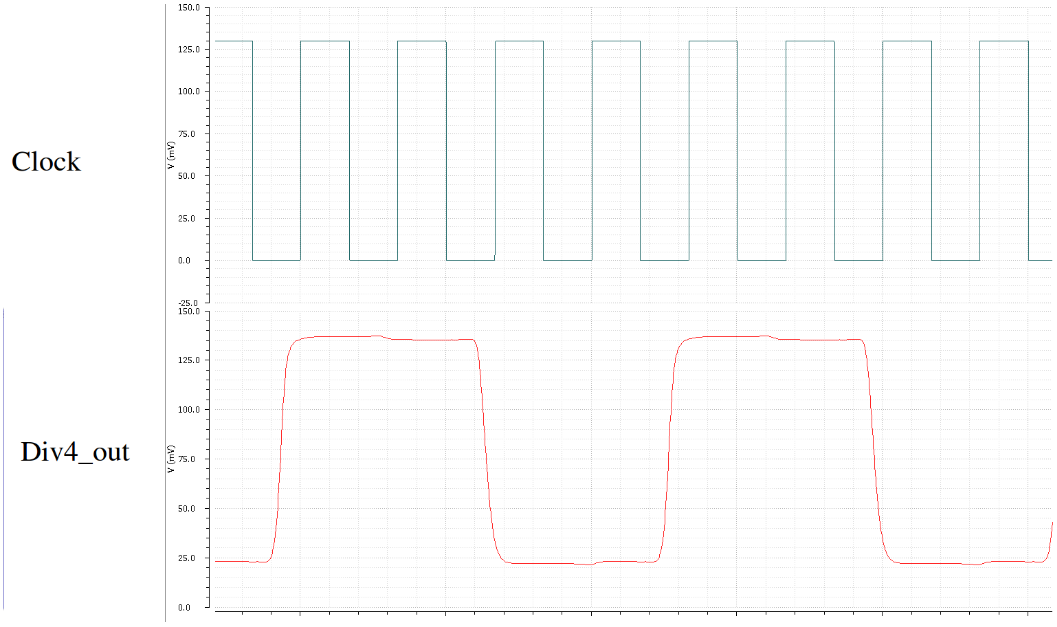

Fig. 4.2 Waveform output of the divide-by-4 module

4.1.2 Divide-by-3 module

The Divide-by 3 is fully functional at 130mV. This is with a clock input of 6MHz, which is the maximum clock frequency in this circuit. The simulation waveform at 120 mV appears without any glitches or issues. 120 mV is lowwer than the minimum functional voltage of the RXTX-unit, and therefore a satisfactory result.

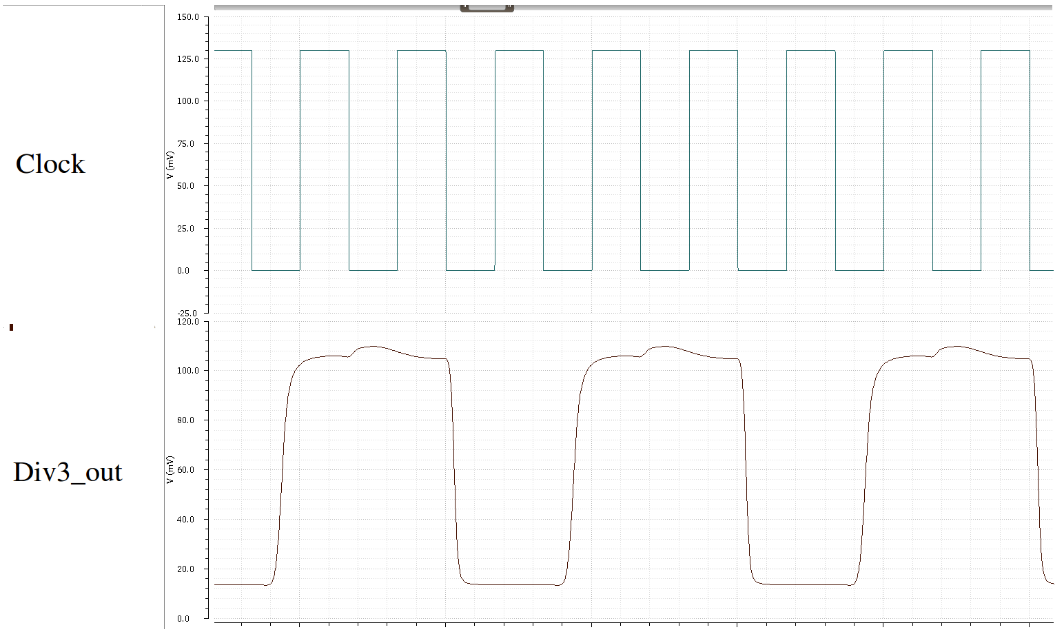

Fig. 4.3 Waveform output of the divide-by-3 module

4.1.3 Divide-by-3 or 4 module

The combined div3 or div4 module works as intended, the clock changes instantly. The lower supply voltage is bound by the div3 module, the power consumption chart shows power for both modules active. A small glitch is visible in the waveform in Figure 4.4.

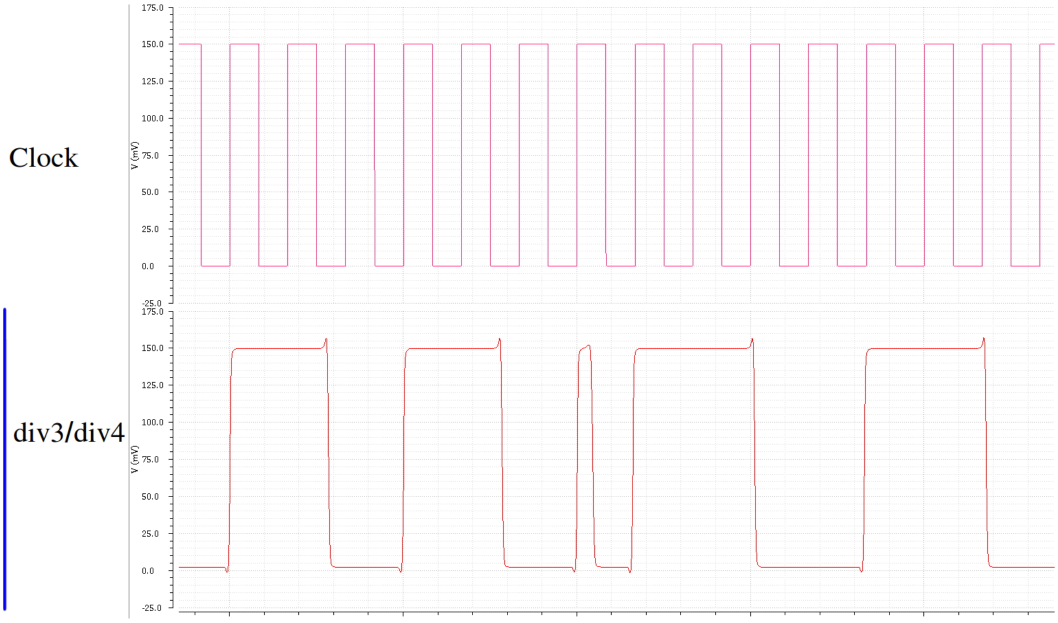

Fig. 4.4 Waveform output of the DIV3/DIV4 module

Sub-carrier clock-frequency is specified by the profile transmitted by RSU equipment, which means a glitch during clock switching would not introduce a hazard as the sub-carrier switch would be done before a frame were transmitted.

4.1.4 TX-module

The Tx-module works at 130 mV. At lower voltages the phase shifts are incorrect, which makes the output unusable. The waveforms in Figure 4.5, Figure 4.7, and Figure 4.6 appear without glitches, and the minimal voltage is satisfactory.

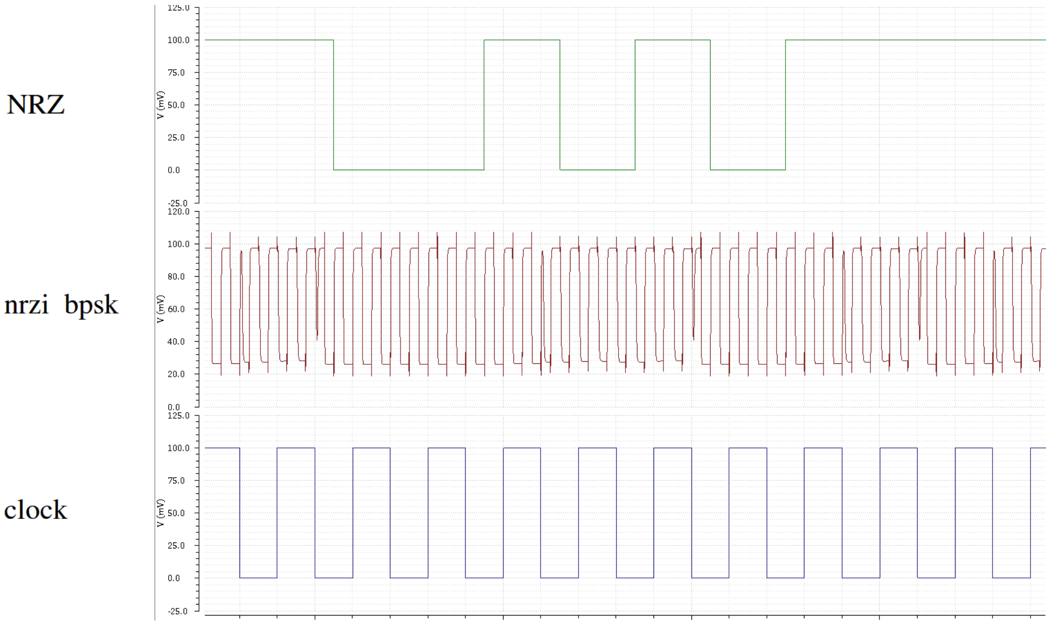

Fig. 4.5 Waveform output of the tx-module

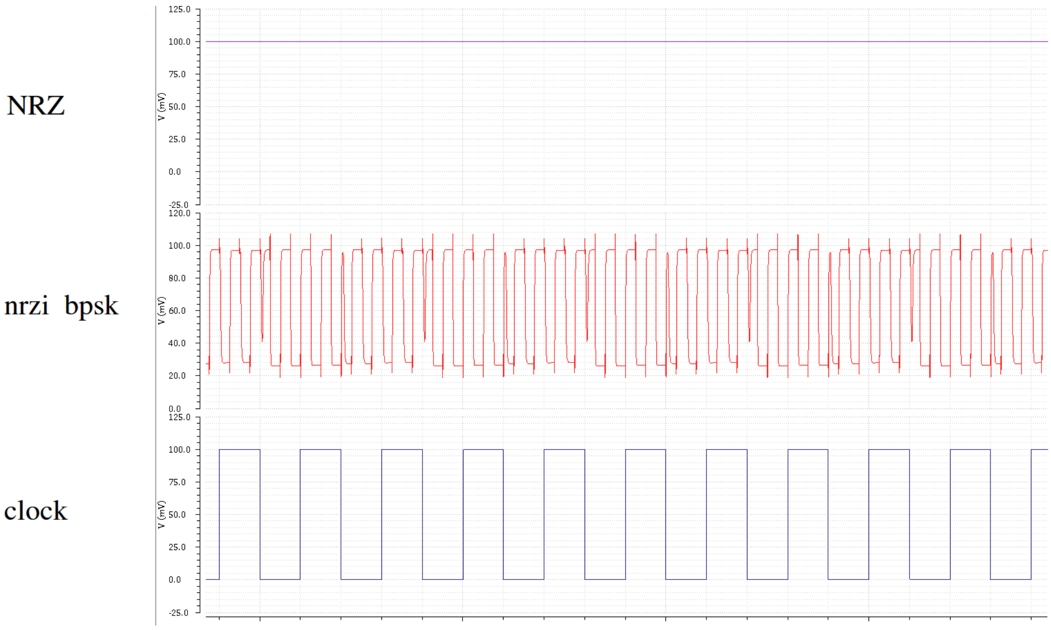

Fig. 4.6 Waveform output of the tx-module with 1 input

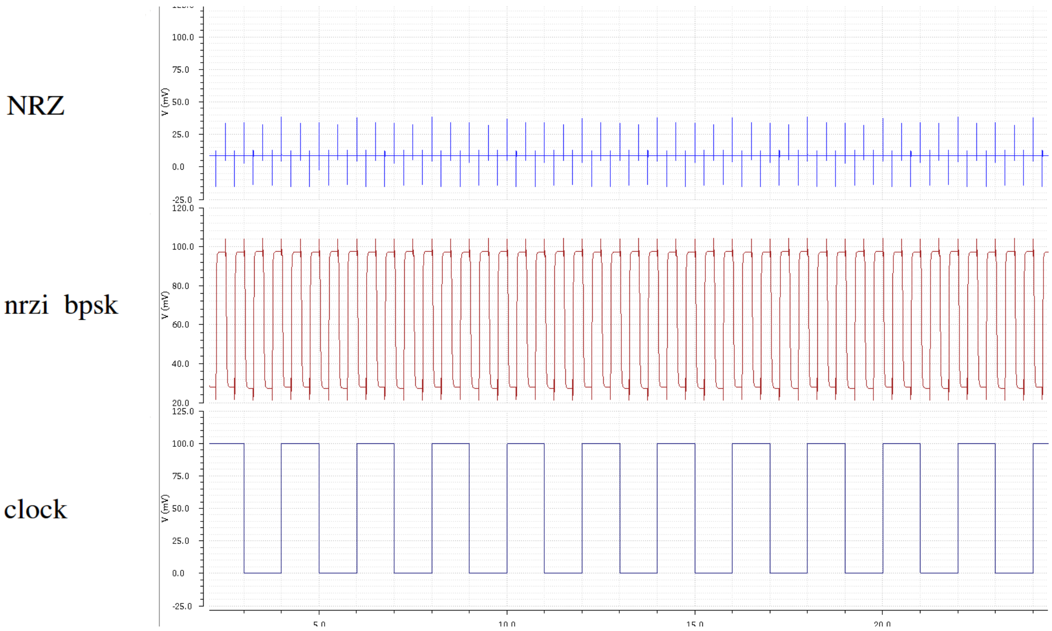

Fig. 4.7 Waveform output of the tx-module with 0 input

4.1.5 RX-module

The RX-module works at 130mV. The waveforms without glitches and with a satisfactory minimal functionial voltage

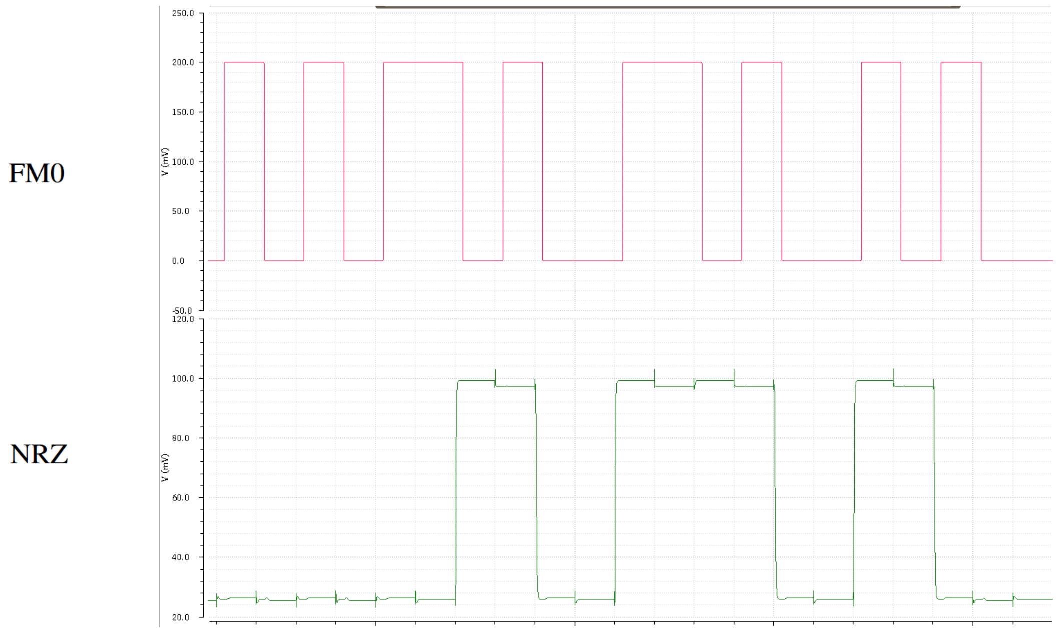

Fig. 4.8 Waveform output of the rx-module

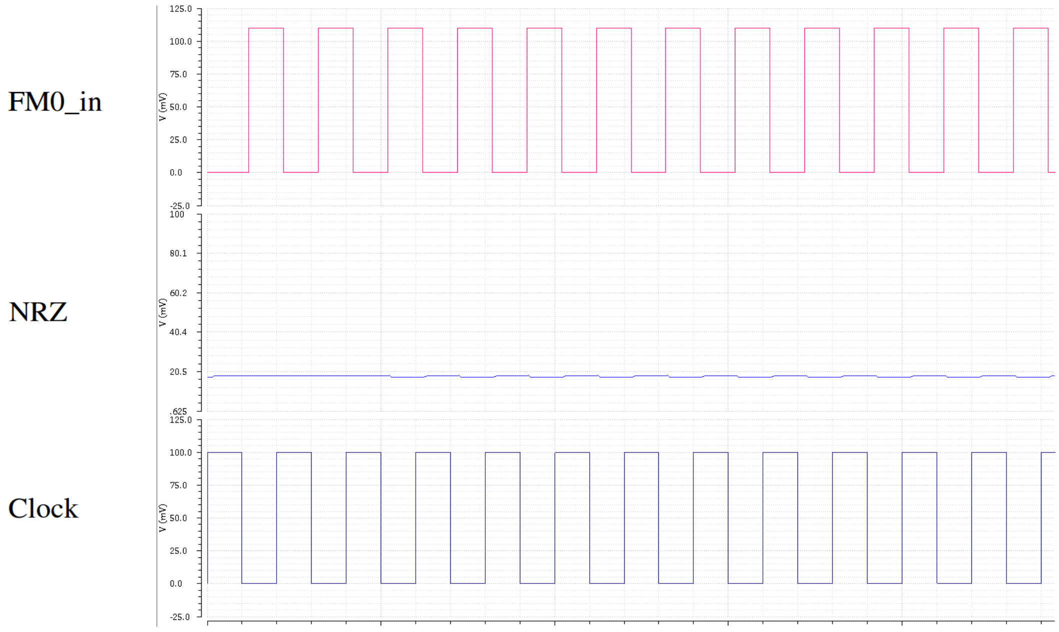

Fig. 4.9 Waveform output of the rx-module with 0 input

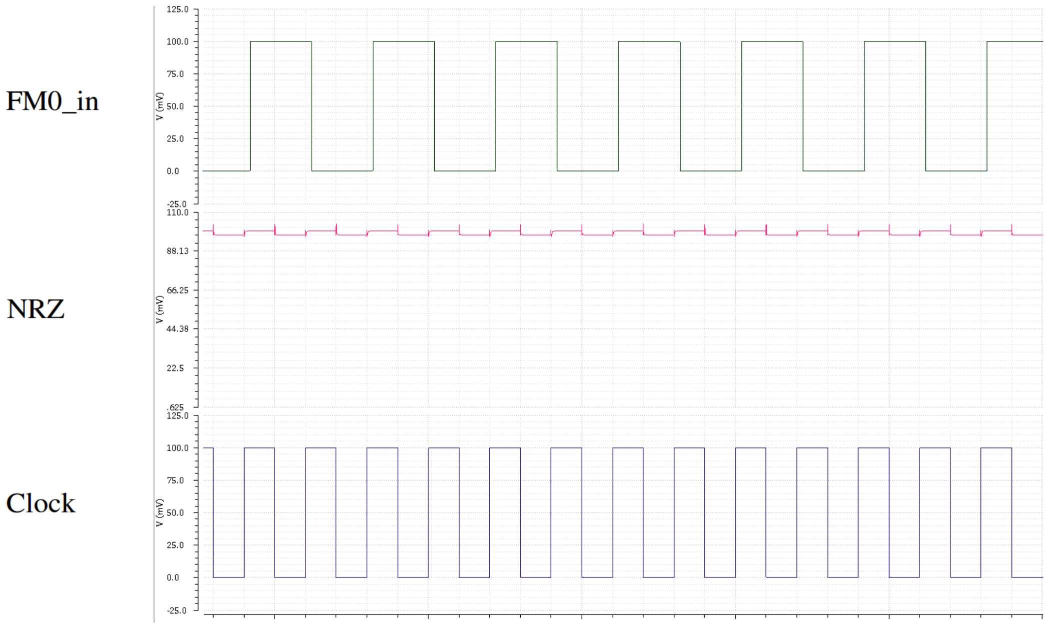

Fig. 4.10 Waveform output of the rx-module with 1 input

4.2 DSRC stack - Test bench

A module implementing a simple command-response functionality is implemented, the stack also has a clear functionality which deleted the transmitted frame.

The minimum functional voltage for the whole DSRC-stack is 200 mV in which the circuit successfully receives and transmits the frames.
The input test vector is shaped like in Figure 4.1, the expected output has a similar shape.
A 500 kHz input clock is used, and a reset input for testing purposes.

4.2.1 Downlink buffer check

After the given input test vector is received, a ’done’ signal is asserted high. This done signal is connected to the input of the uplink.

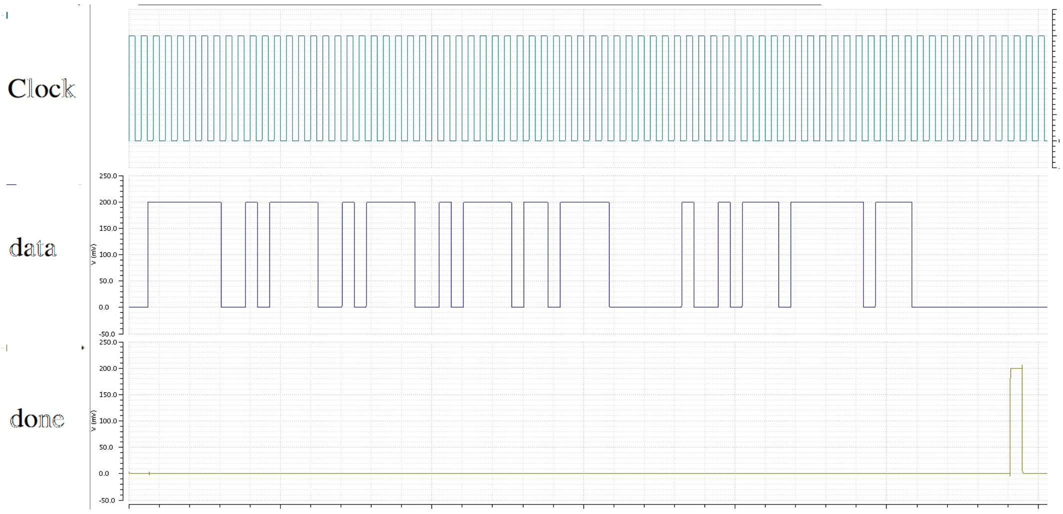

Fig. 4.11 Output/input of the downlink buffer after with correct value in buffer

4.2.2 Abort assertion

After 7 consecutive 1 bits are transmitted a abort signal is asserted high to reset the downlink frame buffer.This works as intended.

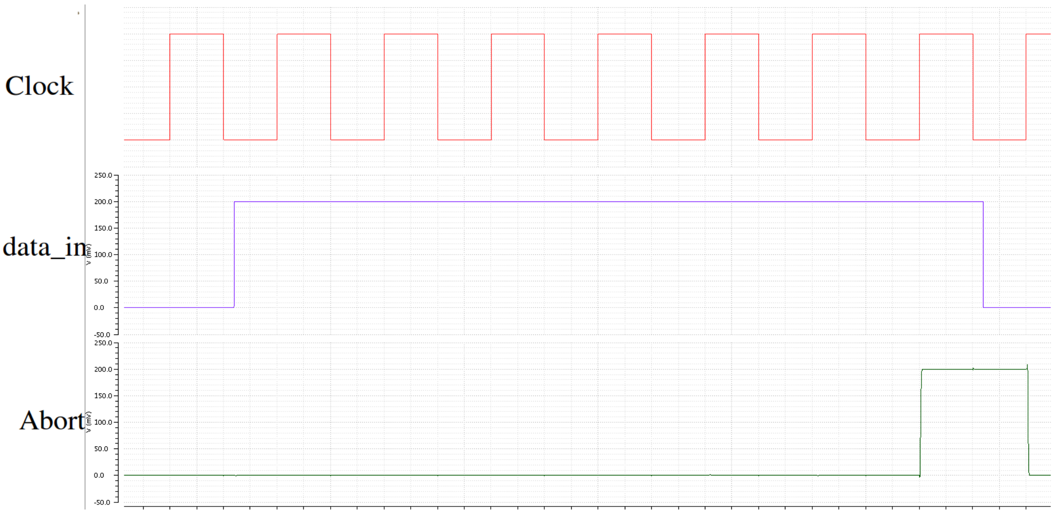

Fig. 4.12 7 consecutive 1 bits asserting the abort bit

4.2.3 Write enable

After 5 ’1’ bits have been transmitted followed by a ’0’ bit. Write enable is asserted low as it clock latches the clock input of the downlink buffer and disables data from being written to the downlink buffer.

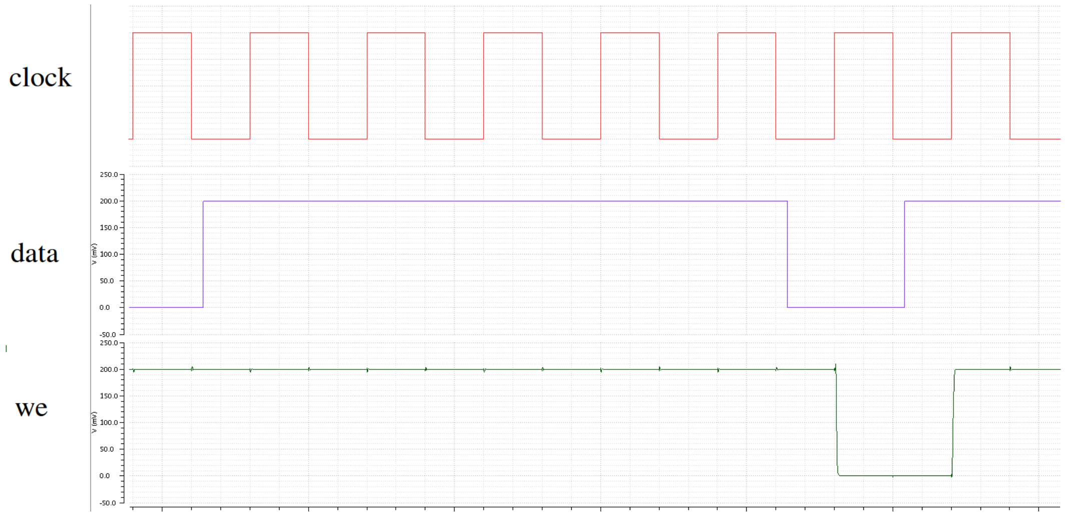

Fig. 4.13

4.2.4 Uplink buffer check

This was left out due to the similarity to the downlink buffer check. The multiplexer circuit and the FIFO buffer is similar to the one used in the downlink buffer check.

4.3 RXTX-module - Power consumption

Power consumption for 65nm and 28nm-FDSOI implementation are presented in the following sections. The 65nm and 28nm-FDSOI simulations are done with three types of transistor types tt, ff, and ss. The clock gates are connected such that all modules are active at the same time, to indicate a worst case scenario power consumption.

The clock latches at the clock input of the rx and tx-module are modified in a way were both modules are active at the same time. This modification is used for the following simulations as it indicates a worst case scenario in terms of power consumption. Special case inputs at both data inputs are used to maximize internal switching activity.
For rx-module; test vector: 0101001011010011
for tx-module; test vector: 111111111

4.3.1 65nm CMOS

In Figure 4.14 TT is under FF and above SS due to differences in internal capacitance. The transistor capacitance affects both the dynamic and static power consumption. For the FF transistor type the static power dissipation is a bigger fraction of the total power consumption as seen in Figure 4.16, while for TT the fraction is smaller and for SS it is smallest as seen in Figure 4.15 and seen in Figure 4.17.

As for the power dissipations under different temperatures, the static power dissipation is sensitive to temperature. This is due to the increased sub-threshold leakage when the temperature is higher, as mentioned in subsection 2.2.2. Comparing Figure 4.18 and Figure 4.21, and Figure 4.23 underlies this statement. The total power dissipation under different temperatures, shows smaller relative differences beeteween the temperatures.

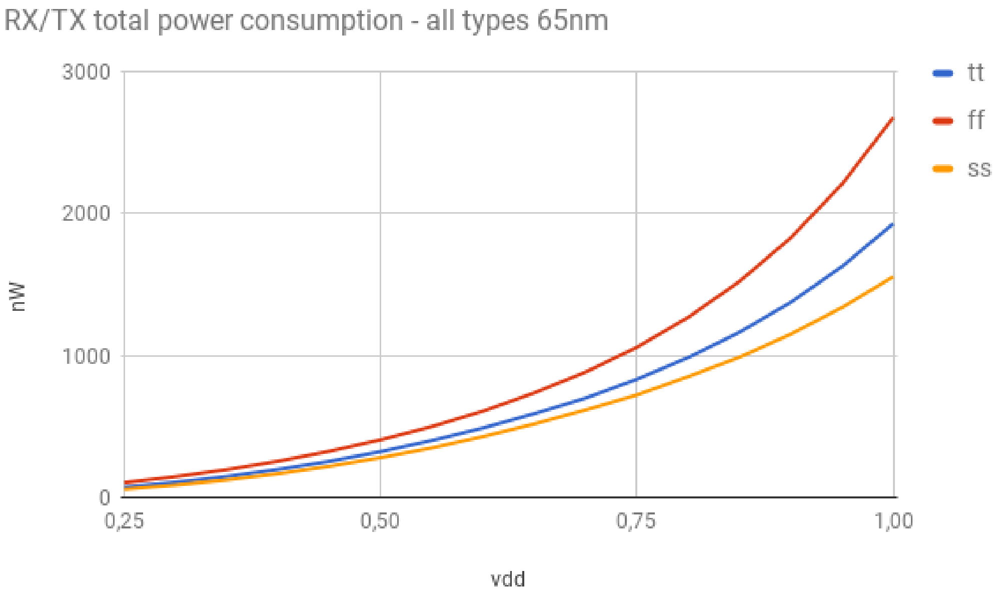

Fig. 4.14 total current consumption for the TT, FF, and SS transistor type

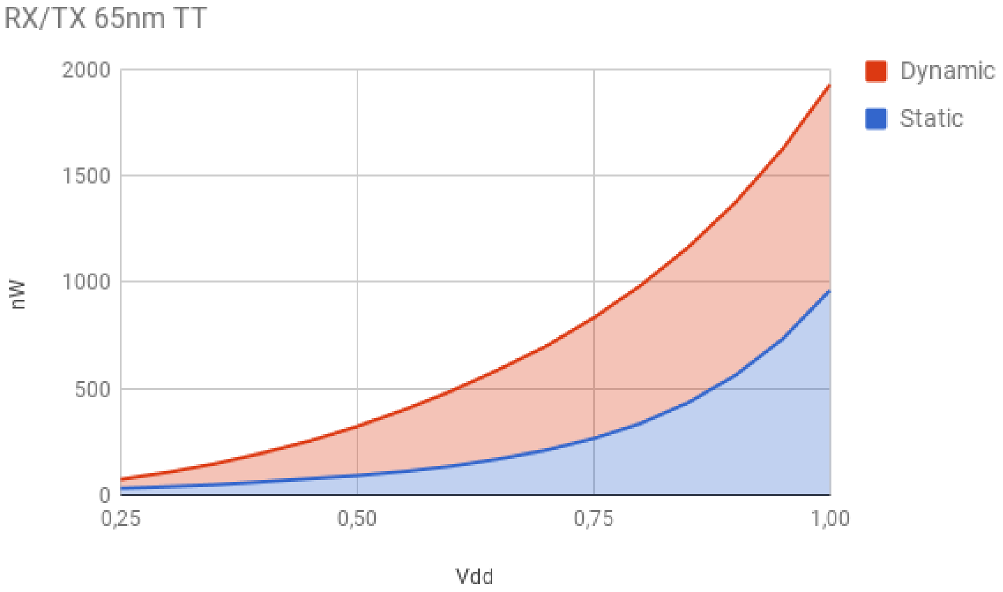

Fig. 4.15 Static and dynamic current consumption for the TT transistor type

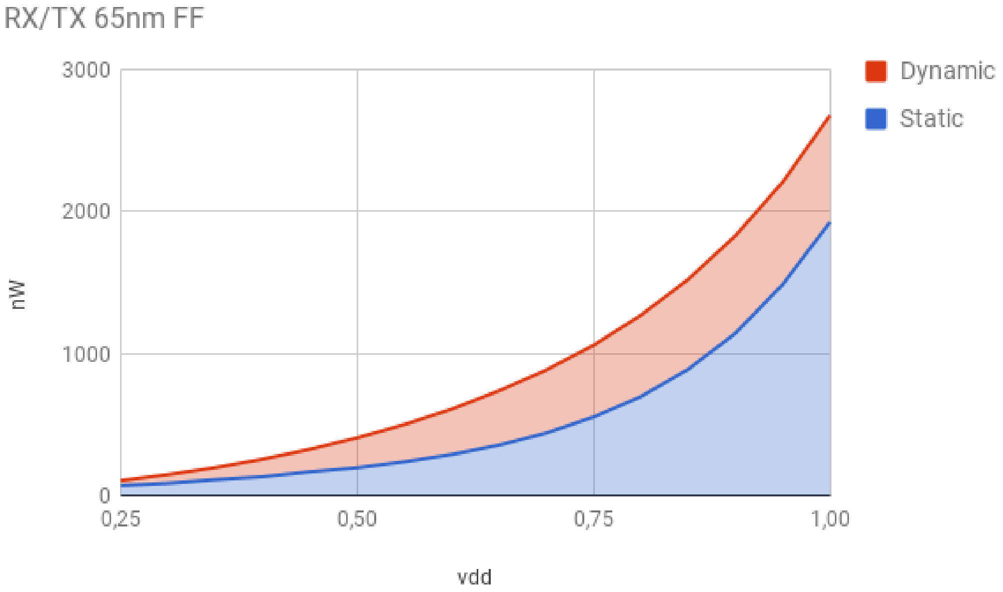

Fig. 4.16 Static and dynamic current consumption for the FF transistor type

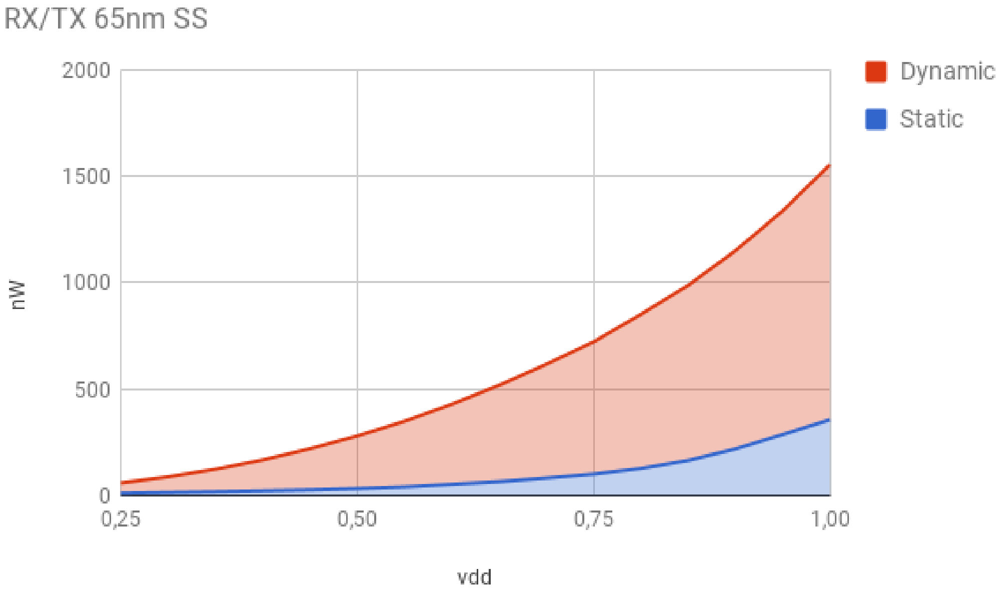

Fig. 4.17 Static and dynamic current consumption for the SS transistor type

Temperature in the following figures.

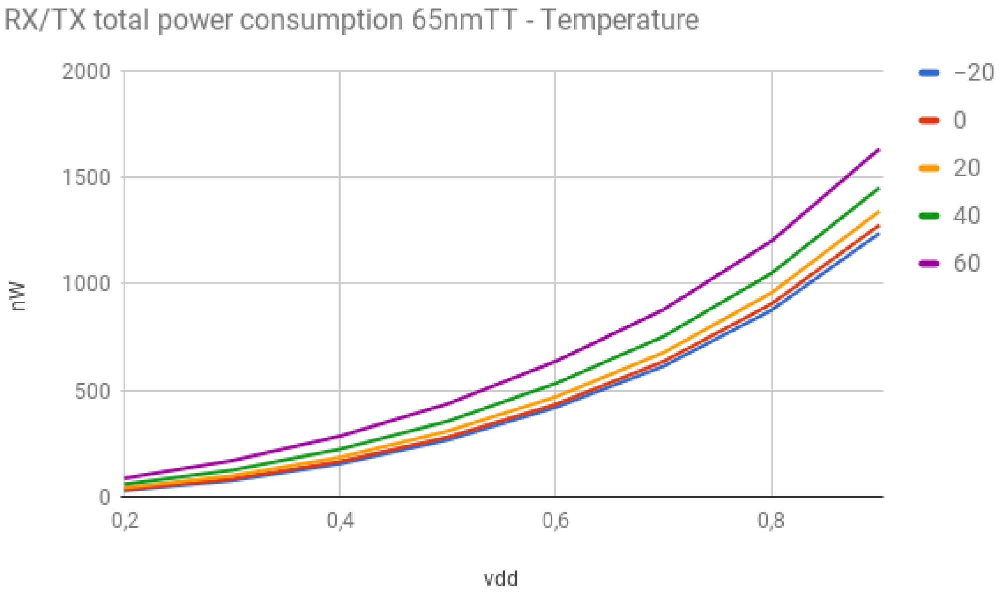

Fig. 4.18 Total current consumption for the TT transistor type under different temperatures

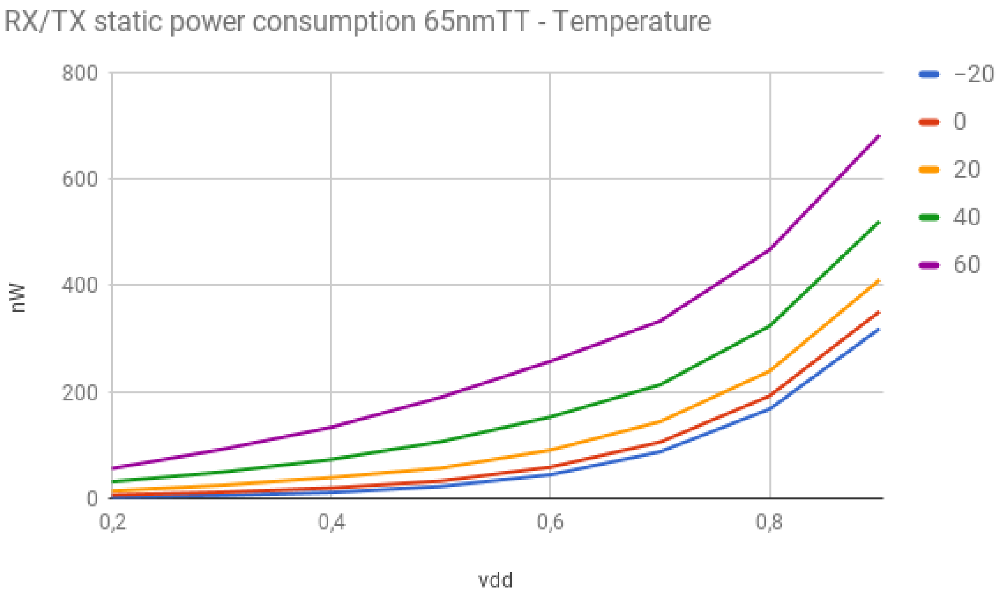

Fig. 4.19 Static current consumption for the TT transistor type under different temperatures

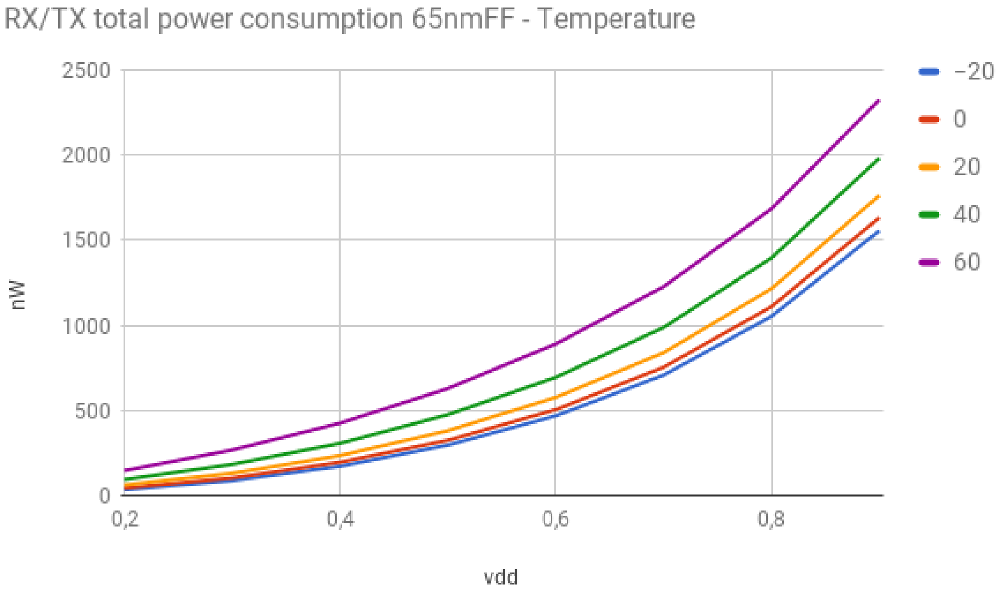

Fig. 4.20 Total current consumption for the FF transistor type under different temperatures

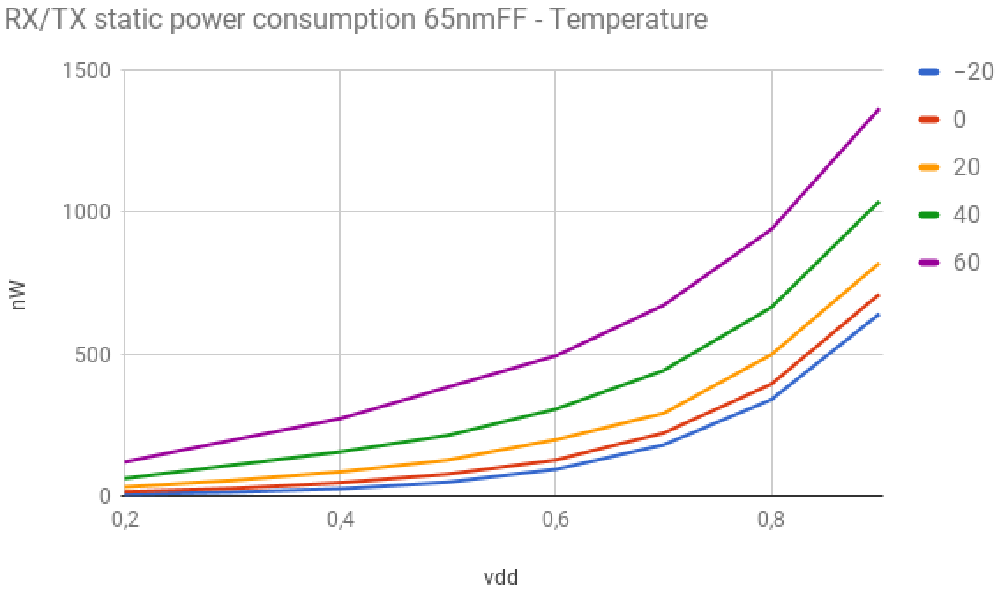

Fig. 4.21 Static current consumption for the FF transistor type under different temperatures

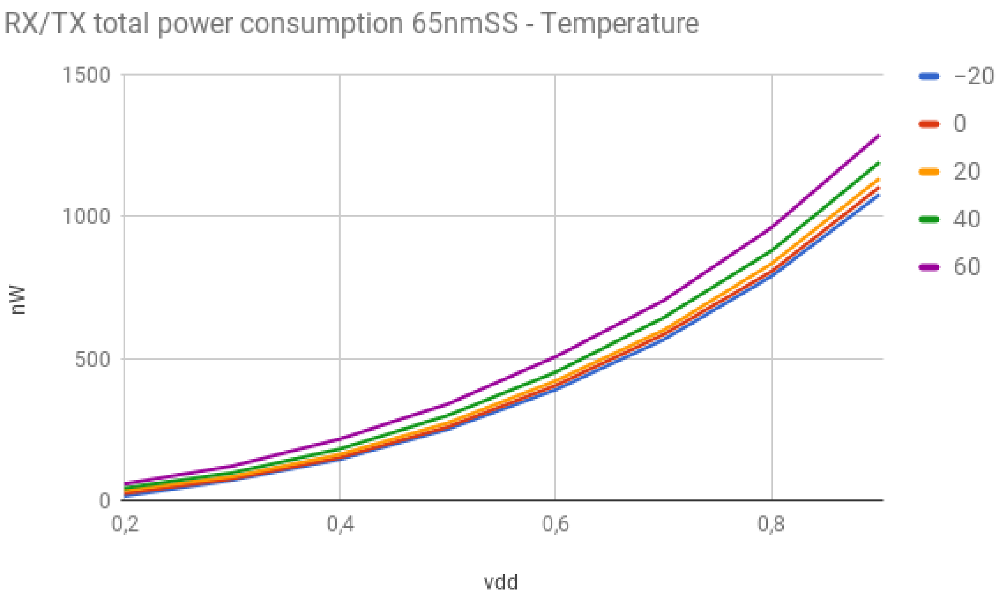

Fig. 4.22 Total current consumption for the SS transistor type under different temperatures

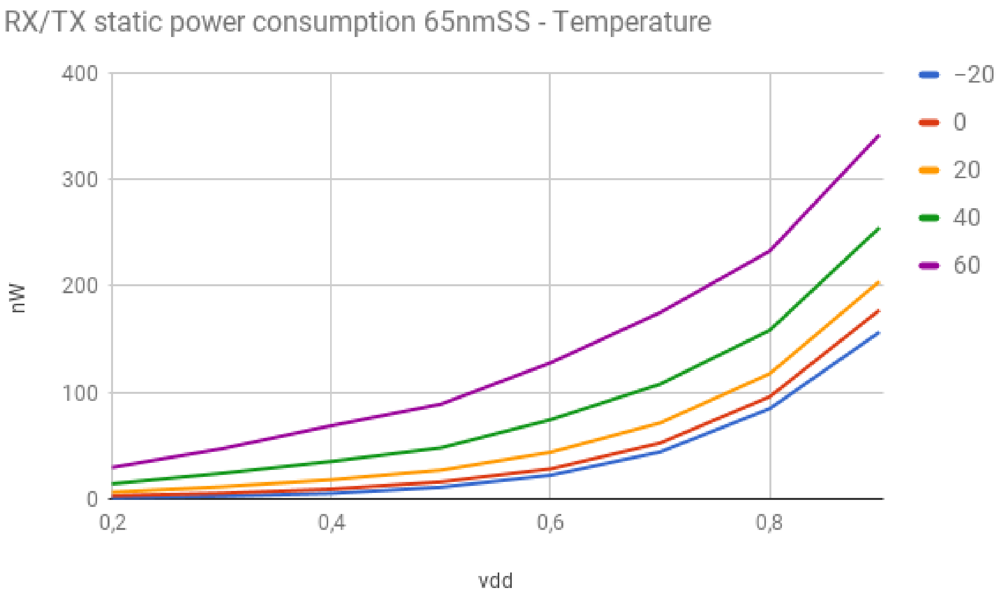

Fig. 4.23 Static current consumption for the SS transistor type under different temperatures

4.3.2 RXTX - 28nm FDSOI

Comparing the Figure 4.24 and Figure 4.14 the differences in power dissipation is significant. The power dissipation is approx. 4 times smaller using 28nm FD-SOI.

As seen in Figure 4.45, Figure 4.46, and Figure 4.47, the capactiance changes the overall power consumption signnificantly. As the dynamic dissipation is influenced by the the capacitance of the transistors.
The way FDSOI transistors are built, helps mitigate the effects of technology downscaling. Among the reduced effects are oxide layer tunneling. Oxide layer tunneling is one of the major sources to leakage when shrinking process node. As for the measurements done under different temperatures. The static power dissipation is a larger fraction of the total power consumption. This was expected due to the size of process node. However, using bulk cmos with a similar sized process node could cause even larger total power consumption than smaller technology nodes.

The temperature simulations also show greater relative differences during different temperatures. This underlies the statement that the sub-threshold leakage is a major contributor of the static power dissipation for smaller technology nodes.

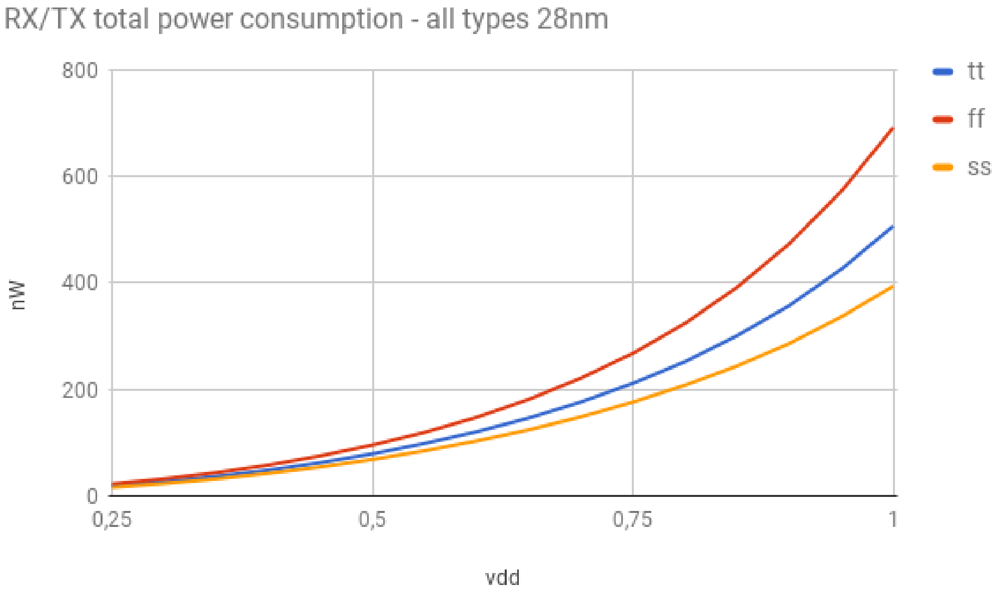

Fig. 4.24 Total current consumption for the TT, FF, and FF transistor type

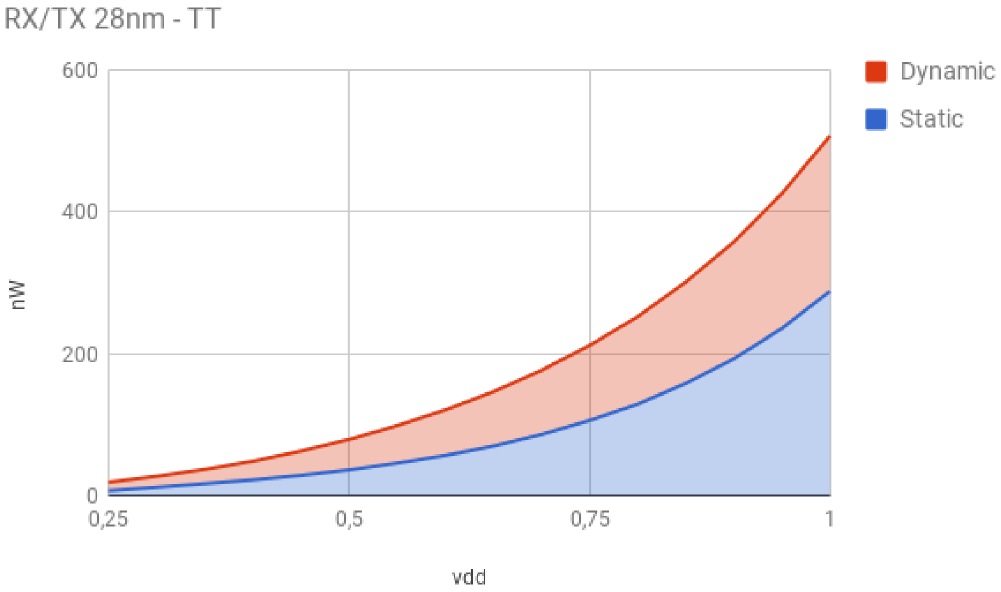

Fig. 4.25 Static and dynamic current consumption for the TT transistor type

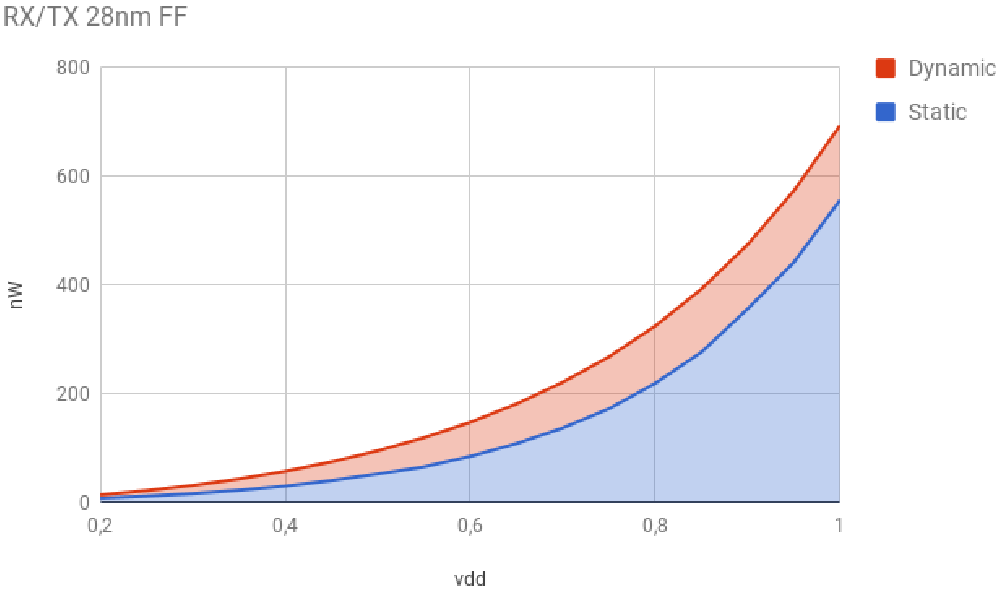

Fig. 4.26 Static and dynamic current consumption for the FF transistor type

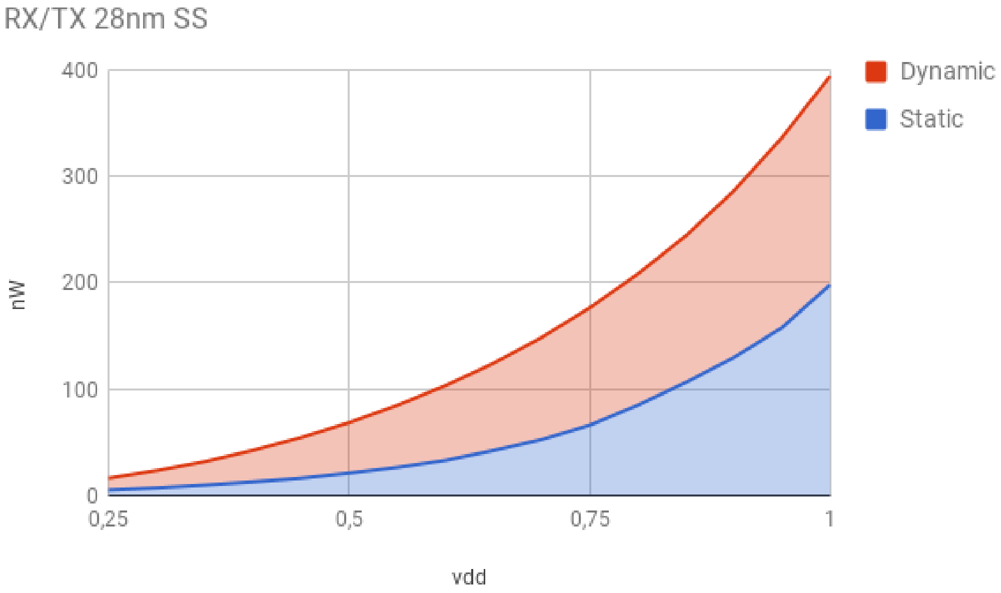

Fig. 4.27 Static and dynamic current consumption for the SS transistor type

Temperature in the following pictures.

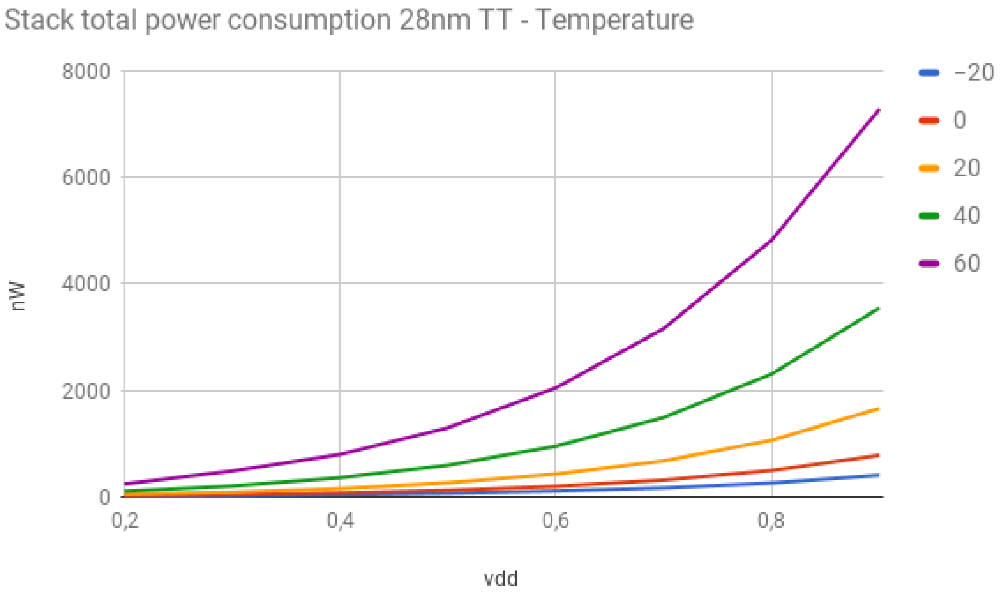

Fig. 4.28 Total current consumption for the TT transistor type under different temperatures

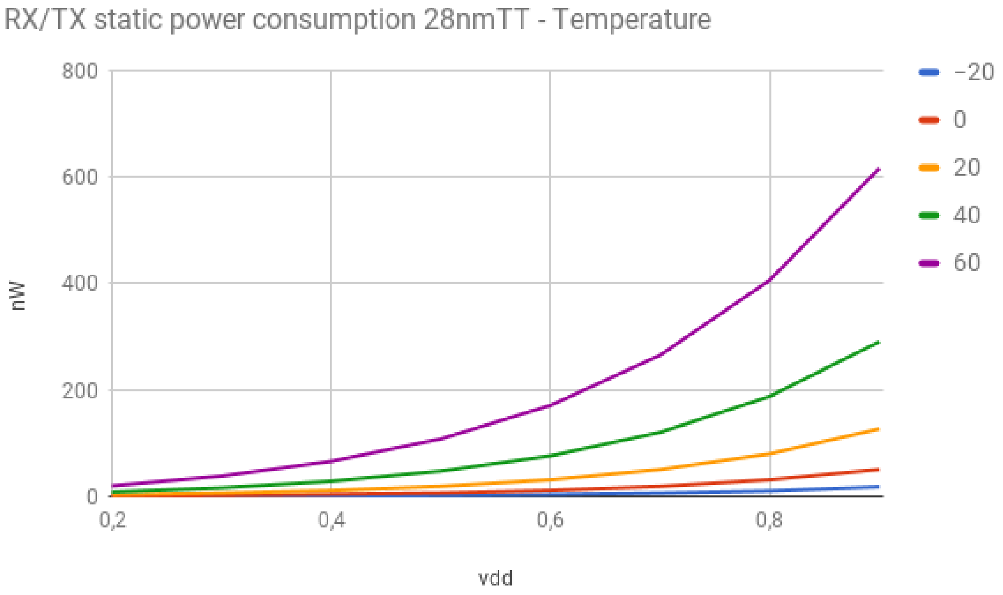

Fig. 4.29 Static current consumption for the TT transistor type under different temperatures

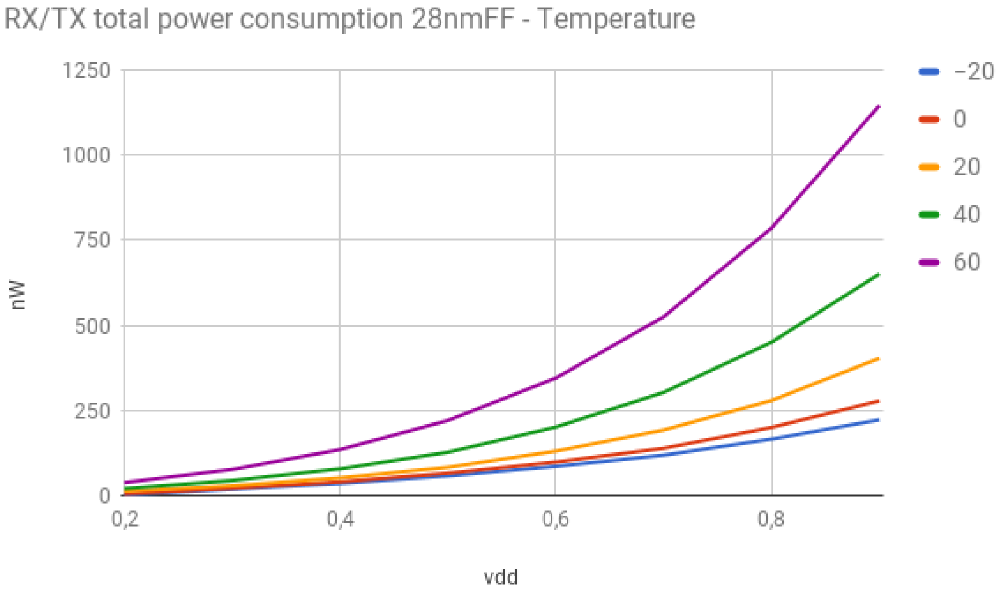

Fig. 4.30 Total current consumption for the FF transistor type under different temperatures

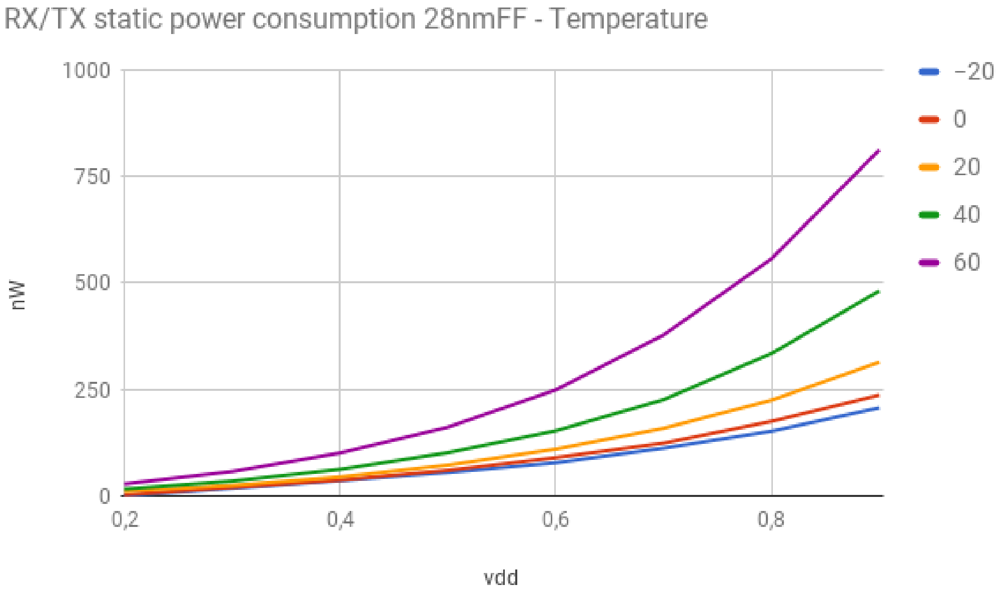

Fig. 4.31 Static current consumption for the FF transistor type under different temperatures

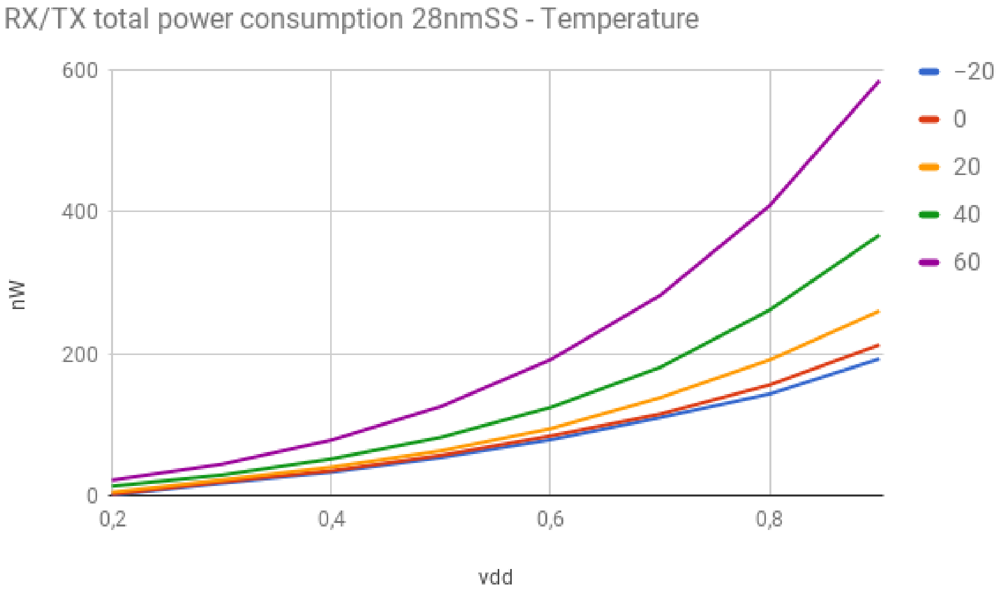

Fig. 4.32 Total current consumption for the SS transistor type under different temperatures

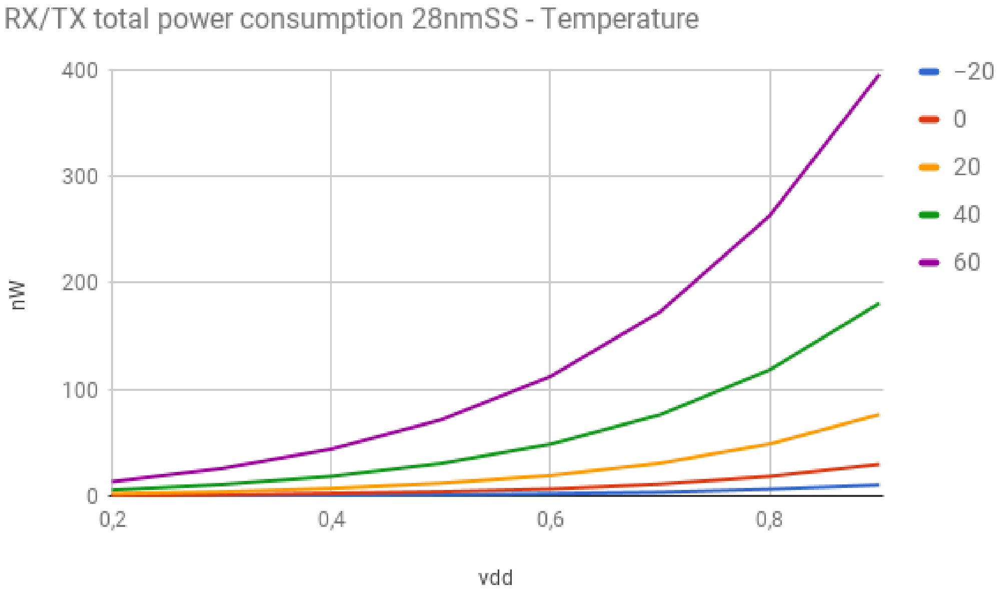

Fig. 4.33 Static current consumption for the SS transistor type under different temperatures

4.4 DSRC-stack - Power consumption

Power consumption for the DSRC stack are presented in the following sections.

4.4.1 DSRC-stack - 65nm CMOS

The power dissipation for the DSRC-stack is as expected several orders higher due to larger circuit area. Although the number of gates is approximately 10 times higher, the power dissipation has not scaled proportionally due to lower clock frequency. The circuit works at a minimum of 200 mV, which is close to the minimum functional voltage for the RXTX-module of 150 mV.

As for static power dissipation, the static dissipation is a larger fraction than for the RXTX-module. This is expected as the frequency is lower and the circuit is larger.

Like in the RXTX-module, the same trends in power dissipation can be seen in the results of the stack. Figure 4.35, Figure 4.35, and Figure 4.35 shows different levels of power dissipation. Where the SS type gives a lower total dissipation due to lower capacitance, while FF gives highest total power dissipation due to high capacitance.

For the temperature simulations seen in Figure 4.38 to Figure 4.41, the behaviour is similar to the ones found for the RXTX-module. As the static consumption accounts for most of the total power consumption, the distribution of power consumption between temperatures are similar for total and static.

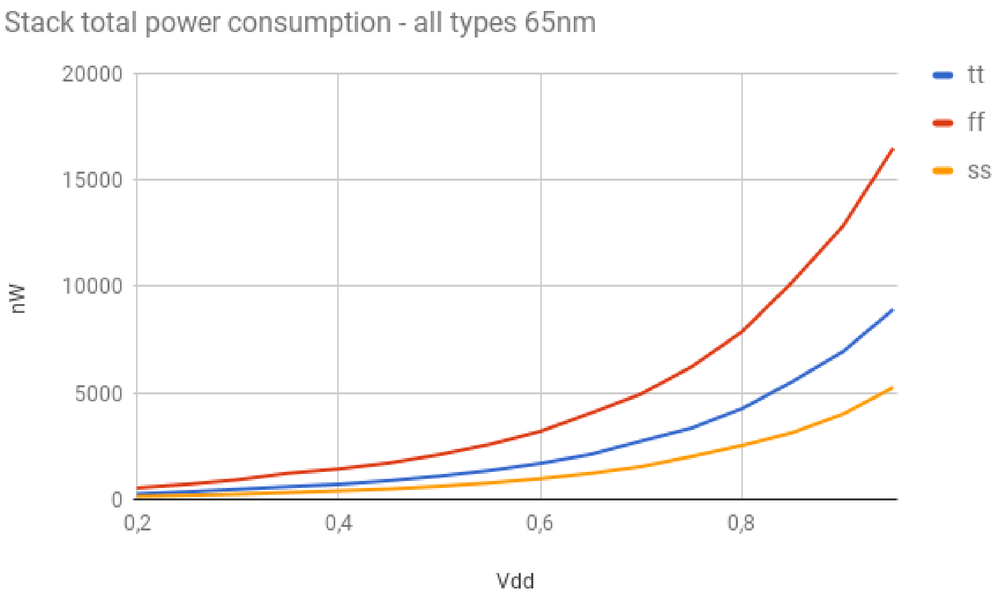

Fig. 4.34 Total current consumption for the TT, FF, and SS transistor type

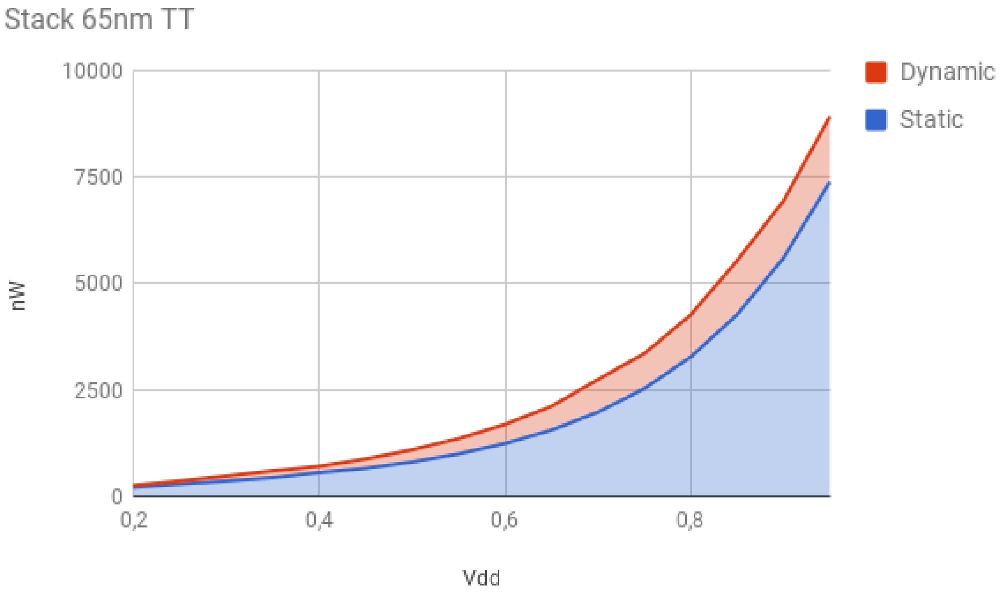

Fig. 4.35 Static and dynamic current consumption for the TT transistor type

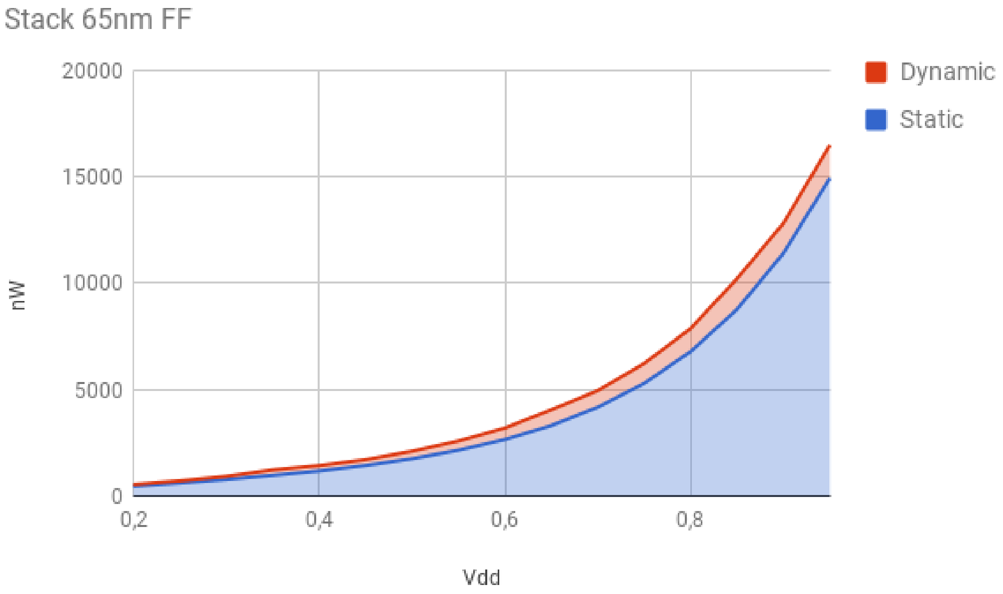

Fig. 4.36 Static and dynamic current consumption for the FF transistor type

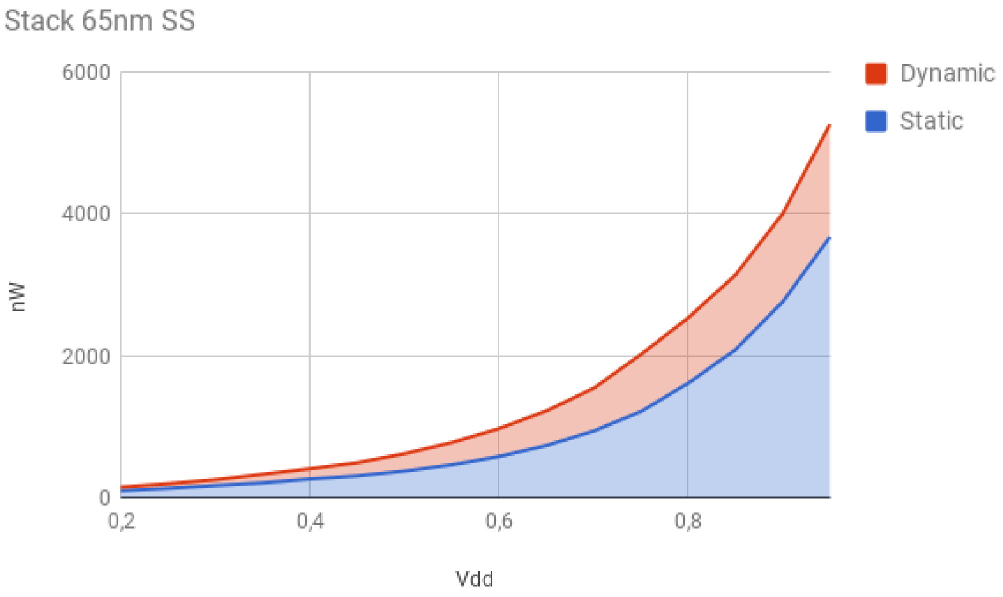

Fig. 4.37 Static and dynamic current consumption for the SS transistor type

Temperature in the following pictures.

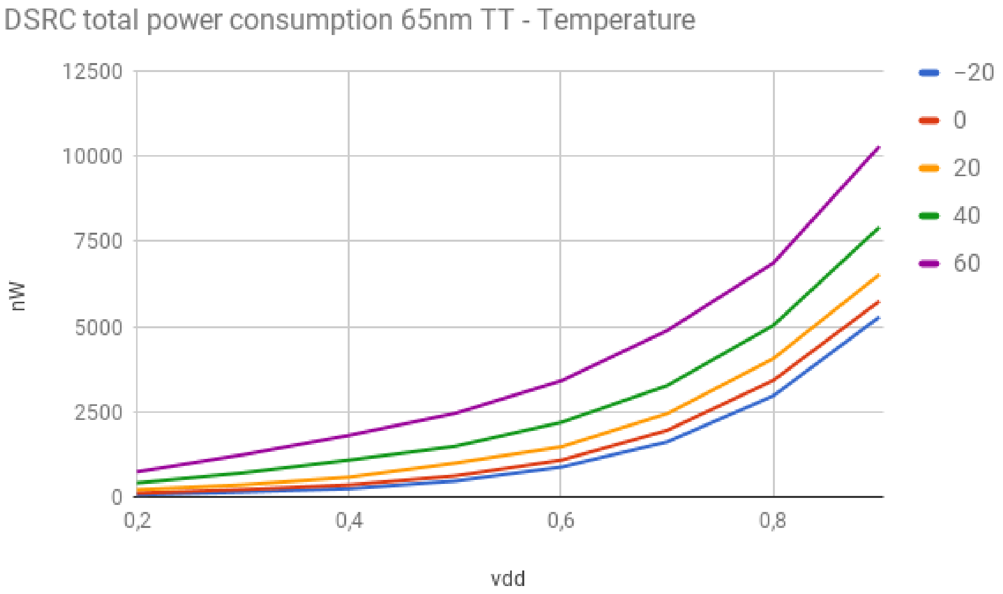

Fig. 4.38 Total current consumption for the TT transistor type under different temperatures

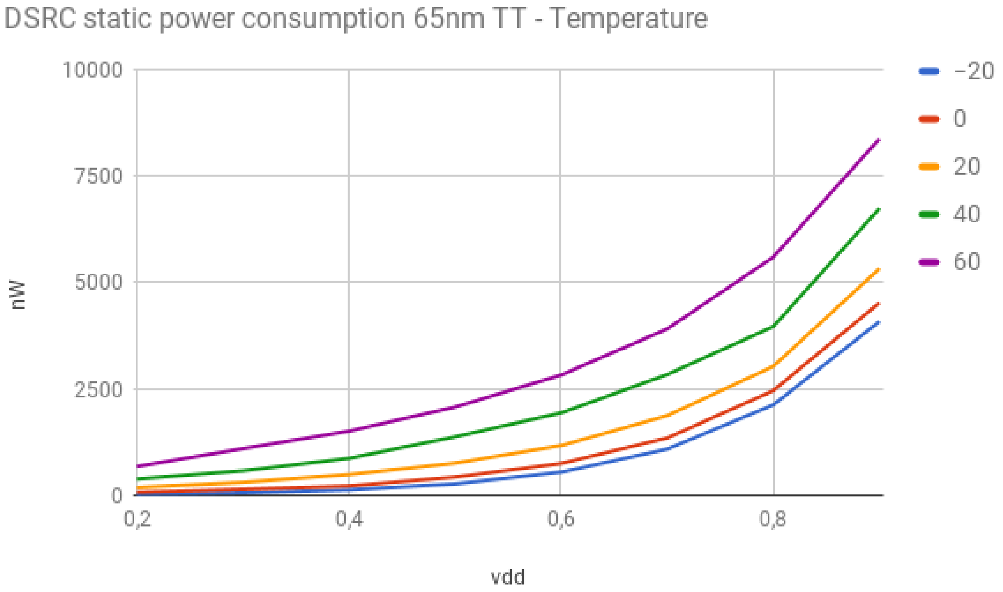

Fig. 4.39 Static current consumption for the TT transistor type under different temperatures

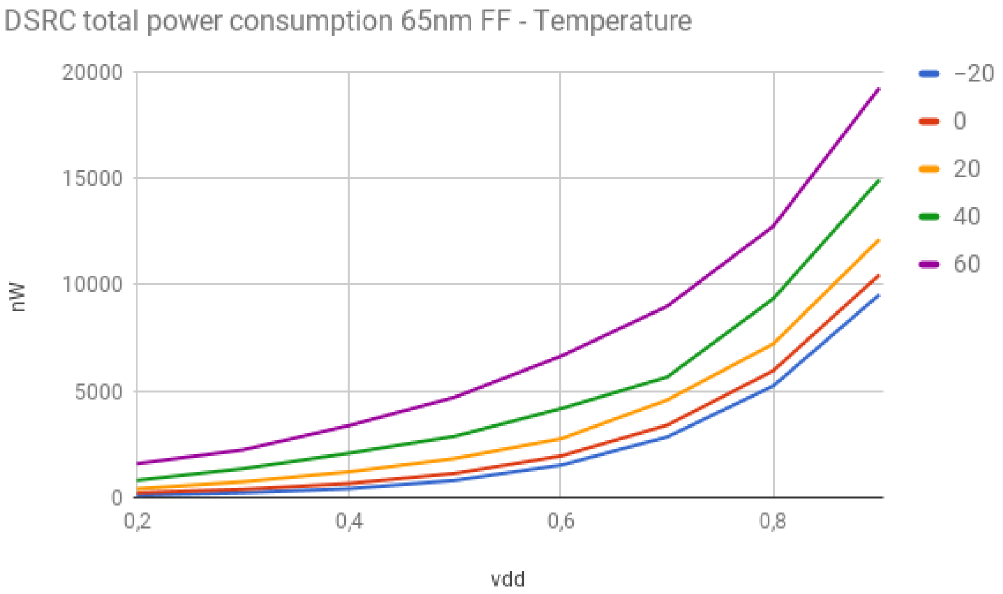

Fig. 4.40 Total current consumption for the FF transistor type under different temperatures

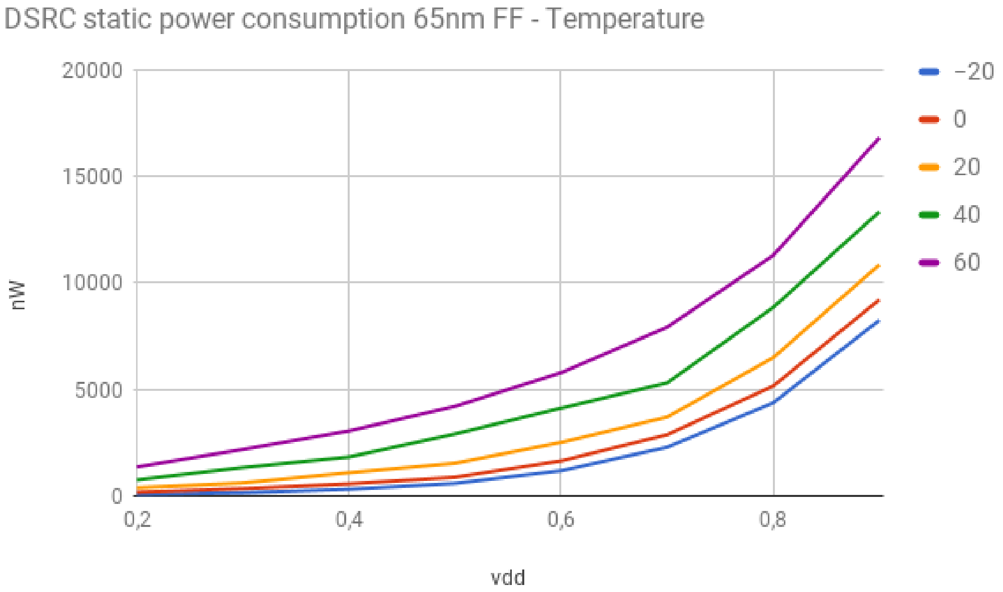

Fig. 4.41 Static current consumption for the FF transistor type under different temperatures

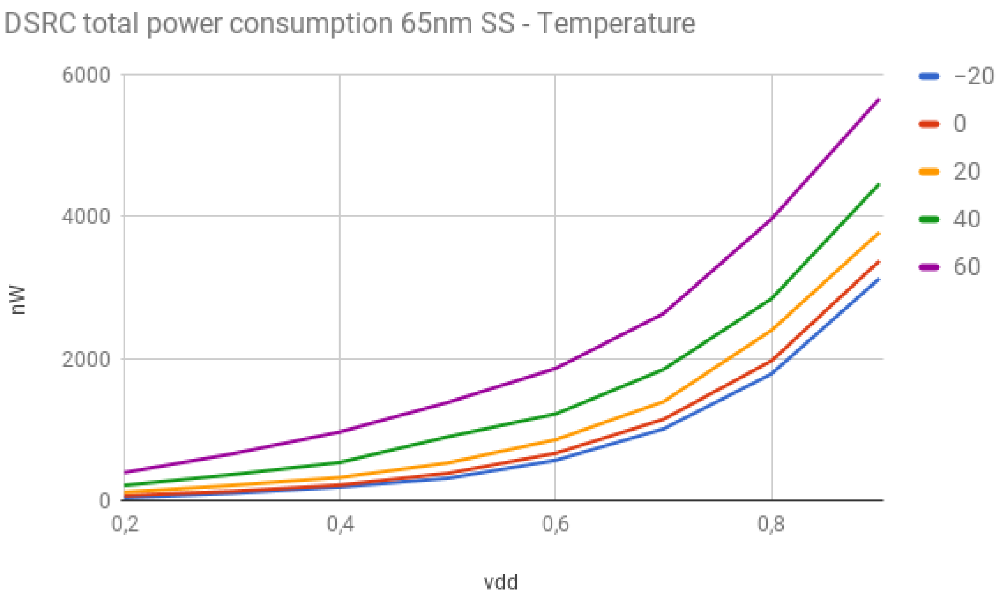

Fig. 4.42 Total current consumption for the SS transistor type under different temperatures

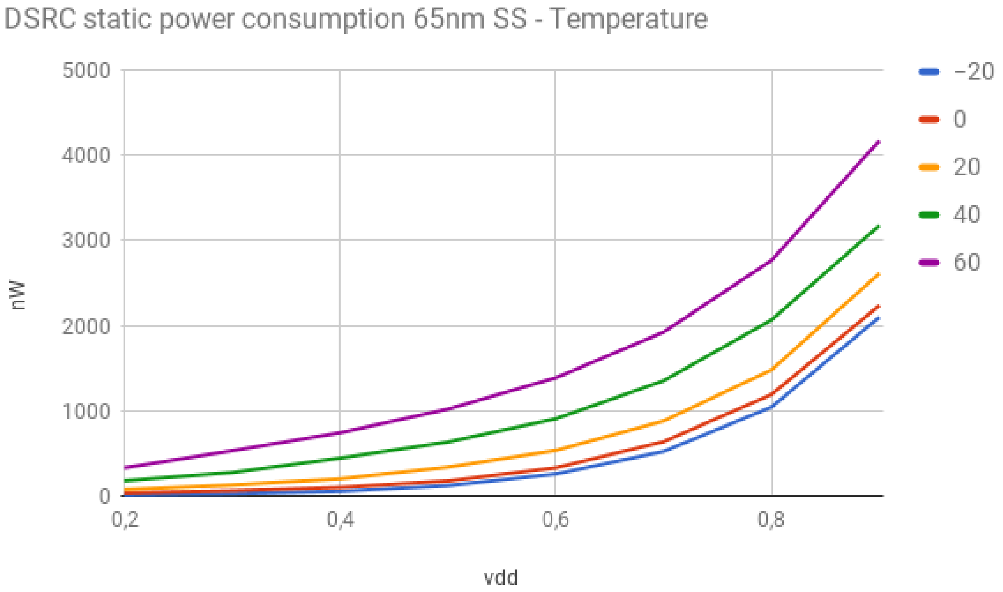

Fig. 4.43 Static current consumption for the SS transistor type under different temperatures

4.4.2 DSRC-stack - 28nm FDSOI

As for the results for the 28nm FDSOI implementation, comparing Figure 4.44 and Figure 4.34 the benefit by using FDSOI 28nm is remarkably strong. The power consumption is on average 1/4th of the 65nm implementaion. As for the temperature simulations, the 28nm shows more sensitivity to temperature, but is always by several orders of magnitude below the 65nm implementation.

The static consumtion accounts for an even larger percentage of the total dissipation. This is very noticable for the temperature simulations, where the static temperature simulations and the total appear with similar shape and characteristics.

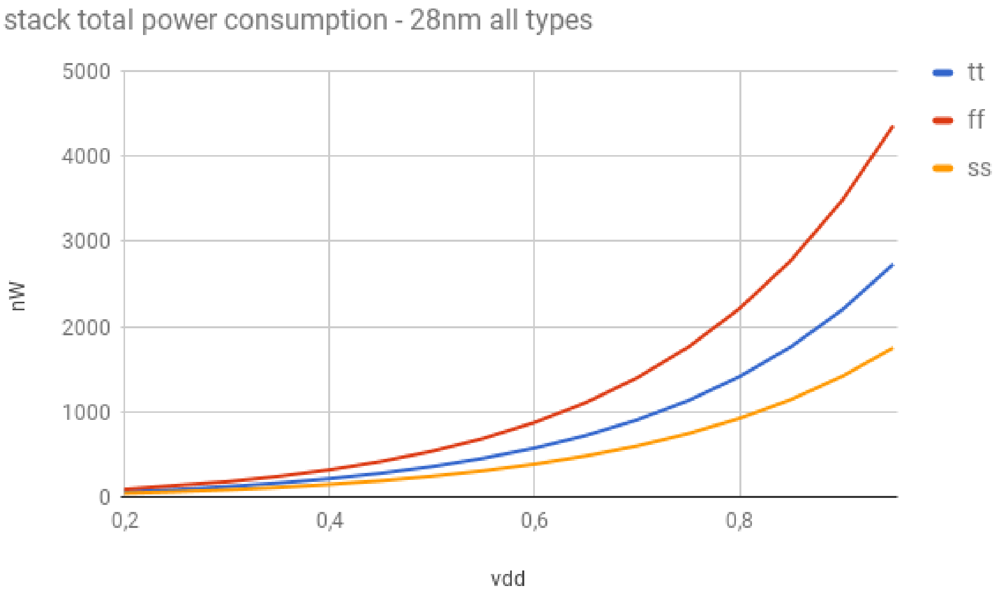

Fig. 4.44 Total current consumption for the TT, FF, and SS transistor type

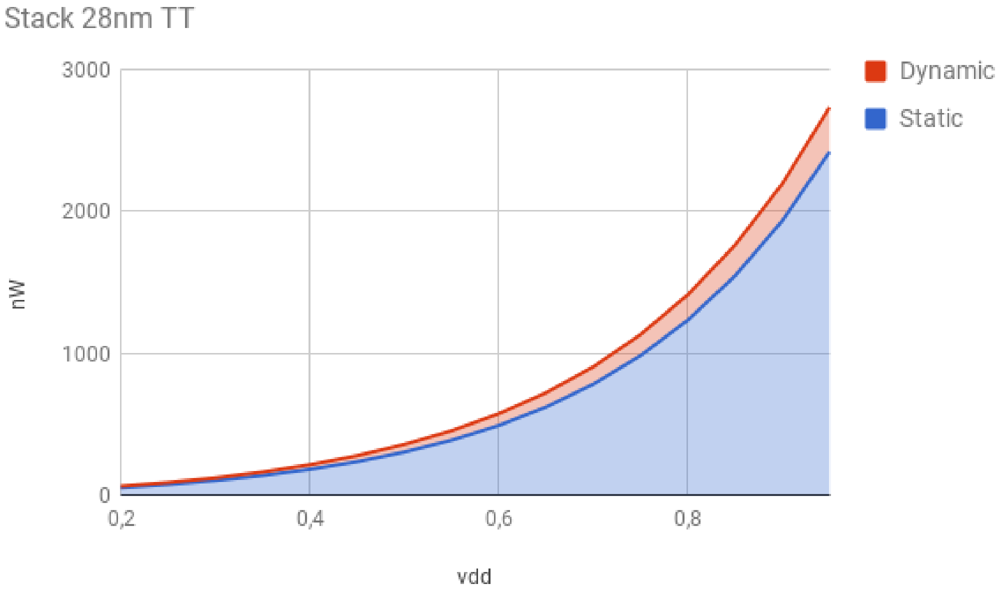

Fig. 4.45 Static and dynamic current consumption for the TT transistor type

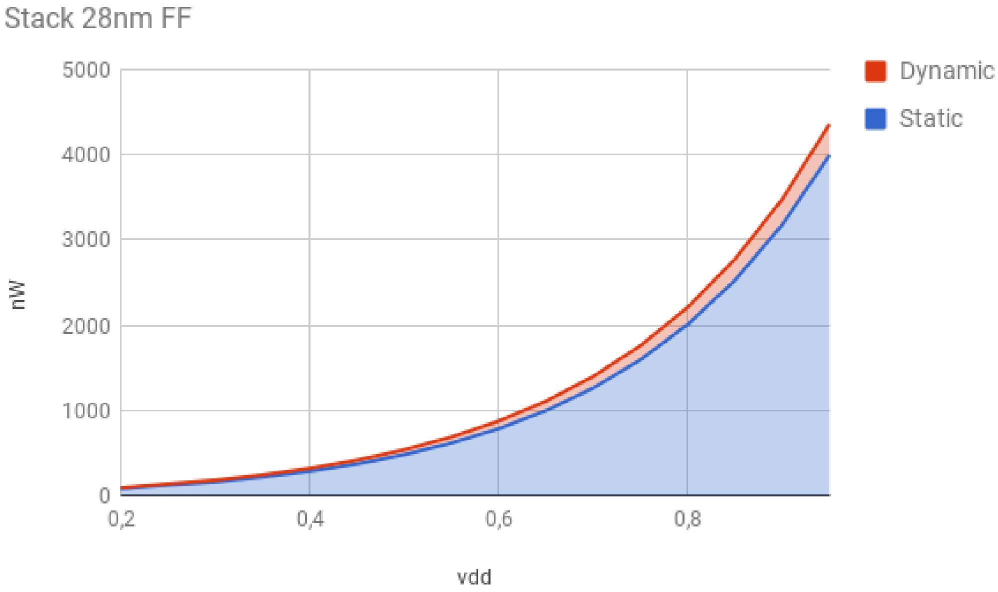

Fig. 4.46 Static and dynamic current consumption for the FF transistor type

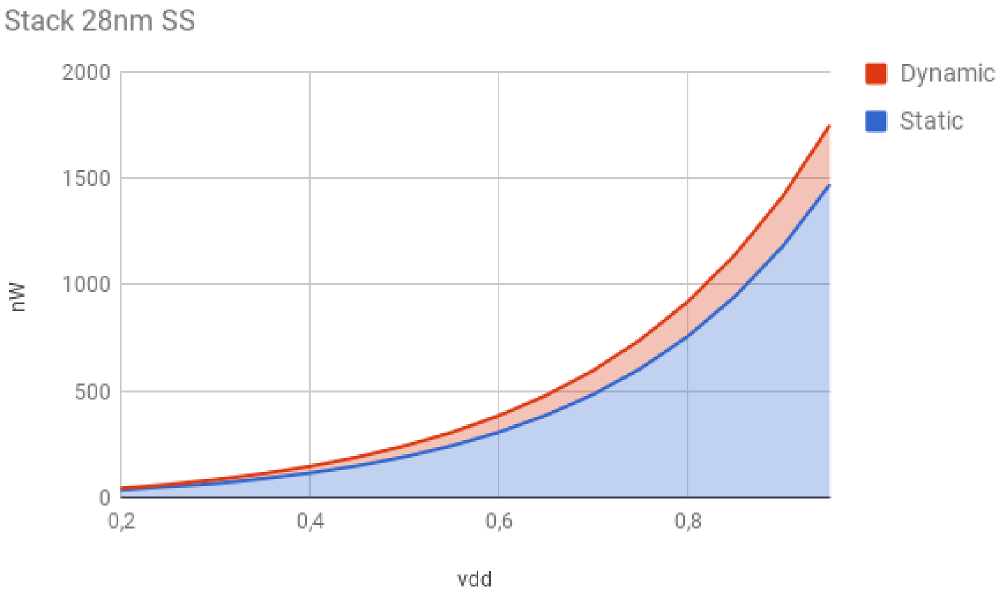

Fig. 4.47 Static and dynamic current consumption for the SS transistor type

Temperature in the following pictures.

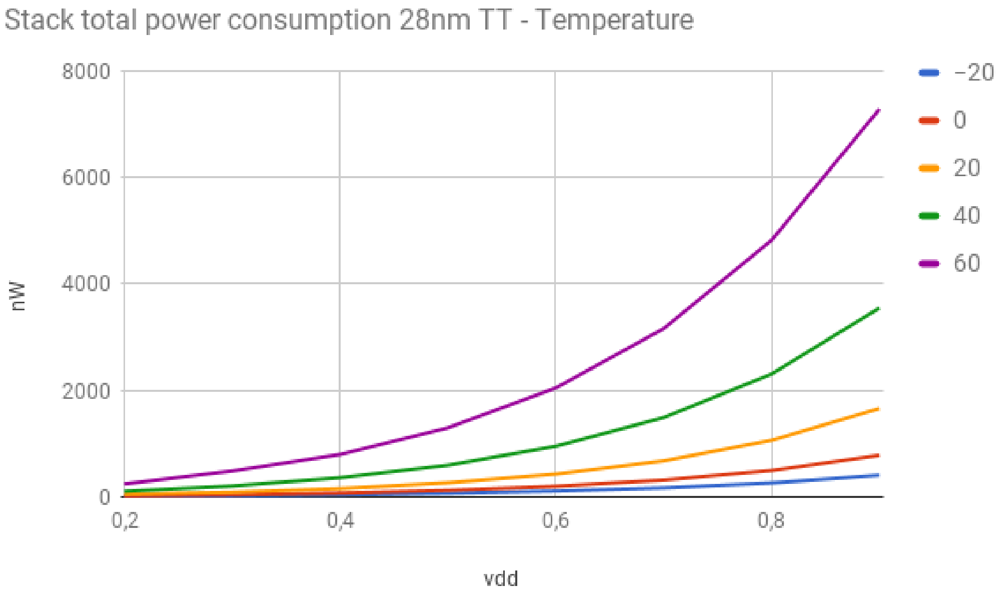

Fig. 4.48 Total current consumption for the TT transistor type under different temperatures

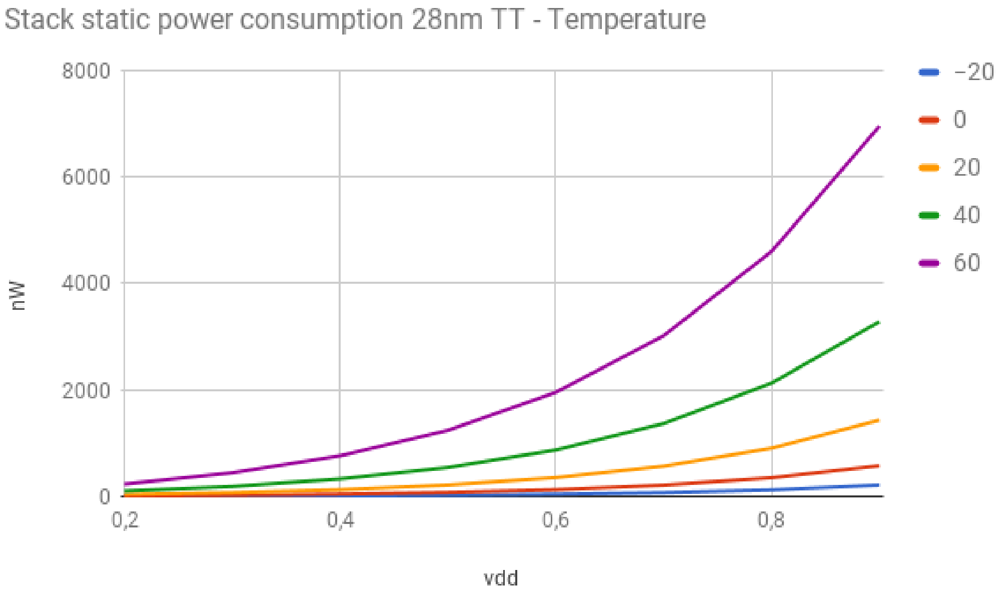

Fig. 4.49 Static current consumption for the TT transistor type under different temperatures

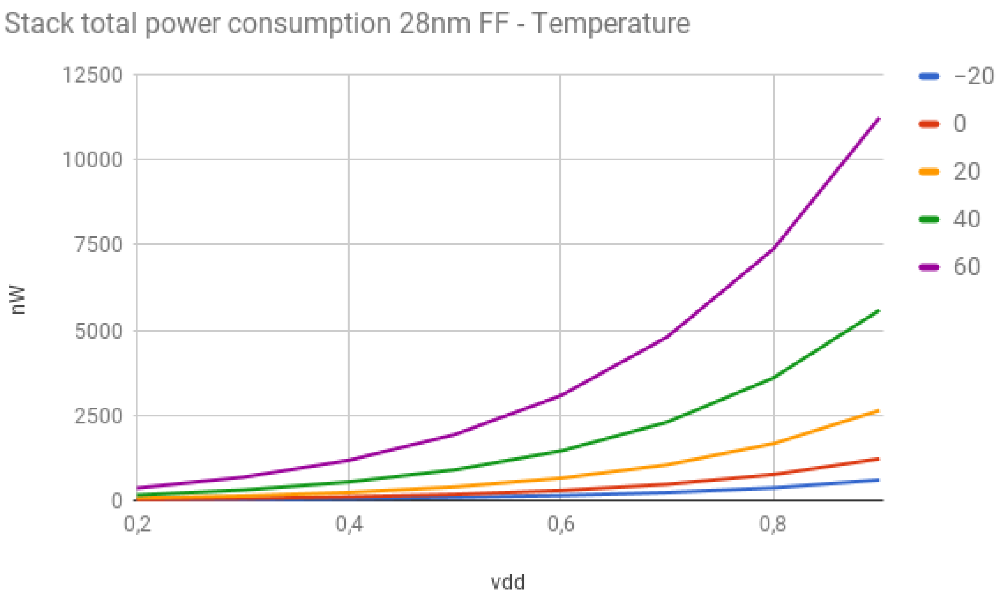

Fig. 4.50 Total current consumption for the FF transistor type under different temperatures

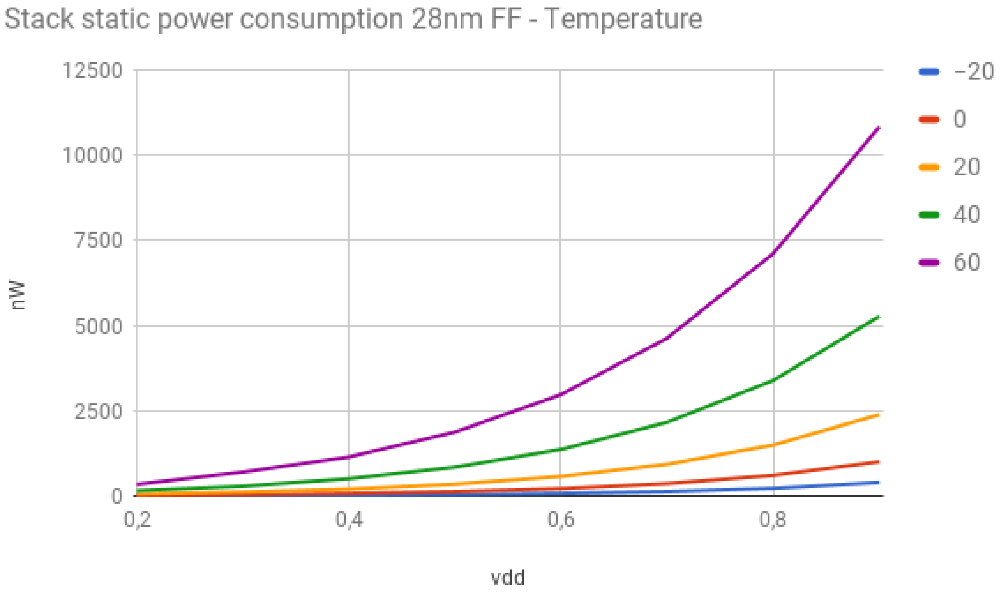

Fig. 4.51 Static current consumption for the FF transistor type under different temperatures

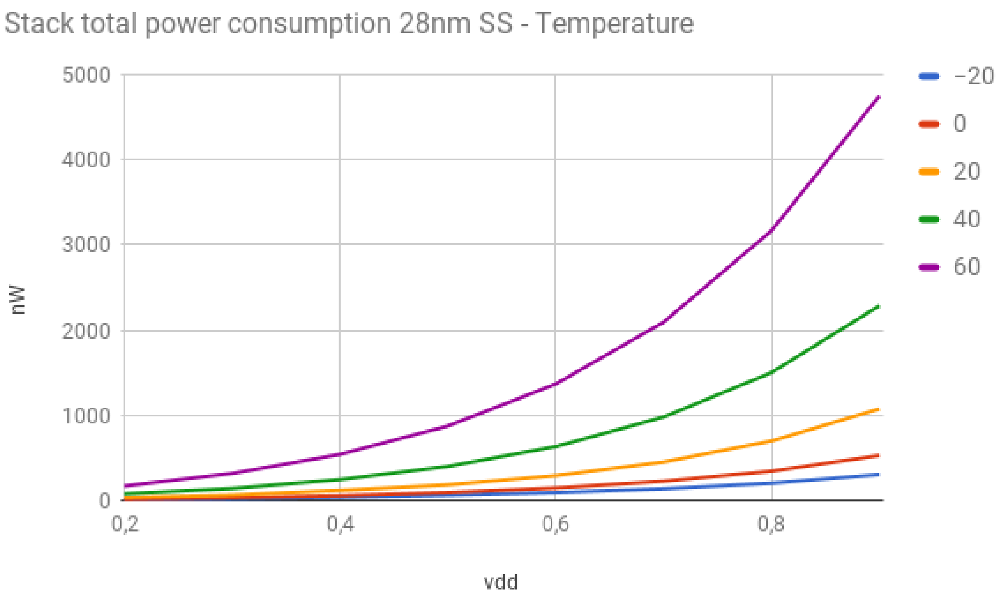

Fig. 4.52 Total current consumption for the SS transistor type under different temperatures

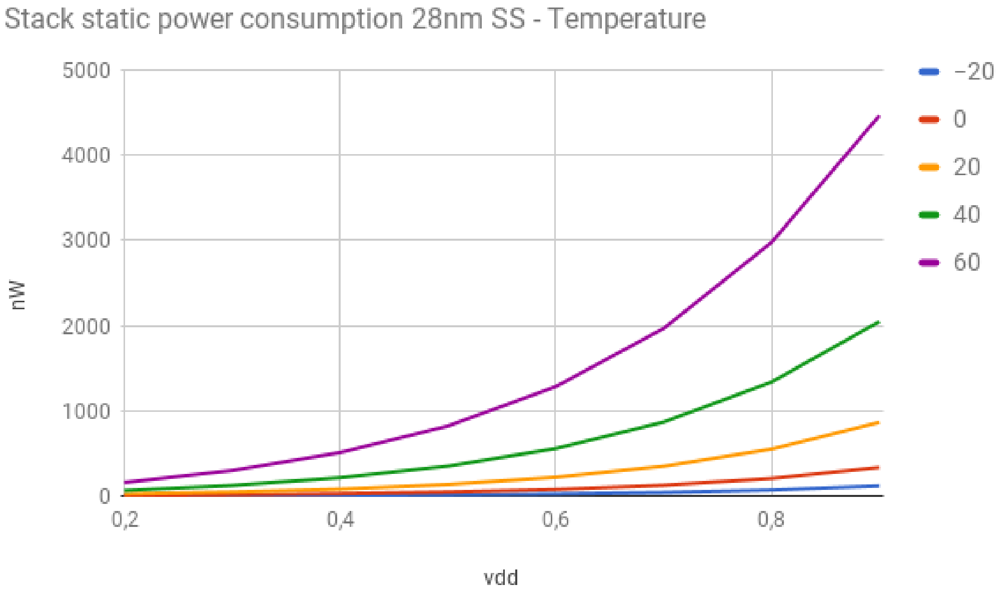

Fig. 4.53 Static current consumption for the SS transistor type under different temperatures

CHAPTER 5

Discussion

The results are satisfactory in terms of expected improvement. This is not a good enough performance for a energy harvesting application. Choosing a even smaller process node is a possible next step in getting closer to a fully functional design. Outside the design improvements in ultra low power voltage pumping are expected to be made as energy harvesting is still in a early phase in terms of application area. As the minimum input signal is very weak, making also the requirements to antenna and voltage pumping fulfill at this time. The future may hold fruitful a solution to many of the issues existing within energy harvesting.

The RX/TX-module is not subject to big improvements design wise. The number of cells used are as low as possible, and there is little to gain power wise by pushing the cell number down.

The DSRC stack can be improved in many ways. The current design does not employ clock gating, since the FIFO buffers already are a big drain of power as it accounts for a lot of the circuit size, a lot of dynamic power consumption could be reduced by implementing a clock gating solution in the stack. Other improvements to the stack could be architectual improvements, as the maximum downlink and uplink frame size is 1024 bits. By comparision the implemented downlink buffer holds 64 bits, and the uplink holds 72 bits. Having a multiplexer implemented like in the current implementation would end in a huge multiplexer tree, probably causing bigger timing issues.

Overall there is always a need for improvement to ensure a functional circuit which can successfully receive and decode and transmit a message/ several messages back. All this under different conditions in terms of weak/variating input signal, low/high temperatures etc. The time constraint is a hard deadline and a OBU not successfully doing its task is critical in this application.

So a implementation using a smaller technology node is a logical next step in the research of this design, which may be fruitful. Changing technology may introduce new challenges and is also a more expensive technology than older technology. Implementing a energy harvesting solution may be far ahead in the future, so doing early research is always useful.

5.1 Concluding remarks

While this is a implementation within the ultra low power region, it is still not within the desired constraints of energy harvesting. As of the current state of energy harvesting technology, it is not possible to power this design with power harvested from DSRC transceiver stations. Additional power sources such as solar power and vibration are considered relevant but not implemented at this stage. Using a chargeable battery with a energy harvesting soultion is also a possible improvement to current implementions, batteries are prone to degradation and will always need exchange sooner or later. A change in the current DSRC standard output signals are highly unlikely as they are regulated at international levels.

A 100% energy harvesting solution may be possible in the future, but further improvements in several layers are needed to make this a possibility. However the reduction of power consumption enables longer battery life, which is a welcome improvement in the world of electronics.

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