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Design of a residue amplifier for a SAR-assisted pipeline ADC

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Problem Description

The main task of this thesis is to model and design a residue amplifier for a pipelined SAR in 28 nm FDSOI.

The following sub-tasks should

- Review litterature and find one or more suitable amplifier topology for futher study
- Model a pipeline ADC in Verilog-A to find specifications for the amplifier. The ADC should have the following specifications
  - Accuracy: 13 bit ENOB
  - Sampling rate: 50Ms/s
- Design one or more of the amplifiers

Abstract

This thesis explores the use of the ring amplifier in 28 nm FDSOI. The intended use is as a residue amplifier in a SAR (successive approximation register) assisted pipeline ADC. The specifications for the ADC are 13 effective bits at a sampling rate of 50 MS/s. This thesis is a continuation of Sivert Krøvel's thesis work from 2016, where he used SAR VerilogA-models and an ideal amplifier. This thesis continues to use the SAR-models, but the amplifier is replaced. The ring amplifier is a relatively new amplifier topology that takes advantage of time domain properties to achieve higher speed and energy efficiency than it is possible to reach using traditional operational amplifiers.
This project does not manage to create an amplifier that meets the specifications, due to issues regarding noise and speed. The amplifier along with the ADC models gives 10.3 effective bits at a sampling rate of 10 MS/s.

Sammendrag

Denne masteroppgaven ser på bruk av en ringforsterker i 28nm FDSOI som residu-forsterker i en laveffekts pipeline ADC som bruker suksessiv tilnærmingsregister (SAR). Spesifikasjonen for ADCen var en samplingsrate på 50 MS/s og et effektivt bit-antall på 13. Oppgaven bygger videre på Sivert Krøvels masteroppgave fra 2016, hvor han brukte VerilogA-modeller og en ideel forsterker. I denne oppgaven blir VerilogA-modellene for SAR tatt med videre, mens forsterkeren byttes ut med en ringforsterker. Dette er en relativt ny form for forsterker-topologi som utnytter tids-domenet for å oppnå høyere hastighet og lavere effektforbruk enn det som er mulig med tradisjonelle operasjonsforsterkere. Oppgaven resulterer i en forsterker som ikke lever opp til spesifiksjonene, da man møtte på problemer i forhold til støy og hastighet. Forsterkeren sammen med SAR-modellene gir 10.3 effektive bit ved en samplingsrate på 10 MS/s.

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of Master of Science at the Department for Electronics and Telecommunication (IET) at Norwegian University of Science and Technology (NTNU).
The work was carried out in the period of Oktober 2016 to May 2017, under the supervision of Professor Trond Ytterdal.

Acknowledgements

I would like to thank Trond Ytterdal for his time and patience in supervising this project.

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Abbreviations

ADC	=	Analog to Digital Converter
CMOS	=	Complementary Metal Oxide Semiconductors
DAC	=	Digital to Analog Converter
DNL	=	Differential Non Linearity error
FDSOI	=	Fully Depleted Silicon On Insulator
FFT	=	Fast Fourier Transform
INL	=	Integral Non Linearity error
LVT	=	Low Voltage Threshold
MDAC	=	Multiplying Digital to Analog Converter
OTA	=	Operational Transconductance Amplifier
RVT	=	Regular Voltage Threshold
SAR	=	Successive Approximation Register
SNDR	=	Signal to Noise and Distortion Ratio
SNR	=	Signal to Noise Ratio

Chapter 1

Introduction and motivation

Most of the information in the physical world is analog. The human brain is good at interpreting such information, our senses tell us if a sound is high pitched, loud or muted, we can feel if the weather is warm or cold, process this information and put on appropriate clothes. We do this without thinking much about it, and we do it fast and efficiently. Some information, especially information about something dangerous like touching a hot plate, does not even need to reach the brain in order for the body to respond. For a computer or other digital systems, the process of gathering information from the environment is not that simple. It can only interpret discreet information and needs a translator to be able to do anything useful with it. This is where the ADC (Analog to Digital Converter) comes in. Information like temperature level, light intensity, heart rate, pressure etc. can be measured by analog sensor circuitry as a voltage or current and converted to a digital signal by an ADC.

CMOS process nodes are getting smaller and smaller. This is illustrated by Moore's law, which tells us that transistors sizes are shrinking so fast that every second year the number of transistors in an integrated circuit doubles. Digital circuits have become more energy efficient and faster, but for analog circuits the down-scaling to sub-micron nodes of technology have presented quite a few challenges, and there was a fear that the speed, resolution and energy efficiency of ADCs had reached a saturation point around the turn of the century. But because of many new innovative techniques, these fears have been shown to be mostly unfounded[14].

1.1 Thesis goal

This thesis looks at one of the popular ways to adapt ADCs to scaling, namely using two or more ADCs in a series, a pipeline. Between each stage in such a pipeline there is most often an amplifier that amplifies the residue from the previous stage to be converted by the next stage. The residue amplifier is often considered the limiting factor in the design, so this thesis will focus mainly on this. [1] and [6]

1.2 Main Contributions

This paper describes the design process for a ring amplifier

1.3 Organization of thesis

This thesis is organized in the following manner.

- Chapter 1 introduces the assignment, the motivation behind the assignment and an outline of the goals.
- Chapter 2 gives general and specific background theory for the task. A basic introduction to SARs and pipeline ADCs and residue amplification is given. The ring amplifier is described, and noise and dynamic range in CMOS circuits is briefly looked into.
- Chapter 3 describes the overall system from a high level perspective. The author describes both a previously used fully differential system, and the single ended adaptation of this. Later in this chapter we move on to the design of the amplifier itself, and the choice of components is justified.
- Chapter 4 presents the results of different simulations. Some of the results given are the dynamic range of the amplifier itself and of the whole system, some information about noise and stability performance of the amplifier.
- Chapter 5 discusses and evaluates the results given in chapter 4, and explores different methods for improving the circuit. A road-map for further exploration of the ring amplifier is outlined.
- Chapter 6 gives the final conclusion of the work done.

Chapter 2

Theory and background

2.1 ADC

An analog to digital converter (ADC) takes an analog signal and quantizes it to a digital signal. This can be done in many different ways, but in this project only a SAR-assisted pipeline is considered.

2.1.1 Successive Approximation Register

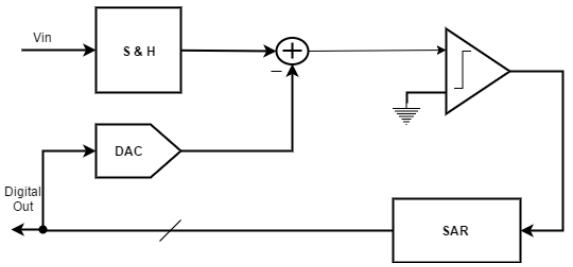

Figure 2.1: Successive approximation register

A successive approximation register (SAR) ADC performs a binary search to convert the analog signal[1]. It resolves one bit at a time, starting with the most significant bit, deciding which half range of the full signal range the input belongs. If it is in the top half, the first bit is set to 1 and for the opposite case it is set to 0. For each successive bit the search range is halved, narrowing the search until the final bit is set. An example block diagram of a SAR circuit is shown in Figure 2.1.

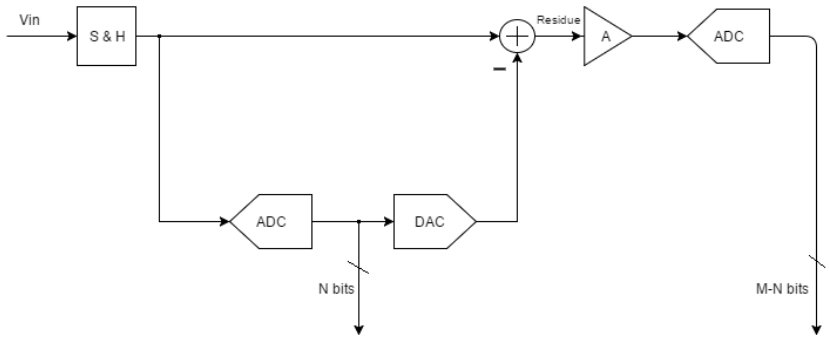

Figure 2.2: Two stage pipeline ADC

2.2 Pipeline ADC

A pipeline ADC places two or more lower resolution ADC in series, together forming a higher resolution ADC. Figure 3.2 shows a two stage pipeline. The sample and hold block takes in a signal that is sent to the first ADC for quantization. The resulting bits are sent to both some kind of control or alignment block (not shown in figure) and to a DAC. The DAC converts the bits back to a voltage level. This voltage is compared to the original sample, and the difference between these is the residue. The residue is amplified and sent to the next ADC for quantization.

2.2.1 Residue Amplifier

The residue is the part of the signal that is unquantized after an ADC stage and is equivalent to the quantization error, $\pm V_{LSB}/2$. In sub-ranging ADC, such as a pipeline ADC, the residue is sent to the next stage to be quantized. In most cases the residue is amplified between stages to relax the resolution requirement for the later stages. It also allows the same reference voltage to be used in both stages. In an N-bit two stage pipeline ADC, where the first (coarse) stage resolves M bits, and the second (fine) stage resolves N-M bits ,the gain of the residue amplifier needs to be 2^M. This can be relaxed through the use of a half-gain multiplying DAC as seen in [10] or through compensation for lower gain through the implementation of some digital correction scheme. The gain can also be lowered by a factor m, if the reference voltage of the second stage is reduced by the same factor.

2.3 Amplifier

Smaller process nodes have brought many benefits to digital circuits, but for analog amplifier circuits scaling can be difficult. Traditional OTAs like the telescopic cascode does

not scale well, consume a lot of power and often require the use of a combination of gain boosting techniques, as short channel lengths also create challenges in generating enough gain. Low supply voltage leaves little headroom for cascoding, and the resulting output swing is low. Still, this type of amplifier is often used at the 65 nm node and above [10, 2]. As scaling favors high speed digital circuits, there is a trend towards looking for new amplifier topologies that take advantage of the time domain [5, 8].

2.3.1 Ring Amplifier

One of the novel methods for residue amplification that take advantage of the time domain is the ring amplifier. It can give almost rail to rail output swing, high gain, has a low component count and is energy efficient. The basic topology is shown in Figure 2.3.

The basis for the ring amplifier is a ring oscillator with three inverters, but where the

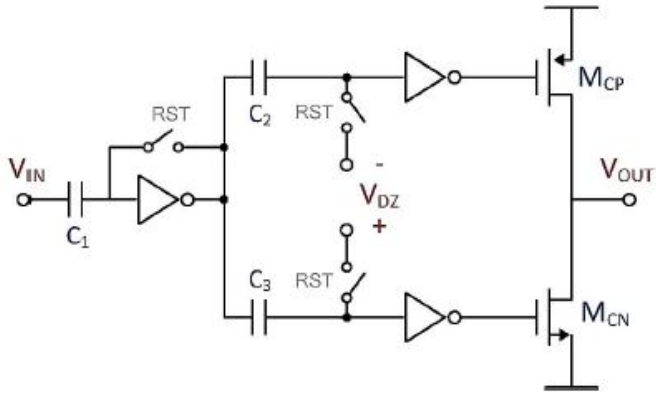

Figure 2.3: Basic ring amplifier, taken from [7]

input signal is split into two different paths to the output[7]. Three inverters in series can result in very high gain, but it has three poles that are close in frequency. Without a dominant pole, the system gets a negative phase margin resulting in an unstable circuit. In a ring oscillator this produces the desired effect, oscillations, but to make a functioning amplifier, a dominant pole has to be created. To do this an offset voltage is applied to the circuit to bias the last stage in the sub-threshold region and thereby increasing the output resistance of this stage substantially. This resistance combined with the output capacitance forms a dominant pole when the circuit is operating in steady state. The two most applied methods for achieving this, are described in the following section.

2.3.2 Ring amplifier topologies

Basic topology

In Figure 2.3, the three inverter oscillator is modified so that the second stage inverter is substituted with two inverters, one to drive the third stage NMOS and one to drive the

third stage PMOS. If no other changes are made, this is still an oscillator. In order to stabilize the amplifier, an offset voltage V_{DZ} is applied. This creates a input voltage range for which neither transistor in the last stage conducts, often referred to as the "dead-zone"[7]. In other words, this voltage is tuned such that the third stage transistors operate in the subthreshold region when input voltage is close to the common mode voltage.

$$V_{G_{p3}} > V_{DD} - |V_{THP}| and V_{G_{3n}} < V_{THN} \tag{2.1}$$

Circuit description:
The capacitor C_1 cancels the difference between the input signal and the trip-point of the first inverter. The other capacitors, C_2 and C_3 stores the voltage offset which is set by external voltage sources when the circuit is in the reset phase.
Time domain behavior:
When the ring amplifier is inserted into a switched capacitor feedback network and satisfies both the above design criteria and stability criteria, it functions in the following manner. There are two non-overlapping phases sample ϕ_s and amplify ϕ_a, where ϕ_s also is used as a reset signal for the amplifier proper. The reset phase auto-zeros the input and output of the amplifier and sets the dead-zone voltage. ϕ_a can be divided into three stages [7], initial ramping, stabilization and steady state. When the amplifier comes out of the reset phase, the output starts slewing towards the target voltage, overshoots the target and starts slewing in the opposite direction. This process repeats itself until it settles at the target. If the dead-zone voltage isn't large enough it may continue the ringing until the next reset phase starts.

Self-biased topology

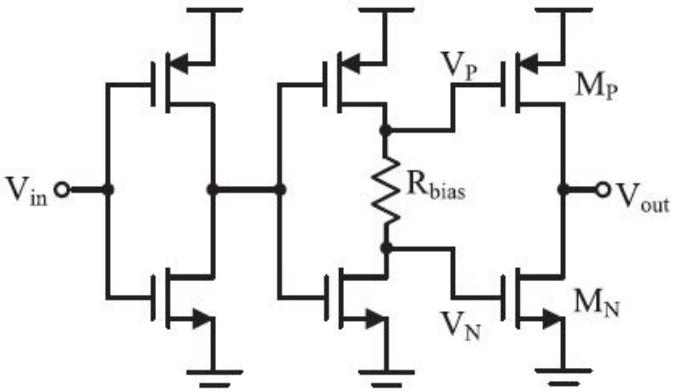

Figure 2.4: Self biased ring amplifier, taken from [13]

In Figure 2.4 a self biased ring amplifier is shown. Several sources [12, 13, 3] describe this topology as preferable over the basic (externally biased) ring amplifier, siting fewer

components and no need for external bias voltages among the reasons.
Instead of using external supplies, this topology sets the dead-zone voltage by inserting a resistor between the gates of the last stage.

2.3.3 Inverter

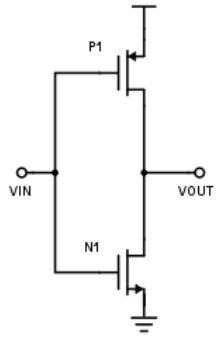

Figure 2.5: Inverter

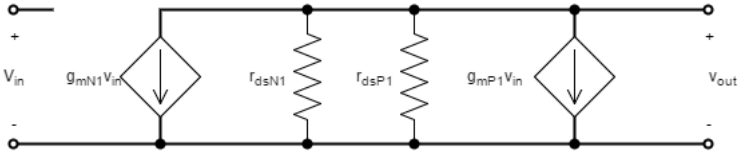

Figure 2.6: Inverter, low frequency, small signal model

Inverters are used in both analog and digital circuits. The ring amplifier's two first stages function as push-pull inverter gain stages. The third stage functions more as a digital inverter where only one of the transistors conduct at a time. In addition, the implementation of an offset between the NMOS and PMOS gate, creates a dead-zone where neither of them conduct. The inverter schematic is shown in Figure 2.5 and a small signal model in Figure 2.6.
The small signal gain of the inverter is given by:

$$A_v = \frac{v_{out}}{v_{in}} = -(g_{mN1} + g_{mP1})(r_{dsN1} || r_{dsP1}) = \frac{-(g_{mN1} + g_{mP1})}{g_{dsN1} + g_{dsP1}} \tag{2.2}$$

2.3.4 Settling time, Gain and Feedback

Feedback in amplifiers can have several different purposes, among them gain reduction, increasing or decreasing input and output impedance and improve linearity. In this project feedback is primarily used for gain reduction. In Figure 2.7 a simple amplifier negative

feedback circuit is shown. Here the capacitors C_1 and C_2 set the feedback factor of the amplifier to $\beta = -\frac{C_2}{C_1}$. The closed loop gain is set by the following equation:

$$A_{CL} = \frac{A}{1 + A\beta}, where A is the open loop gain. \tag{2.3}$$

As long as the loop gain L=Aβ is very large the closed loop gain can be approximated by 1/β.

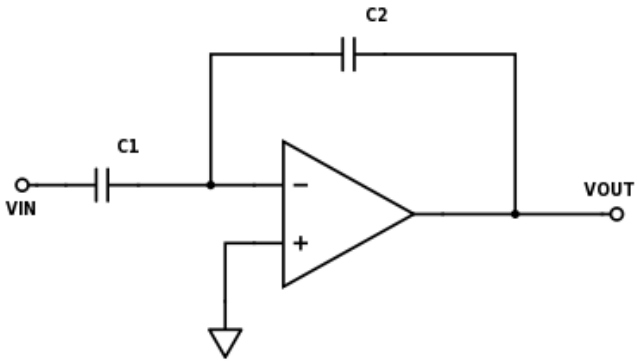

Figure 2.7: Simple feedback

Another important parameter for the residue amplifier is settling time. For a single-pole system with a linear response, the step response can be approximated by[1]:

$$V_{out} = (1 - e^{-\frac{\tau}{t}})V_{step} \tag{2.4}$$

Using this formula it can be found that in order for the amplifier to reach 99.9% of the final value, the settling time needs to be 7τ, for 99% it has to be 4.6τ and for 97% it has to be 3.5τ. It is important to note that this is only a very loose approximation regarding the ring amplifier, as it has more than one pole and instead of having a linear response, it slews towards the target level.

2.4 Noise

Noise is any undesired current or voltage in an electrical circuit. We can divide noise in electronic circuits into two main groups, inherent noise and external noise. The latter is noise introduced by some external circumstance, e.g. electromagnetic interference, coupling etc. from a nearby device. Inherent noise, the noise generated by the circuit components themselves, can be divided into several subcategories. For ADCs there is also quantization noise.

2.4.1 Thermal Noise

Thermal noise, also called Johnson noise is caused by the thermal agitation of the charge carriers in a conductor. It can be modelled as white noise, so it has a flat spectrum. Thermal noise in a resistor can be modelled as a voltage source in series V_{RN} that has a spectral density $V_{RN}^2 = 4kTR$, where k is Boltzmann's constant and T is absolute temperature.

2.4.2 Shot Noise

Shot noise differs from thermal noise in that it is not temperature dependent. It arises from the discrete nature of charges moving unpredictably and is only present if some level of direct current can be found.

2.4.3 Flicker Noise

Flicker noise is also called 1/f noise due to the fact that it is inversely proportional to frequency. This type of noise dominates at low frequencies.
Corner frequency
The frequency where the flicker and thermal noise is the same (the spectrums intersects) is called the corner frequency. This varies significantly between different circuit topologies, transistor types and process nodes.

2.4.4 Quantization noise

An ADC can only quantize the input voltage to the least significant bit, so there will always be an error that ideally is in the range $\pm\frac{V_{LSB}}{2}$. The rms value of the quantization noise is $V_{QN_{rms}} = \frac{V_{LSB}}{\sqrt{12}}$

2.4.5 Dynamic range

Dynamic range is normally expressed in decibel as signal to noise and distortion ratio (SNDR). It is the range between the noise floor and the maximum (full scale) output level. Beyond the full scale signal the ADC input is over-ranged and can't quantize it correctly. In an ideal ADC the lower limit for the signal is $V_{LSB}/2$, a signal lower than this will be lost in the quantization noise. In a non-ideal ADC there will be thermal and other noise that limits the dynamic range.
SNDR is given by equation 2.5

$$SNDR = \frac{P_{signal}}{P_{noise} + P_{distortion}} \tag{2.5}$$

Where P_{noise} includes both quantization and other noise. If there is no distortion (i.e. spurious power from harmonics), SNDR is the same as SNR, the signal to noise ratio.

ENOB or effective number of bits is another measure for dynamic range. The relationship between the two measures is given in equation 2.6 (SNDR in dB).

$$ENOB = \frac{SNDR - 1.763}{6.021} \tag{2.6}$$

If a signal below full scale is used, $-20log(\frac{V_{in}}{V_{fullscale}})$ needs to be added to the SNDR.

2.4.6 Noise in cascaded systems

In a system consisting of several components with either gain or loss in series, it is important to note that the total noise of the system is most affected by the first device in the series.
In an example with a series of three devices, where each one has a gain G and a noise figure F (equation 2.7) , the total noise figure is defined as in equation2.8.

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{2.7}$$

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \tag{2.8}$$

This shows that to combat noise issues it is a good idea to let the first stage in a series have the highest gain.

Chapter 3

Design

The design process began with finding the specifications for the amplifier.

3.1 High level model

Two Verilog-A models were used in the design process. One slightly adapted fully differential SAR-model from a previous thesis [9], seen in Figure 3.1 and a single ended ideal pipeline ADC, seen in Figure 3.2. The ideal model has no separate DAC, as this is inside the first ADC block. The VerilogA code for the ideal model can be found in the appendix A.
A short description of both models follows.

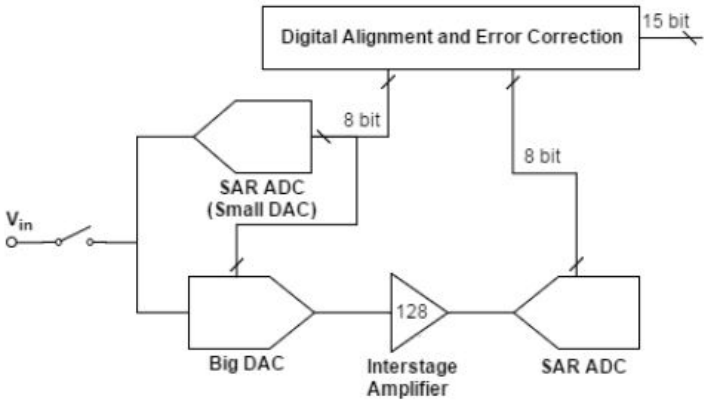

Figure 3.1: Pipeline ADC block diagram

Figure 3.1: Block diagram representation of pipeline SAR model, taken from [9]

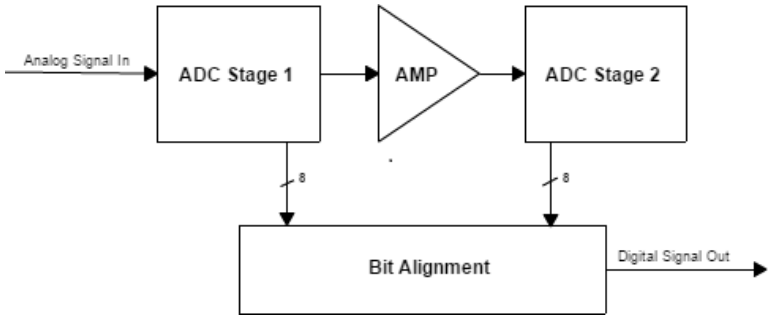

Figure 3.2: Block diagram representation of ideal ADC pipeline model

3.1.1 Single ended ideal pipeline ADC model

The input signal for this model is between 0 and V_{REF}.
Stage1: The signal is quantized to 8 bits by rounding V_{in}/V_{LSB}, where $V_{LSB} = V_{ref}/2^8$ to the nearest integer. The resulting integer is converted to an 8 bit binary number which in turn is sent to the bit alignment block. The residue is the rounding error, and this is sent to stage 2 through the amplifier. A delayed control signal is sent to the alignment block to tell it that the sample is ready.
Stage 2: The amplified rounding error is received. This is quantized to an 8 bit two's complement binary code. Two's complement is used since the residue can be either positive or negative. The result is sent to the bit alignment block. This stage also sends a control signal to the alignment block.
Bit Alignment: This block receives 8 bits from stage 1, and converts them to a base 10 integer. This integer are multiplied by 2^7, equivalent to a bit-shift seven places to the left. When the two's complement number from stage 2 comes in, it is converted to a number between -128 and 127 and added to the stage 1 number. The result is multiplied by $V_{ref}/2^{15}$ and sent to the output.

3.1.2 Differential Pipeline SAR Model

Stage 1 and 2 SAR: These stages are near identical, except for in timing. Both use binary search to quantize the input signal and both send a signal to the alignment block when the sample is ready.
DAC: This stage receives 8 bits from stage 1 and subtracts this from the input signal. The result is the residue and is sent to amplification.
Alignment block: This block does the same as in the single ended model.

3.2 Amplifier

Looking at both the self-biased and the externally biased ring amplifier, and after an exploratory look into both topologies with simulations, it was decided to proceed with the

former. The self biased amplifier uses a resistor to set the offset voltage, thus avoiding the need for external voltage sources. The self-biased amplifier also removes the need for offset capacitors and reduces number of transistors in the second stage from 4 to 2, since it is no longer split. This reduces the load on the first stage and thereby the power consumption [12] .
Being a relatively new and rare amplifier topology, no established design methodology exists. Although regular OTA design is a good a starting point, the highly co-dependent relationship between the different operational domains (AC, DC, transient) makes the ring amplifier design more demanding[7].
As stated in [11], one cannot rely on the ring amplifier to be stable even with a high positive phase margin at the desired operating point. This is because the current in last stage of the amplifier changes drastically around the settling point. Because of this it is important to look at the transient response right from the start of the design process. In Figure 3.3 an example transient response of a ring amplifier with a 78° phase margin in the amplification phase is shown to illustrate this issue. There is significant overshoot. A worse example can be seen in [12], where the amplifier oscillates with a 73° phase margin.

3.2.1 Gain and feedback

Both models resolve 8 bits in each stage and both have one bit redundancy, but in opposite stages. Using the same reference voltage, in both stages, the amplifier needs to have a closed loop gain of $2^8 = 256$. This would result in a feedback-factor $\beta = -\frac{1}{256}$. A low feedback factor negatively affects speed [1]. It is possible to lower the closed loop gain to 2^{8-1}, and thereby increasing β by for example using a half gain MDAC as in [10] or by letting digital correction resolve this. The latter also has the advantage that one can avoid any out-of-range residue [15, p. 162]. The gain error of the amplifier can be approximated by $\frac{1}{A_0\beta}$, so to keep this less than $V_{LSB}/2$ in the later stage, the open loop gain can be calculated by using equation 3.1[15, p.171].

$$A_0\beta > 2^{M-N} \tag{3.1}$$

With M=15 (total bits), N=8 (bits resolved in the last stage), $A_0 = 2^{14} = 84.3dB$

The self-biased ring amplifier is inserted into a feedback an auto-zero network with ideal switches as seen in appendix B.

3.2.2 Settling Time

With a 50MS/s conversion frequency, a new sample has to be ready every 1/50MHz = 20 ns. The SAR-ADC is relatively fast, so as a preliminary assumption can be that the amplifier can use about 60-70% of the the period for amplification (provided the remaining time is enough to charge the sampling capacitor). As the reset phase for the amplifier is the same as the sample period for both the SARs and the amplifier, this is most likely doable. That gives the amplifier about 13 ns to have the amplified residue ready for sampling by stage 2. As the ring amplifier is a slew based amplifier, it needs to have a slew rate of at

least $\frac{0.5V}{13ns} = 38.5MV/s$

Resistor sizing

The resistor is chosen based several factors. The current through it, to ensure that the IR drop is large enough to create a sufficient input-referred dead-zone. The resistor is also paramount in stabilizing the circuit and its size helps regulate the phase margin. The size of the transistor also relates to the total gain and the bandwidth of the amplifier, both decreases as R_{BIAS} increases.

Capacitor sizing

The input, sampling and feedback capacitors sizes are somewhat unknown quantities, as they need to be set in accordance with the actual SAR implementations. As long as the feedback networks switches are ideal, and the sampling capacitor (for stage 2, which is also the load of the amplifier) is large enough to not accumulate KT/C noise larger than the quantization noise they can be set to somewhat arbitrary values. Therefore the capacitor values were set depending on what worked in simulation. When the feedback network is implemented with actual transistor switches, and the unity capacitance size of the SARs DAC is known, the sizing becomes very important.

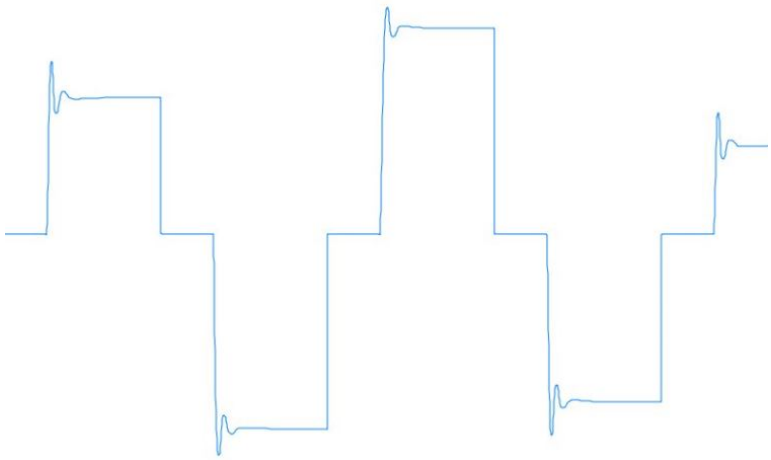

Figure 3.3: Overshoot example, 78° phase margin

Transistor sizing

The ordinary square law mosfet equations for g_m, g_{ds} and current does not hold up for the 28 nm FDSOI process, even though the trends are the same. Therefore the first task in the

design was to create some characteristics plots in Cadence. These were used to help find the sizes of the transistors.
The inverters were chosen so that they would have a total gain of 100-110 dB or more, to have some margin above the 84.3 dB spec. Some gain will also be lost because of the resistor between the second and third stage. The inverters were also adjusted such that they would have a trip-point close to VDD/2
Low threshold voltage transistor (LVT) were used in stage 1 and 2. In stage 3 regular threshold voltage transistors (RVT) were used, as suggested in [12] and [11]. The RVT devices gives the third stage a higher output resistance, which helps to form the dominant pole in the amplification phase. Looking at equation 3.2 which shows the overdrive voltage for the third stage nmos, it is also clear that doing this also extend the voltage range for sub-threshold operation.

$$V_{OV} = V_{GS} - V_{TH} \tag{3.2}$$
$$V_{OV} = \frac{V_{DD}}{2} - \frac{V_{DZ}}{2} - V_{TH}$$

Before choosing to go with RVT in the output stage, it was also attempted to regulate the threshold voltage by changing the bulk (or "back-gate" in FDSOI) voltage. This gave some improvements, but in the end the RVT approach gave better results.

Bandwidth:

The bandwidth of the amplifier is primarily set by the width of the transistors. Increasing width in stage 1 and 3 gives greater bandwidth, but decreases the phase margin and the gain. It also increases the power consumption.

Deadzone:

As mentioned above the dead-zone voltage needs to be large enough to be valid for all input signals. For the self-biased ring amplifier this means that is has to be approximately:

$$V_{DZ} > V_{in_{max}} \cdot \overline{A_1} \cdot \overline{A_2} \tag{3.3}$$

Where $\overline{A_1}$ and $\overline{A_2}$ is the average closed loop gain in the amplification phase of stage 1 and 2 respectively.
The dead-zone voltage is set by $V_{DZ} = i_{d2}R_{BIAS}$, so it is also regulated by the current through stage two in addition the biasing resistor. This means that the width of stage 2 has a linear relationship to the magnitude of the dead-zone voltage.

Slewing and settling

The width of stage 3 is also important in respect to slewing. Since the ring amplifier uses slew based charging, the available current here decides the slew rate. There is a difficult balancing act here, as a high slew rate is needed to charge the load fast enough, but it can't be to high as this causes significant overshoot, potential for ringing and gives long settling time.

Gain

The lengths of the transistors is the deciding factor when it comes to gain. According to noise theory the largest gain should be at the first stage of the amplifier, but unlike most multi-stage amplifiers the ring amplifier relies on a dominant pole being created at the last stage in the amplification phase. This creates some challenges in terms of which stage

should have the longest transistors.

3.2.3 Feedback and reset

The switched capacitor feedback and reset scheme was implemented as shown in Figure 3.4 as suggested in several sources like[7, 12]. The switches used in the network are ideal. there are two non-overlapping clock signals used, amplify (NRST in schematic) and sample (RST in schematic). Two loops can be seen in the circuit, but only the outer loop is closed in the amplification phase. β is set by $\frac{C_{fb}}{C_s}$ in this phase.
In the reset/sample phase the input and output of the amplifier is reset to $V_{CM} = \frac{V_{DD}}{2}$, effectively auto-zeroing the circuit. The feedback and input capacitors (C_{fb}, C_{in}) are reset too, common mode voltage being applied to both the plates of these. The left plate of the sampling capacitor C_s is being charged by the input voltage. Entering the amplify phase this charge is transferred to the input capacitor and the resulting voltage is amplified. The sampling capacitor is reset in the amplification phase.

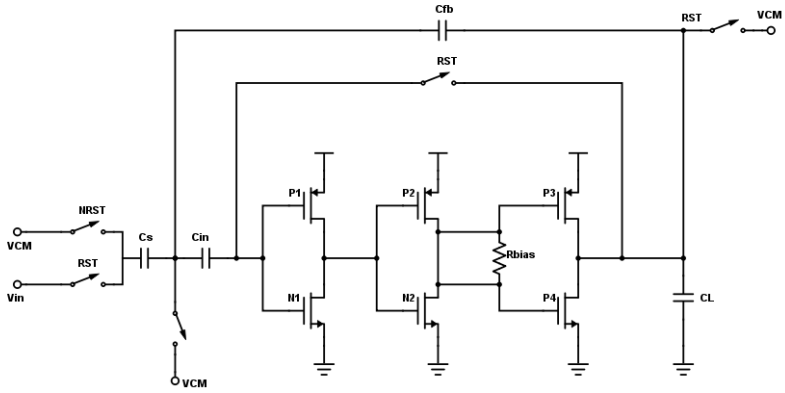

Figure 3.4: Feedback and reset network. The RST phase is also the sampling phase, while the NRST phase would also be called the amplify phase

Chapter 4

Simulations and Results

The circuit schematics were made in Cadence Virtuoso and the simulations were run in ADEXL.

The simulations that were done for the amplifier were:

- AC analysis with open loop circuit, to find the open loop gain A_0 and the uniity gain frequency f_{ug}.
- AC analysis with closed loop circuit, to confirm the closed loop gain A_{CL}.
- STB analysis to find the phase margin PM and the loop gain.
- Transient analysis with and without noise for signal to noise ratio SNR.
- Noise analysis in the frequency domain to find the integrated noise.

The testbenches can be found in appendix B.
In addition, the calculator was used to find the gain bandwidth product. Power was found using two methods, looking at the power consumption in at the dc operating point and through averaging P=UI at the main voltage source in the transient analysis. In most cases the two methods were in accordance.

The amplifier circuit was inserted into a basic switched capacitor feedback system with ideal switches. Different test-benches were made for open loop, closed loop and transient analysis. In the open loop scenarios a duplicate of the whole circuit was used to compensate for the load difference. To confirm that the load size is correct, the unity gain frequencies for open and closed loop were compared. Also to confirm this for the stb analysis, the unity gain frequency for closed loop was compared whith the frequency where the loop gain plot crossed $20log(\beta)$. All three frequencies closely matched, so the loading can be assumed to be correct.

4.1 Stability, Gain and Bandwidth

Stability analysis were only done for the amplify phase, because the feedback network was created using ideal switches. During the sample phase the circuit was reset/auto-zeroed back to the desired mid-point voltage and thereby always stable. In an actual implementation of the amplifier the stability in this phase would be important. The results for the component sizes given in Table 4.1 are seen in Table 4.2. The deadzone voltage of the amplifier was measured to 12.2 mV, which is not large enough for the full scale input signal.

Component	**Size**	**Component**	**Size**
Stage 1 NMOS	$\frac{384nm}{60nm}$	Sampling Capacitor	1280 fF
Stage 1 PMOS	$\frac{1222nm}{60nm}$	Input Capacitor	200 fF
Stage 2 NMOS	$\frac{200nm}{45nm}$	Feedback Capacitor	10 fF
Stage 2 PMOS	$\frac{568nm}{45nm}$	R_{BIAS}	1 kΩ
Stage 3 NMOS	$\frac{100nm}{100nm}$	Load capacitor	400 fF
Stage 3 PMOS	$\frac{270nm}{100nm}$		

Table 4.1: Typical component sizes

Open loop gain A_0	91.94 dB
Phase margin PM	71.28° @ 73.34MHz
Unity gain frequency f_{ug}	1.51 GHz
Power consumption	28.38 uW

Table 4.2: Results for typical component values

4.2 Noise

Signal level	**Without noise**	**Thermal noise**	**Thermal and Flicker noise**
0 dBFS	47.8 dB	29.9 dB	26.2 dB
-12.04 dBFS	83.3 dB	29.9 dB	26.3 dB

Table 4.3: SNR results.
From FFT using rectangular window, f_{in} = 1.005859375MHz sampled at 10MHz

Using the noise analysis in ADEXL, looking at both the noise summary and the output noise plot, flicker noise dominates up to the corner frequency, which was found to be 160 MHz.

The input referred integrated noise (1kHz- 15GHz) was $608.5nV^2$ and the total summarized noise was $1.43mV^2$. According to the noise summary the flicker noise in the first stage is the greatest contributor to the total noise, accounting for 76%. The second highest contributor was stage 1 thermal noise with 16% of the total.
Signal to noise results are listed in Table 4.3. The sampling frequency had to be lowered to 10 MHz as the amplifiers slew rate was to low to accommodate 50 MHz.

4.2.1 Attempted solutions

To improve the speed of the amplifier, the slew rate has to go up and the settling time has to be lowered, both of which can be improved by widening the output transistors. This gives the amplifier higher bandwidth, whilst at the same time increasing the available current. To improve the noise problems, the input transistors can be lengthened to place the majority of the gain there.
Trying to make both these improvements simultaneously easily creates instability.
These attempts were abandoned in favor of making an alternative amplifier with lower closed loop gain.

Alternative amplifier solution
As an alternative to implementing the pipeline ADC as two 7-8 bit stages, a solution for use in a three stage pipeline was attempted. This alternative should be better able to deal with the short settling time allowance and the noise problem. The most important changes are:

- Change the pipeline to three 5 bit stages.
- β is reduced to $\frac{1}{2^4} = 1/16$ (assuming a half gain MDAC as in [10]). The open loop gain should still be above 84.3 dB, as the total number of bits is still 15.
- The maximum input signal in this case has an amplitude of $\frac{1}{2^5}V$,so either the resistor needs to be larger or stage 2 needs be wider to have a dead-zone that can accommodate this.
- To combat the noise problem, the largest gain is implemented in stage 1. To allow this, the widths of amplifier stage 1 and 3 needs to be much wider to avoid bandwidth and stability issues.

The new component sizes are listed in Table4.4 and the results for stability and bandwidth are listed in Table 4.5. The dead-zone voltage for this amplifier was 150 mV, which is a little to small for the full scale input signal.

Noise in alternative amplifier:
The integrated noise in the new amplifier was significantly less than for the original; Total input referred integrated noise (1kHz-15GHz) was $112nV^2$ and total summarized noise was $4.83uV^2$. The corner frequency for the flicker noise was reduced to 30 MHz.
The greatest contributors to the integrated noise was shot noise in stage 1, coming in at 66% of the total. Flicker and thermal noise in stage 1 contributed 15 % each. The signal to

Component	Size	Component	Size
Stage 1 NMOS	$\frac{12*384nm}{120nm}$	Sampling Capacitor	320 fF
Stage 1 PMOS	$\frac{12*1162nm}{10nm}$	Input Capacitor	200 fF
Stage 2 NMOS	$\frac{200nm}{45nm}$	Feedback Capacitor	20 fF
Stage 2 PMOS	$\frac{560nm}{45nm}$	R_{BIAS}	12 kΩ
Stage 3 NMOS	$\frac{2*100nm}{100nm}$	Load capacitor	400 fF
Stage 3 PMOS	$\frac{2*270nm}{100nm}$		

Table 4.4: Alternative component sizes for higher β

Open loop gain A_0	86.6 dB
Phase margin PM	73.7° @ 162.6MHz
Unity gain frequency Closed Loop f_{ug}	1.38 GHz
Power consumption	76.1 uW

Table 4.5: Results for alternative component values

noise ratio was significantly better, also at 50MHz sampling frequency and with inherent noise enabled. The SNR results can be seen in Table 4.6

Signal level	Without noise	Thermal noise	Thermal and Flicker noise
0 dBFS	79.5 dB	37.6 dB	36.2 dB
-12.04 dBFS	85.6 dB	37.8 dB	36.5 dB

Table 4.6: SNR results for alternative components.
From FFT using rectangular window, f_{in} = 21.04492188MHZ sampled at 50MHz. Full scale is set to be a little lower than $1/2^5$, as the output swing is not fully rail to rail

4.3 Step response

A comparison of the step response for the two amplifier alternatives is shown in Figures 4.1 and 4.2. The large step is a full scale pulse and the small step is about -20 dBFS.

4.4 System Model with original components

The full system was first simulated with an ideal amplifier and the differential Verilog model. The input signal is a $2V_{pk-pk}$ sine wave at 1.005859375MHz and f_s=10MHz. These results match up fairly well to the theory. With an open loop gain of 18000 = 85.1 dB, the effective number of bits were 13.6.

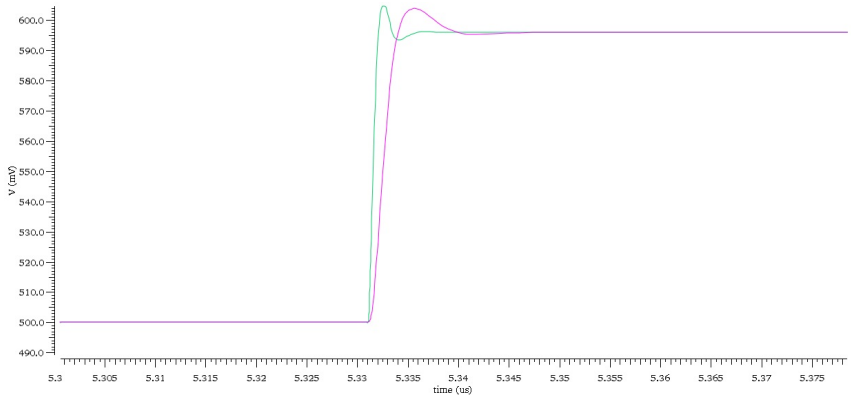

Figure 4.1: Overshoot, small step response. Original components in pink, alternative in green

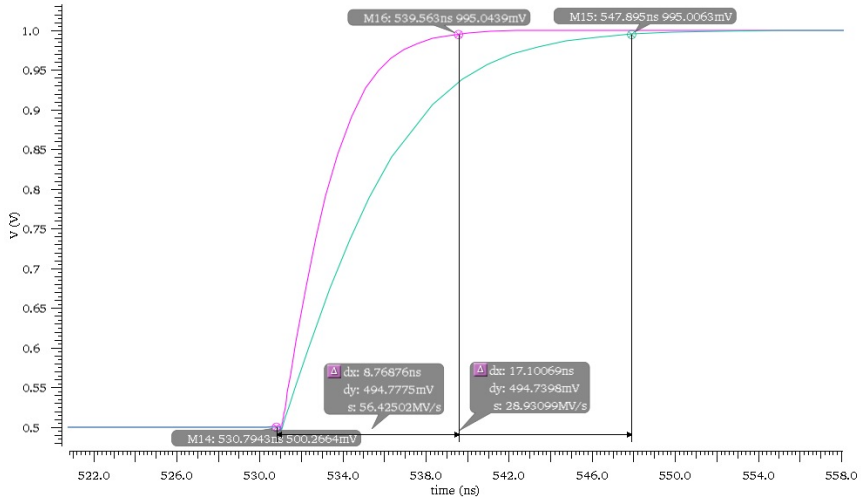

Figure 4.2: Comparison, large step response. Original components in green, alternative in pink

With the help of some ideal baluns and offset voltage sources, the ideal amplifier was replaced by the ring amplifier in the differential model. Without noise this gave an SNR of 81.87dB or 13.31 effective bits, the FFT is shown in Figure 4.3. After turning on thermal noise in the transistor models (FFT in Figure 4.4) this was reduced to 71.25dB or 11.54 effective bits. Fmax for the noise was set to 3 times f_{ug}. Lastly the inherent flicker noise was added to the model, further reducing the SNR to 63.63 dB or 10.28 effective bits.

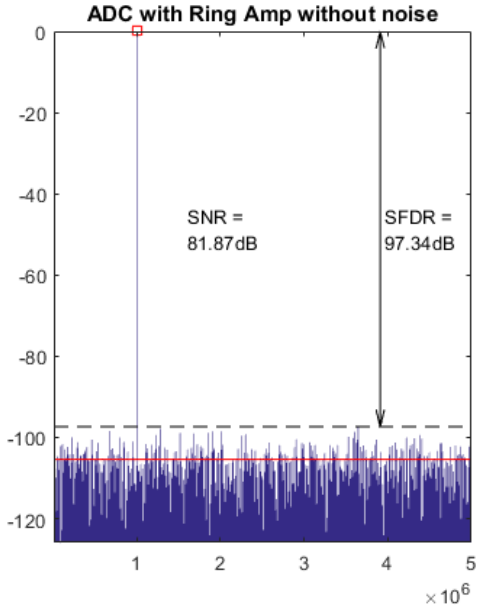

Figure 4.3: FFT of ADC with ring amplifier

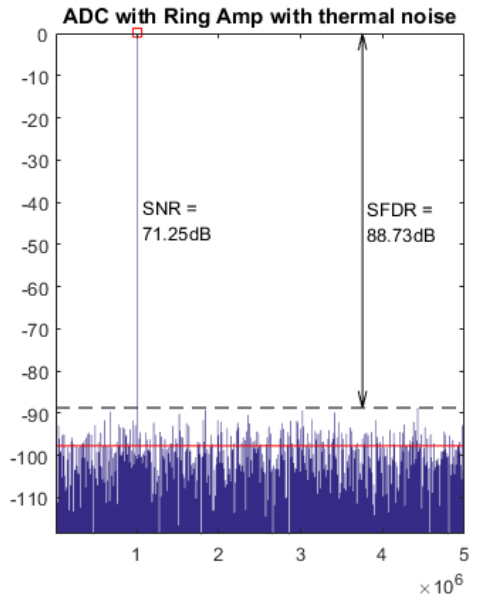

Figure 4.4: Thermal noise added in models

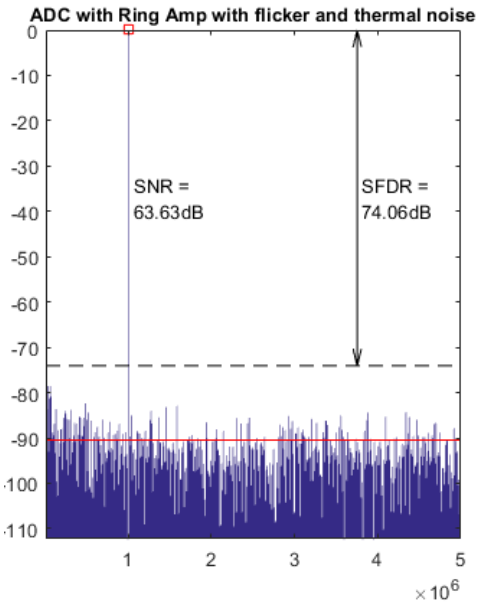

Figure 4.5: Both thermal and flicker noise added

Chapter 5

Discussion

The ADC models worked the way they were supposed to. There are several unsolved issues with the amplifier design.
The main problems in designing the ring amplifier was as follows

- Creating a large enough dead-zone while maintaining high bandwidth and gain.
- Lowering the noise without using large input transistors.
- Avoiding large over-shoot and tendency towards ringing when amplifying small input signals, while keeping a short settling time for larger input signals.

5.1 Original Amplifier

The original amplifier is plagued with two main issues. Lack of speed and severe noise. The noise comes primarily from two factors:

- It operates well below the flicker noise corner frequency.
- The highest gain is at the last stage, creating thermal noise issues.

The decision to reduce the sampling frequency to 10 MHz came after realizing that even though the amplifier seemed to be fast enough while using a 1 mV input signal, it could not handle larger signals because it:

- Was not allowed any overshoot at the small test signal, therefore could not reach output fast enough at larger test signals.
- Had a severely under-scaled dead-zone voltage, thus even if it had been able to reach target, the gain could very well have been incorrect.

5.2 Alternative amplifier

The alternative amplifier shows that the noise problem is reduced by increasing the size of transistors significantly, especially in the first stage. The larger total size decreases the flicker noise, the higher gain also reduces noise. But even with these improvements, the noise problem is still present. The alternative amplifier lowered the closed loop gain with by a factor of 8, tripled the power consumption and greatly increased the silicon area, but still only improved the SNR with flicker and thermal noise turned on by 10dB. The dead-zone of this amplifier is only a few mV to small and a significant SNR improvement is seen at the full scale signal without noise.

5.3 System model

The full system model with noise ac hives 10.3 effective bits. Although not a good result, it is a bit better than feared from looking at the amplifier's dynamic range. This may be explained by the difference in input signal. The stand alone tests of the amplifier used a sine wave which was sampled at the input switch and capacitor, while the signal coming from stage one of the ADC was not sinusoidal in form and already "sampled" by the Verilog model. If the amplifier in its present form was implemented in a pipeline ADC with real components, the SNR would most likely plummet.

5.4 Summary

Trying to design a ring amplifier was challenging. It took a lot of time to even understand the principle behind its operation. The initial approach of treating it as any other operational amplifier was doomed to fail. One of the more important realizations was that overshoot and some tendency towards ringing, as seen in the example in Figure 3.3 is an inherent behavior of the ring amplifier. A lot of time was spent trying to combat this, instead of working with it. If one does not allow the amplifier to behave this way at low input signals, it will not be fast enough to even reach the target output at higher input signals. Many roads were not taken due to this, some of which could may well have led to a working, fast enough result. Another realization was that having a large enough dead-zone voltage range is not somewhat important, it is paramount to the design and should be prioritized. Again, as can be seen in the "noise-less" SNR results for both the original and the alternative implementation, they fall off quite significantly when a full-scale or close to full scale signal is amplified. This is likely due the dead-zone being to narrow and the highest samples not being amplified correctly. An INL/DNL test should be performed to confirm whether the dead-zone voltage is directly related to this as a lack of linearity.

5.5 Future work

If the implementation had been successful, the next steps would have been:

- Replace the ideal switches in the feedback network with transistors and evaluate stability in the sample/reset phase. The results of this may further complicate the design, as it can be expected that ringing around the common mode voltage easily could occur at the beginning of this phase. The opposite could also happen, being unable to reach the common mode voltage at all within the time limit if the switches and capacitors are not correctly sized.
- Evaluate whether to use a pseudo-differential or fully differential approach, and implement this.
- Extract parasitics and create the layout of the amplifier.
- Replace the VerilogA models with actual SAR stages.

As the amplifier stands now, it would be a good idea to explore some of the following to combat the noise and speed issues:

Re-evaluate specifications:
Consider reducing the number of bits at the first stage, or adding another stage to the pipeline to increase β, relaxing the demands on the amplifier. The preliminary results for the alternative amplifier suggests that this is possible to do without having to increase the power budget too severely.

Chopper stabilization:
This technique could be used to reduce or remove the effects of flicker noise. Chopper stabilization is done by essentially modulating the signal to a higher frequency where no such noise is present, and demodulating it again after amplification. An implementation of this approach in ring amplifier design can be found in [16].

Improved auto-zero:
The resetting of the amplifier input and output in this thesis is an unsophisticated form of auto-zero. Other techniques may improve the noise results. In [12] an improved auto-zero method is employed to decrease noise and at the same time help reduce gain error.

Amplifiers working in parallel:
If a conclusion is reached, that it is not possible to meet the specifications using a single ring amplifier, it may be possible to use two or more in parallel, for example using the fine/coarse approach suggested in [4] or combining the ring amplifier with a telescopic cascode to get the best from both worlds as in [7]

Chapter 6

Conclusion

The ring-amplifier designed in this thesis does not meet the requirements for use in a 50 Ms/s 13 bit ENOB pipeline ADC. By lowering the sampling frequency to 10 MHz, an ENOB of 10.28 bits was achieved. The amplifier had severe noise problems, which Further work is required to solve issues when it comes to noise and speed.
The temptation to treat the ring amplifier design the same as one would treat the design of a regular operational amplifier should be resisted. Being based off of an actual oscillator makes the ring amplifier prone to instability. And whilst being in it basic form a seemingly simple design, with few components, the combination of slew based charging, having the dominant pole at the last stage and the importance of having a large enough dead-zone voltage makes the design challenging to say the least.
If the amplifier is to be further explored in a future project, it may be prudent to reevaluate the specifications and consider either lower sampling speed or increasing the feedback factor. Using either a three stage 5+5+5 bit pipeline or decreasing the number of bits in the first stage of a two stage pipeline could be beneficial.

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Appendix

A: Verilog Code

```
// VerilogA for ua_adc, ALIGN_CTRL, veriloga
`include "constants.vams"
`include "disciplines.vams"
/*MSB er B15, LSB er B0. B15 er BIT7 fra trinn1, B7 er BIT7 fra trinn2*/
//todo bytt ut med to busser
module ALIGN_CTRL(B15,B14,B13,B12,B11,B10,B9,B8,B7,B6,B5,B4,B3,B2,B1,B0, DIGOUT, CTRL1,
CTRL2, VREF);
input B15,B14,B13,B12,B11,B10,B9,B8,B7,B6,B5,B4,B3,B2,B1,B0,CTRL1, CTRL2, VREF;
output DIGOUT;
electrical B15,B14,B13,B12,B11,B10,B9,B8,B7,B6,B5,B4,B3,B2,B1,B0, DIGOUT, CTRL1, CTRL2, VREF;
parameter real vth = 0.5;
parameter real tdel = 0;
parameter real trf = 10p;
integer d1,d2,d_hold;
genvar i;
real vlsb15;
real dv;
integer dout;
integer bin1[7:0];
integer bin2[7:0];
analog begin
        vlsb15 = 1/pow(2,15);
@(initial_step)begin
        vlsb15 = V(VREF)/2**15;
        d1 = 0;
        d2 = 0;
        d_hold = 0;
end//initial

@(cross(V(CTRL1)  - vth, 1)) begin
        d1 = 0;
        bin1[7]=V(B15);
        bin1[6]=V(B14);
        bin1[5]=V(B13);
        bin1[4]=V(B12);
        bin1[3]=V(B11);
        bin1[2]=V(B10);
        bin1[1]=V(B9);
        bin1[0]=V(B8);
        $strobe("%m:ALIGN:At simulation time %g \n
        bin1[7]= %d \n
        bin1[6]= %d \n
        bin1[5]= %d \n
        bin1[4]= %d \n
        bin1[3]= %d \n
        bin1[2]= %d \n
        bin1[1]= %d \n
        bin1[0]= %d", $realtime, bin1[7], bin1[6],     bin1[5], bin1[4], bin1[3], bin1[2], bin1[1], bin1[0] );


        for (i = 14; i>=7; i = i - 1) begin

                if(bin1[i-7]>vth) begin
                        d1 = d1+2**i;
                end//if

        end//for
        $strobe("%m:ALIGN:At simulation time %g d1 is %d", $realtime, d1 );
```

```
end//@cross ctrl1
@(cross(V(CTRL1)  - vth, -1)) begin
                d_hold = d1;
                d2 = 0;
end
@(cross(V(CTRL2)  - vth, -1)) begin

                $strobe("%m:ALIGN:At simulation time %g d_hold is %d", $realtime, d_hold );
                bin2[7]=V(B7);
                bin2[6]=V(B6);
                bin2[5]=V(B5);
                bin2[4]=V(B4);
                bin2[3]=V(B3);
                bin2[2]=V(B2);
                bin2[1]=V(B1);
                bin2[0]=V(B0);

                $strobe("%m:ALIGN:At simulation time %g \n
                bin2[7]= %d \n
                bin2[6]= %d \n
                bin2[5]= %d \n
                bin2[4]= %d \n
                bin2[3]= %d \n
                bin2[2]= %d \n
                bin2[1]= %d \n
                bin2[0]= %d", $realtime, bin2[7], bin2[6],     bin2[5], bin2[4], bin2[3], bin2[2], bin2[1], bin2[0] );
                for (i = 7; i>=0; i = i - 1) begin

                                if(bin2[i]>vth) begin
                                                d2 = d2+2**i;
                                end//if

                end//for
                if(d2 > (2**7) -1) begin
                                d2 = (2**8 -d2)*(-1);
                end//if
   dout = (d_hold+d2);
                dv =dout*vlsb15;
                $strobe("%m:ALIGN:At simulation time %g d2 is %d and total is %d, making out %g (also d1 is
%d)", $realtime, d2, dout,dv, d1 );
end//@cross ctrl2
V(DIGOUT) <+ dv;
end //analog
endmodule
```

```
// VerilogA for ua_adc, se_8b_adc_stage1, veriloga
`include "constants.vams"
`include "disciplines.vams"

module se_8b_adc_stage1(CLK, VIN, TEST, CTRL, RES, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5, BIT6, BIT7,
VREF);

input CLK, VIN, VREF;
output RES, TEST, CTRL, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5, BIT6, BIT7;
electrical /*[7:0]BITS1,*/ RES, TEST, CTRL, CLK, VIN, VREF, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5, BIT6, BIT7;

parameter real vth = 0.5;
parameter real tdel = 0;
parameter real trf = 10p;

integer bout[7:0];
integer Qnmbr;
integer rdes15;
integer tmp;
integer ctrl;
real dec8, dec15;
real vin;
real vlsb8;
real vlsb15;
real ctrl_delay;
real resi, resv, resn, resp;
genvar i;

analog begin

@(initial_step)begin
                vlsb8 = V(VREF)/2**8;
                vlsb15 = V(VREF)/2**15;
                resp = 0;
                resn = 0;
   resi =0;
   resv = 0;
                $strobe("%m:STAGE1:At simulation time %g vlsb8 is %g and vlsb15 is %g", $realtime, vlsb8,
vlsb15 );
end

@(cross(V(CLK) - vth,1)) begin

                ctrl = 0;
                /*If CTRl1 ia used to control the next stage then ctrl_delay decides when the next stage will
sample the amplified residue,
                this number must be adjusted according to sampling frequency and settling times.
                 If T_s=100n, this may need to be as high as 99n to make sure the amplifier output is settled
                before.  */
                ctrl_delay = 97n;
                vin = V(VIN);
                Qnmbr = 0;
//              dec8 = (vin+1)/(vlsb8);
//              dec16 = (vin+1)/(vlsb16);
                dec8 = (vin)/(vlsb8);
                dec15 = (vin)/(vlsb15);
                rdes15 =dec15;
```

```
		$strobe("%m:STAGE1:At simulation time %g vin is %g, dec8 is %g and dec15 is %g (so next
out should be %d,%g)", $realtime, vin, dec8, dec15,rdes15,rdes15*vlsb15);
		if ((ceil(dec8) - dec8) < 0.5 ) begin
				Qnmbr = ceil( dec8 );
				resi = dec8 - ceil(dec8);
				resv = resi*(2*vlsb8);
		end //if
		else if (ceil(dec8)- dec8 >= 0.5) begin
				Qnmbr = floor(dec8);
				resi = dec8 - floor(dec8);
				resv = resi*2*vlsb8;

		end//else if
		else $strobe("%m:STAGE1:Error in (if else), input not valid");

		$strobe("%m:STAGE1:At simulation time %g Qnmbr is %d, or %b, resi is %g and resv is %g.\n
		Qnmbr<<7 is %d , making the residue-number(dec15-Qnmb<<7) %g .",$realtime, Qnmbr,
Qnmbr, resi, resv, (Qnmbr*(2**7)),(dec15-(Qnmbr*(2**7))));
		tmp = Qnmbr;
		for (i = 7; i>=0; i = i - 1) begin
				if (tmp >= 2**i ) begin
						bout[i] = 1;
						tmp = tmp - 2**i;
				end//if
				else bout[i] = 0;
		end//for
		$strobe("%m:STAGE1:At simulation time %g \n
		bout[7]= %d \n
		bout[6]= %d \n
		bout[5]= %d \n
		bout[4]= %d \n
		bout[3]= %d \n
		bout[2]= %d \n
		bout[1]= %d \n
		bout[0]= %d", $realtime, bout[7], bout[6], bout[5], bout[4], bout[3], bout[2], bout[1], bout[0] );

end//@cross CLK 1
@(cross(V(CLK) - vth, -1)) begin
		ctrl = 1;
		ctrl_delay = 55n;
end //@cross CLK -1
		V(RES) <+ resv+0.5;

    V(CTRL) <+ transition(ctrl, ctrl_delay, trf);
		V(TEST) <+ transition((Qnmbr*vlsb8 - 1), trf,trf,trf);
		V(BIT0) <+ bout[0];
		V(BIT1) <+ bout[1];
		V(BIT2) <+ bout[2];
		V(BIT3) <+ bout[3];
		V(BIT4) <+ bout[4];
		V(BIT5) <+ bout[5];
		V(BIT6) <+ bout[6];
		V(BIT7) <+ bout[7];
end//analog
endmodule
```

```
// VerilogA for ua_adc, se_8b_adc_stage2, veriloga
`include "constants.vams"
`include "disciplines.vams"

module se_8b_adc_stage2(CLK, VIN, TEST, CTRL, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5, BIT6, BIT7, VREF);

input CLK, VIN, VREF;
output TEST, CTRL, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5, BIT6, BIT7;
electrical /*[7:0]BITS1,*/  TEST, CTRL, CLK, VIN, VREF, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5, BIT6, BIT7;

parameter real vth = 0.5;
parameter real tdel = 0;
parameter real trf = 10p;

integer bout[7:0];
integer Qnmbr;
integer tmp;
integer ctrl;
integer dec8, dec7;
real vin;
real vlsb7;
real vlsb8;
real vlsb16;
real ctrl_delay;
genvar i;

analog begin

@(initial_step)begin
                vlsb7 = V(VREF)/2**7;
                vlsb8 = V(VREF)/2**8;
end

@(cross(V(CLK) - vth,-1)) begin

                ctrl = 1;
                ctrl_delay = 2n;
                vin = (V(VIN)-0.5)/*(-1)*/;
                Qnmbr = 0;
//              dec8 = (vin+1)/(vlsb8);
//              dec16 = (vin+1)/(vlsb16);
                dec8 = (vin)/(vlsb8);
                dec7 = (vin)/(vlsb7);

                $strobe("%m:STAGE2:At simulation time %g vin is %g, dec7 is %g", $realtime, vin, dec7);

                if (dec7 < 0 ) begin
                                Qnmbr = 2**8 + dec7;
                end //if
                else if (dec7 >= 0) begin
                                Qnmbr = dec7;
                end//else if
                else $strobe("%m:STAGE2:Error in (if else), input not valid");

                $strobe("%m:STAGE2:At simulation time %g Qnmbr is %d or %b",$realtime, Qnmbr, Qnmbr);
//              $realtobits(Qnmbr);

                tmp = Qnmbr;
```

```
                for (i = 7; i>=0; i = i - 1) begin
                        if (tmp >= 2**i ) begin
                                bout[i] = 1;
                                tmp = tmp - 2**i;
                        end//if
                        else bout[i] = 0;
                end//for
                $strobe("%m:STAGE2:At simulation time %g \n
                bout[7]= %d \n
                bout[6]= %d \n
                bout[5]= %d \n
                bout[4]= %d \n
                bout[3]= %d \n
                bout[2]= %d \n
                bout[1]= %d \n
                bout[0]= %d", $realtime, bout[7], bout[6], bout[5], bout[4], bout[3], bout[2], bout[1], bout[0] );

end//@cross CLK 1
@(cross(V(CLK) - vth, 1)) begin
                ctrl = 0;
                ctrl_delay = 20p;//This number must be adjusted according to sampling frequency and settling
times
end //@cross CLK -1
    V(CTRL) <+ transition(ctrl, ctrl_delay, trf);
                V(TEST) <+ transition((Qnmbr*vlsb8 - 1), trf,trf,trf);
                V(BIT0) <+ bout[0];
                V(BIT1) <+ bout[1];
                V(BIT2) <+ bout[2];
                V(BIT3) <+ bout[3];
                V(BIT4) <+ bout[4];
                V(BIT5) <+ bout[5];
                V(BIT6) <+ bout[6];
                V(BIT7) <+ bout[7];
end//analog
endmodule
```

B: Circuit schematics

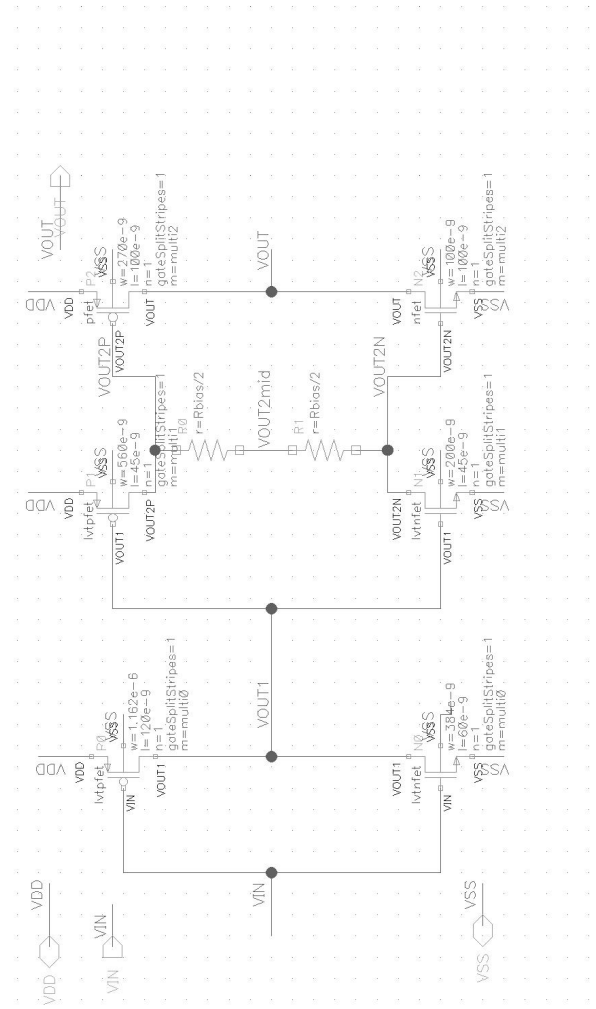

Figure 1: Ring Amplifier

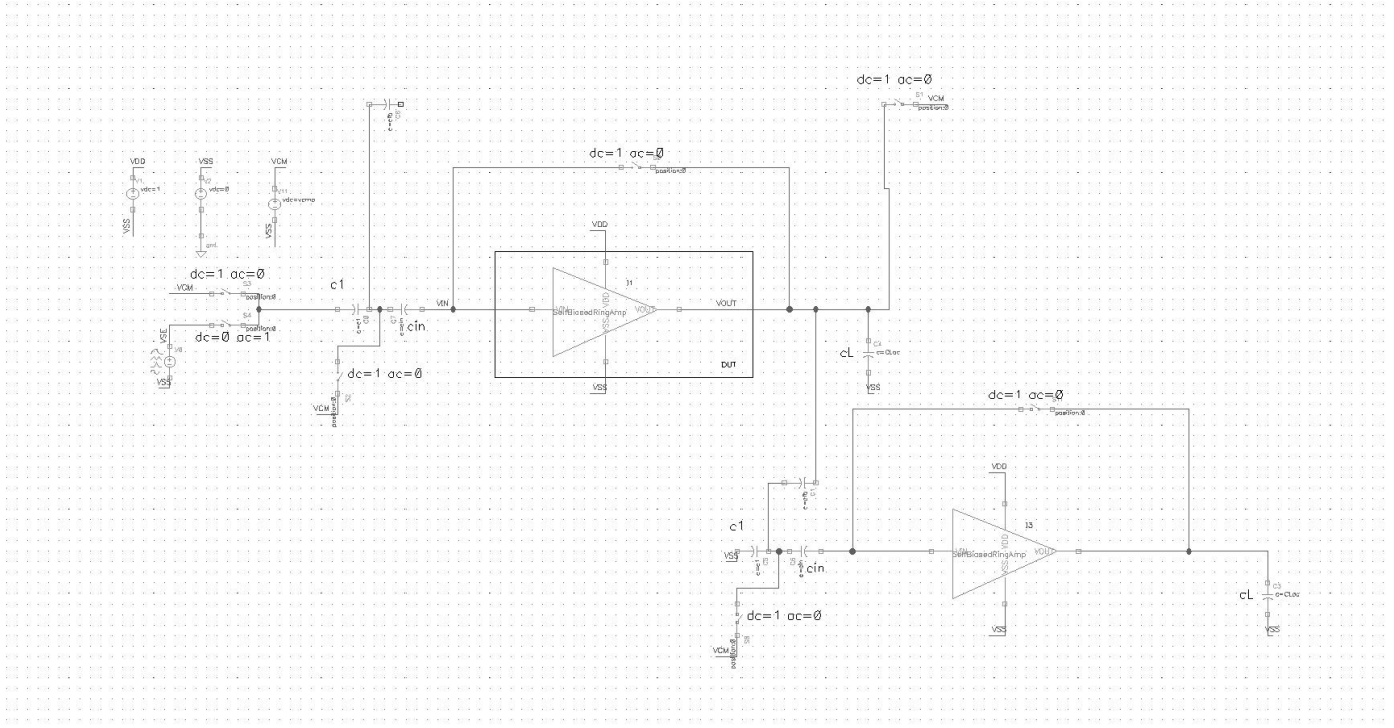

Figure 2: Open loop testbench

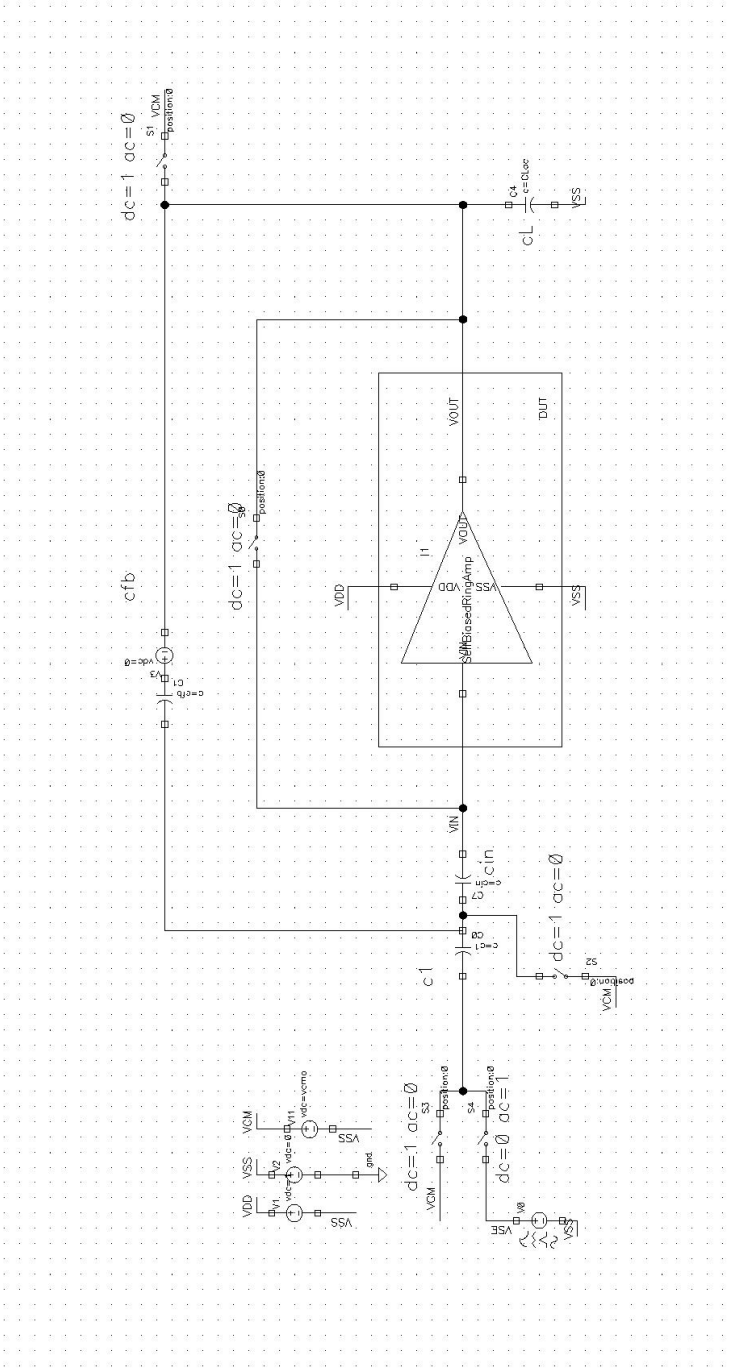

Figure 3: Closed loop testbench

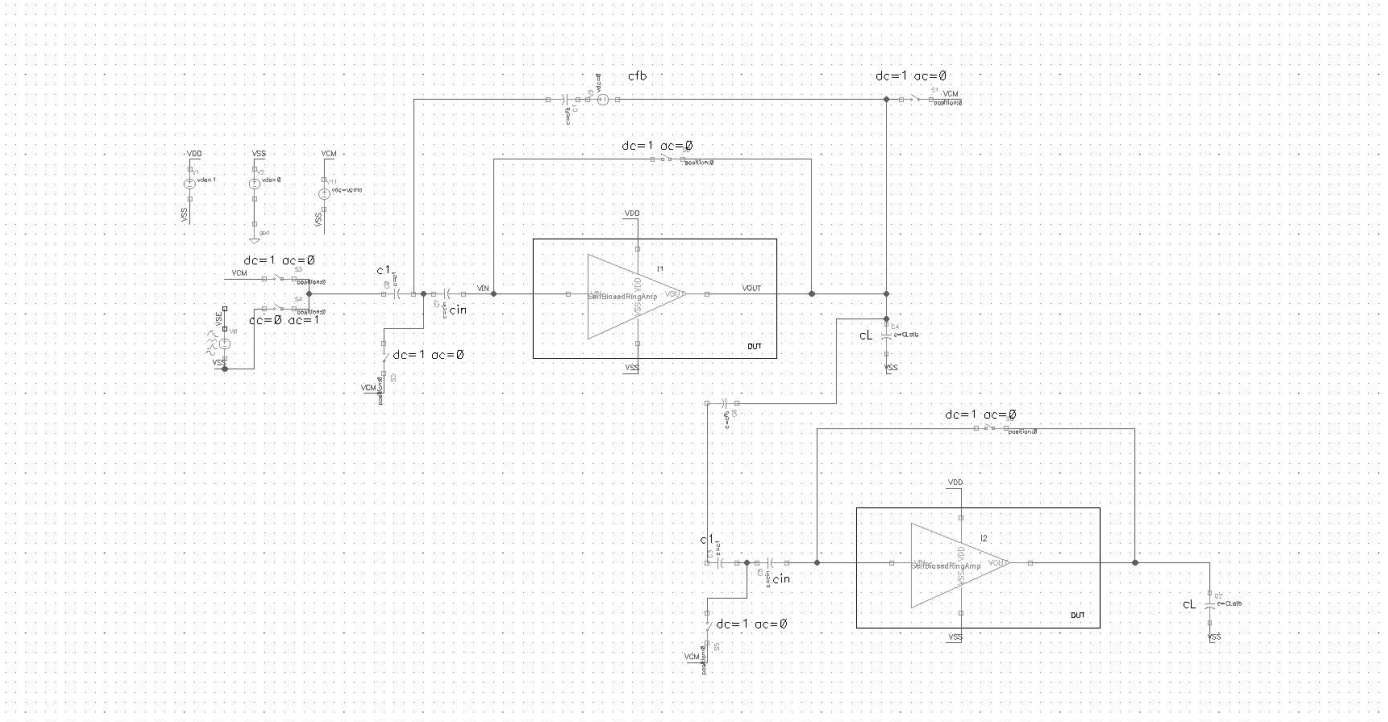

Figure 4: STB testbench

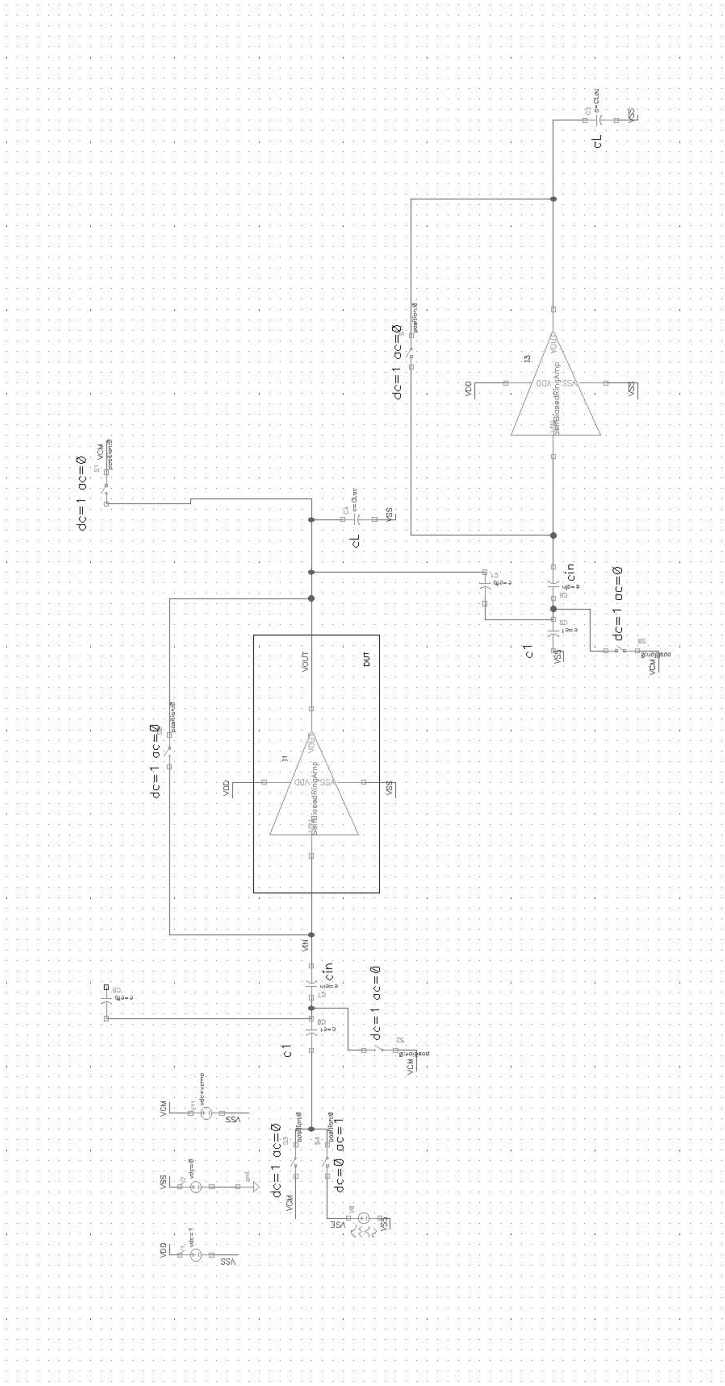

Figure 5: Transient testbench