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# Experimental Investigation of Operational Reliability of Silicon Carbide MOSFETs

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## Abstract

As the performance of silicon power semiconductors is close to the theoretical limit, other semiconductor materials are sought to improve power electronics system efficiency. Devices made with the wide bandgap material silicon carbide (SiC) are promising due to the possibility of significantly improved system efficiency and reduced system volume and weight. However, reliability is still a key issue to be dealt with before wide-spread use of the devices may take place.

In this thesis two of the largest reliability concerns of the SiC MOSFET are evaluated by investigating discrete devices. The issues are the threshold voltage instability and the reliability of packaging of the devices. Dedicated test benches were established to study the issues. The tested devices indicate that the drift of the threshold voltage is still an issue for SiC MOSFETs.

The methodology of performing power cycling tests was investigated. This accelerated life time stress test can be utilized to evaluate packaging reliability. The tests were performed by using the $V_{\mathrm{SD}}(T)$-method to evaluate the junction temperature.

Several devices were tested, all of which indicated failure by bond-wire lift off. The results furthermore indicate that power cycling of SiC MOSFETs is affected by the threshold voltage instability. In particular, a reduction of the on-state voltage was observed at the beginning of almost all the tests, which was attributed to the instability of the threshold voltage. The results call for a discussion as to how power cycling of SiC MOSFETs ought to be performed, in order to reduce the influence of the threshold voltage drift. A suggestion for reducing the influence of the latter is also given.

**Sammendrag**

Krafthalvledere laget av silisium har nesten nådd sin teoretiske ytelsesgrense. Andre materialer har derfor blitt undersøkt for å forbedre effektiviteten til kraftelektronikksystemer. Blant disse er silisiumkarbid (SiC) funnet å være lovende, grunnet muligheten for å forbedre systemkarakteristikker som effektivitet, volum og vekt. Påliteligheten til krafthalvledere av SiC er imidlertid et viktig område som må utbedres før storskala kommersialisering av komponentene kan gjennomføres.

I denne masteroppgaven blir to av de fremste pålitelighetsproblemene for SiC MOSFET studert. Disse problemene er drift av terskelspenning og påliteligheten til pakningen. Dedikerte testoppsett ble laget for å evaluere pålitelighetsproblemene. De testede komponentene indikerer at drift fremdeles er et et problem for SiC MOSFET-komponenter.

Metodikken for å gjennomføre power cycling-tester ble evaluert. Denne testen, som er en akselerert levetidstest, kan bli brukt for å teste påliteligheten til pakningen av komponenter. Testene ble gjennomført ved å bruke $V_{\mathrm{SD}}(T)$-metoden for å estimere temperaturen på halvlederbrikken.

Alle de testede komponentene indikerte feil ved at en del av båndetrådene ble løftet av. Videre indikerte resultatene at drift av terskelspenningen påvirker hvordan power cycling-testen blir gjennomført; en reduksjon i ledespenningen over testobjektet ble observert i starten av nesten alle testene, noe som ble tilskrevet en endring av terskelspenningen. Disse resultatene tilsier at metodikken for power cycling av SiC MOSFET-er bør klargjøres, for å unngå drift av terskelspenningen under testen. En forenklet metode for å gjøre dette er videre foreslått.

## Problem Description

Silicon Carbide (SiC) MOSFETs are promising candidates for being utilized in medium and high voltage applications, due to its potential of drastically reducing system size and losses. However, the present status for SiC MOSFETs is that they suffer from threshold voltage instability and bipolar degradation. This, in addition to possible power cycling reliability issues related to the packaging, call for investigations similar to those normally applied for IGBT devices.

In order to investigate these issues, experimental work will be carried out. In particular, test methodology should be investigated and power cycling experiments of SiC test objects should be performed, the latter with reference to methodologies used for IGBT devices.

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# Abbreviations

**BJT** Bipolar Junction Transistor

**BPD** Basal Plane Dislocation

**CTE** Coefficient of Thermal Expansion

**DBC** Direct Bonded Copper

**DUT** Device Under Test

**FIFO** First In First Out

**FPGA** Field Programmable Gate Array

$I_{\mathbf{D}}$ Drain Current

**IGBT** Insulated Gate Bipolar Transistor

$I_{\mathbf{load}}$ Load Current

$I_{\mathbf{sense}}$ Sensing Current

**JFET** Junction Field Effect Transistor

**MOSFET** Metal Oxide Semiconductor Field Effect Transistor

**NI** National Instruments

$N_{\mathbf{f}}$ Number of Cycles to Failure

**PiN** Positive intrinsic Negative

$P_{\mathbf{V}}$ Power Dissipated in DUT

$R_{\mathbf{DS,on}}$ Drain-Source on-state resistance

**ReliPE** Reliability and Ruggedness of High Power High Voltage Power Electronics

$R_{\mathbf{th}}$ Thermal Resistance

**SAM** Scanning Acoustic Microscopy

**SiC** Silicon Carbide

$T_{\mathbf{c}}$ Case Temperature

**TIM** Thermal Interface Material

$T_{\mathbf{j}}$ Junction Temperature

$T_{\mathbf{off}}$ Power Cycling Off-Time

$T_{\mathbf{on}}$ Power Cycling On-Time

$T_{\mathbf{p}}$ Cycle Period During Power Cycling

**TSEP** Thermo-Sensitive Electrical Parameter

$T_{\mathbf{vj}}$ Virtual Junction Temperature

$V_{\mathbf{DS}}$ Drain-Source Voltage

$V_{\mathbf{DS,warm}}$ Drain-Source Voltage in Warm State During Power Cycling

$V_{\mathbf{GS}}$ Gate-Source Voltage

$V_{\mathbf{GS(th)}}$ Gate Threshold Voltage

**VI** Virtual Instruments

$V_{\mathbf{SD}}(T)$ Source-Drain Voltage Dependency on Temperature

**WBG** Wide Bandgap

**WD** Watchdog

# Chapter 1

# Introduction

## 1.1 Motivation

One of the major challenges currently facing the planet is climate change, due to greenhouse gas emissions resulting to a large extent from the use of fossil fuels [9]. In order to reduce emissions, more renewable energy sources and more efficient power conversion are necessary, both of which heavily depend on power electronics.

Power electronics systems are indispensable in a wide range of applications, such as electric vehicles, power supplies and industrial equipment [10]. The major contributor to losses in such systems is the power semiconductor, and since the conventional silicon power semiconductors have almost reached their theoretical limits [11], it is becoming increasingly difficult to achieve further efficiency increase without resorting to a different power semiconductor.

One option for another semiconductor material is silicon carbide (SiC), being one of the most prominent Wide Bandgap (WBG) materials. SiC devices have several advantages over the conventional silicon semiconductors, enabling high efficiency and compact converters. Among others, these advantages include higher temperature operation, higher voltage ratings for a given chip thickness, lower on-state voltage drops as well as higher thermal conductivity [12]. The SiC MOSFET has been particularly attractive for the market [13], due to having a high blocking voltage capability while retaining the fast switching capability owing to being a unipolar device. In fact, even faster switching may be expected in SiC MOSFETs, due to shorter drift regions in SiC [14].

Many of the benefits of using SiC devices are well established in the literature, as are some of the reliability concerns that the devices are currently facing [15]. Thorough testing of the reliability issues are necessary before widespread use of the device will be possible [16]. Moreover, current reliability testing of SiC MOSFETs in particular has to a large extent focused

on challenges related to the threshold voltage and the internal body diode of the device. The reliability of packaging and encapsulation has not been dealt with to the same extent. These are important issues, considering that the main cause of failure in high power converters is failure of the semiconductor [17].

Reliability is a key concept throughout this work, and is defined by Lutz et. al as "the ability of a system or component to perform its required functions under stated conditions for a specified period of time" [3, p. 380]. Consequently, for a power electronics system to operate reliably, it must be able to operate over time in spite of a certain amount of degradation. This is a challenging task due to the relatively long expected lifetime of power electronic systems.

Reliability is thus a complex subject, as it comprises a wide range of degradation effects, being related to thermal, mechanical and electrical properties of the device. It has therefore been decided to restrict the attention of this master's thesis to reliability issues related to packaging. Although being important for the long-term reliability of a power semiconductor, aspects such as robustness and ruggedness will not be discussed. Moreover, the bipolar degradation of the device will not be covered in detail, as the time did not allow performing testing of this in addition to the threshold voltage instability and power cycling.

The aim of this master's thesis is to evaluate how reliability testing of the packaging may be performed. More specifically, the thesis will evaluate how the accelerated lifetime stress test called power cycling may be utilized to test the reliability of SiC MOSFETs. This has been a challenge due to the threshold voltage instability, which has complicated estimating the temperature of the device during the test. Therefore, the threshold voltage drift will also be investigated. The thesis will evaluate the use of the recently proposed $V_{\mathrm{SD}}(T)$-method [18], and perform power cycling on discrete devices using this approach.

## 1.2 Background

This master's thesis is written in conjunction with SINTEF Energy's project Reliability and Ruggedness of High Power High Voltage Power Electronics (ReliPE) [19]. The project aims to improve the reliability of high power converter systems, in addition to getting a better understanding of fault mechanisms in order to develop models for lifetime estimation during operation. As such, the goal of the thesis is to contribute to deepening the knowledge on reliability challenges of SiC MOSFETs, and how these might be tested.

In the course of the thesis, a test bench for performing power cycling on SiC MOSFETs has been developed. Some parts of the physical set-up has

been reused from a previous a set-up developed by M.Sc. Øyvind B. Frank in his master's thesis [20]. That set-up was used in order to evaluate the power cycling capability of single chips from a press-packed IGBT module, and thus, several modifications were necessary.

## 1.3 Outline of Thesis

The outline of the thesis is provided in the following.

Chapter 2 presents advantages and disadvantages of SiC devices in general, and the SiC MOSFET in particular. Packaging of the device and how the junction temperature may be estimated are also presented.

In Chapter 3, the test rig for testing threshold voltage drift of the SiC MOSFET is presented. The results from the test are also provided.

The conventional power cycling procedure as well as the procedure for performing power cycling of SiC MOSFETs are presented in Chapter 4. Chapter 5 presents the test rig for performing power cycling on SiC MOSFETs.

Chapters 6 and 7 present the results and discusses these, respectively. Finally, the conclusion of the thesis is given in Chapter 8.

# Chapter 2

# SiC MOSFET

The potential advantages of using silicon carbide semiconductor devices have been known for several decades [21, p. 4], yet it was not until the previous decade that some of the SiC devices became commercially available [22]. In this chapter, some of the main advantages and disadvantages for SiC devices will be elaborated on. Moreover, the diode and MOSFET structures will be presented, in addition to the most common packaging types for MOSFETs. Lastly, a method for estimating the junction temperature of a pn-junction will be introduced, as this explains how the $V_{\mathrm{SD}}(T)$-method may be utilized to obtain the junction temperature of the SiC MOSFET.

## 2.1 Silicon Carbide Material Properties

The advantages of SiC devices are well documented in the literature. In the following, therefore, only the main advantages will be described. For a more thorough description of the properties of SiC, see e.g. [21].

Table 2.1 compares some of the most important material properties between silicon and SiC. SiC has several stable polytypes, meaning that the material has numerous stable crystal structures [21, p. 11]. These include amongst other 3C-SiC, 4H-SiC and 6H-SiC. Although 3C-SiC and 6H-SiC have been used for making power semiconductors, 4H-SiC is the current polytype of choice for power semiconductor manufacturers [14]. Therefore, SiC from now on refers to 4H-SiC.

One of the main advantages of SiC over silicon is the wider bandgap. This yields lower intrinsic carrier densities for any given temperature than what is possible for silicon [1, p. 661], leaving pn-junctions effective at much higher temperatures. Thus, SiC devices are able to operate at much higher temperatures for the same doping levels. Furthermore, significantly reduced leakage currents can also be obtained due to the larger bandgap, provided that the production quality is sufficiently good.

Another major advantage is the order of magnitude higher critical elec-

Table 2.1: Comparison of Material Properties Between Si and SiC [7, 8].

| Property | Silicon | Silicon Carbide (4H-SiC) |
|---|---|---|
| Bandgap [eV] | 1,12 | 3,2 |
| Critical Electric Field [$\mathrm{MV\,cm^{-1}}$] | 0,3 | 3 |
| Thermal Conductivity [$\mathrm{W\,m^{-1}\,K^{-1}}$] | 1,3 | 5 |
| CTE [ppm/K] | 3 | 4,3 |
| Youngs Modulus [GPa] | 152 | 501 (Anisotropic) |

tric field. Not only does this reduce the length of the drift region by the same factor [14], but furthermore the specific on-state resistance is drastically reduced [1, p. 662], finally resulting in more than three orders of magnitude reduction of the on-state resistance [23]. This fact has enabled unipolar devices with considerably larger rating in SiC than what is feasible for their silicon counterparts. Moreover, in conjunction with reduced carrier lifetimes in SiC [1, p. 662], the shorter drift region reduces the amount of charge that needs to be moved during switching, hence allowing considerably faster switching [14].

The higher thermal conductivity of SiC devices allows a higher power throughput for the same junction temperature, or lower junction temperature for the same power throughput. Thus, this factor is expected to contribute to reduced losses. However, the higher thermal conductivity also leads to a higher temperature at the edges of the chip [8], which potentially could increase the stress on the underlying solder layer.

SiC has a larger coefficient of thermal expansion (CTE), meaning that for a given rise in temperature, SiC will expand more than silicon. Whether this is advantageous or not depends on the adjacent materials that are utilized in the device package. Generally, if the CTE of adjacent materials are similar, it means that they expand at a similar rate, which leads to reduced stress as opposed to if the CTEs are further apart. Two materials which often are found close to the chip is aluminum oxide and copper. Since the CTE of SiC is closer to their CTE than that of silicon, the SiC CTE is considered to be somewhat better [8].

On the other hand, the much larger Youngs Modulus is a clear disadvantage, as it renders SiC more than 3 times stiffer than Si. In fact, Herold et al. argues that this disadvantage is so crucial that it outweighs the advantages in CTE and thermal conductivity [8]. The increased Youngs modulus yields significant stress on the solder beneath the chip during power cycling, and can lead to drastically reduced reliability compared to silicon counterparts.

In conclusion, it seems like the SiC power semiconductors outperforms the traditional silicon devices in terms of electrical characteristics. However, mechanical properties indicate that silicon devices are preferable [8]. That being said, Herold et. al argues that if state of the art technology is uti-

lized, these disadvantages may be mitigated, thereby achieving the desired reliability [8].

## 2.2 Silicon Carbide Devices

This section will briefly explain the PiN diode and MOSFET structures. The structure of SiC devices is largely identical to what is found in silicon devices [14], and hence, most of this section will be based on literature explaining silicon devices. Whenever there is a difference, however, the particularities of SiC will be emphasized.

### 2.2.1 PiN Diode

The structure of PiN (Positive intrinsic Negative) diode is displayed in fig. 2.1. The + indicates a highly doped region, whereas the - indicates a moderately doped region. The drift region in the centre of the structure is thus several orders of magnitude lower in doping, however it is not truly intrinsic as its name may allude to [21, p. 287].

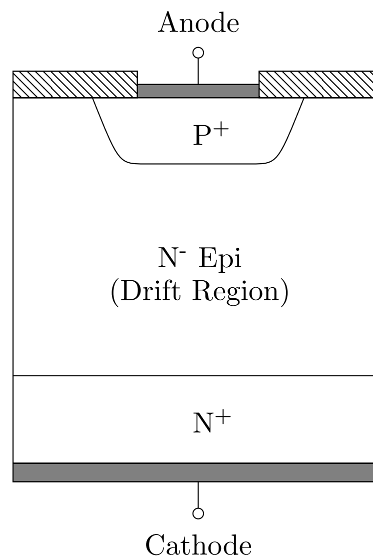



Figure 2.1: Structure of the PiN diode [1, p. 525]

Since both the density of free holes and electrons decrease when approaching the $P^+N^-$ junction, both carriers will diffuse across it, which causes a potential barrier at the same junction. This potential barrier results in a region called the depletion layer, which is depleted of any charge carriers, except those that are generated by thermal ionization. The latter are however immediately swept away from the depletion layer due to the electrical field caused by the potential barrier. Moreover, the potential barrier impedes

any current flow, as the drift and diffusion currents sum to zero for both the holes and the electrons [1, p. 516].

Applying a negative anode-cathode voltage enlarges the potential barrier, such that the device is blocking any current conduction. This is termed reverse bias. If a positive anode-cathode voltage is applied, the potential barrier is reduced and the device is said to be forward biased [1, p. 515]. When in this state, holes diffuse from the $P^+$-region into the drift region. Once the injection of holes is sufficiently large, electrons from the $N^+$ layer are attracted into the same region. This finally results in considerably improved conductivity of the drift region, and is termed conductivity modulation [1, p. 532].

### 2.2.2 MOSFET

There exists several variations of the Metal Oxide Semiconductor Field Effect Transistor MOSFET structure, the major ones being the planar and the vertical MOSFET. Currently, planar devices are commercialized [24], while vertical devices, more specifically trench MOSFETs, are announced for mass production [25], and thus likely close to being commercialized. Since the literature mainly has focused on devices using the planar structure [2, p. 236], this will be considered in the following. Therefore, unless stated otherwise, MOSFET now refers to the planar device type.

The structure of the SiC MOSFET is largely identical to that of the Si MOSFET, except that the base doping is reduced and that a heavily doped shielding layer is added to the conventional silicon D-MOSFET structure [2, p. 236]. This can be seen in fig. 2.2, in which a simplified view of one half of the structure is presented. The larger SiC bandgap would cause excessive threshold voltages, which necessitates the reduction of doping of the base region. Reducing the latter could potentially lead to reach-through problems due to the high critical electric field in SiC. Without the shielding layer, a trade-off between large threshold voltages and small breakdown voltages would have to be made. However, by including it, reasonable threshold voltages can be maintained while at the same time not compromising on breakdown voltage levels.

One important feature of the MOSFET structure is that it contains a parasitic npn-BJT (Bipolar Junction Transistor), where the p-layer acts as the base [2, p. 237]. To reduce the risk of accidental turn-on of this transistor, the shielding region is shorted to the source terminal, such that the emitter and base of the parasitic BJT are close to being at the same potential. The consequence of this is the formation of a parasitic diode, known as the body diode [1, p. 574]. The MOSFET source thus acts as the anode for the diode.

When the MOSFET is blocking, the gate-source voltage $V_{\mathrm{GS}}$ is less than or equal to zero, while the drain source voltage $V_{\mathrm{DS}}$ is positive. The JFET region is then forming a potential barrier that is depleted of charge carriers,

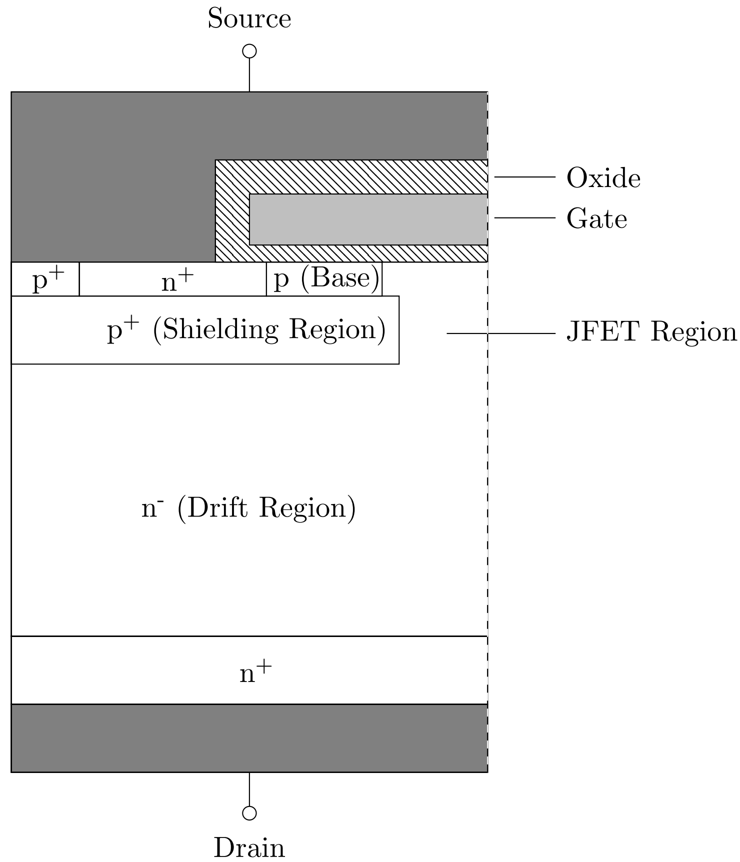



Figure 2.2: Shielded planar inversion-mode n-MOSFET [2, p. 236]

due to the presence of the shielding region [2, p. 237]. This configuration drastically alleviates the stress experienced by the gate oxide, due to almost the entire field laying across the JFET and drift regions [2, p. 236].

If a negative voltage is applied across the drain-source terminals, the internal body diode will be forward biased and thus start to conduct. Depending on the magnitude and sign of $V_{\mathrm{GS}}$, several things may occur. For large values of $V_{\mathrm{GS}} > 0$, the current will flow through the channel, whereas for small values of $V_{\mathrm{GS}} > 0$, a portion of the current will flow over the channel and the body diode. If $V_{\mathrm{GS}} \leq 0$, almost the entire current will flow through the body diode. For SiC devices, however, the channel is slightly conducting until a relatively low value of $V_{\mathrm{GS}}$ is attained. This will be described further in Section 4.3.

For an n-type MOSFET, when both $V_{\mathrm{GS}}$ is at its nominal positive gate voltage and $V_{\mathrm{DS}}$ is positive, the device is said to be in inversion- or enhancement-mode. For low values of $V_{\mathrm{GS}}$, majority carriers (positive charge in this case) are repelled from the base-oxide interface as positive

charge accumulates at the gate. When further increasing the gate voltage to the point where $V_{\mathrm{GS}} = V_{\mathrm{GS(th)}}$, i.e. the threshold voltage of the device, free electrons are attracted to the interface, while free holes are repelled. Once $V_{\mathrm{GS}}$ is further increased the density of free electrons also increases at the interface, at which point the inversion layer is considered to be formed, enabling the conduction of currents [1, p. 578]. This conduction happens through the channel that is established between the drain and source terminals.

The main contributions to the on-state resistance of the device are the channel, drift region and JFET resistances. These have differing signs of their temperature coefficients, the total is however positive [26].

## 2.3 Particular SiC MOSFET Reliability Issues

### 2.3.1 Threshold Voltage Instability

One of the largest reliability concerns of the SiC MOSFET has been the threshold voltage instability, which constitutes a drift of the threshold voltage as a result of a gate bias applied over time [15]. An increase of the threshold voltage leads to higher on-state voltages for a given current, thereby leading to increased losses. On the other hand, a reduction of the threshold voltage increases the leakage current. In addition, a negative drift causes the channel to be open at lower gate-source voltages. As such, this could be detrimental in the event of transients or noise in the gate-source voltage, since it could cause an accidental turn-on of the device.

Even with significant improvements in recent generations [27], the problems related to the drift of the threshold voltage is still considered to be one of the main reliability issues for SiC MOSFETs that needs to be solved. Even though the exact physical mechanisms responsible for the drift are not fully understood, it is believed that charging and neutralization of near-interfacial oxide traps via tunneling is the main mechanism [27].

The instability comes as a result of applying either a positive or negative gate bias. The observed drift has the same polarity as the applied bias, meaning that if a positive bias is applied, a positive drift occurs. The magnitude of the drift further increases with both increasing magnitude of the gate bias, as well as duration of the bias. At room temperature, a typical magnitude of the drift is about 0.25-0.5 V given an oxide field strength in the range of $\pm 2$ to $\pm$ 3 MV/cm and a stress duration from minutes up to one hour [27]. When measuring the threshold voltage, it is important to be aware that the largest shift in threshold voltage happens initially, such that measurements ought to be performed as soon as possible after completing an experiment.

Another factor heavily influencing the observed instability is temperature. At room temperature, equally long positive and negative bias leads

to ending up with the same threshold voltage, i.e. the effect is reversible. At elevated temperatures, however, the rates of charging and neutralization differ, resulting in drift even though the duration of bias is the same [27]. Thus, it can be expected that devices operating at higher temperatures are subjected to a larger shift in the threshold voltage.

### 2.3.2 Bipolar Degradation

Another reliability issue that the SiC MOSFET experiences is the increase in forward voltage of its internal body diode if it carries a considerable forward current. This reliability issue is termed bipolar degradation, and is a problem faced by all SiC PiN diodes [21, p. 156].

Bipolar degradation results due to stacking faults in the basal plane [28], meaning that the SiC polytype is changed at some locations in the crystal. For example, if a device normally is made of a 4H-polytype, the crystal may locally deform into a 3C- or 6H-polytype if experiencing bipolar degradation. The stacking faults originate from a crystal defect called basal plane dislocation (BPD), the propagation of which increase with increasing current density and temperature [29].

The stacking faults serve as recombination centres [28], thus reducing the carrier lifetimes and leading to an increased forward voltage. Moreover, the stacking faults impede current conduction by reducing the available area for current to flow, which also contributes to an increased forward voltage for a given current [29].

Bipolar degradation is unfavorable as an increase in the forward voltage yields higher losses for a given current through the body diode. Another reason for why it is a reliability concern is that a local altering of the forward voltage may result in thermal runaway [29]. Due to the negative temperature coefficient of the body diode, a local increase in the forward voltage will cause a higher current in that region, and thus higher temperatures due to the increased losses. This positive feedback mechanism may in the worst case scenario lead to the mentioned thermal instability.

To begin with, bipolar degradation was considered to be a problem for only bipolar devices. It has been shown, however, that the SiC MOSFET on-state resistance can increase as a result of it [15, 30]. Recent tests in the literature has given ambiguous results as to the present status of the bipolar degradation. While devices from some manufacturers experienced little degradation [31, 32], others did not experience any degradation at all [15, 32]. This might be a result of an ongoing process for improving manufacturing technique.

## 2.4 Packaging Technology

There exists different kinds of packaging depending on the semiconductor device technology as well as the intended use of the device. The main packaging types for MOSFETs are discretes and modules, and hence, these will be briefly discussed in the following. Since the device packaging largely is the same for SiC and Si devices [15], the discussion will be based on similar silicon technology.

### 2.4.1 Discrete Packages

Discrete packages contain one single semiconductor chip, and are consequently made without any internal insulation. This kind of packaging is often utilized for lower power ranges [3, p. 348]. A typical package structure is shown in fig. 2.3, in which a typical TO-package is depicted. The bond wires connect the chip and input pins. The latter is traditionally made in aluminum. The semiconductor chip is soldered directly on top of a copper layer.

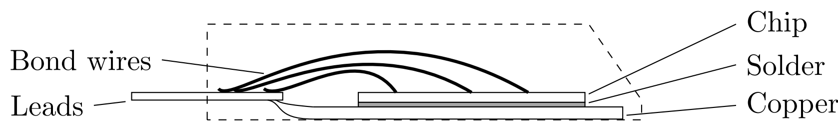



Figure 2.3: Discrete TO package [3, p. 349]

This kind of packaging contains several reliability challenges. One of these is the bond-wires [3, p. 350], which may be physically lifted off the chip, normally as a result of large temperature cycling of the junction [33]. This may occur in real converters as a result of differing operating points over time.

Another weak point in terms of packaging reliability is the interconnecting solder layer. This layer may experience fractures developing as a result of large mechanical stress from layers with differing CTEs [3, p. 403]. Moreover, the fractures lead to an increased internal temperature gradient, finally causing a higher chip temperature. This is particularly severe for devices with a positive temperature coefficient, such as the MOSFET [34], as the increased chip temperature leads to more losses, which again raises the chip temperature. This positive feedback mechanism could thus potentially lead to thermal runaway.

### 2.4.2 Power Modules

Another commonly used packaging type for MOSFETs are power modules [3, p. 353]. A module contains several semiconductor chips in parallel, necessitating electrical isolation within the package. Currently, the packaging

type is widely used in the mid-power range, and is increasingly entering the high-power range [3, p.346]. A schematic structure of a typical module is depicted in fig. 2.4.

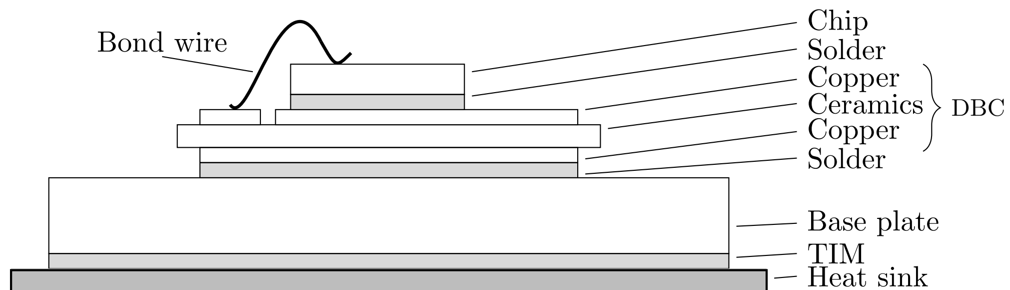



Figure 2.4: Standard power module with corresponding layers [3, p. 354]

The semiconductor chip is placed on the top of the module structure with a bond-wire connected to it. The soldering layer under the chip provides electrical contact to the top of the so-called "direct bonded copper" (DBC) substrate. The DBC constitutes a ceramic with copper on either side of it. The copper layer closest to the chip conducts the current, whereas the ceramic serves as an insulator [3, p. 355]. The DBC is then typically soldered onto a base plate, which concludes the module structure. In applications, the base plate is mounted onto a heat sink. In-between the two is a thermal interface material (TIM), in order to reduce the thermal resistance between the module and heat sink.

Although having several more layers than the discrete package, the two packaging types typically both include bond wires as well as solder layers. Therefore, the main reliability issues for modules are similar to those of discrete packages; module bond-wires are also typically made in aluminum, thereby presenting the same reliability issues as mentioned above. Moreover, solder layers have proven to be a vulnerable part of the module, and the increased number of solder layers of modules increases the possibility for obtaining solder voids, which may lead to increased thermal resistance [3, p.354]. Finally, the differing CTEs of adjacent layers may cause mechanical stress at the interfaces in the event of temperature cycling.

## 2.5 Estimation of Junction Temperature

When performing power cycle testing, it is imperative to estimate the junction temperature of the device under test (DUT) to be able to evaluate the results [18]. In particular, two of the main parameters are the temperature swing, being the difference between the maximum and minimum junction temperature, as well as the minimum temperature [3, p. 391].

However, obtaining an accurate value for the junction temperature is a challenging task. This stems from the inaccessibility of the semiconductor die, yet it is further complicated by the fact that the chip may contain significant lateral thermal gradients [3, p. 405]. In particular, the centre of the chip is often much warmer than the edges. Even though SiC devices have improved thermal conductivity compared to silicon devices, there might still be a large temperature gradient present, as shown in [8]. Hence, the junction temperature is spatially varying.

There are several ways to estimate the junction temperature, some of which are more applicable than others. Two options are to use thermocouples or optical wires to measure the temperature directly. However, these methods require direct access to the semiconductor die, which is only possible by destroying the packaging. Another option is to utilize infrared cameras, which are able to measure sufficiently fast, yet are limited to evaluating the temperature at the surface. Thus, the camera will only be able to measure the case temperature, whereas the actual junction temperature might be considerably higher.

One way of circumventing these issues, is by utilizing a thermo-sensitive electrical parameter (TSEP). As the name implies, the general idea is to measure an electrical parameter that is sensitive to temperature in order to estimate the temperature. To be able to utilize the relationship, a calibration needs to be performed that relates the temperature to the electrical parameter. Then, the parameter can be used to estimate the temperature, for example during power cycling [4]. The advantage of using TSEPs are that these are fairly simple to implement and that the temperature can be estimated without physically accessing the chip. Moreover, depending on the chosen TSEP, a sort of weighted junction temperature is obtained, thereby accounting to a certain degree for the lateral temperature differences. An advantage of the latter is that the estimated temperature reflects the temperature of the entire chip. On the other side, local extrema may not be well accounted for by this method.

Since the temperature is not measured directly, the estimated junction temperature is termed virtual junction temperature ($T_{\mathrm{vj}}$). More precisely, $T_{\mathrm{vj}}$ is defined as "a temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behavior of the semiconductor device" [35].

As for all sensors, it is important that the TSEP displays a sufficiently high sensitivity and accuracy. Moreover, linearity in the relationship between the electrical parameter and temperature is also wanted, as it considerably simplifies the estimation of the temperature. Finally, it is imperative that the TSEP is stable over time, such that the estimated temperature is reliable.

There are several candidates for being utilized as TSEPs to estimate the junction temperature of SiC MOSFETs. These include the on-state resis-

tance, $R_{\mathrm{DS,on}}(T)$, as well as the threshold voltage, $V_{\mathrm{GS(th)}}(T)$ [18]. Another viable TSEP utilizes the turn-off delay of the MOSFET [34]. However, all of these depend explicitly on the threshold voltage, and hence, if a drift of the threshold voltage occurs, their estimation of the junction temperature is rendered unusable. Thus, these are not reliable options to be used in conjunction with the SiC MOSFET.

The problem of finding a trustworthy TSEP for SiC MOSFETs has been addressed in the literature [4], but it was not until recently that a viable TSEP was suggested [18]. The proposed TSEP is the source-drain voltage of the MOSFET, which will be explained in the following.

### 2.5.1 $V_{\mathrm{SD}}(T)$-Method

The $V_{\mathrm{SD}}(T)$-method utilizes the voltage drop across the internal body diode to estimate the temperature of the junction. In order to understand how the $V_{\mathrm{SD}}(T)$-method can be used as a TSEP, the temperature dependency of a pn-junction needs to be explained. Unless stated otherwise, the following is based on Chapters 2 and 3 of [3].

There are two mechanisms that contribute to currents in semiconductors, so-called diffusion and drift currents [1, p. 512]. Diffusion currents arise due to a spatially differing concentration of charge. If for instance one particular region has a higher density of electrons than another, there will be an electron current from the region with the higher density to the one with the lower. Drift currents on the other hand originate when an external field is applied. Then, holes experience a force in the direction of the field, whereas electrons experience a force in the opposite direction of the field, due to their negative charge.

Consider a simplified abrupt pn-junction. An abrupt step junction is characterized by a step-like transition between the n- and p-layers. The resulting space charge distribution $\rho$ as a function of the distance $x$ is displayed in fig. 2.5, in which the p- and n-regions correspond to $x < 0$ and $x > 0$ respectively. The space charge distribution occurs due to diffusion of charge across the boundary. This leaves exposed charge on either side of the junction, resulting in an electric field that creates a drift current opposing the diffusion current. In equilibrium, these currents cancel each other out, finally causing the distribution as seen in the figure.

Consider now the total hole current density, $j_{\mathrm{p}}$, in a semiconductor. This is given by the sum of the hole diffusion and drift current densities, which can be expressed as

$$j_{\mathrm{p}} = q \cdot (\mu_{\mathrm{p}} p E - D_{\mathrm{p}} \frac{dp}{dx}), \tag{2.1}$$

where $q$ is the elementary charge, $\mu_{\mathrm{p}}$ is the hole mobility, $p$ is the hole density, $E$ is the electric field and $D_{\mathrm{p}}$ is the hole diffusion constant. Thus,

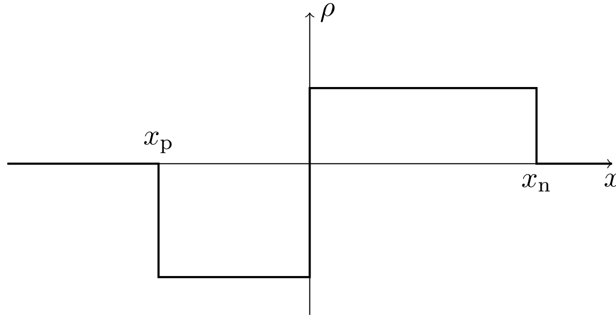



Figure 2.5: Space charge distribution of an abrupt pn-junction

the first term in equation 2.1 corresponds to the drift current, whereas the second is caused by the diffusion current.

In the following, assume a low level of injection of carriers from both sides of the junction, and that the minority carrier densities are small compared to the doping densities. Consider the hole current in the neutral part of the n-region. With the previously stated assumptions, the density of holes is much smaller than the density of electrons, and the applied electric field is relatively small in this region. Therefore, the contribution to the current from the drift term can be neglected, such that equation 2.1 simplifies to

$$j_\mathrm{p} = -qD_\mathrm{p}\frac{dp}{dx}, \tag{2.2}$$

Moreover, in the same region, it also holds that

$$\frac{dj_\mathrm{p}}{dx} = -qR_\mathrm{p}, \tag{2.3}$$

where $R_\mathrm{p}$ is defined as the rate of recombination minus the rate of generation of holes. In the stationary case, $R_\mathrm{p}$ is thus given by the excess generation, $p - p_\mathrm{n0}$, over the minority carrier lifetime $\tau$,

$$R_\mathrm{p} = \frac{p - p_\mathrm{n0}}{\tau}. \tag{2.4}$$

Here, $p_\mathrm{n0}$ denotes the hole density in the n-region at equilibrium. It is further given by $p_\mathrm{n0} = n_i^2/N_\mathrm{D}$, where $n_i$ is the intrinsic carrier density and $N_\mathrm{D}$ is the donor doping density. Thus, assuming stationary conditions, equations 2.2, 2.3 and 2.4 combine to give

$$\begin{aligned} \frac{d}{dx}[-qD_\mathrm{p}\frac{dp}{dx}] &= -qR_\mathrm{p} \\ D_\mathrm{p}\frac{d^2p}{dx^2} &= \frac{p - p_\mathrm{n0}}{\tau} \end{aligned} \tag{2.5}$$

The solution to this second-order differential equation, given a boundary condition of $p(x_\mathrm{n}) = p_{\mathrm{n0}} \cdot \mathrm{e}^{qV/kT}$, is given in equation 2.6:

$$p(x) = p_{\mathrm{n0}} + p_{\mathrm{n0}} \cdot (\mathrm{e}^{qV/kT} - 1) \cdot \mathrm{e}^{-(x-x_\mathrm{n})/L_\mathrm{p}}, \tag{2.6}$$

where $V$ is the voltage applied to the pn-junction and $L_\mathrm{p} = \sqrt{D_\mathrm{p} \cdot \tau_\mathrm{p}}$ is the hole diffusion length. By equating

$$\frac{dp}{dx} = -\frac{p_{\mathrm{n0}}}{L_\mathrm{p}}(\mathrm{e}^{qV/kT} - 1) \cdot \mathrm{e}^{-(x-x_\mathrm{n})/L_\mathrm{p}}, \tag{2.7}$$

and inserting into equation 2.2 evaluated at $x = x_\mathrm{n}$, one finds the hole current density to be given by

$$j_\mathrm{p}(x_\mathrm{n}) = \frac{q \cdot p_{\mathrm{n0}} \cdot D_\mathrm{p}}{L_\mathrm{p}}(\mathrm{e}^{qV/kT} - 1). \tag{2.8}$$

With the same reasoning as above, the electron current density, $j_\mathrm{n}$, evaluated at $x = x_\mathrm{p}$ is given by

$$j_\mathrm{n}(x_\mathrm{p}) = \frac{q \cdot n_{\mathrm{p0}} \cdot D_\mathrm{n}}{L_\mathrm{n}}(\mathrm{e}^{qV/kT} - 1), \tag{2.9}$$

where $n_{\mathrm{p0}}$ is the electron density in the p-region at equilibrium, $D_\mathrm{n}$ is the electron diffusion constant and $L_\mathrm{n}$ is the electron diffusion length, defined analogously to the hole diffusion length. Moreover, $n_{\mathrm{p0}} = n_i^2/N_\mathrm{A}$, where $N_\mathrm{A}$ is the acceptor doping density.

By assuming that recombination and generation of charge is negligible in the relatively thin space charge layer, the electron and hole currents are constant across this layer. In other words,

$$j_\mathrm{n}(x_\mathrm{n}) = j_\mathrm{n}(x_\mathrm{p}) \quad \wedge \quad j_\mathrm{p}(x_\mathrm{p}) = j_\mathrm{p}(x_\mathrm{n}). \tag{2.10}$$

Thus, the total current density can be written as a function of the minority carrier diffusion currents in the neutral regions at the borders to the space charge layer. By combining equations 2.8 and 2.9, the relationship between the current density and voltage across the pn-junction is given by

$$j = j \cdot {}_\mathrm{s}(\mathrm{e}^{qV/kT} - 1), \tag{2.11}$$

where $j_\mathrm{s}$ is defined as

$$\begin{aligned} j_\mathrm{s} &= q(\frac{p_{\mathrm{n0}} \cdot D_\mathrm{p}}{L_\mathrm{p}} + \frac{n_{\mathrm{p0}} \cdot D_\mathrm{n}}{L_\mathrm{n}}) \\ &= q \cdot n_i^2(\frac{D_\mathrm{p}}{L_\mathrm{p} \cdot N_\mathrm{D}} + \frac{D_\mathrm{n}}{L_\mathrm{n} \cdot N_\mathrm{A}}) \end{aligned} \tag{2.12}$$

If considering figure 2.2, it is clear that the doping of the shielding region is much larger than the drift region doping. Therefore, assuming further that the acceptor doping is much larger than the donor doping, $N_\mathrm{A} \gg N_\mathrm{D}$, equation 2.12 can be written as

$$j_\mathrm{s} = q \cdot n_i^2 \cdot \frac{D_\mathrm{p}}{L_\mathrm{p} \cdot N_\mathrm{D}}. \tag{2.13}$$

Solving equation 2.11 for the applied voltage yields

$$V = \frac{k \cdot T}{q} \ln(\frac{j}{j_\mathrm{s}} + 1). \tag{2.14}$$

With $n_i^2 = N_\mathrm{C} \cdot N_\mathrm{V} \cdot \mathrm{e}^{-E_\mathrm{g}/kT}$, where $N_\mathrm{C}$ and $N_\mathrm{V}$ are the density of states in the conduction and valence band respectively, equation 2.14 can be reformulated as

$$V = \frac{k \cdot T}{q} \ln(\frac{j}{q \cdot N_\mathrm{C} \cdot N_\mathrm{V} \cdot \mathrm{e}^{-E_\mathrm{g}/kT} \cdot \frac{D_\mathrm{p}}{L_\mathrm{p} \cdot N_\mathrm{D}}} + 1). \tag{2.15}$$

Assuming $V > 3 \cdot \frac{k \cdot T}{q}$, one finds

$$\begin{aligned} V &\approx \frac{k \cdot T}{q} \ln(\frac{L_\mathrm{p} \cdot N_\mathrm{D} \cdot j}{q \cdot N_\mathrm{C} \cdot N_\mathrm{V} \cdot D_\mathrm{p}} \cdot \mathrm{e}^{E_\mathrm{g}/kT}) \\ &= \frac{E_\mathrm{g}}{q} + \frac{k \cdot T}{q} \ln(\frac{L_\mathrm{p} \cdot N_\mathrm{D} \cdot j}{q \cdot N_\mathrm{C} \cdot N_\mathrm{V} \cdot D_\mathrm{p}}) \end{aligned} \tag{2.16}$$

The fraction $q \cdot N_\mathrm{C} \cdot N_\mathrm{V} \cdot D_\mathrm{p}/(L_\mathrm{p} \cdot N_\mathrm{D})$ represents a very high current density. Since the assumption of low injection is made, the fraction inside the natural logarithm in equation 2.16 is less than one. For clarity, the equation will therefore be written as

$$V = \frac{E_\mathrm{g}}{q} - \frac{k \cdot T}{q} \ln(\frac{q \cdot N_\mathrm{C} \cdot N_\mathrm{V} \cdot D_\mathrm{p}}{L_\mathrm{p} \cdot N_\mathrm{D} \cdot j}) \tag{2.17}$$

It is thus clear that the voltage drop over the pn-junction is merely dependent on the current density and the temperature, since all the other terms are constant for a given pn-junction. By keeping the current through the junction constant too, there is a linear relationship between the voltage across the junction and the temperature at the junction. In particular, the temperature coefficient is negative at the junction.

Clearly, if the relationship between temperature and voltage is known, the temperature of a pn-junction can be estimated by measuring the voltage across it provided that a constant current is flowing. Since the MOSFET structure contains a parasitic diode, the pn-junction of the diode can be used to estimate the virtual junction temperature of the MOSFET. That is the

basic idea in the $V_{\mathrm{SD}}(T)$-method, which is shown in fig. 2.6. One important note, however, is that the constant current needs to be small, such that the self-heating is negligible [3, p. 363]. The small current will in the following be denoted sensing current, $I_{\mathrm{sense}}$.

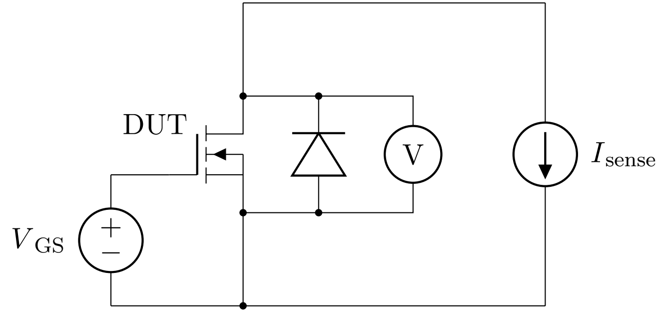



Figure 2.6: Schematic drawing of the $V_{\mathrm{SD}}(T)$-method.

To be able to utilize the $V_{\mathrm{SD}}(T)$-method, it is imperative that the sensing current only flows through the body diode. If a portion of the current flows through the channel instead, there is no way to guarantee a constant current through the diode, hence introducing an error in the temperature estimation. Considering the opposite temperature coefficients of the body diode and the MOSFET [34], their current sharing will differ under differing temperatures, thereby yielding an additional source of error. Finally, if a threshold voltage drift were to occur, the voltage drop across the channel would also change, thereby leaving the method unsuitable for use with SiC MOSFETs.

Thus, it is evident that the channel must be completely closed to use this TSEP. In SiC MOSFETs, that is not the case at $V_{\mathrm{GS}} = 0\,\mathrm{V}$ while the body diode is forward biased [18]. Therefore, a lower gate-source voltage is needed to ensure that the channel is completely closed under all operating conditions. This will be elaborated on in Section 4.3.

# Chapter 3

# Evaluation of Threshold Voltage Instability

Since the utilization of several TSEPs necessitate a stable threshold voltage, it was decided to investigate the threshold voltage instability further. Firstly, in order to gain a deeper understanding of the phenomena, and secondly to evaluate the magnitude of the drift that could be expected. Therefore, a test bench for evaluating the instability was built. The following chapter briefly discusses the set-up, including some of the results from the tests.

## 3.1 Threshold Voltage Instability Test Set-Up

The test itself is rather simple, but due to the drift being dependent on time, it was decided to build an automatic set-up. The threshold voltage is consequently measured with a known delay after the test has completed. This minimizes the associated measurement error between samples. The final test bench for testing the threshold voltage instability is seen in fig. 3.1.

### 3.1.1 Principles of the Test

The test-bench is capable of performing two functions. The first is to apply a gate-source bias, whereas the second is to measure the threshold voltage. Before a test commenced, the threshold voltage was characterized, in order to evaluate if any drift occurred. Then, the gate was biased for 66 hours, before the measurement of the threshold voltage was repeated directly after completion of the test. The duration of the test was chosen long enough such that drift could be expected, according to similar tests performed in the literature [27, 15]. Finally, the threshold voltage was also measured one hour after the test completion.

Characterizing the threshold voltage can be done in several ways, but due

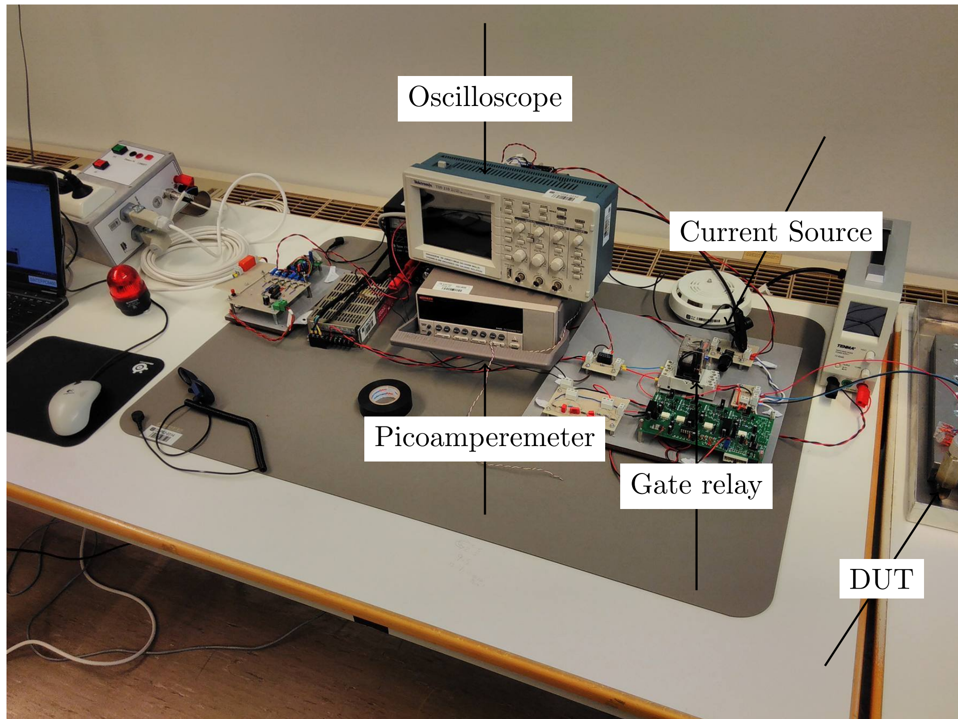



Figure 3.1: Set-up for testing threshold voltage instability

to its simplicity, the constant current method was chosen [36]. A schematic diagram of the method is shown in fig. 3.2. As seen in the figure, the drain-gate terminals are short circuited, while a constant current is run through the drain terminal. The measured $V_{\text{DS}} = V_{\text{GS}}$ is defined as the threshold voltage, $V_{\text{GS(th)}}$. The value of $I_{\text{cc}}$ can be chosen somewhat arbitrarily [36]. For this test, $I_{\text{cc}} = 300\,\mu\text{A}$ was utilized, in accordance with [15].

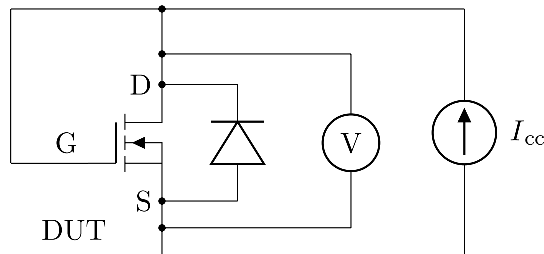



Figure 3.2: Constant Current method for measuring threshold voltage

Following the characterization, the experiment consisted of two parts: a stress mode and a measure mode. In the stress mode, a constant voltage was applied to the gate, with the drain-source terminals shorted. Figure

3.3 summarizes the electric circuit. After completion of this mode, the experiment entered into measure mode, in which the constant current method was again utilized in order to evaluate the threshold voltage. The test was always performed at room temperature.

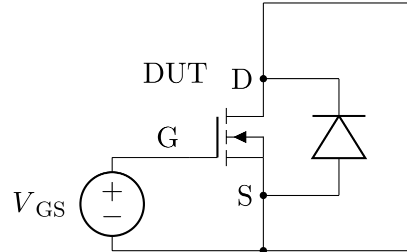



Figure 3.3: Electric circuit of stress mode.

### 3.1.2 Test Bench

A simplified schematic of the test bench circuit is shown in fig. 3.4. The addition of the relay at the gate terminal enabled switching between the stress and measure mode if the switch was in the lower or upper position, respectively. Adding the gate relay to the circuit ensured that the timing between the stress and measure modes stayed consistent between experiments. This made it easier to compare the threshold voltage drift between different samples. Moreover, the measurements directly after the test completed clearly identified the effect of the initial drift.

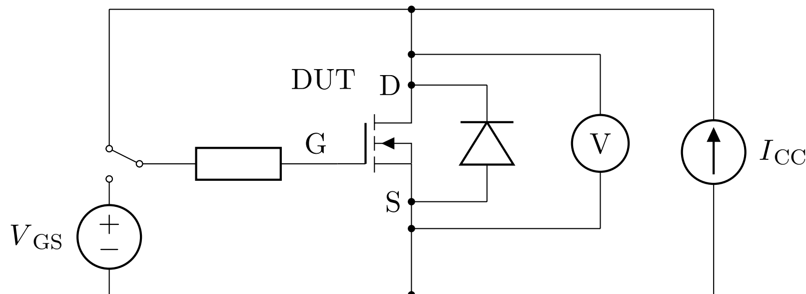



Figure 3.4: Test set-up for threshold voltage instability testing

The measurement of the threshold voltage commenced 37 ms after completion of the stress mode. This relatively long delay was necessary to ensure that the gate relay had switched. Moreover, due to the application of a gate bias, there would be a corresponding charge on the gate capacitances. This charge had to be removed before measuring the drain-source voltage, to ensure that only the threshold voltage was measured.

The measurements were then taken over a longer period of time, since trapping and de-trapping effects still are present some time after removal of the gate-source voltage [27]. Therefore, the measurement was performed directly after the test, in addition to one hour afterwards.

### 3.1.3 Current Source

Due to the temperature dependency of the threshold voltage, it was decided to try to minimize the error from the temperature dependency of other parts of the test. In particular, the current source was configured to have a temperature coefficient as close as possible to zero, according to its datasheet recommendation. The utilized current source was based on a LM334 current source from Texas Instruments. In addition, a potentiometer was added to the circuit to be able to slightly modify the output current. This way, the desired 300 µA could always be obtained. The current was measured with a picoamperemeter, to ensure an accurate output current.

During the application of positive bias, the constant current ran through the DUT, since the channel was open. Due to its very low value, it was assumed not to affect the test. However, when a negative bias was applied, the channel was closed, and hence, the constant current had nowhere to flow. In order to circumvent this issue, a drain-source short was added during negative bias to the circuit in fig. 3.4. This was removed just before entering measure mode to enable measurement of the threshold voltage.

### 3.1.4 Temperature Dependency

The threshold voltage of the MOSFET has a strong negative temperature coefficient [18]. Thus, when the temperature increases, the threshold voltage decreases. Therefore, the pre-characterization and the actual test should ideally be performed at the same temperature, such that the measured threshold voltage is only influenced by any potential change due to drift of the threshold voltage.

All measurements were performed at room temperature. The case temperature of the DUT was measured during the tests, and was found to be very constant; the temperature during measurements was always at 22 °C ±1 °C. Due to the small temperature differences, it was not taken into account when processing the results. As shown in the next section, the drift of the threshold voltage was so substantial that the measurements showed the expected trend anyway. However, an improvement of the measurement set-up would be to place the device on a controllable hot plate, such that a stable temperature could be expected for all tests.

## 3.2 Evaluation of the $V_{GS(th)}$ Instability

The test objects used in the set-up were the SCT2080KE SiC MOSFETs from Rohm. These are second generation devices, from the time when Rohm manufactured planar devices. The reason for choosing a second generation device, was that the observed drift was assumed to be larger. Since the purpose of the test was to gain experience in how the threshold voltage could be tested, this was found to be suitable.

The following subsections describe the results of two test objects that are representative of the other tested devices.

### 3.2.1 Test Object 2

The first test object that was properly tested was TO2. The device was stressed according to the parameters given in Table 3.1. The device was thus tested at its maximum rated gate-source voltage.

Table 3.1: Test Description for TO2

| $V_{GS}$ | Temperature | Test Duration |
|---|---|---|
| 22 V | 22 °C | 66 h |

Before the test, the threshold voltage was $V_{GS} = 2.14$ V. Then, directly following the test, the threshold voltage was as seen in fig. 3.5.

Figure 3.5: Threshold voltage of TO2 directly after test

The figure clearly shows that the threshold voltage is the largest directly after the test, being about 20% higher than the before the test value. Clearly, there is a rapid initial reduction in the threshold voltage. Considerable noise is present in the figure. This came as a result of the low sampling frequency. Ideally, the sampling frequency should have been much higher, and in particular, higher than 50 Hz such that a large portion of the AC noise would be removed. When measured again one hour after the completion of the test, the threshold voltage was 2.32 V.

### 3.2.2 Test Object 3

TO3 was biased equally long as TO2, but with the maximum rated negative bias. The test conditions are repeated in Table 3.2.

Table 3.2: Test Description for TO3

| $V_{\mathrm{GS}}$ | Temperature | Test Duration |
|---|---|---|
| −6 V | 23 °C | 66 h |

The threshold voltage before the test was found to be $V_{\mathrm{GS(th)}} = 2.15\,\mathrm{V}$. The development of the threshold voltage directly after the test is shown in fig. 3.6.

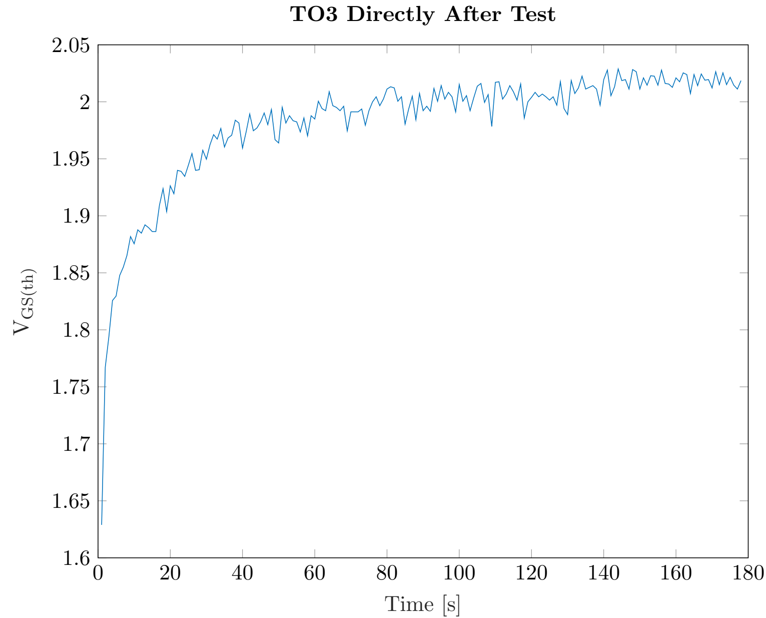



Figure 3.6: Threshold voltage of TO3 directly after test

The figure shows that the threshold voltage was drastically reduced as a result of the test. However, directly after completion, the threshold voltage

recovered quickly, reaching $V_{\mathrm{GS(th)}} = 2\,\mathrm{V}$ within the first two minutes after the test was completed. One hour after the test completion, the threshold voltage was $V_{\mathrm{GS(th)}} = 2.08\,\mathrm{V}$, meaning that it had almost recovered to the pre-stress value.

## 3.3 Conclusions and Possible Improvements

The number of tested devices are far too few in order to have any statistical significance. Thus, it is hard to draw any conclusions based on the experiment. However, the obtained results do support other findings in the literature. In particular, the results clearly show that the direction of the drift is the same as the applied bias. Moreover, the results also indicate that the drift is largest initially, i.e. directly following the removal of the gate bias.

The current set-up contains some uncertainties that should be dealt with if further testing is desirable. In particular, keeping the temperature of the DUT stable would reduce the uncertainty in the results, as the temperature dependency of the threshold voltage would be cancelled. Furthermore, this improvement would make it easier to compare tests of different devices. However, with the very low temperature deviations during the measurement of the threshold voltage, this probably did not affect the results significantly. Including control of the DUT temperature would eliminate this uncertainty.

Another possible improvement of the set-up, would be to increase the measurement sample rate. There exists considerable electrical noise around the circuit, which to a larger degree could be eliminated by applying a filter. However, the results clearly show the expected behavior of an initial reduction (increase) directly after removal of positive (negative) bias.

Finally, performing the test with differing durations of the stress mode would be beneficial in evaluating how fast the drift occurs. Moreover, the influence of temperature on the drift is yet to be understood [27], and hence, performing the experiment at different temperatures could also be valuable.

# Chapter 4

# Power Cycling

Power cycling tests are widely used in order to quantify the reliability of the packaging of power semiconductor devices. As such, the tests have also been used for assessing lifetime of devices [4]. It is therefore a suitable test for comparing reliability of new devices, such as SiC MOSFETs, to that of conventional silicon devices. However, there is little published results on power cycling of SiC MOSFETs, with only three articles published up until 2016 [37]. On the other hand, the methodology for performing power cycling of SiC MOSFETs has been somewhat debated [4]. The following will therefore present a brief review on how power cycling is done for silicon devices, before the specific challenges of power cycling SiC MOSFETs will be discussed.

## 4.1 Accelerated Power Cycling Test

The general idea of an accelerated power cycling test is to let the DUT heat up and cool down repeatedly. The device is actively heated, meaning that the device is self heated by power dissipation due to a load current being conducted through the device. The cycling of the power leads to a cycling of the temperature as well, which, depending on the length of the current pulse, leads to a temperature gradient inside the package [4]; short pulses tend to stress the upper layers more, whereas longer pulses leads to elevated stress on the lower and interconnecting layers, such as the solder layers. This causes mechanical stress on the component due to differing CTEs, which eventually leads to fatigue of the package and the end of the test [3, p. 391]. Figure 4.1 summarizes one cycle of a power cycling test as experienced by the DUT.

As seen in the figure, the load current is flowing through the device until the time $T_{\mathrm{on}}$ is reached. Up until this point, both the junction temperature $T_{\mathrm{j}}$ and the case temperature $T_{\mathrm{c}}$ have increased. After the current through the DUT is switched off at $T_{\mathrm{on}}$, $T_{\mathrm{c}}$ and $T_{\mathrm{j}}$ decreases. After a time $T_{\mathrm{off}}$, the

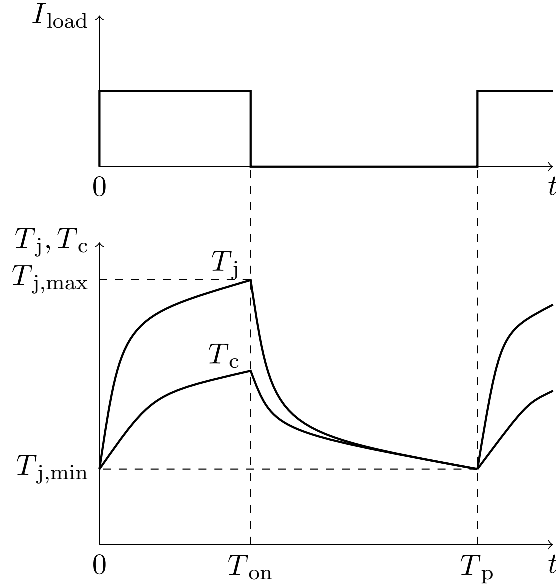



Figure 4.1: Power cycling procedure [4]

minimum junction temperature is reached, thereby concluding one period $T_\text{p}$. Generally, one cycle is much longer than normal switching periods in order to obtain the desired maximum junction temperature.

One of the characteristic parameters for a power cycling test is the temperature swing $\Delta T_\text{j}$, which is given by the difference between the maximum junction temperature $T_{\text{j,max}}$ and the minimum junction temperature $T_{\text{j,min}}$ [3, p. 391]:

$$\Delta T_\text{j} = T_{\text{j,max}} - T_{\text{j,min}}. \tag{4.1}$$

Larger temperature swing significantly increases the stress level of the test[5]. There are also several other factors contributing to determining the stress level of the test. One of these is $T_{\text{j,min}}$ [3, p. 391], while another is the duration of one period. Longer periods are considered to cause higher stress on the device.

There exists different ways of controlling power cycling tests, such as having constant on- and off-times, constant power losses or a constant temperature swing. The first is both the most severe option, but moreover the most application specific [37]. This will therefore be used in the tests.

The number of cycles to failure, $N_\text{f}$, quantifies how many cycles a device lasts before being worn out. Given a predetermined stress level, it is one of the most important outcomes of a power cycling test. Therefore, it is imperative that there be a consistent way of determining when failure occurs. This is achieved by monitoring several device parameters.

During the test, two parameters are monitored in particular. The first is the on-state voltage drop of the DUT, and the other is the thermal resistance. The latter is defined as

$$R_{\text{th}} = \frac{T_{\text{j}} - T_{\text{c}}}{P_{\text{V}}}, \tag{4.2}$$

where $P_{\text{V}}$ is the power dissipated in the device. For shorter power pulses, the measured $R_{\text{th}}$ is not necessarily equal to the actual steady state value. However, for monitoring purposes, it suffices to use this estimated value as it still provides the relative change that the DUT experiences [3, p. 391]. Monitoring these values allows determining whether failure of the device has occurred, according to the following failure criteria [3, p. 392]:

- Increase in the on-state voltage drop by 5 %.
- Increase in the thermal resistance by 20 %.
- Failure of any device function, e.g. blocking capability.

A sudden increase in the on-state voltage drop might indicate a bond-wire lift off, whereas gradual increase in the thermal resistance indicates that the packaging has degraded, typically due to solder fatigue. However, these two effects are dependent on each other, making it difficult to determine the primary underlying failure mechanism solely based on measured values. Thus, in order to evaluate why fatigue has taken place, further failure analysis should ideally be performed [3, p. 392]. This could for example be performed by scanning acoustic microscopy (SAM).

## 4.2 Lifetime Estimation Based on Power Cycling

As already mentioned, power cycling tests can be used in order to evaluate the lifetime of a device. There has been done several attempts of doing this, such as the Lesit project and the CIPS 08 model. The former of these established an equation relating $N_{\text{f}}$ to $\Delta T$ and the medium temperature of the test, given as $T_{\text{m}} = T_{\text{vj,min}} + \frac{T_{\text{vj,max}} - T_{\text{vj,min}}}{2}$. The project used standard modules from several different manufacturers, arguing that these are largely similar to each other, in order to establish the equation. The result of the test are summarized in fig. 4.2 [5].

The results clearly indicate the dependency of the number of cycles to failure on the temperature swing and the medium temperature. Because the medium and minimum temperatures are related by the temperature swing, one can also conclude that the lifetime of a device decreases with increasing minimum temperature. Since the experiment was conducted during the 1990s, module technologies have improved quite significantly, leaving the equation itself outdated [3, p. 393].

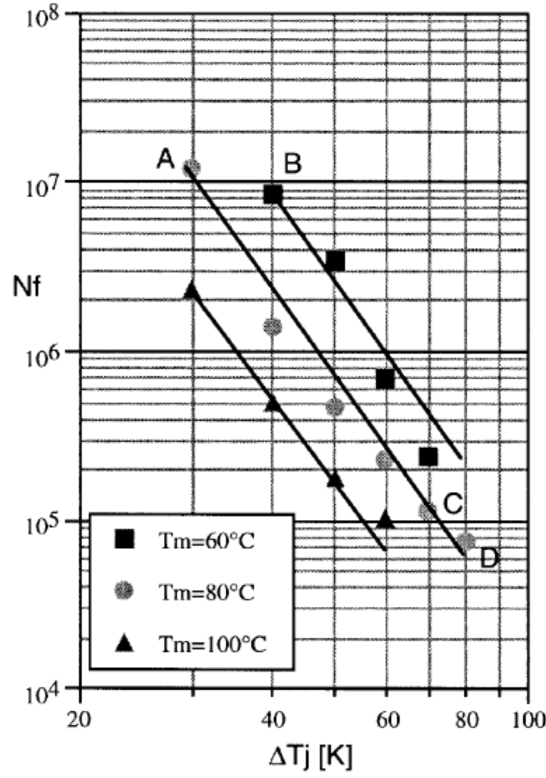



Figure 4.2: Results from the LESIT project [5]

Another approach was taken in the CIPS 08 model, in which a purely statistical analysis of a large number of power cycling results was performed [38]. The exact formula is only applicable to standard silicon modules with $Al_2O_3$ substrates [3, p. 396], however, the equation highlights factors contributing to failure of devices. The CIPS 08 equation is given by:

$$N_{\mathrm{f}} = K \cdot \Delta T_{\mathrm{j}}{}^{-4.416} \cdot \exp(\frac{1285}{T_{\mathrm{j,min}}}) \cdot T_{\mathrm{on}}{}^{-0.463} \cdot I_{\mathrm{load}}{}^{-0.716} \cdot V^{-0.761} \cdot D^{-0.5}, \quad (4.3)$$

where, in addition to previously defined parameters, K is a constant, V is the voltage rating of the device given as V/100, and D is the diameter of the bond wires. It is evident from the equation that increasing temperature swing or minimum temperature both contribute to reduced lifetime of the device. Likewise, longer on-time also contributes to reduced lifetime, as does higher load currents. The voltage ratings of the device reflects the thickness of the device, and thicker devices also contribute to reduced lifetime. Furthermore, thicker bond wires cause larger mechanical stress [3, p. 397].

## 4.3 Power Cycling of SiC MOSFETs

With the general procedure of power cycling in mind, the particularities of power cycling tests with SiC MOSFET can be introduced. As mentioned in Section 2.5.1, the virtual junction temperature may be estimated by the use of the $V_{\mathrm{SD}}(T)$-method. Provided that the channel is not conducting any current, this method is not affected by the threshold voltage instability, and is thus applicable for estimating the virtual junction temperature [18].

According to Herold et. al, the reason for the channel being slightly on at $V_{\mathrm{GS}} = 0\,\mathrm{V}$ while a current is driven through the source-drain terminals is that the voltage drop across the internal body diode is in the range of the device threshold voltage [18]. If applying a sufficient negative gate bias, however, the channel is completely off. In the article, they find that the channel is completely closed for a gate-source voltage of $V_{\mathrm{GS}} = -6\,\mathrm{V}$ [18]. Thus, with a gate-source voltage of $-6\,\mathrm{V}$ or lower, the $V_{\mathrm{SD}}(T)$-method may be utilized, for that particular device.

It is worth noting, however, that due to the potentially differing gate structure layouts between SiC MOSFET manufacturers, the value at which the channel is closed may vary. Before utilizing the $V_{\mathrm{SD}}(T)$-method with a specific SiC MOSFET, it is therefore necessary to determine when the channel turns off, such that an appropriate gate-source voltage can be applied.

Moreover, if a negative drift of the threshold voltage were to occur, the channel would start to conduct at a lower gate-source voltage, which might potentially necessitate a further reduction in $V_{\mathrm{GS}}$ in order to use the method. Hence, a considerable margin in the applied $V_{\mathrm{GS}}$ ought to be utilized, to ensure that the method is applicable even in the event of drift. If for example it is found that the channel is completely off at $V_{\mathrm{GS}} = -6\,\mathrm{V}$, one should utilize an even lower gate-source voltage.

In order to evaluate when the channel is completely closed for the DUT in this master's thesis, a curve tracer could be utilized [18]. As this was not at hand, another approach needed to be taken.

Recall that there is a linear relationship between the voltage across a pn-junction and the temperature at the same junction for a given current. Thus, once the channel is completely closed, the slope of $V_{\mathrm{SD}}(T)$ is constant. Moreover, any further reduction in the gate-source voltage will not contribute to a change in the $V_{\mathrm{SD}}(T)$ relationship. In other words, given $\{V_{\mathrm{GS}_1}, V_{\mathrm{GS}_2}\} < V_{\mathrm{GS}_{\mathrm{min}}}$, where $V_{\mathrm{GS}_1} \neq V_{\mathrm{GS}_2}$ and $V_{\mathrm{GS}_{\mathrm{min}}}$ is the minimum gate-source voltage that closes the channel, the following is true

$$\frac{\partial V_{\mathrm{SD}}(T)}{\partial T}\bigg|_{V_{\mathrm{GS}}=V_{\mathrm{GS}_1}} = \frac{\partial V_{\mathrm{SD}}(T)}{\partial T}\bigg|_{V_{\mathrm{GS}}=V_{\mathrm{GS}_2}}. \tag{4.4}$$

In order to find the gate-source voltage at which the channel is turned off, the circuit in fig. 4.3 was used. By keeping $I_{\mathrm{sense}}$ constant and measuring $V_{\mathrm{SD}}$ of the DUT subject to differing gate-source voltages and junction tem-

peratures, it was thus possible to determine at what gate voltage the channel was completely closed. Furthermore, the experiment was conducted for several different case temperatures. This was achieved by placing the DUT onto a hot plate with a controllable temperature; by waiting until the temperature of the case had stabilized, the temperature distribution of the device was assumed to be homogeneous. In particular, the temperature of the SiC die was assumed to be equal that of the package.

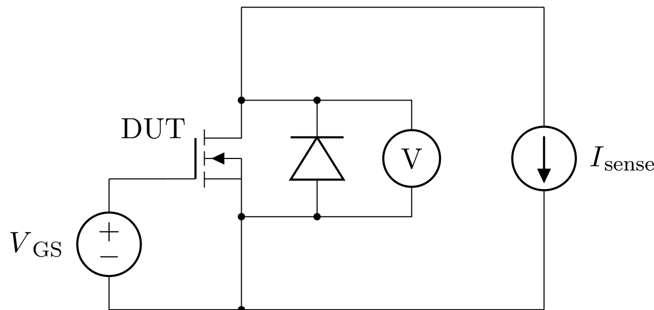



Figure 4.3: Schematic drawing of $V_{\mathrm{SD}}(T)$-method.

The test was carried out on SiC MOSFETs from Cree, in particular the third generation device C3M0075120K. For all the tests, the sensing current was set to 28.2 mA. This value was chosen somewhat arbitrarily, however ensuring that the self-heating of the device was negligible. This was assumed since the rated continuous diode forward current for the device is 22.4 A, i.e. almost three orders of magnitude larger.

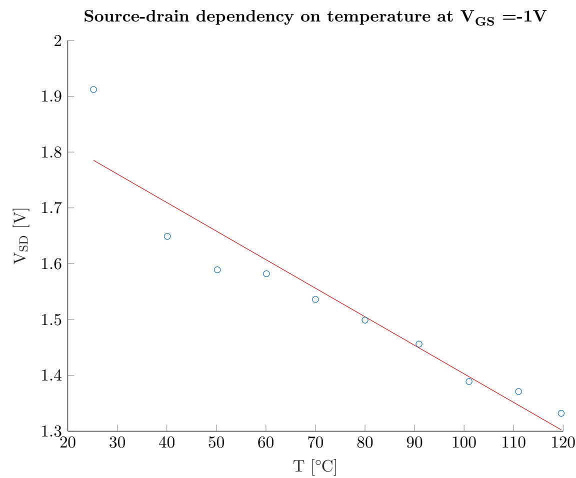



Figure 4.4: Test of whether channel is closed at $V_{\mathrm{GS}} = -1\,\mathrm{V}$

A sample result is shown in fig. 4.4, in which the gate-source voltage is set to $V_{\mathrm{GS}} = -1\,\mathrm{V}$. The circles indicate the measured values, whereas the

line is a best fit obtained by the linear least square method in MATLAB. It is evident from the figure that there is not a linear relationship between the voltage across the device and the temperature. Thus, the channel is not completely closed for this gate-source voltage.

Figure 4.5 plots the above result together with the corresponding one for $V_{\mathrm{GS}} = -8\,\mathrm{V}$. Clearly, the linear fit is significantly better for the latter, indicating that the channel is completely closed for this gate-source voltage. Moreover, it can be noted that the source-drain voltage is significantly lower for $V_{\mathrm{GS}} = -1\,\mathrm{V}$. This is due to the electrically parallel path that exists for the current, as it may flow over the channel in this case.

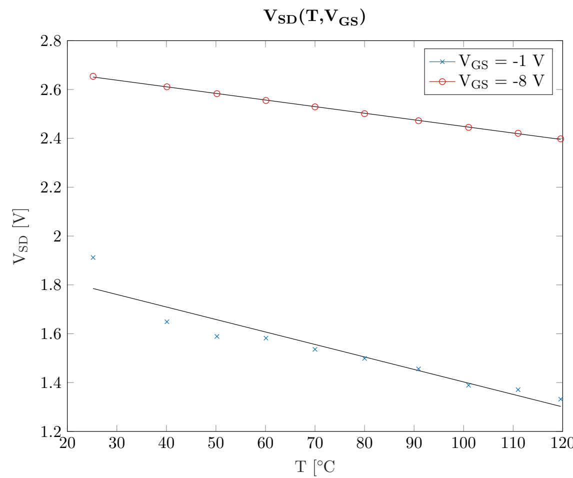



Figure 4.5: Test of whether channel is closed at different gate voltages

As stated by equation 4.4, the criteria for the channel being closed is that the fitted lines have identical slopes for a gate-source voltage less than some particular threshold voltage. Thus, the following criteria must be satisfied in order to have completely closed the channel:

$$\frac{\partial}{\partial V_{\mathrm{GS}}}\left(\frac{\partial V_{\mathrm{SD}}(T)}{\partial T}\right) = 0. \qquad (4.5)$$

To evaluate this, consider fig. 4.6, in which $\frac{\partial V_{\mathrm{SD}}(T)}{\partial T}$ is plotted against $V_{\mathrm{GS}}$. Clearly, the derivative of the curve is zero only for values of $V_{\mathrm{GS}} < -6.5\,\mathrm{V}$. Hence, this is the maximum $V_{\mathrm{GS}}$ that may be utilized in order to ensure that the channel is completely closed for this particular device.

As discussed further in Section 5.1, the DUT has a minimum switching frequency of 1 Hz when utilizing $V_{\mathrm{GS}} = -8\,\mathrm{V}$. The previously described test was carried out without respecting this limit of switching sufficiently fast. It is unclear why this switching constraint is posed, yet one option might be that it is to reduce the threshold voltage drift. Either way, it is likely that a shift of the threshold voltage towards lower values occurred due to

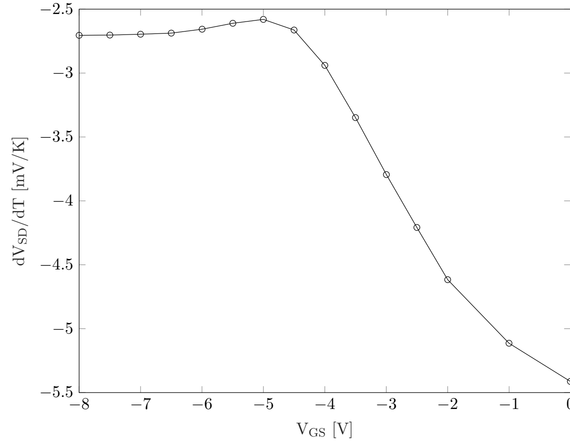



Figure 4.6: Slope of $V_{\mathrm{SD}}(T)$ plotted against $V_{\mathrm{GS}}$

the negative bias applied over time. If this was the case it may have caused the channel to turn off at a lower value of $V_{\mathrm{GS}}$ than what would have been the case otherwise.

Therefore, concluding that $V_{\mathrm{GS}} < -6.5\,\mathrm{V}$ completely closes the channel may be a sufficient, but not necessary condition; the channel may actually be turned off for a higher gate source value. However, it is more important that the channel is completely turned off than utilizing a lower gate-source voltage, and therefore a considerable margin in $V_{\mathrm{GS}}$ ought to be used. As such, the potential drift that may have occurred did not falsify the test results.

Since the maximum negative rating for the device is $V_{\mathrm{GS}} = -8\,\mathrm{V}$, this was chosen to be the value of $V_{\mathrm{GS}}$ in the off-state. Thus, if a threshold voltage drift toward lower values were to occur during an experiment, a margin was kept to ensure that the channel stayed completely closed. Hence, $V_{\mathrm{GS}} = -8\,\mathrm{V}$ was the value used to accommodate use of the $V_{\mathrm{SD}}(T)$-method during power cycling.

# Chapter 5

# Power Cycling Test Rig

This chapter will describe the test rig that was developed for performing power cycling on SiC MOSFETs, in addition to the developed control and measurement system. Moreover, the electrical characterization tests that were performed on the devices under test are presented, as well as the operating points under which power cycling was performed.

## 5.1 Selection of Test Object

In evaluating both the methodology for performing power cycling, but also the power cycling lifetime itself of SiC MOSFETs, it seemed reasonable to use recent generation devices due to the rapid development that the technology is facing. It was desired to test modules, but these were not available. Therefore, it was concluded to use the Cree C3M0075120K, which is a third generation 1200 V device [39]. The device is shown in fig. 5.1.

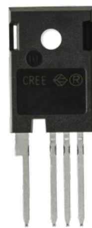



Figure 5.1: Cree C3M0075120K SiC MOSFET [6]

As seen in the picture, it is a discrete package. Some of the most important maximum and minimum ratings of the device at room temperature are repeated in Table 5.1 [40].

Of particular importance for this thesis are the rated values for the gate voltage, $V_{\mathrm{GS}}$. The device manufacturer has included a minimum switching frequency of 1 Hz when utilizing the maximum and minimum gate voltage

Table 5.1: Cree SiC MOSFET Maximum and Minimum Parameters

| Property | $V_{\mathrm{DS,max}}$ | $V_{\mathrm{GS}}$ (dynamic) | $V_{\mathrm{GS}}$ (static) | $I_{\mathrm{D}}$ | $T_{\mathrm{j}}$ |
|---|---|---|---|---|---|
| Value | 1200 V | −8/19 V ($f > 1$ Hz) | −4/15 V | 30 A | 150 °C |

ratings. Why this restriction is posed, is as mentioned unclear, yet it is suspected to have to do with limiting the threshold voltage drift. Since it was found in Section 4.3 that $V_{\mathrm{GS}} < -6.5$ V was a sufficient condition for utilizing the $V_{\mathrm{SD}}(T)$-method, the device ought to be switched at 1 Hz minimum, according to the datasheet. As will be explained later, however, it was not possible to keep this restriction while at the same time obtaining the desired $\Delta T$.

## 5.2 Electric Circuit

As explained in Section 4.1, power cycling occurs by actively heating and cooling the DUT, by turning a load current through the device on and off repeatedly. A simplified view of the circuit used for this thesis is shown in fig. 5.2, which accomplishes the mentioned task.

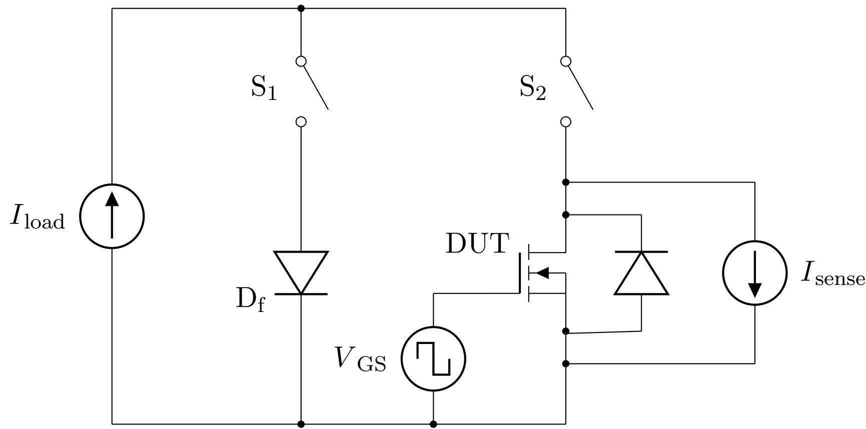



Figure 5.2: Electrical circuit for performing power cycling of SiC MOSFET

The load current $I_{\mathrm{load}}$ is cycled between the two branches. The current path is controlled by the switches $S_1$ and $S_2$. When $I_{\mathrm{load}}$ flows through the rightmost branch, the DUT heats up, whereas it cools down otherwise. When the DUT is cooling down, the current flows in the bypass branch, which contains the diode $D_f$. On the far right in fig. 5.2 is the sensing current source $I_{\mathrm{sense}}$, which enables the estimation of the virtual junction temperature according to the $V_{\mathrm{SD}}(T)$-method described in chapter 2.5.1.

The purpose of the switches $S_1$ and $S_2$ is solely to switch the load current

between the two branches, and will therefore in the following be termed auxiliary switches. Since it is not desired that the auxiliary switches degrade during the testing, their current capability is large; in the real test bench, both $S_1$ and $S_2$ consist of four parallel MOSFETs. Their rated current is 120 A each, resulting in a combined current capability of more than 10 times the rated value of the DUT. This substantially reduces the cycling of these components as it reduces the power dissipated in each MOSFET.

The load current source is shown in fig. 5.3. The rated values of the source is 30 A and 1500 V. Due to the fact that the voltage requirement of the load current source only consists of the on-state voltage of the devices (neglecting switching transients), the source was driven at far below its rated value.

Figure 5.3: Load current source

The function of the bypass diode is to ensure a similar voltage drop in both branches as seen by the load current source, in order to avoid cycling of the latter. This was an important feature of the previous set-up, due to the low power rating of the current source used in that set-up. However, in the present set-up, there is no danger of cycling the current source due to sufficiently large ratings compared to the power actually drawn during the test. After the first power cycling test, it was therefore decided to remove the bypass diode. This led to a larger voltage overshoot when switching the load current, but on the other hand substantially reduced the cooling needs of the rest of the circuit. In addition, the reverse recovery effect disappears with the diode, enabling shorter intermediate times during switching.

In order to use the SiC MOSFET body diode for estimating $T_{\mathrm{vj}}$, the DUT needs to be switched. That results in the timing diagram in fig. 5.4. The overlapping time where all switches are on is necessary in order to ensure a path for the load current to flow. These are exaggerated in the figure to highlight the switching sequence. Since the auxiliary switches, and not the

DUT, are meant to switch the load current, the DUT turns on before and turns off after $S_2$.

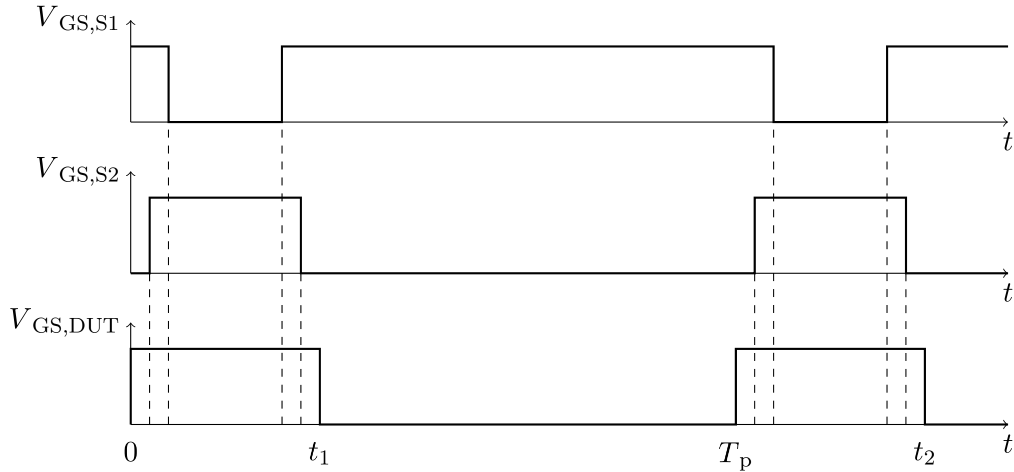



Figure 5.4: Timing diagram for power cycling

### 5.2.1 Sensing Current Source

A diagram of the sensing current source is shown in fig. 5.5. The current source delivers 28.2 mA, thereby contributing only negligibly to self-heating of the device, since the current is significantly smaller than the rated current. The voltage drop across the resistor $R_2$ is used to estimate the sensing current. This is a slightly modified version of the sensing current source which was used in the previous set-up, which will be explained in the following.

A drawback of the $V_{SD}(T)$-method is that the load current could flow through the sensing current branch. For an ideal current source, this is not a problem. However, the actual circuit has to ensure that the load current flows over the DUT only, by making sure that the voltage drop across the DUT is less than that of the alternative path through the current source branch. This was achieved by adding the diode $D_3$ to the circuit.

In fig. 5.5, the output labels S and D denote the DUT source and drain respectively. Since the load current flows from drain to source, it is evident that it has an alternative path over $D_3$, $R_2$, $D_1$ and $D_2$.

During testing, $V_{DS}$ reached values in the range of 3.5 V. Thus, the voltage drop between D and S of the sensing current branch needed to be more than 3.5 V in order to add some safety margin. Therefore, 5 signal diodes were added to the original current source. These are represented by the diode $D_3$ in the figure. This finally resulted in a combined voltage drop over $D_2$ and $D_3$ of roughly 5 V, thereby protecting the sensing current source.

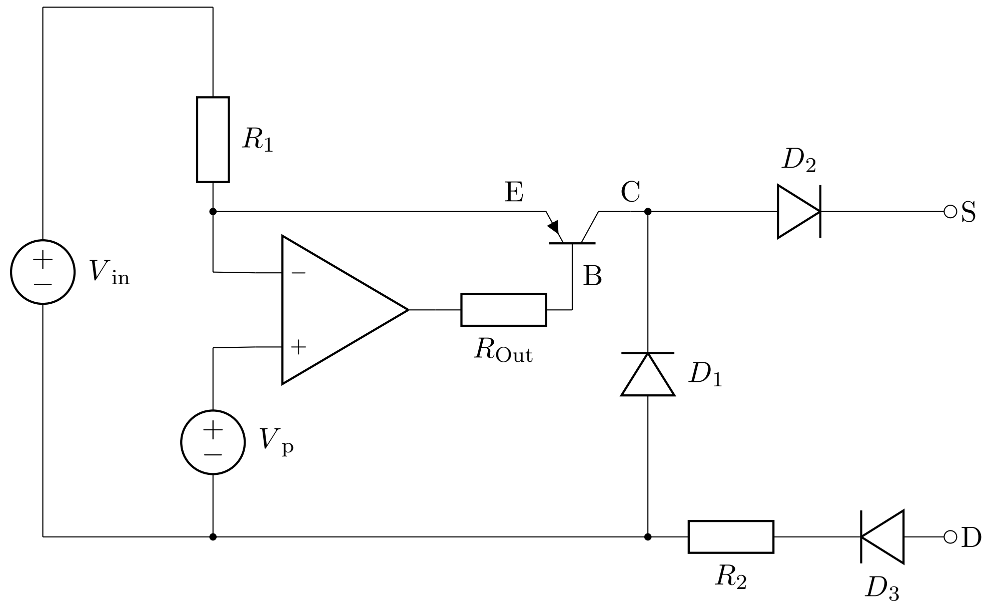



Figure 5.5: Simplified schematic diagram of the sensing current source

In the event of a drain-source voltage larger than this, the load current will flow over the sensing current source. The diode $D_1$ then serves to protect the rest of the circuit, as the load current will flow through this diode. $D_1$ has a low current capability, and will therefore be short circuited. This way, the remainder of the circuit can be protected, and only the diode has to be replaced.

### 5.2.2 DUT gate driver

As discussed in Section 4.3, it is imperative that the channel be completely turned off for estimating $T_{vj}$ by using the internal body diode. Therefore, the gate source voltage of the DUT needs to switch continuously, and more importantly, it needs to switch to sufficiently low values. As mentioned, the chosen negative gate-source voltage was $V_{GS} = -8\,V$.

Since the goal of the thesis was to investigate the methodology of power cycling, it was decided to use a driver already at hand that was rated at $+18\,V/-5\,V$ and modify it to get the desired negative gate voltage. The modification basically consisted of moving the voltage level of the source with respect to the gate driver. The drawback of this approach is the reduction of the positive bias gate voltage, thus leading to a larger on-state voltage than if nominal values of $V_{GS}$ were used. In particular, the device was therefore switched at $+15\,V/-8\,V$. This choice was justified by the fact that it allowed higher power losses for a given current, enabling use of a current source with a lower current capability. Moreover, since the literature on power cycling

SiC devices find solder fatigue to be one of the main issues [8, 18], a lower load current at the expense of a higher on-state voltage seemed justifiable, as this approach would stress the lower layers of the device more.

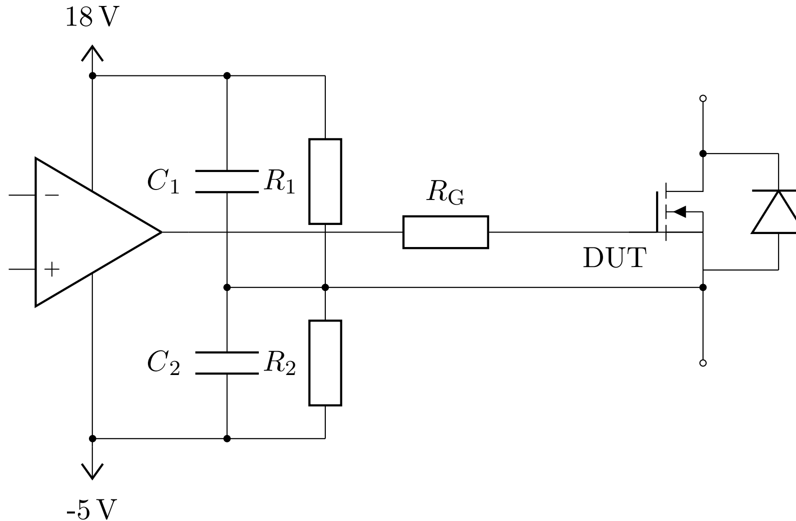



Figure 5.6: Simplified schematic diagram of the gate driver

Figure 5.6 presents how the output from the gate driver was changed in order to obtain the desired negative bias. In steady state, i.e. after the switching transients, the resistors $R_1$ and $R_2$ determine the level of the bridge midpoint. These are therefore chosen such that

$$\begin{aligned}(18\,\mathrm{V} - -5\,\mathrm{V}) \cdot \frac{R_2}{R_1 + R_2} &= 8\,\mathrm{V} \\ \frac{R_2}{R_1 + R_2} &= \frac{8}{23}.\end{aligned} \tag{5.1}$$

Moreover, in order to avoid a large steady state current through the bridge, the resistor values were set to $R_1 = 2.7\,\mathrm{k\Omega}$ and $4R_2 = 1.4\,\mathrm{k\Omega}$. The resulting negative bias was then $-7.8\,\mathrm{V}$.

Without the capacitors, the relatively large values of $R_1$ and $R_2$ would not only cause very slow switching, but also change the mid-point voltage level during switching transients. The purpose of the capacitors is thus to keep the mid-point voltage stable and enable fast switching. Their values were $1\,\mathrm{\mu F}$ each, thus almost three orders of magnitude larger than the DUT capacitances.

Finally, the gate resistor $R_G$ was chosen to enable relatively fast switching, while at the same time keeping ringing at the very minimum. Although it is desirable to sense $V_{SD}$ as fast as possible after turn-off of the DUT, there

needs to be a safety margin of some microseconds to ensure that the values that are measured not come from any non-temperature related electrical transient. In addition, due to the improvised solution for the gate driver leading to increased stray inductance, a relatively large value of the gate resistor was chosen to ensure that no ringing occurred. The final switching waveform for the DUT is seen in fig. 5.7. As seen, the device is switched in about 2 µs, without any ringing.

(a) Turn on

(b) Turn off

Figure 5.7: Switching waveforms of DUT

## 5.3 Control of Set-Up

### 5.3.1 Control Software

Both the control and measurement of the test set-up is performed by the graphical programming language LabVIEW from National Instruments (NI). The power cycling test is controlled by an FPGA (Field Programmable Gate Array), which in turn is controlled by a computer. Both of these run LabVIEW code, denoted VIs (Virtual Instruments). VIs may contain several subVIs, which, in addition to the programming language being graphical, makes documentation of the code difficult. However, a brief overview of the code will be presented in the following.

Any VI consists of a block diagram and a front panel. The block diagram is where the actual code is placed, whereas the front panel acts as a control panel for the user to interact with. The VI for the host computer will be referred to as the top level VI, which is the VI that sets the specific test parameters as entered by the user. These include amongst other the cycle duration, the duration of overlapping times and number of samples to read per measurement. This VI also monitors the measured values, and determines when the test is to be stopped according to the failure criteria given in Section 4.1. A portion of the front panel is displayed in figure 5.8.

The entire LabVIEW program was developed within the thesis. A portion of the top level block diagram is displayed in figure 5.9, in which the code for estimating the maximum and minimum junction temperature is displayed. The top level VI is organized as a state machine, which keeps

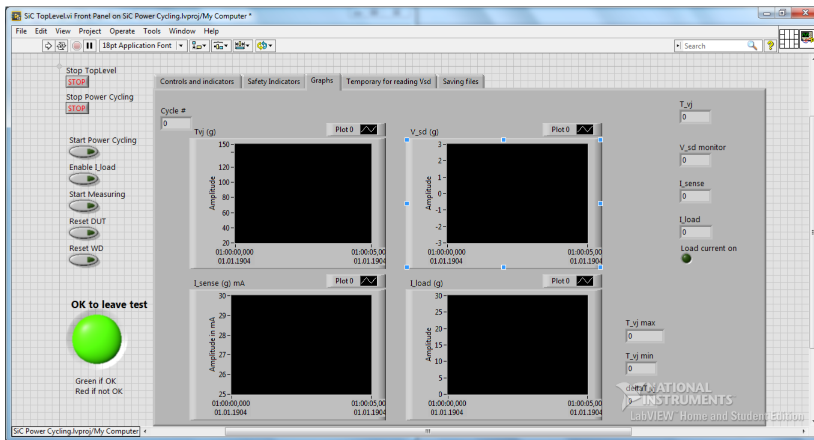



Figure 5.8: Front panel of top level VI

track of the current and the next switching state. A large portion of this VI is also made for reading and saving the measurement values that are obtained by the FPGA. The saved values are placed in a dropbox folder, thereby enabling remote monitoring.

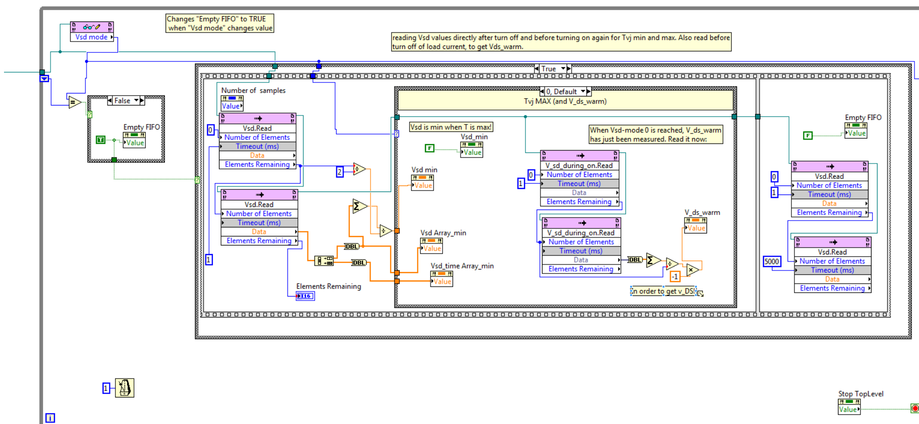


Figure 5.9: Block Diagram of top level VI

### 5.3.2 Control Hardware

The next step in the control is the control hardware. This consists of the cRIO 9076 FPGA from NI. The cRIO 9076 has room for four input/output modules, which are used for monitoring voltages and temperatures, in addition to controlling, respectively. The test set-up utilized the C-series module NI9205 for acquiring voltages, two pairs of NI9401 modules for controlling and reading the status signals from the gate drivers, as well as the NI9211

module for reading temperatures with thermocouples. One of the NI9401 modules is furthermore used to enable or disable the load current source, as well as providing a watchdog (WD) signal.

A separate VI is made for controlling the FPGA. This is written on the host computer and compiled to an executable code on the FPGA. Due to the 400 MHz processor of the FPGA, it has the capability of executing code much faster than the top level VI, and is therefore suitable for obtaining the high-speed measurements and high fidelity timing needed in the power cycling set-up. The top level VI then reads these values in larger portions by using a FIFO (First In First Out) queue, allowing the host computer to work on its normal processor speed.

Since the FPGA is capable of doing several tasks simultaneously, the FPGA VI is designed to run numerous tasks in parallel. This includes writing of various measurements to the top level VI, monitoring safe operation, in addition to controlling a state machine for performing the switching sequence.

One of the NI9205 C-series modules controls the gate signals for the auxiliary switches. In-between the two is the SINTEF Driver Interface Board, which also provides a fault indication to the FPGA. This board further controls the actual drivers for the auxiliary switches, which are called EFI SMD ver. 2 gate drivers.

The load current is measured by the current transducer LEM LA-205-S. It outputs a current with a ratio of 1:2000 to the actual current. The output current is estimated by measuring the voltage across a $100\,\Omega$ resistor. The sensing current is also estimated by the voltage drop across a $1\,\Omega$ resistor.

## 5.4 Safety Measures

Depending on the stress level of the test, a power cycling test may last anywhere from several days to several weeks. An important goal is therefore to let the test run without continuous supervision. This necessitates monitoring the test and adding safety measures that will trip the test if any undesired event takes place. This section will describe the different measures that have been taken in order to accommodate testing without continuous supervision. Figure 5.10 displays a simplified flow diagram for safe shutdown.

The top level VI monitors several values to ensure safe operation. These include the load current, the ambient temperature and the heat sink temperature for the auxiliary switches. If these values surpass a user-defined threshold, the top level trips. Furthermore, both the load and sensing currents have a defined range from their set-point values within which they are allowed to vary, due to measurement inaccuracies. If their instantaneous values are outside the allowed band, the top level trips. Short circuit and

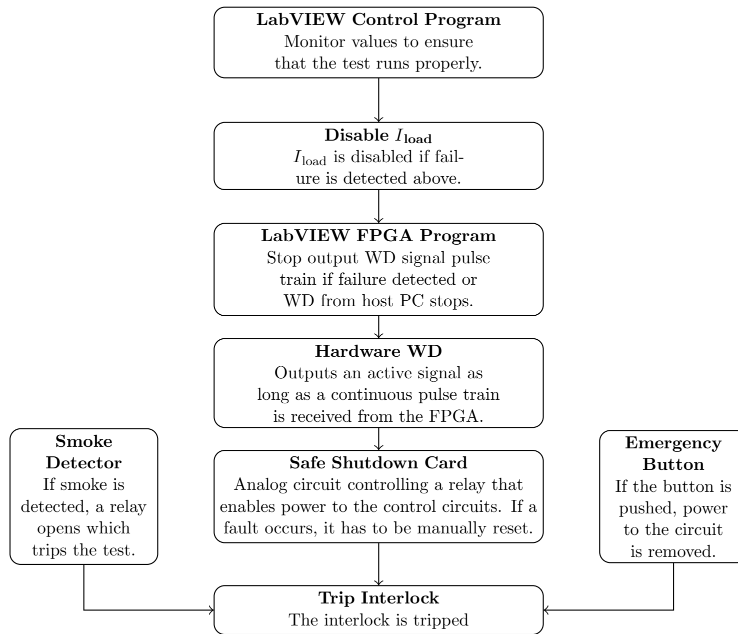



Figure 5.10: Safe shutdown flow diagram

open circuit are also detected by the top level. All drivers provide status signals, which are used to trip the test in the event of a failure of these. In addition, the failure criteria of the test as described in Section 4.1 also forces trip to occur.

The first thing that happens after the top level is tripped is that the load current is disabled. The FPGA VI then stops sending a pulse train to the hardware watchdog. This also occurs if a WD pulse train is not received at the FPGA VI from the top level VI.

The hardware WD outputs an active signal as long as the pulse train from the FPGA is received. This removes power from a safe shutdown card, which finally trips an interlock that controls the power supply to the test bench. The test can also be tripped directly by a smoke detector or a by pushing a stop button on the interlock.

Since the load current is considered to be the main hazard in the test set-up, it has two levels of safety measures to ensure safe operation. The current source is set up such that its DC output is blocked if two terminals are short circuited. Therefore, a normally-closed relay is placed in-between these terminals. The advantage of using the control circuit to trip the current source instead of the auxiliary switches is that the latter would cause a very large voltage overshoot due to the highly inductive power circuit. Moreover, the reliability of tripping the current source by means of the control circuit is also significantly higher, as there are several intermediate stages between the control program and the gate driver for the auxiliary switches.

The first level of safety measures is that the relay state is controlled by the top level VI, where a control for enabling the current source exists. If any fault is detected the DC output is blocked. If the control software were to freeze, leaving the enable signal high, the second level of control will disable the signal by removing the power to the relay, effectively forcing a short circuit between the two current source control terminals, thereby disabling the current source.

## 5.5 Electrical Characterization of Test Objects

Electrical characterization of test objects are done in order to evaluate the degradation of the DUT as a result of power cycling. Four different tests were performed both before and after each test. The conducted tests determined the threshold voltage $V_{\mathrm{GS(th)}}$, gate leakage current $I_{\mathrm{G,leak}}$, drain leakage current $I_{\mathrm{D,leak}}$ as well as the on-state characteristics $R_{\mathrm{DS,on}}(I_{\mathrm{D}})$.

### 5.5.1 Threshold Voltage Characterization

The threshold voltage $V_{\mathrm{GS(th)}}$ was measured using the constant current method, with a constant current of $I_{\mathrm{CC}} = 300\,\mu\mathrm{A}$. The corresponding circuit diagram is shown in fig. 5.11.

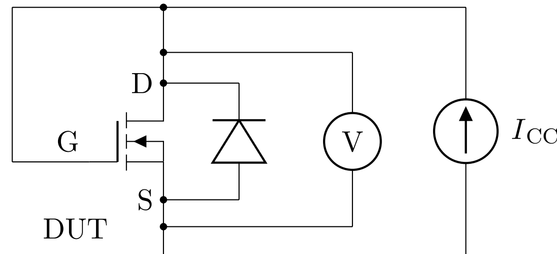



Figure 5.11: Schematic diagram for characterization of the threshold voltage

The equipment used in the experiment was

- Voltage Source: Mascot (B02-0397). For driving the current source.
- Picoammeter: Keithley 6485 (S02-0056). For ensuring 300 µA
- cRIO 9067 and C-series module NI9220. For measuring the threshold voltage.

### 5.5.2 Gate Leakage Current Characterization

The integrity of the gate oxide was checked by measuring the gate leakage current. This was done with the drain-source terminals short circuited.

Then, in accordance with the device datasheet, $V_{\mathrm{GS}} = 15\,\mathrm{V}$ was applied, and the gate current measured. Figure 5.12 summarizes the procedure.

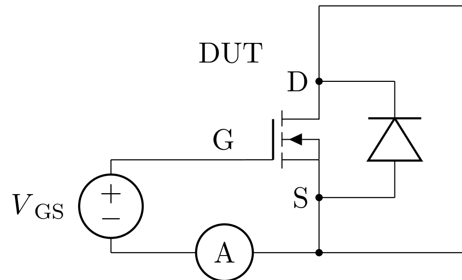



Figure 5.12: Schematic diagram for characterization of the gate leakage current

The equipment that was used in retrieving the gate leakage current was

- Voltage Source: Mascot (B02-0397).
- Multimeter: Fluke 177 (S03-0420). For ensuring $V_{\mathrm{GS}} = 15\,\mathrm{V}$
- Picoammeter: Keithley 6485 (S02-0056). For measuring the gate leakage current $I_{\mathrm{G,Leak}}$.

### 5.5.3 Blocking Voltage Characterization

The blocking voltage characterization was done by measuring the drain-source leakage current under rated drain-source voltage of $V_{\mathrm{DS}} = 1200\,\mathrm{V}$. The purpose of the test is to ensure that the device is capable of blocking the rated voltage, as well as characterizing the magnitude of the leakage current. The electrical diagram is shown in fig. 5.13.

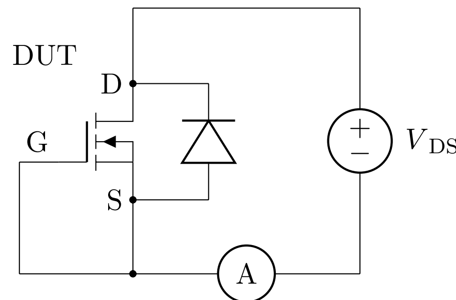



Figure 5.13: Schematic diagram for characterization of the blocking voltage

The equipment used for this characterization was

- Voltage Source: Glassman High Voltage Series EH (B01-0518).
- Multimeter: Fluke 175 (S03-0438). For ensuring $V_{\mathrm{DS}} = 1200\,\mathrm{V}$
- Picoammeter: Keithley 6485 (S02-0056). For measuring the leakage current $I_{\mathrm{D,Leak}}$.

### 5.5.4 On-State Voltage Characterization

The on-state voltage was characterized for differing drain currents $I_{\mathrm{D}}$ under $V_{\mathrm{GS}} = 15\,\mathrm{V}$. The electrical circuit for the test is shown in fig. 5.14

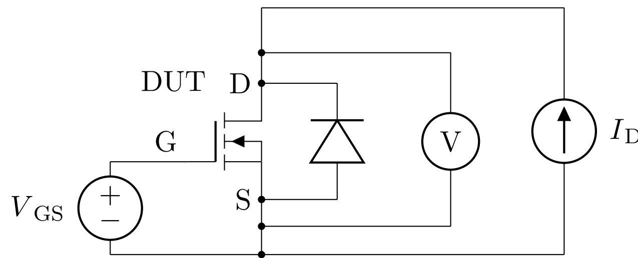



Figure 5.14: Schematic diagram for characterization of the on-state voltage

The equipment used for this characterization was

- Voltage Source: Mascot (B02-0397). For applying gate bias.
- Multimeter: Fluke 177 (S03-0420). For ensuring $V_{\mathrm{GS}} = 15\,\mathrm{V}$
- Current Source and Voltage Measurement: Schuster DM659. For applying $I_{\mathrm{D}}$ and measuring $V_{\mathrm{DS}}$.

## 5.6 Estimation of the Virtual Junction Temperature

As $T_{\mathrm{vj}}$ is one of the most important parameters of the power cycling test, it is crucial to estimate it in a satisfactory way. This section therefore shows how the $V_{\mathrm{SD}}(T)$-method was utilized to obtain the junction temperature.

### 5.6.1 Establishing a Calibration Curve

Firstly, the relationship between the temperature and source-drain voltage needed to be established for each test object. This relationship will be referred to as the calibration curve. The temperature of the DUT was controlled by a hot-plate. By waiting sufficiently long, the measured case temperature was assumed to equal that of the semiconductor chip.

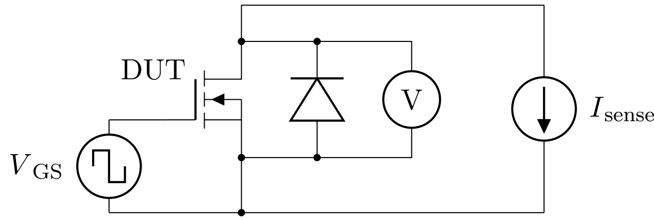



Figure 5.15: Schematic diagram of $V_{\text{SD}}(T)$-method.

The rest of the circuit used for calibration is depicted in fig. 5.15. The sensing current was set to 28.2 mA, while the gate-source voltage was switched continuously according to the datasheet. In particular, the negative voltage was −7.8 V to ensure that the channel was completely closed. The reason for switching the DUT was to remain within the datasheet limits, and hence the switching period was set to 1 s, with $T_{\text{on}} = T_{\text{off}} = 0.5$ s. The measured voltage was then related to the case temperature of the DUT as measured by the thermocouple.

An example of the measurement is given in figure 5.16. The points are the measured values, whereas the line is the best fit. As seen, the fitted line describes the measurements very accurately, and is given by

$$V_{\text{SD}}(T) = a \cdot T + b. \tag{5.2}$$

Thus, when the virtual junction temperature were to be estimated during power cycling, it could be found by evaluating

$$T_{\text{vj}} = \frac{V_{\text{SD}} - b}{a}. \tag{5.3}$$

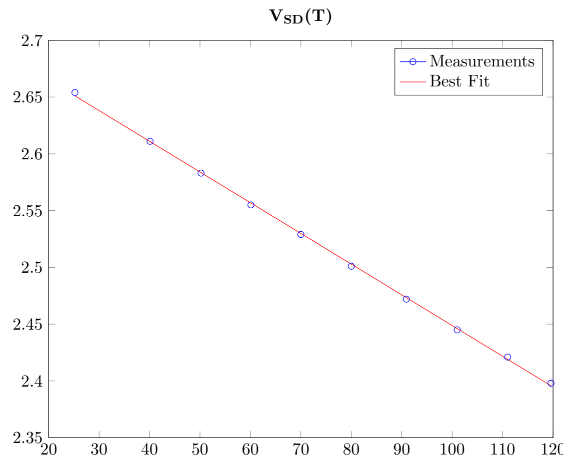



Figure 5.16: Calibration procedure with $V_{\text{SD}}$ plotted against temperature

### 5.6.2 Virtual Junction Temperature

Due to the fast initial thermal transients of the DUT, it was important to ensure a fast measurement and a high sampling rate of the source-drain voltage. In particular, the maximum and minimum junction temperatures were estimated by a large number of samples taken directly after the DUT turned off, and just before it turned on, respectively. This is shown in fig. 5.17. Also shown in the figure is the measurement of the on-state voltage in the warm state, $V_{\mathrm{DS,warm}}$, measured directly before turn-off of the DUT. This value is used to measure a change in the on-state voltage of the device.

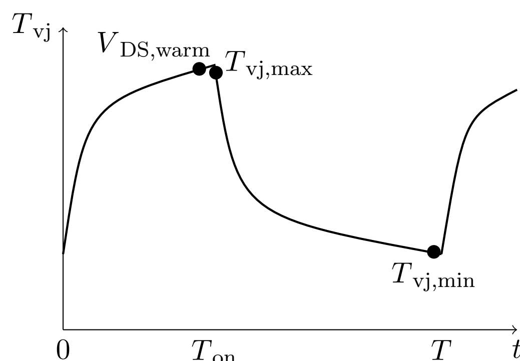



Figure 5.17: Points of measurement during power cycling

In order to perform these measurements the NI-9205 C-series module was utilized. This has a sampling frequency of 250 000 samples per second, implying a maximum sampling rate of 4 µs. However, these are the rated values for the combination of all the module channels, and since several channels were utilized for measuring other parameters, the effective sampling rate for measuring $V_{\mathrm{SD}}$ was considerably lower. More critically, however, the sharing of resources caused the measurements not to be equally spaced in time. Although the sampling rate of measurement is set to 8 µs, considerably longer periods elapsed between some of the measurements due to the sharing of resources.

A dead time exists between when the DUT is carrying the full load current and when the virtual junction temperature is estimated. This is partially caused by a delay set by the control system in order to ensure that the actual temperature phenomena is measured, yet it also comes from the necessity of an overlapping time between the switches, according to fig. 5.4. Thus, the dead time is inevitable. The associated practical implication is that the estimated temperature is somewhat lower than it is exactly when the current through the DUT is turned off.

The error in $T_{\mathrm{vj,max}}$ that is caused by this delay is not very large, however it is clearly present. In the current set-up, the time between when the DUT

carries the full load current and the virtual junction temperature is estimated is 70 µs.

## 5.7 Device Operating Points

As described in Section 4.1, the higher $\Delta T_{\mathrm{vj}}$, the higher the stress level on the device. The degrees of freedom in choosing the stress level of the test is the load current magnitude, the on- and off-times of the DUT as well as the minimum temperature, which is controlled by controlling the heat sink temperature. Higher stress levels leads to sooner fatigue of the DUT.

Since the goal of this thesis mainly was to evaluate the methodology for power cycling with SiC MOSFETs, a relatively high stress level was chosen, corresponding to $\Delta T_{\mathrm{vj}} = 80\,^{\circ}\mathrm{C}$. Elevated stress leads to tests of shorter duration, thereby allowing for several tests to be performed in a relatively short time span. However, it was important that the maximum junction temperature $T_{\mathrm{j,max}}$ stayed below the maximum junction temperature as specified in the datasheet of $150\,^{\circ}\mathrm{C}$. Considering that the semiconductor chip may have large lateral temperature gradients [8], and that the $V_{\mathrm{SD}}(T)$-method provides a sort of averaged junction temperature, it was decided to keep $T_{\mathrm{vj,max}} < 130\,^{\circ}\mathrm{C}$ at the onset of each test, thereby keeping a margin of at least $20\,^{\circ}\mathrm{C}$.

That being said, due to the much higher temperature capability of SiC devices, it is clear that this limit on the junction temperature is not a fundamental limit for the die. That leaves two options: either the packaging material is not suited for such elevated temperatures, or the device manufacturer has simply placed a considerable margin on the actual feasible operating point. If the latter is the case, considerably higher junction temperatures could have been assumed.

The large value of $\Delta T$ inevitably led to breaking another datasheet parameter, namely the restriction for a minimum switching speed when utilizing $V_{\mathrm{GS}} = -7.8\,\mathrm{V}$. With a restriction in the applied current of 30 A, the length of the on- and off-times were adjusted to ensure the desired $\Delta T$. These switching times were longer than the discussed maximum, as summarized below.

Two separate rounds of testing were performed, each with a different batch of components. The first round of testing utilized relatively short on- and off-times combined with a relatively large load current. That way, the devices were highly stressed without needing to resort to long cycle times, thereby allowing more tests to be performed in the scope of the short time at hand. The parameters for the first tests were set according to Table 5.2.

The load current was adjusted slightly for the different test objects in order to ensure the desired temperature swing. The adjustment was is the range of 0.1 A.

Table 5.2: Test Parameters For First Batch

| $\Delta T_{\mathbf{vj}}$ | $T_{\mathbf{vj,min}}$ | $T_{\mathbf{on}}$ | $T_{\mathbf{off}}$ | $I_{\mathbf{load}}$ |
|---|---|---|---|---|
| 80 °C | 44 °C | 500 ms | 1600 ms | 28.4 A |

The parameters for the second round of testing are given in Table 5.3. The same $\Delta T$ and minimum temperature were kept in order to keep the stress level of the tests as similar as possible. On the other hand, the on- and off-times were increased, while the load current was correspondingly reduced. The purpose of the second round of testing was to stress the lower levels of the package to a higher extent than what was the case for the first tests.

Table 5.3: Test Parameters For Second Batch

| $\Delta T_{\mathbf{vj}}$ | $T_{\mathbf{vj,min}}$ | $T_{\mathbf{on}}$ | $T_{\mathbf{off}}$ | $I_{\mathbf{load}}$ |
|---|---|---|---|---|
| 78 °C | 44 °C | 3300 ms | 7500 ms | 20 A |

# Chapter 6

# Results from Power Cycling

The results from the power cycling tests are provided in this chapter. Table 6.1 gives an overview of the tested devices. It can be seen that the stress level was very similar for the tests, as $\Delta T$ was close to 80 °C for all devices. Moreover, the minimum temperature was 44 °C for all devices.

Table 6.1: Overview of Test Results

| DUT | $\Delta T$ | $N_f$ | Comment |
|---|---|---|---|
| TO15 | 80 °C | 68481 | Used to evaluate $V_{GS(th)}$ for first batch |
| TO16 | 77.5 °C | 52250 | Slightly less $\Delta T$ |
| TO17 | 80 °C | 14358 | Early failure |
| TO18 | 80 °C | 67987 | |
| TO20 | 80 °C | 57150 | |
| TO21 | 78 °C | 53039 | Stressed at longer cycling period |
| TO25 | 78 °C | N/A | Used to evaluate $V_{GS(th)}$ for second batch |

During the first round of testing, five test objects were power cycled. These will be denoted as TO20, TO18, TO17, TO16 and TO15. These test objects were stressed at a higher load current and with shorter cycling periods, whereas the test objects in the second round were stressed at a lower current, yet with longer cycling periods. The test objects during the second round of tests will be denoted TO21 and TO25. The two rounds of tests were done with test objects acquired at two different times, and are therefore likely to come from differing batches. In addition to these devices, TO22 was utilized to investigate how the device threshold voltage affects the on-state forward characteristics.

All the power cycled devices failed according to the failure criteria of an increase in $V_{DS,warm}$ by 5 %. The number of cycles to failure was in the range of 50 000 to 70000 for all test objects except for TO17, which failed after 14 358 cycles. TO25 was not tested until failure. The following sections will give a more detailed overview of each test object.

## 6.1 First Batch of Test Objects

### 6.1.1 Test Object 20

TO20 was the first device to be power cycled, and it was the only device that was cycled with the bypass diode in the bypass branch. In order to explain the events that occurred, consider fig. 6.1, which displays the development of $V_{\mathrm{DS,warm}}$. It also displays the low-pass filtered signal for clarity.

The initial dip in the characteristic after 1645 cycles resulted as the test was tripped by the safety features, due to a too high heat sink temperature. Improved cooling was provided by adding a fan, which however led to a slight change in the operating point, yielding a somewhat smaller stress.

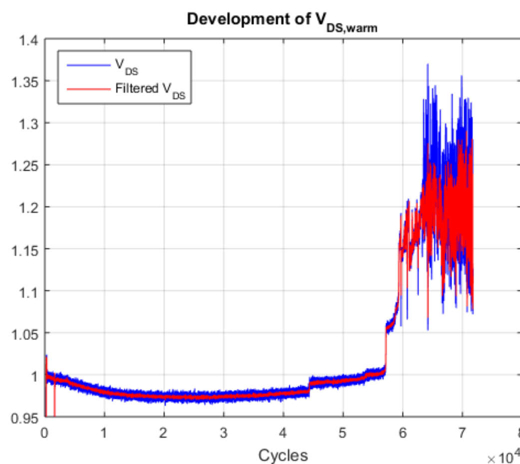



Figure 6.1: Development of normalized $V_{\mathrm{DS,warm}}$ for TO20

As is evident from the figure, there was an initial reduction of $V_{\mathrm{DS,warm}}$. This will be elaborated on in Section 6.2.

Around cycle 44 300 there was a sudden increase in the on-state voltage. The same thing occurred at cycle 53 500, although with a slightly smaller voltage increase. At cycle 57 150 there was a larger sudden increase, resulting in reaching the stated failure criteria. After that point, the test was supposed to stop, but due to accidentally disabling the failure criteria test, the experiment carried on until it was stopped manually at cycle 71 500. Not long after the test was supposed to trip, the measurements became unstable as seen in the figure. In the following, therefore, only the values up until when the device should have tripped is shown.

The maximum and minimum virtual junction temperatures as well as the temperature swing are shown in fig. 6.2. The graph is low-pass filtered to remove noise. This was performed with the MATLAB filtfilt function, in order to obtain zero phase shift. It can be seen that $T_{\mathrm{vj,min}}$ and $T_{\mathrm{vj,max}}$ decreased somewhat after the inclusion of the fan at cycle 3640, but that they

stayed stable after that. It is also evident from the figure that the maximum temperature decreased slightly up until around 20 000 cycles. This is most likely related to the reduction of the on-state voltage as seen in fig. 6.1. Likewise, the stepwise changes seen in that figure is also observable in fig. 6.2, in particular for the $T_{\mathrm{vj,max}}$ and $\Delta T_{\mathrm{vj}}$. The increase in $T_{\mathrm{vj,min}}$ is also slightly evident.

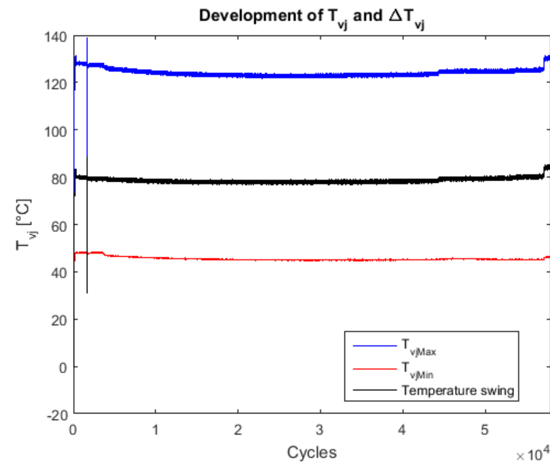



Figure 6.2: Development of $T_{\mathrm{vj,max}}$, $T_{\mathrm{vj,min}}$ and $\Delta T_{\mathrm{vj}}$ for TO20

Figure 6.3 displays the evolution of the thermal resistance during the course of the test. Apparently, the thermal resistance reduces slightly, but this does not make any sense physically, as it would imply that the DUT's ability to transfer heat away would improve as a result of the test. Since the thermal resistance is inversely proportional to the on-state voltage, it is believed that the observed reduction is related to the reduction in $V_{\mathrm{DS,warm}}$.

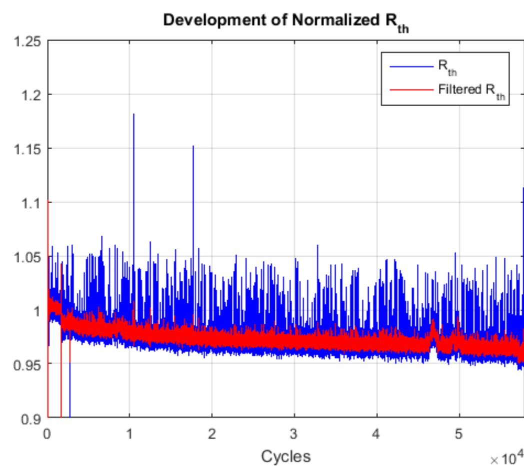



Figure 6.3: Development of normalized $R_{\mathrm{th}}$ for TO20

### 6.1.2 Test Object 17

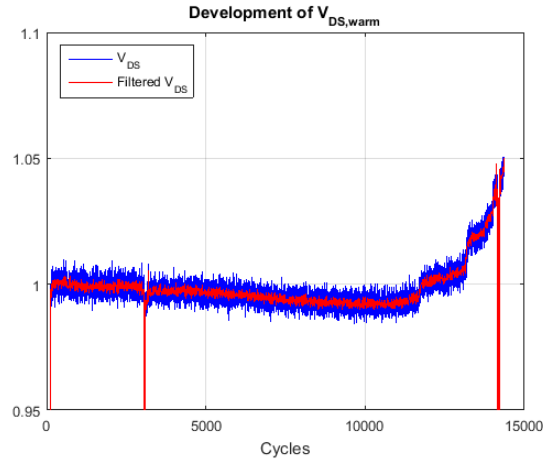



Figure 6.4: Development of normalized $V_{\text{DS,warm}}$ for TO17

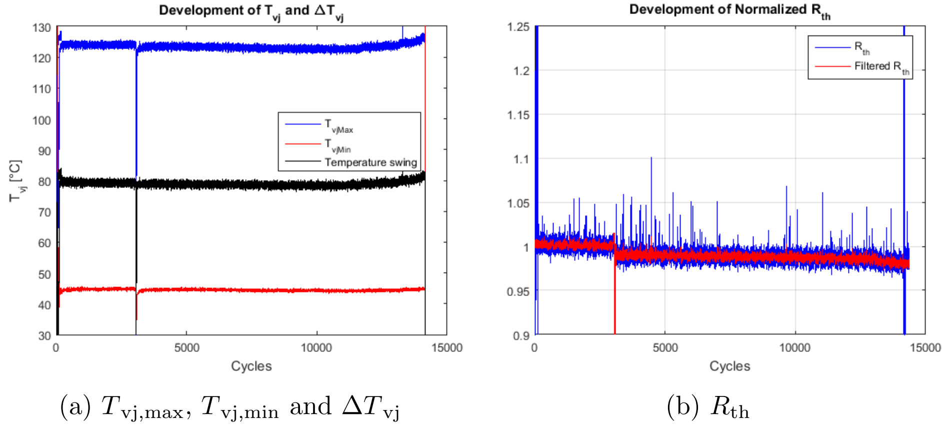
The third test object that was power cycled was TO17, and it too failed due to an increase in $V_{\text{DS,warm}}$. Moreover, the device had three steps in $V_{\text{DS,warm}}$, and showed the same initial reduction of the characteristic as TO20. However, the number of cycles to failure was significantly lower, reaching only 14 358 cycles. Figure 6.4 summarizes the events.

The sudden drop in the on-state voltage at cycle 3059 occurred because the test was stopped due to a failure of the current gain transistor in the sensing current source. The broken component was replaced, and the cycling continued. Unfortunately, it was not realized before the completion of the test that this changed the current from 27.8 mA to 28.2 mA, thus slightly changing the conditions at which the virtual junction temperature was estimated.

The test tripped again shortly before failure at cycle 14156, due to destruction of the sensing current source; one of the signal diodes were short circuited, most likely due to a portion of the load current flowing through the sensing current leg. The failed diode was replaced, and another diode was inserted into the sensing current leg, according to the discussion in Section 5.2.1. The test was resumed, however, the test object failed almost immediately after.

Figures 6.5a and 6.5b depict the evolution of the virtual junction temperatures and thermal resistance, respectively. The minimum temperature seems to have been slightly reduced after the test was restarted after about 3000 cycles. However, the higher sensing current after the test was resumed would according to equation 2.17 give a higher voltage drop $V_{\text{SD}}$. Due to its negative temperature coefficient, that would lead to a reduction of the virtual junction temperature. It is therefore believed that the actual test

conditions were fairly similar before and after the test tripped. It can also be seen in fig. 6.5b that the thermal resistance was reduced after the trip. This is likely also due to the increase in the sensing current, thereby leading to a reduction in $T_{\mathrm{vj,max}}$ and consequently also in $R_{\mathrm{th}}$ according to equation 4.2.




(a) $T_{\mathrm{vj,max}}$, $T_{\mathrm{vj,min}}$ and $\Delta T_{\mathrm{vj}}$

(b) $R_{\mathrm{th}}$

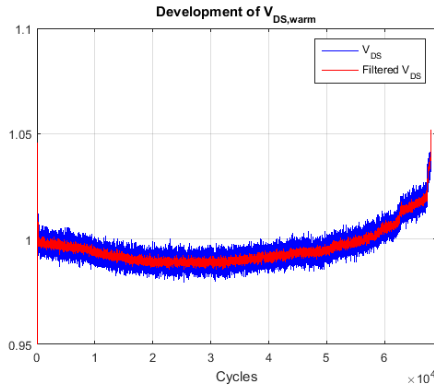
Figure 6.5: TO17 Development

### 6.1.3 Test Objects 18 and 16

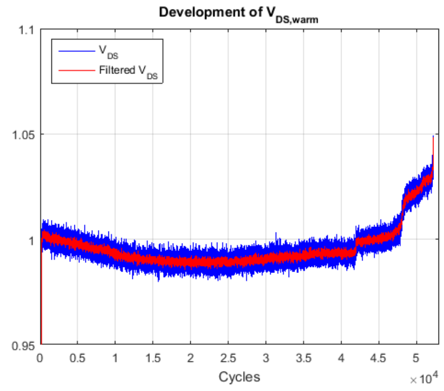
TO18 and TO16 were the second and fourth test objects to be power cycled, and showed very similar results. They will therefore be explained simultaneously in the following.

Both tests stopped due to an increase in the on-state voltage. Moreover, both test objects showed an initial reduction in $V_{\mathrm{DS,warm}}$, before picking up. Furthermore, TO18 experienced two step-like changes in the on-state voltage, whereas TO16 was subjected to three such changes. These results can be seen in fig. 6.6. The number of cycles to failure were 67 987 for TO18 and 52 250 for TO16. Both tests ran without any interruption.

Figure 6.7 depicts $T_{\mathrm{vj,max}}$, $T_{\mathrm{vj,min}}$ and $\Delta T_{\mathrm{vj}}$ for the devices. A low-pass filter is applied in order to see the development of the temperatures more clearly. Both minimum temperatures decreased slightly when $V_{\mathrm{DS,warm}}$ reduced, yet, they are in general very stable during the course of the tests. The maximum temperature also decreases with decreasing $V_{\mathrm{DS,warm}}$. Moreover, $T_{\mathrm{vj,max}}$ for TO18 has two distinct increases in temperature, whereas TO16 has three. All these events fit well with the observed step-like changes in $V_{\mathrm{DS,warm}}$. It can also be seen in the figure that the temperature swing was 80 °C for TO18, while only 77.5 °C for TO16. It is thus unexpected to find that the power cycling lifetime of TO18 was roughly 30 % higher. This will be discussed further in Section 7.3.

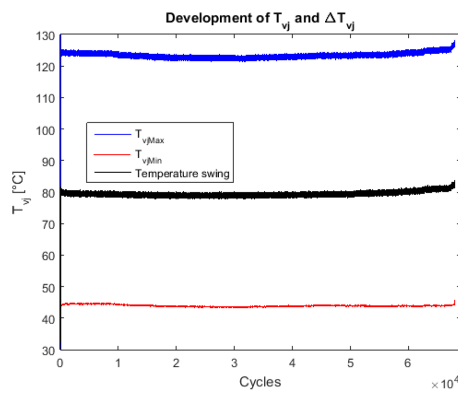



(a) TO18

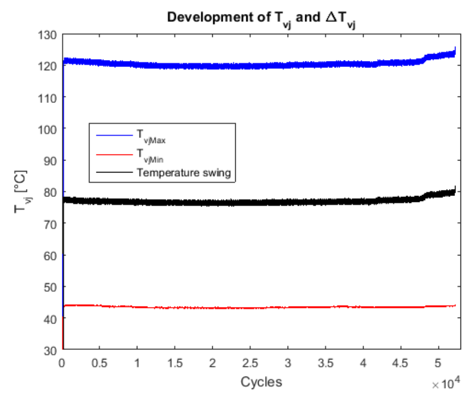



(b) TO16

Figure 6.6: Development of normalized $V_{\text{DS,warm}}$



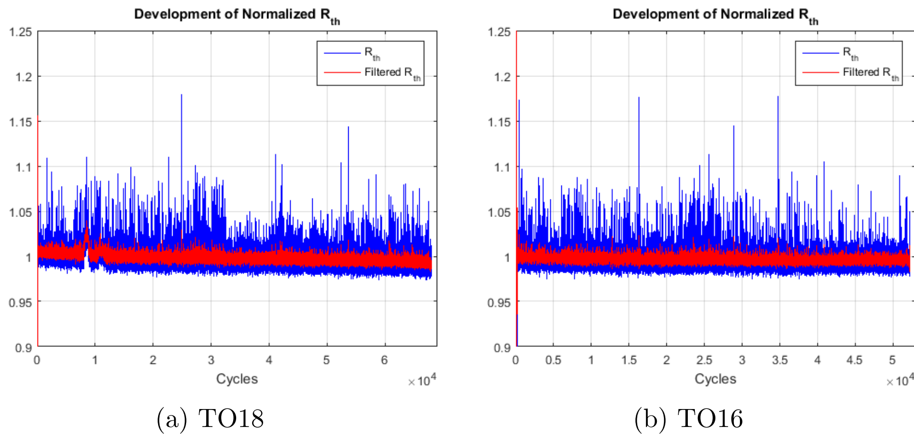

(a) TO18




(b) TO16

Figure 6.7: Development of $T_{\text{vj, max}}$, $T_{\text{vj, min}}$ and $\Delta T_{\text{vj}}$

The development of the thermal resistance for TO18 and TO16 are seen in fig. 6.8. When considering the low-pass filtered curve, it is evident that the thermal resistance was very stable throughout the test. For TO18, it seems to reduce slightly during the course of the test, whereas it appears relatively stable for TO16.




(a) TO18 (b) TO16

Figure 6.8: Development of normalized $R_{\mathrm{th}}$

## 6.2 Investigation of Initial Reduction in $V_{\mathrm{DS,warm}}$

All the first four power cycling tests displayed an initial reduction in $V_{\mathrm{DS,warm}}$. After these tests, the post-characterization of those test objects were made, all of which indicated a substantial reduction in the gate threshold voltage as shown in Section 6.4. This led to a hypothesis for the reduction in $V_{\mathrm{DS,warm}}$ to be caused by the threshold voltage drift. TO15 was power cycled in order to evaluate this hypothesis.

The procedure for evaluating the hypothesis was to run the power cycling test until the reduction of $V_{\mathrm{DS,warm}}$ was visible, and thereafter apply a positive bias of the gate for a long period of time. This bias would lead to an increase of the threshold voltage. Finally, the test were to be started again. If the on-state voltage had significantly increased, it would thus indicate that the power cycling test is in fact affected by the threshold voltage instability.

### 6.2.1 Test Object 15

Figure 6.9 shows the evolution of $V_{\mathrm{DS,warm}}$ during the test. The test ran for 19 190 cycles before it was stopped. Up until that point, a reduction in $V_{\mathrm{DS,warm}}$ had taken place in the same way as for the previous devices. After that, the DUT was biased at $V_{\mathrm{GS}} = 15\,\mathrm{V}$ for 4 hours, before the

test resumed. This seemed to give a slight increase in $V_{\text{DS,warm}}$, but not significantly. It was therefore decided to stop the test, and repeat the bias, however this time for 42 hours.

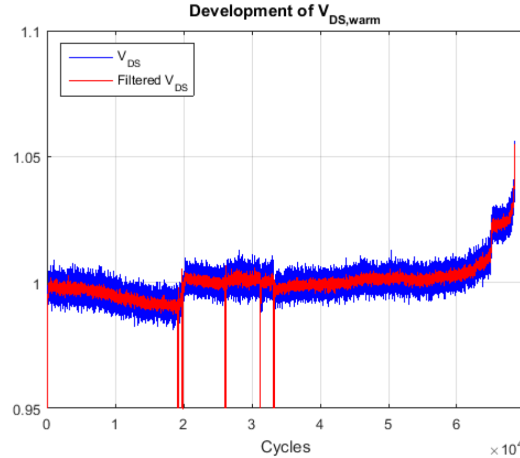



Figure 6.9: Development of normalized $V_{\text{DS,warm}}$ for TO15

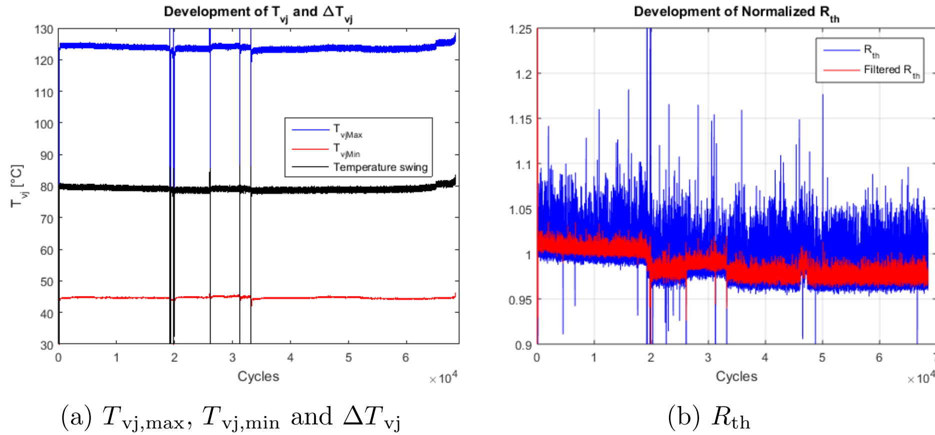
As seen, $V_{\text{DS,warm}}$ jumped to values larger than the initial values, indicating that the drift of the threshold voltage affects the on-state voltage. The practical implications of this will be elaborated on in Section 7.2.

Figure 6.9 also displays three dips in the on-state characteristic after 20 000 cycles, which occurred due to interruptions of the test. These interruptions came as a result of erroneous sensing current measurements; the measured current was negative, indicating that a current flowed the opposite way. However, the measured values for the virtual junction temperatures were stable, which only could be the case if the correct sensing current ran through the device. Hence, the measured current was due to a measurement error only. The test was therefore restarted each time it was tripped by the false current measurement.

The test stopped after experiencing two characteristic steps in the on-state voltage. The power cycling lifetime for the device ended up being 68 481 cycles.

The virtual junction temperatures and temperature swing is shown in fig. 6.10a. It is particularly important to note that the minimum temperature was the same before and after the bias test, such that the conditions applied when evaluating the on-state voltage were comparable.

Figure 6.10b displays the evolution of the thermal resistance. It is evident that the starting and stopping led to differing values, but between each time the test tripped, the thermal resistance stayed fairly constant.




(a) $T_{\text{vj,max}}$, $T_{\text{vj,min}}$ and $\Delta T_{\text{vj}}$

(b) $R_{\text{th}}$

Figure 6.10: TO15 Development

## 6.3 Second Batch of Test Objects

During the testing of second batch components, significantly longer on- and off-times were assumed, in order to increase the stress of the lower levels of the package. The load current was correspondingly reduced in order to achieve the same stress level in terms of $\Delta T$ and $T_{\text{vj,min}}$. The significantly longer on- and off-times resulted in a much longer duration of the test. Only one test object, TO21, from the second batch was tested, due to the limited time available.

### 6.3.1 Test Object 21

Figure 6.11 displays the evolution of the on-state voltage for TO21. The test ran continuously, except for one stop at 18 496 cycles. This was caused by a faulty thermal resistance measurement, due to malfunction of a thermocouple. Recall that the numerator of the thermal resistance is given as $T_{\text{j}} - T_{\text{c}}$, and the latter of these is measured by a thermocouple. Therefore, when the thermocouple displayed a large negative value of $-65\,000\,°\text{C}$, it was clear that the electrical contact between the two conductors was lost, and the test stopped due to the apparent large increase in thermal resistance.

Two courses of action were possible in order to restart the test. The first was to re-establish the electrical contact of the thermocouple. This, however, would probably not give the same measured temperature as before, and hence, cause a change in the measured thermal resistance. The second option was to evaluate the case temperature up until the point of failure, and simply assume that this temperature would remain constant throughout the remainder of the test. The advantage of this approach was its simplicity, as only a software constant needed to be added. The drawback, on the other hand, was that this approach would not take an increase of the case tem-

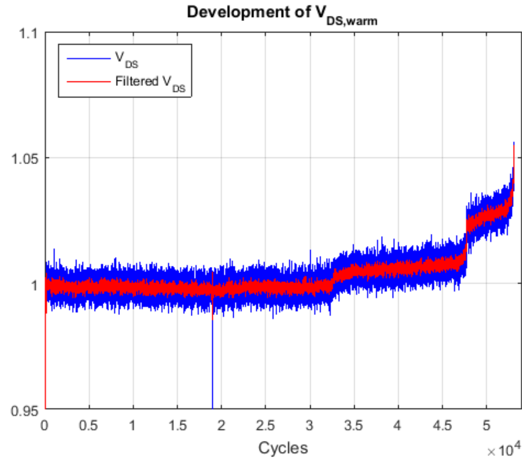
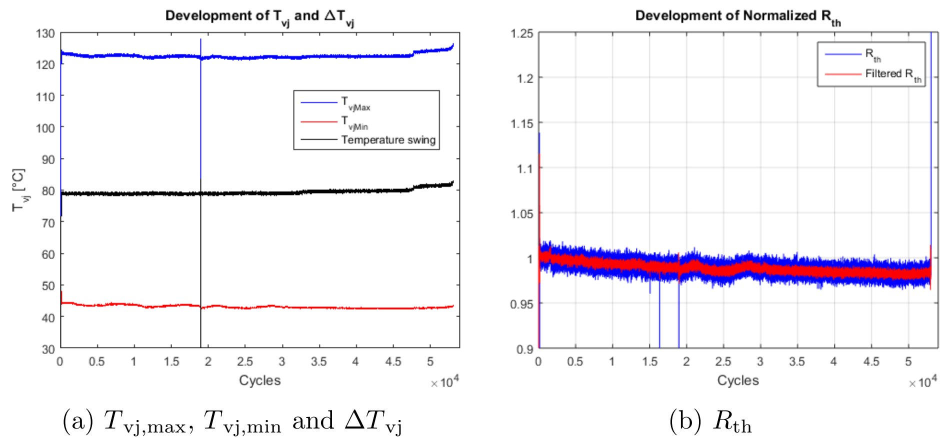



Figure 6.11: Development of normalized $V_{\mathrm{DS,warm}}$ for TO21

perature into account as the device degraded. Thus, the thermal resistance would appear to increase faster than what it really did, provided that any degradation were to occur.

The latter option was chosen, due to the assumption that the device would fail as a result of an increase in the on-state voltage. After resuming testing, three characteristic steps in $V_{\mathrm{DS,warm}}$ occurred, and the device finally failed after 53 039 cycles. Contrary to the previously tested devices, TO21 did not experience an initial reduction in the on-state voltage. In order to evaluate whether this was a specific issue related to the first batch, another test was performed. This will be presented in the next subsection.




(a) $T_{\mathrm{vj,max}}$, $T_{\mathrm{vj,min}}$ and $\Delta T_{\mathrm{vj}}$ (b) $R_{\mathrm{th}}$

Figure 6.12: TO21 Development

Figure 6.12a displays the evolution of the thermal resistance. Up until the point where the test was stopped, it seems to have experienced a slight

reduction. After the test resumed, there seems to be some instability in the measurements. It is not certain why this occurred, but it may be due to the constant that was utilized instead of the thermocouple measurement. As seen, the estimated thermal resistance was very stable and did not show any sign of degradation. As discussed above, if the thermal resistance degraded, it should have been discovered sooner than what would have been the case if the thermocouple was used, and hence, it seems likely that the interconnecting layers were not affected by this test.

Figure 6.12b depicts how the maximum and minimum junction temperatures developed throughout the test. $T_{\mathrm{vj,max}}$ and $T_{\mathrm{vj,min}}$ can be seen to vary slightly up until around 32 000 cycles. This was caused by slightly changing ambient temperatures, as the test ran over several days. However, the relative change they experienced seem to be identical, as seen by the stable temperature swing. Thus, only minor changes in the stress level occurred, due to the slightly changing minimum temperature.

### 6.3.2 Test Object 25

TO25 was used to evaluate whether the second batch also was affected by a drift in the threshold voltage. The test was therefore started with the test parameters as described in Section 5.7. In order to achieve the same stress as TO21, longer durations of the on- and off-times were necessary. In particular, the device was stressed at $T_{\mathrm{on}} = 5500\,\mathrm{ms}$ and $T_{\mathrm{off}} = 8500\,\mathrm{ms}$. Hence, a somewhat different operating point was chosen for TO25 than for TO21. The much longer on-time might indicate that the cooling was improved for TO25 with respect to TO21.

The development of the normalized $V_{\mathrm{DS,warm}}$ is seen in figure 6.13. It can be seen that the device experienced the same initial reduction as the devices from the first batch. It was therefore concluded that also the second batch is affected by the drift. The test was therefore stopped after 6464 cycles. Upon removing the DUT from the test bench, the gate was damaged. Thus the post-characterization of the device was not possible.

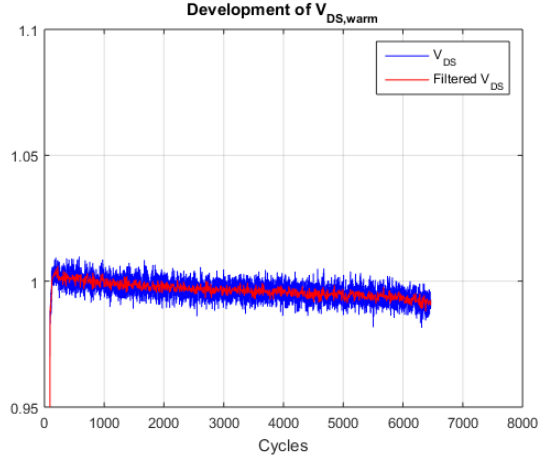



Figure 6.13: Development of normalized $V_{\mathrm{DS,warm}}$ for TO25

## 6.4 Characterization of Test Objects

The test objects were characterized in terms of their electrical performance prior to beginning and after completion of each test. The results from the characterization are summarized in Table 6.2 and fig. 6.14.

Table 6.2: Characterization of Test Objects

| Test Object | Measurement | $V_{\mathrm{GS(th)}}$ [V] | $I_{\mathrm{G,Leak}}$ [nA] | $I_{\mathrm{D,Leak}}$ [nA] |
|---|---|---|---|---|
| TO20 | Before test | 1,951 | 0,10 | 2,0 |
| | After test | 1,615 | 0,038 | 2,6 |
| TO18 | Before test | 1,632 | 0,10 | 1,3 |
| | After test | 1,473 | 0,05 | 2,8 |
| TO17 | Before test | 1,984 | 0,08 | 5,3 |
| | After test | 1,791 | 0,06 | 6,4 |
| TO16 | Before test | 2,068 | 0,11 | 1,0 |
| | After test | 1,691 | 0,05 | 2,65 |
| TO15 | Before test | 2,384 | 0,07 | 2,0 |
| | After test | 1,570 | 0,06 | 11,7 |
| TO21 | Before test | 2,811 | 0,05 | 43,0 |
| | After test | 2,921 | 0,06 | 51,9 |
| TO25 | Before test | 2,790 | 0,06 | 8,0 |
| | After test | N/A | N/A | N/A |

As seen in Table 6.2, the threshold voltage of all devices except TO21 reduced substantially after completion of the tests. The threshold voltage was measured more than 24 hours after completion of the tests. This ensured that measured instability was the permanent shift, and not the shift observed

directly after bias. It is believed that the observed instability origins from the threshold voltage instability of the SiC MOSFET, rather than being a result of the power cycling test.

According to the characterization, the gate leakage current decreased somewhat for some devices, however, the current was so small that this might be due to a measurement error. Likewise, the drain leakage current increased somewhat, especially for TO15 and TO21, but not significantly. Both the integrity of the gate oxide and blocking capability of the devices therefore seemed to experience little or no degradation as a result of the testing.

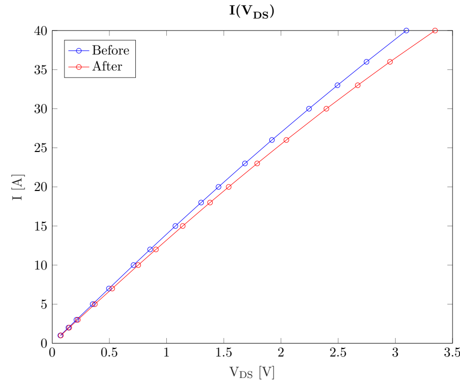
Figure 6.14 displays the *I*-*V* characteristic for the devices before and after power cycling. The blue line is the characteristic before the test, whereas the red line is after. TO20, TO17 and TO21 display an increase in the forward voltage after the completion of the test. This corresponds well with the observed failure mode, since the tests were stopped as a result of an increase in $V_{\mathrm{DS,warm}}$ by 5 %. On the other hand, TO18, TO16 and TO15 seems to have experienced a reduction in their on-state voltage. In other words, the latter devices have apparently *improved* characteristics, even though the tests were stopped due to an increase in the on-state voltage.

Due to these ambiguous results, it was decided to try to investigate this further. The approach for doing so is outlined in Section 6.5.

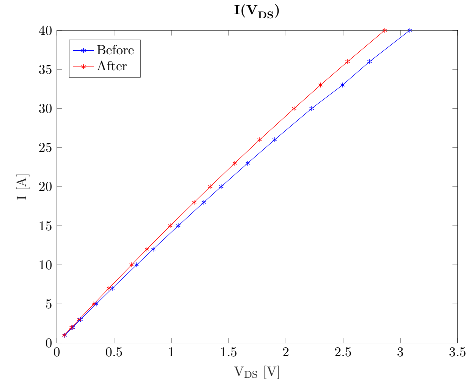
### 6.4.1 Scanning Acoustic Microscopy Analysis

The test objects TO20, TO18, TO17 and TO16 were sent to TU Chemnitz in order to perform a SAM analysis after conclusion of the tests. Ideally, this should have been done before the tests as well, but this was not done due to the limited time available. The results of the analysis are given in the appendix.

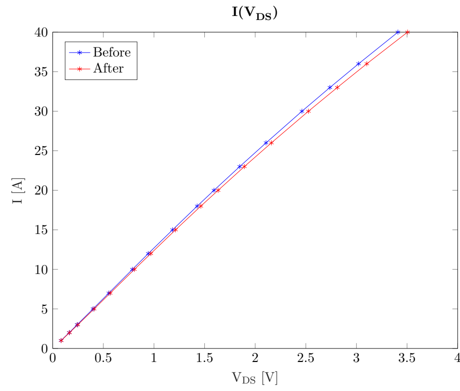
The main results from the analysis was that it seems like there was no damage to the interconnecting layer. Some voids were observed, but these were believed to be developed during the interconnecting process. The investigation could not determine whether the bond wires were lifted off, nor whether it was soldering or silver sintering that was used.



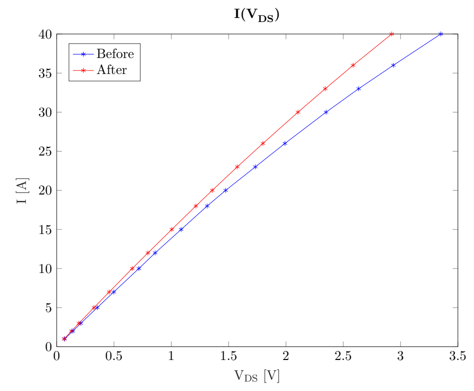

(a) TO20



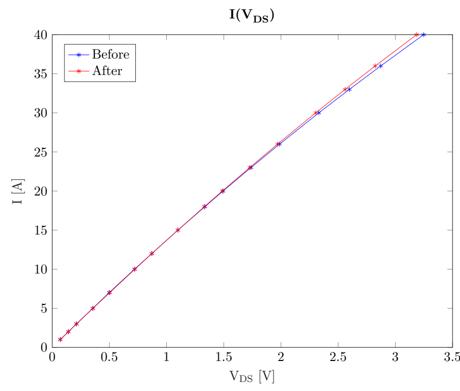

(b) TO18



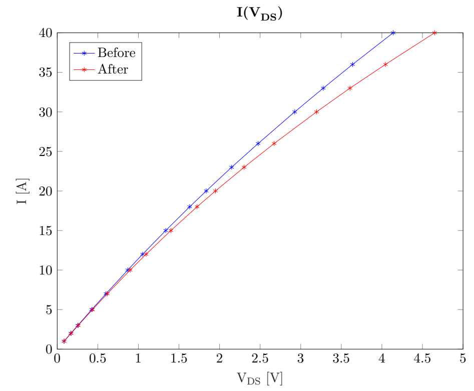

(c) TO17




(d) TO16




(e) TO15




(f) TO21

Figure 6.14: On-state characteristics of DUT before and after power cycling

## 6.5 On-State Characterization Dependency on Drift

It was assumed that the ambiguous results in the preceding section could be related to the threshold voltage instability. In order to investigate this assumption, the on-state characteristic was measured before and after application of a gate bias. In particular, TO22 was placed under a bias of $V_{\mathrm{GS}} = 15\,\mathrm{V}$ for 24 hours. The threshold voltage before the test and 24 hours after the test completion were $2.79\,\mathrm{V}$ and $2.98\,\mathrm{V}$, respectively. Hence, the expected positive shift of the threshold voltage occurred.

Except for the bias test, TO22 did not experience any other applied stress. The result of the on-state characterization is given in figure 6.15. As seen in the figure, the characteristic displayed a slight tendency of reduced forward voltages for low values of the current. However, the tendency at higher currents is more clear, and indicates increased forward voltages. These results will be further discussed in Section 7.2.

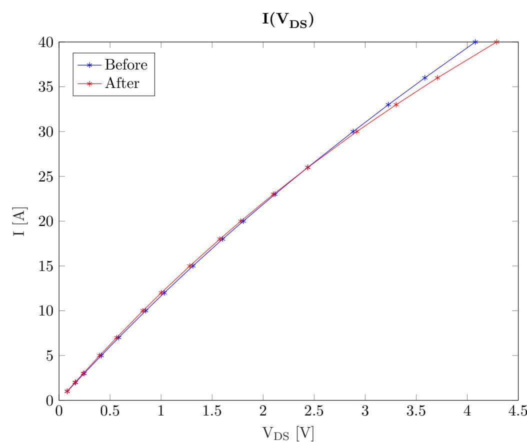



Figure 6.15: Development of normalized $V_{\mathrm{DS,warm}}$ for TO22

# Chapter 7

# Discussion and Further Work

The aim of this master's thesis was to investigate the methodology for performing power cycling on SiC MOSFETs. In particular, the $V_{SD}(T)$-method will therefore be discussed in this chapter. Moreover, the effect of the threshold voltage instability on the tests as well as the actual power cycling results will also be discussed. Finally, the recommended further work will be presented.

## 7.1 Evaluation of the $V_{SD}(T)$-method

As noted in [4], finding a reliable TSEP for use in conjunction with SiC MOSFETs has been difficult, due to the problems with the threshold voltage instability. It is therefore in place to evaluate the $V_{SD}(T)$-method with the results that have been obtained.

### 7.1.1 Threshold Voltage Instability

It is evident that for the method to be reliable, a prerequisite is that the MOSFET channel is completely closed. According to Herold et. al, the channel might conduct a small portion of the current if the voltage drop across the body diode is close to the gate threshold voltage, and $V_{GS}$ is not sufficiently low [18]. In their article, they find that $V_{GS} = -6\,V$ is the limit for where the channel turns completely off. However, if a negative drift of the threshold voltage were to occur, meaning that the channel would become conducting at a lower gate-source voltage, the gate-source voltage at which the channel is completely closed might be further reduced.

Thus, a sufficiently small $V_{GS}$ ought to be utilized in order to ensure that the channel is completely closed, even in the event of a negative threshold voltage drift. On the other hand, using a too small gate-source voltage will increase the rate of any potential drift, leading to an inevitable trade-off.

As noted in Section 4.3, sufficiently low gate voltages are necessary in

order for the $V_{\mathrm{SD}}(T)$-method to be utilized. This gate voltage ought to be evaluated for a given device. Thus, the method necessitates that the particular device under test is able to switch to such low voltages. In particular, the device datasheet needs to allow switching to the gate voltage that ensures the completely closed channel.

### 7.1.2 Stability and Reliability of the TSEP

An indication of a stable TSEP is that $T_{\mathrm{vj,min}}$ is not drifting over time [18]. This is the case because if the device has not degraded, the same minimum temperature will be reached at the end of each cycle. If, on the other hand, the device has started to degrade, the minimum temperature may increase somewhat as the maximum temperature increases. However, the minimum temperature will not increase by the same amount as the maximum temperature, due to the fact that the maximum temperature consist in part of very small thermal time constants corresponding to the semiconductor chip.

It is evident from the previous chapter that the minimum virtual junction temperatures are very stable. The parameter decreases slightly at the beginning of the tests, but this is believed to be due to the threshold voltage drift, thereby causing a reduced on-state voltage, which again yields lower losses. There are some small steps in the minimum temperature, however, these correspond to the points were the on-state voltage degraded. Furthermore, TO21 experienced some slight variation in its minimum temperature, but this was as mentioned due to the varying ambient temperature. Thus, it seems that the minimum temperature does not change much, indicating that the method is reliable for estimating the junction temperature.

One of the strengths and short-comings of the method, however, is its ability to map a spatially varying temperature into one single value. The advantage lies in the simplicity of obtaining a single value for the virtual junction temperature. On the other hand, as mentioned in Section 2.5, the actual temperature of certain areas of the chip might be significantly higher as a result of the lateral temperature gradient. Thus, the maximum temperatures are not accurately reflected by the method.

### 7.1.3 Bipolar Degradation

The bipolar degradation of the SiC MOSFET was described in Section 2.3.2. Clearly, if the body diode were to degrade due to this reliability issue whilst being utilized for estimating the junction temperature, the results would not be valid as it would imply an increase in the forward voltage. Thus, the negative temperature coefficient of $V_{\mathrm{SD}}$ would finally estimate the virtual junction temperature to be lower than the actual temperature.

However, due to the very small sensing current magnitude, and the relatively short times that the internal body diode is utilized for conducting the current, the risk of experiencing bipolar degradation is reduced [29]. Moreover, the very stable minimum virtual junction temperatures throughout the tests indicates that no degradation occurred.

## 7.2 Power Cycling Dependency on $V_{\mathrm{GS,(th)}}$

### 7.2.1 Effect of the Threshold Voltage Drift

All the devices in the first batch experienced an initial reduction in $V_{\mathrm{DS,warm}}$. Exactly what caused this is not certain. One possibility is that the devices experienced some kind of burn-in effect. However, when considering the test of TO15, in which the test was stopped and a positive bias was applied before resuming testing, it seems like a drift in the threshold voltage may be the reason for the reduction in the on-state voltage. This conclusion is also supported by the test of TO22. This device displayed a clear tendency of increasing forward voltage at high currents after a positive drift of the threshold voltage.

On the other hand, testing of TO21 did not lead to an initial reduction of $V_{\mathrm{DS,warm}}$. Yet, TO25 displayed the initial reduction as the devices in the first batch. It is therefore likely that the problem is not related to the devices being from different batches, but rather, that it is in fact depending on the threshold voltage drift. This is supported by the fact that all devices except for TO21 displayed a substantially reduced threshold voltage after the test. TO21 on the other hand actually displayed an increase in $V_{\mathrm{GS(th)}}$.

The on-state characterization indicated that some devices had reduced on-state voltages for a given current, whereas other devices experienced an increase in the same characteristic. This ambiguity is not well understood. However, considering that the devices failed according to an increase in $V_{\mathrm{DS,warm}}$ by 5 %, an increase in the on-state voltage would be expected. On the other hand, the test of TO22 indicates that a reduction of the threshold voltage would lead to reduced on-state characteristics. Thus, these effects influence the on-state characteristic of a device in opposite ways.

However, this does not explain why some of the test objects failed according to an increase in $V_{\mathrm{DS,warm}}$, yet displayed a reduction of the on-state characteristics afterwards. It is important to note, however, that the threshold voltage and on-state characteristics were not measured directly after the test was completed. This could potentially have given clarity to the results, as the threshold voltage would be closer to the value at the completion of the test.

It can also be noted that the two devices indicating the strongest increase in forward voltage were TO20 and TO21. The former of these devices were stressed much longer than it was supposed to according to the failure criteria.

Thus, it is likely that this device experienced a tougher stress than the other tested devices. On the other hand, TO21 was the only device which did not experience a reduction of $V_{\mathrm{GS(th)}}$. Thus, these factors might explain why these devices displayed a positive shift of the on-state voltage.

As mentioned in Section 2.3.1, the threshold voltage instability is not entirely understood. Therefore, it is difficult to evaluate the drift that is observed for the different devices. However, one aspect that clearly differed for the first batch components and TO21 was the duration of the on- and off-times. The duty cycle and cycling period of the first batch components are summarized in Table 7.1. One possibility for the threshold voltage drift is thus that it resulted due to differing operating points.

Table 7.1: Cycle Parameters During Power Cycling

| | First Batch Components | TO21 |
|---|---|---|
| Duty Cycle | 0,238 | 0,306 |
| Period [s] | 2,1 | 10800 |

An important note is that the device was only switched at its nominal minimum negative voltage. It was not switched at its nominal maximum positive voltage. Thus, the observed threshold voltage instability would likely be different if the nominal positive voltage was utilized. However, this does not change the fact that if drift occurs during the a power cycling test, the operating point of the test will change.

The results of this thesis thus indicate that the instability of the SiC MOSFET threshold voltage affects the result of the test. Not only does it change the stress level of the test, but moreover, it can make it harder to evaluate whether the test object has in fact failed according to the test criteria.

Furthermore, an initial reduction of the on-state voltage due to drift will cause a longer power cycling lifetime. This is clearly seen in the characteristic for $V_{\mathrm{DS,warm}}$ in the previous chapter. After the initial reduction, the normalized $V_{\mathrm{DS,warm}}$ is lower than 1. Hence, when the test is finally tripped after a 5 % increase in the on-state voltage, the device has in fact experienced a more severe degradation than the stated conditions. The lifetime may not be much longer, as it depends on the magnitude of the steps in the on-state characteristic. However, since the number of cycles to failure might be increased, a fair comparison to silicon devices is complicated.

These aspects ideally should be clarified when power cycling SiC MOSFETs. In order to do so, the methodology for performing the test might have to be modified. One possibility is to change the failure criteria to a 5 % increase in the on-state voltage from the minimum on-state voltage in the test. However, this too would give an improper comparison to other devices. Another possibility would be to keep the current failure criteria,

while attempting to minimize the drift that occurs during the test. The latter ought to be done either way. A suggestion for doing so is given in the following.

### 7.2.2 Mitigating Drift of $V_{\mathrm{GS(th)}}$ During Power Cycling

Because it is desirable to maintain a the predetermined initial stress during the power cycling test, it is important to try to keep the threshold voltage instability to a minimum. As noted in [27], the threshold voltage is dependent on the magnitude, polarity and duration of the applied bias. Furthermore, the temperature under which bias occurs also affects the instability [41]. Lelis et. al also finds that the drift is largest initially [27]. In an attempt to try to minimize the drift, it therefore seems like an equal duration of positive and negative bias would be advisable, in addition to avoiding long periods without switching the bias.

If for example considering the devices from the first batch, the devices were stressed on average at

$$\frac{15\,\mathrm{V}\cdot 500\,\mathrm{ms} - 8\,\mathrm{V}\cdot 1600\,\mathrm{ms}}{500\,\mathrm{ms} + 1600\,\mathrm{ms}} = -2.5\,\mathrm{V}. \tag{7.1}$$

That might not seem like a lot, but considering the high temperatures that also were present, the threshold voltage instability can get more severe [27]. Moreover, for the DUT used in this experiment, recall that the low switching frequency also may have contributed to drift.

A possible solution for reducing the threshold voltage drift would be to switch the DUT in a more sophisticated way. In particular, by switching such that

$$\int_0^{T_\mathrm{P}} V_{\mathrm{GS}} = 0, \tag{7.2}$$

the threshold voltage instability might be reduced. Assuming the stress level of the first test batch of $T_{\mathrm{on}} = 500\,\mathrm{ms}$ and $T_{\mathrm{off}} = 1600\,\mathrm{ms}$, a possible switching sequence is depicted in fig. 7.1. In the figure, the DUT switches such that it is on and off for equally long times during one period $T_{\mathrm{P}}$. By switching the DUT during the off-time, the switching speed limits are respected without compromising on a lower $\Delta T_{\mathrm{vj}}$. Since the auxiliary switch remains off, the DUT is still cooling down. This way, the drift may be reduced. Moreover, for the particular Cree device tested in this thesis, the switching constraint could be respected. A drawback of the approach is that it would not be possible to estimate the virtual junction temperature during the new on-state of the DUT. Due to lack of time, this was unfortunately not tested in the actual set-up.

Although somewhat more complicated, the same idea could be applied if the on-time was too long. Then, the DUT would have to switch to its

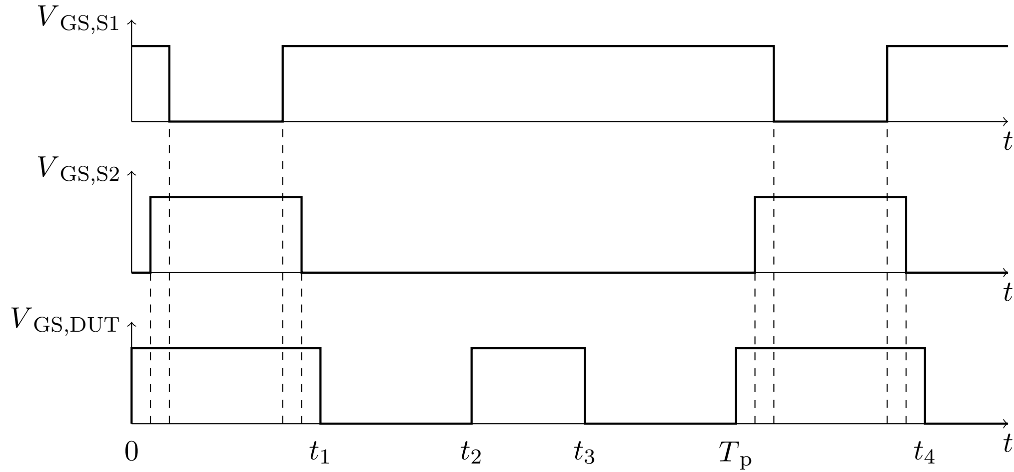



Figure 7.1: Possible switching sequence for reducing threshold voltage drift

negative gate-source voltage, thereby necessitating also switching the corresponding auxiliary switch. This switching sequence ought to be quite rapid, to ensure that the DUT does not have time to cool down considerably.

## 7.3 Results of Power Cycling

The performed power cycling tests need to be considered as preliminary testing because of the limited amount of samples that were tested, but also due to the special effects that were observed due to the threshold voltage drift. To a certain extent, the test rig also needed to be run in, making the results from the tester harder to compare to each other. Ideally, all the tests would have run continuously. However, it is in place to look at the results that were obtained in order to discuss power cycling of SiC MOSFETs.

### 7.3.1 Failure Mode

Contrary to what was expected due to previous literature on power cycling on SiC diodes [8], the devices under test did not fail as a result of an increase in the thermal resistance. This was expected since SiC is stiffer than silicon, thereby increasing the stress on the layers beneath the chip.

Instead, all devices failed as a result of an increased on-state voltage, after having experienced the typical step changes in this characteristic, indicating bond-wire lift off [3, p. 392]. As mentioned in Section 6.4.1, the SAM analysis was not able to identify the lift-off. On the other hand, the thermal resistance measurements were very stable for all test objects, and the results of the SAM analysis showed that the interconnecting layers were seemingly unaffected. These findings indicate that the interconnecting layer

did not degrade, leaving bond-wire lift off more plausible.

One possible explanation might be found in the recent article by Herold et. al regarding power cycling of SiC MOSFET modules [18]. Here, three devices were tested, one of which contained the conventional solder interconnections, while the two others utilized silver sintering. The first device failed due to an increase in the thermal resistance, whereas the latter two failed as a result of an increase in the on-state voltage. Their conclusion was that improving the interconnecting by replacing the solder layer with silver sintering causes the bond-wire, instead of the interconnecting layer, to become the weakest link in terms of reliability [18]. Thus, if silver sintering is utilized for the Cree devices, this may explain the very stable thermal resistance throughout the tests.

On the other hand, the differing structures of discretes and modules may also contribute to differing results in this thesis compared to what is found in the literature. The mentioned articles have utilized modules [8, 18]. In particular, the increased number of interconnecting layers in the module may yield higher mechanical stress during power cycling, and thereby sooner fatigue by an increase in the thermal resistance.

### 7.3.2 Lifetime of Devices

The amount of cycles to failure varied between the devices. With the exception of the early failure of TO17, however, the number of cycles were fairly similar. These are repeated in Table 7.2.

Table 7.2: Number of Cycles to Failure

| Test Object | TO20 | TO18 | TO17 | TO16 | TO15 | TO21 |
|---|---|---|---|---|---|---|
| $N_{\mathrm{f}}$ | 57 150 | 67 987 | 14 358 | 52 250 | 68 481 | 53 039 |

It is not clear why TO17 failed much earlier than the other devices. One possibility could be that the device simply had some malfunction after fabrication. Another possibility is that it somehow experienced fatigue during handling. Either way, it is considered an outlier, and will therefore not be considered when discussing the lifetime of the devices in the following.

The remaining test objects all failed between 52 000 and 69 000 cycles. According to the measured data, out of the devices in the first batch, all were stressed at $\Delta T = 80\,°\mathrm{C}$, except for TO16 which accidentally was tested at $\Delta T = 77.5\,°\mathrm{C}$. One could therefore expect a higher number of cycles for this device due to the reduced stress, if assuming a deterministic process.

On the contrary, however, power cycling is a stochastic process, and thus, a vastly larger population size would be needed to be able to accurately judge the validity and variability of the results. Some variability in the data is inevitable, considering that there are slight manufacturing differences between the test objects, contributing to differing reliability. Based

on the small sample size, it is therefore hard to conclude with any accuracy regarding the validity of single observations.

Moreover, the conditions at which the tests were performed inevitably vary somewhat. Factors such as the ambient temperature influences the test to a certain degree, as was observed with TO21. How tightly the test object was mounted onto the heat sink could also affect the test. Since this was done by hand, it is likely that some devices experienced better cooling conditions than others. Ensuring that the devices are mounted with the same mounting torque could therefore reduce the uncertainty of the tests.

Another factor that may have influenced the results is the way characterization was performed, as this differed slightly between the tests. In particular, the thermocouple measuring the temperature of the test object during calibration had to be replaced between each test run. A new thermocouple was therefore made between each test. If the thermocouples measured different temperatures during calibration, this would translate into differing stress levels during the actual test between devices. Ideally, the same thermocouple should have been used all the time, such that the way the calibration was performed was consistent between each sample.

Finally, since the Cree devices have recently been released, there might be some variability resulting from devices from differing batches. However, as noted, the sample size is too small to judge this from the obtained results.

## 7.4 Recommended Further Work

As mentioned, in order to evaluate the obtained results, a much larger sample size ought to be tested. It is therefore recommended to proceed with testing several devices. Moreover, it could be interesting to perform power cycling with another component than the Cree device. In particular, performing power cycling on power modules is recommended, as the results from this could be more easily compared to what is already found in the literature. These tests could shed light on general aspects on power cycling SiC MOSFETs.

As the current set-up primarily was made in order to investigate the methodology for performing power cycling on SiC MOSFETs, there are several things that may be improved in the set-up if a larger number of devices are to be tested. These will be discussed in the following.

### 7.4.1 Changing the DUT Gate Driver

Adding a gate driver for the DUT that is capable of driving the DUT at the rated voltage would be beneficial for the test. Not only would the test conditions be closer to application, but the DUT would also be able to switch at nominal speeds. Changing the set-up to accommodate switching at rated values might also necessitate using another load current source,

since using a higher gate voltage with the same load current yields lower losses. Otherwise, longer cycles are needed to obtain the same $T_{\text{vj,max}}$.

### 7.4.2 Improving the Sensing Current Source

As mentioned, the utilized current source was made for a previous thesis. Some solutions were not ideal, and ought to have been improved before use in the current work. However, due to limitations in available time, and since the main goal of this thesis was to investigate the methodology of performing power cycling on SiC MOSFETs, the previous source was only modified where it was necessary.

One drawback of the source is that it draws close to the limit of what the voltage source can supply. This is clear when considering Kirchoffs first law around the outer loop of fig. 5.5. This gives

$$V_{\text{in}} = V_{R_1} + V_{\text{pnp}} + V_{D_2} + V_{\text{SD,DUT}} + V_{D_3} + V_{R_2}. \tag{7.3}$$

The voltage drop $V_{R_1}$ is determined by the difference between $V_{\text{in}}$ and $V_{\text{p}}$, and is 8.2 V. Since the voltage drop of the DUT is in the range of 2.5 V, and that of the diodes in the range of 5 V, it is clear that the input voltage of 15 V is at its limit. A way of improving this would be by changing the op amp voltage at the positive terminal. This requires some modification of the current source.

A more severe drawback, however, is that the current source is not controlled with respect to the input voltage. That is, for a change in input voltage, the output current also changes. Currently, therefore, it is necessary to wait until the voltage source is warmed up before both calibration or power cycling may commence. This ensures a stable voltage driving the sensing current source, which is then capable of driving a constant sensing current to ensure validity of the $V_{\text{SD}}(T)$-method.

### 7.4.3 Estimation of $T_{\text{vj}}$

A clear improvement of the present set-up would be to ensure consistent measurements of $V_{\text{SD}}$ for estimating $T_{\text{vj}}$. This could be done by utilizing a separate NI 9205 C-series module, or a module that has a specified sampling rate per channel. This would ensure a consistent spacing of the measurements in time, which would increase the accuracy of each measurement of $T_{\text{vj}}$. Adding an additional module to the set-up would require modifying the set-up by using another chassis such as the NI-9067 to accommodate the extra module. Either way, minor changes in the VIs would be necessary if this is to be improved.

As described in Section 5.6.2, the estimation of $T_{\text{vj,max}}$ is done some time after the load current through the device is actually turned off. Thus, the

estimated temperature is not based on the maximum temperature, due to the very fast initial temperature reduction.

An improved estimate of the actual maximum junction temperature could possibly be implemented by using the $\sqrt{T}$-method [42]; it has been shown that for relatively large chip areas, the initial temperature reduction after turn-off of the current decays according to the square root of time. Hence, the measurement error from the inevitable delay might be somewhat compensated, provided that the method is applicable for this type of device as well.

### 7.4.4 Reducing the Size of DUT Heat Sink

The size of the DUT heat sink is much larger than the DUT. The advantage of that is that the heat sink temperature is very stable. On the other hand, the advantage of reducing its size is that a much smaller thermal mass would be heated during calibration, thereby considerably reducing the time needed for calibration of the device. Reducing the time that the calibration takes also reduces the stress on the component before testing commences, as the case temperature is heated for a shorter time.

### 7.4.5 Monitoring Voltages of Auxiliary Switches

By including measurements of the auxiliary switches, it would be possible to determine any change in their switching characteristics. Thus, it would be possible to monitor degradation, and change these components before breakdown were to occur.

### 7.4.6 Improving Cooling for Auxiliary Switches

The auxiliary switches are currently cooled by a fan. The cooling is sufficient for the current set-up, however, the fan is a source of EMI, which is picked up by the measurement circuit and in particular the DUT gate.

### 7.4.7 Expanding the Test Bench

Finally, due to the removal of the bypass diode, the current sharing in the overlapping time is very unequal; the freewheeling branch carries most of the current, due to the higher voltage drop in the DUT branch. Thus, the DUT experiences a very low current during this period. Having a freewheeling diode, or expanding the test-bench to incorporate another test object would cause a more equal current sharing, which would contribute to slow down the initial fast temperature reduction of the DUT. Having a second test object necessitates modifying the present set-up extensively, however.

# Chapter 8

# Conclusion

The potential benefits of the SiC MOSFET is widely acknowledged by the power electronics community, and improvements in system size, weight, efficiency and operating temperature may be realized compared to utilizing state-of-the-art silicon devices. However, the reliability of the SiC MOSFET needs to be addressed.

As such, this master's thesis has been conducted in order to investigate how power cycling ought to be performed on SiC MOSFETs. In order to do so, the SiC MOSFET reliability issue of the instability of the threshold voltage has been evaluated, and several qualifying tests for power cycling have been performed. Finally, power cycling tests of third generation SiC MOSFETs were conducted.

Evaluating the threshold voltage instability clearly illustrated that SiC MOSFET devices are affected by drift. This was done with a dedicated test bench, in which second generation devices were tested. However, a shift of the threshold voltage seemingly also occurred when performing power cycling on the third generation devices. In addition to being a reliability problem in itself, this was found to impact the power cycling test. The latter is unfortunate, as it causes a varying stress of the device under test during the course of the test. A simple measure for reducing the drift of the threshold voltage drift during power cycling has therefore been proposed.

The challenge of performing power cycling with SiC MOSFETs has been finding a reliable TSEP for monitoring the junction temperature, such that the stress level of the test could be both maintained and monitored. In particular, the maximum junction temperature needs to be estimated by using a thermo-sensitive electrical parameter (TSEP) that is not affected by the threshold voltage instability. The TSEP that was evaluated and used for the thesis is the $V_{\mathrm{SD}}(T)$-method, which utilizes the internal body diode of the SiC MOSFET to estimate the junction temperature. It was shown that in order to utilize this method, a substantial negative gate-source bias was needed. Power cycling with SiC MOSFETs thereby necessitates actively

switching the DUT during the test.

A dedicated test bench was built for power cycling the SiC MOSFETs, and several tests were performed. The results indicated an initial gradual reduction in the on-state voltage for all the tested devices. This is believed to be related to a reduction in the threshold voltage.

All the tested devices were cycled with the same minimum junction temperature of 44 °C, and a temperature swing close to 80 °C. Except for one outlier that failed after only 14 358 cycles, the number of cycles to failure was consistent between 50 000 and 70 000 cycles. All devices finally reached the end of life criteria by an increase in the on-state voltage by 5% with respect to the initial values. The thermal resistance, on the other hand did not seem to degrade for any of the cycled devices.

Thus, power cycling of SiC MOSFETs seems feasible by the use of the $V_{\mathrm{SD}}(T)$-method. However, the drift of the threshold voltage is something which should be minimized, as it affects the power cycling results.

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# Appendix

# Appendix A

# Scanning Acoustic Microscopy Analysis

Scanninc Acoustic Microscopy was performed on the first four test objects after power cycling was performed. This was done by M.Sc. Weinan Chen at TU Chemnitz. The findings are included in the following. The names of the test objects are given according to a label printed on each package. Table A.1 summarizes the relationship.

Table A.1: Labels for Test Objects

| Test Object | TO20 | TO18 | TO17 | TO16 |
|---|---|---|---|---|
| Label | E2 | B9 | B1 | K8 |

SAM-Inspection for SiC MOSFET Device

| B1 | E2 | K8 | B9 |
| --- | --- | --- | --- |

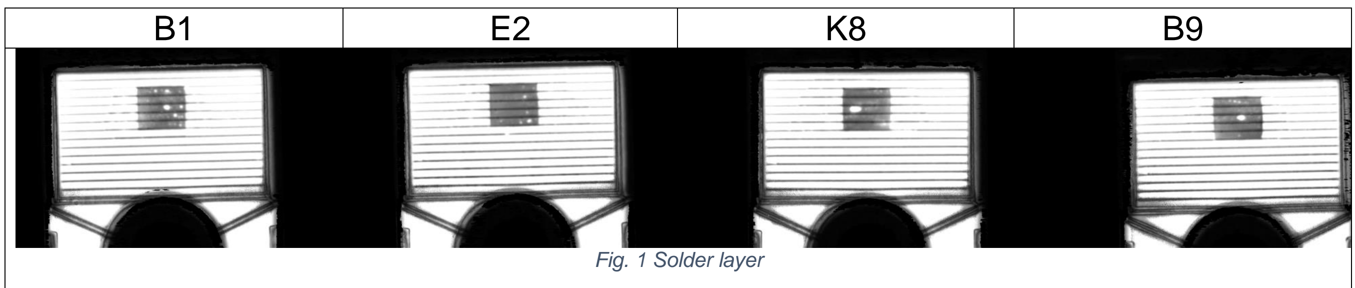

*Fig. 1 Solder layer*

Fig. 1 shows the SAM inspection for four discrete SiC MOSFET in package TO-247. Scanning was performed from the back side of the device using 75 MHz transducer, focal length 12.7 mm (SAM 400, PVA Tepla). Few of voids in the solder layer can be seen in Fig. 1. They are produced during the solder process, the comparison with the scanning picture before power cycling test is needed. The modification of the voids during PCT is rare, typically cracks do not origin at voids. The sharp defined boarders of the voids indicate, however, that they have not been induced by the PCT. The edges of solder layer in each device are clear, except device K8, bottom right corner and upper right corner, see Fig. 2. For the other devices, no obvious degradation was found. Microcracks, however, can not always be detected by SAM.

| B1 | E2 | K8 | B9 |
| --- | --- | --- | --- |

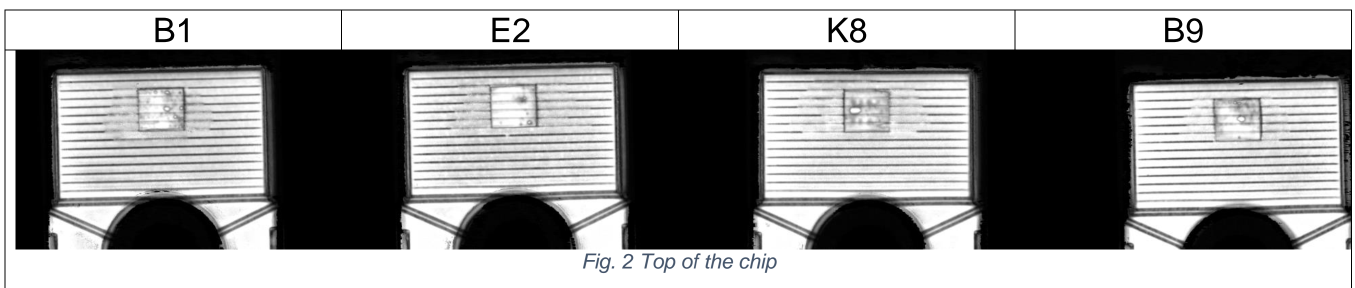

*Fig. 2 Top of the chip*

Fig. 2 shows the scanning focused on the top of the chip. There are some dark points on chip K8, which could be the bond wire patterns. Normally the scanning before PCT will be taken as a reference. Because of the unavailable reference, it unknown, whether the patterns changed before and

after PCT. The bond wire patterns are invisible in other three chips. The inspection of bond wire lift-off under SAM is always difficult and not possible in this case. The regular fine lines through whole device and the voids in the solder layer also cause some difficulties during the scanning. For inspection of possible bond wire failure, the mold is to be removed.