

Meta-parameterisation of Power Semiconductor Devices for Studies of Efficiency and Power Density in High Power Converters

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Keywords

«Power semiconductor device», «IGBT», «IGCT», «Design», «High power discrete device»

Abstract

This paper presents a meta-parameterised approach for evaluation of power switch modules (PSMs) in high power converters (HPCs). General models and parameters for evaluation of power losses and volume of PSMs are presented. Then, meta-parameterisation is performed for the High Power Semiconductor Devices (HPSDs) that are commonly used in HPCs, considering two types of package, press-pack and module type, and including IGBT, IGCT and IEGT chip technologies. A comparative analysis based on current capability and its dependency with the frequency in voltage source converters is introduced for the considered HPSD technologies. Press-pack IGBT technology shows the higher current capability and power dissipation performance, so it can be good choice for increase the operative frequency in HPCs.

Introduction

The efficiency (η) and power density (ρ) of a High Power Converter (HPC) are highly influenced by the type of High Power Semiconductor Device (HPSD) selected for the high power switch module (PSM). HPSDs that are commonly used in HPCs include the Insulated Gate Bipolar Transistor (IGBT), the integrated Gate Commutated Thyristor (IGCT) and the Injection Enhanced Gate Transistor (IEGT) [1, 2, 3]. Normally, HPSDs based on different technologies (e.g. IGBT, IGCT, inter alia) are not available with the same ratings (blocking voltage capability V_{Block} and maximum current rating $I_{sw.mx}$), so the comparison of HPSDs to determine the best for a specific application is not easy and generally the comparison is done for a system specifications which favouring a HPSD over the others.

For example, in [1] and [2] the loss analysis and comparison of press-pack type HPSDs, 6.5kV/3800A IGCT, 4.5kV/2400A IGBT, 4.5kV/2100A IEGT, and a module type 6.5kV/750A IGBT for a 5MW back-to-back type 3LNPC Voltage Source Converter (VSC) is presented. The considered IGCT has been found to have the highest η as it was reported in [1]. However, the $I_{sw.mx}$ of the considered IGCT is around 60% higher than the considered IEGT (with 30% lower V_{Block}) and 5 times higher $I_{sw.mx}$ than the considered IGBT with the same V_{Block} . Since the conduction characteristic of HPSD improves as $I_{sw.mx}$ increases, the selection of the HPSD has favored to the IGCT technology in this case. So the conclusion reported in [1] is only valid for the considered HPSD and not for the HPSD-technology itself.

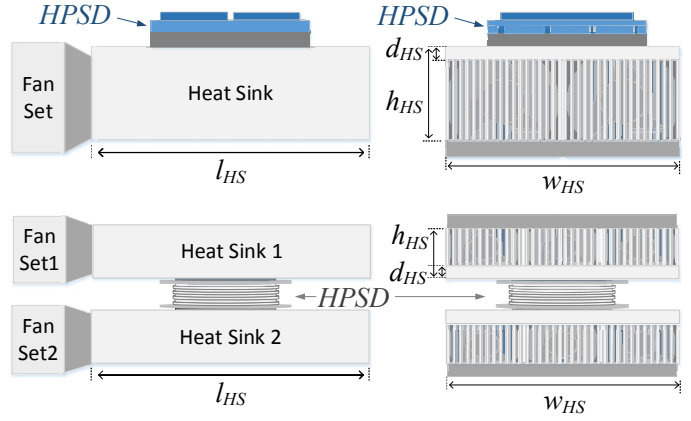
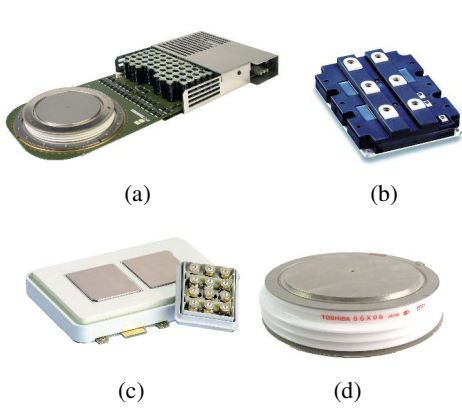


Fig. 1: Typical look of the considered HPSDs: a) IGCT[9], b) IGBT-M[9] or IEGT-M[10], c) IGBT-PP[9], and d) IEGT-PP[10]. Fig. 2: Schematic profile and cross-section of the considered CST for a HPSD: Module type (Top) and Press-Pack type (Bottom)

A more general comparative analysis can be carry out based on the meta-parameterisation of the HPSDs [4]. This method allows a better comparison since the results do not depend on a single HPSD but the family of HPSDs (HPSD-technology), so the analysis can detect the areas of application (power rating, operational frequency and voltage rating) where a semiconductor type and/or technology is better in a more general way. This paper presents the meta-parameterisation of five different HPSD technologies (press-pack IGBTs, module type IGBTs, press-pack IGCTs, press-pack IEGTs and module type IEGTs) to be used in studies of η and ρ of HPC. Then, figure of merit are defined to perform a comparative analysis of HPSDs from the point of view of technology and not using a discrete device approach.

Meta-Parameterisation of High Power Semiconductor Devices

HPSD modelling defines the related HPSD Parameters (HPSD-P) needed for the analytical evaluation of power losses and volume of the HPC. On the other hand, selection of a HPSD for a specific application is mainly determined by the required V_{Block} and $I_{sw.mx}$ that the HPSD should carry and switch off in the worst case scenario. Once the HPSD is selected, the HPSD-Ps are defined and the evaluation can be done. As follows, general models of HPSD are presented to define the main HPSD-Ps needed to evaluated its performance, and at the same time, it is shown how HPSD-Ps vary as function of V_{Block} and $I_{sw.mx}$, so it is possible to predict their values by the proposed models and therefore meta-parameterisation of HPSDs (parameterisation of the HPSD-Ps) can be performed.

In general, the following model is used to parameterise a given HPSD-P χ (meta-parameterize) as function of V_{Block} and $I_{sw.mx}$:

$$\chi = \chi_0 \cdot I_{sw.mx}^{\chi_1} \cdot V_{Block}^{\chi_2} \quad (1)$$

where the meta-parameters $\chi_{i=0...2}$ of the parameter χ are curve-fitting values, which depend on PSD technology. All meta-parameters are calculated by an iterative process in order to reduce the error of meta-parameter estimation and considering some assumptions, which are explained below.

Considered HPSD technologies

Three HPSD technologies commonly used in HPCs are considered in this paper, IGCTs, IGBTs and IEGTs. The IGBT and IEGT devices can be found in two different packages, module type and press-pack type. Since package technology influence thermal HPSD-Ps, even if same chip technology is used, then these two sub-technologies are considered in this paper. Therefore, in total, five different types of HPSD are meta-parameterised and compared. Fig. 1 shows the typical look of the considered devices.

The IGBT press-pack devices, StakPak, from ABB have been considered in order to extract the main properties and HPSD-Ps of IGBT Press-Pack (IGBT-PP) technology. In total, 7 StakPak devices are

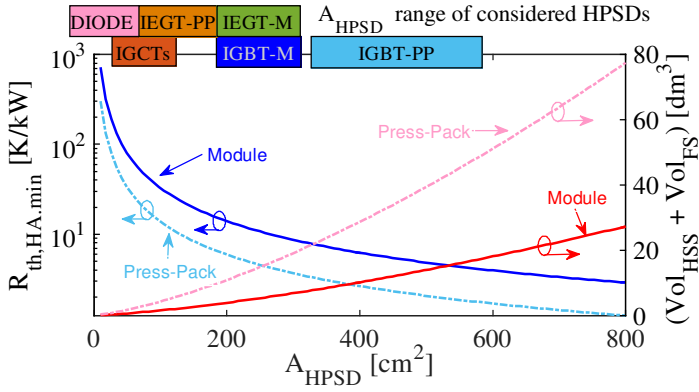


Fig. 3: $R_{th,HA,min}$ for the considered CST and its total volume as function of A_{HPSD} .

Table I: Heat Sink model parameters

Parameter	Value
K_{HS1}	45.3[mm · K/W]
K_{HS2}	0.164[mm · K/W]
K_{HS3}	12.51[mm ³ · K/W]
K_{HS4}	9.016[cm ² · K/W · s]
$K_{\delta A0}$	0.711
$K_{\delta A1}$	-0.1754
K_{FS0}	0.0176[m ³]
K_{FS1}	0.5304
Vel_{fan}	10[m/s]
$d_{HS,min}$	1[mm]
$l_{HS,max}$	$\approx 1.3 \cdot \sqrt{A_{HPSD}}$
$w_{HS,max}$	$\approx 1.3 \cdot \sqrt{A_{HPSD}}$
$h_{HS,max}$	0.5 · $w_{HS,max}$

Table II: Meta-Parameters for thermal evaluation

	Meta parameter	IGBT-M		IGBT-PP		IEGT-M		IEGT-PP		IGCT	DIODE
		AS	D	AS	D	AS	D	AS	D		
$R_{th,JH}$ [°C/W]	$R_{th,JH0}$.37e3	.79e3	.18e3	1.11e4	6.93e5	1.73e6	1.53e5	7.98e6	4.36	3.36e6
	$R_{th,JH1}$	-0.77	-0.80	-0.90	-0.40	-0.96	-0.96	-0.77	-0.96	-0.49	-0.74
	$R_{th,JH2}$	-0.47	-0.45	-0.35	-1.29	-1.23	-1.23	-1.26	-1.45	-0.21	-1.57
A_{HPSM} [m ²]	A_{HPSM0}	4.23e-7		8.10e-6		1.70e-5		8.43e-9		3.30e-5	7.1e-14
	A_{HPSM1}		0.772		0.772		0.328		0.653	0.435	0.797
	A_{HPSM2}		0.605		0.290		0.582		1.030	0.179	2.136
$T_{j,max}$ [°C]		150°C		125°C		125°C		125°C		125°C	115°C

available in 2.5kV and 4.5kV maximum blocking capability. On the other hand, the IGBT Module (IGBT-M) parameters have been calculated based on the HiPak IGBT Modules from ABB. In total, 18 HiPak devices are available with a V_{Block} from 1.7kV up to 6.5kV. Only devices from the last generation with the SPT+ chips technology from both sub-technologies, StakPak and HiPak IGBTs, have been considered.

The IEGT devices from TOSHIBA have been considered for both IEGT press-pack (IEGT-PP) and IEGT Module (IEGT-M) technologies. Five IEGT-PP devices are available with V_{Block} of 3.3kV and 4.5 kV. On the other hand, also five IEGT-M are available in TOSHIBA portfolio with V_{Block} from 1.7kV up to 4.5kV. All devices has the same IEGT chip technology.

Finally, the last generation of IGCTs devices from ABB portfolio, both RC-IGCTs (Reverse Conducting) and AS-IGCTs (Asymmetric) type, have been considered. The RC-IGCT is an IGCT with anti-parallel Free Wheel Diode (FWD) which is comparable with the considered IGBTs and IEGTs devices. However, only two RC-IGCTs devices are offered in ABB portfolio, which limit the meta-parameterisation process. Therefore, the AS-IGCT is the representative IGCT technology considered, and an external press-pack fast recovery diodes from ABB is considered to be connected in anti-parallel, as it is recommended from the manufacturer. The RC-IGCT electrical parameters are considered only to improve meta-parameters. In total, 7 IGCT devices and 9 press-pack diodes have been analysed.

Thermal Model and Cooling System

Average thermal model of the HPSD can be used to calculate the required heat-sink-to-ambient thermal resistance ($R_{th,HA,Rq}$) of the Cooling System Technology (CST) for the worse operating condition, and then size and weight of the CST can be estimated. For a HPSD composed by an Active Switch (AS) (i.e. IGBT or IEGT) and anti-parallel FWD, the $R_{th,HA,Rq}$ to guaranty do not excess the maximum junction

temperature of the HPSD ($T_{j,mx}$) can be estimate by:

$$R_{th,HA,Rq} = \frac{K_{sft}T_{j,mx} - T_a - \max(R_{th,JH,AS}P_{AS}, R_{th,JH,D}P_D)}{P_{AS} + P_D} \quad (2)$$

where P_{AS} and P_D are the power losses of the AS and FWD, respectively, K_{sft} is the safety factor of thermal design to take into account the dynamic variation of temperature in a period of time, T_a is the ambient temperature, $R_{th,JH}$ is the junction-to-heat-sink R_{th} calculated by adding the junction-to-case R_{th} (R_{thJC}) and the case-to-heat-sink R_{th} (R_{thCH}), given in the data-sheet of the PSD, for AS and FWD respectively.

On the other hand, two main types of CSTs are used in high power applications [5]: forced air cooling and liquid cooling. However, only forced air cooling system is considered in this paper. Fig. 2 shows the schematic profile of the Power Switch Module (PSM) with forced air CST considered in this paper, for module type HPSD (Fig. 2(top)) and press-pack type HPSD (Fig. 2(bottom)). Then, the volume of the PSM (Vol_{PSM}) defined in Fig. 2, can be approximated by the sum of HPSD volume (Vol_{HPSD}), the heat sink structure volume (Vol_{HSS}) and the fan set volume (Vol_{FS}). However, since Vol_{HPSD} is much smaller than Vol_{HSS} , normally it can be neglected.

For a given forced air CST, its nominal heat-sink-to-ambient thermal resistance ($R_{th,HA}$), Vol_{HSS} and Vol_{FS} are correlated and can be defined by its geometry. Additionally, the influence of the ratio between HPSD area (A_{HPSD}) and Heat Sink plate area (A_{HS}) ($\delta_A = A_{HPSD}/A_{HS}$) should be taken into account to rigorously compare different HPSDs. Then, based on analytical models reported in [5], and using the meta-parameterisation concept [4], the following simplified model is proposed:

$$R_{th,HA} = K_{HS0} + \frac{(K_{\delta A1} + (1 - K_{\delta A1})\delta_A)K_{HS4}l_{HS}}{w_{HS}l_{HS}(h_{HS} - d_{HS})Vel_{fan}\delta_A}, \quad (3)$$

$$K_{HS0} = \frac{(K_{\delta A0} + (1 - K_{\delta A0})\delta_A)(K_{HS1}d_{HS} + K_{HS2}(h_{HS} - d_{HS}) + \frac{K_{HS3}}{(h_{HS} - d_{HS})})}{w_{HS}l_{HS}\delta_A}, \quad (4)$$

$$Vol_{HSS} = l_{HS} \cdot w_{HS} \cdot h_{HS} \quad (5)$$

$$Vol_{FS} = K_{FS0}Vol_{HSS}^{K_{FS1}} \quad (6)$$

where Vel_{fan} is the lineal fan speed, and the parameters K_{HSi} , $K_{\delta Ai}$, and K_{FSi} are regression coefficients, whose can be found by taking data of heat sink structures and fans available in the market. The heat sink model parameters considered in this paper are presented in Table I.

By solving the set of equations 2-6, the Vol_{PSM} can be estimated for the worst case scenario in the converter design. It should be noted that for press-pack HPSD, two heat sink elements are used (see Fig. 2(bottom)), and each heat sink element is designed to achieve only $0.5 \cdot R_{th,HA,Rq}$. Additionally, CST limitations can be estimated for each HPSD technology by considering physical limits of heat sink structure. Fig. 3 shows the minimum thermal resistance ($R_{th,HA,min}$) achieved by the considered CST as function of A_{HPSD} for each type of HPSD package, when the limiting conditions specified in Table I are considered. It can be noted from Fig. 3 that press-pack package allows smaller $R_{th,HA,min}$ but with a bulky heat sink structure. Also, it should be noted that A_{HPSD} is an important parameter to determine the $R_{th,HA,min}$.

In total four thermal parameters should be estimated for a single HPSD: $T_{j,mx}$, $R_{th,JH,AS}$, $R_{th,JH,D}$ and A_{HPSD} . Fig 4 shows the thermal parameters as function of $I_{sw,mx}$ for different HPSDs types and V_{Block} values. All HPSDs offered by the manufacturer from the considered semiconductor technologies are plotted with marks, and the meta-parameterised models are plotted as dotted lines. The meta-parameters are summarised in Table II. In the case of $T_{j,mx}$, it is a fix value for a given HPSD technology, which is also reported in Table II.

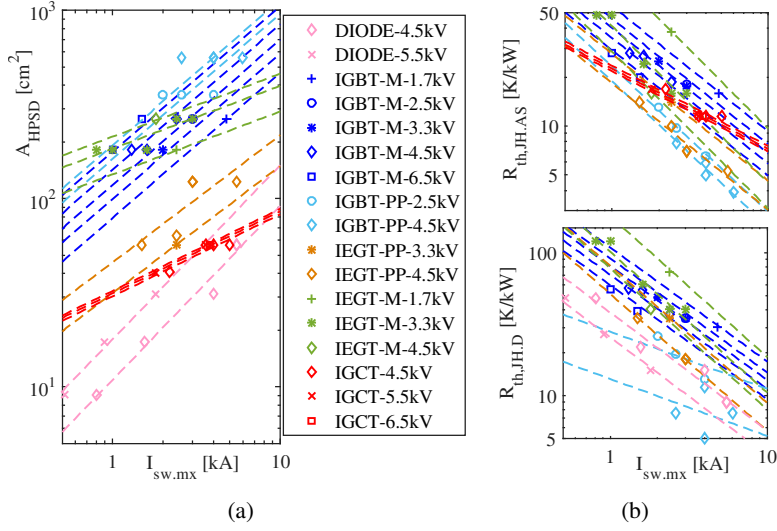


Fig. 4: Thermal Parameters: a) A_{HPSD} , b) $R_{th,JH}$.

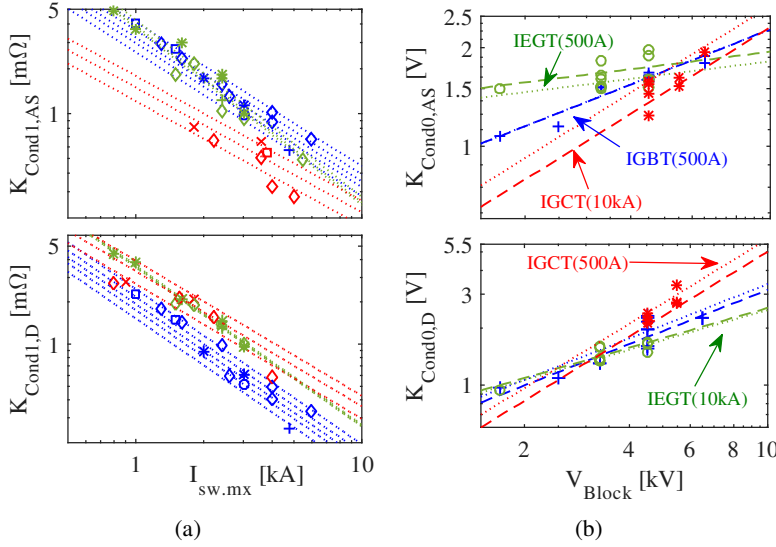


Fig. 5: Cond. Parameters: a) K_{Cond1} , b) K_{Cond0} .

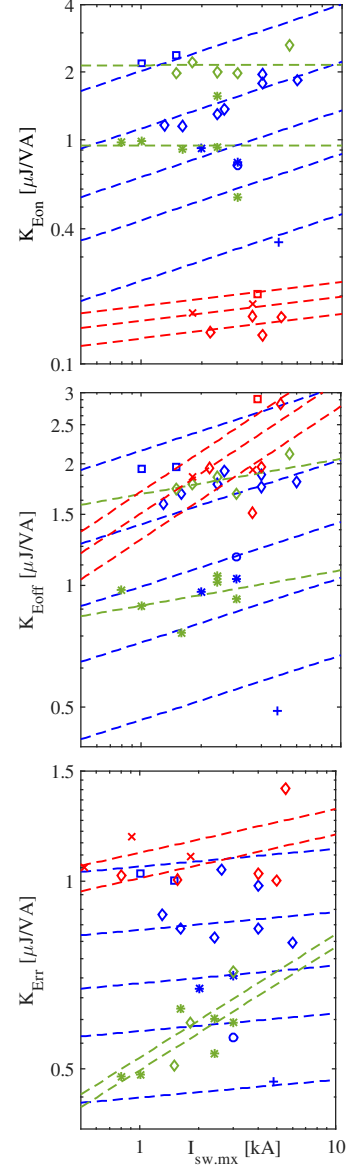


Fig. 6: Switching HPSD-P: K_{Eon} , K_{Eoff} , K_{Err} .

Semiconductor Losses

The components of power losses, P_{AS} and/or P_D , needed for evaluation of equation 2 are: conduction losses (P_{Cond}), switching losses (P_{SW}) (turn on and turn off) and blocking losses (P_{Block}). Generally, P_{Block} may be neglected in HPSDs at nominal operation [6].

The voltage-current characteristic of the HPSD (AS and D) is used to calculate P_{Cond} , and when it is approximated by a linear relation [11], P_{Cond} is estimated by

$$P_{Cond} = K_{Cond0} \cdot I_{SD,avg} + K_{Cond1} \cdot I_{SD,rms}^2 \quad (7)$$

where $I_{SD,avg}$ and $I_{SD,rms}$ are the average and R.M.S. current that the semiconductor is conducting in a period. The HPSD-Ps, K_{Cond0} (known as threshold voltage) and K_{Cond1} (known as on-state resistance), can be calculated using the data-sheet of each HPSD. These conduction parameters depends on junction temperature (T_j) and gate driver voltage (V_{GH}). Here, it is reported values for recommended V_{GH} of each HPSD at $T_{j,mx}$.

Table III: Meta-Parameters for Power Loss evaluation.

	Meta parameter	IGBT		IEGT		IGCT	DIODE
		AS	D	AS	D		
K_{Cond0} [mV]	K_{Cond00}	45.9	5.214	2.25e3	5.788	7.877	0.263
	K_{Cond01}	-3e-4	-0.0231	-0.095	0.034	-0.050	-0.0512
	K_{Cond02}	0.424	0.7191	0.045	0.6499	0.667	1.122
K_{Cond1} [mΩ]	K_{Cond10}	161.31	214.96	279.25	5.204e3	0.0537	0.367
	K_{Cond11}	-0.965	-1.106	-1.070	-1.131	-0.836	-0.962
	K_{Cond12}	0.340	0.362	0.389	0.067	1.057	1.027
K_{Eon} [μJ/VA]	K_{Eon0}	1.92e-7	–	3.97e-10	–	3.176e-5	–
	K_{Eon1}	0.2975	–	1.4e-3	–	0.108	–
	K_{Eon2}	1.608	–	2.663	–	0.899	–
K_{Eoff} [μJ/VA]	K_{Eoff0}	3.14e-5	3.3e-3	3.07e-8	0.0373	2.676e-4	0.012
	K_{Eoff1}	0.1596	0.0285	0.0873	0.1974	0.3292	0.0698
	K_{Eoff2}	1.143	0.6357	2.0467	0.1514	0.7387	0.4695

Fig. 5 shows the calculated conduction HPSD-Ps for all the considered HPSDs (marks) and the approximated models by meta-parameters of Table III. In the case of IGBT and IEGT technologies, it has been considered that these parameters depends on chip technology and are not influenced by the HPSD package, then conduction HPSD-Ps for module type and press-pack type HPSDs are considered to be correlated and therefore all HPSDs are used to calculated meta-parameters for each chip technology.

On the other hand, the average P_{SW} over a complete fundamental period (T) may be calculated by summing all the commutation energy losses (E_{SW} : E_{ON} and E_{OFF}) of the HPSD during a respective interval of time. In order to model E_{SW} and according to the data commonly reported in the data-sheet of the HPSDs, a slightly simpler loss model that involves only linear functions can be used with a quite high engineering accuracy[1]

$$P_{\text{SW}} = \frac{1}{T} \sum (E_{\text{ON}(j)} + E_{\text{OFF}(j)}) \quad (8)$$

$$E_{\text{SW}} = K_{\text{E}} \cdot i_{\text{sw}} \cdot v_{\text{bk}}; \dots (K_{\text{E}} = \frac{E_{\text{test}}}{I_{\text{test}} \cdot V_{\text{test}}}) \quad (9)$$

where i_{sw} is the current through the device after turn-on or before turn-off action (i_{sw} : i_{ON} or i_{OFF}), v_{bk} is the voltage that the HPSD is blocking and the values of E_{test} , I_{test} and V_{test} can be found in the data-sheet of the HPSD foer each type of commutation, turn on (K_{Eon}), turn off (K_{Eoff}) or reverse recovery (K_{Err}) in diodes. For applications with a switching frequency (f_{sw}) much higher than the fundamental frequency ($f = 1/T$), the following simplification can be done

$$P_{\text{SW}} = (K_{\text{Eon}} + K_{\text{Eoff}}) \cdot f_{\text{sw}} \cdot I_{\text{sw,avg}} \cdot V_{\text{bk,avg}} \quad (10)$$

where $V_{\text{bk,avg}}$ is the average voltage than the HPSD should block and $I_{\text{sw,avg}}$ is the average current through the device before turn off and after turn on action. The parameters K_{Eon} and K_{Eoff} depends mainly on gate driver circuit configuration (gate resistance) and T_j . Here, recommended gate circuit configuration according with reported test values in data-sheets at $T_{j,\text{mx}}$ are considered, and Fig 6 summarises the calculated switching HPSD-Ps for all the considered HPSDs and the approximated models by meta-parameters of Table III. The same consideration as for conduction HPSD-Ps regarding chip technology of IGBTs and IEGTs, has been considered for switching HPSD-Ps. All IGBTs (IGBT-M and IGBT-PP) are plotted in blue color, and all IEGTs (IEGT-M and IEGT-PP) are plotted in green color.

Additional considerations regarding IGCT technology

IGCTs are characterised by a hard drive concept, which requires the mechanical integration of gate driver and semiconductor into one single unit[8]. However, this integration also introduce an extra consideration compare with IGBT or IEGT technologies, since the total power consumption of the IGCT gate unit is

Table IV: Meta-Parameters for IGCT gate unit evaluation.

Meta parameter		Value
K_{PG0} [W]	K_{PG00}	14.414
	K_{PG01}	-0.0243
	K_{PG02}	-0.0316
K_{PG1} [mJ]	K_{PG10}	4.885e-3
	K_{PG11}	0.6513
	K_{PG12}	0.4539
K_{PG2} [μJ/A]	K_{PG20}	6.33e-6
	K_{PG21}	0.8692
	K_{PG22}	1.0709
K_{IF0} [A]	K_{IF00}	-74.01
	K_{IF01}	-0.5021
	K_{IF02}	0.6205
K_{IF1} [kA/√s]	K_{IF10}	3.79e4
	K_{IF11}	-0.4328
	K_{IF12}	-0.3355

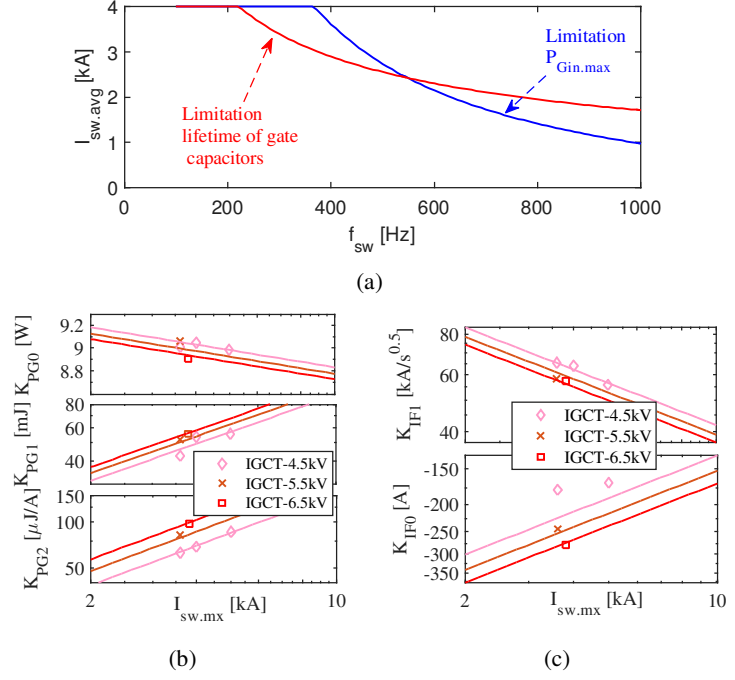


Fig. 7: IGCT Gate HPSD-Ps: a) $I_{sw,avg}$ vs f_{sw} for a 4.5kVx4kA IGCT, b) Gate Losses HPSD-Ps, c) Gate unit lifetime HPSD-Ps

strongly load dependent. The average turn-off current $I_{sw,avg}$, f_{sw} , T_j and HPSD technology (gate charge) are the parameters with major influence on gate power consumption (P_{Gin}). For a given IGCT, it is proposed to model P_{Gin} at $T_{j,max}$ by

$$P_{Gin} = K_{PG0} + K_{PG1} \cdot f_{sw} + K_{PG2} \cdot f_{sw} \cdot I_{sw,avg} \quad (11)$$

where K_{PGi} are curve fitting parameters from P_{Gin} vs. $I_{sw,avg}$ curves at different f_{sw} reported in the IGCT data-sheets. Since the operational gate unit supply power is limited ($P_{Gin} < P_{Gin,max}$), then the operating range ($I_{sw,avg}$, f_{sw}) is also limited. A fixed $P_{Gin,max}$ of 130 W is considered for the IGCT technology.

Additionally, since electrolytic capacitors are incorporated in the IGCT gate unit, then power losses in these capacitors and the T_a become important parameters which affect ageing of the gate unit[8]. Normally, IGCT manufacturer includes $I_{sw,avg}$ vs. f_{sw} curves for electrolytic capacitors lifetime of 20 years at different T_a . It is proposed to model this limitation by

$$I_{sw,avg,LT} = \frac{K_{IFTa1}}{\sqrt{f_{sw}}} + K_{IFTa0} \quad (12)$$

where $I_{sw,avg,LT}$ is the maximum $I_{sw,avg}$ allowed as function of f_{sw} for a 20 years lifetime of gate capacitors, and K_{IFTa1} , K_{IFTa0} are curve fitting parameter of the data-sheet plots at a given T_a . In order to simplify the evaluation, a fixed T_a of 40°C is considered in this paper. Fig. 7(a) shows an example of IGCT gate limitations for a 4.5kVx4kA IGCT, where both limitations, gate power consumption and lifetime operation, are plotted. Fig 7(b) and Fig. 7(c) show the IGCT gate unit parameters of the considered IGCTs for evaluation of P_{Gin} and $I_{sw,avg,LT}$, respectively. Calculated meta-parameters are reported in Table IV

Comparative Analysis of HPSD technologies

The proposed meta-parameterisation approach allows to analyse HPSD technologies to find out the trends of the HPSD-P beyond the available HPSDs in the market. However, comparing HPSDs through parameter-by-parameter comparison is impractical and not useful at all. Instead, some figure of merit can be defined to compare HPSDs technologies in a general way. The comparison is performed for different

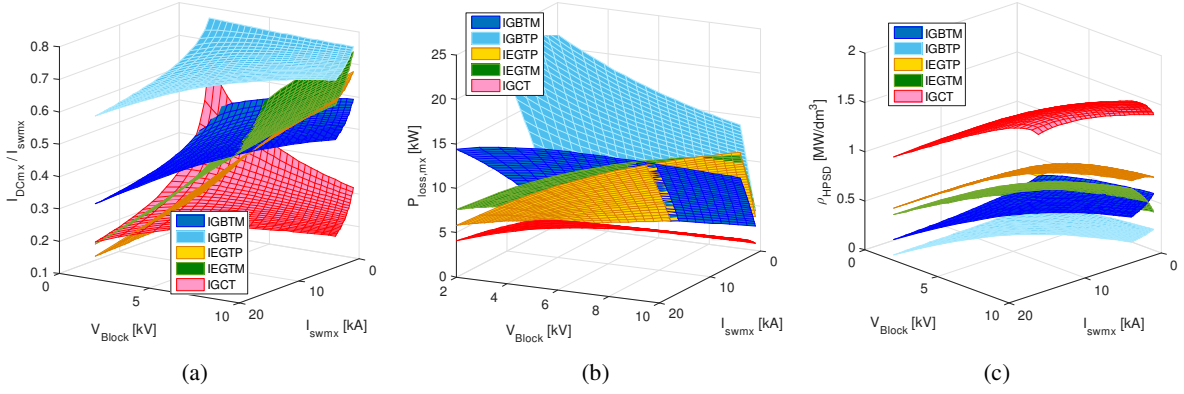


Fig. 8: Comparison of DC current Capability. (a) $I_{DC,mx}$. (b) $P_{Loss,mx}$, (c) ρ_{HPSD}

virtual HPSD, which are evaluated by the calculated metaparameters. A maximum switching power capability (defined as $S_{VA} = 0.5 \cdot I_{sw,mx} \cdot V_{Block}$) of 20 MVA is considered for all HPSD technologies in order to do not evaluate any virtual HPSD too far from the initial set of HPSD.

DC Current capability

Current capability of a HPSD is defined like the maximum current that the HPSD can carry out without excess its $T_{j,mx}$ for some given conditions[8]. This value differs from its $I_{sw,mx}$, and it is mainly limited by the thermal properties of the HPSD. For a given HPSD, the maximum average power ($P_{loss,mx}$) that the HPSD can handle without overpass $T_{j,mx}$, can be estimated by

$$P_{Loss,mx} = \frac{T_{j,mx} - T_C}{R_{th,JC}} = \frac{T_{j,mx} - T_a}{R_{th,HA} + R_{th,JH}} \quad (13)$$

The DC current capability ($I_{DC,max}$) of a HPSD can be estimated by considering operation at very low frequency (negligible switching losses), so only P_{Cond} should be dissipated by HPSD, therefore:

$$I_{DC,mx} = \frac{-K_{Cond0} + \sqrt{K_{Cond0}^2 + 4P_{Loss,mx}K_{Cond1}}}{2 \cdot K_{Cond1}} \quad (14)$$

Fig 8(a) shows the normalised $I_{DC,mx}$ for different virtual HPSDs from each HPSD technology, when $R_{th,HA,min}$ (from Fig 3) is considered and a $T_a = 40^\circ C$. Fig 8(b) shows the $P_{Loss,mx}$ of each virtual HPSD for the considered conditions. It can be noted from Fig. 8(a) that IGBT-PP technology has higher $I_{DC,mx}$ for all the range of considered virtual HPSDs, which is correlated with results from Fig 8(b), where thermal properties of IGBT-PP allows to dissipate higher losses and therefore conduct higher DC currents. It can also be noted that the ratio $I_{DC,mx}/I_{sw,mx}$ decreases as $I_{sw,mx}$ increases for all technologies, and slightly increases as V_{Block} increases, except for IGCTs. IEGT technology shows comparable $I_{DC,mx}$ for high voltage HPSDs. IGCT shows the lowest $I_{DC,mx}$ for high voltage and/or high current HPSDs. This can be explained by the trend of IGCTs to be compact HPSDs and therefore thermal manage is limited. Additionally, the calculated switch power density ($\rho_{HPSD} = S_{VA}/Vol_{PSM}$) is plotted in Fig. 8(c). As it can be expected, IGCTs have the higher ρ_{HPSD} , since they have limited $P_{Loss,mx}$. However, IEGT-PP technology shows high ρ_{HPSD} with high $P_{Loss,mx}$, which means that IEGT-PP technology has a good trade-off between thermal and conduction parameters.

Current capability vs frequency

On the other hand, considering that the HPSD is conducting a half-sinusoidal current under switching operation such that conduction and switching losses are in balance ($P_{Cond} = P_{SW}$), two figures of merit can be defined, the balance peak current capability (I_{peakB}) and the balance switching frequency (f_{swB}),

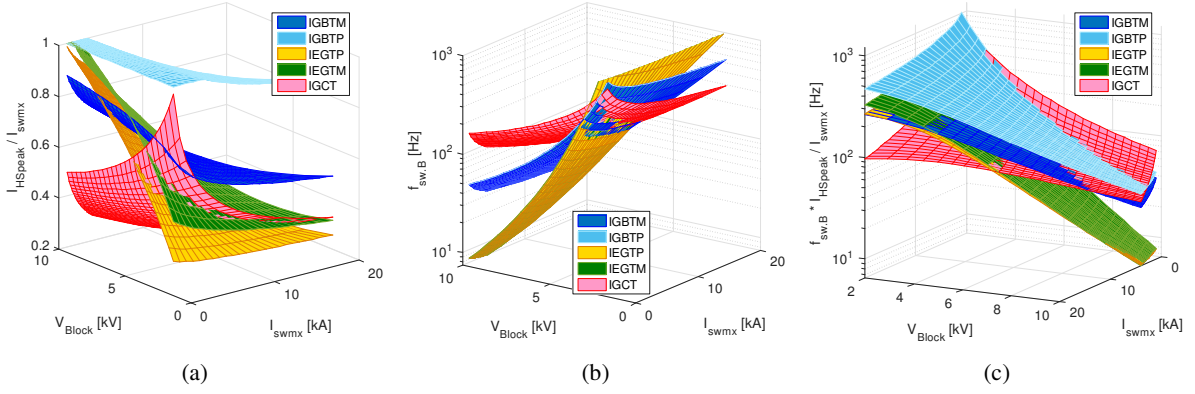


Fig. 9: Comparison of trade-off between peak current capability and switching frequency. (a) Normalized I_{peakB} . (b) f_{swB} . (c) $I_{\text{peakB}} \cdot f_{\text{swB}}$

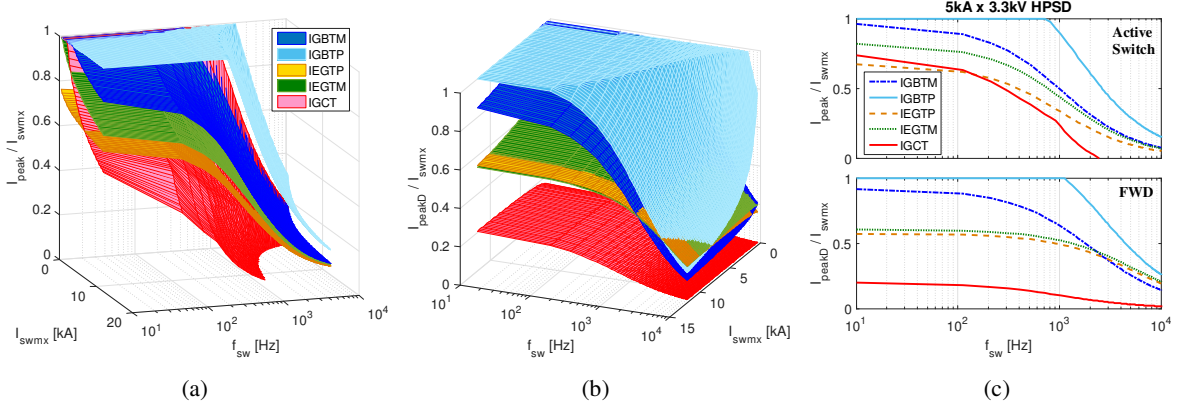


Fig. 10: Peak current capability as function of f_{sw} for 3.3kV class HPSDs. (a) Normalized I_{peak} . (b) Normalized I_{peakD} , (c) Comparison of current capability for 5kA x 3.3kV HPSDs

which can be calculated as follows:

$$I_{\text{peakB}} = \frac{-K_{\text{Cond0}} + \sqrt{K_{\text{Cond0}}^2 + 0.5\pi P_{\text{Loss,mx}} K_{\text{Cond1}}}}{0.5\pi K_{\text{Cond1}}}; \quad f_{\text{swB}} = \frac{\pi K_{\text{Cond1}} I_{\text{peakB}} + 4K_{\text{Cond0}}}{4(K_{\text{Eon}} + K_{\text{Eoff}}) V_{\text{bk,avg}}} \quad (15)$$

Fig. 9 shows the evaluation of these indicator for the considered range of HPSDs. In all cases, the average V_{Block} is considered as 65% of the V_{Block} . It can be noted from Fig. 9(a), that as in the case of $I_{\text{DC,mx}}$, IGBT-P allows higher values of I_{peakB} , with a considerable difference in all the analysed range of HPSDs, except for high V_{Block} HPSDs. This result is linked to the good thermal properties of IGBT-P HPSDs. However, by analysing the results from Fig. 9(b), it can be noted that f_{swB} has a strong dependence on V_{Block} , so high voltage HPSDs are more limited in frequency operation than high current HPSDs. Also, it can be noted that IGCTs shows better properties for high frequency-voltage operation. Additionally, it should be noted that the point of balance between switching and conduction losses is at frequencies lower than 800 Hz, even for low voltage low current HPSDs. The product $I_{\text{peakB}} \cdot f_{\text{swB}}$ can be used as figure of merit in order to compare HPSDs targeting for high f_{sw} applications. Fig. 9(c) shows the balance trade-off between current capability and switching frequency operation. It can be observed that IGBT-P shows a better trade-off for HPSDs with higher ratings, and IGCTs shows good performance for medium voltage medium frequency operation.

Finally, current capability dependence with f_{sw} is evaluated for different HPSDs with fixed V_{Block} , equal

to 3.3kV. Fig. 10(a) and Fig. 10(b) show the maximum peak current I_{peak} for the AS and FWD of the 3.3kV HPSDs with different $I_{\text{sw.mx}}$. It can be noted that IGBT-PP allows used $I_{\text{sw.mx}}$ at higher frequencies in both AS and FWD. Also, the considered FWD for IGCT technology shows the lowest current capability for 3.3kV HPSDs. Detailed comparison for a single HPSD from each technology with the same nominal ratings of 5kA x 3.3kV is presented in Fig. 10(c), for AS (top) and FWD (bottom). Only the considered HPSD from IGBT-P technology is able to operated at $I_{\text{sw.mx}}$ up to around 700 Hz and 1 kHz for AS and FWD, respectively. IGBT technology shows the better performance at the considered current and voltage ratings.

Conclusion

This paper reports the main parameters of the HPSD commonly used in HPC. Meta-parameterised models of HPSD-Ps has been introduced, so the reader can use this information in order to evaluate HPSDs if he attempts to evaluate the η and ρ of a HPC based on HPSD-technology and not only with a single HPSD. Five HPSD technologies have been considered: module type IGBTs, press-pack IGBTs, IGCTs, press-pack IEGTs and module type IEGTs.

It was found that press-pack IGBTs has high current capability for all the range of considered HPSDs ratings, mainly because its good thermal properties, like big package area and very low interface thermal resistance, which allows to dissipate higher losses compare with the other technologies. However, it was found by checking the f_{swB} that IGCTs presents the best trade-off between conduction and switching paramaters, and this technology shows good properties for high voltage medium frequency (between 200 Hz and 500 Hz) applications.

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