NTNU – Trondheim
Norwegian University of
Science and Technology

An Ultra-Low Power SAR-ADC in 65 nm CMOS Technology

Simon Josephsen

Master of Science in Electronics
Submission date: June 2013
Supervisor: Trond Ytterdal, IET

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

Problem Description

The objective of this project is to design an energy efficient 1kS/s, 9-bit SAR-ADC in 65nm CMOS technology. The main performance parameter is energy efficiency (FOM) and area.

The project consists of the following tasks:

- Perform a literature survey of SAR ADCs to establish current state-of-the-art
- Analyze and compare published work
- Based on above, choose an ADC architecture
- Design and layout the ADC at transistor level and characterize the performance by simulation.

The specifications are as follows:

CMOS technology:	STM 65nm
Supply voltage:	Maximum 1V
Maximum input level (FSR):	1V peak-to-peak single-ended
Resolution:	9-bit
ENOB:	>8 bit
Sampling frequency:	1 kHz

Assignment given: January 16, 2013
Supervisor: Trond Ytterdal, IET

Abstract

This master's thesis presents the design, implementation and layout of an ultra-low power 9-bit 1 kS/s successive approximation register (SAR) analog-to-digital converter (ADC) in 65 nm CMOS technology. The proposed ADC operates with a supply voltage of 400 mV and the post-layout simulation resulted in a power consumption of 1.22 nW, which is among the best of the currently state-of-the-art ultra-low-power ADCs. Ultra-low power consumption is achieved by utilizing low power transistors with high threshold voltage to minimize leakage power, optimizing the control logic for sub-threshold operation and using a reference digital-to-analog converter with a monotonic switching procedure. The power consumption and resolution of the ADC is mainly limited by the comparator, however, an effective resolution of 8.16 bits is achieved, which results in a figure-of-merit of 4.27 fJ/conversion-step.

Sammendrag

Denne masteroppgaven presenterer design, implementering og utlegg av en ultra-laveffekt 9-bit 1 kS/s suksessiv-tilnærmingsregister (SAR) analog-til-digital omformer (ADC) i 65 nm CMOS-teknologi. Den foreslåtte ADC'en opererer med en spenning på 400 mV og simulering på utlegget resulterte i et strømforbruk på 1,22 nW, som er blant de beste av dagens beste ultra-laveffekt ADC'er. Ultra-lavt effektforbruk er oppnådd ved å utnytte laveffekt-transistorer med høy terskelspenning for å minimere lekkasjestrømmen, optimalisere styrelogikken for å fungere ved sub-terskel forsyningsspenning og ved hjelp av en digital-til-analog omformer med en monoton veksling. Energiforbruket og oppløsningen til ADC'en er hovedsakelig begrenset av komparatoren, imidlertid er en effektiv oppløsning på 8,16 bit oppnådd, noe som resulterer i et godhetstall på 4,27 fJ/konvertering.

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of Master of Science (MSc) at the Department of Electronics and Telecommunications, Norwegian University of Science and Technology (NTNU). The work was carried out in the period January to June 2013, under the supervision of Professor Trond Ytterdal, who is with the Department of Electronics and Telecommunications at NTNU.

Acknowledgments

First and foremost I would like to thank my supervisor, Professor Trond Ytterdal. He has been extremely motivating ever since he introduced me for design of analog integrated circuits. During the work with this thesis, he has been very supportive and has given me lots of good advice. I would also like to thank Professor Snorre Aunet for many useful comments and Hanne Bjerke for feedback on the report.

Simon Josephsen
Trondheim, June 2013

Contents

List of Figures

List of Tables

Abbreviations

ADC	Analog-to-Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DFF	D flip-flop
DIBL	Drain Induced Barrier Lowering
DNL	Differential Nonlinearity
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FOM	Figure-of-Merit
GP	General Purpose
IC	Integrated Circuit
INL	Integral Nonlinearity
LP	Low Power
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field-Effective Transistor
MSB	Most Significant Bit
NMOS	n-channel MOSFET
PMOS	p-channel MOSFET
RMS	Root Mean Square

RNCE	Reverse Narrow Channel Effect
S/H	Sample-and-hold
SAR	Successive Approximation Register
SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion

Chapter 1

Introduction

The main objective of this master's thesis is to design and implement an analog-to-digital converter (ADC) with 9-bit resolution running at 1 kS/s while minimizing the power consumption. An ADC is the main interface between the real analog world and the digital computer world. Consequently, ADCs are widely used in electronic devices, especially in sensors and radios where information is captured from an analog component and converted into a digital representation. Nowadays there is an increasing trend to make wireless sensors that are powered by battery or an energy harvester. Such devices can be used in several applications, with different requirements for sampling rate, resolution and power consumption. Medical devices, such as pacemakers and cardiac defibrillators, that are implanted into the human body, have strong requirements to power consumption to limit the number of surgeries. Reducing the power consumption of the device will not only increase the lifetime of the battery, but also provide opportunities for alternative energy sources through energy harvesters. An example is the endocochlear potential that is found in and actively maintained by the inner ear [3]. However, the ADC is one of the main components for measuring various electrophysiological signals and as an analog component, the ADC is inherently energy hungry compared to pure digital circuitry. Consequently, energy savings in an ADC will provide significant improvements in the total power consumption of an entire system. In the microcontroller industry, a popular trend to achieve low power consumption is to keep the chip in "sleep-mode" most of its standby time, and operation is happening periodically. An ultra-low power ADC can then be used to wake up the entire system only when it is necessary, for example when the ADC has sensed a certain pattern. However, the opportunities with ultra-low power ADCs are endless.

To meet the ultra-low power requirements, the successive approximation register (SAR) ADC is one of the most popular ADC architectures. As well as low

power consumption, SAR-ADCs can provide reasonably high sampling frequencies and relatively high accuracy. A comparison of published papers on ADCs [1] shows that the SAR architecture has best low power performance and figure-of-merit (FOM). Figure-of-merit is a measurement of the energy efficiency of an ADC where parameters as power consumption, effective resolution and sampling speed are taken into account. Minimizing the power consumption and maximizing the effective resolution and sampling speed will result in an improvement in FOM as it is defined

$$\text{FOM} = \frac{P_{\text{tot}}}{2^{ENOB} \cdot f_{\text{s}}} \, [\text{J/conversion} - \text{step}] \tag{1.1}$$

where P_{tot} is the total power consumption, ENOB is the effective number of bits while f_{s} is the sampling frequency. The currently best published FOM is 2.2 fJ/conversion-step [4], while the lowest power consumption published is 3 nW [5]. However, both architectures were SAR-ADCs, which proves the energy efficiency and ultra-low power capabilities of the SAR architecture.

1.1 Main Contributions

This thesis presents an ADC with lower power consumption than what is ever published to the best of the author's knowledge. This is achieved by:

1) reducing the supply voltage down to 400 mV, without losing any performance,
2) use of high threshold and low power transistors to reduce leakage,
3) custom logic gates for better sub-threshold performance, as presented in [6],
4) use of a monotonic switching algorithm in the reference DAC.

1.2 Thesis Outline

The following presents the organization of the thesis.

Chapter 2 provides the background theory that is necessary to understand the work done in this thesis. The first part presents fundamental theory for data converters, non-idealities, power consumption and sub-threshold theory for CMOS circuit presented. Then, the SAR-ADC and its building blocks are described. Lastly, layout techniques for sub-100 nm technology are presented.

Chapter 3 is presenting the state-of-the-art within ultra-low power analog-to-digital converters, and which techniques that are used to reduce the power consumption while not degrading the performance.

Chapter 4 presents the design mythology for the proposed design presented in this thesis and each building block is described into detail.

Chapter 5 shows the layout of the proposed design and describes how the custom-made DAC is laid out.

Chapter 6 presents the final simulation results of the proposed SAR-ADC, on both schematics and post-layout.

Chapter 7 analyzes and discusses the results obtained. The proposed design is compared with other ultra-low power ADCs and future work and improvements are discussed.

Chapter 8 concludes this thesis based on the previous discussion.

Chapter 2

Theoretical Background

This chapter briefly describe the necessarily background theory for this thesis. Theory to understand data converter fundamentals, non-idealities, power consumption and sub-threshold operation in CMOS circuits is presented. Lastly, the successive approximation register ADC and layout techniques for sub-100 nm CMOS technology are presented.

2.1 Data Converter Fundamentals

Analog-to-digital conversion is the process where a signal with continuous time and amplitude is transformed into a digital representation where time and amplitude are discrete. Conversion is done periodically with a period T_s, and the amplitude is quantified into 2^N levels, where N is the resolution of the ADC. Figure 2.1 shows the relation between an analog sinusoidal and its digital representation marked as red dots, quantified with $N = 2$. The quantification levels are relative to a reference voltage V_ref and each level is defined,

$$V_\mathrm{lsb} \triangleq \frac{V_\mathrm{ref}}{2^N}\,[\mathrm{V}]. \tag{2.1}$$

This makes a change in one V_lsb equally to a change in one least significant bit (LSB) in the digital word. The transfer function for an ideal ADC is given by

$$V_\mathrm{ref} \sum_{i=1}^{N} b_i \cdot 2^{-i} = V_\mathrm{in} \pm V_\mathrm{q}, \tag{2.2}$$

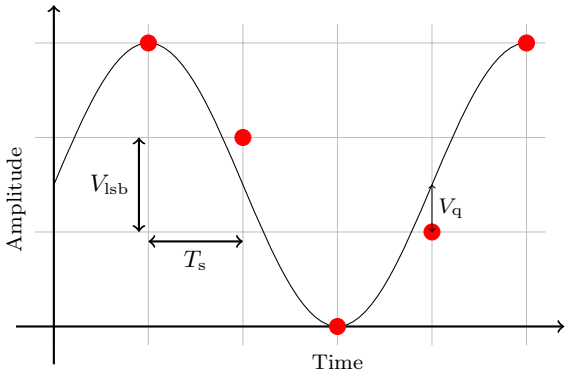


FIGURE 2.1: Analog-to-digital conversion.

where b_i is the binary output value for bit i, V_{in} is the input signal and V_{q} is the quantization error. V_{q} is shown in Figure 2.1, and is the difference between the actual sampled input signal and the nearest quantification level. For an ideal ADC this error is limited to $\pm V_{\text{lsb}}/2$, hence the quantization noise power is given by [7]

$$\overline{V_{\text{q}}^2} = \frac{V_{\text{ref}}^2}{12} 2^{-2N}, \tag{2.3}$$

which implies that quantization error only exists for signals that have been influenced by digitizing, i.e. $\overline{V_{\text{q}}^2} \to 0$ as $N \to \infty$. By assuming V_{in} to be a sinusoidal waveform between 0 and V_{ref}, the signal-to-quantization noise ratio (SQNR) can be derived [7]

$$\text{SQNR} = 6.02N + 1.76\,[\text{dB}]. \tag{2.4}$$

Physical non-idealities will contribute to a degradation of the signal power and affect the effective resolution of the ADC. It is therefore useful to define the effective number of bits (ENOB) of an ADC

$$\text{ENOB} = \frac{\text{SNDR} - 1.76\ \text{dB}}{6.02}\,[\text{bits}], \tag{2.5}$$

where SNDR is the signal-to-noise-and-distortion ratio, i.e. the ratio of the signal power to the total noise and distortion power given in dB [7].

The performance of an ADC is often characterized by the ENOB, in addition the offset and gain error as well as integral nonlinearity (INL) and differential nonlinearity (DNL) are also commonly used for a more detailed performance characterization. The offset error for an ADC is the output-code deviation from $\frac{1}{2}$LSB when the output code is '0 . . . 01', while the gain error is the difference at full-scale output

between the ideal and actual curves when the offset error is removed. Hence [7],

$$E_{\text{off(ADC)}} = \frac{V_{0\ldots01}}{V_{\text{LSB}}} - \frac{1}{2}\text{LSB}, \tag{2.6}$$

and

$$E_{\text{gain(ADC)}} = \left(\frac{V_{1\ldots1}}{V_{\text{LSB}}} - \frac{V_{0\ldots01}}{V_{\text{LSB}}}\right) - (2^N - 2). \tag{2.7}$$

The INL is defined to be the deviation of an ADC's input-output relationship away from the ideal linear relationship, while DNL is defined as the variation in analog steps away from 1 LSB. Both INL and DNL are measured when offset and gain errors are removed [7].

2.2 Non-Idealities

Thermal noise

Generally in electrical circuits the flow of current is associated with noise, moreover only capacitors is free of generating noise, but do accumulate noise generated by other sources. Thermal noise is the most common form of noise, is due to from the Brownian motion[1] of the charge carriers in a conductor [8]. This makes it dependent of temperature and it is assumed to have a uniformly frequency distribution. The thermal noise is given by

$$\overline{V_{\text{t}}^2} = \frac{kT}{C_{\text{s}}}\,[\text{V}], \tag{2.8}$$

where k is Boltzmann's constant, T is the temperature in degrees Kelvin and C_{s} is the capacitor where noise is accumulated [7].

Flicker noise

Another noise source that appears in many forms in nature is the flicker noise. The origins of flicker noise are disputed, but the most common explanation assumes that carriers are trapped and released in charge traps [8]. However, in electronic devices it does show up as a low-frequency phenomenon and it is approximated by

$$\overline{V_{\text{f}}^2} = \frac{k_{\text{v}}^2}{f}, \tag{2.9}$$

where k_{v} is a constant [7].

[1] The presumably random moving of particles suspended in a fluid resulting from their bombardment by the fastmoving atoms or molecules in the gas or liquid.

Process Variation and Mismatch

During fabrication silicon wafers are influenced by process variations. Since the temperature is not constant during each step of the manufacturing process, there will be variation in the oxide thickness and the dopant concentration, which will influence the transistor parameters [7]. For example the threshold voltages of PMOS and NMOS transistor will be smaller or greater than designed and the variation is independent between PMOS and NMOS. This may cause the performance of the circuit and in the worst case, the circuit will not be operational at all. However, process variation is always present and cannot be eliminated, but it can be modeled and should be taken into account when designing CMOS circuits.

Lithographic techniques are used to produce circuits and due to limited accuracy in the equipment, there will be variations in the shape of the device that is being produced. Consequently, the effective sizes and electrical properties of the component produced can differ from those intended by the designer. A different size in a certain component will cause a mismatch between the component and the other components in the circuits. Mismatch is critical for circuits such as current mirrors and differential pairs, where some of the main components must be equal in order to maintain the functionality of the circuit. There are several factors that contribute to a random variation in device parameters, however, the variation is predicted to be a Gaussian distribution with a mean value zero and a variation proportional to the inverse of $\sqrt{WL}$, where W and L are the device width and length, respectively [9].

2.3 Power Consumption

A CMOS circuit is consuming power when electrical charges stored on capacitive nodes are discharged to ground. Whenever a logic gate in a digital circuit is switched, dynamic power (P_{dyn}) is consumed, as capacitive loads are being charged and discharged. P_{dyn} is dependent of the switching activity, α, the clock frequency, f_{clk}, the total load capacitance, C_{load}, and the supply voltage V_{DD}.

During a transition in a gate, for instance the inverter in Figure 2.2, both PMOS and NMOS transistors will be on for a period t_{sc} when the input voltage is about $V_{\text{DD}}/2$. This will cause a short circuit from V_{DD} to ground, such that a current I_{peak} will be lost and short circuit power (P_{sc}) is dissipated. With fast transitions P_{sc} will be small can be almost neglected.

Another source of power dissipation is the leakage power, or the static power P_{stat}. Leakage originates from the sub-threshold current, I_0, in transistors that are switched off [8]. Moreover, leakage is critical for circuits that operate with lower clock frequencies, or circuits that are sleeping for most of their standby time.

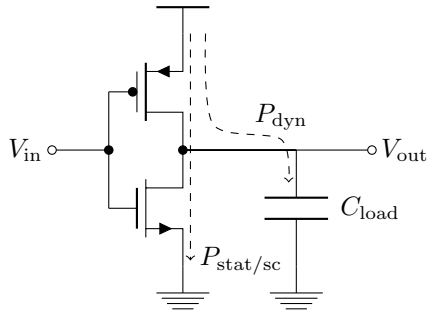


FIGURE 2.2: Power model.

Summarized, the total power consumption of a digital CMOS circuit is given by

$$P_{\text{tot}} = \underbrace{\alpha \cdot f_{\text{clk}} \cdot C_{\text{load}} \cdot V_{\text{DD}}^2}_{P_{\text{dyn}}} + \underbrace{f_{\text{clk}} \cdot t_{\text{sc}} \cdot I_{\text{peak}} \cdot V_{\text{DD}}}_{P_{\text{sc}}} + \underbrace{V_{\text{DD}} I_0}_{P_{\text{stat}}}. \tag{2.10}$$

2.4 Sub-Threshold

An efficient method to reduce power consumption is to decrease the supply voltage, V_{DD}. Equation (2.10) shows that the dynamic power is reduced by the square of V_{DD} while the leakage and short circuit power is reduced linearly. The voltage can be scaled down as far as below the threshold voltage (V_{th}) of the transistors, down in the sub-threshold region. In sub-threshold, the gate-source voltage of the transistors, V_{gs}, is smaller than V_{th}, thus, $V_{\text{eff}} = V_{\text{gs}} - V_{\text{th}}$ is negative and the transistor is operating in weak inversion. Consequently, the square-low relation between voltage and current for a transistor, is no longer valid [7]. The drain current for an NMOS transistor is approximately given by [10]

$$I_{\text{ds}} \approx I_0 \frac{W}{L} e^{(V_{\text{gs}} - V_{\text{th}})/nV_{\text{T}}} \left(1 - e^{-V_{\text{ds}}/nV_{\text{T}}}\right), \tag{2.11}$$

where I_0 and n are technology-dependent parameters, W/L is the transistor width and length ratios, V_{ds} and V_{gs} are the drain-source and gate-source voltage, while $V_{\text{T}} = kT/q$ is the thermal voltage where q is the electron charge. n is often mentioned as the sub-threshold slope factor [7]. An illustration of the relation between the drain-source current and the gate-source voltage of an arbitrary high-V_{th} NMOS transistor is presented in Figure 2.3. The regions of inversion are marked, and the straight line on the curve, within the weak inversion region, is the sub-threshold slope. The transistor has a threshold voltage of approximately 0.7 V, and the inversion regions are limited to ±100 mV of V_{th} [7].

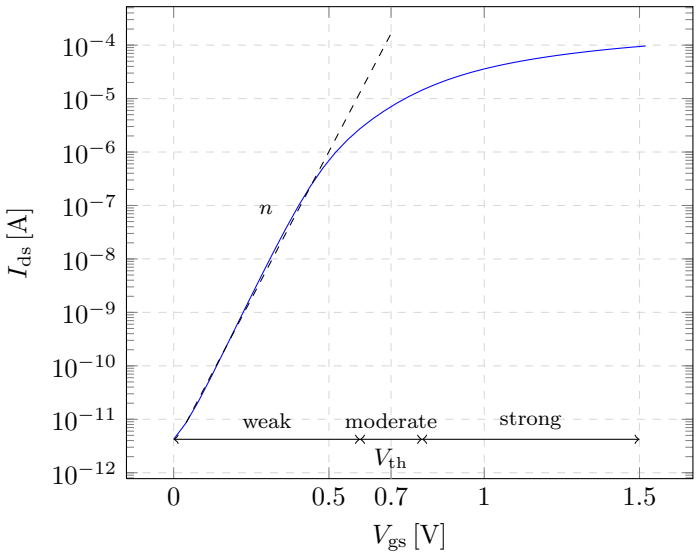


FIGURE 2.3: I_{ds} versus V_{gs}, showing approximated regions for weak, moderate and strong inversion, and the sub-threshold slope, n.

The threshold voltage is implicitly dependent on the drain-source voltage through the effect of drain induced barrier lowering (DIBL) and the bulk-source voltage (V_{bs}) through the body effect. Hence, the threshold voltage is expressed [10]

$$V_{th} = V_{th0} - \lambda_{ds} V_{ds} - \lambda_{bs} V_{bs} \tag{2.12}$$

where V_{th0} is the threshold voltage with $V_{ds} = V_{bs} = 0$, and $\lambda_{ds} > 0$, $\lambda_{gs} > 0$ are technology-dependent coefficients. Moreover, the threshold voltage is increased by lowering V_{ds}. Equation (2.11) and (2.12) can be combined to highlight the dependence of the current on V_{ds} and V_{gs},

$$I_{ds} = \beta \cdot e^{V_{gs}/nV_T} \cdot \left[e^{(\lambda_{ds} V_{ds})/nV_T} \left(1 - e^{-V_{ds}/v_T} \right) \right], \tag{2.13}$$

$$\beta = I_0 \frac{W}{L} e^{-(V_{th0} - \lambda_{bs} V_{bs})/nV_T}. \tag{2.14}$$

A new variable, β, is introduced to represent the strength of the transistor. As of (2.14), the transistor strength can be tuned by tuning the aspect ratio (W/L) of the transistor or the bulk voltage. It is not necessarily most efficient to increase the gate-width to obtain a stronger transistor, because an increased W will increase the threshold voltage due to the reverse narrow channel effect (RNCE) [11, 12]. Moreover, β is rather insensitive to small sizes of W, and an increase of the gate length is more efficient. An increase in L will reduce the threshold voltage due to the RNCE, and consequently β will increase.

When a transistor is operation in the sub-threshold region the difference between the on- and off-current is slightly reduced compared to above-threshold operation. The current is given by (2.13), thus, inserting $V_{\mathrm{gs}} = V_{\mathrm{DD}}$ and $V_{\mathrm{gs}} = 0$ gives

$$I_{\mathrm{on}} \approx \beta \cdot e^{V_{\mathrm{DD}}/nV_{\mathrm{T}}}, \tag{2.15}$$

$$I_{\mathrm{off}} \approx \beta. \tag{2.16}$$

The ratio between the on and off current is then

$$\frac{I_{\mathrm{on}}}{I_{\mathrm{off}}} = e^{V_{\mathrm{DD}}/nV_{\mathrm{T}}}. \tag{2.17}$$

This result shows that lowering the supply voltage will exponentially reduce the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, which implies that the leakage power has stronger impact on the total power consumption than above-threshold. Another consequence, circuit typologies with many transistors connected to the same node will be less robust. Figure 2.4 illustrates this situation, where only one out of n transistors are switched on. To achieve correct operation it is important that the I_{on} current dominates over the overall off-currents $(n-1)I_{\mathrm{off}}$ in order to differentiate the high and low level of the overall current I_{total} [11].

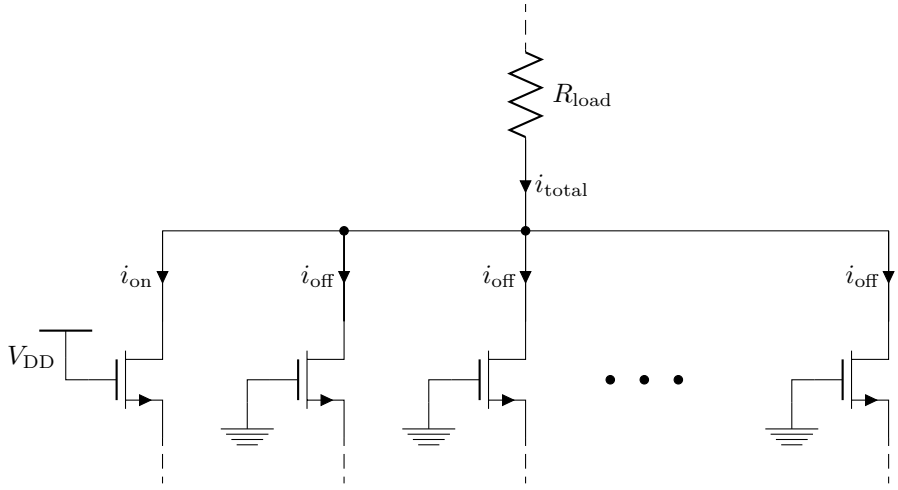


FIGURE 2.4: Impact of reduced $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio.

Another uncertainty in the sub-threshold region is the imbalance in the transistor strength between NMOS and PMOS transistors. Above-threshold the NMOS transistor is typically twice as strong as the PMOS transistor. However, in sub-threshold the imbalance factor

$$\mathrm{IF} = \max\left(\frac{\beta_{\mathrm{n}}}{\beta_{\mathrm{p}}}, \frac{\beta_{\mathrm{p}}}{\beta_{\mathrm{n}}}\right) \geq 1 \tag{2.18}$$

is much higher than above-threshold [11]. Balanced strength in NMOS and PMOS transistors are necessary to achieve symmetrical transitions in logic gates. As an example, consider Figure 2.5, an illustration showing the input to output relation of an inverter. The dashed line shows the transition of an unbalanced inverter where the NMOS transistor is stronger than the PMOS. As a result, the output will be pulled down bellow $V_{\mathrm{DD}}/2$, before the input is above $V_{\mathrm{DD}}/2$. The output swing is also degraded, as the PMOS transistor is not strong enough to pull the output level up to V_{DD}.

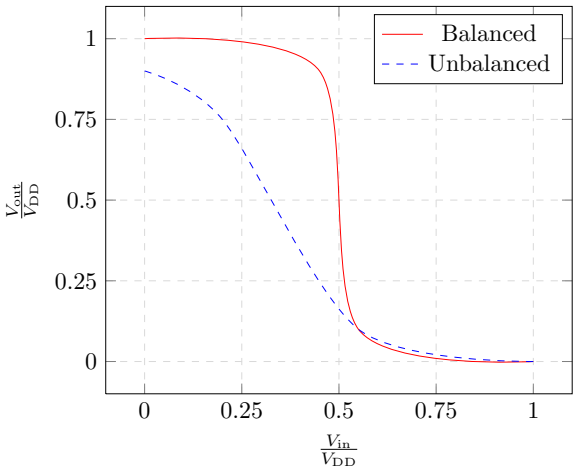
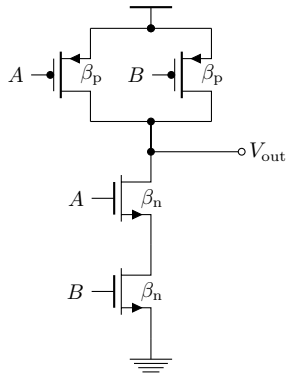


FIGURE 2.5: Illustrated transitions of inverters with balanced and unbalanced NMOS and PMOS transistors. Values are normalized to V_{DD}.

Imbalance has an even higher impact on circuits where transistors are stacked, as stacked transistors will loose strength by a factor of X_{stack} when they are stacked. This factor is dependent on how many transistors that are stacked and the supply voltage of the circuit. For sub-threshold operation X_{stack} is increased for on-currents while it is reduced for off-currents compared to above-threshold [11]. Hence, the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio is reduced. In standard NAND and NOR gates the transistors in either the pull-up or pull-down network are stacked, hence the output strength of the gate will depend on its inputs. Figure 2.6 shows a standard NAND gate together with a table that shows what the output strength is depending on the inputs. The output strength is varying from $2\beta_{\mathrm{p}}$ to $\beta_{\mathrm{n}}/X_{\mathrm{stack}}$, which creates an imbalanced pull up/down network.



Input		Output Strength	
A	B	Pull Down	Pull Up
0	0	-	$2\beta_p$
0	1	-	β_p
1	0	-	β_p
1	1	β_n/X_{stack}	-

FIGURE 2.6: NAND gate with a table of its output strengths.

2.5 The Successive Approximation Register ADC

The successive approximation register ADC is one of the most popular architectures for realizing analog-to-digital conversion. Low power consumption together with medium speed and accuracy makes it suitable for several applications. Energy is saved due to simple analog components and a small amount of digital circuitry [7]. Figure 2.7 shows a SAR-ADC with its main building blocks; a comparator, a sample-and-hold (S/H) circuit, a reference digital-to-analog converter (DAC) and a successive approximation register (Control logic). The comparator is used with the DAC and digital control logic to search for a digital representation of the sampled analog signal, V_{sh}. The conversion can be described as follows; first, the input signal, V_{in}, is captured by the S/H circuit. Then, the output of the DAC, V_{DAC}, settles to $V_{ref}/2$, and the comparator compares these voltages. Depending on the result, the most significant bit (MSB), b_{N-1}, is either set to 0 or 1. Now, the DAC settles to $\frac{1}{4}V_{ref}$ or $\frac{3}{4}V_{ref}$ if b_{N-1} was set 0 or 1, respectively. This binary search algorithm continues until $V_{DAC} = V_{sh} \pm V_{LSB}/2$. Then, the binary code used to generate V_{DAC} is the final output word of the SAR-ADC.

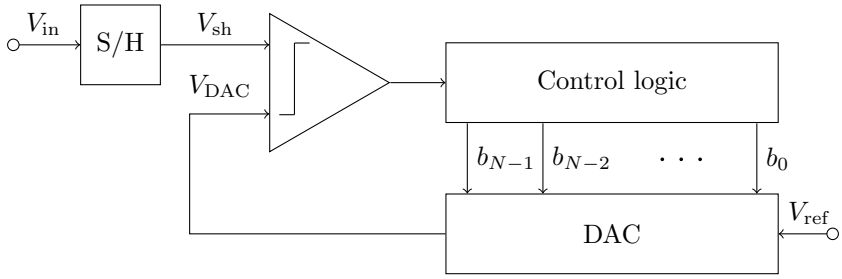


FIGURE 2.7: The successive approximation register ADC.

The SAR-ADC architecture in Figure 2.7 is made for single-ended input signals. However, in analog circuits it is more common with fully differential signals to achieve higher signal power [13]. Consequently, ADCs with differential input signals more are versatile. A SAR-ADC can easily be modified to handle a differential input by adding an extra DAC and connect both to each of the comparator inputs.

2.5.1 Comparator

Comparators are one of the most widely used components general in electrical circuits and is an essential component in ADCs [7]. Its purpose is to detect which of two input signals that is grater than the other, and output either a zero or a one depending of which was greater. For low power operation, a clocked track-and-latch architecture is commonly used. The architecture is composed of two stages; one for tracking the input signal and another for latching the output signal. For one clock period it is tracking the input signal, while the next period the output is latched and only leakage power are consumed. A standard implementation of the latch stage is to connect two inverters back-to-back during the latch period, i.e. connect the output of one inverter to the input of the second inverter, and the output of the second inverter into the input of the first inverter. This positive-feedback connection will force the comparator output to settle.

The performance of a comparator may be degraded by non-ideal effects such as *input offset*, *hysteresis*, *kickback noise* and *metastability*. In worst case, these non-idealities may change the logic output, however, these terms are described below.

Input Offset

In an ideal comparator, the input transistors are equal and perfectly matched. Real comparators may have a mismatch between the input pairs which results in an offset voltage between them [7]. Consequently, the logic output will be affected, as it is not changing when the input voltages are perfectly crossing each other. Mathematically the output is given

$$V_{\text{out}} = \begin{cases} 1, & V_{\text{ip}} + V_{\text{offset}} > V_{\text{in}} \\ 0, & V_{\text{ip}} + V_{\text{offset}} < V_{\text{in}} \end{cases} \tag{2.19}$$

where V_{ip} and V_{in} are the positive and negative input voltages and V_{offset} is the offset voltage, which ideally is zero. Mismatch in the load capacitance of the comparator outputs can also affect the offset voltage [14].

Hysteresis

Hysteresis is memory in the comparator [7]. Internal capacitors in the comparator have stored a certain amount of charge from the previous inputs, which will affect the next decision and potentially cause a wrong logical output. To prevent hysteresis the internal capacitors must be discharged during the reset phase.

Kickback Noise

The inputs of an comparator are either a differential pair of NMOS or PMOS transistors where the input signals are connected to the gates. Hence, there are a certain capacitive coupling between the input nodes and some internal nodes in the comparator. For clocked comparators charge may be transferred into or out of the inputs then the track-and-latch stage goes from track mode to latch mode [7]. This charge transfer is denoted as kickback noise and is caused by the charge needed to turn on the transistors in the latch stage.

Metastability

Track-and-latch comparators need a certain amount of time to decide which of its inputs that are the greater than the other. This time is the time constant of the latch, and it is dependent on the initial voltage difference between the input signals at the beginning of the latch phase. However, if the difference is small, the latch time may be large, and perhaps larger than the allowed time, which can result in an output that is not recognized as the correct logical value. This occurrence is known as metastability [7].

2.5.2 Sample-and-Hold

The sample-and-hold function of a SAR-ADC is often realized as a track-and-hold circuit, which tracks the input signal for one period and holds it stable the next period. A simple CMOS realization consists of a single MOS transistor used as a sampling switch and a capacitor to store the sampled input. However, using a single transistor as a sampling switch has some drawbacks. Firstly, the input signal swing will be limited due to the threshold voltage of the transistor. Secondly, the switch resistance will vary with the input signal as the gate-source voltage, V_{gs}, varies. A popular approach to solve these problems is to boost up the gate voltage of the sampling switch to be higher than $V_{\mathrm{DD}} + V_{\mathrm{in}}$, such that V_{gs} is independent of the input signal. This could be done by either having an external clock signal higher than V_{DD}, so called clock boosting, or using the CMOS bootstrap technique.

The bootstrapped technique provides a gate voltage that is higher than the power supply voltage, and is more or less constant with respect to source and drain [8]. The principle is shown in Figure 2.8; during $\overline{\phi}$, while the sampling switch M_1 is connected to ground, the capacitor C_s is charged to V_DD. In the next phase, the sampling phase, ϕ, the top-plate of the capacitor is connected to the gate of M_1, while its bottom-plate is connected to the input signal, V_in. Thus, the total voltage applied to the gate is equal to $V_\mathrm{DD} + V_\mathrm{in}$, which results in a drain-gate voltage independent of V_in as

$$V_\mathrm{dg} = V_\mathrm{DD} + V_\mathrm{in} - V_\mathrm{in} = V_\mathrm{DD}. \tag{2.20}$$

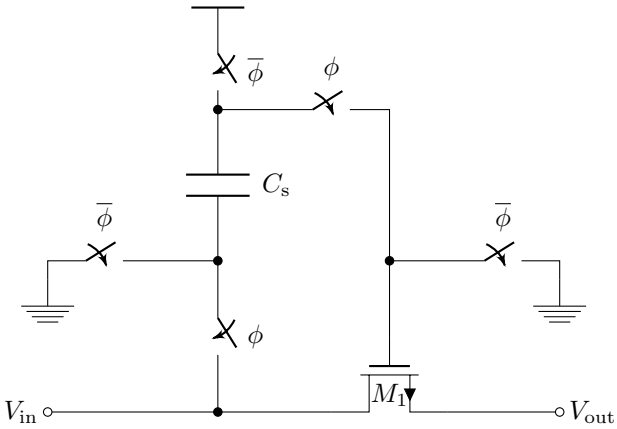


FIGURE 2.8: The principle of a bootstrapped switch architecture.

2.6 Layout Techniques

Layout in the sub-100 nm technology includes a number of non-idealities that must be addressed and overcome to achieve a successful circuit design. When manufacturing semiconductors in the sub-100 nm technology there is no longer a 1-to-1 correspondence between the device image on the rectle's and the layout. This is because the feature sizes of the technology are less than one-quarter of the wavelength of the ultraviolet ($\lambda = 193$ nm) illumination that is used for etching [15]. Consequently, device matching is degraded compared to above 100 nm technologies.

Sharp edges and edge placement is difficult to obtain and will disturb the intended image shape. To reduce this error an enhancement technique called optical proximity correction (OPC) is used during processing to correct the rectile patterns. Figure 2.9 shows the principle of OPC; the black lines are the proposed layout, while the red lines shows rounding corners that occurs in the photolithographic

process and to compensate for the rounded edges do OPC add extra polygons as the blue lines shows. OPC does not have a 1-to-1 correspondence with the layout and is therefore undesired, especially when matching is required. By using regular ploy patterns in a single direction, sharp corners are avoided and consequently less OPC is required.

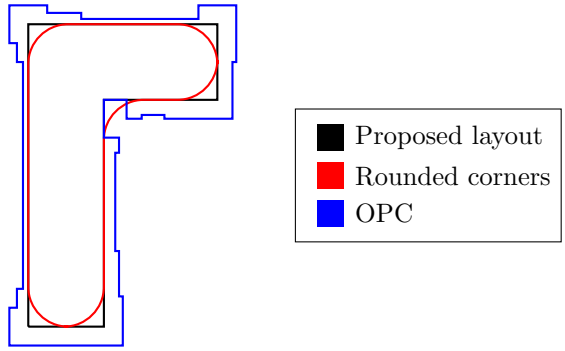


FIGURE 2.9: Illustration of OPC.

Chapter 3

Ultra-Low Power Analog-to-Digital Conversion

State-of-the-art ultra-low power analog-to-digital converters and the techniques used to save power will be presented in this chapter.

3.1 State-of-the-Art

Architectures for analog-to-digital converters can provide different features for sampling speed, accuracy and power consumption. Figure 3.1 and 3.2 shows a comparison of the power consumption and figure-of-merit achieved with different architectures. The ADCs were published in international Solid-State Circuits Conference (ISSCC) and Symposia on VLSI Technology and Circuits (VLSI) between 1997 and 2013 [1]. The SAR architecture achieves low power operation, a great FOM and is suitable for a big variety of sampling speeds and resolutions. Thus, the SAR architecture has a great potential for ultra low power operation. The last few years have some published papers presented SAR-ADCs with power consumption down to 3 nW [5] and supply voltages down to 160 mV [16].

Table 3.1 presents an overview of SAR-ADCs with low power performance and some of them is operating with extremely low supply voltages. In [17] is the low power consumption achieved mainly by reducing the supply voltage down to 0.4 V and by optimizing the channel length of the transistors used in the digital logic to minimize the sum of leakage and switching power consumption. The digital control logic was made asynchronous to minimize the signal leakage through the track-and-hold circuit due to the low sampling frequency. Low voltage operation

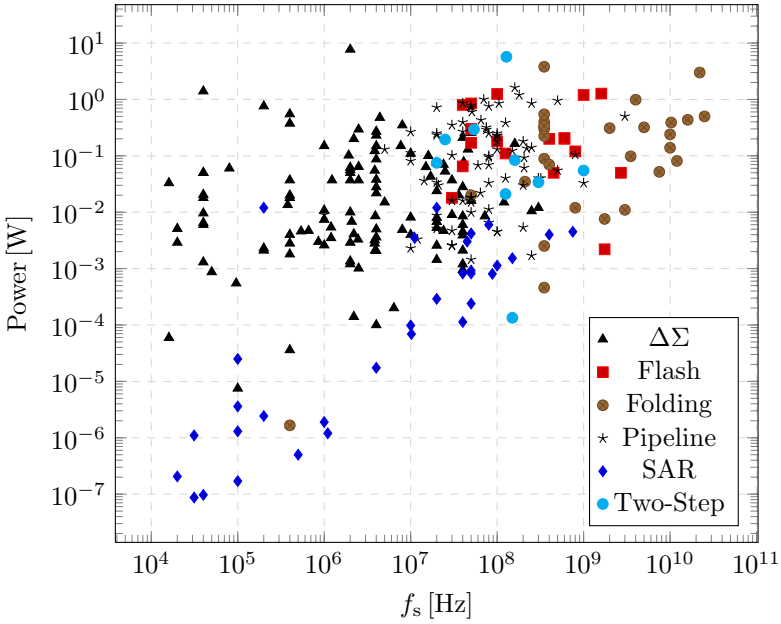


FIGURE 3.1: Power versus Nyquist sampling rate for ADCs published in ISSCC and VLSI during 1997-2013 [1].

TABLE 3.1: Comparison of ultra-low power/voltage SAR-ADCs.

	[17]	[18]	[5]	[16]
Technology	0.18 μm	90 nm	65 nm	0.13 μm
Sampling rate	2.5 kS/s	100 kS/s	1 kS/s	40 kS/s
Resolution [bit]	10	10	10	8
Supply voltage [V]	0.4	0.35	0.7	0.16
Power [nW]	6.5	170	3	670
ENOB [bits]	9.4	9.06	9.1	7.3
FOM [fJ/conv.]	3.98	3.2	5.5	106

has also been achieved in [18], and a better FOM is achieved at a higher sampling frequency. However, the lowest supply voltage is presented in [16], which is, according to the authors, one of the lowest reported supply voltages in analog circuit design. To be able to operate at ultra-low voltage, an amplifier suitable for below 100 mV operation has been implemented alongside with dynamic latches that have both gate and bulk driven inputs. Even with a supply voltage so low, the power consumption is not as low as the other SAR-ADCs in Table 3.1. The lowest reported power consumption, for SAR-ADC, or ADCs in general, is [5] where only 3 nW is needed to perform a conversion. The ultra-low power consumption is achieved by the use of a split capacitor DAC architecture, a multi-V_{th} design and a latch-based control logic. A split capacitor DAC array will save power and

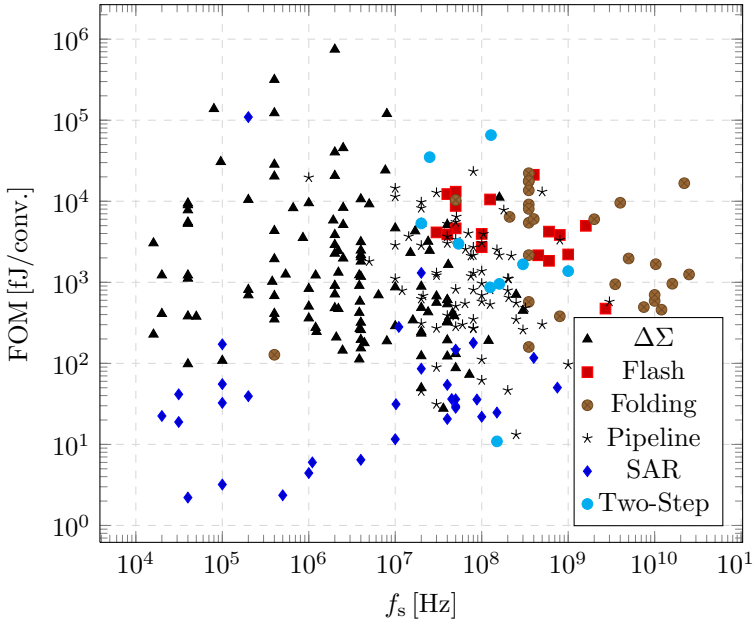


FIGURE 3.2: FOM versus Nyquist sampling rate for ADCs published in ISSCC and VLSI during 1997-2013 [1].

area due to smaller capacitors, while the use of transistors with different threshold voltages will reduce leakage and switching power and allow the circuit to use a single voltage source.

3.2 Digital-to-Analog Converter

The digital-to-analog converter architecture has a big impact on the total power consumption of a SAR-ADC. Moreover, the total accuracy of SAR-ADC is highly dependent of the DAC architecture, therefore, an architecture should be chosen carefully. There are a few different architectures with different switching methods that have been widely used in SAR-ADCs; however, the charge-redistributed capacitor array is the most used DAC in voltage-mode SAR-ADCs. The principle is shown in Figure 3.3, where capacitors with a capacitance that is binary scaled related to a unity capacitance, C_{u}, constitutes a capacitor array. Note that the ADC is fully differential and therefore two capacitor arrays are needed. Each capacitor in the capacitor array has its top-plate connected together, and its bottom-plate is connected to switches. Connecting the bottom-plate either to V_{ref} or V_{ss} and the voltage on the top-plate will change with the same amount as the weight of the respective capacitor. One and one capacitor are switched to perform the SAR algorithm. SAR-ADCs with a charge-redistributed DAC have the benefit that no

sample-and-hold circuit is necessary as the input signal is sampled directly on the capacitor array. Compared to a resistive DAC, the capacitive DAC is more energy-efficient and is less sensitive to mismatch [19].

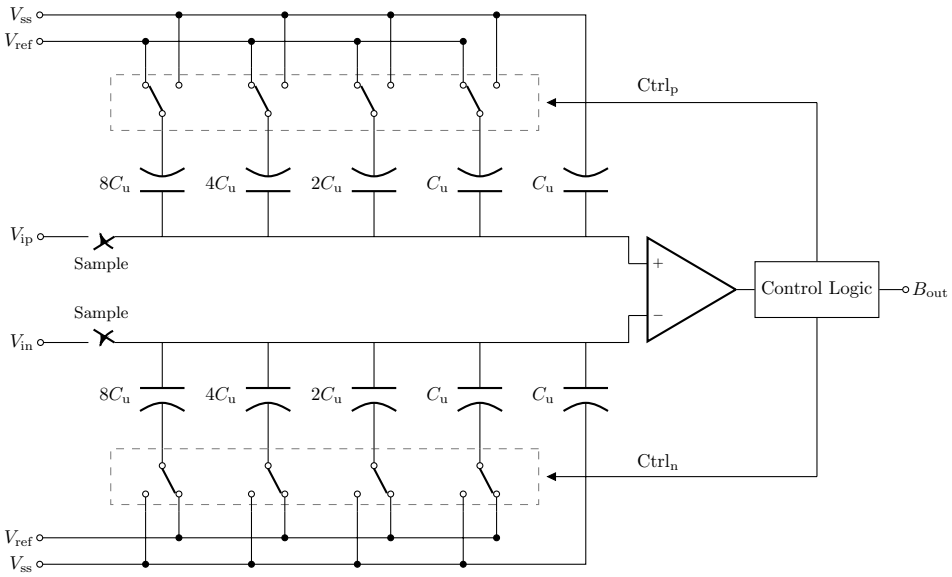


FIGURE 3.3: SAR-ADC with a charge-redistributed capacitor DAC.

3.2.1 Architectures

Since the charge-redistributed SAR-ADC was introduced in 1975 [20] a lot of new architectures and switching algorithms have been introduced. The average switching energy in a conventional architecture with a differential input is given [2]

$$E_{\text{avg,conventional}} = \sum_{i=1}^{N} 2^{N+1-2i}(2^i - 1)C_{\text{u}}V_{\text{ref}}^2\,[\text{J}]. \tag{3.1}$$

However, the energy consumed in the DAC is improved by new techniques. Some of the most energy friendly DAC architectures for SAR-ADCs are described below.

Monotonic

A monotonic switching DAC architecture was first presented in [21] and is now widely used [22–25] due to its low power performance, up to 81% of energy can be saved compared to the conventional DAC architecture. It uses a standard capacitor

array equal to the DAC in Figure 3.3, but in contrast to the conventional switching algorithm, the monotonic switching algorithm only switches one of the positive and negative DACs[1] for each comparison and the first bit is found directly without any switching, which saves both energy and area as the biggest capacitors can be avoided.

The algorithm can be described as follows; during sampling, all bottom plates of the capacitors are connected to V_{ref}, and the differential input signal is stored on the top plates of the positive and negative DAC arrays. The comparator compares the voltage on the positive and negative DACs with each other. If the positive DAC has a higher voltage the MSB is set to 1, and the bottom-plate of the biggest capacitor in the positive DAC is connected to V_{ss} to reduce the voltage with a factor 2. The same procedure yields for the negative DAC, but if its output voltage is higher than the positive the MSB is set to 0. This method follows until each of the remaining bits are set, but the voltage on the DAC is reduced with a factor that is doubled compared to the previous bit. This results in a average energy consumption of [2]

$$E_{\text{avg,monotonic}} = \sum_{i=1}^{N} 2^{N-2-i} C_{\text{u}} V_{\text{ref}}^2 \,[\text{J}]. \tag{3.2}$$

During conversion the voltage levels of the DACs are monotonically decreasing, hence the name "monotonic". Notice that this algorithm can also be implemented with a monotonically increasing common mode voltage, i.e. connect bottom-plates to V_{ss} during sampling, and connect the DAC with the lower voltage level to V_{ref}. The common mode voltage, V_{cm}, which is defined $V_{\text{cm}} = (V_{\text{ip}} + V_{\text{in}})/2$, is consequently monotonically decreasing/increasing. However, a variation in the common mode voltage during conversion will result in a variation of the offset voltage of the comparator as the input transistors of the comparator will have a bias voltage that are varying. If this becomes a problem, the switchback algorithm can easily be applied [26]. It uses the same DAC arrays, but instead of treating all capacitors equally, the biggest capacitor is switched in the opposite direction as the others to keep the common mode voltage within a range of $V_{\text{ref}}/2 \pm V_{\text{ref}}/4$. Unfortunately, this technique will increase the energy consumption compared to the pure monotonic method as [26]

$$E_{\text{avg,switchback}} = \left[2^{N-3} + \sum_{i=1}^{N-1} 2^{N-2-i} \right] \cdot C_{\text{u}} V_{\text{ref}}^2 \,[\text{J}]. \tag{3.3}$$

[1] The positive and negative DAC are referred to the DACs for the positive and negative inputs of the differential input signal.

Merged Capacitor Switching

The merged capacitor switching (MCS) scheme has the same capacitor array as the monotonic scheme, but in addition it has the opportunity to connect the common mode voltage at the bottom-plate of each capacitor. Thus, during sampling each of the bottom-plates are connected to V_{cm}, and the DAC array with the highest voltage level will connect the biggest capacitor to V_{ref} and while the other DAC array connect its biggest capacitor to V_{ss}. This procedure follows until each bit is set, and the corresponding bit is set to 1 when the positive DAC array has a greater voltage level, otherwise 0. This results in an average energy consumption of

$$E_{\mathrm{avg,MCS}} = \sum_{i=1}^{N-1} 2^{N-3-2i}(2^i - 1)C_{\mathrm{u}}V_{\mathrm{ref}}^2\,[\mathrm{J}], \tag{3.4}$$

which is a reduction of 93.4% compared to the conventional method [2]. Another advantage compared to the monotonic method is the constant common mode voltage during conversion. On the other hand, this method require transmission gates to connect V_{cm} to the bottom-plates, while the monotonic method only require inverters on the bottom-plates to connect either V_{ref} or V_{ss}.

To summarize, and for an easy comparison the average energy consumption of each of the DAC architectures are calculated in Table 3.2.

TABLE 3.2: Switching energy comparison of DACs with $N = 9$ [2].

	Conventional	Monotonic	Switchback	MCS
$E_{\mathrm{avg}}/C_{\mathrm{u}}V_{\mathrm{ref}}^2\,[\mathrm{J}]$	680.7	127.5	191.5	42.4

3.2.2 Top-Plate Sampling

The charge-redistributed DAC architectures in the previous section where all described with top-plate sampling, i.e. the input signal is sampled on the top-plate of the DAC array. Bottom-plate sampling is also a widely used [5, 18, 27–30] and a possible method, in fact, it was used in the first presented charge-redistributed SAR-ADC [20]. With bottom-plate sampling the input signal is sampled on the bottom side of the capacitor while the top-plate is connected to the common mode voltage. By disconnecting V_{cm} from the top-plate and then connect the bottom-plates to either V_{ref} or V_{ss} the top-plate voltage will change to $V_{\mathrm{cm}} - V_{\mathrm{input}}$ [7]. This will make the charge injection from the sampling switches independent of the input signal and the sampling time independent of the input signal [8]. However, for bottom-plate sampling a switch with full swing capabilities is needed for each of the capacitors in the DAC arrays. For this reason top-plate sampling is commonly used [4, 16, 24, 31–33] as the design can be simplified by using only an inverter at

each capacitor to connect the bottom-plate to V_{ref} or V_{ss}. In addition, an inverter-switch does only require a single control signal which is beneficial with respect to the control logic.

3.3 Digital Control Logic

There are many different approaches for realizing control logic for an SAR-ADC, both synchronously and asynchronously. However, the main principle is to achieve a behavior that is similar to a shift register. A shift register will mainly perform as a state machine and keep track of which capacitor in the DAC array to switch when the comparator is ready. Thus, logic gates are used to determine which potential to be connected to the respective capacitor. Figure 3.4 outlines a shift register implemented with D flip-flops (DFFs). The outputs 'Ctrl$_i$' determines witch bit to be set, and are controlled by the 'Clock' and 'Reset' signal. Although each DFF is clocked, it does not mean that the shift register is only suitable for synchronous circuits, the 'Clock' signal might as well be generated from the comparator for an asynchronous approach [21].

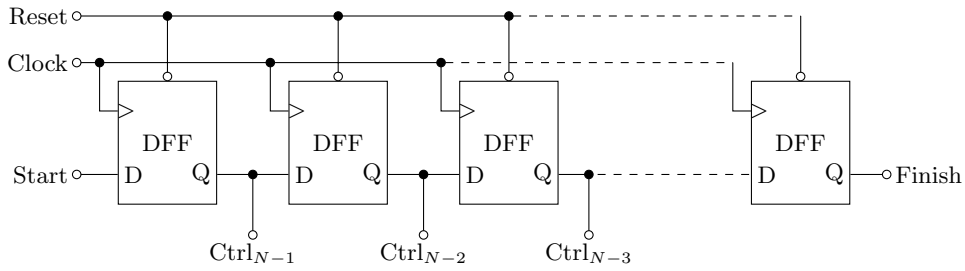


FIGURE 3.4: Shift register.

Asynchronous versus Synchronous

Generally, synchronous circuits consists of building blocks that are synchronized by a clock signal, while asynchronous circuits are not governed by a global clock signal. As already mentioned it is possible to implement the control logic of a SAR-ADC either asynchronous or synchronous, however, there are benefits and drawbacks with both techniques. One of the main arguments for doing asynchronous control logic in SAR-ADCs is to avoid a clock running at a frequency more than N times as fast as the sampling frequency, which is necessarily to run the N bit wide shift register. Clocks running at a high frequency generate more noise and can be hard to generate at high sampling frequencies [34]. For ultra-low power ADCs which

operate at relatively low sampling rates to save power, one of the main benefits with an asynchronous circuit is a relaxed requirement to the sampling switch. When the conversion time is long, may signal leak through the sampling switch during the conversion and consequently cause a error in the output code [17]. Nevertheless, the trend in ultra-low power ADCs is a synchronous operation as the sampling rates are relatively low and signal leakage through the sampling switches is rarely a problem [5, 32, 35, 36].

Chapter 4

Design Methodology

This chapter will present the design methodology for the proposed design and will go into detail of each of the building blocks.

4.1 Transistor Optimization for Ultra-Low Power

For ultra-low power operation it is important to minimize all contributions to power consumption. In Section 2.3, it was stated that power is consumed both dynamically and statically. The dynamic power can easily be reduced by decreasing the sampling speed, which is already proposed in the specification of this design with a sampling frequency of 1 kHz. However, a low sampling period will result in time-slots where the circuit is not operating, it is therefore important to reduce the leakage power. The current flowing through the transistors when they are turned off, i.e. $V_{\mathrm{gs}} = 0$ for NMOS and $V_{\mathrm{gs}} = V_{\mathrm{DD}}$ for PMOS, are known as the leakage current. As stated in Section 2.3 the leakage power is the product of the leakage current and the supply voltage.

The ST Microelectronics 65 nm technology design kit provides both general purpose (GP) CMOS transistors and low power (LP) transistors with extra oxide thickness to reduce leakage. Both GP and LP transistor are available with low, standard and high threshold voltages (V_{th}). Figure 4.1 and 4.2 shows an overview of the drain-source current, I_{ds}, for the different low power transistor types with respect to the drain-source voltage, V_{ds}, and the transistor length, L, when the transistor is turned off. Both figures show a huge difference in leakage current for the different threshold types. To optimize the leakage power the low power transistors with high threshold voltages is the most suitable choice. Lowering the supply voltage

will exponentially reduce the power consumption while increasing the transistor length will result in further improvements in power consumption.

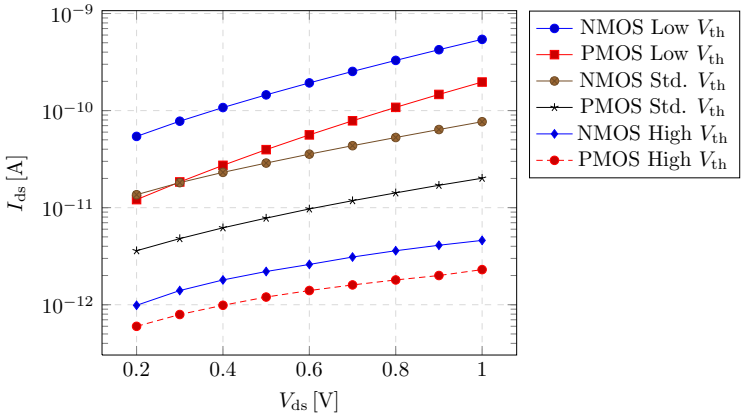


FIGURE 4.1: Leakage current with $L = 0.60$ μm and $W = 0.270$ μm.

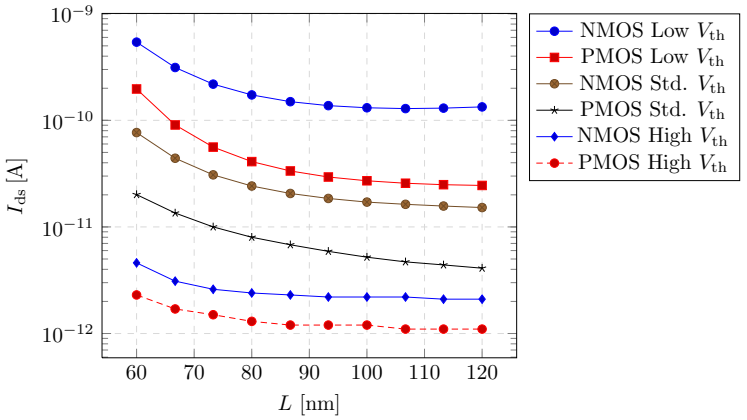


FIGURE 4.2: Leakage current with $V_{ds} = 1$ V and $W = 0.270$ μm.

Increasing the threshold voltage and gate length of a transistor will degrade the speed performance of a transistor [7]. First, a transistor with an increased threshold voltage will be turned on later than a transistor with a lower threshold voltage, assuming an equal slope of the input signal. Secondly, the transconductance, g_m will degrade with an increased gate length and consequently lower the unity-gain frequency of the transistor. The transconductance of a transistor operating in sub-threshold is found by deviating the sub-threshold current (2.11) with respect to V_{gs}

$$g_m \approx \frac{I_{ds}}{nV_T}, \tag{4.1}$$

where I_{ds} from (2.11) is approximated to $I_0(W/L)e^{V_{\mathrm{eff}}/nV_{\mathrm{T}}}$. Thus, the unity-gain frequency, f_{t}, of a transistor is given by [7]

$$f_{\mathrm{t}} \approx \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{gs}} + C_{\mathrm{gd}})}, \tag{4.2}$$

where C_{gs} and C_{gd} is the gate-source and gate-drain capacitance. Combining (4.1) and (4.2) shows that the speed is degrading with the gate length. However, speed is not a critical parameter for the specified design, but should be considered when the transistors are being optimized for ultra-low power operation.

As mentioned in Section 2.4, it is more efficient to increase the gate length of a transistor than the gate width to obtain a stronger transistor with improved β. Consider the sub-threshold transistor strength and the power improvements discussed above, the gate length should be bigger than $L_{\mathrm{min}} = 60$ nm, and the gate width, W, should be to selected accordingly to achieve balanced gates.

4.2 Digital-to-Analog Converter

In Section 3.2 different ultra-low power digital-to-analog converter (DAC) architectures was presented. The merged capacitor switching (MCS) architecture provide the best ultra-low power performance, but it does not have the benefit the monotonic architecture provide; each capacitor can be controlled by an inverter which is eliminating the need of transmission gates and enables a less complex control logic. Hence, from a system level view the monotonic DAC architecture may provide better ultra-low power performance.

4.2.1 Capacitor Sizing

For ultra-low power consumption the unit capacitor, C_{u}, should be as small as possible according to Table 3.2. On the other hand, minimizing C_{u} will reduce the linearity of the DAC due to mismatch between the unit capacitors in the DAC array, and the thermal noise will increase due to a smaller sampling capacitor.

To find the minimum unit capacitor according to the thermal noise requirements the sampling capacitor, C_{s}, is chosen large enough to be equal or greater than the fundamental SNR limit of an ADC which is given by the quantization error [37]. Hence, let $\overline{V_{\mathrm{t}}^2} = \overline{V_{\mathrm{q}}^2}$ and $C_{\mathrm{s}} = 2^{N-1}$ for the monotonic DAC architecture gives

$$C_{\mathrm{u}} = \frac{12kT \cdot 2^{N+1}}{V_{\mathrm{ref}}^2}. \tag{4.3}$$

For $T = 300$ K and $N = 9$ bit a unit capacitance of $C_{\mathrm{u}} = 1$ fF will enable supply voltages down to almost 0.2 V for a 9-bit ADC with a monotonic DAC architecture.

Mismatch between the capacitors in the DAC array will degrade INL and DNL of the ADC. The low bound for the unit capacitor, C_{u}, can be expressed as [19]

$$C_{\mathrm{u}} > 9 \cdot (2^N - 1) K_\sigma^2 \cdot K_C \tag{4.4}$$

where K_σ is the matching coefficient, and K_C is the capacitor density parameter. Thus, 9-bit resolution leads to a minimum capacitance of approximately 1 fF, assumed $K_\sigma \approx 1$ % μm and $K_C \approx 2$ fF/μm^2 for a metal-in-metal capacitor [19].

4.3 Digital Control Logic

The proposed sampling frequency makes synchronous control logic favorable compared to the asynchronous approach. A 9-bit resolution and a sampling frequency of 1 kHz will result in a global synchronization clock of maximum 12 kHz, where one clock period for sampling the input signal, and one clock period for resetting the circuit before next the sampling, was taken into account.

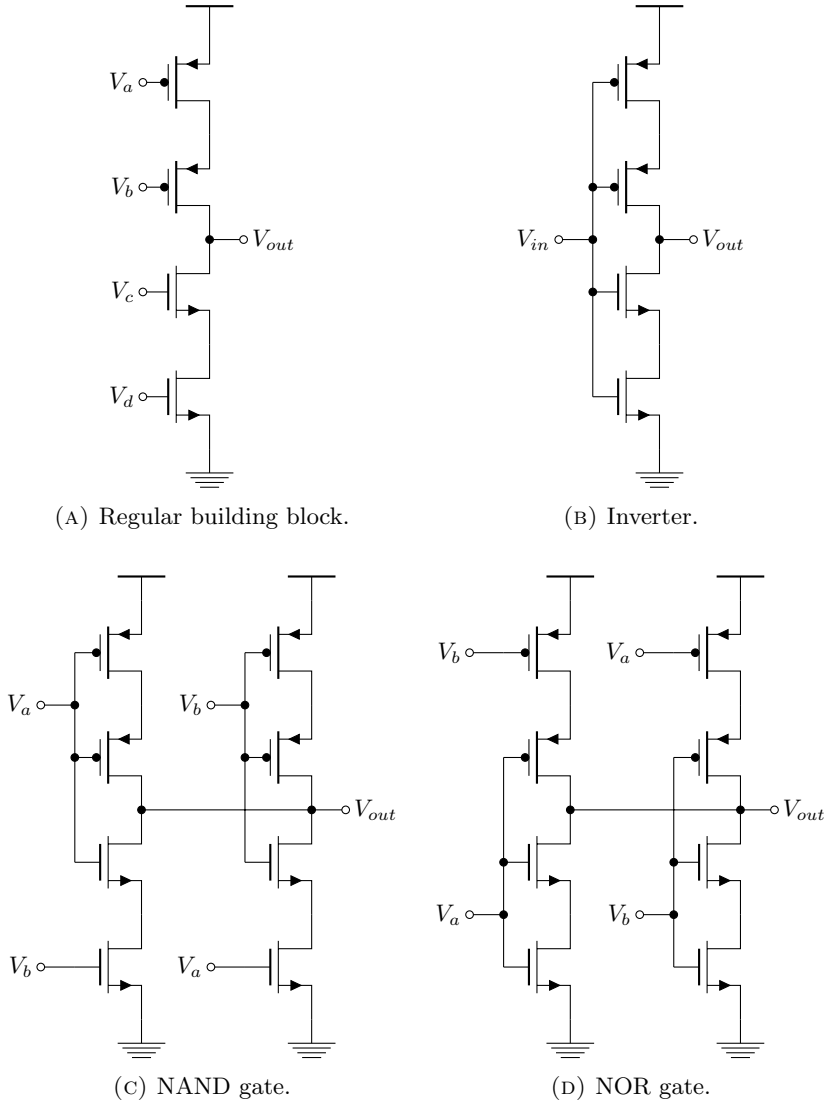
4.3.1 Sub-Threshold Gates

Standard logic gates such as NOT, NOR and NAND need to be custom made for successful sub-threshold operation. Higher imbalance between NMOS and PMOS transistors and other requirements to the transistor size is not taken into account for the standard cells provided by the design kit. Moreover, with customized gates leakage currents can also be reduced by the use of high threshold transistors.

In Section 2.4 design strategies for sub-threshold operation was discussed. NMOS and PMOS imbalance is worse for NAND and NOR gates where the output strength of the gate is varying with the inputs due to stacking of transistors. However, to reduce the variation of the output strength of the gate, the proposed design does stack the transistor pair that is not stacked in a standard gate [6]. Figure 4.3c and 4.3d shows the proposed structure of an NAND and NOR gate. For the NAND gate an extra pair of PMOS transistors is added in series with the existing PMOS pair, and equally for the NOR gate where an extra NMOS pair is added. The extra pair has its gate connected to the same input voltage as the original pair to achieve the same logical operation.

In addition, the pull-down network for the NAND gate is duplicated, equally for the pull-up network for the NOR gate. This is done to achieve a more regular layout, as Figure 4.3 shows, two PMOS and NMOS transistor can be connected in cascode to utilize a regular building block. By connecting all the inputs of the regular building block (Fig. 4.3a) together creates an inverter (Fig. 4.3b), and by using two regular blocks both NAND (Fig. 4.3c) and NOR (Fig. 4.3d) gates can be implemented.

The proposed gate architectures actually contradicts with one of the fundamental sub-threshold design rules as transistors are stacked, but on the other hand their output strength is varying less and even more important is the leakage currents can be reduced by stacking transistors. One example is [38] where reduced leakage



(A) Regular building block.

(B) Inverter.

(C) NAND gate.

(D) NOR gate.

FIGURE 4.3: Logic cells for sub-threshold.

power have been observed by stacking transistors. It should also be mentioned that stacked devices are most critical for gates that are heavily loaded.

4.3.2 D Flip-Flops

As mentioned in Section 3.3, a D flip-flops (DFF) is a suitable building block for realizing the successive approximation register. However, there are a few different approaches for realizing a DFF for sub-threshold operation. In [39] the sub-threshold performance of seven different DFF architectures were compared, where four of them were static, which is suitable for synchronous circuits. The static DFFs compared was *the basic NAND flip-flop*, *Transmission Gate Master-Slave flip-flop* (TGMS), C^2MOS *flip-flop* and *PowerPC 603*. Out of those are both the TGMS and PowerPC 603 using transmission gates, while the basic NAND flip-flop is using standard NAND gates, and consequently the most power hungry. The C^2MOS, presented in Figure 4.4, is not using transmission gates and uses less than 50% of the power consumption of a standard DFF [39]. Moreover, the architecture do fit in with the proposed regular building block in Figure 4.3a, consequently the C^2MOS flip-flop is the most suitable choice for the proposed design.

The C^2MOS flip-flop is built up by clocked CMOS (C^2MOS) blocks [40]. A C^2MOS circuit is basically a standard inverter with two MOS switches, one PMOS and one NMOS, connected in series. The gate of each switch is connected to a complementary clock signal, ϕ and $\overline{\phi}$. When ϕ is high[1], the C^2MOS circuit is operating as a conventional inverter, and when ϕ is low the circuit act as memory since a positive charge is stored at the junction capacitance of the NMOS transistor and equally a negative charge on the PMOS' junction capacitance. The MOS switches are placed between the NMOS and PMOS transistors of an inverter to avoid signal swing degradation, which can be a problem if the inverter transistors are placed between the MOS switches [40].

A modified architecture of the C^2MOS flip-flop is presented in Figure 4.4. The main difference is the architecture of the inverters and a transistor to reset the output, Q, to V_{DD}. To achieve regularity in the layout the reset transistor can be implemented as the regular building block in Figure 4.3a, but leave unwanted transistors as dummy transistors.

4.3.3 Bit Cells

Alongside with the shift register, combinatorial logic and a latch are needed to control the voltage levels of the capacitors in the DAC arrays. Each capacitor must be connected to V_{ref} during sampling, and during the conversion a capacitor of either the positive or the negative DAC array is connected to V_{ss}, according to the

[1] Assumed that ϕ is connected to the NMOS switch and $\overline{\phi}$ is connected to the PMOS switch.

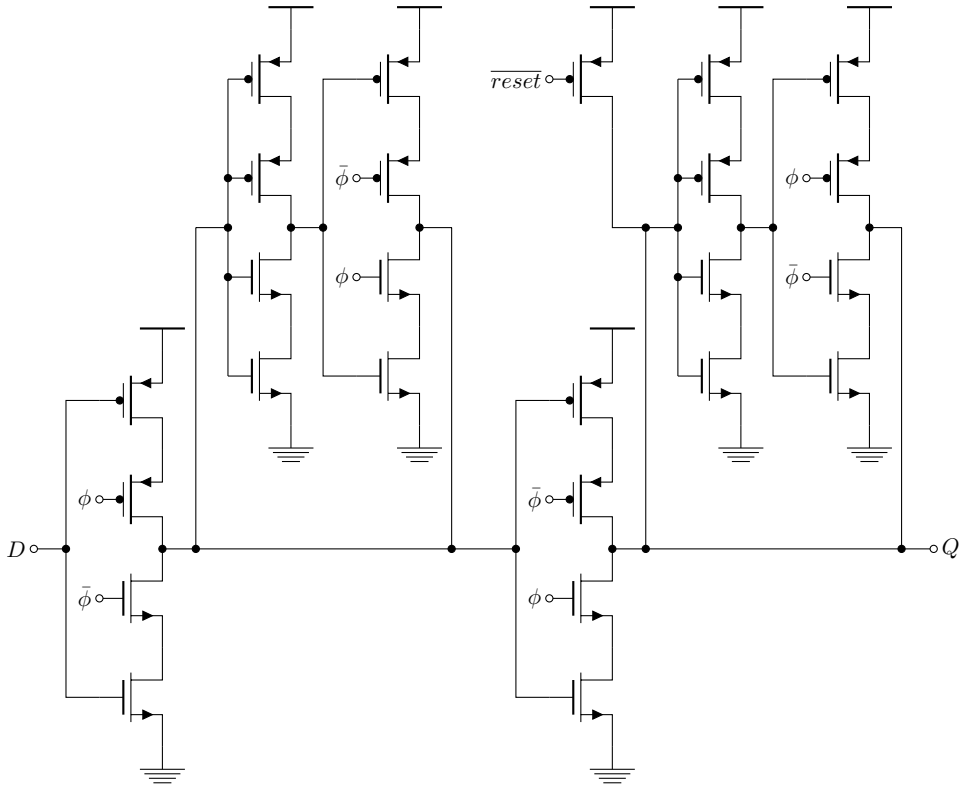


FIGURE 4.4: The proposed C^{2}MOS flip-flop with reset.

outputs of the comparator. In order to obtain a monotonic switching approach, it is important that only one by one capacitor is switched, and its state is kept throughout the conversion. The shift register is used to control which capacitor to switch, while a proposed *bit cell* containing a latch and combinatorial logic decides which of the positive and negative DACs to be switched, and store the respective bit.

The proposed bit cell, built up by the gates in Figure 4.3, is presented in Figure 4.5. Its input signals are the positive and negative output of the comparator, labeled $comp_p$ and $comp_n$, respectively, and a set signal from the shift register, labeled *set*. Thus, it outputs two control signals for the switches of the respective capacitors in the positive and negative DAC arrays, labeled $ctrl\_cap_p$ and $ctrl\_cap_n$, respectively. To store the comparator values throughout the conversion the bit cell contains a standard SR-latch based on NOR gates, as presented in Figure 4.6. The SR-latch is essentially defined to only have complementary outputs, Q and $\overline{Q}$, thus, the inputs $S = 1$ and $R = 1$ are therefore defined as an invalid input combination. However, the bit cell take the advantage of the invalid inputs as equal outputs are convenient

during the sampling period as it enables both DACs to be connected to the same voltage level simultaneously. The opinion with the NAND gates in the bit cell is to only apply comparator outputs to the SR-latch only when the *set* signal goes from high to low. After the comparator outputs are applied to the latch *set* is low and consequently s and r are low, which keeps the bit cell in latch mode throughout the conversion.

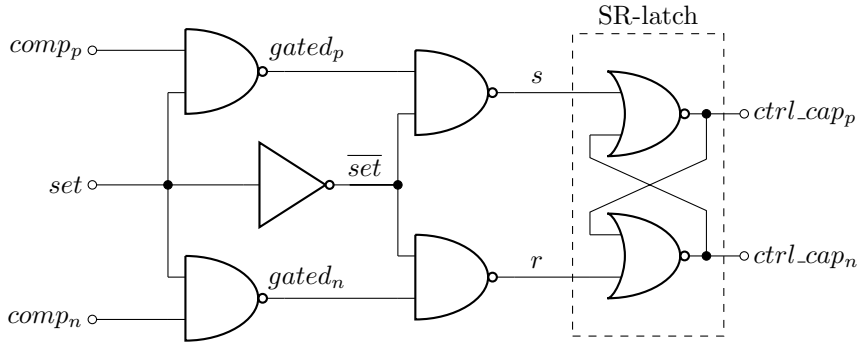
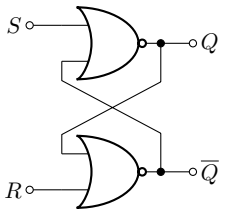


FIGURE 4.5: The proposed bit cell.



Input		Output	
S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	0	0

FIGURE 4.6: Standard NOR-based SR-latch, and its truth table.

4.3.4 Top Level

The SAR-ADC control logic is proposed to be implemented with the C^2MOS flip-flops and the bit cell presented in the previous sections. A top level overview of the control logic is presented in Figure 4.7. In addition to the cells in the figure, some combinatorial logic is needed to generate internal and external signals, for instance a sampling signal for the sampling switches and an external signal to indicate that the output bits are ready to be read. Proposed schematics are presented in Appendix B.

To ensure valid only outputs being applied to the bit cells, is the shift register clocked by an internal clock signal generated by the comparator. Since both comparator outputs are high when the comparator is in track mode a NAND gate

can be used to generate the internal clock signal as a NAND gate will give a low output for two high inputs and a high output otherwise. A proposed schematic is presented in Figure B.1 in Appendix B.

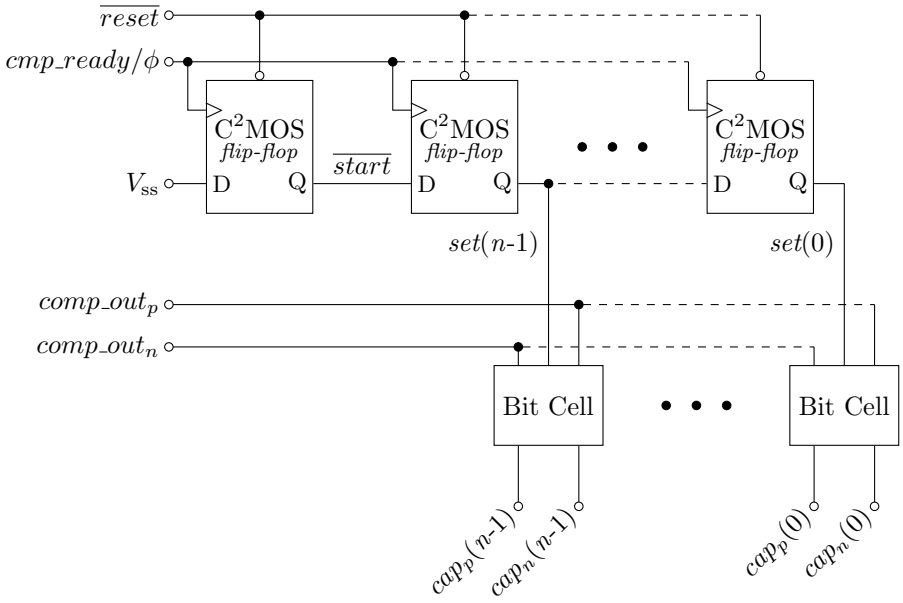


FIGURE 4.7: The proposed control logic.

The proposed behavior of the control logic can be described as follows; first, before sampling are every C^2MOS flip-flop reset, thus its outputs are pulled up from V_{ss} to V_{DD}, resulting in all *set* signals being high and consequently all the bottom-plates of every capacitor in the DAC arrays being connected to V_{ref}. The $\overline{reset}$ signal is pulled down when the internal clock signal, ϕ, is high to avoid short circuit leakage in the proposed C^2MOS shown in Figure 4.4. Secondly, the sampling switches opens to sample the differential input signal on the top-plates of the positive and negative DAC arrays. Thirdly, the bit cycling starts by comparing the voltages on the top plates of both DACs. When the comparator is settled, the shift register is being clocked by the comparator. The input of the leftmost flip-flop in Figure 4.7 is connected to ground; thus, zeroes will be shifted into the shift register. First out will $set(n\text{-}1)$ get low and its corresponding capacitors will be switched according to the capacitor outputs, and latched throughout the conversion since $set(n\text{-}1)$ is low. This procedure follows for the remaining bit cells, when $set(0)$ gets low, the conversion is finished and the shift register reset.

4.4 Comparator

Track-and-latch comparators without pre-amplifiers are the most used comparator architecture in ultra-low power SAR-ADCs due to their low power consumption and reasonable high resolution. A well-known dynamic latched comparator is presented in Figure 4.8 [5, 35]. With PMOS input pairs, it is suitable for a monotonically decreasing switching algorithm. It has two outputs, which are equal during reset and complementary when the comparator is latched. The control voltage V_{reset} is used to reset, or clock the comparator. While it is high, the latch is being reset by connecting its outputs to ground, which results in both the outputs, V_{op} and V_{on} being high. When V_{reset} is low, the comparator compares V_{ip} with V_{in}; the source followers $\text{M}_{1,2}$ controls the current flowing through $\text{M}_{3,5}$ and $\text{M}_{4,6}$ and consequently control the drain voltages on M_5 and M_6. Since the input pairs are PMOS transistors the lower input voltage will result in a higher drain voltage on M_5 or M_6 and the respective inverter will pull the output down. $M_{3,5}$ and $M_{4,6}$ constitute two inverters that are connected back-to-back when the comparator is in latch mode, and as mentioned in Section 2.5.1, the positive-feedback will force the outputs to rail.

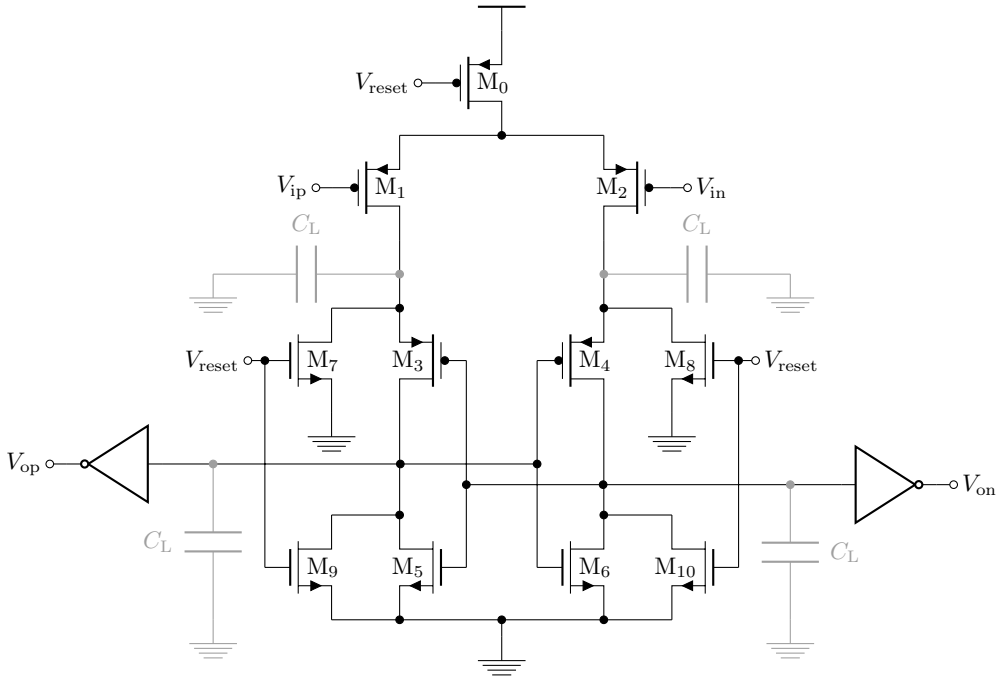


FIGURE 4.8: A dynamic latched comparator.

For ultra-low power consumption, the comparator in Figure 4.8 can be implemented with $M_{0,5\text{-}10}$ as high-threshold transistors to reduce the leakage power. To ensure

the target speed at low voltages, low-threshold transistors can be used for the input transistors and the cross-coupled inverters, $M_{1\text{-}4}$ [5].

A fundamental limitation of the resolution of the comparator stems from thermal noise [37]. However, to reduce the thermal noise in the comparator the capacitance at the bandwidth-limiting nodes can be increased, according to Equation (2.8). Therefore, the load capacitances at the output nodes of the comparator in Figure 4.8 are added. The minimum size of the load capacitance is given by [37]

$$C_{\mathrm{L}} = 12kT\gamma\kappa\frac{2^{2N}}{V_{\mathrm{ref}}^2}, \tag{4.5}$$

where γ is the thermal-noise factor and κ is a constant dependent of the comparator architecture.

4.5 Bootstrapped Switch

The main requirements for the sampling switch are in general to provide a certain on- and off-resistance that fits the size of the sampling capacitor and the speed requirements for the circuit. Since the proposed design is operating synchronously at a relatively low sampling frequency the off-resistance is one of the most critical properties of the sampling switch. A too low off-resistance will result in signal leakage during the conversion and consequently degrade the performance of the ADC. Since the sampling signal is generated internally can clock boosting be used with a level shifter. However, clock boosting requires an extra supply voltage higher than V_{DD}, therefore, a bootstrapped is favorable.

A bootstrapped switch suitable for rail-to-rail operation and 9-bit resolution was presented in [24]. Its schematic is shown in Figure 4.9. The circuit behaves similar to the circuit in Figure 2.8; during $\overline{\phi}$ is V_{sample} connected to ground and M_{P1} is turned on resulting in C_{s} being charged to V_{DD} through M_{P1} as the bottom-plate of C_{s} is connected to ground. M_{P2} is turned off, which disconnects C_{s} from the gate of the sampling switch, in the same way M_{N3} is turned off to isolate the bottom-plate of C_{s} from the source of the sampling switch. In the tracking phase ϕ is high and the bottom plate of C_{s} is connected to V_{in} thorough M_{N3}, and its top-plate is connected to the gate of the sampling switch through M_{P2}. V_{sample} is now equal to $V_{\mathrm{DD}} + V_{\mathrm{in}}$, resulting in the gate-source voltage of the sampling switch being approximately equal to V_{DD}.

To reduce signal-dependent on-resistance caused by the body effect of the sampling transistor, are two cascaded NMOS transistors, M_{N1} and M_{N2} added. Thus, the bulk of the sampling switch is connected to ground during $\overline{\phi}$, but during the track phase the bulk is connected to V_{in} through M_{N1} to cancel the body effect as the bulk voltage is input dependent and not constant [24].

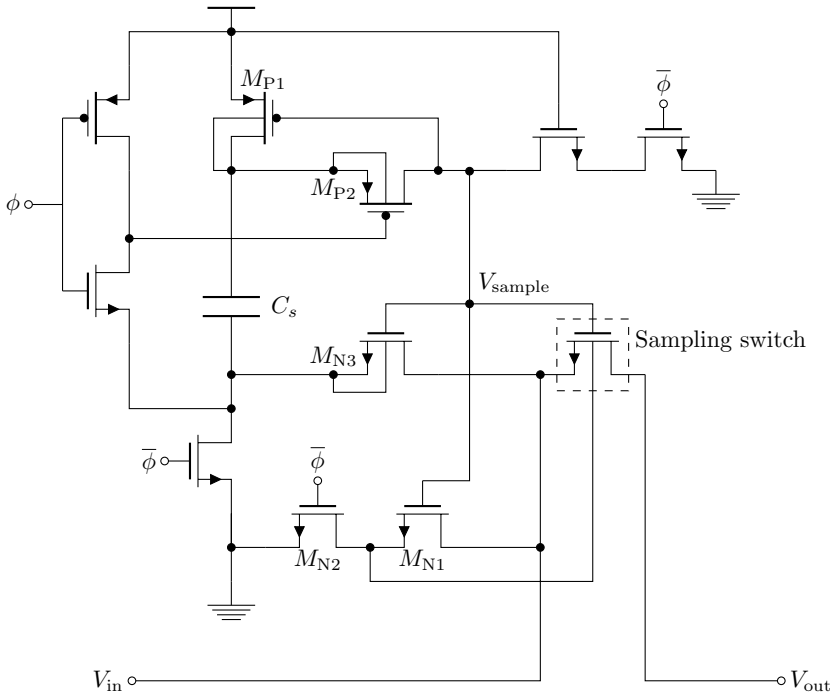


FIGURE 4.9: The proposed design for a bootstrapped sampling switch.

Chapter 5

Layout

This chapter presents the layout of the proposed design. The guidelines for layout in sub-100 nm CMOS technologies presented in [15] and in Section 2.6 were used. Thus, the proposed design was laid out with poly patterns in y-direction having a regular pitch. Metal layer 1, 3 and 5 are laid out in x-direction, metal layer 2 and 4 is laid out in y-direction as long as it was practically achievable.

5.1 Digital Building Blocks

The digital circuitry was designed with the regular cells presented in Section 4.3.1, which inherently enables a regular layout. To illustrate how the digital cells are laid out the layout of the proposed C^2MOS flip-flop (Fig. 4.4), is presented in Figure 5.1. Each transistor has guard rings on both sides for shielding and bulk connection to the power lines that are routed in metal layer 1, at the top (V_{DD}) and bottom (V_{ss}). Extra spacing in x-direction between each cell is made to enable easy signal routing between transistors. The two leftmost cells in Figure 5.1 shows how the regular cell (Fig. 4.3a) is interconnected to achieve the functionality of a clocked inverter and an inverter, respectively. On the rightmost side is a modified version of the regular cell where the PMOS transistors are connected in parallel, and the NMOS transistors are dummy cells. This cell corresponds to the reset transistor in Figure 4.4.

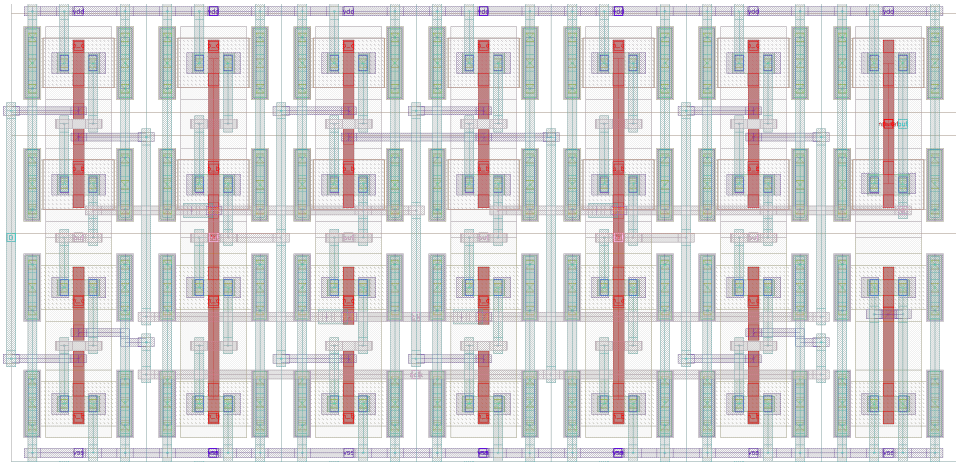


FIGURE 5.1: Layout of the proposed C^2MOS flip-flop presented in Figure 4.4.

5.2 Capacitor Array

To achieve a unit capacitor as small as 2.5 fF custom-designed metal-metal capacitors are implemented as in [41]. Figure 5.2 illustrates the principle where a single metal layer is laid out as finger capacitors on a row, and fingers are combined using a common-centroid approach to achieve a binary weighted capacitor array. To achieve a more compact layout, i.e. avoid too long fingers, each finger in the capacitor array correspond to a half unit capacitance, thus, each finger is designed to have a capacitance of 1.25 fF. The capacitor array is laid out in metal layer 5 to reduce the parasitic capacitance to the power nets, which is routed in metal layer 1. The extracted capacitances is presented in Table A.2 in Appendix A.

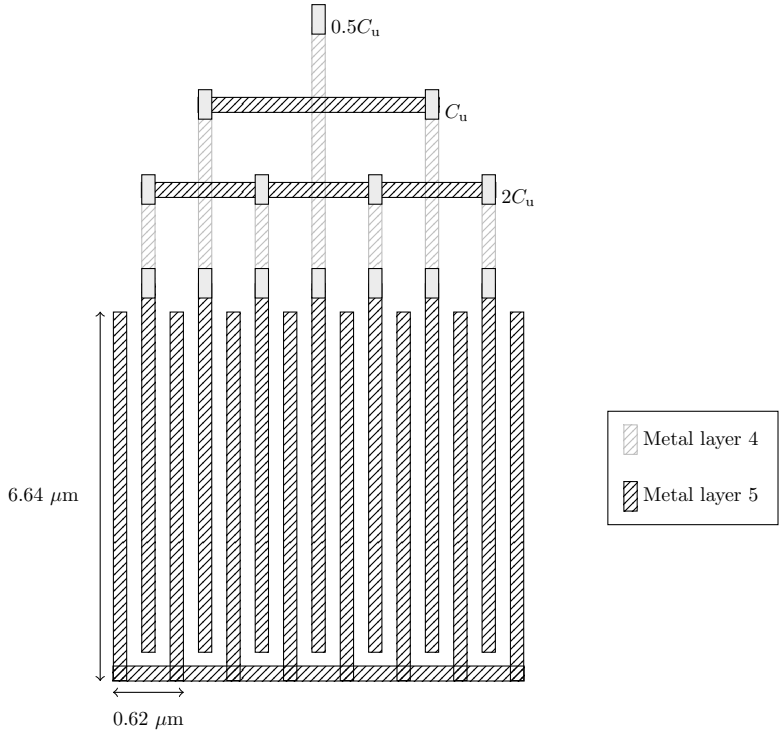


FIGURE 5.2: The principle of how the capacitor array is built up.

5.3 Layout of ADC Core

The top level layout of the proposed SAR-ADC is presented in Figure 5.3, where each module is marked with a colored box. The digital control logic is placed in the middle. It is composed of two rows of digital modules with common V_{DD} between each row and ground on the top and bottom. Since the switches of the DAC arrays have the same shape as the control logic, they are placed on the same row as the digital modules. To make the environment as equal as possible for the two DAC arrays, the positive and negative capacitor arrays are placed on each side of the control logic. The top-plates of the DACs are on the rightmost and leftmost sides of the figure. Consequently, before fabrication dummy devices should be laid out around the ADC for shielding and make the environment as equal as possible for the capacitor arrays.

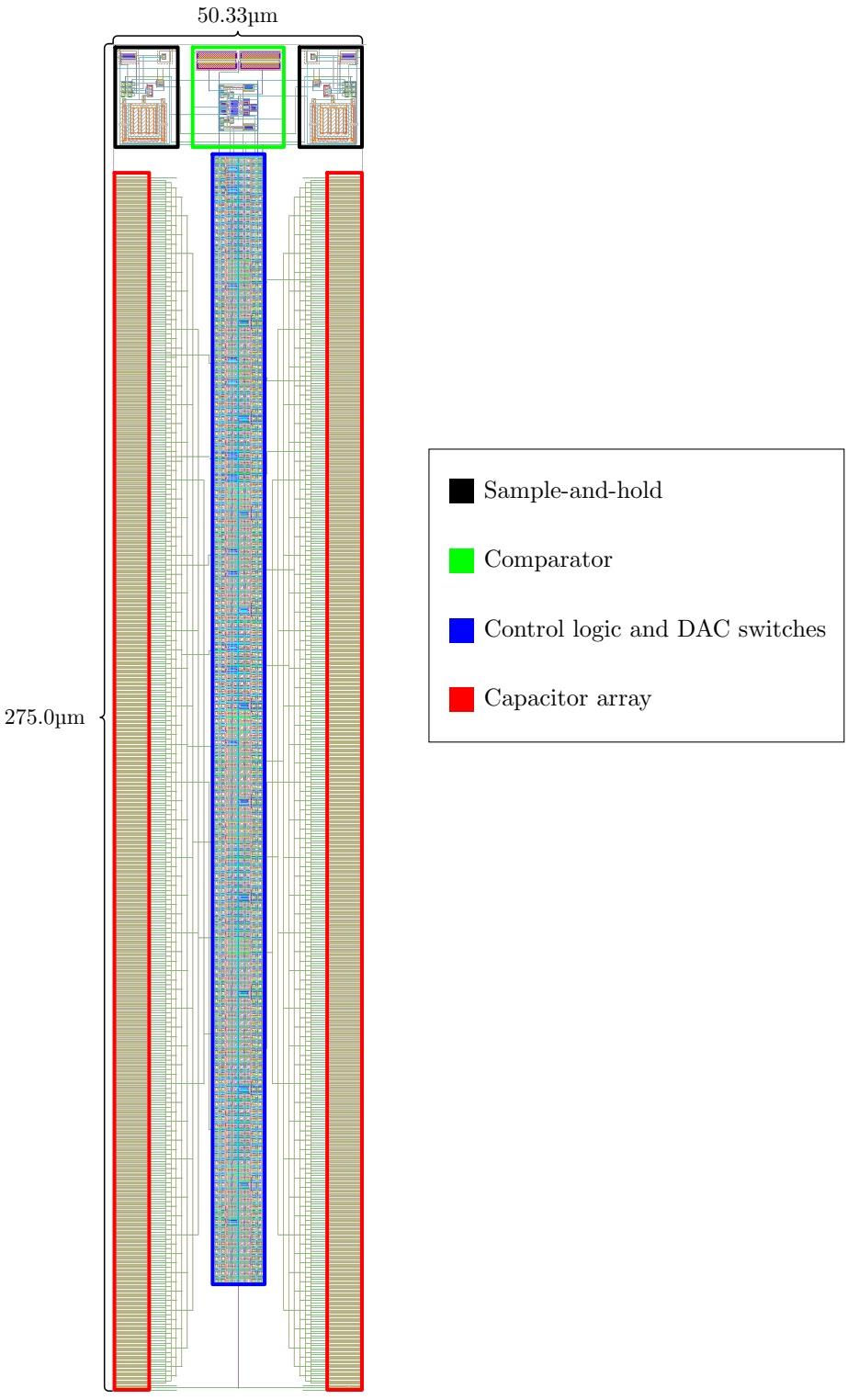


FIGURE 5.3: Top level layout of the proposed SAR-ADC.

Chapter 6

Results

The simulation results of the proposed SAR-ADC are presented in this chapter. Every single module in the proposed design was implemented on transistor level with the transistor models for the 65 nm CMOS technology provided by ST Microelectronics. An overview of the transistors sizes and other parameter used in the proposed design is presented in Table A.1 in Appendix A. Furthermore, Appendix B presents detailed information about the schematic of the proposed design. To test the performance and power consumption, the ADC was simulated with transient analysis, both with and without noise. For performance measurements, the spectrum of the output codes was calculated using fast Fourier transform (FFT). After the schematic was successfully tested, the layout was simulated. The first section will provide the simulation results from the schematic view of the ADC, while the second section presents the post-layout simulation results.

6.1 Schematic

A transient analysis without noise resulted in an ENOB 8.9 bits for the transistor level implementation of the proposed design, which proves that the design is working properly. Furthermore, Table 6.1 shows the performance and power consumption of the ADC during transient noise analysis, and with different process corners where SS stands for slow NMOS slow PMOS, FF stands for fast NMOS fast PMOS and TT stand for typical NMOS typical PMOS. Since the supply voltage is not given in the specification, V_{DD} is adjusted for the SS-corner to achieve the desired performance.

Table 6.2 shows which of the components in the ADC contributing to a performance degradation. To improve the noise performance of the comparator load

capacitances were added at the output nodes as illustrated in Figure 4.8, with $C_{\mathrm{L}} = 99.99$ fF, which is within the requirements of Equation (4.5). In Table 6.1 the noise performance of the ADC without a loaded comparator is presented to show the impact of power consumption.

The results of the Monte Carlo simulations with mismatch enabled, is presented in Table 6.3. Mismatch was mainly causing an offset in the comparator, thus, the input swing of the ADC had to be decreased for some runs to not loose to much performance.

Table 6.1: Power consumption during transient noise analysis on schematics.

Corner		SS	TT	FF	TT[1]
V_{DD} [V]		0.45	0.40	0.40	0.40
ENOB [bits]		8.11	8.29	8.25	5.82
Powoer[pW]	Comparator	667.8	524.3	538.7	51.7
	Control logic	318.0	255.3	280.5	256.8
	DAC	71.1	59.3	73.4	58.6
	S/H	5.3	4.3	4.5	4.3
	Total	1062.2	843.2	897.1	371.4

Table 6.2: Noise contribution.

Module	SNR [dB]	SNDR [dB]	ENOB [bits]
Comparator	51.70	51.64	8.29
Control logic	55.31	54.73	8.80
DAC	55.34	54.73	8.80
S/H	55.17	54.59	8.78
Total	51.67	51.68	8.29

Table 6.3: Monte Carlo simulation results with 15 runs.

	Mean	Sigma
ENOB [bits]	8.55	0.37
Total power [pW]	886.5	29.9

[1]Comparator not loaded with noise reduction capacitors on output nodes.

6.2 Post-Layout

The layout presented in Chapter 5 was simulated with 3D-extracted parasitic capacitances and resistances. In Figure 6.1 an FFT of the output codes from a transient noise analysis is presented, while the post-layout performance parameters of the proposed SAR-ADC is presented in Table 6.4.

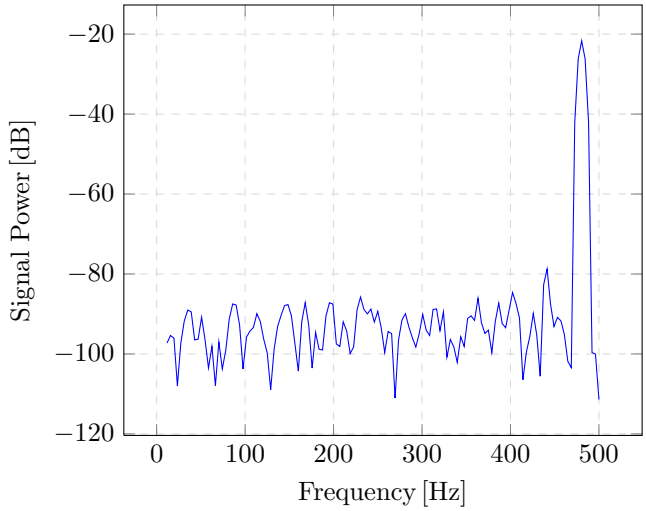


FIGURE 6.1: FFT of the ADC with transient noise analysis.

TABLE 6.4: Post-layout performance summary.

Technology	65 nm CMOS
Area	0.0138 mm^2
Sampling rate	1 kS/s
Supply voltage	400 mV
Common-mode level	200 mV
Input range [2]	380 mV
SNDR	50.89 dB
SFDR	57.04 dB
SNR	51.82 dB
ENOB	8.16 bits
Leakage power	100 pW
Total power	1.22 nW
FOM	4.27 fJ/conv.

[2]Peak-to-peak, single-ended.

Chapter 7

Analysis and Discussion

This chapter will analyze and discuss the design choices and the obtained results presented in Chapter 6. First, the top level performance of the ADC will be discussed, while the next subsections will go into detail of each module. Lastly, future work and improvements will be discussed.

7.1 ADC Core

An ENOB of 8.92 bits on the schematic implementation proves that the topology of the proposed design works as intended. Furthermore, the post-layout simulation results presented in Table 6.4 shows that the proposed SAR-ADC is capable of operating with a single supply voltage of 400 mV while consuming only 1.22 nW. Ultra-low power consumption is obtained mainly by use of custom made control logic designed for sub-threshold operation and by achieving low leakage power by utilizing the low-power high-threshold transistors provided in the 65 nm CMOS design kit. Table 6.4 shows a simulated leakage power of only 100 pW which is crucial to achieve low power consumption at low sampling rates. Low leakage power makes the proposed ADC highly suitable for use in a system that "sleeps" for most of the standby time and only operate periodically.

The total power consumption of the ADC increased from 843.2 pW to 1.22 nW after the ADC was laid out and parasitic capacitances and resistances was extracted. Power dissipated in each building block was not able to be measured in the post-layout simulation, but consider the power consumed in each module when the comparator was not loaded (Tab. 6.1), it is likely the parasitics from the layout resulted in doubled power consumption. Assuming the load capacitances alone is consuming 472.6 pW (Tab. 6.1) both pre- and post-layout as the load capacitances

is significant bigger than its parasites, results in a doubled power consumption in the remaining building blocks as $2 \cdot 371.4$ pW + 472.6 pW $\approx$ 1.2 nW. However, a doubling in power consumption due to parasites is for instance reported in [5], which uses the same 65 nm technology, and the results is therefore considered as reasonable.

Table 6.1 shows that process variation is degrading the power performance of the ADC. The worst case is in the slow corner where the supply voltage had to be increased to achieve a reasonable ENOB. This is not unexpected as the low power high threshold transistors with increased gate lengths used in the design are inherently slow, as explained in Section 4.1, however, the slow process corner makes them too slow. On the other hand are the SS and FF corners two worst case corners that are unlikely to be realistic for a fabricated chip, anyway, the supply voltage can be adjusted afterwards.

Applying noise to the transient analysis of the schematic view shows degradation in the ENOB. To investigate which of the modules that was degrading the performance noise was turned on separately in each of the modules. Table 6.2 shows that the comparator is the component mainly causing a performance degradation. It also shows that SNR and SNDR are almost equal which means the ADC is limited by noise and not distortion. However, the DAC was implemented with ideal capacitors, and mismatch was disabled during the simulation, therefore, the ADC is expected to be limited by noise.

The results of the Monte Carlo simulation with mismatch is presented in Table 6.3. It shows that the ADC is working properly with mismatch. However, mismatch did mainly cause an offset voltage in the comparator, and the performance of the ADC was then improved by adjusting the swing of the input signal. Thus, a degradation of the input swing has to be considered if the mismatch performance of the comparator is not improved. According to the background theory presented in Section 2.2, the offset error can be reduced by increasing the sizes of the input transistors in the comparator.

7.1.1 DAC

The monotonic DAC architecture was working properly and the simulation results from the transistor level model with ideal capacitors showed a power consumption of 59.3 pW. According to Equation (3.2) an average power consumption of 51 pW was expected. However, the theoretical equation does not take into account leakage power in the DAC switches, which can explain the small deviation. The DAC is consuming 7% of the total power, which is relatively low compared to [17] and [5] where the DAC is using 14% and 48% of the total power, respectively. Furthermore, in Section 4.2 the monotonic DAC architecture was favorable over the merged capacitor switching (MCS) scheme as it requires less control logic and could potentially save power from a top level perspective. Still, the MCS DAC was not

realized with associated control logic, thus, the hypothesis cannot be confirmed or disproved. Nevertheless, the simulation results shows how small impact the DAC has on the total power consumption and is therefore supporting the hypothesis.

The extracted capacitor values of the custom-designed DAC array, presented in Table A.2, shows that some of the capacitances are deriving from the intended value. Consequently, the sampled input signals are not perfectly divided by two throughout the bit cycling. Moreover, the positive and negative DAC arrays are not perfectly matched, which is causing nonlinearity. Comparing SNDR and SNR pre- and post-layout shows that distortion has increased and the ADC is no longer limited by just noise. The input swing of the ADC has been reduced due to gain in the DAC, which is caused by the biggest capacitor no longer being half the size of the total capacitance of the DAC array. Therefore, the input swing is reduced as shown in Table 6.4.

7.1.2 Control Logic

The pre- and post-layout simulation results prove that the control logic behaves as it was intended to do. Even though the transistor lengths in the custom made logic gates have been increased to $L = 0.120$ μm to reduce leakage power, the control logic is fast enough to operate at 12 kHz and Table 6.2 shows that it is not sensitive to noise.

One benefit with the proposed control logic that has not been mentioned yet; it can easily be used in an asynchronous circuits as well the proposed synchronous circuit. Since, the proposed bit cells are controlled asynchronously and the shift register is clocked by the comparator, it is possible to make the circuit asynchronous by self-clocking the comparator as done in [4]; the comparator clocks itself by feeding back the output to the comparator clock.

7.1.3 Comparator

The comparator is capable of operating at 400 mV and still being able to make decisions at a clock frequency of 12 kHz. However, as Table 6.2 shows the comparator is the component that degrades the performance when noise is applied to the analysis. To compensate for noise the comparator was loaded with capacitors on its output nodes as explained in Section 4.4. Loading the capacitor had a huge impact on the total power consumption. Without any load, the comparator consumed 51.68 pW, but the comparator had to be loaded with 99.99 fF on each output node (see Fig. 4.8) which resulted in a power consumption of 524.3 pW. Since the load capacitances had such a high impact on the total power consumption C_{L} was chosen as a compromise between performance and power consumption. Non-ideal effects such as hysteresis, kickback noise and metastability appeared to not be an issue for the comparator.

7.1.4 Sample-and-Hold

The bootstrapped switch presented in Figure 4.9, did deliver good enough accuracy for 9-bit resolution, while using a negligible amount of power. However, the boosting capacitor, C_s, had to be as big as 200.4 fF for the proposed supply voltage and DAC. This is more than four times bigger than intended from [24] where it originally was presented. On the other, hand the proposed design operates at 400 mV compared to 1 V and the sampling switch uses a high-threshold device, which require a bigger capacitor for boosting the control voltage.

7.2 Comparison with State-of-the-Art

An overview of state-of-the-art ultra-low power ADCs together with the proposed design is presented in Table 7.1. It shows that the power consumption of the proposed design less than half of the previous state-of-the-art [5]. The results obtained in this work are from post-layout simulations with 3D-extracted parasitics, however, [5] presented a power consumption of 2.81 nW from the post-layout simulation results, while the fabricated chip consumed 3 nW. Since the same technology and transistors types are used in both designs it is likely to assume the same tendencies for the proposed design, nevertheless, comparing post-layout results shows that the proposed design is consuming half of the power. On the other hand the resolution of the proposed design is 8.16 bits compared to 9.1 bits, however, this work achieves a better figure-of-merit.

Table 7.1: Comparison of ultra-low power SAR-ADCs.

Parameter	[17]	[5]	[35]	[This work]
Technology	0.18 μm	65 nm	0.18 μm	65 nm
Area [mm^2]	0.097	0.037	0.04	0.0138
Sampling rate [kS/s]	2.5	1	1	1
Resolution [bit]	10	10	9	9
Supply voltage [V]	0.4	0.7	1	0.4
Power [nW]	6.5	3	9.87	1.22
ENOB [bits]	9.4	9.1	8.7	8.16
FOM [fJ/conv.]	3.98	5.5	23.7	4.27

The layout of the DAC in this design, presented in Section 5.2, contributed to a total small area of the ADC. Compared to other state-of-the-art ADCs, the proposed design is using less area. However, in a physical chip implementation the area may increase do to the need of shielding and dummy devices.

7.3 Future Work

First, the performance and power consumption of the proposed design is mainly limited the comparator. Thus, improving the comparator will be very efficient for the total performance and power consumption of the ADC. According to the pre-layout results from Table 6.1, the proposed design may have the potential of sub-nanopower operation if the comparator is improved.

Secondly, post-layout simulation results showed an increased distortion compared to the results from the schematics. It is assumed the DAC arrays are the main contributors to distortion. However, further investigations should be done and improvements should be made to achieve a better ENOB from the layout, but also on the schematics.

Thirdly, mismatch was tested with just 15 Monte Carlo runs on the schematics, thus, more testing should be done. If possible, should mismatch be tested on the layout as well.

Finally, when the above is fixed, the proposed design can be made ready for fabrication and measurements on chip.

Chapter 8

Concluding Remarks

This thesis has presented the design of an ultra-low power successive approximation register analog-to-digital converter that was implemented and laid out in 65 nm CMOS technology. The post-layout simulation result shows a power consumption of 1.22 nW when the ADC is running at 1 kS/s with a supply voltage of 400 mV. Ultra-low power consumption is achieved by the use of low power and high threshold voltage transistors, custom logic gates optimized for sub-threshold operation and a reference DAC with a monotonic switching procedure. The effective resolution of the ADC is 8.16 bits, which results in a figure-of-merit of 4.27 fJ/conversion-step. Suggestions for further work and improvements have been presented, however, the simulated power consumption is among the best of the currently state-of-the-art ultra-low power ADCs.

Bibliography

[1] B. Murmann, "ADC performance survey 1997-2013," 2013. [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

[2] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," *Electronics Letters*, vol. 46, no. 9, pp. 620 –621, Apr. 2010.

[3] P. P. Mercier, A. C. Lysaght, S. Bandyopadhyay, A. P. Chandrakasan, and K. M. Stankovic, "Energy extraction from the biologic battery in the inner ear," *Nature Biotechnology*, vol. 30, no. 12, pp. 1240–1243, Dec. 2012. [Online]. Available: http://www.nature.com/nbt/journal/v30/n12/full/nbt.2394.html

[4] P. Harpe, E. Cantatore, and A. v. Roermund, "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with data-driven noise reduction," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 270–271.

[5] D. Zhang and A. Alvandpour, "A 3-nW 9.1-ENOB SAR ADC at 0.7 v and 1 kS/s," in *ESSCIRC (ESSCIRC), 2012 Proceedings of the*, Sep. 2012, pp. 369 –372.

[6] J. E. Bjerkedok, "Subthreshold real-time counter," Master's Thesis, Norwegian University of Science and Technology, Trondheim, Norway, Jun. 2013.

[7] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed. Wiley, Dec. 2011.

[8] M. J. Pelgrom, *Analog-to-Digital Conversion*. Springer, 2010.

[9] M. Pelgrom, A. C. J. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[10] M. Alioto, "Understanding DC behavior of subthreshold CMOS logic through closed-form analysis," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1597–1607, 2010.

[11] ——, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 3 –29, Jan. 2012.

[12] T.-H. Kim, J. Keane, H. Eom, and C. Kim, "Utilizing reverse short-channel effect for optimal subthreshold circuit design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 15, no. 7, pp. 821–829, 2007.

[13] E. Snchez-Sinencio and A. G. Andreou, Eds., *Low-Voltage/Low-Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits*, 1st ed. Wiley-IEEE Press, Jan. 1999.

[14] A. Nikoozadeh and B. Murmann, "An analysis of latch comparator offset due to load capacitor mismatch," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 12, pp. 1398–1402, 2006.

[15] L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog circuit design in nanoscale CMOS technologies," *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1687–1714, 2009.

[16] X. Zhou and Q. Li, "A 160mV 670nW 8-bit SAR ADC in 0.13 μm CMOS," in *2012 IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2012, pp. 1 –4.

[17] D.-S. Jo and S.-T. Ryu, "A 0.4V 6.5nW 10b 2.5kS/s asynchronous SAR ADC," in *2011 IEEE MTT-S International Microwave Workshop Series on Intelligent Radio for Future Personal Terminals (IMWS-IRFPT)*, Aug. 2011, pp. 1 –2.

[18] H.-Y. Tai, H.-W. Chen, and H.-S. Chen, "A 3.2fJ/c.-s. 0.35V 10b 100KS/s SAR ADC in 90nm CMOS," in *2012 Symposium on VLSI Circuits (VLSIC)*, Jun. 2012, pp. 92 –93.

[19] D. Zhang, "Design of ultra-low-power analog-to-digital converters," Licentiate Thesis, Linkping Studies in Science and Technology, SE-581 83 Linkping, Sweden, 2012.

[20] J. McCreary and P. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques - part i," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 6, pp. 371 –379, Dec. 1975.

[21] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731 –740, Apr. 2010.

[22] J. Guerber, M. Gande, H. Venkatram, A. Waters, and U.-K. Moon, "A 10b ternary SAR ADC with decision time quantization based redundancy," in *Solid State Circuits Conference (A-SSCC), 2011 IEEE Asian*, Nov. 2011, pp. 65 –68.

[23] W. Guo and S. Mirabbasi, "A low-power 10-bit 50-MS/s SAR ADC using a parasitic-compensated split-capacitor DAC," in *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2012, pp. 1275 –1278.

[24] T.-V. Cao, S. Aunet, and T. Ytterdal, "A 9-bit 50MS/s asynchronous SAR ADC in 28nm CMOS," in *NORCHIP, 2012*, Nov. 2012, pp. 1–6.

[25] Y.-Z. Lin, C.-C. Liu, G.-Y. Huang, Y.-T. Shyu, Y.-T. Liu, and S.-J. Chang, "A 9-bit 150-MS/s subrange ADC based on SAR architecture in 90-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 3, pp. 570 –581, Mar. 2013.

[26] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "10-bit 30-MS/s SAR ADC using a switchback switching method," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. PP, no. 99, p. 1, 2012.

[27] J. Kim, S.-I. Lim, K.-S. Yoon, and S. Lee, "Design of a 12-b asynchronous SAR CMOS ADC," in *SoC Design Conference (ISOCC), 2011 International*, Nov. 2011, pp. 70 –72.

[28] W. Hu, D. Y. Lie, and Y.-T. Liu, "An 8-bit single-ended ultra-low-power SAR ADC with a novel DAC switching method," in *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2012, pp. 2349 –2352.

[29] A. T. Do, C. K. Lam, Y. S. Tan, K. S. Yeo, J. H. Cheong, X. Zou, L. Yao, K. W. Cheng, and M. Je, "A 160 nW 25 kS/s 9-bit SAR ADC for neural signal recording applications," in *New Circuits and Systems Conference (NEWCAS), 2012 IEEE 10th International*, Jun. 2012, pp. 525 –528.

[30] Y.-K. Cho, J.-H. Jung, and K. C. Lee, "A 9-bit 100-MS/s flash-SAR ADC without track-and-hold circuits," in *2012 International Symposium on Wireless Communication Systems (ISWCS)*, Aug. 2012, pp. 880 –884.

[31] C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, and C.-M. Huang, "A 1V 11fJ/conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18 μm CMOS," in *2010 IEEE Symposium on VLSI Circuits (VLSIC)*, Jun. 2010, pp. 241 –242.

[32] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for medical implant devices," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1585 –1593, Jul. 2012.

[33] C.-Y. Liou and C.-C. Hsieh, "A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with charge-average switching DAC in 90nm CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 280–281.

[34] S.-W. Chen and R. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2669 –2680, Dec. 2006.

[35] A. T. Do, C. K. Lam, Y. S. Tan, K. S. Yeo, J. H. Cheong, L. Yao, M. T. Tan, and M. Je, "A 9.87 nW 1 kS/s 8.7 ENOB SAR ADC for implantable epileptic seizure detection microsystems," in *2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Dec. 2012, pp. 1 –4.

[36] T. K. H. Roy and T. Teo, "A 0.9V 100nW rail-to-rail SAR ADC for biomedical applications," in *International Symposium on Integrated Circuits, 2007. ISIC '07*, Sep. 2007, pp. 481 –484.

[37] T. Sundstrm, B. Murmann, and C. Svens, "Power dissipation bounds for high-speed nyquist analog-to-digital converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 3, pp. 509–518, Mar. 2009.

[38] S. Narendra, V. De, S. Borkar, D. Antoniadis, and A. Chandrakasan, "Full-chip subthreshold leakage power prediction and reduction techniques for sub-0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 3, pp. 501–510, 2004.

[39] H. Alstad and S. Aunet, "Three subthreshold flip-flop cells characterized in 90 nm and 65 nm CMOS technology," in *11th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, 2008. DDECS 2008*, Apr. 2008, pp. 1 –4.

[40] V. Suzuki, K. Odagawa, and T. Abe, "Clocked CMOS calculator circuitry," *IEEE Journal of Solid-State Circuits*, vol. 8, no. 6, pp. 462–469, 1973.

[41] P. Harpe, C. Zhou, Y. Bi, N. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1585 –1595, Jul. 2011.

Appendix A

Design Parameters

The parameters used in the proposed design are presented in Table A.1, while the extracted capacitances of the DAC arrays are presented in Table A.2. The sub-threshold gates introduced in Section 4.3.1 was implemented as presented in Figure 4.3. Each gate was balanced by applying $V_{\mathrm{DD}}/2$ to the inputs and tuning the transistor widths of both NMOS and PMOS until the output voltage were approximately $V_{\mathrm{DD}}/2$. The gate lengths were chosen $L = 2L_{\mathrm{min}} = 0.12$ μm, to reduce the leakage currents while still achieving a reasonable transition speed. All transistor sizes in the digital control logic were chosen equally to achieve regularity in the layout. The DAC switches were implemented as standard inverters, i.e. with one PMOS and one NMOS, capable of driving the biggest capacitors in the DAC array. Every transistor in the design are low power high threshold transistors, expect M_{1-4} in the comparator.

TABLE A.1: Transistor sizes and other device parameters.

Cell	Device	W [μm]	L [μm]	C [fF]
Regular cell (Fig. 4.3a)	Both PMOS	0.230	0.120	
	Both NMOS	0.170	0.120	
DAC switches	PMOS	1.400	0.060	
	NMOS	0.200	0.060	
Comparator (Fig. 4.8)	$M_{1,2}$	1.000	0.090	
	$M_{3,4}$	0.400	0.120	
	$M_{0,5,6}$	0.700	0.120	
	$M_{7\text{-}10}$	0.200	0.120	
	C_{L}	1.000	7.640	99.99
Bootstrapped switch (Fig. 4.9)	Sampling switch	2.250	0.180	
	All NMOS	0.140	0.090	
	All PMOS	0.170	0.090	
	C_{s}	6.250	6.250	200.4

TABLE A.2: Extracted capacitances of the DAC arrays.

	Positive DAC		Negative DAC	
Capacitor	Value [fF]	Normalized	Value [fF]	Normalized
C_8	321.28	127.24	321.30	127.25
C_7	161.69	64.04	161.69	64.04
C_6	80.75	31.98	80.74	31.98
C_5	40.37	15.99	40.37	15.99
C_4	20.18	7.99	20.18	7.99
C_3	10.10	4.00	10.10	4.00
C_2	5.05	2.00	5.05	2.00
C_1	2.53	1.00	2.52	1.00

Appendix B

Schematics

Schematics of the design, captured form Cadence, and small modules not presented in detail previous in the thesis are presented in this appendix.

Figure B.1 shows generation of internal clock signals, ϕ and $\overline{\phi}$, which are used to clock the control logic. They are generated by the comparator outputs, $comp_p$ and $comp_n$. Figure B.2 shows the generation of the external ready signal, which indicates that the bits are ready to be read, and the internal reset signal used for resetting the shift register. In Figure B.3 is the circuit for generating the sampling signal for the sampling switches presented. The signal denoted $\overline{clk}$ are from the external clock. A top level schematic captured from Cadence is presented in Figure B.4, note that capacitors are removed as they were custom made in the layout.

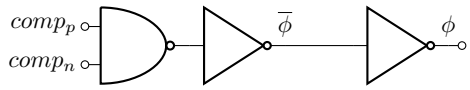


FIGURE B.1: Internal clock generator.

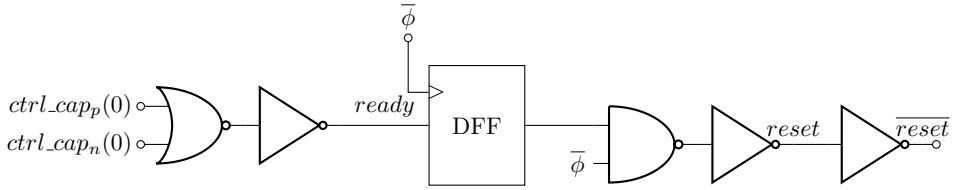


FIGURE B.2: Generation of ready and reset signal.

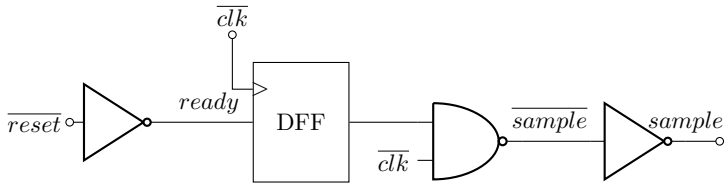


FIGURE B.3: Generation of sampling signal.

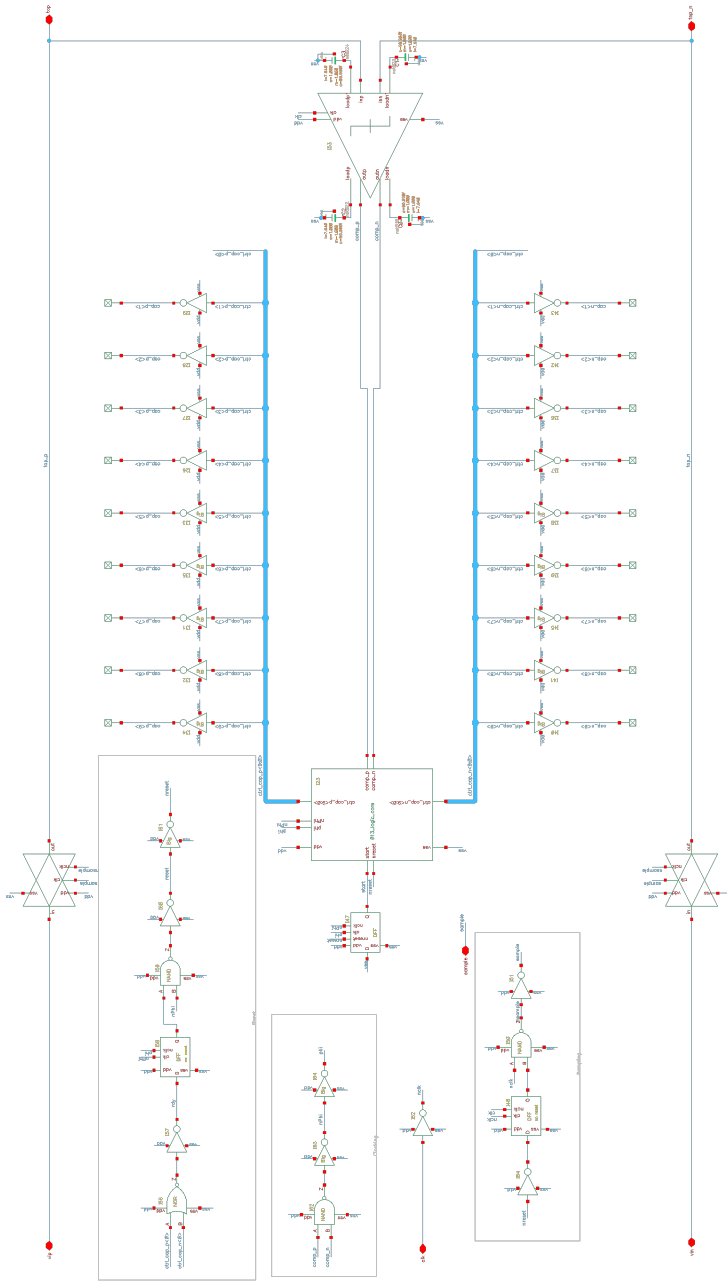


FIGURE B.4: Schematics of the top level, without capacitors.