Experimental Performance Comparison of Six-Pack SiC MOSFET and Si IGBT Modules Paralleled in a Half-Bridge Configuration for High Temperature Applications

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***Abstract*—In this paper, the switching performance of a six-pack SiC MOSFET module (CCS050M12CM2) is investigated experimentally using a standard double pulse test method. The upper three and the lower three MOSFETs of the CCS050M12CM2 are paralleled forming a half-bridge configuration. Moreover, the performance comparison of the CCS050M12CM2 is carried out with a pin to pin compatible Si IGBT module (FS75R12KT4_B15) of the same rating. Thus, switching and driving energy losses can be compared fairly. Laboratory results show that CCS050M12CM2 switches much faster compared to FS75R12KT4_B15 provided the same gate resistor is used. The measured total driving and switching energy losses are approximately 4 times in FS75R12KT4_B15 compared to CCS050M12CM2 at 25 °C. Moreover, the total switching energy loss is nearly independent of the temperature for CCS050M12CM2, whereas, FS75R12KT4_B15 has 1.6 times higher switching energy loss at a junction temperature of 175°C compared to 25 °C.**

I. Introduction

For high temperature applications such as induction heating, photovoltaics, down-hole oil development, and hybrid and electric vehicles; low losses, thermally stable and compact converters are the prerequisites [1]–[3]. Paralleling helps to achieve the required power level for such applications with today's available SiC power devices and also reduces the conduction loss. It can be done in different ways such as discrete paralleling [4], [5], multiple chip paralleling within the single module [6], [7], and outside the module [8] also referred as module paralleling [9]. Discrete and chip paralleling techniques have their own pros and cons. Both inside and outside chip paralleling give lower parasitic inductance compared to discrete paralleling as the chips are closely located.

However, the focus of this paper is on paralleling of the chips outside the module mainly for achieving improved temperature performance compared to paralleling of the chips inside the module.

SiC MOSFETs can take over the role of Si IGBTs because of the following four reasons. Firstly, the gate drive requirement is more adaptable and the gate drive charge/current is comparable to IGBT devices. Secondly, due to the lack of p-n junction in the drain-source of the device, paralleling of devices decreases the conduction loss. For instance, when IGBTs are paralleled, the on-resistance will decrease, but the p-n voltage drop will be constant. However, in MOSFETs, the voltage drop and hence the power loss is only dependent on the on-resistance of the device. Thirdly, SiC MOSFETs can be operated at junction temperatures in excess of 250 °C [10], which allows higher ambient temperature and a higher temperature difference between ambient and junction, thereby less effort in thermal management, as long as the hermetically shielded packages are used. And fourthly, SiC MOSFETs switch very fast, resulting in low switching loss, provided low inductive layout is implemented.

Hence, the outstanding material performance of SiC motivates research on quantification of the losses and comparison with the Si counterparts. In the present paper, a comparison of switching performance of a SiC MOSFET module (CCS050M12CM2) which has the same rating and is pin to pin compatible with a Si IGBT module (FS75R12KT4_B15) is carried out, in order to observe the consequences in switching and driving energy loss.

Additionally, practical solutions for the circuit layout are considered, i.e. separate gate and source return along with resistance in the return path for improved gate coupling between the different paralleled chips. A small gate source capacitor is added in order to maintain the gate voltage stability. Decoupling capacitors are added near the module under test for reducing the inductive loop which will eventually reduce the overshoot and ringing during the switching transients. The optimal value of the gate resistance is decided by the trade-off between the current overshoot and the switching energy loss in CCS050M12CM2. The switching energy loss in FS75R12KT4_B15 is measured for the same value of gate resistor as optimized for CCS050M12CM2.

II. Methodology and Laboratory Setup

Basically, the double pulse test setup is an inductive load buck or boost converter as shown in Fig. 1, where a switching

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device is tested by injecting two switching pulses. These pulses put considerable stress on the device without itself-heating, as the double pulses are given at a very low frequency; for example 1-5 Hz. The first pulse is adjusted to ramp up the current in the inductive load to the value of interest. In order to record the turn-on and turn-off waveforms at a similar current level, the delay between the first and second pulse is maintained very small for instance; 3-10 μs [2]. Finally, the first turn-off and the second turn-on waveforms are recorded.

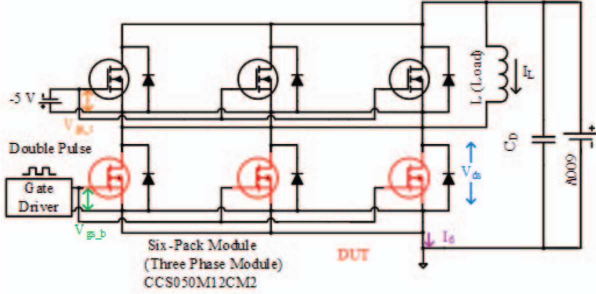

Fig. 1: Circuit diagram. The upper and the lower three transistors are paralleled, forming a single half-bridge configuration

Fig. 2: Six-pack SiC MOSFET (CCS050M12CM2) module

The junction temperature of the device under test (DUT is controlled by a hotplate so that the electrical measurements such as drain current, drain source voltage and gate source voltage can be recorded at different operating temperatures. To be able to vary the temperature of the module, which is mounted to a heat sink, the heat sink is placed over the hotplate. A temperature sensor (K-type) is mounted on the heat sink of the DUT to be able to monitor the temperature. Additionally, the six-pack module has a NTC thermistor, which is used to cross-check the temperature measured by the K-type sensor. Once the desired steady-state temperature is reached, the measurements are taken quickly to avoid self-heating of the device. The temperature measured by the external sensor was in good agreement with the temperature measured by the NTC thermistor in the experiments reported here.

The complete laboratory setup is depicted in Fig. 3. An isolated gate driver with an adjustable output voltage [11] is used for driving the CCS050M12CM2. The gate voltage is set to 20 V for the turn-on and -5 V for the turn-off. A function generator is used for the double pulse generation. A single layer air core inductor is used as a load in order to realize a low stray capacitance. The drain current is measured by a Rogowski coil (CWT6B, 30 MHz), the drain source voltage is measured by a high voltage single ended probe (P5100A, 500 MHz, and the gate source voltage is measured by a low voltage single ended probe (TPP100, 1 GHz).

III. Theoretical Analysis and Anticipated Measurement Results

This section focuses on the expected results from the laboratory measurements based on the information provided in datasheets of CCS050M12CM2 and FS75R12KT4_B15.

A. Datasheet Analysis of the Modules Under Test

The typical characterizing parameters of CCS050M12CM2 and FS75R12KT4_B15 are obtained from the datasheets and are listed in Table I. The input capacitance (C_{iss}) and the reverse transfer capacitance (C_{rss}) are the capacitances at a drain source voltage of 600 V [12], [13].

C_{iss}, C_{rss} and Q_g (the gate charge) are all lower in CCS050M12CM2 than in FS75R12KT4_B15, by a factor of 1.5, 11, and 3 respectively as shown in Table I. This translates to faster switching of CCS050M12CM2 compared to FS75R12KT4_B15 as long as the gate resistances are kept equal.

However, CCS050M12CM2 has higher stray inductance (30 nH) compared to FS75R12KT4_B15 (19 nH). Higher stray inductance together with fast switching of CCS050M12CM2 will result in more oscillations in the current and voltage waveforms. Although the stray inductance from the PCB can be further reduced, the stray inductance inside the module will still cause oscillations in conjunction with the stray capacitances of the module, such as the junction capacitance of anti-parallel diodes and the output capacitance of MOSFETs or IGBTs.

The SiC Schottky diode has 1.2 times higher forward voltage drop compared to the Si diode as shown in Table II. However, the capacitive charge is very low in the SiC schottky diode, which aids the fast switching and a smaller current overshoot during turn-on.

B. Influence of Stray Inductance and Stray Capacitance

CCS050M12CM2 consists of 3 bridge-legs formed by the chip as used in C2M0025120D. During the turn-on, the parallel stray capacitances of the lower side MOSFETs and the anti-parallel diodes are in series with the corresponding upper side capacitances, such that the total stray capacitance

TABLE I: Six-pack Modules used in the measurement

Parts Six-pack	R_{gint} (Ω)	C_{iss} (nF)	C_{rss} (nF)	L_{stray} (nH)
CCS050M12CM2 (Cree)	1.5	2.81	0.014	30
FS75R12KT4_B15 (Infineon)	10	4.3	0.16	19

TABLE II: Anti-parallel diodes of the modules

Diodes Free-wheeling	V_F (V)	Q_{rr} (μC)	I_F (A)
SiC Schottky (Cree)	2	0.28	50
Si (Infineon)	1.65	16	75

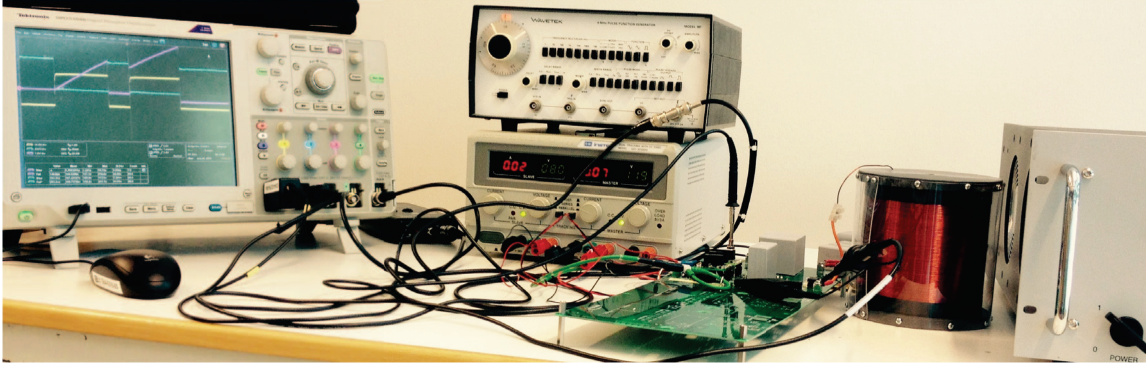

Fig. 3: Hardware setup

(C_{stray}) can be calculated to be 0.68 nF.
C_{stray} = 3/2 · (C_{oss} + C_j) = 1/2 · (0.66 + 0.7) = 0.68

During the turn-off, the capacitance of the upper side MOSFETs and anti-parallel diodes in a half-bridge is zero as the diode shorts all of them during the free-wheeling period. Thus, the total capacitance is estimated to be 1.36 nF.

L_{stray} (the switching loop stray inductance) and C_{stray} cause high frequency (MHz) oscillations during the switching transients which are illustrated in details in section V.

IV. Consideration of Gate Driver

In this section, the gate drivers used for the two different modules under test, the influence of an additional gate source capacitance in the gate voltage stability and the optimization of the gate resistor are discussed.

1) Gate Driver: CCS050M12CM2 is driven by an isolated gate driver with a flexible output voltage. A gate voltage of -5 V is applied for all paralleled upper MOSFETs in order to ensure that they are turned-off all the time. The three paralleled lower MOSFETs are driven by a gate driver with turn-on voltage of 20 V and turn-off voltage of -5 V. These MOSFETs can be turned-off using only 0 V like the Si MOSFETs, but the negative voltage is used for achieving a faster turn-off process.

FS75R12KT4_B15 is driven using the same gate driver, but with a small modification in the DC-DC converter so that it provides +15 V during turn-on and -15 V during turn-off. The power requirement for driving FS75R12KT4_B15 is 3.8 times that of CCS050M12CM2 at 10 kHz switching frequency as calculated in Table III. This is reasonable as the gate charge of FS75R12KT4_B15 is 1710 nC which is approximately 3 times that of CCS050M12CM2.

TABLE III: Power Loss in Gate Driver

Parts Six-pack	V_g (V)	Q_g (nC)	P (mW)
CCS050M12CM2 (Cree)	+20/-5	540	135
FS75R12KT4_B15 (Infineon)	±15	1710	513

2) Separate Gate and Source Path: A separate turn-on and turn-off paths are provided in a gate driver board to control the switching process independently. For better decoupling and reducing the influence of any asymmetry of the source inductances of the paralleled devices, the gate resistors of the paralleled MOSFETs are splitted into a gate side and a source side. In this laboratory experiment, the gate resistance of about 3 Ω and a source resistance of about 1 Ω is considered.

3) Influence of Gate Source Capacitance: Fig. 4 illustrates the influence of placing a small additional capacitance between gate and source (1 nF) for achieving better gate voltage stability. The threshold voltage of CCS050M12CM2 is about 2 V, while the amplitude of transient without the additional capacitance is 5 V, as shown in Fig. 4. If this transient is not suppressed, it can turn on both the upper and the lower switches at the same time in a half-bridge configuration, commonly referred to as shoot-through. Therefore, it is a good practice to add a small gate source capacitor for both the upper and lower MOSFETs.

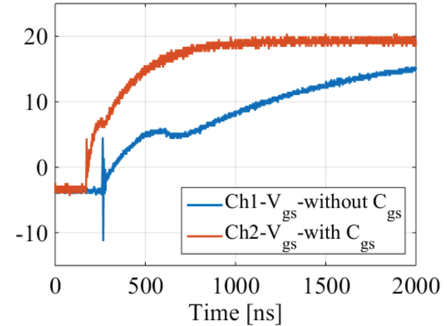

Fig. 4: Influence of an additional gate source capacitance

4) Choice of Gate Resistor: With increasing gate resistance, the current and voltage overshoots decrease but the switching becomes slower. This results in increased switching loss. Therefore, gate resistances of 20 Ω and 15 Ω are selected during turn-on and turn-off respectively, as a trade-off between overshoot and switching loss. Table IV illustrates the current rise, voltage fall and current overshoot for varying gate resistance at 600 V dc link voltage and 20 A load current as an example. However, the details during the turn-off are not shown here.

TABLE IV: Current rise, voltage fall and current overshoot at 600 V dc link voltage and 20 A current for CCS050M12CM2

R_{gon} (Ω)	I_{rise} (ns)	V_{fall} (ns)	$I_{overshoot}$ (A)
10	30	63	44.6
16.67	34	87	29.4
20	44	91	25.8
25	52	103	21.6
33.3	63	131	16.6
50	80	164	12
100	157	325	6.8

V. Switching Characterization of SiC MOSFET and Si IGBT module

This section investigates the turn-on and turn-off switching transients of the six-pack modules. The switching voltage gradient (dv/dt) and current gradient (di/dt), rise and fall times of current and voltage, and switching energy loss are illustrated. These parameters are calculated based on the following definitions.

The dv/dt is the slope of the drain voltage measured at 50 % of the nominal drain voltage. Similarly, the di/dt is the slope of the drain current measured at 50 % of the nominal current.

The voltage fall or current fall time is the time it takes for the drain voltage/drain current to drop from 90 % to 10 % of its nominal value. Likewise, the voltage rise or current rise time is the time it takes for the drain voltage/drain current to rise from 10 % to 90 % of the nominal value.

The switching energy is calculated by integrating the product of voltage and current during switching of the DUT. The range of integration time is taken from current zero to voltage zero during the turn-on and from voltage zero to current zero during the turn-off.

For accurate measurements, the oscilloscope, the current and voltage probes are fully compensated prior to measurement and phase delays between probes are adjusted or de-skewed.

A. Laboratory Testing of the CCS050M12CM2 Module

The turn-on and turn-off transients of CCS050M12CM2 are depicted in Fig. 5 and Fig. 6 respectively. Ch1 is the gate source voltage, Ch2 is the drain source voltage and Ch3 is the drain current. An oscillation frequency of approximately 14 MHz is observed during both turn-on and turn-off. These oscillations are due to the stray inductance in the switching loop (printed circuit board and module itself) and the module parasitic capacitances as discussed in section III (B). During the turn-off, the voltage overshoot is 103 V and di/dt is 0.88 kA/μs. From this, the switching loop inductance is estimated to be 103/0.88 = 117 nH.

1) dv/dt and di/dt: are summarised in Table V. Paralleling of devices increases the total input capacitance (C_{iss}), output capacitance (C_{oss}) and the miller capacitance (C_{gd}). For this reason, the drain current and drain voltage slew rates decrease compared to the single device. Thereby, the device becomes slower. During turn-on, dv/dt is smaller with higher load current, as shown in Table V. This implies slower discharging of C_{oss}. At the same time, the charging of C_{oss} is faster during

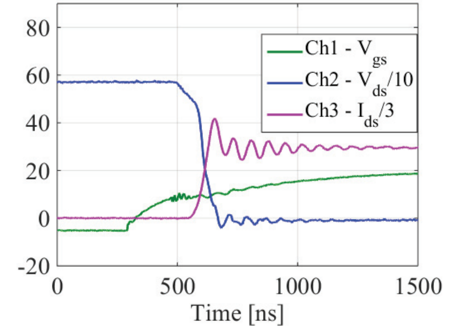

Fig. 5: Turn-on transients of CCS050M12CM2 at 600 V dc link voltage, 90 A load current and gate resistor of 20 Ω

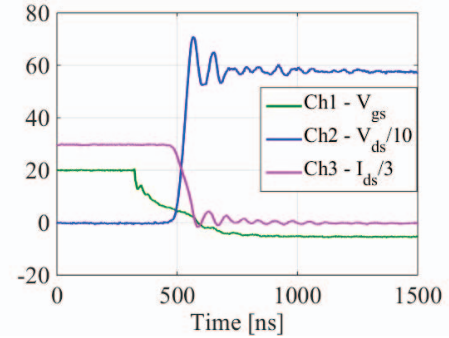

Fig. 6: Turn-off transients of CCS050M12CM2 at 600 V dc link voltage, 90 A load current and gate resistor of 15 Ω

turn-off at higher load current. This is further seen in Table VI, where the voltage fall time increases and the rise time decreases for higher load current.

TABLE V: Voltage and current gradients during turn-on and turn-off transients for CCS050M12CM2 at 600 V dc link

	Turn-on		Turn-off	
Load current (A)	di/dt (kA/μs)	dv/dt (kV/μs)	di/dt (kA/μs)	dv/dt (kV/μs)
30	0.96	8.57	0.35	6.07
60	1.36	7.5	0.65	9.92
90	1.78	7	0.88	10.54
120	1.94	6.47	1.61	12.40
150	2.18	5.35	2.53	13.34

2) rise time and fall time: Table VI further elucidates the charging and discharging phenomena in MOSFET.

TABLE VI: Current rise, voltage fall during turn-on and turn-off transients for CCS050M12CM2 at 600 V dc link voltage

	Turn-on		Turn-off	
Load current (A)	I_{rise} (ns)	V_{fall} (ns)	I_{fall} (ns)	V_{rise} (ns)
30	37	92	126.4	82.4
60	42.6	103.4	81.2	53
90	50.8	114.2	75.4	45
120	58.8	125.8	70.6	39.8
150	66.6	138	64.6	36

3) Switching Energy Loss: Fig. 7 and Fig. 8 depict the turn-on and turn-off switching energy loss of CCS050M12CM2

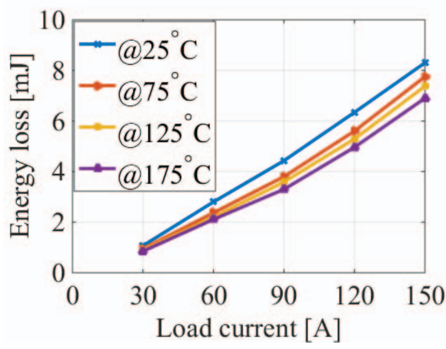

Fig. 7: Turn-on loss of CCS050M12CM2 at 600 V

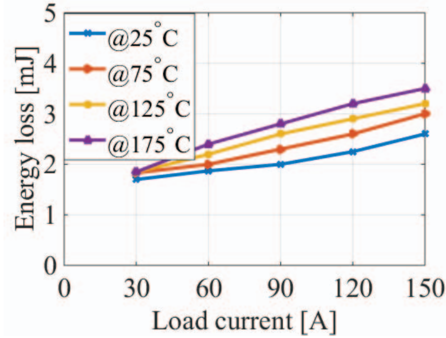

Fig. 8: Turn-off loss of CCS050M12CM2 at 600 V

at 600 V dc link voltage and varying load currents and junction temperatures. The measurement results show that the turn-on switching energy loss decreases slightly with increased junction temperature. This can be explained by the fact that the threshold voltage decreases with higher junction temperature of the device under test as shown in the datasheet of CCS050M12CM2 [12]. This results in faster turn-on of the device. On the other hand, the turn-off switching energy loss increases somewhat for higher temperatures, but with a slightly smaller amount than the decrease in turn-on switching energy loss.

B. Laboratory Testing of the FS75R12KT4_B15 Module

The turn-on and turn-off transients of FS75R12KT4_B15 are depicted in Fig. 9 and Fig. 10, respectively. All the measurements for FS75R12KT4_B15 are recorded for a gate resistance of 20 Ω during turn-on and 15 Ω during turn-off as in SiC CCS050M12CM2 module in order to make a comparison keeping the same value of gate resistor. During the turn-on, the recovery current of the anti-parallel Si diode in the FS75R12KT4_B15 module causes a current peak as exemplified in Fig. 9.

The switching waveforms for FS75R12KT4_B15 have almost no ringing compared to CCS050M12CM2 which is mainly due to two reasons. The first reason is that FS75R12KT4_B15 has a lower package stray inductance of 19 nH compared to 30 nH for the CCS050M12CM2, as shown in section III (A) Table I. Such a fast switching device should have a package with lower stray inductance. The second reason

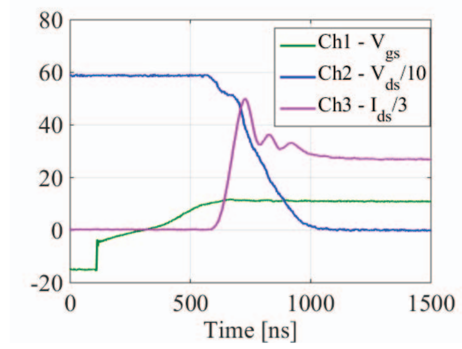

Fig. 9: Turn-on transients of FS75R12KT4_B15 at 600 V dc link voltage, 90 A load current and gate resistor of 20 Ω

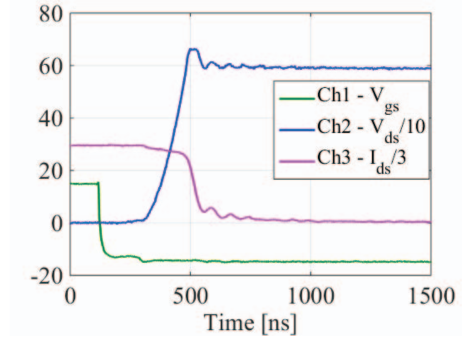

Fig. 10: Turn-off transients of FS75R12KT4_B15 at 600 V dc link voltage, 90 A load current and gate resistor of 15 Ω

is that FS75R12KT4_B15 has higher gate resistance which is deliberately chosen to make a comparison between the two devices for the same value of gate resistance. It should be mentioned that this is somewhat disadvantageous for the FS75R12KT4_B15. It would be a more fair comparison to test the IGBT module with optimized gate resistance as well.

1) dv/dt and di/dt: Table VII illustrates dv/dt and di/dt.

TABLE VII: Voltage and current gradients during turn-on and turn-off transients for FS75R12KT4_B15 at 600 V dc link

	Turn-on		Turn-off	
Load current (A)	di/dt (kA/μs)	dv/dt (kV/μs)	di/dt (kA/μs)	dv/dt (kV/μs
30	0.4	1.8	0.18	3.1
60	0.54	1.3	0.37	4.2
90	0.68	1.0	0.61	4.7
120	0.75	0.85	0.81	5.5
150	0.8	0.83	1.1	6

TABLE VIII: Current rise, voltage fall during turn-on and turn-off transients for FS75R12KT4_B15 at 600 V dc link

	Turn-on		Turn-off	
Load current (A)	I_{rise} (ns)	V_{fall} (ns)	I_{fall} (ns)	V_{rise} (ns)
30	82	269	163	160
60	114	383	161	120
90	133	484	147	107
120	165	588	141	90
150	203	602	135	82

2) rise time and fall time: From Table VI and Table VIII, it is clear that FS75R12KT4_B15 switches much slower compared to CCS050M12CM2.

3) Switching Energy Loss: Fig. 11 and Fig. 12 depict the turn-on and turn-off switching energy losses of FS75R12KT4_B15 at varying temperature. The recovery current of the Si diode is the primary cause of the increased turn-on loss compared to the SiC MOSFET module, and it worsens with the increased junction temperature. Besides, the tail current of FS75R12KT4_B15 increases with temperature, thereby increasing the turn-off switching energy loss. It is observed in Table VIII that with a higher load current, both rise and fall times decrease during the turn-off process and increase during the turn-on process. This is the reason why Eoff increases less with the load current than Eon.

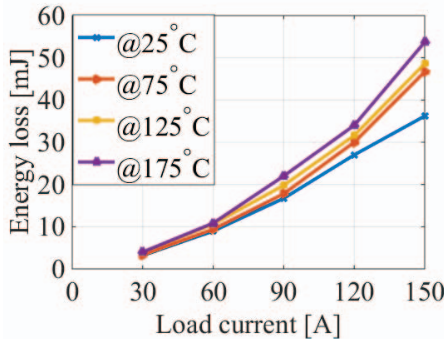

Fig. 11: Turn-on loss of FS75R12KT4_B15 at 600 V

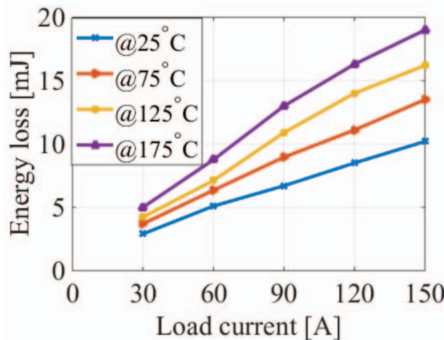

Fig. 12: Turn-off loss of FS75R12KT4_B15 at 600 V

TABLE IX: Improvement factor of switching energy loss in CCS050M12CM2 compared to FS75R12KT4_B15

Temperature	Improvement Factor		
(°C)	E_{on}	E_{off}	E_{total}
25	4.3	3.9	4.2
175	7.8	5.4	7

Table IX shows the factor of improvement of switching energy losses for the SiC MOSFET module compared to the Si IGBT module at 600 V dc link and 150 A load current. The improvement factor refers to a reduction of the energy loss in the SiC MOSFET module by the factor given. At 25 °C, the turn-on, the turn-off and the total switching energy losses are improved by a factor of 4.3, 3.9 and 4.2, respectively. These improvements are mainly due to three reasons; a small reverse recovery charge in SiC SBD compared to Si diode (as shown in Table II), fast switching speed, and the absence of tail current during the turn-off in CCS050M12CM2. The factors of improvement are more pronounced at higher junction temperature as is evident from Table IX.

VI. Conclusion

This paper has presented a comparison between the six-pack modules CCS050M12CM2 and FS75R12KT4_B15 in terms of efficiency. Various issues such as current and voltage gradients, switching speed, and oscillations in the current and voltage waveforms have been discussed. The results from the laboratory measurements show that CCS050M12CM2 switches faster and has lower switching energy loss compared to FS75R12KT4_B15. Moreover, the total switching energy loss of CCS050M12CM2 is nearly constant for different temperatures, whereas for FS75R12KT4_B15, the total switching energy loss increases by a factor of 1.6 when the junction temperature is increased from 25 °C to 175 °C. Thus, CCS050M12CM2 could replace FS75R12KT4_B15 for high temperature applications.

However, the package inductance of CCS050M12CM2 is 1.6 times higher compared to FS75R12KT4_B15, and should be reduced, such that the full potential of the fast switching device can be utilized in applications.

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