

Modeling a Two Stage SAR-Assisted Pipeline ADC

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Master of Science in Electronics Submission date: August 2016 Supervisor: Trond Ytterdal, IET

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Summary

In this work, the 15-bit SAR-assisted pipeline ADC has been examined, and high-level models have been made in Cadence to verify its operation. The goal is to achieve a resolution of more than 14 ENOB at a sampling frequency of 32 MHz. Specifications for the various sub-blocks have been derived based on general circuit design theory and previous work in the field, and the models have been implemented accordingly. Using an amplifier gain of 84.34 dB, the model achieves an ENOB of 14.43 with input frequencies 218.75 Hz and 15MHz, using a sample frequency of 32 MHz.

Samandrag

Denne oppgva tek fre seg ein 15-bit, to stegs pipeline ADC med underomformarar av typen SAR. Hgnivmodellar er laga i Cadence for verifisere arkitekturen. Mlet er oppn ei opplysing p over 14 ENOB med samplingsfrekvens p 32 MHz. For oppn dette har dei ndvendige spesifikasjonene vorte utleia for delblokkene i systemet, basert p generell teori og tidligare arbeid innanfor feltet. Med ei forsterkning p 84.34 dB mellom stega, oppnr modellen ENOB p 14.43 for inngongsfrekvensar p 218.75 Hz og 15 MHz, med ein samplingsfrekvens p 32 MHz.

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Abbreviations

ADC	=	Analog-to-Digital Converter
DAC	=	Digital-to-Analog Converter
CDAC	=	Capacitative Digital-to-Analog Converter
LSB	=	Least Significant Bit
MSB	=	Most Significant Bit
SAR	=	Successive approximation register
IC	=	Integrated circuits
SC	=	Switched capacitor
SNR	=	Signal-to-Noise Ratio
SNDR	=	Signal-to-Noise-and-Distortion Ratio
DNL	=	Differential Non-Linearity
FFT	=	Fast-Fourier Transform

Introduction

One of the most important aspects of modern electronic devices is energy efficiency. The market for small battery driven devices increases rapidly, and energy efficiency is likely to continue being important in the future. Modern electronic systems rely heavily on digital circuits for computation and processing information, as it is usually faster and more energy efficient than analog signal processing. However, most systems also use analog signals to communicate with the outside world, which is inherently analog. Examples of such signals are sensor data and wireless communication. This means that an ADC is needed to translate signals from the analog to the digital domain for further processing. In order to achieve low energy operation of a modern electronic system, it is also essential to consider the consumption of the analog parts present in the system. The ADC usually plays a significant role, and energy efficient operation of ADCs is an important topic. Various implementations of the ADC exists, with wide variations in operating speed and resolution, across multiple architectures.

Many studies have been done on energy efficient operation af ADCs, including [10, 9, 12]. These studies show that in higher resolution ADCs, which is the main topic for this project, SNR is limited by thermal noise. In order to add one more bit of resolution, the noise power needs to be decreased by a factor of four [10]. Halving the thermal noise power usually requires doubling the power consumption, and adding an extra bit of resolution in this group requires quadrupling the energy consumption.

A common way to quantify the performance of ADCs across a wide range of operating speeds, resolutions and architectures is to use a figure-of-merit (FoM). The following is the Walden FoM, which combines the resolution (ENOB), power consumption (P) and operating frequency (f_s) to a single figure, and is commonly used to assess the quality of an ADC. The unit is usually given as fJ/conv-step, and a low number is desirable.

$$FoM = \frac{P}{f_s \times 2^{ENOB}} \tag{1.1}$$

As shown in equation 1.1, adding one bit of resolution allows doubling the power while keeping the FoM unchanged. This means adding one bit of resolution is only a "fair trade" in the first group of converters where power and resolution trade equally. In the second group of thermal noise limited ADCs simply adding one bit would more than double the power consumption, and deteriorate the FoM. This means additional techniquies are required to achieve competitive high resolution converters.

One way to improve the resolution of ADCs in the thermal noise limited regime is to include digital error correction circuitry. Allowing analog errors lets the analog part of the circuit to be less precise, and thus consume less power. This approach utilizes the fact that modern IC processes are capable of creating energy efficient digital circuits, and further advances in the technology will likely lead to even smaller and more efficient digital correction modules. Using digital logic to alleviate the demands on analog components is mentioned in i.e. [9] as a promising method of creating power efficient high-resolution ADCs in the future.

The pipeline ADC is an example of exploiting digital error correction to relax the requirement of its steps. The total number of bits generated by the sub ADCs is usually a little bit more than the total resolution for the ADC, and the redundant bit(s) can be used as part of the digital error correction. By dividing the conversion into smaller steps of lower resolution the problem of converting a signal is divided into smaller, more manageable parts executed in parallel. This division relaxes the requirements of the later stages. In general, parallelisation can often lead to lower power consumption than would be necessary in a linear system [11].

The successive approximation-type (SAR) ADCs seem to currently be the most energy efficient implementations of low to medium converters [8]. SAR ADCs consist of relatively simple analog blocks (a capacitative DAC and a comparator) with corresponding digital control logic. This lack of power hungry analog blocks often found in other architectures (i.e. the multiple comparators in the flash ADC) leads to low power consumption when the resolution is low. As the resolution increases, however, component mismatch and other non-linear effects play an increasing role, and power consumption increases rapidly for higher resolution implementations.

Recently, different techniques to exploit the simplistic operation of the SAR ADC in higher resolution ADCs have been explored. An example of this is the noise shaping SAR, which utilizes oversampling and noise shaping achieve higher SNR. The idea behing noise shaping is to move large parts of the noise generated in the system out of the frequency band of the signal. This approach is studied in i.e. [3]. Another popular approach is the SAR pipeline ADC, which uses low to medium resolution SAR ADCs as sub ADCs. This approach seeks to keep energy consumption down by relaxing the requirements of the different analog sub-circuits. A study on the SAR pipeline ADC can be found in [2]. The subject of this thesis will be the SAR pipeline ADC, and it will be discussed in more detail in the chapters to come.

1.1 Goal

Leading up to this work, a SAR pipeline ADC was modeled in MATLAB as part of a specialization project [5]. The goal of the specialization thesis was to gain an understanding of the operation of the SAR-assisted pipeline ADC, and study how the resolution of the sub-ADCs affect the power consumption in a 15b ADC consisting of a two stage pipeline. The aim of this work is to go into deeper detail on the requirements for the different parts of the system, and make a more realistic model for the SAR pipeline ADC. In this project Cadence will be used as the main tool for modeling and simulation.

The target is to model an ADC with a total resolution of 15 bits using two SAR sub ADCs. Building on the conclusions from the previous project, the two sub ADCs will be of similar resolution, 8 bits each. This implies one bit of stage redundancy which serves to alleviate the accuracy requirements of the interstage amplifier. A digital error correction module resolves the two 8 bit results to the final 15 bit output code. ENOB should be as close to 15 bit as possible.

1.2 Outline

The rest of the thesis is structured as outlined below:

- 1. Chapter 2: Background theory A brief introduction to the basic knowledge needed to read this report.
- 2. Chapter 3: Design An overview of the general architecture studied in this work
- 3. Chapter 4: Specifications and implementation Mathematical specification for the subcircuits, and a description of their implementation in the model when suitable.
- 4. Chapter 5: Results Simulation results.
- 5. Chapter 6: Discussion A discussion of the chosen architecture and other available options.
- 6. Chapter 7: Conclusion Concluding remarks and future direction.

1.3 Own contributions

In this work an architecture for a SAR assisted pipeline ADC is investigated, and specifications for its sub blocks are derived. To verify the architecture, high level models have been developed in Cadence, using Verilog A and ideal circuit elements. Testbenches have been developed to verify the operation of key sub-blocks, like the amplifier, and simulations have been run on the entire system to verify that the desired resolution is achieved.

Background Theory

This chapter will introduce some essential background theory on which the reasoning in the rest of the report is based. The contents of this chapter is assumed known to most readers, and is presented briefly as a reminder. More detailed explanations can be found in i.e. [1]. The background theory chapter from the work preceeding this project, found in [5], touches on some topics in greater detail. Unless otherwise specified, the following content are sourced from these reference materials or assumed to be general knowledge, and will not be specifically referenced in the text.

2.1 SAR ADC

The SAR ADC computes the digital code one bit at a time by comparing the input signal with a fraction of the reference voltage. This operation is usually performed by sampling the input signal on an array of capacitors, subtract the desired fraction of the reference voltage from the array by switching some capacitors to ground and comparing the remaining voltage using a comparator. After the specified number of bits have been converted, a voltage equal to $V_{DIG} - V_{IN}$ remains as stored charge on the capacitor array¹.

A considerable portion of the consumed energy in the SAR ADC is a result of capacitor switching during the bit cycling phase, or binary search. This energy is proportional to the capacitor size, and it is therefore desirable to use as small capacitors as possible. The common limiting factors for capacitor sizes are process limits or thermal noise power.

2.2 Pipeline ADC

The pipeline ADC divides the conversion process into several stages, each resolving only part of the total resolution. Each stage will convert a predetermined number of bits, and the

¹If the LSB capacitor is also switched back in the case of a converted one, which is unnecessary in the case of a single SAR ADC

remainder is sent to the following stage. The remainder is the part of the signal that is not fully quantized by the current stage, also known as the *quantization error*. The following stages will quantize the quantization error, and its magnitude will decrease for each stage. The remainder, or error signal, can be defined as

$$V_{REM} = V_{IN} - V_{DIG} \tag{2.1}$$

where V_{DIG} is the analog equivalent of the code produced in the preceeding stages of the pipeline. The remainder will have an amplitude limited by V_{LSB} . In order to convert this using the same reference voltage in the following stages, the residue is scaled to fit the original voltage swing. This involves amplification by 2^M , where M is the number of bits resolved in the current stage. Once all the stages have finished their conversions, the codes are bit-aligned and combined to form the final code.

2.2.1 Non-ideal effects

The pipeline ADC is vulnerable to non-linearities due to mismatch between the stages. An important source of nonlinearity is errors in the interstage gain element. If the interstage gain is different from its intended value, the later stages will convert signals that are slightly different from their intended value; the quantiziation error-multiplied by 2^M . This is problematic, because when the signals are aligned in the end, a gain of 2^M is assumed in the digital circuit, and the result will be non-linearities in the output waveforms. Non-linearity appears as distortion in the spectrum of the converted signal, and reduces the SNDR of the converter, leading to lower effective resolution. Thus it is important to use interstage gain elements with sufficiently accurate gain in high-accuracy converters.

Redundant bits are often used in pipeline converters to relax the requirements for the subconverters. With redundancy, some bits are effectively being converted by both converters across a stage boundary. To implement this, the interstage gain is halved, and the most significant code is left shifted by only its exclusive bits, i.e. its resolution minus the redundant bits. The digital alignment and error correction block then adds the resulting codes, with the redundant bits overlapping, to create the final code.

Mismatch in the sub-converters themselves, like comparator offset or ADC gain errors, can often be avoided by using redundant bits. Such errors are not discussed further in this work.

2.2.2 Digital alignment and error correction

The results from the different stages are stored and aligned in a digital module, hereafter called the digital alignment and error correction block. In this block redundant bits are combined to achieve higher tolerance for mismatch between stages. This is achieved by overlapping the codes from different stages by a number of bits equal to the desired redundancy, and add them together. Figure 2.1 shows an example adding two four bit codes with a single bit of redundancy. A more detailed description is provided in [1].

Figure 2.1: Generating a 7 bit code from two 4 bit codes

2.2.3 SAR-assisted pipeline ADC

A SAR-assisted pipeline ADC is a pipeline converter which uses SAR ADCs as sub converters. This approach allows larger stage resolutions than i.e. the flash architecture while keeping the power consumption down. A dedicated analysis of the power consumption of the SAR assisted pipeline ADC is performed in [2]. The study done in [5] suggests that it is beneficial to use converters of similar resolution in a two stage SAR-assisted pipeline ADC.

Another benefit of using SAR ADCs in the sub stages is that the residue voltage is readily available after the end of the conversion, and it is not necessary to add an additional DAC for this purpose.

2.3 Feedback Amplifiers

The practise of using amplifiers in a feedback loop is well known in the analog design community, and will not be discussed in detail here. Only some key points and MATHE-MATICAL EXPRESSIONS are mentioned here for use in the following chapters. A more detailed explanation is given in e.g. [1]. The symbols used in this chapter will be reused later.

A feedback amplifier is defined by its feedback factor, β and amplifier gain A. In the ideal case of infinite amplifier gain, $A \to \infty$, the closed loop gain $A_{CL} = \frac{1}{\beta}$. However, in more realistic applications, the amplifier has finite gain, which introduces a gain error in the closed-loop gain. In the general case, the closed-loop gain can be found to be

$$A_{CL} = \frac{1}{\beta} \cdot \frac{A\beta}{1 + A\beta} \tag{2.2}$$

The magnitude of the error decreases as A increases, so for an accurate feedback amplifier, an amplifier with high gain is requred.

The bandwidth of the feedback amplifier is larger than the bandwidth of the amplifier used; ω_{-3dB} of the feedback amplifier is increased by a factor of $(1 + A\beta)$. Figure 2.2



Figure 2.2: The SC amplifier feedback network

shows a feedback amplifier implemented in a switched-capacitor circuit. This amplifier operates in two phases; the sample phase and the amplification phase. During the sample phase the input voltage is sampled on the sampling capacitor, C_S , and the charge is transferred across to the load capacitance in the amplification phase with a voltage gain of $-\frac{C_S}{C_2}$. The feedback factor of this circuit is

$$\beta = -\frac{C_2}{C_S} \tag{2.3}$$

2.4 Thermal noise

The quantization process performed by the ADC introduces noise, named quantization noise. The size of this noise determines the theoretically achievable signal-to-quantization-noise-ratio, SQNR, and is determined by the number of quantization steps.

Another important noise source is thermal noise in the sampling capacitors. If this noise is larger than the quantization noise, the effective resolution of the ADC is decreased. Thus, in order for thermal noise not to negatively affect the performance of the ADC, the thermal noise power must be smaller than the quantization noise power. Using this, it is possible to derive the minimum size of the sampling capacitors given the desired resolution of the converter, as shown in equation (2.4)

$$C_S \ge \frac{12kT}{V_{LSB}^2} = 12kT\frac{2^{2N}}{V_{FS}^2}$$
(2.4)

2.5 Evaluating the ADC performance

A key metric in evaluating an ADC is the effective resolution, given in terms of effectivenumber-of-bits (ENOB) or signal-to-noise-and-distortion-ratio (SNDR). This can be easily found using an FFT analysis. A technique known as coherent sampling is used to place all the signal power within a single bin in the FFT. This involves choosing an input frequency, f_in , sample frequency, f_s , number of samples, $N_{samples}$ and number of cycles, M_{cycles} to satisfy the relation

$$\frac{f_{in}}{f_s} = \frac{M_{cycles}}{N_{samples}} \tag{2.5}$$

Architecture

The ADC modeled in this project is a two-stage SAR-assisted pipeline ADC. Both stages consist of an 8 bit SAR ADC, the outputs of which is aligned and added in a digital error correction block. One bit redundancy is used between the stages to allow some inaccuracies in the first stage. The sampling capacitance is divided into a small and a big DAC. The small DAC is used as apart of the first stage SAR ADC, while the big DAC is used for residue generation. The final output code is resolved to 15 bits in the digital alignment and error correction block. Figure 3.1 shows a block diagram of the ADC.



Figure 3.1: Pipeline ADC block diagram

3.1 First stage and residue generation

Before the first conversion, the input signal is sampled on an array of capacitors. The SAR ADC then performs a binary search for the digital code representing the input voltage, and the residue is left on the capacitor array after the conversion is finished. This means that the SAR ADC is able to perform both the conversion and residue generation at the same time. However, since the accuracy of the full pipeline is 15 bits, the input voltage needs to be sampled on a sufficiently large capacitor for the thermal noise power to be low enough to satisfy the accuracy requirement. The first stage ADC only needs a resolution of 8 bits, so using a large sampling capacitor would result in superfluous energy consumption in the first stage due to switching during the binary search phase¹. This is illustrated in figure 3.2.



Figure 3.2: Excessive switching during the binary search, from [7]

In order to address this issue, the sampling capacitor array is divided into two parts, labeled small DAC and big DAC in figure 3.1. The capacitance of the small DAC satisfies the thermal noise requrements for 8 bits, and is used by the first stage SAR ADC for performing the binary search. After the 8 bit conversion is done, the code is given to the big DAC in order to generate the residue voltage. This approach conserves switching power in the first stage, while providing sufficient sampling accuracy for the following stage. One redundant bit is used to allow a certain degree of inaccuracy between the two stages, which is handled by the digital alignment and error correction block. The approach of using only a part of the capacitor array for searching is also used in i.e [7].

¹This switching is required to perform the search, but wasteful in simple residue generation

3.2 Amplifier

The first stage converts 8 bits with one bit redundancy, this means that the interstage amplifier needs to provide a gain of $A = 2^{8-1} = 128$. This is achieved using a high gain amplifier in a switched capacitor feedback network, as shown in figure 3.3. The actual implementation will be fully differential. The network needs a feedback factor of $\beta = -\frac{1}{128}$, which is obtained by setting the size of C_2 to be equal to $\frac{1}{128}C_S$.



Figure 3.3: The SC amplifier feedback network, repeated from chapter 2 for reference.

3.3 Second stage

The sampling capacitor of the second stage ADC is shown as C_L in figure 3.3. The amplified residue will be sampled during the amplification phase of the amplifier, and once the amplify clock goes low, the ADC will start its conversion. When eight bits have been resolved in the second stage, the code is sent to the digital alignment and correction block, and the final 15 bit code is computed.

3.4 Digital alignment and correction

This digital block serves the purpose of storing and aligning the results from the two stages, as well as perform simple error correction as described in the previous chapter. Since the two sub ADCs work on different samples and finish their conversion at different times, this unit needs to store the code from the first stage until the code from the corresponding sample is finished in the second stage. It will then align and add the 8-bit codes to produce the final 15 bit output, and the conversion is complete.

3.5 Timing diagram

Figure 3.4 outlines the operations of the different sub-blocks during a single clock period. The two ADC stages will be working on different samples.

1 st stage	tracking	conversion		residue transfer
Residue Amplifier	auto-zero	off		residue amplification
2 nd stage	conversio	on	reset	tracking

Figure 3.4: The timing of the various sub-blocks (from [7])

In the beginning of the clock period, the input signal is sampled by the first stage small and big DAC capacitor arrays. At the same time, the amplifier has time to reset. The second stage ADC will have already completed its sampling procedure, and start converting the last 8 bits of the *previous* sample. After the sampling is done in the first stage, the voltage is converted and the residue signal generated. During this time slot, the amplifier is not in use, and may be switched off to conserve power. The second stage ADC will transmit the final 8-bit result when finished, and reset. At this point the digital alignment and error correction block will have the result from both stages, and combine the two codes to make the final 15 bit code of the previous sample. In the final half of the clock period, the residue from the first stage is amplified and sampled on the sampling capacitor for the second stage ADC. The current sample will then be converted by the second stage ADC in the following clock cycle.

Model Implementation and Specification

This chapter will explain in more detail the implementation of the models for the various sub-blocks, and derive the specifications necessary to achieve the desired resolution of more than 14 ENOB. All the models are made using the Cadence Design Suite. The overall specification for the entire ADC is repeated here for reference.

4.1 Interstage amplifier model

The amplifier model is built out of ideal circuit elements in Cadence. The input stage is a voltage controlled voltage source (VCVS) converting the differential input voltages to a single-ended signal, with unity gain. This source also serves to give the amplifier infinite imput impedance. Following the input stage, a series resistor and parallel capacitor create a pole in the transfer function. The gain is provided by a second VCVS. Finally the amplified signal is converted to a differential signal using an ideal balun. Since the balun supplies the same common mode voltage as the input signal, no common mode feedback is required. The schematic of the amplifier model is shown in figure 4.1.



Figure 4.1: Ideal opamp model used for verification

This amplifier is put into a feedback network as shown in figure 3.3 to realize the desired

closed loop gain of 128. The capacitors labeled C_L in this model serve the purpose of sampling capacitors for the second stage ADC. The size of the capacitors is decided by the thermal noise limit for 8 bit accuracy, however, the minimum size is allowed for thermal noise is smaller than the minimum size allowed by the capacitor model in Cadence, so the capacitor value was chosen to be 38.11fF. The two phases used, denoted as ϕ_S and ϕ_A , are the same clock signals used by the two sub ADCs. ϕ_S is used as the sampling clock by the first stage, and ϕ_A is used as the sampling clock for the second stage. These clock signals are non-overlapping. There is also a third clock signal, ϕ_{S_ad} , which is used to prevent charge injection errors in the amplifier. As shown in the clock diagram, figure 4.2, there is an open period of time where both clock signals are low. This period is allocated for the first stage ADC to finish its conversion in the case of a real circuit implementation or transistor level models.

4.1.1 Specification

Gain errors due to finite gain contributes to mismatch between the stages, and give rise to nonlinearities in the final code. Nonlinearity in an ADC can be expressed in terms of deviation from the ideal values by a metric called differential non-linearity (DNL). The effect of finite gain is related to the maximum DNL of the ADC as follows [6]

$$|DNL|_{MAX} \propto \frac{2^{N-M}}{A\beta} \tag{4.1}$$

N is the total resolution, and M is the resolution of the stages to be converted after the amplifier. According to this equation, the amplifier gain A must be at least 2^{14} , or 84,29 dB, to keep the maximum DNL from deteriorating when N = 15 and M = 8.

In order to accomodate the 32 MS/s sampling frequency, the feedback amplifier needs an half-gain frequency, f_{-3dB} , of 16 MHz. This corresponds to a bandwidth of 127 kHz in the amplifier, in accordance with the equations from chapter 2.

4.2 ADC and CDAC models

A functional model for the SAR ADC has been implemented in Verilog A for use in the overall pipeline ADC design, which is modified from a model provided by [13]. The models used for the two stages are almost the identical, with the exception of small differences in the timing to accomodate the interaction between the big CDAC, ADC and amplifier in the first stage during the sample phase. In the first stage, the sampling and conversion is done the instant the sampling clock goes high, so the sampling capacitors, which are located after the residue generation in this model, can use the entire sample-phase to sample the residue signal. The second stage ADC uses the amplify phase for the inter stage amplifier as its sample clock, records the input signal at the falling edge, to give the amplifier plenty of time to reach its steady state. In a more realistic system, the sampling would be complete before the conversion, and the two models could be more similar. The ADCs also provide control signals to noitfy the other blocks of a completed conversion. Both ADC models are provided in the appendix for reference.

The big DAC used for residue generation is also modeled in Verilog A. This block will sample the input signal at the same time as the first stage ADC. Once the ADC is finished quantizing the signal, the residue generation process is started by means of a control signal. The 8 bit code generated by the ADC is converted into its analog representation and subtracted from the preivously recorded input sample to create the residue¹. The CDAC model is supplied in the appendix for reference.

4.3 Digital alignment and error correction

The digital alignment and error correction block is a purely digital block, and is implemented in Verilog A. When notified of a completed conversion, the digital alignment and correction block records and stores the 8 bit code word from the corresponding ADC. In the model, the codes are stored in the form of an integer number representation of the digital code. When the code from the second stage is received, the codes from the two stages are bit-aligned and combined as explained in chapter 2; the MSB code is left shifted 7 bits before being added with to the second stage code. This left shift is done by multiplying the integer representating the code by $2^7 = 128$. The final 15 bit code is provided at the output terminal of the alignment and error correction block in the form of an integer representation of the 15 bit code.

4.4 Top-level module

The top-level model consists of two SAR-ADC-blocks, a CDAC for residue generation, a interstage amplifier, a digital alignment and error correction block along with pulse sources to supply the various clock signals.

4.4.1 Sampling and First Stage

The input voltage is sampled by the first stage ADC and CDAC at the same time. Both these blocks are Verilog A-models, and do not use capacitors to sample the input voltage. The sampling capacitor is placed in the interstage amplifier, and samples the residue signals from the CDAC during the sample phase. In order to accomodate this, the ADC and CDAC models make their outputs available immediately after sampling. This is different from how a real circuit would be implemented, as the input voltage would be sampled by the sampling capacitor, and the CDAC would generate the residue signal from the ADC output code.

4.4.2 Amplification phase

During the amplification phase, the second stage sampling capacitors are charged by the amplifier, and the second stage ADC is tracking its voltage. The second stage ADC records

¹In a real circuit, the quantized voltage would be subtracted from the input sample, and the positive side array would contain the negative side residue for the remaining stages, and vice-versa, as outlined in chapter 2

its input voltage at the end of the amplification phase, and start its conversion once \hat{I}_{QA} goes low.

4.4.3 Second stage and final code

Once the second conversion is finished, signalled by a control signal from the second stage ADC to the digital alignment and error correction block, the final code is computed and made available on the output side.

4.5 Clock generation

The clock generation is done by pulse sources set to use the same frequency, but different time offsets and pulse widths to create clock signals corresponding to the timing diagram presented in figure 4.2 from the previous chapter.



Figure 4.2: Clock signals used to control the ADC

Simulations and Results

The goal of the simulations in this work is to verify the architecture and the derived specification for the sub-circuits of the pipeline as they are integrated into a larger system. Since the models have been made to achieve a given resolution, the only metric that is derived from the simulations is the effective resolution achieved by the converter, expressed in terms of SNDR and ENOB. As this is not a transistor-level model, power consumption is not simulated, but is discussed in the next chapter.

5.1 Amplifier

The feedback amplifier is simulated in order to verify its open-loop gain and unity gain frequency. The testbench consists of the amplifier model in a feedback configuration as shown in figure 3.3 providing a closed-loop gain of about 128. A fully differential sinusoid input signal with an amplitude of 4mV applied as an input. The amplitude of 4mV is similar to the amplitude of the residue signal from the first stage of the pipeline ADC.

An STB-analysis is run to get more information on the loop gain over a range of frequencies. This analysis evaluates the open-loop properties of the system, by breaking the loop and sweeping over a range of frequencies at a specific operating point. The loop is broken by placing a probe, named CMDMPROBE from the Cadence analogLib, between the output terminals of the amplifier and the feedback capacitors. The operating point is chosen to be a point close to the end of the amplification phase, and the frequency sweep is done over a range running from 0 to 10 GHz.

5.1.1 Simulation results

In order to accomodate the desired sampling rate of 32 MS/s, f_{-3dB} for the feedback amplifier should be higher than 16 MHz. The -3dB-bandwidth of the feedback amplifier is found to be 17 MHz in the simulations, which is sufficient.

5.2 Top level testbench

The ADC is simulated with a fully differential input sinusoid signal, ranging from 0V to 1V with a common mode of $V_{DD}/2 = 0.5V$. The full swing of the input is therefore -1V to 1V. The output is a decimal representation of the 15 bit code representing the input. The output will be a "staircase" representation of the input sinusoid signal. This signal can be processed by an FFT analysis to find the effective resolution of the converter, in terms of SNDR or ENOB. In addition to the input signal, the supply voltage V_{DD} , the reference voltage, V_{REF} , and the clock signals are all generated by ideal sources in the testbench. The sample frequency is set to 32 MHz. The testbench schematic is provided in the appendix. The frequency of the input signal is set according to the requirements for coherent sampling, with $N_{samples} = 1024$, $M_{cycles} = 7$, which computes to $f_{in} = 218.75Hz$, according to equation (2.5). A high frequency signal is also tested. This signal uses 2048 samples and 560 cycles, which corresponds to an input frequency of 15 MHz.

5.2.1 Results

A transient analysis with a stop time of $33\mu s$ is run to obtain a time domain waveform from the ADC. $33\mu s$ is sufficient time to cover the specified number of samples, 1024, at the sample frequency, 32 MHz.

An FFT analysis is performed on the simulated waveform. The FFT is run with a rectangular window and 1024 samples. Figure 5.1 shows the FFT of the simulated waveform. The SNDR is derived from the similated spectrum, and is found to be 88.66 dB. This corresponds to an ENOB of 14.43. Similar results are found for the high frequency input signal of 15 MHz.

The SNR is the same as the SNDR, which indicates that there is no distortion effects in the simulated circuit.



Figure 5.1: FFT

Discussion

In this chapter the chosen solution is discussed. Suggestions are also made for circuit implementations of the system. Finally the validity of the models and simulation results is discussed.

6.1 Sub ADC resolutions

A power analysis for SAR assisted pipeline ADCs [2] has found that a large first stage resolution is theoretically beneficial for two stage SAR assisted pipeline ADCs. Three topologies were simulated with different stage resolutions, 4-12, 7-9 and 11-5. It was found that the 7-9 was the most energy efficient. The conclusion of [5] was that using stages of similar resolution seems to be the most energy efficient. Based on these observations, the decision of using two equal stages of 8 bits was made. The two main reasons an 8-8 topology was chosen over a 7-9 topology was that [5] found that equal stages are more efficient, and that a larger first stage implies the need for a larger interstage gain. This would mean using a very small feedback factor, which could lead to problems with regard to bandwidth and stability. It is also worth mentioning that a very low FoM two stage SAR assisted pipeline ADC was implemented in [7], which uses a first stage with 6 bits resolution and a second stage with 8 bits. One merit of using a smaller first stage is the lower interstage gain, which allows a more lenient feedback factor in feedback amplifier topologies. This is something to look into if the proves difficult to implement the $\frac{1}{128}$ feedback factor with sufficient gain and bandwidth.

6.2 Possible amplifier topologies

A high gain amplifier tends to consume a lot of power, and constitutes a large part of the energy budget for the ADC. Implementing an energy-efficient amplifier is thus essential to achieve overall energy-efficient operation. In this ADC, an amplifier with very high gain is required to achieve the desired accuracy, which will further increase power consumption.

Recently, the ring amplifier architecture has been studied and shows promise as a high gain, low power amplifier topology for integrated circuit applications. It has been used in high achieving pipeline ADC implementations in i.e. [7, 4]. It is suggested in [4] that it should be possible to achieve an open-loop gain of at least 90 dB¹.

Another option, which is used in a simulated ADC in [2] is to implement a normal opamp with gain boosting to achieve the required gain. This might end up consuming more power, and seems to be a less promising approach than the ring amplifier.

6.3 Evaluation of the model

This work consists of very ideal models, used to verify the architecture and derived specifications. This introduces potentially large margins of error in the findings. All the models used in this work are high level models, which have quite close to ideal behaviour. This is likely to be a source of inaccuracy in the conclusions drawn from this work. In this section some significant issues are discussed.

6.3.1 ADC and DAC models

The SAR ADC and CDAC models are implemented in Verilog A, and lack the non-ideal effects which are associated with real circuit implementations of these modules, i.e. device mismatch and process variations. These non-ideal effects give rise to non-linearities in the output waveform, which create distortion in the FFT. Since the simulations run in this work does not include these effects, it is safe to assume that the SNDR achieved from a more realistic model would be lower than indicated in this report. The simulation results show that SNR and SNDR are the same, which implies that no distortion is present in the spectrum. This means that the results found here are not very accurate in the context of determining the final accuracy, as possibly large margins of error exist. The simulated result was an ENOB of 14.43, which means there is a some margin. This margin can be increased further by increasing the gain of the amplifier, which might be possible even in a real circuit implementation. It is therefore not unlikely that the system modeled in this work could be implemented using real circuit blocks.

6.3.2 Sampling

Another weakness is the sampling operation. In this work the input voltage is sampled by Verilog A-models, and is therefore very ideal. In a real circuit implementation, the sampling would have to be done using non-ideal switches and capacitors, which introduces additional errors. Especially the switches are problematic, as they would have to provide the same resistance over large amplitude variations in order to not experience signal-dependent errors. This could be achieved using bootstrapped switches, the effects of which are not included in the simulations run in this work, and is liable to introduce further decrease of the SNDR, and consequently the effective resolution.

¹The amplifier implemented in [4] uses a larger feedback factor

The interstage amplifier model also uses ideal switches, but the voltage swing is smaller here, and it is conceivable that transmission gates are sufficient.

6.3.3 Digital circuits

The digital alignment and error correction module is also implemented in Verilog A, but is not as likely to be a source of error. Since this is a simple digital circuit, its actual operation is assumed to be similar to the model, provided that the timing of its input signals are correct.

Conclusion

In this project, a 15-bit two stage SAR-assisted pipeline ADC has been modeled using high-level blocks. Specificications have been derived for the various sub-blocks to achieve a final resolution of more than 14 ENOB. Simulations have been run on a low-frequency signal using a sampling frequency of 32 MHz. The ADC consists of two 8-bit SAR ADCs and a feedback amplifier to act as the interstage gain. An amplifier model with a gain of 84 dB has been implemented in the system. Simulations show that this system achieves an ENOB of 14.43, which satisfies the goal.

There is, however, a large degree of uncertainty as to the validity of the results in the context of a real circuit implementation, as all the sub-blocks are high level models, with a high degree of ideality.

Looking at the specifications derived, it seems plausible that it is possible to implement the system in a real circuit. One promising suggestion is using a ring-amplifier topology in the interstage amplifier, as they have been found to provide more than sufficient gain, while keeping the power consumption down. Opting for a smaller first stage might also be a good choice, in order to achieve a more lenient feedback factor.

7.1 Future directions

The natural continuation of this work would be to create transistor level and layout models in order to run more realistic simulations. The model is made using different sub blocks, and increasingly realistic models can be created and inserted to the system one by one. This allows simple step by step transition from high level to low level, more realistic models. A lot of work has already been done in creating energy-efficient medium resolution SAR ADCs, so it seems natural to start by choosing an architecture and creating a realistic implementation for the amplifier, and verifying its performance in the pipeline. Accurate sampling is also an important issue that is not taken into account in the models presented in this report. The effects of using non-ideal switches may also affect the final performance.

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