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Low Power Electrophoretic Display Module

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Problem Description

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Assignment title: Low Power Electrophoretic Display Module

Assignment text: New types of displays allow for extremely small power dissipation as long as the image is static. These types are often referred to as "electronic paper displays". Such displays are interesting for IoT applications as they would allow display of images or messages when little power is available. The electrophoretic display technology is seen as one of the most promising technologies for IoT due to its low power consumption and flexibility. However, they do require a significant amount of current while updating the display. The challenges are mainly regarding driving and control of the display. Issues like long switching time, poor grayscale, flicker and ghosting effect in the display tends to increase the dynamic power consumption and required area for its driving circuitry.

The assignment consists of the following tasks:

- Study the electrophoretic display technology and identify common hardware components/sub-modules required to operate these displays.
- Find trade-offs and methods to minimize power consumption and size with respect to driving and control of the display.
- Develop detailed module requirement specification and block diagram for a given electrophoretic display.
- Design sub-modules in the display interface focusing on low power and miniaturization.
- If time, implement the sub-modules.

Co-supervisor: Øystein Moldsvor, Disruptive Technologies

Supervisor: Professor Per Gunnar Kjeldsberg, NTNU

Abstract

The electrophoretic display (EPD) technology has great potential for use in small sized, low power portable devices and Internet of Things (IoT) applications. Due to its capability of true *bistability* and *reflectivity*, it can show static images in ambient light without the need of any flowing current. The required power for image updates is found to be highly dependent on the image pattern and driving circuitry architecture. If the driving circuitry is designed specifically for low power consumption and occasional image update, small size EPDs can potentially be integrated in products that never before had the opportunity of an integrated display.

Based on a theoretical and practical analysis of the EPD and its driving circuitry, trade-offs and power-reduction techniques are highlighted in this thesis. The theoretical analysis is approached by dividing the driving circuitry into smaller sub-circuits or common building blocks. Each block is thereafter broken down and analyzed individually. A conceptual low power EPD module is then presented at higher abstraction levels. The practical experiments and analysis is based on a commercially available small size EPD. Different image updating techniques and driving pulse lengths are tested to find the optimal optical performance with minimum energy consumption.

High driving voltages in the range of $\pm 15V$ and updating times of several seconds is typically used for operation of EPDs. This is to achieve best possible optical performance and user experience. The high voltage sub-circuits is found to typically constitute for 90% of the total power consumption. By trading off fast response time and best optical performance with lower driving voltages, the total energy consumption is estimated to be reduced by more than one order of magnitude. Techniques such as unipolar driving waveforms and image updates in several stages at faster stage times can be used in combination. Theoretically, the driving voltages can be reduced to $\pm 2.5V$ with a total updating time in less than one second. This leads to a typical reduction of 20-40% in optical performance. By designing a single chip EPD module based on lower driving voltages, it is estimated that the driving circuitry can potentially have an average power consumption below 1mW. This is less than 5% of the total worst case power consumption compared to the commercially available hardware tested in this thesis.

Sammendrag

Elekroforetiske display (EPD) er en teknologi med stort potensiale for bruk i små, bærbare laveffekt-enheter og anvendelse til Tingenes Internett (IoT). På grunn av dens *bistabile* og *reflektive* egenskaper, kan statiske bilder vises i naturlig lys uten behov for tilført strøm. Effekten som kreves for å oppdatere bilder er sterkt avhengig av bildemønster samt driverkretsarkitektur. Dersom driverkretsen designes spesielt for lavt effektforbruk og sjelden bildeoppdatering, kan små EPD potensielt integreres i produkter som aldri tidligere har hatt mulighet for et integrert display.

Basert på teoretiske og praktiske analyser av EPD og tilhørende driverkrets, vil avveiinger og effektreduksjonsteknikker utheves i denne avhandlingen. Den teoretiske analysen er tilnærmet ved å dele driverkretsen inn i mindre delkretser eller felles byggeblokker. Hver blokk er deretter brutt ned og analysert individuelt. En konseptuell laveffekt EPD-modul er så presentert ved høyere abstraksjonsnivå. De praktiske eksperimentene og analysene er basert på en kommersielt tilgjengelig EPD i liten størrelse. Ulike bildeoppdateringsteknikker og lengder på driverpulsen er testet for å finne optimal optisk ytelse med minst mulig energiforbruk.

Høye driverspenninger i området rundt $\pm 15V$, samt oppdateringstider på flere sekunder, blir typisk benyttet for å operere EPD-teknologien. Dette er for å oppnå best mulig optisk ytelse og brukeropplevelse. Delkretsene i forbindelse med de høye driverspenningene står typisk for rundt 90% av det totale effektforbruket. Ved å bytte rask responstid og best mulig optisk ytelse mot lavere driverspenninger, er det totale energiforbruket estimert til å kunne reduseres med mer enn en størrelsesorden. Teknikker som enpolet bølgeform for driverspenningene og bildeoppdateringer i flere trinn ved raskere tider per trinn kan kombineres. Teoretisk sett så kan driverspenningene reduseres til $\pm 2.5V$ med en total oppdateringstid på under ett sekund. Dette medfører en typisk reduksjon med 20-40% i optisk ytelse. Ved å designe en EPD modul som en enkeltstående integrert krets basert på lavere spenninger, er det estimert at driverkretsen potensielt kan ha et gjennomsnittelig effektforbruk under 1mW. Dette tilsvarer mindre enn 5% av totalt effektforbruk sammenliknet med verste tilfelle i den kommersielt tilgjengelige maskinvaren som ble testet i denne avhandlingen.

Preface

The work in this thesis has been carried out during the spring 2016 at the Institute for Electronics and Telecommunications at NTNU, Trondheim. It is a continuation work from a literature study conducted in the fall 2015 at NTNU. Based on the study of several electronic paper display technologies, this thesis focuses on the driving electronics for one of the most promising display technologies for low power operation. The assignment was created in cooperation with Disruptive Technologies AS.

I will like to use this opportunity to thank my supervisors, Per Gunnar Kjeldsberg and Øystein Moldsvor, for exceptional guidance throughout this period. Through biweekly status meetings, it has been easy to keep a steady work progression with the thesis. I will also thank my fellow students for making the reading room into a joyful place with great work environment, deep discussions and lots of fun.

-Sigbjørn Gunnerød
Trondheim, 16.06.2016

Contents

List of Figures

List of Tables

Abbreviations

I^2C Inter-Integrated Circuit. 27

a-Si:H Hydrogenerated Amorphous Silicon. 18

AM Active Matrix. 16

CIE International Commission on Illumination. 7

COF Chip On Film. 19

COG Chip On Glass. 19

COP Chip On Plastic. 19

COTS Commercial Of The Shelf. 45

DAC Digital-to-Analog-Converter. 21

DIP Dual In-line Package. 62

DMA Direct Memory Access. 56

EPD Electrophoretic Display. 2

FPC Flexible Printed Circuit. 43

FRAM Ferroelectric Random Access Memory. 56

GPIO General Purpose In/Out. 44

HV High Voltage. 20

I/O In/Out. 43

IC Integrated Circuit. 19

IoT Internet of Things. 1

ITO Indium Tin Oxide. 16

LCD Liquid Crystal Display. 9

LDO Low Dropout. 23

MCU Microcontroller Unit. 26

MISO Master In Slave Out. 27

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 17

MOSI Master Out Slave In. 27

OLED Organic Light Emitting Display. 10

OTFT Organic Thin Film Transistor. 19

PARC Palo Alto Research Center. 7

PCB Printed Circuit board. 58

PDI Pervasive Displays Inc.. 42

PM Passive Matrix. 16

poly-Si Polycrystalline Silicon. 18

PWM Pulse Width Modulation. 44

RAM Random Access Memory. 29

RGB Red Green Blue. 22

RT Register Transfer. 35

SID Society for Information Displays. 39

SMPS Switch Mode Power Supply. 24

SPI Serial Peripheral Interface. 27

TFT Thin Film Transistor. 17

Chapter 1

Introduction

This chapter will give an introduction to the topic area for this thesis. An overall description of main problems related to today's display technologies will be presented. A motivation for the project is introduced to describe why the work is performed and how it can be useful for low power product developers. A few specific project goals are created to highlight what the thesis aim for. The chapter will also give an overview of how the thesis is organized and the main contributions from the work.

1.1 Motivation

Electronic displays are widely used in all kinds of systems today to visually show a graphical representation of certain information to the user. While the number of embedded systems and portable devices steadily increases every year, the overall product size tends to decrease. The exponential growth with transistor count in integrated circuits doubling every two years described in Moore's law, has led to more powerful devices in less required volume[1]. Along with the technology scaling and smarter applications, new challenges due to limited battery capacity and need for a better component integration appears. New devices related to Internet of Things (IoT) will allow for a direct integration of physical objects into computer-based systems. This opens up a wide range of opportunities for product development. Low power consumption and miniaturization are considered as some of the most important design criteria for achieving a successful IoT-integration.

The display is in general characterized as one of the most energy consuming components used in electronic devices[2]. The need for a high refresh rate and additional light sources in order to achieve a stable, viewable image on the screen, makes the average display very power hungry. A new type of electronic display, often referred to as "electronic paper display", is currently emerging. The electronic paper display offers a variety of advantages over traditional electronic displays. Two of the most interesting characteristics for this technology is the *reflective* and *bistable* behaviour. Ambient light is reflected in the display, much similar to paper and the bistability can offer image-stability without the need of a flowing current. These properties result in extremely little power consumption as long as the image is static. Electronic paper displays are therefore interesting for portable devices and IoT-applications to display images or text when little power is available. In products that only require occasional image update, the electronic paper display has potential for ultra low power consumption if required power in the driving circuitry is reduced to a minimum.

The Electrophoretic Display (EPD) technology is considered as one of the most popular examples within the electronic paper display category. It has the possibility to be made very small and flexible, in addition to having extremely low power consumption. The EPD is therefore very promising to use in small, battery powered devices designed to last longer than the average electronic device. In order to fully benefit from the EPD characteristics, the driving electronics needs to be optimized specifically for a given set of requirements. By analyzing the hardware components and sub-modules required to operate an EPD, trade-offs and design methodologies to minimize power consumption and size can be highlighted. Focusing on small size EPDs and ultra low power consumption opens up the possibility to use energy harvesting to power the device. It can also allow for a display to be implemented in products that never before had the opportunity of an integrated display.

1.2 Project goals

A typical solar panel can provide approximately 1mW of average power harvested from a $100mm^2$ photovoltaic cell[3]. In order to power a display module from such energy harvesting source, the power consumption should ideally be below 1mW. The display driving circuitry is seen as a major contributor to power consumption

for the EPD technology.

The overall project goal is to specify and design a complete display driver circuitry for a small sized electrophoretic display, optimized for low power consumption and miniaturization. The project can be divided into different stages:

- Research and define required hardware to drive and operate an electrophoretic display.
- Use information to make a functional block diagram. Investigate how the functional blocks can be implemented.
- Find trade-offs and specify methodologies to minimize power consumptions and circuit area (analog/digital hardware and software/firmware).
- Analyze the power consumption and highlight the sub-modules that consume the most power when driving an electrophoretic display.
- Design each sub-module/functional block with optimization techniques, one at a time.
- Implement these functional blocks.

1.3 Outline of this thesis

This thesis is organized into three main parts; Chapter 2-5 is based on research and describes background and theory related to the technical field of the thesis. Chapter 6 is an analytical chapter that will discuss design methodologies based on theory and practical tests/measurements in a commercially available small sized EPD module. Chapter 7-8 will introduce a conceptual EPD module design on system and architectural level based on results and findings in previous chapters. A discussion and conclusion is made to summarize the most important findings in the thesis as well as a describing proposed further work.

Chapter 2 will give an overview of the electrophoretic display technology. It will describe the working principles of the technology and basic background theory to understand how the display is constructed and operated. The main issues and challenges for the technology is also presented in this chapter.

Chapter 3 will give a brief presentation of required sub-modules for the display driving circuitry. With a basis in the more mature LCD driving circuitry, a comparison is drawn towards the EPD technology to find out what parts of the LCD circuit that can be reused and what parts that should specifically be adapted and optimized for the EPD technology.

Chapter 4 will show some general design methodologies and considerations related to low power chip design. A few well-proven techniques and trade-offs for reducing power consumption is introduced and a description of different abstraction levels show the significance of the power at each level.

Chapter 5 will present a few specific previous works that is used as a basis for the work performed in this thesis.

Chapter 6 is considered as the main chapter for this thesis. Based on hypotheses in conjunction with previous work, each sub-module in the EPD driving circuitry is broken down and analyzed to highlight how the total power consumption can be reduced. A commercially available EPD and driving circuitry is then tested with practical measurements. This will be used as a guidance for expected real life power consumption and to find techniques to reduce the overall power consumption. Optimization potential is discussed and a technical requirement specification is made for further design.

Chapter 7 will present a conceptual EPD module architectural design. The chapter is used to describe how the sub-modules can be implemented on a block level with a connection to show the working principle of a full system.

Chapter 8 will present concluding remarks for the work performed in this thesis. It will summarize the most important findings and give a brief proposal for further work.

1.4 Main contributions

- Focusing on small size displays, common hardware blocks for the EPD driving circuitry are identified and analyzed.
- A brief breakdown of expected/estimated power consumption for each hardware block is presented.

- Trade-offs and methods to minimize driving circuitry power consumption are highlighted and discussed.
- Physical tests in a commercially available EPD and driving circuitry are used to point at existing issues and potential improvements with respect to total energy consumption.
- A detailed EPD module requirement specification is made for a conceptual low power EPD module design based on excising solutions together with a theoretical analysis.
- A conceptual design of a full low power EPD module is presented on system and architectural level.

Chapter 2

The Electrophoretic Display

The electrophoretic display (EPD) is a technology primarily designed to mimic ordinary ink on paper. Like most technologies within the category of electronic paper displays, EPDs have advantages of good reflectivity, wide viewing angle, being thin and lightweight in addition to consume very little power[4]. The EPD can show messages or images in all lighting conditions as compared to traditional paper and provide good readability in direct sunlight. For this reason, the technology is most associated with e-paper or e-reader applications today.

Like other types of display technologies, EPDs come in varying sizes, resolution and image contrast. Since EPDs aim to reproduce the appearance of print-on-paper, the most common measure of EPD image quality is optical reflectance measured in lightness, L*. L* is a measurement component of International Commission on Illumination (CIE) 1976 (L*,a*,b*) color space[5]. The measurements closely match the human perception of lightness where the darkest black is L*=0 and the brightest white is L*=100[4]. As a comparison, traditional paper has a white state reflectance of around L*=90, while EPDs typically are in the range of L*=40-50. The brightest white state reflectance achieved in electronic paper displays is around L*=70[4].

2.1 Historical background

The first occurrence of an "electronic paper display" dates back to a patent made by Nick Sheridon at the Xerox's Palo Alto Research Center (PARC) in the early

1970s[6]. The technology was called Gyricon and it was based on the principle of rotating beads encapsulated in an oil-filled cavity.

In the late 1980s when the personal computer started to expand on the market, researchers began to realize the need for electronic paper (e-paper) due to higher paper consumption. The Gyricon technology was considered as a good candidate for e-paper. In 1997, E-ink Corporation was founded and they introduced the world's first active matrix EPD display in 2001, later named E-ink Vizplex[7]. The EPD technology can be considered as an upgraded version of Gyricon with much similar operating principle. In the early 2000s, the EPD technology started to show great progress and more developers got involved in the field of electronic paper displays. The EPD technology has now slowly begun to hit the market primarily through popular e-paper readers as Amazon Kindle, but also in forms of electronic shelf labels, wrist watches, mobile phones and more[8].

E-ink is considered as the leading EPD provider today, but companies like Plastic Logic and FlexEnable has also shown great potential by specializing on developing flexible EPDs based on organic electronics printed on a plastic substrate. These displays are extremely flexible, ultra-thin as well as shatterproof[9][10]. The form factor for these kinds of displays makes it a lot easier to implement in a wider range of applications such as wearables and other non-flat surfaces.

In the recent years a lot of optimizations has been made on the display technology, especially when it comes to reduced switching time and voltage. In 1998, the switching voltage of microencapsulated EPDs was around $300V$ with a response time of about 1 second[11]. By comparing it with today's EPD technology, the typical switching voltage is $15V$ with a response time of about $150ms$[11]. EPD cells with response time of $30ms$ at $15V$ has been reported[12]. Also, touch panel function and color imaging film can be integrated into the display[11]. This has lead to increased interest for the technology among product developers all over the world.

2.2 Operating principle

The Gyricon display is made up of a high concentration of hemispherical bichromal beads with two contrasting colors like black and white[13]. Each bead forms a pixel on the display controlled with a voltage applied to an electrode on at least one

side of the beads. The beads are charged so they exhibit an electrical dipole[14]. When an electrical current is applied to the electrode, the beads will rotate and face the surface according to the polarity of the voltage. If the white side of the bead is facing towards the surface, light is reflected. With the black side facing up, light is absorbed.

Electrophoretic displays (EPDs) are on the other hand based on a phenomenon called *electrophoresis*, which is movement of electrically charged molecules or particles under influence of an electric field[15]. Instead of bichromal beads used in the Gyricon technology, the electrophoretic technology utilize colored microparticles suspended in a clear fluid[16]. The majority of all EPDs today, use a two-particle dispersion, with black and white pigment particles in a microencapsulated and electrically insulating oil. The microcapsules are sandwiched between a single transparent top electrode and a pattern of line electrodes at the bottom plate as shown in Figure 2.1.

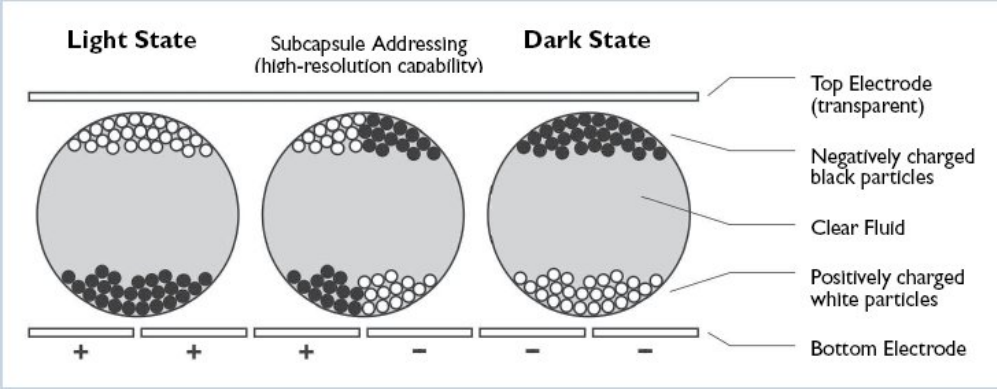


FIGURE 2.1: Basic construction of an electrophoretic display cell[17]

The dark pigment is normally a negatively charged carbon black material, while the white pigments are positively charged Titanium Dioxide (TiO_2) nanoparticles[18]. When a DC-voltage is applied over the two electrodes, the white and black particles are driven to opposite faces that forms the pixel on the display. By applying a positive voltage at the bottom plate, white particles are pushed towards the surface and ambient light is reflected. The more light shining on the display surface, the sharper the image contrast will be.

Figure 2.2 shows a comparison of the operating principles of gyricon and electrophoretic display technology.

A large benefit of the EPD technology is the zero field stability, also called *bistability* behaviour. This means that there is no significant change in the optical state

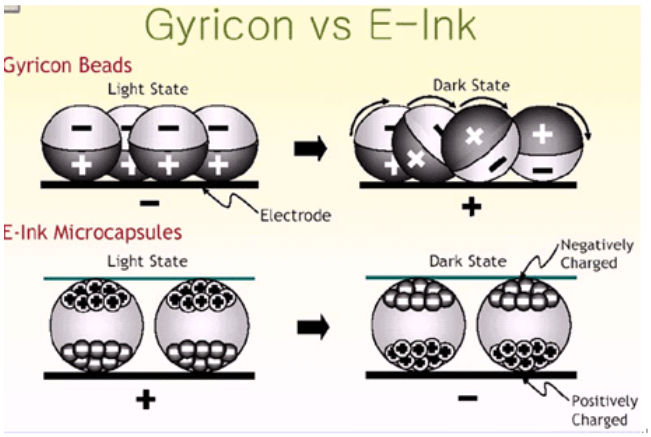


FIGURE 2.2: Operating principle of Gyricon and the E-ink EPD technology[19]

when the driving voltage is removed. Unlike monostable technologies like LCD, the EPD cell has two potential wells and the system can be hold stable in both wells without an external holding field[20]. A weak attractive force between the pigments and the bounding surfaces will lock the particles together, preventing flow when the electric field is removed[4]. The final pixel states are determined by a single polarity impulse signal. EPDs also require a periodic reverse impulse signal to avoid irreversible electromechanical damage of the EPD cell if a net DC voltage builds up across the EPD cell[4]. In order to operate the EPD cells, a specific driving circuitry is required. The display driving circuitry will be further described in Chapter 3.

2.3 Issues regarding the electrophoretic display

Some challenges regarding the EPD technology have been holding it back from the commercial market so far. In addition to limited color performances and video-capability, there are mainly four issues that affect the user-experience and image quality in a way that display technologies like LCD or OLED still are preferred among product developers.

2.3.1 Response time

Slow response time regarding driving of the display from one state to another has always been the dominant issue in electrophoretic displays[4]. Historically,

the switching speed has been improved by using a relatively high supply voltage typically in the range of $50 - 100V$[4]. Today, $15V$ is considered as the upper limit to use in battery powered devices. With a driving voltage of $15V$, a typical response time is several hundreds of milliseconds depending on the display size[21]. In order to obtain a desirable switching-time, the mobility of the charged particles needs to be considered. The particle velocity v is given by Stokes equation stated in Equation (2.1)[22]

$$v(t) = \frac{qE(t)}{6\pi\eta a} \tag{2.1}$$

where q is the charge of the particle, $E(t)$ is the effective electrical field at time t, η is the viscosity of the fluid and a is the radius of the particle[22]. The velocity depends linearly on the particle mobility, μ, and the local electric field, which can be determined by the moving distance of the particles[12]. The electrical mobility of the particles, μ, is defined as the ratio of the particle velocity, v, and the magnitude of the electrical field, E[23]. The moving distance of the particles can be directly related to the capsule diameter, L. The relation between particle velocity, mobility, applied voltage and capsule diameter is shown in Equation (2.2)

$$|\vec{v}| = \mu\left|\vec{E}\right| = \mu V/L \tag{2.2}$$

The response time of an EPD cell can therefore be described as in Equation (2.3)[12].

$$Response\ time = \frac{L}{|\vec{v}|} = \frac{L^2}{\mu V} \tag{2.3}$$

The equation predicts a quadratic dependence of response speed on capsule size, together with inverse dependence of applied voltage. The two most important parameters to consider regarding response time, without changing the physical EPD cell, are applied voltage and the duration of the voltage signal.

Figure 2.3 show a graph presented in Whitesides(2004)[12] where the dynamic range of an EPD cell (in L* units) is shown as a function of driving voltage and pulse length. The best case of white state reflectance ($\sim$ 40%) is obtained at saturation ($15V$, $200ms$). A dynamic range of L*=40 results in a white state

reflectance of around $\sim 36\%$[12].

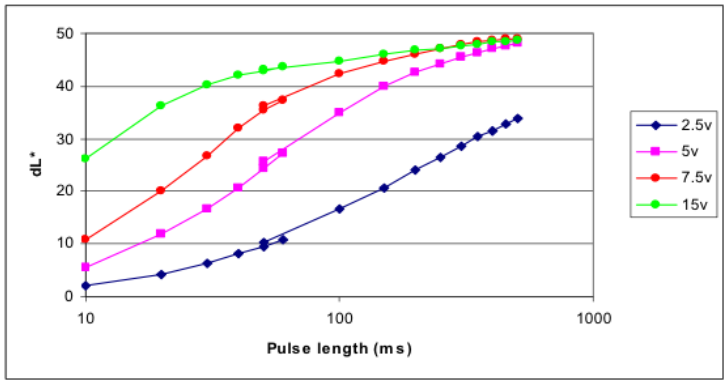


FIGURE 2.3: Dynamic range (L* units) of fast EPD as a function of voltage and pulse length[12]

2.3.2 Grayscale

Due to the bistable behaviour of the display, it is difficult to achieve gray levels with a high accuracy in the EPD-technology. With a two-particle dispersion with black and white particles, it is challenging to drive the display to something different from black or white. Often many particles with different sizes are put into the microcapsule, therefore the particle velocity for each microcapsule will be inconsistent. Today, it is achieved up to 16 gray levels in the EPD[24]. In order to achieve this gray level, pixels are first partially switched by blanking the display, for then to precisely control the amount of energy applied to achieve the desired state[21].

Another technique to achieve grayscale is to use the spatial dithering method as shown in Figure 2.4. By dividing a pixel into a group of adjacent sub-pixels, the human eye will perceive grayscale even though the sub-pixels are driven to fully black or white[25]. This method is also often used in the LCD technology, but a disadvantage with the technique is that it trade pixel resolution for gray levels. Due to the size of the EPD microcapsules, a high resolution gray level is hard to achieve with this technique.

2.3.3 Ghosting effect

Another problem with the EPD technology is the ghosting effect, also called *sticking image*. This means that the previous image content appears as a ghost image

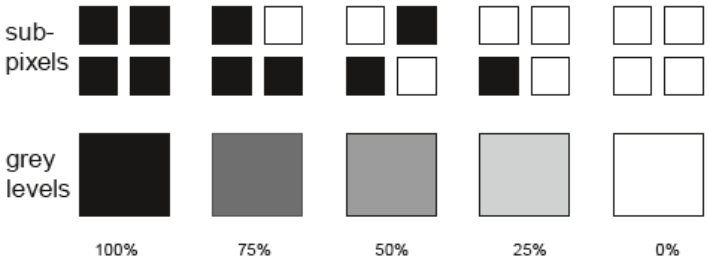


FIGURE 2.4: Example of the spatial dithering technique with four sub-pixels[25]

over the next image. A remnant internal electric field from the previous image affects the external driving electric field for the new image that will suffer from a different amount of gray level than expected[26]. Non-uniformities across the pixels are normally prevented by applying one or more reset pulses that drive the pixel to a uniform state. The reset pulses usually lead to unwanted flicker between the image updates[4].

The conventional method to applying reset pulses and solving the ghosting is to rewrite to the display several times by applying voltage pulses with frequently changing polarity[26]. This is called *shaking waveform*. A shaking waveform will neutralize the electric field, but the switching time and flicker will increase. In Figure 2.5 a conventional shaking waveform is illustrated.

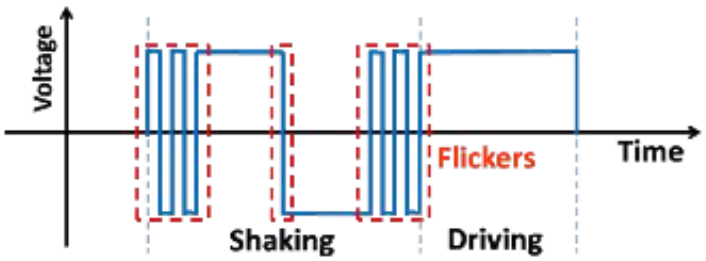


FIGURE 2.5: A conventional ghosting reduction driving method using shaking waveform[26]

It is normal to update an EPD in four stages, as shown in Figure 2.6, in order to eliminate the ghosting effectively. The display gets cleared between each image transition by inverting both previous image and the new image before stabilization of the new image. This quadruples the total stage time.

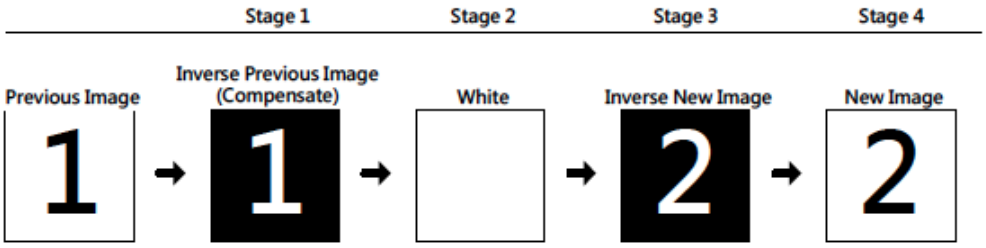


FIGURE 2.6: A traditional four stage image update technique for EPDs[27]

2.3.4 Flicker

Flicker in EPDs appears in the updating process when the display is driven to a stable image. Frequent voltage transitions between two image frames are normally required to either drive display pixels to a certain gray level or to reduce the ghosting effect. The visual effect of flicker can be eliminated if the flicker frequency is higher than $30Hz$[21]. In order to minimize flicker, the EPD driving circuitry should be able to deliver a driving waveform that effectively erase the original image and activate the particles in as few voltage transitions as possible. This is typically controlled from a timing controller and will further be described in Chapter 3.

Chapter 3

Display Driver Circuitry

When it comes to the driving circuitry of the EPD, a lot of its building blocks are inherited directly from the more mature LCD-technology. However, data and logic level processing should be considered differently from standard LCDs. Since the EPD only needs to be driven when the image state changes, systems to detect previous pixels on change request and thereafter change the state in an efficient manner should be implemented. Many chip-designers have taken part in developing display drivers for EPDs, first and foremost to optimize the issues described in Section 2.3 on page 10, and with less focus on miniaturization and reduced power consumption. One approach to build an efficient and low cost EPD driver is to utilize as much as possible from the LCD related hardware and interfaces already available on many host platforms. This chapter will give an overview of how a typical display driver circuit is constructed and an overall comparison of the LCD and EPD required electronics. It will highlight required hardware to further use in the design considerations for a low power EPD circuit design.

Figure 3.1 shows a block diagram of a traditional driver architecture for a small size LCD display. Most of the blocks on the left side are related to image data and video processing specifically designed for the LCD technology[25] and can be neglected for the EPD technology. The following sections will further describe the common building blocks used for both the LCD and EPD driver circuitry.

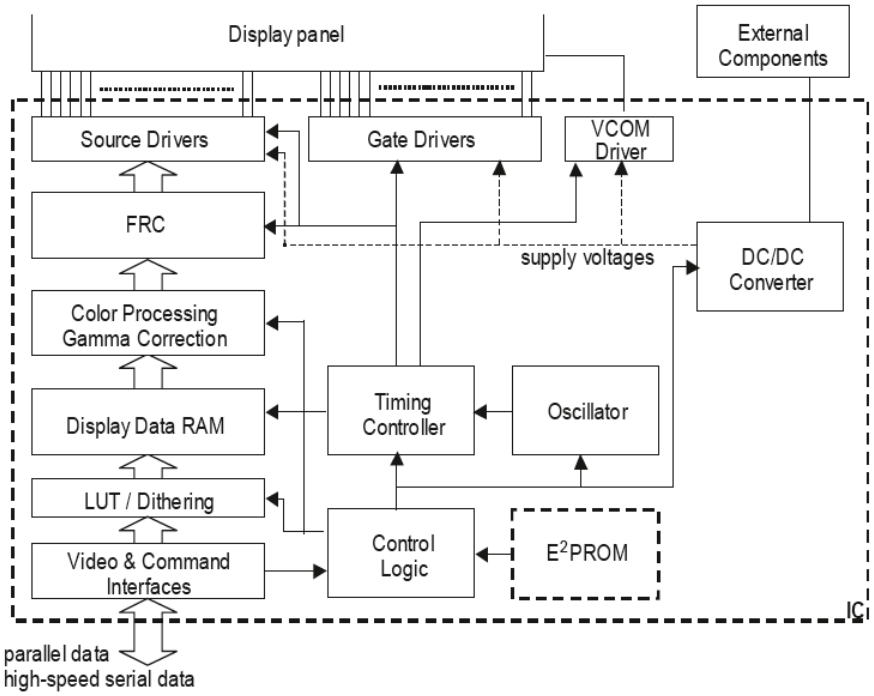


FIGURE 3.1: Internal driver architecture of a small size LCD[25]

3.1 Electrical addressing

There are mainly three different addressing methods in the display technology; direct, Passive Matrix (PM) or Active Matrix (AM)[4]. The first method is the direct addressing where each display segment is connected and individually controlled by the peripheral electronics. This method does not include any signal multiplexing. Direct addressing segmented displays are limited to be used in low-information-content displays.

High-information-content displays normally require arrayed pixels driven using a matrix of row and column electrodes. The simplest form for electrical matrix addressing is PM-addressing, where the crossing of transparent row and column Indium Tin Oxide (ITO)-electrodes forms a pixel. ITO-electrodes are widely used in flat panel displays due to their electrical conductivity and optical transparency properties[28]. A display with $m \times n$ pixels is constructed with m column electrodes and n row electrodes. The pixel values are determined from the voltage at the column electrodes. Pixels are normally written one row at a time by sequentially activate each row electrode from top to bottom with a specific voltage. Resolution and frame-rate is often limited by cross-talk between pixels in PM-addressing. Due to the bistable behaviour of the particles in EPDs, there are no threshold value

for precisely controlling the electric field[4]. This makes passive matrix addressing in EPDs difficult to achieve since cross-talk will appear even though the current at the rows are "OFF".

A more used electrical addressing technique is the AM-addressing. The AM drive relies on the presence of a Thin Film Transistor (TFT) for each pixel. Each transistor gate is connected to the row electrodes, while the column electrodes are connected to the pixel electrodes through the transistor sources. In addition, there is a dedicated storage capacitor for each pixel that can hold the pixel at a given state. Due to the bistable behaviour of EPDs, the storage capacitor is not a necessity, but is often used to hold the pixel state while scanning other rows. Figure 3.2 shows the basic principle of both PM and AM addressing. Here, the resistor and C_{LC}-capacitor is used to model the LCD pixel.

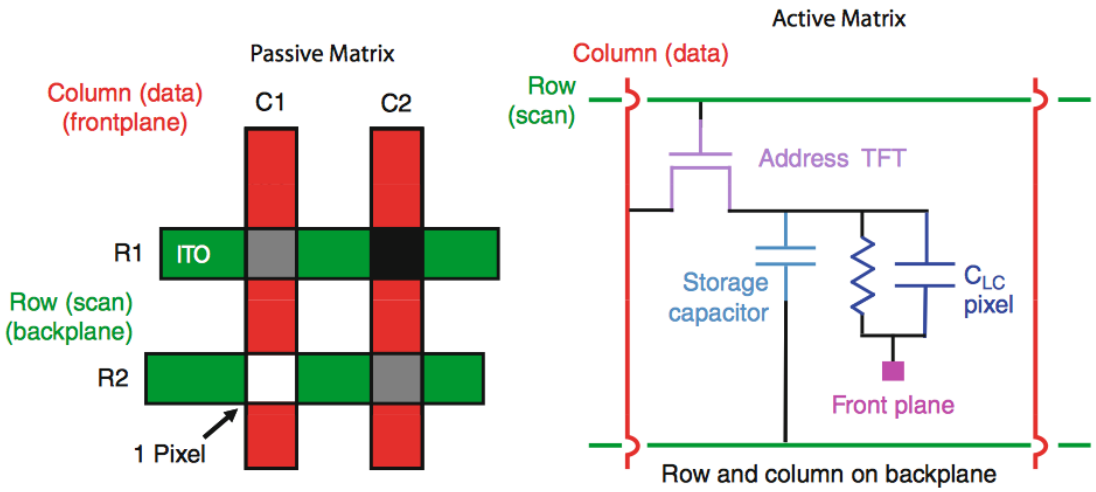


FIGURE 3.2: Basic principle of passive and matrix addressing for LCDs[29]

3.1.1 Thin-film transistor (TFT)

The Thin-Film Transistor has become the spearhead in flat panel development over the past 20 years[25]. In flat panels, the TFT is used as a switch to control the voltage transfer from the data line to the pixel electrode. Compared to conventional MOSFETs, TFTs have similar model equations, but the carrier mobility, μ, is much slower. This means that TFTs exhibit poorer performance, both in terms of conductance and switching speed[25]. TFTs also lack the substrate electrode, called *bulk* or *body* in conventional MOSFETs. However, TFTs are more suitable for flat panel displays due to their capability of transparency. Light must

pass through the substrate material of the transistor in order to reach the user. The most common substrate material used in TFTs are glass and a thin film of silicon is deposited on the top[25]. Traditional bulk MOSFETs are made of non-transparent silicon wafers, and will not be suitable as pixel electronics integrated on a flat panel display.

The two most commonly used types of TFTs are Hydrogenerated Amorphous Silicon (a-Si:H) and Polycrystalline Silicon (poly-Si). The main difference between these two types is that poly-Si can provide both n-type and p-type devices, while a-Si:H are just n-type[30]. a-Si:H is the most dominant technology used in flat panel displays because it is more cost efficient due to easy fabrication with lower processing temperatures. It is also probably the second most important transistor-technology on the market after MOSFET/CMOS. Poly-Si has on the other hand advantages of higher carrier mobility which can provide high driving current. The operation of both a-Si:H and poly-Si TFTs are similar to ordinary silicon MOSFETs. When TFTs behave like an electrical switch, it operates in the triode region of the MOS transistor[31]. The triode region is characterized by $V_{gs} > V_{th}$ and $V_{ds} \leq V_{gs} - V_{th}$. It is the region where I_{ds} changes linearly with V_{ds}. The current between drain and source terminal I_{ds} in this region can be described as Equation (3.1)[32][31]

$$I_{ds} = \mu C_{OX} \left(\frac{W}{L}\right) \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{3.1}$$

where μ is the mobility, C_{OX} is the gate insulator capacitance per unit, W and L is the channel width and length, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage and V_{ds} is the drain-source voltage[32][31].

Due to the low mobility in a-Si:H, it requires extremely large aspect ratios (proportional relationship between its width and its height) which leads to reduced aperture-ratio (a hole or an opening through which light travels) and image definition in traditional LCD technology[25]. To mitigate the problem, the gate of the TFTs are often driven at a higher voltage, typically in the range of $20V$[25]. The threshold voltage is also relatively high for this technology with V_{th} typically ranging from $2V$ to $5V$[33]. Poly-Si has larger OFF-currents and is typically driven to negative gate-source voltages in the range of $-5V$ to $-8V$ adopted to minimize the leakage current condition.

Organic Thin-Film Transistors (OTFTs) are now starting to compete with traditional TFT materials due to low fabrication cost and high flexibility. A piece of plastic can be coated with OTFT material together with a EPD-film and be made into an extremely flexible and robust display. Improvement of the development processes for OTFTs has recently lead to increased carrier mobility and products with OTFTs are slowly starting to emerge on the market[8][9][10]. OTFTs are still slower than silicon based TFTs, but its mobility has been proven to be sufficient to operate the EPD technology[34].

3.2 Driver electronics packaging

The display driver Integrated Circuit (IC) can be bonded onto different substrates. Reel-to-reel Chip On Film (COF) technology has been developed specifically to fit flat panel displays such as LCD[35]. The COF technology makes it possible to load a number of individual chips (multiple-chip technology) on the tape. Depending on the display substrate, the display driver can be bonded and integrated onto the display with technologies like Chip On Glass (COG)[36] or the ultra-thin and flexible alternative Chip On Plastic (COP)[37]. TFTs can also be used when designing the driver IC instead of standard bulk CMOS processes[38].

3.3 Output drivers

The purpose of the output drivers are to interface the driver IC with the display column and rows. A traditional active matrix display consist of a *gate driver*, a *source driver* and in some cases a separate V_{COM}*-driver*. The output drivers are responsible of driving all of the rows and column in the display matrix with the correct voltage-pulses. For an $m \times n$ pixel display, the source driver has normally m output lines, while the gate driver has n output lines. The V_{COM}-driver has its own output.

3.3.1 Gate driver

The main purpose of the gate driver is to scan the TFT-array and activate the pixels one row at a time (referred to Figure 3.2 on page 17). The gate driver has

primarily three functions:[25]
1) To read in the start signal
2) Progressively turn on pixel-TFTs on each gate
3) Turn off TFTs during pixel holding period

A typical gate driver (or scan driver) consist of three main circuit blocks; a *shift register*, *level shifter* and a *digital buffer* as shown in Figure 3.3[25].

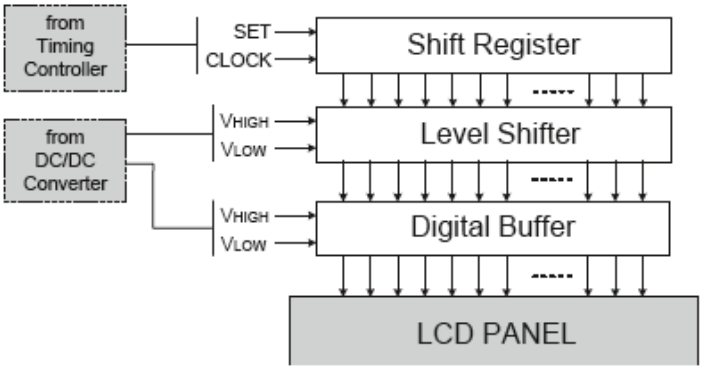
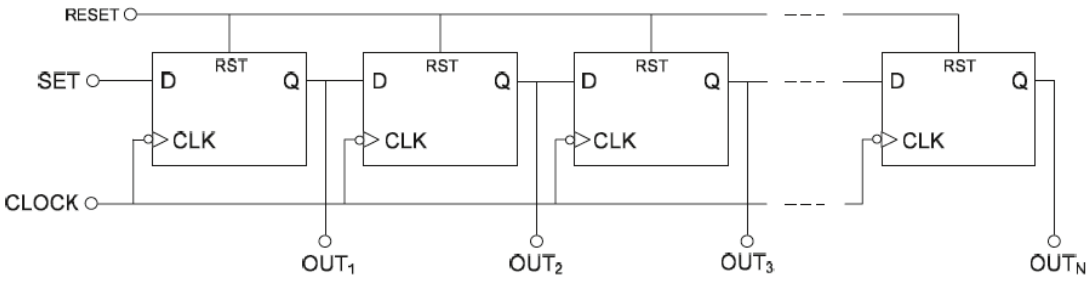


FIGURE 3.3: Block diagram of a conventional gate driver[25]

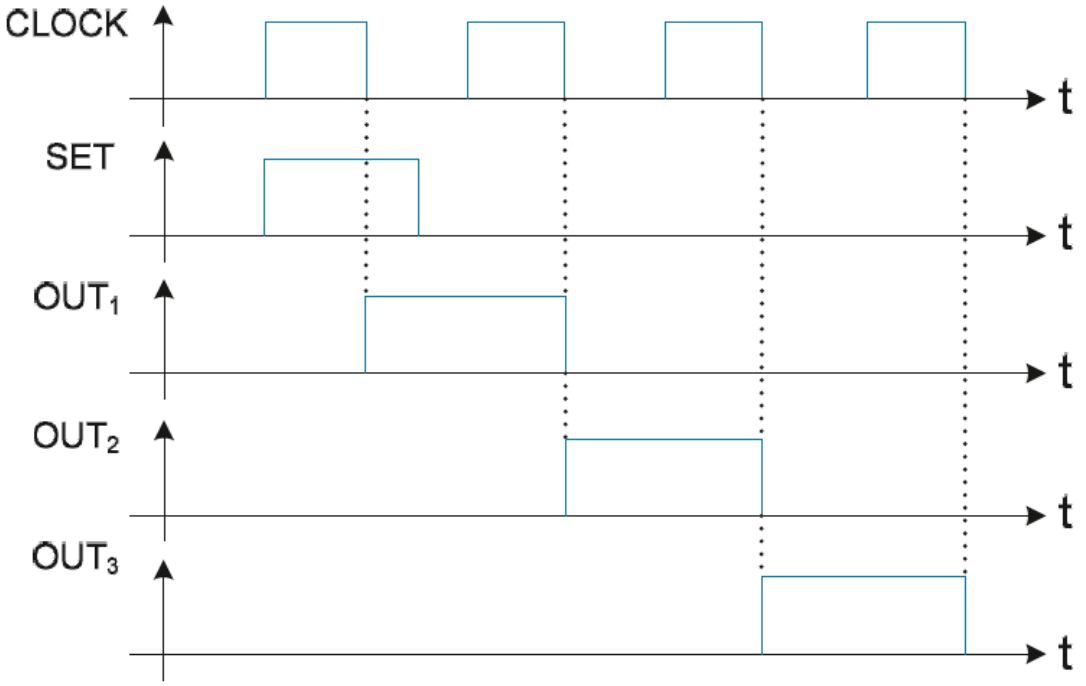
The shift register is used to set a scan impulse voltage at one row and shift to the next row at the next clock. An N-bit shift-register is normally composed of N series connected data flip-flops as shown in Figure 3.4a that forms a walking '1' data at the row scan rate as shown in Figure 3.4b[25].

The level shifter converts a low voltage input signal to an output signal with higher voltage swing and enables the TFTs in the EPD panel to be turned ON/OFF. Since the TFT gates are driven at a higher voltage typically at $\pm 20V$, a High Voltage (HV) dual supply level shifter is required. Figure 3.5 shows a schematic of a conventional CMOS level shifter circuitry[25]. It consist of a CMOS inverter (M1-M2) and two latches. The first latch (M3-M6) is used for negative supply shifting, while the second latch (M7-M10) is used for positive supply shifting. Here, V_{DDL} and V_{SSL} represents the low voltages used for the digital logic, while V_{DDH} and V_{SSH} is the high driving voltages used for the TFTs.

The digital output buffers are normally used to enhance the driving capability for adequate switching speed[25]. The buffers are most important for larger-area and high resolution displays. An EPD gate driver has the same functionality as an LCD gate driver and can potentially be re-used without any modifications.



(A) Shift register circuit[25]



(B) Shift register walking '1' waveform[25]

FIGURE 3.4: A flip-flop shift register with N outputs[25]

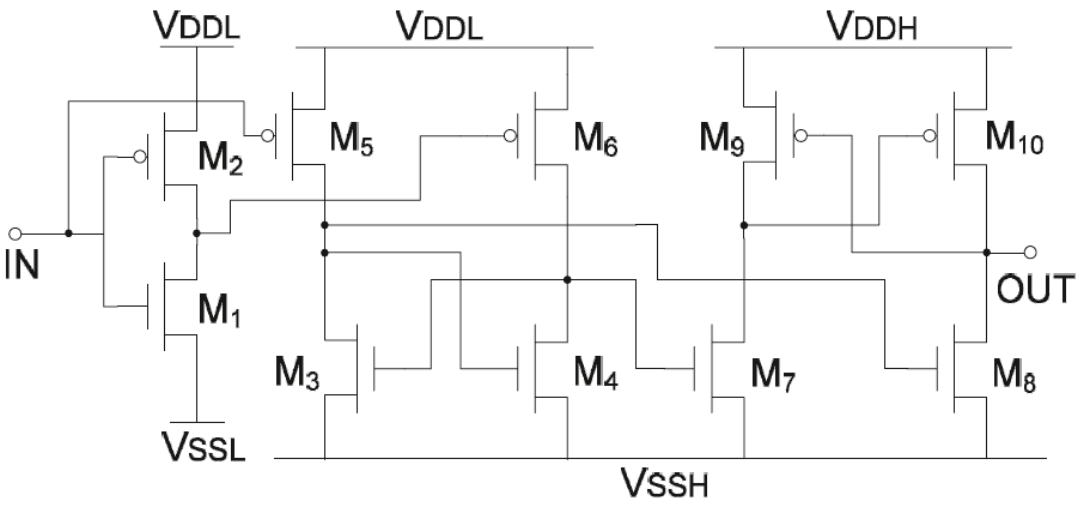


FIGURE 3.5: Schematic of a conventional CMOS level shifter[25]

3.3.2 Source driver

The purpose of the source driver is to receive image data as input, convert the data into appropriate voltages and drive the columns in the TFT-array (referred to Figure 3.2 on page 17). A traditional LCD source driver (or data driver) consist of five main circuit blocks; a *shift register*, two *latches*, a *Digital-to-Analog-Converter (DAC)-architecture* and an *analog buffer*. The shift register makes the sampling clock for the first latch. It serially shift the data input corresponding to all column lines. The content of the shift registers are transferred in parallel to the latches so it can be applied to the column electrodes simultaneously[25]. The first latch samples the data by sampling the clock. The second latch holds the sampled data until the load signal is triggered. The DACs converts the digital signal to analog signal according to a reference voltage in order to avoid electrophoresis or sticking image in the LCD, while the analog buffer drives and ensure exact voltage control for the display[39]. Figure 3.6 shows a block diagram of a typical LCD source driver adapted to 128 Red Green Blue (RGB)-pixels, which is equivalent to 384 outputs. Here, the two latch stages are hidden into the "Data latch" block. The first latch stage input the pixel data (RGB) and the second latch stage input a control signal (Load), that loads the digital data into the DAC.

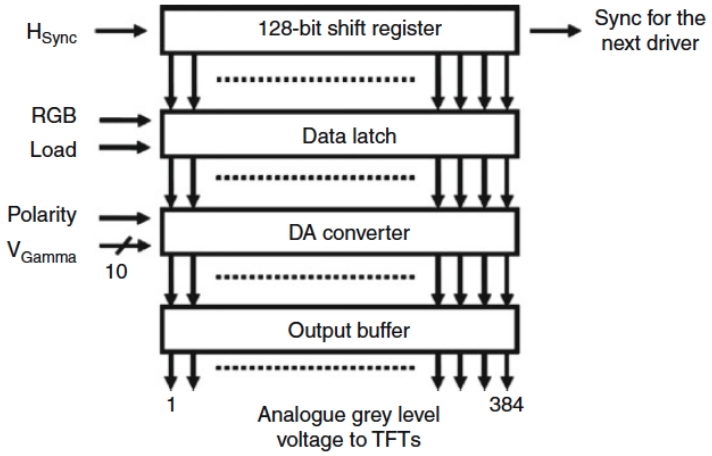


FIGURE 3.6: Block diagram of a conventional AM-LCD source driver[40]

An EPD source driver can be made simpler since the display does not require a high frequency update and analog data signals like LCDs. Since the output of an EPD source driver only require a basic ON/OFF control function, a conventional level shifter circuitry as shown in Figure 3.5 can be used also for the source driver.

In LCDs a basic ON/OFF control function is not sufficient to display images,

therefore a non-linear DAC-architecture is used for gamma correction and gray-level generation[25]. Normally, there are a precisely matched DAC for every source line, which occupy a lot of area on the source driver[41].

For the LCD-technolgy, external source driver ICs are necessary because the mobility is too low to achieve sufficient high speed with TFTs. Due to long EPD response time it is possible to also integrate the source driver onto a panel using TFTs[42].

3.4 Power management

For battery-operated portable devices, the external supply is normally kept as low as possible to contain a reasonable power consumption. Pixel addressing in EPDs typically require higher voltages for best optical performance. In order to generate row and column voltages in both positive and negative amplitudes, a DC/DC-converter is required that can produce these kinds of high voltages.

There are several types of architectures for a DC/DC-converter available. It can primarily be grouped into two different categories; *inductive* and *capacitive* architectures.

3.4.1 Linear regulator

A linear regulator is considered as one of the simplest DC/DC converter architectures. Often a Low Dropout (LDO) regulator is used to regulate the input voltages in a circuit, to achieve a stable, noise-free voltage[43]. It has the advantage of high efficiency regulating of the output voltage, even when the supply voltage is very close to the output voltage. It can also be made fully on-chip in silicon processes. However, linear regulators need to dissipate power across the the device in order to regulate the voltage. Therefore, it can only convert down the voltage and the larger the difference is between the input and output voltage, the more power is dissipated. Equation (3.2) shows how the power loss in an LDO typically is calculated[43].

$$P_{loss} = (V_{in} - V_{out}) \times I_{out} + (V_{in} \times I_Q) \tag{3.2}$$

Here, I_Q is the quiescent current required for the internal circuitry. Typically, $I_Q << I_{out}$. An LDO schematic of an LDO-regulator is illustrated in Figure 3.7. The main components are a power Field Effect Transistor (FET) and a differential amplifier[43]. As a basic functionality, the power FET is used to drive the output voltage relative to a voltage reference and the input voltage. Further details of the circuit functionality is considered as outside the scope for this thesis.

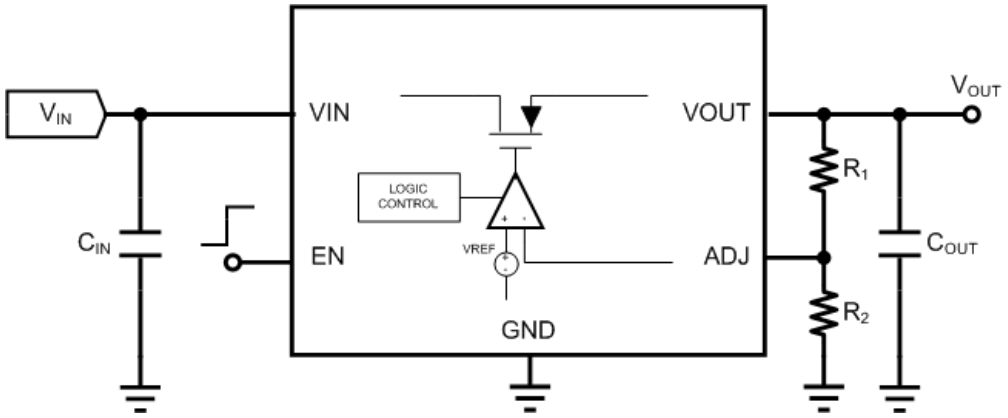


FIGURE 3.7: Schematic of an LDO regulator[43]

3.4.2 Switch mode power supply

The Switch Mode Power Supply (SMPS) is a discrete inductive power converter widely used in systems that needs to achieve a high power conversion efficiency with high output power[44]. The circuit is constructed of a power switch, an inductor and a diode to transfer energy from input to output. The arrangement of the component topology decide the function. Voltages can either be converted up (boost), down (buck) or inverted (flyback).

Figure 3.8 illustrates the basic boost converter circuit. V_{sup} represent the input DC supply. In the on-state when the switch is closed, the current is flowing in a loop through the inductor L, where the inductor current gradually will increase over time and a magnetic energy is building up. At this time no current will flow through the diode, instead the filter capacitance will provide the energy required by the load resistance[44]. In the off-state when the switch opens, the voltage across the inductor will add to the supply voltage and current will flow through the diode. The output voltage will therefore be higher than the supply voltage. In case the inductor provides higher current than required by the load resistance, the filter capacitance will absorb the excessive energy[44].

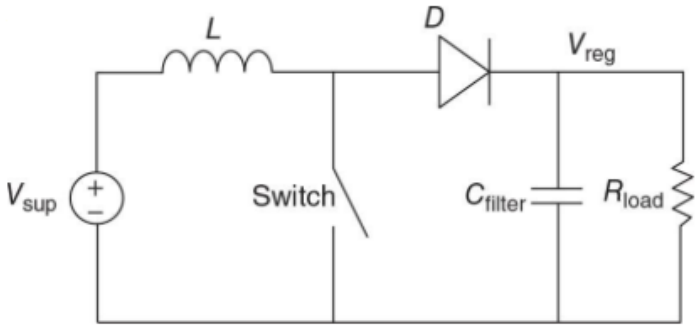


FIGURE 3.8: Boost converter configuration[44]

3.4.3 Charge pump

The charge pump architecture is based on switched-capacitor circuits. There is no inductive element involved in this architecture. A charge pump is made up of only capacitors and switches (or diodes) and allows for integration on silicon. The charge pump can be configured to cover different functionalities, such as a positive charge pump (step-up), negative charge pump (step-down) or as a charge pump LDO regulator[44].

The most widespread charge pump topology is the Dickson charge pump shown in Figure 3.9. Here $\phi 1$ and $\phi 2$ represents two non-overlapping clocks. Precharging of the capacitors and level shifting occur in two alternating phases of a pump clock for each stage.

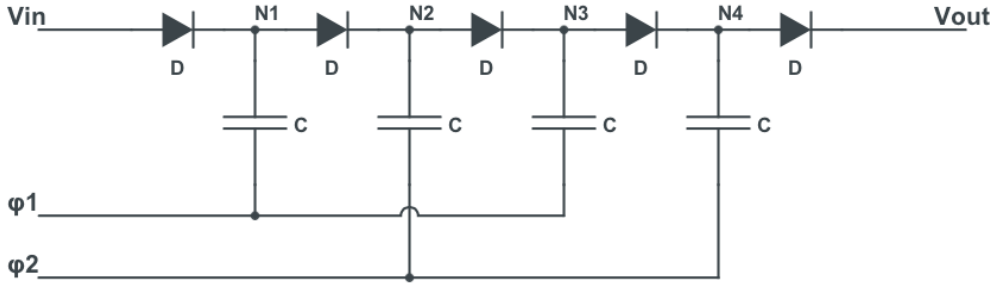


FIGURE 3.9: Basic 4-stage Dickson charge pump[45]

Before $\phi 1$ switches from low to high, the total charge at node $N1$ is given by Equation (3.3)[44].

$$Q_{N1} = V_{in}C \tag{3.3}$$

During the switching of the clocks, the charge will be moved from node $N1$ to

node $N2$. Since the diodes are reverse-biased, the maximum potential that can be achieved at node $N1$ is seen in Equation (3.4)[44].

$$V_{N1_{max}} = V_{in}\big(1 + \frac{C}{C + C_p}\big) \approx 2V_{in} \qquad (if\ C_p << C) \tag{3.4}$$

C_p represent the parasitic capacitance located on the node. If we consider all components as ideal, the voltage at node $N2$ will be minimum $2V_{in}$. If the number of pump stages is cascaded, the maximum voltage level will increase accordingly. By considering a positive charge pump, the maximum voltage level achievable is roughly determined by the number of pump stages together with the input voltage as seen in Equation (3.5)[44].

$$V_{out_{max}} = nV_{in} \qquad (n = no.pump\ stages) \tag{3.5}$$

The maximum output voltage for the 4-stage Dickson charge pump in Figure 3.9 will therefore be four times larger than the input voltage. It is worth noticing that capacitor-based voltage converters are inherently lossy compared to inductor-based converters[44]. Therefore, charge pumps are often limited to drive small size displays, typically up to around 8 inch for the LCD-technology[25].

3.5 Timing control

A timing controller is responsible for interpreting the data and display it on the screen. It synchronizes the column and row operations by selecting the proper rows from the image data stored in memory[25]. Normally, the timing controller generate the driving waveform to the output drivers. As shown in Figure 3.3, the timing controller provide the SET and CLOCK signal for the shift register in the gate driver. In Figure 3.6 on page 22 the timing control signals are illustrated as H_{Sync}.

A timing controller can either be an external module like a host Microcontroller Unit (MCU), or it can be integrated into the same driver chip as the rest of the driving circuitry. An external waveform generator, such as an MCU, is most commonly interfaced to the driving chip through a serial bus. The driving waveforms

are thereafter distributed to the output drivers internally in the driver chip, which translate the waveforms from serial data into parallel driving voltages.

A traditional bipolar waveform used in EPDs is shown in Figure 3.10. The common top electrode of the EPD cell (referred to Figure 2.1 on page 9) is normally connected to a voltage around $0V$, while the bottom electrode voltage switches between a positive or negative voltage related to the pixel values from the image-data. The pixel electrode voltage is here represented as the source driver outputs as shown in Figure 3.6 on page 22.

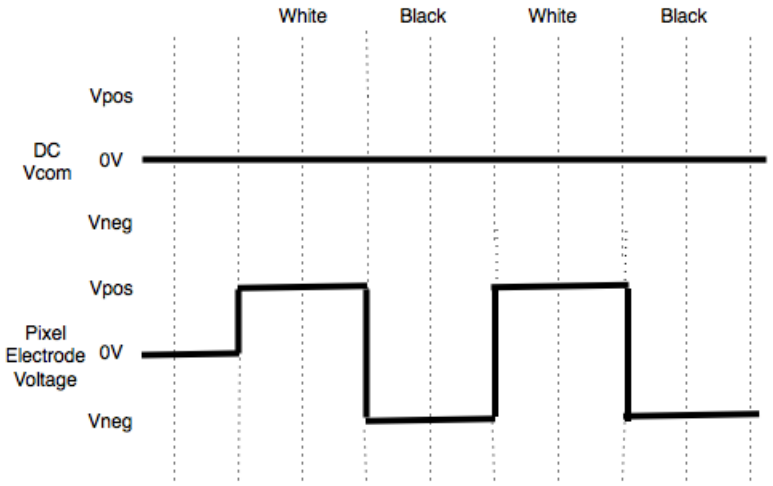


FIGURE 3.10: Traditional bipolar driving waveform for EPDs[46]

The timing controller is usually a fully digital circuit operating at low voltages with respect to a clock signal most commonly generated by the host system. An internal oscillator as shown in Figure 3.1 can also be used.

3.6 Communication interface

In order for the EPD module to communicate with the host system, a communication interface needs to be set up. The most common alternatives to interface peripheral display driving circuits with a host system is to use synchronous protocols like Inter-Integrated Circuit (I^2C) or Serial Peripheral Interface (SPI). Both of these interfaces are considered as easy to implement, low cost and ideal for small embedded devices[47].

I^2C require only two signal lines for communication. One for data (SDA) and one for the clock (SCL)[47]. The I^2C bus driver is "open drain"/active low and each

signal line has a pull-up resistor to restore the signal to high when not asserted by another device. Since I^2C only has two signal lines, it require a more complex communication protocol and hardware than SPI. While SPI is not limited to a maximum clock speed, I^2C is limited to a clock speed between 1-5MHz[47].

Serial Peripheral Interface (SPI) is a widely used protocol that provides a low cost and simple interface between microcontrollers (master) and peripheral chips (slaves). It is known as a four-wire interface using the signals *Master Out Slave In (MOSI)*, *Master In Slave Out (MISO)*, *Serial Clock (SCLK)* and *Chip Select* ($\overline{CS}$). SPI is a synchronous protocol where all transmissions are referenced to a common clock, generated by the master. Both master and slaves contain a serial shift register to transfer and exchange one byte of data between master and slave simultaneously as shown in Figure 3.11[47].

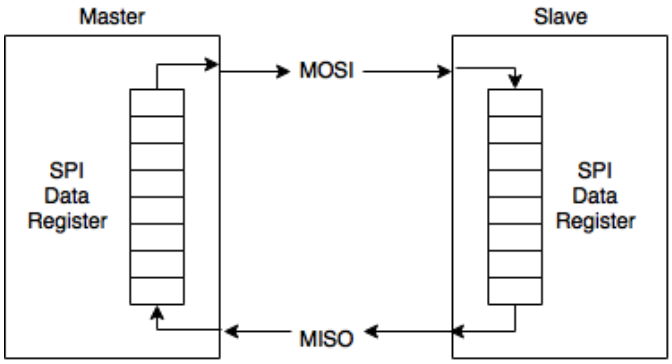


FIGURE 3.11: SPI transmission[47]

The timing diagram of the transmission is dependent on how the clock polarity and clock phase is configured with respect to the data sample. There are four different modes and the most commonly used is SPI Mode 0. In Mode 0, data is sampled when clock polarity (CPOL) is low and the clock phase (CPHA) is zero[47]. Figure 3.12 show a conventional timing diagram for one byte transfer with SPI Mode 0.

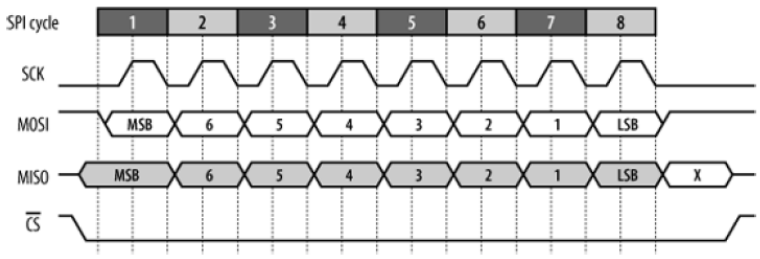


FIGURE 3.12: SPI timing diagram Mode 0; CPOL=0, CPHA=0[47]

3.7 Temperature sensor

A temperature sensor is normally utilized in flat panel displays that shall be able to operate at varying temperatures. Both the LCD and EPD technology are based on liquids and the driving circuitry needs to be compensated for temperature changes for best possible optical performance. The liquid viscosity changes with respect to temperature. A colder environment makes the particles in the pixel cell to move more slowly. A typical representation of a practical response time as a function of temperature is shown in Figure 3.13[48].

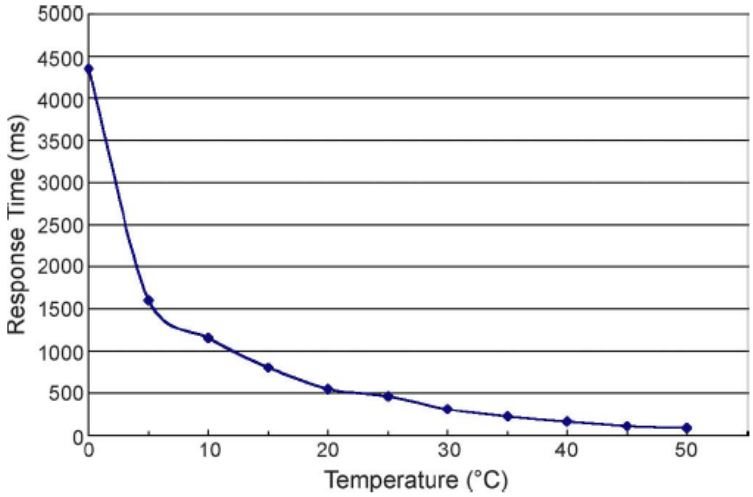


FIGURE 3.13: Response time as a function of temperature in EPDs[48]

To compensate the driving circuitry for temperature changes, a temperature factor should be set to calculate the total stage time when updating the display. As shown in Figure 3.13, the operational temperature in EPDs are normally between 0-50°C. A colder environment require the display to be rewritten more to avoid ghosting-effect.

The threshold voltage V_{th} of the transistors also tends to decrease with temperature[25], therefore the ON-current in a-Si:H TFTs are reduced in colder environment (referred to Equation (3.1) on page 18).

A temperature sensor can be constructed in many ways. A possible block diagram of a 7-bit temperature sensor is shown in Figure 3.14[25]. Details regarding its functionality is considered as outside the scope for this thesis.

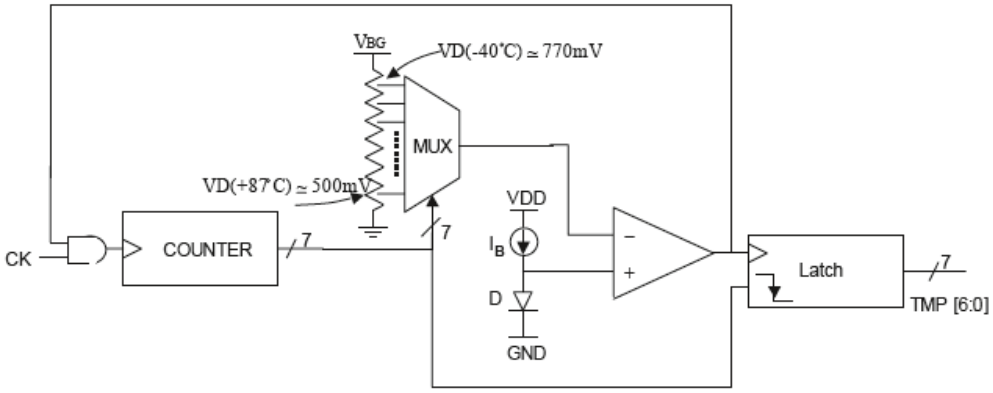


FIGURE 3.14: Block diagram of a temperature sensor[25]

3.8 Memory

The MCU should keep two frame buffers in memory in order to compare a new image with the previous. Memory and processing power will be required to render and store images. A frame buffer is normally defined as a portion of Random Access Memory (RAM) that contains a bitmap of image data[49]. The information in the image frame is normally composed of a two-dimensional array of pixel values according to the resolution of the display. The simplest form of image data is a 1-bit binary representation of every pixel. For instance, by defining a binary zero as black and binary one as white, a simple monochrome image can be stored in the memory. A processor can then be used to generate more texture, lighting or shading in the image, which is a part of the rendering process. Since EPD-cells primarily are constructed to show monochrome black and white images, a 1-bit representation of the image data will be used as basis for further discussion.

It is important that the image patterns are converted to a 1-bit bitmap format prior to writing to the display. In order to allocate and store both previous and new image pattern, the size of the memory should be at least $\frac{m \cdot n}{8} \times 2$ bytes, where m and n represents the number of row and column pixels.

A complete connection between each sub-circuit and more details on how the pixel-addressing can be achieved for an EPD driving circuitry will be shown in later chapters.

Chapter 4

Low-Power Design Methodologies

In chip and circuit designs, there are always multiple sources for power consumption and the power use is different from chip to chip. The design process involves several steps ranging from system specification, architectural design, functional design, logic, circuit and physical design. There are different forms of power saving opportunities at each level. A good low power design requires optimizations at all levels and designers should be energy aware already from design planning and throughout the whole design process. This section will highlight some sources for power dissipation and describe a few well proven techniques that can be used at different abstraction levels to reduce the power consumption.

4.1 Power consumption in CMOS circuits

Before entering a discussion of low-power design techniques related to the EPD driving circuitry, it is important to understand the concepts of power consumption in the CMOS circuit. Figure 4.1 shows a simple CMOS inverter consisting of one PMOS and one NMOS. Normally, the power consumption is decomposed into static and dynamic power consumption. The total power consumption can be written as Equation (4.1).

$$P_{total} = P_{static} + P_{dynamic} \tag{4.1}$$

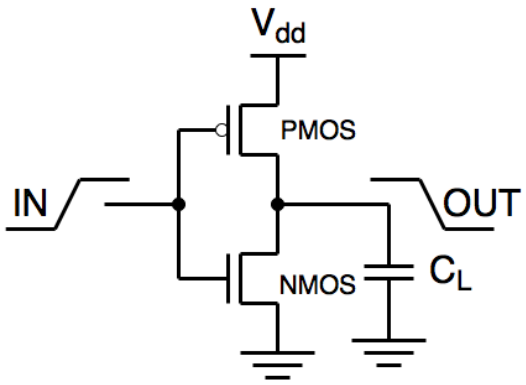


FIGURE 4.1: A simple CMOS inverter circuit

4.1.1 Static power

Static power consumption in CMOS is due to leakage currents in the MOS-transistors. Leakage current in CMOS consist of sub-threshold currents, diode leakage and gate leakage[50]. By taking these three currents and multiply with the supplied voltage, we get the static power consumption as shown in Equation (4.2). Since the MOS-transistor is not a perfect switch in reality, leakage current will always occur. As CMOS technology and threshold voltages are scaled down, the leakage currents will increase[51].

$$P_{static} = I_{leakage} V_{dd} \tag{4.2}$$

Traditionally, techniques as transistor stacking, multiple/dynamic V_{th} and multiple/dynamic V_{dd} are used to effectively reduce the leakage current at circuit level for high-performance logic[50].

4.1.2 Dynamic power

The dynamic power consumption occur when the MOS-transistors are switching from one state to another. It has two contributing factors; *short-circuit power* and *switching power*[51]. Considering the simple CMOS inverter shown in Figure 4.1, short-circuit power arises at a point during the switching transient, where both the NMOS and PMOS devices are turned on simultaneously. For a short time period a short-circuit exist and currents are allowed to flow freely between V_{dd} and ground.

The most dominant part of the dynamic power consumption is the switching power[52]. The dynamic switching power can be described as Equation (4.3)

$$P_{dynamic} = \alpha C_L V_{dd}^2 f_{clk} \tag{4.3}$$

where α is the switching activity factor, C_L is the load capacitance, V_{dd} is the supplied voltage and f_{clk} is the operating frequency of the device. By reducing each factor in this equation, we can reduce the total power consumption. Several research efforts have been proposed to reduce these factors[51][52][53]. For instance, switching activity (α) can be reduced by switching off inactive blocks and use conditional clock, precharge and execution. The active load (C_L) can be reduced by minimizing the circuits, use charge-recycling and focusing on more efficient design and layout[53]. Technology scaling will effect the threshold voltages and the voltage supply can often be reduced when technology is scaled down. In order to reduce the operating frequency, more parallelism and using less pipeline stages for shorter critical path should be considered.

4.1.3 Energy versus power

Energy is defined as the capacity to do work[54]. It is measured in Joules and equals to power integrated over time. Power is defined as the rate at which work is performed[54] and is measured in Watts. Using Ohm´s law of power as shown in Equation (4.4), power (P) can be found by taking the voltage (V) applied to a circuit and multiplying with the current (I) flowing through it.

$$P = V \cdot I \tag{4.4}$$

By summing the average power with the delta time, the total energy consumption can be calculated as shown in Equation (4.5). Here, E is the total energy consumption, N is the total number of sub-circuits, P_i is the average power consumption per sub-circuit and Δt_i is the time for which the specific sub-circuit consume power.

$$E = \sum_{i=0}^{N} P_i \cdot \Delta t_i \tag{4.5}$$

4.2 Power consumption trade-offs

From Equation (4.3), we can see that voltage has a quadratic relationship on power. Therefore, voltage reduction offer the most direct means of minimizing power consumption. By reducing the supply voltage with a factor of two, the power consumption will decrease with a factor of four without requiring any special circuits. Unfortunately, the overall system performance is affected by lowering the supply voltage, leading to increased circuit delay[51].

The physical capacitance in CMOS circuits comes from two main sources; *devices* and *interconnect*. The most significant contribution for devices comes from the capacitance associated with the thin gate oxide of the transistor[51]. Source and drain capacitance will also in some extent contribute to the overall device capacitance. The capacitances related to the interconnect are called parasitics. As technology continue to scale down, parasitic capacitances tend to dominate more than past technologies. These capacitances appear between each metal layer and the substrate. Capacitances can be kept to a minimum by using small devices and short wires[51].

The activity determine how often the switching occurs. For instance, a chip with large capacitances that does not switch will have no dynamic power consumption. If switching occurs at a high frequency over a longer period, the total power consumption will be high no matter if the rest of the design is well designed regarding power reduction techniques. Therefore, the switching activity should be kept to a minimum either by reducing the frequency or the time period for which the switching occurs.

4.3 Abstraction levels

While a low power system should be optimized at all levels of abstraction, it is important to understand the impact each level have on the total power. The largest power savings are normally achieved at the highest abstraction levels. Typically, the power savings are less than $2\times$ on circuit and gate level, while improvement on architecture and algorithm strategies can offer power savings of $10 - 100\times$ or more[51]. Therefore, low power design strategies should address high-level issues before dealing with low-level concerns. Following is an overview of some low power

design techniques used at each abstraction level presented in Landman(1994)[51], Rabaey(2012)[52] and Chandrakasan(2012)[53] with the EPD driving circuitry in mind.

4.3.1 System and architecture level

For this thesis, system level is considered as the highest abstraction level. The system level is primarily used to describe the system functionality through so-called black boxes. There are no details regarding physical circuitry. The architecture refers to the Register Transfer (RT) level of abstraction. It is described through blocks such as memory, controllers and combinational logic. At this level some of the most rewarding low power strategies to look at, involves trading area and performance for power through concurrent processing at low voltages. With techniques as parallelism and pipelining at block level, it can allow for reduction in supply voltage at same performance primarily through the reduced clock frequency. Since reduced voltage offer a quadratic reduction in power, this can have a great impact on the total power consumption.

Power management should also be evaluated carefully, since any power consumed by the system that does not lead to useful results are wasted. Selective power down, sleep modes and adaptive clocking and voltage techniques should be considered.

4.3.2 Gate level

Several techniques has been proposed to reduce power consumption at the gate-level. Complex gates tend to have overall lower physical capacitance since signals are confined to internal nodes rather than more heavily loaded output capacitances. By decomposing the Boolean network to achieve minimum switching activity and then hide the high activity nodes inside a complex CMOS gate, power consumption can be reduced. Of course there is a trade-off between performance and power if the gate is too complex and slows down the circuit dramatically.

Activity can also be reduced by avoiding wasted transitions associated with glitching. A lot of glitch reduction at this level is about reordering the gate structure. For instance, if a logic function can be implemented as a balanced tree, instead of

cascading the logic gates, fewer transitions are necessary. By using concurrency, the tree structure achieves a shorter critical path than the cascaded structure.

4.3.3 Circuit level

Many circuit-level techniques are also available for low power design. Circuit style can play an important role on power consumption and should be carefully selected. A careful evaluation of whether the circuit should be static vs. dynamic, synchronous vs. asynchronous, fully complementary vs. passing transistor, etc. can often be of importance for the power consumption. Standard cells are often severely over-sized for best performance and worst case loads. By customizing cells, wasted power can be avoided.

4.3.4 Layout and component level

The lowest level of abstraction is design strategies related to the specific technology process used and how it is laid out into the package. The two most important process-based techniques to reduce power consumption is *technology scaling* and *threshold voltage scaling*. By scaling down dimensions such as transistor widths and lengths, oxide thickness, depletion region widths, interconnect widths etc., device capacitances are scaled down accordingly. Then if supply voltages remain unchanged, this reduction of capacitance is passed directly to power consumption. This relationship can also be seen in the current Equation (3.1) for MOSFETs presented in Subsection 3.1.1 on page 17.

Reducing threshold voltages V_{th} is also of significance when operating at lower supply voltages. In reality there will be a sub-threshold conduction even if $V_{gs} < V_{th}$ and the transistor ideally is turned off. Often low-V_{th} transistors are used in critical paths of the circuit where good performance is important, but at the expense of much larger leakage currents. High-V_{th} transistors can be used to compensate for the leakage in less critical paths. They are normally up to an order of magnitude slower, but power consumption can be reduced significantly.

Chapter 5

Previous Work

This chapter will describe previous work related to design of low power EPD modules and associated research. The results described in this chapter are considered as important basis for the work performed in this thesis. Since the majority of the previous research in the EPD-field is related to larger sized displays with e-paper applications in mind, it is important to find out how this research relates to smaller sized EPDs, with approximately 1" in diameter, which is rarely described in previous publications. This will be the focus for the rest of this thesis.

5.1 Static displays - specialization project

A review of different electronic paper technologies was conducted as a specialization project at Norwegian University of Science and Technology (NTNU), fall 2015[55]. The focus for the project was to study and compare the different electronic paper display technologies and highlight which technologies that are most promising for low power IoT-applications.

Following are the main studied display technologies:

- Electrophoretic
- Electrowetting
- Electrofluidic
- Electromechanical Interface Modulation (MEMS)

- Photonic Crystal
- Electrochromic
- Cholesteric Liquid Crystal

The electrophoretic display technology was seen as the most promising to use in IoT-applications. This is mainly due to its bistability behaviour with no static power consumption and potential of very low dynamic power consumption. It is also one of the most mature electronic paper technologies with well established manufacturing processes that brings down the total cost. Appendix A shows a comparison with the main differences in today´s electronic paper display technologies.

5.2 Power consumption of microencapsulated EPDs for smart handheld applications

A detailed investigation of power consumption in microencapsulated EPDs for smart handheld applications was performed by Michael G. Pitt in cooperation between Philips Mobile Display Systems and E-ink Corporation in 2002[11]. According to their power analysis, most of the power loss in EPDs arise from driving the source lines related to data addressing (referred to Figure 3.2 on page 17). In a monochrome EPD, voltages to the source lines are only applied when changing the state from either white (W) to black (B) or from black (B) to white (W). Figure 5.1 shows how a typical source driver voltage pulse controls the electronic ink transition between two images in one column of the display. We can see that the voltage transition is highest in cases where two vertically adjacent pixels are changing from either $B \rightarrow W$ to $W \rightarrow B$ or opposite. Here, the arrows represent the vertically adjacent pixels. Since the capacitive component only consume energy when the source voltages changes, the power consumption will be highly dependent on the images used.

Table 5.1 shows a matrix of the voltage transition levels between two images when the applied voltage is $\pm 15V$. Referred to Figure 5.1, the transition from Image 1 to Image 2 changes from $B \rightarrow B$ to $B \rightarrow W$ at the top row, so the voltage transition will be $+15V$. The power loss is largest where the voltage transition

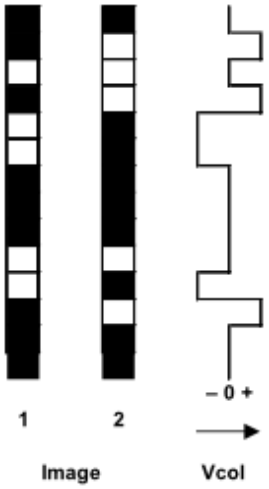


FIGURE 5.1: Schematic showing column voltages for electronic ink transitions[11]

TABLE 5.1: Voltage transition matrix[11]

Image 2 / Image 1	$B \rightarrow B$	$B \rightarrow W$	$W \rightarrow B$	$W \rightarrow W$
$B \rightarrow B$	0	+15V	-15V	0
$B \rightarrow W$	-15V	0	-30V	-15V
$W \rightarrow B$	+15V	+30V	0	+15V
$W \rightarrow W$	0	+15V	-15V	0

is $+30V$ or $-30V$. The worst case image pattern is therefore alternating vertical B/W/B/W pixels that is inverted to alternating vertical W/B/W/B pixels.

Figure 5.2 shows an example of a breakdown of the power consumption in a EPD driving circuitry[11]. The analyzed display was a 7" diagonal SVGA (800×600 pixels) resolution B/W display. As shown in the diagram, there are also a significant power loss from DC/DC conversion due to large transient power of the source lines.

5.3 System integration of EPDs

In 2006, Society for Information Displays (SID) published a paper written by Robert. W. Zehner at E-ink corporation that shows how a variety of supporting components can be combined to form a fully functional consumer EPD product, in addition to a few important requirements that need to be considered when designing an EPD driving circuitry[56]. By studying requirements of EPDs and

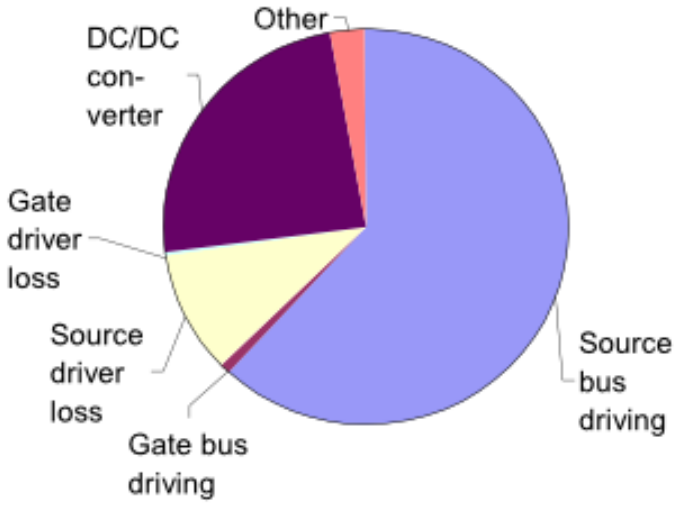


FIGURE 5.2: Breakdown of power consumption in EPD driving circuitry[11]

comparing them with LCD-focused components, reusable components as well as target areas for improvement can be highlighted in order to bring an active matrix EPD to the market.

Regarding driving and control of the EPD panel, a few components needs to be customized in order to fully exploit the technology. Unlike LCD, the EPDs are sensitive to polarity of the applied voltage. Since the response time improves dramatically with higher voltages, the source driver should be implemented as a high-voltage tri-level driver to drive pixels to both black and white with $\pm 15V$, while holding non-switched pixels at $0V$.

Electrophoretic displays also respond to the time-integrated voltage, which means that the pixels respond to both applied voltage and the time for which the voltage is applied. A timing controller should be capable of applying a time-dependant voltage, depending on the previous image on the display.

Since the EPDs does not require continuously scanning of the display like LCDs, more software-related controller based power reduction techniques can play an important role in EPD driver development. Table 5.2 shows the difference between power consumption of various controller modes of a 6" SVGA EPD module. It can be seen that even when the display does not actively update the image, it consume a considerably amount of power as long as the module is active. By turning off the entire module when not in use or using power-saving modes to put the module in standby, the power consumption is reduced dramatically.

TABLE 5.2: Power consumption of 6" SVGA EPD Module[56]

Controller Mode	Power
Actively updating image (average over 15 images)	$447mW$
Quiecent (active, not updating image)	$155mW$
Standby	$5.1mW$

5.4 EPD power model

A power characterization of EPDs at the sub-pixel level was modelled and presented in Baker(2007)[57]. The power consumed through physical movement of a single particle can be determined by manipulating the Stokes Equation (2.1) on page 11. The force acting on the particles can be based on the pigment particle charge. By multiplying the pigment particle concentration by the volume per capsule, an approximation of how many particles there are per capsule can be made. Table 5.3 lists the fundamental properties used in this specific power characterization. It was approximated that one capsule contain around 1300 particles. The work performed by each particle was found by multiplying the force with the particle velocity, which equals to 4.33E-13W per pigment particle or 5.63E-10W per microcapsule.

TABLE 5.3: Simulated EPD attributes[57]

	Value	Unit
pigment particle radius (r)	0.5	μm
pigment particle charge (q)	4.8E-16	Coulomb
microcapsule diameter	50	μm
supply voltage	15	Volts
suspension resistivity	1.0E12	Ωm
particle consentration	2E16	particles/m^3
microcapsules/subpixel	6	capsules

The leakage power is calculated based on the capsule's resistance and operating voltage. In Baker(2007)[57] the resistance is found based on the resistivity on the suspended particles in the clear fluid. With a driving voltage of $15V$ and 6 microcapsules per sub-pixel, both dynamic and static power consumption for the sub-pixels are calculated with the result shown in Table 5.4.

Since the value for the static power consumption is in four orders of magnitude smaller than the dynamic power consumption, it can be ignored when calculating the total sub-pixel power consumption. The total power consumed is also highly

Table 5.4: Subpixel power consumption[57]

	Watts
Steady-state power consumption due to electrophoretic particle motion	3.24E-9
Capsule leakage power	8.84E-13

dependent on the size of the storage capacitor and transistor process used at the pixel-circuit.

5.5 Configurable timing controller for AM EPD

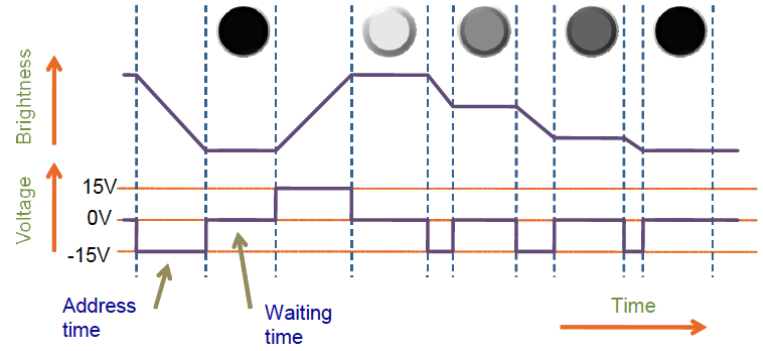
A configurable timing controller to support various types of EPD panels is presented in Kao2009[22]. The paper describe that the three most important things to consider when designing an EPD timing controller is the following:
1) The activation sequence of the particles.
2) The movement of charged particles for displaying desired gray-levels.
3) The bistable properties and image erase sequence.

In conjunction with discussion of the gray-level driving sequence, two types of EPD driving methods are compared in the paper. Figure 5.3 shows the two different driving waveforms. Figure 5.3a shows a bipolar driving waveform, while Figure 5.3b shows a unipolar driving waveform. A comparison between the two waveforms with respect to power and performance is discussed in the following chapters.

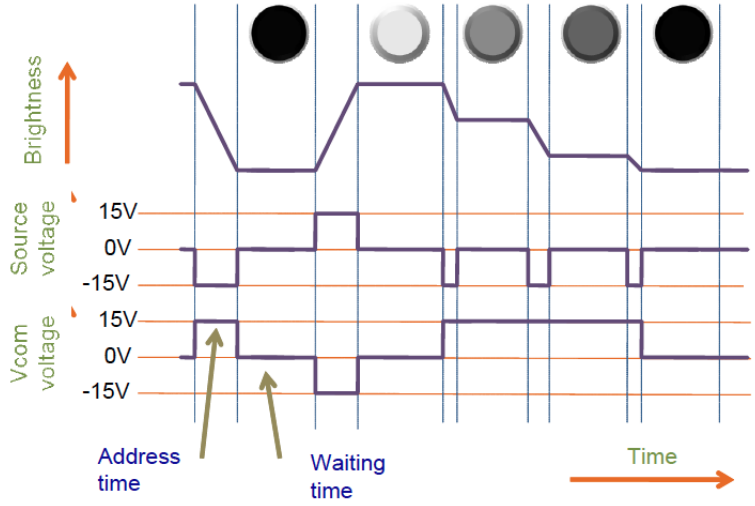
5.6 RePaper

RePaper[58] is a project which intend to make EPDs easy to use by providing open source codes, documentation, development kits and learning guides for controlling the display. The site is brought out by Pervasive Displays Inc. (PDI). The hardware development kits are based on popular open platforms such as Raspberry Pi, Beaglebone, Arduino and LaunchPad[58]. Today, PDI is considered as one of the largest providers for commercially available active matrix EPDs[58].

The following sections describe the hardware that the physical tests and measurements in this thesis are based on. The complete test setup will be further described in Chapter 6.



(A) Bipolar driving waveform



(B) Unipolar driving waveform

FIGURE 5.3: Two types of driving waveform, bipolar and unipolar

5.6.1 Aurora Mb EPD panel

An EPD panel provided by Pervasive Displays Inc (PDI), has been used in this work. The display is designed with basis from the trademarked E-ink Aurora, which is tuned for non-eReader applications and most commonly used in electronic shelf labels (ESLs)[8]. The smallest PDI display is a 1.44" a-Si:H, TFT active matrix EPD with a resolution of 128 × 96 black/white pixels[59] as illustrated in Figure 3.2 on page 17. The EPD panel has an integrated Chip on Glass (COG) driver IC, which is interfaced via SPI through a 40-pin Flexible Printed Circuit (FPC)-connector. The COG driver is fully implemented with a gate driver, source driver, a partial charge pump circuitry and In/Out (I/O) for activation and deactivation of the display.

5.6.2 TI EPD BoosterPack (extension kit)

An extension board made by Texas Instruments (TI) is used to support the EPD panel with necessary sub-circuitry. The extension board mainly consist of a $256Kbit$ serial RAM, $8Mbit$ serial flash, a temperature sensor, an LDO voltage regulator and passive components related to the charge pump circuitry and COG. The TI EPD BoosterPack features open documentation for the PDI EPD panel. See Appendix B for a full schematic.

5.6.3 Arduino Mega 2560

An Arduino Mega 2560 is used to upload images to the frame buffer and control the display. The Arduino Mega 2560 is based on the Atmel ATmega2560 8-bit microcontroller. It has a variety of digital I/O pins which can be configured for Pulse Width Modulation (PWM) and serial communication with support for SPI and I^2C, as well as analog inputs for sensors etc. It runs at $16MHz$ clock frequency and has $256KB$ Flash memory, $8KB$ SRAM and $4KB$ EEPROM available[60]. Instead of traditional C-code microcontroller programming, Arduino is based on the object oriented programming language $C++$. The huge open source community for Arduino and pre-defined libraries makes it less time consuming to prototype embedded systems, compared to setting up an alternative microcontroller circuitry from scratch.

The Arduino has six sleep modes with varying degree of power saving potential. The sleep mode with highest power saving is the "Power down" sleep mode. When active, the AtMega2560 consume around 10mA at 8MHz and 5V, while the "Power down" sleep mode is typically below 10μA at 5V[61]. The General Purpose In/Out (GPIO)-pins at the Arduino is limited to source a current of maximum 20mA, while the power pins can source a current of 50mA[61].

Chapter 6

Low Power EPD Module Design Methodology

This chapter will focus on two separate paths for designing a low power EPD module. First, a theoretical power analysis for each EPD sub-module is performed. Then a small sized Commercial Of The Shelf (COTS) EPD panel with existing driving circuitry will be analyzed. By monitoring the power consumption and comparing different updating techniques, stage times and images for the display, trade-offs and power saving optimizations on a higher abstraction level will be highlighted. Design considerations from physical measurements together with theoretical analysis and evaluation then leads to further focus areas for designing a new low power EPD driving circuitry.

In order to make reasonable decisions regarding design of a low power EPD module, it can be useful to find relevant information by studying available hardware and to get hands-on experience with existing solutions. The idea behind analysing the COTS hardware is to find potential optimizations that can be implemented in software/firmware on a higher abstraction level. With basis in the previous work presented in Table 5.1 on page 39, it is interesting to see how different image updates on a small size display relates the power consumption. By comparing the previous image with the new one, smarter algorithms with partial updating techniques can potentially be implemented in order to reduce both switching time and number of transitions to save power.

It is also possible to visually see the consequences of ghosting effect by reducing the stage time and find trade-offs between acceptable ghosting and minimum power

consumption. If the conventional four-stage display update as shown in Figure 2.6 on page 14 can be avoided, shorter updating time will result in overall lower energy consumption. A benefit of doing measurements on physical hardware is that current-measurements can be related to the code to debug what parts of the circuit that consume most power in practice.

6.1 Theoretical power analysis

In order to design a complete low power EPD module for small size displays, it is important to get a full overview of each required sub-module and break them down into smaller sub-circuits to get an understanding of their basic functionality. Trade-offs can then be highlighted and used to propose specific power reduction techniques. This section will address hypotheses and a theoretical power analysis for each sub-module that will be used as a basis for further design.

Based on Figure 5.2 on page 40, it is interesting to see how these results relates to a smaller display size. Clearly the largest issues regarding power consumption in previous studied EPD driving circuits are related to the source driver and DC/DC-converter. A power analysis is made focusing on the main display driver sub-circuits. By analyzing what parts of each sub-circuit that represents the largest power dissipation, power reduction techniques can be customized for a new low power EPD driving circuitry design.

The power analysis in this thesis is based on monochrome black and white images only. Although gray-levels are achievable in EPDs, power analysis including gray-levels are far more complex. However, the power consumption is expected to be largest for black and white images without gray-levels. If traditional EPD grayscale techniques, as presented in Subsection 2.3.2 on page 12, is used, the voltage transitions for gray-level pixels are scaled to be lower than typically required for best optical black or white pixels. If the spatial dithering grayscale method as shown in Figure 2.4 on page 13 is used, the analysis for monochrome display will be valid if every subpixels are taken into account. Considering color EPDs with RGB-pixels, the number of source lines are tripled, and hence the power consumption is expected to be approximately three times larger than an equivalent monochrome EPD[11].

6.1.1 Overall design considerations

By looking at trade-offs for the EPD module, the voltage supply is the parameter with most significance on EPD power consumption and is therefore natural to look at first. Ideally, the response time of the display should be as fast as possible, while the supplied voltage should be as low as possible in order to consume the least power. As described in Subsection 2.3.1 on page 10, the voltage and response time are closely related to each other. The response time will get slower when the voltage decreases. In this thesis, the physical parameters of the EPD cell are considered as fixed. The focus on power reduction techniques will therefore be limited to the driving circuitry. Otherwise it would also be possible to decrease the response time by reducing the sizes of the microcapsules in the EPD cell or increase the mobility of the charged particles.

In cases where low power consumption is a higher priority than fast response time, the response time can be traded off by lowering the driving voltages to the EPD cells. Figure 6.1 shows a simple model of one pixel circuit in an active matrix EPD. The model was made to get a circuit representation of the EPD pixel and to isolate the driving voltages into separate voltage sources. Here, the EPD cell (referred to Figure 2.1 on page 9) can be modelled as a resistor with a very high resistance in the range of giga-ohms, since there are no expected current flowing between the top and bottom electrode except from a small leakage current as shown in Table 5.4 on page 42. V_{COM} represents the common top electrode voltage, V_G is the gate voltage and V_S is the source voltage at the bottom electrodes.

Although lower voltages traditionally result in lower power consumption, there are limits to how low the voltages can be in the EPD driving circuitry. Theoretically, the EPD cells can be driven at voltages down to $5V$ at the cost of poorer optical reflectance or longer pulse lengths as shown in Figure 2.3 on page 12. As the graph shows, voltages below $5V$ will not be able to saturate at the best possible optical reflectance with EPDs available today. Driving the EPD cells at a voltage of $5V$ will typically result in a contrast/reflectivity of $60 - 80\%$ of the full performance achieved at $15V$.

If an active matrix addressing display is used, it is important to remember that the characteristics of TFTs are related to higher voltages than what is normal for traditional bulk CMOS processes. Due to low mobility and high threshold voltages as described in Subsection 3.1.1 on page 17, the TFTs require a gate

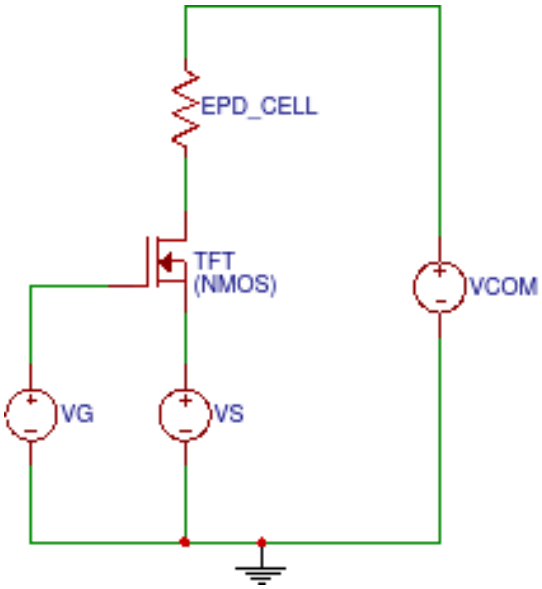


FIGURE 6.1: A simple model of an EPD pixel circuit

voltage around $5V$ higher than the source voltages to be able to operate in the correct region. This means that even if the EPD cells are driven at $\pm 5V$, the TFT gates typically require a voltage of around $\pm 10V$.

The driving circuitry for a segmented EPD can be made simpler than an active matrix display, because the electrodes can be driven directly without the need for TFTs. If a segmented EPD can fulfill the requirements for a product to show necessary content, it should be considered since it has the potential for less circuit complexity and lower power consumption than achievable in high information content active matrix EPDs. However, if the EPD-product shall be able to show a large variety of images and messages, active matrix and use of TFTs are a necessity. As described in section 3.1 on page 16, passive matrix is not a good alternative for electrical addressing of EPDs.

By using active matrix EPDs, reducing the current consumption in sub-modules such as the DC/DC converter, timing controller and gate/source drivers become a more fundamental objective for the overall power consumption.

6.1.2 EPD power

The expected current load for the EPD panel can be interesting to know for further design considerations. By estimating how much current the EPD panel draws, it will be easier to see the significance of the driving circuitry power consumption

when measurements on the physical hardware is performed.

A segmented E-ink EPD is known to consume around $0.5\mu A/cm^2$ when the image is updating[62]. If we assume that the EPD panel will have similar attributes as the simulated EPD presented in Table 5.3 on page 41, another approximation of the current consumption can be made. Since each subpixel consist of six microcapsules with a diameter of $50\mu m$, the total surface area of the subpixel will be approximate $6 * (50\mu m)^2 = 0.015mm^2$. Using Ohm´s law from Equation (4.4) on page 33, the current consumption for each subpixel are approximated to be 0.216nA when the display is updating. The current consumption per area can therefore be calculated to be $0.000216\mu A/0.00015cm^2 = 1.44\mu A/cm^2$. By using the calculated value together with information from E-ink, the estimated current consumption for the EPD panel will be in the range of 0.5 to $1.5\mu A/cm^2$ when the image is updating. This current consumption is related to the bare EPD cell as shown in Figure 2.1 on page 9.

The TFT array and storage-capacitors used in an active matrix EPD panel will result in an additional leakage current dependent on the TFT process that is used. However, the expected leakage current will be very small compared to the switching current. Considering a small size EPD panel, the EPD power is expected to be negligible compared to its driving circuitry power.

Since the physical parameters of the EPD cell are considered as fixed, the only parameters that can be changed to reduce the current through the TFTs, are to reduce the driving voltages V_{gs} and V_{ds}. If the driving voltage is reduced in an active matrix display, the drain-source current through all the TFTs will decrease (referred to Equation (3.1) on page 18). The ON-resistance of the TFTs between the source and the gate can be expressed as Equation (6.1)[25] and we can see that the conductivity will decrease when the overdrive voltage $(V_{gs} - V_{th})$ is decreased.

$$R_{ON} = \left(\frac{\partial I_{ds}}{\partial V_{ds}}\right)^{-1} = \frac{1}{\mu C_{OX}\frac{W}{L}(V_{gs} - V_{th})} \tag{6.1}$$

From Equations (4.2) and (4.3) on page 32 we know that the static power consumption related to the TFTs will decrease proportionally with the voltage reduction, while the dynamic power consumption will have an quadratic reduction related to the decrease in voltage.

6.1.3 Source driver power

The source driver is normally considered as a complex building block consisting of sub-circuits with both digital and analog parts. An EPD source driver can be made fully digital since the driving voltages can be held at a fixed voltage potential. Instead of precisely driving analog output voltages, it is the duration of the driving voltages that typically will control the pixel values. However, it is normal so separate the low voltage from the high voltage circuit. For the rest of this thesis the high voltage parts related to driving will be considered as the analog part, while the low voltage control circuitry will be considered as the digital part.

Since the source driver is related to pixel-data, the switching activity is dependent on the image pattern as described in Section 5.2 on page 38. The high driving voltage in EPDs is a factor that will increase both the static and dynamic power in accordance with the switching activity. Power dissipation in a conventional source driver has several contributors, some more significant than others.

6.1.3.1 Source driver power - digital part

The digital part of the source driver is mainly represented by shift-registers and latches. The architecture of a shift register, as shown in Figure 3.4a on page 21, is quite simple, but also very area consuming especially for larger display sizes. A typical data flip-flop is twice the size of a data latch due to the extra circuitry required for the clock signal. Therefore, delay and power consumption in flip-flops are higher compared to latches. Since it is required an N-bit shift register for a display with N columns, there will typically be N flip-flops and 2N latches in a traditional source driver. Every single logic gate carries a static and dynamic power consumption as described in Section 4.1 on page 31. The power dissipated by a shift register is proportional to the clock scan frequency and its total capacitance. Traditionally, this power dissipation is reduced by adopting multi-phase drive clock strategy[25]. For instance, if a two-phase clock is used, the total power consumption in the shift register is theoretically reduced by a factor of 2, since the clock drives an equivalent capacitance of $C/2$ at a frequency $f/2$.

The digital part of the source driver power consumption is hence very dependent on the display size and resolution. However, since the digital part of the source driver

typically is related to smaller voltages, it is expected to be negligible compared to the high voltage analog part. For a typical LCD source driver, the digital part represents less than 10% of its total power dissipation[25]. An EPD source driver is expected to have a similar power distribution. The digital part of small size display source drivers will naturally be less of a problem compared to larger display sizes because of less circuitry is required with respect to flip-flops and latches.

6.1.3.2 Source driver power - analog part

The analog part of the source driver is the part that is related to the high voltage driving at the source lines. This is expected to be the relevant contributor on power dissipation. Even though a static power related to leakage is present in the high voltage transistors, the most significant power dissipation in the analog part of the source driver comes from the dynamic power. Cross-conduction current in the level-shifter circuitry, as shown in Figure 3.5 on page 21, results in short-circuit power loss when the transistors changes their logic state[25]. Although this cross-conduction current only takes place in a short fraction of the clock cycle, the current can be quite large since the voltage is high and only the ON-resistance (as described in Equation (6.1) on page 49) in the transistors limits its magnitude[25].

The most significant power consumption at an EPD source driver is expected to be related to charging and discharging capacitive outputs. As described in Section 5.2 on page 38, the power consumption in the source driver is highly dependent on the written image since the capacitive component only consume energy when the voltages changes. Therefore, the less changes there are in the pixel-data between two images, the less power is consumed by the source driver. Since the display usually is written one row at a time, it is the vertically adjacent pixel changes that matter the most.

6.1.4 Gate driver power

The gate driver also consist of a digital and analog part. The digital part of the gate driver is basically just a shift register as shown in Figure 3.4, where N is equal to the number of display rows. The gate driver is the sub-circuit related to the highest voltages in the driving circuitry. Since the TFTs are operated as switches ($V_{ds} \leq V_{gs} - V_{th}$), the TFT gates will require a high gate-source voltage. However,

the gate driver has no load other than a small capacitive parasitic related to the transistor gates. The power consumption will hence be much lower than what is expected for the source driver. The isolation layer between the gate and channel (gate oxide) causes a high input resistance in TFTs as compared to traditional MOSFETs. Therefore, there will be no real current associated with the transistor gate, except from a small gate leakage current as described in Chapter 4.

The gate leakage typically increase exponentially as the oxide thickness is reduced. Therefore, the TFT process play an important role on the gate leakage. However, the gate leakage in TFTs are several orders of magnitude lower than the power consumption related to other sub-modules in the driving circuitry as shown in Figure 5.2 on page 40.

By reducing the driving voltage, both static and dynamic power in the gate driver will decrease. Since the voltage in the gate driver also is scaled according to the other sub-modules in the driving circuit, the power consumption in all sub-modules will decrease when the voltage is reduced. The gate driver power will hence be negligible.

Designing a gate-driver that only activates the specific rows that require an update from the previous image will however result in a lower total power consumption. This is because unnecessary activity and stage times related to the source driver is reduced.

6.1.5 Charge pump power

If we take a look at the Dickson charge pump shown in Figure 3.9 on page 25, we can see that the maximum current capability of the circuit is determined by the circuit design with trade-offs between pump clock frequency, coupling capacitance sizes and pump clock amplitude. For most charge pumps, the pump clock amplitude is usually equal to the input voltage for less circuit complexity. Therefore, the two main trade-offs related to charge pump designs are clock frequency and capacitor sizes. The larger the coupling capacitances are, the longer it takes to charge and discharge the capacitors. The charge pump is most efficient at lower frequencies due to cross conduction losses in the transistors as described in Subsection 4.1.2 on page 32. When clock frequencies are reduced, the capacitances must be scaled up accordingly in order to achieve the same required current capability.

It should be noted that using diodes as shown in the Dickson charge pump from Figure 3.9, the threshold voltages of the diodes also need to be considered in the design. Often low voltage implementations of charge pumps use switches instead of diodes as it allow us to avoid the threshold voltages of the diodes[63].

Power losses in charge pumps mainly arise from capacitor charging and discharging losses, resistive conduction losses, and losses due to parasitic capacitances and short-circuit currents[44]. The output voltage of an N stage charge pump with ideal diodes or switches can be modelled as Equation (6.2)[63]

$$V_{out} = (N+1)V_{in} - \frac{NI_L}{fC} \tag{6.2}$$

where f is the clock frequency and I_L is the load current. The current consumption of the charge pump can be modelled as Equation (6.3)[63]

$$I_{power} = (N+1)I_L + I_{nl} \tag{6.3}$$

where I_{nl} represents the non-idealities related to the power losses described above. We can see that the power consumption of the charge pump circuit is highly related to the number of pump stages, N. In order to minimize the power consumption of the charge pump circuit, the current in Equation (6.3) should be minimized. The first step is normally to find the optimum number of stages which can be calculated using Equation (6.4)[63]

$$N_{op} = \left(1 + \sqrt{\frac{\alpha}{1+\alpha}}\right)\left(\frac{V_{out}}{V_{in}} - 1\right) \tag{6.4}$$

where $\alpha = C_p/C$. α is a technology dependant number between 0 and 1 where the most ideal case is when $C_p << C$ and α is close to zero. By using Equation (6.2) together with the optimum number of stages calculated in Equation (6.4), the optimum capacitor sizes for minimized power consumption can be calculated. If clock frequency is increased, the capacitor values can be reduced to achieve the required output voltage, but at the expense of reduced efficiency.

If we consider an input voltage of $V_{in} = 3V$, we can see that an optimum number of pump stages using Equation (6.4) is 8 stages, if the output voltage shall be pumped up to $V_{out} = 20V$ to drive the TFT gates and assumed $\alpha \approx 0.2$. This result in

an approximate charge pump current consumption of $9 \times I_L$ if we neglect non-idealities. Now, if Equation (6.2) is rearranged to calculate required capacitances, we find out that the pumping capacitors need to be in the order of $130pF$ if we assume $I_L = 1mA$ and $f = 10MHz$. This leads to a total capacitance of $1040pF$, which is considered as relatively high for capacitors integrated in a low power chip, depending on the process that is used. It should be noted that this calculation is just a ballpark figure, since non-idealites of course needs to be accounted for when designing the physical circuit and both area and current consumption will be increased.

6.1.6 Timing control power

The timing control can play an important role on the total energy consumption. Although a timing controller usually is associated with low voltage, fully digital circuits, it is responsible of generating the waveforms that controls the more power hungry blocks such as the source driver. By designing a driving waveform that consider how to efficiently activate the charged particles and drive the display in as few stages and time period as possible, the total energy consumption can be drastically reduced.

In the previous work, two different driving waveforms were introduced (referred to Figure 5.3 on page 43). As an alternative to the traditional bipolar driving waveform presented in Figure 3.10 on page 27, the unipolar driving waveform as shown in Figure 6.2 can be used. By dynamically change the V_{COM}, (referred to Figure 6.1 on page 48), with the opposite polarity of V_S, the voltage difference between the top electrode and bottom electrode at the EPD cell will become twice as much of what is obtained when V_{COM} is fixed at $0V$. Using a unipolar driving waveform opens up some new possibilities for lower energy consumption.

If a driving voltage of $\pm 15V$ is used, the effective electric field become $30V$ and the particle transition will speed up (referred to equations presented in Subsection 2.3.1 on page 10). Hence the unipolar driving waveform will improve the response time with a factor of 2. For e-reader applications and large size EPDs, the biggest gain in using a unipolar waveform is to reduce image updating time, ghosting effects and flicker. Therefore, previous work as presented in Kao2009[22] (referred to Section 5.5 on page 42) only focus on the aspects of improving the response time by using a unipolar waveform.

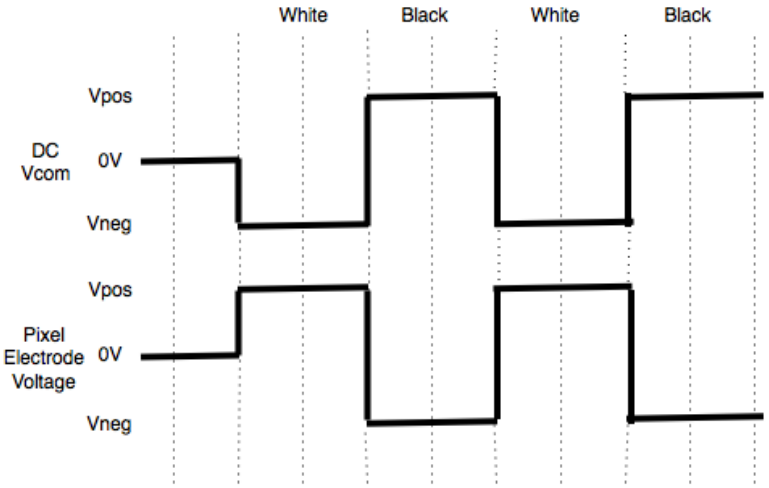


FIGURE 6.2: Unipolar driving waveform for EPDs[22]

Since this thesis focus on small size EPDs and low power consumption, another interesting aspect regarding the unipolar driving scheme can be considered in the design process. The voltage can potentially be reduced to half of what is used in a bipolar driving waveform and still have the same optical performance and response time. In cases where the display only shall have an occasional update and a driving voltage of $5V$ is sufficient, the driving voltage can theoretically be reduced to $\pm 2.5V$ with a unipolar waveform. This will have a huge impact on the total power consumption since voltage has a quadratic relationship on the dynamic power (referred to Chapter 4). Circuit complexity regarding high voltage processes and current capability in the DC/DC converter will also be reduced when less charge pump stages is required.

The driving algorithm controlled by the timing controller is important for how the pixel data is processed. If smarter algorithms that consider how to update images with the least possible voltage transitions are implemented, the dynamic source driver power consumption will be reduced.

6.1.7 Peripheral circuit power

In order to reduce the current consumption in peripheral circuits, a trade-off between energy consumption and area must often be met. Since most of the peripheral circuits such as memory, MCUs and communication interface is based on digital logic, many of the power reduction techniques as mentioned in Chapter 4 can potentially be used in the implementation. This thesis will not focus on

specific hardware designs for peripheral architectures, but a few considerations should be taken into account, in order to minimize the total power consumption.

MCU: The chosen MCU should first and foremost provide a low power active mode. While the AtMega2560 is expected to consume around 10mA at 8MHz, there are other alternatives on the market that consume a lot less in comparison. Sleep-modes should be actively used to turn off parts of the circuit that is not in use. The clock frequency should also be dynamically decreased to a minimum of what is required to to not introducing a large delay in image updating time. If the MCU is integrated with internal RAM and Direct Memory Access (DMA), this will often result in the lowest possible power consumption.

Communication interface: By comparing the two communication interfaces introduced in Section 3.6 on page 27, the power consumption will be traded off with circuit area. SPI has typically lower power requirements than I^2C due to less circuitry required. Slaves use the master´s clock and does not need precision oscillators nor a unique address like I^2C. SPI has also higher throughput, but it requires more pins available than I^2C.

Memory: The chosen memory should preferably be a low leakage non-volatile memory where data can be retained without power. The write speeds should be as fast as possible and the average active power as small as possible. The Ferroelectric Random Access Memory (FRAM) is a technology that is considered as promising for ultra low power consumption and energy harvesting products[64].

Temperature sensor: Since the temperature sensor primarily is used for compensating the response time with temperature, this will directly impact the energy consumption as the response time will get slower at lower temperatures. It is therefore important that the temperature factor set from the sensor is as close to the practical EPD response time (referred to Figure 3.13 on page 29). If the EPD module is operated at slower response time than required to drive the pixels, energy will go to waste.

6.1.8 Summary of the theoretical power analysis for small size EPDs

Following is a short summary of the most important findings in the theoretical power analysis for small size EPDs and its driving circuitry:

- The power analysis is made for monochrome black and white images only. It is expected that the total energy consumption for gray-level addressing will be less, since it require less updating time than a fully white or black pixel write. If extra sub-pixels are used for gray-level (spatial dithering) or color (RGB), the power analysis is valid if all sub-pixels are taken into consideration.

- Voltage is the parameter with most significance to the driving circuitry. Increase voltage with a factor of 2 and response time improves with a factor of 2. Decrease voltage with a factor of 2 and static power consumption decrease with a factor of 2, while dynamic power consumption decrease with a factor of 4. Hence, the driving voltages should be as low as possible to consume the least energy.

- The minimum required driving voltage for today´s EPDs is 5V. This will typically result in 60-80% of the optical performance achieved at 15V driving.

- Expected current draw for EPD-panels is 0.5 to $1.5\mu A/cm^2$. This is much lower than the expected current draw for its driving circuitry.

- The source driver is divided into an analog and a digital part. The analog part is expected to consume around 90% of its total power.

- The gate driver is also divided into an analog and a digital part. The only expected current draw for the analog part is due to gate leakage in the TFTs, hence the gate driver power consumption will be negligible compared to the other sub-modules. A multiphase clock scheme can be used to reduce the power consumption of the shift register in the digital part.

- The charge pump power consumption is very dependent on the required pumping voltage and current capability. A rule of thumb is the less pump stages required, the less power is consumed.

- The timing controller can play an important role on the total energy consumption. By using smarter driving waveforms the total image updating time or driving voltage can be reduced. By using a unipolar driving waveform, either the image updating time or voltage can potentially be halved and still have the same optical performance.

- In peripheral units, energy consumption is often traded off with circuit area. By using MCUs and memory with low active power consumption an important foundation is laid. SPI can be used as a low power communication interface. The temperature factor set from the temperature sensor should preferably be as close as possible to the practical response time of the EPD cells to reduce the energy consumption to a minimum.

6.2 Practical power analysis

This section will describe the practical part of the EPD analysis. It will show how the COTS hardware is tested and the results from the various measurements are discussed. The chosen COTS hardware is used to find out the following:
1. How does the written image impact on the power consumption for small sized EPDs? Compare worst case image versus best case image.
2. In what range are the driving voltages for that specific EPD module? Does it correspond with the expected values?
3. How long does it take to update the image with a traditional four-stage image update?
4. What is the current consumption related to circuit activity? Analyze what sub-circuits that require the most energy.
5. Comparison of the current consumption in the display driver IC and the surrounding discrete electronics. How significant is the discrete components on the Printed Circuit board (PCB) related to the total power consumption?
6. Test different stage times to see visual consequences on ghosting effect. What is the absolute minimum stage time in order to avoid a significant ghosting effect?
7. Compare different image updating techniques and stage times to find trade-offs between optimal image quality and short updating time.

In order to measure current consumption with various images and stage times, a

test setup was made for the COTS hardware. With basis in predefined libraries and Arduino sketches found at RePaper[58], the EPD panel and driving circuitry could be controlled from the Arduino code and serial monitor. First, test images was made using the 1-bit X BitMap (XBM) format[65]. The image data is encoded as a comma-separated list of byte-values represented in C hexadecimal notation as shown in Listing 6.1. Here, a $0x00$ is one byte of zeroes which translates to eight black pixels in a row. $0xff$ is a byte of ones, which give eight white pixels in a row.

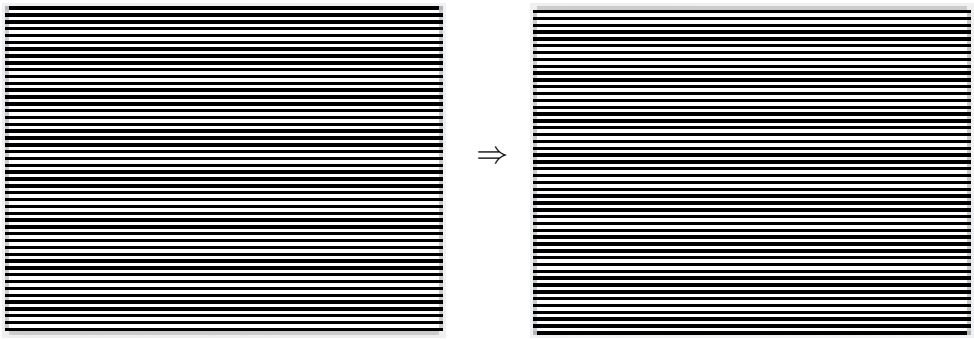
```
#define TEST_1_44_width 128
#define TEST_1_44_height 96
static unsigned char TEST_1_44_bits[] = {
   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
   0x00, 0x00, 0x00, 0x00, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
   ...};
```

Listing 6.1: A section of a 1-bit XBM format image frame

Figure 6.3 shows a representation of the worst case image. According to the voltage transition matrix in Table 5.1 on page 39, this image pattern with alternating black and white horizontal lines will have the largest power loss. As described in Subsection 2.3.3 and Figure 2.6 on page 14, inverting the images is a often used technique to neutralize the electric field and avoid ghosting. It is therefore interesting to see the negative effects of not inverting the image in an image refresh, in order to find a trade-off between less power loss at the source lines and less total updating time required.

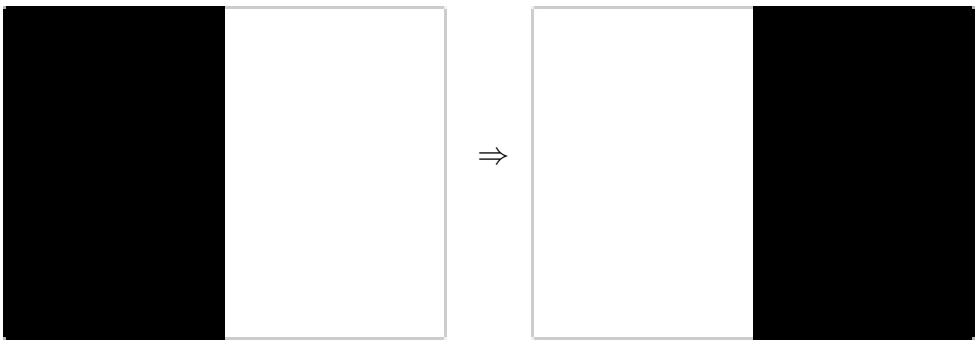
Figure 6.4 on the other hand, represent an image with the fewest possible voltage transitions and is considered as a best case image pattern regarding power loss at the source lines when the image is inverted. As described in Section 5.2 on page 38, it is the vertically adjacent pixel changes that is related to the largest power consumption.

A simple serial port driven control system was used to upload images to flash memory and display the images on the EPD panel. An additional function for writing pixel by pixel or line by line in desired B/W colors was also set up in order for a partial update scheme. This was set up using Adafruit GFX Graphics Library[66], which is an Arduino $C++$ library that provides a common syntax and graphic functions adapted for most LCD and OLED displays.



(A) Test image 1 (B) Test image 1 inverted

FIGURE 6.3: Worst case image refresh



(A) Test image 2 (B) Test image 2 inverted

FIGURE 6.4: Best case image refresh

6.2.1 Test setup

Figure 6.5 shows a picture of the extension kit hardware together with the PDI Aurora Mb EPD panel. The picture highlight the most important components and placements related to the driving circuitry. It can be noted that a substantial part of the circuit area is used on bulky off-chip capacitors for the charge pump in the COG. The default stage time for the tested EPD kit is set to be 480ms and an internal clock divider is used to reduce the Arduino clock frequency from 16MHz to 8MHz.

Before measuring the current consumption, it would be interesting to see what kind of voltages that are generated from the charge pump at the source lines V_{DH} and V_{DL}, as well as the gate voltages V_{GH} and V_{GL} (referred to Appendix B). Regarding the common voltage V_{COM}, is also interesting to find out if it is fixed at a voltage close to zero. Here, V_{DH} and V_{DL} is equivalent to the positive and negative output voltage of the source driver (VS) as modelled in Figure 6.1, while V_{GH} and V_{GL} is equivalent to the positive and negative output voltage of the gate driver

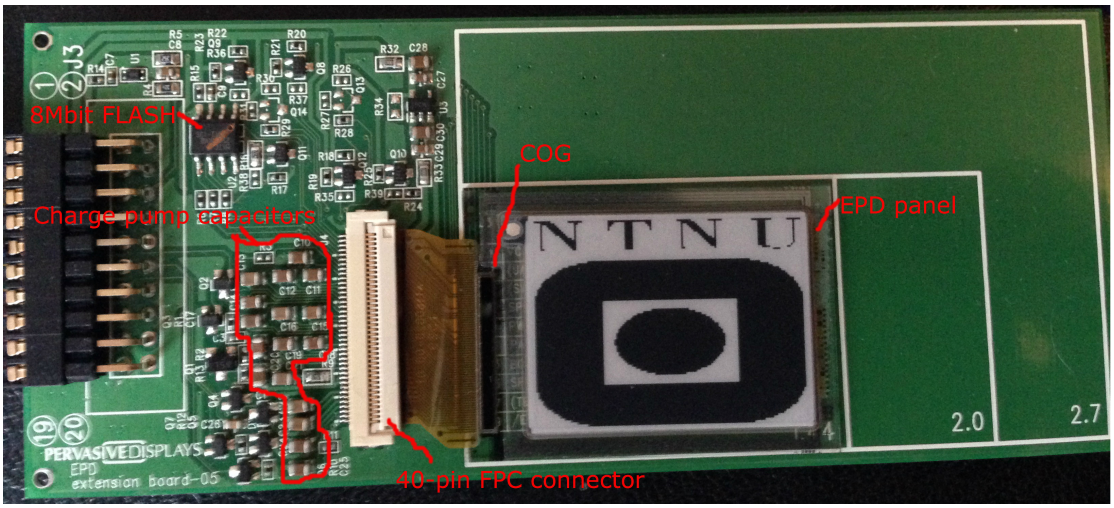


FIGURE 6.5: Picture of the EPD panel and extension kit

(VG). Voltages at the input of the driving circuitry in the TI Boosterpack (V_{in}) and source driver in the COG (V_{CC}/V_{DD}) should also be measured to calculate the total power and energy consumption.

Since most of these voltages just appears for a short time period, the voltage measurement was performed using an analog input pin at the Arduino. By dimensioning a three-way voltage divider for a potential voltage difference of $\pm 25V$, the internal ADC in the Arduino referenced to $5V$ could be used. Figure 6.6 shows the voltage divider circuit designed to be able to measure voltages between $\pm 25V$, scaled to a reference voltage between $0V - 5V$. Using the nodal voltage method, Equation (6.5) for the output voltage was derived to find appropriate resistor values.

$$\frac{V_{out} - V1}{R1} + \frac{V_{out} - V2}{R3} + \frac{V_{out}}{R2} = 0 \tag{6.5}$$

With $V2$ limited to voltages between $\pm 25V$, $V_{out} = 5V$ when $V2 = 5V1$ and $V_{out} = 0V$ when $V2 = -5V1$. From this we can see that $R3$ needs to be $5R1$. With a basis in $R1 = 10k\Omega$, $R2$ was originally calculated to be $12.5k\Omega$ and $R3$ to be $50k\Omega$ and the closest standard resistor values was chosen.

In order to separate power use of the surrounding microcontroller-circuitry from the driving circuitry, the current consumption should preferably be measured directly at the source driver in the COG. The COG on the PDI EPD panel has its own power supply for the analog (V_{CC}) and digital part (V_{DD}) of the source driver.

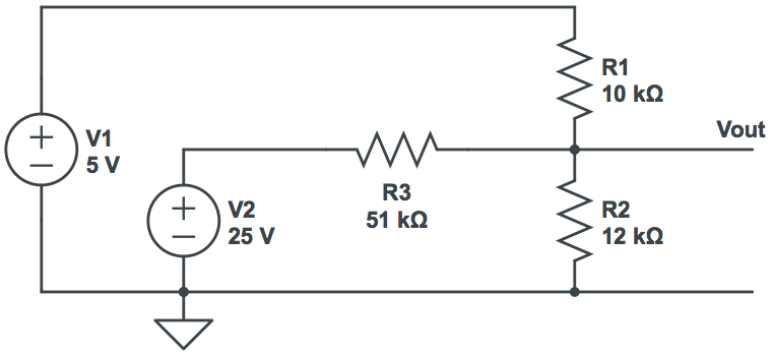


FIGURE 6.6: Three-way voltage divider dimensioned to measure voltages at $\pm 25V$ with an $5V$ resolution ADC

To be able to access pins in the miniature FPC-connector with a current meter or a probe, a breakout kit was made using two FPC-to-Dual In-line Package (DIP)-boards as shown in Figure 6.7 connected together with jumper-wires as shown in Figure 6.8.

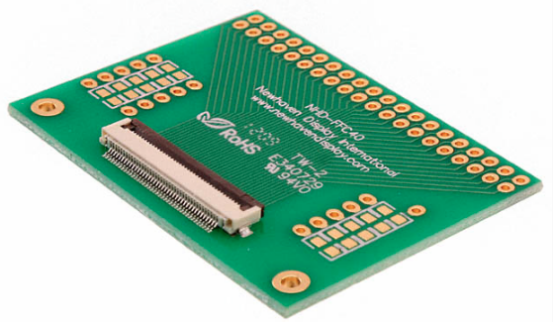


FIGURE 6.7: Newhaven display FPC to DIP board[67]

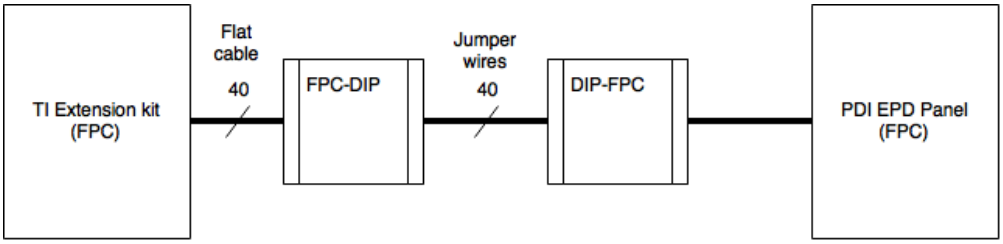


FIGURE 6.8: Breakout kit using two FPC-to-DIP boards and jumper wires

Current consumption was thereafter measured with a μCurrent Gold[68]. A precision operational amplifier and shunt resistors scaled with correct impedance converts current into voltages similar to regular current meters, but with higher precision at lower currents. With the μCurrent Gold scaled to 1mV/100mA, the current consumption could be measured with an oscilloscope or with a voltage divider circuit and an analog input on the Arduino as described above. The complete test setup for current measurement is shown in Figure 6.9.

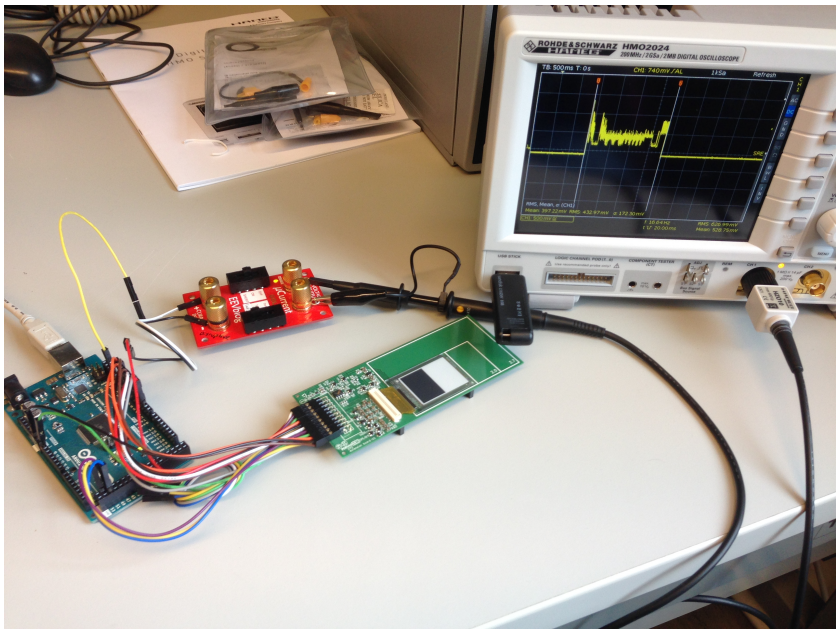


FIGURE 6.9: Test setup current measure

6.2.2 Experimental results

Following is the experimental results together with a discussion forming the basis for the practical analysis.

6.2.2.1 Voltage measure

The voltage measurements during image updates are shown in Table 6.1. The measured voltages are in the range of what was expected from the theory described in previous chapters. It is also noted that voltages are slightly lower at Image 1 updates than Image 2 updates.

TABLE 6.1: Average voltage measurements during an image update, referenced to ground

Test Image	V_{DH}	V_{DL}	V_{GH}	V_{GL}	V_{COM}	V_{in}	$V_{CC/DD}$
Image 1	$13.5V$	$-13.4V$	$19.2V$	$-18.9V$	$-1.2V$	$5V$	$3V$
Image 2	$14.1V$	$-14.1V$	$19.3V$	$-19.1V$	$-1.2V$	$5V$	$3V$

6.2.2.2 Current measure at the COG source driver

By using an oscilloscope, the current at the source driver supply ($I_{SS} \approx I_{CC} + I_{DD}$) was measured with the result as shown in Figure 6.10. Here, the current

consumption equals to approximate $1.8mA$ over a time period of 2.7 seconds. The energy consumed at a four stage image update is therefore approximate 14.6mJ at the source driver. By making a simple voltage divider dimensioned to the output of the μCurrent, an analog input at the Arduino was used to measure the current consumption related to the code. Voltages were sampled at different places in the code and printed into the terminal. The high current spikes shown in Figure 6.10 was found to be related to the power up/power down sequence of the charge pump circuitry, while the long updating time is directly related to the four stage image updating sequence. Here, the highest current spikes are in the range of 13mA, while the EPD panel has a mean current consumption of around 2mA at the source lines, depending on the image that is written.

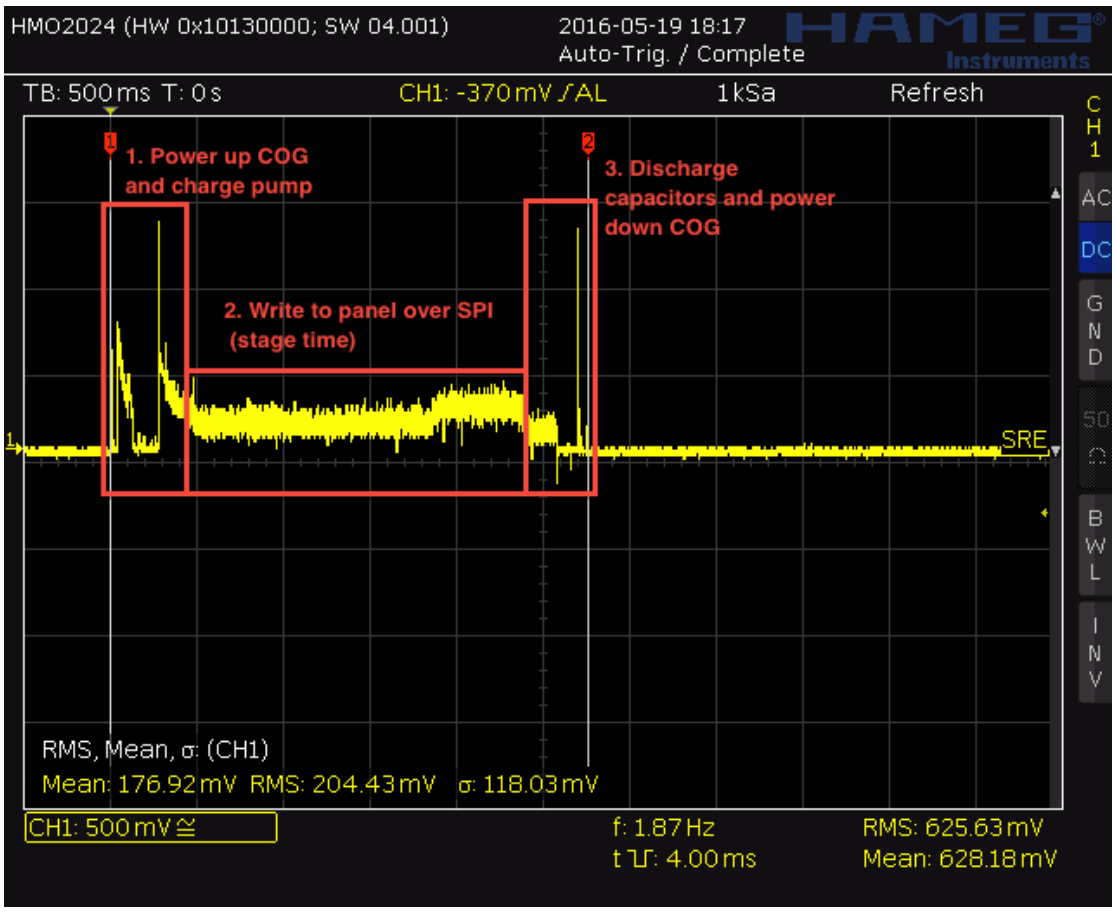


FIGURE 6.10: Current measurement of a four-stage image update at the source driver supply. 1mV=1/100mA

Current measurements for the two test images in both the analog (I_{CC}) and digital (I_{DD}) part of the source driver is shown in Table 6.2. The power consumption at the source driver (P_S) is then calculated. The results show that there is a significant difference between the worst case and best case image update in current

consumption. Since the current consumption is highly dependent on the image pattern, even for small size EPD panels, power can be saved by using images with a low occurrence of alternating vertical black/white pixels. Algorithms can potentially be implemented in software that detects and avoid these kinds of images, or to generate a less power consuming image alternative. However, there are limits to how much an image can be adjusted without a noticeable degradation.

TABLE 6.2: Current and power measure at source driver supply in COG, temp=22°C. Currents shown in mean values from power up to power down of the COG

Test Image	I_{CC}	I_{DD}	$I_{SS} \approx I_{CC} + I_{DD}$	P_S
Image 1	2.30mA	0.14mA	2.39mA	7.17mW
Image 2	1.56mA	0.11mA	1.70mA	5.10mW

Several other images were also tested and the current consumption is in the range between the values shown in Table 6.2. The measurements also confirmed that the analog part of the source driver related to switching at high voltages, constitutes for more than 90% of its total current consumption.

6.2.2.3 Current measure at the TI Boosterpack

Measurements including the discrete components in the TI EPD Boosterpack is shown in Figure 6.11 and Table 6.3. By using a two-stage image update, the current consumption between the worst case image and best case image update was measured for the full EPD driving circuitry. A general purpose in/out (GPIO) pin at the Arduino was used to power the circuit. By enabling the circuit to be powered up prior to update and powered down immediately after update, it was easier to filter out standby currents and measure the most relevant current consumption and updating time related to just the image update. The worst case image update had a mean current consumption of around 4.57mA, which equals to a power consumption of 22.85mW. The best case image update had a mean current and calculated power consumption of respectively 3.97mA and 19.85mW. By comparing these results with the current measurements and calculated power consumption at the source driver supply as shown in Table 6.2, we can see that the discrete components related to the TI EPD Boosterpack consume around 15mW when the image is updating.

It shall be noted that the input voltage is 5V and power is dissipated over the

LDO-regulator that regulate the input voltage down to 3V for the rest of the driving circuitry. By using Equation (3.2) on page 23, and assuming $I_Q << I_{out}$ and $I_{out} \approx I_{in}$, the estimated power loss over the LDO-regulator is around 9mW.

TABLE 6.3: Current measure at input supply in TI Boosterpack, temp=22°C. Currents shown in mean values from power up to power down of the COG

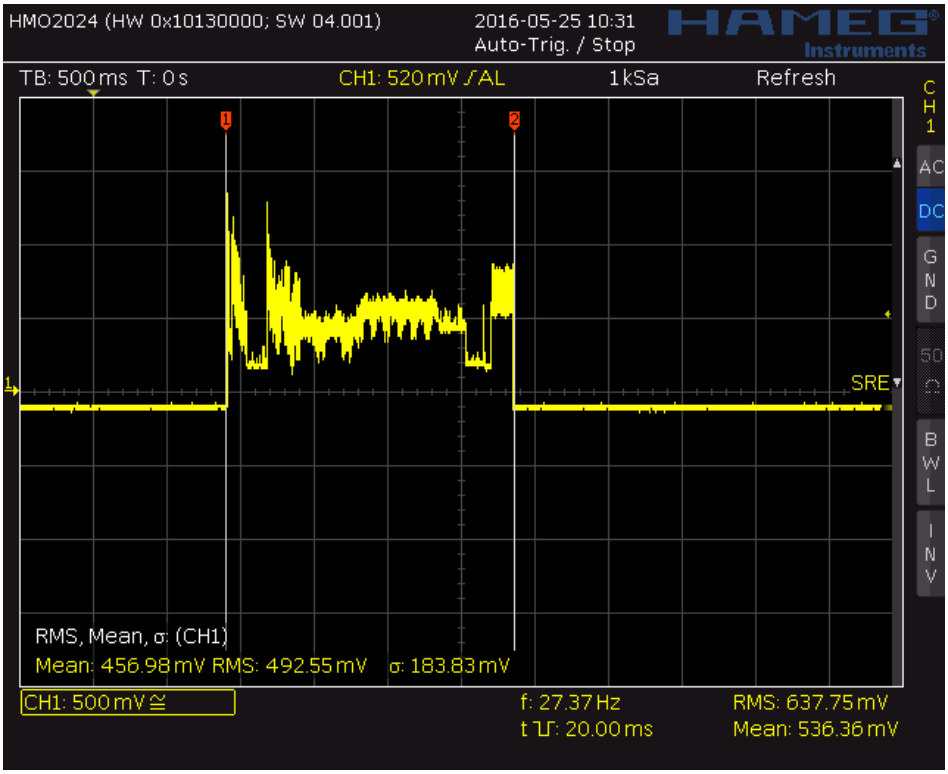
Test Image	I_{in}	P_{in}
Image 1	4.57mA	22.85mW
Image 2	3.97mA	19.85mW

6.2.2.4 Stage time measure and ghosting effect

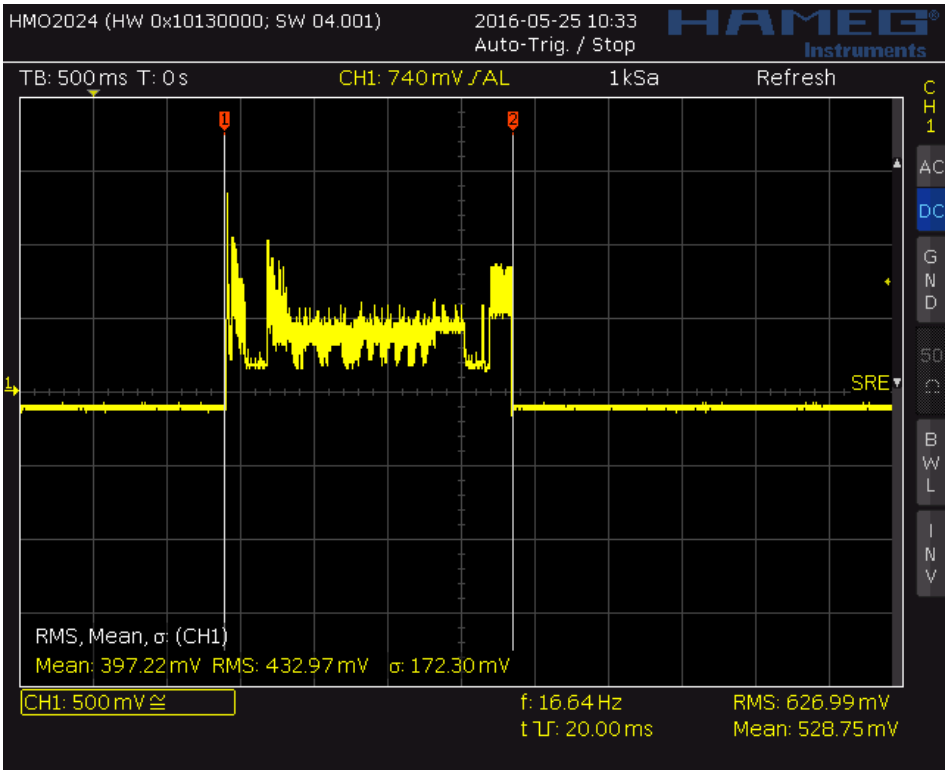
Next, different stage times and image updating techniques were tested. All visual measurements are performed by using two similar EPD-panels and just comparing the images with eyesight. The first thing that was noticed was that the stage time could be reduced to around 200ms without any visually noticeable image degradation or ghosting effect at all. This finding relates to previously tested EPDs presented in Figure 2.3 on page 12, since a 200ms pulse length at 15V is close to saturation in the dynamic range. By further reducing the stage time to around 50ms, the image was starting to get a visible image degradation, where the most noticeable negative effect was a higher level of ghosting effect when trying to clear the display to white. Writing black pixels on a white background with 50ms stage time resulted in slight image degradation where the pixels had a gray-level of around 70% black. Clearing the display back to white took about 3× as long to get rid of all ghosting from the previous image. Figure 6.12 shows a representation of stage times versus experiental image gray-levels.

Figure 6.13 shows the visual effect of a stage time at 480ms versus 50ms. First, Figure 6.13a shows the difference between two image updates where the previous image was all white and a two-stage image updating technique was used. The two-stage image updating technique used, is illustrated in Figure 6.14. In Figure 6.13b, the images are reverted back to white with the same two-stage image updating technique. By comparing the top image with the bottom image, the visual effects of long versus short stage time can be seen.

We can notice the significant visual ghosting effect when trying to clear the display back to white at a 50ms stage time. The left side of the bottom image in Figure 6.13b seem almost more black than white as it is supposed to be. From this we can



(A) Current measure worst case image at 22°C



(B) Current measure best case image at 22°C

FIGURE 6.11: Current consumption EPD panel + TI Boosterpack (1mV=1/100mA)

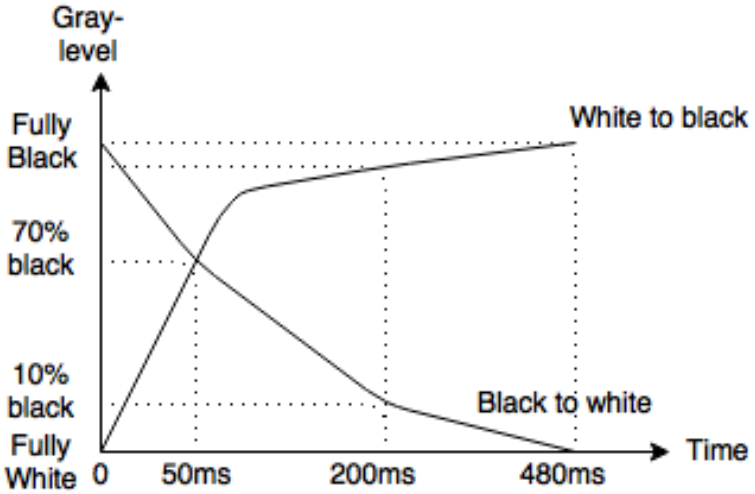
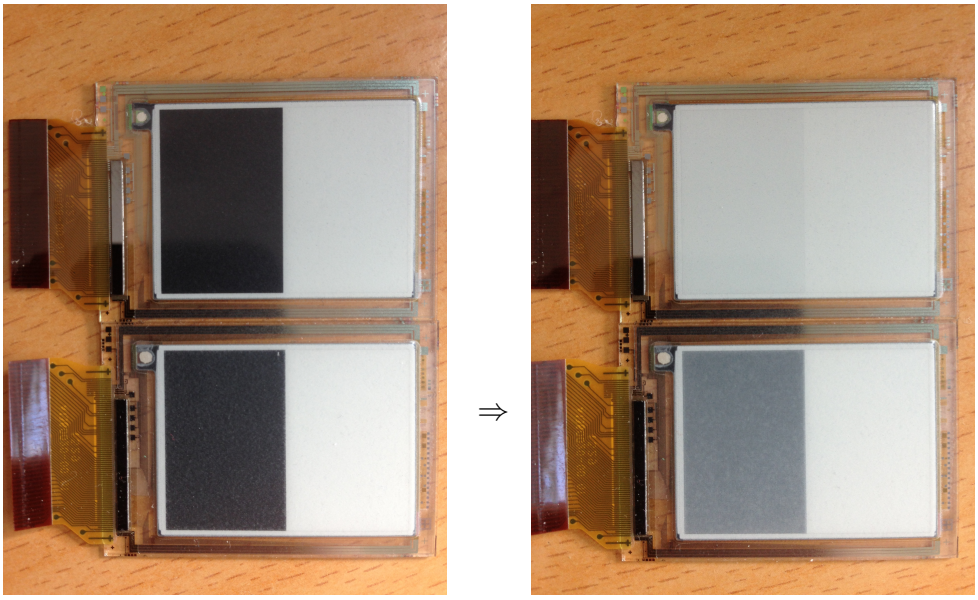


FIGURE 6.12: Stage time vs. gray-level (experiental measure)



(A) Write image (B) Clear to white

FIGURE 6.13: Image update from white at stage times 480ms (top) vs. 50ms (bottom)

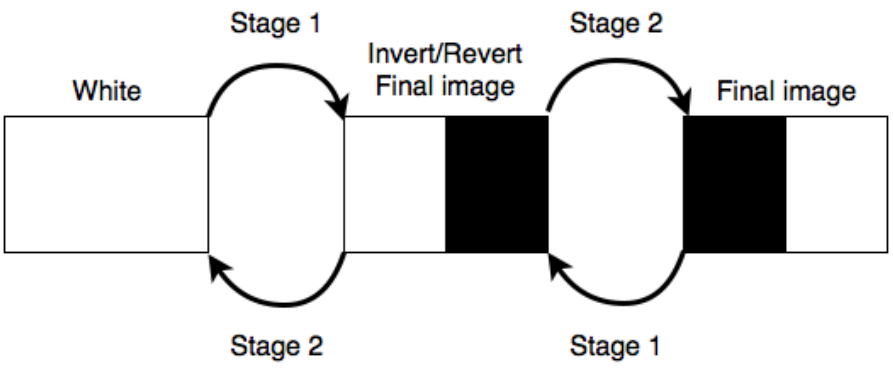


FIGURE 6.14: Two stage image update, white as basis

conclude that if a one-stage image updating technique shall be used, it becomes more important to use a shaking waveform to neutralize the electric field and avoid ghosting. Here, it is required a total stage time around 1 second to clear the display to white without inverting the new image.

The same test was performed with black as basis as shown in Figure 6.15. The results are shown in Figure 6.16.

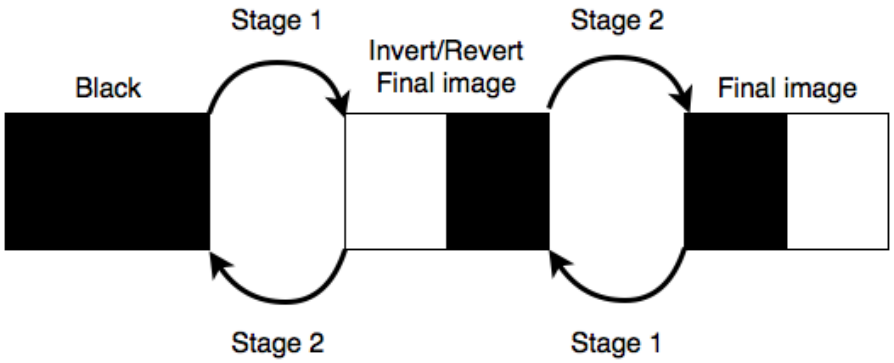
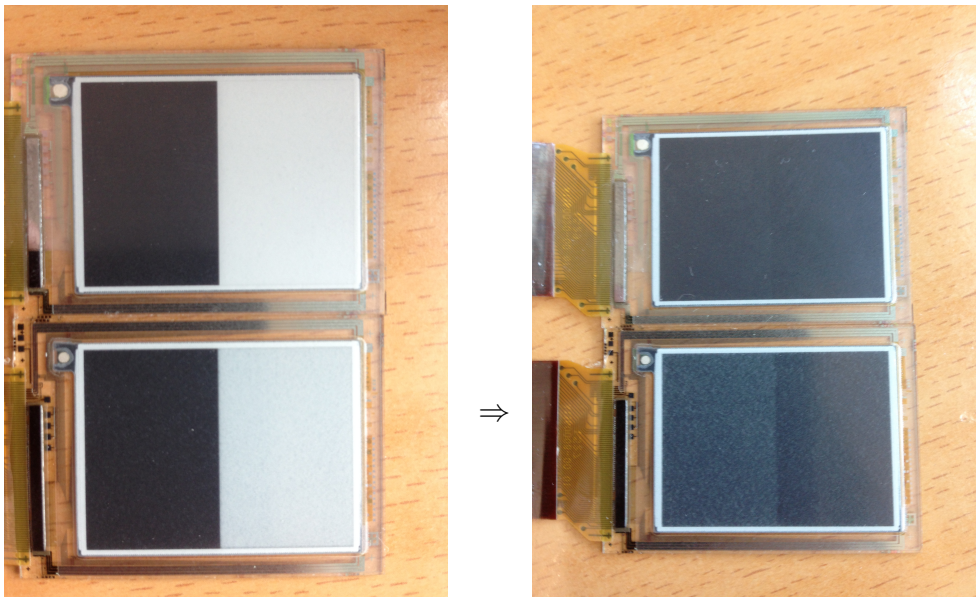


FIGURE 6.15: Two stage image update, black as basis



(A) Write image (B) Clear to black

FIGURE 6.16: Image update from black at stage times 480ms (top) vs. 50ms (bottom)

We can see that the visual effect of ghosting is less when writing from white to black as shown in Figure 6.16b, than writing from black to white as shown in Figure 6.13b. It is also clear that inverting the final image has a better effect on ghosting than reverting the initial image or write an image in one stage.

Instead of reverting the initial image before clearing to white as shown in Figure 6.14, a more traditional image updating technique as shown in Figure 6.17 was tested with the results as shown in Figure 6.18.

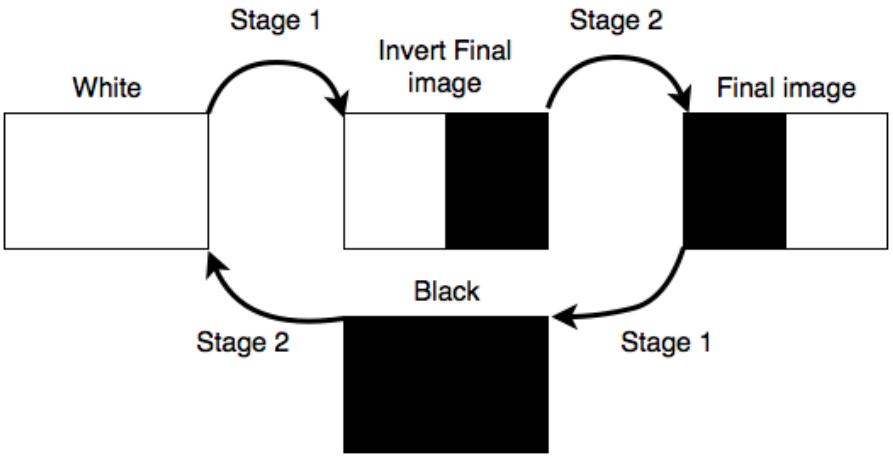
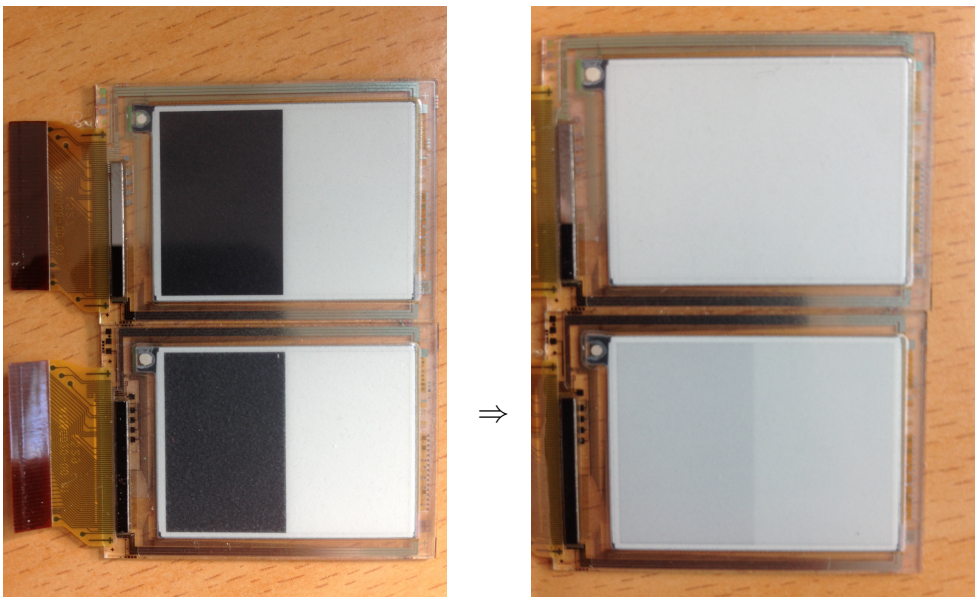


FIGURE 6.17: Two stage image update, white as basis, invert



(A) Write image (B) Clear to black

FIGURE 6.18: Image update from white, inverting at stage times 480ms (top) vs. 50ms (bottom)

Here, it is only required a total stage time around 100ms to clear the display to white with a two-stage image update as shown in Figure6.17. This illustrates that neutralizing the electrical field by inverting images is an efficient way to reduce ghosting and the total stage time. It will be more energy efficient to use a two-stage image update where images are inverted at shorter time period, than writing a one-stage image at a long time period. For comparison, a best case one-stage

image update with a total stage time of 1 second (not inverting), equals to 5.1mJ. A worst case two-stage image update with a total stage time of 100ms (inverting), equals to 0.7mJ.

The same two-stage image update was tested where the initial image was all black as illustrated in Figure 6.19. Figure 6.20 shows the results.

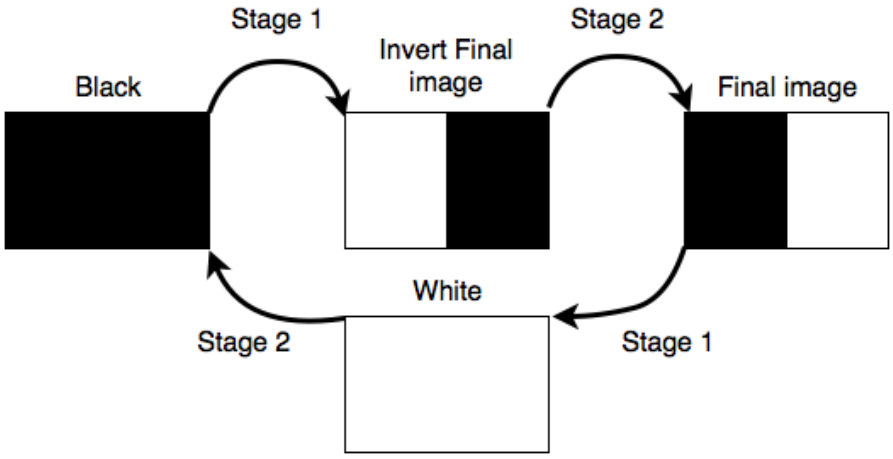
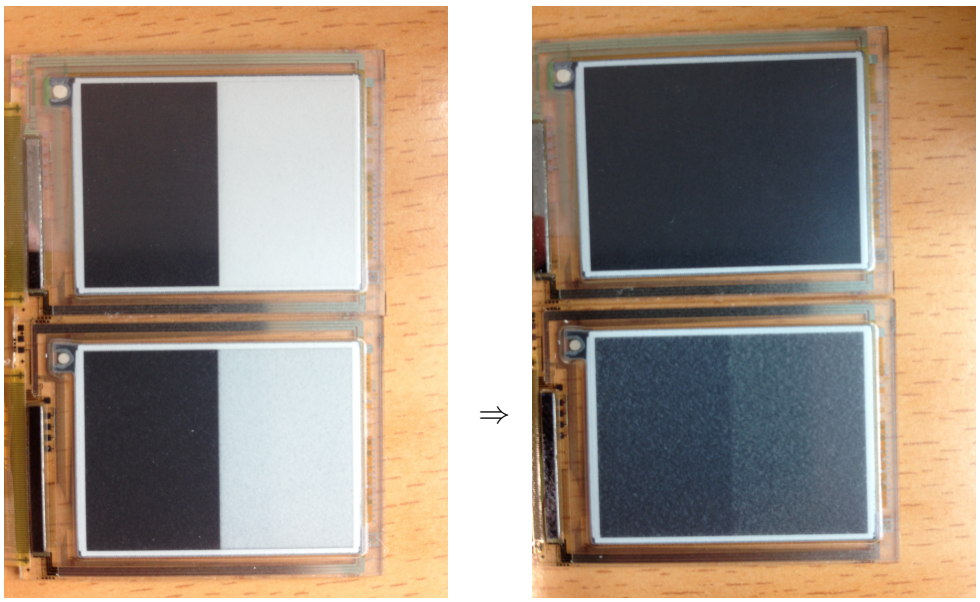


FIGURE 6.19: Two stage image update, black as basis, invert



(A) Write image (B) Clear to black

FIGURE 6.20: Image update from black, inverting at stage times 480ms (top) vs. 50ms (bottom)

It is quite obvious that the most negative visual effect at faster stage times is when images is written directly without inverting the final image first. If the image is not inverted, longer image updating time is required. In order to erase images

efficiently at faster stage times, the importance of shaking waveform or several updating stages will increase. This has to be taken into consideration when the driving waveform and timing controller is designed. By comparing the top image at Figure 6.13b with the bottom image at Figure 6.18b, it can be seen that the ghosting effect at 480ms stage time where the final image is not inverted, is close to the ghosting effect at 50ms stage time where the final image is inverted before it is written.

6.2.2.5 Stage time measure and energy consumption

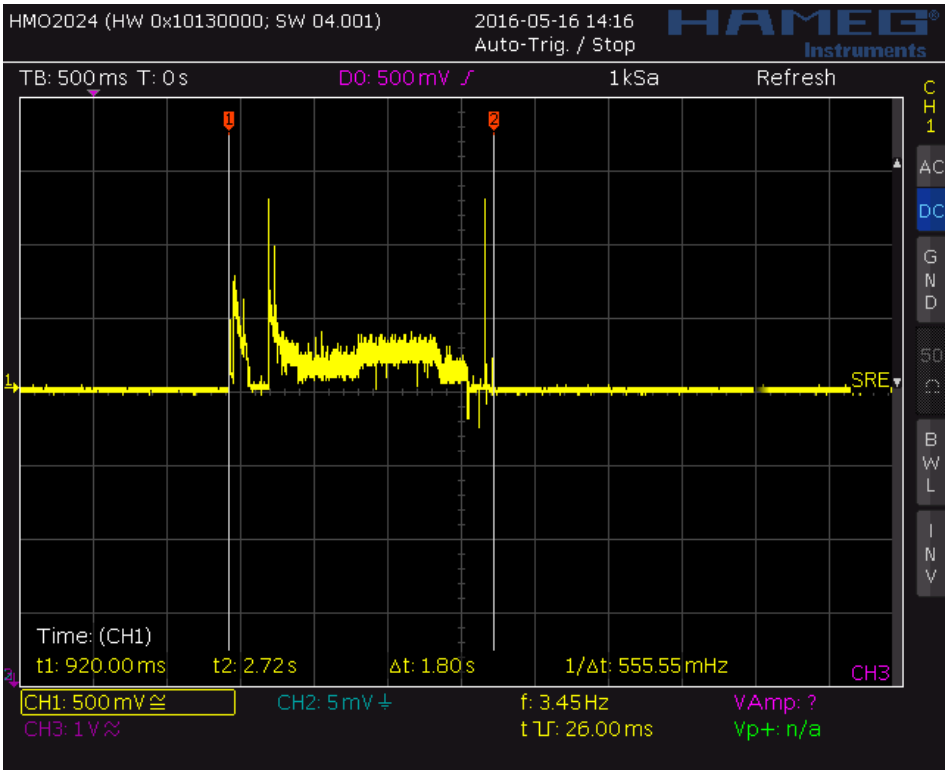
Figure 6.21 shows a comparison of a two-stage image update at a stage time of 480ms versus 50ms. With a stage time of 480ms, the total image updating time took 1.8 seconds from power up to power down of the COG. A stage time of 50ms resulted in a total image updating time of 870ms. If the stage time is subtracted from the total updating time, we can see that the EPD-panel require more than 750ms just to power up and power down.

Table 6.4 shows a few updating times related to different stage times and updating techniques. The first updating technique is a one-stage partial update where single pixels or line by line is written to the EPD-panel. The two-stage image update is written on a white background, where it first writes the inverted image before the new image is written. Related to Figure 2.6 on page 14, the two-stage image update is based on stage 2 to stage 4.

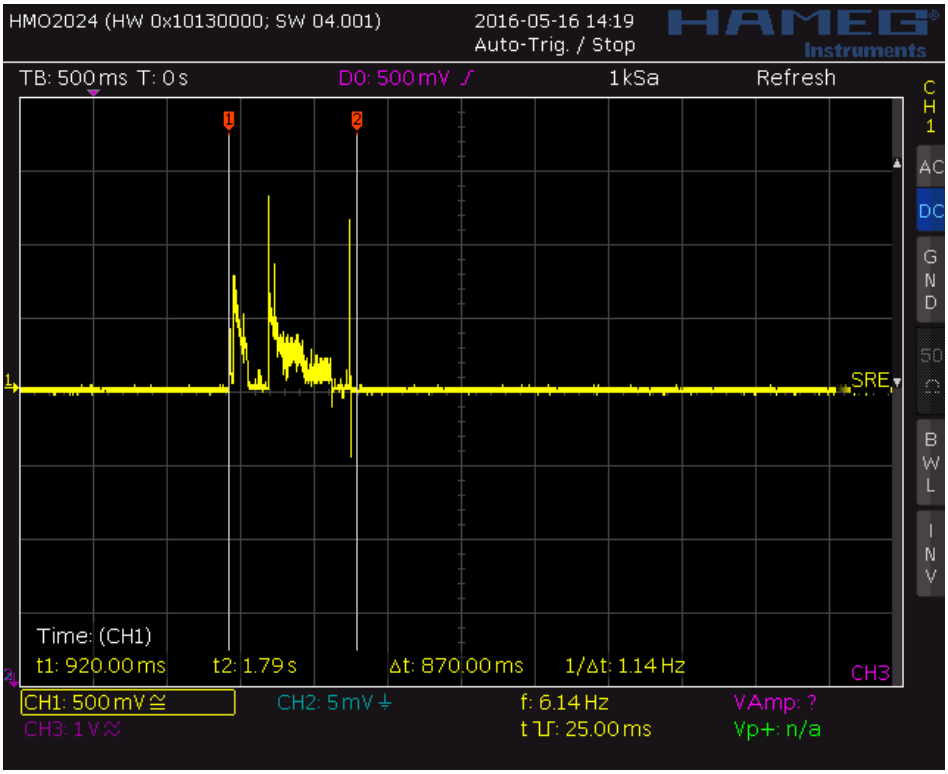
TABLE 6.4: Stage time versus the total image updating time at different updating techniques @ 22°C

Stage time	**Partial update (line-by-line)**	**Two-stage image update (inverse+new)**	**Four-stage image update (compensate+white+ inverse+new)**
50ms	830ms	870ms	980ms
200ms	950ms	1.21s	1.55s
240ms	1.03s	1.34s	1.79s
480ms	1.24s	1.80s	2.71s

The total energy consumption per image update can be calculated by multiplying the average power shown in Table 6.2 and Table 6.3 with the total updating time presented in Table 6.4. For instance, a four-stage image update with a stage time of 480ms, will have a total energy consumption of 62.92mJ for the worst case



(A) Current measure at 480ms stage time and 22°C



(B) Current measure at 50ms stage time and 22°C

FIGURE 6.21: Two-stage image update at 480ms vs. 50ms stage times and current consumption (1mV=1/100mA)

image, while a two-stage image update has an energy consumption of 41.13mJ. By comparing this, the total energy consumption is reduced by 33% just by reducing the updating time. Hence, by reducing the stage time to a minimum in addition to make use of as few updating stages as possible, the total energy consumption will automatically be minimized without the need of any hardware changes. If the stage time is reduced to 50ms and a two-stage image updating technique is used, the total energy consumption is approximately 19.87mJ, which is a reduction of almost 68% in total energy consumption compared to a four-stage image update at a stage time of 480ms.

If several images should be written in a short time period, a full power up and power down between each image might be more energy consuming than just putting the EPD in standby between the image updates. The current spikes related to leakage during charging and discharging of the charge pump capacitors is also a large contributor on the total current consumption as they are in the range between 10-15mA. Sleep-modes can be used if there should be frequent image updating sequence over a few seconds. However, by assuming only occasional image updates, the EPD-module should be powered down completely between every single image update.

6.2.3 Summary of the practical power analysis for small size EPDs

Following is a short summary of the most important findings in the practical power analysis for a commercially available small size EPD and its driving circuitry:

- Practical tests are based on a bipolar driving waveform, where the driving voltages are in the range of $\pm 15V$ and the top electrode (V_{COM}) is fixed close to 0V. The gate voltages that activates the TFTs in the display are close to $\pm 20V$, so the charge pump circuitry is pumping the voltage from a regulated input of 3V to $\pm 15V$ and $\pm 20V$. Bulky off-chip capacitors are used for this purpose.
- The image that is written will impact the power consumption also for small size displays. Related to power consumption at the internal COG source driver, the difference between worst case image update and best case image update is around 2mW.

- A traditional four stage image update takes about 2.7 seconds with default settings from the EPD provider. The stage time is set to 480ms. This means that the EPD module require about 780ms just for power up and power down.
- The average current consumption at the source driver (COG) is around 2mA. Current spikes around 13mA are observed when the COG is powered up and down. This is expected to be due to short-circuit power in the level-shifting circuitry for the high voltage driving.
- The average current consumption at the TI Boosterpack (PCB+COG) is about 4mA. This means that the discrete components in the PCB constitute for the majority of the total power consumption. It shall be noted that the input voltage is 5V and a significant power is wasted at the input LDO regulator.
- It is found that the visual effect of ghosting takes much longer to get rid of if the display is written in one continuous pulse compared to several stages where the image is inverted. With respect to ghosting effect, it is estimated that a one-stage image update without a shaking waveform will take 10× as long compared to a two-stage image update where the new image is inverted before it is written to its final state. Writing from black to white will typically take longer than writing from white to black. The absolute minimum stage time is considered to be around 50ms for the tested EPD.
- The total image updating time is tested for three different image updating techniques. With respect to energy consumption and image quality, the most optimal combination is a two-stage image updating technique with a 50ms stage time. This results in a reduction of almost 68% in energy consumption compared to a traditional four-stage image update with a 480ms stage time. The initial image should preferably be all black before new images are inverted and written to its final state.

6.2.4 Miniaturization

The most obvious area reduction technique is to implement as much as possible of the driving circuitry on-chip. Ideally, there should be no need for a printed circuit board (PCB), but instead integrate the whole driving circuitry into the

EPD panel. Using a small size EPD, the possibilities to integrate the driver chip onto the EPD panel using only TFTs might become more viable. Today, small size EPDs are normally delivered with a single chip driving circuitry like the COG bonded onto the COTS EPD panel studied in this thesis. However, off-chip driver circuits are often utilized as buffers for the input and output of signals connected to the chip. These off-chip circuits does not only require more physical space, but they also contribute significantly on the total chip power mainly due to charging and discharging of large output capacitances and leakage in short-circuit power in the transistors.

We already know that an EPD source driver is more suited to integrate onto the panel compared to an LCD source driver, due to long EPD response time as described in Subsection 3.3.2 on page 22. By taking advantage of the slow speed requirements and simpler driving circuits, the EPD is considered as a better candidate for a fully integrated driving circuit than LCD. Since a host MCU potentially can be used as timing controller, the main issue regarding area consumption is due to large off-chip capacitors related to high voltages and current capability in the DC/DC-converter.

Alternatively, a hybrid version of SMPS and charge pump can be used if the load current is too high for using only on-chip capacitors in a charge pump. A possibility can be to use a SMPS that convert the input voltage to $\pm 15V$ for the source driver and use a charge pump that pumps the $\pm 15V$ to $\pm 20V$ for the gate driver as presented in Figure 6.22[46]. Since the gate driver only require a fraction of the current capability that is required by the source driver, a hybrid DC/DC-converter might result in the least possible off-chip components if the current load is high.

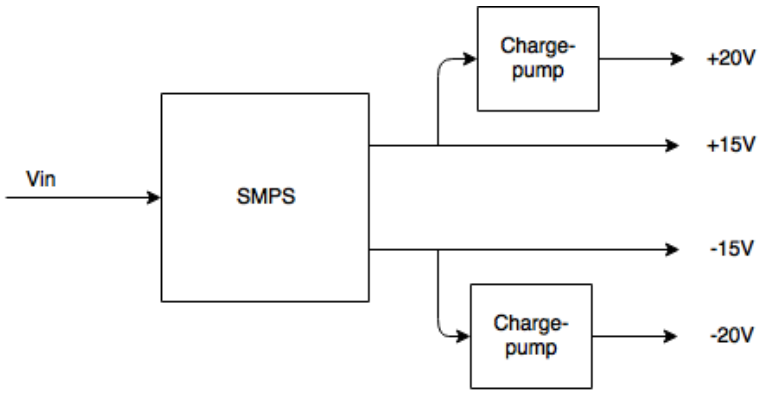


FIGURE 6.22: A hybrid DC/DC-converter using both SMPS boost converter and charge-pumps[46]

6.2.5 Optimization potential

From analysing power consumption in the COTS hardware together with the theoretical power consumption, it became clear that the largest power savings in a small sized EPD-driver lays in hardware design. More specifically in the analog part related to the high voltage charge pump and source driving circuitry. In the COTS hardware, driving of large off-chip capacitances is seen as one of the biggest contributors on both area and power consumption. This is not so surprising as off-chip capacitances often are several orders of magnitude larger than on-chip capacitances. If we look at the charge pump capacitors used in the TI EPD boosterpack (referred to Appendix B), they are on the order of a few microfarads, which is much larger than necessary for driving the load of a small size EPD. By assuming the conceptual EPD driving circuitry is customized for a TFT EPD equal to or below the smallest PDI display size, an on-chip charge pump can be considered. With an on-chip charge pump, the driving capacitances can be reduced to values in the order of picofarads. With this in mind, designing a single chip TFT-EPD driver will reduce both area and power consumption drastically compared to the COTS hardware studied in this thesis.

If the driving voltage can be reduced, both static and dynamic power consumption for most sub-modules in the EPD driving circuit will drastically decrease. Figure 2.3 on page 12 show that a pulse length around 50ms at 15V equals to a pulse length around 200ms at 5V in the dynamic range of the EPD. Tests from the COTS hardware show that an EPD stage time of 50ms at 15V is feasible with respect to image quality, but is seen as the absolute minimum required stage time in commercially available EPDs today. If a driving voltage of 5V is used, the minimum required stage time will therefore be about 200ms.

Theoretically, a voltage reduction to 5V will result in more than 3× lower static power consumption and more than 9× lower dynamic power consumption in the analog high voltage related circuitry compared to 15V driving. By using a unipolar driving waveform, the driving voltage can further be reduced to $\pm 2.5V$ with the same optical performance, which will both reduce circuit complexity and the total power consumption. However, an active matrix EPD at a reduced driving waveform have to be tested physically. The velocity models presented in this thesis is not exact models due to different particle sizes and charges in reality, so the consequences of reducing the driving voltages are hard to predict in theory.

The characteristics of TFTs also makes them more unstable at lower voltages, so the threshold voltage of the TFTs is an important parameter to remember when designing the driving waveforms. By using the simple model presented in Figure 6.1 and assuming a $V_{th} \leq 4V$, the gate voltage V_G should at least be around $\pm 7V$ if the V_{COM} and V_S is $\pm 2.5V$.

The second most important thing to consider besides designing a single low voltage TFT-EPD driver chip, is to use techniques that reduces the total stage time between image updates. It was found that a conventional four-stage image-refresh takes about 2.7 seconds with the 1.44" EPD panel with default settings from the EPD provider. This stage time can be further reduced without influence of any noticeable image degradation. If the driving voltage is reduced, it is also important to adjust the stage time for an optimal image contrast. A natural consequence of reducing the driving voltage in EPDs is that image updating time will get slower, but the gains in power savings will typically outweigh slower response time in low power, small size EPD products. Assuming image updates only on rare occasions, the entire EPD module could also be turned off completely between image transitions, which remove standby currents and minimizes the total power consumption.

6.3 Technical requirement specification

A technical requirements specification is developed for this thesis. The specification is intended to provide necessary basis for developing an EPD driving circuitry, with respect to electrical properties and hardware setup. It will be used as a guideline for designing a conceptual EPD driving circuit presented in the following chapter as well as limiting the scope of work for this thesis. These requirements sets the foundation for how the EPD module is to be designed, as well as which power reduction techniques that can be used at the different abstraction levels. See Appendix C for the full requirements specification.

The requirements specification is highly based on the COTS hardware used for practical tests in this thesis. As a short summary, the idea is to implement a single chip EPD module based on a timing controller that provides a unipolar driving waveform. The EPD module is to be designed for a 1-bit active matrix a-Si:H TFT panel with 128×96 pixel resolution. The EPD module shall be able

to be operated from a host MCU via SPI and the MCU shall provide the supply voltage for the EPD module via a GPIO pin, which normally has an output voltage between 3V and 5V. Driving voltages is supposed to be $\pm 2.5V$ at the TFT sources and $\pm 7V$ at the TFT gates. The clock frequency is based on 8MHz. In addition, a memory shall be able to store at least two image frames and a temperature sensor shall be used to monitor temperature changes in order to compensate the driving electronics for a colder environment. Operational temperature is intended to be between 0°C and 50°C.

Chapter 7

Conceptual EPD Module Architectural Design

In this chapter a conceptual EPD module architecture on block level will be presented. Based on the information presented in previous chapters and the requirements specification presented in Appendix C, alternative architectural low power solutions for the EPD driving circuitry will be proposed and discussed. Starting on the highest level of abstraction, an overall system level block diagram will be used to describe the basic functionality of the entire EPD module. Thereafter, entering the architectural level will show important aspects on how the module can be constructed based on various building blocks.

The overall purpose of the driving circuitry is to address the individual display pixels and generating the driving voltages required to change those pixels. This chapter will describe the basic behaviour of the various functional blocks and show what parts of the circuit that require clock and input dependent digital low voltage signals and what parts that typically require analog high voltage operation. It will cover the most important aspects of how an EPD-panel can be driven, but some simplifications will be made to highlight the basic functionality of the EPD module. The conceptual EPD module presented in this chapter is intended to be a process independent design.

7.1 System level block diagram

Figure 7.1 shows an EPD module block diagram at system level. The EPD module is controlled by a host MCU. The main tasks for the host is to provide power, clock-signal and image-data to the EPD module. It will also be the communication interface to other units such as a temperature sensor and memory. The host will take care of data processing and control the power-on sequence at response from the user or the program and the power-off sequence at response from the EPD module after an image update is finished.

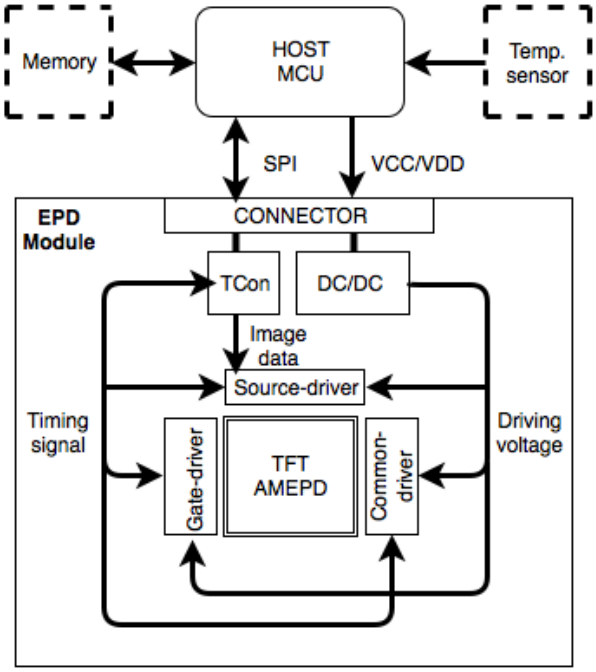


FIGURE 7.1: EPD module block diagram at system level

The four main building blocks required to drive an active matrix TFT EPD is a *gate driver*, *source driver*, *DC/DC-converter* and a *timing controller (Tcon)*. When using a unipolar driving waveform it is also required an additional *common driver*. Here it is assumed that the host MCU will take care of the data processing and provide necessary signals and power in order to update the EPD. This will include writing images to memory, power on and initialize the driver before data is sent to the EPD module, in addition to control the power off sequence at response from the EPD module. It is also assumed that the *memory* required for image frames and a *temperature sensor* is peripheral parts of the EPD module.

7.1.1 EPD-panel addressing

The TFT AM-EPD is composed of a multitude of EPD cells as shown in Figure 2.1 on page 9 and forms an EPD panel with a pixel addressing as shown in Figure 7.2. Here, pixel (1,1) is at the top left corner, while pixel (m,n) is at the bottom right corner. Since the driving circuitry design is highly dependent on the size and electrical addressing of the EPD panel, a specific display size of 128×96 pixels is chosen also for the conceptual EPD module design. Using a 1-bit active matrix a-Si:H TFT panel, the foundation for a low cost, high information content, black and white EPD module is laid. The top electrode is connected to a common voltage source (V_{COM}), while the bottom electrodes are connected to individual voltage sources (V_S) via the sources of the thin film transistors as shown in Figure 6.1 on page 48.

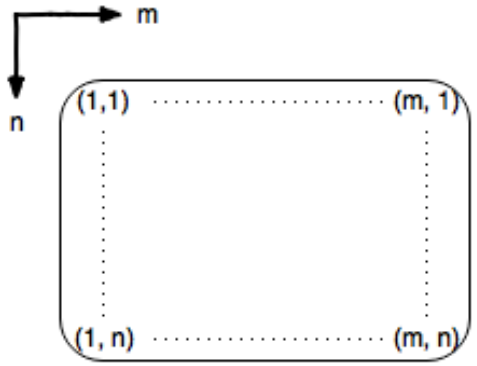


FIGURE 7.2: EPD panel addressing

Figure 7.3 shows a section from the complete active matrix EPD panel and an example of how the addressing can be done. With a display size of 128×96 pixels, $m = 128$ and $n = 96$. The gate driver activates one row at at a time and during this specific time the source driver writes to all the pixels in the activated row simultaneously. In this example, row number two is activated by setting the gate driver voltage Vg_2 high. By using a bipolar driving waveform where the common voltage source V_{COM} is fixed at zero, we can see that pixels (1,2), (3,2) and (m,2) will turn white, while pixels (2,2) and (4,2) will turn black. All other rows are off at this specific time and every single pixel in these rows are unchanged.

In a unipolar driving waveform, the common voltage source toggles between a positive and negative voltage. If V_{COM} is negative, pixels (1,2), (3,2) and (m,2) will turn white, while pixels (2,2) and (4,2) will be unchanged. If the V_{COM} is positive, pixels (1,2), (3,2) and (m,2) will be unchanged, while pixels (2,2) and

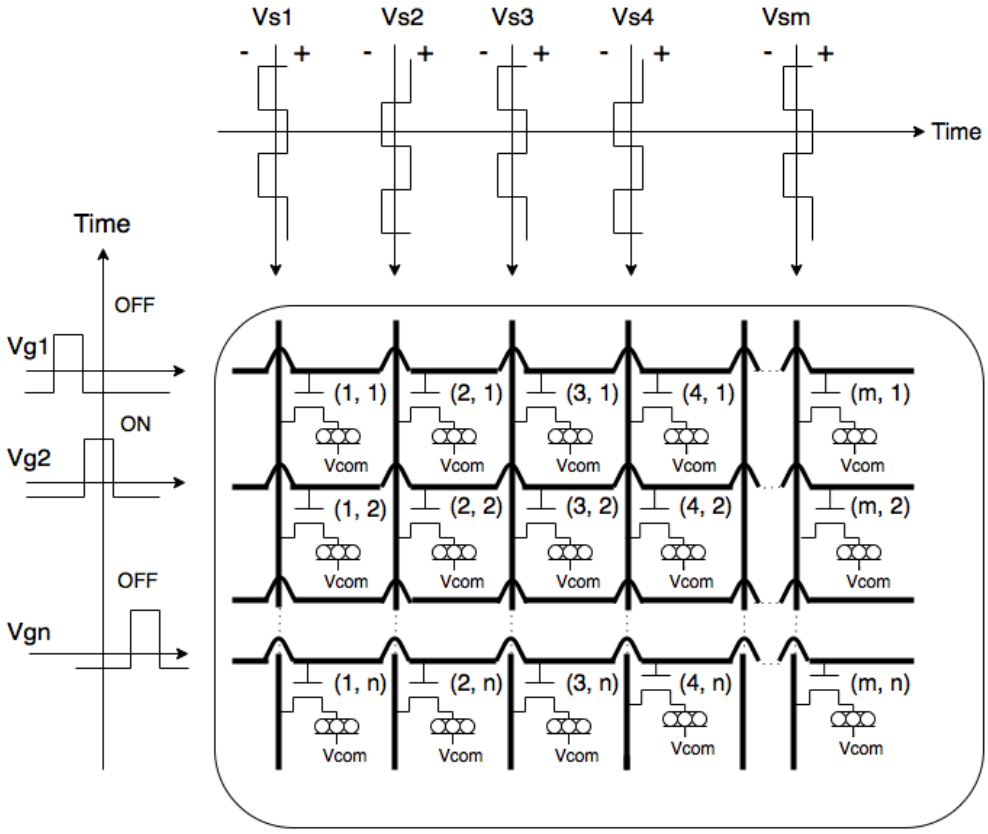


FIGURE 7.3: EPD panel addressing example

(4,2) will turn black.

From analysing the unipolar driving waveform, it is can be seen that at least two stages are required to update the display using this waveform. This is because the source driver is not able to write both white and black simultaneously when V_{COM} is at the same voltage potential as V_S. Figure 7.4 shows a transition diagram comparison of the traditional bipolar waveform versus a two stage unipolar waveform. With a basis in Figure 5.1 presented in the previous work on page 39, it is shown how a unipolar driving waveform can execute the same image transition in one column of the display.

By first clearing the display to black, for then to write the white pixels in the new image, a simple voltage transition scheme can be implemented. When writing the display to black, only the frame buffer for the previous image is scanned to re-write the white pixels to black. When the display is all black, an additional stage to activate all particles and neutralize the electric field should be applied. This can be done with a shaking waveform with a frequency higher than 30Hz to avoid visible flicker. An example of the proposed driving waveform is shown in

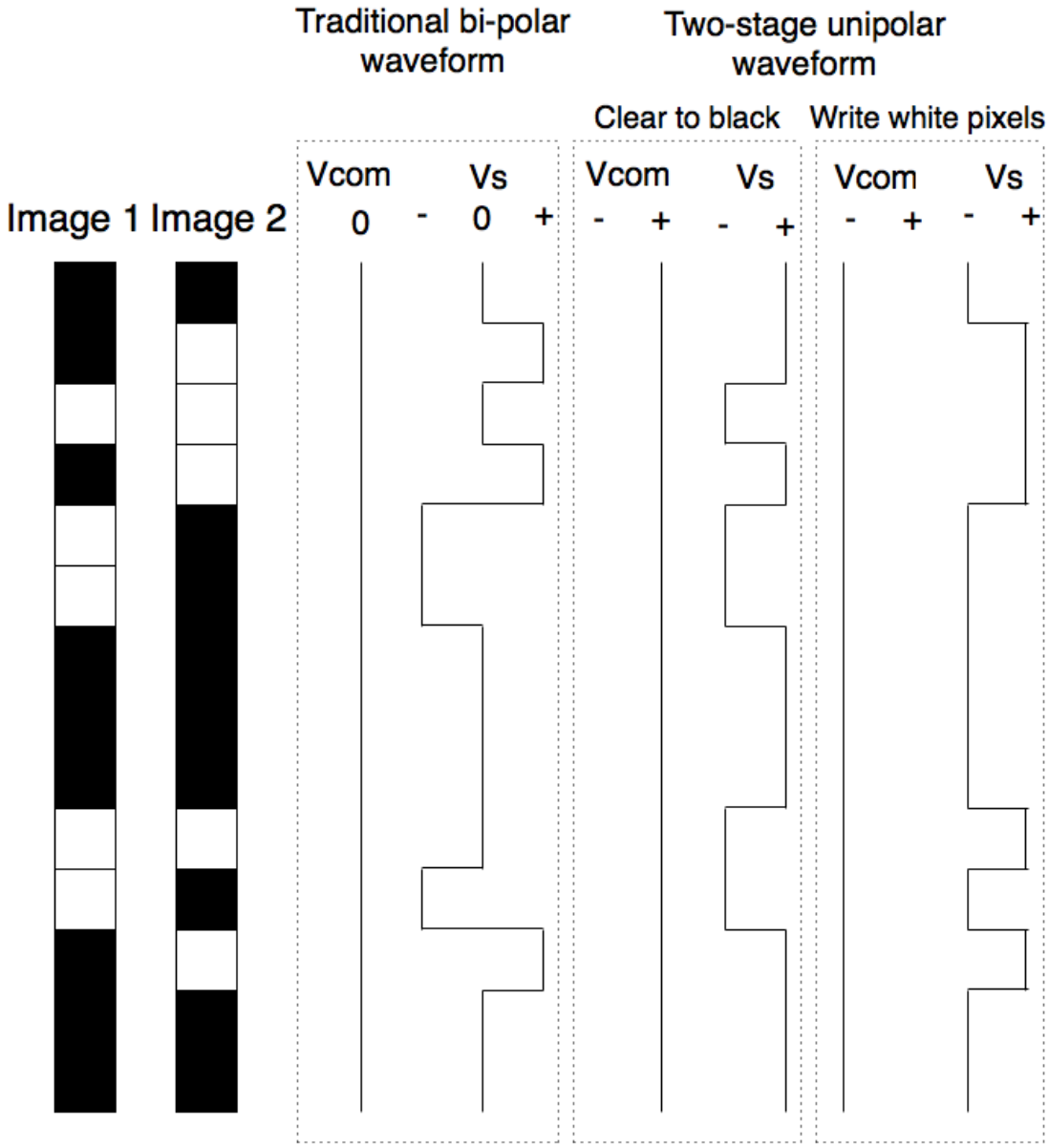


FIGURE 7.4: Transition diagram between two images in one display column

Figure 7.5. After the display is activated and cleared to white, the frame buffer for the new image is scanned to write the black pixels. Since the EPD typically takes longer time to write from black to white as shown in Figure 6.12 on page 68, the activation/clearing to white stage will typically require a longer time than the first and third stage.

A three-stage image update for a unipolar waveform can be justified since the traditional bipolar waveform also normally use up to four stages in order to reduce the ghosting effect efficiently. We already know that writing black pixels only require a short stage time and the EPD consume less power when writing

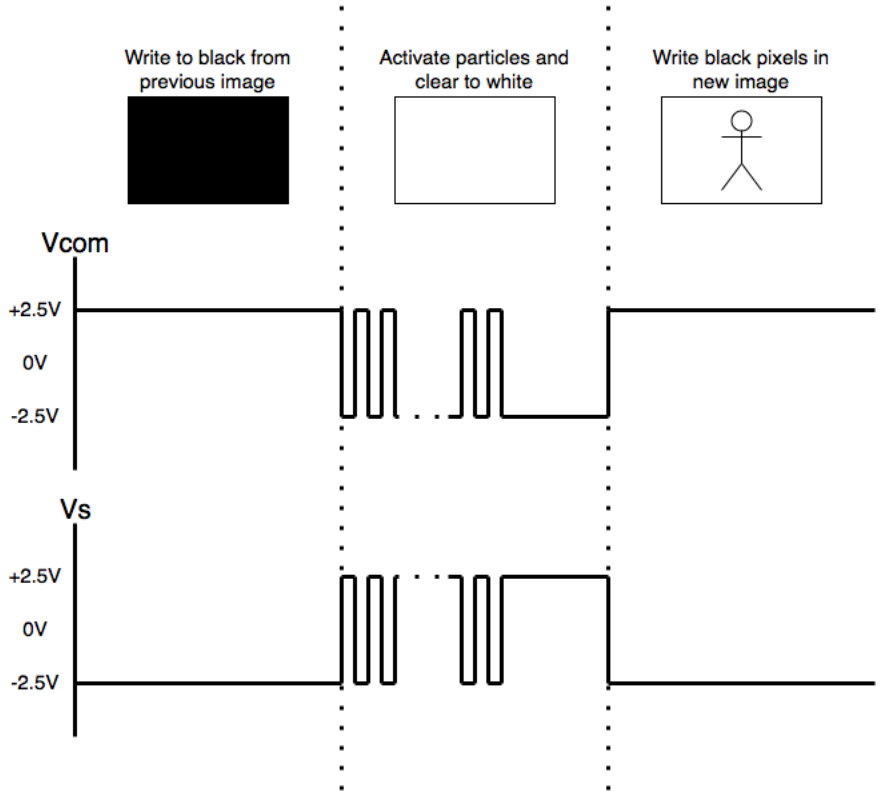


FIGURE 7.5: An example of a three-stage image update using unipolar waveform and shaking

from all black to all white, than having many voltage transitions with alternating black/white pixels. Flicker will remove ghosting effect faster and the total stage time will hence be expected to be improved. The total stage time is estimated to be around 600-800ms depending on the required time to clear the display to white. This estimation is based on Figure 2.3 on page 12 and the results from the analysis in Chapter 6.

7.2 Architecture level block diagram

Figure 7.6 shows the different building blocks in the EPD module with specified inputs and outputs. The DC/DC-converter takes in power from the host MCU and provides both positive and negative driving voltages to the gate driver, source driver and the common driver. The source driver need to take in pixel data and convert the serial data into positive or negative driving voltages for all columns depending on the binary pixel value. The source driver require 128 parallel outputs, $Vs_1 \rightarrow Vs_{128}$, since the display has 128 columns. The gate driver has 96

outputs, $Vg_1 \rightarrow Vg_{96}$.

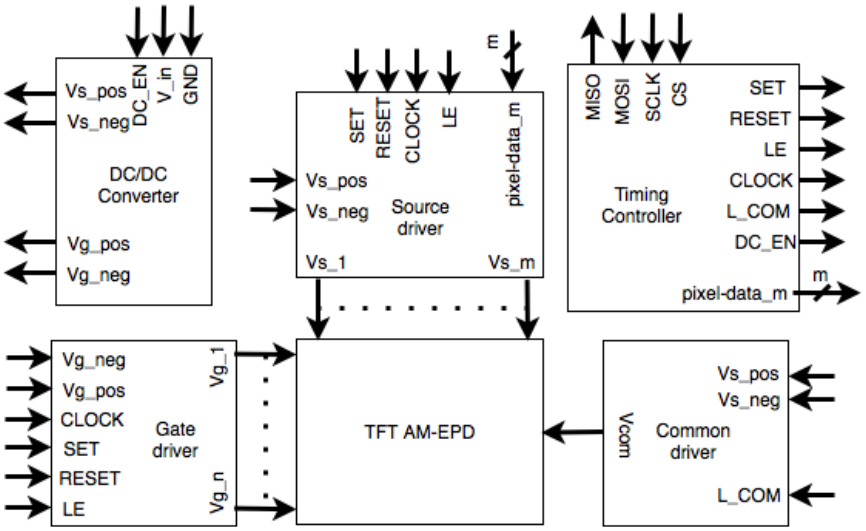


FIGURE 7.6: EPD module block diagram at architectural level

Since the source driver and gate driver needs to be synchronized, they shall be able to take in a start pulse (SET), clock signal (CLOCK) and latch enable (LE), as well as a common reset signal (RESET). The common driver is supposed to take in a digital signal (L_COM) and convert it to a positive or negative driving voltage, depending on whether the display shall be able to write white (L_COM=high) or black (L_COM=low) pixels.

The timing controller is responsible of receiving digital signals and data from the host MCU and synchronize the the display drivers. By implementing an SPI receiver, the timing controller is able to give notice back to the host MCU when a data transfer is finished. The pixel data in the timing controller (pixel-data_m) shall output an 128-bit bus connected to the source driver. The timing controller will also provide a control signal to enable the DC/DC-converter (DC_EN) for synchronization of the internal circuitry in the EPD module.

7.2.1 Source driver architecture

One section of an example source driver architecture is shown in Figure 7.7. In this case, there is required 128 flip-flops for the shift register that is connected as shown in Figure 3.4 on page 21. There is also 128 individual "Latch 1" and "Latch 2"- D-latches and voltage selector circuits for each column of the display. The optional output buffer-stage is not included in this architecture.

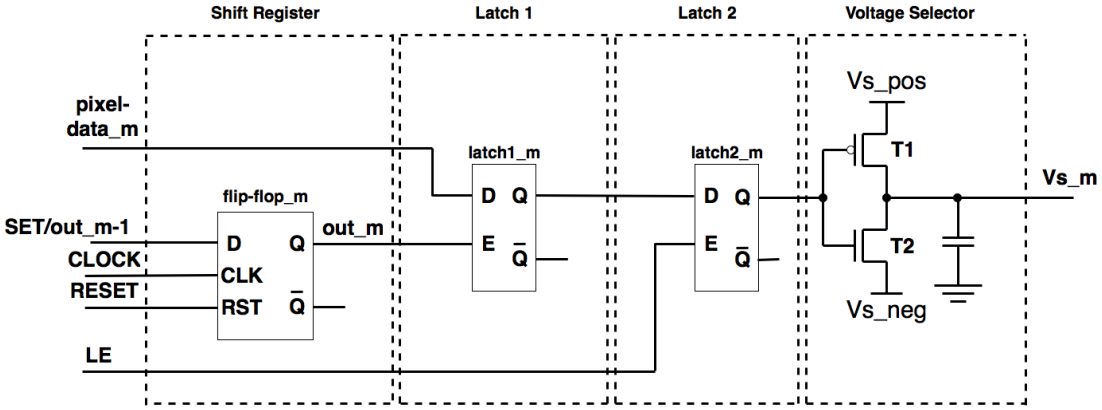


FIGURE 7.7: Source driver hardware architecture

The pixel-data is sequentially loaded into the first latch stage using the shift register. If a clock of 8MHz is used, the source driver will require 16ms to load all 128 bits of data into the first latch stage. Once all 128 latches in the first latch stage is loaded with the binary pixel values, a common latch enable (LE) for the second latch stage is enabled to transfer one row of data to the voltage selector. If the pixel value for a specific column is binary high, there shall be a negative driving voltage at the output. A binary low pixel value, will result in a positive driving voltage at the output.

In this architecture, transistor T1 and T2 is used as an inverter to transfer the source driving voltage from the DC/DC-converter to each output. In order to reduce sub-threshold leakage and short-circuit power, additional stacking transistors as shown in Figure 7.8 can potentially be used. Since the two transistors are connected in series, they share the same current and functionality. Sub-threshold leakage current is reduced because V_{ds} across the two transistors are less than V_{ds} for the original transistor[69].

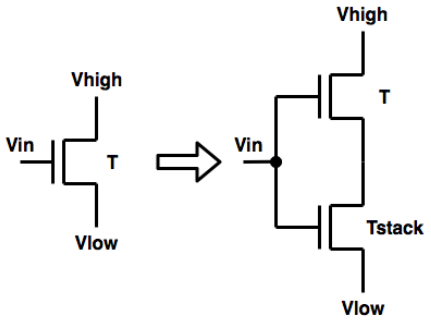


FIGURE 7.8: Stacking transistor[69]

7.2.2 Gate driver architecture

A proposed gate driver architecture is shown in Figure 7.9. The shift register stage and voltage selector is similar to the source driver, except for it is only required 96 individual outputs since the display shall have 96 rows. In order to synchronize the gate driver and the source driver, a clock divider is used to reduce the frequency of the clock signal into the shift register flip-flops. The idea is to compensate for the source driver delay of 16ms in the gate driver, so a common latch enable can be used for both source-and gate drivers.

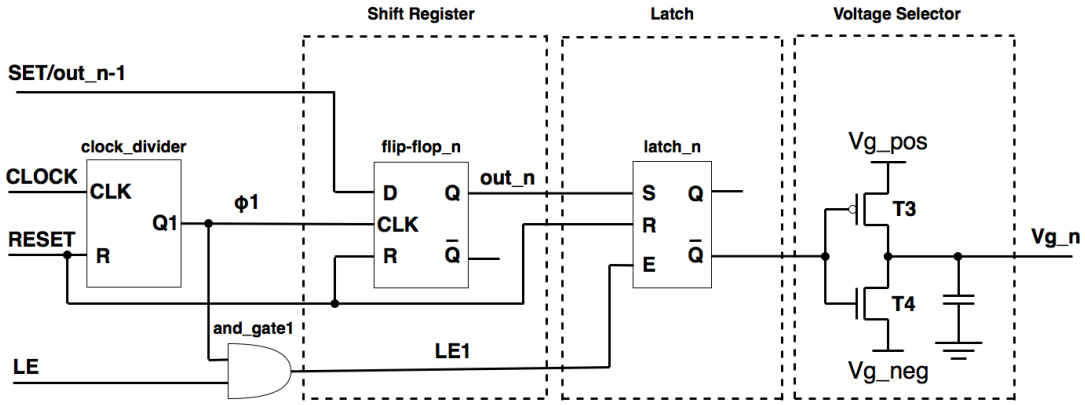


FIGURE 7.9: Gate driver hardware architecture

By utilizing a separate latch stage with 96 enabled Set/Reset (SR) latches in the gate driver, it is possible to just activate the specific rows that require a pixel update. For instance, if the display shall be cleared to white and a whole row already is white, the latch enable signal (LE) can be skipped for that specific row during the update. This detection needs to be done in the timing controller. The architecture will require extra logic that takes up more area than a traditional gate driver as presented in Figure 3.3 on page 20, but the total energy consumption will be reduced in cases where just a fraction of the display needs to be updated.

A possibility is to use multiphase clocks to reduce the power consumption in the shift register as described in Section 6.1.3 on page 50. By implementing a clock divider circuitry with one specific output per clock phase, a clock diagram as shown in Figure 7.10 can be used. Here, S/R represents the shift register flip-flops. Since it is required that the the stage time shall be more than 100ms and we assume that the latch enable (LE) will be activated approximately every 16ms, the gate driver architecture is designed with an AND-gate for each clock phase output from the voltage divider. Therefore, both the clock and LE needs to be high in order

to enable the latches.

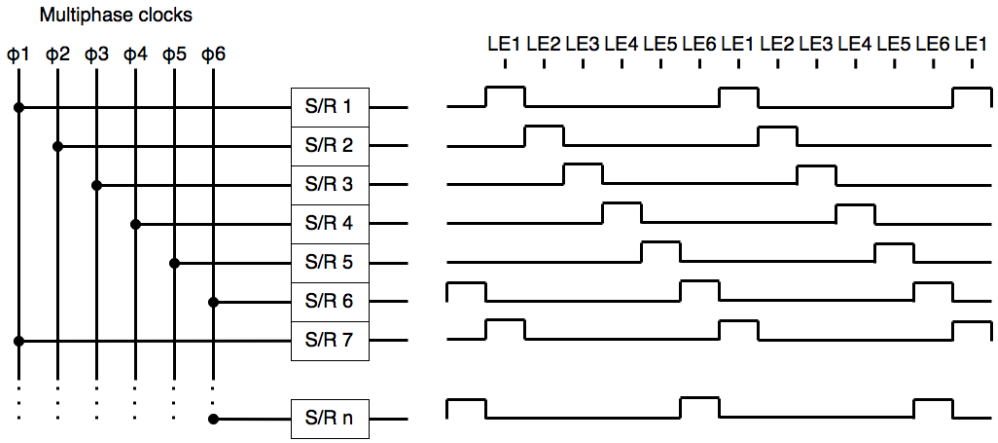


FIGURE 7.10: Multiphase clocks (six-phase)

By using a six-phase clock as shown in Figure 7.10, we can see that the first shift register flip-flop has a high output (Q=1), when SET=1 and ϕ1=1. When LE1=1, Vg_1=Vg_pos since the latch_1 output ($\bar{Q} = 1$) is set high. Vg_1 will stay positive until LE1 is set high again. Now, the flip-flop output (out_1) will be low and row 1 (Vg_1) will become negative, while row 7 is set high and Vg_7=Vg_pos. If the delay between every LE pulse is 16ms, every row will be active for approximately 6*16ms=96ms. By using more clock phases, each row can potentially be active for a longer time period.

Every latch in the latch stage should be reset prior to the activation of the gate driver, while SET=0, so every gate is OFF before the scanning begins. The clock divider circuitry should therefore set all the outputs high when the reset pulse is high (RESET=1). By setting both RESET and LE high, every gate driver output will become negative (Vg_n=Vg_neg).

In cases where the latch stage is not enabled, the switches in the voltage selector will not output the driving voltage. Hence, the power dissipation will be reduced since there will be no changes in the voltages at the source lines. If only a few rows require a update between two images, the total stage time can be reduced if image processing is performed prior to activation of the EPD module.

7.2.3 Common driver architecture

The primary function of the common driver is to provide the common top electrode with either a positive or negative driving voltage, depending on the image updating stage. A simple common driver architecture can be based around an inverter configuration as shown in Figure 7.11. If the input signal (L_COM) is high, the common driver will output a negative driving voltage. A positive Vcom output will appear if the input signal is low.

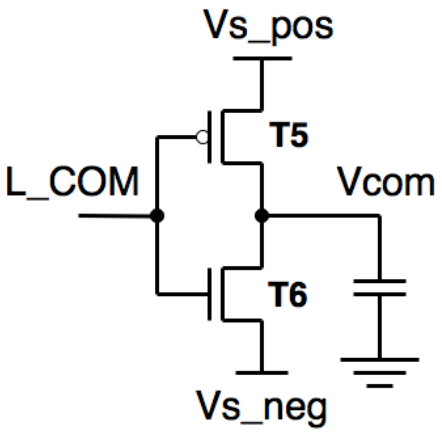


FIGURE 7.11: Common driver hardware architecture

7.2.4 DC/DC converter architecture

The DC/DC converter architecture is very dependent on key factors such as input voltage, output voltage, current capability and IC process. The idea for this conceptual design is to use a GPIO-pin from the host MCU as the power input (V_in). Most MCUs are like the AtMega2560, limited to source a current of maximum 20mA from the GPIO-pins. Since the expected current consumption of the entire EPD module is below 1mA, this will be no problem.

The DC/DC converter shall be able to convert an input voltage in the range of 3V to 5V into $\pm 2.5V$ for the source-and common driver (Vs) and $\pm 7V$ for the gate driver (Vg). This is to achieve a voltage difference of 5V over the EPD cells if a unipolar driving waveform and TFTs are used to control the pixels.

Typically, an LDO regulator will be used at the input to achieve a clean and stable reference voltage for the circuitry. In order to get minimum power loss over the the LDO regulator, the input voltage should preferably be as close as possible to the

output voltage. The LDO regulator can be used to regulate the input voltage down to $2.5V$ with relative high efficiency. A polarity inverting charge pump can then be used to convert the positive voltage of $2.5V$ into a negative voltage of $-2.5V$ with high voltage-and power conversion efficiency with little circuit complexity.

If a charge-pump circuitry is used to pump these voltages up to around $7V$, we can see that the optimum number of pump stages is N=3 by using Equation 6.4 on page 53. The load current (I_L) is expected to very low at the output since the voltages only are used to drive the TFT gates. The required charge pump power will therefore be very low (referred to Equation 6.3 on page 53). Capacitor sizes will also be so small that on-chip capacitors will be ok to use. If we assume $I_L \approx 0.1mA$ and $f = 8MHz$, we can by rearranging Equation 6.2 on page 53 see that the capacitor sizes required will be in the range of 0.125pF.

Circuit delay in the charge pumps will of course need to be accounted for. The timing controller should therefore make sure that the voltages are stable after power up, before driving the display pixels. An example of a DC/DC architecture is shown in Figure 7.12. Here, the non-overlapping clocks required for the charge pump circuits are not shown.

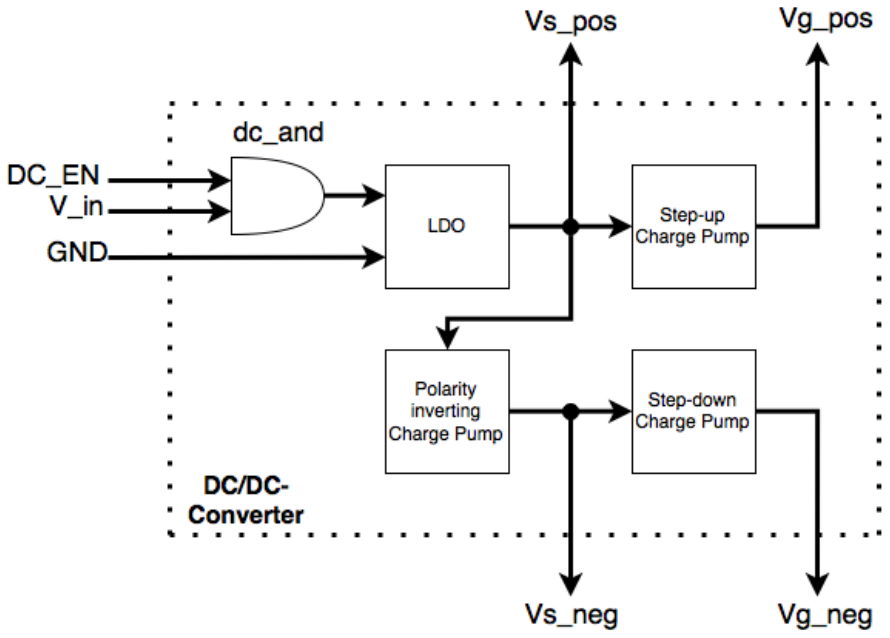


FIGURE 7.12: Example of a DC/DC-converter hardware architecture

7.2.5 Timing controller architecture

In this thesis, the timing controller is intended to be primarily based on the host MCU. The main hardware architecture of the architectural timing controller block presented in Figure 7.6 will therefore be based around an SPI-receiver circuitry. The SPI-reciever circuitry shall interpret SPI commands from the host MCU (master) and be a interface between the MCU and the other sub-modules. In order for the EPD module to function properly, it is important that the commands come in right order. The timing controller architecture described in this subsection will focus on the timing sequences more than the physical hardware. A basic timing sequence is presented in Figure 7.13.

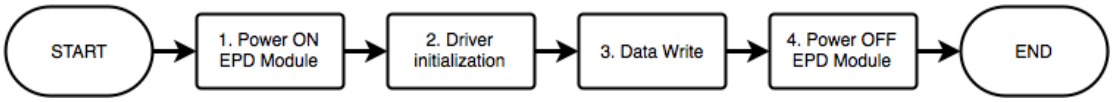


FIGURE 7.13: Timing sequence

7.2.5.1 Power ON EPD module

The first stage is the power ON of the module. In the initial START state, all the control signals and voltages will be off. At the power ON, V_in will be set high from the GPIO-pin in the host MCU. The chip select (CS) signal will also be enabled to activate SPI communication between the EPD module and the host MCU. A reset pulse will then make sure that all the shift registers, latches and other circuitry is cleared and ready for data-input.

7.2.5.2 Driver initialization

The driver initialization stage shall be able to set the power for the driving voltages. It shall start the DC/DC-converter and wait until all the output voltages are ready. When the output voltages of the DC/DC converter are stabilized at $\pm 2.5V$ and $\pm 7V$, the EPD module is ready to write the pixels to the display.

7.2.5.3 Data write

The data write stage is the main stage and will typically be looped until the EPD module receive a shut-down signal. This stage can be divided into several sub-

stages depending on what image updating technique that is used. If a three-stage image update like shown in Figure 7.5 on page 86 is used, it will be natural to divide this stage into three sub-stages:

Sub-stage 1: First L_COM shall be set low in order to drive the white pixels to black on the display. Then a SET-pulse will enable the shift registers in the source and gate driver. Since $Vcom$ will be set to a positive voltage ($Vcom = Vs\_pos$), a black pixel will appear on the display if the TFT sources are set to a negative driving voltage ($Vs = Vs\_neg$). By scanning through the image buffer for the previous image, the EPD module shall set all white pixels to a negative driving voltage (Vs_neg) and all black pixels to a positive driving voltage (Vs_pos). By reading in the pixel-data from the memory, a logic low will result in a positive output voltage (Vs_pos) with the source driver hardware architecture shown in Figure 7.7 on page 88. It is worth noticing that a logic low is a black pixel in the XBM-format as shown in Listing 6.1 on page 59. The latch enable (LE) will give a pulse when one full row has got a value from the pixel-data. Since the EPD has 128 columns, this will happen for every 16th byte that is read into the first latch stage in the source driver.

Sub-stage 2: In this stage, a shaking waveform can be implemented by clearing all control signals in addition to resetting and bypassing the shift registers and latches in the gate and source driver. All TFT gates are set to Vg_pos to activate all the rows in the display. $Vcom$ and Vs should be set with alternating Vs_pos and Vs_neg in a frequency higher than 30Hz to activate the particles without any visible flicker. The display is then cleared to white by setting all sources to a negative driving voltage ($Vs = Vs\_neg$) and Vcom to a positive driving voltage ($Vcom = Vs\_pos$).

Sub-stage 3: L_COM is now set low again and this sub-stage follows the same activation pattern as described in Sub-stage 1. The difference is that in this sub-stage, the image buffer for the new image is scanned. Black pixels are written when the pixel-data inputs a logic low.

7.2.5.4 Power OFF EPD module

After the new image is uploaded to the EPD, a shut-off signal will be sent to the EPD-module. As a power off sequence, all latches are reset, the charge pumps are

powered off and all internal capacitances are discharged. Then the SPI communication will typically be turned off by ensuring that the MOSI and CLOCK are low before the chip select (CS) is set low. Lastly, V_in is set low from the GPIO-pin.

Chapter 8

Concluding remarks

In this work, an elaboration of a low power electrophoretic display (EPD) module is carried out by following a stepwise design process. Based on a theoretical and practical analysis of the EPD technology and its required driving circuitry, it is found that more than 90% of the total power consumption typically is related to high voltage driving in monochrome EPDs. High voltages in the range of $\pm 15V$ are used for best possible optical performance and user experience when refreshing images. The high voltages result in extra circuit complexity and bulky off-chip components tend to be used. By reducing the driving voltage, several problems with respect to circuit area and power consumption can be solved.

Lower driving voltages can be traded off with slower updating times and poorer optical performance in the EPD-technology. However, the lowest possible driving voltages for today´s EPDs are considered to be 5V. A driving voltage at 5V will typically result in 60-80% of the optical performance achieved at a driving voltage of 15V. By using a unipolar driving waveform, the driving voltage can theoretically be reduced to $\pm 2.5V$ with the same optical performance. This will have a great impact on less dynamic power consumption and circuit complexity in the driving circuit. By reducing the total image updating time to a minimum of accepted image contrast, the total energy consumption is estimated to decrease drastically compared to existing small size EPD-solutions.

It is found that driving pixels from white to black typically takes shorter time than writing from black to white. In order to efficiently reduce ghosting, it is more important to use shaking waveform or inverting images in several stages at faster stage times. The most optimal image updating technique at a low voltage

unipolar driving waveform is considered to be a three stage image update. The first stage will write the image to black based on the previous image uploaded to the display. The second stage will activate all particles and clear the display to white using shaking waveform and the last stage will write black pixels from the new image.

From designing a conceptual low power driving circuit, following design steps are considered as the most essential:
1. Customize driving circuit to a specific EPD panel. Small size display equals to less circuit and power consumption.
2. Reduce driving voltage to a minimum of acceptable optical performance.
3. Use smarter algorithms and waveforms to keep the response time as fast as possible.
4. Turn off the EPD module as soon as the display image is updated.
5. As much on-chip circuitry as possible.

Based on the history of the EPD-technology, the required driving voltage for best optical performance will most likely continue to decrease in the future. Optimizations for a driving circuitry based on low driving voltages will contribute to increased demand of the EPD technology, since it potentially can be used in a wider range of small sized, ultra low power products.

8.1 Further work

As a next step to verify the analyzes and hypotheses introduced in this thesis, a configurable driving circuitry should be set up and tested on physical EPD-cells. The driving circuitry should be able to be configured for driving voltages between $\pm 2.5V$ and $\pm 7.5V$. In order to find the minimum acceptable voltage and image updating time with respect to ghosting and image degradation, the driving voltages should be compared to different stage times. Due to time constraints, this could not be performed in this thesis.

Parts of the DC/DC converter in the hardware kit used for this thesis, is integrated into the Chip-on-Glass (COG) on the EPD panel. This makes the hardware unsuitable for testing the EPD with lower driving voltages. In order to make a

driving circuitry used to test various stage times and driving voltages, both the timing controller and the DC/DC converter should be externally controlled.

A test-setup can be composed from discrete components to control an EPD pixel circuit as modelled in Figure 6.1 on page 48. Preferably, an active matrix EPD should be used for this purpose to include the effects of the Thin-Film Transistors (TFTs). Another approach is to use segmented E-ink displays as shown in Figure 8.1. The segments can mimic one column in an active matrix display like shown in Figure 7.4 on page 85. By using discrete n-type MOSFETs as switches, the basic behaviour of the driving circuitry is kept. The effects of ghosting and optical performance at lower voltages can be monitored, but the discrete components will of course consume more power than expected for an equivalent on-chip circuit.

FIGURE 8.1: E-ink segmented 14 bar EPD cells[70]

If the tests show positive results, the driving circuitry can be implemented on-chip by following specified requirements and process parameters. The basic architecture presented in Chapter 7 can potentially be used together with the power reduction techniques at the different abstraction levels as described throughout this thesis.

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Appendix A

Electronic paper display technologies

The following pages include a comparison of different electronic paper display technologies. The technologies were reviewed to find the most promising technology for Internet of Things (IoT)-applications. The tables are taken from a specialization project that was conducted at Norwegian University of Science and Technology (NTNU), fall 2015[55]. The tables are primarily based on data presented in Heikenfeld(2011)[4].

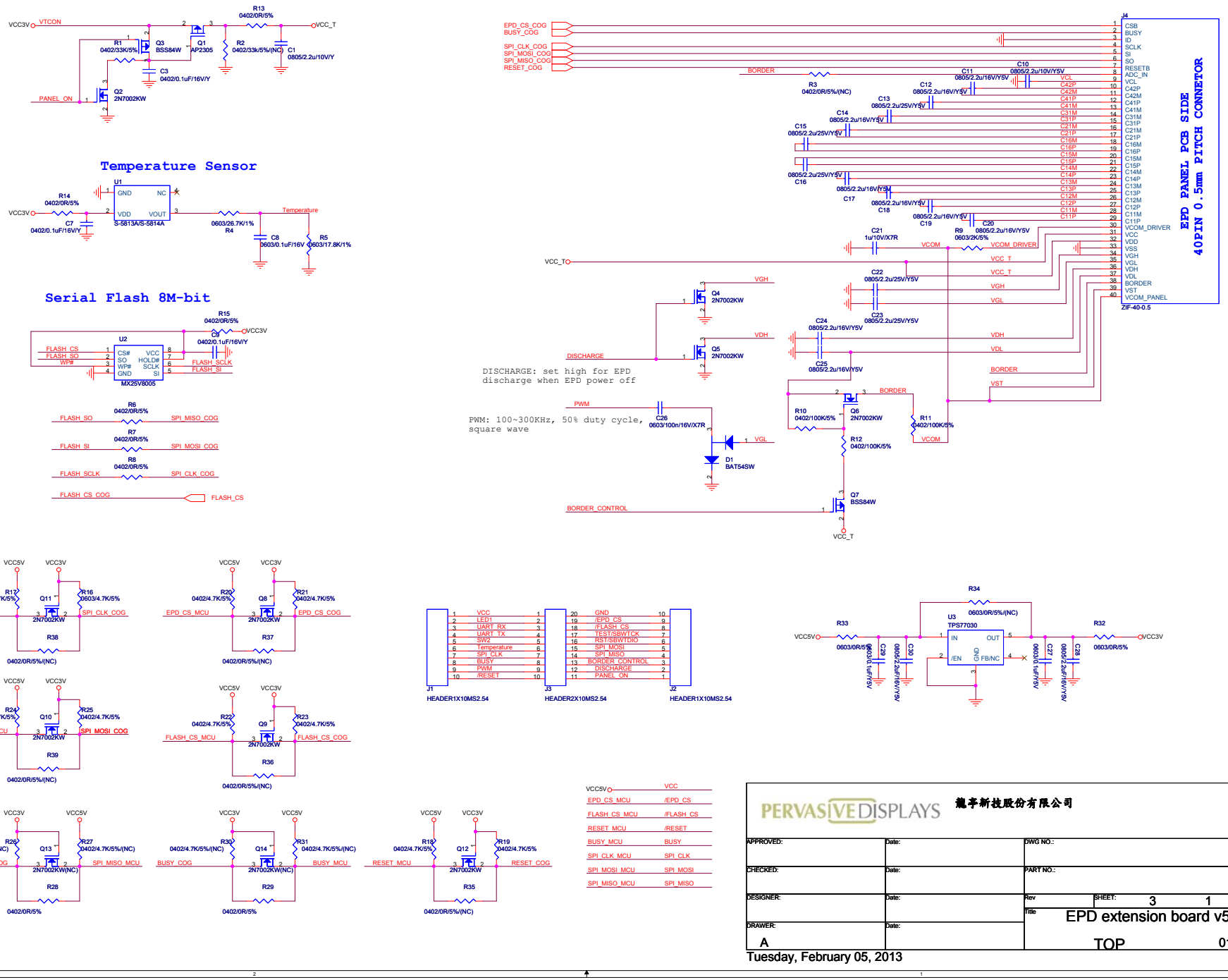
Section	Technology	Advantages	Disadvantages
3.1.2	Electrophoretics	• Currently dominant on the market. • Very low power. (No static power consumption, low dynamic power) • Thin and lightweight. • Rugged	• No/poor color. • Slow response time. • Low brightness. • Ghosting effect.
3.1.4	Electrowetting	• Fast (resp.time<10ms) • Good color and contrast. • Thin and lightweight.	• No volume production. • Needs a refresh rate to keep image. (down to 1Hz). • High dynamic power.
3.1.5	Electrofluidic	• Very high reflectance. • Fast • Good color and contrast. • Thin and lightweight. • No static power.	• No volume production. • High dynamic power. • New technology with unproven performance.
3.1.6	MEMS	• Very fast (resp.time<1ms). • Low static power. • Good color.	• Very low pixel/color depth (few gray levels). • Size limitation. Cost goes up and yield goes down exponentially with increased size. • Narrow viewing angle. • High dynamic power.
3.1.7	Photonic Crystal	• Capable of single-layer coloring.	• Relativley undeveloped/unproven.
3.1.8	Electrochromic	• Mature technology. • Large viewing angle. • Memory effect. • Low fabrication cost. • Simple construction.	• Very high dynamic power consumption (current driven). • Slow response time. • Image diffusion/Cross-talk. • Needs occasional image refresh.
3.1.9	Cholesteric LCD	• Low power (no static power consumption) • Thin and lightweight. • Good color. • Possible to integrate solar cells behind the display.	• Slow response time. • Poor optical performance. • Low contrast ratio. • Very high cost.

	Electrophoretic	In-plane Electrophoretic	Electrokinetic	Electrowetting	Electrofluidic	MEMS	Electrochromic	Ch-LCD
Bistable	Yes	No	No	No	Yes	Yes	Hours	Yes
Voltage (V)	15(typical) 5(optional)	~10	5-40	15-20	10-20	5-10	~1	<4(lab) 25-40(products)
Refresh rate (msec)	100´s	~1000	100´s	10	10´s	0.01´s	~1	500-700 per frame
Static Power	None	Very low	Very low	Moderate	None	Very low	Very low	None
Dynamic Power	Low	N/A	N/A	High	High	High	Very High	Moderate
Color	Poor	Good	Good	Good(theory)	Good(theory)	Fair	Uncertain	Good
Reflectance W=White C=Color	40% W	>48% W	70% W	55% W	70% W	45% C	>50% W	30-35% C
Matrix Drive	AM	AM/PM	AM	AM	AM/PM	PM	PM	PM
Years in development	~15	~6	~5	~13	~6	23+	~43	~20
Thickness	0.5mm(glass) 0.1mm(plastic)	N/A	0.75mm (prototype)	<0.5mm	<0.3mm	10-100 μm (typically for one iMoD-element)	<0.1mm (display can be as small as 25 μm, complete device depend on substrate)	90μm(glass) 60μm(plastic)
Maturity	Many Products	AM and PM demo	AM demo	AM demo	Segment demo	PM products	Smartcard products	PM products

Appendix B

TI EPD BoosterPack Schematic

Following is a schematic for the extension kit used to connect the EPD panel with the Arduino. Measurements are performed on J3 (including full circuit) and J4 (directly at COG)



PERVASIVE DISPLAYS 龍亭新技股份有限公司

APPROVED:	Date:	DWG NO.:
CHECKED:	Date:	PART NO.:
DESIGNER:	Date:	Rev SHEET: 3 1
DRAWER: A	Date:	Title: EPD extension board v5 TOP 01

Tuesday, February 05, 2013

Appendix C

Technical Requirements Specification

The following pages include the complete requirements specification developed as a basis for the conceptual EPD module design. It can also be found in the attached zip-file.

EPD Module Requirements Specification

Version 2.0

May 20, 2016

Table of Contents

1. Executive Summary

1.1 Project Overview

The overall project is to specify and designing a complete electrophoretic display (EPD) module, customized for a small sized optimized for low power consumption and miniaturization. A customized EPD module will be able to make a simple and low power interface between an EPD and a host MCU. By making an EPD module specified for low driving voltages, it would also provide necessary background to further explore the EPD technology and make use for it in new products powered by a single coin cell battery or energy harvesting.

1.2 Purpose and Scope of this Specification

This document specifies the functional, non-functional and hardware requirements for a complete EPD module. It will also specify necessary functions performed by the system in response of inputs and outputs. The requirements are intended to provide necessary basis for development of an EPD module, with respect to electrical properties and hardware setup.

2. Revision History

Revision	Date	Responsible	Action
1.0	April 17, 2016	S. Gunnerød	First revision
2.0	May 20, 2016	S. Gunnerød	Adapt specification for EPD module design with low voltage unipolar driving waveform.

3. Abbreviations

Following abbreviations apply to this document:

ASIC	Application-Specific Integrated Circuit
EPD	Electrophoretic Display
GPIO	General Purpose In/Out
IC	Integrated Circuit
L*	Lightness (measure for human perception of lightness, 0<L*<100)
MCU	Microcontroller Unit
PCB	Printed Circuit Board
TBC	To Be Completed

4. Product Description

The EPD module is in this content considered as the complete EPD including pixel electronics and its driving circuitry as shown in Figure 1. In order to drive the EPD pixels, a peripheral driving circuitry is required. The circuit shall be able to receive image-data from a host MCU and translate the data into proper signals to control the pixels on the EPD. The circuitry should be implemented as an application-specific integrated circuit (ASIC) in order to minimize the effective area and power consumption.

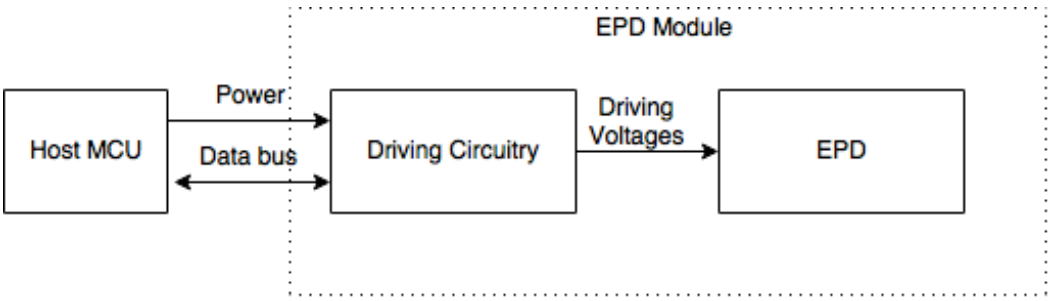


Figure 1: EPD Module Top

4.1 Product Context

The EPD module should be an independent product that interfaces with a variety of host MCUs and display sizes. The idea is to be able to control the EPD with as few external connections and discrete components as possible. Focusing on small size EPDs, more of the electronics can be integrated into a single chip, which lower the cost due to PCB-design and manufacturing as well as it reduces required area and power consumption.

4.2 User Characteristics

The EPD module is to be used as a reference by product designers and engineers that want to implement a small size, low power EPD into a new product.

4.3 Assumptions

It is assumed that the host MCU will provide all necessary signals and power as input to the driving circuitry. Types of MCUs and specific operating system/firmware details are neglected in this document, as the EPD module should be able to be operated by most MCUs that have enough processing capability to operate a traditional flat panel display. It is also assumed that memory for image frames and external components such as sensors and other components not required directly for driving the EPD are considered as peripheral units and are not integrated into the EPD module design.

4.4 Constraints

TBC

4.5 Dependencies

TBC

5. Requirements

5.1 Functional Requirements

Requirement ID	Description	Comments
FR-01	The EPD panel shall be able to be operated by a host MCU with the EPD driving flow chart presented in Figure 2. Communication interface via SPI.	EPD module require setup for input clock, slave-select/chip-enable input, serial data input and a stable input power supply.
FR-02	The EPD panel shall be able to show all kind of images or texts in black and white.	Active matrix black/white EPD
FR-03	The EPD panel shall be able to be operated in a temperature range between 0 and 50°C	
FR-04	The EPD module shall be able to drive an EPD panel with image resolution of 128 x 96 pixels.	128 output source-driver 96 output gate-driver
FR-05	The EPD module shall not consume any power when the EPD panel is in static mode (not updating).	Turn off driving circuitry after image write
FR-06	The EPD panel shall at all times and temperatures provide a white state reflectance above L*=30 during update of image.	Driving voltage (larger than): 5V/100ms.
FR-07	There shall be no visual ghosting-effect/sticking image after an image update.	
FR-08	The EPD panel shall not be able overwrite black pixels with black pixels or white pixels with white pixels.	Need to be able to compare previous image with new image and control the driving waveform in accordance to the specific image patterns.

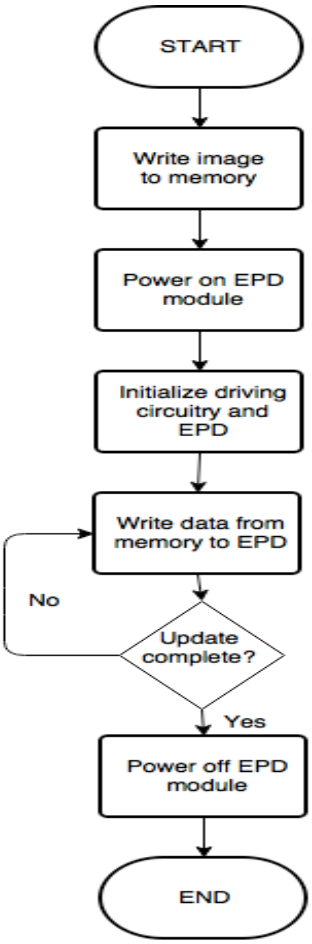


Figure 2: EPD driving flow chart [1]

5.2 Non-functional Requirements

Requirement ID	Description	Comments
NFR-01	Design priorities (most relevant): 1. Low power consumption 2. Miniaturization 3. Cost 4. Performance	
NFR-02	The EPD module should preferably be a single chip designed to be integrated on the EPD panel.	
NFR-03	EPD panel dimension shall be no larger than 40x30mm (30x22mm)	

NFR-04	Input voltage supply of EPD module shall be powered from a GPIO pin at host MCU.	Typically 3.3V or 5V
NFR-05	EPD module shall draw no more than 1mA for less than 500ms or 500µA for less than 1 second at each display update.	At room temperature = 22°C
NFR-06	The EPD module should at all temperatures consume the least possible power without any significant image degradation.	
NFR-07	The clock frequency should be limited to 8MHz.	

5.3 Hardware Requirements

Requirement ID	Description	Comments
HWR-01	The EPD panel shall be a 1-bit active matrix a-Si:H TFT panel with an image resolution of 128 x 96 pixels	Derived from FR-02, FR-04, NFR-01 and NFR-03
HWR-02	A temperature sensor shall be used to measure the temperature.	Derived from FR-03, FR-06 and NFR-06
HWR-03	A memory unit shall be able to store at least two image frames at the same time. With an image resolution of 128 x 96, this translates to a memory larger than 3072 bytes.	Derived from FR-04 and FR-08
HWR-04	EPD module requires a SPI-reciever to receive data from the master (MCU host). EPD module shall be the SPI-slave.	Derived from FR-01
HWR-05	EPD module requires a DC/DC converter to convert input voltage to TFT gates/sources, respectively ±7V and ±2.5V.	Derived from NFR-04 and HWR-01
HWR-06	EPD module requires a regulator to stabilize input voltage ranging from 3V to 5V.	Derived from NFR-04 and HWR-05
HWR-07	EPD module requires a timing controller to decode input serial data into waveforms that control and match inputs to both TFT gates and TFT sources.	Derived from HWR-01

HWR-08	EPD module require a gate driver that converts a low voltage serial waveform from the timing controller into driving voltages that provide all the TFT gates in accordance to the input waveform.	Derived from FR-04, HWR-05 and HWR-07 (Approx. ±5V higher than the source voltages)
HWR-09	EPD module require a source driver that converts a low voltage waveform from the timing controller into driving voltages that provide all the TFT sources in accordance to the input waveform.	Derived from FR-04, HWR-05 and HWR-07 (Approx. ±2.5V)

5.4 Interface Requirements

TBC

5.5 Performance

TBC

REFERENCES

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