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Design of a 20W GaN MMIC Doherty Power Amplifier for the Frequency Range 4400MHz - 5000MHz

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Abstract

The Doherty Power Amplifier architecture is becoming increasingly popular for many RF producers because of its enhanced efficiency characteristics compared to traditional amplifier classes. One major constraint of practical Doherty designs is its limited bandwidth, which is due to its use of transmission lines. At the request of Kongsberg Aerospace, methods of implementing a 20W Doherty PA to cover the frequency range 4400 - 5000 MHz was explored. To achieve this, the theoretical frequency response of transmission lines and the Doherty system was deducted using Z-parameters, and lumped component equivalents of transmission lines is proposed.

A practical Doherty PA using a Π-equivalent of the transmission line was implemented in CAD using CREE's GaN MMIC technology. The main PA of the Doherty system was implemented as a class-B amplifier, and the auxiliary PA was implemented as a class-C amplifier. A practical method of finding passive MMIC components from ideal components using Z-parameters is given, and practical restrictions of MMIC design and general PA design is also explored. The method of using small-signal analysis to design the Doherty output network using Z-parameters with the Doherty equivalent circuit is also explored, with the aim of saving time and complexity.

The finished Doherty design is given with results for the frequency band 4400 - 5000 MHz. The design was able to deliver above 18.9W RMS power across the frequency range, with a peak power of 20.3W at 4.7GHz. At saturation, the system delivers above 44% drain efficiency with a mean value of 50.6% across the frequency range. In 6dB backoff, the system delivers above 38% with a mean value of 42.2%. The system also has a power gain between 12.2dB and 13.3dB across the frequency band. A simple layout of the Doherty MMIC is given, using transmission lines as interconnects. The total area of the layout became $4.92mm^2$ with interconnects and $1.33mm^2$ without. Finally, the results are compared to other practical Doherty designs, and practical methods to improve the performance and frequency response further is given.

Sammendrag

Doherty effektforsterkerarkitekturen øker i popularitet blant mange RF produsenter, på grunn av sin forbedrede effektivitetskarakteristikk sammenlignet med de tradisjonelle forsterkerklassene. En betydelig begrensning av praktiske Doherty design er dens begrensede båndbredde, som kommer av dens bruk av transmisjonlinjer. På forespørsel av Kongsberg Aerospace utforskes derfor metoder for å implementere en 20W Doherty effektforsterker for frekvensområdet 4400 - 5000 MHz. For å oppnå dette har den teoretiske frekvensresponsen til transmisjonslinjer såvel som for Doherty systemet blitt deduktert ved bruk av Z-parametre, og ekvivalentkretser som bruker diskrete komponenter er foreslått.

En praktisk Doherty effektforsterker som bruker en Π-ekvivalent for transmisjonslinjer har blitt implementert i CAD ved bruk av CREEs GaN MMIC teknologi. Hovedforsterkeren til Dohertysystemer er implementert som en klasse-B forsterker, og auxiliærforsterkeren er implementert som en klasse-C forsterker. En praktisk metode for å finne MMIC-komponenter fra ideelle komponenter, og praktiske restriksjoner ved MMIC design og generelt effektforsterkerdesign er utforsket. Bruken av småsignalanalyse for å designe utgangsnettverket til Dohertysystemet ved hjelp av Z-parametre har også blitt utforsket, med hensikt å spare tid og kompleksitet.

Det ferdigstilte Dohertydesignet er gitt med resultater for frekvensområdet 4400 - 5000MHz. Designet var i stand til å levere over 18.9W RMS-effekt over frekvensområdet, med maksverdi på 20.3W ved 4.7GHz. Ved metning leverer systemet over 44% drain-effektivitet, med gjennomsnittsverdi på 50.6% over frekvensområdet. For 6dB backoff leverer systemet over 38% med gjennomsnittsnittsverdi på 42.2%. Systemet har også en effektforsterkning mellom 12.2dB og 13.3dB for frekvensområdet. En enkel layout for Doherty MMIC-kretsen er gitt ved bruk av transmisjonslinjer som koblinger. Arealbruken ble $4.92mm^2$ med koblinger og $1.33mm^2$ uten. Til slutt er det gitte resultetet sammenlignet med andre praktiske Dohertysystemer, og metoder for å videre øke ytelsen og frekvensresponen er gitt.

Preface

This master thesis has been developed by Børge Myran for the IME faculty at NTNU, with the problem description given from Kongsberg Aerospace. Through many hours spent with my supervisor Morten Olavsbråten and the student Jørn Frøysa, a gradual better understanding of amplifier design and MMIC design has been developed through the autumn of 2015 and spring of 2016. I would especially give a big thank you to Morten Olavsbråten for being genuinely interested in teaching me and other students RF and amplifier design.

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1 Introduction

1.1 Problem description

The master thesis was written as part of a task given by Kongsberg Defence & Aerospace AS. The projects description, translated from Norwegian, is as follows:

> Kongsberg wants an assessment of the possibility to implement a 20W Doherty PA which covers the frequency range 4400 - 5000MHz. The relative bandwidth surpasses what is managed by the traditional Doherty amplifier, but the student may simulate how large bandwidth it is possible to achieve as well as propose measures to improve the bandwidth. Kongsberg proposes to implement the amplifier in CREEs GaN MMIC technology. The task may continue in an implementation of a Doherty PA in GaN MMIC centered at 4700MHz.

1.2 Motivation

When discussing the future of radio communication, it is common to talk about *the Internet of things*, in which everyday household items would be connected to the Internet using a radio device, which means a lot more traffic through base stations and satellite communication hubs. Also, the trend across the world is that people are able to buy communication units such as phone and computers. All this means a lot more communication would be done wirelessly, both locally and globally. As signal processors develop methods to improve the bandwidth usage of signals further, with example of the LTE system using orthogonal carriers which theoretically need infinite bandwidth, hardware designers need to keep up the pace. Common for phones, base stations, communication satellites and the likes are that they contain a radio system, containing an RF amplifier. With an increasing number of devices containing a radio system, the need to improve both efficiency and bandwidth requirements becomes more stringent. At the same time, devices becomes smaller, meaning a hardware designer need to keep area usage in mind.

One good way to overcome the efficiency requirements is to use the Doherty Power Amplifier, which is a amplifier architecture used to increase efficiency, i.e. to convert more of the DC power into RF power at low RF input levels compared to traditional amplifier classes. But as the problem description states, the Doherty

PA has bandwidth limitations due to the use of transmission lines as impedance inverters.

1.3 Background

As is common for MSc students at NTNU, a semester project was conducted a semester before the master thesis. In this project [1], the author explored the theoretical concept of the Doherty amplifier using mainly [2] as a literature source, and a Doherty PA was designed at $f = 100MHz$, implementing all components but the transistor with ideal components, and ignoring any bandwidth limitations. The transistors used came from the CREE GaN MMIC foundry, chosen for their good performance at high frequencies and high power levels. The result of the semester project was an almost ideal Doherty PA with drain efficiency $\eta = 59.5\%$ at 9dB backoff. The resulting waveform showed idealized behaviour with negligible parasites and over-harmonics. In short, an ideal Doherty PA was successfully created.

1.4 Thesis Scope

Expanding on the semester project, the scope of the master thesis was to implement a Doherty PA with a center frequency $f_0 = 4.7GHz$, and with performance and behaviour optimized for the frequency band $4.4GHz$ to $5.0GHz$. The PA should be able to deliver 20W RMS output power at f_0. The main PA and the aux PA of the Doherty should be realized with a class-AB and class-C amplifier respectively. To explore the Doherty frequency response, a literature study was done where Z-parameters for transmission lines as well as the Doherty equivalent circuit was deducted, and used used in simulations. To optimize bandwidth, the parasites of the GaN MMIC transistor was found using the *Olavsbråten Parasite Model*, and these parasites was attempted used as lumped components in a small-signal analysis of the output network. Unlike the semester project, the complete Doherty PA in this thesis should be realizable, and all components was therefore implemented in GaN MMIC using the CREE foundry. This included a literary study on the foundation of MMIC, mainly using [3] as a source. The Z-parameter also became an important tool in comparing MMIC and ideal passive components.

Another MSc Electronics student at NTNU, Jørn Frøysa had a similar project description to this project, and the two of us have cooperated when writing each our reports. Some parts of the theory section may therefore therefore be similar,

if not identical in our reports.

1.5 Report overview

This report uses a quite standard setup for scientific reports, having the sections *Theory*, *Practical Design*, *Results* and *Discussion* consecutively. The Theory section aims to introduce all aspects of the Doherty PA, and should give the reader the theoretical background for all design choices made for the Doherty PA. Next, the Practical Design section gives the finished amplifier topology as well as the road to get there. Practical obstacles of realizing passive MMIC components, MMIC transistors and PAs in general is explored, with references to the theory. The stepwise implementation of the sub-networks of an amplifier are given, with an emphasis on the method of realizing the output network using transistor parasites and using small-signal analysis. Next, the Results section gives the results of the practical design. The results are given for the each sub-network, with references to the theory. Finally, the results are summarized in the Discussion section, where propositions to enhance the design further is given.

2 Theory

2.1 Impedance Matrix

Although the concept of the Impedance matrix, i.e. Z-parameters, are somewhat basic, they are an important basis when comparing MMIC and ideal passive components, as well as making a frequency analysis of the Doherty Power Amplifier. A brief summary goes here, with theory taken from [4].

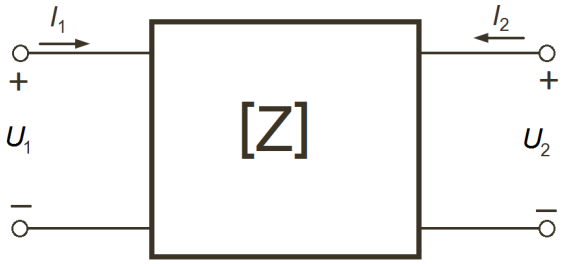


Figure 1: Generic 2-port network described by Z-Parameters

The general concept is that for a N-port network ($N = 1, 2, \ldots,$), each port have a voltage potential, U_n across the port and a current, I_n flowing into the port. This is illustrated with a 2-port in figure 1. The relation of all currents and voltages in the N-port network can be described by a NxN impedance matrix. A key point of the Z-parameters are that impedance is the relation of the voltage and current rather than the physical ohmic value, and Z-parameters can be complex. Still, the Z-parameters have the unit Ohm [Ω]. The Z-parameters can be expressed in symbolic form as $[U] = [Z][I]$, or in matrix form as

$$\begin{bmatrix} U_1 \\ U_2 \\ \cdot \\ U_N \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdot & Z_{1N} \\ Z_{21} & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ Z_{N1} & \cdot & \cdot & Z_{NN} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \cdot \\ I_N \end{bmatrix} \tag{2.1}$$

The element Z_{ij} in the matrix is found by open circuit all ports except port j, i.e. setting $I_k = 0$ for $k \neq j$, and then measure the voltage drop across port i. This is expressed mathematically as

$$Z_{ij} = \frac{U_i}{I_j}\bigg|_{I_k=0 for k\neq j} \tag{2.2}$$

2.2 Gallium Nitride (GaN)

2.2.1 Basic semiconductor theory

Gallium Nitride is a semiconducting material which is a compound of the chemical elements Gallium (Ga) and Nitrogen (N). A semiconductor is in essence a material that conducts electricity under some conditions, and not for others. This allows for active components, such as transistors and diodes. In its fundamental properties, a semiconducting material has 4 electrons in its outer electron shell, out of a total of 8 (true for the second shell and true only in basic chemistry, disregarding any quantum theory). Thus the material itself is electrically neutral. By doping the material with either electrons or holes (lack of electron) makes the material either negatively or positively charged. This slight electron inbalance makes it possible for the semiconductor to change between behaving as a insulator and as a conductor, depending on outer conditions. In the periodic table, Gallium has 3 valence electrons and Nitrogen has 5 valence electron, giving their compound 4 valence electrons before doping.

2.2.2 The GaN Advantage

The best way to explain the properties of GaN is to compare some of its basic properties to other materials, mostly semiconductors, which is done in table 1. The table are taken from a presentation slide found at [5]. The value of E_g gives the energy gap, alas band-gap, and is the range where no electrons can exist. GaN has the highest E_g-value among semiconductors in the table, which means GaN are able to support higher internal electric fields. High E_g also means it has a higher breakdown voltage compared to other semiconductors, which means GaN are able to support more W/m^2. Next, its relatively low dielectric constant, ϵ_r means lower capacitive loading, and are as a result able to support higher RF currents. Also, a lower ϵ_r value means a higher propagation speed through the device, in accordance with equation 2.33. Further, it has relative good thermal conductance, K, which means dissipated thermal power can be extracted from the device more easily. Lastly, the value of E_c gives the carrier mobility, which is also seen to be high. A higher E_c-value means electrons can move faster through the

Material	$E_g(eV)$	ϵ_r	$K(W/^\circ K - cm)$	$E_c(V/m)$
Vacuum	-	1	-	-
Si	1.12	11.9	1.5	3×10^5
GaAs	1.43	12.5	0.54	4×10^5
InP	1.34	12.4	0.67	4.5×10^5
3C-SiC	2.3	9.7	4	1.8×10^6
4H-SiC	3.2	10.0	4	3.5×10^6
6H-SiC	2.86	10.0	4	3.8×10^6
GaN	3.4	9.5	1.3	2×10^6
Diamond	5.6	5.5	20-30	5×10^6

Table 1: Comparison of semiconductors

material, which allows for a higher operating frequency without adding significant parasites. To sum up, GaN performs well over a range of variables, making it a preferred material in MMIC, where all the above mentioned parameters are important for overall performance. As GaN is not a ferromagnetic material, its relative permeability, $\mu_r = 1$.

2.3 MMIC

A Monolithic Microwave Integrated Circuit (MMIC) is as the name suggests a type of integrated circuit. The word monolithic means "single stone", and any MMIC is based on a single semiconductor material. When all passive and active components, as well as the interconnect between them are based on the same semiconductor material, any transition in the circuit becomes smooth, causing little boundary effects of the transversing EM-wave. This avoids fringe-field effect and minimize unwanted wave reflection and diffractions. The word "Microwave" indicates operation in the frequency range, typically $300MHz \leq f \leq 300GHz$. As mentioned in subsection 2.6, the characteristic impedance of a transmission line (equation 2.23) is given by its material parameters, and to achieve Z_C in the range around 50Ω for microwave frequencies, the MMIC circuits has to be small, which is generally an advantage. Typical MMIC area dimensions ranges from $1mm^2$ to $10mm^2$, though smaller and bigger chip sizes are both theoretically and practically possible [3]. For practical MMIC design, a designer needs to choose a *foundry*, which in essence is a library of components which has a number of material properties in common, and can therefore be thought of as "one technology". A foundry is inherently connected to its producer.

2.3.1 The MMIC advantage

The main advantages of using MMIC over other techniques ([3], p.6), is that it combines several important design factors. MMIC Transistors are generally high-performance, meaning they can be expected to reliably deliver high powers at high frequencies, compared to for example analog CMOS, which generally cannot reliably deliver the same high powers [3]. Another advantage is the MMIC's ability to handle mechanical impacts, making it suitable for military devices. The dimensions of MMIC are generally an order of magnitude smaller than both the *Hybrid MIC (HMIC)*, and discrete components. This allows MMIC to be used mobile electronic applications, and also decreases material cost if a large scale production is wanted. This can be a strong advantage if costly semiconducting or conducting materials are used. This also means that MMIC weigh less than HMIC or discrete, which can be an advantage in both commercial electronics as well as in space applications, where each gram of equipment may cost a multitude of dollars. Combining the above factors make MMIC an attractive technology for both commercial, military and space applications. One main drawback of MMIC is the cost of producing a wafer for a single circuit, making the "per-unit" price for small quanta large compared to other technologies.

2.3.2 Fundamental MMIC architecture

Figure 2 shows a general MMIC layout including both active and passive components. In the figure, GaAs technology is used for illustration, though the same principles apply for GaN. In the fundamental MMIc achitecture, components lie on top of a substrate, with conductive metal interconnects between them. The substrate consists of the semiconducting technology used, which allows propagation of the electric fields. Under the substrate, a conductive metal ground plane gives the circuit a reference to ground. Any component that is connected to ground in the circuit achieves this with a VIA hole connected through the substrate.

2.3.3 MMIC Transmission Lines

Transmission lines in MMIC are usually implemented as *Microstrip* Transmission Lines, with the general layout shown in figure 3. The architecture consists of a microstrip conductor on top of a substrate, and the ground plane underneath the substrate. With reference to figure 2, the interconnects between the components are done with a microstrip transmission line. For the CREE foundry, the trans-

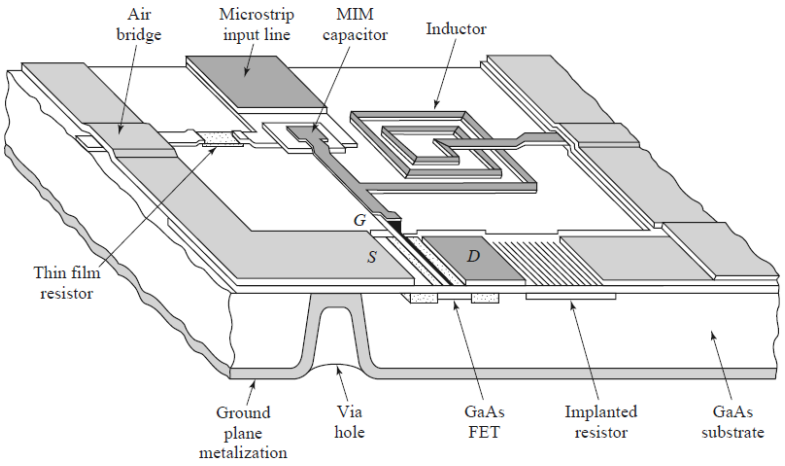


Figure 2: General MMIC layout, [4][p.550]

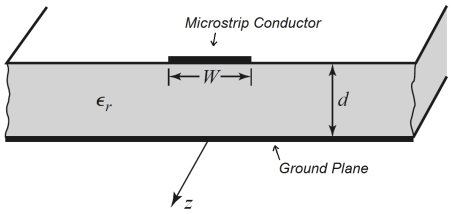


Figure 3: General Microstrip Transmission Line, [4][p.147]

mission line conductors can be implemented in two ways. Either by using just one conductor material, *Metal1*, or by reinforcing Metal1 with another conductor material, *Metal2*. For the MMIC designer, two important parameters of the conductor is its minimum width parameter and its maximum current per-unit-width parameter. These are not given here due to the confidential nature of the CREE foundry, but can be found in [6].

2.3.4 MMIC Resistors

In general, there are two ways of realizing MMIC resistors, which is either done by using the active semiconductor layer under the MMIC surface, or by laying a thin film of resistive metal on top of the surface. For both methods, the resistivity of the component is defined by the length-to-width relation, denoted, $R_{\square}$. Thus the general formula for a MMIC resistor is given in equation 2.3, with $R_{\square}$ varying between technologies. Theoretically from equation 2.3, a $20x20$um resistor has the same ohmic resistance as a $200x200$um resistor, though any size changes would yield a phase change, making the impedance of the resistor complex. Also, most

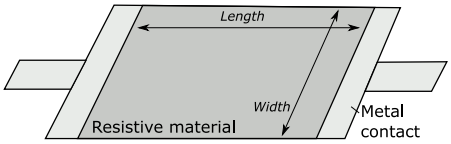


Figure 4: General MMIC resistor construction

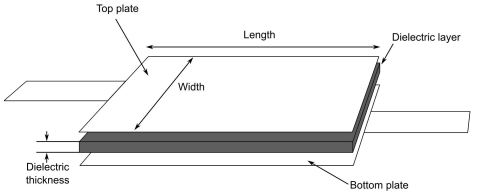
technologies has a minimum width, W_{min} value, giving restrictions to how physical small the resistor can be.

The CREE MMIC Foundry offers three different resistor type, with different resistivity. These are *Thin Film Resistor*, *Bulk GaN Resistor 1 (BGR1)* and *Bulk GaN Resistor 2 (BGR2)* respectively. [6] gives the minimum, typical and maximum value of $R_{\square}$ for the three and their W_{min} values. From [6] it's readily seen that BGR2 has the larger square resistivity, but also a larger uncertainty range, making it useful for large resistors where precision is not important. For smaller resistors where precision is more important, the thin film should be used.

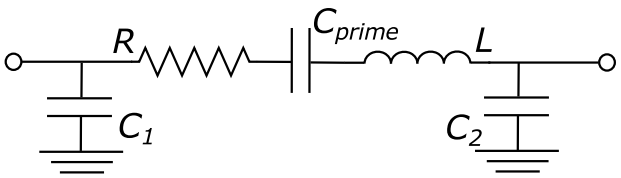
$$R_{eq} = \frac{L}{W} \cdot R_{\square} \tag{2.3}$$

2.3.5 MMIC Capacitors

As with resistors, there are generally two methods of realizing MMIC capacitors, which are *Interdigital Metal Strips* capacitor and *metal-insulator-metal (MIM)* capacitor. The interdigital capacitor uses in essence a number of fingers, spaced a certain *Finger Spacing* distance apart from each other, which in turn gives the capacitance of the component, depending of number of fingers and finger spacing. As the interdigital capacitor is not part of the Cree foundry, it's not explored in further detail here. The MIM capacitor construction is given in figure 5a, with the corresponding equivalent circuit in figure 5b.



(a) MIM construction, [3][p.45]



(b) MIM equivalent, [3][p.77]

Figure 5: Construction and Equivalent of the MIM MMIC Capacitor

In figure 5b, C_{prime} is the primary capacitance and should be much larger than the parasites C_1 and C_2. R and L gives the resistive loss and inductive parasite of the MIM. Examining figure 5a, the EM-wave has two main paths of propagation, which is either through the dielectric, or between the plate edges outside the dielectric. This in turn means that a MIM capacitor has two main sources of capacitance, which is the parallel plate capacitance C_A, and edge parasitic capacitance, C_p. C_A is dependent of plate area and has unit $[F/\mu m^2]$, while C_p has unit $[F/\mu m]$. A general formula for MMIC MIM capacitor is given as

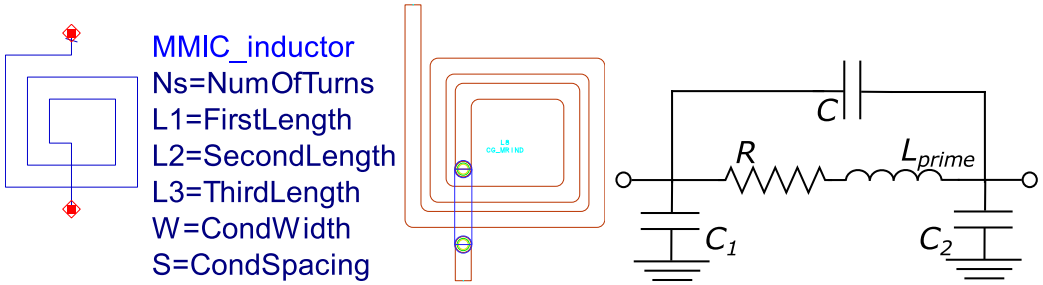
$$C_{eq} = L * W * C_A + 2(L + W)C_p \tag{2.4}$$

For many practical applications, C_p can be assumed close to zero, reducing equation 2.3 to $C_{eq} = L * W * C_A$. In the Cree foundry, no value of C_p is given, and the value of C_A is given in [6].

2.3.6 MMIC Inductors

Generally, a components ability to store current gives its inductance, and as described above, this may also occur as unwanted parasites in any conducting material. For a transmission line, the narrower the conductor width in relation to substrate height, the better its inductance. But for a high power PA, this means that the current density becomes high, and may in extreme cases overheat the MMIC, burning up the substrate. It is therefore generally hard designing inductors in MMIC, and they generally use more space than resistors and capacitors. For increased powers and currents, the resulting size of the inductor increases proportionally, making it a challenge for a PA designer. A common design method to realize MMIC inductors, and also the inductor found in the Cree foundry is the *Spiral Track* inductor, which basically is transmission lines spiraling inwards, with a bridge from the innermost conductor to the output. Figure 6a shows a schematics of the Cree inductor with some basic parameters, figure 6b shows the equivalent inductor layout and figure 6c gives the lumped component equivalent.

NumOfTurns in figure 6a gives the number of straight segments in the inductor, illustrated here with Ns = 9. As the name implies, $L1$, $L2$ and $L3$ are the first, second and third segment of the inductor, illustrated here with $L1 > L2 > L3$. W gives the conductor width and S the spacing between the conductors, illustrated here with $W > S$. Perhaps the most important conclusion of the above is that MMIC inductors contains a much larger number of variables compared to capacitors and resistors, and no single equation of width and length yield the inductance.



(a) Schematics (b) Layout (c) Equivalent, [3][p.80]

Figure 6: Illustration of inductors in MMIC

Designing inductors also requires a trade-off between increasing inductivity, satisfying $[mA/\mu m]$ demands while keeping the area low. Therefore, as a designer rule of thumb, the use of inductors should be kept to a minimum, and if capacitor can replace an inductor, a designer should do so.

2.3.7 MMIC HEMT Transistor

The general behaviour of a HEMT transistor is described in subsection 2.4. In the CREE foundry, a number of HEMT transistors exists for the designer to choose from. The details of the CREE foundry transistors are not explained in detail here, but in subsection 3.5 the choice of transistor for this project is given with an explanation of some HEMT parameters. In essence the HEMT MMIC has two main parameters to define its size, and corresponding $I_{D,max}$. These are the number of gate fingers, Ngf, and Wg, the length of each gate finger. These are illustrated in figure 7 with Ngf $= 4$. Figure 7 also gives an illustration of the parasites given schematically in figure 11. The Gate parasites are omitted for readability.

2.3.8 The Olavsbråten Parasite model

As shown in figure 11 and 7, a general HEMT MMIC transistor have a variety of parasitic effects occurring when applying voltages and currents to the transistor. These can be modeled with lumped components and a general parasitic model for a FET transistor is shown in figure 11. When designing both input and output networks of an amplifier, as described in subsection 2.5, the parasites can be useful as circuit elements if they correctly portray the equivalent effect of an lumped component. To find the equivalent lumped component values of the parasites, a model

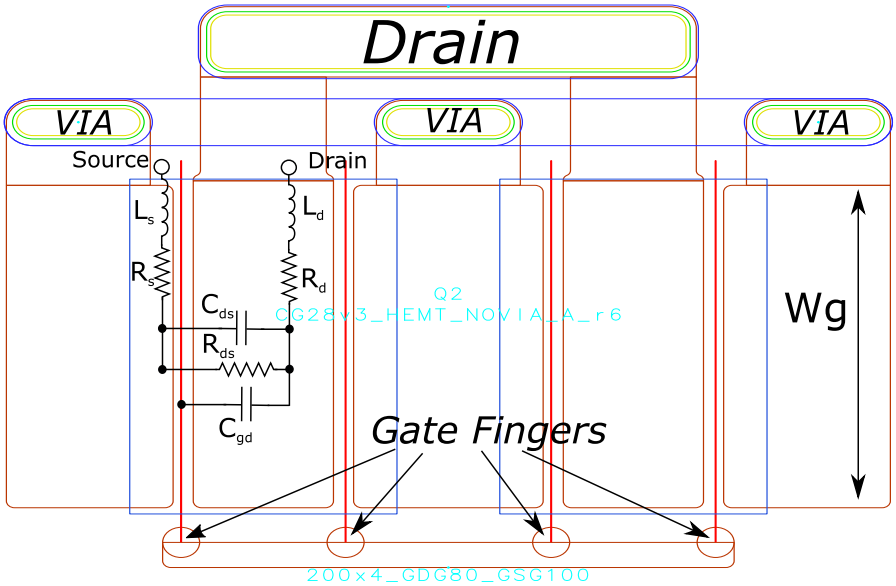


Figure 7: General HEMT layout with parasites illustration

was created by Morten Olavsbråten which gives the values of the components. This is shown in figure 8, with the circuit symbol given in figure 9.

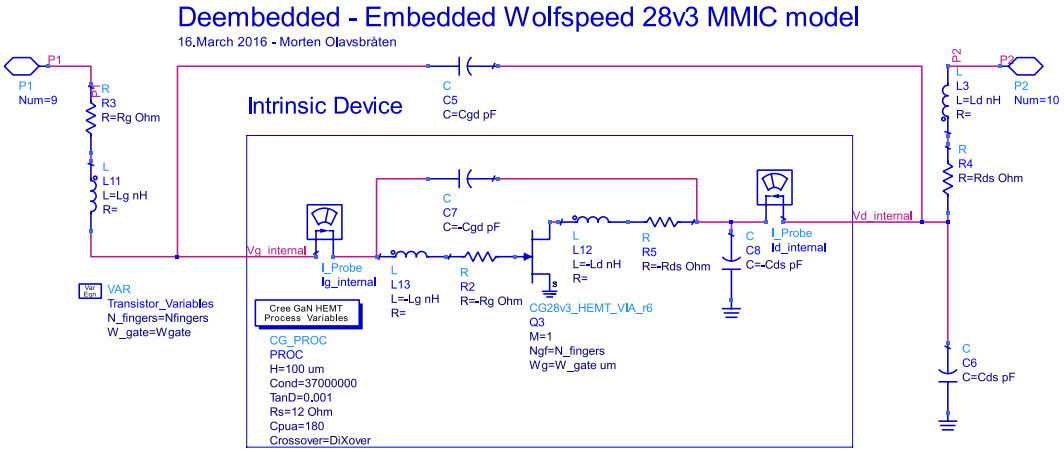


Figure 8: The Olavsbråten Parasite Model circuit

The idea behind the model is that the parasites are dependent on transistor geometry, and for the most part, independent of frequency. As an MMIC HEMT transistors geometry are mainly dependent on the number of fingers, $N_{fingers}$, and the width of each finger, W_g, equations could be developed for $L_g, R_g, C_{gd}, C_{ds}, R_d$ and L_d, all dependent only on geometry. These equations are not written here due to their confidential nature, but can be found in [6]. The method in find-

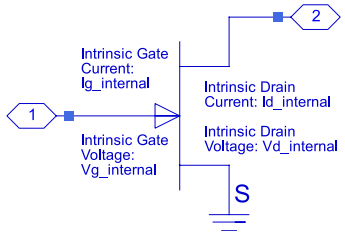


Figure 9: The Olavsbråten Parasite Model symbol

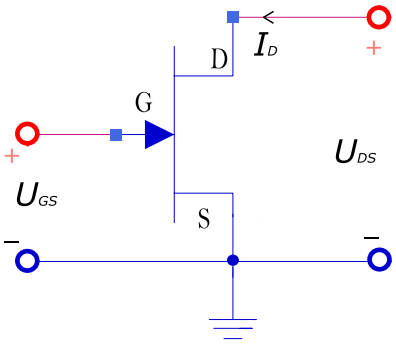


Figure 10: FET Transistor circuit element

ing these values exploits the CADs possibility to use negative component values. Adding a negative resistor or inductor in series, or a negative capacitor in shunt effectively eliminates the the parasites of figure 11. Thus by consecutively adding negative components, a designer should be left with only the ideal voltage controlled current source in figure 11. The Olavsbråten model of figure 8 omits some parasites for simplicity, and can not be seen as a complete model. Specifically, the CG28v3_HEMT_VIA_r6 transistor model creates a VIA-hole directly to ground, not allowing any manipulation of the Source node.

2.4 Transistor Design

2.4.1 FET Transistors

The *Field Effect Transistor (FET)* is a transistor type that uses an electric field to control the electrical conductivity of a channel. Put in other terms, a FET uses an applied voltage to control the flow of current through the channel. Figure 10 shows the circuit symbol of a FET, where the *Gate Voltage*, U_{GS} controls the flow of *Drain Current*, I_D through the channel. I_D is in turn inherently connected to

the *Drain-to-Source Voltage*, U_{DS} across the transistor. The I_D-U_{DS} relation can be modeled by a *Loadline Resistor*, R_{OPT}, and a FET transistor can therefore be modeled as a variable resistor. Many sub-types of FET exist, and one of these is the *High-Electron-Mobility Transistor (HEMT)*, which were used for this project. More detailed explanation of the channel construction and properties of the HEMT is given below.

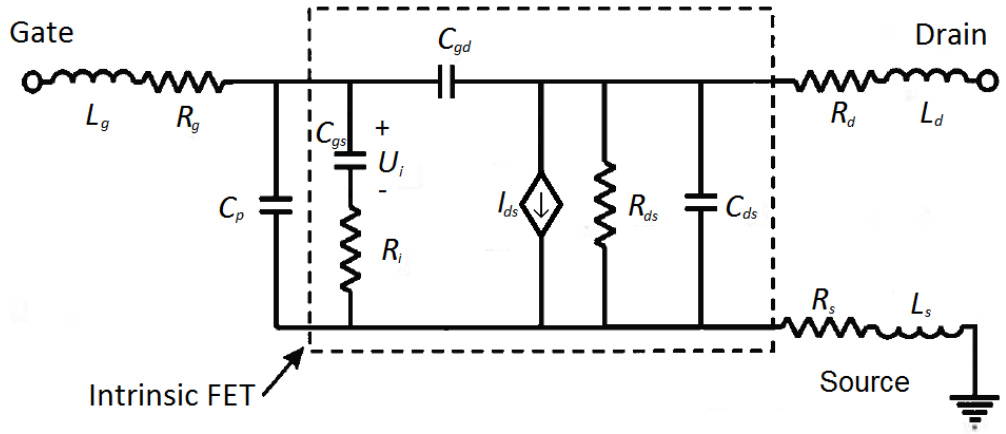


Figure 11: FET equivalent circuit, taken from [3]

Figure 11 gives an equivalent circuit of the FET, with the corresponding parasites. A parasite is any lumped component equivalent to model the physical behaviour of a component. Any loss or phase change can therefore be modeled by lumped components. The intrinsic FET parasites are fundamental in the overall component architecture, and it's neither possible nor desirable to remove them, only to adjust them for wanted behaviour. It may therefore be confusing to call them parasite, as the word implies they are unwanted. The components outside the intrinsic FET can be removed in practical applications if perfect conductors, semiconductors and isolators are used.

2.4.2 HEMT

The following theory are taken from [5], mainly from the PHD-thesis [7] found on the website. HEMTs, also known as Heterostructure FET (HFET), are field effect transistors which uses the junction between two materials with differing band gap levels as conduction channel, rather than using regions of doped versions of the intrinsic material. The combination of Gallium arsenide (GaAs) and Aluminium gallium arsenide (AlGaAs) is quite common, but Gallium Nitride and Aluminium Gallium Nitride is growing in popularity due to their ability to handle higher

power. An illustration of a GaN/AlGaN HEMT is shown in figure 12. The 2DEG abbreviation stands for 2-dimensional electron gas, which forms due to free electrons wandering from the AlGaN layer, down to the GaN layer due to the lower energy band level of GaN. This gas, or plasma, is free to move in any direction but vertical, and helps improve the gain of the transistor at high frequencies. Figure 13 shows the energy bands for the first two layers in an section under the gate.

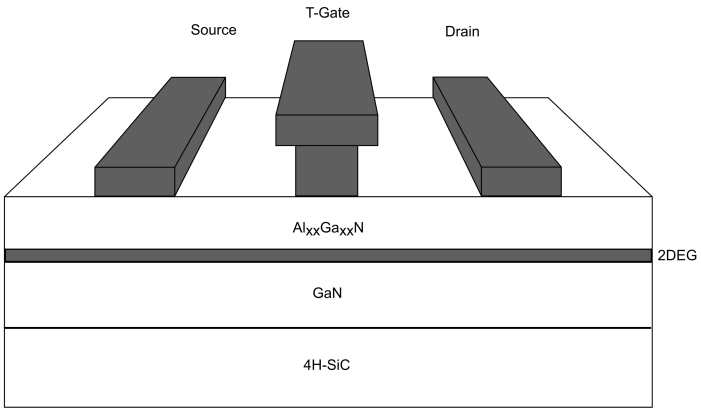


Figure 12: Cross section of a general HEMT transistor

The conduction band, E_c, and the valence band, E_v, represents the two energy states the electrons can have. The area between them are energy states the electrons cannot have. The fermi-level, denoted E_f is the highest energy level containing an electron. Semiconductor technology is based on having the fermi-level between these two bands. As the valence band is entirely below the fermi-level, the electrons there are unable to move. Similarly there is no current due to the conduction band either as the fermi level lies entirely beneath it. In HEMT transistors there is a portion of the conduction band which dips below the fermi level, which means there will be free electrons present even when no voltage is applied. This dip is caused by the increased number of electrons in that part of the cross section. The electrons moving from the AlGaN layer "sees" a high net negative charge, and their energy is therefore increased, leading to the heightened tip just before the dip. The dip itself is formed by the electrons in the GaN section observing an abundance in positive charge carriers from the donors in the AlGaN material, which reduces the electrons energy.

As energy is delivered to the materials from an increasing input signal E_f rises, causing more and more electrons to enter the conduction band. The transistor will quickly begin conducting current as the electrons in the 2DEG is already free.

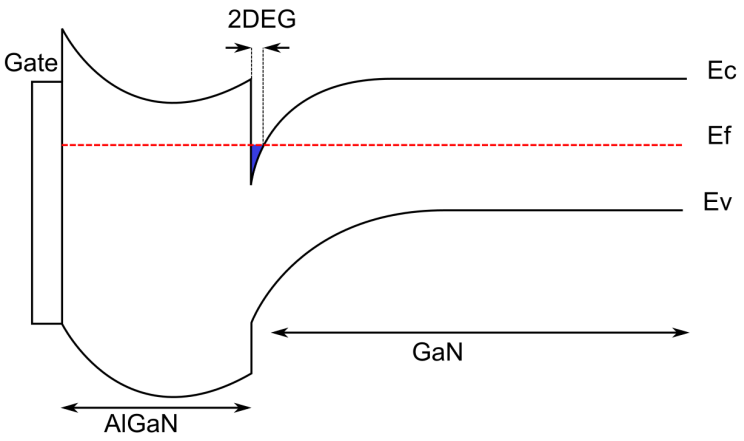


Figure 13: Energy bands of a general HEMT transistor

2.4.3 Transistor biasing and amplifier classes

Transistors are the most fundamental component in most amplifier design. Though possible, it is difficult to obtain amplification of oscillating signals without using transistors. As an example, the original Doherty design was made using vacuum tubes for amplification. Diodes, and other active components can both in theory and practice be used to achieve amplification, but transistors are by far the most used component used for RF amplification due to its semiconducting ability to convert DC power into RF power. A detailed explanation of amplifier functionality is given in detail in subsection 2.5, but a brief explanation of how to bias transistors to achieve different amplifier classes goes here.

In an amplifier, the input RF signal, u_{in} lies across the Gate node, as shown in figure 10 . Between the Drain and the Source nodes lies a DC voltage U_{dc} which allows the semiconductor to operate. By applying a DC Bias voltage, U_{GS} to the Gate, the super-positioned gate voltage becomes $u_{GS} = u_{in} + U_{GS}$. By adjusting the DC value of U_{GS}, one can control the current I_D flowing from Drain to Source. Given an sinusoidal u_{in}, this control of I_D gives various functionality of the transistor, which commonly are divided into amplifier classes. The most common amplifier classes are -A, -AB, -B and -C. Figure 14 shows a DC simulation of a FET transistor, and for a given geometrical size, a transistor is capable of delivering I_{max} from Drain to Source. Figure 14 shows the bias point of a class-A and a class-B amplifier, with its resulting effect on I_D and U_{DS}. Using the normalization $U_q = (U_{GS} - U_{GS,min})/(U_{GS,max} - U_{GS,min}$, U_q for a class-A amplifier is 0.5, which allows both I_D and U_{DS} a full swing between its peaks. A full swing

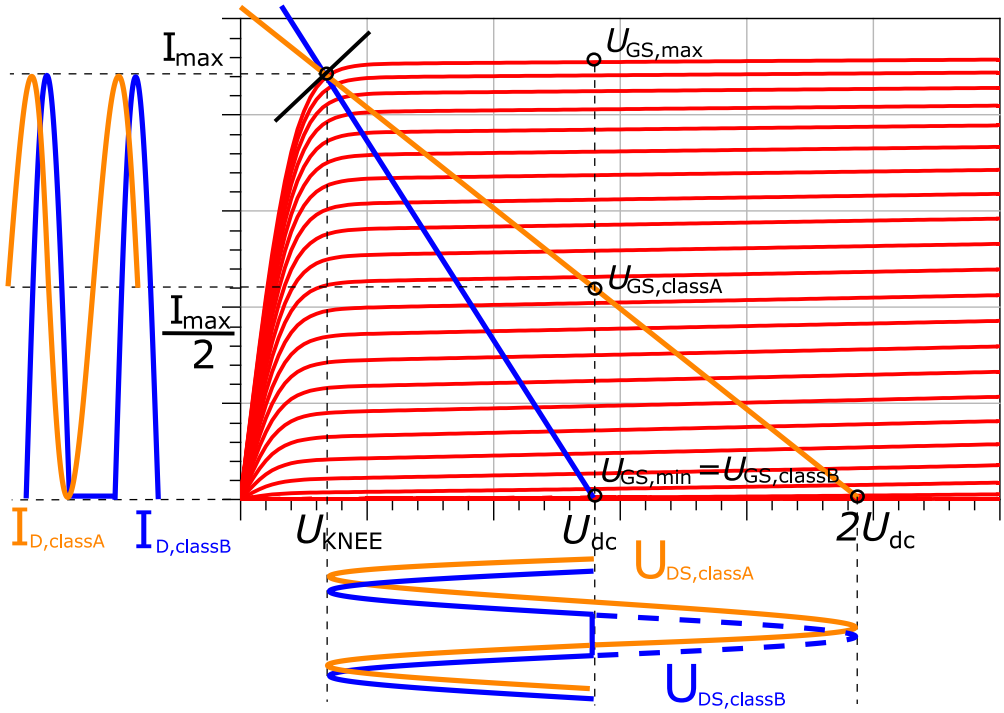


Figure 14: I-V cures and loadlines of FET transistors

indicates that the whole sinusoidal period has been conducted by the transistor. This is measured by the *Conduction Angle*, α, given as 2π for a class-A amplifier. A class-A amplifier is therefore said to be the most linear amplifier, as the output is a linear multiplication of the input. Next, the class-B biasing point gives $U_q = 0$. As a transistor cannot conduct current in its cur-off region, only the positive half-period of I_D and U_{DS} are conducted, thus making $\alpha = \pi$. Though only half the period is conducted, the resulting amplitude of I_D for a class-B amplifier is readily bigger compared to its class-A counterpart. This means a larger RMS value on the output current, meaning more of the DC power has been converted to RF power. As will be discussed in subsection 2.5, the ratio of DC power to RF power in an amplifier is measured by its *efficiency*, η, and an important advantage of class-B amplifiers over class-A amplifiers is the higher efficiency. It is also possible to bias the transistor such that $U_q < 0$, which means $\alpha < \pi$ and resulting in a even higher efficiency. This is called class-C operation. It is also possible to bias the transistor between class-A and class-B operation, which is called a class-AB amplifier. The theoretical properties of the different amplifier classes are summarized in table 2

Class	U_q	$\overline{I_{dc}}$	α	η
A	0.5	0.5	2π	50%
AB	0-0.5	0-0.5	$\pi - 2\pi$	50-78.5%
B	0	0	π	78.5 %
C	< 0	0	$0 - \pi$	78.5-100 %

Table 2: Amplifier classes fundamental properties

2.4.4 Loadline Theory and Output Power Design

Figure 14 reveals several important transistor properties. For one, it can be found graphically that the $2U_{dc}$ point is not twice of U_{dc} but rather $2(U_{dc} - U_{\text{KNEE}})$ The KNEE-effect is a physical limit where the transistor transitions from the linear to the saturation region. As shown in figure 14, U_{KNEE} puts a restriction on the voltage swing, and therefore also the output power. If a transistor is fed higher input power levels in saturation, the current will decrease from its I_{max}-value rather than stay in saturation. This is called the *KNEE-walkback* effect, where the current follows the I-V curve back towards the origin. A measurement of the ratio of U_{KNEE} to I_{max} is R_{ON}, given in equation 2.5. R_{ON} is a important factor for a PA designer as a lower value indicates that a larger voltage swing is possible, resulting in a larger output RF power.

$$R_{ON} = \frac{U_{\text{KNEE}}}{I_{max}} \tag{2.5}$$

Next, the ratio of I_D to U_{DS} for the different amplifier classes can be described by its loadline. The loadline for a class-A and class-B amplifier are both given in figure 14, and its readily seen that the class-B loadline has a higher negative slope than the class-A loadline. As the loadline gives the relation between I_D and U_{DS}, this can be inverted be become a resistance value. Given the slope, the resistance value is given as $R_{OPT} = -1/slope$. This can be put into more practical terms in relation to I_{max} and U_{dc} as

$$R_{OPT} = \begin{cases} \frac{2U_{dc} - U_{\text{KNEE}}}{I_{max}} \approx \frac{2U_{dc}}{I_{max}} & \text{Class-A operation} \\ \frac{U_{dc} - U_{\text{KNEE}}}{I_{max}} \approx \frac{U_{dc}}{I_{max}} & \text{Class-B operation} \end{cases} \tag{2.6}$$

The reason for denoting it R_{OPT} is that as long the transistor operates in the linear region, the transistor can be modeled as a resistor of value R_{OPT}. Basic

circuit theory gives max power transfer when $R_L = R_{in}$, and a PA designer needs therefore to design the transistor output network for R_{OPT}. Last, when designing an amplifier according to an output power specification, with $P_{O,max} = 20W$ given for this project, finding the optimal R_{OPT} is a necessary starting point. A common method for designing an transistor for output power is to assume class-A operation, and calculate the DC power in this point. With respect to Figure 14, the bias point of a class-A amplifier is $U_q = 0.5$. Therefore, the maximum output RMS power of which to design the transistor is given in equation 2.7.

$$P_{OPT} = U_{dc,peak}\frac{I_{max,peak}}{2} = \frac{I_{max}U_{dc}}{4} \tag{2.7}$$

2.5 Amplifier Design

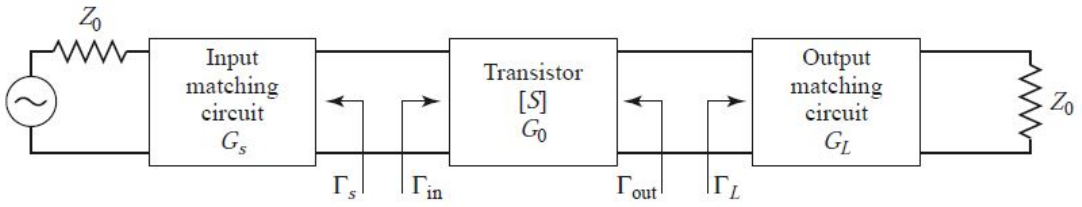
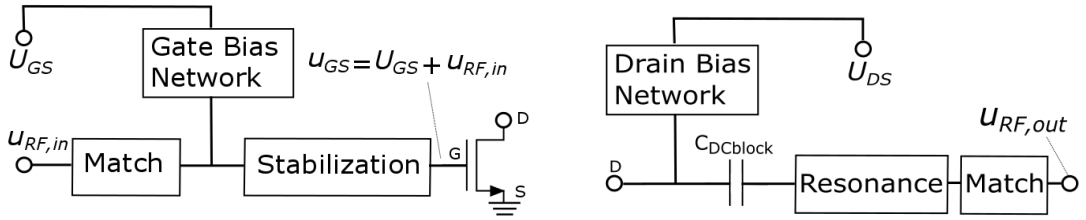


Figure 15: General amplifier circuit [4, p.198]

An amplifier is a device that, when given an input signal, produces an amplified version of the signal by converting DC power to AC power. At the heart of this operation is the transistor, a non-linear device which conducts differing amounts of current based on an input current (BJT) or voltage (FET). By careful design of the surrounding circuitry, a stable amplifier with the desired characteristics can be achieved. With respect to Figure 15, 16a and 16b, there are four main modules needed in most amplifier circuits. These are *stability circuit*, *input match*, *output match* and *resonant tank*. Additionally, the Bias networks need reactive components to avoid RF leakage into the DC source, and the output network also need a reactive component to avoid DC leakage to the RF output, illustrated with $C_{DCblock}$. Figure 16a and 16b show one of many possible topologies for an amplifier. As an example, it is possible to move the stabilization network to the Source node, and a feedback from the Drain node to the Stabilization network is also possible. Figure 16a and 16b are thus only illustrations of a typical amplifier, and should be treated as such.



(a) Typical input network (b) Typical output network

Figure 16: Generalized amplifier sub-networks

2.5.1 Stability

Amplifier stability is dependent on signal frequency and load impedance, and therefore be calculated from the amplifiers S-parameters. An unstable amplifier will uncontrollably produce large amounts of power at a certain frequencies which, that the designer cannot control This will reduce the amount of power that can be generated at the desired frequency as well as potentially damage the amplifier or load circuitry. It is common to differentiate between two states of stability, *conditional* and *unconditional*. A conditionally stable amplifier is only stable for certain frequencies and load impedances, making it generally unwanted. If used it must be designed with great care and only to be used in specific applications where stability is ensured. An unconditionally stable amplifier is stable for all frequencies and load impedances. Instability occurs when the input or output impedances of the transistor has a negative real part, causing oscillation. This would equate $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$ in Figure 15. Since these reflection coefficients are dependent on Γ_S and Γ_L the stability of the amplifier is dependent on the source and load networks. Thus, from [4] the following conditions must be satisfied for unconditional stability.

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.8a}$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{2.8b}$$

Where S_{xx} refers to the scattering matrix parameters of the transistor, when the transistor is viewed as a 2-Port network. As long as the device is bi-lateral, equations 2.8a and 2.8b represents a range of values for which the amplifier is stable. These values can be used to create stability circles which can be plotted in a Smith Chart. The circles then represents impedances for which the amplifier is stable, or

unstable. By setting the above equations equal to 1 and manipulating them algebraically, it is possible to deduct equations for *Stability Circles*, giving its radius and center point. Stability circles can be made for both the source and the load of the amplifier circuit, and in general, impedances and reflection coefficients within the stability circles in the Smith Chart gives the values where the amplifiers are potentially unstable. Thus, the clue is to create circuitry such that both the source and load stability circles are completely outside the Smith Chart of the source and load reflection coefficients. Further deduction of the stability circles are omitted here.

While stability circles gives a good indication when deciding on, and tuning for a stabilizing network, they are mathematically complicated if only a simple indication for stability is necessary. One suitable mathematical tool then is the K-factor, or stability factor, which shows wether the device is unconditionally stable if Rollet's conditions, given in equation 2.9, are both satisfied for all frequencies.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.9a}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.9b}$$

While the K-factor does indicate whether or not a device is unconditionally stable it does not indicate how stable the device is. A measurement of stability which does have this property are the μ-factors.

$$\mu_{prime} = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^*\Delta| + |S_{21}S_{12}|} \tag{2.10a}$$

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*\Delta| + |S_{21}S_{12}|} \tag{2.10b}$$

Where μ_{prime} is the distance from the center of the Smith Chart to the nearest source stability circle and μ is the corresponding factor for the load side. As long as $\mu_{prime} > 1$ and $\mu > 1$ the amplifier is unconditionally stable, and the larger the number is, the more stable it is. μ_{prime} and μ are often denoted as μ_{source} and μ_{load} respectively, which is also the preferred notation used in this text.

2.5.2 Input match - max voltage gain

An amplifier can be designed for different purposes. Characteristics of the amplifier is largely decided by the transistor, and the impedances it observes. Manipulating these impedances will change the current-voltage ratio, affecting power, noise figures, efficiency and gain. The gain of the system in Figure 15 can be found as

$$G_T = G_s G_0 G_L \tag{2.11}$$

where

$$G_S = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}\Gamma_S|^2} \tag{2.12a}$$

$$G_0 = |S_{21}|^2 \tag{2.12b}$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.12c}$$

Maximum *voltage* gain will be achieved by ensuring a conjugate impedance match between the transistor and the source and load matching networks, such that

$$\Gamma_{in} = \Gamma_S^* \tag{2.13a}$$

$$\Gamma_{out} = \Gamma_L^* \tag{2.13b}$$

Since a transistor is a bilateral device, Γ_{in} is affected by Γ_{out} and vice-versa, and the two must be matched simultaneously. We have

$$\Gamma_S^* = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.14a}$$

$$\Gamma_L^* = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.14b}$$

An ideal transistor is uni-lateral, with $S_{12} = 0$ which makes $\Gamma_S^* = S_{11}$ and $\Gamma_L^* = S_{22}$. The idea for creating maximum voltage gain at the input match is therefore to create circuitry such that $S_{11} \to 0$. Since an incident voltage wave of a lossless two-port amplifier must either be reflected, given by S_{11} or transferred to port

2, given by S_{21} then making $S_{11} \to 0$ increases S_{21} proportionally, resulting in a higher voltage gain for the transistor. Since this model for gain does not take the I-V characteristics of the transistor into consideration, and only its small-signal response, the voltage gain of an amplifier is sometimes referred to as its small-signal gain.

2.5.3 Output Match - Max Power Gain

In basic circuit theory, given a Thévenin equivalent of any circuit, maximum power transfer to a load impedance occurs when the load impedance is equal to the thévenin impedance, $Z_L = Z_{Th}$. As discussed in subsection 2.4, optimal power gain is obtained when the loadline of the transistor allows for maximum voltage and current swing. Still, the loadline of a transistor is determined by the load impedance seen on its output. Therefore, maximum power transfer happens when the load impedance is equal to optimal loadline resistance, $Z_L = R_{OPT}$. Thus an output matching circuit needs to manipulate the impedance seen by the transistor to match the load impedance. This can be done by a $\lambda/4$ transmission line with characteristic impedance $Z_0 = \sqrt{R_{OPT} \cdot Z_L}$. As discussed in subsection 2.6, this can also be achieved with a lumped components equivalent.

2.5.4 Resonance

For an amplifier designed around a center frequency, f_0, it is common to have a bandpass filter on the amplifier output which is resonant for the frequency band around f_0, and is short circuited for all other frequencies. Ideally, this will short circuit all over-harmonic created by both non-linearities in the transistor as well as from saturation, and will therefore increase the linearity of the amplifier. Still, as discussed below, distortions products which lie in the f_0-band cannot be removed by the resonance network. Being a bandpass filter, the resonance network is typically a CL-circuit parallel to ground, and can also be implemented using transmission lines.

2.5.5 Non-linearities and Intermodulation Distortion Products

Generally, the characteristic of the transistor can be divided into three: Cut-off, linear region and saturation. In the cut-off region the Gate-Source voltage v_{GS} is too small, and the transistor does not conduct current. In saturation, v_{GS} is so

large the transistor cannot deliver enough current. Between these two extremes is the linear region, where the output signal is approximately a linear function of the input. An amplifier operating purely in the linear region such as the class-A amplifier will, in theory, amplify the signal without changing it. In reality any real transistor of any amplifier class will create distortion and a multitude of non-linear signals on its output. These signals will interfere with each other, and can be represented mathematically as over-harmonic signals. These harmonics will alter the shape of the output signal, and divert power away from the fundamental frequency. Generally, the output signal of an amplifier can be represented by an infinite Taylor series

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + ... \tag{2.15}$$

A common test to check how non-linear a device is, is the two-tone test. By applying an input signal $v_{in} = A(\cos(\omega_1 t) + \cos(\omega_2 t))$, with $\omega_1 < \omega_2$ and $\omega_2 - \omega_1 \approx small$. Figure 17 shows the spectrum of a two-tone test on a non-linear device, which is found by inserting v_{in} into equation 2.15, and manipulating the resulting equation algebraically. When calculating the trigonometric product of the third-order distortion, shown as $a_3 U_{in}^3$ in equation 2.15, the resulting equation will contain the frequency components $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, which lies close to the fundamental harmonics. These are called *Intermodulation Distortion (IMD) Products*, which are a fundamental aspect of understanding non-linearities in an amplifier. All odd-order distortion products will create IMD-products that interferes with and distort the fundamental harmonic, in the same way all even-order distortion products will affect DC. In the linear region the harmonic components will ideally be very small, but if the transistor is in the saturation region, the over-harmonic components will quickly grow in size. It is worth noting that all the above-mentioned theory is just a mathematical approach to real-life physical effects that takes place at an atomic level in the non-linear device, and would best be understood by analyzing the electromagnetic waves in the semiconductor material.

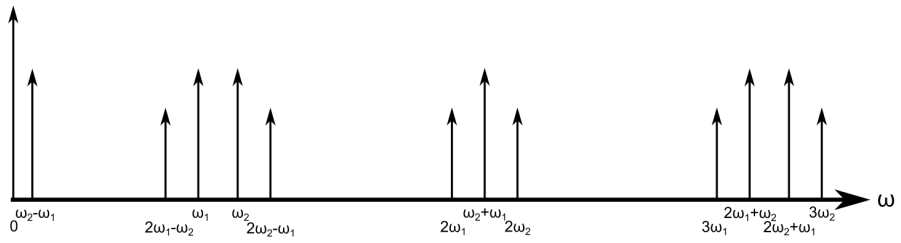


Figure 17: Frequency components of a two-tone test[4, p.101]

Figure 18 shows the 1dB compression point for a non-linear amplifier. At this point, the output power is 1dB lower than it would be if it were allowed to continue to follow the linear characteristic. The 1dB compression point is an important concept for amplifier designers because it indicates the point at which the transistor goes from the linear to the saturated region. Figure 18 also shows the cubic response of the third-order distortion product, which also has a slope of 3 in the dB-domain. The point at which the third-order products becomes of comparable magnitude to the linear response, is where compression takes place. Thus another method of defining the transition from the linear region to the saturation region is the third-order Intercept Point (IP), as shown in Figure 18.

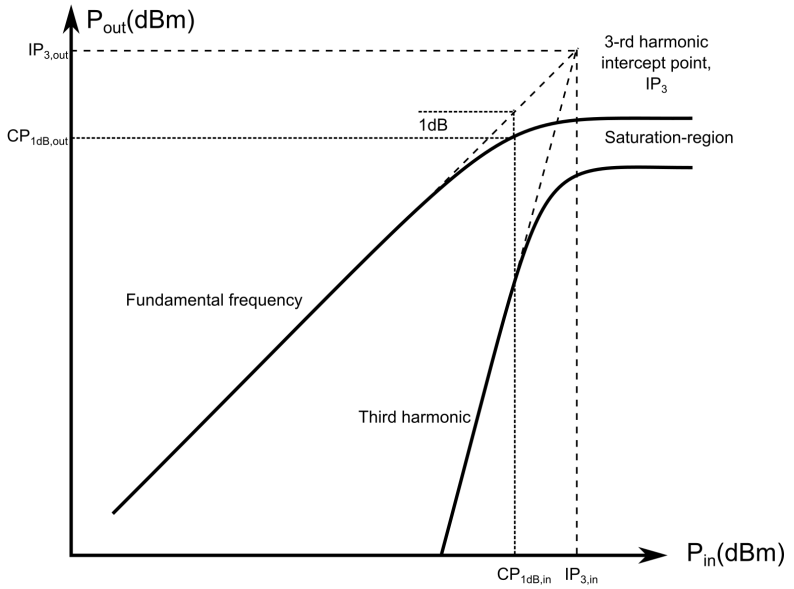


Figure 18: P_{out} vs P_{in} with compression point illustrations

2.5.6 Efficiency

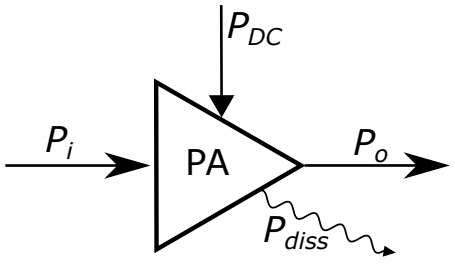


Figure 19: Basic power budget of a Power Amplifier

The basic power budget of a PA is shown in figure 19, where input RF power is amplified to output RF power with the help of DC power. Any power not delivered to P_o can be regarded as dissipated power, usually in the form of excess heat, alas thermal power. To measure the ratio of P_{diss} to P_o, it is common to use *efficiency* measurements. Equation 2.16a gives the drain-efficiency. η and is the ratio between output power, and the total input DC power. This definition is widely used, but is inaccurate for amplifiers with low gain where the input signal is large [4]. A more complete definition is the Power Added Efficiency (PAE), given in equation 2.16b. Here the input power is subtracted from the output power, giving a more correct magnitude for the RF power. Note that if the input signal is very small compared to the output signal, meaning the gain is high, then equation 2.16b reduces to equation 2.16a. A drawback of PAE is that it may become negative if $P_i > P_o$, which may occur for increasing P_i in deep saturation. Still, a negative efficiency is un-physical in nature. Examining the power budget of figure 19, it is readily seen that $P_i + P_{DC} = P_o + P_{diss}$, thus a less used but perhaps more precise measurement of efficiency is the $\eta_{Overall}$, given in equation 2.16c. One important property of $\eta_{Overall}$ is that its never negative, making it more practical than PAE for some applications.

$$\eta = \frac{P_o}{P_{DC}} \tag{2.16a}$$

$$PAE = \frac{P_o - P_i}{P_{DC}} = \left(1 - \frac{1}{G}\right)\frac{P_{out}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\eta \tag{2.16b}$$

$$\eta_{Overall} = \frac{P_o}{P_i + P_{DC}} = \frac{P_o}{P_o + P_{diss}} \tag{2.16c}$$

2.5.7 Class-F Amplifier

Beyond the traditional amplifier classes, which are only defined by their Bias point, several modified classes or sub-classes exists. One of these are the class-F amplifier, which is a modified class-B amplifier which uses the over-harmonics to achieve higher efficiency. The basic concept is that by adding odd-harmonics to the voltage and even-harmonics on the current, the peak amplitude is reduced and the transistor voltage U_{DS} can be driven harder, allowing more of the DC power to be converted to RF power at high input drive levels. The theory explained here are taken from [2][p.143].

Figure 20 shows the waveform of $V = \cos(\theta) - V_3\cos(3\theta)$ for various values of V_3. A generic input signal with fundamental and third harmonic can be given as

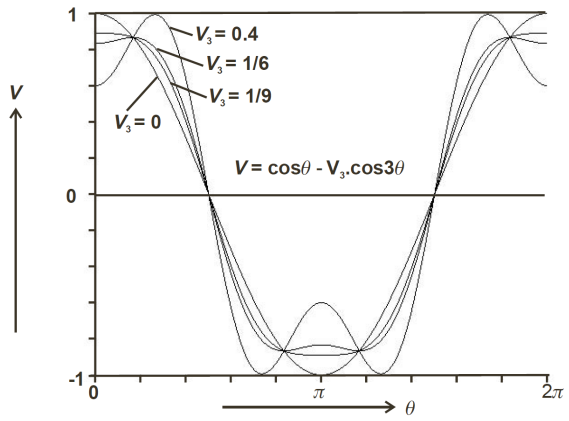


Figure 20: Third harmonic squaring effect, [2][p.143]

$$v(\theta) = V_1 \cos(\theta) - V_3 \cos(\theta) \tag{2.17}$$

Then, any value of $V_3/V_1 < 1/9$ yields a single amplitude peak, given as $V_{pk} = (V_1 - V_3)$, while values of $V_3/V_1 > 1/9$ yields a double peak. Both of which are shown in figure 20. The value of the double peak decreases up to the global maximum point of $V_3/V_1 = 1/6$, to which V_{pk} reaches its global minimum point of

$$V_{pk} = \frac{\sqrt{3}}{2} V_1 \tag{2.18}$$

For V_3 values higher than $V_1/6$, the amplitude of the waveform increases. Thus by only adding the 3rd order harmonic, a maximum possible amplitude decrease given by equation 2.18 can be achieved. By deducting equation 2.17, it can be seen that for V_3 values of $0 \leq V_3 \leq V_1/2.5$, the corresponding waveform amplitude are decreased by a factor κ, making $V_{pk} = \kappa V_1$. This makes the maximum possible amplitude increase from $V_{max} = V_1$ to $V_{max} = V_1/\kappa$. The increased value of V_{max} allows more of the DC power to be converted to RF power, yielding a maximum theoretically drain efficiency of $\eta = 90.7\%$. Dependency of η and its corresponding potential increase of P_{out} to the 3rd harmonic amplitude V_3 are given in figure 21, where the amplitude is normalized as $v_3 = V_3/V_1$.

2.5.7.1 Maximal flat waveforms Adding the odd over-harmonics naturally alters the waveform of both the voltage and current across the transistor. As explained above, values of $V_3 < V_1/9$ yields single peaks while $V_3 > V_1/9$ yields

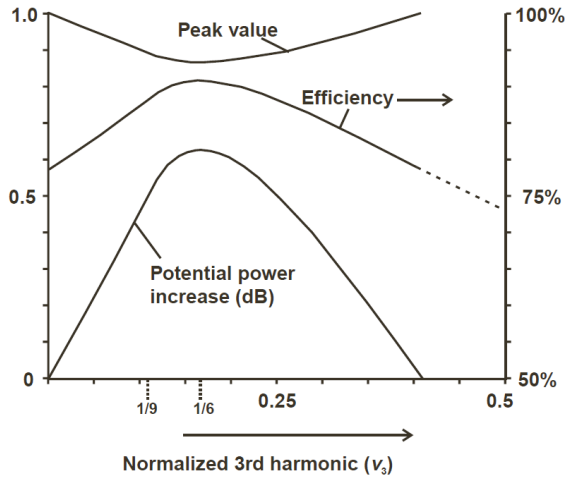


Figure 21: Reduction in amplitude, with corresponding efficiency and increased $P_{out,dB}$, [2][p.145]

double peaks. Thus the case $V_3 = V_1/9$ is the maximal flat waveform possible only using 3rd harmonics, yielding $\kappa = 8/9$ and $\eta = 88.4\%$. The voltage and current waveform of this values are given in figure 22, and these waveforms are interesting as they may occur unintentionally, as will be seen in section 4

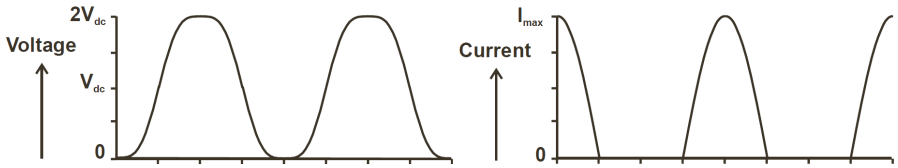


Figure 22: Voltage and current waveform for $V_3 = V_1/9$, [2][p.145]

2.5.7.2 Higher order odd-harmonics Theoretically its possible to add any number of odd over-harmonics to achieve a perfect square voltage signal, which would increase the maximum possible peak amplitude to $V_{max} = (4V_1)/\pi$, giving $\kappa = \pi/4(\approx 1dB)$. The mathematical deduction of the signal using higher order odd harmonics are similar to the above, but for sake of simplicity, the most important results are given in table 3 [2], where the normalized odd harmonic amplitudes are given together with the potential increased power in dB and the corresponding efficiency. The table only gives up to 4 odd over-harmonics, but adding a infinite number would yield $\eta \to 100\%$.

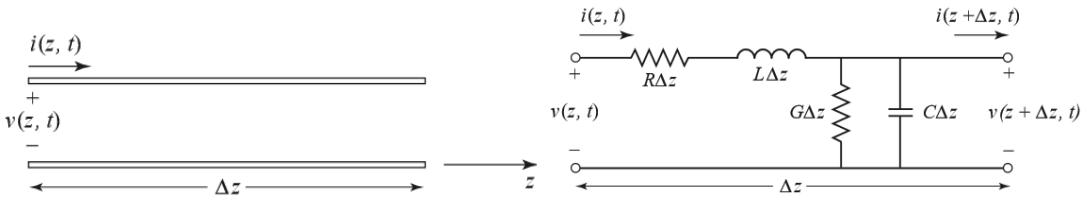
v_1	v_3	v_5	v_7	$P(dB)$	$\eta[\%]$
1	-	-	-	0	78.5
1.155	0.1925	-	-	0.625	90.7
1.207	0.2807	0.073	-	0.82	94.8
1.231	0.3265	0.123	0.0359	0.90	96.7

Table 3: Class-F optimal results

2.6 Transmission Lines

The transmission line are a fundamental component in many electrical circuits and systems, The Doherty amplifier included. In [1], the author wrote about the fundamentals of Transmission Lines with a short introduction to its frequency dependence, with most theory taken from [4]. This subsection reviews the fundamentals of the transmission line and expands on its frequency dependence. The problem of using transmission lines in MMIC is explained, and a solution by using equivalent lumped component models are given.

2.6.1 Basic Transmission Line Theory



(a) Voltage and current definitions (b) Lumped component equivalent

Figure 23: Basic transmission line definitions, taken from [4]

A basic transmission are shown in figure 23a, which consists of two conductors, through which a signal propagates. Having two or more conductors are needed for the voltage differentiation, allowing the signal to have both a current and voltage value across the line, allowing the transmission line to have an characteristic impedance. This impedance can be described by lumped components which are shown in figure 23b. In short, the resistance R, and the conductance G describes the signal *attenuation* across a Δz segment of the transmission line, while the inductance, L and the capacitance, C describes the phase change across the Δz segment. The relation of attenuation, α and phase-change, β across the transmission line are given in the complex propagation factor γ as

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.19}$$

In the frequency domain, with a sinusoidal steady-state condition, the voltage and current change per length unit Δz is found by applying Kirchoff's Voltage Law (KVL) and Kirchoffs Current Law (KCL) to the circuit in figure 23b. These equations are called the *telegrapher equations*, and are given in the frequency domain as

$$\frac{dU(z)}{dz} = -(R + j\omega L)I(z) \tag{2.20a}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)U(z) \tag{2.20b}$$

The voltage and current of figure 23a are the sum of the forward traveling and reflected wave, and are denoted as the *traveling wave solution*. These equations gives the signal as a superposition of forward traveling and reflected signal, both as a function of γ, and are given as

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.21a}$$

$$\begin{aligned} I(z) &= I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \\ &= \frac{V_0^+}{Z_0} e^{-\gamma z} - \frac{V_0^-}{Z_0} e^{\gamma z} \end{aligned} \tag{2.21b}$$

From figure 23b, it is apparent that a transmission line of a fixed length l have a characteristic impedance Z_0 (sometimes interchanged with Z_C). Z_0 are generally defined by the length and the width of a Transmission Line, as well as its material parameters such as permittivity and permeability, thus Z_0 are independent of external circuitry and therefore a fundamental parameter in Transmission Line theory. Z_0 can be found by first differentiating equation 2.21a with respect to z, and then combine it with equation 2.20a which yield

$$I(z) = \frac{\gamma}{R + j\omega L}[U_0^+ e^{-\gamma z} - U_0^- e^{\gamma z}] \tag{2.22}$$

Finally, equation 2.22 can be compared to equation 2.21b to find the characteristic, time-independent and length-independent impedance of a transmission line. With the physical understanding that a reflected current will have have a different sign

than the incident current, while the reflected voltage will have same sign as the incident voltage, the characteristic impedance can be found as

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.23}$$

Equation 2.23 reveals that Z_0 can be complex, and can be real even with $R = G = 0$.

2.6.2 S- and Z-Parameters

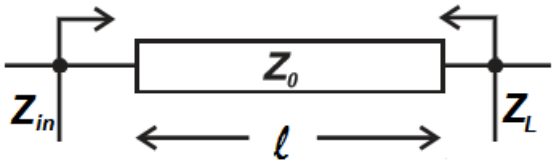


Figure 24: Generic terminated 2-port transmission line [2]

At the input terminal of a transmission line, the *Reflection coefficient*, Γ_{in}, determines the ratio of the input signal which is reflected back, while the *Transmission coefficient*, T_{in}, determines the ratio of the input signal which are transferred through the line. With reference to figure 24, the complex value of Γ_{in} and T_{in} are given by the mismatch between Z_0 and Z_L as

$$\Gamma_{in} = \frac{U_{in}^-}{U_{in}^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.24a}$$

$$T_{in} = \frac{2Z_0}{Z_L + Z_0} \tag{2.24b}$$

By adding 2.24a and 2.24b together, it is readily seen that $\Gamma_{in} + T_{in} = 1$, which is to be expected from a lossless passive component. As a transmission line is a reciprocal element, equation 2.24a and 2.24b can be mirrored to give the Γ_L and T_L seen from the load. Together these four variables give the S-parameters of a generic terminated transmission line.

$$[S_{TL}] = \begin{bmatrix} \Gamma_{in} & T_L \\ T_{in} & \Gamma_L \end{bmatrix} = \begin{bmatrix} \frac{Z_L - Z_0}{Z_L + Z_0} & \frac{2Z_0}{Z_{in} + Z_0} \\ \frac{2Z_0}{Z_L + Z_0} & \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \end{bmatrix} \tag{2.25}$$

While the reflection coefficients and transmission coefficients of 2.25 gives values at the ports of the 2-port transmission line, the travelling wave equation of 2.21a can be used to give the reflection at a variable length of the transmission line. As Γ is the ratio of reflected and transversing voltage wave, then by introducing the variable $l = -z$ (the distance backward from the load), the reflection coefficient can be adjusted to become

$$\Gamma(l) = \frac{U_0^- e^{-j\beta l}}{U_0^+ e^{j\beta l}} = \Gamma(0) e^{-2j\beta l} \tag{2.26}$$

Equation 2.26 can also be combined with equation 2.21a to give

$$U(l) = U_0^+ [e^{j\beta l} + \Gamma e^{-j\beta l}] \tag{2.27}$$

Which is an important equation when finding the Doherty Z-parameters in subsection 2.8. Next, with reference in figure 24, and using equations 2.21a, 2.21b, 2.24a and 2.26 together with eulers identity ($e^{jx} = \cos(x) + j\sin(x)$), the relation of Z_{in}, Z_0 and Z_L can be found as

$$\begin{aligned} Z_{in} = \frac{U(-l)}{I(-l)} &= Z_0 \frac{1 + \Gamma e^{-2j\beta l}}{1 - \Gamma e^{-2j\beta l}} \\ &= Z_0 \frac{(Z_L + Z_0) e^{j\beta l} + (Z_L - Z_0) e^{-j\beta l}}{(Z_L + Z_0) e^{j\beta l} - (Z_L - Z_0) e^{-j\beta l}} \end{aligned} \tag{2.28a}$$

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \ \tan(\beta l)}{Z_0 + jZ_L \ \tan(\beta l)} \tag{2.28b}$$

Having derived the above formulas, it is possible to give the Z-parameters for the transmission line, which is fundamental in understanding the Z-parameters for the Doherty equivalent circuit. Transmission lines are both reciprocal and bilateral, which yields $Z_{11} = Z_{22}$ and $Z_{21} = Z_{12}$. Using the definition of Z-parameters from equation 2.2, Z_{11} can be found from equation 2.28b with $I_L = 0 \longrightarrow Z_L \to \infty$,

using the trigonometric identities $\cot(x) = 1/\tan(x)$, $\csc(x) = 1/\sin(x)$ which gives

$$Z_{11} = Z_{22} = -jZ_0 cot(\beta l) \tag{2.29}$$

Further, Z_{21} gives by definition $Z_L \to \infty$, which then yields $\Gamma_{in} = 1$. Z_{21} can then be found from equations 2.21a and 2.21b as

$$\begin{aligned} Z_{21} &= \frac{U_L}{I_{in}} = \frac{U(0)}{I(-l)} \\ &= Z_0 \frac{U_0^+ + U_0^-}{U_0^+ e^{j\beta l} - U_0^- e^{-j\beta l}} = Z_0 \frac{1 + \Gamma_{in}}{e^{j\beta l} - \Gamma_{in} e^{-j\beta l}} \\ &= Z_0 \frac{2}{e^{j\beta l} - e^{-j\beta l}} = -jZ_0 \frac{1}{\sin(\beta l)} \end{aligned} \tag{2.30}$$

Finally, the complete Z-parameter matrix of the transmission line is given as

$$[Z_{TL}] = \begin{bmatrix} -jZ_0 \cot(\beta l) & -jZ_0 \csc(\beta l) \\ -jZ_0 \csc(\beta l) & -jZ_0 \cot(\beta l) \end{bmatrix} \tag{2.31}$$

2.6.3 Frequency dependence of the quarter-wave transmission line

A commonly used and important feature of transmission lines is to adjust the length to fractions of the wavelength to achieve the wanted impedance effect. From the definition of wavelength comes the important formula $\beta = 2\pi/\lambda$, which inserted into 2.28b with $l = \lambda/4$ yields $Z_{in} = Z_0^2/Z_L$, which inverts the impedance compared to Z_L. The $\lambda/4$ impedance inverting effect is an important transmission line effect and fundamental in the Doherty architecture. Using $\beta = 2\pi/\lambda$ with $l = \lambda/2$ yields $Z_{in} = Z_L$, showing that transmission line length can be adjusted to acheive impedance effects. Obviously, for a $\lambda/4$ impedance inverter, changing the length away from $\lambda/4$ so that $l \neq \lambda/4$ would diminish the impedance inverting effect. But the same would also be true if the frequency and the resulting wavelength deviates from the design value. Therefore, transmission lines are said to have bandwidth restrictions.

By further examining equation 2.28b for a $l = \lambda/4$ TL, the frequency-length relation βl yield

$f_k\ [GHz]$	ΔZ_{in}	$\Delta\theta(Z_{in})$	ΔZ_{11}	ΔZ_{12}
4.4	-1.84%	$8.5°$	$-j5.0\Omega$	$-j0.3\Omega$
4.5	-0.83%	$5.7°$	$-j3.4\Omega$	$-j0.1\Omega$
4.6	-0.21%	$2.9°$	$-j1.7\Omega$	$-j0.03\Omega$
4.7	0%	$0°$	0	0
4.8	-0.21%	$-2.9°$	$j1.7\Omega$	$-j0.03\Omega$
4.9	-0.83%	$-5.7°$	$j3.4\Omega$	$-j0.1\Omega$
5.0	-1.84%	$-8.5°$	$j5.0\Omega$	$-j0.3\Omega$

Table 4: Impedance deviation in the f_0-band

$$\beta_0 l = \frac{2\pi}{\lambda_0} \cdot \frac{\lambda_0}{4} = \frac{(v_p/f_0)}{(v_p/f_0)} \cdot \frac{\pi}{2} = \frac{\pi}{2} \tag{2.32}$$

Where v_{TL} is the phase velocity through a lossless TL, which is given by the equation [4]

$$v_p = \frac{c}{\sqrt{\epsilon_r \mu_r}} \tag{2.33}$$

Here, c, ϵ_r and μ_r are the speed of light, relative material permittivity and relative material permeability respectively. If the frequency deviates from f_0, that is $f_k \neq f_0$, then equation 2.32 changes to

$$\beta_k\, l = \frac{f_k}{f_0}\frac{\pi}{2} \tag{2.34}$$

The factor f_k/f_0 is denoted as the normalized frequency with a corresponding normalized bandwidth. For this project, a center frequency of $f_0 = 4.7GHz$ is used, with bandwidth $4.4GHz$ to $5.0GHz$. To give an indication of the the frequency dependence of a $\lambda/4$ transmission line, numerical values for the deviation could be developed, which is shown in table 4 and 5 for the f_0-band and $2f_0$ band respectively. The values of Z_{in} are given with a load impedance $Z_L = 25\Omega$ and characteristic impedance $Z_0 = 50\Omega$, with the percentage and angle deviation relative to f_0 and $2f_0$. The values of ΔZ_{11} and ΔZ_{12} are also given relative to f_0 in the fundamental band, while given as actual numerical value in the $2f_0$ band due to the asymptotic nature of Z_{11} and Z_{12} in this band.

Any percentage deviation from the center frequency value, is given by

$f_k\ [GHz]$	ΔZ_{in}	$\Delta\theta(Z_{in})$	Z_{11}	Z_{12}
8.8	7.4%	$-16.3°$	$j246\Omega$	$-j251\Omega$
9.0	3.3%	$-11.2°$	$j372\Omega$	$-j371\Omega$
9.2	0.8%	$-5.7°$	$j747\Omega$	$-j749\Omega$
9.4	0%	$0°$	∞	∞
9.6	0.8%	$5.7°$	$-j747\Omega$	$j749\Omega$
9.8	3.3%	$11.2\circ$	$-j372\Omega$	$j371\Omega$
10.0	7.4%	$16.3°$	$-j246\Omega$	$j251\Omega$

Table 5: Impedance deviation in the $2f_0$-band

$$\Delta F = \frac{F(f_0) - F(f_k)}{F(f_0)} * 100\% \tag{2.35}$$

It's worth noting that while the absolute numbers given in table 4 and 5 may not seems like much, the super-position of all harmonics adds to the overall effect. As an example, Z_{11} and Z_{12} are assumed open-circuited for the 2nd harmonic in the ideal TL, thus all input voltages waves should have full reflection. When the signal frequency reaches the band edges of $f_k = 8.8GHz, 10GHz$, the relative rounded impedance $Z_{11} \approx Z_{12} \approx 250\Omega$ presumably is comparable to other impedances in the design, and thus a portion of the 2nd harmonic voltage wave would be transmitted through the TL. The same would be true for higher harmonics, and these become more dominating as the signal frequency deviates from the center frequency. Finding exact values of over harmonic transmission and reflection could be done by expanding the S-parameters of equation 2.25 to include frequency dependence, but this is a cumbersome task and omitted here.

2.6.4 Using transmission lines in GaN MMIC

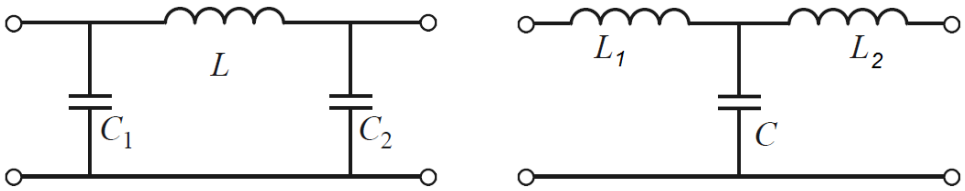
The above subsection gives the frequency response and bandwidth limitations of an ideal transmission line, and this is indeed an important limitation in using TL in any practical system, including the Doherty design. Another limitation of TLs, as apparent when used in MMICs, is their physical length in relation to the wavelength. Table 1 gives $\epsilon_r \approx 9.5$ at high frequencies, and with $\mu_r = 1$ inserted into equation 2.33 gives phase velocity of $v_p \approx 97.3 * 10^6 m/s$. At a center frequency $f_0 = 4.7GHz$ this equals $\lambda_0 = 20.7mm$. A $\lambda/4$-TL would thus have length $l = 5.18mm$, which is large compared to the typical MMIC chip area of $1mm^2$ to $10mm^2$, as described in subsection 2.3. Both lumped components and

transistors in MMIC are much smaller, and using TL in MMIC, even with bends to maximize area, would dominate the area usage. Transmission lines as impedance inverters are therefore impractical to use in MMIC.

2.6.5 Lumped component equivalent model

The above subsections presented two main challenges in using transmission lines in a broadband microwave MMIC circuit, namely bandwidth limitations and size limitations. With much of modern RF electronics development, the requirement to make hardware smaller and with better bandwidth properties becomes more stringent as an increasing amount of devices have some sort of wireless communication system, thus the impracticality of transmission lines are important to address.

A way to overcome these challenges is to use equivalent models for the TL, consisting of passive lumped reactive components such as capacitors and inductors. As shown in figure 23b, any lossless TL ($R = G = 0$) can be modeled with a serie inductor and a shunt capacitor for a line of any length. To satisfy the reciprocal nature of the TL, that is to make $Z_{11} = Z_{22}$, an extra component need to be inserted into the LC-circuit to make the Z-parameters symmetric. This can be done either by adding an extra shunt capacitor or an extra series inductor, and the resulting circuit is called a Π-equivalent or a T-equivalent circuit respectively, as shown in figure 25.



(a) Π-equivalent (b) T-equivalent

Figure 25: Lumped component equivalent circuit

2.6.5.1 Π-equivalent model The Z-parameters of circuit 25a can be found by using the Z-parameter definitions of equation 2.2. Denoting $Z_{C1} = -j/(\omega C_1)$, $Z_{C2} = -j/(\omega C_2)$, $Z_L = j\omega L$ and $Z_{\Pi,sum} = Z_{C1} + Z_{C2} + Z_L$, the Z-parameters are found by standard circuit analysis, using KVL and KCL, as

$$[Z_\Pi] = \begin{bmatrix} \frac{Z_{C1}(Z_L+Z_{C2})}{Z_{\Pi,sum}} & \frac{Z_{C1}Z_{C2}}{Z_{\Pi,sum}} \\ \frac{Z_{C2}Z_{C1}}{Z_{\Pi,sum}} & \frac{Z_{C2}(Z_L+Z_{C1})}{Z_{\Pi,sum}} \end{bmatrix} \tag{2.36}$$

The parameter value of L, C_1 and C_2 should be adjusted such that the Z-parameter values of equation 2.36 is as identical to the ideal $\lambda/4$ transmission line Z-parameters of equation 2.31 as possible in the f_0 frequency band. As mentioned above, this is acheived by setting $C_1 = C_2 = C_\Pi$. Further, it is fundamental that that Z_{11} and Z_{22} achieves resonans at f_0, thus making $Z_L + Z_{C\Pi} = 0$. Deducing the above formulas lead to the well known LC-circuit formula, which can be used to relate the practical values of L and C_Π.

$$\omega_0 = 2\Pi f_0 = \frac{1}{\sqrt{LC_\Pi}} \tag{2.37}$$

2.6.5.2 T-equivalent model Using the same method as above, the Z-parameters for the T-equivalent model in figure 25b can be derived as

$$[Z_T] = \begin{bmatrix} Z_{L1} + Z_C & Z_C \\ Z_C & Z_{L2} + Z_C \end{bmatrix} \tag{2.38}$$

As a side note, the Z-parameters of a T-equivalent is readily simpler than the Π-equivalent, and it is common to use Y-parameters rather than Z-parameters to express the response of the Π-equivalent model. The Y-parameters are the inverse of the Z-parameters, defined as $[Y] = [Z]^{-1}$. Further, equation 2.37 can be used to find the relation between inductors and capacitor, interchanging $L_T = L_1 = L_2 \leftrightarrow L$ and $C \leftrightarrow C_\Pi$.

2.7 Active Loadpull

The Doherty is one of many Loadpull configurations of amplifiers used to control currents, impedances and inherently also the power on the output of a given system. To better understand the principle of the Doherty Loadpull configuration, it is important to first understand the basic *active* Loadpull configuration.

Figure 26 shows a basic circuit with two generators. Simple circuit theory gives

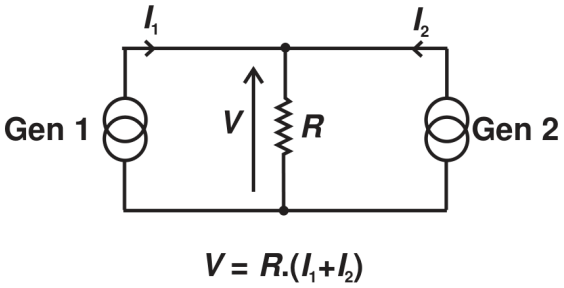


Figure 26: Active Loadpull with two generators, taken from [2]

the output voltage $V = R_L(I_1 + I_2)$. If generator 2 is shut-off, then generator 1 would see a resistance $R_1 = R_L$ over its terminals. As generator 2 starts to conduct the current I_2, the voltage over the resistor increases, but generator 1 still only sees its current I_1, thus the resistance seen by generator 1 needs to increase proportionally. In this way, the load resistance seen by generator 1 is "pulled" up by generator 2. The voltage over the terminals of generator 1 can be represented as $V_L = R_1 I_1$. The above equations can then be combined to give the resistance over the terminals of generator 1, dependant of both currents.

$$R_1 = R_L(\frac{I_1 + I_2}{I_1}) \tag{2.39}$$

A similar equation can be made for generator 2 by interchanging R_1 and R_2 as well as I_1 and I_2. Equation 2.39 can be expanded to account for phase and magnitude in AC circuits, where a complex impedance notation can be used for the resistors.

$$Z_1 = Z_L(1 + \frac{I_2}{I_1}) \tag{2.40}$$

As seen from equation 2.40, the impedance seen from generator 1 is increasing with I_2. To best understand the concept, the extreme points of equation 2.40 can be explored. If $I_2 = 0$ then I_1 contributes all the current through Z_1 and the voltage drop is only created by generator 1. If $I_2 \gg I_1$ then I_1 contributes very little to the voltage drop over Z_L, and the equivalent impedance seen by generator 1 would approach infinity.

Thus by introducing a second current, the load seen by a device can be "pulled" up to any wanted impedance. The Doherty design expands on this concept, introducing $\lambda/4$ transmission lines which can transform an impedance symmetrically the

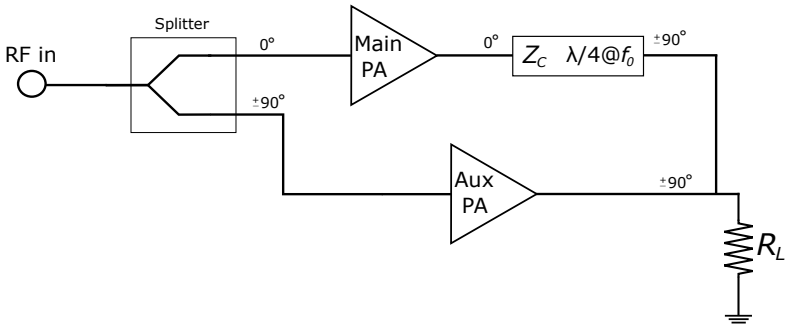


Figure 27: Basic Doherty architecture

characteristic impedance Z_C, thus allowing increasing currents to create decreasing equivalent impedances. This will be expanded on in subsection 2.8

2.8 Doherty

The Doherty amplifier technique is a load modulation method where the load resistance seen on the transistor output is modulated from active loadpull to achieve greater efficiency over a larger range of backed-off input power levels. While traditional transistor classes will have linear increase in efficiency with increasing input power levels, the Doherty technique theoretically allows maximum efficiency at backed-off power levels.

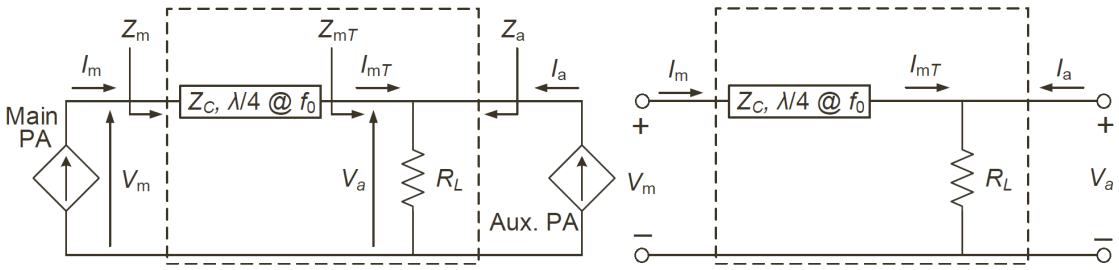
The Doherty architecture was developed by the American William Humphrey Doherty in 1936 [8] while working at Bell Laboratories. This was in the early days of radio communication, and vacuum tubes were used to amplify the RF signals. Vacuum tubes generally need high supply voltages to operate, and also have low efficiency, creating lots of excessive heat loss over the device. As the 1930s also was the time of the great depression, the need to conserve resources and energy was not just a motivation for radio engineers, but indeed the driving force in its contemporary time. Doherty's basic motivation was to create an amplifier that allowed for high efficiency while maintaining signal fidelity, that is to not lose signal quality. Doherty achieved this by putting an auxiliary amplifier in parallel with the main amplifier, and using $\lambda/4$-lines to separate the signals through each amplifier from each other as well as to transform impedance.

The basic principle of Doherty architecture is given in Figure 27. The architecture can be used for any amplifying device, as explained with vacuum tubes in the above section, but this subsection will assume FET transistors for the power amplifiers,

with the defined FET characteristics described in subsection 2.4. The input signal is divided equally at the input between the two PAs using a splitter, which creates a 90° phase shift between the PAs. The main PA is biased for class-B operations, and will be conducting signal for any input drive level. The aux PA is turned off until some power level is reached, from which it will start to conduct current. The $\lambda/4$-line also inverts the impedance seen from the main PA due to the active loadpull from the aux PA, pulling its output voltage as explained in subsection 2.7.

2.8.1 Equivalent circuit

In the semester project [1], the theory was explained based mostly on [2], which assumes two identical class-B amplifiers with "onset" level at 6db backoff, that is the input power level at which the aux amplifier starts to conduct current. In [2], the frequency response of the Doherty system is also disregarded. This subsection takes most theoretical foundation from [9], which is a PHD-thesis exploring different methods of extending the Doherty PA Bandwidth, with practical implementations mostly done in GaN MMIC, thus highly relevant for this master thesis. [9] explores variable onset levels and the systems frequency response, which are fundamental knowledge when aiming to expand the bandwidth of the Doherty design in MMIC. It is assumed that all over-harmonic are short circuited and that both PAs have drain bias voltage of U_{DS}. Variables Z_0 and Z_C are used interchangeably, both denoting the characteristic impedance of the $\lambda/4$-line.



(a) Equivalent circuit, taken from [9] (b) 2-port representation

Figure 28: Doherty equivalent circuit, taken from [9]

2.8.2 Doherty Z-parameters

As discussed in subsection 2.1, any N-port network can be described by the Z-parameter matrix. For the 2-port representation of the Doherty equivalent circuit

in figure 28b, a fundamental property is that

$$U_m = Z_{11}I_m + Z_{12}I_a \tag{2.41a}$$

$$U_a = Z_{21}I_m + Z_{22}I_a \tag{2.41b}$$

One important assumption here is that both current sources of figure 28a can be represented as ideal with zero output capacitance. Finding the Doherty Z-parameter matrix requires a look back at the formulas given in subsection 2.6. First, Z_{11} is found by using equation 2.2, and using equation 2.28b directly with $Z_L = R_L$, which yield

$$Z_{11} = Z_{in}(Z_L = R_L) = Z_0 \frac{R_L \cos(\frac{f_k\pi}{f_02}) + jZ_0 \sin(\frac{f_k\pi}{f_02})}{Z_0 \cos(\frac{f_k\pi}{f_02}) + jR_L \sin(\frac{f_k\pi}{f_02})} \tag{2.42}$$

Further, Z_{22} is found by using equation 2.28b with $Z_L = \infty$, and noting that R_L and Z_{in} is parallel in the resulting circuit. The value of $Z_{in}(Z_L \to \infty)$ is incidentally the same as Z_{11} and Z_{22} for the transmission line Z-parameters in equation 2.31, that is $Z_{in}(Z_L \to \infty) = -jZ_0 cot(\frac{f_k\pi}{f_02})$. Combining the above yields

$$Z_{22} = R_L//(-jZ_0 \cot(\frac{f_k\pi}{f_02})) = \frac{Z_0 R_L \cos(\frac{f_k\pi}{f_02})}{Z_0 \cos(\frac{f_k\pi}{f_02}) + jR_L \sin(\frac{f_k\pi}{f_02})} \tag{2.43}$$

Next, as with transmission line, the Doherty equivalent circuit are reciprocal giving $Z_{21} = Z_{12}$. To find Z_{12}, a natural starting point is to use the Z-parameter definition in equation 2.2. With $I_1 = I_m = 0$, equation 2.41b reduces to $U_a = U_2 = Z_{22}I_a$. Further, $I_1 = 0$ implies that all voltage wave on the input a transmission line with $Z_L = \infty$ are reflected, giving $\Gamma = 1$. Also, the total reflection indicates $U_1^+ = U_1^-$, which reduces equation 2.21a to $U(0) = U_1 = 2U_1^+$. Using this with equation 2.27 gives $U(l) = U_2 = U_1[e^{j\beta l} + e^{-j\beta l}] = U_1 \cos(\beta l)$. Combining the above then yields

$$U_1 = \frac{U_2}{\cos(\beta l)} = \frac{Z_{22}I_2}{\cos(\beta l)} \to \frac{U_1}{I_2} = Z_{12} = \frac{Z_{22}}{\cos(\frac{f_k\pi}{f_02})} \tag{2.44}$$

Finally, equation 2.44 can be combined with equation 2.43 to give

$$Z_{12} = \frac{R_L Z_0}{Z_0 \cos(\frac{f_k \pi}{f_0 2}) + jR_L \sin(\frac{f_k \pi}{f_0 2})} \tag{2.45}$$

Combining equations 2.42, 2.45 and 2.43 gives the complete Doherty Z-parameter matrix

$$[Z_{Doherty}] = \begin{bmatrix} Z_0 \frac{R_L \cos(\frac{f_k \pi}{f_0 2}) + jZ_0 \sin(\frac{f_k \pi}{f_0 2})}{Z_0 \cos(\frac{f_k \pi}{f_0 2}) + jR_L \sin(\frac{f_k \pi}{f_0 2})} & \frac{R_L Z_0}{Z_0 \cos(\frac{f_k \pi}{f_0 2}) + jR_L \sin(\frac{f_k \pi}{f_0 2})} \\ \frac{R_L Z_0}{Z_0 \cos(\frac{f_k \pi}{f_0 2}) + jR_L \sin(\frac{f_k \pi}{f_0 2})} & \frac{Z_0 R_L \cos(\frac{f_k \pi}{f_0 2})}{Z_0 \cos(\frac{f_k \pi}{f_0 2}) + jR_L \sin(\frac{f_k \pi}{f_0 2})} \end{bmatrix} \tag{2.46}$$

The matrix of equation 2.46 can be expanded to yield results for the over-harmonics of the system, that is for $f_k = nf_0, (n = 2, 3, 4 \dots)$. Given the odd and even characteristics of $\cos(x)$ and $\sin(x)$

$$\cos(n\frac{\pi}{2}) = \begin{cases} 0 & \text{if } n \text{ is odd} \\ (-1)^{\frac{n}{2}} & \text{if } n \text{ is even} \end{cases} \tag{2.47a}$$

$$\sin(n\frac{\pi}{2}) = \begin{cases} (-1)^{\frac{n-1}{2}} & \text{if } n \text{ is odd} \\ 0 & \text{if } n \text{ is even} \end{cases} \tag{2.47b}$$

Inserting equations 2.47a and 2.47a into 2.46 yields two different Z-parameters matrices for odd and even harmonics respectively

$$[Z_{odd}] = \begin{bmatrix} Z_0^2/R_L & jZ_0(-1)^{\frac{n+1}{2}} \\ jZ_0(-1)^{\frac{n+1}{2}} & 0 \end{bmatrix} \tag{2.48a}$$

$$[Z_{even}] = \begin{bmatrix} R_L & R_L(-1)^{\frac{n}{2}} \\ R_L(-1)^{\frac{n}{2}} & R_L \end{bmatrix} \tag{2.48b}$$

2.8.3 Currents, Voltages and Impedances

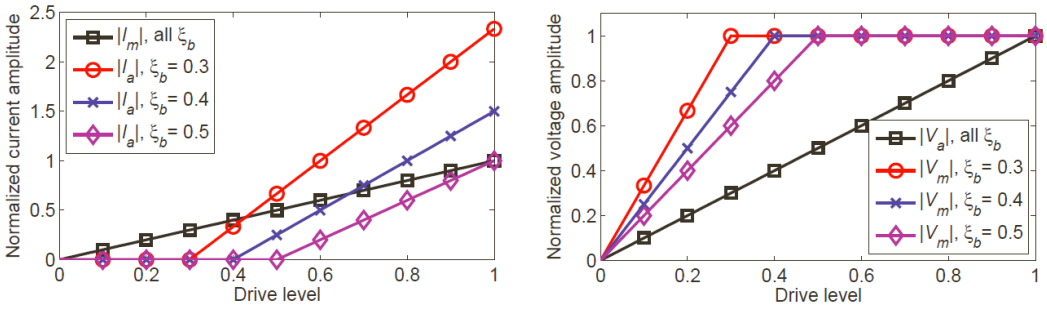
The general equivalent circuit of a Doherty amplifier circuit is shown in figure 28a, where the main and the auxiliary PA are separated by a transmission line with

electrical length $l = \lambda/4$ at center frequency f_0 and characteristic impedance Z_C. The onset level, ξ_b depends on the amplifier voltage drive level $0 \leq \xi \leq 1$, which corresponds to $0 \leq P_{in} \leq P_{in,max}$, with $P_{out,max} = P_{out}(P_{in,max})$. The drive level ξ are also related to the power backoff level by $P_{BO} = -20log(\xi)$. From this, the currents across the 2-port given in subfigure 28b can be expressed as

$$I_m = \xi \frac{I_{max,m}}{2} \tag{2.49}$$

$$I_a = \begin{cases} 0 & 0 \leq \xi \leq \xi_b \\ \frac{I_{max,m}}{2} \frac{\xi - \xi_b}{\xi_b} e^{-j\frac{f_k \pi}{f_0 2}} & \xi_b \leq \xi \leq 1 \end{cases} \tag{2.50}$$

Here, $I_{max,m}$ is the maximum possible current on the main PA output. The phase shift on I_a comes from the splitter input, given in figure 27.



(a) Doherty Currents, [9], p.11 (b) Doherty Voltages, [9], p.12

Figure 29: Currents and Voltages normalized to $I_{max,m}/2$ and U_{DS}

Now, the optimal values of Z_0 and R_L can be found. At center frequency, $f_k = f_0$, equation 2.41b evaluates to $U_a = -jZ_0 I_m$. When the aux PA reach compression, the output voltage should equal $U_a = U_{DS}$. Using equation 2.49 with $\xi = 1$, and using absolute values, the resulting aux voltage is given as $U_a = U_{DS} = Z_0 I_{max,m}/2$. Comparing this to the optimal loadline resistance for a class-B amplifier, given in equation 2.6 reveals an important feature of the Doherty amplifier

$$Z_0 = \frac{2U_{DS}}{I_{max,m}} = R_{OPT} \tag{2.51}$$

Continuing the analysis for $f_k = f_0$, the main PA output voltage is found from

equation 2.41a and 2.46 as $U_m = (Z_0^2/R_L)I_m - jZ_0I_a$. For drive levels where $I_a \neq 0$, combining equations 2.49, 2.50 with 2.41a yields

$$U_m = \frac{I_{max,m}}{2} Z_0 \xi (\frac{Z_0}{R_L} - \frac{1}{\xi_b}) + \frac{I_{max,m}}{2} Z_0 \tag{2.52}$$

By choosing

$$R_L = \xi_b Z_0 \tag{2.53}$$

equation 2.52 is reduced to $U_m = Z_0 I_{max,m}/2$ for $\xi > \xi_b$, and is constant and independent of drive level. For values of $\xi < \xi_b \rightarrow U_m = (U_{DS}\xi)/\xi_b$. Equation 2.53 differs the basic Doherty theory given in [1] and [2] in one important aspect. In the basic Doherty, the onset level is fixed to $\xi_b = 0.5$ corresponding to $6dB$ backoff. Having this value fixed, as well as having a fixed R_{OPT} for a given transistor size implies fixed values for Z_0 and R_L, and a designer must therefore add extra output matching on transistor output and on Doherty output to satisfy these constraints. In contrast, allowing ξ_b to be variable withing reasonable limits allows a designer to optimize Z_0 and R_L directly without extra matching circuitry. Though the constraint given in equation 2.51 still holds true, so matching for a low R_{OPT} may still require extra matching circuitry.

2.8.4 Power and Efficiency

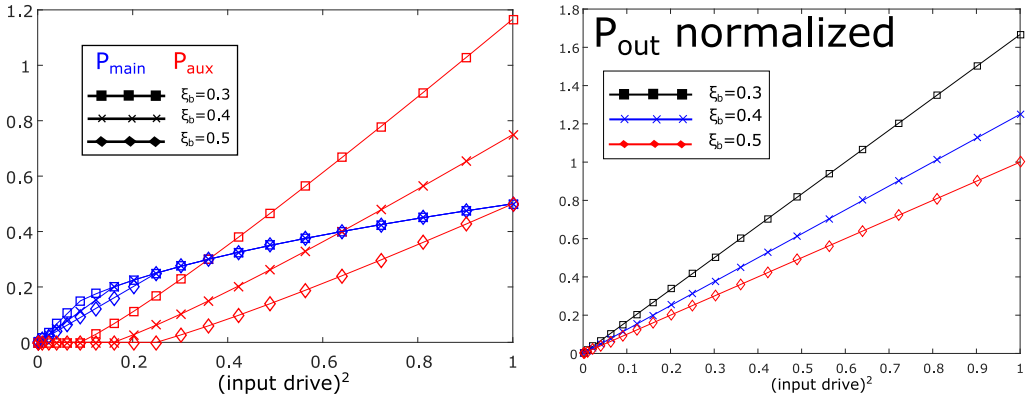
The powers of the Doherty design can be found from the currents and voltages, using the RMS power equation $P_{RMS} = 0.5 * |U_{RMS}| * |I_{RMS}|$, thus P_{main} and P_{aux} are generally found as

$$P_{main} = 0.5 * |U_m| * |I_m| \tag{2.54a}$$

$$P_{aux} = 0.5 * |U_a| * |I_m| \tag{2.54b}$$

By inserting equation 2.49 and 2.41a into 2.54a, and inserting 2.50 and 2.41b into 2.54b, the powers could be found graphically as given in figure 30a, with the current ant voltage normalized for $I_{max,m}/2$ and U_{DS} respectively. Recalling that U_a is the voltage over R_L, the composite output power at f_0 is given as

$$P_{out} = P_{main} + P_{aux} = \frac{|U_a|^2}{2R_L} = \frac{Z_0|I_m|^2}{2\xi_b} = \frac{Z_0}{2\xi_b}(\xi\frac{I_{max,m}}{2})^2 \tag{2.55}$$



(a) Normalized PA powers (b) Normalized output powers

Figure 30: Doherty power characteristics

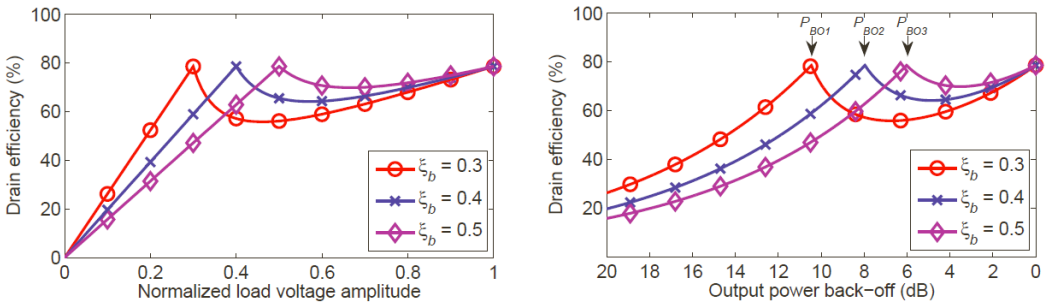
Equation 2.55 is plotted for various drive levels in figure 30b, with currents and voltages normalized. One important property to note from figure 30a and 30b is that in designing a Doherty system to deliver a total RMS power of P_{Design}, the different PAs need to be designed to deliver $P_{main,max} = P_{Design}/(1-\xi_b)$ and $P_{aux,max} = P_{Design}/\xi_b$ respectively, with respect to equation 2.7. In the literature source [2], the basic case of $\xi_b = 0.5$ is given, which gives $P_{main,max} = P_{aux,max}$. Next, from [2] p.298, the equation for the total DC power consumption for both PAs are given as

$$P_{DC} = \frac{2U_{DS}(|I_m| + |I_a|)}{\pi} \tag{2.56}$$

Combining equation 2.55 and 2.56 gives the drain efficiency as

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\pi Z_0|I_m|^2}{2U_{DS}\xi_b(|I_m| + |I_a|)} \tag{2.57}$$

The dependency of drive level for equation 2.57 lies within the formulas for I_m and I_a. The drain efficiency for various onset levels can be plotted vs normalized U_L and P_{BO}, shown in figure



(a) η vs normalized U_L, [9], p.13 (b) η vs P_{BO}, [9], p.13

Figure 31: Drain efficiency for various onset drive level ξ_b

2.8.5 Frequency response analysis

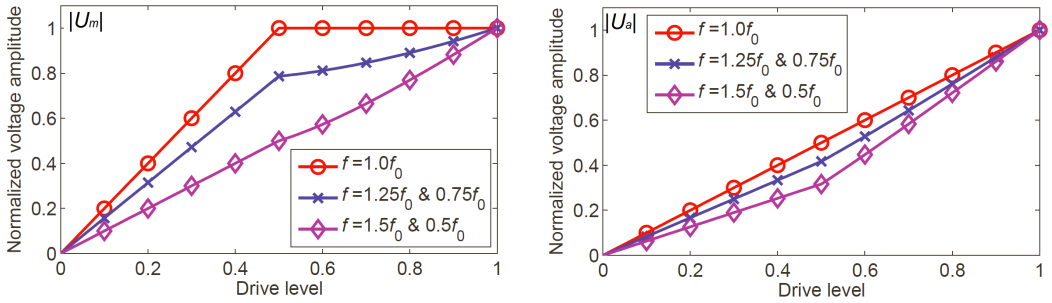
The equations for U_m and U_a derived above uses the Doherty Z-parameters with $f_k = f_0$, omitting all trigonometric of the Z-parameters of equation 2.46. For $f_k \neq f_0$, or any over-harmonic, the trigonometric dependencies cannot be omitted, and by combining equation 2.46 with equations, 2.49, 2.50, 2.41a and 2.41a, the resulting expressions of U_m and U_a becomes "ugly", and are given as

$$U_m = \begin{cases} U_{DS}\left(\frac{\xi\xi_b \cos(\frac{f_k\pi}{f_0 2})+j\xi \sin(\frac{f_k\pi}{f_0 2})}{\cos(\frac{f_k\pi}{f_0 2})+j\xi_b \sin(\frac{f_k\pi}{f_0 2})}\right) & 0 \leq \xi \leq \xi_b \\ U_{DS}\left(\frac{(\xi\xi_b+\xi-\xi_b) \cos(\frac{f_k\pi}{f_0 2})+j\xi_b \sin(\frac{f_k\pi}{f_0 2})}{\cos(\frac{f_k\pi}{f_0 2})+j\xi_b \sin(\frac{f_k\pi}{f_0 2})}\right) & \xi_b \leq \xi \leq 1 \end{cases} \tag{2.58a}$$

$$U_a = \begin{cases} U_{DS}\left(\frac{\xi\xi_b}{\cos(\frac{f_k\pi}{f_0 2})+j \sin(\frac{f_k\pi}{f_0 2})}\right) & 0 \leq \xi \leq \xi_b \\ U_{DS}\left(\frac{\xi\xi_b+(\xi-\xi_b) \cos(\frac{f_k\pi}{f_0 2})(\cos(\frac{f_k\pi}{f_0 2})-j \sin(\frac{f_k\pi}{f_0 2}))}{\cos(\frac{f_k\pi}{f_0 2})+j\xi_b \sin(\frac{f_k\pi}{f_0 2})}\right) & \xi_b \leq \xi \leq 1 \end{cases} \tag{2.58b}$$

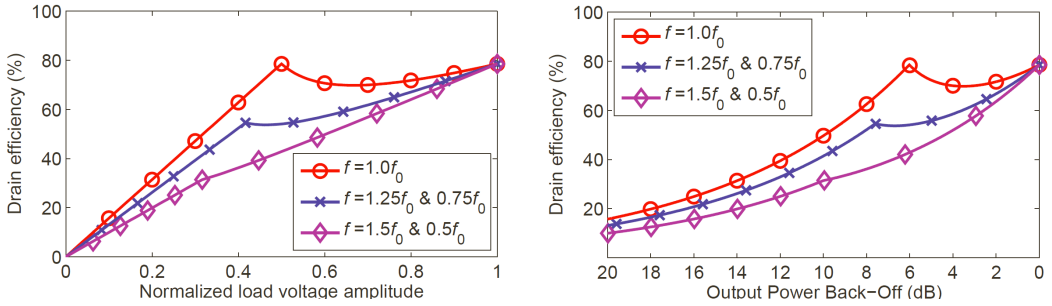
The response of U_m and U_a for various f_k-levels are shown in figure 32. The corresponding frequency response of η_{drain} is shown in figure 33. All values are given with $\xi_b = 0.5$.

The important result of figures 32 and 33 is that the loadpull effect deviates as the frequency moves away from f_0. This is due to the $\lambda/4$ frequency response described in subsection 2.6, as readily seen from the figures, at $f_k = 1.5f_0$ and



(a) U_m frequency response (b) U_a frequency response

Figure 32: Doherty voltage frequency response, [9][p.14]



(a) η_{drain} frequency response (b) η_{drain} vs OPBO frequency response

Figure 33: Doherty efficiency frequency response, [9][p.14]

$0.5f_0$, η_{drain} shows very little Doherty effect at the onset-level, and shows almost the same efficiency curve as a single class-B PA. It's worth noting that at the point the PA reaches saturation, the theoretical efficiency is 78.4% independently of frequency response.

2.8.6 Realization with class-C Power Amplifier

The theory above assumes two equally sized class-B amplifiers, with their onset level varying. In practical applications, using the auxiliary amplifier in class-B operations is difficult, as external circuitry is needed to keep the amplifier in cut-off before the onset level. Also, as shown in figure 30a and 30b, using two identical amplifiers leads to different output powers between the two, which is generally unwanted. One way to overcome this problem, and perhaps the most common approach of realizing a Doherty design is to realize the aux PA as a class-C PA. This is also the method chosen for this project. The concept is to bias the aux PA a voltage value $V_{q,classC} = \Delta V_q$ lower than the main class-B PA, so that the

aux PA starts conducting current for input voltage values V_q higher than that for the main PA. By designing $V_q = V_{max}/2$, the class-C aux PA will ideally start conducting current when $v_{in} = V_{q,classC} = V_{max}/2$, and the aux PA will conduct linearly increasing current until the threshold value $v_{in} = V_{max}$, at which point the class-C should reach its own saturation point to optimize the DC power usage and efficiency. For the class-C PA deliver the same max output current of $I_{aux} = I_{max}/2$, the periphery of the transistor has be increased, depending on which conduction angle is chosen for the PA. Increasing the periphery of a transistor is the same as making it physically bigger, which will be explained further i subsection 2.3. According to [2], a typical transistor scaling factor for making a class-C amplifier that delivers the same current as a class-B is 2.5.

3 Practical Design

3.1 Design Choices and Design Flow

3.1.1 Design Choices

The main motivation behind this project was to make an practical realizable Doherty Power Amplifier using CAD (Computer Aided Design). In making a finished design to specifications, those who gave the project description would be able to either realize the design directly, or use it further in their own design. A summary of the design choices is given here:

- Design with real MMIC components using CREE GaN MMIC foundry.
- Main PA implemented as deep class-AB PA.
- Auxiliary PA implemented as class-C PA.
- Capable of delivering 20W RMS output power .
- Center frequency $f_0 = 4.7GHz$
- Optimize performance in frequency band $4.4GHz$ to $5.0GHz$.
- Load R_L variable within reasonable limits
- ADS Keysight used as CAD for implementation and simulation.

3.1.2 Design Flow

There is not one correct approach when designing large complex system such as the Doherty PA. Different designers have different methods, depending on various factors such as theory knowledge, CAD knowledge and more. Still, some practical rules do apply for all amplifier designers. As an example, choice of transistor type and size always comes first since the whole design depends on this. The design flow used in this project is shown in figure 34.

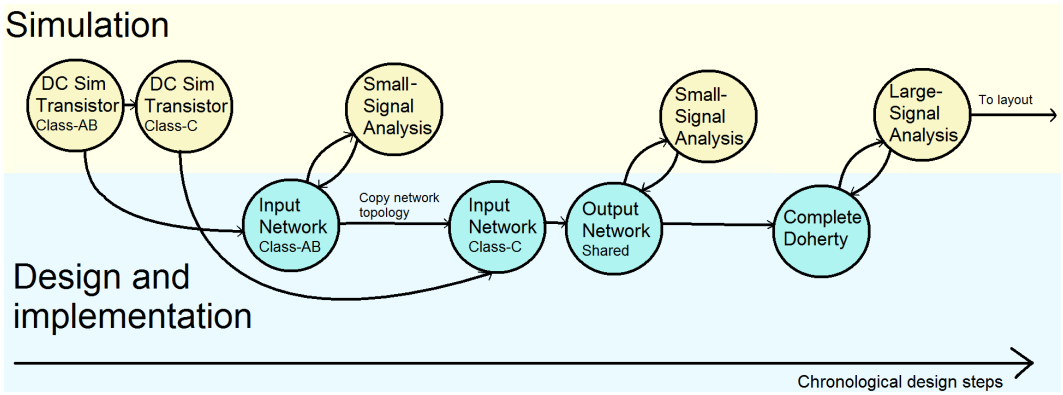


Figure 34: Design flow illustration

3.2 Using Computer Aided Design

3.2.1 Choosing Keyisght ADS

For this project, it was chosen to implement and simulate the Doherty design in Keysight ADS (Advanced Design System). The main reasons for this was the authors familiarity with the program, as well as its availability through the university. Other CADs (Computer Aided Design) that gives the same range of possibilities exist, such as AWR (Applied Wave Research) by National Instruments and Ansoft Designer by ANSYS. Still, for many reasons, ADS was chosen as CAD to realize the Doherty design. The software allows for simulation and implementation of most aspects of analog circuit design, as well as digital signal processing. Detailed layout of circuits can also be produced, which is an important feature for an MMIC designer working with size restrictions. ADS also uses an *Application Extension Language (AEL)* for simulation results. This is a C#-alike language, and allows a designer to use algebraic manipulation of simulation results, and even write simple scripts. Simulation in ADS usually sweeps over discreet values, which creates vectors and matrices of output values, making it possible for a designer create and plot functions dependant of input and output values.

3.2.2 Small-Signal analysis

In small-signal analysis, the input drive response of the system is omitted, and only the frequency response of the system are evaluated. In the analysis, a low energy signal oscillates around the systems DC Bias point, and from this the Z-

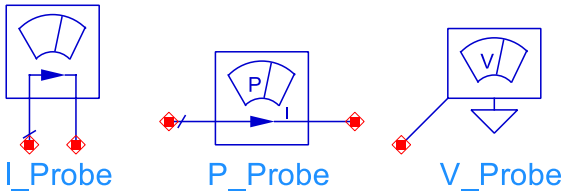


Figure 35: Basic ADS probe components

parameters, S-parameters, delay, noise and more can be calculated. In ADS, a small-signal analysis is done by using a *Terminal*, which are able to calculate the different parameters by changing its behaviour. For Z-parameters, the Terminal changes between operating as an ideal open circuit and an ideal current source, and for S-parameters it changes between being an ideal matched load and not.

3.2.3 Large-Signal analysis

In large-signal analysis the input drive response as well as the frequency response are calculated. As discussed in subsection 2.5, over-harmonics of a signal causes distortion in a non-linear amplifier, and this is a mathematical description of physical effects in the amplifier. The theory behind Fourier series states that any periodic signal of frequency f_0 can be expressed as a finite of infinite series of harmonics of f_0, including DC. As the CAD are only capable of a finite number of calculations, the number of over-harmonics has to be chosen before simulations, and a higher number give higher simulation time. A good trade-off was found when 16 harmonics was used, which gives 17 simulation points including DC. To account for input drive, several source exist for the desiger to choose from. In this project, both the *V_1Tone* voltage source and the *P_1Tone* power source was used, as these are proportional to ξ and ξ^2 respectively. Simple ADS syntax also makes it easy to change between linear scale and dBm-scale in using the power source.

As mentioned above, both the drive level and the over-harmonics needs to be variables for the simulation. To achieve this, probe components are used, which is shown in figure 35. When used in simulations, the probes generate a $A \times B$ matrix, where A is the vector of harmonic components of f_0 and B the vector of drive level data points. For more complex simulations, the value of f_0 can also become a variable, in which the probe components generate a 3-dimensional $C \times (A \times B)$ matrix, where C is the vector of swept frequencies. This setup is used throughout subsection 4.3, with $C = [4.4GHz, 4.7GHz, 5.0GHz]$.

3.2.4 Optimization

Optimization was used throughout the design period, and was an important tool for this project. Optimization is indeed a vital tool for all Rf designers, as it takes many order of magnitude less time than manually tuning a system with many variables. Using optimization also takes control away from the designer, and it is therefore very important in setting up the optimization correctly. In subsection 5 it will be discussed that indeed the wrong use of optimization goals may have caused results that could have been improved if other optimization goals was used. One advantage of ADS is that both small-signal and large-signal results can be manipulated algebraically mid-simulations, allowing their results to be calculated and used for optimization in real time. A number of optimization types exist, though only two has been used in this project, which is *Random* and *Gradient*. As the name implies, Random uses an algorithm to randomly check different values within the pre-defined variable range. Gradient uses a more complex algorithm to check the first derivatives of the error from the ideal values, and can thereby find a set of variable values where changing any variable a small *Delta* would increase the errors, thus implying a local point where all variables are optimized.

3.3 Pitfalls of Power Amplifiers in MMIC

There are a few pitfalls in making MMIC Power Amplifiers that a designer should be aware of before implementation. This subsection introduces some aspects which was fundamental in the design process.

One on the major challenges is to make find a good trade off between size and performance. As discussed in subsection 2.3, MMIC areas should generally be in the scale of $1mm^2$ to $10mm^2$. This poses a challenge for the PA designer, since the currents in a PA design can generally be relative large. In basic theory [2], using two class-B amplifiers for the Doherty circuit, the whole design should ideally have $\mu = 78.5\%$ efficiency at $P_{out,max}$, which is equal to 20W. This means that at $P_{out,max}$, the DC sources should deliver a total of $P_{DC} = P_{out,max}/0.785 = 25.48W$. With $U_{dc} = 28V$, this roughly means that a total DC current of $2A$ would flow through the circuit. In reality, due to component loss and mismatch among other factors, μ is lower than its theoretical max value, and in this project it will be seen to be around 60% at $P_{out,max}$. This indicates that a larger DC-current flows in the circuit. In subsection 2.3, it was shown that the CREE MMIC components had a maximum $[mA/\mu m]$-rating, which means that the components would have to increase in size to accommodate this limitation. By not taking the current density

restriction into consideration, a designer risks having the components overheat or burn up. This in turn challenges the small area MMIC advantage, and a designer needs to find a good compromise between size and performance.

Further, when operating with large power outputs, the transistors need to increase its size to accommodate for the relative large drain currents. As given by the Olavsbråten parasite model, the values of the transistor parasites are geometry dependant, and increases with size. As a rule of thumb, this applies to passive MMIC components as well, the more it will deviate with frequency and with varying power levels.

3.4 Comparison of MMIC and ideal passive components

3.4.1 Finding MMIC components from ideal components

As resistors, capacitors and inductors in the CREE MMIC foundry are only defined by their geometrical size, the equivalent value of the component can be found by comparing the impedance values of the MMIC and the ideal component in the wanted frequency band. As a starting point for resistors and capacitors, equation 2.3 and 2.4 can be used, but Z-parameter analysis as still necessary to find exact measured values. By making the MMIC and the ideal component each a 1-port network, measuring the Z-parameters of the network would then give the impedance value of the component. This method is best understood with an example, given in figure 36 using a capacitor.

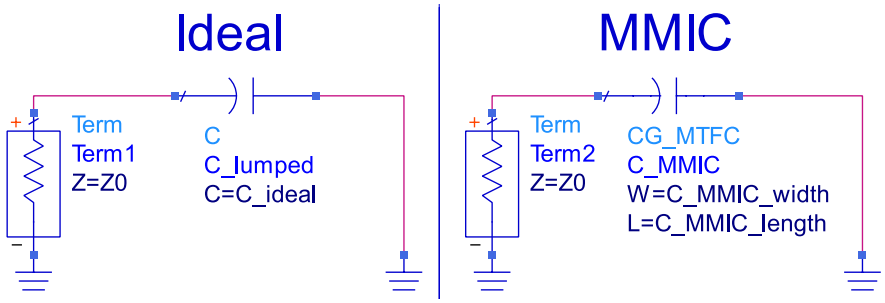


Figure 36: Z-parameter setup

For the example, an ideal capacitor of $C_{ideal} = 6pF$ is used. In setting up a two-port Z-parameter simulation, which de-facto is two 1-port simulations, and using the Z-parameter definition given in equation 2.2, the values of Z_{11} and Z_{22} equals the ohmic impedance value of the ideal and MMIC capacitor respectively. Thus,

for an MMIC designer, with any impedance given as $Z = R + jX$, the goal is to minimize

$$\Delta Real(Z) = |R_{ideal} - R_{MMIC}| \tag{3.1a}$$

$$\Delta Imag(Z) = |X_{ideal} - X_{MMIC}| \tag{3.1b}$$

Minimizing equations 3.1a and 3.1a is done by tuning the geometrical values of the MMIC component. For this exemplified $6pF$ capacitor, the corresponding width and length of the MMIC component was found by tuning to be $240um$ and $120um$ respectively. Inserting these values into equation 2.4 with C_A found in [6] and $C_p = 0$ gives C_{eq} at a little more than $5pF$ (exact value omitted for secrecy reasons), indicating a quite large deviation between calculated and measured values. This is probably mainly due to the lack frequency dependence in the calculated value. Continuing the Z-parameter analysis, the corresponding $\Delta Real(Z)$ and $\Delta Imag(Z)$-values are shown in figure 37. Any resistive value for Z_{22} are pure loss and thereby unwanted. If a resistor was used, any reactive value would create an unwanted phase shift across the component.

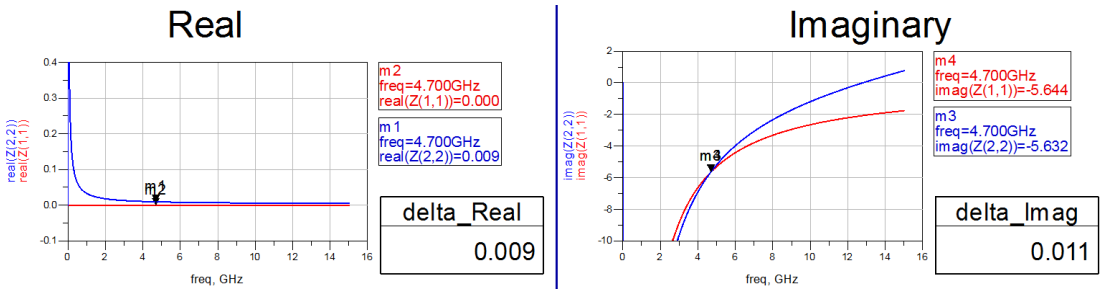


Figure 37: Z-parameter results

Figure 37 reveals that the MMIC capacitor has an unwanted resistance $R = 9m\Omega$, which generally is small and can be neglected. The reactance difference at f_0 equals $X = 11m\Omega$, which also can be regarded as small. Having the impedance value, the equivalent capacitance and inductance value can be found using the well known formulas

$$C_{eq} = \frac{-1}{2\pi * freq * imag(Z)} \tag{3.2a}$$

$$L_{eq} = \frac{imag(Z)}{2\pi * freq} \tag{3.2b}$$

f_k	$C_{eq}(f_k)$	ΔC_{eq}
$4.4GHz$	$6.138pF$	2.1%
$4.7GHz$	$6.012pF$	0%
$5.0GHz$	$5.899pF$	1.88%

Table 6: Center and fringe values in the design frequency band

Continuing the $C_{ideal} = 6pF$ example, equation 3.2a is used to equate the equivalent MMIC capacitance, which yields $6.012pF$. This is shown in figure 38

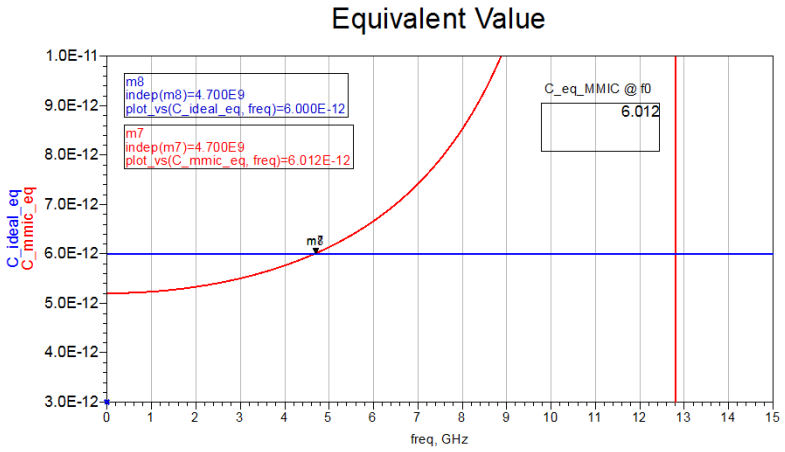


Figure 38: Equivalent capacitance

3.4.2 Frequency dependence

As shown in figure 38 the equivalent value of a MMIC capacitance are varying with frequency, which indicates a limited bandwidth of use. Table 6 gives the equivalent capacitance for the fringe and center frequency in the design bandwidth. Here, equation 2.35 is used for ΔC_{eq}

Table 6 reveals the MMIC capacitor to have a relative small deviation within the f_0-band, and the capacitor are readily a good equivalent of the ideal capacitor. Similar calculations to the above could be made for the MMIC inductor, but this component generally have too many variables to make a simple geometry-inductance relation. Still, finding MMIC inductors from ideal inductors are done using the same method as for the capacitor, where each geometry variable are tuned to give the wanted results.

3.4.3 Resonance

In figure 38, it can be seen an asymptote at $f \approx 12.8GHz$, where C_{MMIC} decreases rapidly. By inspecting the same frequency in figure 37, it can be seen that the reactance here is zero and becoming positive, and thus becomes an inductor. This can be illustrated by using a smith chart, where resonance occur in the low ohmic area of the chart, going from the capacitive to the inductive area. This is shown in figure 39

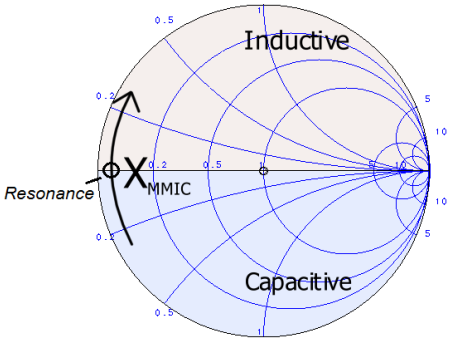


Figure 39: Smith Chart illustration of resonance

For a designer, the resonance point should not affect the circuit greatly as long as it is a distance from the f_0-band. As readily seen in figure 37, the deviation from the wanted reactance value increases logarithmically as it approaches resonance frequency, and thus the fringe values of table 6 would increase if the resonance frequency was closer to the fundamental band. As a rule of thumb, the resonance should occur at frequencies above the 2nd harmonic band.

3.5 Transistor Type and Sizes

At the start of the design process, transistor types and sizes needs to be chosen to which the rest of the Doherty network will be designed around. In the CREE MMIC foundry, a designer have to make some choices in choosing a transistor. With the exception of a switching FET, all transistors are HEMTs, making the choice to use HEMT obvious. Among the HEMTs, the designer has to make three transistor choices:

- 28V or 50V design drain voltage.
- Version 3 (v3) or version 4 (v4) components.

- VIA or NOVIA.

The first choice of design drain voltage relates directly to the supported power levels. As a rule of thumb, a designer should choose the smaller transistor if this one still satisfy the output power specifications. As given in equation 2.7, designing the class-B amplifier for $10W$, a drain voltage $U_{DS} = 28V$ gives currents well within the maximum ratings for the transistor given in [6], thus the $28V$ design drain voltage was chosen. Next, the difference between the v3 and v4 components is found by further examining the datasheet values [6]. As explained in subsection 2.4, R_{ON} indicates the increase rate from which I_D in the I-V goes from cut-off to saturation for the maximum applied U_{GS}. In practical terms, a lower R_{ON} means the transistor reach saturation for a lower U_{DS}-value, which in terms allow for a larger voltage swing in class-B operation. A larger voltage swing means larger power swing, and ultimately larger output power. The v3 transistors have a smaller R_{ON} compared to the v4, and the v3 transistors are therefore a natural choice. This comes at the cost of small-signal gain, where the v4 transistors are better. Thus the v3 components are best suited for PAs, while the v4 components are best suited for low power/low noise amplifiers. Last choice is whether to use the VIA or NOVIA transistors. The NOVIA transistors lets Source be a node in the design, where a designer may add other components. The VIA transistor on the other hand creates a VIA hole on Source directly to the ground plate, grounding this node directly. The choice was made to use the VIA component since this gives less variables in the overall design. It is not uncommon to attach passive components to the Source node to achieve certain functionality, most often stabilization [2], but this was not explored in this project due to knowledge and experience constraints from the designer. Summarizing the choices, the CG28v3_HEMT_VIA_r6 transistor was the natural choice.

3.5.1 Class-AB Transistor

The main motivation behind the class-B amplifier was for it to deliver at least $P_{OPT} = 10W$ in saturation, while keeping R_{OPT} as high as possible and the transistor as small as possible. To avoid unideal behaviour in the cut-off/linear region transition, the gate bias U_{GS} was chosen to be $-3.0V$, which is a small ΔU_{GS} value above the ideal class-B bias of $-3.2V$. To account for some loss in the external circuitry, a $P_{OPT} = 10.7W$ was chosen. Using equation 2.6 for the resulting current, this yields $R_{OPT} = 14.1\Omega$, with corresponding transistor size Ngf = 6 and Wg = $340\mu m$. The given R_{OPT} value are generally low, and recalling equation 2.53, this would make R_L smaller, which could be a problem if the design is to be

matched for 50Ω on the output. Still, considering the large powers and currents of a PA, it is natural that R_{OPT} is small, and a designer should take this into consideration.

3.5.2 Class-C Transistor

As described in subsection 2.8, the class-C transistor should be scaled up from the class-B to deliver a $I_{max,classC} \approx 2.5 I_{max,classB}$. Since the voltages of the DC-simulation remains constant, this equals $P_{OPT,classC} = 2.5 P_{OPT,classB} \approx 25W$. From the semester project, and originally in the design process, a class-C transistor size of $Ngf = 8$ and Wg = $600\mu m$ was chosen, as this size yields $P_{OPT} = 25.77W$. This was also a convenient transistor size since it's the biggest allowed without increasing Gate-Source-Gate (GSG) width, thus allowing for a somewhat smaller transistor area usage. Though during the design process, using large-signal analysis, it was difficult to make this transistor reach saturation for $P_{classC,out} = 10W$ (i.e. to "stop" at $10W$), which in turn distorts the loadpull effect. It was therefore found experimentally that lowering the class-C transistor size to Ngf = 6 and Wg = $430\mu m$, while decresing the $|U_{GS}|$ value (i.e. making it less negative), yielded the best results for the Doherty. The reasons for this will be further explained in section 5.

3.6 Input Network

As shown in figure 34, the methodology in designing the input network was to first implement the network for the class-AB amplifier, then copy the network topology, including values to the class-C design.

3.6.1 Stabilization

In designing the input network of an amplifier, it is common and good design practice to start with stabilization network, as this network gives restrictions on the maximum voltage gain for the amplifier. The motivation in designing the stabilization network was to make it as unstable as allowed while remaining unconditionally stable. This choice can be justified because real component will always add some extra loss, thus making physical design more stable than a simulated one. Also, adding real MMIC components on input match network and output network adds

extra loss after the stabilization network is designed. The chosen stabilization circuit topology is shown in figure 40

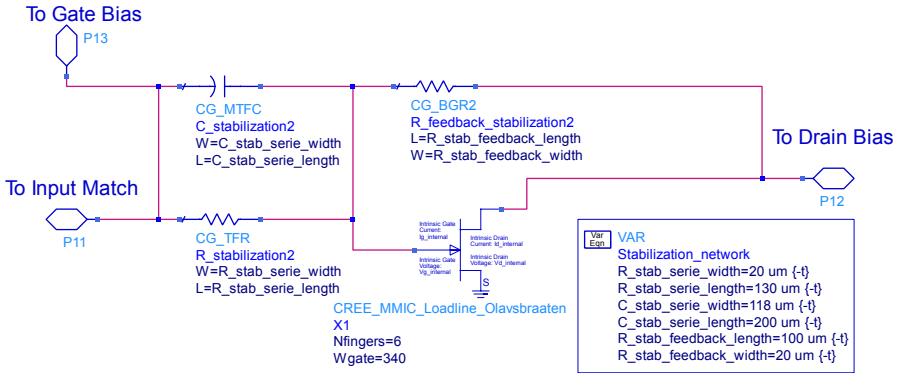


Figure 40: Stabilization Network

The parallel RC-circuit on transistor input gives good stability for low frequencies, where unwanted oscillation is most common. As frequency increases, the impedance over C_{stab} decreases and less input signal power is lost across R_{stab}. Usually, the RC-circuit is not enough to avoid oscillation at higher frequencies, and another component needs to be added to increases high frequency stability. In the semester project [1], a topology with a resistor to ground on transistor input was chosen. Such a resistor would introduce loss which in turn would reduce the voltage gain, which was no concern for the low frequencies used in [1]. For the higher frequencies used in this project, a feedback resistor from Drain to Gate allows high voltage gain while stabilizing high frequency oscillation. The drawback of using such a topology is that the input network becomes dependent of the output network, and $R_{feedback}$ should be chosen high relative to Z_{stab}. Since $R_{feedback} >> R_{stab}$, the BGR2 resistor model was chosen for $R_{feedback}$ and the TFR resistor model chosen for R_{stab}.

3.6.2 Input Matching Network

The input network of the class-B amplifier was created with the wide-band Doherty specifications in mind. The gain and linearity results of the overall Doherty design are limited by the response of the input matching network, and making an input network with good gain across the f_0-band is therefore fundamental for the overall frequency response of the Doherty design. When matching for a single frequency, it is often enough to use two reactive components for matching to 50Ω, but with requirements for an extended bandwidth, an extra component should be used.

As discussed in subsection 3.4, the capacitors should be used over inductors if possible. Also, a capacitor should be used in series to the RF input node to avoid DC leakage to the input, working as a DC block. With these restrictions, and by the method of trial and error, the chosen input network topology is given in figure 41

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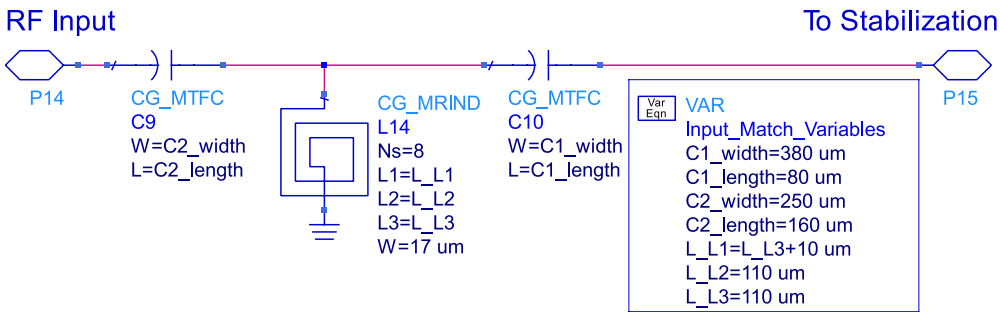


Figure 41: Input matching network

When inserting real MMIC components on the input, this usually introduces extra loss for the overall circuit, making it more stable, but decreasing the possible gain output. Thus the used designing method was to go back and forth between the matching circuit and stabilization circuit to tune for maximum gain and minimum unconditional stability.

3.6.3 Gate Bias Network

The motivation behind the Gate Bias Network was to make it simple, saving area usage and avoiding extra loss. Ideally, the U_{GS} DC source should introduce no current, and a small inductor can be used to choke the RF signal from entering the DC source, while not affect the DC signal flowing in the opposite direction. As mentioned above, using a real MMIC inductor introduces resistive loss which increases stability in the circuit. The inductor used as a RF choke in the Gate Bias Network is shown in figure 42

3.6.4 Complete Input Network

Combining the above mentioned sub networks, the complete input network for both the class-B and class-C input network is shown in figure 43. The only physical

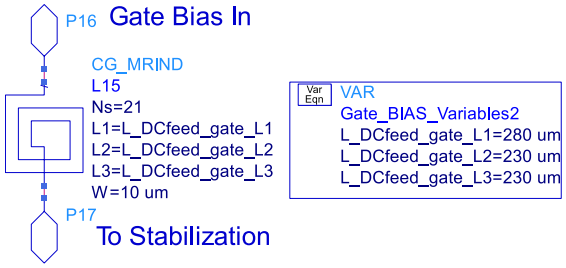


Figure 42: Gate Bias Network Inductor

difference between the them is the transistor size, which is given as Ngf = 6, Wg = 340μm for the class-B PA and Ngf = 6, Wg = 430μm for the class-C PA. The Olavsbråten parasite model was used to measure the current and voltage inside the parasites.

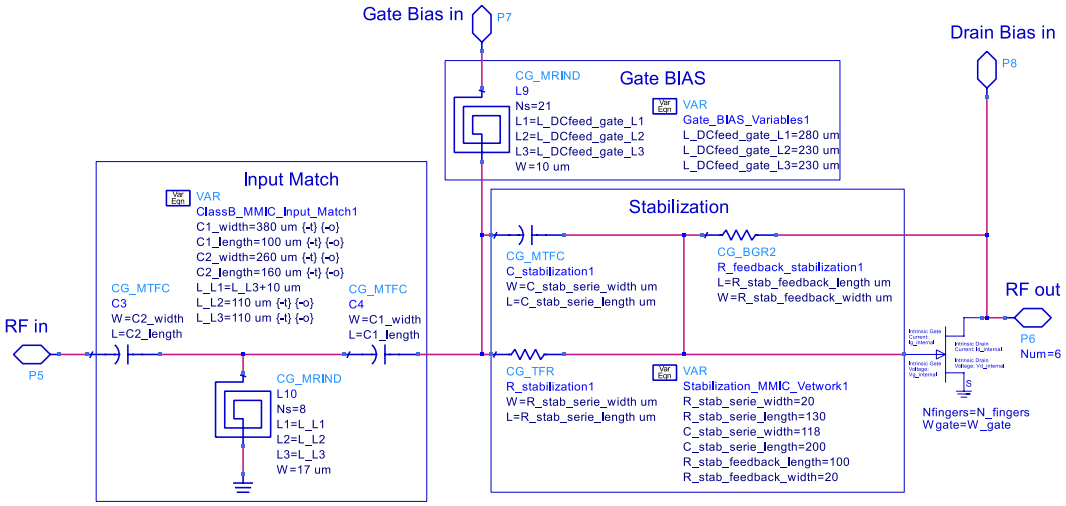


Figure 43: Complete input network

3.7 Output Network

3.7.1 The small-signal approach

As discussed in subsection 2.3, the parasitic values of the transistor could be found by using the Olavsbråten model. In general, the largest currents occur on the Drain node of the transistor, and thus the parasites on this node would cause the biggest impact on the overall behaviour of the circuit. In contrast to the

	Class-B	Class-C
C_{ds}	$0.483pF$	$0.610pF$
R_d	0.763Ω	0.623Ω
L_d	$0.088nH$	$0.099nH$

Table 7: Calculated parasite values

method used in the semester project [1], where the output network was directly implemented using large-signal analysis, the approach used in this project was to first implement the wanted network topology and behaviour using small-signal analysis, and then optimize and tune the values of the topology using large-signal analysis, as shown in figure 34. The idea was to create a circuit which included parasites of both transistors, as well as the Drain Bias Network and Output Match network, as shown in figure 16b. Then, the small-signal behaviour of the circuit could be optimized to become as identical to the ideal Doherty equivalent circuit as possible. Here, a designer must differentiate between using S-parameters and Z-parameters. S-parameters are by definition matched for an impedance, usually 50Ω, and this effectively creates an resistor in parallel with the parasites during simulation, and which may cause simulated results to deviate from actual results. Z-parameters avoids this problem directly from its definition given in equation 2.2, since $I_n = 0$ yields $Z_L \to \infty$. Therefore, Z-parameters was preferred.

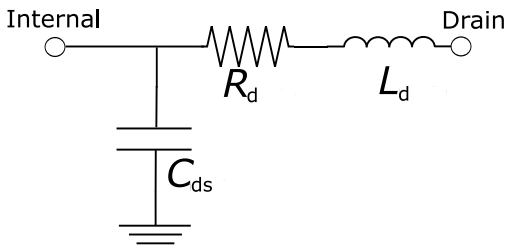


Figure 44: Simplified FET Parasite Model

As the parasites of the drain node is the most prominent in a FET transistor, a simplified parasite model is given in figure 44. By using the equations from the Olavsbråten model, given in [6], the parasite values could be calculated as shown in table 7

Expectedly, C_{ds} and L_d is higher for the larger class-C transistor, while R_d decreases. Knowing the parasite values, the small-signal Doherty model could be set up as shown in figure 45. Next, the Π-equivalent transmission line model was chosen over the T-equivalent to minimize the use of inductors. Comparing the sub-modules of figure 45 to those discussed in subsection 2.5 and 2.8, the max

power gain and the $\lambda/4$ line effect could be achieved by adjusting the values of the Π-equivalent together with the $C_{DCblock,main}$ component. The *Resonant Tank* is more difficult to realize in a system with large bandwidth requirements, and thus the simple CL bandpass filter model does not have sufficient bandwidth to be used in the system. Still, as the L_d and R_d component of both amplifiers are relatively small, the L_{DCfeed} component could be regarded as in parallel with C_{ds}, yielding a resonant tank at $f_0 = 4.7GHz$ if the value of L_{DCfeed} are adjusted accordingly, combining the Drain Bias network and Resonance network into one.

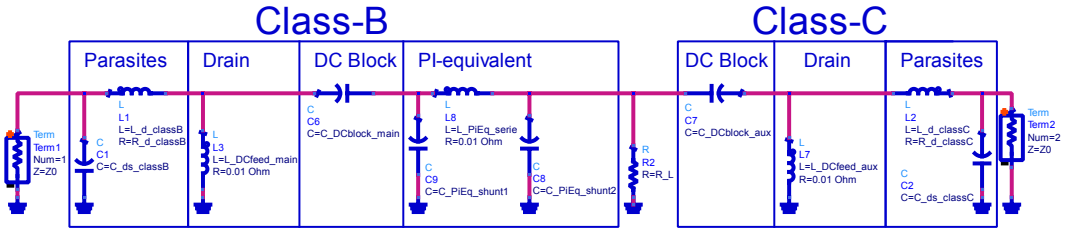


Figure 45: Small-signal Doherty Network

The values of the lumped components in figure 45 was found by performing an ADS Optimization, with goals to minimize the Z-parameter difference from the Doherty equivalent circuit of figure 28b. Ideally, all over-harmonic components should dissipate in the Resonant Tank, and no over-harmonic component should lie across R_L, but examining the Doherty Z-Parameter matrices of the odd and even harmonics, given in equations 2.48a and 2.48a respectively, yields that the resulting $|Z_{21}|$ value for the n-th harmonic is

$$|Z_{21}| = |Z_{12}| = \begin{cases} Z_0 & \text{if } n \text{ is odd} \\ R_L & \text{if } n \text{ is even} \end{cases} \tag{3.3}$$

Ideally, with a perfect resonant tank, $|Z_{21}| = |Z_{12}| = 0$, and here in lies an important restriction of the Doherty equivalent circuit model. To surpass this problem in simulations, a 1-port network was added in shunt to ground. This network was used with ADS' *if-else* syntax yielding full reflection ($S_{11} = 1$) for $f \leq 7GHz$ and full transmission ($S_{11} = -1$) for $f > 7GHz$. The frequency limit was chosen well below the 2nd harmonic band. The resulting ideal Doherty equivalent circuit is shown in figure 46

The optimal lumped components values could then be found by optimization. All variables shown in figure 45 excluding the parasites but including Z_C was allowed to vary within reasonable limits. The optimization was done by making the Z-parameters as close to the ideal as possible in the f_0-band, thus $[Z_{\text{MMIC}}] \rightarrow [Z_{ideal}]$.

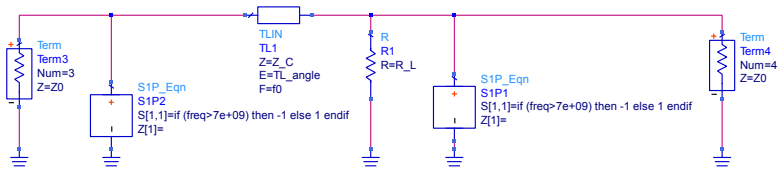


Figure 46: Ideal Doherty equivalent small-signal circuit

For the 2nd harmonic band, it was more practical to use S-parameters with the ideal result of $S_{11} = S_{22} = 1\angle 180°$ and $S_{21} = S_{12} = 0$. Thus the goals could be expressed mathematically as

$$|Z11_{\text{MMIC}} - Z11_{ideal}| \text{ optimized for } (\leq 0.1\Omega \text{ @ } 4.4GHz \leq f_k \leq 5.0GHz) \quad (3.4a)$$

$$|Z12_{\text{MMIC}} - Z12_{ideal}| \text{ optimized for } (\leq 0.1\Omega \text{ @ } 4.4GHz \leq f_k \leq 5.0GHz) \quad (3.4b)$$

$$|Z22_{\text{MMIC}} - Z22_{ideal}| \text{ optimized for } (\leq 0.1\Omega \text{ @ } 4.4GHz \leq f_k \leq 5.0GHz) \quad (3.4c)$$

$$|S11_{\text{MMIC}} - S11_{ideal}| \text{ optimized for } (\leq 0.2 \text{ @ } 8.8GHz \leq f_k \leq 10.0GHz) \quad (3.4d)$$

$$|S12_{\text{MMIC}} - S12_{ideal}| \text{ optimized for } (\leq 0.2 \text{ @ } 8.8GHz \leq f_k \leq 10.0GHz) \quad (3.4e)$$

$$|S22_{\text{MMIC}} - S22_{ideal}| \text{ optimized for } (\leq 0.2 \text{ @ } 8.8GHz \leq f_k \leq 10.0GHz) \quad (3.4f)$$

Running the optimization yielded component value results as shown in figure 47, where the values was rounded for readability.

Var Eqn
VAR
Doherty_Output_Network_Variables
L_DCfeed_main=3.8 nH {o}
L_DCfeed_aux=3.3 nH {o}
C_PiEq_shunt1=930 fF {o}
C_PiEq_shunt2=880 fF {o}
L_PiEq_serie=980 pH {o}
C_DCblock_main=8.6 pF {o}
C_DCblock_aux=10 pF {o}
R_L=20 Ohm {-o}
Z_C=30 Ohm {o}

Figure 47: Component values found from small-signal optimization

The S-parameters in the 2nd-harmonic band was generally given more slack as these produces a higher error in optimization. Comparing the Z_C and R_L to equation 2.53 should theoretically yield a $\xi = 0.67$. After finding the optimal lumped component values, the output network could be inserted into the complete Doherty design.

3.8 Complete Doherty

By combining the input network and output network, the complete Doherty design could be realized. To split the signal between the PAs on the input, an ideal 3-Port S-parameter block was used that allows a designer to state the S-parameters explicitly. Tuning for best results in the final stages of the design process showed that a phase change of $-80°$ rather than $-90°$ gave the best results. By using ADS' probe components, equations could be made to calculate efficiency, over-harmonic components, output power and more directly, allowing these variables to be optimized. The chosen optimization goals were as follows

$$\mu_{Drain} = \frac{P_{out}(@f_0)}{\Sigma P_{DC}} \text{ optimized for } (\geq 0.5 \,@\, P_{BO}) \text{ and } (\geq 0.6 \,@ P_{out,max}) \tag{3.5a}$$

$$P_{out}(@f_0) \text{ optimized for } (\geq 20W \,@\, P_{out,max}) \tag{3.5b}$$

$$|I_{aux}(@f_0)| \text{ optimized for } (\leq 0.1A \text{ for } P_{in} < P_{BO}) \tag{3.5c}$$

$$|U_{main}(@f_0) - U_{aux}(@f_0)| \text{ optimized for } (\leq 4V \text{ for } P_{in} \geq P_{in,max}) \tag{3.5d}$$

$$|I_{main}(@f_0) - I_{aux}(@f_0)| \text{ optimized for } (\leq 0.1A \text{ for } P_{in} \geq P_{in,max}) \tag{3.5e}$$

$$|P_{main}(@f_0) - P_{aux}(@f_0)| \text{ optimized for } (\leq 1.5W \text{ for } P_{in} \geq P_{in,max}) \tag{3.5f}$$

$$|I_{Load}(@2f_0)| \text{ optimized for } (\leq 0.2A \text{ for all } P_{in}) \tag{3.5g}$$

$$|I_{Load}(@3f_0)|, |I_{Load}(@4f_0)| \text{ and } |I_{Load}(@5f_0)| \text{ optimized for } (\leq 0.1A \text{ for all } P_{in}) \tag{3.5h}$$

To avoid confusion, $P_{in,max}$ and $P_{out,max}$ refers to input and output power levels to which the Doherty system reaches saturation. Here, goal 3.5a was chosen with respect to equation 2.16a and figure 31b. Goal 3.5b was chosen according to system specifications. Goals 3.5c, 3.5d, 3.5e and 3.5f was chosen with respect to figures 29a, 29b and 30b respectively, these goals should also ideally force $\xi_b = 0.5$. Goals 3.5g and 3.5h was added to minimize distortion products on I_{Load}, and make the amplifier as linear as possible. All goal values was given some slack compared to their ideal counterpart, allowing the optimizer to find a trade-off between the different goals. As with the small-signal output network, all variables was allowed to vary within reasonable limits. Ideally, the new optimization goals should not change the component values from the output network small-signal analysis significantly, as the goals should not be conflicting. Still, a significantly change occurred, which is to be discussed in section 5. Interchanging lumped components with equivalent MMIC components, and further optimizing the capacitors widths

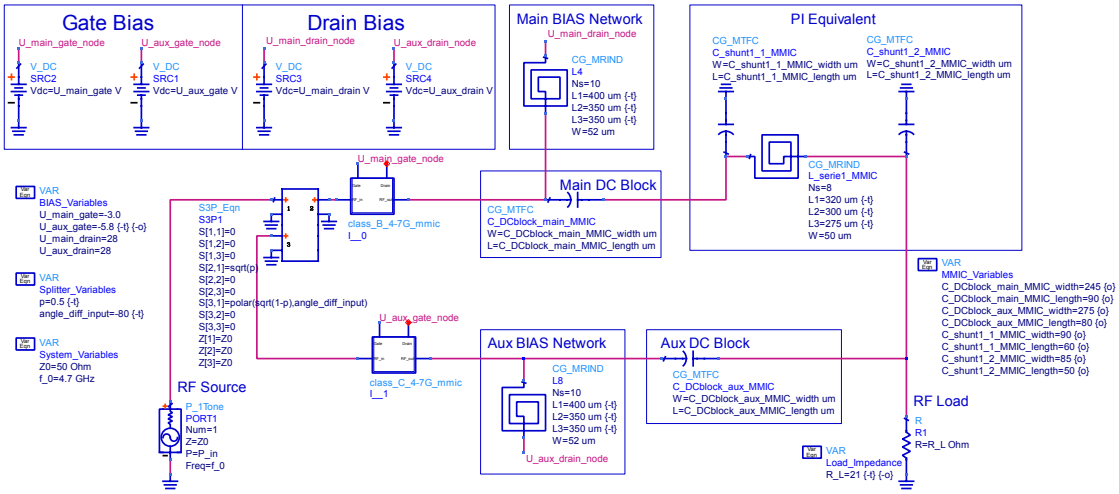


Figure 48: Complete Doherty Power Amplifier

and lengths yield the final Doherty circuit as shown in figure 48, where the class-B and class-C input networks are both given in figure 43. The values is rounded for readability, which had a negligible affect the performance.

4 Results

4.1 Input Network

4.1.1 Input Matching

As stated in subsection 2.5, the aim of the input matching network is to maximize the voltage gain of the circuit, that is to maximize the S(2,1) parameter. By performing a small-signal analysis on the the network topology shown in figure 41, the corresponding S(2,1) plot in db-scale is given in figure 49

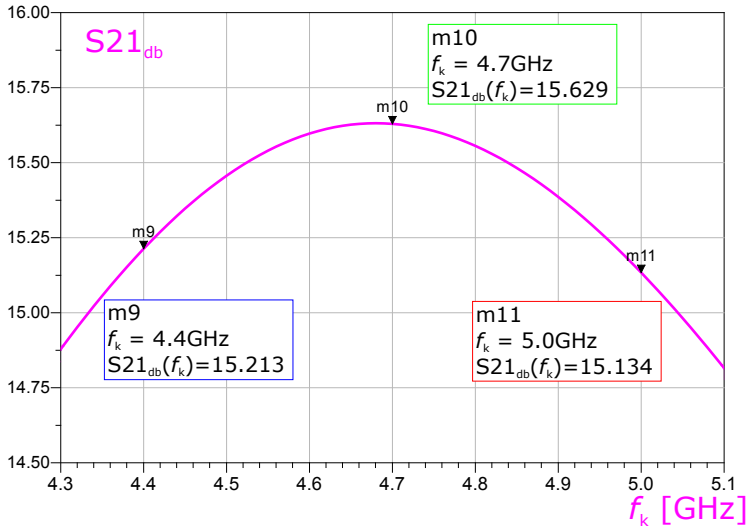


Figure 49: Voltage Gain results

As readily seen, the gain is well above $15dB$ across the band. And, using equation 2.35, the deviation from the center frequency at the fringe band value $f_k = 5.0GHz$ is 3%, which can be considered low, making the in-band gain relatively flat. It can also be expected that the upper fringes of the band yield lower S(2,1)-results than the lower band fringes, as the relative *Maximum Available Gain (MAG)* decreases with frequency. The corresponding S(1,1)-value is given in figure 50

As readily seen from the figure, S(1,1) is inverse proportional to S(2,1), having its lowest value ($f_k \approx 4.75GHz$) close to where S(2,1) has its peak ($f_k \approx 4.7GHz$). This corresponds well with the theory explained in subsection 2.5, where S(1,1) $\rightarrow 0$ was explained to give the best voltage gain. Ideally, the min point of S(1,1) and the max point of S(2,1) should be the same, but tuning for optimal results

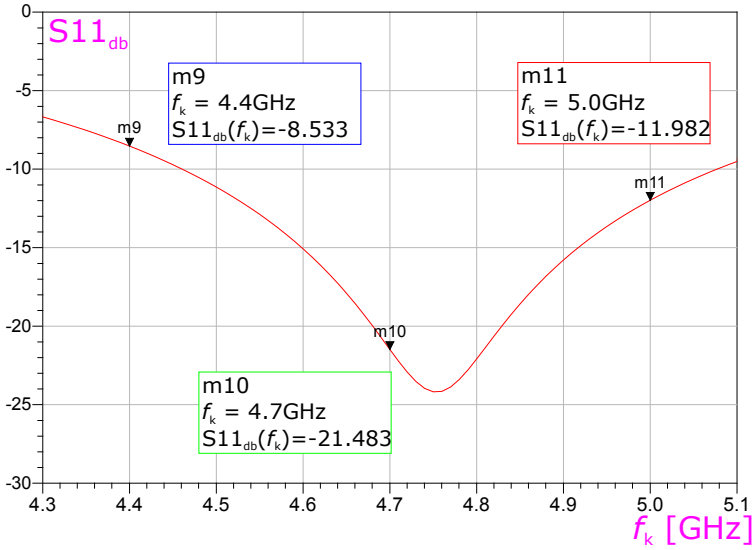


Figure 50: S11 results

showed that by allowing the S(1,1) minimum point to shift slightly, improved the overall in-band gain.

4.1.2 Stabilitzation

The stability for the input network is given in figure 51 with the corresponding minimum values given in table 8. Theoretically, a stable input network would remain stable for any added circuitry on the output, and adding real MMIC components on the output would introduce loss and extra stability. Thus even though having $\mu_{source} = 1$ contradicts the theory in subsection 2.5 which states that $\mu_{source} > 1$ is needed, it can be justified knowing the behaviour of real MMIC components. Although not specified, the minimum value of μ_{source} occurs at DC ($f_k = 0$), and care should be given if a RF signal with a DC component is introduced to the input.

min(K-factor)	$min(\mu_{source})$	$min(\mu_{load})$
1.014	1.000	1.006

Table 8: Minimum Stability Factor values

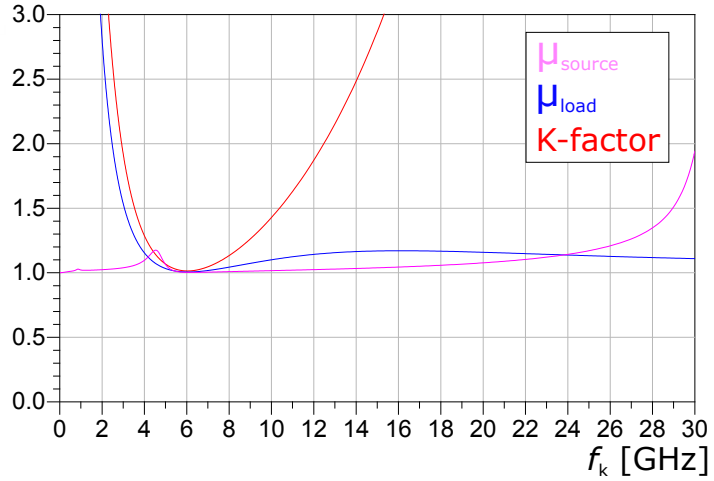


Figure 51: Stability Factors vs frequency

4.2 Output Network - Small-Signal Results

The main goal of the Output Network small-signal analysis was to make the Z-parameters of the output network as similar to the ideal Doherty Z-parameters in the f_0-band as possible. Since Z-parameters are complex, it makes most sense to compare real and the imaginary parts separately. Keeping in mind that $Z12 = Z21$, figure 52 and 53 shows the ohmic values of real and imaginary part of the Z-parameters respectively, while figure 54 shows the Smith Chart behaviour of S11, S12 and S22.

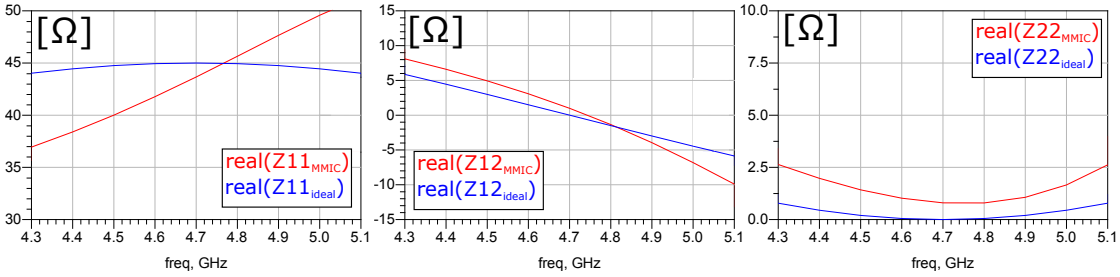


Figure 52: Z-Parameters real values

The deviation from the ideal values can also be expressed with absolute values, as shown in table 9. The biggest deviations in the table occurs for $\Delta real(Z11)$ at $f_k = 4.4GHz$ and $5.0GHz$. Calculating S-parameter deviation in the $2f_0$-band is not as interesting, as the S-parameters at $2f_0$ already contains significant deviation. Making a circuit of lumped components cannot simultaneously match

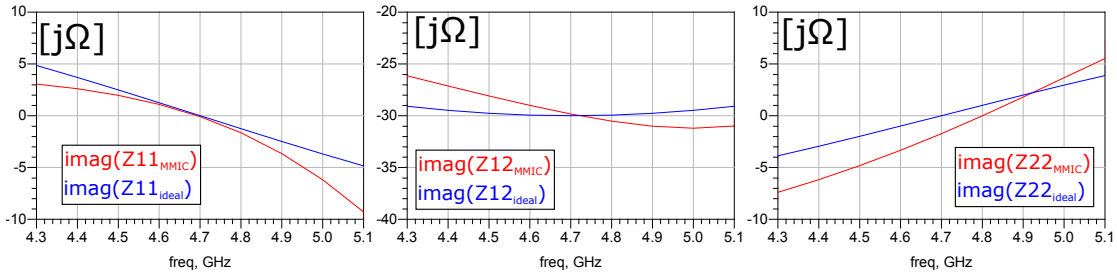


Figure 53: Z-Parameters imaginary values

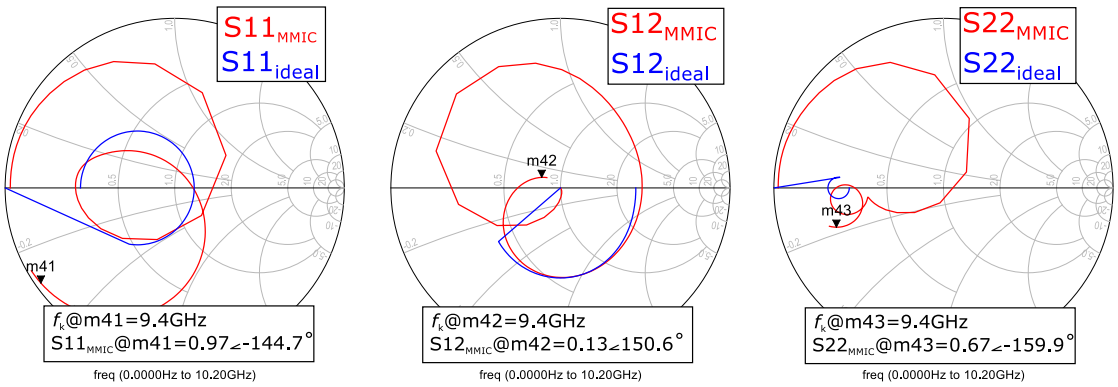


Figure 54: S-parameters Smith Chart

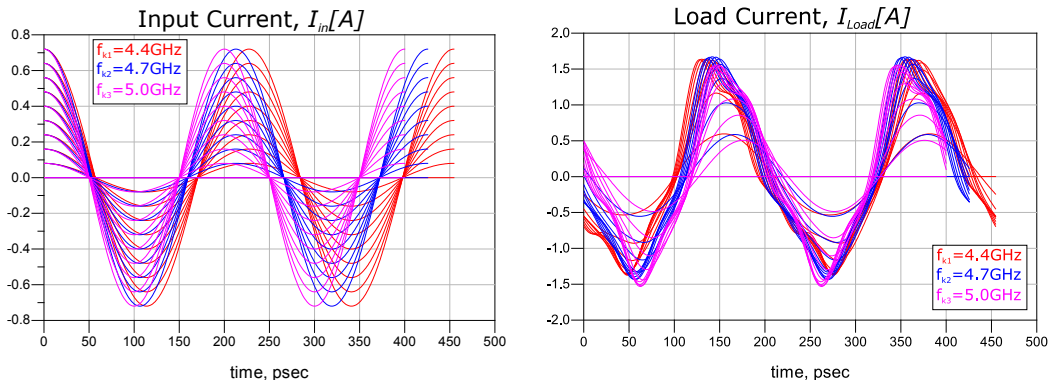
the Z-parameters of an ideal Doherty in the f_0 band while short-circuiting all over-harmonics. Therefore, making a lumped component circuit with the frequency response of the ideal S-parameters in figure 54 should be phsyically impossible. The straight lines in the Smith Chart is for $f_k = 7GHz$ where all over-harmonics is short circuited in the ideal Doherty equivalent circuit.

f_k	$\Delta\mathrm{Re}(Z_{11})$	$\Delta\mathrm{Im}(Z_{11})$	$\Delta\mathrm{Re}(Z_{12})$	$\Delta\mathrm{Im}(Z_{12})$	$\Delta\mathrm{Re}(Z_{22})$	$\Delta\mathrm{Im}(Z_{22})$
4.4	6.05Ω	1.09Ω	2.15Ω	2.35Ω	1.53Ω	3.22Ω
4.7	1.33Ω	0.09Ω	0.99Ω	0.17Ω	0.80Ω	1.74Ω
5.0	5.14Ω	2.50Ω	2.36Ω	1.72Ω	1.21Ω	0.71Ω

Table 9: Z-parameter deviation in f_0-band

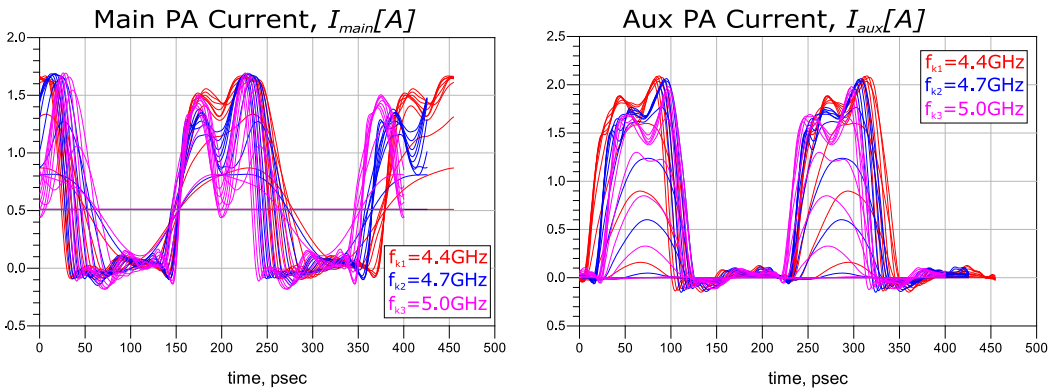
4.3 Complete Doherty

4.3.1 Time-domain analysis and over-harmonic analysis



(a) RF input (b) Load

Figure 55: Input and output RF currents

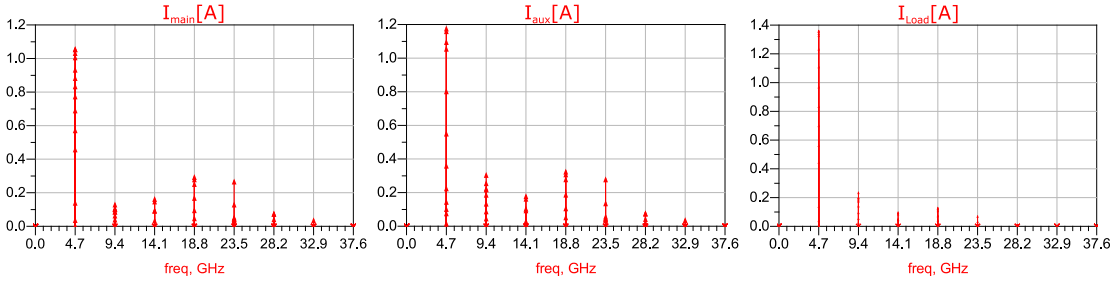


(a) Main PA (b) Aux Pa

Figure 56: RF currents through the transistors

4.3.1.1 Currents Figure 55 and 56 shows the time-domain behaviour of the currents in the Doherty network. The values of I_{main} and I_{aux} are found inside the transistor parasites using the Olavsbråten model, and are the output of the $Id_{internal}$-probe in figure 8. The I_{main} waveform shows resemblance to the ideal half-wave behaviour of an ideal class-B, but over-harmonics make the minimum value less than zero. At strong input drive levels the square wave dips, which is due the the knee-walkback effect, where the I_D of a transistor in saturation decreases for increased input drive. The I_{aux} waveform shows stronger cut-off behaviour

between the half-waves, making the odd-numbered over-harmonics less dominant for the current. The knee-walkback effect of I_{aux} is also less dominant, which is due the lower class-C Gate Biasing. Examining figure 56a closely for low drive levels ($U_{in} \leq 8V$) reveals an interesting property. The waveform behaves as an *inverse class-F* amplifier. Comparing figure 56a to the current waveform of figure 22 shows a clear resemblance to the max flat case of a class-F waveform, with the waveform mirrored horizontally, and the assumption can be made that the 3rd harmonic are the only dominant harmonic here, with $\kappa = 8/9$. This may also be a factor why the design has good efficiency for low drive levels, as will be discussed below. As the Aux PA starts to conduct current, significant over-harmonics are seen out from both PAs. The relative value are also increasing with increased input drive. Still, as seen in figure 55b, the current across the load are significantly more linear, and shows strong unlinearity only for $U_{in} \geq 24V$ ($P_{in} = 2.5W$). The reason for this is best understood by examining figure 57, together with table 10 which gives the magnitude and phase of the fundamental and the over-harmonic currents. As a large number of input drive levels are used in simulations, two sample levels are used in the table to illustrate the behaviour. Lastly, I_{main} are seen to have a DC component of $I_{main,DC} \approx 0.5A$, which is due to distortion products and discussed in more detail under *Loadline Analysis*.



(a) Main PA (b) Aux PA (c) Load

Figure 57: Magnitude of current over-harmonics

The currents $I_{main,T}$ and I_{aux} of table 10 are the currents that are combined before the load, and with respect to figure 48, $I_{main,T}$ and I_{aux} are the output currents of the Π-*equivalent* and *Aux DC Block* respectively. Basic KCL gives $I_{Load} = I_{main,T} + I_{aux}$, and by representing the values of table 10 as complex values, the value of I_{Load} can be seen as the phasor sum of the incident currents. More importantly, the phases of the over-harmonics have in all cases a delta value of $90° \leq \Delta\theta \leq 180°$, which means that both incident currents are close to being in anti-phase, causing destructive interference and yielding a lower magnitude on I_{Load}. This is also the main explanation why the resulting over-harmonic current magnitude-to-carrier for I_{Load} is much lower than for both $I_{main,T}$ and I_{aux}. By

$f_k = nf_0$	U_{in}	$I_{main,T}$	I_{aux}	I_{Load}
$9.4GHz$	$36V$	$0.15\angle 145.1°$	$0.34\angle -80.6°$	$0.26\angle -105.3°$
	$20V$	$0.10\angle 115.0°$	$0.23\angle -114.3°$	$0.18\angle -138.8°$
$14.1GHz$	$36V$	$0.08\angle -83.6°$	$0.09\angle 70.2°$	$0.04\angle 7.4°$
	$20V$	$0.17\angle -157.2°$	$0.19\angle -9.4°$	$0.1\angle -74.3°$
$18.8GHz$	$36V$	$0.26\angle 110.6°$	$0.29\angle -93.3°$	$0.12\angle -159.3°$
	$20V$	$0.26\angle 47.5°$	$0.29\angle -155.9°$	$0.11\angle 139.2°$
$23.5GHz$	$36V$	$0.34\angle -118.2°$	$0.36\angle 46.9°$	$0.09\angle -26.2°$
	$20V$	$0.06\angle 112.6°$	$0.07\angle -82.5°$	$0.02\angle -148.9°$

Table 10: Magnitude and phase of over-harmonic currents of f_0

borrowing the *decibel relative to carrier (dBc)* equation (which is only defined for powers and voltages), given as

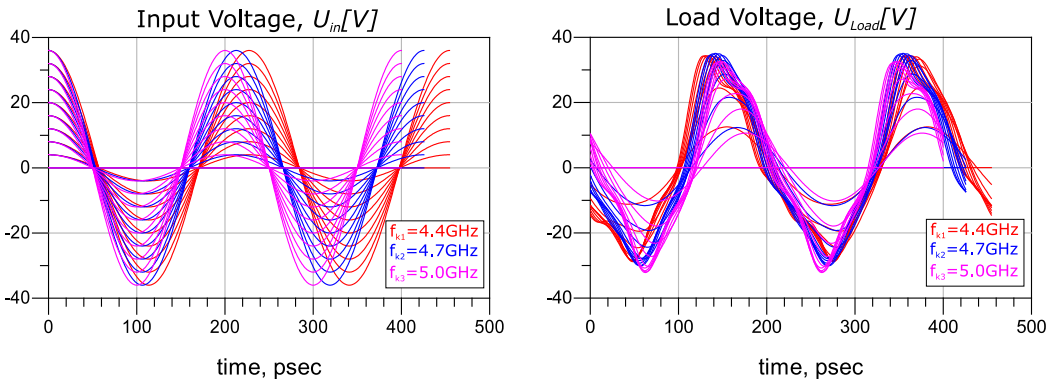
$$S_{dBc} = 20log\frac{|U|}{|U_{carrier}|} \approx 20log\frac{|I|}{|I_{carrier}|} \tag{4.1}$$

The magnitude values of table 10 can be related to the current magnitude at f_0. This is given in table 11, where, for readability reasons only the values for $U_{in} = 36V$ are used.

$f_k = nf_0$	$9.4GHz$	$14.1GHz$	$18.8GHz$	$23.5GHz$
$S_{dBc}(I_{main,T})$	$-16.7dBc$	$-22.6dBc$	$-11.8dBc$	$-9.6dBc$
$S_{dBc}(I_{aux})$	$-10.0dBc$	$-22.0dBc$	$-11.4dBc$	$-9.5dBc$
$S_{dBc}(I_{Load})$	$-14.3dBc$	$-30.9dBc$	$-21.1dBc$	$-23.2dBc$

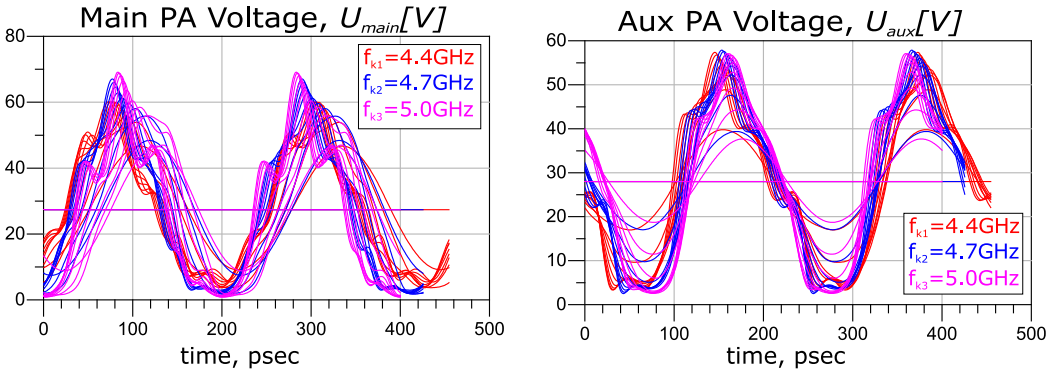
Table 11: decibel-to-carrier values of currents

4.3.1.2 Voltages The time-domain behaviour of the voltages of the Doherty network are given in figure 58 and 59. Compared to I_{main} and I_{aux} of figure 56a and 56b respectively, their counterpart of U_{main} and U_{aux} are seen to behave more linear, yielding a sinusoidal wave form. Thus the S_{dBc} values for all over-harmonics can be expected to be smaller (more negative) compared to the currents. As seen in figure 59a and 59b, the amplitude value never drops below $0V$, which is in accordance with class-B and class-C amplifier theory described in subsection 2.4. As with I_{main}, both U_{main} and U_{aux} are seen to have a DC component of about $28V$, which will be discussed under *Loadline Analysis*



(a) RF input (b) Load

Figure 58: Input and output RF voltages



(a) Main PA (b) Aux Pa

Figure 59: RF voltages across the transitors

4.3.2 Phase of Fundamentals

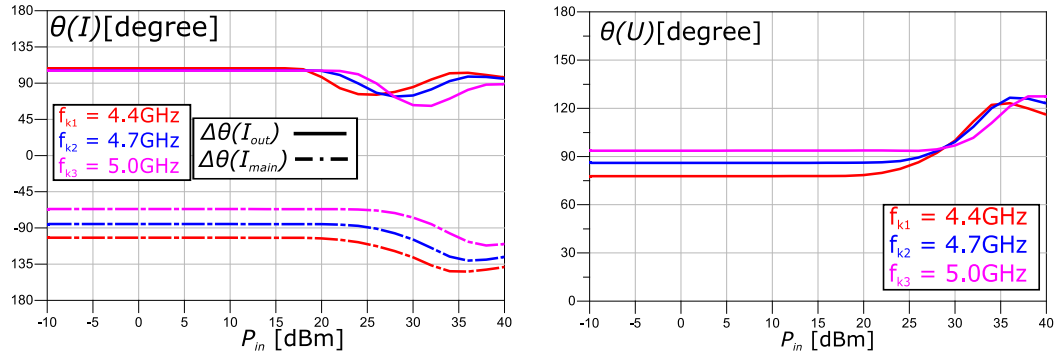
Figure 60a shows the phases of currents in the network. Here, $\Delta\theta(I_{out})$ and $\Delta\theta(I_{main})$ are given as

$$\Delta\theta(I_{main}) = \theta(I_{main,internal}) - \theta(I_{main,T}) \tag{4.2a}$$

$$\Delta\theta(I_{out}) = \theta(I_{main,T}) - \theta(I_{aux}) \tag{4.2b}$$

Put into words, $\Delta\theta(I_{out})$ gives the phase difference of the currents that are combined to give I_{Load}, while $\Delta\theta(I_{main})$ gives the phase difference between the current through the main PA and the current out of the Π-equivalent. As expected, $|\Delta\theta(I_{main})| \approx 90°$ at f_0 which is according to the Doherty theory and

the impedance inverter effect. With respect to figure 60a, the phase deviation from f_0 is 17.3° and 18.6° for f_{k1} and f_{k3} respectively. This is above the theoretical value for a $\lambda/4$ transmission line given in table 4, but still within reasonable limits. Further, examining $\Delta\theta(I_{out})$ reveals results that unfortunately cannot be said to be reasonable. The phase difference of the currents are about 108.5° across the f_0-band, and this value should ideally be 0° which in phasor theory would add them together in-phase. This out-of-phase behaviour of the current poses a serious limitation on the Doherty design, to be further discussed in section 5. Next, examining $\Delta\theta(U_{main})$ of figure 60b expectedly reveals that $\Delta\theta(U_{main}) \approx 90°$ at f_0 with a deviation of 8.2° and 7.6° for f_{k1} and f_{k3} respectively. These numbers are also more in accordance with the theoretical values of table 4 in subsection 2.6. Measuring the difference between $U_{main,T}$ and U_{aux} makes no sense as this is the same voltage.



(a) Fundamental current phase

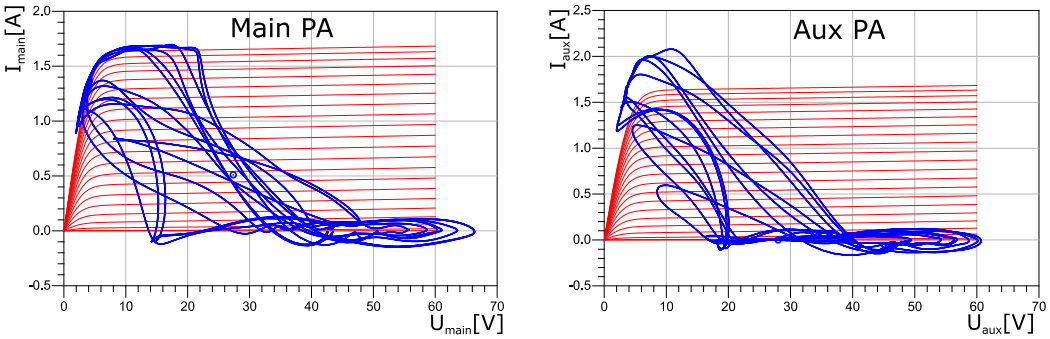
(b) Fundamental voltage phase

Figure 60: Phases of current and voltage fundamentals

4.3.3 Loadline Analysis

With time-domain analysis of both currents and voltages of both PAs given, these could be plotted versus the I-V DC characteristics of the class-B amplifier. With the non-linearities of the currents described above, the resulting Loadline plot cannot be expected to show ideal linear behaviour. Figure 61 shows the loadline behaviour of the main PA and aux PA at f_0. Examining figure 61a closely reveals that at low drive levels, the main PA behaves similar to light class-AB amplifier, with a bias point $U_q \approx= 0.3$ (with reference to table 2). This is surprising as the transistor is biased with $U_q = 0$, but as described in subsection 2.5, distortion from the even over-harmonics may create a DC component. This is likely also because of the significant distortion, seen on the current waveform. As input drive level

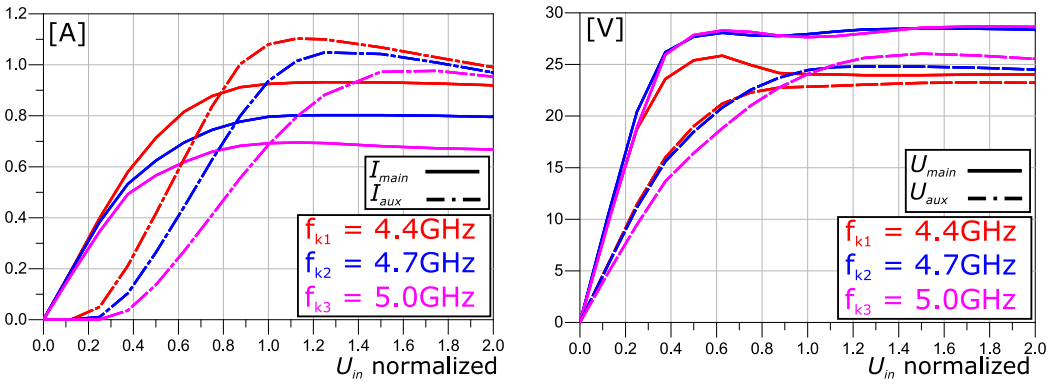
increases, the bias point decreases and more classical class-B loadline behaviour can be seen. In general Doherty theory [2], the main PA loadline should reach the $I_{max}/2$ value at the onset level, and then increase up to I_{max} for $\xi > \xi_b$. This general behaviour can be seen in the figure, but with significant knee-walkback at the highest drive levels, and the conclusion can be made that the class-B amplifier is driven too hard here. Next, the loadline of a class-C PA is expected to increase linearly as both I_{aux} and U_{aux} increases linearly for $\xi_b \leq \xi \leq 1$. This behaviour can also be seen in figure 61b, with a slight change in slope at high drive levels, which is probably due influence from the main PA.



(a) Main PA (b) Aux PA

Figure 61: Loadline characteristics

4.3.4 Currents and Voltage characteristics of fundamental



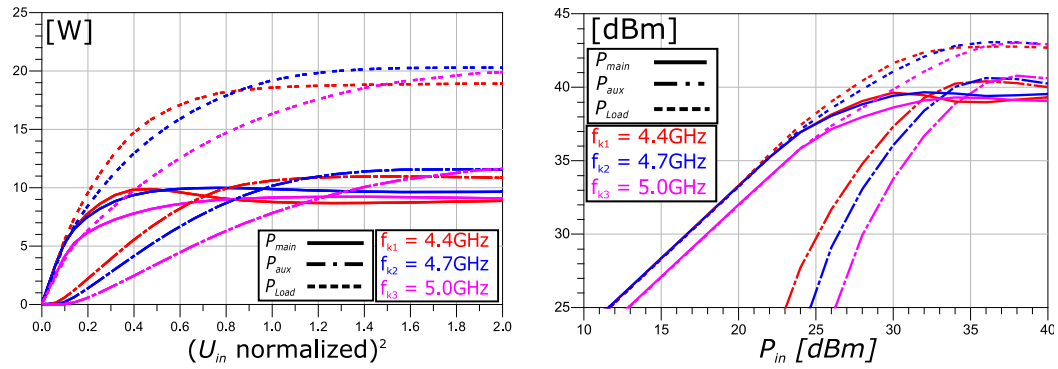
(a) I_{main} and I_{aux} characteristics (b) U_{main} and U_{aux} characteristics

Figure 62: Current and voltage characteristics in the f_0-band

Figure 62 gives the magnitude of the fundamental currents and voltages in the Doherty network. Both figure are plotted versus the normalized input voltage drive

($\bar{U}_{in} = u_{in}/U_{max}$), where U_{max} has been found graphically at $16V$. One problem of using normalized voltages is that the value of U_{max} varies for different frequencies, and may also be inconsistent between current and voltage characteristics. Still, for reading consistency and for a reference value, a normalized $\bar{U}_{in}$ is used. I_{main}, I_{aux}, U_{main} and U_{aux} are all measured inside the parasites using the Olavsbråten parasite model. Analysing figure 62a it's seen that the aux PA is in cut-off for small input drive levels, which corresponds with the theory. Further, it can be estimated that $\xi_b \approx 0.3$ across the f_0-band, corresponding to $U_{in} \approx 5V$. The value of ξ_b is generally low and would cause deviation between I_{main} and I_{aux} in saturation, as shown in figure 29a. This deviation increases for f_{k3}, while it decreases for f_{k1}. Comparing with the voltages in figure 62b show that at f_{k1} both U_{main} and U_{aux} lies below the ideal $U_{dc} = 28V$ in saturation.

4.3.5 Power characteristics



(a) Powers in linear scale

(b) Powers in dB-scale

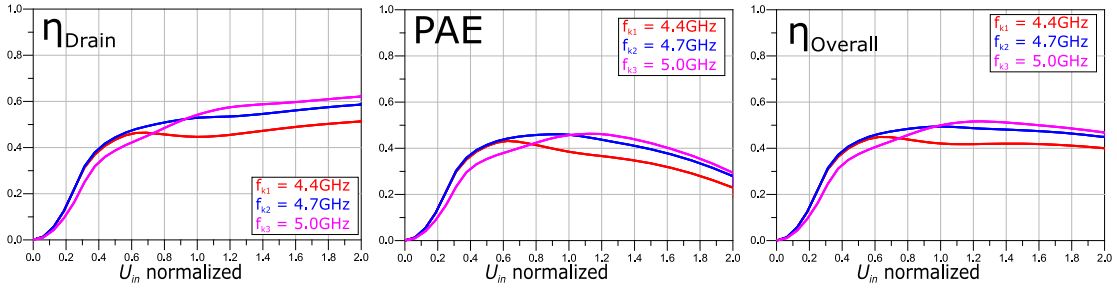
Figure 63: Power characteristics in the f_0-band

Figure 63 gives the powers of the Doherty design both in linear scale and in dBm-scale. Comparing figure 63a to figure 30a reveals that for P_{aux}, a higher f_k value behaves similar to a higher ξ_b value, with P_{aux} at f_{k3} behaving almost similar to the theoretical P_{aux} at $\xi_b = 0.5$. Re-examining figure 56b shows that I_{aux} at f_{k3} has the lowest conduction angle, α, giving it the deepest class-C operation in the f_0-band. A lower α equals a higher ξ_b, which corresponds to the behaviour seen in figure 63a. It's further seen that the system are able to deliver $20W$ at $\xi = 1.2$ at f_0, which is close to being according to specification, as it should ideally occur at $\xi = 1$. As the output match are designed for f_0, it cannot deliver the same output power across the band, and are unfortunately not able to deliver $20W$ across the f_0-band. P_{Load} are able to deliver $18.9W$ and $19.8W$ for f_{k1} and f_{k3} respectively.

Figure 63b shows the system powers in dBm-scale. Compared to the theoretical theoretical power curve of the fundamental frequency in figure 18, the curve for P_{Load} is not perfectly linear until the saturation point. At $P_{in} \approx 25dBm$, the curve changes slope slightly, which is due to the onset of the Aux PA, corresponding to $\xi_b = 0.3$. The 1dB compression point for P_{Load} at f_{k1}, f_{k2} and f_{k3} can be graphically at $P_{in} = 33dBm$, $35dBm$ and $36dBm$ respectively.

4.3.6 Efficiency

The main purpose of the Doherty amplifier is its enhanced efficiency characteristics, and examining the systems efficiency is therefore vital in determining the quality of the design. In subsection 2.5, three methods of calculating efficiency was given. The simulated value of these are shown in figure 64 and were found by calculating fundamental of P_{Load} vs the sum of all frequency components (including DC) of P_{DC} and P_{in}. Starting with figure 64a, η_{Drain} for $f_{k2} = f_0$ does not show the perfect Doherty characteristics shown in figure 31a with its distinctive peak at ξ_b. The main reason for this is due to an imperfect loadpull effect at the onset level, where U_{main} is not pulled correctly by I_{aux}. Also, the onset level can be estimated to be $\xi_b \approx 0.5$ which is higher than the estimated $\xi_b = 0.3$ above, which means less efficiency at backed-off levels. Still, the η_{Drain} for f_0 is generally good, yielding above 53% in $0dB$ backoff, above 44% in $6dB$ backoff and above 30% in $10.5dB$ backoff ($\xi_b = 0.3$). Incidentally, η_{Drain} for f_{k1} give the most distinctive Doherty curve, with its characteristic peak at onset. It also has the lowest mean efficiency, well below 50%. Comparing with figure 63a reveals that P_{Load} at f_{k1} has the most linear response of the three, but does also deliver the lowest output power in saturation. The reason all η curves keep increasing is due to the low simulated thermal resistance, R_{th} of the transitor, which allows for more voltage through the channel in deep saturation. Next, η_{Drain} at f_{k3} has less efficiency in backoff, but does indeed exceed η_{Drain} at f_0 for high drive levels. This is due to the class-C property of the aux PA at higher frequencies described above. Next, figure 64b shows expectedly that the PAE decreases for increasing drive levels. For $\xi = 2$, the PAE @f_{k1} is down to 20%, which may indicate very bad efficiency for the system. But as discussed in subsection 2.5, PAE has some limitations in measuring a systems efficiency. Figure 64c gives the $\eta_{Overall}$ of the system, and are readily seen to give a middle ground between η_{Drain} and PAE, indicating its usability as an efficiency indicator. As with PAE, $\eta_{Overall}$ decreases for increased drive levels.



(a) Drain efficiency (b) PAE (c) Overall efficiency

Figure 64: Efficiency characteristics in the f_0-band

4.3.7 Power gain

The main purpose of an RF PA is indeed to amplify a RF signal, and any discussion of the PA characteristics would be insufficient without discussing its gain. In subsection 49, the voltage gain was found to be above 15dB across the f_0-band. The resulting power gain is given in figure 65 are are shown to be well below 15dB before saturation. The gain for both f_{k1} and f_{k2} have a flat characteristic with gain value at about 13.3dB for $P_{in} \leq 20dBm$. Having a lower power gain than voltage gain is expected due to a number of factors. Mismatch between R_{OPT}, Z_C and R_L may be one factor, and ohmic loss in MMIC components may be another. A deviation of about 2dB between the voltage gain and power gain is therefore within reasonable limits. As $S_{21}@f_{k2}$ is about 0.45dB better than $S_{21}@f_{k1}$ in figure 49, then the power gain at f_{k1} is generally better than at f_{k2}. Last, the power gain at f_{k3} lies quite flat at 12.2dB before saturation, which is well below the other frequencies. This is due to the class-C effect desribed above, where the lower conduction angle and higher efficiency are traded off for lower gain.

4.4 Layout and Size measurements

The main focus in this project was to develop a circuit that gave the wanted wide-band Doherty behaviour, and generally explore methods of making the Doherty less frequency dependant. It was therefore made a choice not to focus on the MMIC layout, and thereby give the components some more freedom in size. Still, as MMIC is a very practical way of implementing RF circuits, the layout measurements cannot be ignored completely. In the final stages of the project period, the author implemented a MMIC layout of the complete Doherty network from figure 48, with all passive and active component sizes as chosen in the design. For

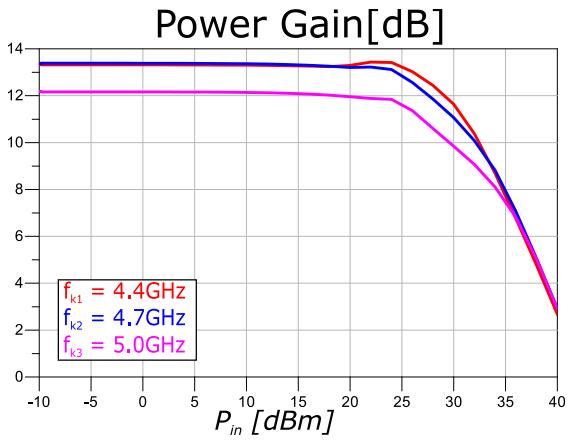


Figure 65: Power Gain in the f_0-band

interconnect between the components, the microstrip transmission line was used with default parameters. Due to the copy-righted nature of the CREE foundry, the complete Doherty layout is not given here, but can be found in [6]. The layout has not been simulated, and has also not been optimized for size usage, and are only meant to give the reader a visual understanding of the complete Doherty network.

4.4.1 Size measurements

The total area of the layout in [6] became roughly $(3.28mm \times 1.50mm) = 4.92mm^2$, which is within the practical limits of an MMIC circuit given in subsection 2.3, but still in the upper range. As mentioned above, this layout is not optimized for area usage, and could be made smaller. To find the sizes and area usage of the complete Doherty design without the microstrip interconnects, the size of each component was found separately and then added together. For the resistor and capacitor, this was simply done as $length \times width$, while for the inductor this was done as $L1 \times L2$. For each transistor, this was found visually in the layout. Semantically, IN denotes the Input Networks, ON denotes the Output Networks and Q denotes the HEMT transistors. The results are shown in table 12.

	$A_{IN,m}$	$A_{IN,a}$	$A_{Q,m}$	$A_{Q,a}$	$A_{ON,m}$	$A_{ON,a}$	$\boldsymbol{A_{tot}}$
Sizes $[mm^2]$	0.176	0.176	0.267	0.321	0.270	0.162	**1.327**

Table 12: Calculated MMIC network area usage

5 Discussion

For many practical systems, including MMIC, an efficiency of $50 - 60\%$ is considered good [3], making the results in figure 63a decent on any account.

5.1 Amplifier results and behaviour

5.1.1 Transistor Choice and Input Network

Choosing transistor size for the main PA was done according to theory, and gave the wanted results. The size for the aux PA was in contrast found experimentally. As mentioned in subsection 3.5, the choice was originally to use Ngf = 8 and Wg = $600\mu m$, but better overall results was found in the large-signal analysis using a smaller transistor and decreasing the Bias voltage. This makes the aux PA behave more asa class-B PA. It's difficult to establish exact reasons for this, as it is somewhat counter to the theory. On possible reason is that as a PA is biased deeper into class-C operation, the conduction angle becomes smaller and the resultant I_{aux} wave form becomes steeper. This also makes it more sensitive to phase deviations when added together with I_{main}. In improving the current phase deviations of the system, changing aux PA size and biasing should be explored further. The results from the input network showed overall good results, with perhaps frequency response of the S_{21} gain as the most predominant. The maximum $|S_{21}|$ value of 15.6dB at f_0 combined with a relative low deviation of 3% for $f_k = 5.0GHz$ are good results in the authors opinion considering the relatively high RF frequency and that real MMIC components are used. For the stabilization network, using a feedback resistor gave much better gain compared to using a resistor to ground, which was used in the semester project [1]. Though using a feedback resistor creates a Gate-Drain connection that may cause unwanted results, and it also gives the designer less control. In designing the small-signal output network, the current sources was assumed to be ideal, with zero capacitance, but in using a feedback loop, this equivalent circuit is effectively no longer true. Still, the $R_{feedback}$ value should be quite large, measured to $Z_{feedback} = (1936 - j547)\Omega$ at f_0. This also indicates a strong capacitive effect of the BGR2 resistor at high frequencies. It was verified post-production that the feedback loop did not affect the behaviour of the output network significantly, where removing $R_{feedfback}$ did not significantly change the results, but this was only done superficially, and this should perhaps be explored in more detail as it may be a source of error.

5.1.2 Output Network and Small-Signal model

One of the goals of this project was to use small-signal analysis and Z-parameters to find a output network topology which would yield results close to the ideal Doherty equivalent circuit, and hopefully would make the large-signal analysis easier. Inserting the components into the complete Doherty network, given in figure 48 did unfortunately not yield the wanted results, with little of the characteristic Doherty behaviour found using large-signal analysis. This may be due to several reasons. For one, it is assumes that the numeric values from the Olavsbråten parasite model is correct. As described in subsection 2.3, the model only gives the parasites as dependent on transistor size, and any frequency or drive level dependence is not included, which may cause errors in the large-signal analysis. Another general obstacle in optimizing the small-signal model was the large degree of freedom used. Here, all variables, including R_L and Z_C was allowed to vary within reasonable limits. Although it may sound as an advantage, the high degree of freedom forces the system to minimize the numerical Z-parameter deviation, rather than to give the wanted Doherty behaviour. In subsection 2.8, theoretical doherty behaviour was given for $\xi_b = 0.3$, 0.4 and 0.5, and it would perhaps yield better results if R_L was fixed (using for example $R_L = 25\Omega$ from [2]), and then only allow Z_C to vary between $R_L/0.5$ and $R_L/0.3$. Also, for the Π-equivalent it may have been more advantageous to force $C_{\Pi 1} = C_{\Pi 2}$. Generally speaking, giving the optimizer too much freedom may partly be the reason for the un-ideal small-signal results. Last, by studying the results in figure 52, 53 and 54 reveals a significant deviation for $real(Z11_{\text{MMIC}})$ at $f_k = 4.4GHz$ and $5.0GHz$, with a percentage deviation of 13.5% and 11.6% from the ideal value respectively. Examining the $real(Z11)$ graph also reveals that the $real(Z11_{\text{MMIC}})$ curve behaviour deviates significantly from the $real(Z11_{\text{ideal}})$. Examining the smith chart behaviour for $2f_0$ also reveals significant deviation for $S22$. These deviations combined may also add to the un-ideal behaviour.

The goal of using the small-signal model was to find a simple, efficient and fast way of designing the output network of the Doherty, and to minimize the use of large-signal analysis, as this generally introduces complexity in both implementation and simulations. The conclusion here is not that the small-signal model is useless, but rather that it has to be used with care. By giving the optimizer less freedom, and by carefully choosing network topology, the small-signal model can still be a strong tool for the PA designer.

5.1.3 Complete Doherty

As shown in subsection 4.3, a phase difference of 108.5° between I_{main} and I_{aux} at f_0 gave sub-optimal current results on the output. As I_{Load} is the phasor sum of I_{main} and I_{aux}, $|I_{Load}|$ could have been increased further if lass phase difference was achieved. The reason for this phase difference was due to the optimization variables chosen, and this result could be improved if more care was given to the optimization goals. Still, examining the current, voltage and power characteristics of the fundamental shows strong resemblance to their theoretical values, and showed that lumped components could indeed create a Doherty system with good loadpull effect and overall quite linear response. As the Doherty loadpull inverts voltages and currents relative to each other, the highest voltages and lowest current occurred at 4.4GHz, and vice versa for 5.0GHz, with 4.7GHz as the middle ground. The system was able to deliver up to $20.25W$ RMS power for 4.7GHz, with $18.9W$ and $19.8W$ RMS power for 4.4GHz and 5.0GHz, which gives a deviation of 6.7% and 2.2% respectively. This number is quite low, indicating a good frequency response of the system, though a goal for future improvements should be to deliver above $20W$ across the f_0-band. Next, the main goal of the Doherty system is to improve its efficiency, and as dicussed in subsection 4.3, the general efficiency results of the system was quite good. The drain efficiency results of figure 64a are compiled into table 13.

	η(@4.4GHz)	η(@4.7GHz)	η(@5.0GHz)
0dB BO	44.6%	53.0%	54.2%
6dB BO	43.4%	44.4%	38.8%
10.5dB BO	31.3%	31.8%	25.0%

Table 13: Drain efficiency values

From the table a maximum deviation of 15.8% is found for 4.4GHz in 0dB BO, which is significant, but within reasonable limits. The system has above 44% efficiency at 0dB BO and above 38% at 6dB BO, which can be considered good and with reasonable bandwidth response. Last, the power gains of the system was 13.3dB for 4.4GHz and 4.7GHz, and 12.2dB for 5.0 GHz, giving a deviation of 8.3%. A power gain above 12dB across the f_0-band is can be considered good. In general, all the performance results of the system has improvement potential, and some methods of achieving better performance are discussed below, as well as methods of implementing the subsystems not finished in this project.

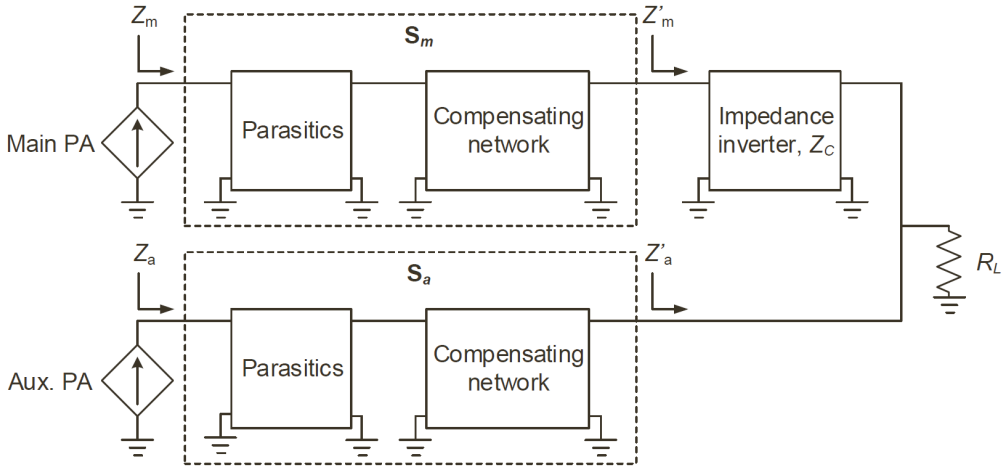


Figure 66: Illustration of compensating networks

5.2 Future works

5.2.1 Exploring methods of implementing the output network

In this project, the method of absorbing the parasites on the output to improve the bandwidth was explore, but only to some detail. The transistor parasites, with the necessary Bias networks, DC block capacitors and the Π-equivalent of the $\lambda/4$-line was optimized to give the best results. Still, the network was fairly simple, and the absorption of the parasite was only done by the optimizer. In [9], a number of techniques to include the parasites in the output network was explored. These are *Offset-lines*, *Compensation networks*, *Quasi-lumped parasitic absorption* among others. Common for these is that the extra added network are given for both the main PA and the aux PA, and that the impedance inverter is its own network. To illustrate this, the principle of the compensation network is given here, shown in figure 66

The S-parameters $\mathbf{S_m}$ and $\mathbf{S_a}$ is then principally given as

$$\mathbf{S_m} = \mathbf{S_a} = \begin{bmatrix} 0 & \pm 1 \\ \pm 1 & 0 \end{bmatrix} \tag{5.1}$$

Understanding the above principle is important in understanding what could have been improved for this project. For almost any real system, the parasites for the main PA and the aux PA is different, but in carefully designing the each

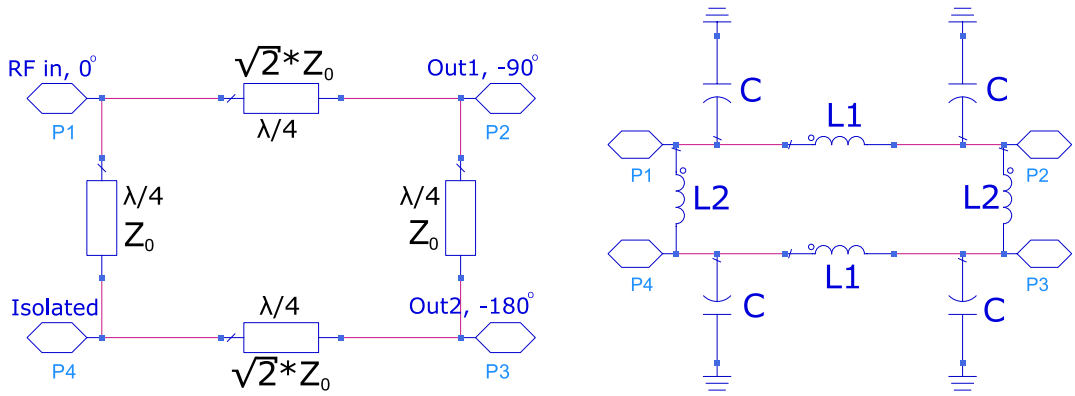
compensating network such that $\mathbf{S_m} = \mathbf{S_a}$, the currents and voltages propagating through the output network would have the exact same phase shift $\Delta\theta$. The phase shift value itself is not of significant importance, but that $\Delta\theta$ is equal for both the main PA and the aux PA is very important. If the signals from the current sources of figure 66 are perfectly 90° phase shifted, then the resulting signals out of the compensating networks would yield the same 90° phase shift. This in turn means that a perfect impedance inverter would shift the signal back 90°, combining the signals in-phase. In this project, the chosen optimization variable gave the CAD freedom to ignore the internal signal phase values, and only focus on getting the correct loadpull effect, as well as minimizing over-harmonics on I_{Load}. As a result, the combined Π-network, $C_{DCblock,main}$, $L_{DCfeed,main}$ and parasites becomes the complete impedance inverter, shifting the signal 90° while ignoring any phase shift on the aux PA. The combined $I_{Load} = i_{main,T} + I_{aux}$ is not added in-phase, meaning $I_{Load,max}$ does not become the potential I_{max} in saturation. One important potential improvement to the implemented system would therefore be to make the Π-network of figure 48 as a stand-alone impedance inverter, and then adjust $L_{DCfeed,main}$, $L_{DCfeed,aux}$, $C_{DCblock,main}$ and $C_{DCblock,aux}$ to make $\mathbf{S_m} = \mathbf{S_a}$, potentially adding more passive components. This would allow more current to load, and gives the designer more control of the signal propagation in the network, at the expense of adding components.

5.2.2 Splitter

One important part of the Doherty design that was not implemented with real components is the splitter on the Doherty input, given in figure 48 using an ideal 3-port S-parameter block. Originally in the design process, the idea was to let the phase difference and power split factor be variables for the optimizer to use. Although the mid-production results were quite good, adding extra variables added more complexity to the system, adding simulation and optimization time, and also made it more difficult to explain the overall system behaviour. The choice was therefore made to use as ideal Doherty splitter characteristics as possible, with $S_{21} = S_{31} = \sqrt{0.5} = 0.707$, and $\angle S_{31} = -90°$. Still, post-production tuning revealed that a $-80°$ phase difference allowed more delivered power to the load, which was because it allowed the currents to be added more in-phase, as discussed above.

For a practical realization of the splitter in MMIC, two common topologies exists, namely the *Wilkinson Power Divider* and *Quadrature Hybrid branch-line Coupler*. Both methods uses transmission lines to achieve the splitter effect, and in a MMIC

application both would require the use of lumped component equivalents. For the classical Doherty design, the main advantage of the Quadrature Coupler over the Wilkinson is that the output ports gets a 90° phase shift, as shown in figure 67a, while the Wilkinson splits the signal in-phase. For a practical implementation of the splitter, the quadrature coupler would have been chosen.



(a) Principle schematics (b) Lumped equivalent

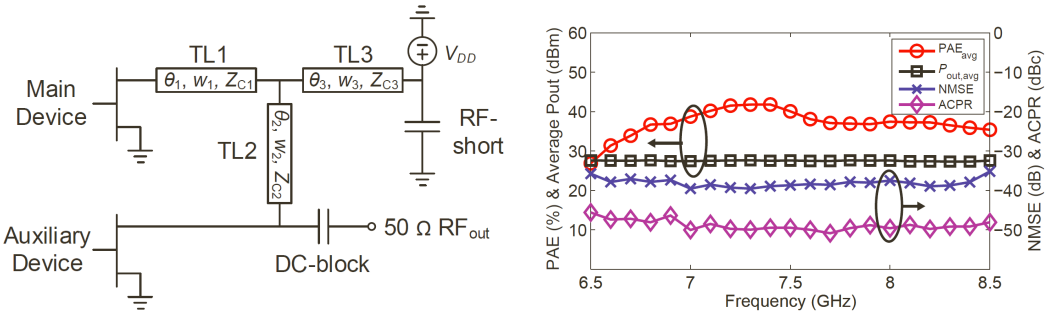
Figure 67: Quadrature Hybrid branch-line coupler illustration

The basic design of the quadrature coupler is shown in figure 67a, with the lumped component equivalent in figure 67b. With ideal transmission lines, the 4-port S-parameter matrix would yield $S_{21} = 0.707\angle -90°$ and $S_{31} = 0.707\angle -180°$, while all other $S_{ij} = 0$. For MMIC applications, the Π-equivalent could be used for each transmission line, and simplifying the circuit would yield the lumped component equivalent circuit. Still, in the finished network for this project a total of 7 inductors was used, and using the quadrature coupler on the input would ass 4 more, increasing the total area significantly. Still, such are the real life obstacle a designer meets in realizing a system.

5.2.3 Using transmission lines in MMIC anyway

An important assumption used through this project, discussed in detail in subsection 2.6 is that $\lambda/4$ transmission line impedance inverters has too large physical length and has too narrow bandwidth characteristics to be used in MMIC applications. In table 4 the theoretical Z-parameter deviation of a transmission line in the f_0-band was shown to be 1.84% in the band fringes, which one can argue is only modest, and within reasonable limits. The question then becomes whether transmission lines can be used as impedance inverters in MMIC anyway. Again, a good literature source to find the answer is [9], where a design using transmission

lines was implemented. The circuit for this design is given in figure 68a, with its frequency dependent results given in figure 68b. Here, C_{ds} was assumed as the only significant parasite from the transistors, and by adding capacitors to the outputs, the resulting Doherty equivalent circuit changes. In a quite elegant way, the designer started with a Π-equivalent of the circuit, and worked his way back to transmission lines, finding their electrical lengths (θ), width (w) and characteristic impedances mathematically.



(a) Design schematics (b) Design results

Figure 68: Design of a MMIC Doherty PA using transmission lines, [9]

To answer the question whether transmission lines can be used as impedance inverters, both the TL lengths and the results need to be examined. The lengths of TL1, TL2 and TL3 in figure 68a was $2800\mu m$, $840\mu m$ and $750\mu m$ respectively. But as their widths was relatively modest, the lines could be curled to maximize area usage, and the resulting MMIC size was $2.1mm \times 1.5mm$, well within reasonable limits. Examining the results shows very good frequency response for both average PAE and average P_{out}, indicating very good bandwidth properties. From this the conclusion can be made that transmission lines can indeed be used in Doherty MMIC PA as originally intended, but in doing so material parameters of the TL become more important, and a designer needs to always keep size restrictions in mind. For this project, exploring the potential use of lines could indeed yield better bandwidth results than what is obtained, contrary to the original premise. Also, in the future of communications, even higher frequencies will be explored, which in turn yields shorter wavelengths, and transmission lines may therefore become preferred over lumped components for high frequencies Doherty MMIC designs in the future.

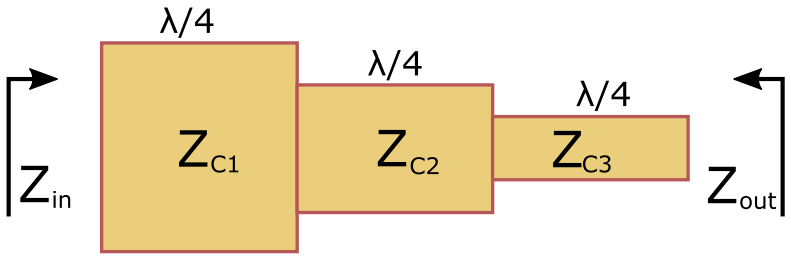


Figure 69: Simple illustration of impedance matching circuit

5.2.4 Matching to 50Ω

One aspect of PA design that has not been pursued in this project is matching to 50Ω on the output. It has become a industry standard to always match any RF design to 50Ω. This was omitted in this project as the focus was to make a wide-band design, and the resulting circuit was matched to 21Ω. This means that for any practical use of the circuit, the matching needs to be done off-chip. Matching to a given impedance can mainly be done in two ways, either by adding a resistive component, which would directly increase the seen impedance, or by adding reactive components, which would introduce frequency dependence. Using a $\lambda/4$-line with $Z_C = \sqrt{21 * 50}\Omega$ would do the trick for this design, but this would add a large ripple in the smith chart, indicating a strong frequency dependence. Another way is to use several $\lambda/4$ with a small difference between the Z_C-values, as shown in figure 69. Here, the characteristic impedances are given as $Z_{in} < Z_{C1} < Z_{C2} < Z_{C3} < Z_{out}$. Examining the behaviour in the smith chart gives more, but smaller ripples, indicating that the whole system has better frequency response compared to the single $\lambda/4$-line.

6 Conclusion

This thesis has attempted to give the reader a complete understanding of all aspects in designing a wide-band Doherty Power Amplifier in GaN MMIC centered at 4.7GHz and with behaviour optimized in the frequency band 4.4 - 5.0GHz. It is the authors ambitious intention that theory has been given for all aspects of designing a Doherty PA, and that most aspects of the practical design has a reference to the theory section. It has therefore been a focus of the thesis to give detailed theoretical explanations and deductions behind each PA design aspect, which aims to explain the physical behaviour of the implemented design. The material properties of GaN is compared to other semiconductor materials, indicating its advantage. The method of MMIC is explored in some detail, with practical design rules and restrictions given. Next a detailed explanation of transistor design is given with important transistor parameters needed to design an amplifier, as well as general amplifier parameters. The class-F amplifier is explored in some detail, as its behaviour has similarities to the implemented result. Last for the theory, the frequency response of transmission lines and correspondingly for the Doherty circuit is deducted using wave equations and Z-parameters. Characteristics of the theoretical Doherty design is given, and the practical method of using class-C amplifiers for implementation is given.

The practical design part of the project gave a practical use of Z-parameters to find MMIC equivalents of ideal passive components. Further, the Doherty Input Network, Output Network and Complete Network was each broken down to submodules and explained individually. The method of implementing the output network in small-signal analysis using the Z-parameters the Doherty equivalent circuit was attempted, with varying luck. The approach and results of the method was found to not been have been used to its potential. Setting R_L as fixed and decreasing the degree of optimizer freedom would likely yield better results. Also more care should be given in not only making the numerical deviation from the ideal Doherty Z-parameter small, but also making the individual Z-parameters behave similar to the ideal case. Last, a large-signal analysis was performed on the design to give its performance vs voltage and power drive level. It was shown that due to uncareful choice of optimization goals, a large number over-harmonics across the main and aux PA currents, which was added in anti-phase. The fundamental components of the combined currents also contained a 108.5° phase difference, which caused the load current not to give a optimal amplitude. The finished Doherty design was able to deliver above 18.9W RMS power across the frequency range, with a peak power of 20.25W at 4.7GHz. Efficiencies of the design yielded a mean value of 50.6% in 0dB backoff across the f_0-band, and a mean value of 42.2%

for 6dB backoff. The system also produced a power gain of 12.2dB - 13.3dB across the f_0-band. A simple layout proposal is given given using transmission lines as interconnects. The area usage became $4.92mm^2$ for the layout with the active and passive components taking up $1.33mm^2$ of these, excluding the interconnects.

From the results of the implemented design, some proposals of improvements are given, mainly exploring the concept of Compensation Networks, as this ideally give the designer more control of the parasite behaviour and also more control of the delays and phase changes through both the main PA and aux PA sub-networks. Implementing a Doherty using this methodology should therefore remove any anti-phase current behaviour, which would optimize load current amplitude and subsequently allow for increased output power. Also, The hypothesis that transmission lines are too long in physical size and with too narrow frequency response are challenged with reference to a practical Doherty MMIC design. Here it was shown that a almost perfectly flat frequency response of P_{out}, and a PAE above 30% was obtained across a 2GHz frequency range. The design used transmission line with a slightly different topology compared to the classical Doherty circuit, and the total MMIC are usage was $2.1mm \times 1.5mm$, which is within reasonable limits for a MMIC.

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