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Bulk fabrication and properties of solar grade silicon microwires

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We demonstrate a substrate-free novel route for fabrication of solar grade silicon microwires for photovoltaic applications. The microwires are fabricated from low purity starting material via a bulk molten-core fibre drawing method. *In-situ* segregation of impurities during the directional solidification of the fibres yields solar grade silicon cores (microwires) where the concentration of electrically detrimental transition metals has been reduced between one and two orders of magnitude. The microwires show bulk minority carrier diffusion lengths measuring ~40 μ m, and mobilities comparable to those of single-crystal silicon. Microwires passivated with amorphous silicon yield diffusion lengths comparable to those in the bulk. © 2014 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. [http://dx.doi.org/10.1063/1.4902140]

In recent years, solar power has experienced increasing attention due to the negative environmental impact of fossil fuel use and political resistance against nuclear power. Most solar modules today are made from crystalline silicon (c-Si), due to the abundance of the material and existing expertise, but various novel technologies for future solar cells are being investigated, including thin films,¹ novel materials,² multi-junction cells,³ intermediate bandgap cells,⁴ and radial junction solar cells.^{5–10}

Silicon radial junction solar designs offer several advantages over conventional silicon wafer designs; they are more material efficient, they promote effective light trapping, and they allow more efficient carrier collection due to a decoupling of the light absorption and carrier collection directions. Single or multi-wire designs have been realized using a range of techniques, with deep reactive ion etching (DRIE) of $c-Si^{8,11,12}$ and vapour liquid solid (VLS) growth on c-Si substrates^{9,10,13} being dominant. These approaches have demonstrated efficiencies of ~10% and significant enhancements in light trapping per unit of silicon.¹⁴ New approaches have recently been reported where silicon fibres are independently fabricated and subsequently assembled into a substrate-free cell. He *et al.*¹⁵ recently showed a 0.5% conversion efficiency in a silicon fibre produced through high pressure chemical vapour deposition (HPCVD), followed by our group that produced a 3.5% efficiency cell from a single silicon core silica-sheath fibre drawn using the molten core fibre drawing technique.¹⁶ This cell was made from a vertically aligned fibre segment and the paper suggests a design that utilizes the glass as a reflector. In the latter paper, it was suggested that the efficiency was limited by device processing rather than the quality of the silicon, implying that large gains in efficiency should be possible.

Here, we report on the properties of silicon microwires produced through the molten core fibre pulling method^{17,18} and their potential for use in radial junction solar cells. The microwires have

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been analysed with a broad range of techniques, with a focus on purity and electronic characterisation. The production method, where the silicon is crystallized directionally in a small diameter glass capillary as the fibre is drawn, results in an *in-situ* segregation-based purification. The increased purity results in long minority carrier diffusion lengths and mobilities comparable to those observed in high purity silicon wafers.

Silicon core glass fibres were fabricated using the molten core fibre drawing technique where a solid 99.98% pure silicon rod was placed inside a CaO (99.9% Sigma Aldrich) coated silica tube (preform) and drawn into fibres on a Heathway draw tower at temperatures measuring 1950 °C with a feed rate of 3 mm min⁻¹ and pull rate of 2.7 m min⁻¹. The resulting fibres have silicon cores (microwires) with diameters of 50-200 micrometers and a silicon to silica ratio of 1:100. An as-drawn fibre can be seen in Figure 1(b) and a microwire, stripped of the cladding using 40% HF acid in water can be seen in Figure 1(c). The microwires have mm length grains,¹⁶ making long segments monocrystalline across their cross section. The CaO was used as an interface modifier to relieve stress between the silicon and the silica and to reduce oxygen in-diffusion during production.^{16,18}

During fabrication, impurities in the silicon undergo a segregation process based on differing solubilities in the liquid and solid phases. This segregation causes changes in the concentration of impurities based on their respective effective segregation coefficient k_{eff} , defined as the ratio between the impurity concentration after and before solidification (C_f/C_i) . Most impurities have $k_{\text{eff}} \ll 1$ for the very low solidification velocities used for commercial purification of silicon ingots, but it has been demonstrated¹⁹ that significant segregation occurs in micro-scaled silicon samples at solidification velocities measuring ≈ 4.5 m s⁻¹. This velocity was calculated using the continuous growth segregation model²⁰ that was shown to be the most accurate model for describing segregation at high solidification velocities.¹⁹ With the solidification velocity for our fibres assumed to be much lower than 4.5 m s⁻¹ (similar to that of the drawing speed of 0.045 m s⁻¹), a significant segregation effect is predicted even at higher drawing rates.

The starting silicon material, the calcium oxide, and the silicon microwires were analysed with inductively coupled plasma mass spectroscopy (ICPMS) in order to investigate changes in the impurity concentrations as a result of the fabrication process. Oxygen concentrations of the starting material and microwires by secondary ion mass spectroscopy have previously been reported.¹⁶ For ICPMS, the silica portion of several cm of fibres was removed by etching in aqueous 40% HF. The starting material and microwires were dissolved in a mixture of ultra pure nitric acid and supra



FIG. 1. Silicon-core fibres: (a) schematic illustration of the structure, (b) a photomicrograph of an as-drawn fibre, and (c) a SEM micrograph of a silicon microwire after the cladding has been stripped using 40% hydrofluoric (HF) in water.

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FIG. 2. ICPMS determined purity of the source materials compared to the microwires with literature values for oxygen.¹⁶

Element

pure grade 40% aqueous HF (Romil) while the CaO sample was dissolved in ultra pure nitric acid before analysis in an Element 2 high resolution ICPMS from Thermo Electronics. Microwires were cleaned with 0.1 M ultra pure nitric acid immediately before dissolution to remove any impurities accumulated on the surface between the HF etch and the dissolution. The starting silicon was not cleaned prior to dissolution as it was not treated prior to the fibre-drawing process.

From Figure 2 it can be seen that, as a result of the fabrication process, aluminium, iron, and titanium are reduced by between one and two orders of magnitude ($k_{eff,Al} = 0.11$, $k_{eff,Fe} = 0.0088$, and $k_{eff,Ti} < 0.025$), the magnesium and oxygen concentrations are almost unchanged ($k_{eff,Mg} = 0.71$ and $k_{eff,O} = 1.61$), while the concentration of calcium is increased approximately four times ($k_{eff,Ca} = 4.3$). The impurity contribution of the CaO (not shown) was found to be negligible due to the high purity of the CaO combined with a low volume ratio (1:100) compared with the silicon. The impurity level of the titanium is at the detection limit in the ICPMS, and thus represents the maximum possible concentration. The k_{eff} values observed for the fibre drawing were similar to those reported for flakes with 100 times the cooling rate,¹⁹ suggesting that solidification speed is not the limiting factor in the purification.

Aluminium contacts were deposited onto microwires using a shadow mask and a sputter coater for resistivity measurements, and the samples were measured using a four point probe, yielding values of $0.3 - 0.9 \Omega$ cm. For Hall voltage measurements, a 6 contact Hall bar was patterned onto a microwire, as shown schematically in Figure 3(a) using photo-lithography, and the contacts were subsequently formed by sputter deposition of aluminium. As shown by Storm *et al.*,²¹ the Hall voltage across a wire geometry can be approximated to depend on the magnetic field according to Eq. (1), and the carrier density can be obtained from the slope of the Hall voltage plotted against the magnetic field

$$V_{\rm H} = \frac{I \cdot d}{p \cdot e \cdot A_{\rm wire}} B. \tag{1}$$

Here, *I* is the constant current through the microwire, *p* is the majority carrier density, *d* is the spacing between the contacts measuring the Hall voltage $V_{\rm H}$ (Figure 3(a)), *e* is the elementary charge, $A_{\rm wire}$ is the cross-sectional area of the microwire, and *B* is the strength of the magnetic field.

By applying a 0.5 mA current through contact 5-6 (I_{56}), the Hall voltage $V_{\rm H}$ shown in Figure 3(b) was obtained by measuring the voltages across the contacts 1-2 and 3-4 (V_{12} and V_{34} , respectively) while varying the *B*-field between ±0.5 T. The microwires were found to be p-type with a carrier density $p = 2.15 \times 10^{16}$ cm⁻³, determined by averaging the slope of the Hall voltage between the contacts 1-2 and 3-4 (Figure 3(b)) and solving Eq. (1) for *p*. By combining the resistivity with the carrier density, the hole mobility, $\mu_{\rm h}$, was found to be 385 cm² V⁻¹ s⁻¹, with a corresponding hole diffusivity $D_{\rm h} = 9.72$ cm² s⁻¹. Assuming the ratio between the electron and hole



FIG. 3. A schematic of the Hall bar pattern deposited on to a microwire (a) with the Hall voltage (b) for the contact pairs 1-2 and 3-4 when passing 0.5 mA through a 173 μ m diameter microwire with $\rho = 0.76 \Omega$ cm and $d = 70 \mu$ m when varying the magnetic field.

mobilities to be the same as that for bulk silicon results in an electron mobility $\mu_e = 915 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with a corresponding diffusivity $D_e = 23.1 \text{ cm}^2 \text{ s}^{-1}$.

In order to estimate the minority carrier lifetime and diffusion length, the microwires were measured with the electron beam induced current (EBIC) measurement technique and analysed following the method of Chan *et al.*³¹ The microwires were contacted with a titanium Schottky contact at one end, and an aluminium ohmic contact at the other. With zero applied bias across the two contacts, an electron beam was then scanned across the sample generating minority carriers on impact, and the current through the Schottky junction was measured with respect to the location of the electron beam to obtain a current collection map (Figure 4).

The current collected by the junction drops off with the distance from the junction, and the resulting current profile follows the relation

$$I \propto x^{\alpha} e^{-x/L_{\rm b}},\tag{2}$$

where x is the distance from the Schottky contact, L_b is the bulk minority carrier diffusion length, and α is a fitting parameter related to the surface recombination velocity.³¹ The equation is generally



FIG. 4. A schematic illustration of an EBIC line scan of a silicon microwire contacted with one Schottky and one ohmic contact (a) together with the current profiles and their respective fits for a passivated (b) and non passivated (c) sample.

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considered to be valid when $x \gg L_b$ or in the region where the semi log plot of $\ln(I/x^{\alpha})$ versus x is linear.

The surface recombination velocity v is given by equation (8) in the work of Chan *et al.*,³¹ and can, according to Allen *et al.*,²⁸ be used to obtain the effective minority carrier lifetime τ_{eff} by solving the continuity equation for the cylindrically symmetric carrier concentration profile. The resulting τ_{eff} is then given as

$$\frac{1}{\tau_{\rm eff}} = \frac{1}{\tau_{\rm b}} + \frac{\beta^2 D}{r^2},\tag{3}$$

where β is given as the solution to the equation

$$\beta J_1(\beta) - \frac{vr}{D} J_0(\beta) = 0. \tag{4}$$

In the above relations, $\tau_{\rm b} = L_{\rm b}^2/D_{\rm e}$ is the bulk minority carrier lifetime, *r* is the radius of the microwire, and $J_{0,1}$ are the zero and first order Bessel functions, respectively. The effective minority carrier diffusion length can thus be found by combining the effective lifetime with the electron diffusivity ($D_{\rm e}$) found from the Hall measurements through the relation $L_{\rm eff} = \sqrt{D_{\rm e}\tau_{\rm eff}}$.

EBIC current profiles were collected from the top of the central region of microwires with diameters $(2r) \approx 100 \ \mu m$, both for a non-passivated sample and a sample passivated with 10 nm amorphous intrinsic silicon deposited using plasma enhanced chemical vapour deposition (PECVD). The data were subsequently fitted to (2) using the method of least squares in order to obtain α and L_b . For a passivated sample, L_b was found to be 43 μm and α to be -0.51, and L_b was subsequently held constant in the fitting of the data from the non-passivated sample obtaining $\alpha = -1.21$. The resultant values can be found in Table I; the passivated surface recombination velocity is much lower than that for the non-passivated surface, leading to a $\sim 2\times$ increase in the effective minority carrier diffusion length. Some selected values from wires made using VLS-growth and HPCVD have been added in Table I for comparison.

The molten core fibre drawing technique, used in this work to produce bulk lengths of silicon core glass sheath fibres, has shown to cause an *in-situ* purification of the silicon material used in the fabrication, reducing the concentration of several impurities as a part of the fabrication process. The purification is believed to be caused by segregation of the impurities to the microwire surface during the crystallization of the silicon together with the slag-refining properties of the CaO interface layer between the silicon and the silica. Although calcium has been observed to increase in concentration, the impurities most detrimental for minority carrier lifetimes have been reduced by more than an order of magnitude. As 2.4 mg (~10 cm) of fibre was used to get sufficient signal in the ICPMS, it is inevitable, despite the high crystallinity reported for these microwires, that impurities located at grain boundaries have been included in the analysis. The in-grain impurity levels of the silicon microwires are thus expected to be lower than the combined impurity concentrations given by

TABLE I. Electrical parameters for a non passivated sample and a sample passivated with 10 nm amorphous intrinsic silicon together with selected values for VLS-grown wires and HPCVD-made wires taken from the literature. Note that the mobility values cannot be compared directly as these have a strong dependence on the doping concentration in the sample.

		Non		
	Passivated	passivated	VLS	HPCVD
$\mu_{\rm e} [{\rm cm}^2 {\rm V}^{-1} {\rm s}^{-1}]$	915	915	370, ²² 95, ²³ 28 ²⁴	$30 (n = 8 \times 10^{15})^{15}$
$\mu_{\rm h} [{\rm cm}^2 {\rm V}^{-1} {\rm s}^{-1}]$	385	385	130, ²² 3, ²⁵ 560 ²⁶	$2 (p = 1 \times 10^{17})^{15}$
$v [{\rm cm}{\rm s}^{-1}]$	502	9154	$\ll 70,^{10}450-600,^{10}20,^{27}(\gg 10^5),^{28}>300,^{29}$	-
$\tau_{\rm b}$ [ns]	796	796	~2 ²⁹	-
$\tau_{\rm eff}$ [ns]	701	193	~15, ¹³ ~0.1 ³⁰	-
$L_{\rm b}$ [μ m]	43	43	-	-
$L_{\rm eff}$ [µm]	40	24	$\gg 30,^{10} 5 - 10,^{10} 2 - 4,^{13} 0.08,^{28} 0.5^{29}$	≤0.1 ¹⁵
2 <i>r</i> [µm]	118	93	1.2-1.8, ¹⁰ 0.1-0.2, ²⁷ 0.03-0.1, ²⁸ ~0.1 ²⁹	5-15 ¹⁵

the ICPMS data, and this is strongly supported by the large bulk minority carrier diffusion length ($\approx 40 \ \mu m$). The increase in the measured calcium concentration and unchanged magnesium concentration in the microwires are believed to be caused by fluorides remaining on the microwire surface that the diluted nitric acid clean prior to ICPMS analysis failed to dissolve.

Unless there is substantial undercooling, the solidification velocity in the microwires is comparable to the drawing rate of 0.045 m s⁻¹. Inserting this velocity together with the respective equilibrium segregation coefficients^{32,33} into the continuous growth segregation model²⁰ results in modelled $k_{\rm eff}$ values equal 0.03, 0.003, and 0.0033 for aluminium, iron, and titanium, respectively. Comparing these to the experimentally determined values 0.11, 0.0088, and 0.025 for the same elements, one finds an approximately one order of magnitude difference, likely caused by impurities included from the few remaining interior grain boundaries. The modelled effective segregation coefficients can thus be used as an estimate for the true in-grain purity of the microwires, which results in a concentration of 1.3×10^{17} cm⁻³, 9.8×10^{15} cm⁻³, and 9.3×10^{14} cm⁻³ for aluminium, iron, and titanium, respectively. These numbers are in better agreement with the measured minority carrier diffusion length and as most radial junction solar cells typically will consist of $\lesssim 500 \ \mu m$ segments containing on average one grain only,¹⁶ these numbers will represent an average solar cell purity. Performing the same calculation for oxygen results in an estimated $k_{\rm eff,O} = 1.25$ $(C_{\rm f} = 2.1 \times 10^{17} \,{\rm cm}^{-3})^{16}$ being slightly lower than the experimentally observed 1.61, likely caused by in-diffusion of oxygen into the starting material during pre-heating of the preform. Segregation coefficients for magnesium and calcium were not modelled due to their anticipated presence as fluorides on the sample surface.

A bulk minority carrier diffusion length of ~40 μ m is amongst the longest ever measured in silicon wires,^{15,28,29} comparable to those measured by Kelzenberg *et al.*, in VLS-grown nanowires,¹⁰ despite the low purity of our starting material. The non-passivated silicon surface is found to have a surface recombination velocity of ~9000 cm s⁻¹ and passivation with amorphous intrinsic silicon reduces this to ~500 cm s⁻¹, resulting in an effective minority carrier diffusion length comparable to that of the bulk. The values for the surface recombination velocities are similar to those earlier reported for free silicon surfaces³⁴ and a-i-Si passivated silicon^{10,27,29} indicating a good fit of the EBIC-profiles. Due to a high sensitivity of the fitting procedure and difficulties in detecting the noise levels in the EBIC profiles, an uncertainty of $\leq 20\%$ in α and L_b was estimated from the sensitivity of varying the current region where Eq. (2) was fitted.

The hole mobility, μ_h , in the microwires, derived from the measured resistivity and carrier density, is 385 cm² V⁻¹ s⁻¹. This value is comparable to that for single crystal silicon wafers, indicating a negligible increase in surface scattering as a result of the increase in surface to bulk ratio in the microwire geometry. Surface scattering has been shown though simulations by Ramayya *et al.*³⁵ to become the dominant scattering event only when the microwire diameter becomes very small (~nm), supporting the indication that the microwires described here are largely free of this effect. More interestingly, the mobility reported for our samples is significantly larger than that reported for microwires created with HPCVD.¹⁵ With doping concentration in the HPCVD wires reported to be comparable to that of the microwires reported here, hence similar ionized impurity scattering, the \approx 30 times larger mobility in our samples demonstrates an advantage of the molten core fibre pulling technique over HPCVD in production of microwires for PV-applications.

In conclusion, we have shown that silicon microwires with a quality suitable for high efficiency PV applications can be fabricated from low purity UMG (99.98%) silicon, primarily due to an *in-situ* segregation based purification of the material during production. The p-type microwires in this study have a hole mobility of 385 cm² V⁻¹ s⁻¹, comparable to that measured in single crystal wafers. The effective minority carrier diffusion length of the microwires has been shown to be $\approx 40 \ \mu$ m if the sample is passivated with amorphous intrinsic silicon. The high effective diffusion length and carrier mobility would allow microwires to successfully be used in efficient radial junction solar cell designs.

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