NTNU – Trondheim
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Self-Poling and Ageing in PZT Thin Films With Interdigitated Electrodes

Work done at Laboratoire de Céramique (LC),
EPFL

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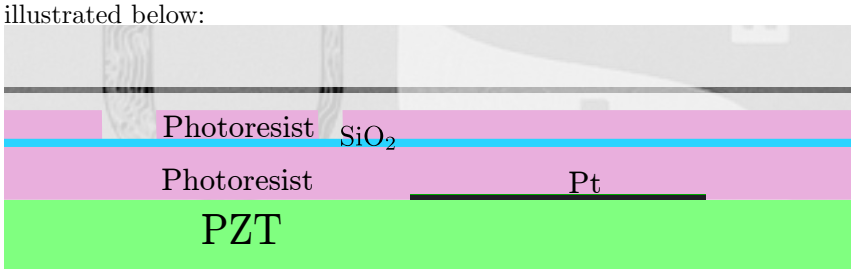
Cover Image:
The cover image is a micrograph taken during fabrication. The LC logo is made of Pt sputtered onto the PZT. A layer of photoresist and SiO_2 has been deposited on top of the PZT and Pt. The SiO_2 has then crumpled, giving the ripples seen in the NTNU logo. A second layer of photoresist covers the SiO_2, but this layer has been exposed and developed to give the outline of the NTNU logo. An IDE structure can be seen at the bottom of the image, and another can be seen at the top. The stack of different layers is illustrated below:



Abstract

This work details advances in thin-film lead zirconate titanate (PZT) devices with interdigitated electrodes (IDEs). They are interesting for energy harvesting applications, as they can provide small amounts of electrical energy to devices such as wireless sensors. A simple equation relating the electric field to the sample geometry of IDEs was derived in this work, and PV hysteresis loops of fabricated films were used to verify the validity of the numerical finding. A fabrication route was developed for partially covering samples with SiO_2 and self-poling was observed in these samples by measuring the piezoelectric coefficient descriptive of IDEs, e_{IDE}. The self-poling observed was limited in magnitude and the origin is still not clear. Slanted PV loops were observed when measuring as-fabricated samples and the slanting was compared to the effect of an interface layer, modelled as described by A.K. Tagantsev and G. Gerra. The model gave inconsistent values for the thickness of the interface layer when comparing samples with varying electrode spacing, and the slanting is therefore thought to have other causes. The time evolution of PV loops has been observed and characterised, and possible causes are discussed. The time evolution of individual samples was found to fit well with the model by M. Grossmann et al. for charge injection across a passive layer at the electrode interface, but this model does not agree with the observed dependence on electrode spacing. Charge injection across passive regions at the grain boundaries is suggested as an alternative that would agree with the observed dependence on electrode spacing. The models by A.K. Tagantsev and M.Grossmann were made to describe devices with parallel plate electrodes, and some inconsistency with the experimental results is to be expected.

Sammendrag

Denne oppgaven beskriver fremskritt i strukterer av tynnfilm blyzirkonattitanat (PZT) med interdigitaserte elektroder (IDE). Disse strukturene er interessante for energihøsting, fordi de kan gi små mengder elektrisk energi til for eksempel trådløse sensorer. Teoretisk arbeid har resultert i en enkel ligning som kobler det elektriske feltet i prøven til prøvens geometri. Hysterese (PV) kurver fra fabrikerte prøver ble brukt til å verifisere disse funnene. En fabrikasjonsrute ble utviklet for å dekke prøver delvis med SiO_2 og, selv-polarisering ble observert i disse prøvene ved å måle den piezoelektriske responsen. Selv-polariseringen som ble observert var begrenset i størrelse, og opphavet til denne effekten har ikke blitt identifisert. Framoverlente kurver ble observert når prøver ble målt rett etter fabrikasjon, og helningen i disse kurvene ble sammenlignet med effekten av et grensesjikt, modelert som beskrevet av A.K. Tagantsev og G. Gerra. Modellen ga inkonsistente verdier for tykkelsen av grenssjiktet da prøver med ulik geometri ble sammnlignet, og helningen i kurven antas derfor å ha et annet opphav. Aldring av prøver etter poling ble observert og karakterisert, og mulige årsaker er diskutert i rapporten. Aldring av individuelle målinger passer godt til en modell av M. Grossmann et al. for ladningsforflyttelse over passivsjikt ved elektrodene, men denne modellen stemmer ikke overens med den observerte avhengigheten av avstanden mellom elektrodene. Passivsjikt ved korngrenser er foreslått som et alternativ som vil ha riktig skalering. Modellene av A.K. Tagantsev and M.Grossmann ble laget for å beskrive prøver med paralelle elektroder og noe avvik må derfor forventes.

Preface

Circumstances have led me to write my semester project and now master's thesis as an exchange student at EPFL. My semester project[1] was closely related to the work by Robin Nigon as part of his PhD thesis, and this allowed me to learn how to measure ferroelectrics as well as the pros and cons of IDE structures. I must thank Prof. Paul Muralt and Robin Nigon for the warm welcome I received.

This master's thesis must be understood in the context that it builds on previous research on IDE structures carried out by Nachiappan Chidambaram and more recently Robin Nigon. My original proposal for this thesis was to partially cover samples with SiO_2, and then annealing them in reducing atmosphere in an effort to introduce self-poling[1]. I knew that Robin Nigon had previously studied the effect of using asymmetric electrode materials, but had not found self-poling in such samples. My proposal was therefore in line with his PhD thesis, in that it studies the effect of introducing asymmetry into IDE structures. While working on this thesis, I discussed my progress and results frequently with Robin Nigon, and although this thesis details my work and the theories presented are my own, I would not have been able to make this much progress without the support of R. Nigon.

This thesis, like so many other things in life, has gone through several phases. First there was about three months of fabrication, followed by two months of measurements, and one month of writing. It was during fabrication that I discovered how Gevorgian's model could be simplified, so that I could write a simple expression for the effective field in the IDE structure. This finding builds on previous work by Nachiappan Chidambaram and is completely in line with the PhD thesis of Robin Nigon. R. Nigon has done simulations in `Comsol` that support this expression, and is seeking to publish our findings in Applied Physics Letters.

Similarly, the work done on self-poling in this thesis was carried out as an independent work, but Robin Nigon will continue this work where I leave it when I go back to Norway. This is because it fits nicely into his PhD thesis.

I did the first ageing measurement as part of my semester project last semester[1], after I noticed significant ageing in the samples. Intrigued by this measurement, the ageing behaviour of many old samples were characterised by Robin Nigon and myself during the fabrication phase of this project. The results from this are not presented here but a comparison of the ageing characteristics of tetragonal and MPB PZT with IDEs was presented by Robin Nigon at the 2015 Joint ISAF/ISIF/PFM Conference. A paper has been published in the proceeding with myself as a co-author[2]. However, the cause of ageing was not discussed there, and it is only here in my master's thesis that ageing measurements are compared to different models and possible causes

[1] A short note on the original proposal is included in Appendix E.

are evaluated in a systematic manner. It is too early to publish the results of these comparisons, but if epitaxial films were made and evaluated in terms of ageing, it is likely that this could lead to a publication. Despite this, it is not certain if Robin Nigon will have the time to continue working on this topic, as it is not so closely tied to the topic of his PhD thesis.

Thanks to the group for including me in group meetings, and special thanks to Prof. Paul Muralt and Robin Nigon for listening to my ideas, accepting my proposals, and discussing my theories. I could not have written this thesis without you.

Trygve Magnus Ræder,
August 9, 2015

Contents

List of Abbreviations

AFM	Atomic force microscopy
DMD	Digital micromirror device
ICDD	International Centre for Diffraction Data
IDE	Interdigitated electrodes
LOR	Lift-off resist
MLA	Maskless aligner
MPB	Morphotropic phase boundary
PFM	Piezoresponse force microscopy
PPE	Parallel plate electrode
PV loop	Polarisation-voltage hysteresis loop
PZT	$PbZr_xTi_{i-x}O_3$
RF	Radio Frequency
sccm	Standard cubic centimetres per minute, a unit of gas flow.
XRD	X-ray diffractometry

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Chapter 1

Introduction

Miniature piezoelectric devices can be used to harvest electrical energy from vibrations in order to provide power for small sensors or other electrical devices[3, 4]. Such devices have become more feasible as recent developments in the semiconductor industry have reduced the power consumption of devices with logic capabilities. However, miniature energy harvesters must still overcome the forward bias of a rectifying bridge. In piezoelectric materials, the output voltage is proportional to the electrode spacing, and in traditional thin film devices, this means that the voltage is proportional to the thickness of the piezoelectric layer. Such a device is shown in Figure 1.1(a). Interdigitated electrodes (IDE), as seen in 1.1(b), can be used to increase the output voltage, and such devices have been studied in [5, 6, 7, 8]. These devices have favourable characteristics for energy harvesting, but the electric field and its dependence on the electrode spacing is not well understood. The design also has the advantage that multiple samples with different geometries (electrode spacings) can be made on the same wafer, in order to easily analyse dependence on the electrode spacing in the observed properties. For parallel plate (PPE) devices, a similar analysis generally requires the fabrication of multiple films (wafers), and is therefore much more labour intensive.

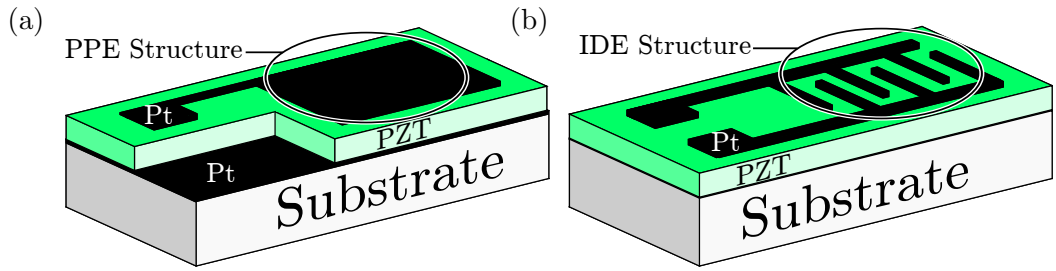


Figure 1.1: (a) Schematic drawing of a traditional device with a parallel plate electrode (PPE) structure, and such structures have been extensively studied[9]. (b) Drawing of a sample with an IDE structure. Figure adapted from [1].

Piezoelectric devices based on ferroelectric materials also require poling. Poling is the process where the domains in a ferroelectric material are oriented, so that that the device as a whole produces a non-zero piezoelectric effect. This generally requires applying a high voltage at a high temperature for an extended period of time. Self-poling is a phenomenon observed in some devices where the fabrication process leads to a device in which the ferroelectric domains are already partially oriented along a preferred direction. The design and fabrication can then be simplified as such devices may not need to be poled. Self-poling has previously only been observed along the growth direction of thin films in parallel plate devices, and symmetry dictates that self-poling along the growth direction will give no net piezoelectric effect in IDE structures.

Such structures are therefore suited for studying possible causes of self-poling not related to asymmetry along the growth direction.

1.1 Aim of the Work

The main goals of this work was to introduce self-poling in devices with IDEs, and to increase the understanding of ferroelectric devices with interdigitated electrodes in general. A specific aim was to find a fabrication route to produce samples with a partial SiO_2 cover, in order to introduce self-poling in samples with IDE structures. An example of such a structure is shown in Figure 1.2.

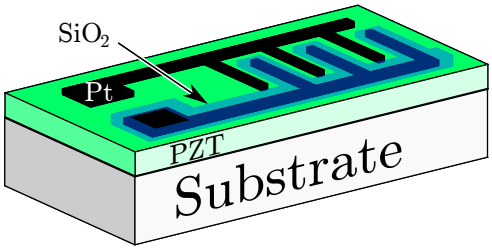


Figure 1.2: Schematic drawing of a sample where the IDE structure has been partially covered with SiO_2.

To increase the understanding of samples with IDEs, theoretical work was done to simplify the model by Gevorgian et al. for capacitance of IDE structures[10], so that a simple expression for the electrical field as a function of the geometry and applied voltage can be obtained. Ferroelectric measurements of the fabricated samples were then used to verify this relation.

Another specific aim was to characterise the time evolution of the ferroelectric hysteresis loops. This was done so that the observed time evolution could be fitted to different models, and the origin of the phenomenon could be identified.

1.2 Thesis Overview

This thesis includes the theory behind the piezoelectric effect, and how it can be used in energy harvesters. A description the piezoelectric and ferroelectric measurement techniques used is also included. This is done because the piezoelectric measurements are non-standard, and because readers not familiar with ferroelectric measurements should be introduced to the important features of the hysteresis loops prior to the results. The process flow for fabrication of samples is reproduced in detail, as self-poling can be very sensitive to variations in process flow.

Several appendices are included after the Conclusions chapter. Appendix A and B describe the tests undertaken to develop the fabrication procedure presented in Chapter 3. Appendix C and D are excerpts from [1] detailing parasitic capacitance and how the electrode spacing of the samples is measured. These are reproduced here as they are highly relevant to this work. Finally, Appendix E describes the original proposal for this thesis

Chapter 2

Theory

This chapter is meant to provide the necessary theory in order to interpret the results presented later. Some effects described here, most notably ageing, is studied in this thesis because was found to be a prominent feature when measuring PV loops, and a description of PV loops follows in Section 3.1. As the aim of this work is the understanding of piezoelectric devices, this chapter starts with a description of the Piezoelectric effect.

2.1 Piezoelectric Effect

The piezoelectric effect relates mechanical force or deformation, with electric field or charge displacement. The effect can therefore be seen in four possible regimes, shown in Equations 2.1-2.4[11].

Strain-Charge regime:

$$\xi = sT + dE \tag{2.1a}$$
$$D = dT + \varepsilon E \tag{2.1b}$$

Strain-Field regime:

$$\xi = sT + gD \tag{2.3a}$$
$$E = -gT + \beta D \tag{2.3b}$$

Stress-Charge regime:

$$T = c\xi - eE \tag{2.2a}$$
$$D = e\xi + \varepsilon E \tag{2.2b}$$

Stress-Field regime:

$$T = c\xi - hD \tag{2.4a}$$
$$E = -h\xi + \beta D \tag{2.4b}$$

Where ξ is the strain, T is the stress, E is the electric field, D is the displacement field, s is the elastic compliance, c is the elastic stiffness, ε is the dielectric constant and $\beta = 1/\varepsilon$. d, e, g and h are the piezoelectric coefficients. Different regimes are used in different applications, where for example the strain-field regime is used to describe precision actuators for the movement of an AFM tip. Furthermore, each regime consists of two equations, #a and #b. #a describes the converse piezoelectric effect, where a voltage or charge is applied to produce stress or strains, while #b describes the direct piezoelectric effect where an applied force or deformation produces electric field or charge.

Equations b of the stress-charge and stress-field regimes are most relevant for sensor and energy harvesting applications. During operation of a device, Equation 2.4b with the coefficient h, will describe the open circuit voltage, and Equation 2.2b with the coefficient e will describe short circuit current. The product eh (with units J/m) is therefore often used as a figure of merit of

such a device, estimating the power output of a given deformation[5]. However, it should be noted that the actual power delivered will be dependent on the load, and will be lower than what is expected from the figure of merit alone.

Equation 2.2b, used for short circuit mode of an energy harvester or sensor, is the most important for this work, as this type of measurement is used to characterise the samples. The equation is therefore reproduced below in matrix form for ceramic material with a random orientation of grains poled along the 3 direction[12]:

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \xi_1 \\ \xi_2 \\ \xi_3 \\ \xi_4 \\ \xi_5 \\ \xi_6 \end{bmatrix} + \begin{bmatrix} \varepsilon_{11} & 0 & 0 \\ 0 & \varepsilon_{11} & 0 \\ 0 & 0 & \varepsilon_{33} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{2.5}$$

In converse mode, e_{33} and e_{31} describe the charge generated from deformation in the cardinal directions, while e_{15} describes charge generated by a shear force perpendicular to the polarisation. e_{33} and e_{31} in direct mode are illustrated Figure 2.1.

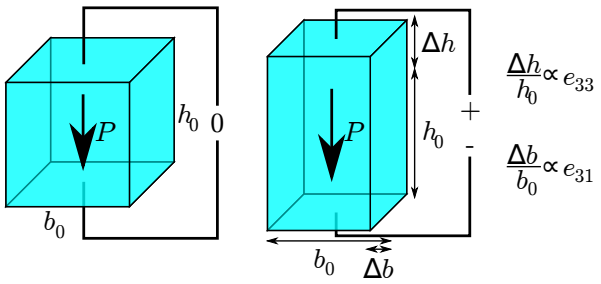


Figure 2.1: Change in height and width of a piezoelectric material when a voltage is applied. Figure adapted from [1].

The piezoelectric effect is caused by a distortion or creation of a dipole as the unit cell is deformed, and can therefore not exist in centrosymmetric unit cells, or the class 432.[1] Of the remaining 20 crystal classes, all have non-zero piezoelectric coefficients[13]. 10 of these crystal classes have a polar axis and are pyroelectric, and some materials in these crystal classes will also be ferroelectric, as seen in Figure 2.2.[12]

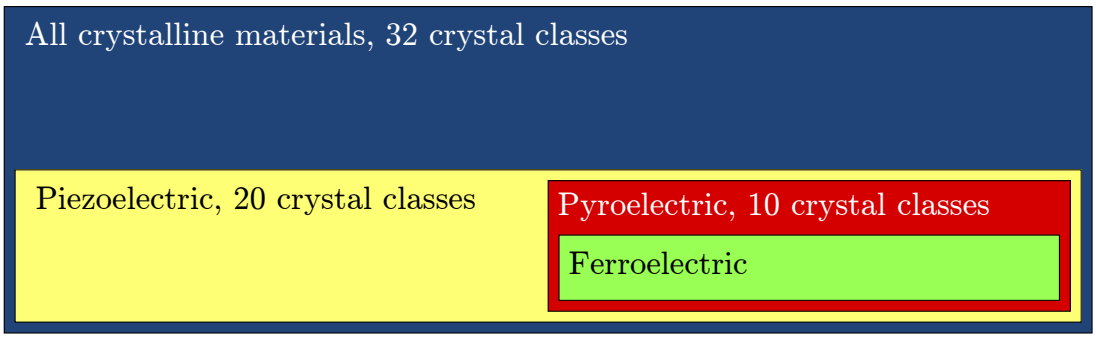


Figure 2.2: Venn diagram showing possible combinations of material properties.

[1]The crystal class is here written using the Hermann–Mauguin notation. The class 432 does not display any piezoelectric effect because the two-fold axis of rotation is perpendicular to the four-fold axis of rotation.

2.2 Ferroelectricity and PZT

Materials that have more than one possible direction of polarisation, and for which that direction can be switched by an electric field, are called ferroelectric. PZT ($PbZr_xTi_{1-x}O_3$) is one such material which has 6 possible directions of polarisation in the tetragonal phase, and has eight possible directions of polarisation in the rhombohedral phase. The phase diagram of PZT is shown in Figure 2.3. The boundary between the tetragonal and rhombohedral phase is called a morphotrophic phase boundary, because the phase transition appears by varying composition rather than temperature.

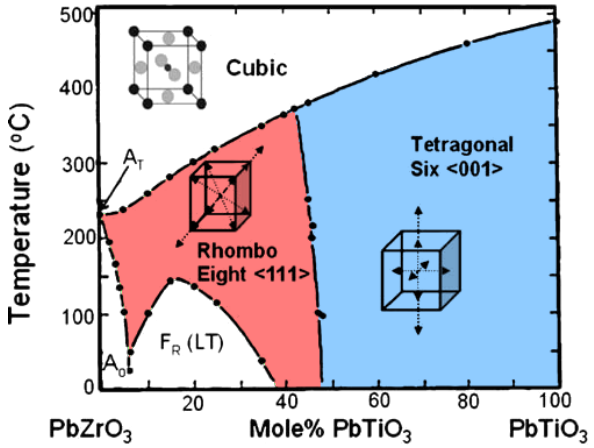


Figure 2.3: PZT phase diagram where the piezoelectric phases have been shaded red and blue. The morphotropic phase boundary can be seen at around 48 % $PbTiO_3$.[14]

PZT also has a cubic paraelectric phase above the Curie temperature T_c, and the structure in the cubic and tetragonal phase is shown in Figure 2.4. The direction of polarisation in the tetragonal or rhombohedral phase can be switched by an opposing electric field. If the polarisation is switched by 180°, the shape of the unit cell remains the same, but switching the polarisation to a different direction will distort the unit cell and is associated with stress and strain in polycrystalline materials.

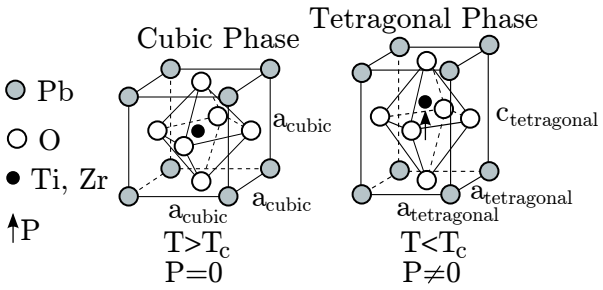


Figure 2.4: Structure of PZT above and below the Curie temperature T_c, for [Ti]>[Zr]. Adapted from [12]. The polarisation $\vec{P}$ is caused by the displacement of the O and Pb ions with respect to the Ti and Zr ions. Figure from [1]

PZT, is commonly chosen for devices because it has very high piezoelectric coefficients in both in the tetragonal and rhombohedral phases. At the morphotropic phase boundary (MPB), shown in Figure 2.3, the structure is degenerate and can take rhombohedral and tetragonal symmetry at the same time, causing the piezoelectric coefficient to peak[14].

2.3 Ferroelasticity

Ferroelasticity describes how strain in a material has an impact on the axis of polarisation (and the phase, in the case of the morphotropic phase boundary). The corresponding terms in Gibbs

free energy can be expressed in as in Equation 2.6[15]:

$$\Delta G = ... - Q_{ji} T_i P_j^2 + ... \tag{2.6}$$

Where the terms are second order in polarisation, and first order in stress. These terms are the origin of both the piezoelectric and ferroelastic effect, and give for example the g_{33} and g_{31} piezoelectric coefficients as shown in Equations 2.7a and 2.7b[15].

$$g_{33} = -\frac{\partial^2 G}{\partial T_3 \partial P_3} = 2Q_{33}P_3 \tag{2.7a}$$

$$g_{31} = -\frac{\partial^2 G}{\partial T_1 \partial P_3} = 2Q_{31}P_3 \tag{2.7b}$$

The ferroelastic coefficient also relate to this term in Gibbs free energy, as shown in Equations 2.8a and 2.8b[15],

$$\xi_{s,3} = -\frac{\partial G}{\partial T_3} = Q_{33}P_{s,3}^2 \tag{2.8a}$$

$$\xi_{s,1} = -\frac{\partial G}{\partial T_1} = Q_{31}P_{s,3}^2 \tag{2.8b}$$

which describes a spontaneous strain $\xi_{s,3}$ and $\xi_{s,1}$ arising from the spontaneous polarisation $P_{s,3}$ present in the material. Note that as the polarisation is squared, so that only the axis of polarisation is connected to strain, not the direction itself.

In this work a PZT thin film is deposited using a sol-gel method, and this film will shrink during crystallisation at 650 °C developing in-plane tensile stress. It also has a thermal expansion coefficient greater than the Si wafer, and after crystallising the PZT will develop more in-plane tensile strain as it cools down. In PZT $Q_{33} > 0$ and $Q_{31} < 0$, so that in-plane tensile stress will favour the axis of polarisation to also be in-plane.[2] For (100) oriented PZT thin films with an MPB composition, it is further believed that this will favour the tetragonal phase. This is because the tetragonal phase will have the polarisation in-plane with the film, while the rhombohedral phase will always have the polarisation 45 ° to the plane of the film.

2.4 Gevorgian's Model and the Corrective Factor $\alpha_{\text{Gevorgian}}$

When applying voltage to a sample with IDE structures, the electrical field is commonly approximated as $E = V/a$, where a is the electrode spacing. This is here referred to as the simple model[3]. A sample where this model would be accurate is shown in Figure 2.5(a), while the actual IDE structure is shown in Figure 2.5(b).

[2] In ceramic PZT which is not clamped to a substrate, grains typically obtain polarisation in different directions to relieve strain. This causes strain to develop when the ferroelectric is poled, and the ferroelastic effect becomes a cause of back-switching, returning domains to their original state.

[3] The design in Figure 2.5(a) could be realised by etching trenches through the film and depositing the electrodes in the trenches. Although difficult, this could be done. However, this process is expected to yield poor electrical properties as etching will damage the surface where the electrodes would later be contacted to the PZT, and has therefore not been considered further.

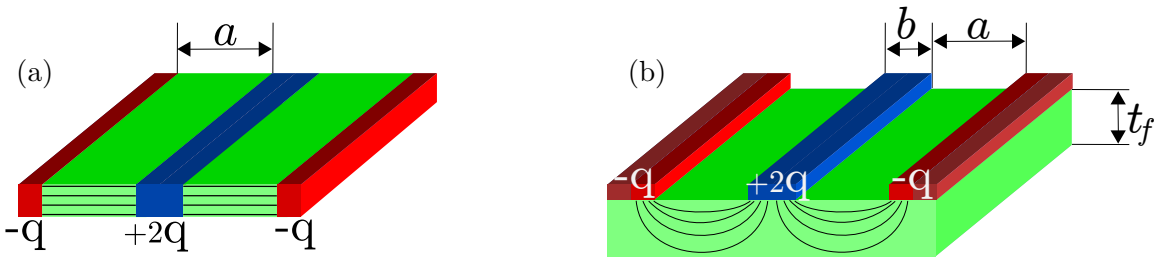


Figure 2.5: The simple model describes the structure in (a) accurately, but it is also often used1 to describe the IDE structure shown in (b), ignoring the differences in the shape of the electric field. The field lines are shown, showing straight field lines in (a) and curved field lines in (b). Figure from [1]

A model by Spartak Gevorgian et al.[10][4] can be used to accurately calculate the capacitance of the IDE structure, and is commonly used in reverse to calculate the dielectric constant ε in such samples. The model by Gevorgian assumes that the dielectric constant is not dependent on the strength of the applied electric field, and is reproduced in Equation 2.9[10],

$$C_{\text{Gevorgian}} = \frac{\varepsilon}{2}\frac{K(k)}{K(k')} \tag{2.9a}$$

$$K(k) = \int_0^1 \frac{\mathrm{d}t}{\sqrt{(1-t^2)(1-k^2t^2)}} \tag{2.9b}$$

$$k = \frac{\sinh\left(\frac{\pi b}{4t_f}\right)}{\sinh\left(\frac{\pi(a+b)}{4t_f}\right)}\sqrt{\frac{\cosh^2\left(\frac{\pi(a+b)}{4t_f}\right)+\sinh^2\left(\frac{\pi(a+b)}{4t_f}\right)}{\cosh^2\left(\frac{\pi b}{4t_f}\right)+\sinh^2\left(\frac{\pi(a+b)}{4t_f}\right)}} \tag{2.9c}$$

$$k' = \sqrt{1-k^2} \tag{2.9d}$$

where $K(k)$ is known as an elliptical integral of the first kind, defined in Equation 2.9b. t_f is the thickness of the film, a is the electrode spacing, and b is the electrode width. It can be seen that although this model is accurate, it is also relatively complicated, and the dependence on the input parameters is non-trivial. By comparing this model to the capacitance obtained by the simple model, a corrective factor $\alpha_{\text{Gevorgian}}$ has previously been employed[6], as shown in Equation 2.10b.

$$C_{\text{Simple}} = \varepsilon\frac{t_f}{a} \tag{2.10a}$$

$$\alpha_{\text{Gevorgian}} = \frac{C_{\text{Simple}}}{C_{\text{Gevorgian}}} \tag{2.10b}$$

This corrective factor has been used to scale the electrical field in hysteresis loops, as shown in Equation 2.11, and this has been found to cause a significant increase in overlap between hysteresis loops obtained from samples with different electrode spacing a compared to the simple model[6]. However, there is limited theoretical background to support this, due to the

[4]Gevorgian's model is based on a Schwartz-Chrisoffel mapping of space and a calculation of capacitance.

complicated nature of the model by Gevorgian.

$$E_{\text{corrected}} = \frac{E_{\text{simple}}}{\alpha_{\text{Gevorgian}}} = \frac{V/a}{\alpha_{\text{Gevorgian}}} \tag{2.11}$$

2.5 Poling of Ferroelectrics

As-fabricated[5], a PZT film may have ferroelectric domains in all possible directions, and different domains may therefore have piezoelectric contributions in different directions. In order to increase the net piezoelectric effect, all ferroelectric domains should therefore be oriented in one direction.

Poling is the process of orienting ferroelectric domains by applying an electric field larger than the coercive field E_c on a sample. Ferroelectric domains will then align with the field. When the electric field is removed, some domains may switch back to the previous polarisation, due to material stress and trapped charge in the material that makes the previous state more energetically favourable. To reduce back-switching poling can be done at elevated temperatures and for a long time, so that the material can adapt to the new conditions and relax before the field is removed. Increasing the temperature also reduces the coercive field. The state of the samples when poled with a positive or a negative voltage is shown in figure 2.6.

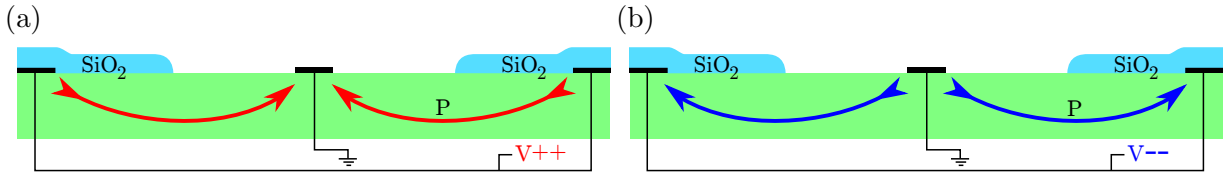


Figure 2.6: Direction of polarisation P when poled with (a) a positive voltage and (b) a negative voltage. The grounded electrode always remains the same.

2.6 Ageing

Ageing is a process where the current polarisation direction is stabilised over time. This process is illustrated in Figure 2.7. There are several possible causes for ageing, and some will be described below.

This change in the shape of the energy landscape of the film will have an effect on the observed properties. It can be seen from Figure 2.7(b) that the energy required to switch the film from $\leftarrow$ to $\rightarrow$ is higher than from $\rightarrow$ back to $\leftarrow$. This manifests itself as different values for the coercive fields ($E_{c,+}$ and $E_{c,-}$) in the hysteresis curve, as shown in Figure 2.8. The offset can be quantified by Equation 2.12.

$$E_{\text{offset}} = \frac{E_{c,-} + E_{c,+}}{2} \tag{2.12}$$

[5] As-fabricated refers in this work to samples not annealed or poled after fabrication.

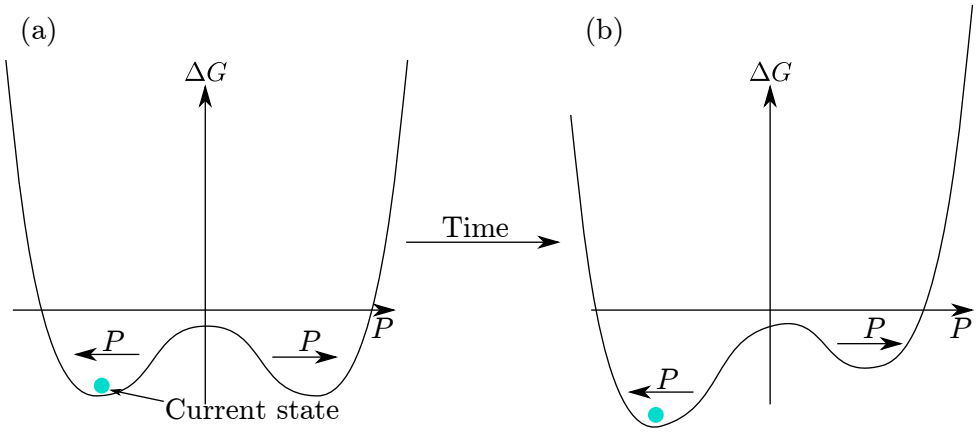


Figure 2.7: (a) Gibbs free energy as a function of polarisation (energy landscape) of tetragonal thin-film PZT with 2 possible polarisation directions shown (up, down, in and out not shown). The two states shown will initially have equal energy. (b) As the sample ages, the current polarisation direction is stabilised, changing the energy landscape, and reducing the energy of the current polarisation direction. The lower energy of this state means that this state is now favoured relative to the other possible polarisation directions.

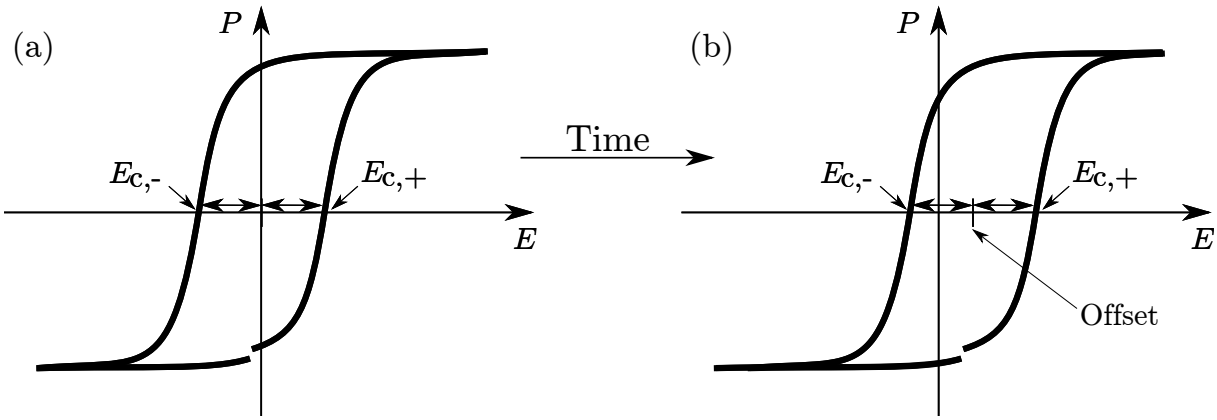


Figure 2.8: Change in PV loop as sample ages. (a) The hysteresis loop is centred around zero electric field prior to ageing. (b) After ageing, the loop is no longer centred, and has developed an offset. The loops in (a) and (b) are illustrative of the corresponding states in Figure 2.7. A description of other features of the PV loop follows in Section 3.1.

2.6.1 Defect Dipoles

One possible process responsible for ageing is rotation of defect dipoles. Defect dipoles are most commonly formed from oxygen vacancies (V_O^{**})[6] and cation substitutions (for example Fe^{3+} on a Ti,Zr site, $Fe'_{Ti,Zr}$)[16]. The oxygen vacancy is positively charged with respect to the lattice, while the Fe^{3+} is negatively charged. The two defects will therefore attract, and the oxygen can move between different sites in the oxygen octahedra so that the dipole aligns favourably with the current direction of polarisation.

First principle calculations have shown that defect dipoles with oxygen vacancies prefer to align with the polarisation direction in the tetragonal phase, due to a relaxation of elastic energy in the lattice surrounding the defects[17, 18]. The effect of the defect dipole on the lattice is shown

[6]Kröger–Vink notation is used here, where V_O^{**} denotes a vacancy (V) on an oxygen site ($_O$) that is positive (**) with respect to the lattice site. O_O^x denotes a neutral oxygen on an oxygen site, while $Fe'_{Ti,Zr}$ denotes iron on a Ti,Zr site, negative with respect to the lattice site.

in Figure 2.9[7]. In rhombohedral PZT, the preferred orientation of a defect dipole is not known, but it is assumed that it will depend on the polarisation direction, and the observed effect will therefore be the same.

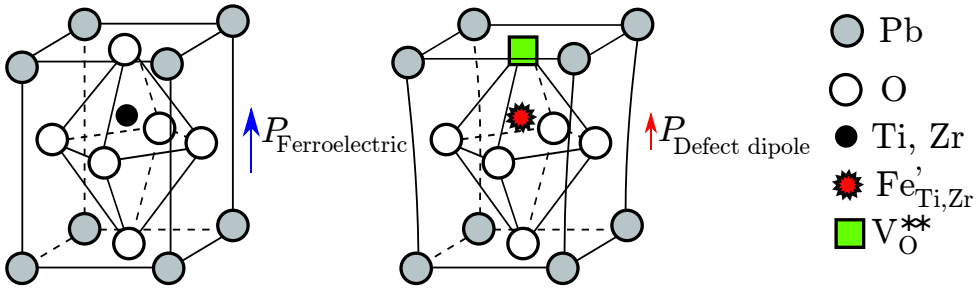


Figure 2.9: The figure shows a normal unit cell (a) and a unit cell that has deformed due to the presence of a defect dipole.

Reorientation of defect dipoles after poling is illustrated in Figure 2.10. First principle calculations have shown that orientation of defect dipoles occurs on a timescale of hours to days at room temperature, with a strong temperature dependence[18]. Each defect dipole is seen as independent, and will need to overcome an energy barrier in order to move between different sites, giving a probability distribution as in Equation 2.13[18].

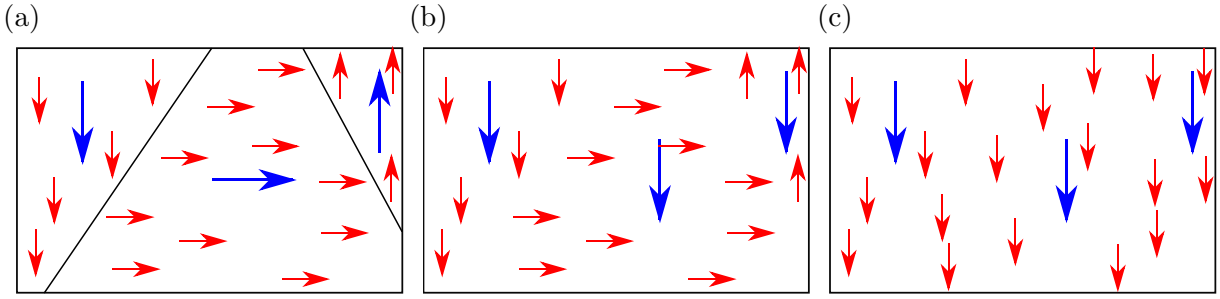


Figure 2.10: (a) Domain structure of aged, as-fabricated ferroelectric, where domains (large blue arrows) are randomly distributed. The defect dipoles (small red arrows) have aligned with the local polarisation direction. (b) Immediately after poling (for example by a PV measurement) the polarisation has switched, but the defect dipoles have not rotated. (c) After ageing in the new state, the defect dipoles have reoriented in order to relax the lattice in the new state.

$$P_{\text{switched}} \propto 1 - e^{-t/\tau} \tag{2.13}$$

Where P_{switched} is the probability that the defect dipole has switched to the new favourable position at a time t after switching the polarisation direction. The shift of the coercive field (offset) due to this is expected to be proportional to the probability distribution function. This is because each defect dipole will behave independent of all other defect dipoles, and each dipole brings an equal contribution to the total offset. However, the time constant τ could be different for different sets of defect dipoles in different strain situations.

[7]This figure is made based on a conversation with Prof. Dragan Damjanovic, who has studied the effect of defect dipoles on the lattice[17]. This figure will also be used for future versions of the course 'Dielectric properties of materials', taught by Prof. Damjanovic.

2.6.2 Interface Screening by Local Charge

Another possible mechanism for ageing is charge injection at the electrodes. When a ferroelectric material is poled, charges will remain at the electrodes to compensate for the charges from the remanent polarisation. However, a passive layer may be present between the electrode and the ferroelectric. This passive layer may for instance be PZT that has lost its ferroelectric properties due to damage from sputtering of the electrode. The charge from the polarisation and the compensating charge at the electrode will then be spatially separated, and an electric field will be present across the passive layer. The energy contained in this field will be reduced if the charge at the electrode moves closer to the ferroelectric PZT[19]. This process is illustrated in Figure 2.11. Charge relocated in this way will stabilise the current polarisation. As such, switching the polarisation to the opposite direction becomes more difficult.

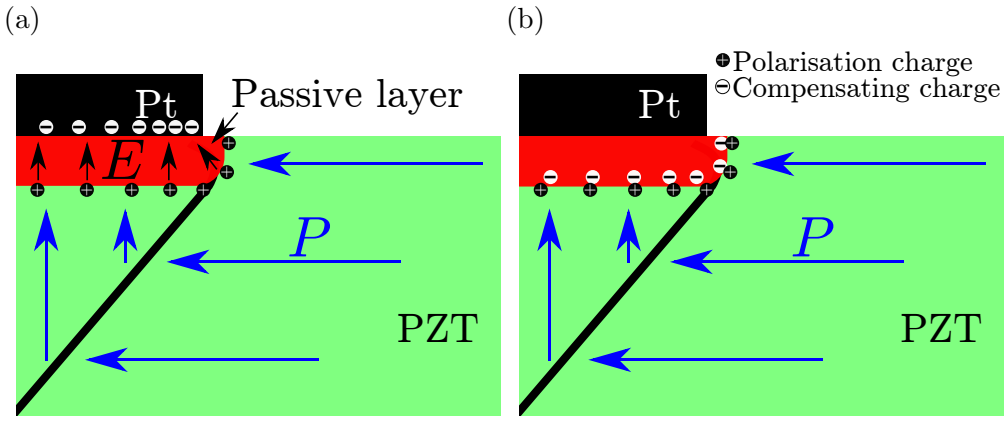


Figure 2.11: (a) A poled PZT film with compensating charge at the electrode and a large electric field across the passive layer surrounding the electrode. (b) The compensating charge has moved across the passive layer and the total energy of the system is reduced. Two domains are shown in the PZT, separated by a domain wall. The domain wall is neutral as the charges from the two domains cancel. The domain structure surrounding the electrode is not known, but the structure shown is plausible since the neutral domain wall has low energy.

Initially, ageing by this mechanism is expected to follow an exponential function, similar to the orientation of defect dipoles. However, as more charge is moved across the barrier, the electric field decreases, and the energy barrier becomes higher[19]. The phenomenon could therefore be expected to be described by a stretched exponential function, depending on the initial energy barrier and how much the barrier is lowered by the electric field. The time scale of this phenomenon can also be expected to vary significantly with the size of the energy barrier.

In practice the expected mechanism for the movement of charge is charge separation from traps within the passive layer, rather than charge tunnelling directly from the electrode. This is based on the fact that no electrode dependence has been observed experimentally[19]. Experimental results have been found to agree with this model for shallow traps in a passive layer (0.35 eV) and a passive layer of about 5nm[19]. This mechanism is shown in Figure 2.12.

Charge separation is also expected to be enhanced by UV illumination, as UV illumination energises electrons so that they can move across energy barriers more easily[20]. The fact that UV enhances ageing is known from previous studies[21, 22, 23]

Grossmann et.al [19] has presented a model for charge separation in the boundary layer, as

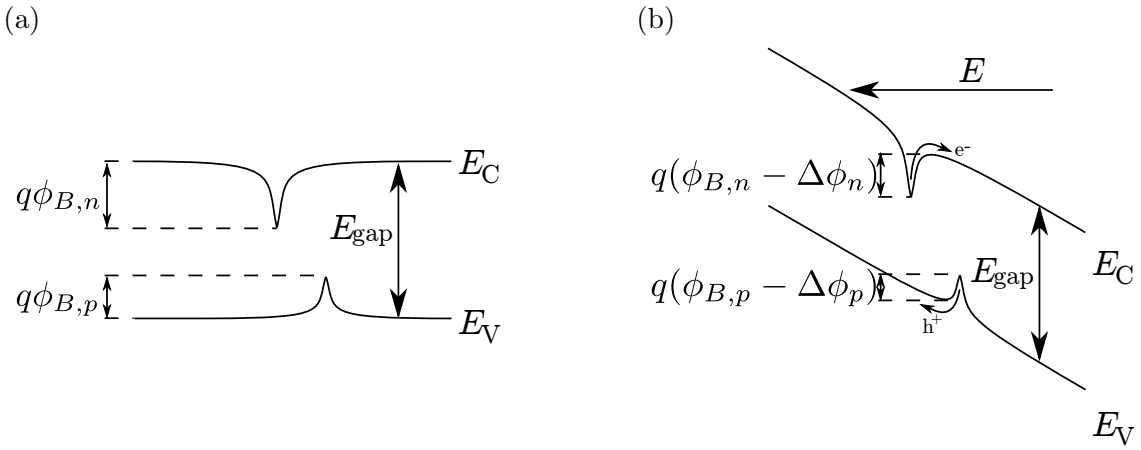


Figure 2.12: Potential wells in the band (a) in the absence of an electric field, and (b) in the presence of an electric field. Charge in the form of electrons and holes may escape the wells as indicated in (b).

shown in Equations 2.14a to 2.14d.

$$J(t) = \sigma_{FP} E_i(t) e^{\frac{-q}{k_b T}(\phi_B - \Delta\phi(t))} \tag{2.14a}$$

$$\Delta\phi(t) = \sqrt{\frac{qE_i(t)}{\pi\varepsilon_{opt}}} \tag{2.14b}$$

$$E_i(t) = \sigma_e(t)\frac{A/\delta_a}{C_i + C_{fe}} \tag{2.14c}$$

$$\sigma_e(t) = \sigma_e(0) - \int_0^t J(t) \tag{2.14d}$$

In these equations, $J(t)$ is the current across the boundary due to charge separation and σ_{FP} is a conductivity relating to this transport, determined among others by the density of trapping centres and mobility of the electrons and holes[24]. E_i is the time-dependent electric field in the interface, ϕ_B is the potential barrier of the trapping centres and $\Delta\phi$ is the lowering of the potential barrier due to the electric field. ε_{opt} is the optical component of the dielectric constant in the interface layer. σ_e is the charge remaining at the electrode, while $\sigma_e(0)$, is the total amount of compensating charge assumed to be $\sigma_e(0) \approx P$ where P is the polarisation charge. δ_a is the thickness of the interface layer, A is the area, and C_i and C_{fe} are the capacitances of the interface and ferroelectric layer respectively. k_b is Boltzmann's constant, T is temperature, and q is the elementary charge.

In the case where $a_{\mathrm{eff}} >> \delta_a$ it can be assumed that $C_{fe} << C_i$ and Equation 2.14c can be simplified to Equation 2.15.

$$E_i(t) = \frac{\sigma_e(t)}{\varepsilon_i} \tag{2.15}$$

In this equation, ε_i is the dielectric constant of the interface layer. The voltage offset in the case where $C_{fe} << C_i$ can be found by considering the two cases shown in Figure 2.13.

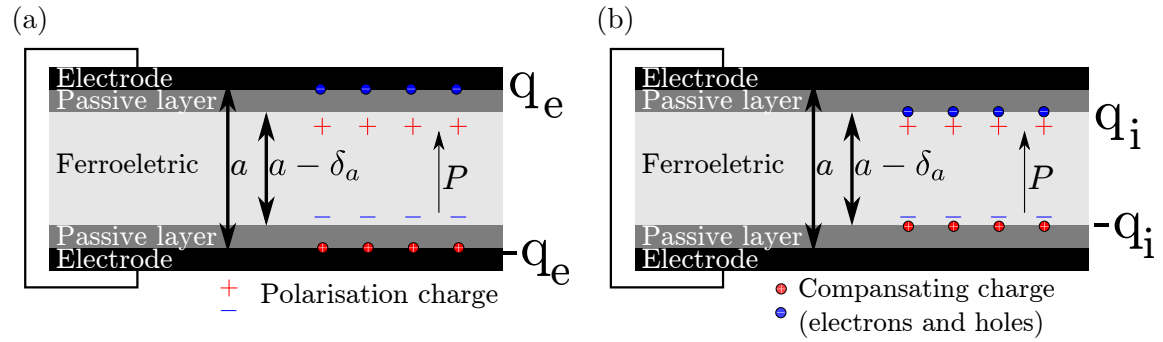


Figure 2.13: (a) compensating charge at the electrode, (b) compensating charge at the interface between the ferroelectric and passive layer. This figure shows a PPE design, and it is assumed here that the same theory can be used for IDE designs.

By integrating the electric field along the circuit in Figure 2.13(a) and (b) one obtains Equations 2.16a and b.

$$\frac{Pa}{\varepsilon_{fe}} - q_e \frac{C_i + C_{fe}}{C_i C_{fe}} = 0 \tag{2.16a}$$

$$\frac{Pa}{\varepsilon_{fe}} - q_i \frac{1}{C_{fe}} = 0 \tag{2.16b}$$

The maximum voltage offset is the difference in voltage needed to compensate these two charges, shown in Equation 2.17.[8]

$$V_{\text{offset,max}} = (q_e - q_i)\frac{C_i + C_{fe}}{C_i C_{fe}} = \frac{PA}{C_i} = \frac{P\delta_a}{\varepsilon_i} \tag{2.17}$$

With a maximum offset in the PV loop:

$$E_{\text{offset,max}} = \frac{V_{\text{shift}}}{a} = \frac{P}{\varepsilon_i}\frac{\delta_a}{a} \tag{2.18}$$

The offset will scale linearly with the moved charge, so that the offset can be described by Equation 2.19:

$$E_{\text{offset}}(t) = (\sigma_e(0) - \sigma_e(t))\frac{\delta_a}{a\varepsilon_i} = \frac{\delta_a}{a}\frac{\int_0^t J(t)}{\varepsilon_i} \tag{2.19}$$

The simplifications done in the case $C_{fe} << C_i$ lead to a much simpler model than the one presented in [19]. The simplifications separate the variables, so that the dependence on the various factors can be found:

- The thickness of the interface layer only changes the maximum offset, and increasing the thickness increases the offset. The total thickness may be a series a thin layers throughout the film, or one thicker layer at the electrode.

- ε_i scales the offset, and the electric field in the passive layer before ageing starts. A change

[8] A more comprehensive version of this model is found in [19], but this leads to a more complicated expression, and the added complexity is not needed to describe the results obtained in this work. The simplified version presented here has been developed for this work.

in ε_i/δ_a will only affect the electric field in the passive layer, in such a way that increasing ε_i/δ_a decreases the electric field, shifting the ageing to longer time scales.

- The optical part of the dielectric constant ε_{opt} only affects the reduction in energy barrier $\Delta\phi$. Decreasing ε_{opt} increases the reduction in energy barrier in the initial state, and this controls the time at which ageing starts to become significant in the plot.

- The trap depth, ϕ_B controls the maximum energy barrier, and this largely controls the time at which ageing is 'complete'.

- $\sigma_e(0)$ can be found from experiments, as it is assumed to be approximately the remnant polarisation.

- σ_{FP} will shift the entire curve on the x-axis, but as this is a logarithm in time, the dependence is very weak.

- The temperature T will also have a large effect on the ageing rate, where higher temperature shifts the ageing to shorter time scales.

How the shape of the curve changes with the variables is indicated in Figure 2.14.

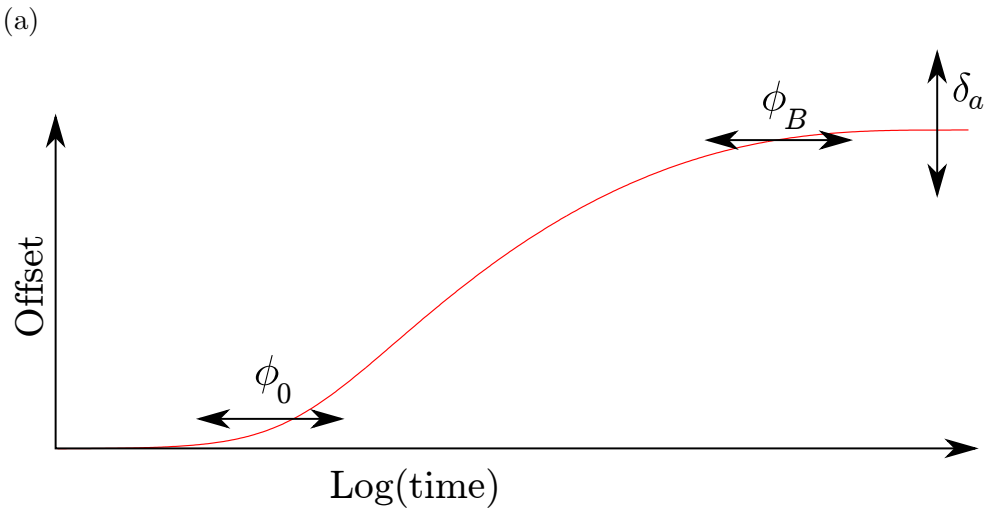


Figure 2.14: The figure shows qualitatively how the model behaves when different parameters are varied. $\phi_0 = \phi_B - \Delta\phi(0)$ controls when the offset first appears in the plot, ϕ_B controls when the sample is done ageing. δ_a controls the maximum offset, scaling the graph along the y-axis.

Fitting the model to experimental data[9] can then be done by using δ_a, ϕ_B and $\phi_0 = \phi_B - \Delta\phi(0)$ as independent variables, and fixing $\sigma_e(0) = P$, σ_{FP} and ε_i based on estimates. If these parameters are not fixed the fit will not be unique, as multiple parameters control the same features. Using $\phi_0 = \phi_B - \Delta\phi$ as an independent variable, ε_{opt} can be found by Equation 2.20.

$$\varepsilon_{\text{opt}} = \frac{q\sigma_e(0)}{\pi\varepsilon_i(\phi_B - \phi_0)^2} \tag{2.20}$$

[9] As the model is based on numerical integration of $J(t)$, fitting the model to experimental data must be based on a variation of the parameters.

2.6.3 Grossmann's Model and Grain Boundaries

Grain boundaries can be considered as passive layers, and there is a chance that charge injection may also happen across them. The papers by Grossmann do not discuss grain boundaries as a possible passive layer. This may be because the experimental results used by Grossmann for verification are obtained from thin films deposited by sol-gel, and are measured using a traditional PPE design. These films have a quasi-columnar grain structure, and one can assume that there are no grain boundaries perpendicular to the electric field[20, 19].

The films studied in this work are also deposited by sol-gel and have a columnar grain structure, but since the electric field is predominantly in-plane in the IDE structure, there will be a large number of grain boundaries between the electrodes. It is possible that each grain boundary can be considered as a thin passive region, and therefore contribute to ageing in a manner similar to a passive region at the electrode. This is illustrated in Figure 2.15.

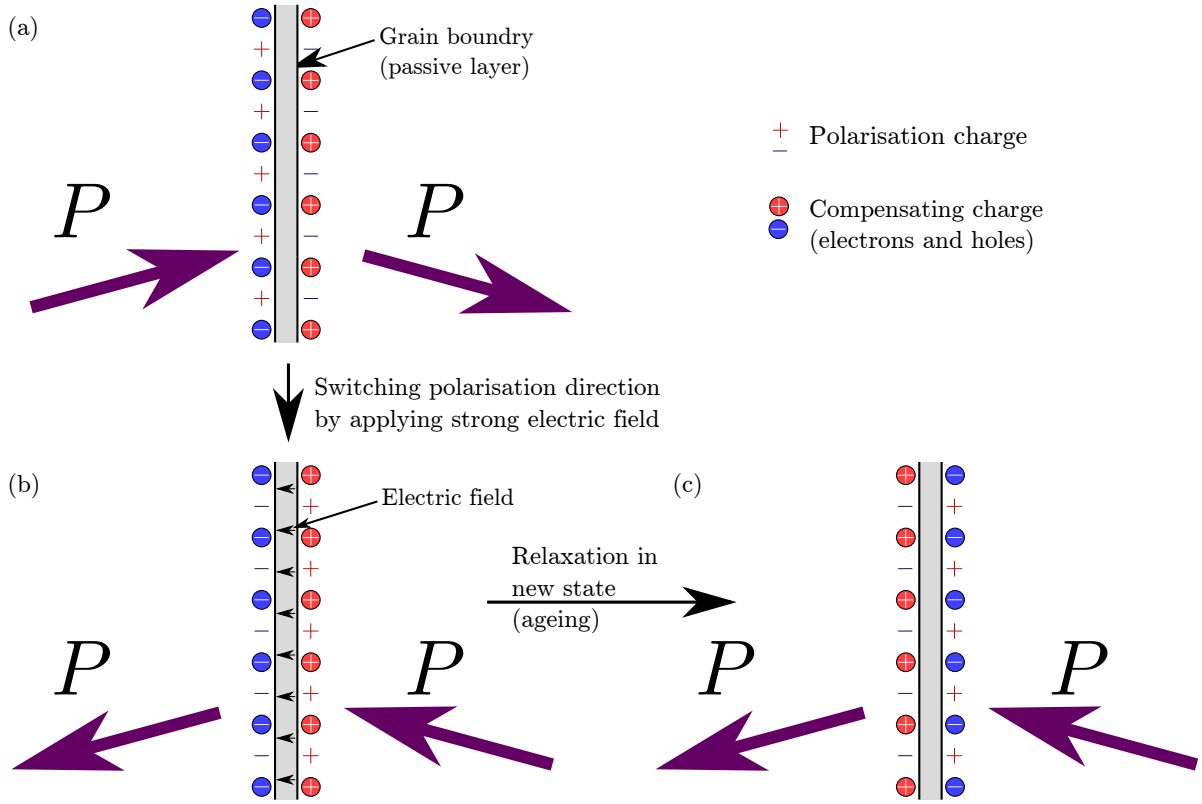


Figure 2.15: Illustration of compensating charge moving across a grain boundary. (a) Grain boundary between two grains where both grains have polarisation going left to right. Mobile charge is compensating the polarisation charge on both sides of the grain boundary, so that the grain boundary as a whole is in the lowest energy state[10]. (b) Switching the polarisation in the grains causes a large electric field to form across the grain boundary, as the compensating charge can not easily move across the boundary. (c) After ageing for an extended period of time, the compensating charge has relaxed by relocating across the grain boundary, and the grain boundary has again reached a lowest energy state.

Grossmann's model does not differentiate between one 'thick' passive layer at the interface, and a number of thinner passive layers dispersed throughout the film, as would be the case for grain

[10]The lowest energy state of the grain boundary does not require that there is no electric field across the grain boundary. It is simply the state where no motion of electrons and holes can reduce the total energy of the system.

boundaries. However, one would need to re-evaluate the assumptions made, as grain boundaries are often riddled with defects, and the energy landscape of the bands may contain numerous localised states.

Despite this, if one applies the same assumption as for Grossmann's model, one would expect similar behaviour, even if the passive layer consist of multiple thin layers, rather than one relatively thick layer at the interface.

If ageing is driven by charge moving across passive layers at grain boundaries, one would expect $\delta_a \propto a$, and the offsets seen in the coercive fields would be expected to be independent of the electrode spacing a.

This interpretation of Grossmann's model has been developed for this work, since there are numerous grain boundaries in the sample studied here, and it is possible that they play a role in the ageing process.

2.6.4 Motion of Mobile Charge

Motion of mobile charge, such as oxygen vacancies not bound in defect dipoles, to charged surfaces in the material has been suggested as a mechanism of ageing. As presented by Yuri A. Genenko et al.[25], the time-scale depends on the number and size of domains in the ferroelectric material, as charge is thought to move between domains of opposite polarisation. However, one could also imagine charge moving to (or from) a grain boundary where the polarisation direction of neighbouring grains has caused the grain boundary to be charged. Due to the random in-plane orientation of grains, the polarisation vectors of neighbouring grains cannot match perfectly, and it is therefore likely that the grain boundaries become charged. The time scale in Genenko's model is of the order of days, but this would depend strongly on the temperature and the mobility of oxygen vacancies[25]. This mobility could be much greater at grain boundaries.

2.6.5 Characterisation of Ageing

Ageing is measured most accurately by the offset of the polarisation loop, easily defined from the positive and negative coercive fields, $E_{\text{offset}} = \frac{E_{c,-}+E_{c,+}}{2}$. This shift is best seen on a logarithmic time-scale and has been described using the logarithmic law shown in Equation 2.21[26].

$$E_{\text{offset}} = F \log(t/t_0) \tag{2.21}$$

Where F and t_0 are constants.

Alternatively, one can describe this is as a relaxation process. However, no single time constant τ can be found to fit with experiments[1], as required for Debye type relaxation. This indicates that the speed of relaxation is dependent on the state of relaxation in the material, or that there is a number of relaxation processes in the material with different time constants τ. An asymptotic power law may be used to fit the experimental data in this case[27]:

$$\Phi = \frac{1}{1+(t/\tau)^{\delta}} \ , \quad \delta > 0 \tag{2.22}$$

Where Φ is the relaxation function, τ is the characteristic time constant and δ is a constant.

This relaxation distribution gives rise to a shift in the coercive field as given below:

$$E_{\text{offset}} = E_{\text{offset,max}}\left(1 - \frac{1}{1 + (t/\tau)^{\delta}}\right) \tag{2.23}$$

Where $E_{\text{offset,max}}$ is the offset as t reaches infinity.

Fitting experimental data to such a function is useful in the case where the origin of the phenomenon is not known and several theories exist that can explain the observed phenomenon. This empirical function is also very simple, as it has only three variables, so that each fit is unique. This is in contrast to Grossmann's model, where a fit is not unique, and the parameters obtained therefore have a large uncertainty.

2.7 Effect of Exposure to UV

Due to the semiconductor nature of PZT, it is expected that UV radiation with energy greater than the band gap will excite electrons from the valence band to the conduction band. This will produce holes in the valence band as well as electrons in the conduction band and allow a photocurrent to pass through the material. The band gap of PZT is given as 3.41 eV in[28], corresponding to a wavelength of 364 nm, but this is debated[21].

Sub-bandgap radiation may also introduce a photocurrent, namely if electrons are excited to or from a defect state such as an oxygen vacancy. This is illustrated in Figure 2.16. UV illumination of wavelength 405 nm (3.06 eV) is of particular interest, as samples are exposed to this wavelength during photolithography.

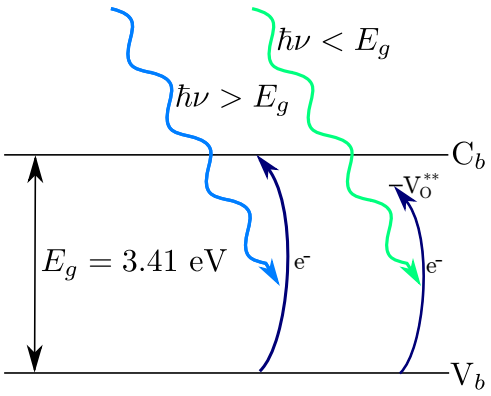


Figure 2.16: Incoming photons with energy $\hbar\nu > E_g$ may excite electrons directly to the conduction band. Photons with energy $\hbar\nu < E_g$ may excite electrons to (or from) states in the band gap, generating holes in the valence band (or electrons in the conduction band). An oxygen vacancy is shown as an example of such a state. Electrons in a defect state may be further exited by light or thermal energy to the conduction band (not shown).

Chapter 3

Measurement Techniques

This chapter includes details of the measurement techniques used, so that the reader becomes familiar with them before the results are presented. Emphasis is placed on details in the PV loops. Some theory relating to how the shape of a PV loop is affected by the presence of a passive layer is also included. This is included here because it is intimately linked with the measurement technique. Following this, e_{IDE} is defined, and the setup used to measure e_{IDE} is discussed.

3.1 PV Loops

A PV loop is obtained by cycling a sample with a triangle pulse, and measuring the collected charge, as shown in Figure 3.1. The charge collected will include leakage ($I \propto \rho V$), capacitive charging current ($I \propto \varepsilon \frac{\partial V}{\partial t}$), and polarisation current ($I \propto \frac{\partial P}{\partial t}$). Ferroelectric materials typically have a high resistivity, so that the leakage current is very small, and leakage can in most cases be neglected. Furthermore, when ferroelectric switching occurs, the switching current will be much larger than the capacitive charging current, so that the major features in the loop can easily be attributed to ferroelectric switching. The approximations $P \approx D$ and $A\frac{\partial D}{\partial t} \approx I$, are frequently employed, where P is the polarisation, D is the electric displacement field, and A the is area.

The loop is obtained by plotting the polarisation $P \approx D$, as a function of the electric field E, as shown in Figure 3.2. Major features are easily identified when the results are displayed in this way, but it should be noted that the shape of the loop depends on the frequency of the electric field, and this information is not shown in PV loops.

Important features of the PV loop are shown in Figure 3.2, such as the positive and negative coercive fields ($E_{c,+}$ and $E_{c,-}$), which describe the field at which the ferroelectric switching takes place. These values can be defined as the fields at the maximum slope $\frac{\partial P}{\partial E}$, or the field where the curve crosses the x-axis. Ideally these two definitions are expected to yield the same result, but this is not always the case. It should also be noted that the loop is centred with $P_{\max} = -P_{\min}$, so that the point where the curve crosses the x-axis is somewhat arbitrarily defined. Nonetheless, this definition of the coercive field is easily implemented and is used throughout this work. An offset can also be seen in Figure 3.2, and this is commonly observed due to ageing.

The remanent polarisation is the amount of polarisation remaining when the field has been removed. After the loop is complete, the ferroelectric will relax in the current state, and this

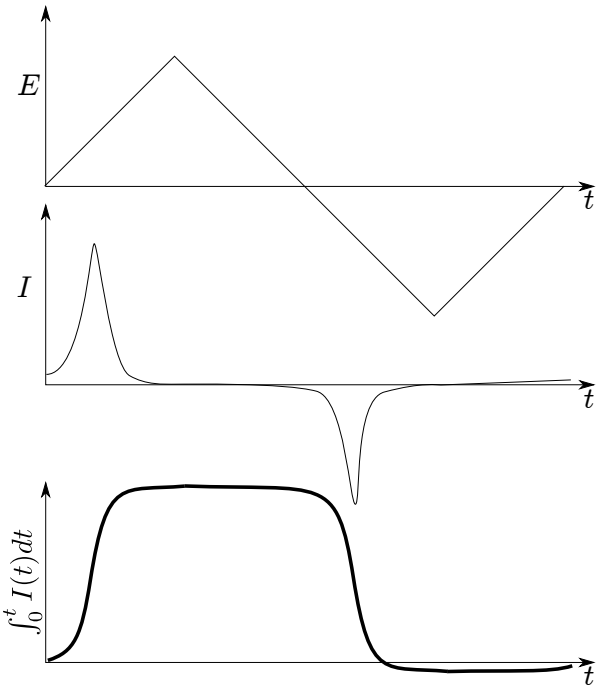


Figure 3.1: Applied electric field, current, and collected charge of a PV loop.

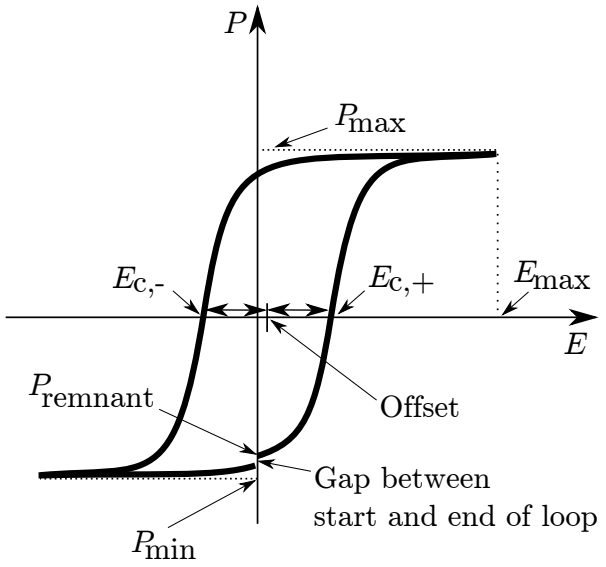


Figure 3.2: Schematic diagram of a PV loop showing important features[1].

results in small decrease in the remanent polarisation. The time between subsequent loops, and relaxation of the polarisation during this time is the reason why there is a gap between the start and end of the loop[1]. Furthermore, it should be noted that the slope $\frac{\partial P}{\partial E}$ at $E_{\max}$ will show capacitive effects, and the maximum slope $\frac{\partial P}{\partial E}$ describes how fast the film switches.

3.1.1 First Loop

The first loop measured on a sample will be different from the subsequent loops, as there is no remanent polarisation from a previous loop. Such a loop is schematically shown in Figure

[1]In order to have reproducible results, a prepol pulse is used on all PV loops with the exception of the first in a series, and the PV loops for measuring ageing. The prepol pulse is a pulse identical to the voltage pulse of the PV loop. There is a 1 s delay between the end of the prepol pulse and the start of the PV loop.

3.3(a). If the sample is self-poled, the self-poling will be evident by the location of the start of the curve. Since the curve is centred with respect to the maximum and minimum polarisation, self polarisation can only be identified in this way if the maximum and minimum polarisations are equal. A loop with positive self-poling is shown in Figure 3.3(b).

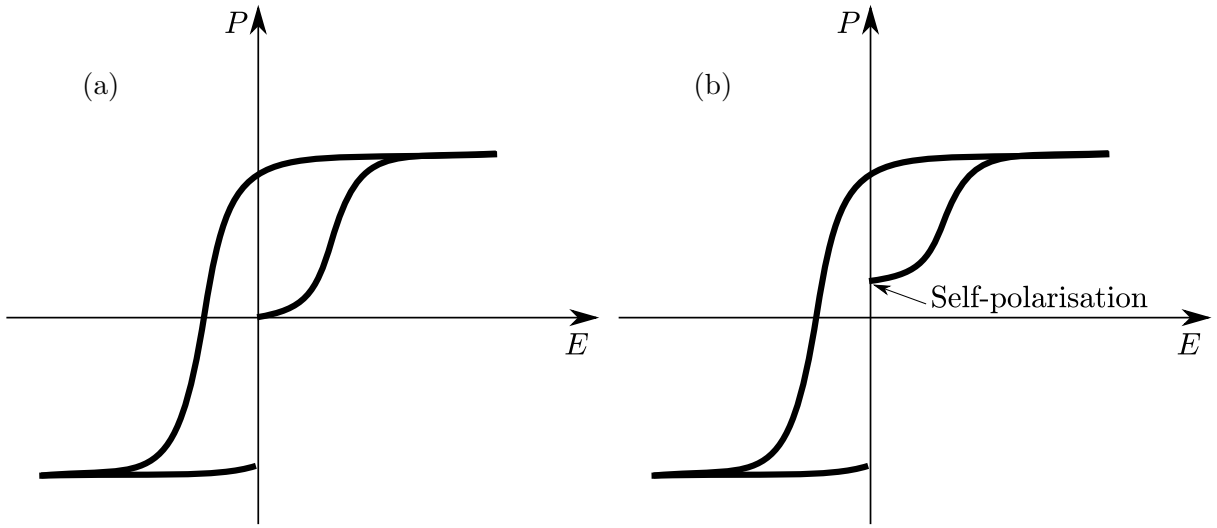


Figure 3.3: Schematic diagram of first PV loop on a sample. (a) Sample with no self-poling. (b) Sample with positive self-poling.

3.1.2 Pinched Loops

Some samples may also show loops that look like they have been pinched at the center. This is thought to be because different parts of the sample displays different offsets. This will typically be the case in as-fabricated samples, as each domain forms in a random direction after fabrication, and each domain will age in its current configuration. The coercive fields of some domains will therefore be shifted to the right, while the coercive fields of other domains will be shifted to the left. A drawing of a pinched loop is shown in Figure 3.4.

3.1.3 Effect of Passive Layers on PV Loops

A passive layer of non-ferroelectric PZT may be present in series with the PZT. A drawing of such a layer is shown in Figure 3.5(a) for a PPE design. This layer will have a profound effect on PV loops, causing them to become slanted and reducing the maximum polarisation, as shematically shown in Figure 3.5(b).

The effect of a passive layer is modelled in [29] by A. K. Takantsev and G. Gerra for parallel plate devices and this theory is expected to be valid also for IDE devices. In the case of IDE devices, the passive region could be located surrounding the electrodes, as shown in Figure 3.6. Such a region could possibly be caused by damage during sputtering.

Simulating the Effect of a Passive Region on a PV Loop

The model in [29] can be used to simulate the effect of a passive layer on a PV loop, and this model is reproduced here. When used in this way, the model takes a PV loop from a sample

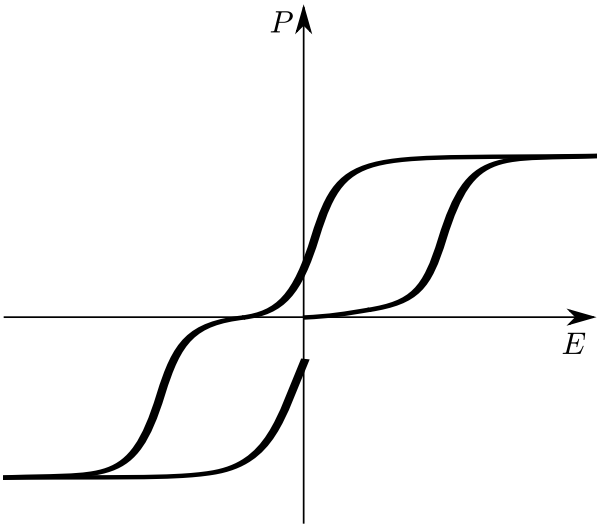


Figure 3.4: Schematic diagram of a pinched PV loop. Such loops are most commonly understood as two ferroelectric hysteresis loops with different coercive fields combined.

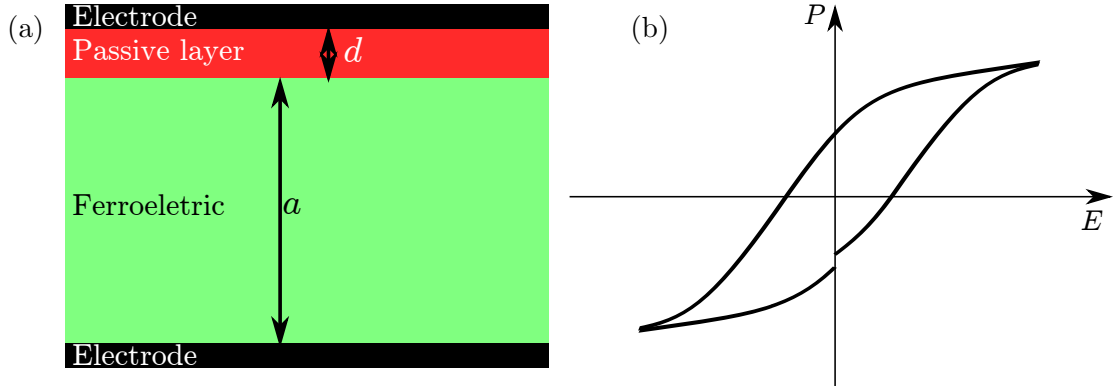


Figure 3.5: (a) Schematic drawing of a passive layer of non-ferroelectric material of thickness d in series with a ferroelectric of thickness a in a PPE structure. (b) Expected behaviour of PV loop in the case where a passive layer is present.

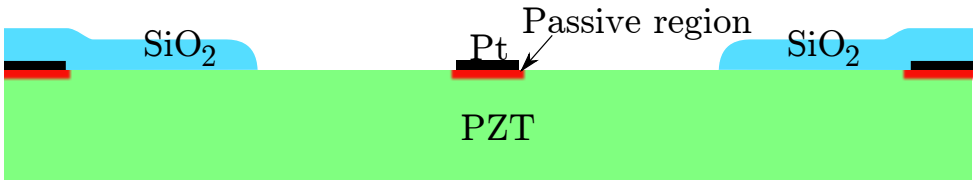


Figure 3.6: Schematic drawing of a passive region of non-ferroelectric PZT under the Pt contact pads, caused by damage during sputtering.

without a passive layer as input, and gives the expected PV loop of a stack including a passive layer as output.

The model assumes the presence of a non-ferroelectric (dielectric) layer of thickness d in series with a ferroelectric layer of thickness a, as shown in Figure 3.5(a). An applied electric field will be distributed between the two regions as shown in Equation 3.1, based on the conservation of the electric displacement field D.

$$\varepsilon_0 \varepsilon_d E_d = \varepsilon_0 E_f + P_f \tag{3.1}$$

Here, ε_d is the dielectric constant of the passive layer, E_d electric field in the passive layer, E_f electric field in the ferroelectric, and P_f is the polarisation of the ferroelectric. The voltage drop across the stack must also be equal to the sum of the voltage drop over the passive layer and ferroelectric layer, described by Equation 3.2.

$$V = (d + a)E_{\text{average}} = dE_d + aE_f \tag{3.2}$$

In most cases, the passive layer (d) will be much smaller than the ferroelectric layer (a) so that $d + a \approx a$. In ferroelectric PZT, the dielectric constant is much larger than 1, so that the electric displacement can be assumed to be equal to the polarisation. Using Equation 3.1 and 3.2, the electric field in the ferroelectric can then be found by Equation 3.3.

$$E_f = E_{\text{average}} - \frac{P_f}{\varepsilon_0 \varepsilon_d} \frac{d}{a} \tag{3.3}$$

The polarisation in the ferroelectric P_f will depend on the electric field in the material E_f, but the dependence is highly non-linear, displays hysteresis, and depends on the frequency and maximum field. To utilise Equation 3.3, the relation $P_f(E_f)$ must therefore be obtained experimentally, ideally from a sample where there is no passive layer. If such a measurement can be obtained, Equation 3.3 can be used to simulate the effect of a passive layer described by the dimensionless parameter $\frac{d}{a\varepsilon_d}$, as shown in Equation 3.4, where all dependence on the electric field in the ferroelectric is on the right hand side.

$$E_{\text{average, simulated}} = E_f + \frac{P_f(E_f)}{\varepsilon_0} \frac{d}{a\varepsilon_d} \tag{3.4}$$

The model, and Equation 3.4, can be explained as follows: When cycling a stack with a passive layer between $\pm E_{\text{average,max}}$, the ferroelectric layer is actually cycled between $\pm E_{f,\text{max}}$ with $E_{f,\text{max}} < E_{\text{average,max}}$, because of the voltage drop caused by the passive layer. This means that the coercive field may not be reached completely throughout the film, and the maximum polarisation seen may be lower than without the presence of a passive layer. This will also cause some slanting. Moreover the x-axis displays E_{average} and not E_f, so when plotted, the PV loop appears stretched from $\pm E_{f,\text{max}}$ to $\pm E_{\text{average,max}}$, which gives more slanting. When equation 3.4 is used to simulate the effect of a passive layer, a sample is cycled between $\pm E_{\text{f,max}}$ of various values lower than the $E_{\text{average,max}}$ targeted. Then the loop is stretch from $\pm E_{f,\text{max}}$ to $\pm E_{\text{average,max}}$ according to Equation 3.4 with a value of $\frac{d}{a\varepsilon_d}$, found by Equation 3.5.

$$\frac{d}{a\varepsilon_d} = \varepsilon_0 \frac{E_{\text{average, simulated,max}} - E_{f,\text{max}}}{P_f(E_{f,\text{max}})} \tag{3.5}$$

Such simulations have previously been made by [29, 1], and an example can be seen in Figure 3.7. The dielectric layer leads to more slanted loops, and a decreased maximum polarisation. It can be seen that if the dielectric constant of the passive layer at the interface (ε_d) is small, even a layer several orders of magnitude thinner than the film will have an effect. If the relative permittivity ε_d is comparable to that of PZT ($\varepsilon_d \sim$600) the loops will be much less sensitive to the effect of an interface layer. For the legend in Figure 3.7, ε_d is set to 5. This value is chosen because it is shows the limiting case where even thin layers can cause detrimental effects of the PV loops. Higher values of ε_d may be more realistic, and in the case of $\varepsilon_d = 50$, the values for d in the legend would be 10 times as large.

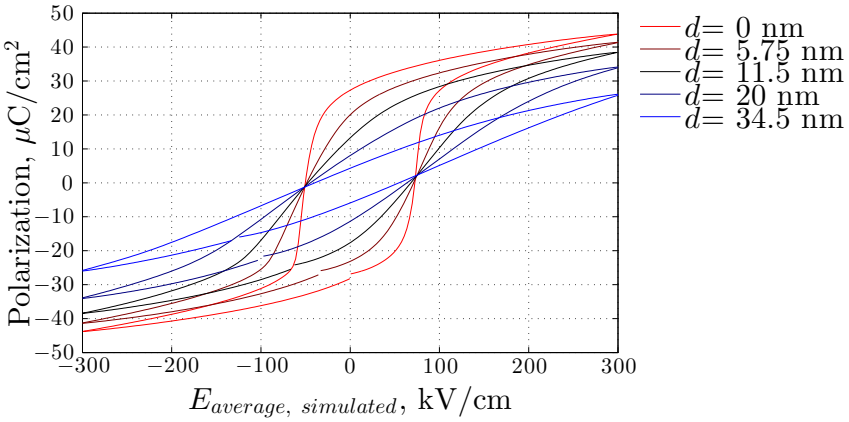


Figure 3.7: PV loops from tetragonal PZT with IDE electrodes. Simulations of the effect of different passive layers are shown[1]. The legend shows the corresponding thickness of the dielectric layer, d, if the electrode spacing a is 10 µm, and ε_d is set to 5.

3.2 e_{IDE} measurements

A measurement of e_{IDE} is the preferred technique for measuring the direct piezoelectric effect in samples with IDE structures. This can be realised by applying a force to the end of a sample, forcing it to bend, as shown in Figure 3.8(a). The thin PZT film on the top of the sample is then in compressive stress, and this causes a decrease in the polarization, releasing the compensating charge from the contacts.

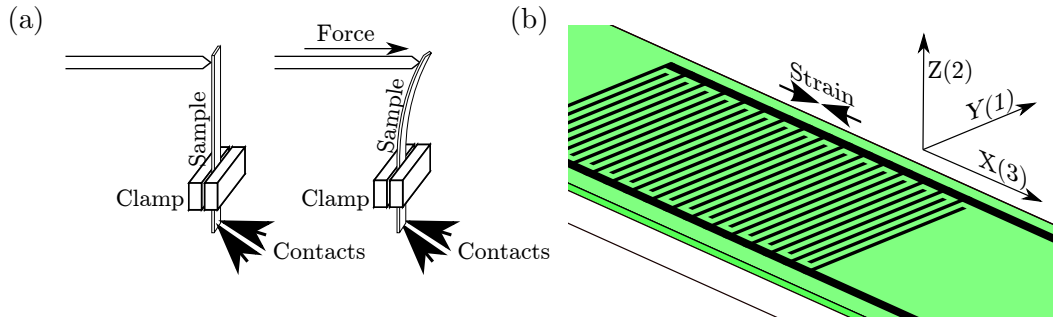


Figure 3.8: (a) Schematic drawing of a setup for $e_{31,\mathrm{IDE}}$ measurements[1]. (b) Coordinate system for a poled IDE structure, with the 3-axis between the electrodes. During measurement there is compressive stress of the PZT film in the X(3) direction.

3.2.1 Definition of e_{IDE}

e_{IDE} will be defined as the coupling between strain in the X(3) direction, and the D-field in the same direction. The coupling between the displacement field and strain can be found from Equation 2.5[30], using the coordinate system of Figure 3.8(b),

$$D_3 = e_{31}(\xi_1 + \xi_2) + e_{33}\xi_3 \tag{3.6}$$

As can be seen, this also depends on the strain in the other cardinal directions. Equations 3.7 describe how the different strains are coupled to stress[30].

$$T_1 = c_{11}^E \xi_1 + c_{12}^E \xi_2 + c_{13}^E \xi_3 \tag{3.7a}$$
$$T_2 = c_{12}^E \xi_1 + c_{11}^E \xi_2 + c_{13}^E \xi_3 = 0 \tag{3.7b}$$
$$T_3 = c_{13}^E (\xi_1 + \xi_2) + c_{33}^E \xi_3 \tag{3.7c}$$

where the stress out of the plane T_2 is zero.

The film is clamped to the substrate, which will expand in the Y(1) direction as the sample is bent[30]. The strain in this direction must follow the Poisson equation given below:

$$\xi_1 = -\nu_{\mathrm{Si}} \xi_3 \tag{3.8}$$

Where ν_{Si} is the Poisson ratio of the Si substrate. From Equation 3.6, 3.7b and 3.8 the electronic displacement field can be coupled to the strain along the X(3) direction, as shown in Equation 3.9. This relation can then be used to define e_{IDE}.

$$\begin{aligned} D_3 &= \Big(e_{31} \Big(\frac{\nu_{\mathrm{Si}} c_{12}^E - c_{31}^E}{c_{11}^E} - \nu_{\mathrm{Si}} \Big) + e_{33} \Big) \xi_3 \\ &= e_{\mathrm{IDE}} \xi_3 \end{aligned} \tag{3.9}$$

3.2.2 Measuring e_{IDE}

The definition in 3.9 can then be used to find the charge per area q_3 of a device:

$$q_3 = e_{\mathrm{IDE}} \xi_3 \tag{3.10}$$

By approximating the IDE sample as a series of parallel plate devices (shown in Figure 2.5), the total charge Q can be found by Equation 3.11:

$$\begin{aligned} Q &= \sum_{1}^{N} w t_f 2 e_{IDE} \xi_3 \\ &= N w t_f 2 e_{IDE} \bar{\xi_3} \end{aligned} \tag{3.11}$$

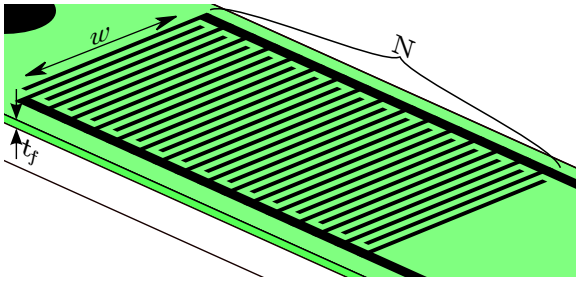


Figure 3.9: Dimensions used in equation 3.11.

In these equations, N is the number of fingers, w is the length of each finger where the field is present, and $\bar{\xi_3}$ is the average strain found by equation 3.12:
where l is the distance from the clamp to the tip applying force, h is the thickness of the cantilever, x_0 and x_1 are the distances from the clamp to the start and end of the finger structure and z_l is the displacement along the z-axis caused by the tip. Using Equation 3.11 and 3.12, e_{IDE} can be calculated based on the measured properties:

$$e_{\mathrm{IDE}} = \frac{l^3 Q}{3 N w t_f z_l h \Big(l - \frac{x_1 + x_0}{2} \Big)} \tag{3.13}$$

$$\bar{\xi_3} = \frac{1}{x_1 - x_0}\int_{x_0}^{x_1} \xi_3(x)dx = \frac{3z_l h}{2l^3}\left(l - \frac{x_1 + x_0}{2}\right) \quad (3.12)$$

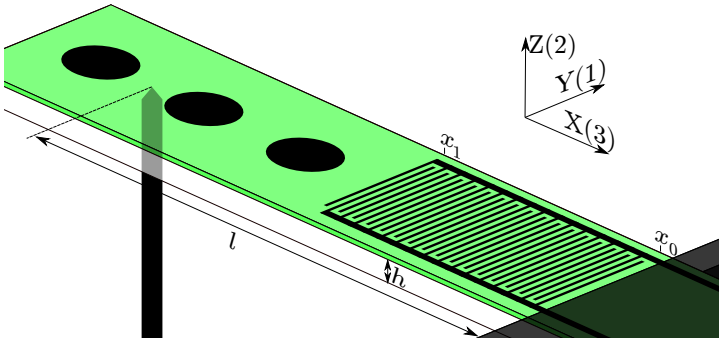


Figure 3.10: Dimensions used in equation 3.12.

3.2.3 Amount of Self-Poling

To interpret the results from self-poling, it is useful to consider how a partially poled sample is expected to behave. A schematic drawing of a partially self-poled sample measured in short-circuit mode is shown in Figure 3.11.

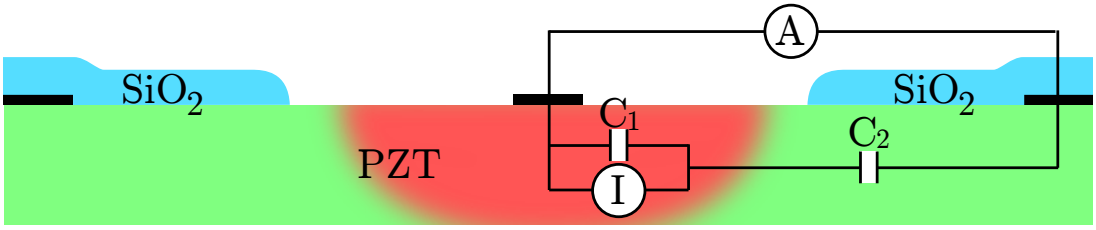


Figure 3.11: Schematic drawing of a PZT thin film with self-poled(red) and not-poled(green) regions. A circuit is drawn on the right side to show how the different regions will act when the film is deformed by a mechanical force.

By pushing the cantilever, the self-poled region acts as a current source (I) in parallel with a capacitor (C_1), and the not-poled region of the film will act as a capacitor (C_2). The charge Q_{tot} generated by the poled region will be distributed according to Equations 3.14 to 3.17

$$Q_{tot} = Q_1 - Q_2 \quad (3.14) \qquad Q_1 = C_1 V_{C_1} \quad (3.16)$$

$$0 = V_{C_1} + V_{C_2} \quad (3.15) \qquad Q_2 = C_2 V_{C_2} \quad (3.17)$$

In these equations, $C_1 = \varepsilon\frac{A}{d_1}$ and $C_2 = \varepsilon\frac{A}{a-d_1}$, where A is the area, d_1 is the extent of the self-poled region, ε is the dielectric constant of the PZT, assumed to be the same in both regions, and a is the electrode spacing.

The charge going through the amperemeter to C_2 is measured, and using Equations 3.14-3.17 the fraction of self-poling ($\frac{d_1}{a}$) can be calculated by Equation 3.18 if Q_{tot} is known.

$$\text{Fraction of self-poling} = \frac{d_1}{a} = \frac{Q_2}{Q_{tot}} \quad (3.18)$$

Q_{tot} can be found by measuring a poled sample where $d_1 = a$.

It would be expected that the region of self-poled PZT does not scale with the electrode spacing in partially self-poled samples. Because of this, the fraction of self-poled PZT would be seen to decrease with increasing electrode spacing.

Additional complications arise in as-fabricated samples, where there may be a passive layer surrounding the electrode caused by damage during sputtering. Such a layer can be seen as an increase of d_2, but may in reality also show a different dielectric constant. To get an accurate measurement of Q_{tot}, the film should therefore be annealed prior to poling, so that all damage from sputtering can be cured. The presence of a passive layer therefore limits the maximum amount of self-poling in as-fabricated films.

Chapter 4

Fabrication

Fabrication of the PZT in this work followed the process developed by F. Calame [31]. This was followed by additional processing needed for the electrodes and SiO_2 cover. Fabrication of the electrodes was based on the work by N. Chidambaram [32]. The fabrication route of the SiO_2 cover was developed for this work. Samples were made on a per-wafer basis, where each wafer was composed of about 180 samples.

The samples had the general design with IDEs as shown in the Introduction chapter. The extent of SiO_2 coverage in the samples was varied, and the masks therefore contained two different designs (H and F), as shown in Figure 4.1. In addition, a wafer containing control samples with no SiO_2 cover was fabricated (N)[1]. H samples occupied the left side of the wafer, while F samples occupied the right side of the wafer. In the design H, the SiO_2 covered one set of electrodes and half the gap between the electrodes, while in design F, the SiO_2 covered one set of electrodes and all of the gap between the electrodes, leaving only a small gap of uncovered PZT next to the uncovered electrode. The samples were designed with varying electrode spacings (4-20 μm), and widths ($2 - 5\mu m$).

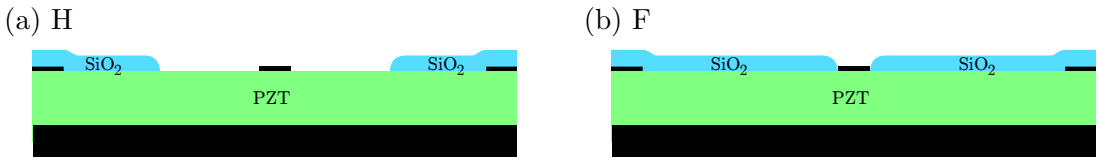


Figure 4.1: Schematic cut-out of PZT thin film with partial SiO_2 cover. (a) design H (Half). (b) design F (Full). Samples from the control wafer are designated N (none).

The following section describes the process flow by following a cross section from the IDE structure of a sample with the F design.

4.1 PZT processing

The PZT thin film was fabricated by sol-gel processing, and the process flow is shown in Figure 4.2.[2]

[1] This wafer was fabricated by Robin Nigon, and also serves as the control wafer for research he is conducting.

[2] Precursor synthesises and spin-coating was done by Ph.D student Robin Nigon. Since the synthesis and spin-coating of PZT involve hazardous chemicals, and the quality of the produced films have previously been unreliable, it was decided that a single operator would spin-coat all films. A total of 6 wafers were made this semester, all involved in various research, but only results from 2 wafers are shown here. Nevertheless, it has been useful for the researchers to be able to compare samples from all 6 wafers.

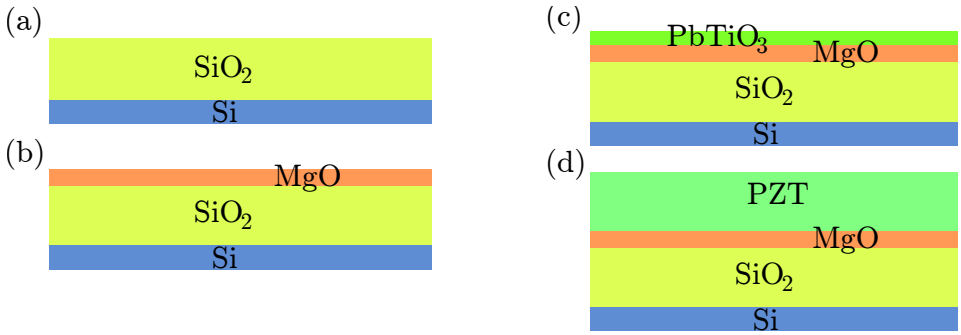


Figure 4.2: Process flow for PZT fabrication.

Figure 4.2(a) shows a 2 µm thick SiO_2 layer grown on a Si wafer to provide an insulating substrate. Following this, a 100 nm layer of MgO was evaporated onto the surface to provide good adhesion and oriented growth for the following layers (Figure 4.2(b)). A `Leybold Optics LAB 600H` e-beam evaporator was used for this deposition.

A layer of $PbTiO_3$ precursor was spin-coated and crystallised to provide a seed layer for the PZT (c). The sol-gel solution is fabricated following the process presented in [33]. The PZT layer was deposited by spin-coating a series of 60 nm thick layers (between 1 and 2 ml of solution), each with a slightly different composition, so that the PZT layer became gradient-free after crystallisation at 650 °C[31]. A total of 8 layers were needed to provide approximately 500 nm of PZT, and the film was crystallised after every 4 layers (d). Previous studies have shown that the $PbTiO_3$ layer merges with the PZT during this process.

4.2 Electrode and SiO_2 Processing

It is known from previous research in the same lab [32] that lift-off is a very suitable technique for depositing and patterning Pt onto PZT. No accounts of deposition and patterning of SiO_2 onto PZT have been found, and a suitable process flow for this was therefore developed as part of this work. A series of tests were made to determine the most suitable process flow, and the results from these tests are included in Appendix A and B. The process flow chosen to fabricate the samples is shown in Figure 4.3.

The process flow started with coating of a two-layer photoresist, as seen in Figure 4.3(a). This was done using an `EVG150` automatic coater and developer. The top layer was a 1.6 µm thick layer of photosensitive image resist (AZ1512 from MicroChem), while the bottom layer was a 700 nm thick lift-off resist (LOR5A from MicroChemicals) designed to aid the lift off process.

Exposure of the image resist was done using a `Süss MA6/BA6` double side mask aligner and bond aligner, see Figure 4.3(b). It is equipped with a mercury source, but no filter, providing exposure with multiple wavelengths. The mask was made using a `Heidelberg VPG200` photoresist laser writer, and the mask for a single sample is shown in Figure 4.4.

Development was done using the `EVG150`. Development dissolved the image resist where it had been exposed, and also dissolved the LOR. By controlling the time the wafer was exposed to the developer, the amount of dissolved LOR was controlled. It is beneficial that the LOR has a wider gap than the image resist (Figure 4.3(c)), to aid lift-off.

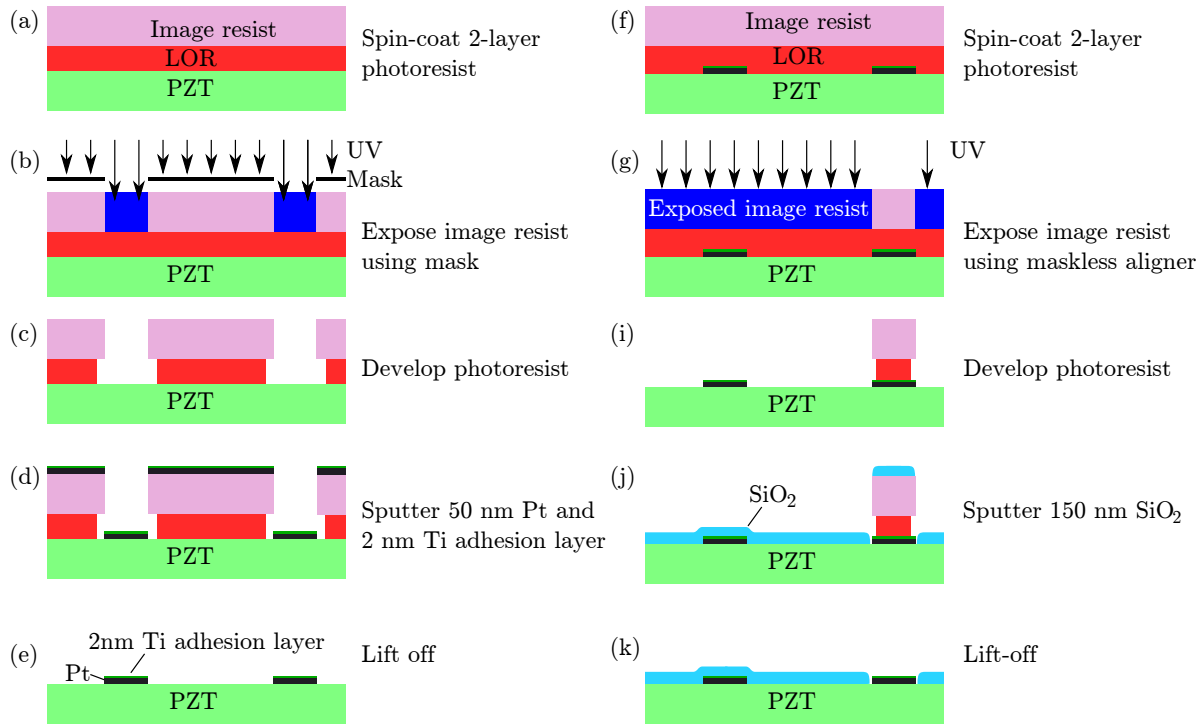


Figure 4.3: Process flow for fabrication of electrodes and SiO_2 cover, see the text for explanation.

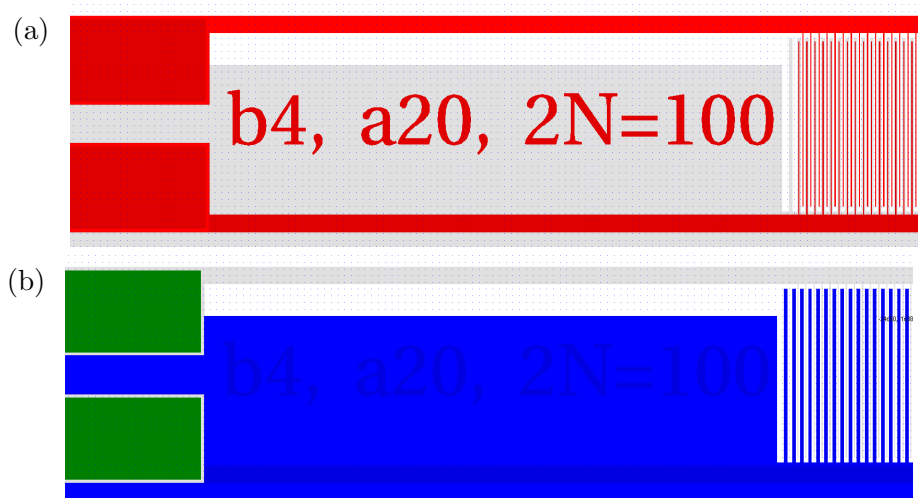


Figure 4.4: (a) Cut-out of mask design for Pt deposition of a single sample, designated 'b4a20'. (b) Cutout of mask design for SiO_2 deposition (blue), and opening of the contact pads (green). All masks are made using the `Expert` software provided by `Silvaco`.

50 nm Pt and 2 nm Ti was sputtered through the gaps in the photoresist to provide electrodes. An `Alliance-Concept DP 650` was used for the sputtering. The titanium acts as an adhesion layer between the Pt and SiO_2, since it is known from tests that SiO_2 sputtered directly on Pt de-laminates. The tool was equipped with a shutter, so that the plasma was ignited before deposition began, and this allowed for precise control of film thickness.

Lift-off was done by placing the wafer in a bath of `MICROPOSIT Remover 1165` photoresist remover overnight, and rubbing the wafer in an acetone bath to remove any remnants of the photoresist (Figure 4.3(e)).

Fabrication of the SiO_2 cover started with a new coating of photoresist, Figure 4.3(f). This was exposed in an `Heidelberg MLA 150` prototype maskless aligner, with the mask design shown in blue in Figure 4.4(b). The working principle of this tool is shown in Figure 4.5.

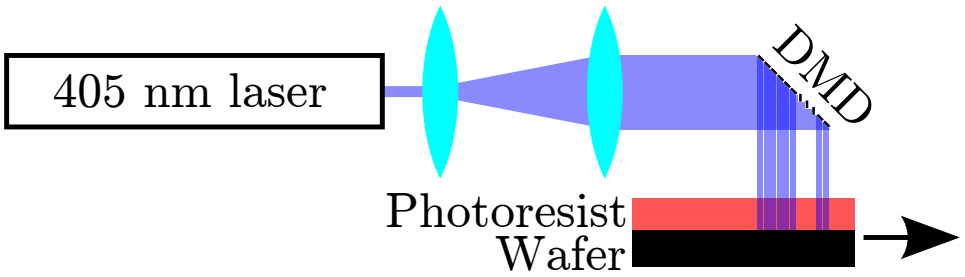


Figure 4.5: Working principle of the `Heidelberg maskless aligner`. A 405 nm laser illuminates a Digital micromirror device (DMD). By rotating the individual micromirrors, illumination on the selected pixel is turned on or off. Each pixel is 1×1 µm on the wafer. To expose the entire surface, the wafer is moved under the DMD, while the wafer is exposed in pulses at set intervals.

The same development procedure was repeated to develop the photoresist (Figure 4.3(i)). 150 nm SiO_2 was sputtered in a `Pfeiffer SPIDER 600` RF magnetron sputterer at room temperature (Figure 4.3(j)). The `SPIDER` was not equipped with a shutter, and there was a 30s ramp time until the plasma stabilised. Total deposition time was 12 minutes, 51 seconds. To increase the density of the SiO_2, a small oxygen flow (1 sccm) was directed into the chamber during deposition.

Lift-off for the SiO_2 (Figure 4.3(k)) was performed in the same way as for the Pt (Figure 4.3(e)). However, SiO_2 did not lift off very well from large surfaces, such as the contact pads. The reason was assumed to be that the SiO_2 film did not break off after the photoresist was removed but instead blocked the flow of remover to the photoresist inside the bath.

4.3 Opening the Contact Pads

An image of the contact pads after lift-off is shown in Figure 4.6(a). It can be seen that the contact pads are still partially covered with photoresist, and cannot be connected.

Additional processing was required to open the contact pads, with the process steps shown in Figure 4.7(b-e). New layers of photoresist were spin-coated in the same way as described previously, and patterned using the `Heidelberg MLA`.[3] The mask design is shown in green in Figure 4.4(b). An `SPTS APS` dry etcher with fluoride chemistry was used to etch the excess SiO_2. Octafluorocyclobutane (C_4F_8) in mixture with He was used as the etching gas. The process had little or no effect on any uncovered Pt, but would have etched any uncovered PZT. The mask was therefore designed so that only the contact pads were exposed to the etchant. The process

[3]The cover image of this thesis was taken at the step shown in Figure 4.7(c), where the NTNU logo has been made by exposing and developing the photoresist on top of the SiO_2 on top of a buried layer of photoresist. The image is located in the bottom right PFM group shown in Figure 4.8(b). The wavy pattern seen inside the logo comes from the SiO_2 buckling on top of the buried photoresist.

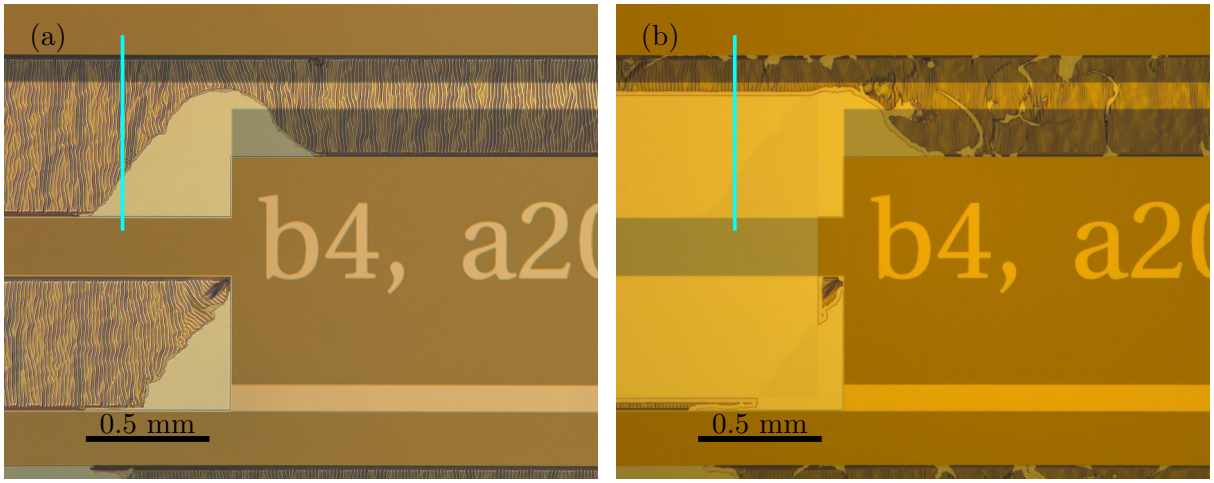


Figure 4.6: (a) After the processing shown in Figure 4.3(k), the photoresist and SiO_2 have not lifted off at the contact pads. (b) After additional processing, shown in Figure 4.7 for the cross section indicated in light blue, the contact pads are opened, so that they can be connected. Photoresist and SiO_2 still remain surrounding the contact pad and at the branch leading to the IDE structure. It should be noted that these micrographs are taken from a test wafer, but the process is the same and the images are therefore representative.

can burn the photoresist, making removal difficult, and a short oxygen plasma (in a `Tepla 300` dry etcher) was used to strip the burnt resist. The wafer was then placed in remover to eliminate the remaining resist.

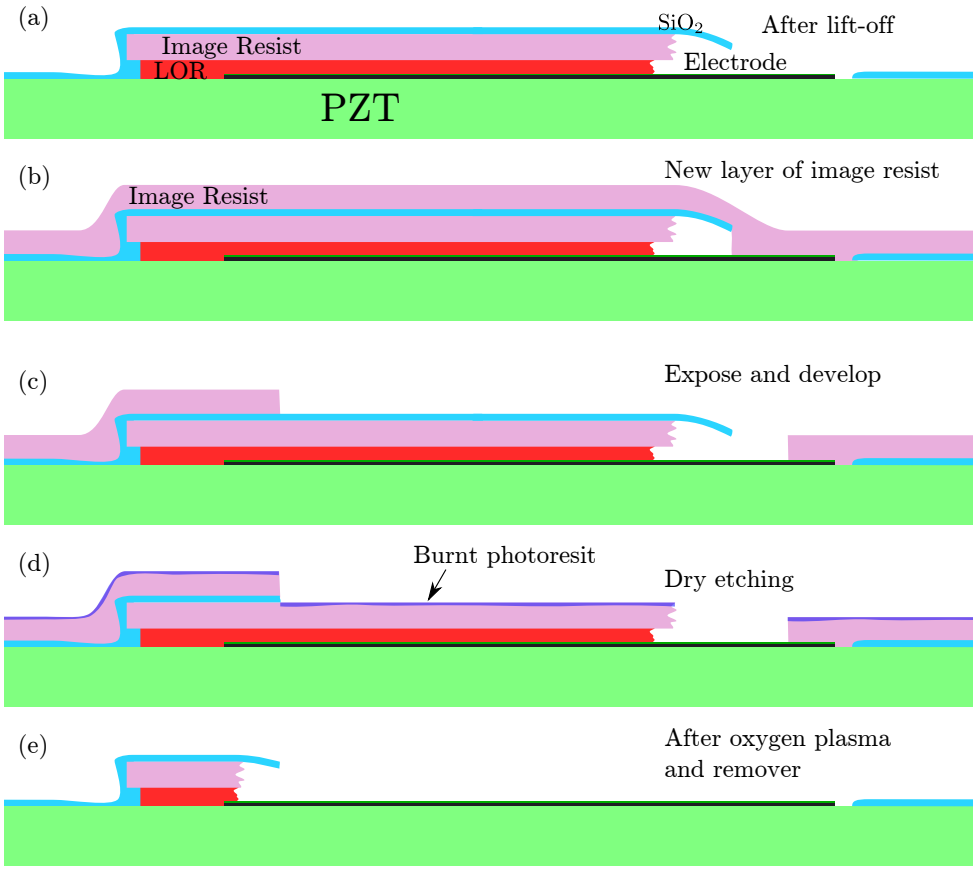


Figure 4.7: Process flow for opening of contact pads, see text for explanation.

The finished wafer was then diced using a `Disco DAD321` automatic dicing saw. At this point the wafer was split into 186 individual samples.[4] The full masks used with all samples are shown in Figure 4.8.

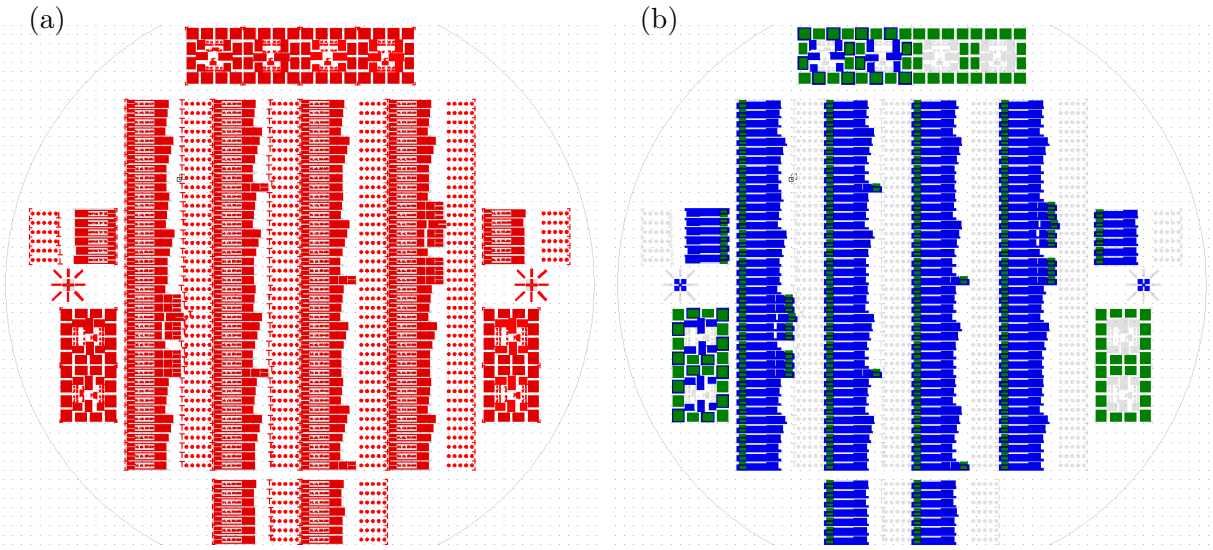
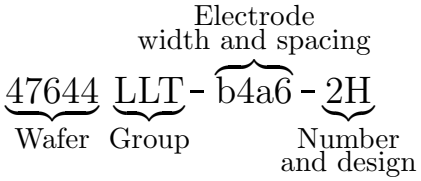


Figure 4.8: (a) Mask design for Pt deposition. (b) Mask design for SiO_2 deposition (blue), and opening of the contact pads (green).

4.4 Sample Names

Finally, all samples were named using the following naming scheme, illustrated here by an example:



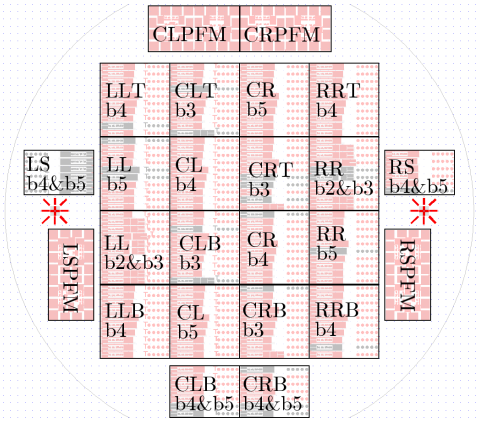


Figure 4.9: Map of the groups as designed on the wafer.

The wafer number is etched into the wafer before fabrication begins. Wafer 47644 was made with partial SiO_2 cover, and wafer 47643 was the control wafer. The wafer numbers are often shortened to just 44 and 43. The group is designated according according to the map in Figure 4.9. The designed electrode width and spacing are included in the sample name with unit µm.

[4]The wafer also contained 8 groups designed to be used for piezoelectric force measurements (PFM), but no PFM measurements were carried out as part of this work.

When there are more than one sample with the same dimensions in the same group, the number is used to differentiate them. The design is included at the end, but it should be noted that the left side of the wafer contains samples of the H design, while the right side contains the samples of F design. In this way, the group name also encodes the design.

27 samples are coloured black in Figure 4.9. These samples are known from micrographs to be defective. Coincidently, the sample 47644LLT-b4a6-3H used as an example here is the black sample to the top left in the figure. It was also found that all samples 'a4', were short circuited, and could not be used.

From the working samples, 1067 PV loops and numerous e_{IDE} measurements were obtained[5]. All PV loops have been plotted and considered, but only a subset is included in the results. They have been chosen because they are seen as representative for the entire set.

[5]433 CV loops were also captured, but they have not been presented here as the details of these plots are not needed to evaluate the theories discussed herein.

Chapter 5

Results and Discussion

This chapter will describe results from fabrication, theoretical work, and experimental results. The experiential results are grouped according to the effect discussed, such as self-poling, ageing, etcetera. Each section is accompanied by a small discussion, where the results on that topic are evaluated. This is done so that it becomes easier for the reader to follow.

5.1 Results from Fabrication

5.1.1 PZT characterisation

To check that the PZT film was fully perovskite phase, and assess the out-of-plane orientation of the film, XRD patterns were recorded. This was done before the Pt and SiO_2 was deposited. XRD pattern from the wafer used for samples with partial SiO_2 cover, as well as the wafer used for control samples are shown in Figure 5.1.

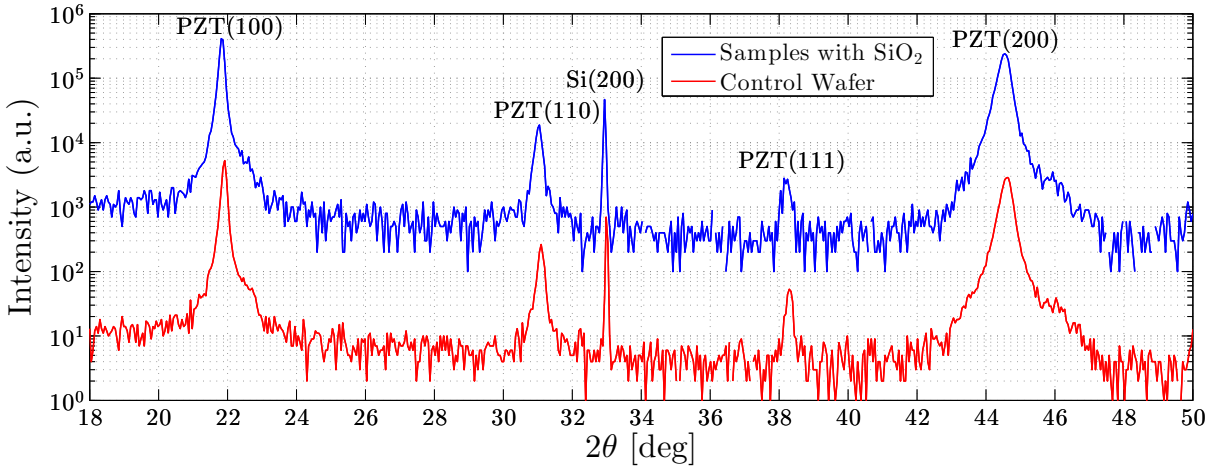


Figure 5.1: XRD patterns from the two wafers. The PZT(100) peaks can be seen to be much higher than the (110) and (111) peaks, indicating high (100) orientation. The Si(200) peak from the substrate can also be seen.

The diffractograms in Figure 5.1 show that the diffraction peaks for (100) orientation are more than one order of magnitude higher than the peaks for (110) and (111) orientation, indicating that the wafers are mostly (100) oriented.

The intensity of various peaks in samples with random distribution is known from powder diffraction measurements (ICDD database[34]). By using these data, combined with the results above, one can calculate that the wafer with SiO_2 cover is 93.8 % (100) oriented, 4.9 % (110) oriented, and 1.3 % (111) oriented. Corresponding values for the control wafer are 92.8 %, 5.4 % and 1.8% respectively. The PZT peaks are broadened by small grain size, and possibly by non-uniform

stress in the film as different domains form in different directions.

Before fabrication of electrodes, the films were inspected by SEM and AFM. The different wafers have different PZT thickness, but otherwise the films appear similar. For this reason, no images of the control wafer are included here. SEM images of the top surface can be seen in Figure 5.2.

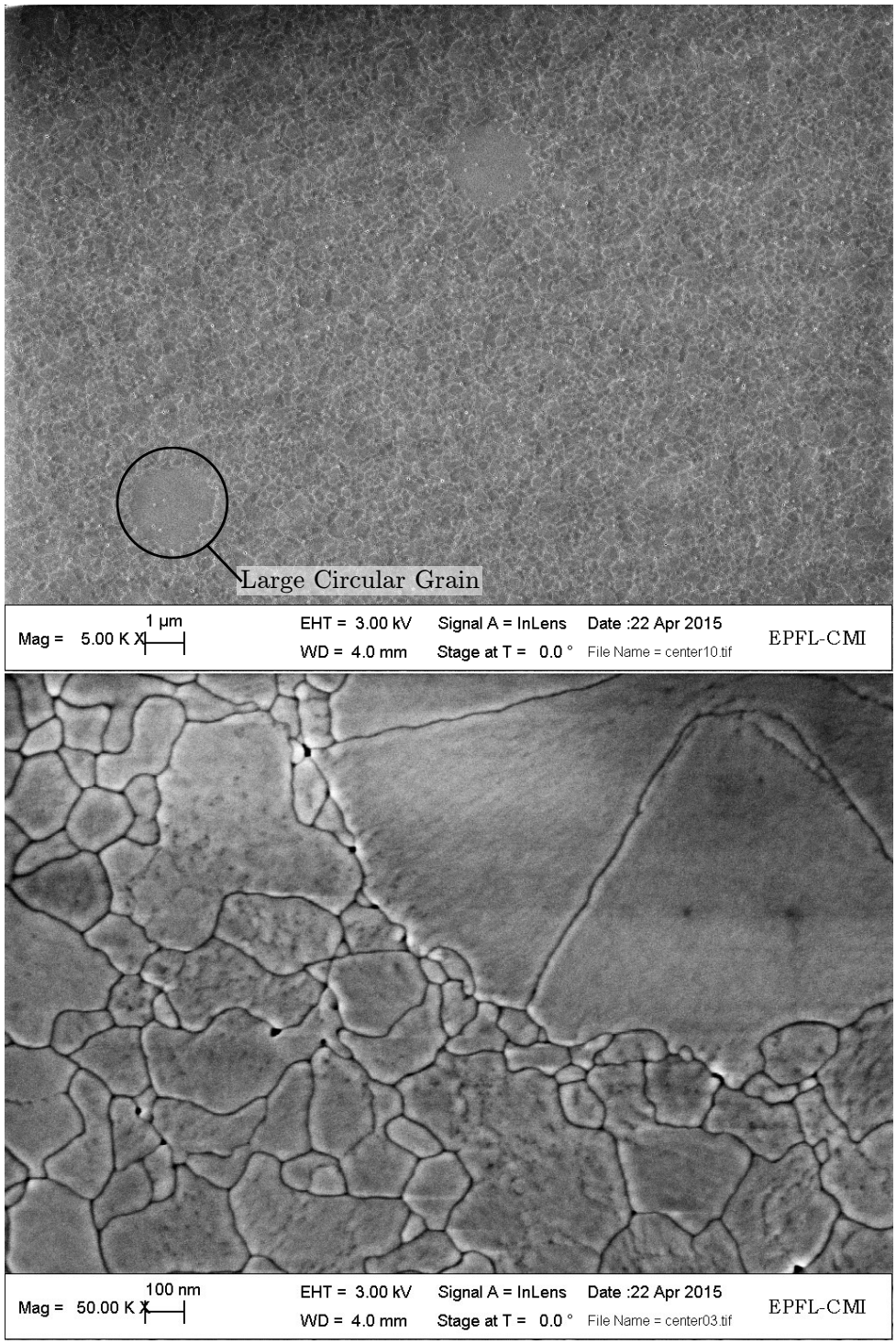


Figure 5.2: SEM images of PZT film showing grain structure at the surface. (a) Using low magnification it can be seen that the majority of the film consists of small grains, with some larger circular grains interspersed. (b) High resolution SEM image reveals the shape of the grains. Faint lines structures can be seen on some some grains, and these are believed to be caused by ferroelectric domains.

Figure 5.2(b) shows that the film mainly consists of grains with diameter 50 to 300 nm, with some large circular grains interdispersed. These large grains are in about 1 µm in diameter, and are known from previous studies by Nachiappan Chidambaram to be Ti-rich compared to the rest of the film[1]. It is believed that these large grains are ferroelectric because the faint lines seen in the SEM images have spacing and periodicity consistent with ferroelectric domain walls. This is also supported by the fact that there is no parasitic non-ferroelectric phase seen in the XRD pattern.With no measurement techniques available to discern the properties of the small versus large grains, the films are for the purpose of this work treated as if they have a homogeneous grain structure.

After cleaving the samples, SEM images of the cross sections were captured. They reveal the columnar nature of the grains, and have been used to measure the film thickness. A SEM image of a cross section is shown in Figure 5.3. The film was found to be 546 ± 6.5 nm thick based on 7 measurements.

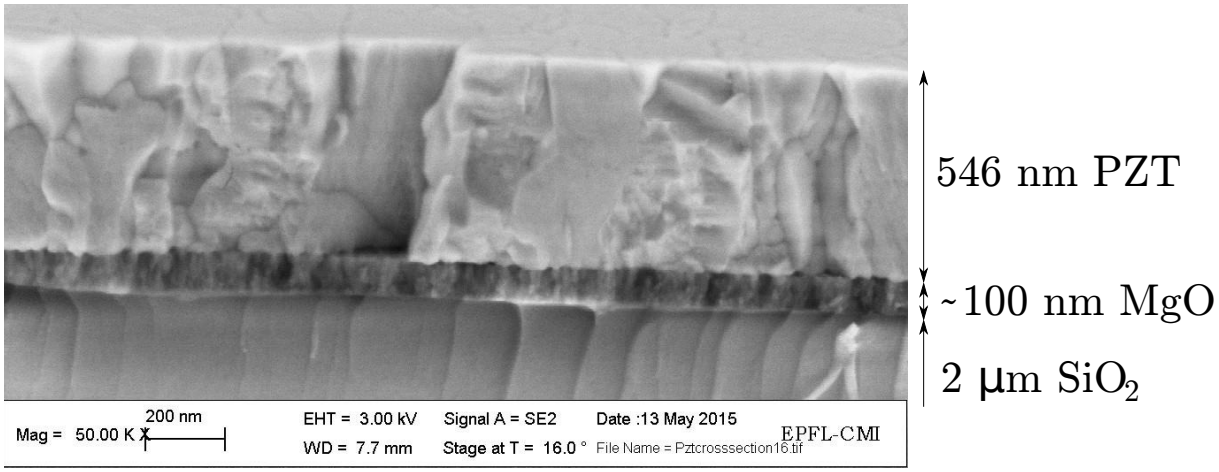


Figure 5.3: SEM image from a cross section of the PZT film. This image has been used in combination with other SEM images to determine the thickness of the PZT film. The cleavage pattern indicates that the PZT structure is mainly columnar.

AFM scans were also taken of the PZT film. One such scan is shown in Figure 5.4. These scans reveal the same basic grain structure as the SEM images, but also show topography differences between the grains. This difference may be due to different domain distribution in the grains. The AFM scans estimate the root mean square surface roughness to be about 1.91 nm.

5.2 Electrode and SiO_2 Cover Characterisation

After depositing the Pt and SiO_2, all samples were imaged at low and high resolution in an optical microscope in the cleanroom. This was done before the wafer was diced. Examples of such micrographs are shown in Figure 5.5.

The photoresist and SiO_2 seen to cover the top branch in Figure 5.5(a) is expected to have no impact on the electrical or mechanical properties of the device. This is because it is only

[1]From personal correspondence, not published.

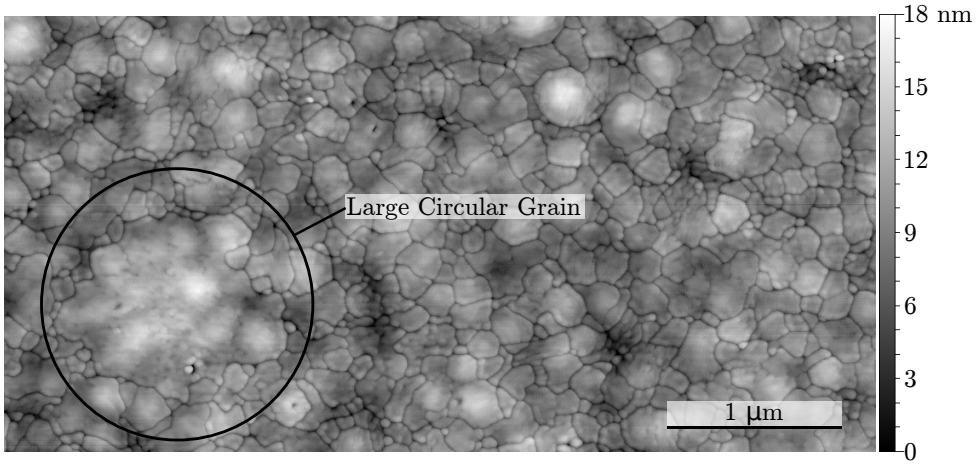


Figure 5.4: AFM scan of the PZT film, showing the grain structure. Some grains appear to have an upwards bulge, as evident by the lighter color. This could be due to different domain orientations (and orientation of the c-axis) in different grains. Artefacts have been removed from the scan using the software package `Gwyddion`.

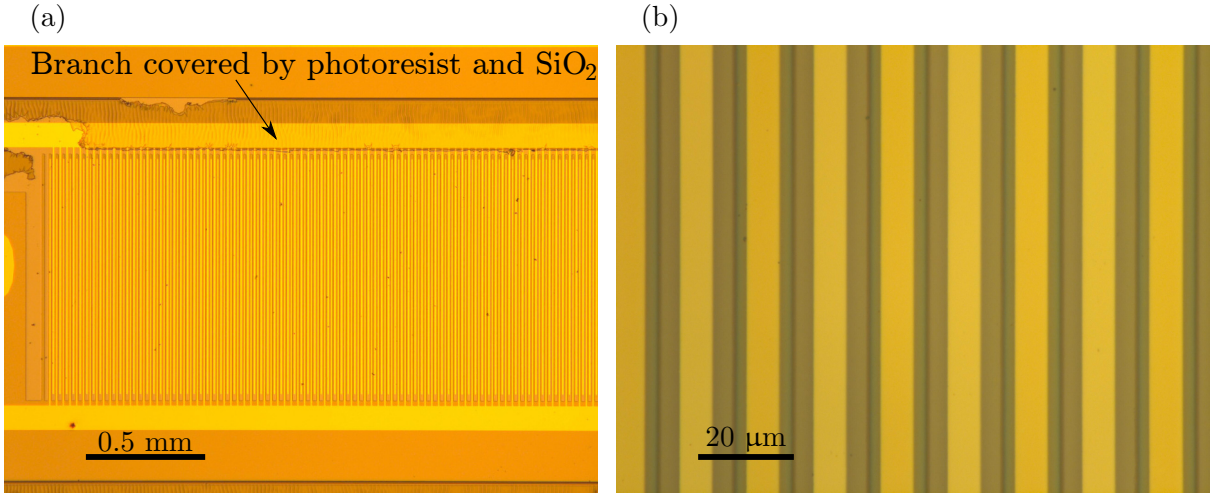


Figure 5.5: Micrographs of sample LLB-b4a10H, where H indicates the sample design. The periodicity of the structure is 28 µm. (a) low magnification, (b) high magnification. Photoresist still covered in SiO_2 that has not been removed during fabrication can be seen on the upper branch in (a).

in contact with one electrode, so no potential difference develops across this layer during device operation. However, during annealing at high temperature, the photoresist will crack, and easily delaminate if scratched. When the photoresist delaminated after annealing, it was observed that the Pt branch would often delaminate together with it. This is especially a problem when mounting and removing samples from the e_{IDE} setup, where the sample is clamped at the branches, and is easily scratched.

The low magnification images were used to identify any errors made during photolithography, while the high magnification images were used to measure the width of the electrodes and the extent of the SiO_2 cover. All electrode fingers were approximately 3± 0.3µm wider than the mask design, so that a sample designed to have electrodes 4 µm wide would in fact have electrodes about 4+3=7 µm wide. This is thought to be be the reason why all samples 'a4' to were short-circuited. The script developed for [1] was used to automatically measure the electrode spacing from the images using `Matlab`. The details of this script is reproduced in Appendix D.

The SiO_2 cover was generally in agreement with the design, but showed about 1 µm too little cover on one side. This is of minor importance for most samples, but becomes important for small gaps. The smallest gaps in the design are about 3 µm, and a 1 µm deviation becomes important in this case. The micrographs showing this can be seen in Figure 5.6.

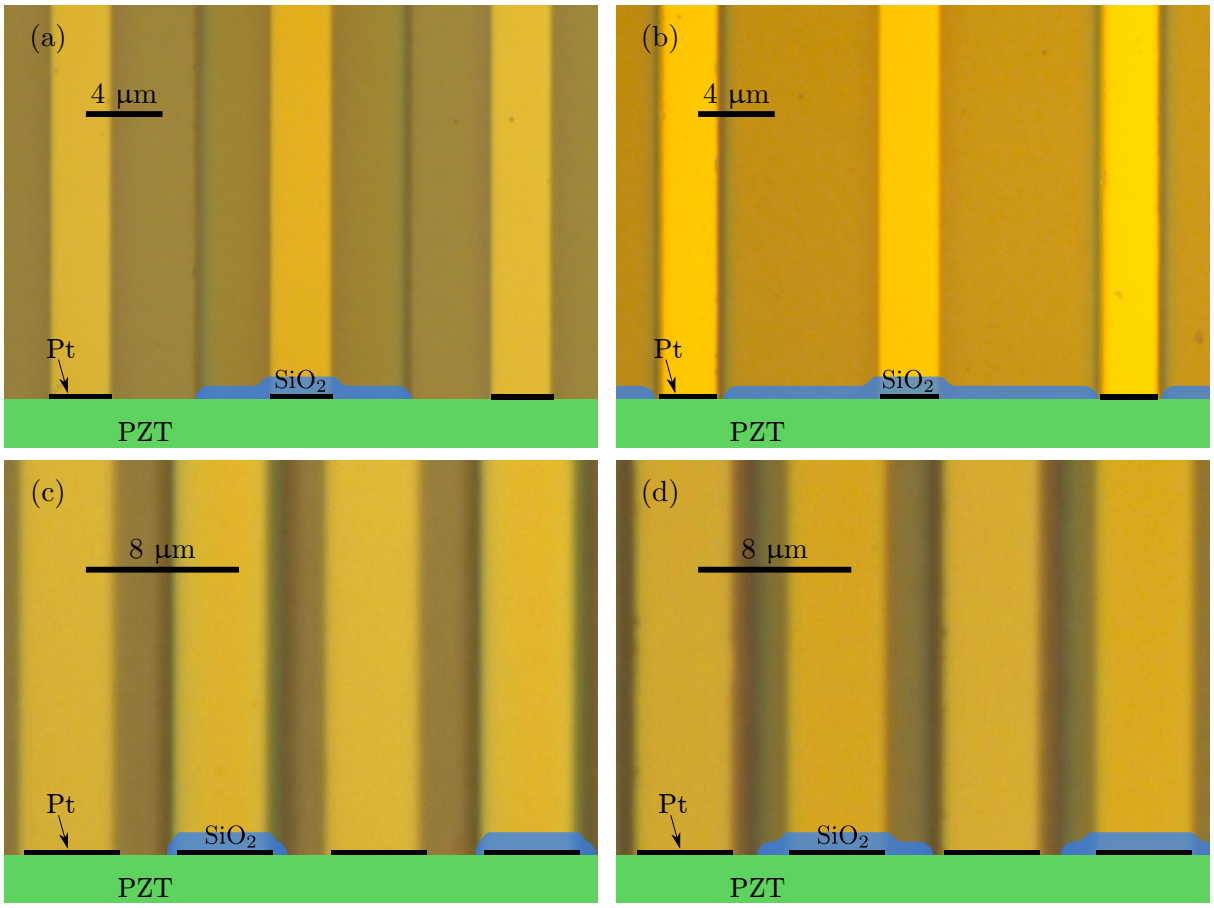


Figure 5.6: Micrographs of samples (a) b3a20H, (b) b3a20F, (c) b2a6H and (d) b2a6F. See Section 4.4 for a description of how samples are named. The width of the electrodes, b, are 6 µm in (a) and (b), and 5 µm in (c) and (d). The gaps between the electrodes, a, are 17 µm in (a) and (b), and 3 µm in (c) and (d). Note the different scale bars for (a) and (b), and (c) and (d). The low gap samples, (c) and (d), can be seen to have significantly smaller SiO_2 cover than designed. The wide gap samples, (a) and (b), also have lower SiO_2 cover than designed but due to the wider electrode spacing and lower magnification in the images it can not clearly be seen.

5.3 Simplification of the Gevorgian Model and Effective Field

The Gevorgian model is mathematically complicated due to the inclusion of elliptical integrals and hyperbolic functions. However, the model is in this work only used in the limit $b > 6t_f$ and $a > 3t_f$ (see Figure 2.5), and the Gevorgian model can be greatly simplified in this region. This limit is common for research: several studies have been carried out on IDE structures with $b > 6t_f$ and $a > 3t_f$ [5, 6, 7, 1, 32], while the author could not find any studies on ferroelectric samples outside of this limit.

The aim of this simplification is to find find a simple expression where the dependence on

electrode spacing a and electrode width b is clear. Comparing such an expression to the simple model may also give further insight into the Gevorgian model, and the IDE structure in general.

5.3.1 Simplification of k

In order to simplify Equation 2.9c, it is useful to define $A = e^{\frac{-\pi a}{4t}}$ and $B = e^{\frac{-\pi b}{4t}}$. This is done so that a Taylor expansion can be made of Equation 2.9c with respect to first B and then A. Both A and B will be small in the limit $b > 6t_f$ and $a > 3t_f$, so that the Taylor series can be truncated at a given order to obtain a good approximation of the expression. The hyperbolic functions used in Equation 2.9c can be expressed in terms of A and B as follows:

$$\sinh\left(\frac{\pi b}{4t}\right) = \frac{B^{-1} - B}{2} \tag{5.1a}$$

$$\cosh\left(\frac{\pi b}{4t}\right) = \frac{B^{-1} + B}{2} \tag{5.1c}$$

$$\sinh\left(\frac{\pi(a+b)}{4t}\right) = \frac{A^{-1}B^{-1} - AB}{2} \tag{5.1b}$$

$$\cosh\left(\frac{\pi(a+b)}{4t}\right) = \frac{A^{-1}B^{-1} - AB}{2} \tag{5.1d}$$

Inserting Equation 5.1a-d into Equation 2.9c, gives the following expression.

$$k = \frac{\sinh\left(\frac{\pi b}{4t}\right)}{\sinh\left(\frac{\pi(a+b)}{4t}\right)} \sqrt{\frac{\cosh^2\left(\frac{\pi(a+b)}{4t}\right) + \sinh^2\left(\frac{\pi(a+b)}{4t}\right)}{\cosh^2\left(\frac{\pi b}{4t}\right) + \sinh^2\left(\frac{\pi(a+b)}{4t}\right)}} \tag{5.2a}$$

$$= \frac{B^{-1} - B}{A^{-1}B^{-1} - AB} \sqrt{\frac{(A^{-1}B^{-1} + AB)^2 + (A^{-1}B^{-1} - AB)^2}{(B^{-1} + B)^2 + (A^{-1}B^{-1} - AB)^2}} \tag{5.2b}$$

$$= A \frac{1 - B^2}{1 - A^2B^2} \sqrt{\frac{(1 + A^2B^2)^2 + (1 - A^2B^2)^2}{A^2(1 + B^2)^2 + (1 - A^2B^2)^2}} \tag{5.2c}$$

$$= \sqrt{2} A \frac{1 - B^2}{1 - A^2B^2} \sqrt{\frac{1 + A^4B^4}{1 + A^2 + A^2B^4 + A^4B^4}} \tag{5.2d}$$

A Taylor series of Equation 5.2d on B is shown in Equation 5.3. The colors in Equation 5.2d and 5.3 indicate what Taylor series in 5.3 corresponds to what part of Equation 5.2d [35,35,36].

$$\begin{aligned} k = &\sqrt{2} A (1 - B^2) \\ &\left(1 - A^2B^2 + A^4B^4 + o(B^5)\right) \\ &\left(1 + \frac{A^4B^4}{2} + o(B^5)\right) \\ &\left(\frac{1}{\sqrt{1 + A^2}} + \frac{A^2B^4}{2\sqrt{1 + A^2}} + o(B^5)\right) \end{aligned} \tag{5.3}$$

Where $o(B^5)$ signifies terms in the Taylor series of order B^6 and higher[2]. Simplifying to first order in B, Equation 5.3 becomes 5.4.

[2]little-o notation is used here, more information on little-o notation can be found in [37]

$$k = \frac{\sqrt{2}A}{\sqrt{1+A^2}} \tag{5.4}$$

It can be seen that there is no longer a dependence on B. This is because there are only second order and higher dependences on B in 5.3. This means that with this simplification, the Gevorgian model no longer depends on the electrode width b. Further simplifications can be done by expanding Equation 5.4 as a Taylor series on A as follows:

$$k = \sqrt{2}A\Big(1 - \frac{A^2}{2} + \frac{A^4}{2} + o(A^5)\Big) \tag{5.5}$$

Where $o(A^5)$ signifies terms in the Taylor series of order A^6 and higher that have been omitted. A first order approximation of 5.5 on A can then be found:

$$k = \sqrt{2}A \tag{5.6a}$$
$$= \sqrt{2}e^{\frac{-\pi a}{4t}} \tag{5.6b}$$

5.3.2 Simplification of $\frac{K(k)}{K'(k)}$ and α

The fraction $\frac{K(k)}{K'(k)}$ will be simplified in a manner similar to k. That is by expanding $K(k)$ and $K'(k)$ to Taylor series before expressing the fraction $\frac{K(k)}{K'(k)}$ in terms of A, and reduced to first order.

In the limit $a > 3t_f$, it can be seen from Equation 5.6 that k is less than 1/2. For this limit, Taylor series for K(k) and K'(k) can be found in [38], reproduced here as Equation 5.7b and 5.8b.

$$K(k) = \int_0^1 \frac{\mathrm{d}t}{\sqrt{(1-t^2)(1-k^2t^2)}} \tag{5.7a}$$
$$= \frac{\pi}{2}(1 + \frac{1}{4}k^2 + \frac{9}{64}k^4 + o(k^5)) \tag{5.7b}$$

$$K'(k) = \int_0^1 \frac{\mathrm{d}t}{\sqrt{(1-t^2)(1-(1-k)^2t^2)}} \tag{5.8a}$$
$$= \log\Big(\frac{4}{k}\Big)\Big(1 + \frac{k^2}{4} + \frac{9}{64}k^4 + o(k^5)\Big) - \Big(\frac{k^2}{4} + \frac{21}{128}k^4 + o(k^5)\Big) \tag{5.8b}$$

Interestingly, one can express $K'(k)$ using $K(k)$, as follows:

$$K(k') = \frac{2}{\pi}\log\Big(\frac{4}{k}\Big)K(k) - \Big(\frac{k^2}{4} + \frac{21}{128}k^4 + o(k^5)\Big) \tag{5.9}$$

Using Equation 5.7b and 5.9, one can then write $\frac{K'(k)}{K(k)}$ as follows:

$$\frac{K(k')}{K(k)} = \frac{2}{\pi}\log\Big(\frac{4}{k}\Big) - \frac{k^2}{\pi/2}\frac{\frac{1}{4} + \frac{21}{128}k^2 + ...}{1 + \frac{1}{4}k^2 + \frac{9}{64}k^4 + ...} \tag{5.10}$$

As $k < 1/2$, the last term in Equation 5.10 has a finite limit of order k^2 when k goes to 0:

$$\frac{K(k')}{K(k)} = \frac{2}{\pi}\log\Big(\frac{4}{k}\Big) + o(k) \tag{5.11}$$

Inserting equation 5.6a, into 5.11 and simplifying gives the following expression:

$$\frac{K(k')}{K(k)} = \frac{2}{\pi}\log(2\sqrt{2}) - \frac{2}{\pi}\log(A) + o(A) \tag{5.12}$$

As done in Section 5.3.1, one can then do a first order approximation on A.

$$\frac{K(k')}{K(k)} = \frac{2}{\pi}\log(2\sqrt{2}) - \frac{2}{\pi}\log(A) \tag{5.13}$$

Inserting $A = e^{\frac{-\pi a}{4t_f}}$ into 5.13 allows for further simplifications:

$$\frac{K(k')}{K(k)} = \frac{1}{2t_f}\Big(\frac{4t_f}{\pi}\log(2\sqrt{2}) + a\Big) \tag{5.14a}$$

$$= \frac{1}{2t_f}\Big(a + \Delta a\Big) \tag{5.14b}$$

Where $\Delta a = \frac{4t_f}{\pi}\log(2\sqrt{2})$. Inserting Equation 5.14b into Equation 2.9a gives Equation 5.15 describing the capacitance of the structure:

$$C_{\text{Gevorgian, Approximation}} = \frac{\varepsilon t_f}{a + \Delta a} \tag{5.15}$$

And the Equation 5.16 for α form Equation 2.10b:

$$\alpha_{\text{Approximation}} = \frac{a + \Delta a}{a} \tag{5.16}$$

Equation 5.15 deserves some emphasis, as it provides a very simple description of the difference in electric field between a PPE design, and the IDE design with a single parameter, Δa.

One can compare $\alpha_{\text{Approximation}}$ as described by Equation 5.16 to $\alpha_{\text{Gevorgian}}$ as described by Equation 2.10b. Such a comparison is shown in Figure 5.7. One can see from Figure 5.7(b) that the approximation is very good in the region $a > 3t_f$ and $b > 6t_f$.

5.3.3 Effective Electrode Spacing a_{eff} and Effective field E_{eff}

In Equation 5.15, the complicated geometry of the sample is treated as if it was a simple PPE geometry, but with an electrode spacing $a + \Delta a$. This gives rise to the concept of effective electrode spacing a_{eff}, and the effective electric field E_{eff}, defined as in Equations 5.17a and

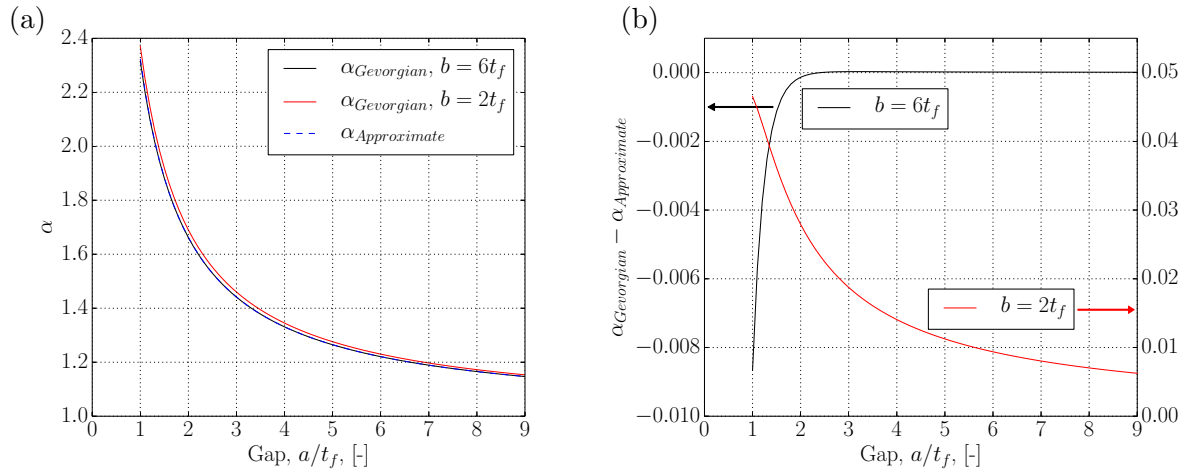


Figure 5.7: Comparison of $\alpha_{\text{Gevorgian}}$ and $\alpha_{\text{Approximation}}$ for $b = 6t_f$. $\alpha_{\text{Gevorgian}}$ for $b = 2t_f$ is shown for comparison. (a) The alphas are plotted in same graph. $\alpha_{\text{Approximation}}$ and $\alpha_{\text{Gevorgian}}$ for $b = 6t_f$ overlap perfectly, and the two curves can not be distinguished in the plot. The overlap is poorer for $b = 2t_f$, and this curve can be seen to deviate from the others slightly. (b) The difference between alpha $\alpha_{\text{Gevorgian}}$ and $\alpha_{\text{Approximation}}$ for $b = 6t_f$ and $b = 2t_f$. Again, the difference can be seen to be very small for $b = 6t_f$, being close to zero for $a > 3t_f$. For $b = 2t_f$, the difference is significant. This is as expected, since the simplification was derived for the case $b > 6t_f$ and $a > 3t_f$, and will perform poorly outside of this region.

5.17b.

$$a_{\text{eff}} = a + \Delta a \tag{5.17a}$$

$$E_{\text{eff}} = \frac{V}{a_{\text{eff}}} \tag{5.17b}$$

Where V is the voltage applied to the sample.

This interpretation of the Gevorgian model can be visualised by considering the sample as consisting of 3 separate regions, one central region with straight field lines, and two contact regions with curved field lines. This is shown in Figure 5.8. The effective field E_{eff} is the field found in the central region, with straight field lines.

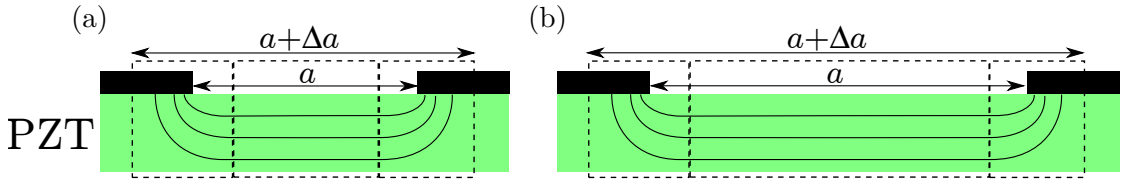


Figure 5.8: Schematic drawing of electric field lines in the PZT. (a) Sample with small electrode spacing. (b) Sample with larger electrode spacing. One central region with straight field lines, and two contact regions with curved field lines are indicated in each figure. The size and shape of the contact regions are the same in the two figures, and only the central region has a different shape in (b) compared to (a). The contact regions are responsible for the additional voltage drop caused by Δa in Equation 5.17. In this model Δa is independent on the electrode spacing a because the size and shape of the contact regions are independent on a.

5.3.4 Experimental Verification

The simplified expression for the electric field E_{eff} has been verified experimentally, as illustrated in Figure 5.10. The left side of the figure shows loops cycled with the simple model for the electric field E_{simple}, while on the right the same loops are plotted according to the effective field E_{eff}. It can be seen that Figure 5.9(b) shows better overlap compared to 5.9(a). The author wanted to test this before fabrication was complete, and for this reason this test was done on an old batched of samples available from previous research. However, these samples are of similar composition and design to the samples fabricated here[3].

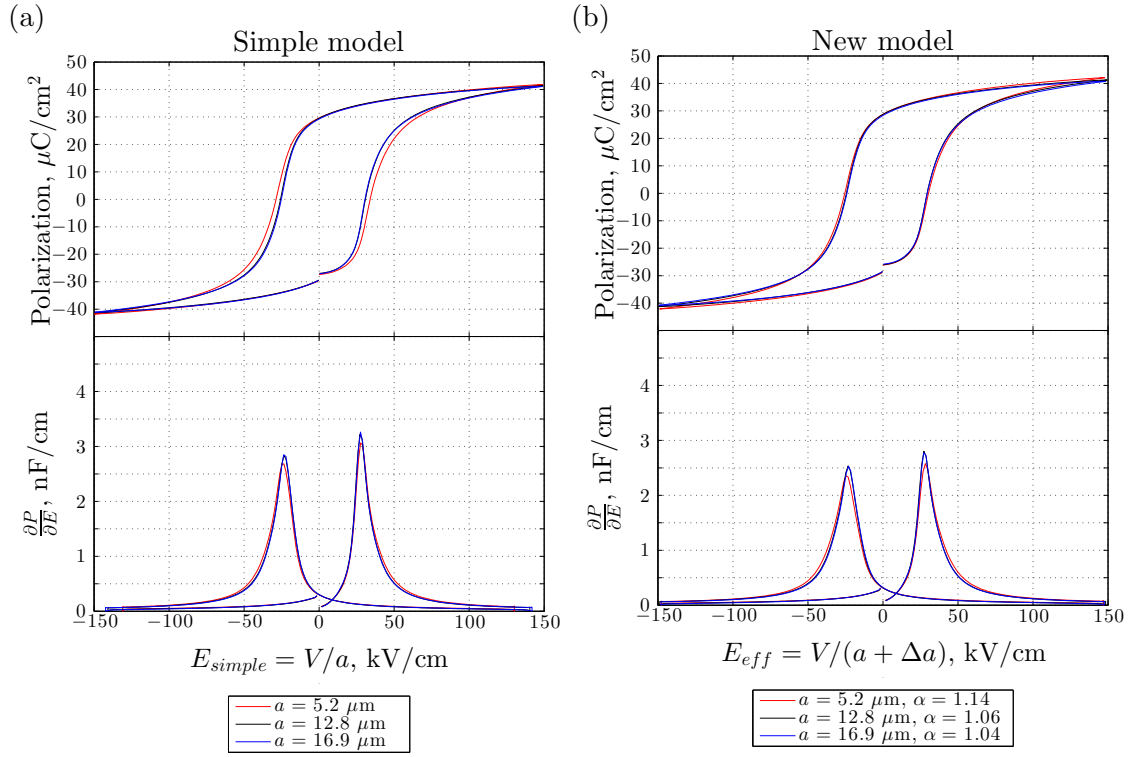


Figure 5.9: PV loops obtained from samples after annealing in oxygen at 550 °C. (a) Cycled with the simple model to determine the maximum voltage so that the electric field reaches 150 kV/cm. (b) After annealing again and cycled with the new model to determine the maximum voltage. The electrode spacing a is listed in the legend with unit µm, and $\alpha = (a + \Delta a)/a$ is also listed. The two samples with electrode spacing larger than 10 µm can be seen to have good overlap in both subfigures. The sample with electrode spacing 5.2 µm can be seen to overlap well with the others only in subfigure (b).

The excellent overlap seen in Figure 5.10(b) is very useful for further research, since the effective field model is seen to minimise the effect of geometrical factors on the shape of the loop, as it is designed to do. This makes it much easier to study the influence of other factors that affect the shape of the loop, such as the atmosphere during annealing, damage from sputtering, effect of UV, and varying the PZT composition.

Once new samples were fabricated, these could also be used to show that there is increased overlap when using the effective field. Such loops are shown in Figure 5.10. In this case both subfigure (a) and (b) show the same experimental data, with maximum field determined by $E_{\text{eff}} = 150$ kV/cm. In subfigure (a) the experimental data is plotted according to the simple field, $E_{\text{simple}} = V/a$, and in (b) the data is plotted as a function of the effective field $E_{\text{eff}} = V/(a+\Delta a)$.

[3]Samples from this wafer was also used in [32].

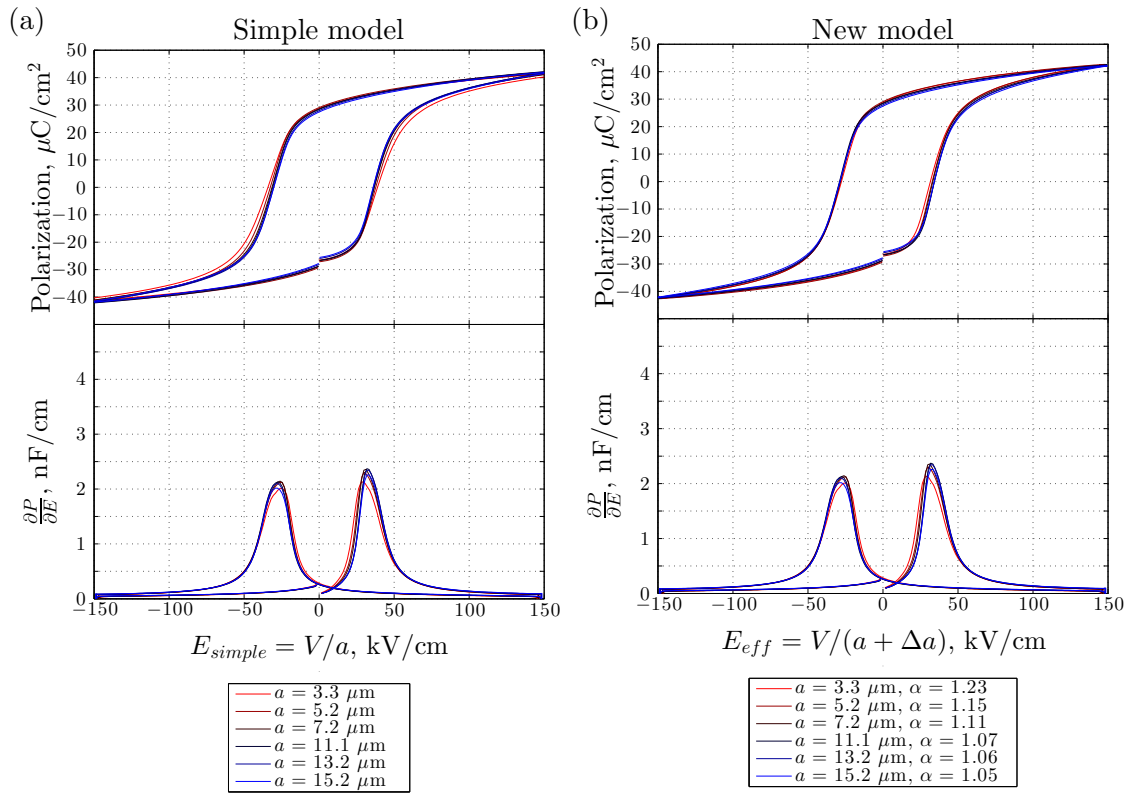


Figure 5.10: PV loops obtained from samples after annealing in oxygen at 550 °C. (a) Plotted with the simple model to determine the field and (b) with the new model to determine the field. The samples have the H design, but the loops obtained are indistinguishable from loops obtained from samples with F design or control samples (N).

5.4 Self-Poling

The results from e_{IDE} measurements on samples prior to cycling or annealing are shown in Figure 5.11. Self-poling is observed in these measurements. Previously, no signal of comparable magnitude has been observed in e_{IDE} measurements directly after fabrication[4]. These results are therefore the first accounts of self-poling observed in IDE structures. The self-poling can be seen to be greater for samples with small gaps. This is consistent with the proposals made in Section 3.2.3. Namely that all samples contain a section of self-poled PZT, and that this section is of the same size in all samples. The samples also contain non-polarised PZT, spanning the rest of the electrode spacing, and acting as a passive region.

Figure 5.12 shows schematically how the samples were connected to measuring circuits. The ground was connected to the uncovered electrodes, while charge was collected as flowing from the covered electrodes. An amperemeter could have been used for this, as indicated in the figure, but for higher accuracy a charge amplifier was used in this role. For PV measurements, a voltage was applied at the location of the amperemeter in the figure.

The direction of self-poling observed is so that the polarisation goes from the covered electrode to the uncovered electrode, as shown in Figure 5.13.

[4]For samples with symmetric electrodes, no signal is typically observed. Samples with asymmetric electrodes have previously produced very low signal, as the measurement equipment is quite sensitive. This very low signal is of insignificant amplitude compared to what is commonly measured in poled samples, unlike the signal found for self-poled samples in in this work, which reaches an appreciable amount of the poled signals (not published)

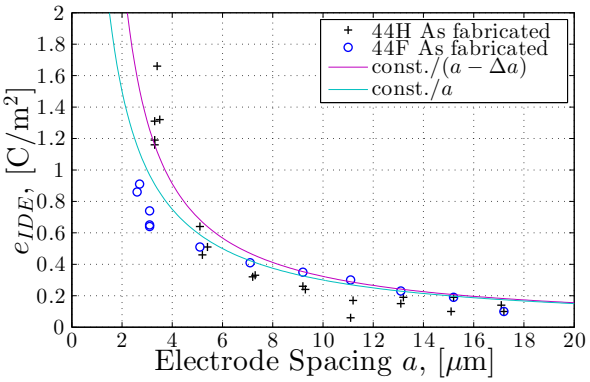


Figure 5.11: Measured e_{IDE} for as-fabricated samples. The lines indicate the expected behaviour if the amount of self-poled PZT is constant between different samples. As it is not certain if a or a_{eff} should be used here, two lines are shown.

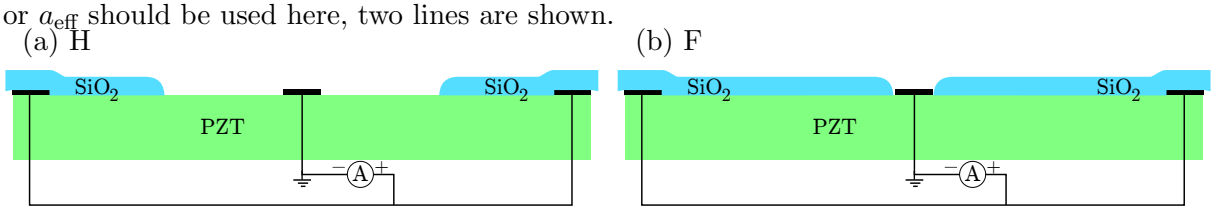


Figure 5.12: Schematic drawing of a PZT thin films with partial SiO_2 cover, (a) design H (half), (b) design F (full). The illustration shows how the sampels were connected to the measuring apparatus.

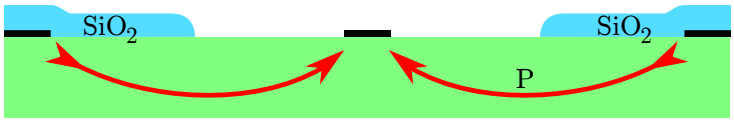


Figure 5.13: Direction of self-poling, as indicated by red arrows.

It is useful to compare e_{IDE} from self-poling, with e_{IDE} in poled samples. The e_{IDE} measured after annealing in oxygen and cycling with PV and CV loops (cold poling) is shown in Figure 5.14. Note that the y-axis is different in Figure 5.11 and 5.14[5]. e_{IDE} can be seen to be relatively stable in poled samples at around -9 C/m^2. The self-poling observed is up to 1.66 C/m^2, which is 18.4 % of the poled value, indicating that a region of about 600 nm is self-poled according to the model presented in Section 3.2.3, while the rest of the PZT is not self-poled.

Self-poling was also observed in PV loops obtained from as-fabricated samples (before annealing). This self-poling is only clearly seen in the first loop, as the measurement itself poles the sample. The self-poling is evident from the fact that start of the loop $P(0)$ does not start at the origin, and that the loop otherwise seems symmetrical, so that we assume it is well centred. $P(0)$ has been plotted as a function of electrode spacing in Figure 5.15(b), while the loops themselves are shown in 5.15(a). It can be seen that the general trend observed in $P(0)$ is similar to that

[5] e_{IDE} by definition is always positive, as it is defined with respect to the direction of polarisation. In this work, the sign of e_{IDE} is used to describe the direction of polarisation, as e_{IDE} is calculated directly from the current measured in the measurement set up, and by using the same set up regardless of polarisation direction, the calculated e_{IDE} will be negative in the case of a negative polarisation direction. After cycling in PV and CV, the sample is left in a negative state, and therefore the measured e_{IDE} of these samples is by convention listed as negative.

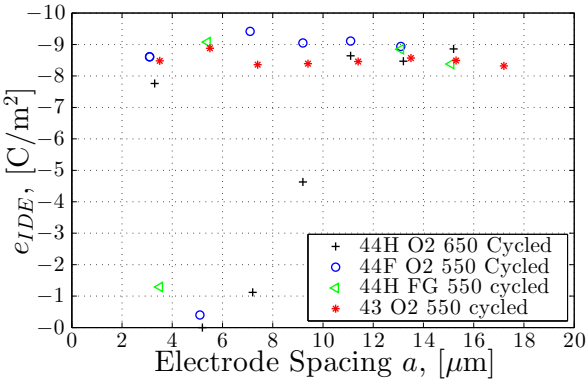
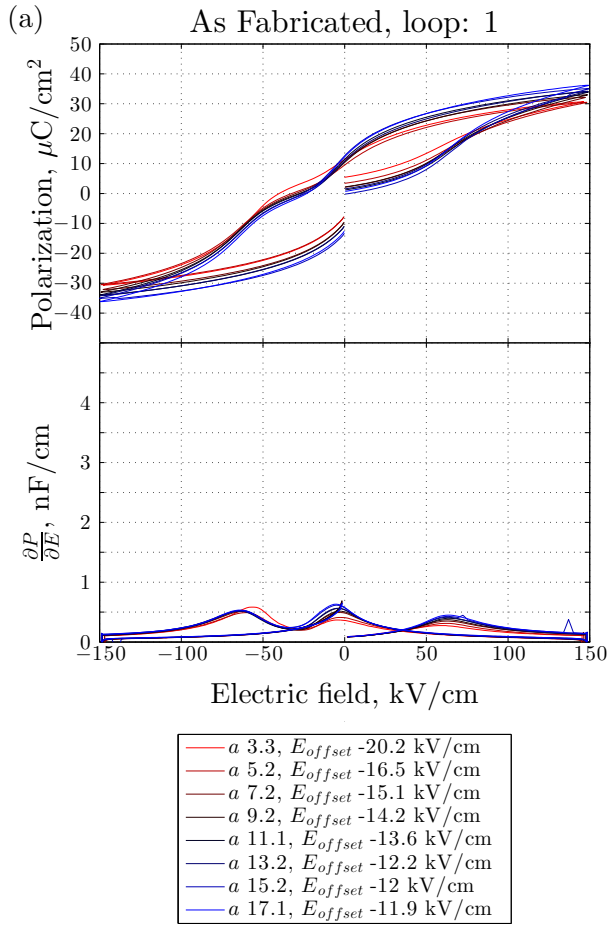


Figure 5.14: Measured e_{IDE} for samples after annealing above 550 °C and cycling with PV and CV loops. The legend includes the wafer, with 44 for the samples covered with SiO_2, and 43 for the control wafer, the design, H or F, the atmosphere during annealing, with 'O2' for oxygen, and 'FG' for reducing atmosphere, and the annealing temperature, 650 or 550 °C. All samples have been annealed for 10 minutes. Samples with e_{IDE} less than 6 C/m^2 are assumed to be broken or improperly mounted in the e_{IDE} setup. The differences between different groups are not thought to be significant.

observed from e_{IDE} measurements, and Figure 5.15(b) appears similar to Figure 5.11, but one cannot compare the plots directly as they measure different observables.



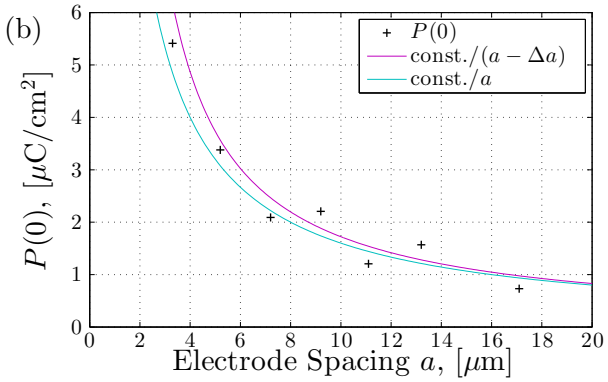


Figure 5.15: As-fabricated PV loop on samples with H design. (a) The first PV loops. The loops can be seen to be pinched, as described in Section 3.1.2, most likely due to ageing in the as-fabricated state. (b) The polarisation at the start of the loop as a function of electrode spacing. The F design shows similar results.

One can estimate the amount of self-poling by comparing $P(0)$ in Figure 5.15 to $P(0)$ in Figure 5.10. These two figures show loops obtained from the same samples, but Figure 5.10 shows

measurements done after annealing in oxygen at 550 °C and cold-poling the samples[6]. $P(0)$ is about -28 $\mu C/cm^2$ for all loops in Figure 5.10, while the highest value in Figure 5.15 is 5.41 $\mu C/cm^2$. This indicates a self-poling fraction of 19.3 %, or a self-poled region of about 640 nm while the rest of the film is not self-poled, according to the theory presented in Section 5.5.

Samples with no SiO_2 cover (control wafer) show no self-poling. Also, annealing at 550 °C is found to remove all polarisation from self-poled and cold-poled samples.

5.4.1 Cause of Self-Poling

The origin of the self-poling is assumed to be in the fabrication process, as the samples get no other treatment before they are measured. Furthermore, any treatment that is symmetric on both electrodes, cannot cause self-poling due to symmetry. This leaves only asymmetric steps in the fabrication process as possible causes for self-poling. The asymmetric steps in the fabrication sequence are:

1. Exposure to UV of 405 nm before deposition of SiO_2. The UV penetrates through the photoresist, and will also expose the PZT below.
2. Development of the photoresist. During development the parts of the structures not covered by photoresist are exposed to the chemicals in the developer.
3. Sputtering of SiO_2. Sputtering is known to damage the PZT surface, and may also charge the exposed PZT.
4. Removal of the photoresist. During removal of the photoresist, the parts of the structure not covered by SiO_2 is exposed to the chemicals in the remover.

All of the above procedures are carried out at room temperature, and changing the polarisation direction at room temperature is associated with a large energy barrier. During sputtering, the surface of the PZT is exposed to incoming ions of high energy, and there may be a surface temperature higher than room temperature. The surface may also become charged during sputtering, providing an electrical field through the material that may cause self-poling. Sputtering was therefore hypothesised to be the most likely step to cause self-poling.

5.4.2 Possibility of Self-Poling by Sputtering

One can speculate that oxygen is dislodged from the PZT during sputtering of the SiO_2 cover, leaving positively charged oxygen vacancies as a surface charge surrounding the covered electrode. This could potentially pole the PZT in the observed direction, but the exact mechanism of how this would occur has not been investigated further here. Self-poling away from the surface that is sputtered upon has previously been observed in PPE devices[2].

The hypothesis that self-poling was caused by sputtering of SiO_2 was investigated by sputtering another layer of SiO_2 onto samples with partial SiO_2 cover. This is illustrated in Figure 5.16. The 'old' SiO_2 acted as a mask, and only the uncovered part of the PZT was exposed directly to the plasma. As the exposed region here was the inverse of the exposed region during fabrication (Figure 4.3 step (j)), it was theorised that this would cause self-poling in the opposite direction.

[6]Figure 5.10 shows the the final PV loop obtained after the sample has been cycled with 5 PV loops and 3 CV loops previously, and is therefore in a cold-poled state at the start of the measurement.

The samples were annealed at 550 °C in order to remove any self-poling already present in the PZT before sputtering the second layer.

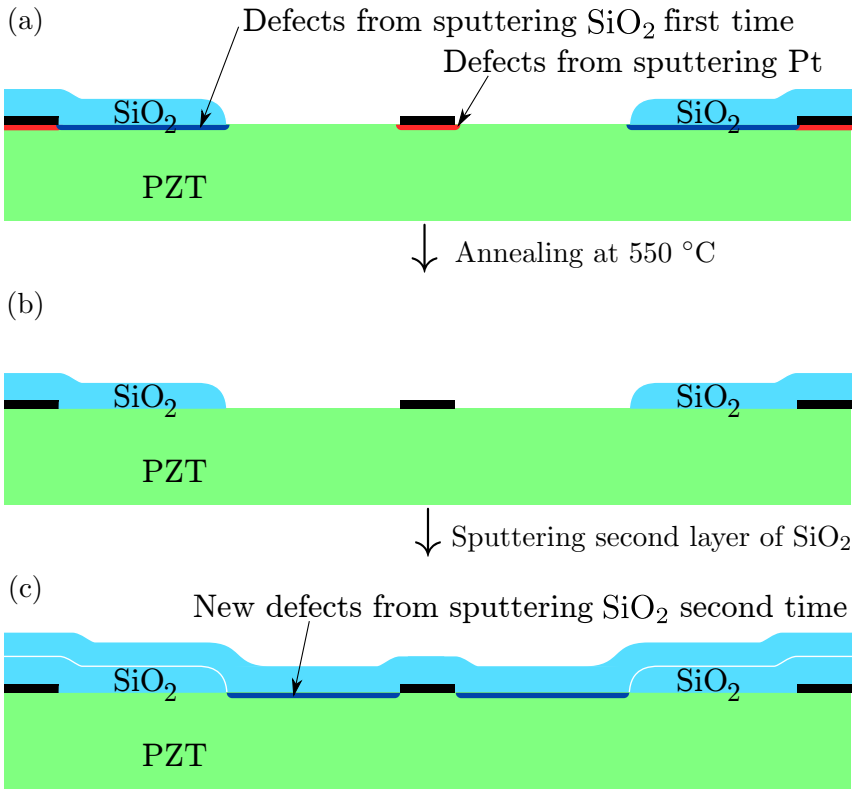


Figure 5.16: (a) Regions damaged by sputtering during deposition of Pt electrodes and SiO_2. It is hypothesised that this damage may have caused the self-poling. (b) Sample after annealing, where all damage cause by sputtering is thought to be cured. (c) Sample where a second layer has been sputtered, introducing new defects.

The results after sputtering are shown in Table 5.1. The sputtering can be seen to affect the measured e_{IDE}, but with a very small magnitude, and an inconsistent direction. This shows that defects from sputtering of SiO_2 alone is not sufficient to cause self-poling.

Table 5.1: Effect of second layer of SiO_2 on annealed samples on e_{IDE}.

Sample	**gap** [µm]	e_{IDE} [C/m^2] As-fabricated	**Treatment**	e_{IDE} [C/m^2] After	Difference
44RRT-b4a6-2F	3.1	0.65	Anneal in O_2 at 550 °C	-0.04	
			Second layer of SiO_2 sputtered	-0.13	-0.09
44RRB-b4-a6-2F	3.4	unknown[7]	Anneal in O_2 at 550 °C	unknown	
			Second layer of SiO_2 sputtered	-0.08	$\sim$ -0.08
44LLB-b4-a6-3H	3.3	unknown	Anneal in O_2 at 550 °C	unknown	
			Second layer of SiO_2 sputtered	0.1	$\sim$ 0.1

With these results in mind, it was investigated if the self-poling was due to interactions between the damage caused by sputtering of the Pt electrodes and the damaged caused while sputtering the SiO_2. If this was the case, self-poling would only manifest itself if the damage from sputtering of the electrodes was still present. To test this, a second layer of SiO_2 was sputtered

[7] Unfortunately, some samples were not measured before and after every step

onto samples that had not been annealed, schematically shown in Figure 5.17. The results are presented in Table 5.2. Also here it can be seen that the effect of sputtering a second layer is much lower than the self-poling already observed, and that the sign is not consistent. As the differences in Table 5.2 are qualitatively similar to those in Table 5.1, this experiment does not prove such an interaction. However, neither do these results disprove such an interaction, as explained in the next paragraph.

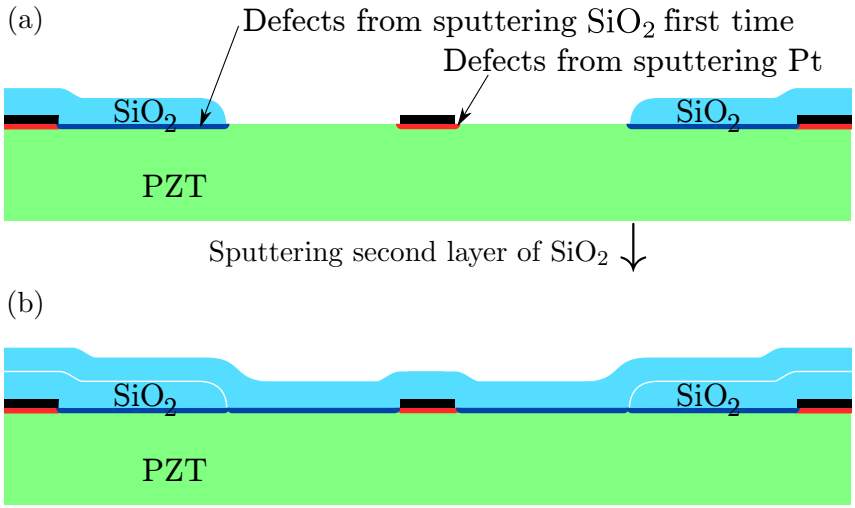


Figure 5.17: (a) Regions damaged by sputtering during deposition of Pt electrodes and SiO_2. (b) Sample where a second layer has been sputtered, introducing new defects.

Table 5.2: Effect of sputtering of a second layer of SiO_2 onto not annealed samples.

Sample	a [µm]	e_{IDE} [C/m^2] As-fabricated	**Treatment**	e_{IDE} [C/m^2] After	Difference
44LC-b5a6-3H	3.3	1.16	Second layer of SiO_2 sputtered	1.31	0.15
44LC-b5a8-H	5.1	0.64	Second layer of SiO_2 sputtered	0.67	0.03
44RRT-b4a6-3F	3.1	0.64	Second layer of SiO_2 sputtered	0.44	-0.2

When a sample is poled, it is done by applying a voltage, and then removing the voltage. The ferroelectric material then retains the same state as when the voltage was applied. An analogy to this can be seen in depositing first one and then a second layer of SiO_2. The first layer introduces defects only on one region, creating a potential across the sample. This can be seen as similar to applying a voltage across the sample. The second layer will introduce defects to the rest of the surface, removing the potential as the sample is now symmetric with respect to defects, as seen in Figure 5.17. This would be similar to removing the applied voltage. In this analogy it would be expected that the second layer of SiO_2 does not affect the self-poling, as it only serves to remove the asymmetry that is already there. In this way, interactions between the damage caused by sputtering of the Pt electrodes and the damaged caused while sputtering the SiO_2 may still be the cause of self-poling, and is consistent with the results of the measurements done.

This hypothesis could be tested further by fabricating a new wafer of samples, and annealing this wafer at 550 °C after depositing the electrodes, but before sputtering the first layer of SiO_2. If this wafer does not show self-poling, it can reasonably be assumed that self-poling is caused by interactions between defects caused by sputtering the Pt electrodes and defects caused by sputtering the SiO_2. As this would require the fabrication of new samples, this has not been

done in this work.

5.4.3 Possibility of Self-Poling by Exposure to UV

Based on the results from sputtering of a second layer of SiO_2, asymmetric exposure to UV was again considered as a potential cause of self-poling. This was considered even though no mechanism for how UV could pole the sample has been proposed. The `Heidelberg MLA 150` maskless aligner is capable of aligning and exposing single samples, and a single sample from the control wafer was chosen for asymmetric exposure. This exposure was done with the same mask design as the one used for patterning of the photoresist prior to deposition of SiO_2 for the other wafer. The result is shown in Table 5.3. Asymmetric exposure to UV is found to not introduce any self-poling.

Table 5.3: Effect of asymmetric exposure to UV on e_{IDE}.

	a	e_{IDE} [C/m^2]		e_{IDE} [C/m^2]	
Sample	[µm]	As-fabricated	**Treatment**	After	Difference
47643LLB-b4a6-2N	3.5	0	Anneal in O_2 at 550 °C	-0.03[8]	
			Asymmetric UV[9]	-0.03	0

However, there were concerns that the alignment of the tool was not accurate, and that the exposure conditions were different since this sample was not covered with photoresist. With this in mind it was decided to investigate the effect that UV could have on polarisation. Several samples were exposed to UV using a mercury lamp and a optical fiber to direct the light. This was done both with and without a filter for 405 nm, as this wavelenght is used by the `Heidelberg MLA 150`, and is slightly below the band gap of PZT. The results are shown in Table 5.4. Symmetric exposure to UV is shown to reduce the self-poling, but only for long exposure times. The intensity of the UV source is not known, as no tool was available to measure this, but it is thought that 30 minutes of exposure from the mercury lamp is a much higher dosage than the 130 mJ/cm^2 used in the MLA during fabrication. As lower exposure times show little or no change in e_{IDE}, these results indicate that asymmetric exposure to UV is not the cause of self-poling.

Table 5.4: Effect of symmetric exposure to UV on self-poling.

	a	e_{IDE} [C/m^2]		e_{IDE} [C/m^2]	
Sample	[µm]	As-fabricated	**Treatment**	After	Difference
44LL-b3-a6-1H	3.4	1.64	10 min UV with filter	1.64	
			10 min UV	1.62	-0.02
44LC-b5a6-2H	3.3	1.31	30 min UV	1.14	-0.17
44RC-b5a6-2F	2.7	0.91	30 min UV	0.66	-0.25

5.4.4 Discussion of Possible Self-Poling Mechanisms

As the self-poling could not be reproduced by sputtering of SiO_2 nor by asymmetric exposure to UV, one could consider again the possibility of self-poling by exposure to chemicals in the developer and the remover. These chemicals are not very aggressive, and are not expected to react with the PZT. Also note that the entire surface has been exposed to remover previously, during deposition of the Pt electrodes. As the energy barrier for switching ferroelectric domains

[9]This sample was cycled with PV loops before annealing. The measured e_{IDE} measured after annealing is what remains of this polarisation. It is very small, and considered to be insignificant.

is very high, no specific tests have been done to find out if these chemicals affect the polarisation.

The `Pfeiffer SPIDER` used to sputter SiO_2 in this work is not equipped with a shutter. This means that the sample is exposed to the plasma as the plasma is ignited. The plasma has a 30 s ramp time, and the plasma is only stable after the ramp. It may be that the self-poling is caused by sputtering, but that it is very sensitive to how the plasma is ignited, and to the conditions during the ramp. These may vary, as the plasma is unstable during this time. The first few seconds of the sputtering are considered important, as it is only during this time that the PZT is uncovered, as the SiO_2 quickly grows on the surface. This could explain the varying results obtained from sputtering another layer of SiO_2. However, more research would be needed to confirm this theory.

5.4.5 Experiments With Reducing Atmosphere

Oxygen vacancies caused by damage during sputtering has been suggested as a possible cause of the self-poling in [39][10], and in the previous section. It has therefore theorised that oxygen vacancies induced by a reducing atmosphere may have a similar effect, as described below.

Reducing atmosphere was provided by forming gas (N_2 with 5 at.% H_2). It was expected that oxygen would leaving the sample in the form of O_2 or as volatile lead oxide PbO[40]. Both of these processes would provide oxygen vacancies, that may have diffused into the PZT. Hydrogen may also have entered the material, forming OH_O^* during annealing. These processes may have occurred at the surface of the PZT, or they may have been catalysed by the Pt electrode. Hydrogen diffusion into PZT has previously been linked to catalytic activity of a Pt electrode [41].

5.4.6 $e_{31,\mathrm{IDE}}$ Measured After Annealing in Reducing Atmosphere

The $e_{31,\mathrm{IDE}}$ results after annealing in forming gas at 650 °C are shown in Figure 5.18. A series of samples were annealed in oxygen at the same temperature as a control group, and is also shown.

All samples show a similar self-poling behaviour. This self-poling is very small, and is of limited significance due to the low magnitude. The results obtained are at the limit of what the experimental setup can resolve in terms of noise and resolution, however, because they are consistent between many different samples, they are assumed not to be noise.

The small self-poling found here is not seen in the first PV loop measured on these samples (not shown). This is most likely because the signal is too small.

5.4.7 PV Loops Following Annealing in Reducing Atmosphere

Annealing in forming gas at 550 °C provides loops similar to those obtained by annealing in oxygen at 550 °C (Figure 5.25), indicating that there is little or no exchange with the ambient atmosphere at this temperature[11]. As these loops are indistinguishable from those obtained after annealing in oxygen, they have not been included here. Annealing at 650 °C in forming

[10] [39] describes self-poling observed in PPE devices.

[11] There may for example be oxygen exchange at the surface during annealing at 550 °C, but not in the bulk, and the effect of oxygen exchange at the surface may be too small to be detected in PV loops.

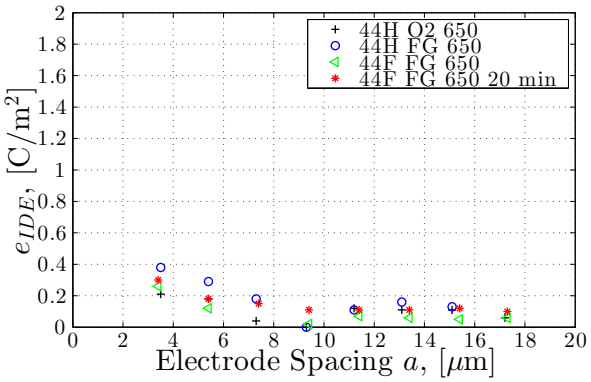


Figure 5.18: Measured $e_{31,\mathrm{IDE}}$ for samples that have been subject to annealing at 650 °C. 'O2' refers to samples annealed in oxygen atmosphere, while 'FG' refers to samples annealed in vacuum with a flow of 200 sccm of forming gas. Samples were annealed for 10 minutes, unless otherwise stated.

gas was found to give slightly slanted loops as seen in Figure 5.19. Slanting of the PV loops after samples have been annealed in forming gas has previously been observed in [41], although much more slanting was observed in that case.

It is interesting to note that the control samples (N) are less slanted than the samples with partial SiO_2 cover. One could theorise that the covered and uncovered regions of samples with partially covered electrodes show different ferroelectric properties, for example different coercive fields, and this translates to more slanted loops, while the uncovered samples show more homogeneous properties, and are therefore comparatively less slanted.

Annealing in oxygen atmosphere at 650 °C does not cause slanted loops, and the loops of these samples are similar to those after annealing at 550 °C (not shown).

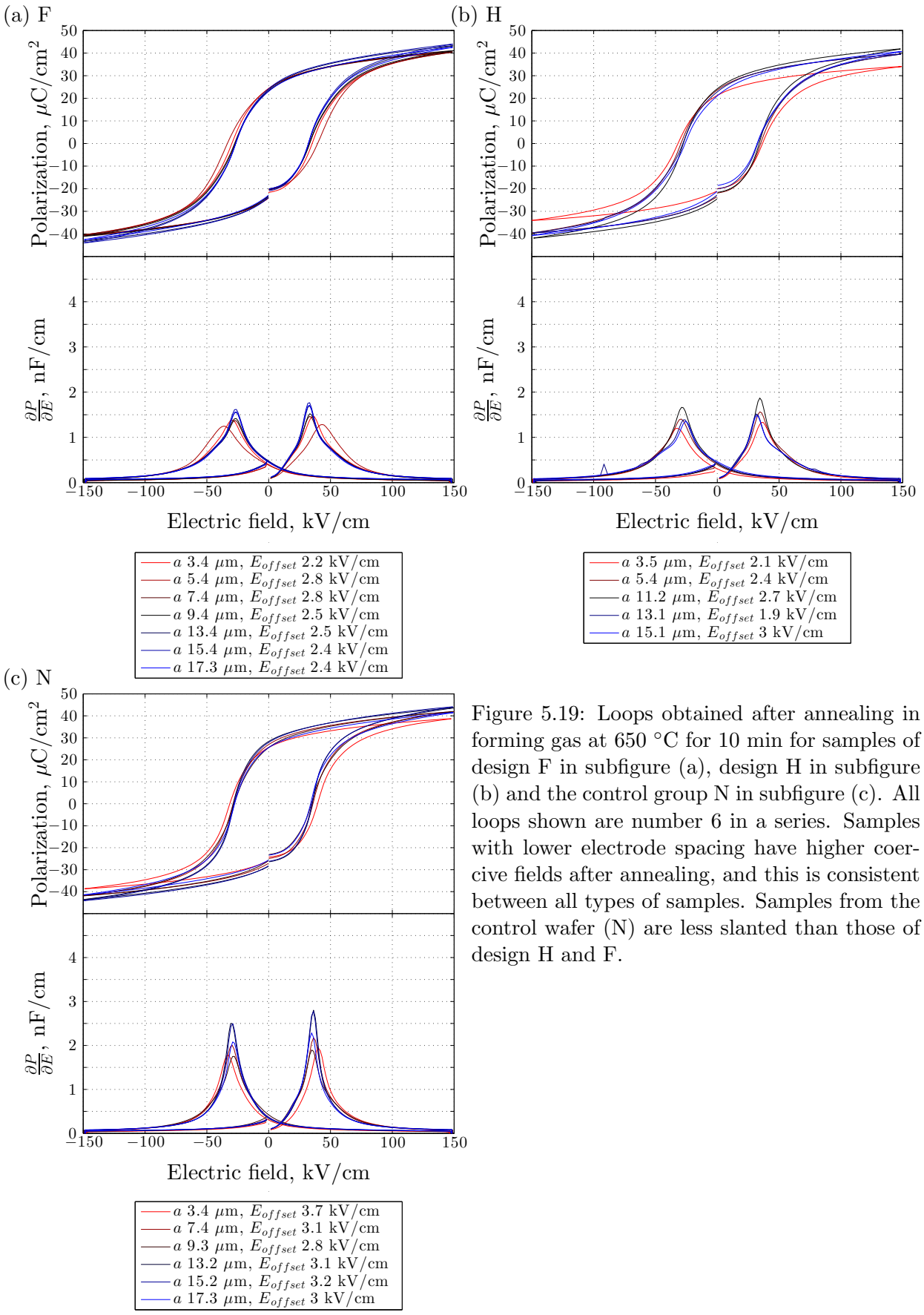


Figure 5.19: Loops obtained after annealing in forming gas at 650 °C for 10 min for samples of design F in subfigure (a), design H in subfigure (b) and the control group N in subfigure (c). All loops shown are number 6 in a series. Samples with lower electrode spacing have higher coercive fields after annealing, and this is consistent between all types of samples. Samples from the control wafer (N) are less slanted than those of design H and F.

5.4.8 Discussion on the Effects of Reducing Atmosphere

The self-poling observed after annealing at 650 ° is very minor, and is therefore of little practical interest. This self-poling could be caused by PbO or O_2 evaporating from the surface, forming positively charged oxygen vacancies V_O^{**} that then diffuse into the material. This would leave negatively charged Pb vacancies or electrons at the surface or the electrode. An electric field would then be formed by separation of charge as the oxygen vacancies diffuse, and this electric field could cause self-poling. This is illustrated in Figure 5.20. However, it should be noted that the magnitude of the effect is so small that additional experiments with lower gaps (where the effect is expected to be stronger) would be needed to confirm this.

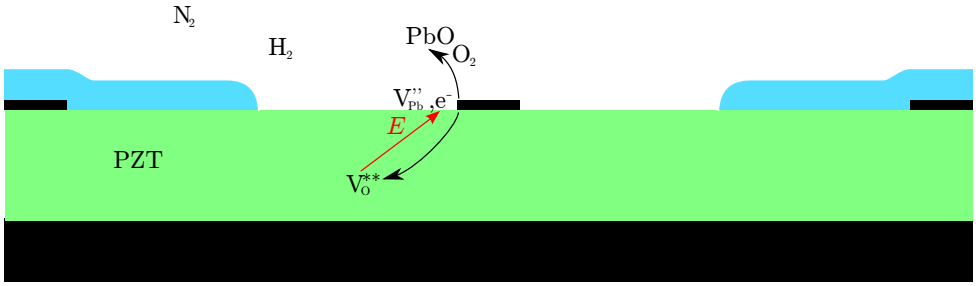


Figure 5.20: Electric field (E) generated by oxygen vacancies diffusing into the PZT, while lead vacancies or electrons remain at the surface or Pt catalyst. This electric field may then cause self-poling as the sample cools down past the Curie temperature T_C.

Degradation of the PV loops after annealing in reducing atmosphere is similar for the two designs, and this supports the finding in [41] that hydrogen exchange with the atmosphere only occurs at the exposed Pt contact, regardless of design.

Forming gas has been found to degrade the ferroelectric properties, and the PV loops become more slanted. Further research into the effect of forming gas on these samples is therefore seen as unlikely to lead to practical applications, as the degradation of ferroelectric properties makes for poor devices.

5.5 Slanting of Loops Prior to Annealing

Prior to annealing, the PV loops were highly slanted, as shown in Figure 5.21. The loops on the left are the first loops of the series. After this loop, 4 more PV loops were measured, followed by 3 CV loops, and one more PV loop. The last PV loop obtained for each sample is shown to the right. It can be seen that the first loop is pinched, while the sixth loop is more quadrilateral. The pinching seen in the first loop is thought to be caused by different parts of the samples ageing in different states, as described in Section 3.1.2. This ageing may have been enhanced by exposure to UV during fabrication. After cycling numerous times, all parts of the sample start to share a common history of switching, and this is thought to cause the disappearance of the pinching. De-ageing by cycling is well known, and has been studied by K. Carl and K. H. Härdtl [26]. As the shape of the loop depends on the history of the sample, all samples were cycled with the same regime, 5 PV loops, followed by 3 CV loops and 1 more PV loop, so that the individual loops could be compared between samples.

After annealing, the loops are not slanted, as shown in Figure 5.10. Slanted loops could be

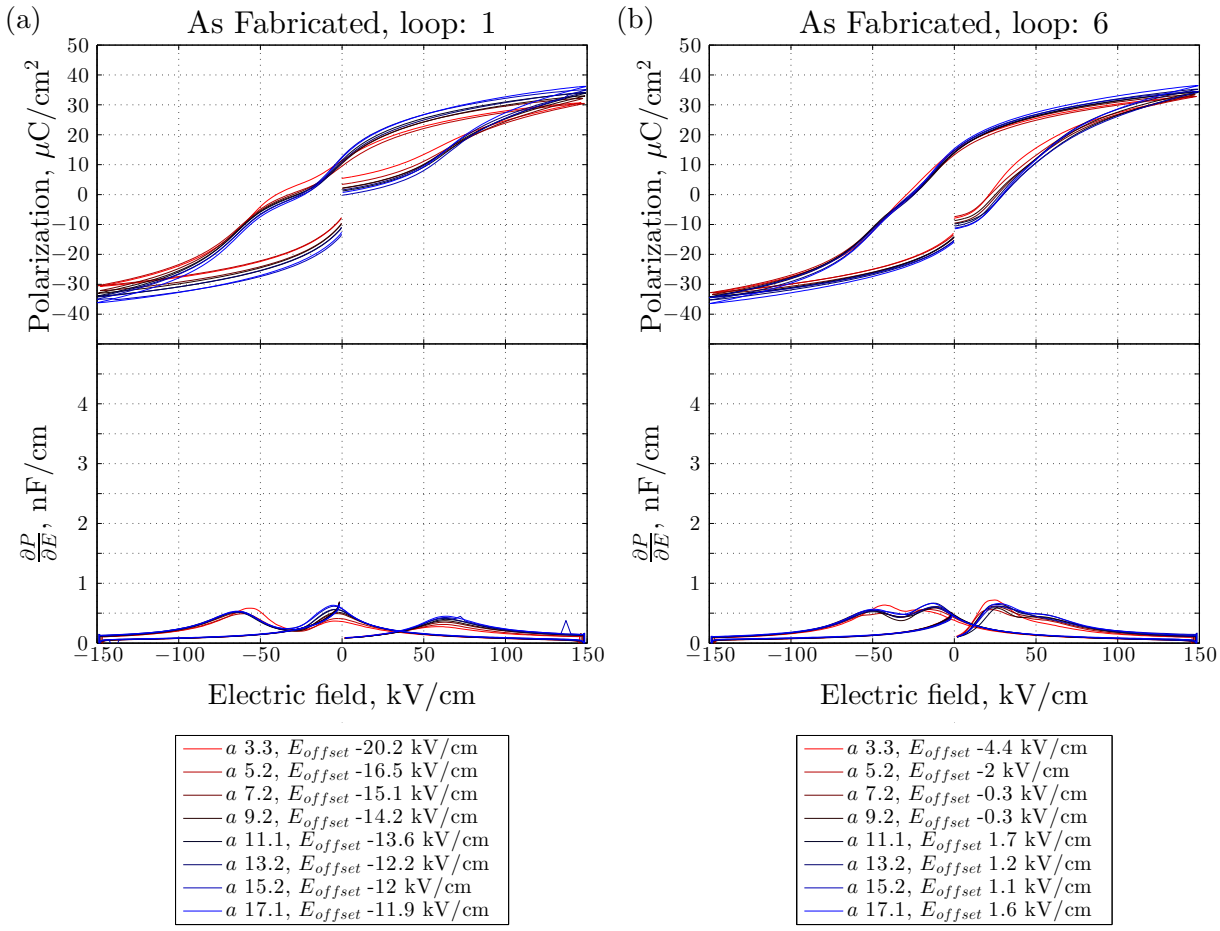


Figure 5.21: As-fabricated samples. (a) loop 1, (b) loop 6.

related to a dielectric layer at the interface, or alternatively the switching kinetics, where some domains switch before others. Domain kinetics could possibly be investigated by piezoresponse force microscopy (PFM), but this has not been done in this work.

Slanted loops prior to annealing have previously been observed in [1], and was attributed to a low quality interface between the electrodes and the PZT. This low quality interface could be due to damage of the PZT under the electrode during sputtering. In this case, one can imagine a layer of PZT surrounding the electrode that has lost its ferroelectric properties and become paraelectric. The effect of such a layer is discussed in Section 3.1.3, where a model is presented for simulating the effect of a passive layer, and it is shown that this causes slanting of the loops, depending on the parameter $\frac{d}{\varepsilon_d a}$, which is strongly dependent on the electrode spacing.

5.5.1 Simulations of Passive Layer

In order to evaluate if the slanting is caused by a passive layer, one can use the model presented in Section 3.1.3. To implement this model, one needs a sample with properties similar to that of the samples that produce slanted loops, but where it is known that there is no dielectric layer at the interface.

It was assumed that annealed samples have no dielectric layer at the interface, and these samples could therefore fill this role. This assumption was made because loops obtained from these

samples show very little slanting, and because samples of different electrode spacing have been shown to produce loops with excellent overlap, as shown in Figure 5.10. If there was a dielectric layer in these samples, all samples would be expected to have some degree of slanting, and the low-gap samples would be expected to be much more slanted, as the effect of a dielectric layer is very gap-dependent.

To simulate the effect of a passive layer, an annealed sample was measured a multiple maximum fields, and the model presented in Section 3.1.3 was used on the results. The results are shown in Figure 5.22. This was done so that the slanting observed in Figure 5.21 could be compared with the simulated effect of a passive layer. It can be seen from Figure 5.22 that even a low value for $\frac{d}{\varepsilon_d a}$ has a significant effect on the loop. A large number of loops were captured, so that one would be able to potentially produce good matches for all the loops in Figure 5.21(b).

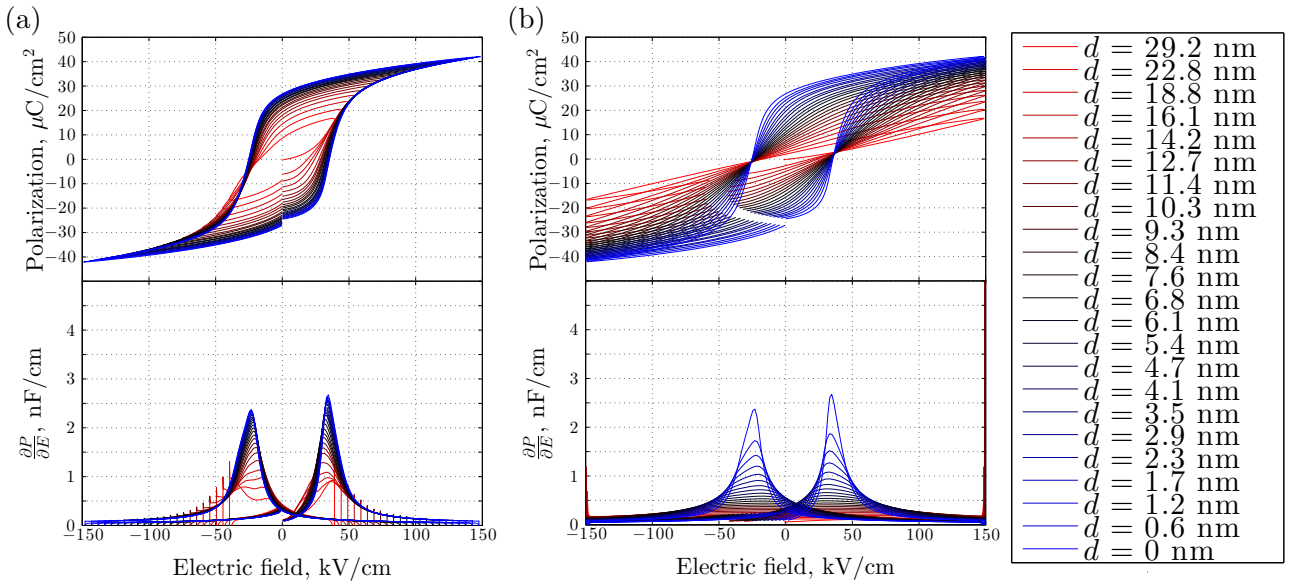


Figure 5.22: (a) Loops captured at different maximum field. (b) Simulated effect of a passive layer added to the loops in (a) as described in Section 3.1.3 with the parameter $d/\varepsilon_d a$ set so that the maximum field of the simulated stack reaches 150 kV/cm. The legend shows the corresponding thickness of the dielectric layer d if a is 10 μm and ε_d is assume to be 5.

5.5.2 Comparison of Experimental Results and Simulations

The best fit for the sample with the largest electrode spacing in Figure 5.21(b) (17.1 μm) is shown in Figure 5.23(a). A very good fit can be observed when $\frac{d}{\varepsilon_d a}$ takes a value of $1.23 \cdot 10^{-4}$. Based on this fit, and a constant thickness of the passive layer d, one would expect the sample with the lowest gap in Figure 5.21(b) (3.3 μm) to fit well with a simulated passive layer with $\frac{d}{\varepsilon_d a} \approx 5.51 \cdot 10^{-4}$. The simulated loop that is closest to this is plotted in Figure 5.23(b) together with the loop obtained from the sample with the lowest gap in Figure 5.21(b). Based on the model one would expect these two loops to overlap well, but this is not the case.

This model is therefore found to fit well with individual measurements[12], as in Figure 5.23(a), but does not scale correctly with the electrode spacing, as seen in Figure 5.23(b). This shows

[12]For all curves in Figure 5.21, a curve can be found in Figure 5.22 so that the two curves overlap well, but only one such fit is shown here (Figure 5.23(a))

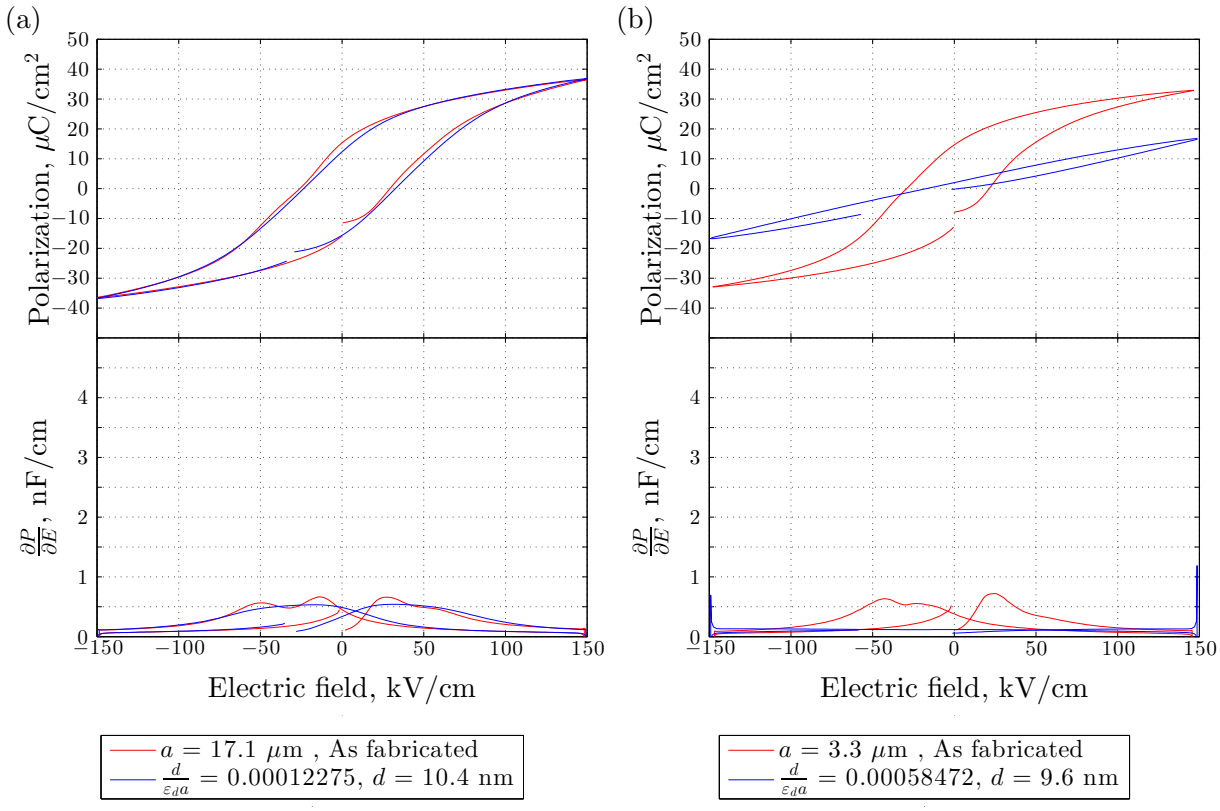


Figure 5.23: Comparison of slanted loops observed (red) and the simulated effect of a passive layer (blue). (a) A best fit is chosen for the sample with the largest electrode spacing in the series, and the curves can be seen to overlap well. The thickness of the passive layer d is shown with a as given by the electrode spacing, and ε_d set to 5. (b) The PV loop of a sample with a gap of 3.3 μm is plotted along a loop showing the simulated effect of a passive layer. The simulated loop in this subfigure has a similar $\frac{d}{\varepsilon_d}$ as compared to that in subfigure (a). One would therefore expect good overlap of the two loops in (b) if the slanting was caused by a passive layer. This is not the case.

that a paraelectric layer at the interface as described by the model is probably not the cause of the observed slanting.

An alternative theory is therefore needed to explain the slanting in these loops. Such a theory could be based on switching kinetics, i.e. how domains form and domain walls move in the sample. Domain walls can be pinned by defects, and the amount of defects therefore affects how the sample switches. Sputtering of Pt is expected to cause a large amount of defects at the interface with the electrode, and this would lead to many pinning centres for domain walls, affecting the switching kinetics. The region around the electrode is of specific importance in these samples, as the electric field is concentrated here, and domains therefore are more likely to nucleate here. Annealing would possibly cure these defect, making the sample switch more easily and giving sharper transitions, as observed in the experimental results.

Sputtering of SiO_2 could also introduce defects, affecting the switching kinetics. This would cause defects at the film surface, forming pinning centres here. It is known from PV loop obtained from samples that have been annealed (curing all defects) and then covered with a second layer of SiO_2 (introducing new defects at the exposed PZT surface) that the slanting caused by sputtering of SiO_2 is small compared to that found in as-fabricated samples, as shown in Figure 5.24. These are the same samples where a second layer of SiO_2 was sputtered in order to see if

a second layer of SiO_2 would cause self-poling in the opposite direction. Defects created during sputtering of the SiO_2 cover are therefore not considered as the primary cause of the slanting seen in the as-fabricated loops, but could be a contributing factor.

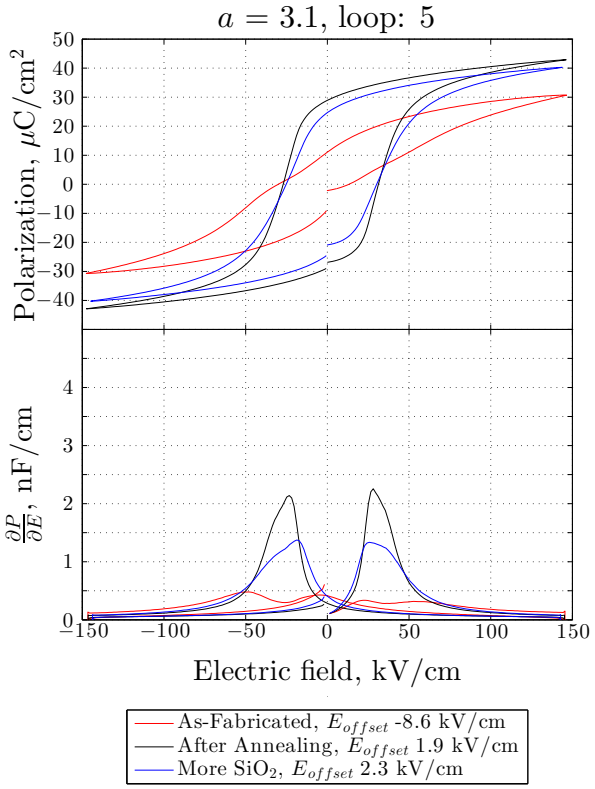


Figure 5.24: Comparison of three loops captured from the same sample. The first loop (red) is captured after fabrication. The second loop (black) is captured after the sample has been annealed in oxygen at 550 °C, curing all defects caused by sputtering. The third loop (blue) is captured after a second layer of SiO_2 has been sputtered onto the sample, causing new defects to form at the previously exposed PZT surface.

A more detailed description of switching kinetics is beyond the scope of this work, but it is seen as a likely candidate to cause the slanting observed in the loops. An investigation into switching kinetics should be coupled with PFM and possibly simulations to support the theory.

5.6 Ageing

It can be seen in Figure 5.10 that the loops are not centred at zero electric field, and that there is an offset in the coercive fields, as described in Section 3.1. This offset is indicative of ageing. Figure 5.10 shows the sixth PV loop in a series of PV and CV loops. The offset is found to increase for each subsequent loop the sample is subject to. An example of this is shown in Figure 5.25. Previous work has suggested that this offset is dependent on the time since the first measurement was initiated[1]. An alternative hypothesis would be that the offset is dependent on the number of loops that the sample has been subjected to.

To distinguish between these two hypotheses, a sample was cycled again two weeks after the first series of measurements was done. If ageing is a product of the time spent in a poled state, one should see a large increase in the offset, while if ageing is a product of the number of loops, the

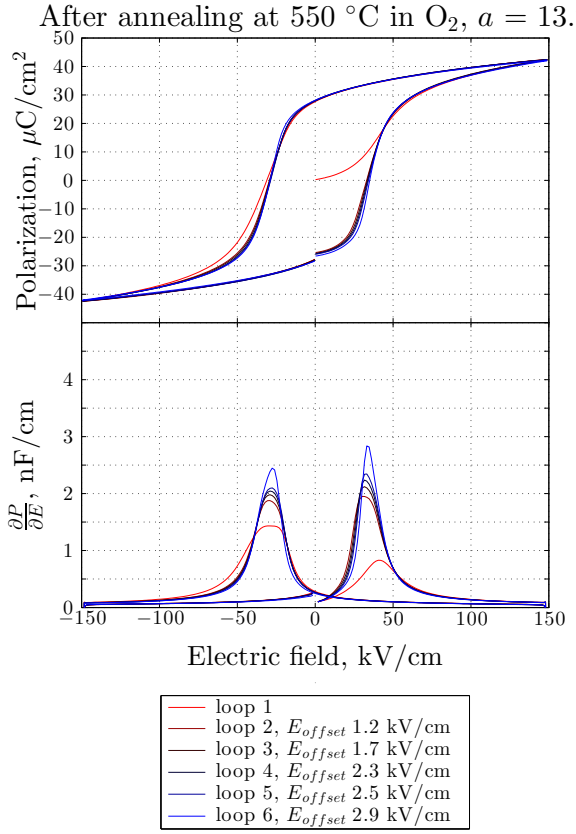


Figure 5.25: The evolution of the loop in a sequence of loops. The electrode spacing a of this sample is 13.2 µm. The offset can be seen to increase between loops, and has units kV/cm. The first loop was captured after annealing at 550 °C in oxygen, and was immediately followed by 4 more PV loops. Following this 3 CV loops were captured, before the 6th PV loop. The offset can be seen to have increased for each subsequent loop. When the first loop was captured, the sample was in an unpoled state, and this is why this loop starts close to the origin. The offset of this loop is not properly defined, as there is no easily definable coercive field on the positive side. A relatively large change in the offset can be seen between the 5th and 6th loop . This is likely due to the CV loops captured between the 5th and 6th loop.

increase in offset should be minor. Such a comparison is shown in Figure 5.26. It can be clearly seen that the offset has increased significantly, showing that the offset increases as a function of time spent in a poled state. It can also be seen that the loop becomes less slanted after ageing.

Possible origins of a time dependent offset have been discussed in Section 2.6, where three possible mechanisms were presented. Orientation of defect dipoles[17, 18], motion of electrons and holes across passive layers[20, 19], and motion of oxygen vacancies in the lattice between domains[25].

These theories differ by how the offset is expected to behave as a function of time. Orientation of defect dipoles is expected to have a time evolution similar to a Debye relaxation process. This is because the orientation of each dipole is independent of the orientation of all other dipoles in the lattice, and that all defect dipoles of the same kind are expected to behave according to the same time constant τ. If this is the dominant mechanism for ageing, one would expect to be able to identify the time constant τ of the most common type of defect dipole from a plot of offset versus time.

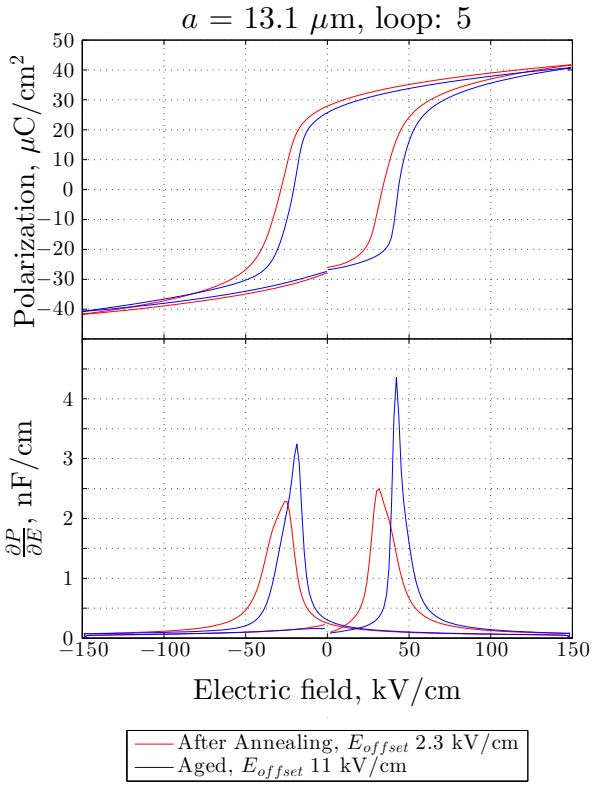


Figure 5.26: The offset of the 5th loop measured after annealing, compared with a loop obtained after leaving the sample in a drawer for about two weeks.

In the model by Grossmann for motion of electrons and holes across a passive layer[13], the probability that an electron or hole will move is dependent on the location of all other electrons and holes. The time evolution is therefore expected to follow a stretched exponential function.

The expected time evolution of the offset in the case of motion of oxygen vacancies between domains is less clear, as no detailed model for this has been presented. However, the motion of oxygen vacancies in this mechanism is driven by a potential gradient, and as more vacancies move a greater distance, the potential gradient becomes smaller. In this way, the change in offset is also expected to follow a stretched exponential function.

5.6.1 Characterisation of Ageing

In order to find the dominant mechanism, samples were cycled numerous times, and the offset was plotted as a function of time since the first loop was measured on a log scale, as shown in Figure 5.27. The PV loops obtained from one sample is shown to the left, while the offset as a function of time is shown to the right. In this plot, results from 6 different samples are shown, and they have been fitted to the empirical function presented in Section 2.7.4, reproduced below:

$$E_{\text{offset}} = E_{\text{offset,max}}\left(1 - \frac{1}{1 + (t/\tau)^{\delta}}\right) \tag{5.18}$$

[13]It is important to keep the passive layer discussed here separate from the discussion of a passive layer in Section 5.5. The possible passive layer discussed in Section 5.5 would be removed by annealing, while the passive layer discussed here would also exist in samples after annealing, as samples are found to age both before and after annealing. Furthermore, a passive layer may have a thickness d and dielectric constant ε_d so that it causes significant ageing, but does not cause significant slanting. This would for example be the case if $d \approx 10$ nm, while $\varepsilon_d \approx 400$.

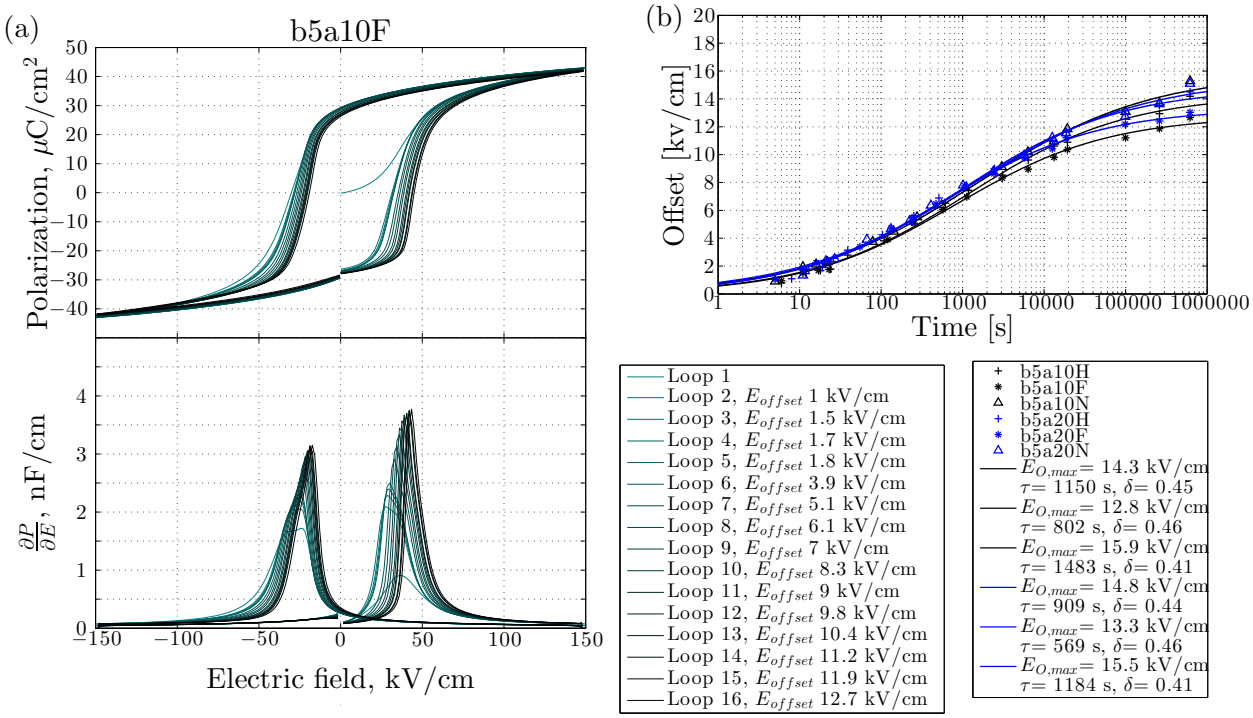


Figure 5.27: (a) PV loops of sample b5a10F after annealing in oxygen. (b) The offset measured from 6 samples plotted against time since the first measurement was initiated. Samples 'a10' have an electrode spacing of about 7 µm, while samples 'a20' have about 17 µm between the electrodes. Different samples can be seen to have different ageing profiles, but these differences do not follow a trend with respect to electrode spacing.

5.6.2 Comparison to Different Models

The time evolution of the offset seen in Figure 5.27(b) shows a stretched exponential function.[14] This indicates that orientation of defect dipoles in the lattice is presumably not the primary cause of ageing.

The two remaining possible causes for ageing both describe motion of charge. The model presented by Grossmann describes motion of electrons and holes across a passive layer, while the proposal by Genenko describes motion of oxygen vacancies. Electrons and holes can be excited by UV, and exposure to UV causes greatly increased mobility for these species. Oxygen vacancies on the other hand do not experience increased mobility when exposed to UV. Exposure to UV can therefore be used to differentiate between these two mechanisms. A comparison between the offset of a sample that has been aged and exposed to UV with samples that have only been aged is shown in Figure 5.28. It can clearly be seen that exposure to UV has a major impact on the offset.

From the results in Figure 5.28, it can also be seen that exposure to UV increases the offset beyond what has been obtained purely by ageing. The highest offset observed in the aged samples, shown in Figure 5.27, is about 15 kV/cm, while after exposure to UV the offset is found to be close to 25 kV/cm. The reason for this is not known, but following Grossmann's model, it is possible that UV radiation excites electrons and holes from deep traps, and that the electrons and holes then move across a passive layer. UV may be able to excite from traps too deep to

[14] If one fits Equation 5.18 to a relaxation function, as expected from orientation of defect dipoles, one would expect δ larger than or close to 1, while δ obtained from the experimental data is closer to 0.5.

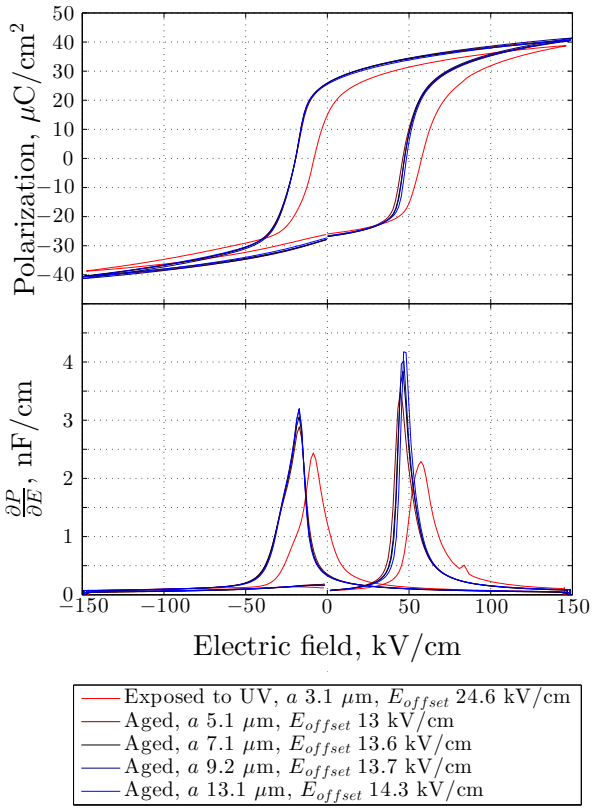


Figure 5.28: The loops in this figure are taken from samples that have been aged for about two weeks. One of the samples, plotted in red, has also been exposed to UV. The exposure to UV has increased the offset. The loops of samples that have not been exposed to UV, but only aged, show very similar offset. This indicates that ageing is not dependent on the electrode spacing.

be excited by thermal excitation, and UV therefore causes a larger offset than only ageing. It is also possible that ageing would cause an offset of this magnitude after a longer time, or if the sample was aged at temperatures above room temperature.

Based on the fact that the offset behaves as a stretched exponential function, and the fact that UV affects ageing, the model by Grossmann appears to be the most likely origin of ageing.

The ageing plots in Figure 5.27 can be fit to Grossmann's model. One such fit is shown in Figure 5.29, while the parameters used in this fit are shown in Table 5.5. σ_{FP}, was here fixed to a value close to that used by Grossmann in [19], ε_i was fixed to the same value as that used in [19], and close to that of PZT, σ_e was fixed based on the remanent polarisation in Figure 5.29(a), and T was fixed close to the room temperature in the building. δ_a, Φ_B and ϕ_0 were set as free parameters for this fit. ε_{opt} then follows from ϕ_0. The experimental results can be seen to fit well to the model.

Table 5.5: Parameters used for Grossmann's model in Figure 5.29.

δ_a	ϕ_B	ϕ_0	$\varepsilon_{opt}/\varepsilon_0$	$\varepsilon_i/\varepsilon_0$	$\sigma_e(0)$	σ_{FP}	T
29.8 nm	0.38 eV	0.038 eV	2.77	400	28 μC/cm^2	$4{\cdot}10^{-10}$ A/Vm	300 K

The value for ϕ_B found in the fit appears reasonable as a defect state, and is comparable to the value found by Grossmann in [19]. The value found for ε_{opt} is also close to that found by

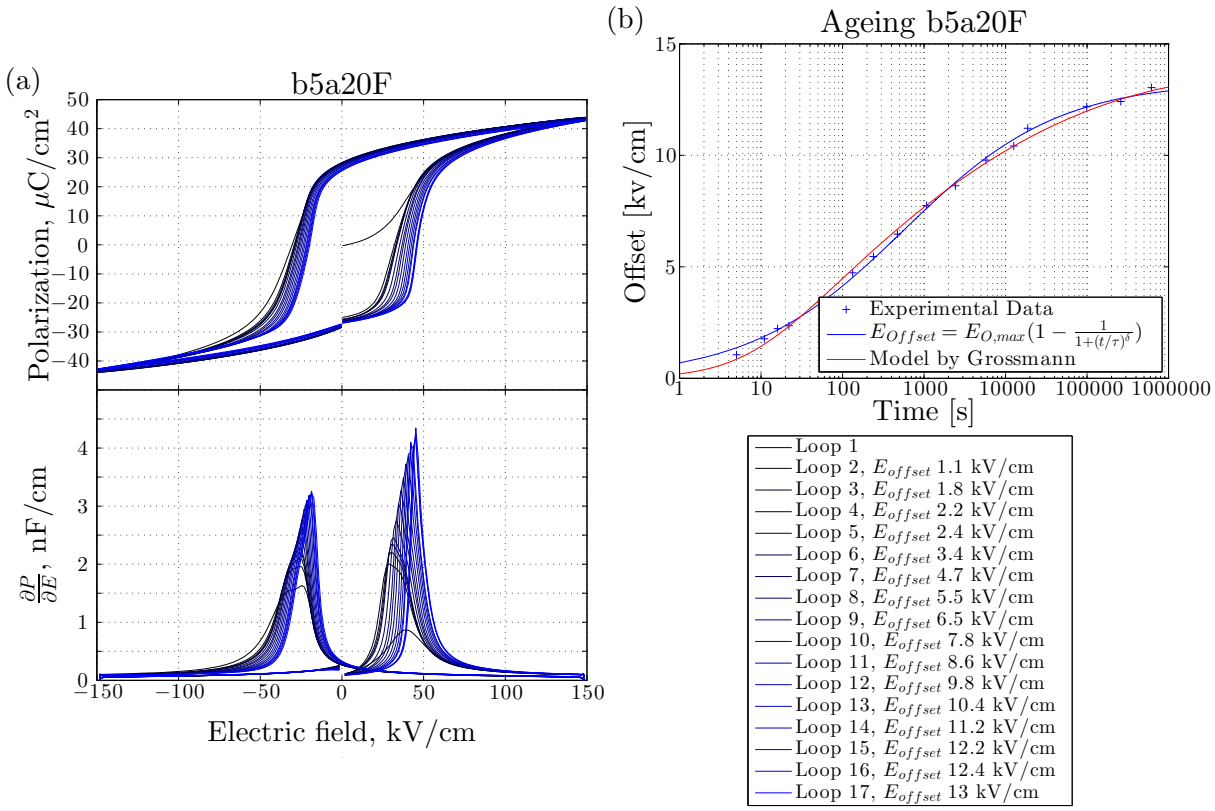


Figure 5.29: Ageing of sample b5a20F. (a) PV loops. (b) The offset measured from the loops in (a) plotted against time since the first measurement was initiated, with fits of the empirical function, and the model by Grossmann.

Grossmann. The value fond for δ_a appears large for being a passive layer at the interface, and is much larger than the about 5 nm found by Grossmann in [19].

In this model one would expect the offset after ageing for a set amount of time to be proportional to the thickness of the passive layer, and inversely proportional to the electrode spacing, as described in Section 2.7.2. In Figure 5.28 where the loops of 4 aged samples with different electrode spacing are shown, they are found to have very similar offset. If the model presented by Grossmann is correct, this means that the thickness of the dielectric layer must scale with the electrode spacing of the film.

It is unlikely that the thickness of a passive layer at the electrode interface would scale with the electrode spacing. The theory presented by Grossmann has therefore been reinterpreted to describe motion across a series of passive layers at the grain boundaries, rather than one passive layer at the electrode, as described at the end of Section 2.7.2. If one assumes an average grain size of 200 nm, one would expect about 85 grain boundaries between the electrodes in the case of a sample with 17 µm between the electrodes. Based on the thickness of the passive layer found by the the fit shown in Figure 5.29, this would indicate that a passive region at each grain boundary of about 0.35 nm. This is about the size of one unit cell, as the lattice parameter along the short axis, a, of tetragonal MPB PZT is about 0.404 nm and the lattice parameter on the long axis, c, is about 0.414 nm[42]. This seems reasonable, as grain boundaries are typically only one or a few unit cells thick.

One can evaluate if a passive layer with these parameters is expected to cause a slanting of the

loops. In the model discussed in Section 5.5, the slanting is dependent on the parameter $\frac{d}{a\varepsilon_d}$. With the values in Table 5.5, this parameter takes a value[15] $4.3 \cdot 10^{-6}$. The simulated loops with $\frac{d}{a\varepsilon_d}$ closest to this is shown in Figure 5.30, plotted there together with a loop with no simulated layer.

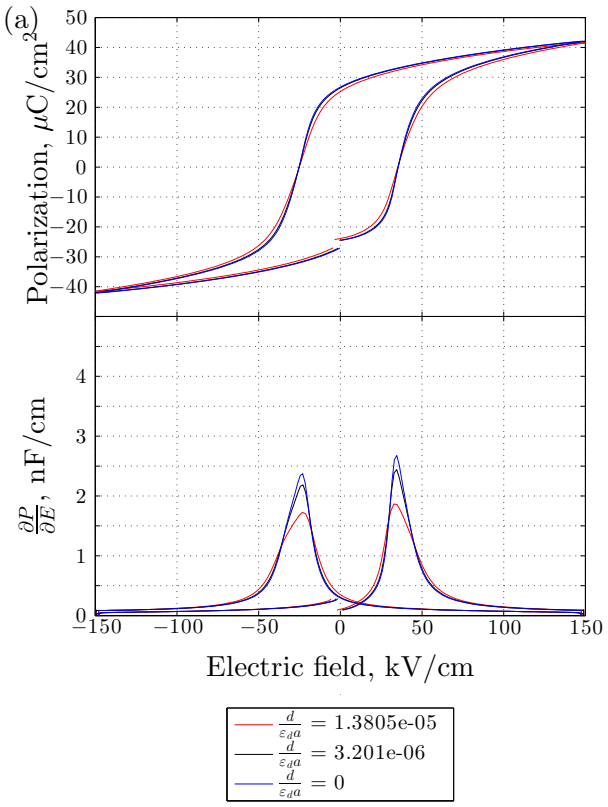


Figure 5.30: Simulated slanting caused by low value of $\frac{d}{a\varepsilon_d}$. The values from Table 5.5 is expected to have about the slanting of the black loop, and the black loop is close to indistinguishable from the blue loop with no passive layer.

It can be seen from Figure 5.30, that a passive layer with $\frac{d}{a\varepsilon_d} = 4.3 \cdot 10^{-6}$ would not be expected to cause significant slanting, and such a passive layer may in fact be present in all loops, as no loops are completely straight.

[15]Since the fit to Grossmann's model is not unique, one can re-balance ε_i, ε_{opt} and δ_a so that $\frac{d}{a\varepsilon_d}$ becomes smaller or larger.

Chapter 6

Conclusions

This work has led to significant advances in the understanding of the electric field in IDE structures. A method to simplify the Gevorgian model was developed, making it easier to carry out and interpret common ferroelectric measurements. Electrical characterisation of films with IDEs confirmed the validity of the numerical solution derived in this work. In this research, samples with electrode spacing less than 6 times the thickness have not been available, since all samples 'a4' were found to be short-circuited. Fabrication and analysis of such samples could be used to further validate the finding presented in this work.

Self-poling was observed in sapmles with partial SiO_2 cover. No other references to self-polarisation observed in IDE structures have been found, and it is believed that this work represents the first account of self-polarisation in IDE structures. The cause of self-polarisation is still not clear, but is thought to be related to charging of the surface during sputtering, and the introduction of oxygen vacancies. Further work should be focused on understanding the cause of self-polarisation, with basis in the fabrication process developed for this thesis.

Annealing samples at 650 °C was found to introduce a small self-poling. This was found to be the case in both reducing and oxygen atmosphere. The effect was too small to be of much practical significance, but supports the notion that oxygen vacancies are related to self-poling.

The PV-loops measured for as-fabricated samples showed slanted PV loops. These were compared to simulations of the effect of a passive layer at the electrode. Based on this it was shown that the slanting observed is not consistent with the effects of a passive layer, since the slanting does not scale as one would expect if a passive layer was present. Pinning of domain walls due to defects at the interface is seen as the most likely alternative explanation.

Ageing was characterised and fit to both an empirical and a theoretical model. Both models were able to fit the data well. Even though the theoretical model by Grossmann with passive layers at the electrodes was able to fit individual ageing curves well, the theory does not display the observed dependence on electrode spacing. It was therefore suggested that passive layers exist at the grain boundaries rather than at the electrodes. However, more theoretical work would be needed to describe this properly. The insight gained by fitting the ageing measurements to Grossmann's model is therefore qualitative and not quantitative in nature.

6.1 Further Work

Since the cause of self-poling has not been clearly identified, the fabrication route that produced self-polarisation should be replicated and varied. This will hopefully lead to a clear identification of the cause of self-poling.

Surface charge created during sputtering appears to be the most likely hypothesis to cause the self-poling shown in this work. Exposing samples to surface charge in other ways may also cause self-poling. Surface charge could for example be introduced by directing an electron flood gun on partially covered samples. An electron flood gun has a much simpler effect on the sample compared to electron plasma, and the results should therefore be more easy to interpret. Such an experiment could include a way to control the temperature of the sample, and possibly a way of grounding of the covered electrode.

PFM measurements could reveal more information on the switching kinetics, and could potentially reveal why as-fabricated samples show slanted loops and samples annealed at 550 °C do not. PFM is suited for studying IDE structures, as the sample has an exposed PZT surface, even after fabrication is finished. This is unlike the PPE structure, where the electrodes cover both the top and bottom and there is thus no exposed PZT surface. No previous study on IDE structures with PFM have been found.

The films used here are polycrystalline, and contain many grain boundaries. These grain boundaries were suggested as a possible cause of the ageing observed. It would therefore be very interesting to compare the results obtained here with results from epitaxial films. If epitaxial films show little or no ageing, it would go a long way to prove the hypothesis presented here with charge migration across grain boundaries.

Appendices

Appendix A

Optimisation of Process Flow

A total of 5 test wafers were produced. These were blank Si wafers, and did not have a PZT layer. Test wafers were produced since fabrication of high-quality PZT thin films it time consuming and has had in the past a limited success rate.[1] 3 test wafers were made using lift-off to pattern the SiO_2, and 2 wafers were made using etching. The target structures is shown in Figure A.1.

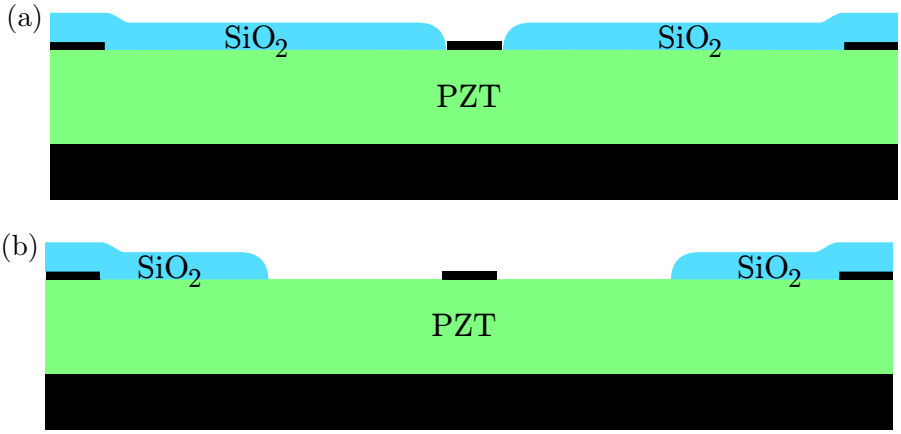


Figure A.1: Target structures for fabrication. The finished samples are designed to be annealed in oxidizing and reducing atmosphere, changing the composition of PZT in the exposed areas. Previous research have shown that the grain boundaries in the Pt electrodes can conduct oxygen, and the PZT under an exposed contact may therefore be changed during annealing[43]. The design in subfigure (a) requires precise alignment of the SiO_2 with the Pt electrodes. From geometric considerations one would aim for a misalignment less than the film thickness (500nm). Alignment is less important for the design in subfigure (b).

All test wafers have had Pt electrodes deposited using lift-off. For this purpose a mask was made using `Heidelberg VPG200` and this mask has been used for the electrodes on all wafers. This mask has also been used to make a wafer of control samples without any SiO_2.

A.1 Test Wafers Using Lift-off to Pattern SiO_2

The process flow for patterning the SiO_2 using lift-off is shown in figure A.2.

[1] Robin Nigon made 6 wafers with PZT thin films this winter, and obtained (100) textured ferroelectric PZT with a 100 % success rate. It is believed that this is due to the low ambient humidity while the MgO surface was exposed.

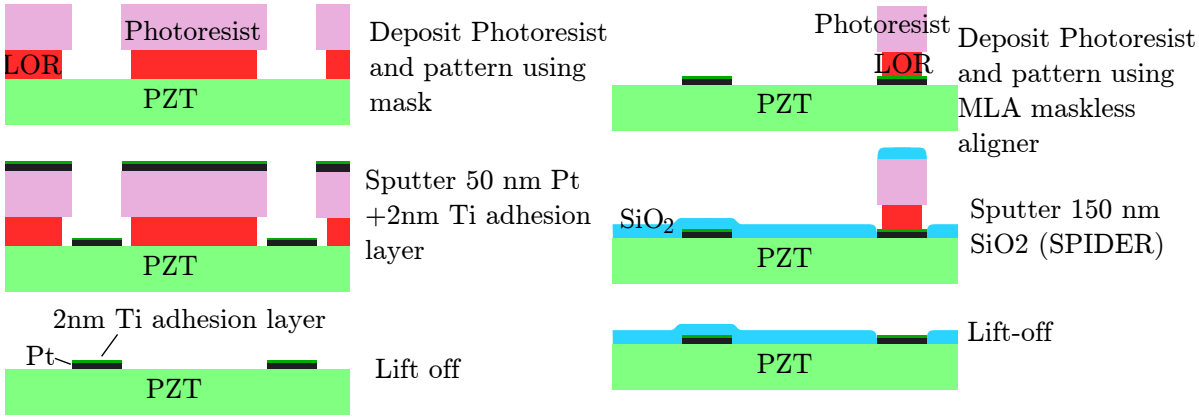


Figure A.2: Process flow for wafers using lift-off to pattern SiO_2. The left column shows the process flow for the Pt electrodes, while the right column shows the process the SiO_2 layer.

A.2 Wafer 51456

The first test wafer, labelled 51456, used a mask for the photolithography to pattern the SiO_2, and the mask was made using the `VPG200` . No Ti adhesion layer was used, and this caused the SiO_2 to delaminate from the Pt electrodes. It should also be noted that only 50 nm of SiO_2 was used. Images of this wafer can be seen in figure A.3.

The delamination observed caused the introduction of the Ti adhesion layer. It also became apparent that a new mask design would have to be made to reduce the overlap shown in figure A.3(b).

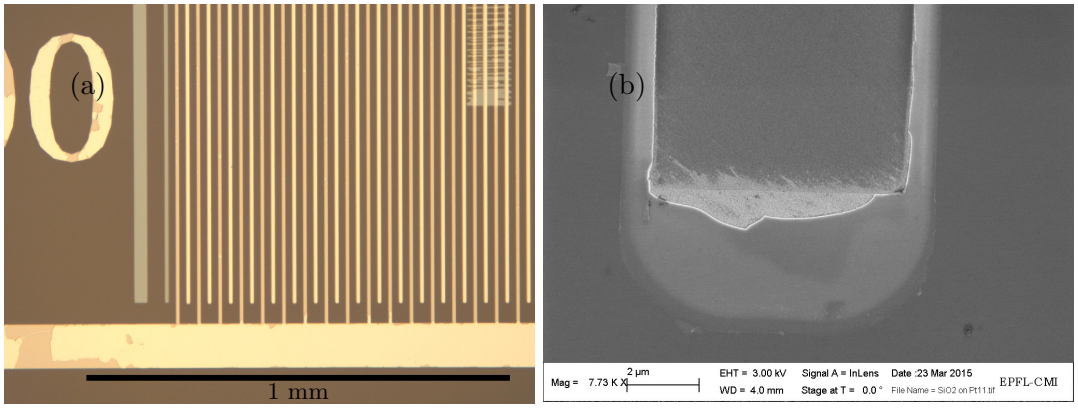


Figure A.3: (a) Micrograph of a sample, showing how the SiO_2 has delaminated from the branch leading to the finger structure. In the top right corner of the image there can also be seen a series of horizontal lines. These are an artefact introduced by the mask writer. (b) SEM image taken of the end of a finger. It can be seen from the image that the alignment is acceptable, but there is overlap of SiO_2 with the Pt on both sides of the finger.

A.3 Wafer 51495

Wafer 51495 along with wafer 51492 was made as a test to see if the new Heidelberg MLA 150 could be used instead of a mask for writing the pattern for SiO_2 deposition. Another feature of wafer 51495 is the use of 100 nm Pt and 10 nm Ti adhesion layer. The thickness of Pt was increased as a test, but was reduced back to 50 nm for the remaining test wafers to ensure good

step coverage for the SiO_2.

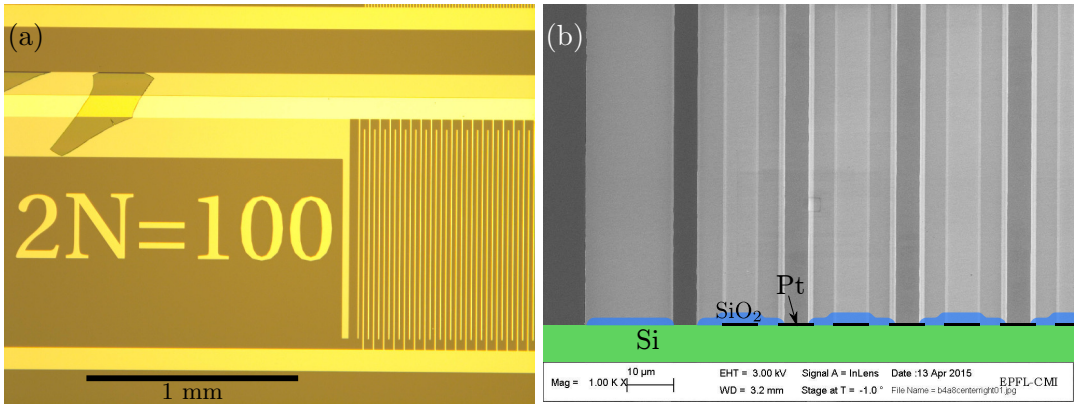


Figure A.4: (a) Micrograph from wafer 51495. There is no delamination of the SiO_2 due to the presence of the Ti adhesion layer. Some SiO_2 covered photoresist is remaining in the top left corner. (b) SEM image, showing overlap of SiO_2 with the Pt finger.

Figure A.4(a) shows a micrograph from wafer 51495. It can be seen that not all the SiO_2 has lifted off correctly, and some photoresist remains at the top left corner even after 4 days in remover. Figure A.4(b) shows a SEM micrograph of the sample, an overlap of the SiO_2 with the underlying Pt finger can be seen, this was used to calibrate the mask design.

A.4 Wafer 51490

Wafer 51490 was used to test the calibration done from the images of wafer 51495. The process flow follows figure A.2 exactly, and this process flow was also used for the PZT wafer.
It can be seen from Figure A.5(b) that the calibration was successful. However, since the lift off was so ineffective in large regions, many of the contact pads remained closed after lift-off. These contact pads were therefore opened using a third mask and an etching step, this can be seen in Figure A.5(a) and (b). The masks used are shown in Figure A.6.

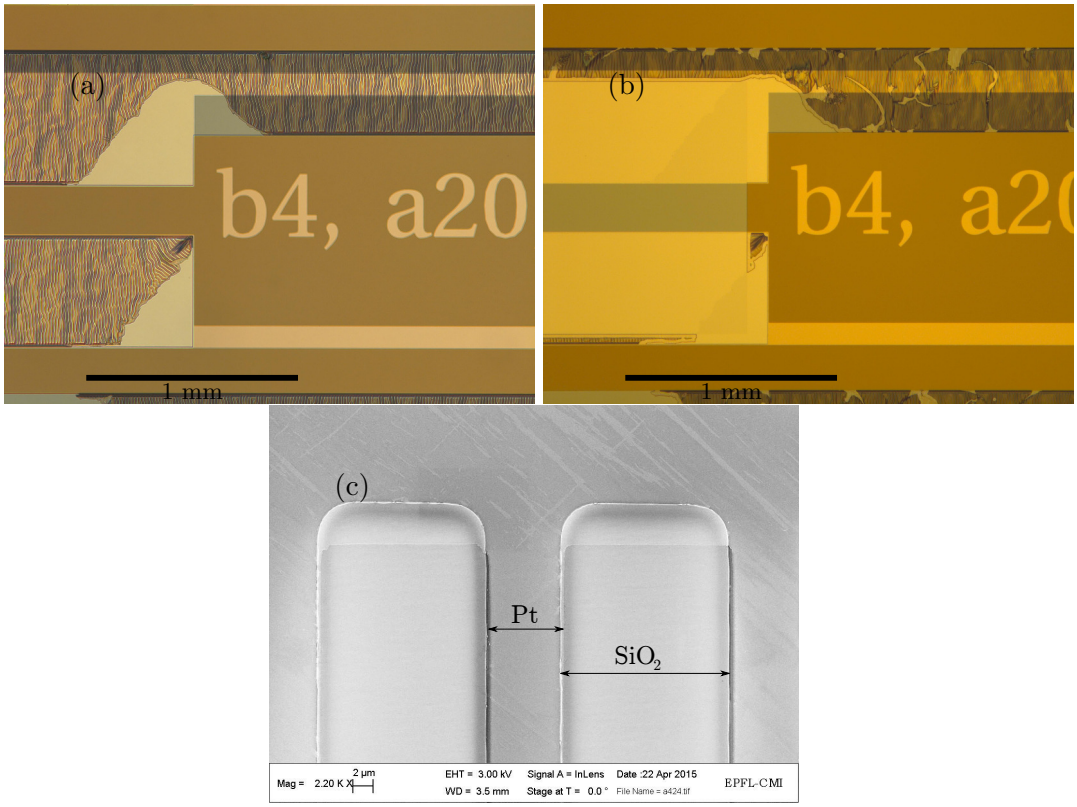


Figure A.5: (a) Micrograph from wafer 51490. The SiO_2 had not lifted off well from the contact region. (b) Photolithography has been used to selectively etch down to the contact pad. (c) SEM image, showing correct width of the SiO_2 after calibration, but approximately 200 nm misalignment.

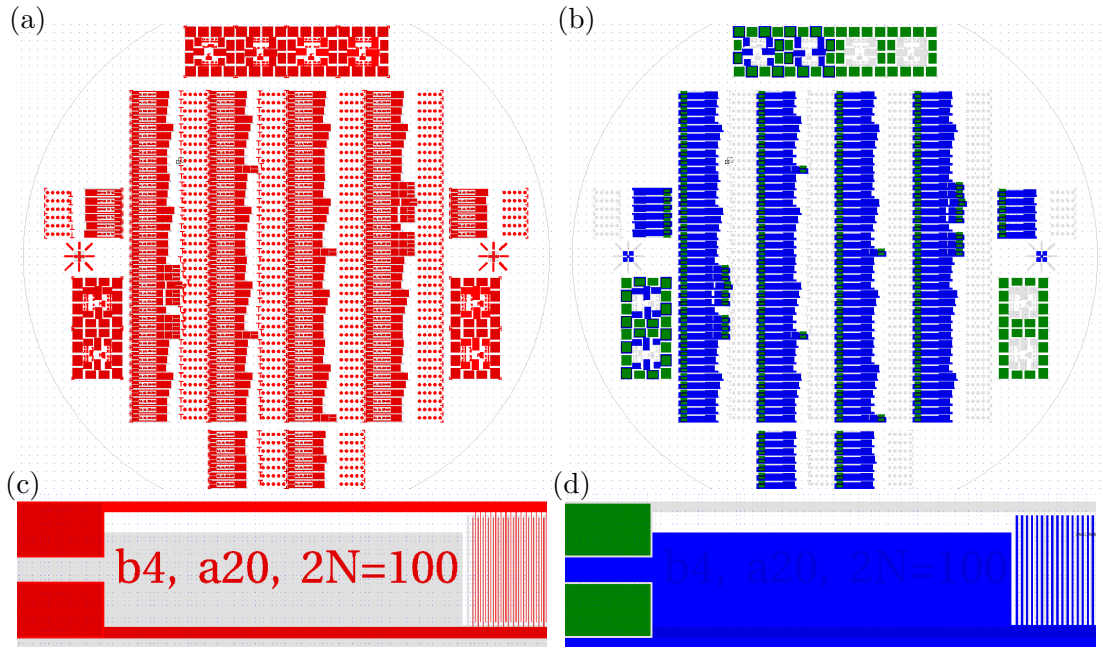


Figure A.6: Mask designs used. (a) Mask used for Pt electrodes. (b) Mask used for SiO_2 shown in blue, and mask used to etch down to the contact pads (green). (c) and (d) close up of a single sample showing individual masks. In this case the sample is designed to have a finger width of 4 µm, a gap of 20 µm, and 100 fingers in the interdigitated structure.

A.5 Etching Tests

Two test wafers were fabricated using etching to pattern the SiO_2. The process flow is shown in figure A.7.

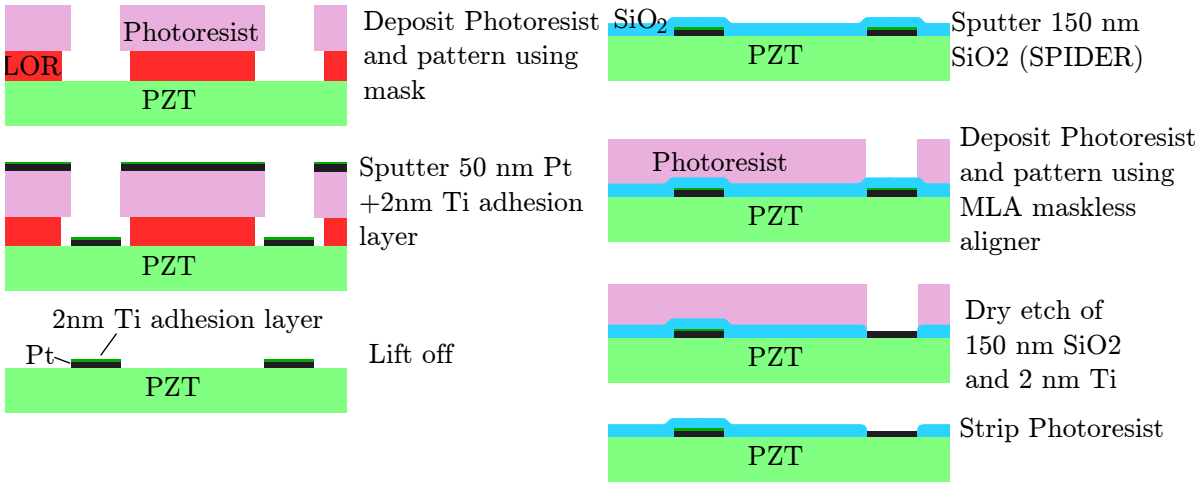


Figure A.7: Process flow for wafers using etching to pattern SiO_2. The left column shows the process flow for the Pt electrodes, and is the same as in Figure A.2, while the right column shows the process to pattern and deposit the SiO_2 layer.

The advantage of this process flow is that the Ti adhesion layer will be removed along with the SiO_2 during etching. This may be important, as it is believed that the Pt grain boundaries allow the passage of oxygen, but the Ti layer may block this. All photolithography for etching was done on the `Heidelberg MLA 150`.

A.6 Wafer 51492

This wafer was made using the process flow shown in Figure A.7, but used a 10 nm Ti adhesion layer rather than the 2 nm listed, and only 50 nm SiO_2. The wafer suffered from delamination of the photoresist due to bad adhesion on the SiO_2.

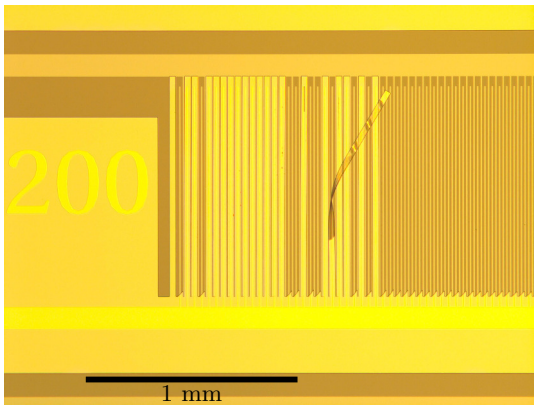


Figure A.8: Micrograph from wafer 51492 with photoresist before etching. Delamination of the photoresist can be seen.

A.7 Wafer 51491

This wafer was made according to the process flow of Figure A.7, and the etching mask was calibrated based on SEM images of wafer 51492. To prevent delamination of the photoresist, the SiO_2 was primed in oxygen plasma. A SEM image of a Pt finger surrounded by SiO_2 on both sides is seen in Figure A.9.

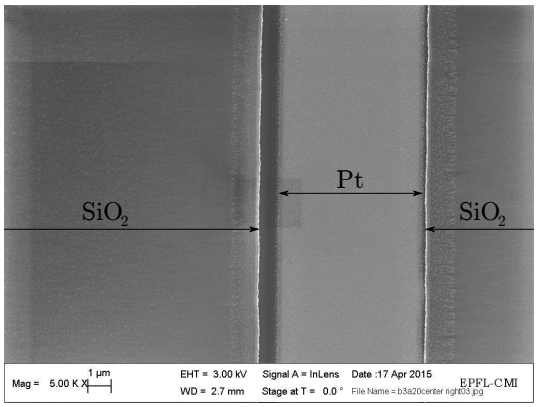


Figure A.9: SEM image from wafer 51491, showing approximately 200 nm misalignment. The opening in the SiO_2 also appears to be approximately 600 nm too wide. The edge of the Pt finger also appears to be less sharp than in the samples prepared by lift-off, possibly due to the damage from etching.(needs labels)

Wafer 51491 also revealed that 40 s of plasma etching using the SPTS in 'soft' mode was not sufficient to etch 150 nm SiO_2. This is despite the fact that the etch rate is listed as 350 nm/min, and could be due to an unspecified time required to ignite the plasma. The SPTS is designed to be manually stopped by the operator based on continious spectroscopy of the gases pumped out of the chamber, but this is difficult to control for short times. Since the SiO_2 coverage is not even, it must also be expected that the underlying layers will also be etched, at least in some parts of the wafer.

A.8 The 'Ramin' process flow

Ramin Matloub Aghdam suggested the following process flow, where the same photolithography is used first to etch the SiO_2 and then to deposit the second Pt electrode. The etching step may still damage the PZT, and in this case Pt will be deposited onto the damage surface. This process flow has not been tested for this reason.

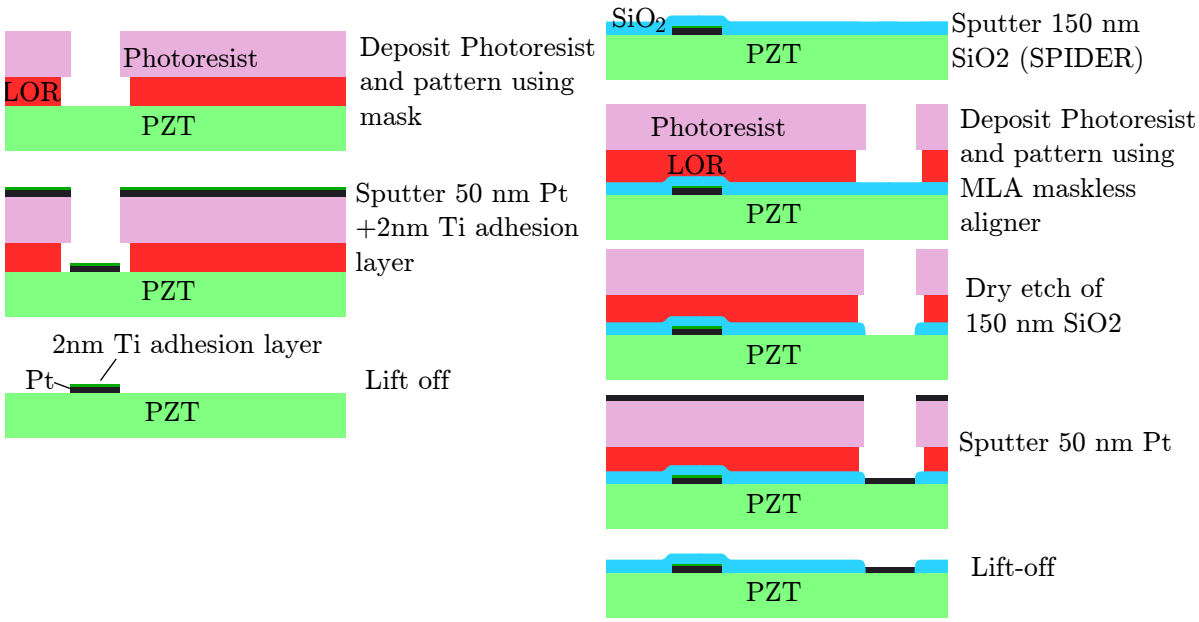


Figure A.10: The Ramin process flow, where one electrode is deposited after etching the SiO_2 to provide perfect alignment.

Appendix B

Etching Tests

Previously fabricated samples (with Pt electrodes, but no SiO_2) were etched for 15 or 30 s in the SPTS. The ramp time of the SPTS is not known, and may be as long as 10 to 15 s.

B.1 Samples from wafer 3347

Two samples from wafer 3347 were etched. Wafer 3347 is made with tetragonal PZT (morphotrophic composition is used in all other samples in this thesis), and the samples had previously been measured. The samples were rejuvenated by annealing at 550 °C under 100 sccm oxygen flow for 10 minutes, measured and rejuvenated again before being placed in the SPTS for 30 s. They were then measured, rejuvenated and measured again. The results are shown in Figure B.1.

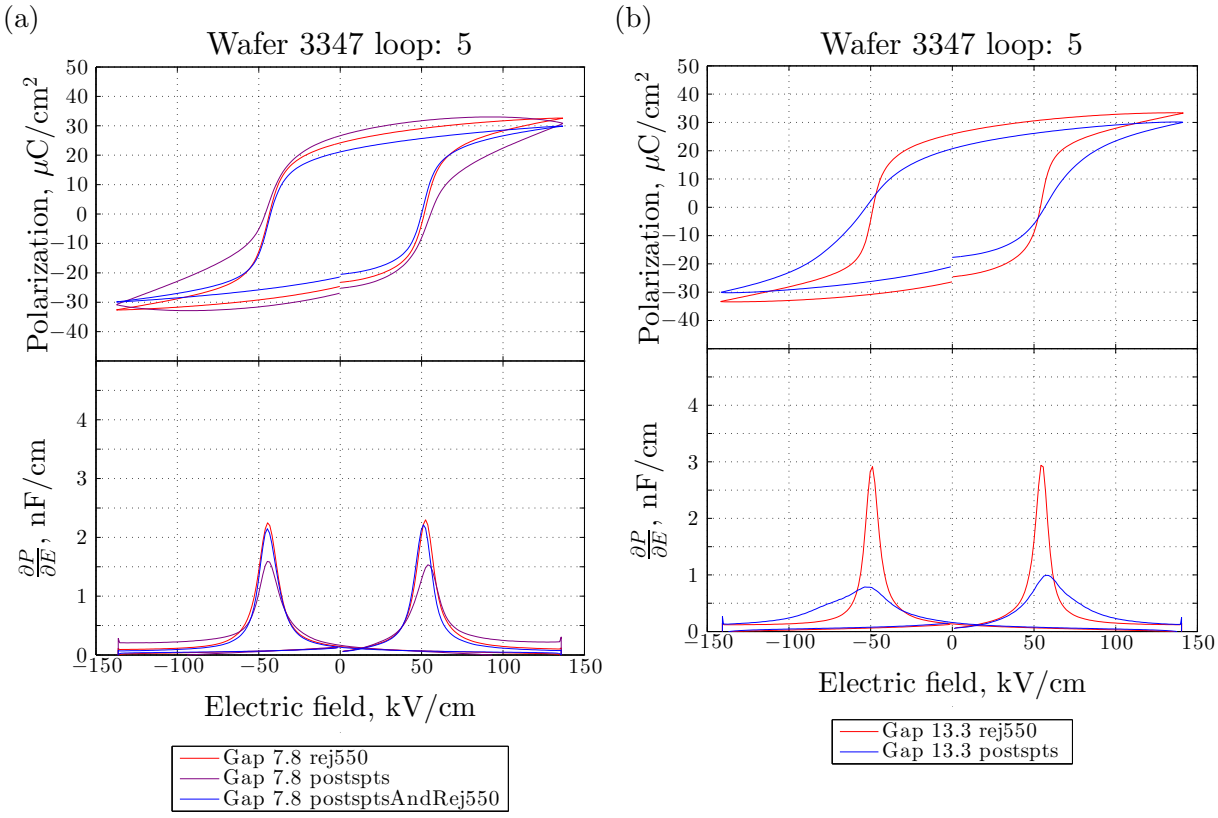


Figure B.1: Results from SPTS tests on samples from wafer 3347. The fifth PV loop in a series is shown. The sample in (b) broke down after the third rejuvenation step.

From figure B.1 a large leakage can be seen directly after etching, and this is reduced by anneal-

ing. A drop in maximum polarisation can also be seen, and this is not recovered by annealing. The drop in max polarisation was thought to be either from the etching itself, or from delamination of Pt fingers as a result of the etching. If the cause was delaminated fingers, then these could be counted and the results could have been corrected. Both samples showed broken fingers, but no high resolution micrographs of the samples were captured before etching, so it is not known if these fingers were broken also prior to etching.

B.2 Samples from wafer 47643

A total of 4 samples from wafer 47643 were etched in the SPTS. Two samples were etched for 15 s, and these samples show increased leakage, but little or no drop in maximum polarisation. The leakage was reduced back to normal levels after annealing for 10 minutes at 550 °C in 100 sccm of oxygen.
Results from samples etched for 30 s is shown in Figure B.2.

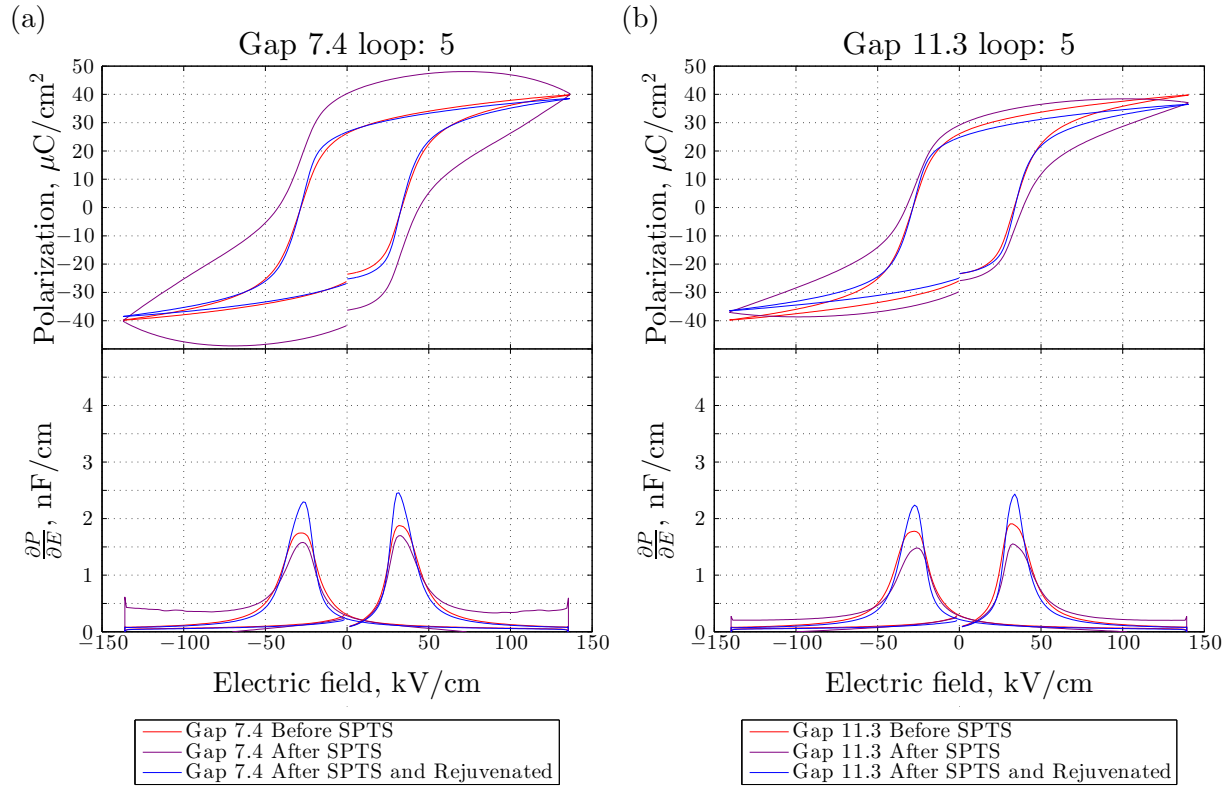


Figure B.2: Results from SPTS tests on samples from wafer 47643. Increased leakage is found after the SPTS, and the maximum polarisation is decreased. The maximum polarisation is not recovered after annealing at 550 °C.

The trend seen in Figure B.2 is the same as in figure B.1, and by consulting micrographs it is confirmed that the drop in maximum polarisation is not due to broken fingers, but rather due to damaged to the PZT. AFM was used to investigate this damage, and an image of the surface is shown in figure B.3
From the figure it can be seen that that the PZT has been severely damaged, and has been etched by 50 nm. Interestingly, this damage only occurs at distances more than 1.5 μm away from the Pt electrode. This could be due to charging of the Pt electrode that shields the nearby PZT from the plasma.
After the AFM images were captured, it was clear that etching should be avoided, and lift-off became the obvious choice for fabrication. However, the SPTS may be used in further research

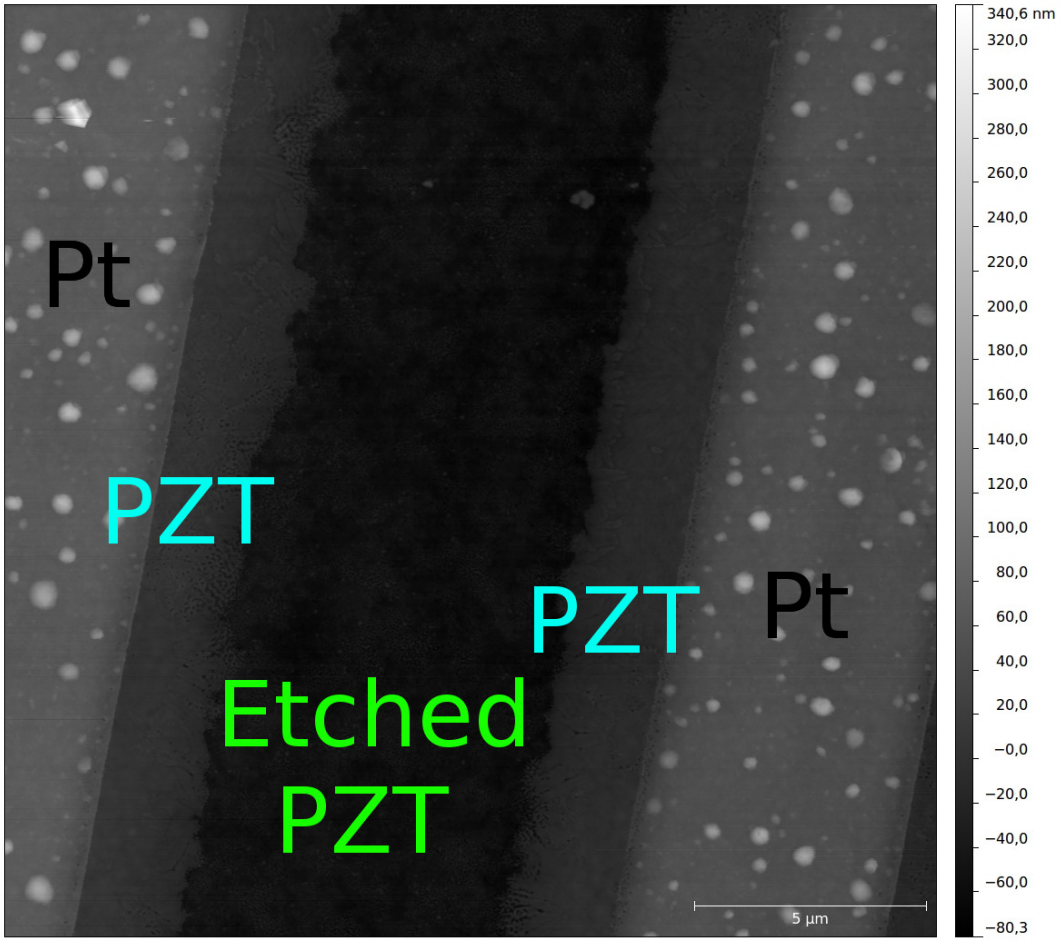


Figure B.3: AFM image showing a trench in the PZT that has been etched by approximately 50 nm. This region also shows increased surface roughness. The trench starts approximately 1.5 µm away from the Pt electrode.

to etch the region around one of the electrodes, to provide an asymmetry and possibly an offset or self-poling.

Appendix C

Parasitic Capacitance

This chapter has been copied in its entirety from [1], and is reproduced here because of its relevance for the new samples.

Previous results have shown that a parasitic capacitance is present in the system. A model has therefore been introduced where the Si substrate is assumed to be conducting with a resistivity of 15-25 Ωcm.

In this model, each contact is modelled as a parallel plate capacitor connected to the substrate. Between the contact and the substrate there is a ≈0.5μm PZT layer, a 100 nm MgO layer, and a 2.0μm SiO_2 layer. The capacitance of this stack is dominated by the SiO_2 layer since this has a much lower dielectric constant. A resistance is modelled between the capacitors to account for the resistivity in the substrate. This is shown in figure C.1.

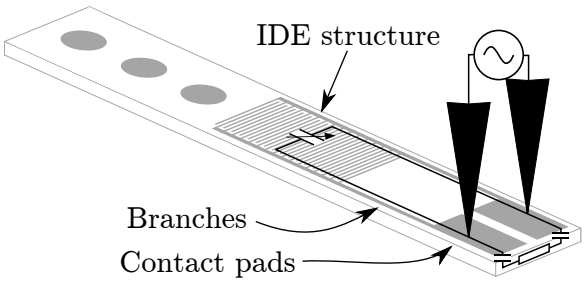


Figure C.1: Schematic drawing of a sample with a simple model of the circuit superimposed. The IDE structure is shown as a variable capacitor, and a parasitic circuit is shown between the contact pads.

A circuit consisting of capacitors and resistances in series will have a large frequency dependence around the cut-off frequency defined by the RC time constant in the following way:

$$f_c = \frac{1}{2\pi\tau} = \frac{1}{2\pi RC} \tag{C.1}$$

Where τ is the RC time constant, R is the resistance in the system, and C is the capacitance of the system. For frequencies smaller than f_c, charge has time to flow through the resistor and the voltage drop occurs over the capacitors. In this case the resistor can safely be neglected.

A conservative estimate of f_c can be made by calculating the resistance between the center of the electrodes:

$$R = \frac{w_0 + b_0}{t_{Si} a_0} \rho \tag{C.2}$$

$$C = \frac{1}{2} \varepsilon_{SiO_2} \frac{b_0 a_0}{t_{SiO_2}} \tag{C.3}$$

$$f_c = \frac{1}{\pi} \frac{t_{Si}}{(w_0 + b_0)\rho} \frac{t_{SiO_2}}{b_0 \varepsilon_{SiO_2}} \tag{C.4}$$

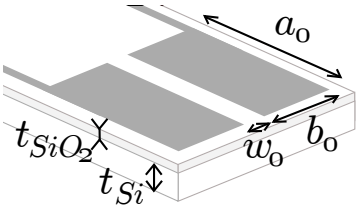


Figure C.2: Labels of sample dimensions.

Using the sample parameters of $a_0 = 1300\mu m$, $b_0 = 500\mu m$, $w_0 = 150\mu m$, $t_{Si} = 500\mu m$, $t_{SiO_2} = 2\mu m$, $\varepsilon_{SiO_2} = 4\varepsilon_0$ and $\rho = 20\Omega cm$, Equation C.4 gives $f_c = 138MHz$.

Since the CV measurements are carried out at 1kHz, the resistance from the substrate can be safely neglected. Equation C.3 estimates the parasitic capacitance to be 5.8pF. This is one order of magnitude below the capacitance typically measured in CV measurements, and therefore significant.

One can expand this model to include capacitance under the conductors going to the IDE structure. These conductors have a length of 3700µm, and a width of 100µm, leading to an additional parasitic capacitance of 3.3pF.

Additional parasitic capacitance will be present under the branches at the base of the electrodes, and this capacitance depends on the number of electrodes, electrode width and gap spacing.

C.1 Effect of Parasitic Capacitance on PV loops

Polarisation is measured as charge over area, as shown in Equation C.5, and a parasitic capacitance will lead to an overestimate of the polarisation if it is not corrected for:

$$P_{\text{measured}} = \frac{Q_{\text{measured}}}{A} \tag{C.5}$$

Where Q is charge and A is area. The measured charge includes contributions from the parasitic capacitance as well as the PZT in the following way:

$$Q_{\text{measured}} = Q_{\text{PZT}} + Q_{\text{parasitic}} = Q_{\text{PZT}} + VC_{\text{parasitic}} \tag{C.6}$$

Using Equation C.5 and C.6 the measured polarisation can be corrected in the following way[1]:

$$P_{\text{corrected}} = \frac{Q_{\text{PZT}}}{A} = P_{\text{measured}} - \frac{VC_{\text{parasitic}}}{A} \tag{C.7}$$

C.2 Effect of Parasitic Capacitance on CV loops

For CV loops, the measured capacitance is the sum of the parasitic capacitance and the capacitance of the IDE structure. The capacitance can be corrected in the following way:

$$C_{\text{IDE structure}} = C_{\text{measured}} - C_{\text{parasitic}} \tag{C.8}$$

[1]The measurement apparatus used records the derived parameter P rather than the measured parameter Q. For this reason, equation C.6 is written as $P_{corr} = P_{meas} - \frac{VC_{paras}}{A}$ rather than the equivalent $P_{corr} = \frac{Q_{meas} - VC_{paras}}{A}$.

This can then be used to calculate the dielectric constant in the following way:

$$\varepsilon_{r,\mathrm{PZT}} = C_{\text{IDE structure}}\frac{\mathrm{a}}{\varepsilon_0 A} = (C_{\text{measured}} - C_{\text{parasitic}})\frac{\mathrm{a}}{\varepsilon_0 A} \tag{C.9}$$

Where a is the electrode spacing.

C.3 Validation

To validate the predictive model of parasitic capacitance, several samples were cleaved between the contact pads and the finger structure. The capacitance of these samples were then measured using an `Agilent 4294A Precision Impedance Analyzer` at 5V, scanning frequencies from 40 Hz to 100 MHz. It was confirmed that the capacitance is stable up to the MHz range (i.e. stable in the range where other measurements are done) and the capacitance at 1kHz was recorded. The results can be seen in Figure C.3.

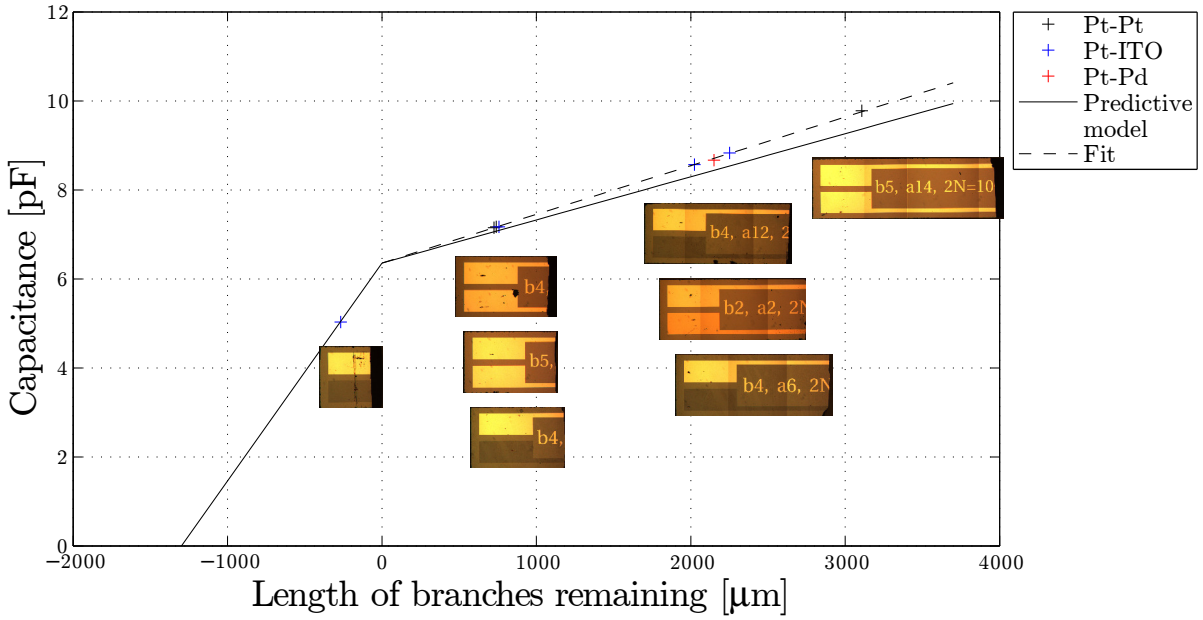


Figure C.3: Plot of measured parasitic capacitance. The solid line represents the predictive model and the dashed line shows a fit of the data points.

As Figure C.3 shows, the predictive model is not accurate, and the parasitic capacitance is higher than predicted. The reason has not been found but an empirical fit (dashed line in Figure C.3) has been used to correct PV and CV loops.

Appendix D

Characterisation of Electrode spacing

The following is a description of the `Matlab` function used to automatically measure the electrode spacing from images. This section is an excerpt from [1], and is reproduced here since this function is still in use.

The function will rotate the image so that all the fingers are parallel to the image y-axis, and sum the pixel value in each column to produce a vector of average intensities. The red image channel is found to have superior contrast, and only this channel is analysed by the program. An exception is made for the Pt-Pd samples, where the blue channel is used to separate Pt fingers from Pd fingers. The function identifies plateaus in the intensity vector, and produces a fit as shown in Figure D.1. This fit is used to determine the finger width and spacing.

To validate the use of this function, a comparison is made by measuring the same images manually and by using the function. A total of 8 images are captured of a singe sample but in different locations. 4 micrographs are taken at 500x zoom, and 4 are captured at 1000x zoom. All images are then measured using the function. The function produced 6 finger widths and 6 gap widths as output for each images, providing 48 data points at each level of zoom. This process is then repeated manually, and the results are compared. The results are presented graphically in Figure D.2.

It is seen from Figure D.2 that the variance is lower when using the function compared to manual measurements. It can also be seen that manual measurements of the finger widths tend to give wider estimates. This may be due to chromatic aberrations that makes the finger appear wider when viewing a RGB image for manual measurements, as compared to the script that only considers the red channel. Since the average values obtained by the script for 500x zoom deviates from the measurements done by hand, and this deviation is less for the images taken at 1000x zoom, 1000x zoom was considered to be the most reliable method for measuring samples. This choice was made despite the fact that the variance is smaller for 500x zoom.

As the quality of data obtained was found to be satisfactory, no further study is done to identify the discrepancies between the measurements in `Matlab` and the manual measurements. It should be noted that from visual inspection of the images, it is clear that some variance in finger width is produced by the deposition, and it is not known how much of the variance shown in Figure D.2 comes from inaccurate measurements, and how much comes from actual variance in finger width.

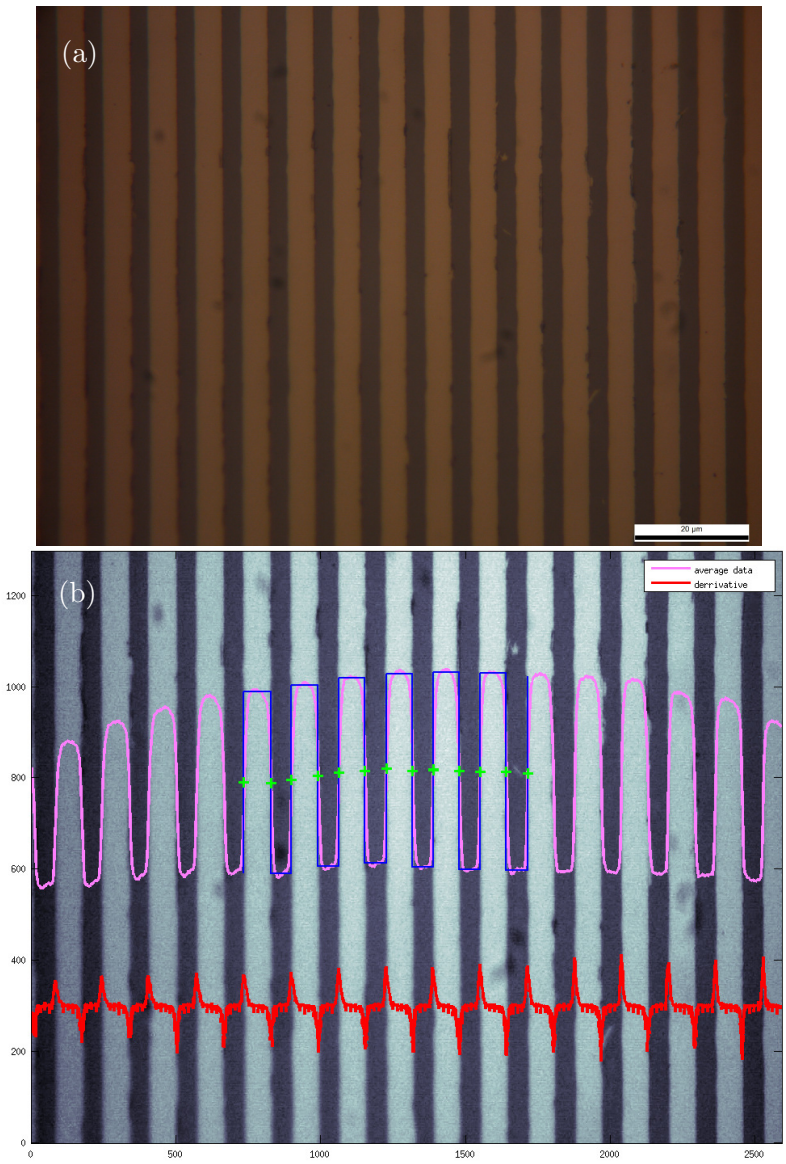
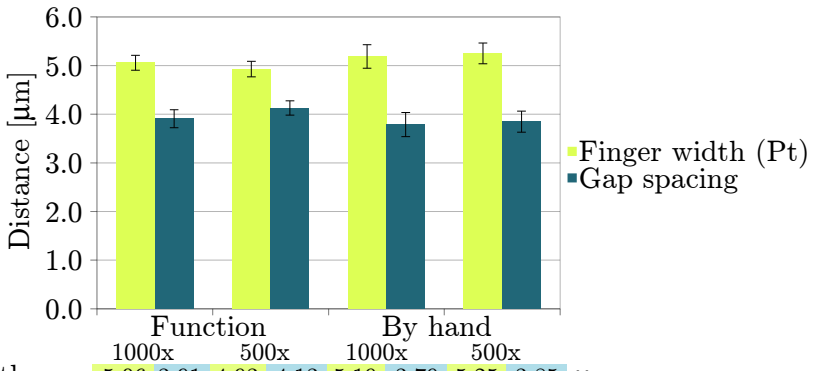


Figure D.1: Image of a Pt-Pt sample with finger width of 5μm and spacing of 4μm. (a) shows the image as taken by the microscope, while (b) shows the graphic produced by the function. Note the absence of the original scale bar in (b) since the image has been cropped. Also note that (b) is rotated and has a distorted aspect ratio. Superimposed on the image data in (b) is shown the average columnar data (pink) as well as its derivative (red). The blue line shows the fit produced by the script while the green crosses indicate where the blue and pink lines intersect. The function gives the distance between the green crosses as output.



Average width	5.06	3.91	4.93	4.13	5.19	3.79	5.25	3.85	µm
Standard deviation	0.15	0.18	0.16	0.15	0.24	0.25	0.21	0.22	µm

Figure D.2: Comparison of results from the Matlab function and manual measurements of finger width and spacing. Each bar represents 24 data points and has a height equal to the average value while the error bar shows the standard deviation. The data is reproduced as a table below the graphs.

Appendix E

Original Proposal

The original proposal of this thesis was to produce a P-N junction in PZT. P-N junctions are well known from semiconductor physics, and are associated with a built-in electric field. It was thought that such a field could be used to produce self-poled samples.

P-N junctions in silicon are typically made by implanting ions into the lattice. As PZT is an oxide, it was thought that a P-N junction could instead be made in PZT by controlling oxygen vacancies. Sol-gel PZT is believed to be P-type when fabricated, and increasing the amount of oxygen vacancies by annealing in reducing atmosphere would make it n-type, as electrons are released by the following reaction:

$$O_O^x \rightarrow V_O^{**} + 2e^- + \frac{1}{2}O_2(g) \tag{E.1}$$

An SiO_2 cover was then designed so that only part of the sample would be affected by annealing in reducing atmosphere, and the uncovered region was expected to become N-type. As the covered region remained P-type, a P-N junction was expected to form, as shown in Figure E.1.

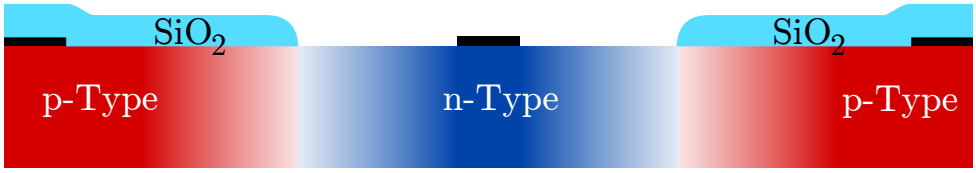


Figure E.1: Illustration of a PN junction formed by doping the region around the uncovered electrode with oxygen vacancies.

As samples were fabricated and measured, only minor self-poling was observed after annealing in reducing atmosphere, while a larger self-poling was found in as-fabricated samples. The small self-poling observed after annealing in reducing atmosphere was also of opposite sign compared to what would be expected if the self-poling was caused by a P-N junction. The topic of this thesis then shifted towards identifying the cause of the observed self-poling in as-fabricated samples.

When oxygen leaves the surface, oxygen vacancies and electrons appear in the lattice according to Equation E.1. The oxygen vacancies and electrons then form a dipole. A P-N junction can form if the electrons diffuse to a P-type region, and annihilate in contact with a hole. If the electrons do not move to the p-type region, then the P-N junction will not form, and instead an electric field is formed between the oxygen vacancies and the electrons. This may be one explanation as to why the self-poling did not appear as expected. Another explanation would

be that oxygen vacancies are instead formed by evaporation of PbO, and as no electrons appear in the lattice as PbO evaporates, a P-N junction cannot form.

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