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Three 10W C-band Power Amplifier Alternatives for use in TT&C-Transmitters

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Abstract

This thesis describes the first stage in designing and realizing three 10W C-band power amplifier alternatives based on the GaN-technology for use in Kongsberg Norspace' future TT&C-transmitters. The operational frequency range spanned from 3.4GHz to 4.25GHz. It was decided to build one single-stage amplifier based on the 10W CGH40010F transistor from Cree and two dual-stage amplifiers with a balanced second stage based on the 6W CGH40006P transistor, from the same manufacturer. A Wilkinson power divider was used to feed each branch in the second stage.

In the design procedure, source and load pull simulations were performed in order to retrieve the optimal impedances for each transistor and as a basis for the design of the matching networks. By utilizing a looping method in the design process of the matching networks, it was possible to obtain results that, to some extent, fulfilled the requirements. Simulations and design were carried out in ADS by Keysight (former Agilent).

The simulated results showed that all three designs were capable of delivering 10W output power throughout the frequency band. The single-stage amplifier obtained a simulated power added efficiency (PAE) above 45% at 40dBm output power, while the two dual-stage designs achieved a PAE between 41-44% and 34-36%, respectively.

S-parameter simulations reviled that the single-stage design accomplished a small signal gain of 11.3dB-11.7dB, while the input reflection coefficients varied between -3dB and -5dB. To achieve the requirement of having the input reflection coefficients less than -10dB, the dual-stage designs utilized an attenuator with 1.5dB loss at the input match, both designs obtained a small signal gain above 20dB.

Like the simulated results, the large signal measurements showed that the amplifiers were capable of delivering 10W output power, except the single-stage design at 4.0375GHz (which were one of the test frequencies). The measured power added efficiency for the single-stage amplifier varied between 27%-44%, while the two dual-stage amplifiers obtained a PAE between 39-43% and 35-42%, respectively. This implied that non of the designs managed to fulfill the requirement of having a total power consumption less than 25W over the specified frequency range.

A simulated large signal stability analysis were performed on each design and the results revealed that one of the dual-stage designs had a potential instability around 790MHz, and practical spectrum measurements confirmed frequency components at 750MHz, 1.51GHz and 2.25GHz. However, the spurious frequency components had no measurable impact on the performance.

A small section presenting the future prospects in terms of utilizing the GaN-technology in Space and suggestions for future work, have also been included.

The thesis concluded that several iterations must be done before an integration with the transmitter can be made.

Sammendrag

Denne masteravhandlingen beskriver det første steget i å designe og realisere tre 10W C-bånd effektforsterkeralternativer basert på GaN-teknologien for bruk i Kongsberg Norspace' fremtidige TT&C-sendere. Den operasjonelle bndbredden spente fra 3.4GHz til 4.25GHz. Det ble bestemt å lage en ett-trinns effektforsterker basert på 10W CGH40010F transistoren fra Cree, og to to-trinnsforsterkere med et balansert utgangstrinn basert på 6W CGH40006P transistoren, fra den samme fabrikanten. En Wilkinson effektdeler ble brukt for å mate hver gren i andre-trinnet.

I designprosessen ble det utført source og load-pulling for å finne de optimale impedansene for hver transistor og som en basis for utformingen av tilpasningsnettverkene. Ved å benytte seg av loop-metoden i designeprosessen av tilpasningsnettverkene ble det mulig å oppnå et resultat som, til en hvis grad, tilfredsstilte kravene. Simulering og utformingen av forsterkerene ble utført i dataprogrammet ADS fra Keysight (tidligere Agilent).

Simuleringsresultater viste at de tre designene hadde alle mulighet til å levere en effekt på 10W på utgangen gjennom hele frekvensbåndet. Ett-trinnsforsterkeren oppnådde en power added efficiency (PAE) på over 45% ved 40dBm utgangseffekt, mens to-trinnsforsterkerene henholdsvis hadde en PAE mellom 41-44% and 34-36% ved samme uteffekt.

S-parametersimuleringer viste at ett-trinnsdesignet oppnådde et småsignalgain mellom 11.3dB-11.7dB, samtidig som refleksjonskoeffisientene på inngangen varierte mellom -3db og -5dB. For å oppnå kravet på -10dB til refleksjonskoeffisientene på inngangen, ble to-trinnsforsterkerene designet med et 1.5dB dempeledd på inngangsmatchen. Småsignalgainet for to-trinnsforsterkerene var begge over 20dB.

I likhet med de simulerte resultatene, viste de målte resultatene at alle tre design klarte å levere 10W, bortsett fra ett-trinnsdesignet ved frekvensen 4.0375GHz (som var en av testfrekvensene). Målt PAE for den samme forsterkeren varierte mellom 27%-44%, mens to-trinnsforsterkerene oppnådde en effektivitet på henholdsvis 39-43% and 35-42%. Disse resultatene viser at ingen av forsterkerene klarte kravet til effektbruk på maksimalt 25W.

Det ble også foretatt en simulert storsignal stabilitetsanalyse på hvert av designene noe som førte til at mulige ustabiliteter ble påvist i et av to-trinnsforsterkerene rundt 790MHz. Praktiske spektrumsmålinger bekreftet frekvenskomponenter ved 750MHz, 1.51GHz og 2.25GHz, men disse uønskede frekvenskomponentene hadde ingen målbar innvirkning på ytelsen.

Et avsnitt som presenterer fremtidsutsiktene på bruk av GaN-teknologien i verdensrommet og forslag til fremtidig arbeid er også tatt med.

Avhandlingen konkluderer med at flere designiterasjoner må bli gjort før man kan integrere en forsterker med senderen.

Preface

This thesis is submitted for the degree of Master Of Science (MSc) at the Department of Electronics and Telecommunications, Norwegian University of Science and Technology (NTNU). The work was carried out in the period January to June 2015 under the supervision of associate professor Morten Olavsbråten (NTNU) and Stein Hollung, principal RF design engineer at Kongsberg Norspace AS. The assignment was given by Kongsberg Norspace.

First, I would like to thank Kongsberg Norspace for giving me the opportunity to work with the topic of RF power amplifiers and Stein Hollung for support and providing me with equipment. I would also like to thank my supervisor, Morten Olavsbråten for assisting me and as a source for motivation during this work. In addition, I would like to thank Tore Landsem and Tore Berg at the mechanical workshop together with Terje Mathiesen and his crew for cutting the heat sink and producing the PCB's, respectively.

A special thanks to my friends and fellow students for five fun and unforgettable years. And last but not least, a special thanks to Maren and my family.

Trondheim, Norway, June 2015
Fabian Eckholdt

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Abbreviations

ADS	=	Advanced Design System
CAD	=	Computer-Aided Design
CNC	=	Computer Numerical Control
DC	=	Direct current
DUT	=	Device under test
ESA	=	European Space Agency
GaAs	=	Gallium Arsenide
GaN	=	Gallium Nitride
HEMT	=	High Electron Mobility Transistor
MMIC	=	Monolithic Microwave Integrated Circuit
NASA	=	National Aeronautics and Space Administration
PA	=	Power amplifier
PAE	=	Power Added Efficiency
PCB	=	Printed Circuit Board
RF	=	Radio Frequency
SiC	=	Silicon Carbide
SNA	=	Signal Network Analyzer
S-parameters	=	Scattering parameters
SOLT	=	Short, Open, Load, Thru
TT&C	=	Telemetry, Tracking and Command
VNA	=	Vector Network Analyzer

Chapter 1

Introduction

This chapter will present the motivation and goal of the project, but to put it all into context, the chapter starts with a brief description of the system in which the final power amplifier is going to be a part of. At the end of the chapter, the overall requirements are presented in addition to an overview of each chapter.

1.1 Telemetry, tracking and command system

From the second a satellite leaves the earth to the end of its life, the telemetry, tracking and command (TT&C) subsystem monitors the condition, executes commands and transmits and receives messages between itself and the Earth. Regardless of application, every satellites needs such a system.

In more detail, the telemetry part collects health information (e.g. battery status, charging cycles and temperature in critical components) from the different submodules of the satellite, before it encodes the data and transmits it back to Earth. The transmitter uses the time division multiplexing technique to combine the different sensor signals.[1]

The command subsystem, on the other hand, receives and decodes the messages before they are forwarded and executed in the correct submodule. The telemetry and command subsystem are said to have complementary functions.

By using angle, range and velocity information the tracking module are able to determine the satellite's orbital parameters. This helps to maintain the satellite in the right position and the ground control center to point the antennas in the optimal direction.[1]

1.2 Motivation and goal

Kongsberg Norspace AS (Norspace) have established themselves as one of the world leading suppliers of on-board satellite electronic equipment. And to retain this position, Norspace have now started to investigate the possibility of using transistors based on the gallium nitride (GaN) technology to work as the active component in a power amplifier

Figure 1.1: Kongsberg Norspace' telemetry transmitters and beacons, photo: Kongsberg Norspace

(PA). The amplifier will eventually be incorporated at the output of their C-band telemetry transmitters and will have the capability to either work as the last PA-stage before the antenna or as a driver amplifier for traveling wave tube amplifiers. Regardless of use, the amplifier will finally serve as a gap filler as customers currently needs to deal with a third part. Figure 1.1 shows the telemetry transmitters and beacon systems made by Norspace.

The goal of this thesis is to develop three different power amplifier topologies based on the GaN-technology for future C-band telemetry transmitters. Each amplifier should be able to deliver 10W or more and have 14dB gain or higher. The applied signal has a constant envelope and will occupy a bandwidth between 100kHz and 1MHz, however the amplifiers must cover the frequency band from 3.4GHz to 4.25GHz with a gain ripple less than 0.5dB/500MHz. Maximum allowed power consumption is restricted to 25W which implies a drain efficiency of at least 40%. The input and output reflection coefficients must be less than -10dB.

1.3 Required specifications

The following amplifier specification has been given by Kongsberg Norspace.

Parameters	Requirement
Frequency band	3.4-4.25GHz
Linear gain, S21	14 dB
Gain flatness	$<$ 0.5 dB/500MHz
$P_{1dB,out}$	$>$ 40dBm
Noise Figure	$<$ 7dB (Not critical)
Input and output reflection coefficients	-10dB
DC power consumption	$<$ 25W

Table 1.1: Required specifications for power amplifier

1.4 Outline of report

The report is organized as follows.

Chapter 1 provides an introduction to the problem investigated in this report, together with a brief description of a general telemetry, tracking and command system.

Chapter 2 contains the theory needed to understand the report and the choices that have been made. This includes, a short introduction to S-parameters and power amplifiers with focus on the linear classes in addition to, CAD software and measurement equipment. There is also included a brief introduction to large-signal stability and a theoretical description of performing a large-signal stability analysis.

Chapter 3 presents the process of designing each power amplifier together with the choice of transistors, substrates and passive components. Smith charts are also included for easily displaying optimal reflection coefficients for both source and load matching networks.

Chapter 4 covers the results obtained from simulation and measurements of the realized amplifiers. The results includes, among others, P_{in}/P_{out}-plots, PAE and drain efficiency plots. At the end of the chapter several tables are shown and provides information about the simulated and measured performance of each amplifier at 40dBm output power.

Chapter 5 presents a detailed method of performing a large-signal stability analysis in ADS. It includes relevant information on how to set up the simulation correctly in addition to the large-signal stability results.

Chapter 6 goes through the discussion and possible improvements for the future. Practical issues are also presented and a section which discuss the future of power amplifiers utilizing the GaN-technology in space applications are briefly covered.

Chapter 7 summarizes and concludes the project.

Chapter 2

Preliminaries

This chapter will present important topics that are essential to understand how power amplifiers (PAs) works and how to design them. It also contains information about the GaN transistor technology and how simulation tools are used in this project. An extended presentation of power amplifier stability is also included.

2.1 Active Two-Port Network

2.1.1 S-Parameters

To describe the total voltages and currents in a microwave circuit are often a tedious and difficult task. Instead scientists and engineers, and especially electrical engineers, uses scattering parameters, or S-parameters, to completely describe a microwave network. This way of representing a microwave network is based upon the measurement of the incident and reflected voltage waves, and is done with a network analyzer which will be described in a later section. In general S-parameters are complex numbers that both describes the magnitude and phase through a microwave network. A N-port network will produce N^2 parameters.

Consider the generalized 2-port network in Figure 2.1, the relationship between incident(V_1^+, V_2^+) and outgoing (V_1^-, V_2^-) voltage waves can be found to be

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{2.1}$$

where S_{11} and S_{22} are the input and output reflection coefficients and S_{12} and S_{21} are the transmission coefficients when both ports are terminated with matched loads, respectively. [2]

The four reflection coefficients are also shown in Figure 2.1, and by looking towards

the load it is possible to define the reflection coefficient, Γ_L as

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{2.2}$$

and the reflection coefficient looking towards the source is defined as

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}, \tag{2.3}$$

where Z_0 is known as the reference characteristic impedance, and Z_L and Z_S are the load and source impedances, respectively.

The two reflection coefficients, Γ_{in} and Γ_{out}, can be determined from the definition of S-parameters in 2.1 and the equations $V_1^+ = \Gamma_S V_1^-$ and $V_2^+ = \Gamma_L V_2^-$. These are:

$$\Gamma_{in} = \frac{V_1^-}{V_1^+} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{2.4}$$

and

$$\Gamma_{in} = \frac{V_2^-}{V_2^+} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} = \frac{Z_{out} - Z_0}{Z_{out} + Z_0}. \tag{2.5}$$

Where Z_{in} is the impedance seen towards input of the network when the output port is terminated. Similarly, Z_{out} is the impedance seen into the output port when the input port is terminated.

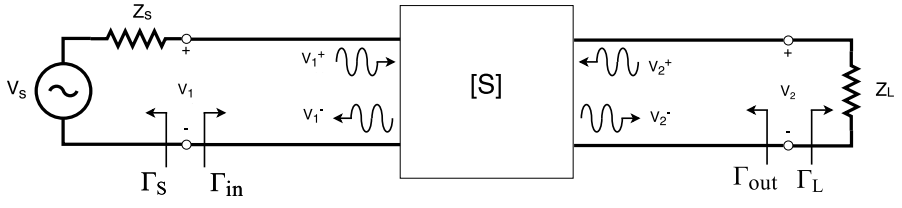


Figure 2.1: A two-port network with general source and load impedances. [2]

2.2 Gain

When dealing with active two-port networks there exists three different types of gain. These are *power gain, available gain* and *transducer power gain*, and can be expressed in terms of the S-parameters corresponding to the network.

Power gain is defined to be the ratio between the dissipated power at the load to the power delivered to the input of the network, $G = \frac{P_L}{P_{in}}$. In addition this gain is independent of Z_S. The expression of G is

$$G = \frac{|S_{21}|^2(1 - |\Gamma_L|^2)}{(1 - |\Gamma_{in}|^2)|1 - S_{22}\Gamma_L|^2} \tag{2.6}$$

The available gain is defined to be the ratio between the power available from the two-port network to the power available from the source, $G = \frac{P_{avn}}{P_{ave}}$. This assumes conjugated matching networks at both source and load.

$$G_A = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2(1-|\Gamma_{out}|^2)} \tag{2.7}$$

Transducer power gain is defined as the ratio of the power delivered to the load to the power available from the source, $G = \frac{P_L}{P_{avs}}$, and depends on both Z_S and Z_L.

$$G_T = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_S\Gamma_{in}|^2|1-S_{22}\Gamma_{out}|^2} \tag{2.8}$$

By looking closer at the transducer power gain formula, one sees that this definition takes into account both source and load mismatch. By separating this equation into three parts - G_S, G_0 and G_L, each gain factor can tell how much the different parts of the network are contributing to the overall transducer power gain. G_S and G_L accounts for the gain one can achieve by having conjugated matching networks at the source and the load, respectively. The G_0 is the gain of the transistor itself.

$$G_S = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2} \tag{2.9a}$$

$$G_0 = |S_{21}|^2 \tag{2.9b}$$

$$G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{2.9c}$$

2.3 Stability and Oscillations

To be able to analyze the stability of a circuit, the circuit must either operate in the linear regime (small-signal), disregarding the influence of the small-signal sources, or be linearized about a time-varying steady-state solution obtained in the presence of the circuit's sources (large-signal). The two cases are studied in the following and a two port circuit is assumed.

2.3.1 Even-Mode Oscillations and Small-Signal Stability Analysis

Any transistor which is partially or conditionally stable, can give rise to even-mode oscillations. This can happened if either the source or load network impedance has a negative real part, which would lead to $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$, or due to finite isolation, $S_{12} \neq 0$. Since Γ_{in} and Γ_{out} depends on the input and output network impedance, these reflection coefficients will also depend upon Γ_S and Γ_L. Pozar [2, p. 199] defines two types of stability:

- Unconditional stability: A network is unconditional stable if both $|\Gamma_{in}|$ and $|\Gamma_{out}|$ are less than unity for all passive source and load impedances. Hence $|\Gamma_S|$ and $|\Gamma_L|$ are less than unity.

- Conditional stability: A network is conditionally stable if $|\Gamma_{in}|$ and $|\Gamma_{out}|$ are less than unity only for certain source and load impedances. This case is also referred to as potentially unstable.

Since source and load matching networks will change characteristics with frequency, the designer has to check the stability for the entire frequency interval [0,ω_{max}], where ω_{max} is the maximum frequency of which the transistor exhibits gain. The K-Δ test together with the Rollett's condition are able to determine if an amplifier is unconditional stable or not, and it is defined as:

$$K = \frac{1 - |S_{11}(\omega)|^2 - |S_{22}(\omega)|^2 + |\Delta(\omega)|^2}{2|S_{12}(\omega)S_{21}(\omega)|} > 1 \tag{2.10}$$

together with

$$|\Delta(\omega)| = |S_{11}(\omega)S_{22}(\omega) - S_{12}(\omega)S_{21}(\omega)| < 1 \tag{2.11}$$

Both criteria have to be met simultaneously in order to determine if the amplifier is unconditionally stable. Unfortunately, the K-Δ test cannot be used to compare the relative stability of two or more devices, just that they are stable or not. However there exist a second method that copes with this problem, called the μ-test. It is defined according to Eq. 2.12 and provides the distance from the center of the Smith chart to the nearest point of the load stability circle. If μ is greater than 1, the device is unconditionally stable. In addition, larger μ-values will indicate a more stable device than smaller values. [2]

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{2.12}$$

A drawback with the previously mentioned tests, is that they are not applicable to spot internal oscillations. A multistage amplifier might be stable when the overall design is analyzed, but oscillates nevertheless. This is because internal transistor stages are terminated in a passive network followed by an active device that can give rise to a negative resistance. The solution is to analyze each stage separately and a final analysis of the total design. If each stage and the overall system is stable, one can then assume that it will not exhibit even-mode oscillations.[3]

2.3.2 Odd-Mode Oscillations and Large-Signal Stability Analysis

In power amplifier architectures with transistors placed in parallel, potential odd-mode oscillations might arise. Due to slight variations of I_{ds}, breakdown voltage and transconductance or different source or collector inductance, the transistors will exhibit slightly different gains and output powers which might lead to instabilities. In addition, the matching networks might have small production variations and coupling between the microstrip lines that can influence the different transistors and hence create conditions for odd-mode oscillations. Also, odd-mode oscillations might arise due to finite isolation between the output and input of the transistor. As the length of the feedback loop, in an amplifier with parallel transistors, is close to the wavelength of the operating frequency, the odd-mode oscillations are normally close to the operating band or much higher. Odd-mode oscillations are also known as parallel transistor oscillations. [3]

As previously mentioned, the instability might be caused by a nonlinear capacitance in the active device which give rise to a negative resistance in the small-signal regime. In addition, the nonlinear capacitance might encounter the right conditions which enables oscillations when undergoing large-signal perturbation. E.g. an apparently stable amplifier will start to oscillate when the input power reaches a specific level or inside a power range, as seen from Figure 2.2, and will stop oscillating below or above a certain level. In the following paragraphs a method of performing a large-signal stability analysis is presented. [4, p.359]

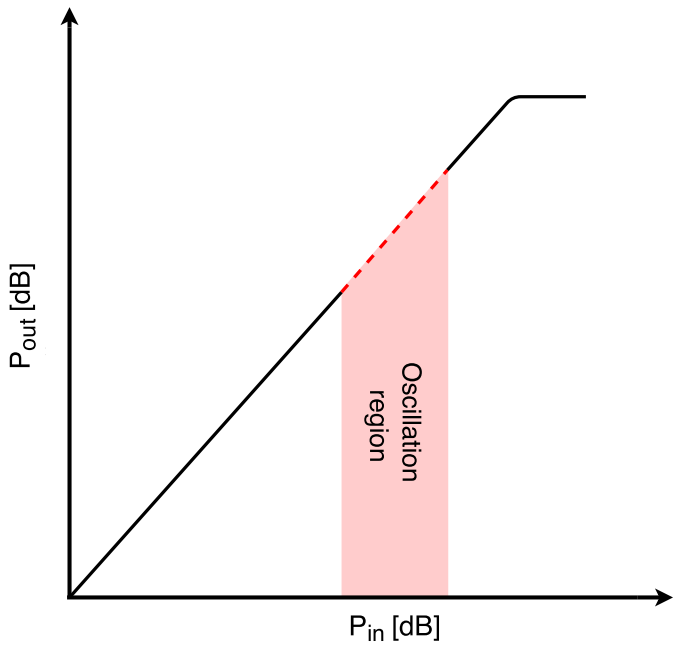


Figure 2.2: Idealized P_{in}/P_{out}-characteristics with oscillation region caused by transistor nonlinearities or variations in circuit. The amplifier is be stable outside.

Despite that a nonlinear two port circuit is fulfilling the Rollett's criteria or the μ-test in small-signal mode, it is not guaranteed that it will remain stable as the input power increases. To be able to examine the large signal stability behavior, a technique called admittance/impedance analysis can be performed where the conductance/resistance and susceptance/reactance are plotted separately, but investigated together at different nodes in the circuit.

The conductance is calculated from the total admittance (impedance) estimated by introducing a small-signal parallel current (series voltage) source, $I(\omega)$ ($V(\omega)$), at a given node (branch). In power amplifier designs, the node is often chosen to be the gate or drain as these nodes are the most sensitive. By knowing the ratio of the small-signal current and the branch voltage, it is possible to calculate the admittance $Y(\omega) = \frac{I(\omega)}{V(\omega)}$ (impedance,

$Z(\omega) = \frac{V(\omega)}{I(\omega)}$) and thus be able to find the conductance (resistance). The oscillation criteria is met when: $Re\{Y(\omega)\} < 0$, $Im\{Y(\omega)\} = 0$ and $\partial(Im\{Y(\omega)\})/(\partial\omega) > 0$, and a fulfillment of these conditions will generally imply the existence of a pair of complex-conjugated poles at the right hand side of the complex plain. However, it is also important to consider the case where only the conductance/resistance is negative. Although it might not lead to oscillations, the circuit will most likely be unstable. A conceptual model of the test setup is shown in Figure 2.3. Please refer to [5, Kurokawa] and [4, Surez] for further analysis of oscillators and oscillation analysis.

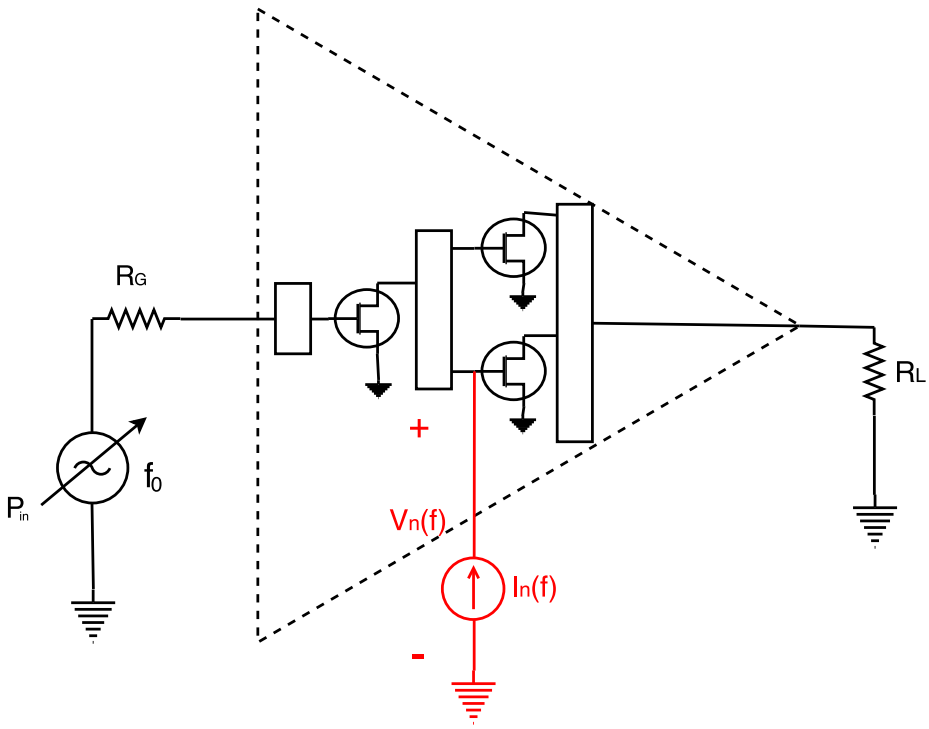


Figure 2.3: Theoretically setup of admittance/impedance large-signal stability analysis. P_{in} - Large-signal input power level, f_0 - Large-signal frequency, $V_n(f)$ - The node voltage where the small-signal current source, I_n(f), is connected.

Since the instabilities may occur at any frequencies, the small-signal source is swept over a large frequency interval (typically from $\omega \cong 0$ to ω_c, where ω_c lies in the operating frequency band), while the input generator holds its power level and frequency fixed. It can be compared to a mixer-like simulation, where the large-signal input drive acts as the local oscillator and the small-signal current source is the RF signal to the mixer.

By stepping through different power levels and frequencies of the large-signal input source, it is possible to make a detailed analysis of possible instabilities and how they react upon different input power levels and frequencies. Emphasis that the circuit is operating

in a linear mode with respect to the small-signal source and that the small-signal source must not alter the steady-state periodic regime. It is also worth mentioning that finding the optimal nodes (branches) for large and complex circuit designs may be a challenging task. Even if the start up requirements for oscillation is met, choosing the wrong node (branch) may mask the instabilities [4, p. 360]. A large-signal stability analysis setup in ADS is will be presented in chapter 5.1.

2.4 Efficiency

In satellite communication systems, wireless devices and other low power radio systems it is often preferable to convert as much DC power to RF power as possible. The efficiency parameter is one of the most important figure of merit, and one way of measure amplifier efficiency is the the ratio of how much DC input power that gets converted into RF power. This parameter is known as the *drain efficiency* and is defined

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.13}$$

Unfortunately the drain efficiency does not take into account the input RF power and would tend to overestimate the actual efficiency. A better way of defining the efficiency is to include the input RF power.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = (1 - \frac{1}{G})\frac{P_{out}}{P_{DC}} = (1 - \frac{1}{G})\eta \tag{2.14}$$

where G is the power gain of the amplifier. The power that is not converted to RF power will be dissipated as heat. Note that in high gain amplifiers the 1/G term will decrease towards zero, and PEA will become equal to η.

2.5 Power Amplifier Classes

Power amplifiers may be divided into two main categories - linear and nonlinear. Linear attempts to preserve the RF input wave shape at the output, while the nonlinear amplifiers does not. In addition there exists several sub-categories or *classes*, and according to [6] the main linear amplifier classes are A, AB and B, while the nonlinear classes are C, D, E and F (in addition to several others). The nonlinear classes, except class C, are also known as switch mode amplifiers, and will not be further introduced. For more information see [7].

2.5.1 Class A

A class A amplifier is the most linear amplifier, since the transistor is always on i.e. the quiescent drain current is always flowing. These amplifiers are ideally biased at $\frac{1}{2}V_{ds,max}$ with a drain current of $\frac{1}{2}I_{dss}$, and with a conduction angle of 2π [1]. If the transistor is not driven into compression (saturated class A) or cut-off, this configuration will lead to a

[1] The conduction angle, α, indicates the proportion of the RF cycle for which conduction occurs. [8]

minimum of distortion. This amplifier class is the least efficient of the linear classes with a theoretical maximum efficiency of 50%. A detailed derivation can be found in [6, p. 96]. Hence, the power dissipation in the active device will be 50% or more, and a careful design of a cooling system must be taken into account.

2.5.2 Class B

In comparison with a class A amplifier, a class B amplifier only conducts the positive part of a sinusoidal wave and the conduction angle is then equal to π. This implies that the quiescent current of this class is ideally 0A. A class B amplifier has significantly higher efficiency than class A, and the theoretical maximum is 78.5%. The downside is that a class B amplifier will produce a significant amount of harmonics that will distort the output signal causing poorer linearity properties than a class A amplifier.

2.5.3 Class AB

The compromise between class A and class B is called class AB. This class has a theoretical efficiency between 50%-78.5%, and the linearity will decrease as the efficiency increase. The added distortion by a class AB amplifier is less than that of a class B amplifier, but higher than that for a class A amplifier. The conducting angle can vary between π and 2π depending on where the transistor is biased.

2.5.4 Class C

A class C amplifier is biased according to Figure 2.4, and will only conduct less than half of a sinusoidal cycle. In other words this class has a conducting angle of less than π. This amplifier class will produce even higher distortion than a class B amplifier, which will result in a misshaped waveforms, thus making this amplifier class unusable for linear applications.

2.6 1dB Compression point

A typical power amplifier will have a characteristic according to the curved line in Figure 2.5, and the gain (in dB) is given as the difference between the output power and the input power. When the amplifier starts to saturate it will deviate from the ideal straight line, resulting in reduced gain. To measure the linear range of an amplifier, one can define a point called 1dB compression point, which refers to the point where the output power level differs from an ideal linear characteristic by 1dB. [6] [2]

2.7 GaN Technology

Gallium nitride (GaN) high electron mobility transistors (HEMT) have from the start received great attention from power amplifier designers world wide, due to the vast increase

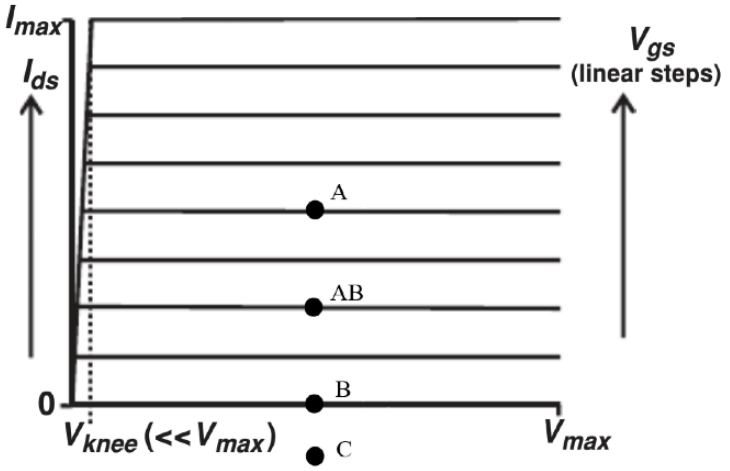


Figure 2.4: IV-curves containing the bias points for different PA classes. [8]

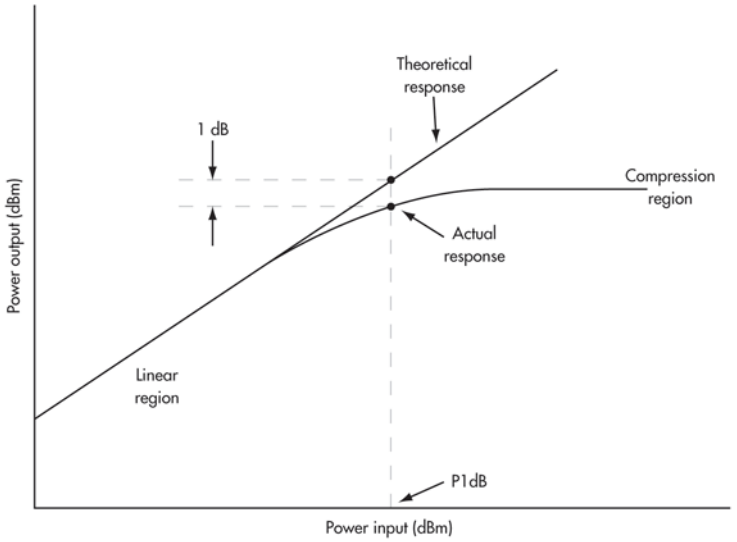


Figure 2.5: 1dB compression piont. [9]

in power density. It is a binary III/V wide bandgap (3.4eV) semiconductor which is usually grown on a silicon carbide (SiC) substrate. Its low RF losses and exceptional thermal performance makes this semiconductor ideal for RF-application especially in space where convection is non-existent. In addition, this combination of materials leads to a high breakdown field, that allows the GaN semiconductor to handle much higher voltages and to operate at higher junction temperatures than other material combinations [10]. GaN

have also a high saturation velocity, which is the velocity of an electron at very high electric fields. This means that the device can handle higher current densities, which implies higher power densities. [11]

2.8 Load Pull

Load pull refers to the action of varying the load of the transistor, while measuring the performance. As this method is performed under true operating conditions, this method gives valuable information about which impedances are the most ideal to achieve e.g. high efficiency or output power. After finding the optimal impedances for the transistor, the strategy of finding an appropriate matching network is now converted from a highly nonlinear problem into a linear problem which can be solved much faster. This method can also be used at the source, and is then referred to as source pull. [8]

2.9 Power Divider

Power dividers are passive circuits used for power division in e.g. balanced amplifier design. It consists of an input port with arbitrary number of output ports. One of the most common power divider is called Wilkinson power divider, and a brief introduction will given in the following section. For further analysis, see [12, p. 328-331]. Power dividers have also the capability to combine power from two or more inputs and are then called power combiners.

2.9.1 Wilkinson Power Divider

The Wilkinson power divider was invented by Ernest J. Wilkinson in 1960. It is a matched, reciprocal and lossy network with an arbitrary number of output ports, but in this project the the three port configuration is utilized.

The three port network is realized with an input port with characteristic impedance, Z_0, followed by two parallel quarter wavelength transmission lines with an impedance of $\sqrt{2}Z_0$. Each branch ends up in an output port with characteristic impedance, Z_0, respectively. Between the two branches, a $2Z_0$ resistor is added to fulfill the network theorem[2]. The resistor ensures that all three ports are matched, in addition to fully isolate the two output ports. Figure 2.6 shows a conceptual model of the Wilkinson power divider. [13][12]

Its S-parameters are given by:

$$S = \frac{-j}{\sqrt{2}} \begin{pmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{pmatrix} \tag{2.15}$$

[2] An electrical network can not satisfy all three conditions of being matched, reciprocal and loss-less at the same time.

2.10 T-attenuator

An attenuator is used to reduce the amplitude of a signal. The T-attenuator utilizes three resistors with two of equal value connected in series. The third resistor is connected such that the circuit shapes a T and is usually of much higher value. The resistor values are calculated according to:

$$R_1 = Z_0 \frac{10^{L/20} - 1}{10^{L/20} + 1} \tag{2.16}$$

$$R_2 = 2Z_0 \frac{10^{L/20}}{10^{L/10} - 1} \tag{2.17}$$

where R_1 refers to the series resistor, R_2 to the parallel resistor and L to the desired loss in dB. The equations were retrieved from [14].

This section has been included as the attenuator is used in the matching network to reduce the reflected signal from the transistor, hence an apparently better match is achieved. The design procedure of the matching networks will be described in Section 3.7.2.

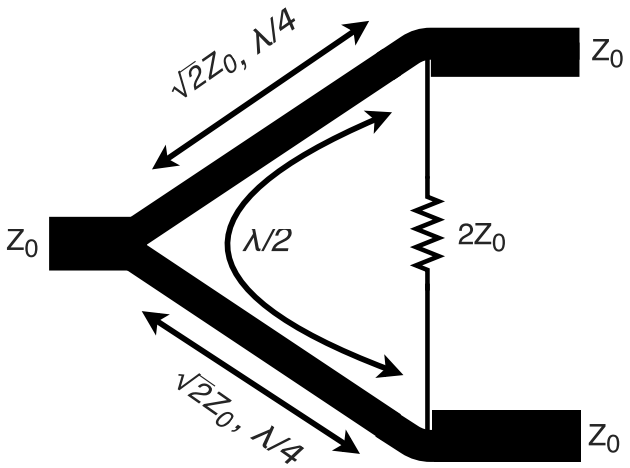


Figure 2.6: Conseptual drawing of Wilkinson power divider.

2.11 Simulation Tool

Advanced Design System (ADS), made by Keysight (former Agilent Technologies), is a CAD-software for RF, microwave and high speed digital applications and have been used

for designing the power amplifiers. The following sections will present the simulation tools which are used in the design procedure.

2.11.1 Small Signal

S-parameter simulation is used to retrieve the small-signal characteristics of an active device at a specific bias, and also used for passive RF circuit characterization. A simulation of nonlinear devices starts with a DC bias simulation followed by a linearization of all nonlinear elements about the specified bias point. This includes linearization of passive devices.

The resulting linearized circuit is then analyzed as a multiport device, by stepping through and excite each port one by one. The circuit response is then converted into S-parameters and showed to the user. [15]

2.11.2 Large Signal

Harmonic balance enables large signal analysis of non-linear systems, and is carried out in the frequency domain. This technique is iterative and based on the presumption that for a given sinusoidal excitation, it will exist a steady-state solution that can be approximated by means of a finite Fourier series. The harmonic balance method handles elements differently, depending on if they are linear or not. While current flowing into linear element are calculated in the frequency-domain, nonlinear elements (transistors, diodes) are calculated in the time-domain and converted into frequency-domain via the fast fourier transform (FFT). The analysis stops when the error function, which sums the currents in all nodes, converges.[16]

2.11.3 Optimizers

There exist several optimizers in ADS, but this report only deals with the two used in this project - The random optimizer and the gradient optimizer. These optimization techniques are differentiated by their search methods, how the optimizer decides new parameter values, and the error function formulations, how the optimizer measures the error between the computed and the desired value. [17]

- The *Random Optimizer* utilizes a random-number generator to perform a random search and to calculate new parameter values. By picking a random number within an interval and a set of starting/initial parameters, for which the error function is known, it will calculate a new set of parameters and then re-evaluate the error function. This optimizer uses the least-square error function to minimize the weighted average error.

- The *Gradient Optimizer* uses the gradient search method to retrieve new parameter values by utilizing the gradient information of the network's error function. It reduces the error by changing the parameter values in the direction of which the gradient of the error function is indicating. This optimization method does also utilize the least-square error function, and guarantees to find a local minimum result.

2.12 Measurement methods

2.12.1 Small-signal measurements

The small-signal measurements are performed with a network analyzer, which is a device that can measure the S-parameters of a RF/microwave network. There are basically two types of network analyzers: the scalar network analyzer (SNA) which only measures the amplitude, and the vector network analyzer (VNA) which measures both amplitude and phase. The VNA is also the most common network analyzer.

In general the architecture of both the SNA and VNA involves a frequency sweeping source, a test set that routes the generated signal, a receiver that detects and mixes down the incoming signal and a processor and display that can calculate and show the S-parameters. The device (DUT) that are going to be tested are then connected to the VNA with RF certified cables.

Because of non-ideal measuring equipment there will always be errors causing unwanted variations in the measurement result, and the errors are mainly due to:

- *Systematic errors:* Which is caused by non-ideal effects of VNA, the test set and the measuring setup. These errors are repeatable and can be viewed as time-invariant. However, through calibration these effects can be characterized and mathematically be removed from the measurements.

- *Random errors:* The main contribution to random errors are phase noise, sampling noise and IF noise. These are unpredictable and cannot be removed by using calibration, but the effect can be minimized by using averaging.

- *Operational errors:* These errors are mainly due temperature variations which will influence both the test setup and/or instrument after calibration. By recalibrating the VNA these errors are minimized.

2.12.2 Large single-tone measurements

To be able to characterize a power amplifier under normal circumstances, single tone measurements can be performed. By applying a single frequency signal at the input of the amplifier and measure the output signal together with the drain current and supply voltage, one are able to calculate parameters such as gain, efficiency, power consumption and to some extent linearity. A spectrum analyzer or a power meter can be used to measure the output signal. The benefit of using a spectrum analyzer is that it only measures a specified frequency range, compared to the power meter which measures the absolute power. This means that one are able to measure the power level of the fundamental frequency, without the contribution of the harmonics. However, the power meter is more accurate than the spectrum analyzer.

2.13 Calibration

There exists several types of calibration methods depending on the calibration components, complexity and how to connect the device under test (DUT).

SOLT (Short, Open, Load, Thru) calibration is one of the most common calibration method and is also the preferred method in this thesis. This method calibrates each port separately using the known short, open and load standards to remove the systematic errors and thus find the input and output complex reflection coefficient. The thru standard will calculate the forward and reversed complex transmission coefficients.[18]

Chapter 3

Design and topology

This chapter covers the design process of the three amplifier topologies. It will start with a general presentation of the amplifiers, followed by information about the transistors, substrates and other components used in this work. It also includes a thorough description of the design procedure for each amplifier. In addition, measurement setup and configuration are presented at the end.

3.1 Power Amplifier Topologies and Architectures

As mentioned in the introduction, the goal of this master thesis is to develop and investigate three different power amplifier topologies that can be used in a TT&C-transmitter and this section will introduce the different amplifier concepts.

3.1.1 Design 1: Single-stage PA

The idea behind the single-stage PA is to design a simple and relatively small amplifier as a reference design, and see how close to the requirements the performance is. The transistor which will be used, should just overcome the requirements and the total circuit must fit inside an area of 85mm*85mm, which is the size of the standard cooling plate used at the Microwave laboratory at NTNU. Figure 3.1 displays a block diagram of the circuit.

3.1.2 Design 2: Two-stage PA with balanced second-stage and joint output match

Due to the gain requirement and the input return loss, the second design is dimensioned with two stages. The first stage will work as a preamplifier and the second stage will ensure enough output power. It was decided that the second stage will consist of two transistors in a balanced configuration. This setup will also be able to operate even if one of the transistors at the second stage should fail, however the performance will be gracefully degraded. A block diagram of the circuit is shown in Figure 3.2.

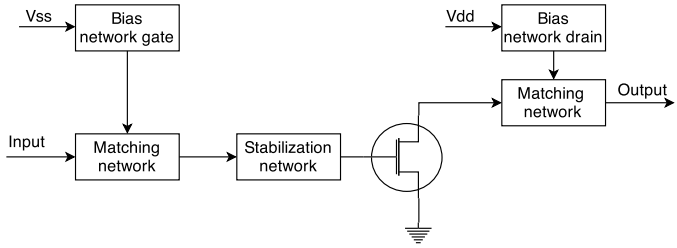


Figure 3.1: Block diagram of design 1 - Single-stage power amplifier.

To be able to feed each transistor in the second stage, the need of a power divider is present. The choice fell on a Wilkinson power divider, as this is a 3dB splitter and isolates the input of each transistor. To combine the output power from each transistor, a simple T-junction will be used. This solution does not isolates the output of each transistor from each other, but prevents all the power to be dissipated in the resistor if one of the transistors shuts down, and a Wilkinson power combiner had been used. A simple t-junction is also smaller than a Wilkinson power combiner.

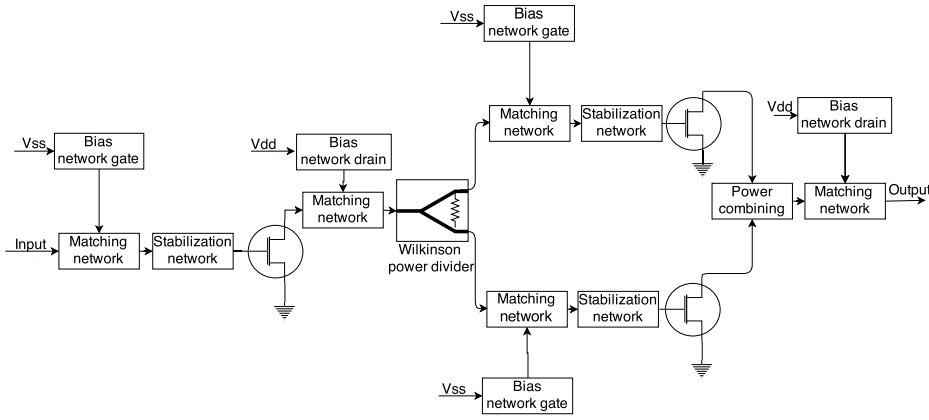


Figure 3.2: Block diagram of design 2 - Dual-stage power amplifier with balanced second stage and common output match.

3.1.3 Design 3: Two-stage PA with balanced second-stage and separate output match

In addition to the choices made in the previous section, it was decided to make the third design based on design 2. The third design will utilize the whole circuit except the power combination and the output match at the second stage. Instead, the transistors at the second stage will be separately matched before the power combining is done. A simple block

diagram of the circuit is shown in Figure 3.3.

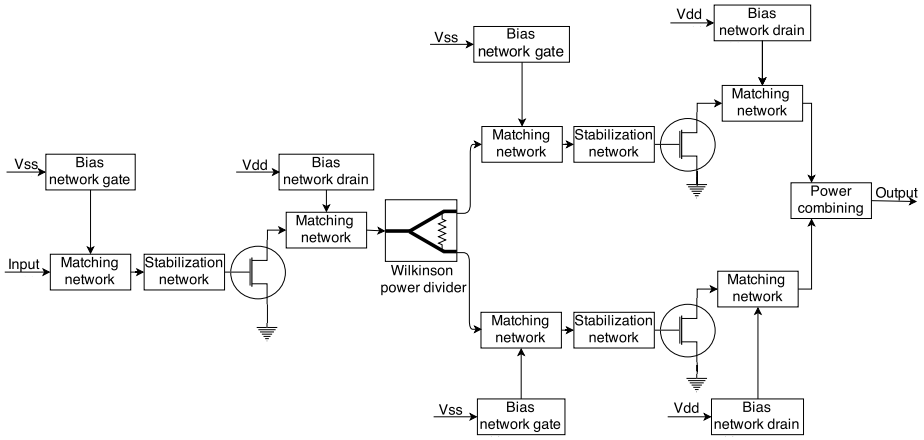


Figure 3.3: Block diagram of design 3 - Dual-stage power amplifier with balanced second stage and separate output matches.

3.2 Component technology

3.2.1 Transistors

Design 1: Single-stage

The CGH40010F 10W gallium nitride (GaN) high electron mobility transistor (HEMT) from Cree was chosen to be the active component in the single-stage amplifier design as it fulfills the output power requirement. It is an unmatched device with a frequency range spanning from DC to 6GHz which makes it ideal for use in the C-band. The transistor offers about 14dB gain at 4GHz and the efficiency properties are good throughout the bandwidth. In addition, the transistor has a screw-down flange, which makes it easy to mount. [19]

Devices from other companies were also considered, but good knowledge and simulation models favored the Cree transistor.

Design 2 & 3: Two-stage

For the two dual-stage designs the CGH40006P 6W GaN HEMT from Cree rendered itself as the best alternative. These designs will utilize this transistor in both stages, with one transistor in the first stage and two transistors in the second stage working in balanced mode, producing 12W output power.

Similar to the 10W transistor, the CGH40006P transistor has a wide frequency range spanning from DC to 6GHz and a typical output power P_{typ} = 8 W at 32dBm input power.

With a small-signal gain of approximately 12dB, it should be more than sufficient to fulfill the requirements of 14dB gain when used in a two-stage design. The transistor must ether be mounted using clamps or soldered onto the PCB, as it comes in a pill package format. [20]

3.2.2 Substrate

Design 1: Single-stage

The single-stage design used the RT/duroid6002 high frequency laminate from Rogers Corporation. As it is a low loss substrate with low outgassing properties, it is ideal choice for high frequency aerospace applications in hostile environment [21]. Table 3.1 shows the substrate parameters used in the simulations.

Parameters		Value
Substrate hight	H	1.524 mm
Dielectric constant	ϵ_r	2.94
Relative permeability	μ_r	1
Dissipation factor	$tan(\delta)$	0.0012
Conductivity	Cond	$5.96{*}10^7$ S/m
Conductor hight	T	18μm

Table 3.1: RT/duroid6002 substrate parameters used in the simulations of the single-stage design.

Design 2 & 3: Two-stage

Design 2 and 3 utilized the RO4003C substrate from Rogers Corporation. It is a woven hydrocarbon ceramic laminate which can be fabricated using standard epoxy/glass processes, and ordinary CNC milling machines can be used to produce PCBs. The dielectric constant of the substrate is stable over a broad frequency range, which makes it to a good choice in broadband applications. The dielectric constant used in simulation was 3.55, which is the average value from several testes of the 4000 series substrate. [22]

The substrate parameters used in the simulations are shown in Table 3.2

Parameters		Value
Substrate hight	H	0.813 mm
Dielectric constant	ϵ_r	3.55
Relative permeability	μ_r	1
Dissipation factor	$tan(\delta)$	0.0021
Conductivity	Cond	$5.96{*}10^7$ S/m
Conductor hight	T	17.5μm

Table 3.2: RO4003C substrate parameters used in the simulations of the two-stage designs.

3.2.3 Passive Components

The capacitors used in this work was the Johanson R14S series and the Murata GRM series. Both series are ceramic multilayered capacitors. The Johanson capacitors are ultra-high Q devices and are used as DC-blocks and for decoupling, together with the Murata series, in the bias networks. In addition, these capacitors has a NP0 (negative-positive zero) temperature characteristic, which refers to the temperature coefficient, α, and hence the variation of capacitance due to change in temperature. The NP0 characteristic implies almost constant capacitive value regardless of temperature variations.

The existence of parasitic effects are always present. Figure 3.4 shows a simple equivalent circuit model of the Johanson capacitors that also accounts for these effects. The model is the basis for the simulation model, and is developed by Associate Professor Morten Olavsbråten.

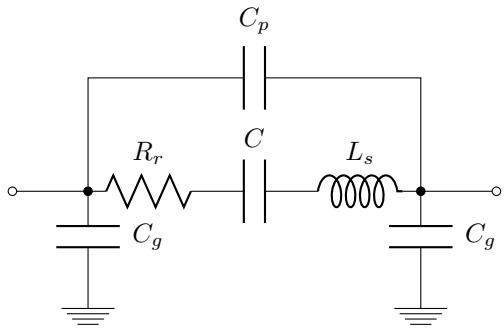


Figure 3.4: Equivalent circuit of Johanson R14S surface mounted capacitor

The parallel capacitance, C_p, accounts for parasitic effects between the pads, the two shunt capacitors, C_g, describes the capacitive effects between the pads and the ground. Since the capacitor is not ideal, the resistance, R_s, account for loss and the series inductance, L_s modulates the inductive effect due to the ceramic layers.

Simulation models for the Murata capacitors were also used but due to restrictions, the equivalent circuit models are unknown.

3.3 Quiescent Point

In order to decide the class of operation, it has to be taken into account that the small-signal gain requirement is quite high, and that the excited signal does not vary in amplitude (i.e. frequency or phase modulated). This leads to a deep class AB as the best alternative for all three designs. The class does not suffer as much as class B and C with regards to the gain reduction, and will be much more efficient than a class A power amplifier.

The IV-characteristics for the 10W and 6W Cree transistors are plotted in Figure 3.5 with solid and dotted lines, respectively. Based on the discussion above and the maximum drain currents, which are 1.5A for the 10W transistor and 700mA for the 6W transistor, the 10W device was biased with a 110mA drain current and the 6W transistor was biased with 100mA. Both with a supply voltage of 28V.

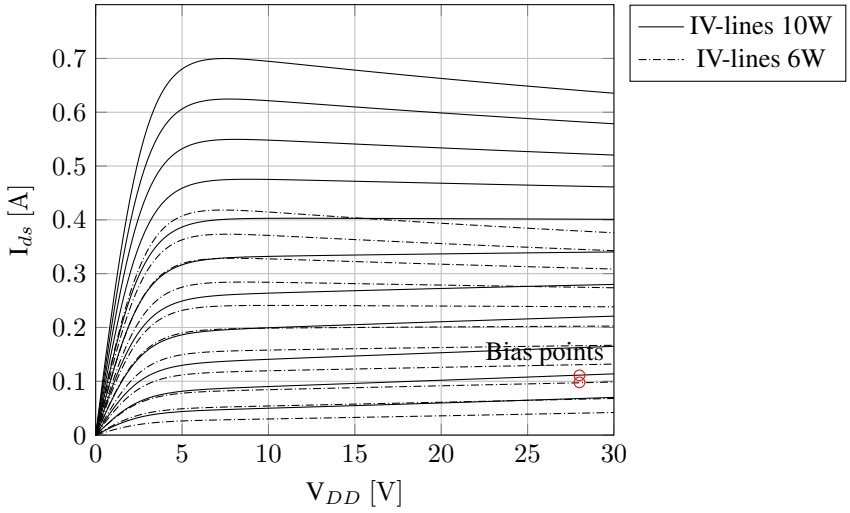


Figure 3.5: IV-Curves of the Cree CGH40010F transistor (solid lines) and the Cree CGH40006P transistor (dotted lines).

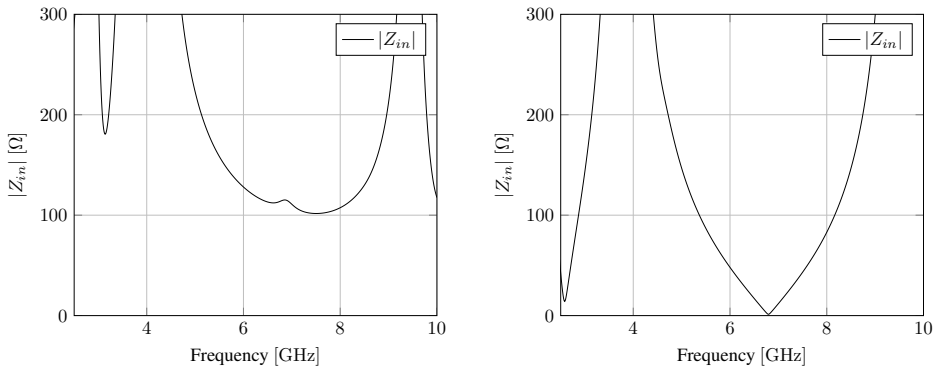
3.4 Bias Network

The job of a bias network is to prevent leakage of the RF-signal into the DC-feeds and hence modulate the DC-sources. A general bias network consists of decoupling capacitors and a RF-choke, which in microwave designs are realized with a quarter wavelength transmission line.

3.4.1 Design 1: Single-stage

The gate and the drain bias networks was realized with a quarter wavelength microstrip line, with a length which corresponds to the wavelength of the center frequency. At the DC-feeding point a short microstrip stub was added to be able to solder on the RF-bypass capacitors, from Johansson and Murata. The capacitor values were chosen to be: 1pF, 10pF, 100nF and 10μF. At the gate, the quarter wave line is then followed by a second quarter wavelength stub so that, when looking into to bias network from the RF-side, the impedance is ideally infinite. At the RF-side a 100Ω resistor connects the bias network to the matching circuit. The resistor suppresses the possible instabilities at low frequencies and hence the chance of oscillation. The input impedance, reflection coefficient and the transmission coefficients can be seen in Figure 3.6a and 3.7a and 3.7b, respectively. It is worth noting the indications of small in-band resonance in the reflection coefficient at the gate side. However, due to the high input impedance, these possible resonances were partially ignored.

At the drain side, the bias network consists of a quarter wave length microstrip line followed by a fan shaped stup. This method provides better bandwidth properties than a quarter wavelength open line, in addition to be smaller and shorter [3]. As seen from



(a) $|Z_{in}|$ of gate bias network

(b) $|Z_{in}|$ of drain bias network

Figure 3.6: Design 1: Input impedance, $|Z_{in}|$, seen into the bias network from the RF side

the red line in Figure 3.7a there is almost total reflection between 3.4GHz and 4.25GHz and Figure 3.7b shows that the transmission through the bias network is quite low in the frequency band. Figure 3.6b shows the bias network's input impedance at the drain-side. The same capacitor values as the ones used at the gate side, were utilized here.

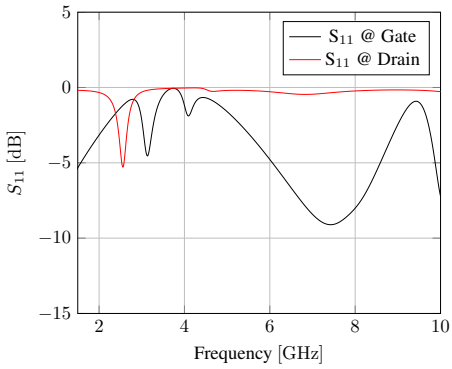
The reason for not choosing a fan shaped stub at the gate side, was that the achieved RF-blocking and low frequency damping were better with a regular quarter wave length microstrip line when the resistor was connected.

3.4.2 Design 2 & 3: Two-stage

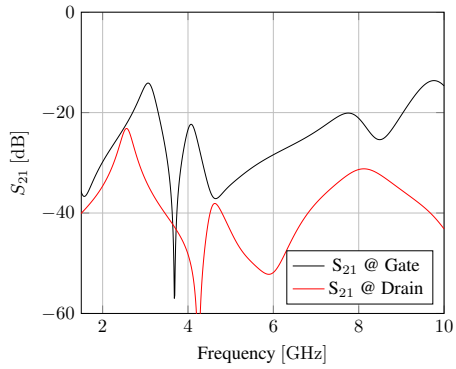
The DC bias networks adopted in design 2 and 3 consists of a quarter wavelength microstrip lines together with two parallel radial stubs. The radial stubs are connected in an asymmetric manner based on an idea from [23]. At the gate-side, a 22Ω resistor is connected to help stabilize the circuit at lower frequencies. Like design 1, the same capacitor models and values were used as decoupling capacitors. Based on the plots in Figure 3.9a, it is seen that this method achieves good results with regards to the reflection coefficients for both bias networks. The gate-side has a rounded characteristic between 3.4GHz and 4.25GHz, while the bias network at the drain side has a flat response from around 1.8GHz to 9GHz. The corresponding transmission through both circuits are below -40dB in the frequency band. The absolute value of the input impedances are plotted in Figures 3.8a and 3.8b

3.5 Stability

To prevent even-mode oscillation, a series stabilization network was attached to the gate of the transistors in all three designs. The stabilization network was realized with a high-pass filter consisting of a capacitor and a resistor in parallel. This will introduce loss at lower frequencies and hence stabilize it.

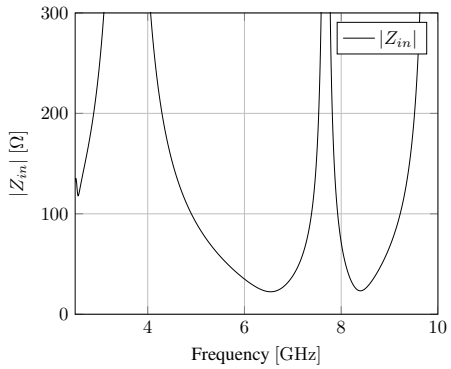


(a) S_{11} of gate and drain bias network

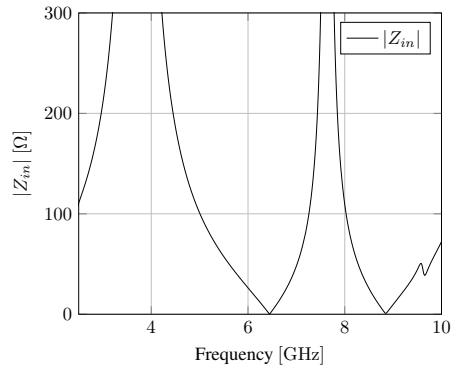


(b) S_{21} of gate and drain bias network

Figure 3.7: Design 1: Input reflection and the transmission coefficients of the gate and drain bias network.

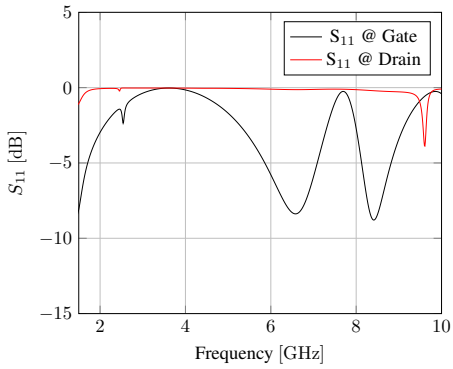


(a) $|Z_{in}|$ of gate bias network

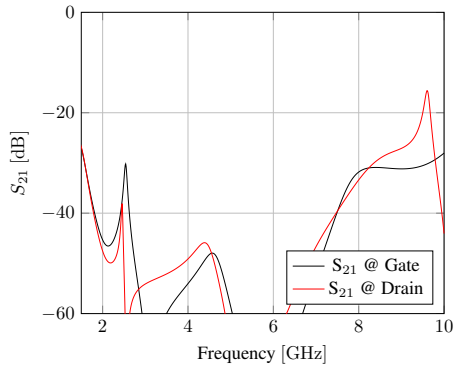


(b) $|Z_{in}|$ of drain bias network

Figure 3.8: Design 2 & 3: Input impedance, $|Z_{in}|$, seen into the bias network from the RF side



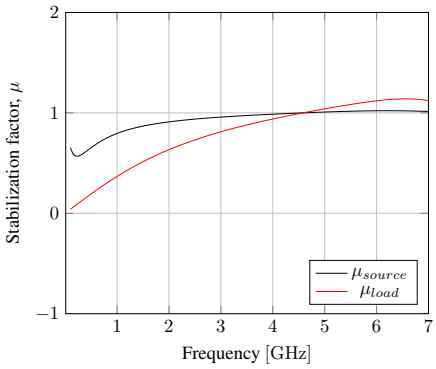
(a) S_{11} of gate and drain bias network



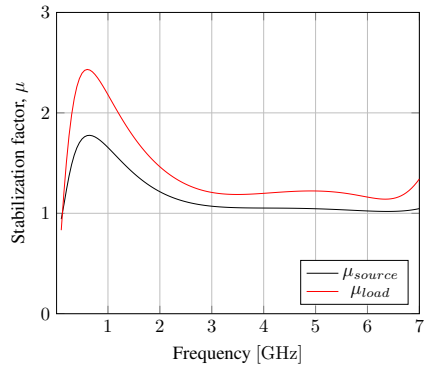
(b) S_{21} of gate and drain bias network

Figure 3.9: Design 2 & 3: Input reflection and the transmission coefficients of the gate and drain bias network.

The cut-off frequency of the filter can be computed by $f_c = \frac{1}{2\pi RC}$. For design 1 (single-stage) the stabilization factors, μ_{source} and μ_{load}, before and after stabilizing are plotted in Figure 3.10. A high-pass filter with a f_c of approximately 800 MHz were enough to stabilize the transistor. The values of the resistor and capacitance were 55Ω and 3.3pF, respectively.



(a) Stabilization factor, μ, without stabilization network

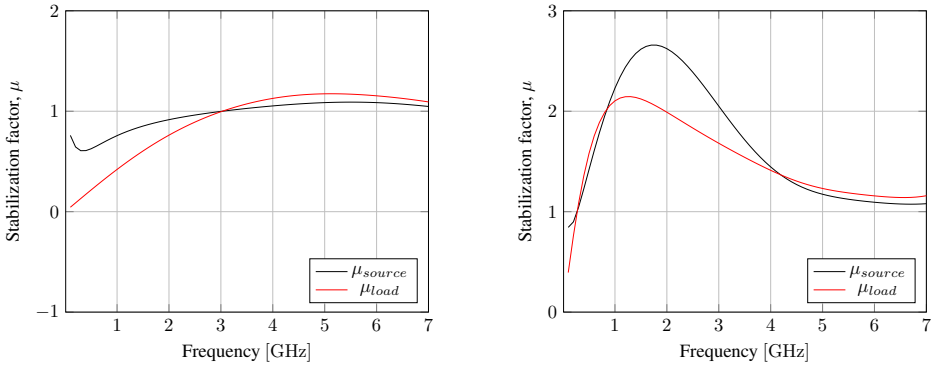


(b) Stabilization factor, μ, with stabilization network

Figure 3.10: Stabilization factor before and after stabilization for 10W transistor

Figure 3.11a shows the stability factors of design 2 and 3 before the stabilizing circuit was added. Like design 1, the stabilization networks in design 2 and 3 were realized with a resistor and capacitor in parallel, disregarding the component values. In order to make the transistor unconditionally stable, a resistor of value 33Ω and a capacitor of value 1.2pF were needed. This filter has a cut-off frequency, f_c, equal to 4.01GHz and the stability

factors after stabilization are shown in Figure 3.11b.



(a) Stabilization factor, μ, without stabilization network

(b) Stabilization factor, μ, with stabilization network

Figure 3.11: Stabilization factor before and after stabilization for 6W transistor.

3.6 Designing matching networks - General approach

This section will describe the general method used to obtain the optimal impedances and the design of the matching networks of all three designs. For design specific methods, please see section 3.7

3.6.1 Method

The source pull and the load pull techniques described in the Chapter 2 have been used to find the optimal impedances at the input and output of the transistor, respectively. By tuning the reflection coefficients and the related phase for five in-band frequencies (3.4/3.6125/3.825/4.0375/4.25GHz), and their corresponding second harmonic components, optimal reflection coefficients were found.

By extracting the transistor's optimal reflection coefficients, the problem of finding a matching network now became a passive problem. This method greatly reduced the computational time, hence a greater sample space could be explored in equal amount of time. In addition, there were used ideal voltage sources and DC-blocks, when finding the reflection coefficients, which made the bias network's connection point independent. This meant that it could be integrated as a part of the matching network and not be fixed to a single point in the circuit.

ADS comes with a predefined block that calculates the reflection coefficients, as a function of frequency, seen at a specific port. This function was used to retrieve a variable which again was used in the optimization procedure to compare the actual reflection coefficients with the optimal reflection coefficients. By changing the widths and lengths of the microstrip lines, the reflection coefficients also changed. When a satisfying result was

obtained, each matching network was tested together with the rest of the circuit. The procedure continued with different matching network topologies until the overall performance fulfilled, or were close to, the requirements.

The impedance of a passive circuit network, also known as a Foster network, will move in a counter clock wise direction in the smith chart. Since a power amplifier contains active elements it does not obey the Foster theorem, hence the impedance can move in a clock wise direction. As a consequence, it is almost impossible to match the transistor exactly over the full bandwidth. For this reason, it was decided to use a looping method which creates small loops which travels in the ”opposite” direction in the smith chart. The small loops are created due to resonance in the circuit.

As the optimizer had a tendency of favoring some of the frequencies, where the requirements were more easily met, the optimizer provided the capability of weighting the optimization goals differently. This feature was of great help to ensure a good result.

3.7 Designing matching networks - Specific approach

The previous section presented the general method of obtaining the optimal reflection coefficients and the procedure of how the matching networks were realized. This section however, will go through the design specific tradeoffs and what was emphasized when finding the reflection coefficients. Note that some of the sections have been combined, as the matching networks were based on the same procedure. Pictures, circuit diagrams and PCB layout have been included in the Appendices C, D and E.

3.7.1 Design 1: Single-Stage

Input Matching Network

The input matching network was optimized with respect to the small signal gain. This was done by matching the 10W transistor as close to 50Ω as possible, by the help of the previously found reflection coefficients. To achieve the requirement of having a gain ripple less than 0.5dB, some manual tuning were done, and the resulting small signal gain varied between 11.3-11.7dB. The optimal reflection coefficients and the reflection coefficients of the realized matching network are shown in Figure 3.12 and 3.13, respectively.

Output Matching Network

As mentioned above, the load pull bench was used to find the optimal reflection coefficients at the output of the transistor at the five frequencies and their accompanying second harmonics. The reflection coefficients at the fundamental frequencies were optimized with respect to output power, while the reflection coefficients for the second harmonics were optimized with respect to efficiency.

By experimenting with different matching network topologies, the matching network with the corresponding impedances shown in Figure 3.13 were found to give the best result. The optimal impedances are plotted in Figure 3.12

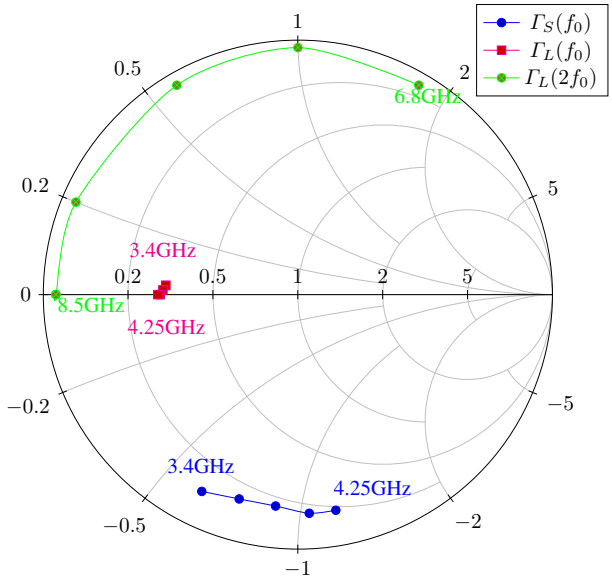


Figure 3.12: Optimal reflection coefficients for input match, $\Gamma_S(f_0)$, and output match, $\Gamma_L(f_0)$ and $\Gamma_L(2f_0)$ - Design 1.

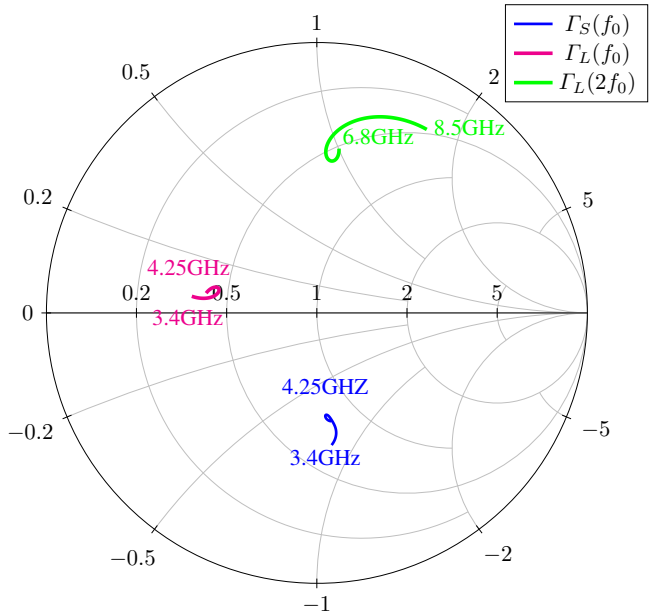


Figure 3.13: Realized reflection coefficients for input match, $\Gamma_S(f_0)$, and output match, $\Gamma_L(f_0)$ and $\Gamma_L(2f_0)$.

3.7.2 Design 2 & 3: Two-Stage

Design 2 and 3 are based on the same circuit topology. The main difference is the output matching network at the second stage. As previously stated, design 2 has utilized a common matching network for the balanced second stage, while design 3 has two separately matched transistors followed by a power combiner. Unlike design 1, the dual-stage designs utilizes the 6W transistor and thus requiring separate source- and load-pull simulations to find the optimal reflection coefficients. The following sections will present the details of design 2 and 3.

First and Second Stage Input Matches

The first and second stage input matches were at first identical as they were both based on the same reflection coefficients. The ideal reflection coefficients were optimized to provide high small signal gain whilst the input return loss was minimized. As it turned out to be difficult to comply the return loss requirement, a T-attenuator was added at the input to fulfill the requirement. The equations presented in Section 2.10 were used to calculate the initial values of the resistor that corresponded to a loss of 1.5dB. The values of the resistors were 4.3Ω and 293Ω. However, these values showed only an attenuation of 1.4dB in the simulations and manual tuning were done in order to achieve the requirement. The final attenuator was made by two 4.7Ω resistors and a 330Ω resistor.

Unfortunately, this reduced the total small signal gain, however the as the two stages produced a total gain of approximately 22dB a reduction of 1.5dB still fulfilled the requirements by 6.5dB.

To provide a small signal gain with ripple less than 0.5dB, the input matching network for both stages were separately tuned until a satisfying result was obtained. The optimal impedances is shown in Figure 3.14 (blue line), while the realized impedances are shown in Figures 3.15, 3.16, 3.17 and 3.18 (blue lines).

Another solution of implementing the second stage input matches were also considered. Since the output match of the first stage included a DC-block it was possible to omit the DC-blocks in the intermediate match, and use a common DC-feed for the two transistors in the second stage. However, it was desirable to be able to control the drain current of each transistor individually, as production variations may change the required bias voltage to obtain the same drain current. Hence it was necessary to include DC-blocks in the second stage input match.

Output Match - First Stage

The procedure of designing the output match of design 2 and 3 was exactly the same as design 1, and will not be repeated. However, the optimal impedances were different and can be seen in Figure 3.14 (magenta colored line). The input impedances for the realized network can be seen in Figure 3.15 and 3.17 (magenta colored lines).

Design 2: Output Match - Second Stage

The output match of the second design, was made by connecting the outputs of each transistors together with a tee-junction, followed by a load pull measurement to find the opti-

mal output reflection coefficients. The reflection coefficients for the fundamental frequencies were optimized with respect to output power and the second harmonics with respect to efficiency. Figure 3.14 shows the optimal impedances (purple and red line).

Several matching networks were simulated in order to find the one that could match the optimal impedances best. The input impedances for the matching network that gave the best result has been plotted in Figure 3.16 (magenta colored line).

Design 3: Output Match - Second Stage

In design 3, the outputs at the second stage were matched separately by to identical networks followed by a power combination circuit. Like design 1 and 2, the two output matching networks were based on the reflection coefficients found by utilizing the load pull tuner at one of the outputs terminated to 100Ω. The matching networks were then combined in parallel and the resulting output impedance became 50Ω.

Since the realized matching networks are suboptimal, compared to the optimal load-pull values and were combined without isolation, each network influences the other's impedance and leads to a greater matching deviation. As seen in Figure 3.18, the impedance of the realized network are far from the optimal impedances at certain frequencies, but the overall performance is satisfying.

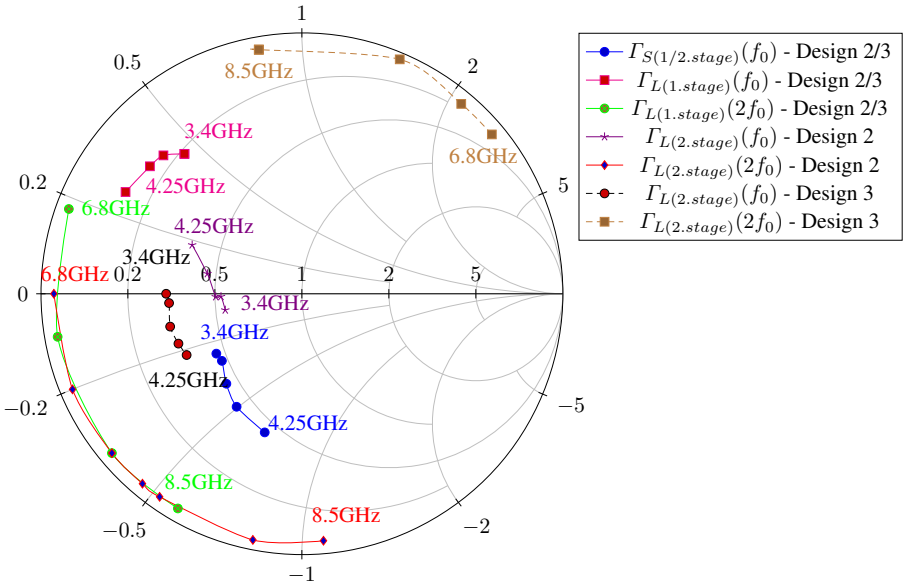


Figure 3.14: Optimal impedance for input and output matching networks. The matching networks in design 2 and 3 are based on the same optimal impedances except output match at second stage.

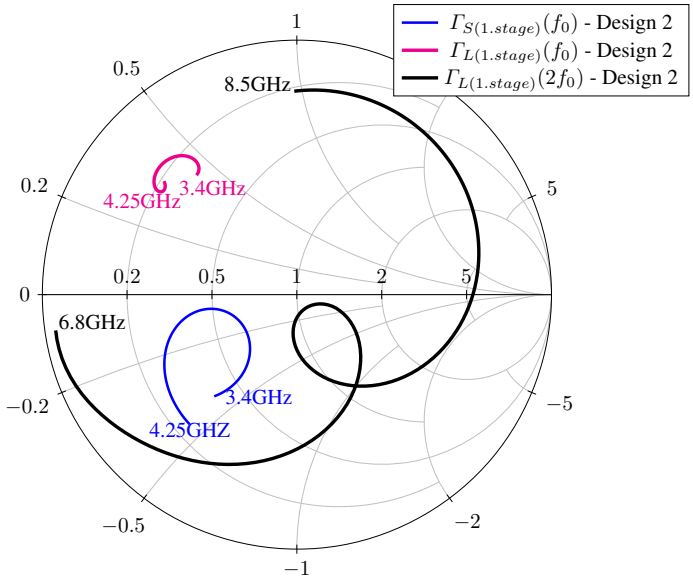


Figure 3.15: Design 2: The impedance of the realized output matching network at first stage.

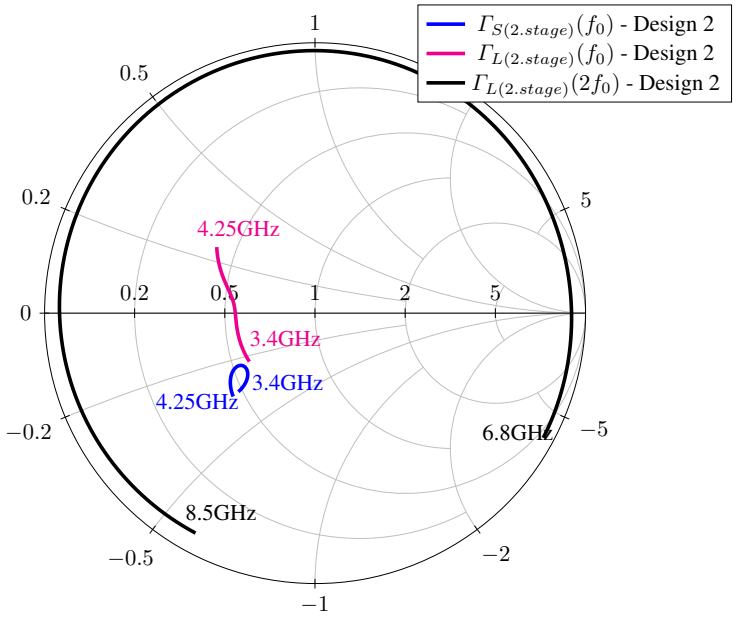


Figure 3.16: Design 2: The impedance of the realized output matching network at second stage.

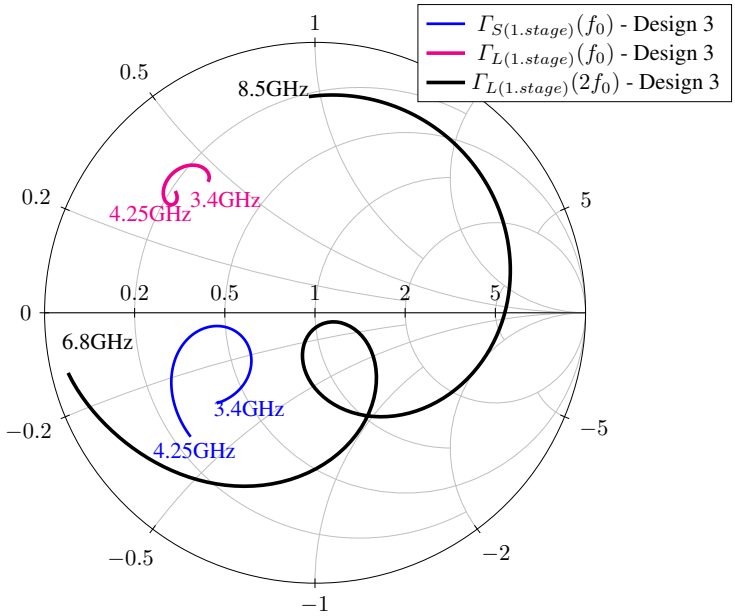


Figure 3.17: Design 3: The impedance of the realized matching networks at first stage.

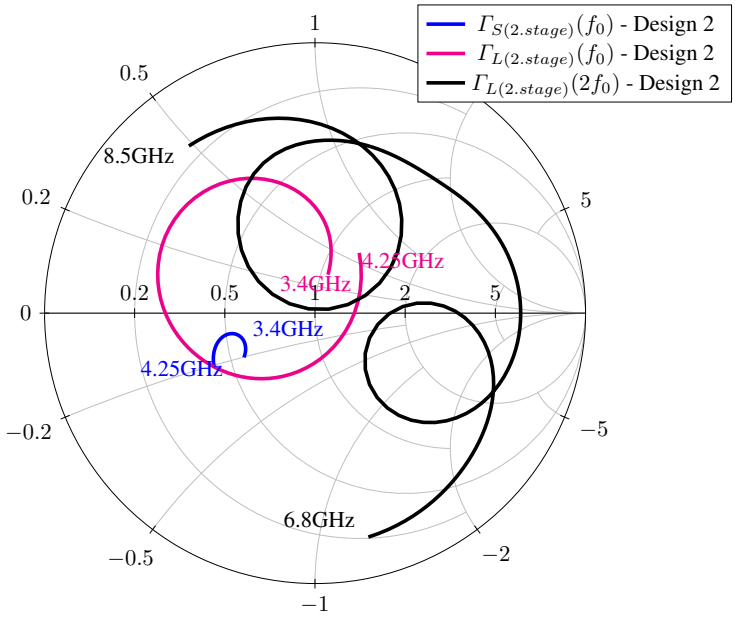


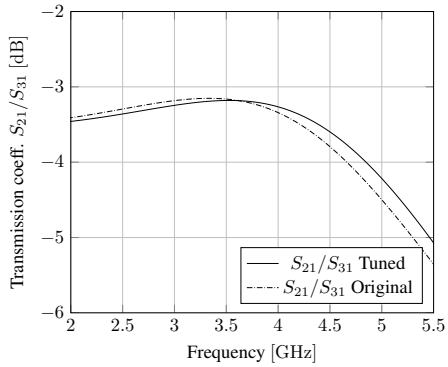
Figure 3.18: Design 3: The impedance of the realized matching networks at second stage.

3.8 Wilkinson Power Divider

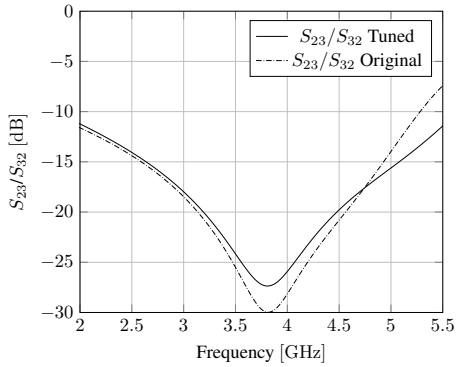
The Wilkinson power divider was designed using a function in ADS called ”LineCalc”. It has the ability of calculate the width and the length of a microstrip line based on the parameters of the substrate, the frequency of operation, the impedance and electrical length specified by the designer. Since each stage in design 2 and 3 had been matched to 50Ω, the characteristic impedance, Z_0, of the Wilkinson power divider was set to 50Ω. This meant that the impedance of the two quarter wavelength microstrip lines had to be approximately 70.7Ω and that the isolation resistor had to be 100Ω.

Together with center frequency (3.825GHz), the electrical length of 90° and the substrate parameters, the LineCalc function then calculated the width and length of the quarter wave line to be 1,04mm and 7.2mm, respectively.

Due to the physical dimensions of the substrate, the maximum length of the total design had to be less than 30cm. The length of the quarter wavelength microstrip lines were shortened to 6.4 mm and the isolation resistor was changed to 150Ω. Due to this change, the coupling between the two output ports increased about 2.6dB at the center frequency and 1-2dB at the edges. However, the transmission through the two branches got enhanced at the upper part of the frequency band. The S-parameters for the Wilkinson power divider is plotted in Figure 3.19. This modification was necessary to accommodate the entire circuit.



(a) Comparison of the original and tuned transmission coefficients, S_{21}/S_{31}, of the Wilkinson power divider.



(b) Comparison of the original and tuned transmission coefficients, S_{23}/S_{32}, of the Wilkinson power divider.

Figure 3.19: Comparison of the original and tuned transmission coefficients, S_{21}/S_{31} and S_{23}/S_{32}, of the Wilkinson power divider. The tuned version achieves better power splitting results than the original, but the isolation between the output ports decreases.

3.9 Measurement configuration

This section will describe how the small and large signal measurements were done. All measurements were performed at the microwave laboratory at NTNU, and the equipment used for measurements are listed in Appendix A.

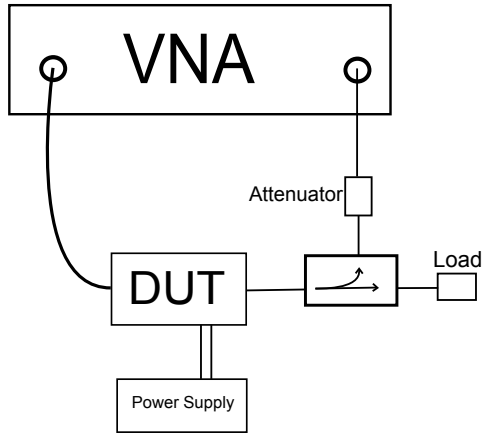


Figure 3.20: Small signal measurement setup

3.9.1 Small signal measurements

The small signal measurement setup are seen in Figure 3.20. The S-parameter measurements were performed by an Agilent E836B network analyzer. A directional coupler in combination with an attenuator ensured that the output power of the power amplifier did not exceed the maximum rated level of the VNA. Before the measurement was done, a SOLT calibration procedure were performed in order to remove the different errors explained in Section 2.13, and to move the reference plane to the point where the power amplifier was connected.

Despite that the loss in the coupler and the attenuator is removed in the calibration procedure, S_{12} and S_{22} will suffer from additional attenuation due to several passes through the attenuators. Hence, S_{12} and S_{22} will be less noise resistant and will lead to inaccurate measurements. For this reason, these results are omitted.

3.9.2 Large signal measurements

Due to the shape and the modulation of the TT&C signal, only single tones measurement was performed.

The measurement setup is shown in Figure 3.21. Since the signal generator is only capable of delivering a maximum of 26dBm, one of the other designs were used as a preamplifier to be able to drive the DUT into compression. A circulator between the to amplifiers ensures that both are terminated to 50 Ω, and that the reflected signal at the input of the DUT is not transmitted back to the driver.

The output of the DUT is connected to a coupler which splits the signal into two parts and terminates one of them. The other signal is attenuated and connected to the spectrum analyzer. The measured data, which includes output power of the signal generator, drain current and output power, are then stored on a computer. The coupler and the attenuator are used for the same reason as stated in Section 3.9.1.

The stored measurements contains unprocessed data and the loss through the coupler,

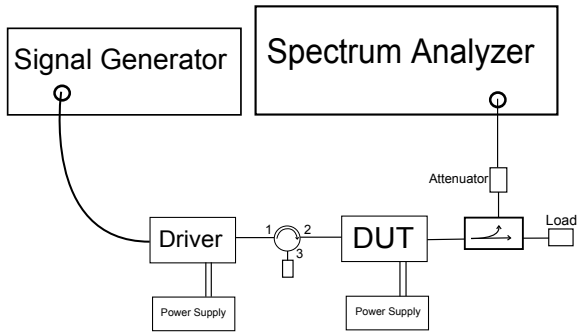


Figure 3.21: Large signal measurement setup

attenuator and cable needs to be compensated. This was done by measuring the attenuation through these components with the VNA and then added to the corresponding large signal measurements.

Chapter 4

Results

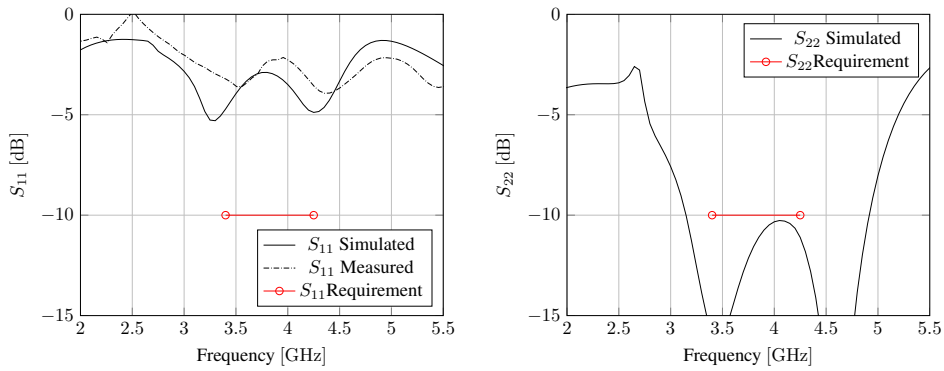
This chapter contains the simulated and the measured results of the three designs. It is divided into four sections and the first three presents the small and large signal results of each design. The last section summarizes the key numbers at 40dBm output power. Simulated noise figure plots for each PA is included in Appendix F due to the requirements. Normally, when dealing with power amplifiers, the noise figure is of little interest.

4.1 Results - Design 1

4.1.1 Small signal results

Figure 4.1a shows the resulting simulated and measured input reflection coefficients. It shows that the simulated result has been overestimated compared to the measurements. In addition, the measured characteristic has been shifted to the right. Still, the overall performance is not satisfying, as the requirement is between -5dB to -7.5dB below the simulated, as well as the measured results, in the specified frequency range.

The output reflection coefficient in Figure 4.1b is below -10dB between 3.2GHz and 4.9GHz and consequently satisfies the requirement of -10dB output reflection coefficients between 3.4GHz and 4.25GHz. The curve has a local maxima of -10.2dB around 4GHz which is the closest point S_{22} will come to the requirement. Due to small-signal measurement procedure, the measurement results of S_{22} is inaccurate, and hence been omitted.



(a) Comparison of simulated and measured input reflection coefficient, S_{11} - Design 1

(b) Simulated output reflection coefficient, S_{22} - Design 1

Figure 4.1: Simulated input and output reflection coefficients - Design 1

The small-signal gain is shown in Figure 4.2. The achieved simulated gain varies between 11.3dB and 11.7dB and achieves the requirement of less than 0.5dB gain ripple per 500MHz. However, the single-stage design does not fulfill the requirement of having 14dB gain throughout the bandwidth.

The dotted line in Figure 4.2 represents the measured small signal gain. Generally it follows the simulated curve, but at the lower half of the frequency range the gain drops bellow 10dB. Hence the amplifier does not satisfy the ripple requirement.

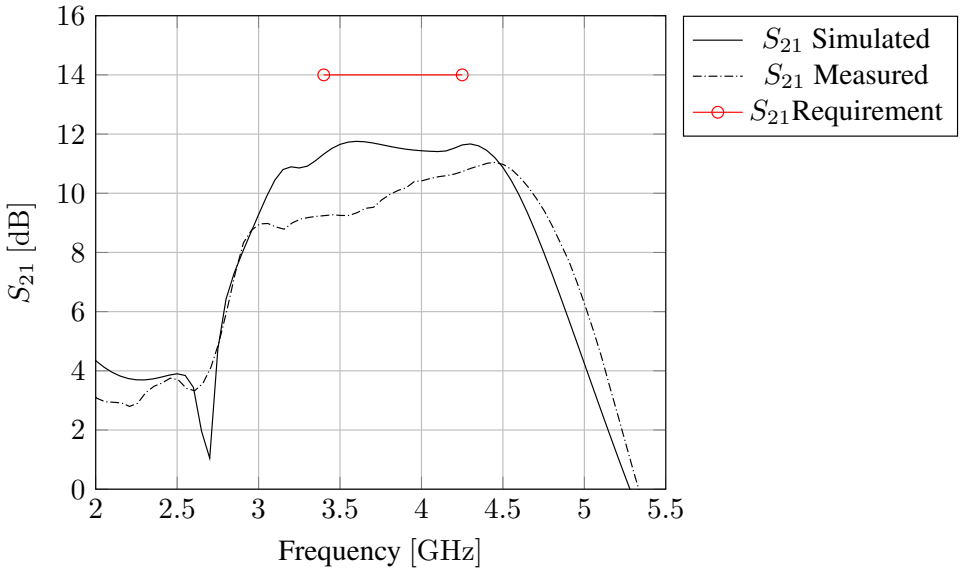


Figure 4.2: Comparison of simulated and measured S_{21} - Design 1

4.1.2 Large signal results

The P_{in}/P_{out}-plot for the simulated circuit are shown in Figure 4.3. It reveals that the power characteristics for all five frequencies in general follows each other and enters the compression region for the same input power. According to the simulations the amplifier is able to deliver 40dBm before entering the compression region and around 40.8dBm (12W) well into compression.

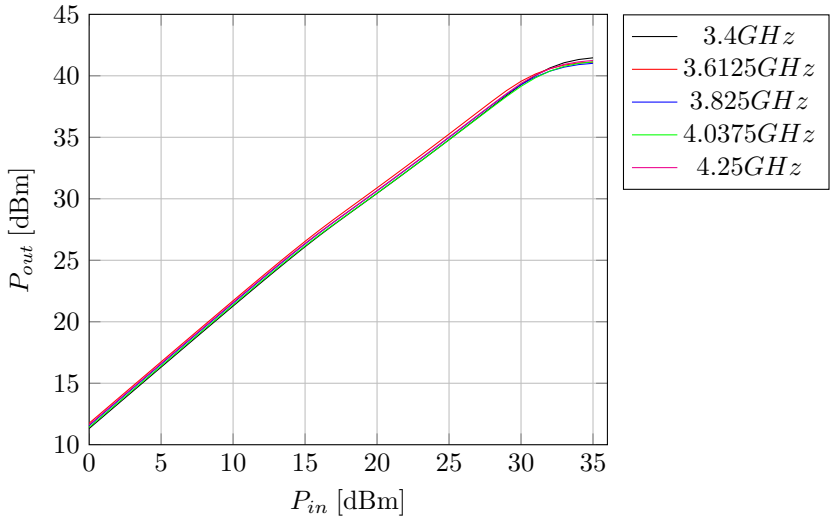


Figure 4.3: Simulated P_{in}/P_{out}-characteristics at five different frequencies - Design 1

The measured P_{in}/P_{out} results are plotted in Figure 4.4 and shows a small variation among the five plots. The amplifier is capable of delivering 40dBm at all frequencies except at 4.0375GHz. It peaks with an output power of 39 dBm at around 33dBm input power.

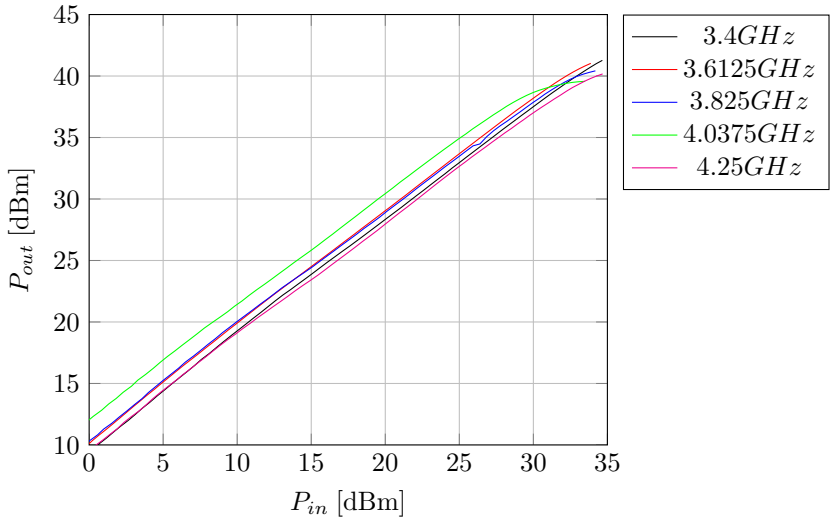


Figure 4.4: Measured P_{in}/P_{out}-characteristics at five different frequencies - Design 1

Figure 4.5 shows the simulated power added efficiency (PAE). At 40dBm output power, the PAE is above 45% for for all frequencies. Compared to the simulated results, the measured characteristics are shown in Figure 4.6. It reveals that the PAE for are generally lower at 40dBm input power, except the PAE-curve at 3.4GHz which reaches 45%.

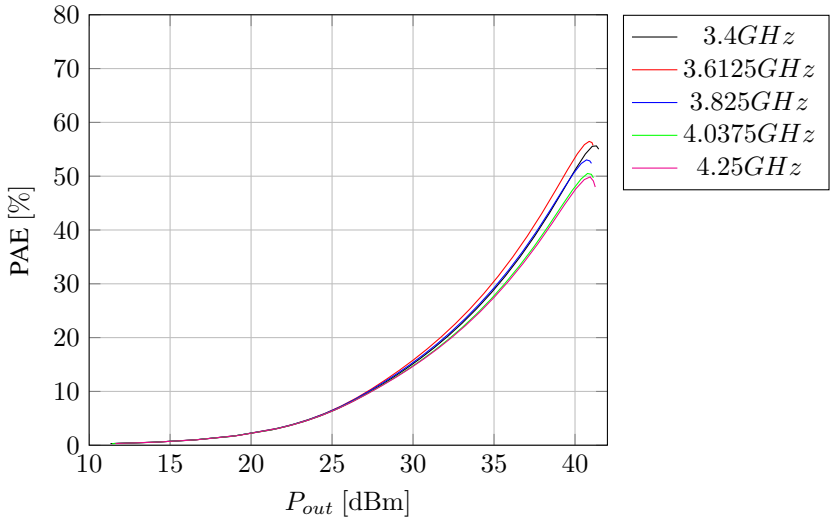


Figure 4.5: Simulated PAE at five different frequencies - Design 1

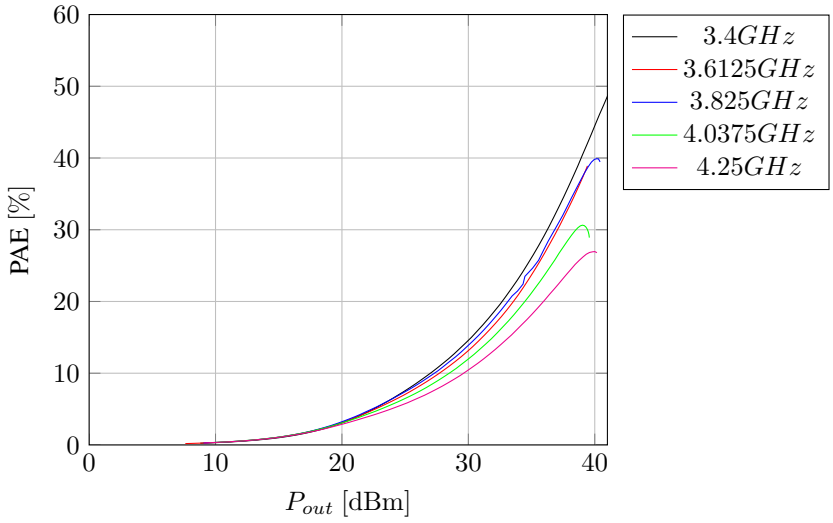


Figure 4.6: Measured power added efficiency at five different frequencies - Design 1

The simulated and measured drain efficiency are plotted in Figure 4.7 and 4.8, respectively. And the results of the simulated drain efficiency shows that it is well above 50% for all frequencies. The measured response however, reveals for the two highest frequencies that, the drain efficiency barely reaches 35%. For the three lowest frequencies the drain efficiency is greater than 50%.

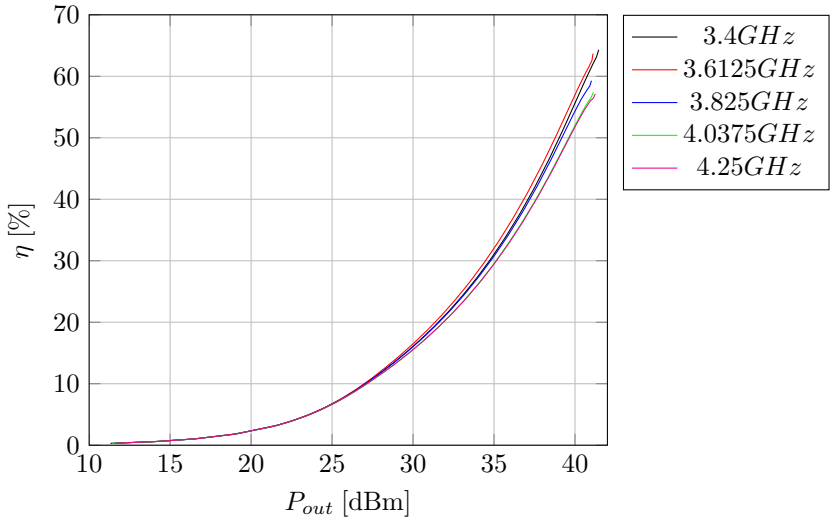


Figure 4.7: Simulated drain efficiency at five different frequencies - Design 1

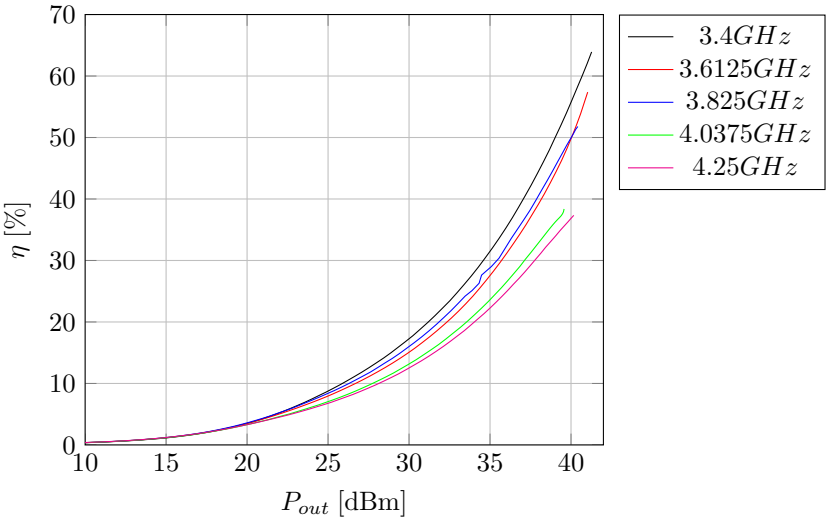


Figure 4.8: Meausred drain efficiency at five different frequencies.

The simulated transducer gain is plotted in Figure 4.9. The transition from the linear region to compression is clearly seen between 39dBm-40dBm and around 27dBm output power, the transistor goes from operating in class A to operate as a class AB amplifier. The measured transducer gain varies much more than the simulated, and at 4.0375GHz, the gain is approximately 2dB higher compared to the other four frequencies. The measured gain curves can be seen in Figure 4.10

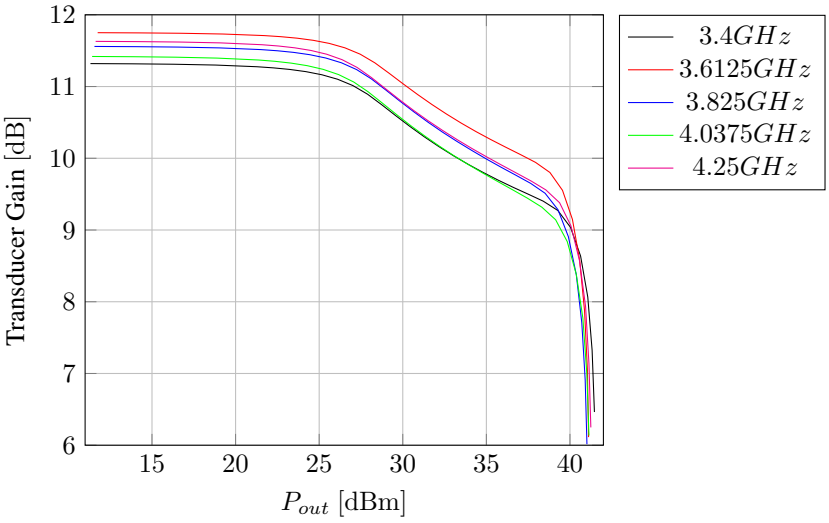


Figure 4.9: Simulated transducer gain at five different frequencies.

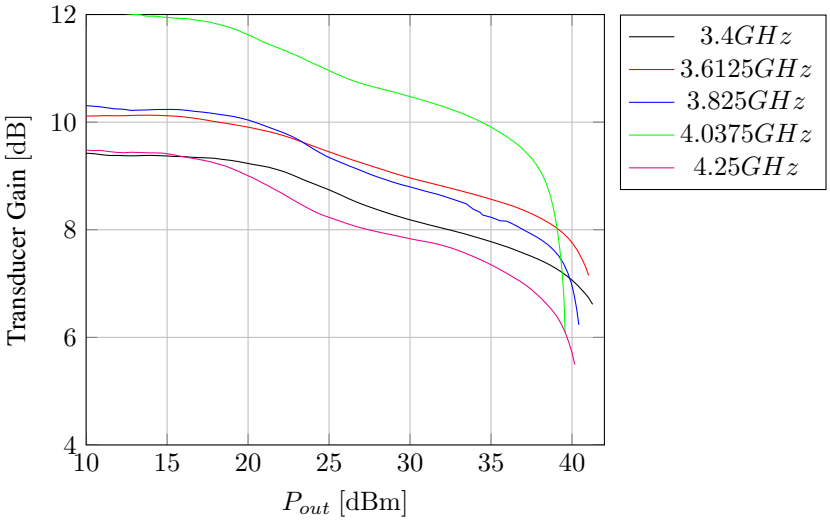
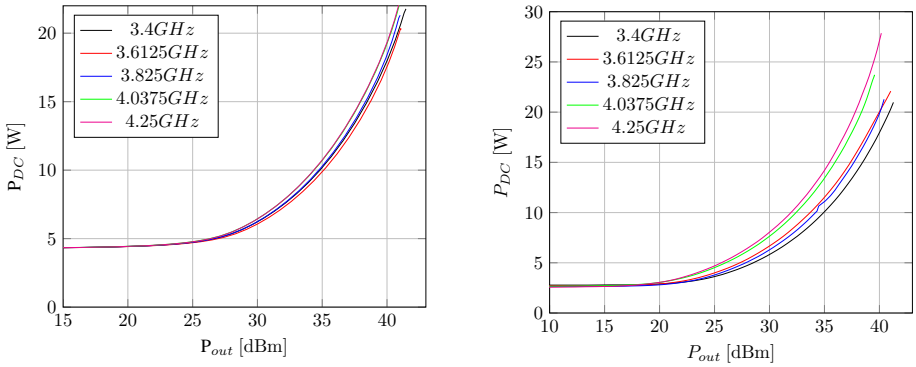


Figure 4.10: Measured transducer gain at five different frequencies - Design 1

The DC-power consumption for the simulated and the measured case are both displayed in Figure 4.11. By comparing the two plots, it is possible to see that the simulated results are about 1.2W greater than the measured, but for unknown reasons.[1] As the transistor was biased at 100mA, the resulting quiescent power consumption would be 2.8W with a drain voltage set to 28V.

The measured power consumption shows that the requirement of using maximum 25W is exceeded for the two highest frequencies.



(a) Simulated DC power consumption

(b) Measured DC power consumption

Figure 4.11: Simulated and measured DC power consumption - Design 1

[1] Simulation setup, equations and circuit have been checked in ADS, but no errors were found.

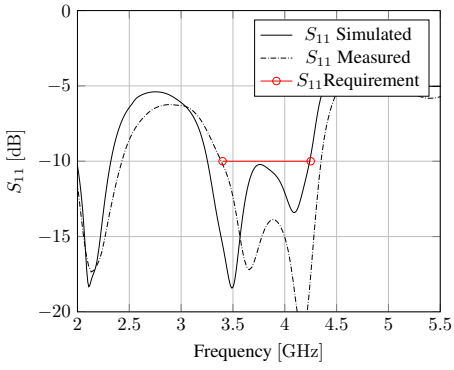
4.2 Results - Design 2

4.2.1 Small signal results

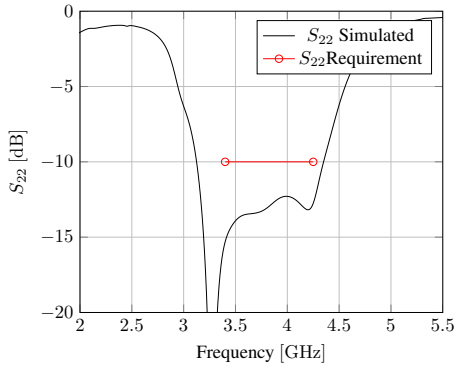
Figure 4.12a shows the simulated and measured input reflection coefficients. Both plots are quite similar despite the right shift of the measured characteristic and complies the requirement of -10dB input return loss. The measured result shows that S_{11} is even lower than simulated result.

The output reflection coefficient, S_{22}, shown in Figure 4.12b meets the requirement of -10dB output return loss by 2dB or more between 3.2GHz to 4.3GHz.

In Figure 4.13 the results of the simulated and measured small-signal gain are plotted. The two-stage amplifier has a simulated gain between 21.27dB and 21.77dB which just fulfills the ripple requirement. The measured gain curve shows that the simulated model is quite good, but has over estimated the gain between 3.3GHz to 3.9GHz. At the lower part of the frequency band the gain is approximately 20dB while in the upper part is almost the same as the simulated value. Hence the ripple requirement has not been achieved.



(a) Comparison of simulated and measured input reflection coefficient, S_{11}.



(b) Simulated output reflection coefficient, S_{22}.

Figure 4.12: Simulated input and output reflection coefficients - Design 2

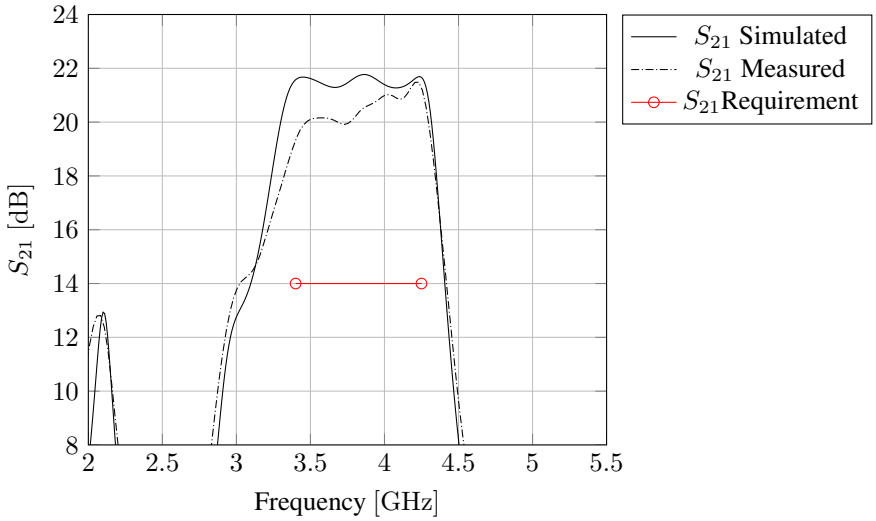


Figure 4.13: Comparison of simulated and measured S_{21} - Design 2

4.2.2 Large signal results

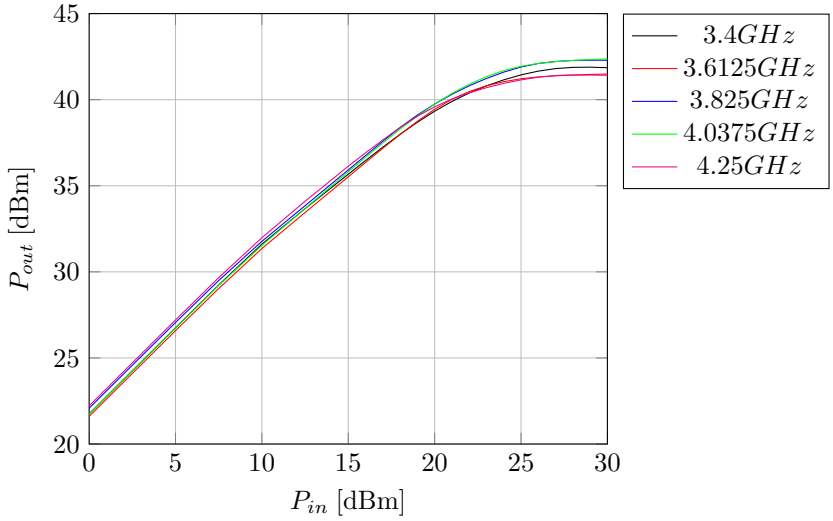


Figure 4.14: Simulated P_{in}/P_{out}-characteristics at five different frequencies - Design 2

As seen from Figure 4.14 the amplifier reaches 40dBm output power around 21dBm input power. This means that the gain have been reduced by approximately 2dB compared to the small-signal simulations. Well into the compression region, the amplifier delivers between 41.2dBm (13.2W) and 42.1dBm (16.2W).

Figure 4.15 shows the P_{in}/P_{out}-characteristics for the realized amplifier. It shows that the gain have been reduced compared to the simulated results. Between 22dBm and 25dBm in the amplifier is capable of delivering 40dBm output power and the output power continues to increase all the way up to approximately 42dBm.

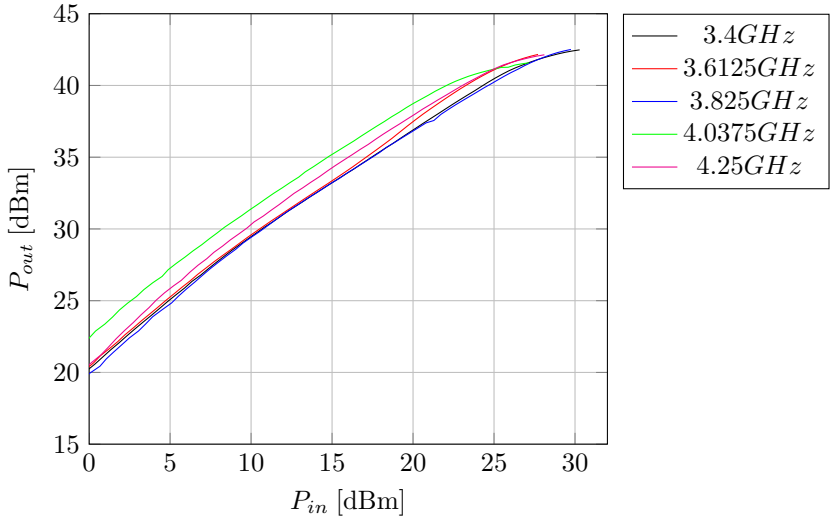


Figure 4.15: Measured P_{in}/P_{out}-characteristics at five different frequencies - Design 2

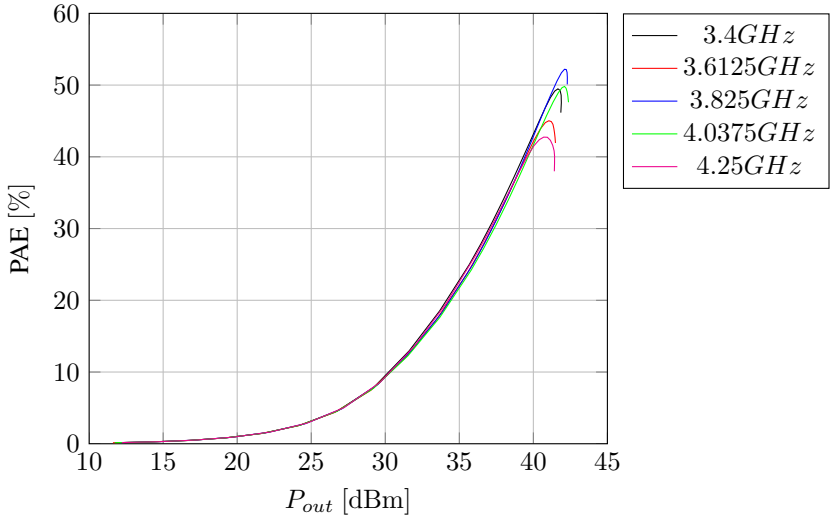


Figure 4.16: Simulated PAE at five different frequencies - Design 2

Figure 4.16 shows the simulated PAE of the second design. For the highest frequency

the maximum PAE is 42.5%, while the maximum PAE regardless of frequency is 52%. According to the simulated results the amplifier will have a PAE between 41% and 44% when delivering 40dBm.

The measured power added efficiency is plotted in Figure 4.17. It shows that the PAE varies between 39% and 49% at 40dBm output power. This results matches the simulated results well, and for the center frequency, the PAE exceeds 60% which is about 8% better than the corresponding simulated result.

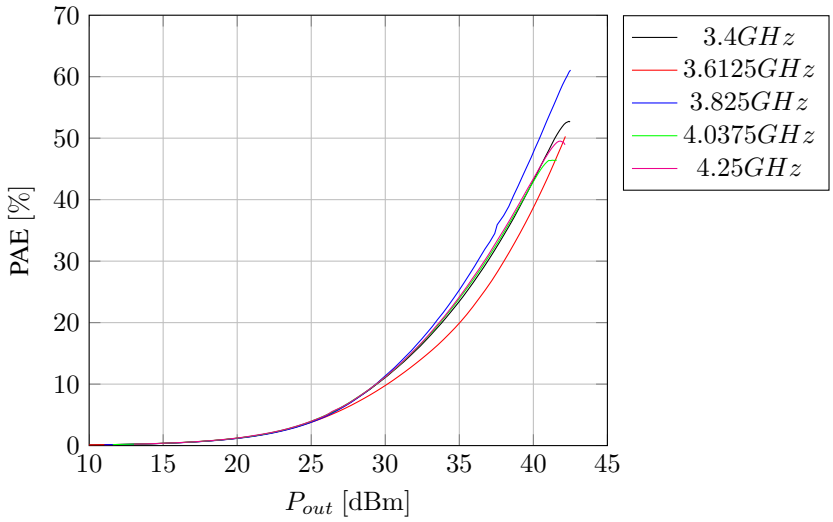


Figure 4.17: Measured power added efficiency at five different frequencies - Design 2

Figure 4.18 displays the drain efficiency at the five frequencies. It shows that all follows approximately the same curve up to 41dBm output power, then the amplifier goes into the compression area and the drain efficiency starts to decrease for the 4.25GHz-curve. At 40dBm output power the drain efficiency is varying between 41%-42% throughout the frequency range.

The measured drain efficiency characteristics for the second design is shown in Figure 4.19. And the highest achieved drain efficiency was at the center frequency. With an efficiency of almost 50%, it is between 5%-10% higher than the other frequencies.

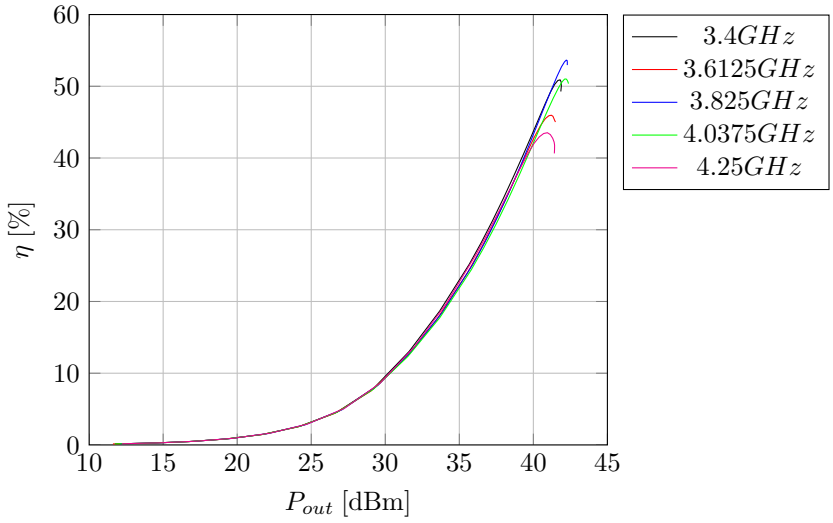


Figure 4.18: Simulated drain efficiency at five different frequencies - Design 2

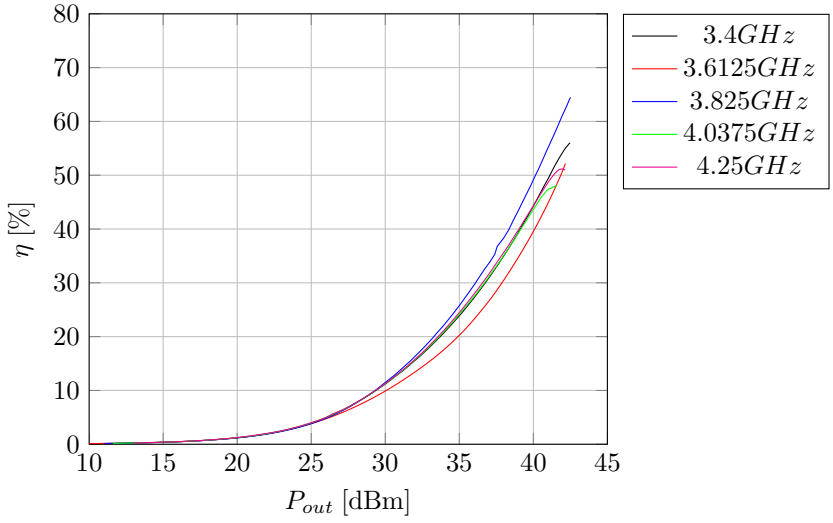


Figure 4.19: Measured drain efficiency at five different frequencies - Design 2

The curves shown in Figure 4.20 has a flat gain characteristic up to 30dBm before the PA moves into class AB operation. At 40dBm output power the gain has dropped about 3dB. Comparing the measured results in Figure 4.21, it is only the gain curve corresponding to 4.0375GHz which matches the simulated gain, the rest have decreased with 1dB-2dB. At 40dBm output power the gain has dropped nearly 5dB for the most extreme cases. However, the amplifier has not reached the compression region yet. This does not

happen until the amplifier outputs 41dBm-42dBm.

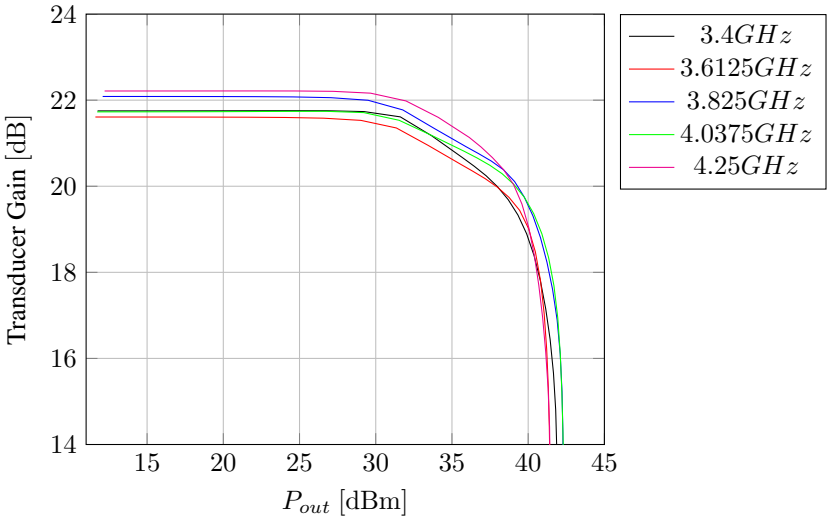


Figure 4.20: Simulated transducer gain at five different frequencies - Design 2

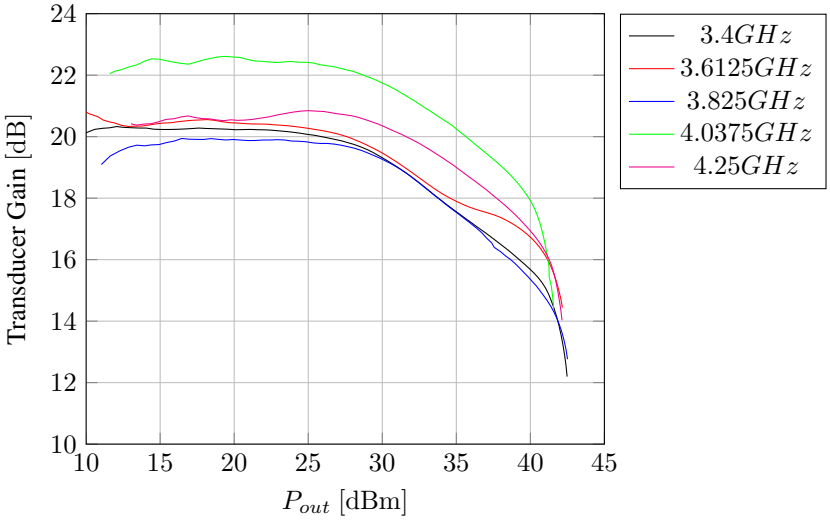
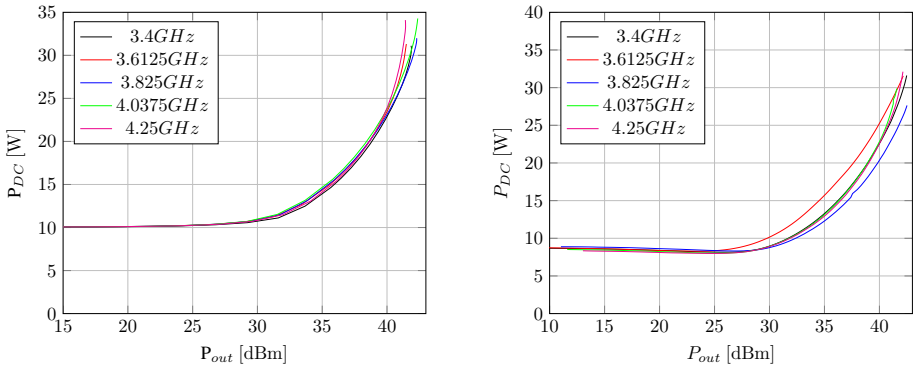


Figure 4.21: Measured transducer gain at five different frequencies - Design 2

Figure 4.22a and 4.22b shows the simulated and measured DC power consumption, respectively. The curves from each figure follows approximately the same slope and both starts to rise at around 30dBm output power. As seen from both figures, the amplifier barely fulfills the requirement of consuming less than 25W at 40dBm.



(a) Simulated DC power consumption

(b) Measured DC power consumption

Figure 4.22: The simulated and measured DC power consumption of amplifier - Design 2

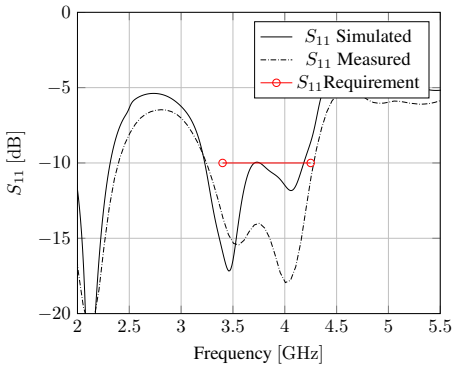
4.3 Results - Design 3

4.3.1 Small signal results

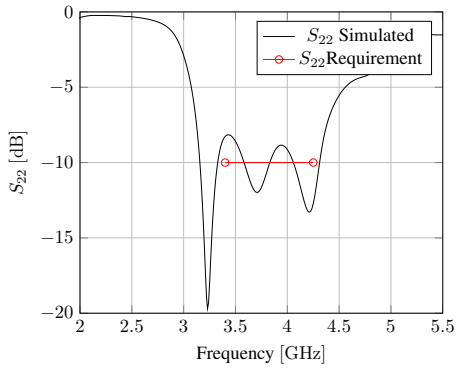
The results of the simulated and measured input reflection coefficients are plotted in Figure 4.23a. The simulated characteristics complies the requirements almost throughout the frequency band, except at 3.75GHz and between 4.2GHz and 4.25GHz as it barely creeps above the input return loss requirement. However, the measured results shows that the input reflection coefficient meets the requirement from 3.25GHz to 4.55GHz.

Figure 4.23b shows the output reflection coefficient. It varies between -8.8dB and -13dB inside the specified frequency band, and hence does not obtain the requirements.

The small-signal gain results, from the simulations and measurements, are plotted in Figure 4.24. The simulated gain fluctuates between 20.2dB and 20.8dB, while the measured small-signal gain spans from 20dB to 21.6dB. The increase in gain at the upper end of the frequency band is most likely caused by the improvement of S_{11} in the same frequency range. Due to the gain variation, this design does not fulfill the ripple requirement. However, the gain requirement of 14dB or higher, is achieved.



(a) Comparison of simulated and measured input reflection coefficient, S_{11}.



(b) Simulated output reflection coefficient, S_{22}.

Figure 4.23: Simulated input and output reflection coefficients - Design 3

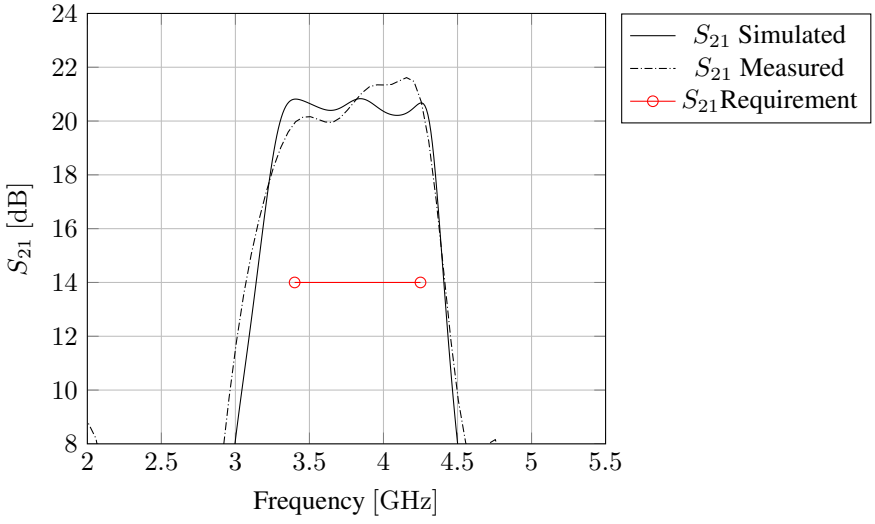


Figure 4.24: Comparison of simulated and measured S_{21}. Design 3

4.3.2 Large signal results

The simulated P_{in}/P_{out}-characteristics are shown in Figure 4.25. Between 22dBm-23dBm input power, the amplifier delivers 40dBm output power before it enters the compression region at around 25dBm. By increasing the input power further, the PA is capable of delivering between 42dBm and 42.5dBm output power.

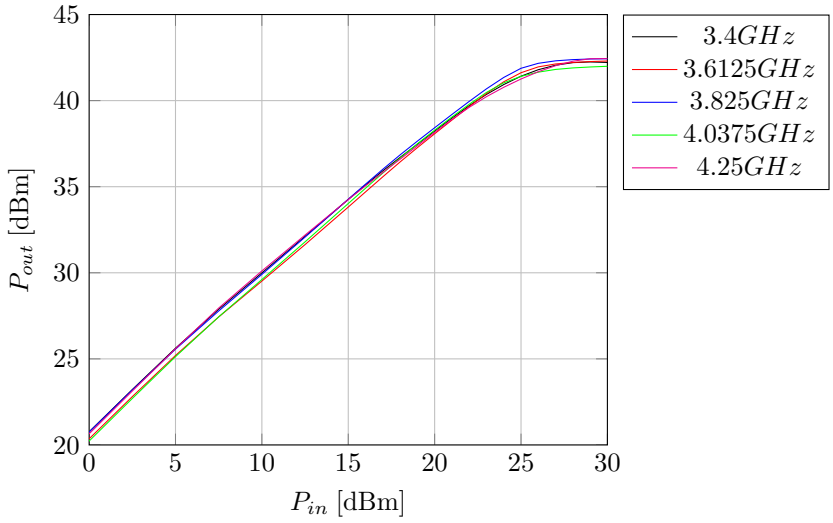


Figure 4.25: Simulated P_{in}/P_{out}-characteristics at five different frequencies - Design 3

Figure 4.26 shows the measured P_{in}/P_{out}-curves for the third design. Compared to the simulated results, the achieved performance of the realized amplifier are generally good. All frequencies except the center frequency have gain greater than 20dB at low input power level. The amplifier is able to output 40dBm between 22.5dBm and 25dBm input power. The maximum measured output power was 43.5dBm at 3.825GHz.

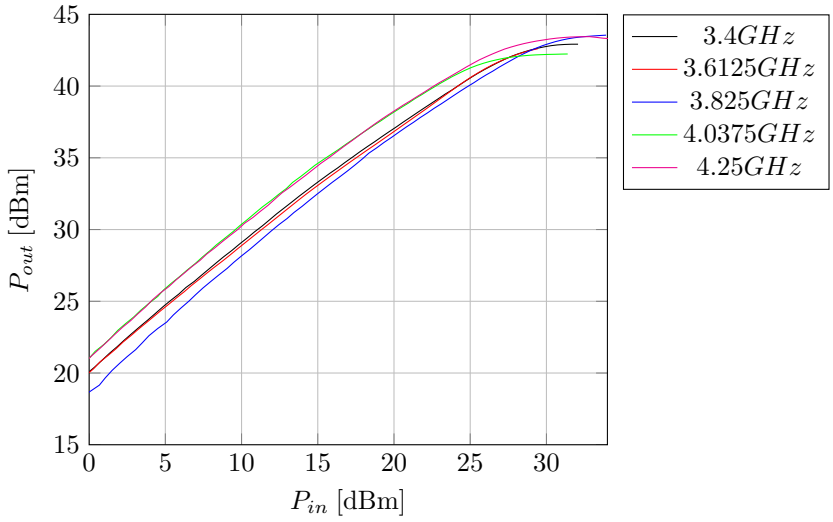


Figure 4.26: Measured P_{in}/P_{out}-characteristics at five different frequencies - Design 3

According to Figure 4.27 the power added efficiency will be around 36% depending

on the frequency when delivering 40dBm. The maximum PAE the amplifier achieves is 44.2%, which is at 3.6125GHz, well into compression. The amplifier has a PAE of 40% or more from 25dBm input power.

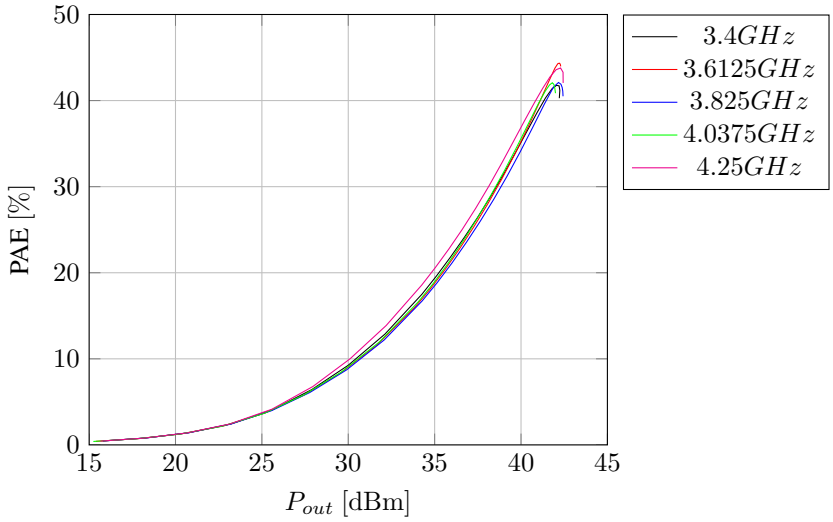


Figure 4.27: Simulated PAE at five different frequencies - Design 3

The measured PAE in Figure 4.28, shows that the amplifier has an efficiency greater than 40% at 3.825GHz and 4.25GHz at 40dBm output power, while the other three frequencies have an efficiency around 35% at the same input level. It is noticeable that the amplifier has been driven into deep compression as some of the curves decreases at around 42dBm output power.

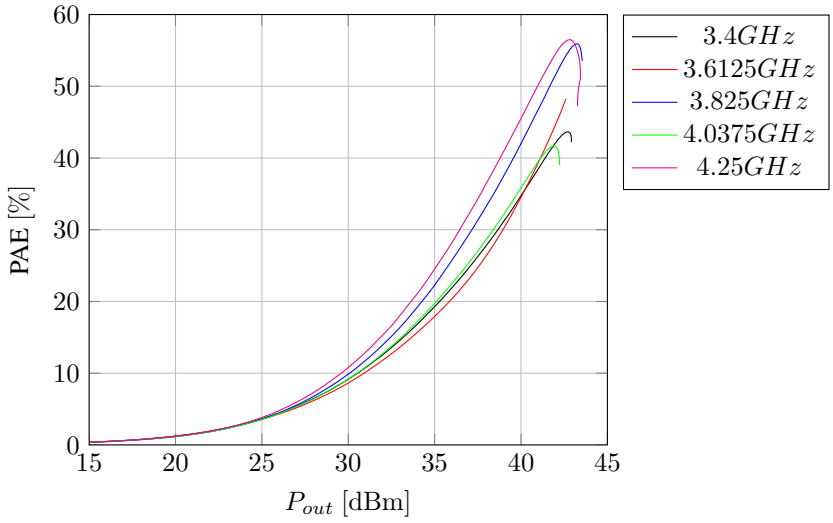


Figure 4.28: Measured power added efficiency at five different frequencies - Design 3

The results of the simulated and measured drain efficiency can be seen in Figure 4.29 and 4.30, respectively. The measured results reveals that the actual performance is almost equal or better than the simulated results. At 40dBm output power, the simulated circuit has a drain efficiency between 34% and 37%. The measured results however, shows that a drain efficiency of 44%-46% is achieved at 3.825GHs and 4.25GHz.

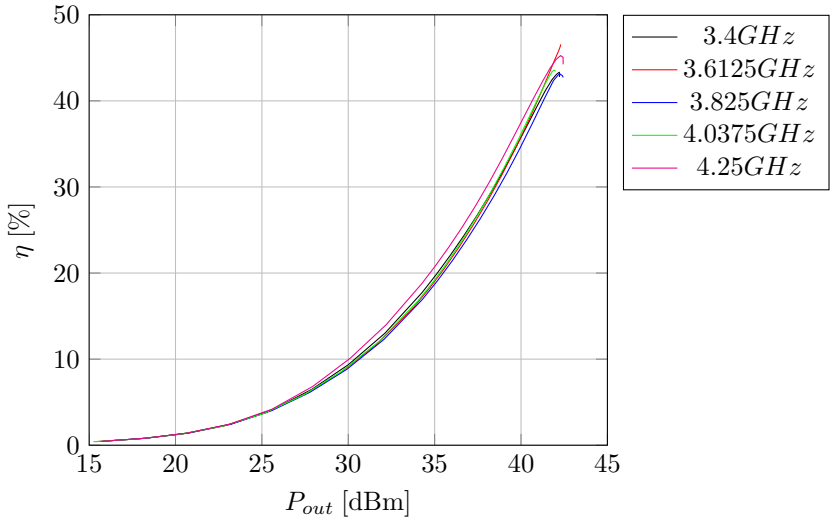


Figure 4.29: Simulated drain efficiency at five different frequencies - Design 3

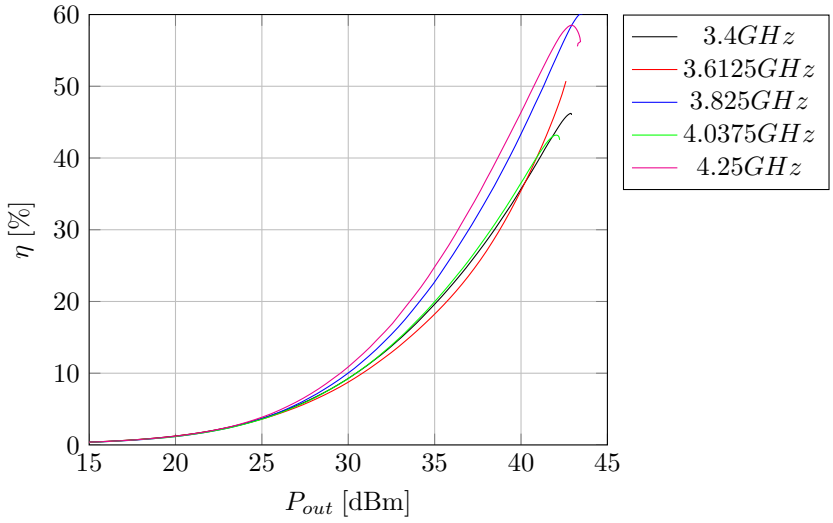


Figure 4.30: Meausred drain efficiency at five different frequencies - Design 3

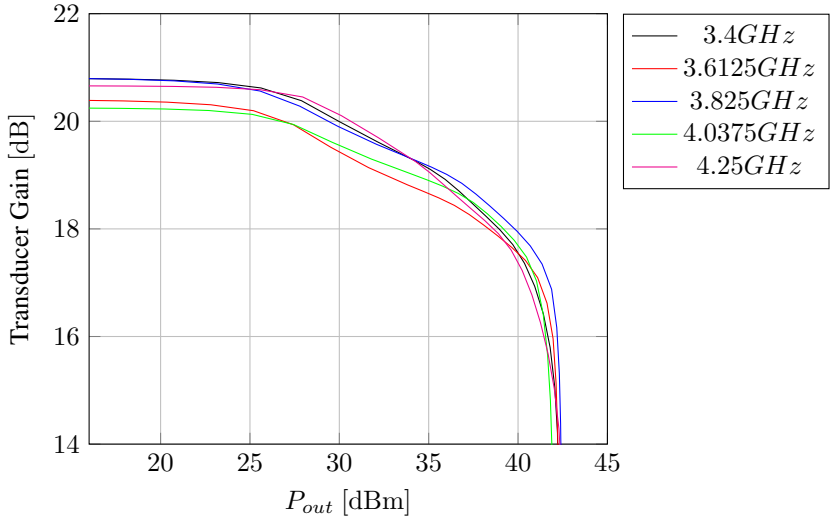


Figure 4.31: Simulated transducer gain at five different frequencies - Design 3

The simulated transducer gain at the five frequencies are shown in Figure 4.31. At 20dB back-off the power amplifier operates in class A and the obtained gain varies between 20.2dB and 20.8dB. As the output power increases, the amplifier goes into class AB operation. At 40dBm output power the gain has been reduced around 3.5dB.

Figure 4.32 shows the measured transducer gain related to the third design. Compared to the previous figure, it is seen that the gain corresponding to the center frequency has de-

creased almost 3dB, while the other varies between the same gain levels as in the simulated case.

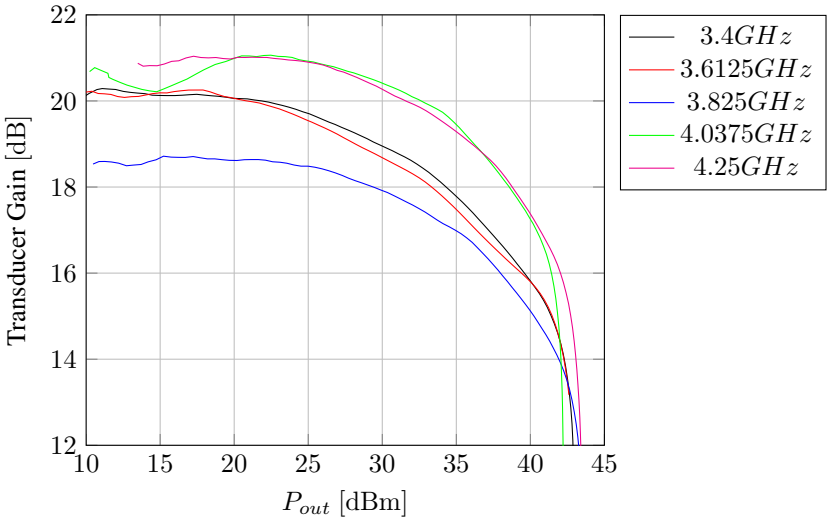
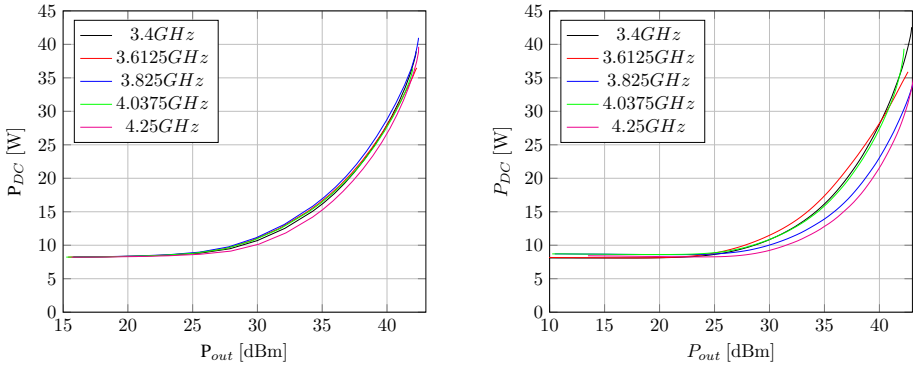


Figure 4.32: Measured transducer gain at five different frequencies.

The simulated and measured DC power consumption have both been included and can be seen in Figure 4.33a and 4.33b. Both have a quiescent DC power consumption of 8W, approximately. And does not increase significantly until the amplifier delivers 30dBm output power. The simulated results shows that the amplifier does not fulfill the power consumption requirement. However, the measured results reveals that, the curves which corresponds to 3.825GHz and 4.25GHz, have a power consumption between 22W-23W, while the other curves exceeds the requirement by approximately 2W.



(a) Simulated DC power consumption

(b) Measured DC power consumption

Figure 4.33: The simulated and measured DC power consumption of amplifier.

4.4 Performance at 40dBm output power

It was decided to include the key figures for each circuit at 40dBm output power in the main report instead of the performance at 1dB compression point, due to the fact that design 2 and 3 enters the compression region later than design 1. Please refer to Appendix B for key figures at 1dB compression point.

Table 4.1, 4.2 and 4.3 shows the key figures of the simulated circuits at 40dBm output power, while Table 4.4, 4.5 and 4.6 displays the measured figures.

It is seen that, in general, the measured circuits have poorer performance than the corresponding simulated circuits. However, at some frequencies the measurement shows better performance. For design 1, at 4.0375GHz, the amplifier did not reach 40dBm output power.

Freq. [GHz]	$\mathbf{P}_{out}$ [dBm]	$\boldsymbol{\eta}$ [%]	**PAE** [%]	**DC power** [W]	**Tr. Gain** [dB]
3.4	40	51.38	51.14	17.98	9.05
3.6125	40	54.43	53.42	17.51	9.30
3.825	40	53.86	50.87	18.37	8.84
4.0375	40	51.19	48.03	19.20	8.74
4.25	40	52.10	47.44	19.30	9.1

Table 4.1: Selected simulated key figures of design 1 at 40dBm output power. (Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{out}$ [dBm]	$\boldsymbol{\eta}$ [%]	**PAE** [%]	**DC power** [W]	**Tr. Gain** [dB]
3.4	40	43.20	43.12	22.76	18.78
3.6125	40	42.72	42.10	23.43	19.04
3.825	40	44.61	42.73	23.14	19.50
4.0375	40	43.29	41.79	23.54	19.33
4.25	40	40.65	40.30	24.49	18.65

Table 4.2: Selected simulated key figures of design 2 at 40dBm output power. (Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{out}$ [dBm]	$\boldsymbol{\eta}$ [%]	**PAE** [%]	**DC power** [W]	**Tr. Gain** [dB]
3.4	40	37.03	35.07	27.89	17.58
3.6125	40	37.25	35.23	27.92	17.55
3.825	40	37.35	34.19	28.76	17.94
4.0375	40	36.76	35.60	27.66	17.70
4.25	40	37.89	36.86	26.64	17.39

Table 4.3: Selected simulated key figures of design 3 at 40dBm output power. (Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{out}$ [dBm]	η[%]	**PAE** [%]	**DC power**[W]	**Tr. Gain**[dB]
3.4	40	56.10	44.50	17.30	7.10
3.6125	40	50.00	41.00	20.00	7.75
3.825	40	50.00	40.00	20.00	6.90
4.0375	-	-	-	-	-
4.25	40	37.00	27.00	26.40	5.80

Table 4.4: Selected measured key figures of design 1 at 40dBm output power. At 4.0375GHz the amplifier didi not reach 40dBm output power. (Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{out}$ [dBm]	η[%]	**PAE** [%]	**DC power**[W]	**Tr. Gain**[dB]
3.4	40	45.00	43.00	22.50	15.80
3.6125	40	40.00	39.00	25.10	16.80
3.825	40	50.00	48.00	21.00	15.60
4.0375	40	45.00	43.00	22.50	18.00
4.25	40	45.00	43.10	22.50	17

Table 4.5: Selected measured key figures of design 2 at 40dBm output power. (Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{out}$ [dBm]	η[%]	**PAE** [%]	**DC power**[W]	**Tr. Gain**[dB]
3.4	40	36.00	35.00	27.50	15.90
3.6125	40	36.00	35.00	27.50	15.90
3.825	40	43.00	42.00	23.50	15.10
4.0375	40	36.00	35.00	27.50	17.20
4.25	40	46.00	45.00	22.80	17.20

Table 4.6: Selected measured key figures of design 3 at 40dBm output power. (Tr = transducer)

Based on the previous presented tables, it is clear that design 2 is the one that fulfills most of the requirements, both simulated and measured.

Chapter 5

Extended Stability Analysis

This chapter presents a detailed analysis of the stability of the three power amplifiers operating under large-signal conditions. The analysis utilizes the harmonic balance method together with a small-signal current/voltage source connected at different nodes in the circuit, which are used to calculate the admittance/impedance at that node. By plotting the conductance/resistance and susceptance/reactance it is possible to analyze the stability in the circuit. If the conductance/resistance is negative and the suscepance/reactance is zero and ascending, the oscillation criteria are fulfilled. A more thoroughly description of the method was presented in Section 2.3.2. In the following, a description of practical implementation of the test is illustrated and explained.

It is worth mentioning that the analysis was performed after the PCBs were produced, tested and measured. At the end of the chapter an example showing that choosing an insensitive node might mask a possible instability.

5.1 ADS Test Bench Setup

To be able to perform a large signal stability analysis in ADS, some variables in the schematics have to be defined. Figure 5.1 shows the variable blocks ”Var5” and ”Var6” which initializes the frequency interval, of which the small-signal frequency is going to be swept, and the number of frequency points. These variables are then linked to the fields in the ”Small-signal” tab in the ”Harmonic Balance” block. In addition, the ”Small-signal” and ”Use all small-signal frequencies” have to be checked. The large-signal frequency was set equal to the center frequency, f_c=3.825GHz.

As shown in Figure 5.2, a small-signal current source must be connected to the circuit through a current probe and a node name must be specified at the interconnection in order to retrieve the node voltage. The source is then defined to generate a small current at the upper side band. As stated in Section 2.3.2, it is important that the current is small enough so it does not alter the steady-state periodic regime. However, a too small current may give rise to inaccurate simulations due to lack of sensitivity. (Note: It is also possible to define the current at the center frequency or of the lower side band as well. The only difference

will be how the mix()-function is specified in the equations. The mix()-function will be described in the next paragraph. [4]

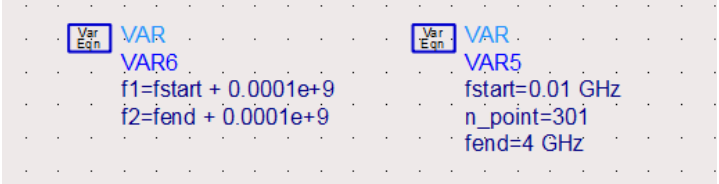


Figure 5.1: Large signal stability analysis variable setup in ADS.

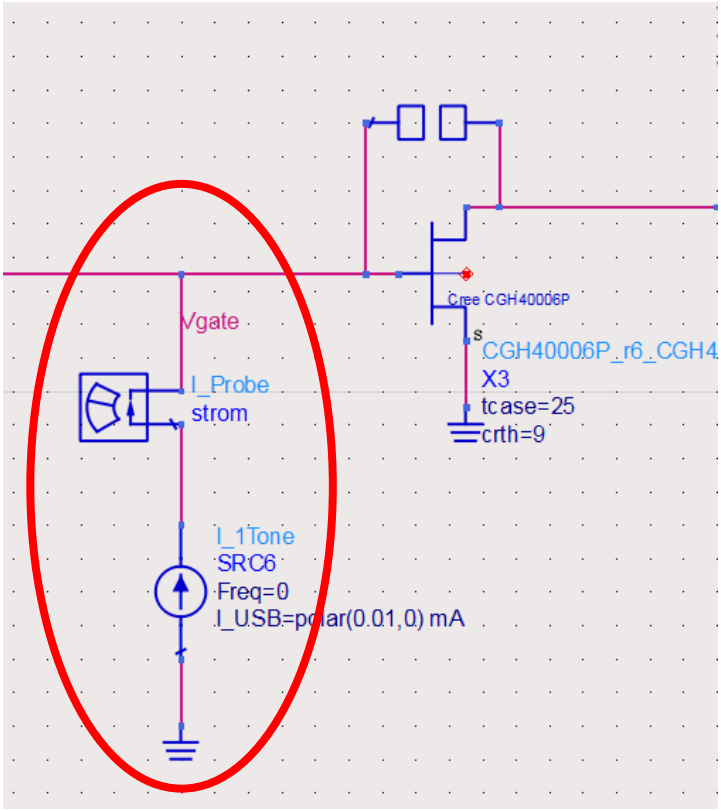


Figure 5.2: Small-signal current source connected at source through a current probe.

Next will be to define the equations which calculates the conductance and susceptance. In ADS, these are defined as:

$$Conductance = real(mix(SM.strom.i, \{0,1\})/mix(SM.Vgate, \{0,1\})) \quad (5.1a)$$

$$Susceptance = imag(mix(SM.strom.i, \{0,1\})/mix(SM.Vgate, \{0,1\})) \quad (5.1b)$$

As seen from the two equations, the mix()-function is used together with a vector ”{0,1}”. This function returns a spectrum component based on the vector that specifies the mixing indices. In this case, the small signal frequency. Figure 5.3 shows how equation 5.1a and 5.1b are used in ADS together with a variable called ”frequency” which is set equal to ”ssfreq”. This makes it easier to retrieve the small-signal sweeping frequency when the conductance and susceptance are plotted.

Figure 5.3: Equations setup for calculating the conductance and susceptance Variable in ADS.

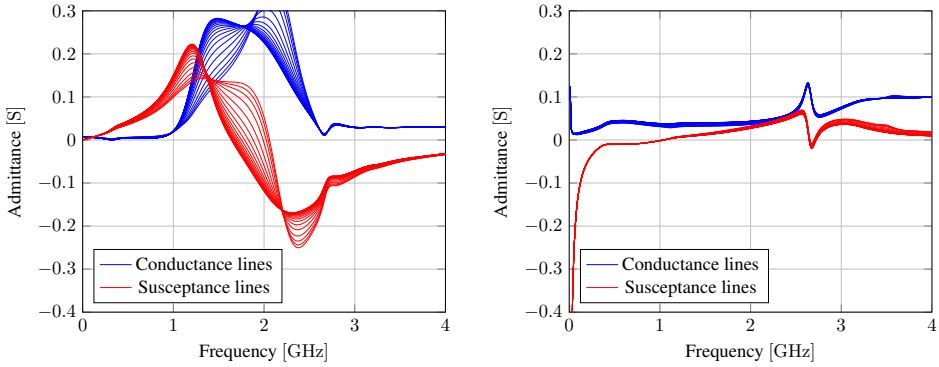
Due to the fact that the impedance/admittance often will vary with respect to the input power, a ”Parameter Sweep” block can be added. By specifying the input power as the sweep variable and the simulation instance as ”HB1”, the test bench will now simulate the circuit and calculate the impedance/admittance as a function of the small-signal frequency and input power.

As the test-bench was based on one of the large-signal benches provided by ADS, the small-signal source at the load had to be deactivated to not disturb the analysis.

5.2 Large Signal Stability Analysis - Results

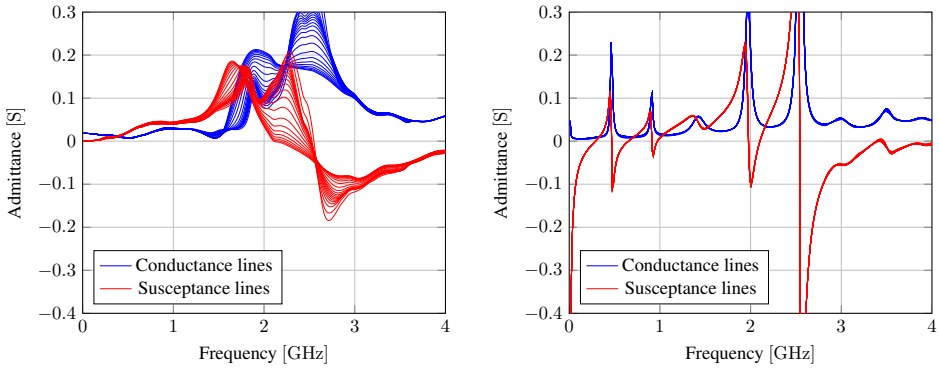
This section will present the results of the large signal stability analysis performed on the three designs. The small-signal current source was swept from DC to 4GHz while increasing the large signal input power 1dB at the time from 0dBm to 20dBm. The stability analysis was performed two times per design. For the single-stage design the nodes which were test were the gate and the drain, while the two other designs were analyzed at the drain of the first stage and at the gate of the second stage. As this is a time consuming task, the analysis was only performed at the large signal frequency of 3.825GHz. A more thorough analysis would include several large signal frequencies.

The admittance analysis of Figures 5.4, 5.5 and 5.6 reveals that all three designs does not fulfill the oscillations criteria. However, this does not mean that they are stable. Note that in Figure 5.6a, around 800MHz, the conductance is barely below 0. As this test does not tell wether or not this frequency interval is critical with regards to stability, more advanced stability analysis methods (e.g. Nyquist stability analysis) can be performed for further investigation. In addition, practical measurements will also reveal instabilities, and Figure 5.7 shows the frequency spectrum from DC up to 4GHz of the realized circuit. These spurious frequencies are hidden unless the reference level at the spectrum analyzer is set to -20dBm, and poses no danger to the performance of the circuit. Nevertheless, potentially instabilities must be eliminated in future work.



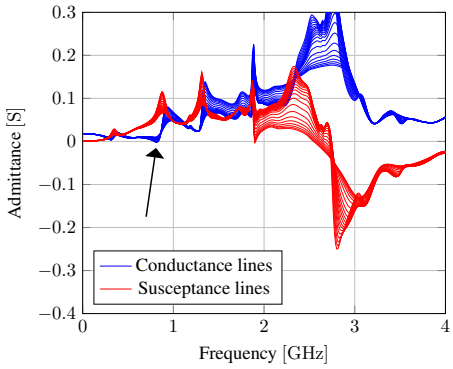
(a) Admittance diagram at gate **(b)** Admittance diagram at drain

Figure 5.4: Simulated conductance and susceptance variations at drain with input power ranging from 0dBm to 20dBm with 1dB step - Design 1

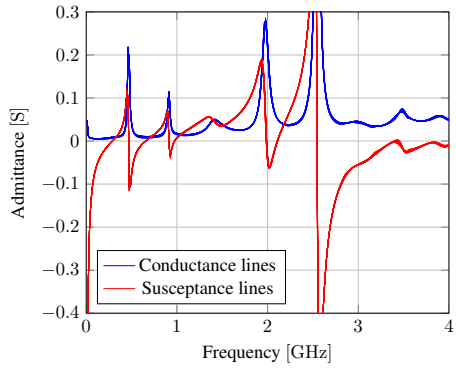


(a) Admittance diagram at gate **(b)** Admittance diagram at drain

Figure 5.5: Simulated conductance and susceptance variations at drain with input power ranging from 0dBm to 20dBm with 1dB step - Design 2



(a) Admittance diagram at gate. Potential instability at 800MHz.



(b) Admittance diagram at drain

Figure 5.6: Simulated conductance and susceptance variations at drain with input power ranging from 0dBm to 20dBm with 1dB step - Design 3

A further analysis of the spectrum in Figure 5.7 shows that the leftmost frequency component (∼750MHz) coincides with the results obtained from the stability simulations of design 3. However, a larger frequency component appears at 1.51GHz. One possible explanation of why this component appears in the spectrum-plot and not in the stability simulations in Figure 5.6a, might be due to masking of possible instabilities and would have been visible if another node had been chosen.

A second theory is that the frequency component at 750MHz fulfills the star up oscillation criteria but changes frequency when the amplitude rises. This phenomenon have been further investigated in [5] by Kurokawa.

The rightmost arrow points at a frequency component which probably results from the mixing of the two previously discussed frequency components.

5.3 Provoked instability - An example

As previously mentioned, choosing a wrong node might mask possible instabilities. This section will illustrate the outcome of choosing an insensitive node when performing a large signal stability analysis. To provoke a instability, one of the resistors at the gate bias at the second stage was shorted. In addition, the resistor in the stability circuit at the corresponding side was reduced to 0.01Ω.

The small-signal current source was first attached to the drain-side of the first stage and the resulting admittance can be seen in Figure 5.8a. As seen from the plot, the conductance is well above zero siemens all the way from DC to 4GHz.

The second analysis was performed at the drain side of the second stage at the same branch of which the resistors were shorted and reduced. Unlike Figure 5.8a, Figure 5.8b shows clearly that the start-up conditions for oscillations is met at around 450MHz. The conductance is well below zero siemens while the susceptane is zero with a positive slope.

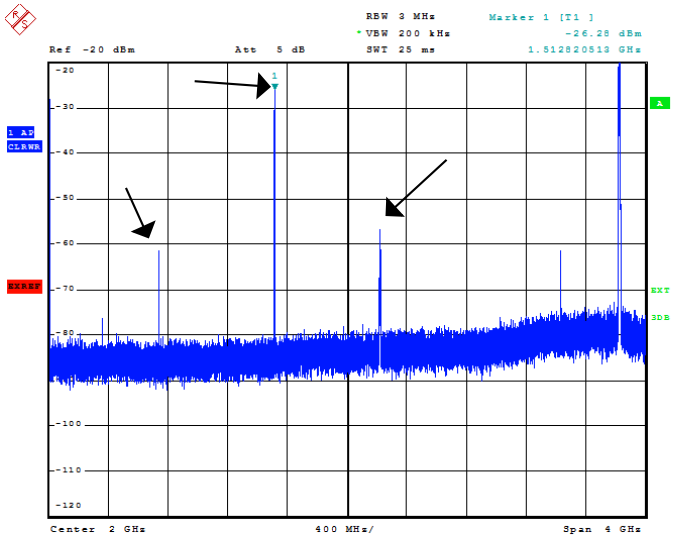
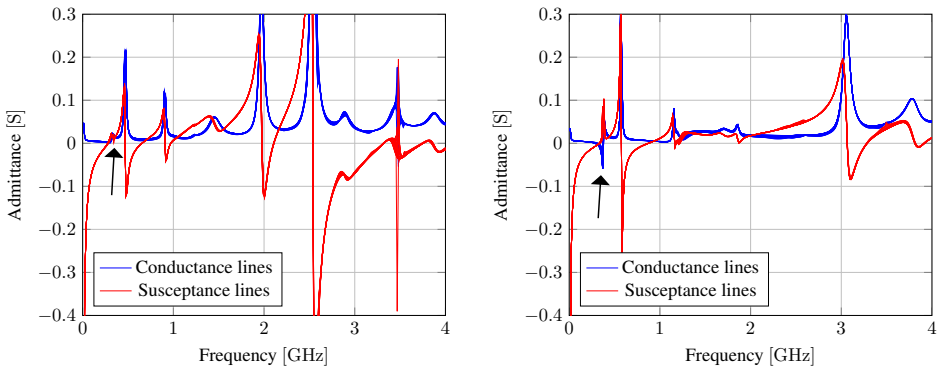


Figure 5.7: Measured frequency spectrum from DC to 4GHz. The amplified signal is shown at 3.825GHz together with low level spurious frequencies.

This example illustrates the importance of performing the admittance-impedance analysis at different nodes. What is masked in one node, might be clearly seen at another.



(a) Admittance diagram at drain

(b) Admittance diagram at drain

Figure 5.8: Provoked instabilities in Design 3. (a) Shows the admittance at drain-side of the first stage, while (b) shows the admittance on the drain-side of the second stage. The start-up conditions for oscillation is met around 450MHz and can be seen in (b).

Chapter 6

Discussion & Analysis

Most of the comparison between the simulated and the practical results have been presented in the previous chapter and will not be repeated here. Instead, this chapter will focus on practical issues related to the assembling of the three designs, followed by a section which will address the problems it is possible to encounter if one of the transistors at the second stage of design 2 and 3 stops working.

In terms of the gallium nitride technology, an overview of the future prospects will be presented. Last, suggestions for future work are presented.

6.1 Practical issues

As previously mentioned, the single-stage design was made to fit the standard 85mmx85mm cooling plate used at the microwave laboratory at NTNU. However, design 2 & 3 had no constraints regarding the physical size, and with a length and width of 300mm times 100mm, respectively, the need of a custom build cooling plate was necessary to be able to mount the circuits.

The plate was made of aluminum and the screw holes, for mounting the circuits, was drilled out with the help of the mechanical workshop at the electronics department.

Compared to the Cree-transistor used in design 1, which has a screw down flange, the transistors used in dual-stage design had to be, soldered onto the cooling plate or mounted using clamps. The preferred method was to use clamps as this technique potentially inflicts less damage when reusing the transistors. In addition, this method is easier and less time consuming than the other. The clamps was made of acrylic glass and Figure 6.1 shows how it was used to attach the transistors to the substrate and cooling plate.

Due to a height difference of 0.1mm between the substrate and the transistors used in the dual-stage designs, the transistors where at first not grounded properly, which resulted in zero current through the transistors. The solution was to add a thin copper film between the cooling plate and the source of the transistors.

No practical issues were experienced with design 1.

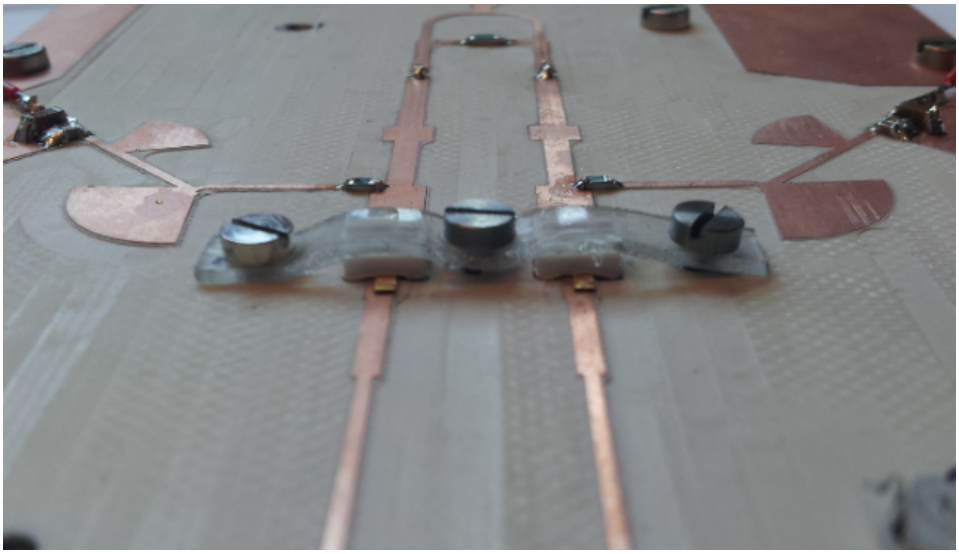


Figure 6.1: Clamps made of acrylic glass for attaching the transistors to the substrate.

6.2 Unexpected errors in second stage

The two dual-stage designs have been made with a balanced second stage, to have the ability to output a signal even if one transistor should fail. As previously mentioned, this was due to the requirement of having 10W or more output power. But what happens if an unexpected error such as a shortening of one of the transistors or the internal bonding wires break? In the following, these questions are tried to be answered.

6.2.1 Shorted transistor at second stage

The second design has one major drawback as the last stage shares a common drain feed. If an unexpected event occurs which results in a shorted transistor, the common power supply will also be shorted. Hence, the entire second stage will be put out of action due to a single fault. The second stage in design 3 however, does not share a common DC-supply and a shorted transistor will only influence itself disregarding the reduction of output power and efficiency. Based on that, a plot showing the simulated output power for the third design, with one transistor shorted at the second stage, is shown in Figure 6.2. It is seen that the amplifier is capable of delivering between 32dBm and 36dBm output power. However, the results might be a bit optimistic. Due to practical reasons, measurements have not been conducted.

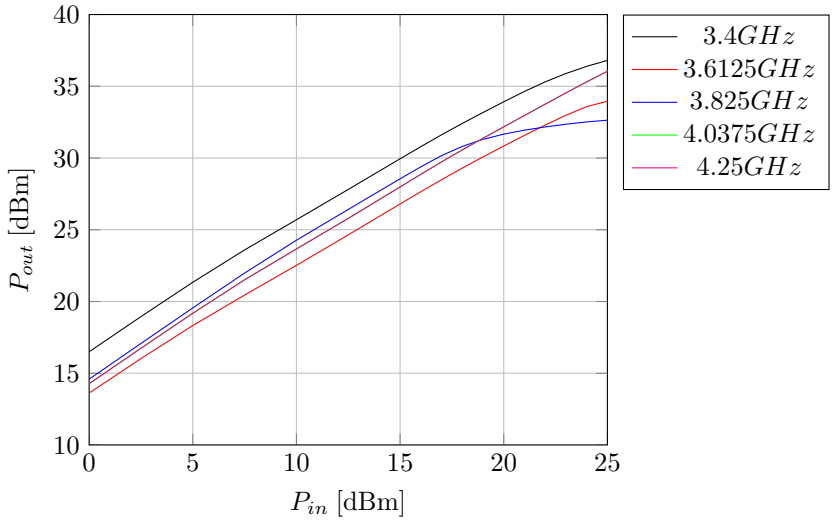
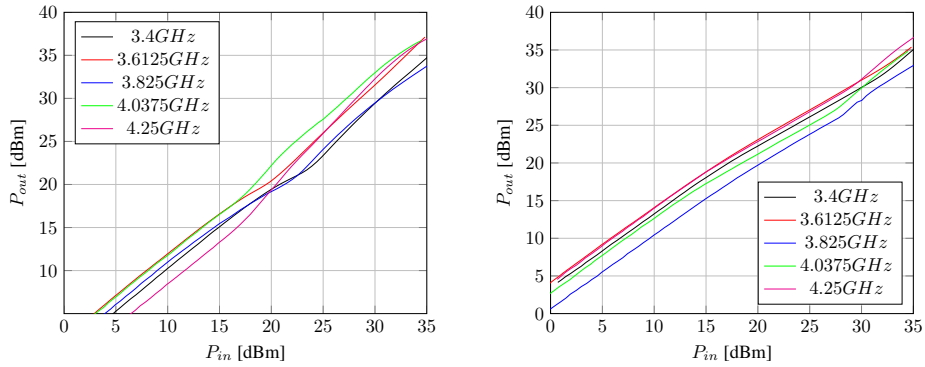


Figure 6.2: Simulated P_{in}/P_{out}-characteristics with one out of two transistor shorted at the second stage - Design 3 .

6.2.2 Open circuit

If, for one reason, the internal bonding wires breaks in one of the transistors at the second stage, the corresponding branch will more or less act as an open circuit disregarding the capacitive effects to ground, and the impedance which the other transistor experience will suddenly change. This will lead to a mismatch for the other transistor. Figure 6.3 shows the measured performance for design 2 and 3 when one of the second-stage transistors had been turned off. In general, both plots shows that the gain is almost gone at certain frequencies. In addition, Figure 6.3a shows that some of the curves have a small dip at a specific input power level. As the second design shares a common DC-feed one of the transistor had to be biased below the threshold voltage in order to emulate an open branch. It might be that it was not biased low enough and when the input power reached a certain level it was turned on. If that is the case, the performance is even lower than the one presented here.

Another method would be to remove the transistor from the circuit while performing the measurements, but as this is not the case when the amplifier is spaceborne it was decided to leave the transistor attached to the circuit. In addition, the capacitive effects, previously mentioned, would not have been counted for.



(a) Measured response - Design 2

(b) Measured response - Design 3

Figure 6.3: Measured P_{in}/P_{out}-characteristics when one of two transistors acts as an open circuit or is off due to an unexpected event

6.3 GaN transistors in space - Future prospects

Since the first commercially gallium nitride (GaN) power transistors appeared on the market in 2006/2007, several studies have been performed to investigate the possibility of using this technology in space applications [24][25]. Yet, the European Space Agency has still not released the derating standard for the GaN technology. However, the process is ongoing and in the meanwhile the derating standard for the gallium arsenide (GaAs) technology is used. One drawback of using the standard of another technology is that it restricts and limits the full potential of the GaN transistor, which is considered to have much better overall performance than GaAs-transistors. (It is unknown how far NASA has come in the process of publishing their derating standard).

One of the most interesting benefits of the GaN technology is the ability to handle high junction temperatures. As the normative junction temperature for silicon (Si) and GaAs systems is limited to 110°C by ESA, the future targeted temperature is 200°C for the GaN technology [26]. Due to this benefit, it is expected that thermal control subsystems which handles the dissipated heat from the amplifiers can be much reduced [27]. In addition, the GaN technology is much more radiation resistant than GaAs, this means that future shielding requirements can be simplified. [28]

Compared to other technologies such as traveling wave tube amplifiers (TWTAs), GaN transistors does not possess the impressive power added efficiency level that TWTAs have under multi-carrier and high power (250W) operations. However, studies have shown that for low power (20W-40W) C-band operations solid state power amplifiers (SSPAs) are able to compete side by side with TWTAs[29, p. 154] [26]. It should also be mentioned that a 100W X-band GaN SSPA has successfully been made as a replacement for a TWTA and that the first GaN-based PA, sent into space with the Proba V-satellite, is still working. [30] [24]

A specific application for SSPAs is when phased array or reflector-based antennas are used as transmitting antennas in the L-, S- or C-band. As each antenna element often has

its own power amplifier, the SSPAs are better suited due to the small size and the relatively low cost compared to TWTAs. [29, p. 170]

6.4 Suggestions for future work

The purpose of this thesis was to design and investigate three power amplifiers based on the GaN HEMT technology for Kongsberg Norspace. The three designs serves as possible prototypes for the last power stage for their C-band TT&C transmitters. Still, there is much work to be done and in this section suggestions for further improvements, analysis and other technologies are presented.

Simulation models

The simulation model belonging to the 6W transistors, which was used in the dual-stage designs, where only based on external measurements. This means that the internal current and voltage are not known exactly and there are still opportunities for further efficiency enhancement if these are known. The internal model got released at the time of writing, and would have been used if it was available sooner. It is recommended to use the internal model as the basis for simulations in further work.

PA redesign with hermetically sealed packaging

When future prototypes have reached a satisfying performance, the next natural iteration would be to redesign the working prototype with components with hermetically sealed packaging. Due to the hostile environment in Space, special packaging technology which protects the unit from moisture and radiation is required. [3]

Thermal analysis of transistor

Due to the extreme variations in temperature in Space, the transistors which are used in the final power amplifier needs to undergo thorough thermal analysis. This is to ensure that the amplifier are able to operate under harsh conditions and to check for irregularities which are triggered by temperature variations, in addition to investigate how the heat flow and heat dissipation acts in the semiconductor.

Other integration methods

The size of the two dual-stage designs are quit large and therefor inconvenient to use in space applications. One of several opportunities is to make a monolithic microwave integrated circuit (MMIC) which would only occupy a fraction of the area compared to the dual-stage designs. However, this would require access to a MMIC process e.g. from Cree Inc. or Qorvo.

Another possibility would be to use discrete capacitors in combination with microstrip transmission lines as reported in [23].

Chapter 7

Conclusion

This report presented the design of three class-AB 10W power amplifier stages for use in future C-band TT&C transmitters. The amplifiers were based on the GaN-technology and each design have been modeled and simulated using ADS, before they were prototyped and measured at the microwave laboratory at NTNU. The first design was a single-stage amplifier which utilized a 10W transistor from Cree, while the second and the third design were dual-stage amplifiers consisting of a preamplifier and a balanced second stage. The dual-stage amplifiers utilized three 6W transistors, also from Cree. The dual-stage amplifiers were based on the same topology, but had different output matches. The project and specifications were been given by Kongsberg Norspace AS.

All amplifiers were made with matching networks which were designed to match the optimal impedances found by using source and load pull tuners in ADS. Since the impedances of a passive network moves in the opposite direction in the smith chart, compared to the optimal impedances, a looping method was utilized to match the transistors. The transistors were optimized with respect to gain and output power at the fundamental frequencies and harmonic tuning was performed to increase the efficiency. This was achieved with varying degree of success.

The amplifiers were designed according to the requirements and showed good simulated performance in specified frequency range from 3.4GHz to 4.25GHz. The achieved small-signal gain for the single-stage amplifier varied between 11.3dB-11.7dB which is 2.3-2.7dB below the requirements. However, the two dual-stage amplifiers achieved a small-signal gain above 20dB. In general, the measured gain followed the simulated characteristics, but deviated between 1-2dB at the lower part of the frequency band for the dual-stages designs and 3dB for the single stage design.

The simulated input reflection coefficient, S_{11}, showed that singel-stage amplifier did not fulfill the requirements of being less than -10dB. This was solved in the dual-stage design by introducing a T-attenuator at the input. Measurements reviled that the performance was better than the simulated results for the two designs, while the single-stage amplifier experienced a frequency shift in S_{11}.

Simulations and measurements showed that all three amplifiers were able to deliver

40dBm output power, except the single-stage design which only reached 39dBm at 4.0375GHz. The measured power added efficiency for each design varied between 27%-44%, 39-43% and 35-42%, respectively. This implied that none of the designs managed to fulfill the requirement of having a total power consumption less than 25W over the specified frequency range. The simulated results however, showed that design 1 and 2 would fulfill this requirement.

After each prototype were produced and tested, a large-signal stability analysis was included to investigate possible instabilities. This was performed with the harmonic balance simulation technique in ADS. The analysis reviled no fulfillment of the oscillation start-up criteria, but possible instabilities in design 3 were discovered. Measurements confirmed that spurious frequencies existed at lower frequencies, but had no measurable impact on the performance.

To summarize, this thesis have reported the design and realization of three power amplifiers for Kongsberg Norspace' future TT&C-transmitters. Still, none of the amplifiers fulfilled all requirements and several iterations are needed before an integration with the transmitter can be made.

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Appendix A

Measurement equipment

This appendix holds the information of the equipment used when performing the measurements.

A.1 Small signal characterization

Equipment	Producer	Model
VNA	Agilent Technologies	E836B
Calibration kit	HP Agilent	85052D
Cables	Huber+Suhner	Sucoflex 104P
Coupler	ATM Inc.	2-18GHz
Load	ATM Inc.	50Ω DC-12GHz

Table A.1: List of used equipment in the small signal measurements

A.2 Large signal characterization

Equipment	Producer	Model
Spectrum analyzer	Rhode & Schwarz	FSQ40
Signal generator	Rhode & Schwarz	SMU 200A
Cables	Huber+Suhner	Sucoflex 104P
Coupler	ATM Inc.	C124H-10
Circulator	MCL Inc.	CS-144-35
Load	ATM Inc.	50Ω DC-12GHz

Table A.2: List of used equipment in the large signal measurements

Appendix B

1dB compression point - Key figures

Freq. [GHz]	$\mathbf{P}_{1dB,out}$ [dBm]	η [%]	**PAE** [%]	**DC power** [W]	**Tr. Gain** [dB]
3.4	40.99	59.38	55.32	20.46	8.20
3.6125	40.50	60.20	55.56	18.74	8.70
3.825	40.50	56.24	52.63	19.72	8.20
4.0375	40.49	53.90	49.82	20.56	8.24
4.25	40.60	55.10	49.60	21.51	8.32

Table B.1: The performance of the simulated amplifier at 1dB compression point. (Freq = frequency, Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{1dB,out}$ [dBm]	η [%]	**PAE** [%]	**DC power** [W]	**Tr. Gain** [dB]
3.4	40.48	44.10	43.70	23.65	18.53
3.6125	40.60	44.55	44.00	25.11	18.44
3.825	40.48	46.30	45.19	24.45	19.08
4.0375	40.48	45.91	45.56	25.90	18.74
4.25	40.10	41.05	40.60	25.67	18.35

Table B.2: The performance of the simulated amplifier at 1dB compression point. (Freq = frequency, Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{1dB,out}$ [dBm]	η [%]	**PAE** [%]	**DC power** [W]	**Tr. Gain** [dB]
3.4	39.98	37.03	35.07	27.89	17.58
3.6125	40.00	37.25	35.23	27.92	17.55
3.825	40.51	37.50	36.20	30.56	17.76
4.0375	40.48	38.16	37.52	29.24	17.48
4.25	41.00	42.05	40.53	30.44	16.55

Table B.3: The performance of the simulated amplifier at 1dB compression point. (Freq = frequency, Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{1dB,out}$ [dBm]	η[%]	**PAE** [%]	**DC power**[W]	**Tr. Gain**[dB]
3.4	41.40	62.50	48.50	19.60	6.75
3.6125	41.07	50.30	43.30	21.40	7.15
3.825	40.30	50.25	40.00	20.10	6.45
4.0375	39.00	37.80	29.50	24.00	8.2
4.25	39.90	37.20	27.20	26.00	6.1

Table B.4: The performance of the measured amplifier at 1dB compression point. (Freq = frequency, Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{1dB,out}$ [dBm]	η[%]	**PAE** [%]	**DC power**[W]	**Tr. Gain**[dB]
3.4	42.00	55.50	50.00	28.00	14.2
3.6125	41.75	46.00	43.00	29.50	16.0
3.825	42.10	61.00	56.00	26.00	13.5
4.0375	41.60	48.00	44.00	27.50	16.2
4.25	41.75	50.00	45.00	27.50	15.9

Table B.5: The performance of the measured amplifier at 1dB compression point. (Freq = frequency, Tr = transducer)

Freq. [GHz]	$\mathbf{P}_{1dB,out}$ [dBm]	η[%]	**PAE** [%]	**DC power**[W]	**Tr. Gain**[dB]
3.4	42.00	44.00	42.00	36.00	14.50
3.6125	42.00	44.50	42.00	34.00	14.50
3.825	41.90	51.00	49.50	30.00	14.00
4.0375	41.75	40.00	38.50	33.00	15.50
4.25	42.50	57.00	55.00	33.00	15.00

Table B.6: The performance of the measured amplifier at 1dB compression point. (Freq = frequency, Tr = transducer)

Appendix C

Photo of amplifiers

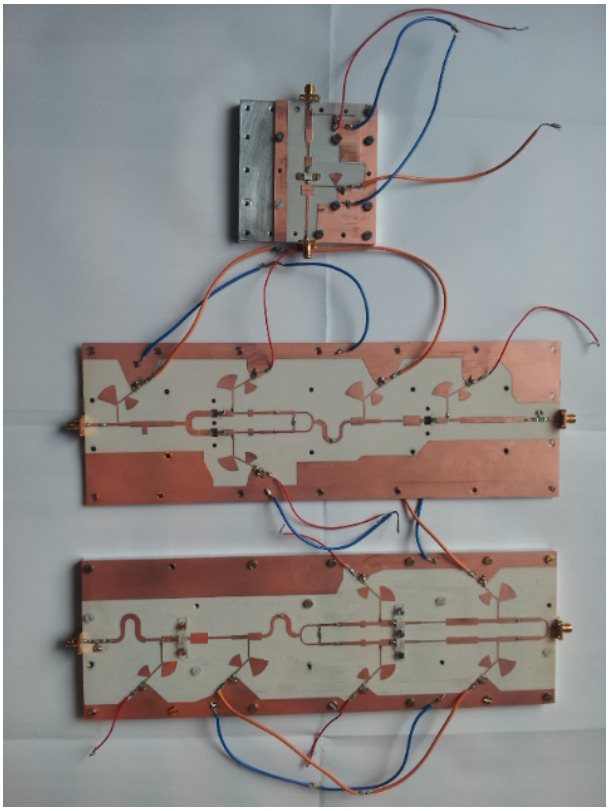

Figure C.1: Photo of amplifiers. Design 1 (left), design 2 (middle) and design 3 (right).

Appendix D

Schematics

Design 1

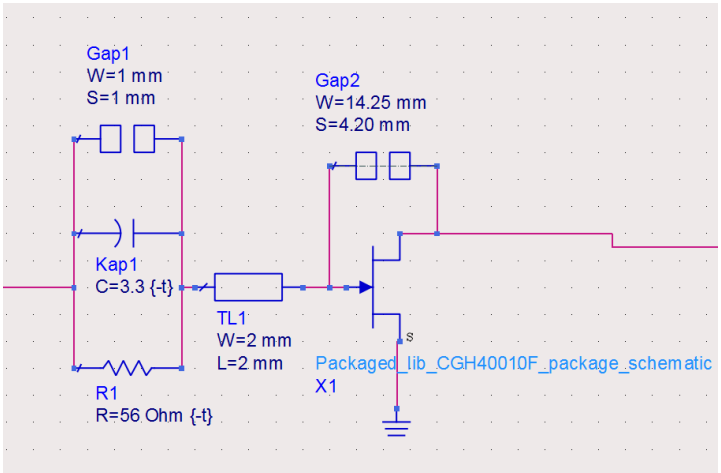

Figure D.1: Design 1: Stability circuit and 10W CGH40010F transistor model from Cree

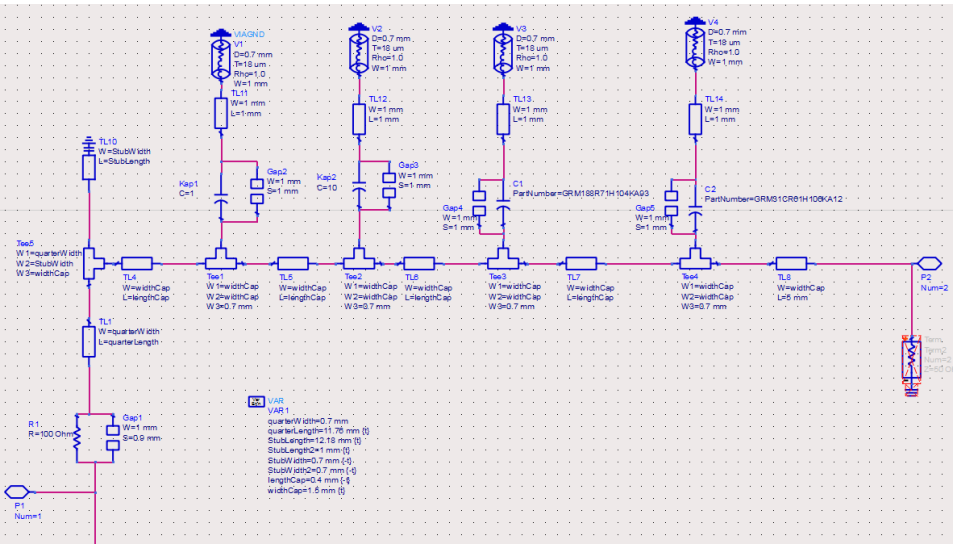

Figure D.2: Design 1: Bias network at gate

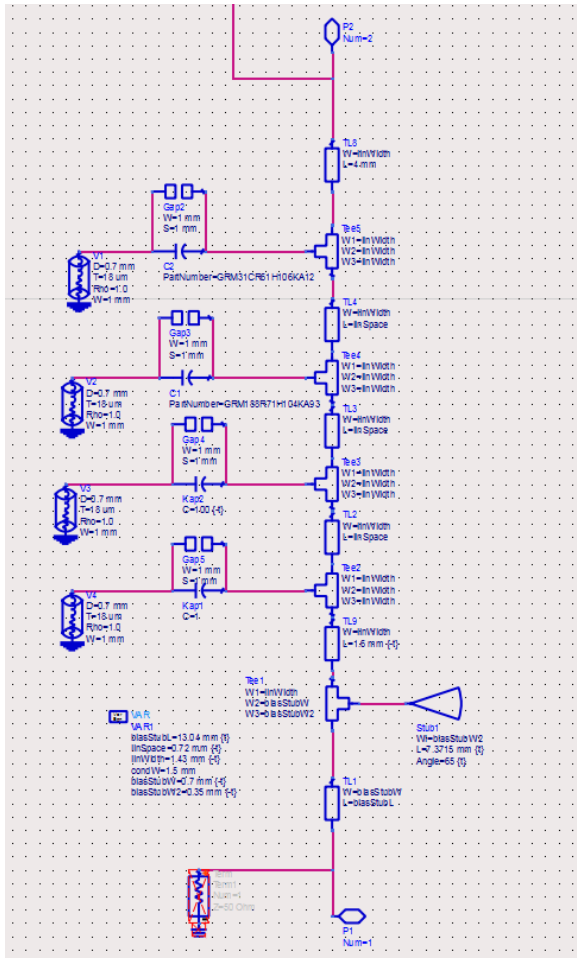

Figure D.3: Design 1: Bias network at drain

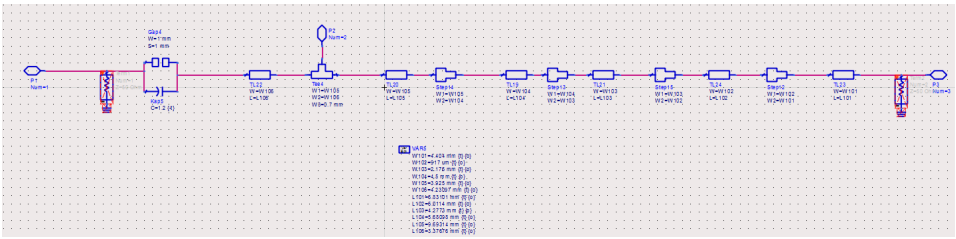

Figure D.4: Design 1: Input match witch DC-block

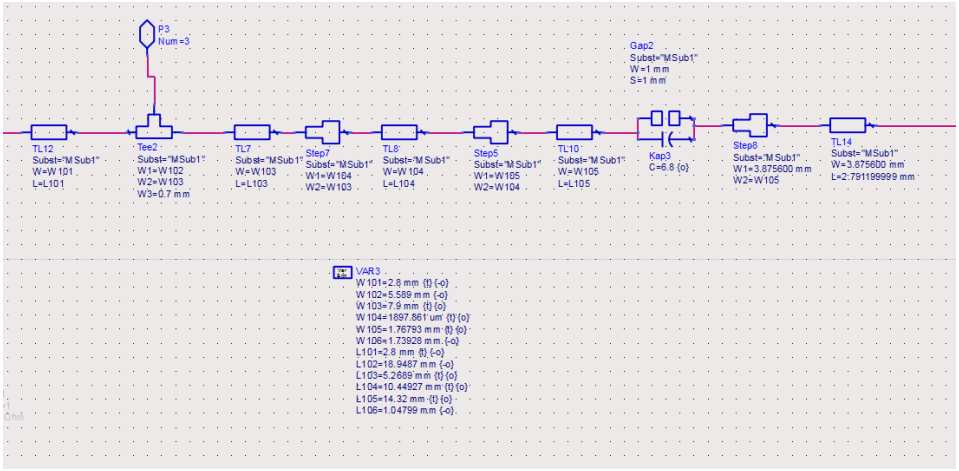

Figure D.5: Design 1: Output match witch DC-block

Design 2 & 3

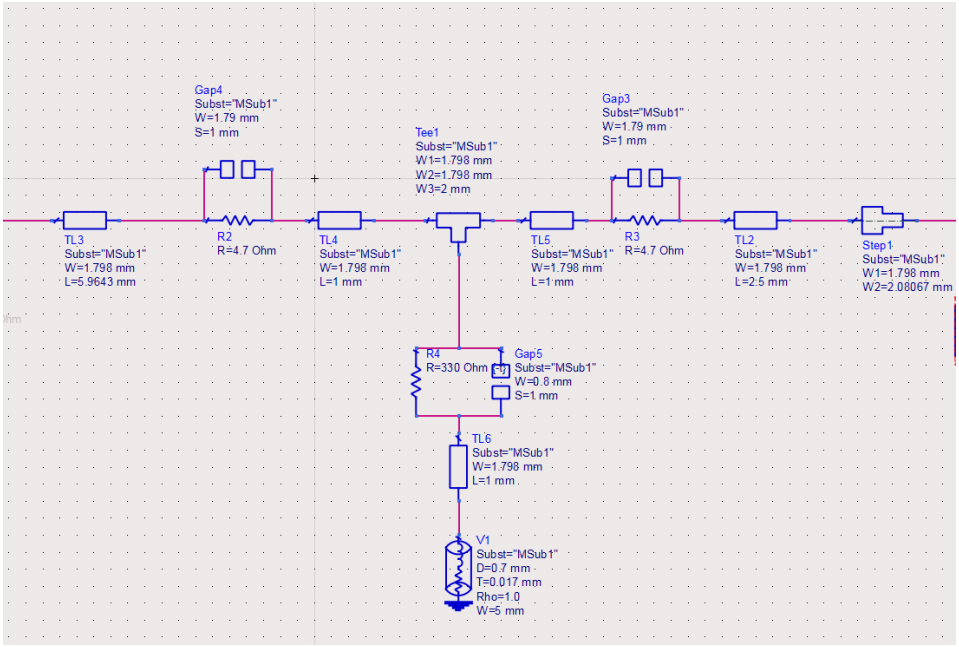

Figure D.6: Design 2 & 3: T-Attenuator with 1.5dB attenuation.

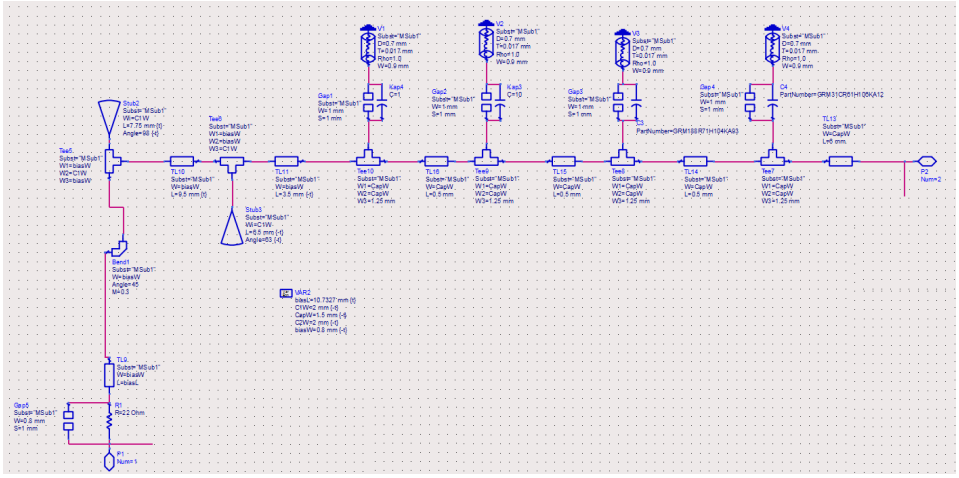

Figure D.7: Design 2 & 3: Bias network at gate.

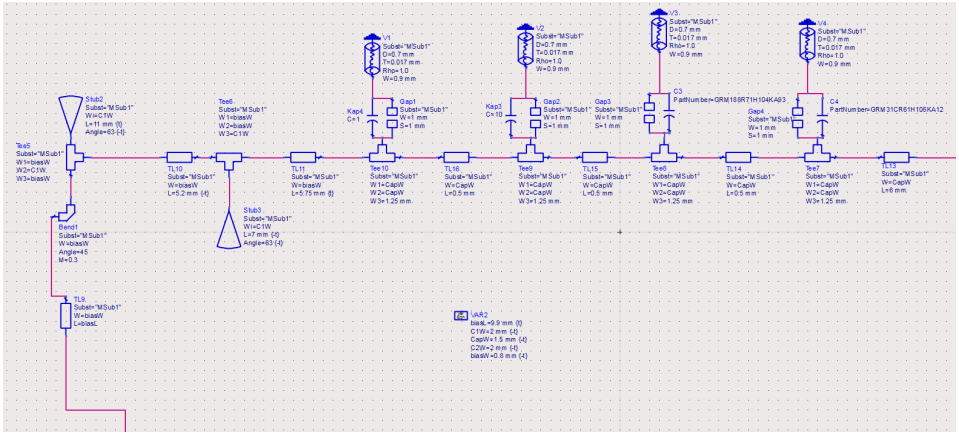

Figure D.8: Design 2 & 3: Bias network at drain.

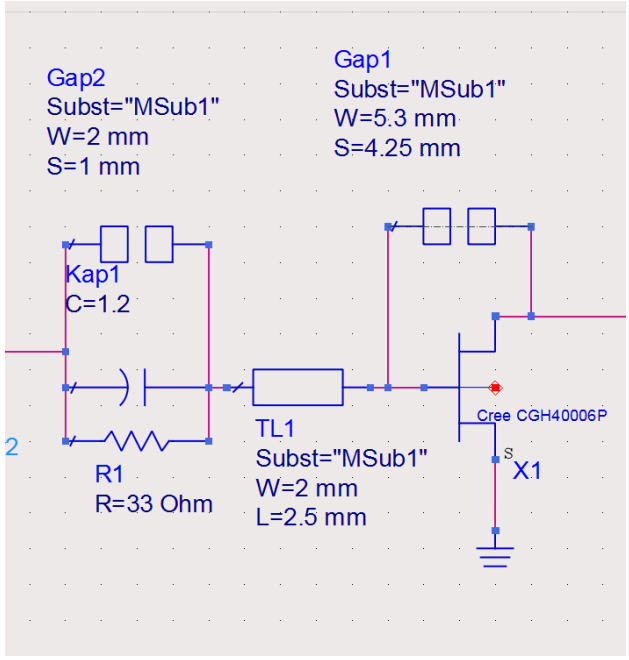

Figure D.9: Design 2 & 3: Stabilization circuit and 6W CGH40006P transistor model from Cree.

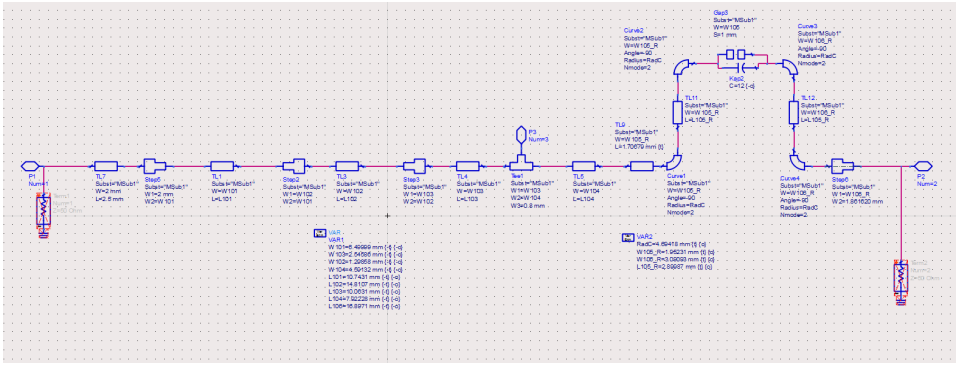

Figure D.10: Design 2 & 3: First stage output match with DC-block. Equal for both designs.

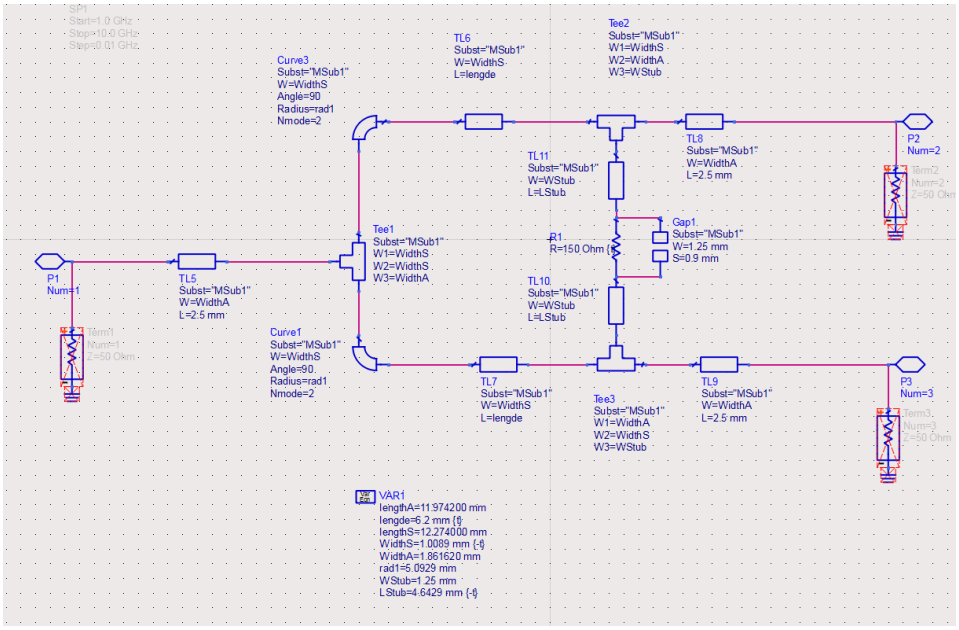

Figure D.11: Design 2 & 3: Customized wilkinson power divider.

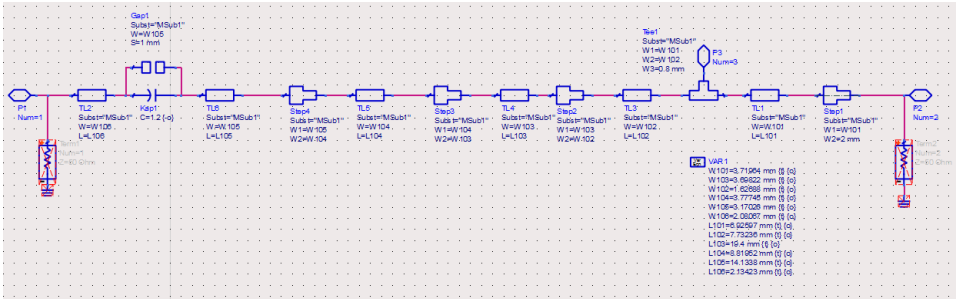

Figure D.12: Design 2: First stage input match with DC-block.

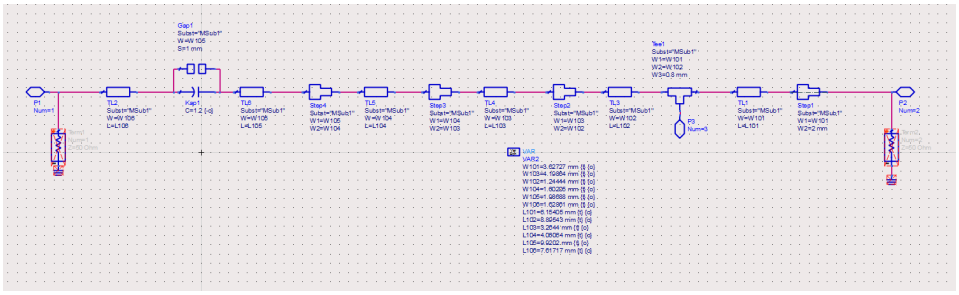

Figure D.13: Design 2: Second stage input match with DC-block.

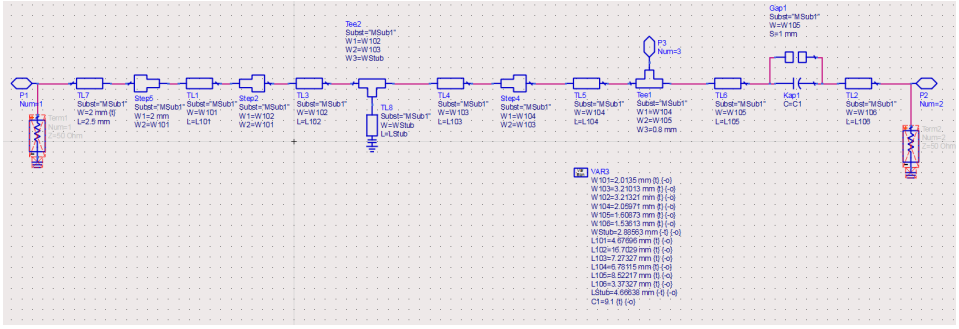

Figure D.14: Design 2: Second stage output match with DC-block.

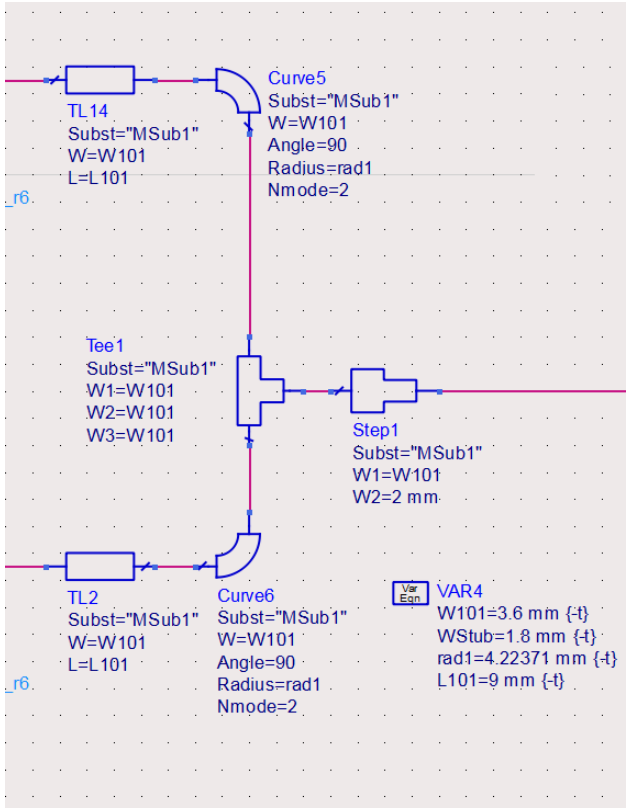

Figure D.15: Design 2: Power combiner at second stage.

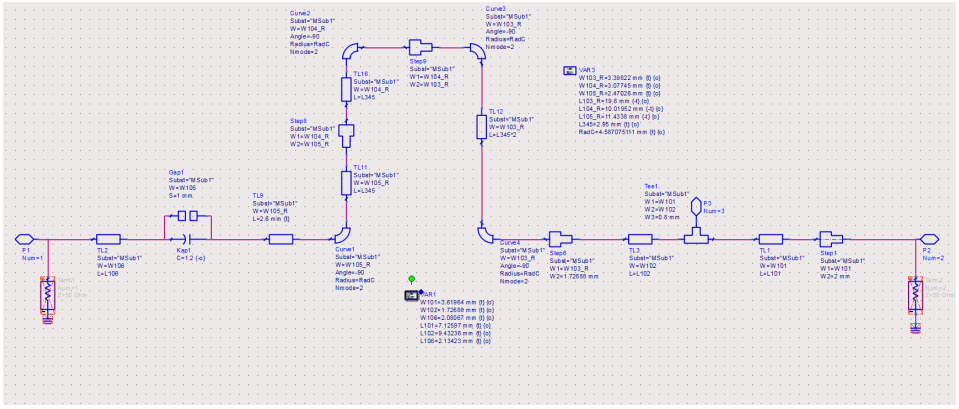

Figure D.16: Design 3: First stage input match with DC-block.

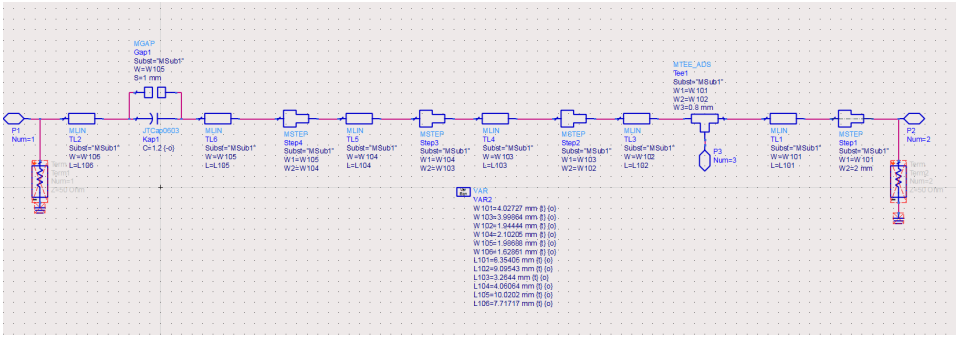

Figure D.17: Design 3: Second stage input match with DC-block.

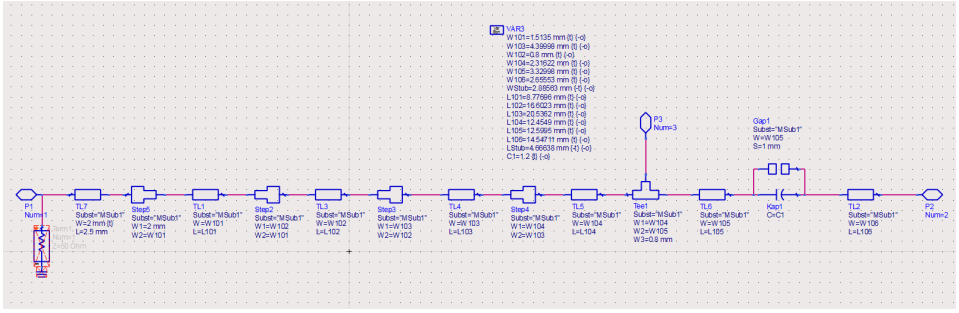

Figure D.18: Design 3: Second stage output match with DC-block.

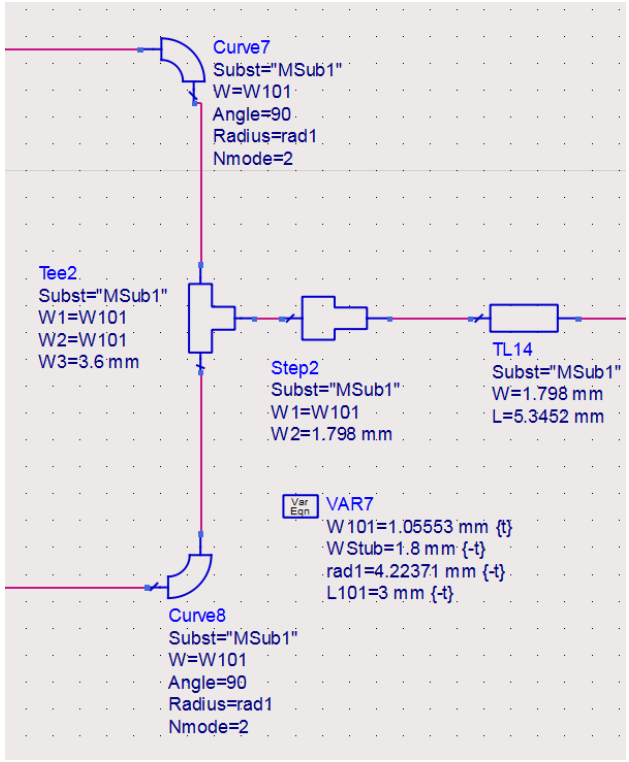

Figure D.19: Design 3: Power combiner at second stage.

Appendix E

PCB layout

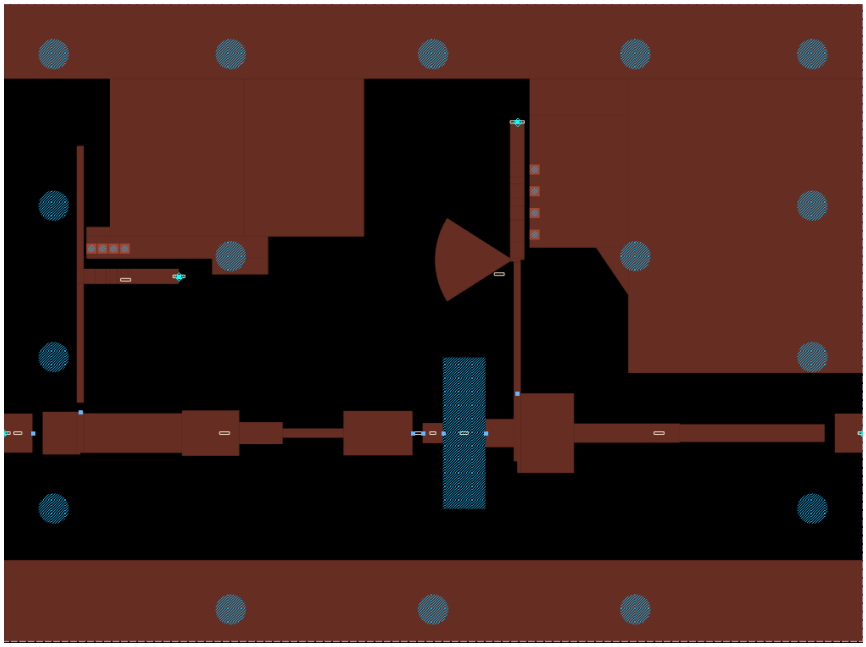

Figure E.1: Final design of single-stage power amplifier.

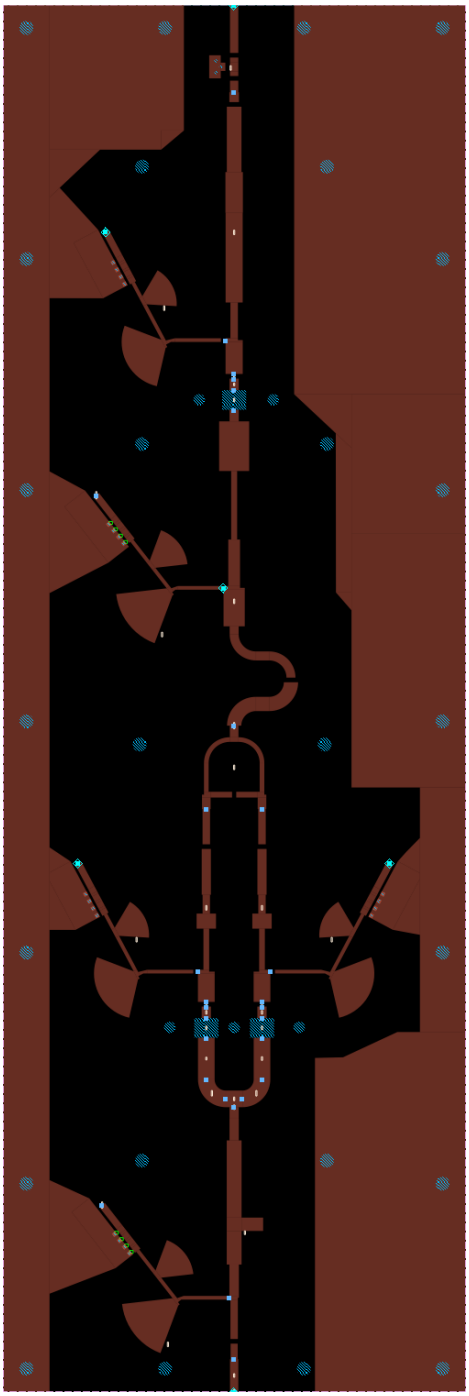

Figure E.2: Final design of dual-stage power amplifier. Joint output match at second stage.

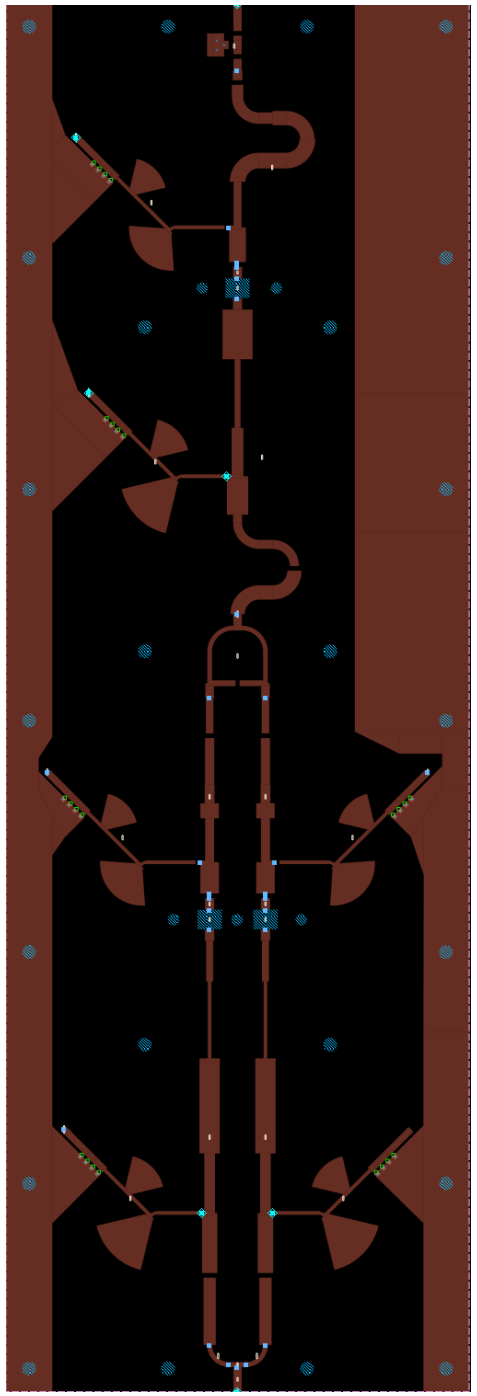

Figure E.3: Final design of dual-stage power amplifier. Single output matches at second stage.

Appendix F

Noise Figures

Design 1

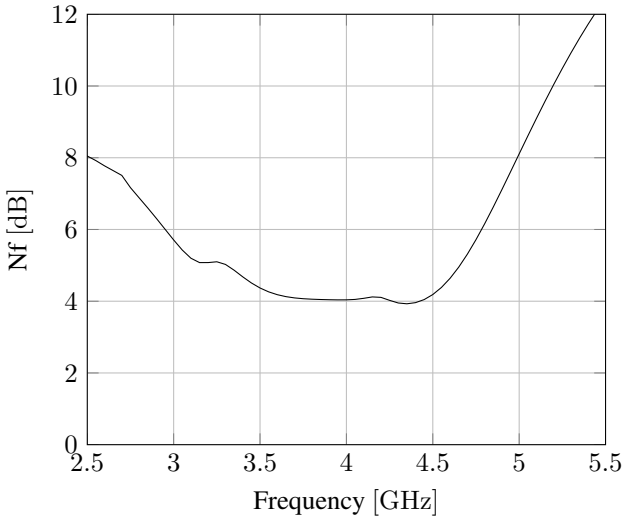

Figure F.1: Design 1: Noise figure

Design 2

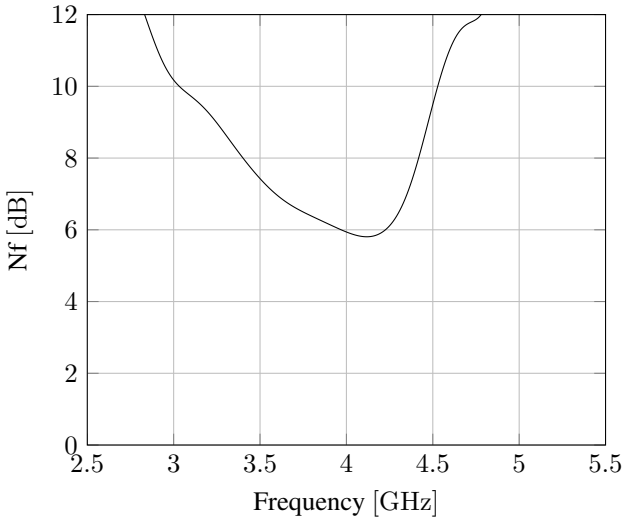

Figure F.2: Design 2: Noise figure

Design 3

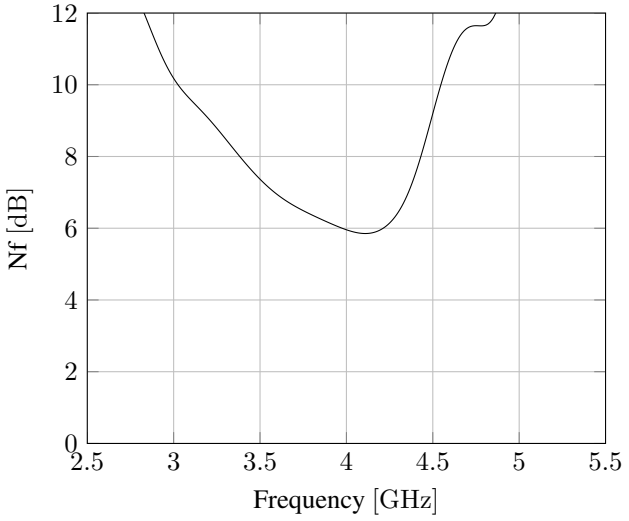

Figure F.3: Design 3: Noise figure