```
--------------------------------------------------------------------------------
Release 14.7 Trace  (lin64)
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/tools/ISE_r/14.7/ISE_DS/ISE/bin/lin64/unwrapped/trce -tsi ./GeneticAlg.tsi
-fastpaths -e 200 -u 10 ./GeneticAlg GeneticAlg.pcf -o ./GeneticAlg.twr

Design file:              GeneticAlg.ncd
Physical constraint file: GeneticAlg.pcf
Device,package,speed:     xc6vlx195t,ff784,C,-2 (PRODUCTION 1.17 2013-10-13)
Report level:             error report, limited to 200 items per constraint
                          unconstrained path report, limited to 10 items

Environment Variable      Effect
--------------------      ------
NONE                      No environment variables were set
--------------------------------------------------------------------------------

INFO:Timing:3386 - Intersecting Constraints found and resolved.  For more
   information, see the TSI report.  Please consult the Xilinx Command Line
   Tools User Guide for information on generating a TSI report.

INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612
INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on
   a 50 Ohm transmission line loading model.  For the details of this model,
   and for more information on accounting for different loading conditions,
   please see the device datasheet.

================================================================================
Timing constraint: TS_SystemClock = PERIOD TIMEGRP "tnm_SystemClock" 5 ns HIGH
For more information, see Period Analysis in the Timing Closure User Guide (UG
 470800 paths analyzed, 159941 endpoints analyzed, 428 failing endpoints
 428 timing errors detected. (428 setup errors, 0 hold errors, 0 component swi
 Minimum period is   5.534ns.
--------------------------------------------------------------------------------
Slack (setup path):     -0.534ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[3]_im_5 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][1
  Requirement:          5.000ns
  Data Path Delay:      5.628ns (Levels of Logic = 0)
  Clock Path Skew:      0.129ns (1.571 - 1.442)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[3]_im
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                            Logical Resource(s)
    ------------------------------------------------------  -------------------
    SLICE_X110Y116.BQ     Tcko                    0.322   i_GeneticAlg/Mut2CostWe
                                                          i_GeneticAlg/Mut2CostW
    SLICE_X63Y25.BX       net (fanout=11)       5.290   i_GeneticAlg/Mut2CostWei
    SLICE_X63Y25.CLK      Tdick                   0.016   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    ------------------------------------------------------  -------------------
    Total                                         5.628ns (0.338ns logic, 5.290ns
                                                          (6.0% logic, 94.0% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.522ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[8]_re_6 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][8
  Requirement:          5.000ns
  Data Path Delay:      5.642ns (Levels of Logic = 1)
  Clock Path Skew:      0.155ns (1.603 - 1.448)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[8]_re
    Location              Delay type         Delay(ns)  Physical Resource
                                                            Logical Resource(s)
    ------------------------------------------------------  -------------------
    SLICE_X105Y126.CQ     Tcko                    0.283   i_GeneticAlg/Mut2CostWe
                                                          i_GeneticAlg/Mut2CostW
    SLICE_X74Y34.C5       net (fanout=11)       5.323   i_GeneticAlg/Mut2CostWei
    SLICE_X74Y34.CLK      Tas                     0.036   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/Mut2CostW
                                                          i_GeneticAlg/i_SerialC
    ------------------------------------------------------  -------------------
    Total                                         5.642ns (0.319ns logic, 5.323ns
                                                          (5.7% logic, 94.3% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.489ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].i
  Requirement:          5.000ns
  Data Path Delay:      5.226ns (Levels of Logic = 1)
  Clock Path Skew:      -0.228ns (1.360 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X60Y104.D2     net (fanout=2307)      4.850   i_GeneticAlg/i_SerialCos
    SLICE_X60Y104.CLK    Tas                    0.019   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                       5.226ns (0.376ns logic, 4.850ns
                                                        (7.2% logic, 92.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.484ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[8]_re_1 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[1][8
  Requirement:          5.000ns
  Data Path Delay:      5.462ns (Levels of Logic = 0)
  Clock Path Skew:      0.013ns (1.459 - 1.446)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[8]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X105Y110.BQ    Tcko                   0.283   i_GeneticAlg/Mut2CostWe
                                                        i_GeneticAlg/Mut2CostW
    SLICE_X55Y160.BX     net (fanout=11)        5.163   i_GeneticAlg/Mut2CostWei
    SLICE_X55Y160.CLK    Tdick                  0.016   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                       5.462ns (0.299ns logic, 5.163ns
                                                        (5.5% logic, 94.5% rou

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Slack (setup path):     -0.483ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
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  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.146ns (Levels of Logic = 2)
  Clock Path Skew:      -0.302ns (1.371 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.C4     net (fanout=2304)     4.184   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.146ns (0.513ns logic, 4.633ns
                                                       (10.0% logic, 90.0% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.475ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_im_1 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][(
  Requirement:          5.000ns
  Data Path Delay:      5.469ns (Levels of Logic = 0)
  Clock Path Skew:      0.029ns (1.479 - 1.450)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X104Y117.BQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
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                                                          i_GeneticAlg/Mut2CostW
    SLICE_X63Y42.BX      net (fanout=11)       5.131   i_GeneticAlg/Mut2CostWei
    SLICE_X63Y42.CLK     Tdick                 0.016    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.469ns (0.338ns logic, 5.131ns
                                                          (6.2% logic, 93.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.474ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].i
  Requirement:          5.000ns
  Data Path Delay:      5.211ns (Levels of Logic = 1)
  Clock Path Skew:      -0.228ns (1.360 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X56Y108.B6     net (fanout=2307)     4.835   i_GeneticAlg/i_SerialCos
    SLICE_X56Y108.CLK    Tas                   0.019   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.211ns (0.376ns logic, 4.835ns
                                                       (7.2% logic, 92.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.469ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[1]_im_0 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[4][1
  Requirement:          5.000ns
  Data Path Delay:      5.327ns (Levels of Logic = 0)
  Clock Path Skew:      -0.107ns (1.282 - 1.389)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[1]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X116Y99.AQ     Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X27Y100.AX     net (fanout=11)       4.989   i_GeneticAlg/Mut2CostWei
    SLICE_X27Y100.CLK    Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.327ns (0.338ns logic, 4.989ns
                                                       (6.3% logic, 93.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.466ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[7]_re_3 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][7
  Requirement:          5.000ns
  Data Path Delay:      5.559ns (Levels of Logic = 0)
  Clock Path Skew:      0.128ns (1.572 - 1.444)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[7]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X108Y123.DQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X58Y30.DX      net (fanout=11)       5.221   i_GeneticAlg/Mut2CostWei
    SLICE_X58Y30.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.559ns (0.338ns logic, 5.221ns
                                                       (6.1% logic, 93.9% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.464ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].i
  Requirement:          5.000ns
  Data Path Delay:      5.173ns (Levels of Logic = 1)
  Clock Path Skew:      -0.256ns (1.332 - 1.588)
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```
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X50Y103.B3     net (fanout=2307)     4.797   i_GeneticAlg/i_SerialCos
    SLICE_X50Y103.CLK    Tas                   0.019   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.173ns (0.376ns logic, 4.797ns
                                                       (7.3% logic, 92.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.459ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[1]_im_9 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][
  Requirement:          5.000ns
  Data Path Delay:      5.409ns (Levels of Logic = 0)
  Clock Path Skew:      -0.015ns (1.418 - 1.433)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[1]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X109Y105.BQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X45Y58.BX      net (fanout=11)       5.110   i_GeneticAlg/Mut2CostWei
    SLICE_X45Y58.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.409ns (0.299ns logic, 5.110ns
                                                       (5.5% logic, 94.5% rou
```

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--------------------------------------------------------------------------------
Slack (setup path):     -0.456ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[1]_re_8 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[4][
  Requirement:          5.000ns
  Data Path Delay:      5.261ns (Levels of Logic = 0)
  Clock Path Skew:      -0.160ns (1.288 - 1.448)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[1]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X102Y105.AQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X24Y97.AX      net (fanout=11)       4.939   i_GeneticAlg/Mut2CostWei
    SLICE_X24Y97.CLK     Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.261ns (0.322ns logic, 4.939ns
                                                       (6.1% logic, 93.9% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.446ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.110ns (Levels of Logic = 2)
  Clock Path Skew:      -0.301ns (1.371 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    SLICE_X62Y111.C4     net (fanout=2304)     4.184   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.060    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                      5.110ns (0.506ns logic, 4.604ns
                                                       (9.9% logic, 90.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.445ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_im_0 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][(
  Requirement:          5.000ns
  Data Path Delay:      5.382ns (Levels of Logic = 0)
  Clock Path Skew:      -0.028ns (1.422 - 1.450)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X104Y117.AQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                          i_GeneticAlg/Mut2CostW
    SLICE_X43Y43.AX      net (fanout=11)       5.044   i_GeneticAlg/Mut2CostWei
    SLICE_X43Y43.CLK     Tdick                 0.016    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                      5.382ns (0.338ns logic, 5.044ns
                                                       (6.3% logic, 93.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.440ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.203ns (Levels of Logic = 1)
  Clock Path Skew:      -0.202ns (1.386 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X94Y113.B2     net (fanout=2307)     4.789   i_GeneticAlg/i_SerialCos
    SLICE_X94Y113.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.203ns (0.414ns logic, 4.789ns
                                                       (8.0% logic, 92.0% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.440ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[7]_re_2 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][
  Requirement:          5.000ns
  Data Path Delay:      5.533ns (Levels of Logic = 0)
  Clock Path Skew:      0.128ns (1.572 - 1.444)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[7]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X108Y123.CQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X58Y30.CX      net (fanout=11)       5.195   i_GeneticAlg/Mut2CostWei
    SLICE_X58Y30.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.533ns (0.338ns logic, 5.195ns
                                                       (6.1% logic, 93.9% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.440ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_re_8 (FF)
```

```
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[4][(
  Requirement:          5.000ns
  Data Path Delay:      5.264ns (Levels of Logic = 0)
  Clock Path Skew:      -0.141ns (1.327 - 1.468)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X92Y108.AQ     Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW(
    SLICE_X18Y87.AX      net (fanout=11)       4.942   i_GeneticAlg/Mut2CostWei
    SLICE_X18Y87.CLK     Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.264ns (0.322ns logic, 4.942ns
                                                       (6.1% logic, 93.9% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.431ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[8]_re_9 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[2][8
  Requirement:          5.000ns
  Data Path Delay:      5.347ns (Levels of Logic = 0)
  Clock Path Skew:      -0.049ns (1.389 - 1.438)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[8]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X109Y108.CQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW(
    SLICE_X92Y157.BX     net (fanout=11)       5.064   i_GeneticAlg/Mut2CostWei
    SLICE_X92Y157.CLK    Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    ----------------------------------------------------  ----------------------
    Total                                                 5.347ns (0.283ns logic, 5.064ns
                                                                  (5.3% logic, 94.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.431ns (requirement - (data path - clock path skew + u
  Source:                i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:           i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:           5.000ns
  Data Path Delay:       5.096ns (Levels of Logic = 2)
  Clock Path Skew:       -0.300ns (1.373 - 1.673)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.D5     net (fanout=2304)     4.137   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                              5.096ns (0.510ns logic, 4.586ns
                                                              (10.0% logic, 90.0% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.428ns (requirement - (data path - clock path skew + u
  Source:                i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:           i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:           5.000ns
  Data Path Delay:       5.093ns (Levels of Logic = 2)
  Clock Path Skew:       -0.300ns (1.373 - 1.673)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
```

```
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.D5     net (fanout=2304)     4.134   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.093ns (0.510ns logic, 4.583ns
                                                       (10.0% logic, 90.0% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.426ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.091ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.A5     net (fanout=2304)     4.129   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.091ns (0.513ns logic, 4.578ns
                                                       (10.1% logic, 89.9% ro
```

```
--------------------------------------------------------------------------------
Slack (setup path):     -0.425ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_re_0 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][(
  Requirement:          5.000ns
  Data Path Delay:      5.345ns (Levels of Logic = 0)
  Clock Path Skew:      -0.045ns (1.397 - 1.442)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X108Y112.AMUX  Tshcko                 0.394   i_GeneticAlg/Mut2CostWe
                                                        i_GeneticAlg/Mut2CostW(
    SLICE_X39Y45.AX      net (fanout=11)        4.935   i_GeneticAlg/Mut2CostWei
    SLICE_X39Y45.CLK     Tdick                  0.016   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                       5.345ns (0.410ns logic, 4.935ns
                                                        (7.7% logic, 92.3% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.424ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[3]_re_8 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[4][:
  Requirement:          5.000ns
  Data Path Delay:      5.242ns (Levels of Logic = 0)
  Clock Path Skew:      -0.147ns (1.297 - 1.444)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[3]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X108Y118.AMUX  Tshcko                 0.394   i_GeneticAlg/Mut2CostWe
                                                        i_GeneticAlg/Mut2CostW(
```

```
    SLICE_X39Y115.AX     net (fanout=11)       4.832   i_GeneticAlg/Mut2CostWei
    SLICE_X39Y115.CLK    Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.242ns (0.410ns logic, 4.832ns
                                                       (7.8% logic, 92.2% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.423ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.074ns (Levels of Logic = 2)
  Clock Path Skew:      -0.314ns (1.359 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y98.B1      net (fanout=2304)     4.115   i_GeneticAlg/i_SerialCos
    SLICE_X62Y98.CLK     Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.074ns (0.510ns logic, 4.564ns
                                                       (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.421ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.153ns (Levels of Logic = 1)
  Clock Path Skew:      -0.233ns (1.355 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X56Y104.D1     net (fanout=2307)      4.777   i_GeneticAlg/i_SerialCos
    SLICE_X56Y104.CLK    Tas                    0.019   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                       5.153ns (0.376ns logic, 4.777ns
                                                        (7.3% logic, 92.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.416ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.081ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                   0.283   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)         0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                   0.170   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X63Y123.A5     net (fanout=2304)      4.119   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                    0.060   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                       5.081ns (0.513ns logic, 4.568ns
                                                        (10.1% logic, 89.9% ro
```

```
--------------------------------------------------------------------------------
Slack (setup path):     -0.414ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Requirement:          5.000ns
  Data Path Delay:      5.439ns (Levels of Logic = 2)
  Clock Path Skew:      0.060ns (1.474 - 1.414)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X46Y89.CQ      Tcko                  0.322   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X47Y154.B5     net (fanout=9)        2.998   i_GeneticAlg/i_SerialCos
    SLICE_X47Y154.B      Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X46Y162.B6     net (fanout=1)        0.532   i_GeneticAlg/i_SerialCos
    SLICE_X46Y162.B      Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X1Y69.A2       net (fanout=1)        1.208   i_GeneticAlg/i_SerialCos
    DSP48_X1Y69.CLK      Tdspdck_A_AREG        0.257   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.439ns (0.701ns logic, 4.738ns
                                                       (12.9% logic, 87.1% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.409ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[7]_re_7 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][
  Requirement:          5.000ns
  Data Path Delay:      5.335ns (Levels of Logic = 0)
  Clock Path Skew:      -0.039ns (1.409 - 1.448)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[7]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X105Y127.DQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X41Y53.DX      net (fanout=11)       5.036   i_GeneticAlg/Mut2CostWei
    SLICE_X41Y53.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.335ns (0.299ns logic, 5.036ns
                                                       (5.6% logic, 94.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.407ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[5]_im_9 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[1][5
  Requirement:          5.000ns
  Data Path Delay:      5.259ns (Levels of Logic = 0)
  Clock Path Skew:      -0.113ns (1.279 - 1.392)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[5]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X116Y101.BQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X37Y141.BX     net (fanout=11)       4.921   i_GeneticAlg/Mut2CostWei
    SLICE_X37Y141.CLK    Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.259ns (0.338ns logic, 4.921ns
                                                       (6.4% logic, 93.6% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.404ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.067ns (Levels of Logic = 2)
  Clock Path Skew:      -0.302ns (1.371 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.D5     net (fanout=2304)     4.108   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.067ns (0.510ns logic, 4.557ns
                                                       (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.398ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.061ns (Levels of Logic = 2)
  Clock Path Skew:      -0.302ns (1.371 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.A5     net (fanout=2304)     4.099   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
                                                          i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ----------------------
    Total                                          5.061ns (0.513ns logic, 4.548ns
                                                           (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.397ns (requirement - (data path - clock path skew + u
  Source:                i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:           i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:           5.000ns
  Data Path Delay:       5.131ns (Levels of Logic = 1)
  Clock Path Skew:       -0.231ns (1.357 - 1.588)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X56Y105.B3     net (fanout=2307)      4.755   i_GeneticAlg/i_SerialCos
    SLICE_X56Y105.CLK    Tas                    0.019   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          5.131ns (0.376ns logic, 4.755ns
                                                           (7.3% logic, 92.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.394ns (requirement - (data path - clock path skew + u
  Source:                i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:           i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:           5.000ns
  Data Path Delay:       5.128ns (Levels of Logic = 1)
  Clock Path Skew:       -0.231ns (1.357 - 1.588)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X56Y105.D1     net (fanout=2307)     4.752   i_GeneticAlg/i_SerialCos
    SLICE_X56Y105.CLK    Tas                   0.019   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.128ns (0.376ns logic, 4.752ns
                                                       (7.3% logic, 92.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.394ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].:
  Requirement:          5.000ns
  Data Path Delay:      5.060ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.D5     net (fanout=2304)     4.137   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.060ns (0.503ns logic, 4.557ns
                                                       (9.9% logic, 90.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.392ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_im_5 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][(
  Requirement:          5.000ns
```

```
  Data Path Delay:       5.313ns (Levels of Logic = 0)
  Clock Path Skew:       -0.044ns (1.398 - 1.442)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X108Y112.BQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X38Y43.BX      net (fanout=11)       4.991   i_GeneticAlg/Mut2CostWei
    SLICE_X38Y43.CLK     Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.313ns (0.322ns logic, 4.991ns
                                                       (6.1% logic, 93.9% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.391ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.057ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.D5     net (fanout=2304)     4.134   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
                                                          i_GeneticAlg/i_SerialC
    ------------------------------------------------  ----------------------
    Total                                          5.057ns (0.503ns logic, 4.554ns
                                                           (9.9% logic, 90.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.389ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.055ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.A5     net (fanout=2304)     4.129   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ------------------------------------------------  -------------------
    Total                                      5.055ns (0.506ns logic, 4.549ns
                                                       (10.0% logic, 90.0% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.388ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[4]_im_6 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[1][4
  Requirement:          5.000ns
  Data Path Delay:      5.241ns (Levels of Logic = 1)
  Clock Path Skew:      -0.112ns (1.298 - 1.410)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
```

```
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[4]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X116Y117.CQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X38Y156.C5     net (fanout=11)       4.914   i_GeneticAlg/Mut2CostWei
    SLICE_X38Y156.CLK    Tas                   0.005   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/Mut2CostW
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.241ns (0.327ns logic, 4.914ns
                                                       (6.2% logic, 93.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.386ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.038ns (Levels of Logic = 2)
  Clock Path Skew:      -0.313ns (1.359 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y98.B1      net (fanout=2304)     4.115   i_GeneticAlg/i_SerialCos
    SLICE_X62Y98.CLK     Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.038ns (0.503ns logic, 4.535ns
                                                       (10.0% logic, 90.0% ro

--------------------------------------------------------------------------------
```

```
Slack (setup path):     -0.385ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[5]_re_8 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][5
  Requirement:          5.000ns
  Data Path Delay:      5.541ns (Levels of Logic = 0)
  Clock Path Skew:      0.191ns (1.574 - 1.383)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[5]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X122Y102.AMUX  Tshcko                 0.394   i_GeneticAlg/Mut2CostWe
                                                        i_GeneticAlg/Mut2CostW
    SLICE_X63Y28.AX      net (fanout=11)        5.131   i_GeneticAlg/Mut2CostWei
    SLICE_X63Y28.CLK     Tdick                  0.016   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                       5.541ns (0.410ns logic, 5.131ns
                                                        (7.4% logic, 92.6% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.384ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_im_6 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[9][0
  Requirement:          5.000ns
  Data Path Delay:      5.270ns (Levels of Logic = 1)
  Clock Path Skew:      -0.079ns (1.363 - 1.442)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X108Y112.CQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                        i_GeneticAlg/Mut2CostW
    SLICE_X57Y153.C5     net (fanout=11)        4.912   i_GeneticAlg/Mut2CostWei
```

```
    SLICE_X57Y153.CLK     Tas                   0.036   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/Mut2CostW
                                                        i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ---------------------
    Total                                         5.270ns (0.358ns logic, 4.912ns
                                                          (6.8% logic, 93.2% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.379ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.045ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  ------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.A5     net (fanout=2304)     4.119   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                        5.045ns (0.506ns logic, 4.539ns
                                                         (10.0% logic, 90.0% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.369ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.034ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.B6     net (fanout=2304)     4.075   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.034ns (0.510ns logic, 4.524ns
                                                       (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.367ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.032ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.C6     net (fanout=2304)     4.070   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
```

```
    Total                                             5.032ns (0.513ns logic, 4.519ns
                                                              (10.2% logic, 89.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.367ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.031ns (Levels of Logic = 2)
  Clock Path Skew:      -0.301ns (1.371 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.D5     net (fanout=2304)     4.108   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                             5.031ns (0.503ns logic, 4.528ns
                                                              (10.0% logic, 90.0% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.364ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.073ns (Levels of Logic = 1)
  Clock Path Skew:      -0.256ns (1.332 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X51Y103.D5     net (fanout=2307)      4.659   i_GeneticAlg/i_SerialCos
    SLICE_X51Y103.CLK    Tas                    0.057   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                       5.073ns (0.414ns logic, 4.659ns
                                                        (8.2% logic, 91.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.361ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.026ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                   0.283   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)         0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                   0.170   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X63Y123.B6     net (fanout=2304)      4.067   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                    0.057   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                       5.026ns (0.510ns logic, 4.516ns
                                                        (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.361ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
```

```
  Requirement:          5.000ns
  Data Path Delay:      5.025ns (Levels of Logic = 2)
  Clock Path Skew:      -0.301ns (1.371 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.A5     net (fanout=2304)     4.099   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.025ns (0.506ns logic, 4.519ns
                                                       (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.360ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.025ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.C6     net (fanout=2304)     4.063   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.025ns (0.513ns logic, 4.512ns
                                                       (10.2% logic, 89.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.352ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].:
  Requirement:          5.000ns
  Data Path Delay:      5.101ns (Levels of Logic = 1)
  Clock Path Skew:      -0.216ns (1.372 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X103Y113.B4    net (fanout=2307)     4.687   i_GeneticAlg/i_SerialCos
    SLICE_X103Y113.CLK   Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.101ns (0.414ns logic, 4.687ns
                                                       (8.1% logic, 91.9% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.352ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].:
  Requirement:          5.000ns
  Data Path Delay:      5.061ns (Levels of Logic = 1)
  Clock Path Skew:      -0.256ns (1.332 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X51Y103.A5     net (fanout=2307)     4.644   i_GeneticAlg/i_SerialCos
    SLICE_X51Y103.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.061ns (0.417ns logic, 4.644ns
                                                       (8.2% logic, 91.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.351ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[6]_im_0 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][(
  Requirement:          5.000ns
  Data Path Delay:      5.476ns (Levels of Logic = 1)
  Clock Path Skew:      0.160ns (1.578 - 1.418)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[6]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X115Y106.AQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW(
    SLICE_X63Y35.A5      net (fanout=11)       5.158   i_GeneticAlg/Mut2CostWei
    SLICE_X63Y35.CLK     Tas                   0.035   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/Mut2CostW(
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.476ns (0.318ns logic, 5.158ns
                                                       (5.8% logic, 94.2% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.351ns (requirement - (data path - clock path skew + u
```

```
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_im_6 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][(
  Requirement:          5.000ns
  Data Path Delay:      5.450ns (Levels of Logic = 0)
  Clock Path Skew:      0.134ns (1.576 - 1.442)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X108Y112.CQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW(
    SLICE_X61Y39.CX      net (fanout=11)       5.112   i_GeneticAlg/Mut2CostWei
    SLICE_X61Y39.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.450ns (0.338ns logic, 5.112ns
                                                       (6.2% logic, 93.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.339ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_re_2 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[9][(
  Requirement:          5.000ns
  Data Path Delay:      5.200ns (Levels of Logic = 0)
  Clock Path Skew:      -0.104ns (1.338 - 1.442)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X108Y112.CMUX  Tshcko                0.395   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW(
    SLICE_X49Y156.CX     net (fanout=11)       4.789   i_GeneticAlg/Mut2CostWei
    SLICE_X49Y156.CLK    Tdick                 0.016   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          5.200ns (0.411ns logic, 4.789ns
                                                           (7.9% logic, 92.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.337ns (requirement - (data path - clock path skew + u
  Source:                i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:           i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:           5.000ns
  Data Path Delay:       5.002ns (Levels of Logic = 2)
  Clock Path Skew:       -0.300ns (1.373 - 1.673)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y119.D5     net (fanout=2304)     4.043   i_GeneticAlg/i_SerialCos
    SLICE_X63Y119.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          5.002ns (0.510ns logic, 4.492ns
                                                           (10.2% logic, 89.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.334ns (requirement - (data path - clock path skew + u
  Source:                i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:           i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:           5.000ns
  Data Path Delay:       5.043ns (Levels of Logic = 1)
  Clock Path Skew:       -0.256ns (1.332 - 1.588)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X50Y103.D5     net (fanout=2307)      4.667   i_GeneticAlg/i_SerialCos
    SLICE_X50Y103.CLK    Tas                    0.019   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                       5.043ns (0.376ns logic, 4.667ns
                                                        (7.5% logic, 92.5% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.332ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.998ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                   0.283   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)         0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                   0.163   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X62Y123.B6     net (fanout=2304)      4.075   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                    0.057   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                       4.998ns (0.503ns logic, 4.495ns
                                                        (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.330ns (requirement - (data path - clock path skew + u
```

```
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.996ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.C6     net (fanout=2304)     4.070   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      4.996ns (0.506ns logic, 4.490ns
                                                       (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.328ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.991ns (Levels of Logic = 2)
  Clock Path Skew:      -0.302ns (1.371 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
```

```
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.B6     net (fanout=2304)     4.032   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.991ns (0.510ns logic, 4.481ns
                                                       (10.2% logic, 89.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.328ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.017ns (Levels of Logic = 1)
  Clock Path Skew:      -0.276ns (1.312 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X41Y109.D6     net (fanout=2307)     4.603   i_GeneticAlg/i_SerialCos
    SLICE_X41Y109.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.017ns (0.414ns logic, 4.603ns
                                                       (8.3% logic, 91.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.328ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.145ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
```

```
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A19      net (fanout=32)       0.475   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.145ns (3.356ns logic, 1.789ns
                                                       (65.2% logic, 34.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.328ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.145ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A18      net (fanout=32)       0.475   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    ---------------------------------------------------  ----------------------
    Total                                                5.145ns (3.356ns logic, 1.789ns
                                                                 (65.2% logic, 34.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.328ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.145ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A17      net (fanout=32)       0.475   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                                5.145ns (3.356ns logic, 1.789ns
                                                                 (65.2% logic, 34.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.326ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.089ns (Levels of Logic = 1)
  Clock Path Skew:      -0.202ns (1.386 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X94Y113.D2     net (fanout=2307)      4.675   i_GeneticAlg/i_SerialCos
    SLICE_X94Y113.CLK    Tas                    0.057   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                       5.089ns (0.414ns logic, 4.675ns
                                                        (8.1% logic, 91.9% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.326ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.035ns (Levels of Logic = 1)
  Clock Path Skew:      -0.256ns (1.332 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X50Y103.A5     net (fanout=2307)      4.657   i_GeneticAlg/i_SerialCos
    SLICE_X50Y103.CLK    Tas                    0.021   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                       5.035ns (0.378ns logic, 4.657ns
                                                        (7.5% logic, 92.5% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.325ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.361ns (Levels of Logic = 1)
  Clock Path Skew:      0.071ns (1.484 - 1.413)
```

```
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A11      net (fanout=32)       0.518   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.361ns (3.356ns logic, 2.005ns
                                                       (62.6% logic, 37.4% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.325ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.990ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y119.A5     net (fanout=2304)     4.028   i_GeneticAlg/i_SerialCos
```

```
    SLICE_X63Y119.CLK     Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ---------------------
    Total                                       4.990ns (0.513ns logic, 4.477ns
                                                        (10.3% logic, 89.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.325ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.014ns (Levels of Logic = 1)
  Clock Path Skew:      -0.276ns (1.312 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X41Y109.A6     net (fanout=2307)      4.597   i_GeneticAlg/i_SerialCos
    SLICE_X41Y109.CLK    Tas                    0.060   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                       5.014ns (0.417ns logic, 4.597ns
                                                        (8.3% logic, 91.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.325ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.142ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
```

```
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A16      net (fanout=32)       0.472   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.142ns (3.356ns logic, 1.786ns
                                                       (65.3% logic, 34.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.324ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.990ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.B6     net (fanout=2304)     4.067   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      4.990ns (0.503ns logic, 4.487ns
                                                       (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
```

```
Slack (setup path):     -0.323ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.086ns (Levels of Logic = 1)
  Clock Path Skew:      -0.202ns (1.386 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X94Y113.A2     net (fanout=2307)     4.669   i_GeneticAlg/i_SerialCos
    SLICE_X94Y113.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.086ns (0.417ns logic, 4.669ns
                                                       (8.2% logic, 91.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.323ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.989ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.C6     net (fanout=2304)     4.063   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.989ns (0.506ns logic, 4.483ns
                                                       (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.320ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[5]_re_3 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[1][5
  Requirement:          5.000ns
  Data Path Delay:      5.233ns (Levels of Logic = 1)
  Clock Path Skew:      -0.052ns (1.332 - 1.384)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[5]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X120Y101.DQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X51Y143.D4     net (fanout=11)       4.879   i_GeneticAlg/Mut2CostWei
    SLICE_X51Y143.CLK    Tas                   0.032   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/Mut2CostW
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.233ns (0.354ns logic, 4.879ns
                                                       (6.8% logic, 93.2% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.318ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.135ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A15      net (fanout=32)       0.465   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.135ns (3.356ns logic, 1.779ns
                                                       (65.4% logic, 34.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.318ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.135ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A14      net (fanout=32)       0.465   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.135ns (3.356ns logic, 1.779ns
```

(65.4% logic, 34.6% ro

Slack (setup path): -0.318ns (requirement - (data path - clock path skew + u
Source: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
Destination: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
Requirement: 5.000ns
Data Path Delay: 5.135ns (Levels of Logic = 1)
Clock Path Skew: -0.148ns (1.395 - 1.543)
Source Clock: Clk_BUFGP rising at 0.000ns
Destination Clock: Clk_BUFGP rising at 5.000ns
Clock Uncertainty: 0.035ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.070ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
SLICE_X53Y37.BQ	Tcko	0.283	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC
SLICE_X13Y39.C5	net (fanout=2)	1.314	i_GeneticAlg/i_SerialCos
SLICE_X13Y39.C	Tilo	0.061	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC
DSP48_X0Y17.A13	net (fanout=32)	0.465	i_GeneticAlg/i_SerialCos
DSP48_X0Y17.CLK	Tdspdck_A_PREG_MULT	3.012	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC
Total		5.135ns	(3.356ns logic, 1.779ns (65.4% logic, 34.6% ro

---

Slack (setup path): -0.316ns (requirement - (data path - clock path skew + u
Source: i_GeneticAlg/Mut2CostWeights2[2]_re_7 (FF)
Destination: i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][
Requirement: 5.000ns
Data Path Delay: 5.489ns (Levels of Logic = 1)
Clock Path Skew: 0.208ns (1.604 - 1.396)
Source Clock: Clk_BUFGP rising at 0.000ns
Destination Clock: Clk_BUFGP rising at 5.000ns
Clock Uncertainty: 0.035ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.070ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[2]_re

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X118Y105.DMUX  Tshcko                 0.394   i_GeneticAlg/Mut2CostWe
                                                        i_GeneticAlg/Mut2CostW
    SLICE_X74Y37.D3      net (fanout=11)        5.067   i_GeneticAlg/Mut2CostWei
    SLICE_X74Y37.CLK     Tas                    0.028   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/Mut2CostW
                                                        i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.489ns (0.422ns logic, 5.067ns
                                                       (7.7% logic, 92.3% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.316ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.967ns (Levels of Logic = 2)
  Clock Path Skew:      -0.314ns (1.359 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                   0.283   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)         0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                   0.170   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X62Y98.C3      net (fanout=2304)      4.005   i_GeneticAlg/i_SerialCos
    SLICE_X62Y98.CLK     Tas                    0.060   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.967ns (0.513ns logic, 4.454ns
                                                       (10.3% logic, 89.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.315ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.358ns (Levels of Logic = 1)
```

```
  Clock Path Skew:      0.078ns (1.484 - 1.406)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A11      net (fanout=32)       0.518   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.358ns (3.356ns logic, 2.002ns
                                                       (62.6% logic, 37.4% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.312ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.348ns (Levels of Logic = 1)
  Clock Path Skew:      0.071ns (1.484 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    DSP48_X0Y25.A24      net (fanout=32)       0.505   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.348ns (3.356ns logic, 1.992ns
                                                       (62.8% logic, 37.2% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.307ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.124ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A12      net (fanout=32)       0.454   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.124ns (3.356ns logic, 1.768ns
                                                       (65.5% logic, 34.5% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.305ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[2]_re_4 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[1][1
  Requirement:          5.000ns
  Data Path Delay:      5.214ns (Levels of Logic = 0)
  Clock Path Skew:      -0.056ns (1.340 - 1.396)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
```

```
    Total Input Jitter (TIJ):    0.000ns
    Discrete Jitter (DJ):        0.000ns
    Phase Error (PE):            0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[2]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X118Y105.AMUX  Tshcko                 0.394   i_GeneticAlg/Mut2CostWe
                                                         i_GeneticAlg/Mut2CostW
    SLICE_X51Y150.AX     net (fanout=11)        4.804   i_GeneticAlg/Mut2CostWei
    SLICE_X51Y150.CLK    Tdick                  0.016   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                       5.214ns (0.410ns logic, 4.804ns
                                                         (7.9% logic, 92.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.302ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].i
  Requirement:          5.000ns
  Data Path Delay:      5.345ns (Levels of Logic = 1)
  Clock Path Skew:      0.078ns (1.484 - 1.406)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                   0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)         1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                   0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A24      net (fanout=32)        0.505   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT    3.012   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                       5.345ns (3.356ns logic, 1.989ns
                                                         (62.8% logic, 37.2% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.302ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
```

```
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.965ns (Levels of Logic = 2)
  Clock Path Skew:      -0.302ns (1.371 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.C4     net (fanout=2304)     4.184   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.965ns (0.511ns logic, 4.454ns
                                                       (10.3% logic, 89.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.300ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.966ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    SLICE_X63Y119.D5     net (fanout=2304)     4.043   i_GeneticAlg/i_SerialCos
    SLICE_X63Y119.CLK    Tas                   0.057    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      4.966ns (0.503ns logic, 4.463ns
                                                       (10.1% logic, 89.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.296ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.113ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A10      net (fanout=32)       0.443   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.113ns (3.356ns logic, 1.757ns
                                                       (65.6% logic, 34.4% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.295ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.112ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
```

```
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A11      net (fanout=32)       0.442   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.112ns (3.356ns logic, 1.756ns
                                                       (65.6% logic, 34.4% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.291ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.955ns (Levels of Logic = 2)
  Clock Path Skew:      -0.301ns (1.371 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.B6     net (fanout=2304)     4.032   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
                                                          i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ----------------------
    Total                                          4.955ns (0.503ns logic, 4.452ns
                                                           (10.2% logic, 89.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.290ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[8]_re_1 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][8
  Requirement:          5.000ns
  Data Path Delay:      5.206ns (Levels of Logic = 0)
  Clock Path Skew:      -0.049ns (1.397 - 1.446)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[8]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X105Y110.BQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X38Y44.BX      net (fanout=11)       4.923   i_GeneticAlg/Mut2CostWei
    SLICE_X38Y44.CLK     Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.206ns (0.283ns logic, 4.923ns
                                                       (5.4% logic, 94.6% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.288ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.954ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y119.A5     net (fanout=2304)     4.028   i_GeneticAlg/i_SerialCos
    SLICE_X63Y119.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      4.954ns (0.506ns logic, 4.448ns
                                                       (10.2% logic, 89.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.284ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].i
  Requirement:          5.000ns
  Data Path Delay:      5.233ns (Levels of Logic = 1)
  Clock Path Skew:      -0.016ns (0.960 - 0.976)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y79.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X10Y73.D5      net (fanout=10)       1.117   i_GeneticAlg/i_SerialCos
    SLICE_X10Y73.D       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A3       net (fanout=2)        0.760   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.233ns (3.356ns logic, 1.877ns
                                                       (64.1% logic, 35.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.279ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
```

```
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.931ns (Levels of Logic = 2)
  Clock Path Skew:      -0.313ns (1.359 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y98.C3      net (fanout=2304)     4.005   i_GeneticAlg/i_SerialCos
    SLICE_X62Y98.CLK     Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.931ns (0.506ns logic, 4.425ns
                                                       (10.3% logic, 89.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.273ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Requirement:          5.000ns
  Data Path Delay:      5.306ns (Levels of Logic = 2)
  Clock Path Skew:      0.068ns (1.482 - 1.414)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X46Y89.AQ      Tcko                  0.322   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    SLICE_X46Y83.A5      net (fanout=10)       0.817    i_GeneticAlg/i_SerialCos
    SLICE_X46Y83.A       Tilo                  0.061     i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    SLICE_X49Y77.B5      net (fanout=3)        0.678    i_GeneticAlg/i_SerialCos
    SLICE_X49Y77.B       Tilo                  0.061     i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    DSP48_X2Y30.A8       net (fanout=2)        0.355    i_GeneticAlg/i_SerialCos
    DSP48_X2Y30.CLK      Tdspdck_A_PREG_MULT   3.012     i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.306ns (3.456ns logic, 1.850ns
                                                       (65.1% logic, 34.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.271ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[5]_im_6 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][5
  Requirement:          5.000ns
  Data Path Delay:      5.386ns (Levels of Logic = 1)
  Clock Path Skew:      0.150ns (1.574 - 1.424)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[5]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X111Y101.CQ    Tcko                  0.283    i_GeneticAlg/Mut2CostWe
                                                          i_GeneticAlg/Mut2CostW
    SLICE_X62Y28.C2      net (fanout=11)       5.066    i_GeneticAlg/Mut2CostWei
    SLICE_X62Y28.CLK     Tas                   0.037     i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/Mut2CostW
                                                          i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.386ns (0.320ns logic, 5.066ns
                                                       (5.9% logic, 94.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.271ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[7]_re_8 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][7
  Requirement:          5.000ns
  Data Path Delay:      5.345ns (Levels of Logic = 0)
  Clock Path Skew:      0.109ns (1.559 - 1.450)
  Source Clock:         Clk_BUFGP rising at 0.000ns
```

```
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[7]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X105Y123.AQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X55Y39.AX      net (fanout=11)       5.046   i_GeneticAlg/Mut2CostWei
    SLICE_X55Y39.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.345ns (0.299ns logic, 5.046ns
                                                       (5.6% logic, 94.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.270ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.007ns (Levels of Logic = 1)
  Clock Path Skew:      -0.228ns (1.360 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X60Y104.B6     net (fanout=2307)     4.631   i_GeneticAlg/i_SerialCos
    SLICE_X60Y104.CLK    Tas                   0.019   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.007ns (0.376ns logic, 4.631ns
                                                       (7.5% logic, 92.5% rou
```

```
--------------------------------------------------------------------------------
Slack (setup path):     -0.267ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.004ns (Levels of Logic = 1)
  Clock Path Skew:      -0.228ns (1.360 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X60Y104.C6     net (fanout=2307)     4.626   i_GeneticAlg/i_SerialCos
    SLICE_X60Y104.CLK    Tas                   0.021   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.004ns (0.378ns logic, 4.626ns
                                                       (7.6% logic, 92.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.266ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_6 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[6].
  Requirement:          5.000ns
  Data Path Delay:      5.167ns (Levels of Logic = 1)
  Clock Path Skew:      -0.064ns (0.956 - 1.020)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X67Y110.AQ     Tcko                  0.283   i_GeneticAlg/i_SerialCo
```

```
                                                                 i_GeneticAlg/i_SerialC
    SLICE_X27Y51.C5      net (fanout=2307)     2.888   i_GeneticAlg/i_SerialCos
    SLICE_X27Y51.C       Tilo                  0.061    i_GeneticAlg/i_SerialCo
                                                                 i_GeneticAlg/i_SerialC
    DSP48_X2Y33.CEA2     net (fanout=77)       1.769   i_GeneticAlg/i_SerialCos
    DSP48_X2Y33.CLK      Tdspdck_CEA_AREG      0.166    i_GeneticAlg/i_SerialCo
                                                                 i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                              5.167ns (0.510ns logic, 4.657ns
                                                                 (9.9% logic, 90.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.265ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].:
  Requirement:          5.000ns
  Data Path Delay:      5.290ns (Levels of Logic = 2)
  Clock Path Skew:      0.060ns (1.474 - 1.414)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X46Y89.BQ      Tcko                  0.322    i_GeneticAlg/i_SerialCo
                                                                 i_GeneticAlg/i_SerialC
    SLICE_X47Y153.B6     net (fanout=8)        2.859   i_GeneticAlg/i_SerialCos
    SLICE_X47Y153.B      Tilo                  0.061    i_GeneticAlg/i_SerialCo
                                                                 i_GeneticAlg/i_SerialC
    SLICE_X47Y155.D6     net (fanout=1)        0.206   i_GeneticAlg/i_SerialCos
    SLICE_X47Y155.D      Tilo                  0.061    i_GeneticAlg/i_SerialCo
                                                                 i_GeneticAlg/i_SerialC
    DSP48_X1Y69.A1       net (fanout=1)        1.524   i_GeneticAlg/i_SerialCos
    DSP48_X1Y69.CLK      Tdspdck_A_AREG        0.257    i_GeneticAlg/i_SerialCo
                                                                 i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                              5.290ns (0.701ns logic, 4.589ns
                                                                 (13.3% logic, 86.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.264ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].:
  Requirement:          5.000ns
  Data Path Delay:      5.013ns (Levels of Logic = 1)
```

```
  Clock Path Skew:      -0.216ns (1.372 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X103Y113.C5    net (fanout=2307)     4.596   i_GeneticAlg/i_SerialCos
    SLICE_X103Y113.CLK   Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.013ns (0.417ns logic, 4.596ns
                                                       (8.3% logic, 91.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.264ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.306ns (Levels of Logic = 1)
  Clock Path Skew:      0.077ns (1.490 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A24      net (fanout=32)       0.463   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          5.306ns (3.356ns logic, 1.950ns
                                                           (63.2% logic, 36.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.262ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[7]_re_0 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[1][
  Requirement:          5.000ns
  Data Path Delay:      5.113ns (Levels of Logic = 0)
  Clock Path Skew:      -0.114ns (1.330 - 1.444)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[7]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X108Y123.AQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X50Y142.AX     net (fanout=11)       4.791   i_GeneticAlg/Mut2CostWei
    SLICE_X50Y142.CLK    Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                          5.113ns (0.322ns logic, 4.791ns
                                                           (6.3% logic, 93.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.262ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[3]_im_9 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][
  Requirement:          5.000ns
  Data Path Delay:      5.356ns (Levels of Logic = 0)
  Clock Path Skew:      0.129ns (1.573 - 1.444)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[3]_im
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X109Y119.BQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X61Y30.BX      net (fanout=11)       5.057   i_GeneticAlg/Mut2CostWei
    SLICE_X61Y30.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.356ns (0.299ns logic, 5.057ns
                                                       (5.6% logic, 94.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.256ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.298ns (Levels of Logic = 1)
  Clock Path Skew:      0.077ns (1.490 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A17      net (fanout=32)       0.455   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.298ns (3.356ns logic, 1.942ns
                                                       (63.3% logic, 36.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.256ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.298ns (Levels of Logic = 1)
  Clock Path Skew:      0.077ns (1.490 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
```

```
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A19      net (fanout=32)       0.455   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.298ns (3.356ns logic, 1.942ns
                                                       (63.3% logic, 36.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.256ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.298ns (Levels of Logic = 1)
  Clock Path Skew:      0.077ns (1.490 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A16      net (fanout=32)       0.455   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          5.298ns (3.356ns logic, 1.942ns
                                                           (63.3% logic, 36.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.256ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.298ns (Levels of Logic = 1)
  Clock Path Skew:      0.077ns (1.490 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A18      net (fanout=32)       0.455   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                          5.298ns (3.356ns logic, 1.942ns
                                                           (63.3% logic, 36.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.256ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[4]_re_8 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][4
  Requirement:          5.000ns
  Data Path Delay:      5.229ns (Levels of Logic = 0)
  Clock Path Skew:      0.008ns (1.417 - 1.409)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
```

```
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[4]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X116Y114.AQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X43Y51.AX      net (fanout=11)       4.891   i_GeneticAlg/Mut2CostWei
    SLICE_X43Y51.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.229ns (0.338ns logic, 4.891ns
                                                       (6.5% logic, 93.5% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.255ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[2]_im_5 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][2
  Requirement:          5.000ns
  Data Path Delay:      5.428ns (Levels of Logic = 1)
  Clock Path Skew:      0.208ns (1.604 - 1.396)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[2]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X118Y105.BQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X74Y38.B5      net (fanout=11)       5.069   i_GeneticAlg/Mut2CostWei
    SLICE_X74Y38.CLK     Tas                   0.037   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/Mut2CostW
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.428ns (0.359ns logic, 5.069ns
                                                       (6.6% logic, 93.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.254ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.303ns (Levels of Logic = 1)
  Clock Path Skew:      0.084ns (1.490 - 1.406)
```

```
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A24      net (fanout=32)       0.463   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.303ns (3.356ns logic, 1.947ns
                                                       (63.3% logic, 36.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.254ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].i
  Requirement:          5.000ns
  Data Path Delay:      5.203ns (Levels of Logic = 1)
  Clock Path Skew:      -0.016ns (0.960 - 0.976)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y79.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y72.D5      net (fanout=10)       1.094   i_GeneticAlg/i_SerialCos
    SLICE_X11Y72.D       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A1       net (fanout=2)        0.753   i_GeneticAlg/i_SerialCos
```

```
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          5.203ns (3.356ns logic, 1.847ns
                                                           (64.5% logic, 35.5% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.253ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.918ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y119.B6     net (fanout=2304)     3.959   i_GeneticAlg/i_SerialCos
    SLICE_X63Y119.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          4.918ns (0.510ns logic, 4.408ns
                                                           (10.4% logic, 89.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.252ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.917ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
```

```
    Total Input Jitter (TIJ):    0.000ns
    Discrete Jitter (DJ):        0.000ns
    Phase Error (PE):            0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X62Y34.AQ       Tcko                 0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C1       net (fanout=6)       0.449   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX     Tilo                 0.170   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X63Y119.C6      net (fanout=2304)    3.955   i_GeneticAlg/i_SerialCos
    SLICE_X63Y119.CLK     Tas                  0.060   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                      4.917ns (0.513ns logic, 4.404ns
                                                         (10.4% logic, 89.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.251ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].i
  Requirement:          5.000ns
  Data Path Delay:      5.000ns (Levels of Logic = 1)
  Clock Path Skew:      -0.216ns (1.372 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX     Tshcko               0.357   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X103Y113.A4     net (fanout=2307)    4.583   i_GeneticAlg/i_SerialCos
    SLICE_X103Y113.CLK    Tas                  0.060   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                      5.000ns (0.417ns logic, 4.583ns
                                                         (8.3% logic, 91.7% rou

--------------------------------------------------------------------------------
```

```
Slack (setup path):     -0.250ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.915ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.D5     net (fanout=2304)     4.137   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.915ns (0.508ns logic, 4.407ns
                                                       (10.3% logic, 89.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.249ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_0 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.279ns (Levels of Logic = 1)
  Clock Path Skew:      0.065ns (1.497 - 1.432)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  -------------------
    SLICE_X105Y101.DMUX  Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X102Y41.A5     net (fanout=2307)      2.399   i_GeneticAlg/i_SerialCos
    SLICE_X102Y41.A      Tilo                   0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    DSP48_X3Y26.CEA2     net (fanout=83)        2.296   i_GeneticAlg/i_SerialCos
    DSP48_X3Y26.CLK      Tdspdck_CEA_AREG       0.166   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ---------------------
    Total                                       5.279ns (0.584ns logic, 4.695ns
                                                         (11.1% logic, 88.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.247ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.912ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                   0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)         0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                   0.168   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X63Y123.D5     net (fanout=2304)      4.134   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                    0.057   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ---------------------
    Total                                       4.912ns (0.508ns logic, 4.404ns
                                                         (10.3% logic, 89.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.247ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[3]_re_0 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][
  Requirement:          5.000ns
  Data Path Delay:      5.223ns (Levels of Logic = 0)
```

```
  Clock Path Skew:      0.011ns (1.418 - 1.407)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[3]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X116Y111.AQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X44Y58.AX      net (fanout=11)       4.901   i_GeneticAlg/Mut2CostWei
    SLICE_X44Y58.CLK     Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                      5.223ns (0.322ns logic, 4.901ns
                                                       (6.2% logic, 93.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.246ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.295ns (Levels of Logic = 1)
  Clock Path Skew:      0.084ns (1.490 - 1.406)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A16      net (fanout=32)       0.455   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    ----------------------------------------------------  ----------------------
    Total                                                 5.295ns (3.356ns logic, 1.939ns
                                                                  (63.4% logic, 36.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.246ns (requirement - (data path - clock path skew + u
  Source:                i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:           i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:           5.000ns
  Data Path Delay:       5.295ns (Levels of Logic = 1)
  Clock Path Skew:       0.084ns (1.490 - 1.406)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A18      net (fanout=32)       0.455   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                              5.295ns (3.356ns logic, 1.939ns
                                                              (63.4% logic, 36.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.246ns (requirement - (data path - clock path skew + u
  Source:                i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:           i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:           5.000ns
  Data Path Delay:       5.295ns (Levels of Logic = 1)
  Clock Path Skew:       0.084ns (1.490 - 1.406)
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

```
  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A19      net (fanout=32)       0.455   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.295ns (3.356ns logic, 1.939ns
                                                       (63.4% logic, 36.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.246ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.295ns (Levels of Logic = 1)
  Clock Path Skew:      0.084ns (1.490 - 1.406)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A17      net (fanout=32)       0.455   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.295ns (3.356ns logic, 1.939ns
                                                       (63.4% logic, 36.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.245ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
```

```
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.062ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A24      net (fanout=32)       0.392   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                      5.062ns (3.356ns logic, 1.706ns
                                                       (66.3% logic, 33.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.245ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[3]_im_9 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[4][
  Requirement:          5.000ns
  Data Path Delay:      5.066ns (Levels of Logic = 0)
  Clock Path Skew:      -0.144ns (1.300 - 1.444)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[3]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X109Y119.BQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
```

```
    SLICE_X24Y115.BX     net (fanout=11)       4.783   i_GeneticAlg/Mut2CostWei
    SLICE_X24Y115.CLK    Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.066ns (0.283ns logic, 4.783ns
                                                       (5.6% logic, 94.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.245ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.276ns (Levels of Logic = 2)
  Clock Path Skew:      0.066ns (1.512 - 1.446)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X61Y92.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X85Y61.C4      net (fanout=8)        3.273   i_GeneticAlg/i_SerialCos
    SLICE_X85Y61.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X94Y61.D6      net (fanout=1)        0.568   i_GeneticAlg/i_SerialCos
    SLICE_X94Y61.D       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X4Y23.A3       net (fanout=1)        0.773   i_GeneticAlg/i_SerialCos
    DSP48_X4Y23.CLK      Tdspdck_A_AREG        0.257   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.276ns (0.662ns logic, 4.614ns
                                                       (12.5% logic, 87.5% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.245ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.910ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.A5     net (fanout=2304)     4.129   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.910ns (0.511ns logic, 4.399ns
                                                       (10.4% logic, 89.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.242ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.124ns (Levels of Logic = 2)
  Clock Path Skew:      -0.083ns (1.418 - 1.501)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X122Y70.BQ     Tcko                  0.322   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X105Y54.C5     net (fanout=83)       2.460   i_GeneticAlg/i_SerialCos
    SLICE_X105Y54.C      Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X105Y66.D6     net (fanout=1)        0.670   i_GeneticAlg/i_SerialCos
    SLICE_X105Y66.D      Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    DSP48_X4Y37.A7       net (fanout=1)        1.293   i_GeneticAlg/i_SerialCos
    DSP48_X4Y37.CLK      Tdspdck_A_AREG        0.257   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.124ns (0.701ns logic, 4.423ns
                                                       (13.7% logic, 86.3% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.242ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.893ns (Levels of Logic = 2)
  Clock Path Skew:      -0.314ns (1.359 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y98.B1      net (fanout=2304)     4.115   i_GeneticAlg/i_SerialCos
    SLICE_X62Y98.CLK     Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.893ns (0.508ns logic, 4.385ns
                                                       (10.4% logic, 89.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.236ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Requirement:          5.000ns
  Data Path Delay:      5.292ns (Levels of Logic = 2)
  Clock Path Skew:      0.091ns (1.505 - 1.414)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X46Y89.AQ      Tcko                  0.322   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X46Y83.A5      net (fanout=10)       0.817   i_GeneticAlg/i_SerialCos
    SLICE_X46Y83.A       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X49Y77.B5      net (fanout=3)        0.678   i_GeneticAlg/i_SerialCos
    SLICE_X49Y77.B       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y30.A8       net (fanout=2)        0.341   i_GeneticAlg/i_SerialCos
    DSP48_X3Y30.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.292ns (3.456ns logic, 1.836ns
                                                       (65.3% logic, 34.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.236ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].i
  Requirement:          5.000ns
  Data Path Delay:      4.897ns (Levels of Logic = 1)
  Clock Path Skew:      -0.304ns (1.284 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X39Y101.D4     net (fanout=2307)     4.483   i_GeneticAlg/i_SerialCos
    SLICE_X39Y101.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.897ns (0.414ns logic, 4.483ns
```

(8.5% logic, 91.5% rou

Slack (setup path): -0.236ns (requirement - (data path - clock path skew + u
Source: i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
Destination: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
Requirement: 5.000ns
Data Path Delay: 4.985ns (Levels of Logic = 1)
Clock Path Skew: -0.216ns (1.372 - 1.588)
Source Clock: Clk_BUFGP rising at 0.000ns
Destination Clock: Clk_BUFGP rising at 5.000ns
Clock Uncertainty: 0.035ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.070ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
SLICE_X80Y68.AMUX	Tshcko	0.357	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC
SLICE_X103Y113.D4	net (fanout=2307)	4.571	i_GeneticAlg/i_SerialCos
SLICE_X103Y113.CLK	Tas	0.057	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC i_GeneticAlg/i_SerialC
Total		4.985ns	(0.414ns logic, 4.571ns (8.3% logic, 91.7% rou

---

Slack (setup path): -0.235ns (requirement - (data path - clock path skew + u
Source: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
Destination: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
Requirement: 5.000ns
Data Path Delay: 4.900ns (Levels of Logic = 2)
Clock Path Skew: -0.300ns (1.373 - 1.673)
Source Clock: Clk_BUFGP rising at 0.000ns
Destination Clock: Clk_BUFGP rising at 5.000ns
Clock Uncertainty: 0.035ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.070ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)

```
    ----------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.A5     net (fanout=2304)     4.119   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ---------------------
    Total                                      4.900ns (0.511ns logic, 4.389ns
                                                       (10.4% logic, 89.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.235ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[0]_im_4 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][(
  Requirement:          5.000ns
  Data Path Delay:      5.334ns (Levels of Logic = 0)
  Clock Path Skew:      0.134ns (1.576 - 1.442)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[0]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X108Y112.AQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X61Y39.AX      net (fanout=11)       4.996   i_GeneticAlg/Mut2CostWei
    SLICE_X61Y39.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ---------------------
    Total                                      5.334ns (0.338ns logic, 4.996ns
                                                       (6.3% logic, 93.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.234ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.183ns (Levels of Logic = 2)
  Clock Path Skew:      -0.016ns (0.960 - 0.976)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
```

```
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y79.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X10Y73.A5      net (fanout=10)       0.491   i_GeneticAlg/i_SerialCos
    SLICE_X10Y73.A       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X10Y75.A6      net (fanout=3)        0.327   i_GeneticAlg/i_SerialCos
    SLICE_X10Y75.A       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A7       net (fanout=2)        0.948   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.183ns (3.417ns logic, 1.766ns
                                                       (65.9% logic, 34.1% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.233ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_6 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[6].i
  Requirement:          5.000ns
  Data Path Delay:      5.132ns (Levels of Logic = 1)
  Clock Path Skew:      -0.066ns (0.954 - 1.020)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X67Y110.AQ     Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X27Y51.C5      net (fanout=2307)     2.888   i_GeneticAlg/i_SerialCos
    SLICE_X27Y51.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    DSP48_X2Y35.CEA2      net (fanout=77)       1.734   i_GeneticAlg/i_SerialCos
    DSP48_X2Y35.CLK       Tdspdck_CEA_AREG      0.166   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ---------------------
    Total                                       5.132ns (0.510ns logic, 4.622ns
                                                        (9.9% logic, 90.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.231ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.273ns (Levels of Logic = 1)
  Clock Path Skew:      0.077ns (1.490 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location              Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X11Y94.AQ       Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4       net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C        Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A15       net (fanout=32)       0.430   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK       Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ---------------------
    Total                                       5.273ns (3.356ns logic, 1.917ns
                                                        (63.6% logic, 36.4% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.231ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.273ns (Levels of Logic = 1)
  Clock Path Skew:      0.077ns (1.490 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
```

```
    Total Input Jitter (TIJ):    0.000ns
    Discrete Jitter (DJ):         0.000ns
    Phase Error (PE):             0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X11Y94.AQ       Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4       net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C        Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A12       net (fanout=32)       0.430   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK       Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                       5.273ns (3.356ns logic, 1.917ns
                                                         (63.6% logic, 36.4% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.231ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.199ns (Levels of Logic = 2)
  Clock Path Skew:      0.003ns (1.489 - 1.486)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X73Y77.AQ       Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X73Y77.C1       net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X73Y77.CMUX     Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X93Y37.D2       net (fanout=2304)     4.240   i_GeneticAlg/i_SerialCos
    SLICE_X93Y37.CLK      Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                       5.199ns (0.510ns logic, 4.689ns
                                                         (9.8% logic, 90.2% rou
```

```
--------------------------------------------------------------------------------
Slack (setup path):     -0.231ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.267ns (Levels of Logic = 1)
  Clock Path Skew:      0.071ns (1.484 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A10      net (fanout=32)       0.424   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.267ns (3.356ns logic, 1.911ns
                                                       (63.7% logic, 36.3% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.229ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.159ns (Levels of Logic = 2)
  Clock Path Skew:      -0.035ns (0.970 - 1.005)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                          Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X63Y52.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X63Y56.D3      net (fanout=7)        0.702   i_GeneticAlg/i_SerialCos
    SLICE_X63Y56.D       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X63Y56.C5      net (fanout=1)        0.274   i_GeneticAlg/i_SerialCos
    SLICE_X63Y56.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A8       net (fanout=2)        0.766   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                      5.159ns (3.417ns logic, 1.742ns
                                                       (66.2% logic, 33.8% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.225ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.193ns (Levels of Logic = 2)
  Clock Path Skew:      0.003ns (1.489 - 1.486)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                          Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X73Y77.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X73Y77.C1      net (fanout=6)        0.449   i_GeneticAlg/i_SerialCos
    SLICE_X73Y77.CMUX    Tilo                  0.170   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X93Y37.B2      net (fanout=2304)     4.234   i_GeneticAlg/i_SerialCos
    SLICE_X93Y37.CLK     Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                      5.193ns (0.510ns logic, 4.683ns
                                                       (9.8% logic, 90.2% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.225ns (requirement - (data path - clock path skew + u
```

```
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.261ns (Levels of Logic = 1)
  Clock Path Skew:      0.071ns (1.484 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A9       net (fanout=32)       0.418   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.261ns (3.356ns logic, 1.905ns
                                                       (63.8% logic, 36.2% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.223ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.886ns (Levels of Logic = 2)
  Clock Path Skew:      -0.302ns (1.371 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    SLICE_X62Y111.D5     net (fanout=2304)     4.108   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.057    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
                                                          i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.886ns (0.508ns logic, 4.378ns
                                                       (10.4% logic, 89.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.221ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].:
  Requirement:          5.000ns
  Data Path Delay:      5.264ns (Levels of Logic = 1)
  Clock Path Skew:      0.078ns (1.484 - 1.406)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A10      net (fanout=32)       0.424   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.264ns (3.356ns logic, 1.908ns
                                                       (63.8% logic, 36.2% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.221ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].:
  Requirement:          5.000ns
  Data Path Delay:      5.270ns (Levels of Logic = 1)
  Clock Path Skew:      0.084ns (1.490 - 1.406)
  Source Clock:         Clk_BUFGP rising at 0.000ns
```

```
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A15      net (fanout=32)       0.430   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.270ns (3.356ns logic, 1.914ns
                                                       (63.7% logic, 36.3% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.221ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.270ns (Levels of Logic = 1)
  Clock Path Skew:      0.084ns (1.490 - 1.406)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y27.A12      net (fanout=32)       0.430   i_GeneticAlg/i_SerialCos
    DSP48_X0Y27.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                          5.270ns (3.356ns logic, 1.914ns
                                                           (63.7% logic, 36.3% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.219ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.253ns (Levels of Logic = 2)
  Clock Path Skew:      0.069ns (1.512 - 1.443)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X63Y95.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X101Y59.B2     net (fanout=2)        3.908   i_GeneticAlg/i_SerialCos
    SLICE_X101Y59.B      Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X103Y58.D6     net (fanout=1)        0.208   i_GeneticAlg/i_SerialCos
    SLICE_X103Y58.D      Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X4Y23.A24      net (fanout=16)       0.475   i_GeneticAlg/i_SerialCos
    DSP48_X4Y23.CLK      Tdspdck_A_AREG        0.257   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                          5.253ns (0.662ns logic, 4.591ns
                                                           (12.6% logic, 87.4% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.218ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[3]_im_8 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[4][3
  Requirement:          5.000ns
  Data Path Delay:      5.039ns (Levels of Logic = 0)
  Clock Path Skew:      -0.144ns (1.300 - 1.444)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[3]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X109Y119.AQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X24Y115.AX     net (fanout=11)       4.756   i_GeneticAlg/Mut2CostWei
    SLICE_X24Y115.CLK    Tdick                 0.000   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.039ns (0.283ns logic, 4.756ns
                                                       (5.6% logic, 94.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.217ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.880ns (Levels of Logic = 2)
  Clock Path Skew:      -0.302ns (1.371 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.A5     net (fanout=2304)     4.099   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      4.880ns (0.511ns logic, 4.369ns
                                                       (10.5% logic, 89.5% ro

--------------------------------------------------------------------------------
```

```
Slack (setup path):     -0.216ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.882ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y119.B6     net (fanout=2304)     3.959   i_GeneticAlg/i_SerialCos
    SLICE_X63Y119.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.882ns (0.503ns logic, 4.379ns
                                                       (10.3% logic, 89.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.216ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      4.950ns (Levels of Logic = 1)
  Clock Path Skew:      -0.231ns (1.357 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X56Y105.A4     net (fanout=2307)      4.572   i_GeneticAlg/i_SerialCos
    SLICE_X56Y105.CLK    Tas                    0.021   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                       4.950ns (0.378ns logic, 4.572ns
                                                        (7.6% logic, 92.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.216ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_6 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[6].i
  Requirement:          5.000ns
  Data Path Delay:      5.053ns (Levels of Logic = 1)
  Clock Path Skew:      -0.128ns (0.892 - 1.020)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X67Y110.AQ     Tcko                   0.283   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X27Y51.C5      net (fanout=2307)      2.888   i_GeneticAlg/i_SerialCos
    SLICE_X27Y51.C       Tilo                   0.061   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X40Y80.CE      net (fanout=77)        1.608   i_GeneticAlg/i_SerialCos
    SLICE_X40Y80.CLK     Tceck                  0.213   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                       5.053ns (0.557ns logic, 4.496ns
                                                        (11.0% logic, 89.0% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.215ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].i
  Requirement:          5.000ns
  Data Path Delay:      5.258ns (Levels of Logic = 1)
  Clock Path Skew:      0.078ns (1.484 - 1.406)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
```

```
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y98.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C5      net (fanout=2)        1.484   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A9       net (fanout=32)       0.418   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.258ns (3.356ns logic, 1.902ns
                                                       (63.8% logic, 36.2% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.215ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.881ns (Levels of Logic = 2)
  Clock Path Skew:      -0.299ns (1.373 - 1.672)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y33.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C3      net (fanout=4)        0.420   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y119.C6     net (fanout=2304)     3.955   i_GeneticAlg/i_SerialCos
    SLICE_X63Y119.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          4.881ns (0.506ns logic, 4.375ns
                                                           (10.4% logic, 89.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.214ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.031ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A9       net (fanout=32)       0.361   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                          5.031ns (3.356ns logic, 1.675ns
                                                           (66.7% logic, 33.3% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.210ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      4.871ns (Levels of Logic = 1)
  Clock Path Skew:      -0.304ns (1.284 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
```

```
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                0.357   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X39Y101.C1     net (fanout=2307)     4.454   i_GeneticAlg/i_SerialCos
    SLICE_X39Y101.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      4.871ns (0.417ns logic, 4.454ns
                                                       (8.6% logic, 91.4% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.209ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.872ns (Levels of Logic = 2)
  Clock Path Skew:      -0.302ns (1.371 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X62Y34.CQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C5      net (fanout=4)        0.177   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y111.C4     net (fanout=2304)     4.184   i_GeneticAlg/i_SerialCos
    SLICE_X62Y111.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      4.872ns (0.511ns logic, 4.361ns
                                                       (10.5% logic, 89.5% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.208ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
```

```
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.134ns (Levels of Logic = 1)
  Clock Path Skew:      -0.039ns (0.970 - 1.009)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X63Y48.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X53Y59.C1      net (fanout=4)        1.266   i_GeneticAlg/i_SerialCos
    SLICE_X53Y59.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A18      net (fanout=32)       0.512   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                      5.134ns (3.356ns logic, 1.778ns
                                                       (65.4% logic, 34.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.208ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.134ns (Levels of Logic = 1)
  Clock Path Skew:      -0.039ns (0.970 - 1.009)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X63Y48.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    SLICE_X53Y59.C1      net (fanout=4)        1.266   i_GeneticAlg/i_SerialCos
    SLICE_X53Y59.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A17      net (fanout=32)       0.512   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                              5.134ns (3.356ns logic, 1.778ns
                                                               (65.4% logic, 34.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.208ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.134ns (Levels of Logic = 1)
  Clock Path Skew:      -0.039ns (0.970 - 1.009)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X63Y48.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X53Y59.C1      net (fanout=4)        1.266   i_GeneticAlg/i_SerialCos
    SLICE_X53Y59.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A19      net (fanout=32)       0.512   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                              5.134ns (3.356ns logic, 1.778ns
                                                               (65.4% logic, 34.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.207ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.087ns (Levels of Logic = 2)
  Clock Path Skew:      -0.085ns (1.395 - 1.480)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X30Y34.DQ      Tcko                  0.322   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X23Y38.C5      net (fanout=8)        0.657   i_GeneticAlg/i_SerialCos
    SLICE_X23Y38.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X23Y38.B6      net (fanout=1)        0.296   i_GeneticAlg/i_SerialCos
    SLICE_X23Y38.B       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A8       net (fanout=2)        0.678   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.087ns (3.456ns logic, 1.631ns
                                                       (67.9% logic, 32.1% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.207ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[4]_re_6 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[9][4
  Requirement:          5.000ns
  Data Path Delay:      5.207ns (Levels of Logic = 0)
  Clock Path Skew:      0.035ns (1.477 - 1.442)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[4]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X110Y117.CQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X62Y166.CX     net (fanout=11)       4.869   i_GeneticAlg/Mut2CostWei
    SLICE_X62Y166.CLK    Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
```

```
    Total                                          5.207ns (0.338ns logic, 4.869ns
                                                           (6.5% logic, 93.5% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.207ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_3 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].i
  Requirement:          5.000ns
  Data Path Delay:      4.868ns (Levels of Logic = 1)
  Clock Path Skew:      -0.304ns (1.284 - 1.588)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X80Y68.AMUX    Tshcko                 0.357   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    SLICE_X39Y101.B1     net (fanout=2307)      4.454   i_GeneticAlg/i_SerialCos
    SLICE_X39Y101.CLK    Tas                    0.057   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
                                                        i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                       4.868ns (0.414ns logic, 4.454ns
                                                        (8.5% logic, 91.5% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.206ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].i
  Requirement:          5.000ns
  Data Path Delay:      5.083ns (Levels of Logic = 1)
  Clock Path Skew:      -0.088ns (1.395 - 1.483)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                          Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X29Y38.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X25Y34.D2      net (fanout=6)        0.770   i_GeneticAlg/i_SerialCos
    SLICE_X25Y34.D       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A6       net (fanout=2)        0.957   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                      5.083ns (3.356ns logic, 1.727ns
                                                         (66.0% logic, 34.0% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.205ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[8]_im_8 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[6][8
  Requirement:          5.000ns
  Data Path Delay:      5.145ns (Levels of Logic = 1)
  Clock Path Skew:      -0.025ns (1.417 - 1.442)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[8]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X111Y118.CQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X41Y42.A4      net (fanout=11)       4.828   i_GeneticAlg/Mut2CostWei
    SLICE_X41Y42.CLK     Tas                   0.034   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/Mut2CostW
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.145ns (0.317ns logic, 4.828ns
                                                       (6.2% logic, 93.8% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.205ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.131ns (Levels of Logic = 1)
  Clock Path Skew:      -0.039ns (0.970 - 1.009)
  Source Clock:         Clk_BUFGP rising at 0.000ns
```

```
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X63Y48.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X53Y59.C1      net (fanout=4)        1.266   i_GeneticAlg/i_SerialCos
    SLICE_X53Y59.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A16      net (fanout=32)       0.509   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.131ns (3.356ns logic, 1.775ns
                                                       (65.4% logic, 34.6% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.201ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.018ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A22      net (fanout=32)       0.348   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          5.018ns (3.356ns logic, 1.662ns
                                                           (66.9% logic, 33.1% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.201ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.018ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A23      net (fanout=32)       0.348   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                          5.018ns (3.356ns logic, 1.662ns
                                                           (66.9% logic, 33.1% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.200ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.017ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
```

```
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A20      net (fanout=32)       0.347   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                      5.017ns (3.356ns logic, 1.661ns
                                                       (66.9% logic, 33.1% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.199ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.235ns (Levels of Logic = 1)
  Clock Path Skew:      0.071ns (1.484 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y68.B4      net (fanout=3)        1.370   i_GeneticAlg/i_SerialCos
    SLICE_X11Y68.B       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A8       net (fanout=2)        0.509   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                      5.235ns (3.356ns logic, 1.879ns
                                                       (64.1% logic, 35.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.198ns (requirement - (data path - clock path skew + u
```

```
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.015ns (Levels of Logic = 1)
  Clock Path Skew:      -0.148ns (1.395 - 1.543)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y17.A21      net (fanout=32)       0.345   i_GeneticAlg/i_SerialCos
    DSP48_X0Y17.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.015ns (3.356ns logic, 1.659ns
                                                       (66.9% logic, 33.1% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.194ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[2]_im_9 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[4][
  Requirement:          5.000ns
  Data Path Delay:      5.035ns (Levels of Logic = 1)
  Clock Path Skew:      -0.124ns (1.281 - 1.405)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[2]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X117Y109.BQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
```

```
                                                          i_GeneticAlg/Mut2CostW
    SLICE_X28Y97.B3      net (fanout=11)       4.746   i_GeneticAlg/Mut2CostWei
    SLICE_X28Y97.CLK     Tas                   0.006   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/Mut2CostW
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.035ns (0.289ns logic, 4.746ns
                                                         (5.7% logic, 94.3% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.193ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Requirement:          5.000ns
  Data Path Delay:      5.226ns (Levels of Logic = 2)
  Clock Path Skew:      0.068ns (1.482 - 1.414)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X46Y89.AQ      Tcko                  0.322   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    SLICE_X46Y83.A5      net (fanout=10)       0.817   i_GeneticAlg/i_SerialCos
    SLICE_X46Y83.A       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    SLICE_X47Y83.B6      net (fanout=3)        0.199   i_GeneticAlg/i_SerialCos
    SLICE_X47Y83.B       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    DSP48_X2Y30.A7       net (fanout=2)        0.754   i_GeneticAlg/i_SerialCos
    DSP48_X2Y30.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.226ns (3.456ns logic, 1.770ns
                                                         (66.1% logic, 33.9% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.192ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.160ns (Levels of Logic = 2)
  Clock Path Skew:      0.003ns (1.489 - 1.486)
  Source Clock:         Clk_BUFGP rising at 0.000ns
```

```
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X72Y76.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X73Y77.C3      net (fanout=4)        0.417   i_GeneticAlg/i_SerialCos
    SLICE_X73Y77.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X93Y37.D2      net (fanout=2304)     4.240   i_GeneticAlg/i_SerialCos
    SLICE_X93Y37.CLK     Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.160ns (0.503ns logic, 4.657ns
                                                       (9.7% logic, 90.3% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.192ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[3]_im_0 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[0][3
  Requirement:          5.000ns
  Data Path Delay:      5.227ns (Levels of Logic = 0)
  Clock Path Skew:      0.070ns (1.495 - 1.425)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[3]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X114Y111.AQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X81Y64.AX      net (fanout=11)       4.889   i_GeneticAlg/Mut2CostWei
    SLICE_X81Y64.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
```

```
    Total                                          5.227ns (0.338ns logic, 4.889ns
                                                           (6.5% logic, 93.5% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.192ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[2]_re_8 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][2
  Requirement:          5.000ns
  Data Path Delay:      5.355ns (Levels of Logic = 1)
  Clock Path Skew:      0.198ns (1.603 - 1.405)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[2]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X117Y109.AMUX  Tshcko                 0.357   i_GeneticAlg/Mut2CostWe
                                                        i_GeneticAlg/Mut2CostW
    SLICE_X74Y35.C2      net (fanout=11)        4.961   i_GeneticAlg/Mut2CostWei
    SLICE_X74Y35.CLK     Tas                    0.037   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/Mut2CostW
                                                        i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                          5.355ns (0.394ns logic, 4.961ns
                                                           (7.4% logic, 92.6% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.192ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[5]_im_4 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[1][5
  Requirement:          5.000ns
  Data Path Delay:      5.041ns (Levels of Logic = 1)
  Clock Path Skew:      -0.116ns (1.308 - 1.424)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[5]_im
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                          Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X111Y101.AQ    Tcko                  0.283   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X43Y142.A1     net (fanout=11)       4.721   i_GeneticAlg/Mut2CostWei
    SLICE_X43Y142.CLK    Tas                   0.037   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/Mut2CostW
                                                       i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ----------------------
    Total                                      5.041ns (0.320ns logic, 4.721ns
                                                       (6.3% logic, 93.7% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.188ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.853ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y123.B6     net (fanout=2304)     4.075   i_GeneticAlg/i_SerialCos
    SLICE_X62Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ----------------------
    Total                                      4.853ns (0.508ns logic, 4.345ns
                                                       (10.5% logic, 89.5% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.188ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.137ns (Levels of Logic = 1)
  Clock Path Skew:      -0.016ns (0.971 - 0.987)
```

```
  Source Clock:          Clk_BUFGP rising at 0.000ns
  Destination Clock:     Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:     0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y15.A22      net (fanout=32)       0.467   i_GeneticAlg/i_SerialCos
    DSP48_X0Y15.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.137ns (3.356ns logic, 1.781ns
                                                       (65.3% logic, 34.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.188ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.137ns (Levels of Logic = 1)
  Clock Path Skew:      -0.016ns (0.971 - 0.987)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y15.A21      net (fanout=32)       0.467   i_GeneticAlg/i_SerialCos
```

```
    DSP48_X0Y15.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                              5.137ns (3.356ns logic, 1.781ns
                                                               (65.3% logic, 34.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.188ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.137ns (Levels of Logic = 1)
  Clock Path Skew:      -0.016ns (0.971 - 0.987)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X53Y37.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5      net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y15.A23      net (fanout=32)       0.467   i_GeneticAlg/i_SerialCos
    DSP48_X0Y15.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                              5.137ns (3.356ns logic, 1.781ns
                                                               (65.3% logic, 34.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.188ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      5.137ns (Levels of Logic = 1)
  Clock Path Skew:      -0.016ns (0.971 - 0.987)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):        0.000ns
    Phase Error (PE):            0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X53Y37.BQ       Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X13Y39.C5       net (fanout=2)        1.314   i_GeneticAlg/i_SerialCos
    SLICE_X13Y39.C        Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    DSP48_X0Y15.A20       net (fanout=32)       0.467   i_GeneticAlg/i_SerialCos
    DSP48_X0Y15.CLK       Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                       5.137ns (3.356ns logic, 1.781ns
                                                         (65.3% logic, 34.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.187ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[9].
  Requirement:          5.000ns
  Data Path Delay:      5.243ns (Levels of Logic = 2)
  Clock Path Skew:      0.091ns (1.505 - 1.414)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X46Y89.AQ       Tcko                  0.322   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X46Y83.A5       net (fanout=10)       0.817   i_GeneticAlg/i_SerialCos
    SLICE_X46Y83.A        Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    SLICE_X46Y83.B5       net (fanout=3)        0.275   i_GeneticAlg/i_SerialCos
    SLICE_X46Y83.B        Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    DSP48_X3Y30.A6        net (fanout=2)        0.695   i_GeneticAlg/i_SerialCos
    DSP48_X3Y30.CLK       Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                         i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                       5.243ns (3.456ns logic, 1.787ns
```

(65.9% logic, 34.1% ro

Slack (setup path): -0.186ns (requirement - (data path - clock path skew + u
Source: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
Destination: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
Requirement: 5.000ns
Data Path Delay: 4.851ns (Levels of Logic = 2)
Clock Path Skew: -0.300ns (1.373 - 1.673)
Source Clock: Clk_BUFGP rising at 0.000ns
Destination Clock: Clk_BUFGP rising at 5.000ns
Clock Uncertainty: 0.035ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.070ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
SLICE_X62Y34.BQ	Tcko	0.283	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC
SLICE_X62Y34.C4	net (fanout=5)	0.270	i_GeneticAlg/i_SerialCos
SLICE_X62Y34.CMUX	Tilo	0.168	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC
SLICE_X62Y123.C6	net (fanout=2304)	4.070	i_GeneticAlg/i_SerialCos
SLICE_X62Y123.CLK	Tas	0.060	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC i_GeneticAlg/i_SerialC
Total		4.851ns	(0.511ns logic, 4.340ns (10.5% logic, 89.5% ro

---

Slack (setup path): -0.186ns (requirement - (data path - clock path skew + u
Source: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
Destination: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
Requirement: 5.000ns
Data Path Delay: 5.154ns (Levels of Logic = 2)
Clock Path Skew: 0.003ns (1.489 - 1.486)
Source Clock: Clk_BUFGP rising at 0.000ns
Destination Clock: Clk_BUFGP rising at 5.000ns
Clock Uncertainty: 0.035ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.070ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

```
  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X72Y76.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X73Y77.C3      net (fanout=4)        0.417   i_GeneticAlg/i_SerialCos
    SLICE_X73Y77.CMUX    Tilo                  0.163   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X93Y37.B2      net (fanout=2304)     4.234   i_GeneticAlg/i_SerialCos
    SLICE_X93Y37.CLK     Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.154ns (0.503ns logic, 4.651ns
                                                       (9.8% logic, 90.2% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.185ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[1]_re_9 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[0][1
  Requirement:          5.000ns
  Data Path Delay:      5.196ns (Levels of Logic = 0)
  Clock Path Skew:      0.046ns (1.494 - 1.448)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[1]_re
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X102Y105.BQ    Tcko                  0.322   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/Mut2CostW
    SLICE_X80Y63.CX      net (fanout=11)       4.858   i_GeneticAlg/Mut2CostWei
    SLICE_X80Y63.CLK     Tdick                 0.016   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.196ns (0.338ns logic, 4.858ns
                                                       (6.5% logic, 93.5% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.180ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].1
  Requirement:          5.000ns
  Data Path Delay:      5.216ns (Levels of Logic = 1)
```

```
  Clock Path Skew:      0.071ns (1.484 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A21      net (fanout=32)       0.373   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                      5.216ns (3.356ns logic, 1.860ns
                                                       (64.3% logic, 35.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.180ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/DataValidVector_6 (FF
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[6].
  Requirement:          5.000ns
  Data Path Delay:      5.255ns (Levels of Logic = 1)
  Clock Path Skew:      0.110ns (1.580 - 1.470)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/D
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X67Y110.AQ     Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X27Y51.C5      net (fanout=2307)     2.888   i_GeneticAlg/i_SerialCos
    SLICE_X27Y51.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
```

```
    DSP48_X1Y3.CEA2      net (fanout=77)       1.857   i_GeneticAlg/i_SerialCos
    DSP48_X1Y3.CLK       Tdspdck_CEA_AREG      0.166   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.255ns (0.510ns logic, 4.745ns
                                                       (9.7% logic, 90.3% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.180ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.845ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.B6     net (fanout=2304)     4.067   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.057   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      4.845ns (0.508ns logic, 4.337ns
                                                       (10.5% logic, 89.5% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.180ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.216ns (Levels of Logic = 1)
  Clock Path Skew:      0.071ns (1.484 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A20      net (fanout=32)       0.373   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.216ns (3.356ns logic, 1.860ns
                                                       (64.3% logic, 35.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.180ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.216ns (Levels of Logic = 1)
  Clock Path Skew:      0.071ns (1.484 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A23      net (fanout=32)       0.373   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ---------------------
    Total                                      5.216ns (3.356ns logic, 1.860ns
                                                       (64.3% logic, 35.7% ro
```

```
--------------------------------------------------------------------------------
Slack (setup path):     -0.180ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[1].
  Requirement:          5.000ns
  Data Path Delay:      5.216ns (Levels of Logic = 1)
  Clock Path Skew:      0.071ns (1.484 - 1.413)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y94.AQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X11Y65.C4      net (fanout=3)        1.487   i_GeneticAlg/i_SerialCos
    SLICE_X11Y65.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X0Y25.A22      net (fanout=32)       0.373   i_GeneticAlg/i_SerialCos
    DSP48_X0Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.216ns (3.356ns logic, 1.860ns
                                                       (64.3% logic, 35.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.179ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[3]_re_9 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[5][1
  Requirement:          5.000ns
  Data Path Delay:      5.246ns (Levels of Logic = 0)
  Clock Path Skew:      0.102ns (1.546 - 1.444)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[3]_re
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                          Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X108Y118.BMUX  Tshcko                 0.396    i_GeneticAlg/Mut2CostWe
                                                          i_GeneticAlg/Mut2CostW
    SLICE_X51Y36.BX      net (fanout=11)        4.834    i_GeneticAlg/Mut2CostWei
    SLICE_X51Y36.CLK     Tdick                  0.016    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                       5.246ns (0.412ns logic, 4.834ns
                                                          (7.9% logic, 92.1% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.179ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/Mut2CostWeights2[5]_im_6 (FF)
  Destination:          i_GeneticAlg/i_SerialCostFunction/InputVectorWArray[1][5
  Requirement:          5.000ns
  Data Path Delay:      5.028ns (Levels of Logic = 1)
  Clock Path Skew:      -0.116ns (1.308 - 1.424)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/Mut2CostWeights2[5]_im
    Location             Delay type         Delay(ns)  Physical Resource
                                                          Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X111Y101.CQ    Tcko                  0.283    i_GeneticAlg/Mut2CostWe
                                                          i_GeneticAlg/Mut2CostW
    SLICE_X43Y142.C2     net (fanout=11)       4.708    i_GeneticAlg/Mut2CostWei
    SLICE_X43Y142.CLK    Tas                   0.037    i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/Mut2CostW
                                                          i_GeneticAlg/i_SerialC
    ----------------------------------------------------  -------------------
    Total                                      5.028ns (0.320ns logic, 4.708ns
                                                          (6.4% logic, 93.6% rou

--------------------------------------------------------------------------------
Slack (setup path):     -0.179ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[3].
  Requirement:          5.000ns
  Data Path Delay:      5.134ns (Levels of Logic = 2)
  Clock Path Skew:      -0.010ns (0.957 - 0.967)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns
```

```
  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X104Y111.AQ    Tcko                  0.322   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X104Y116.A5    net (fanout=10)       0.853   i_GeneticAlg/i_SerialCos
    SLICE_X104Y116.A     Tilo                  0.061   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/i_SerialC
    SLICE_X105Y117.A5    net (fanout=3)        0.388   i_GeneticAlg/i_SerialCos
    SLICE_X105Y117.A     Tilo                  0.061   i_GeneticAlg/Mut2CostWe
                                                       i_GeneticAlg/i_SerialC
    DSP48_X5Y47.A8       net (fanout=2)        0.437   i_GeneticAlg/i_SerialCos
    DSP48_X5Y47.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  ---------------------
    Total                                      5.134ns (3.456ns logic, 1.678ns
                                                       (67.3% logic, 32.7% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.179ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[5].
  Requirement:          5.000ns
  Data Path Delay:      4.844ns (Levels of Logic = 2)
  Clock Path Skew:      -0.300ns (1.373 - 1.673)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X62Y34.BQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X62Y34.C4      net (fanout=5)        0.270   i_GeneticAlg/i_SerialCos
    SLICE_X62Y34.CMUX    Tilo                  0.168   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X63Y123.C6     net (fanout=2304)     4.063   i_GeneticAlg/i_SerialCos
    SLICE_X63Y123.CLK    Tas                   0.060   i_GeneticAlg/i_SerialCo
```

```
                                                          i_GeneticAlg/i_SerialC
                                                          i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ----------------------
    Total                                          4.844ns (0.511ns logic, 4.333ns
                                                           (10.5% logic, 89.5% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.178ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.104ns (Levels of Logic = 1)
  Clock Path Skew:      -0.039ns (0.970 - 1.009)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X63Y48.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X53Y59.C1      net (fanout=4)        1.266   i_GeneticAlg/i_SerialCos
    SLICE_X53Y59.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A12      net (fanout=32)       0.482   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.104ns (3.356ns logic, 1.748ns
                                                       (65.8% logic, 34.2% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.178ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.104ns (Levels of Logic = 1)
  Clock Path Skew:      -0.039ns (0.970 - 1.009)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
```

```
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X63Y48.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X53Y59.C1      net (fanout=4)        1.266   i_GeneticAlg/i_SerialCos
    SLICE_X53Y59.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A15      net (fanout=32)       0.482   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.104ns (3.356ns logic, 1.748ns
                                                       (65.8% logic, 34.2% ro

--------------------------------------------------------------------------------
Slack (setup path):     -0.178ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.104ns (Levels of Logic = 1)
  Clock Path Skew:      -0.039ns (0.970 - 1.009)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    SLICE_X63Y48.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X53Y59.C1      net (fanout=4)        1.266   i_GeneticAlg/i_SerialCos
    SLICE_X53Y59.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A13      net (fanout=32)       0.482   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      5.104ns (3.356ns logic, 1.748ns
                                                       (65.8% logic, 34.2% ro

--------------------------------------------------------------------------------
```

```
Slack (setup path):     -0.178ns (requirement - (data path - clock path skew + u
  Source:               i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[0].
  Requirement:          5.000ns
  Data Path Delay:      5.104ns (Levels of Logic = 1)
  Clock Path Skew:      -0.039ns (0.970 - 1.009)
  Source Clock:         Clk_BUFGP rising at 0.000ns
  Destination Clock:    Clk_BUFGP rising at 5.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: i_GeneticAlg/i_SerialCostFunction/C
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X63Y48.DQ      Tcko                  0.283   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    SLICE_X53Y59.C1      net (fanout=4)        1.266   i_GeneticAlg/i_SerialCos
    SLICE_X53Y59.C       Tilo                  0.061   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    DSP48_X3Y25.A14      net (fanout=32)       0.482   i_GeneticAlg/i_SerialCos
    DSP48_X3Y25.CLK      Tdspdck_A_PREG_MULT   3.012   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                      5.104ns (3.356ns logic, 1.748ns
                                                       (65.8% logic, 34.2% ro

--------------------------------------------------------------------------------

================================================================================
Timing constraint: PATH "TS_InputShiftReg_path" TIG;
 37399 paths analyzed, 31805 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
--------------------------------------------------------------------------------

================================================================================
Timing constraint: TS_Correlation = MAXDELAY FROM TIMEGRP "TG_Correlation" 15 n
For more information, see From:To (Multicycle) Analysis in the Timing Closure U
 720 paths analyzed, 720 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Maximum delay is   7.481ns.
--------------------------------------------------------------------------------

================================================================================
Timing constraint: Unconstrained OFFSET IN BEFORE analysis for clock "Clk_BUFGP"
 57017 paths analyzed, 54191 endpoints analyzed, 0 failing endpoints
 0 timing errors detected.
 Minimum allowable offset is  21.568ns.
```

```
--------------------------------------------------------------------------------

Hold Paths: Unconstrained OFFSET IN BEFORE analysis for clock "Clk_BUFGP"

--------------------------------------------------------------------------------
Offset (hold paths):    -1.573ns (data path - clock path + uncertainty)
  Source:               Rst_n (PAD)
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[2].
  Destination Clock:    Clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.238ns (Levels of Logic = 1)
  Clock Path Delay:     2.836ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AB7.I                Tiopi                0.630   Rst_n
                                                       Rst_n
                                                       Rst_n_IBUF
    SLICE_X88Y154.CE     net (fanout=7180)    0.599   Rst_n_IBUF
    SLICE_X88Y154.CLK    Tckce       (-Th)    -0.009   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                     1.238ns (0.639ns logic, 0.599ns
                                                       (51.6% logic, 48.4% ro

  Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF10.I               Tiopi                0.673   Clk
                                                       Clk
                                                       Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.528   Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.079   Clk_BUFGP/BUFG
                                                       Clk_BUFGP/BUFG
    SLICE_X88Y154.CLK    net (fanout=12747)   1.556   Clk_BUFGP
    -------------------------------------------------  -------------------
    Total                                     2.836ns (0.752ns logic, 2.084ns
                                                       (26.5% logic, 73.5% ro

--------------------------------------------------------------------------------
Offset (hold paths):    -1.573ns (data path - clock path + uncertainty)
  Source:               Rst_n (PAD)
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[2].
  Destination Clock:    Clk_BUFGP rising at 0.000ns
```

```
  Data Path Delay:      1.238ns (Levels of Logic = 1)
  Clock Path Delay:     2.836ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AB7.I                Tiopi                0.630   Rst_n
                                                       Rst_n
                                                       Rst_n_IBUF
    SLICE_X88Y154.CE     net (fanout=7180)    0.599   Rst_n_IBUF
    SLICE_X88Y154.CLK    Tckce       (-Th)    -0.009   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                     1.238ns (0.639ns logic, 0.599ns
                                                       (51.6% logic, 48.4% ro

  Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF10.I               Tiopi                0.673   Clk
                                                       Clk
                                                       Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.528   Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.079   Clk_BUFGP/BUFG
                                                       Clk_BUFGP/BUFG
    SLICE_X88Y154.CLK    net (fanout=12747)   1.556   Clk_BUFGP
    -------------------------------------------------  -------------------
    Total                                     2.836ns (0.752ns logic, 2.084ns
                                                       (26.5% logic, 73.5% ro

--------------------------------------------------------------------------------
Offset (hold paths):    -1.573ns (data path - clock path + uncertainty)
  Source:               Rst_n (PAD)
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[2].
  Destination Clock:    Clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.238ns (Levels of Logic = 1)
  Clock Path Delay:     2.836ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
AB7.I	Tiopi	0.630	Rst_n Rst_n Rst_n_IBUF
SLICE_X88Y154.CE	net (fanout=7180)	0.599	Rst_n_IBUF
SLICE_X88Y154.CLK	Tckce (-Th)	-0.009	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC
Total		1.238ns	(0.639ns logic, 0.599ns (51.6% logic, 48.4% ro

Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
AF10.I	Tiopi	0.673	Clk Clk Clk_BUFGP/IBUFG
BUFGCTRL_X0Y0.I0	net (fanout=1)	0.528	Clk_BUFGP/IBUFG
BUFGCTRL_X0Y0.O	Tbgcko_O	0.079	Clk_BUFGP/BUFG Clk_BUFGP/BUFG
SLICE_X88Y154.CLK	net (fanout=12747)	1.556	Clk_BUFGP
Total		2.836ns	(0.752ns logic, 2.084ns (26.5% logic, 73.5% ro

---

Offset (hold paths): -1.573ns (data path - clock path + uncertainty)
  Source: Rst_n (PAD)
  Destination: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[2].
  Destination Clock: Clk_BUFGP rising at 0.000ns
  Data Path Delay: 1.238ns (Levels of Logic = 1)
  Clock Path Delay: 2.836ns (Levels of Logic = 2)
  Clock Uncertainty: 0.025ns

  Clock Uncertainty: 0.025ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ): 0.050ns
    Total Input Jitter (TIJ): 0.000ns
    Discrete Jitter (DJ): 0.000ns
    Phase Error (PE): 0.000ns

Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
AB7.I	Tiopi	0.630	Rst_n Rst_n Rst_n_IBUF
SLICE_X88Y154.CE	net (fanout=7180)	0.599	Rst_n_IBUF

```
    SLICE_X88Y154.CLK     Tckce        (-Th)     -0.009   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ----------------------
    Total                                          1.238ns (0.639ns logic, 0.599ns
                                                           (51.6% logic, 48.4% ro

  Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
    ----------------------------------------------------  -------------------
    AF10.I                Tiopi                 0.673   Clk
                                                          Clk
                                                          Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0      net (fanout=1)        0.528   Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O       Tbgcko_O              0.079   Clk_BUFGP/BUFG
                                                          Clk_BUFGP/BUFG
    SLICE_X88Y154.CLK     net (fanout=12747)    1.556   Clk_BUFGP
    ----------------------------------------------------  ----------------------
    Total                                          2.836ns (0.752ns logic, 2.084ns
                                                           (26.5% logic, 73.5% ro

--------------------------------------------------------------------------------
Offset (hold paths):    -1.563ns (data path - clock path + uncertainty)
  Source:               Rst_n (PAD)
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[8].i
  Destination Clock:    Clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.248ns (Levels of Logic = 1)
  Clock Path Delay:     2.836ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
    ----------------------------------------------------  -------------------
    AB7.I                 Tiopi                 0.630   Rst_n
                                                          Rst_n
                                                          Rst_n_IBUF
    SLICE_X90Y153.CE      net (fanout=7180)     0.596   Rst_n_IBUF
    SLICE_X90Y153.CLK     Tckce        (-Th)    -0.022   i_GeneticAlg/i_SerialCo
                                                          i_GeneticAlg/i_SerialC
    ----------------------------------------------------  ----------------------
    Total                                          1.248ns (0.652ns logic, 0.596ns
                                                           (52.2% logic, 47.8% ro

  Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
```

```
    ---------------------------------------------------  ------------------
    AF10.I                Tiopi                   0.673   Clk
                                                          Clk
                                                          Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0      net (fanout=1)        0.528   Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O       Tbgcko_O              0.079   Clk_BUFGP/BUFG
                                                          Clk_BUFGP/BUFG
    SLICE_X90Y153.CLK     net (fanout=12747)    1.556   Clk_BUFGP
    ---------------------------------------------------  ----------------------
    Total                                       2.836ns (0.752ns logic, 2.084ns
                                                          (26.5% logic, 73.5% ro

--------------------------------------------------------------------------------
Offset (hold paths):    -1.563ns (data path - clock path + uncertainty)
  Source:               Rst_n (PAD)
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[8].
  Destination Clock:    Clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.248ns (Levels of Logic = 1)
  Clock Path Delay:     2.836ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF
    Location              Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ---------------------------------------------------  ------------------
    AB7.I                 Tiopi                 0.630   Rst_n
                                                        Rst_n
                                                        Rst_n_IBUF
    SLICE_X91Y153.CE      net (fanout=7180)     0.596   Rst_n_IBUF
    SLICE_X91Y153.CLK     Tckce       (-Th)    -0.022   i_GeneticAlg/i_SerialCo
                                                        i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                       1.248ns (0.652ns logic, 0.596ns
                                                        (52.2% logic, 47.8% ro

  Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu
    Location              Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ---------------------------------------------------  ------------------
    AF10.I                Tiopi                 0.673   Clk
                                                        Clk
                                                        Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0      net (fanout=1)        0.528   Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O       Tbgcko_O              0.079   Clk_BUFGP/BUFG
                                                        Clk_BUFGP/BUFG
    SLICE_X91Y153.CLK     net (fanout=12747)    1.556   Clk_BUFGP
    ---------------------------------------------------  ----------------------
```

```
    Total                                          2.836ns (0.752ns logic, 2.084ns
                                                           (26.5% logic, 73.5% ro

--------------------------------------------------------------------------------
Offset (hold paths):    -1.563ns (data path - clock path + uncertainty)
  Source:               Rst_n (PAD)
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[8].:
  Destination Clock:    Clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.248ns (Levels of Logic = 1)
  Clock Path Delay:     2.836ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AB7.I                Tiopi                0.630   Rst_n
                                                       Rst_n
                                                       Rst_n_IBUF
    SLICE_X91Y153.CE     net (fanout=7180)    0.596   Rst_n_IBUF
    SLICE_X91Y153.CLK    Tckce       (-Th)    -0.022  i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    -------------------------------------------------  -------------------
    Total                                     1.248ns (0.652ns logic, 0.596ns
                                                      (52.2% logic, 47.8% ro

  Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF10.I               Tiopi                0.673   Clk
                                                       Clk
                                                       Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.528   Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.079   Clk_BUFGP/BUFG
                                                       Clk_BUFGP/BUFG
    SLICE_X91Y153.CLK    net (fanout=12747)   1.556   Clk_BUFGP
    -------------------------------------------------  -------------------
    Total                                     2.836ns (0.752ns logic, 2.084ns
                                                      (26.5% logic, 73.5% ro

--------------------------------------------------------------------------------
Offset (hold paths):    -1.563ns (data path - clock path + uncertainty)
  Source:               Rst_n (PAD)
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[8].:
  Destination Clock:    Clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.248ns (Levels of Logic = 1)
```

```
  Clock Path Delay:     2.836ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    AB7.I                Tiopi                 0.630   Rst_n
                                                       Rst_n
                                                       Rst_n_IBUF
    SLICE_X90Y153.CE     net (fanout=7180)     0.596   Rst_n_IBUF
    SLICE_X90Y153.CLK    Tckce       (-Th)    -0.022   i_GeneticAlg/i_SerialCo
                                                       i_GeneticAlg/i_SerialC
    ---------------------------------------------------  -------------------
    Total                                      1.248ns (0.652ns logic, 0.596ns
                                                       (52.2% logic, 47.8% ro

  Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    AF10.I               Tiopi                 0.673   Clk
                                                       Clk
                                                       Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)        0.528   Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O              0.079   Clk_BUFGP/BUFG
                                                       Clk_BUFGP/BUFG
    SLICE_X90Y153.CLK    net (fanout=12747)    1.556   Clk_BUFGP
    ---------------------------------------------------  -------------------
    Total                                      2.836ns (0.752ns logic, 2.084ns
                                                       (26.5% logic, 73.5% ro

--------------------------------------------------------------------------------
Offset (hold paths):    -1.563ns (data path - clock path + uncertainty)
  Source:               Rst_n (PAD)
  Destination:          i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[8].i
  Destination Clock:    Clk_BUFGP rising at 0.000ns
  Data Path Delay:      1.248ns (Levels of Logic = 1)
  Clock Path Delay:     2.836ns (Levels of Logic = 2)
  Clock Uncertainty:    0.025ns

  Clock Uncertainty:          0.025ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns
```

Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
AB7.I	Tiopi	0.630	Rst_n Rst_n Rst_n_IBUF
SLICE_X90Y153.CE	net (fanout=7180)	0.596	Rst_n_IBUF
SLICE_X90Y153.CLK	Tckce (-Th)	-0.022	i_GeneticAlg/i_SerialCo i_GeneticAlg/i_SerialC
Total		1.248ns	(0.652ns logic, 0.596ns (52.2% logic, 47.8% ro

Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
AF10.I	Tiopi	0.673	Clk Clk Clk_BUFGP/IBUFG
BUFGCTRL_X0Y0.I0	net (fanout=1)	0.528	Clk_BUFGP/IBUFG
BUFGCTRL_X0Y0.O	Tbgcko_O	0.079	Clk_BUFGP/BUFG Clk_BUFGP/BUFG
SLICE_X90Y153.CLK	net (fanout=12747)	1.556	Clk_BUFGP
Total		2.836ns	(0.752ns logic, 2.084ns (26.5% logic, 73.5% ro

---

Offset (hold paths): -1.563ns (data path - clock path + uncertainty)
  Source: Rst_n (PAD)
  Destination: i_GeneticAlg/i_SerialCostFunction/CostFunctionCores[8].
  Destination Clock: Clk_BUFGP rising at 0.000ns
  Data Path Delay: 1.248ns (Levels of Logic = 1)
  Clock Path Delay: 2.836ns (Levels of Logic = 2)
  Clock Uncertainty: 0.025ns

  Clock Uncertainty: 0.025ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ): 0.050ns
    Total Input Jitter (TIJ): 0.000ns
    Discrete Jitter (DJ): 0.000ns
    Phase Error (PE): 0.000ns

Minimum Data Path at Slow Process Corner: Rst_n to i_GeneticAlg/i_SerialCostF

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
AB7.I	Tiopi	0.630	Rst_n Rst_n Rst_n_IBUF
SLICE_X90Y153.CE	net (fanout=7180)	0.596	Rst_n_IBUF
SLICE_X90Y153.CLK	Tckce (-Th)	-0.022	i_GeneticAlg/i_SerialCo

```
                                                          i_GeneticAlg/i_SerialC
    ---------------------------------------------------  ----------------------
    Total                                          1.248ns (0.652ns logic, 0.596ns
                                                           (52.2% logic, 47.8% ro

  Maximum Clock Path at Slow Process Corner: Clk to i_GeneticAlg/i_SerialCostFu
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    AF10.I               Tiopi                0.673   Clk
                                                       Clk
                                                       Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.I0     net (fanout=1)       0.528   Clk_BUFGP/IBUFG
    BUFGCTRL_X0Y0.O      Tbgcko_O             0.079   Clk_BUFGP/BUFG
                                                       Clk_BUFGP/BUFG
    SLICE_X90Y153.CLK    net (fanout=12747)   1.556   Clk_BUFGP
    ---------------------------------------------------  ----------------------
    Total                                          2.836ns (0.752ns logic, 2.084ns
                                                           (26.5% logic, 73.5% ro

--------------------------------------------------------------------------------

==============================================================================
Timing constraint: Unconstrained OFFSET OUT AFTER analysis for clock "Clk_BUFGP'
 1 path analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected.
 Maximum allowable offset is   7.411ns.
--------------------------------------------------------------------------------

==============================================================================
Timing constraint: Unconstrained path analysis
 54297 paths analyzed, 54297 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Maximum delay is   3.073ns.
--------------------------------------------------------------------------------


1 constraint not met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock Clk
------------------+------------+------------+------------+------------+------
                  |Max Setup to|  Process   |Max Hold to |  Process   |
Source            | clk (edge) |   Corner   | clk (edge) |   Corner   |Interna
------------------+------------+------------+------------+------------+------
MutationRate<0><0>|    4.806(R)|      SLOW  |   -0.639(R)|      FAST  |Clk_BUF(
MutationRate<0><1>|    5.179(R)|      SLOW  |   -0.552(R)|      FAST  |Clk_BUF(
MutationRate<0><2>|    4.862(R)|      SLOW  |   -0.614(R)|      FAST  |Clk_BUF(
MutationRate<1><0>|    4.148(R)|      SLOW  |   -0.491(R)|      SLOW  |Clk_BUF(
```

```
MutationRate<1><1>|    4.078(R)|      SLOW  |   -0.401(R)|      SLOW  |Clk_BUF
MutationRate<1><2>|    3.679(R)|      SLOW  |   -0.411(R)|      SLOW  |Clk_BUF
MutationRate<2><0>|    4.939(R)|      SLOW  |   -0.573(R)|      FAST  |Clk_BUF
MutationRate<2><1>|    4.975(R)|      SLOW  |   -0.357(R)|      SLOW  |Clk_BUF
MutationRate<2><2>|    4.696(R)|      SLOW  |   -0.487(R)|      SLOW  |Clk_BUF
MutationRate<3><0>|    4.003(R)|      SLOW  |   -0.306(R)|      SLOW  |Clk_BUF
MutationRate<3><1>|    4.118(R)|      SLOW  |   -0.412(R)|      SLOW  |Clk_BUF
MutationRate<3><2>|    3.588(R)|      SLOW  |   -0.338(R)|      SLOW  |Clk_BUF
Rst_n             |   21.568(R)|      SLOW  |    1.623(R)|      SLOW  |Clk_BUF
------------------+------------+------------+------------+------------+------

Clock Clk to Pad
------------+-----------------+------------+-----------------+------------+--
            |Max (slowest) clk|  Process   |Min (fastest) clk|  Process   |
Destination |  (edge) to PAD  |   Corner   |  (edge) to PAD  |   Corner   |Inte
------------+-----------------+------------+-----------------+------------+--
OutWeightBit|         7.411(R)|      SLOW  |         3.762(R)|      FAST  |Clk
------------+-----------------+------------+-----------------+------------+--

Clock to Setup on destination clock Clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
Clk            |   10.139|         |         |         |
---------------+---------+---------+---------+---------+


Timing summary:
---------------

Timing errors: 428  Score: 66780  (Setup/Max: 66780, Hold: 0)

Constraints cover 620234 paths, 0 nets, and 220746 connections

Design statistics:
   Minimum period:   7.481ns   (Maximum frequency: 133.672MHz)
   Maximum combinational path delay:   3.073ns
   Maximum path delay from/to any node:   7.481ns
   Minimum input required time before clock:  21.568ns
   Maximum output delay after clock:   7.411ns


Analysis completed Fri Mar 27 12:47:10 2015
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Trace Settings:
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Trace Settings

Peak Memory Usage: 2026 MB
```