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Silicon Photonic Components: Characterization and Optimization of Fabrication

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Problem Description

The purpose of this project is to optimize the fabrication of silicon photonic components. To achieve low loss and high resolution, minimizing roughness and achieving high anisotropy will be prioritized. To keep down costs, a low number of processing steps is preferred, and as much of the process as possible will be performed in-house, altough outsourcing opportunities will be discussed based on the results.

The target material for processing is plasma enhanced chemical vapor deposition (PECVD) grown amorphous silicon on PECVD grown silicon oxide. However, processes will also be tested on monocrystalline silicon since commercially bought SOI is a highly relevant platform. Structuring will be performed using electron beam lithography (EBL) and inductively coupled plasma reactive ion etching (ICP-RIE). The structure quality will be evaluated visually using scanning electron microscopy (SEM).

The ultimate goal of this project is to manufacture a working silicon photonic waveguide and couple light through it. The waveguide should have a thickness of 220 nm and a width of 550 nm, as determined by Vigen[69]. This work will aid in later NTNU work with designing and fabricating a silicon photonic biosensor. All fabrication work will be performed at NTNU NanoLab, and coupling will be performed at the Department of Electronics and Telecommunications. The characterization setup will be constructed or adapted from existing setups, and will itself be characterized and tested.

Abstract

Photonics is the science of manipulating photons, and silicon photonics is the application of silicon as the optical medium. It leverages the vast body of knowledge about semiconductor manufacturing and the established use of infrared wavelengths in telecommunications to simplify design, manufacture and testing. It also promises a relatively smooth integration of electronics and photonics.

This work lays the foundation for further work with silicon photonics at NTNU. Starting with the bare silicon wafer, it explores the processing from scratch of the necessary materials and the nanostructuring of them to create devices. The entire process flow from the empty wafer to a device in the characterization lab is documented. Silicon-on-insulator wafers are grown using PECVD, and the film quality is evaluated. The wafers are patterned using EBL and etched with ICP-RIE.

The bulk of the work is the development of etching recipes that minimize sidewall roughness. Simultaneously, the lithographic parameters of dose and spatial dimensions are optimized. Two candidate etch recipes are identified and their weaknesses and strengths relative to each other are discussed.

Several mm long waveguides without discontinuities are fabricated, with features such as S-curves and racetrack resonators. These are characterized in an optical setup based on butt coupling with micrometer control of in- and out-coupling fibers, infrared imaging and a photodetector for quantitative measurement. The setup has been characterized and verified to work, however no coupling has been achieved. Suggestions for further work are outlined for the benefit of later researchers.

Sammendrag

Fotonikk er vitenskapen om å manipulere fotoner, og silisiumfotonikk er anvendelsen av silisium som optisk medium. Det utnytter den enorme mengden kunnskap om produksjon av halvledere og den veletablerte bruken av infrarøde bølgelengder i telekommunikasjon for å forenkle design, produksjon og testing. Det lover også en relativt enkel integrering av elektronikk og fotonikk.

Dette arbeidet legger grunnlaget for videre arbeid med silisiumfotonikk ved NTNU. Med utgangspunkt i en bar silisiumwafer utforsker den fra grunnen prosessering av nødvendige materialer og mikromaskinering av dem for å lage komponenter. Hele prosessen fra standard råvarer en enhet i karakteriseringsoppsettet er dokumentert. Silicon-on-isolator-wafere er grodd ved hjelp av PECVD, og filmens kvalitet blir vurdert. Wafere er strukturert med EBL og etset med ICP-RIE.

Utvikling av etseoppskrifter som minimerer sideveggsruhet utgjør mesteparten av arbeidet. Samtidig blir de litografiske parametrene dose og dimensjonering optimalisert. To spesielt interessante etseoppskrifter er identifisert og deres svakheter og styrker i forhold til hverandre blir diskutert.

Flere mm lange bølgeledere uten diskontinuiteter er fabrikert, med funksjoner som S-svinger og racetrackresonatorer. Disse er karakterisert ved et optisk oppsett basert på butt-kopling med mikrometerkontroll på inn- og ut-koblingsfiber, infrarød mikroskopi og en fotodetektor for kvantitative målinger av signal. Oppsettet har blitt karakterisert og det er bekreftet at det fungerer, men ingen kobling er oppnådd. Elementer av videre arbeid er foreslått for senere forskeres nytte.

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of Master of Science in Nanotechnology at the Department of Electronics and Telecommunications at the Norwegian University of Science and Technology. The experimental work described in this work was performed in cooperation between Jens Høvik and the author. The text of the thesis is entirely the work of the author.

Acknowledgements

I sincerely thank my supervisor professor Astrid Aksnes for her guidance in this project and for being available at all times and at short notice. She has coordinated the research efforts and involved department resources in a way that made everything a lot easier. She has also been extremely helpful in reviewing this thesis and has given helpful feedback on the smallest detail.

I extend my greatest thanks to my co-supervisor Jens Høvik who I have worked closely with on a near-daily basis. We have spent countless hours in the lab together, discussing results, throwing ideas back and forth and planning further experiments. He has also performed a number of the experiments that are part of this thesis, including a lot of etching and EDS imaging.

My other co-supervisor Kay Gastinger has also been of great help. I am grateful to him for sharing of his vast experience and asking the tough, critical questions along the way that helped us steer clear of mistakes and blind alleys. He has also helped form the structure of this thesis and made it more organized and coherent.

The very helpful engineers of NTNU NanoLab also deserve my thanks. Especially Espen Rogstad and Mark Chiappa have been most helpful in being available whenever there have been issues and with debugging problems with the processing. I also thank René Wolf, who substituted for Espen when he was on his paternity leave, and who shared his wisdom and experiences with thin film processing.

I extend my thanks to Tron Arne Nilsen for sharing his experiences with device processing and for helping Jens and me characterize the laser used in this work.

The Department of Electronics and Telecommunications' mechanical workshop receives my thanks for being service-minded, educational and efficient in constructing components for our optical test setup.

The Research Council of Norway is acknowledged for the support to NTNU NanoLab through the Norwegian Micro- and Nano-Fabrication Facility, NorFab (197411/V30).

I have not failed 10,000 times. I have successfully found 10,000 ways that will not work.

Thomas Edison

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Chapter 1

Introduction

1.1 Background

Photonics is the science of optics brought into the modern age. Whereas classical optics concerns itself with the wave nature of light, photonics started its life with Einstein's seminal 1905 paper on the photoelectric effect[22] wherein the quantization of light was predicted. With further developments of quantum mechanics and novel material phenomena such as semiconductivity, the way was paved for revolutionary devices such as the laser, LED, photodetector, optical fiber and LCD.

While electronics primarily works by moving around electrons which are massive particles by disturbing them with electric fields, photonics takes the opposite approach, maneuvering the electromagnetic field itself through an environment of electrons and nuclei. Sometimes it fuses with electronics by exciting semiconductors to higher energy levels or by exploiting quantum mechanical phenomena such as in the laser. The capabilities enabled by such technologies have increased the standard of living worldwide and has led the UN to declare 2015 the International Year of Light and Light Technologies[66].

Like with electronics, work is ongoing to push photonics further, and in particular there are being put in efforts to bring the two fields closer together. This takes place both spatially, bringing photonic and electronic components together on the same chip, and conceptually, having photonics perform the tasks currently in the realm of electronics[11].

In squeezing different technologies together on the same piece of silicon, the strategy of using the same fabrication process for both has been promising. This leverages the mature CMOS processes by allowing existing assembly lines to be used, reducing cost and complexity relative to purchasing new equipment and developing new processes. As modern electronics are fabricated in silicon, the silicon on insulator (SOI) platform has been developed.

SOI technology uses a regular silicon wafer as a structural bottom layer, coated with SiO_2 as an insulator and then with a thin silicon layer which is used as an optical medium. Silicon being a semiconductor with

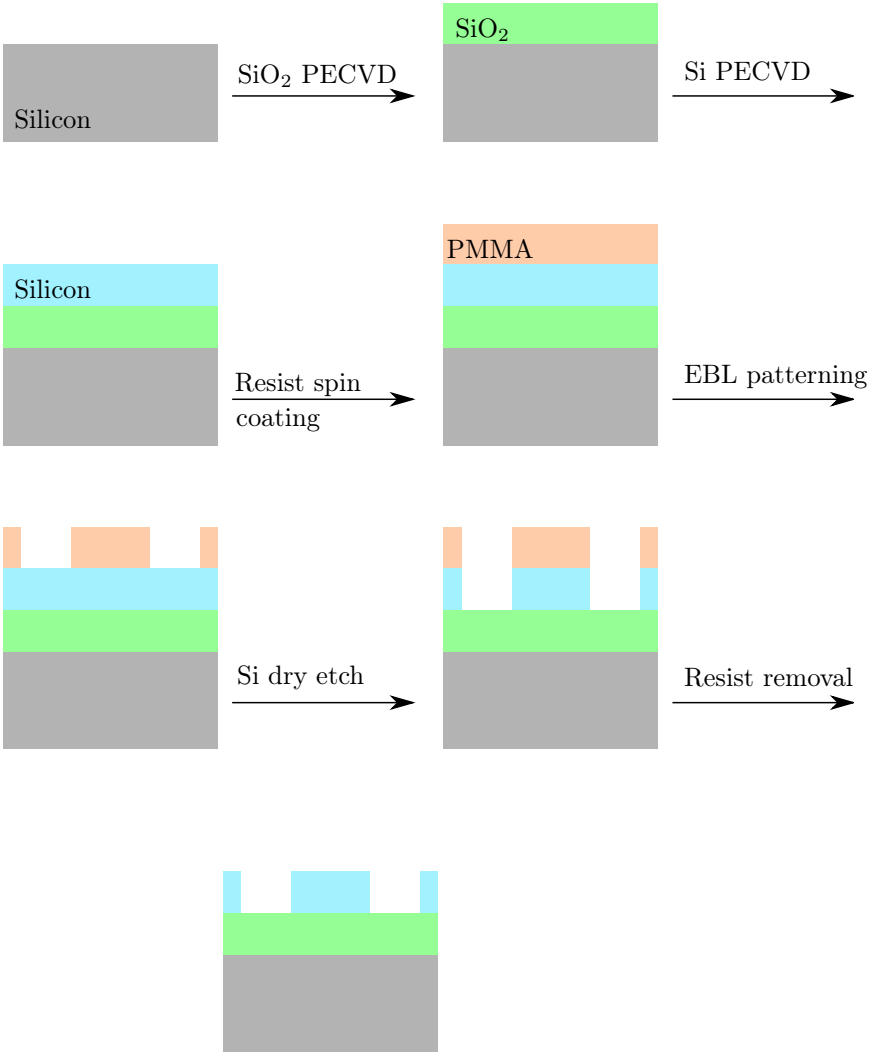


Figure 1.1: Sketch of the major steps in fabricating a waveguide on PECVD grown SOI. Dimensions not to scale.

a bandgap of 1.1 eV, it is necessary to use light with a wavelength longer than 1.13 µm in order to get any transmission. While this is a quite long wavelength which requires space, the high refractive index of silicon ensures a short effective wavelength and a high degree of confinement, which makes it possible to reduce the footprint of the devices. Conveniently, the 1550 nm wavelength is widely used in telecommunications applications, making existing equipment such as lasers and single-mode fibers plentiful and cheap.

Although a benefit of sharing the processing line with electronics is

that the two may be combined, silicon photonics has applications outside of computation and communication. This work supports an ongoing effort at NTNU to make a silicon photonic biosensor. Such devices promise rapid and sensitive detection of biomolecules in a very small disposable sensor that requires minute volumes of analyte[21, 71].

In this work, the devices will be fabricated using electron beam lithography and reactive ion etching. An overview of the fabrication process is given in Figure 1.1.

1.2 Previous Work

This work builds on several other master's theses written at NTNU's Department of Electronics and Telecommunications, supervised by Professor Astrid Aksnes. Importantly, Vigen's 2014 thesis Silisium Racetrack Resonator[69] has had a major impact on this thesis. Specifically, the specifications for the waveguide and resonator geometries are drawn from his work and theoretical considerations. Attempts will be made to replicate and improve on his work.

The master's theses of Bolstad[6], Lorvik[41] and Høvik[27] also built up to this project. However, they focus on photonic crystal structures, which is outside the scope of this work. Their work on fabrication has influenced this project and justified some of the choices made here.

In addition, the author draws on his experiences from his preliminary thesis[44], on the fabrication and characterization of plasmonic particles. The aforementioned work was to a great extent focused on EBL techniques, and the extensive experience gained from it caused large amounts of time to be saved on this project, as the lithography is by far the part of the cleanroom work that requires the most skill.

1.3 Thesis Overview

This thesis uses a variation on the AIBC (Abstract, Introduction, Body, Conclusion) method described by Burgess and Cargill[9].

This chapter gives a brief overview of the motivations for performing the work. This thesis contributes to an ongoing research effort at the Department of Electronics and Telecommunications, and research from this project and the previous work is presented.

Chapter 2 presents the theoretical basis for the work. It describes the optical waveguide devices that are to be built, without going into detail about the fabrication process. It also gives an introduction to the SOI platform.

Chapter 3 presents the experimental equipment that was used. This chapter was kept separate from the theory due to its focus on applications and methods. At the same time, it was kept separate from methods because of its scope and generality, and because no specific experimental procedures are presented.

Chapter 4 contains the bulk of the work. The experimental trials are described one by one, and the results are presented immediately after with short comments. This was deemed to be an appropriate way to format the thesis due to the nature of the task. This thesis is primarily an engineering effort performed incrementally. Each experiment is based on the previous, therefore it makes sense to present them sequentially, so that the motivation remains clear to the reader without having to cross-check back and forth between chapters

Chapter 5 sums up the results and compares them. The results are examined to look for cross-experimental trends and draw conclusions that are difficult to notice when analyzing each experiment individually. The effectiveness of the experimental approach will be evaluated. Furthermore, recommendations will be made to future researchers about methods that may produce better results.

Chapter 6 presents the most significant findings and makes recommendations for further work.

Appendix A contains the results from the laser characterization, in particular the tunability, spectral width and power.

Chapter 2

Theory

This chapter presents an overview of the underlying theory necessary to understand this work. It covers the physical basis of optical waveguides and explains some of the tools used in fabricating the samples. This is necessary in order to make the reasoning behind the choices made more apparent.

2.1 Waveguides

Electromagnetic Optics

Maxwell's equations[45] serve as the foundation of classical electromagnetics, and thus also for electromagnetic optics. This set of coupled differential equations states the relation between electric and magnetic fields in arbitrary media. These equations are very powerful and entirely classical, allowing for description of complex nanophotonic and plasmonic effects without resorting to quantum mechanics[43]. In the "macroscopic" form of the equations, they are stated as follows:

$$\nabla \cdot \boldsymbol{D} = \rho \tag{2.1}$$

$$\nabla \cdot \boldsymbol{B} = 0 \tag{2.2}$$

$$\nabla \times \boldsymbol{E} = -\frac{\partial \boldsymbol{B}}{\partial t} \tag{2.3}$$

$$\nabla \times \boldsymbol{H} = \boldsymbol{J} + \frac{\partial \boldsymbol{D}}{\partial t} \tag{2.4}$$

This formulation depends on the auxiliary fields $\boldsymbol{D}$ and $\boldsymbol{H}$, defined as

$$\boldsymbol{D} \equiv \epsilon \boldsymbol{E} = \epsilon_0 \boldsymbol{E} + \boldsymbol{P} \tag{2.5}$$

$$\boldsymbol{H} \equiv \frac{1}{\mu_0} \boldsymbol{B} - \boldsymbol{M} \tag{2.6}$$

Here $\boldsymbol{D}, \boldsymbol{E}, \boldsymbol{P}$ and $\boldsymbol{J}$ are the electric displacement, electric field, polarization and current density, and ϵ_0 and ρ the vacuum permittivity and charge density. Similarly, $\mathbf{H}$, $\mathbf{B}$ and $\mathbf{M}$ are the magnetic induction, magnetic field and magnetization, and μ_0 the vacuum permeability. In the general case, ϵ and μ are tensors, of the form

$$\bar{\bar{\epsilon}} = \begin{bmatrix} \epsilon_{xx} & \epsilon_{xy} & \epsilon_{xz} \\ \epsilon_{yx} & \epsilon_{yy} & \epsilon_{yz} \\ \epsilon_{zx} & \epsilon_{zy} & \epsilon_{zz} \end{bmatrix}. \tag{2.7}$$

The symmetry properties as described by Singh[60] will not be repeated here, except to mention that they will be the same as for the medium. This needs to be taken into consideration when working with uniaxial and biaxial materials as well as certain nanostructures[43]. However, as neither silicon, silicon oxide or amorphous materials in general fall into this category, the dielectric function will from here on be assumed to be scalar.

Magnetization and current will be neglected as we will not consider metallic materials, and Equations (2.3) and (2.4) can be rewritten. Using Equations (2.5) and (2.6) and setting $\mu = \mu_0$ and $\epsilon = \epsilon_0 n^2$, we arrive at the simpler form

$$\nabla \times \boldsymbol{E} = -\mu_0 \frac{\partial \boldsymbol{H}}{\partial t} \tag{2.8}$$

$$\nabla \times \boldsymbol{H} = \epsilon_0 n^2 \frac{\partial \boldsymbol{E}}{\partial t}. \tag{2.9}$$

These equations can be decomposed into two sets of coupled equations for linear polarized fields:

$$\begin{aligned} \frac{\partial E_y}{\partial x} - \frac{\partial E_x}{\partial y} &= -j\omega\mu_0 H_z \\ \frac{\partial H_z}{\partial y} + jkH_y &= j\omega\epsilon_0 n^2 E_x \\ -\frac{\partial H_z}{\partial x} + jkH_x &= j\omega\epsilon_0 n^2 E_y \end{aligned} \tag{2.10}$$

$$\begin{aligned} \frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} &= j\omega\epsilon_0 n^2 E_z \\ \frac{\partial E_z}{\partial y} + jkE_y &= -j\omega\mu_0 H_x \\ -\frac{\partial E_z}{\partial x} - jkE_x &= -j\omega\mu_0 H_y \end{aligned} \tag{2.11}$$

Now consider a plane wave of the form

$$\boldsymbol{E} = \boldsymbol{E}(x, y)e^{j(\omega t - kz)} \tag{2.12}$$

$$\boldsymbol{H} = \boldsymbol{H}(x, y)e^{j(\omega t - kz)}. \tag{2.13}$$

This wave, propagating through a waveguide as shown in Figure 2.1, can be viewed as a superposition of fields adhering to Equations (2.10) and (2.11). These have no electric or magnetic field respectively in the direction of propagation, and are termed transverse electric (TE) or transverse magnetic (TM) waves.

Planar-Mirror Waveguides

We will begin our discussion of waveguides by considering the simplest configuration, the planar-mirror waveguide. The reader with a background in quantum mechanics will note the similarities between the particle in box model and the planar-mirror waveguide, as opposed to the finite potential well and planar dielectric waveguide. In both quantum mechanics and photonics, the first scenario has a sinusoidal field distribution and complete confinement, while the other has less confinement and exponential decay outside the boundaries.

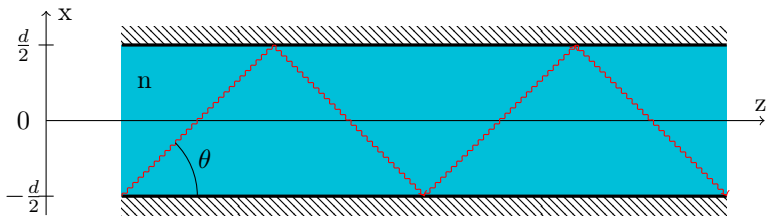


Figure 2.1: Schematic of a planar-mirror waveguide

The planar-mirror waveguide consists of two parallel, infinite planar mirrors enclosing a dielectric slab. A monochromatic plane wave, TE or TM, propagates along the slab at an angle θ, reflecting off of the mirrors as shown in Figure 2.1. It has wavelength $\lambda = \lambda_0/n$, wavenumber $k = nk_0$ and phase velocity $c = c_0/n$. With each reflection, the wave undergoes a phase shift π, ensuring that the net field at the dielectric-mirror interface exactly cancels itself.

Now consider waves that will reflect such that they retain their phase after exactly two reflections. Such waves will maintain the same transverse field distribution along the entire waveguide axis, and are called modes. It can be easily shown that for any given wavelength, this is only possible for a discrete set of bounce angles, given by

$$\theta_m = sin^{-1}\left(\frac{m\lambda}{2d}\right), m \in \mathbb{N}_{>0} \tag{2.14}$$

Requiring the argument of sin^{-1} to be less than 1, we find the number of modes M to be restricted:

$$M = \left\lfloor \frac{2d}{\lambda} \right\rfloor \tag{2.15}$$

The value enclosed by the $\lfloor\rfloor$ brackets is rounded down to the nearest integer. This leads to a cutoff wavelength of $\lambda_c = 2d$ for the planar-mirror waveguide, intuitively obvious by considering a wave in a cavity smaller than its wavelength.

As the bounce angle is never exactly zero, it is useful to vectorize the wave number. From simple trigonometric considerations and Equation (2.14), we obtain

$$k_{xm} = k\sin(\theta_m) = m\frac{\pi}{d} \tag{2.16}$$

$$k_{zm} = k\cos(\theta_m). \tag{2.17}$$

From Equation (2.16) it can be inferred that the modes propagate along the waveguide at different velocities. A convenient way to handle this is to introduce the propagation constant $\beta_m = k_z = k\cos\theta_m$. Furthermore, we introduce the effective index n_e:

$$n_e = \frac{\beta}{k_0} \tag{2.18}$$

Using Equation (2.14), we obtain the useful expression

$$\begin{aligned} \beta_m^2 &= k^2(0.5 - \sin^2\theta_m) \\ &= k^2 - \frac{m^2\pi^2}{d^2} \\ &= \frac{\omega^2}{c^2} - \frac{m^2\pi^2}{d^2}. \end{aligned} \tag{2.19}$$

This is also the dispersion relation for the system, as it links the frequency to the propagation constant.

The field distributions of the modes is obviously of great interest as well. Consider an upward-travelling wave $E_{y\uparrow} = A\exp(-jk_{xm}x - j\beta_m z)$ and a downward-travelling wave $E_{y\downarrow} = Ae^{j(m-1)\pi}\exp(+jk_{xm}x - j\beta_m z)$ interfering. The total field then becomes

$$E_y(x,z) = au_m(x)\exp(-j\beta_m z) \tag{2.20}$$

where

$$u_m(x) = \begin{cases} \sqrt{\frac{2}{d}}\cos(m\pi\frac{x}{d}), & \text{m odd} \\ \sqrt{\frac{2}{d}}\sin(m\pi\frac{x}{d}), & \text{m even.} \end{cases} \tag{2.21}$$

The field distributions of the lowest four modes is shown in Figure 2.2.

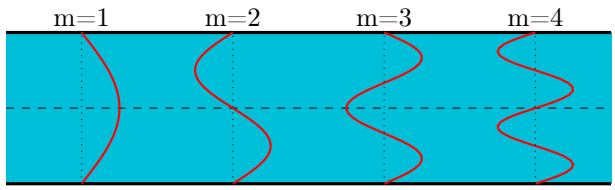


Figure 2.2: Field distributions of the lowest 4 modes of a planar-mirror waveguide.

Planar Dielectric Waveguides

The planar dielectric waveguide is a step away from the planar-mirror waveguide in terms of simplification. Introduced is a dielectric cladding layer in place of the top mirror, and a substrate material which may or may not be the same as the cladding[49]. The substrate and cladding must have refractive indices lower than that of the core, such that total internal reflection will occur. As will be seen, this change has consequences for the whole system. Here, n_s is the refractive index of the substrate, and n_0 and n_1 of the core and cladding, as in Figure 2.3.

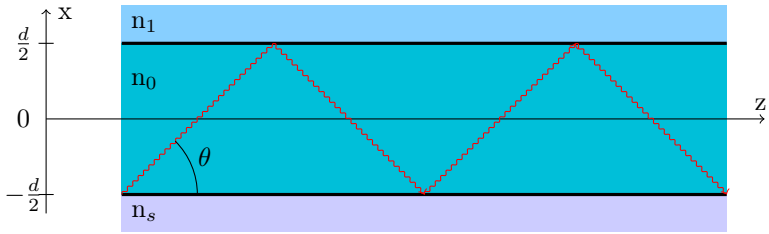


Figure 2.3: Schematic of a planar dielectric waveguide

Importantly, as can be derived using Fresnel's equations[57], the reflection coefficients become complex. This effects a phase change ϕ that unlike in the planar-mirror case is not necessarily π, and which is different for TE and TM modes.

$$\tan\frac{\phi_{TE}}{2} = \sqrt{\frac{\sin^2\overline{\theta}_c}{\sin^2\theta} - 1} \qquad \text{, TE} \tag{2.22}$$

$$\tan\frac{\phi_{TM}}{2} = \frac{-1}{\cos^2\overline{\theta}_c}\sqrt{\frac{\sin^2\overline{\theta}_c}{\sin^2\theta} - 1} \qquad \text{, TM} \tag{2.23}$$

Here, θ_c is the critical angle above which total internal reflection will occur, and $\overline{\theta_c}$ is its complementary angle,

$$\theta_c = \arcsin \frac{n_1}{n_0} \tag{2.24}$$

$$\overline{\theta_c} = 90° - \theta_c = \arccos \frac{n_1}{n_0}. \tag{2.25}$$

By convention θ_c is defined such that it is equal to 0 when perpendicular to the waveguide. By another convention θ, the bounce angle experienced by the light, is defined such that it is equal to 0 when parallel with the waveguide. For this reason, $\overline{\theta_c}$ is used in this work, in accordance with textbooks such as Fundamentals of Photonics[57].

The consequence of this phase difference is that the field at the boundary is no longer exactly 0. In order to fulfill Maxwell's equations, an evanescent (exponentially decaying) field appears in the cladding and substrate. The time averaged field distribution can then be described as[49]:

$$E_y = \begin{cases} A\cos\left(\kappa d/2 - \phi\right) e^{-\sigma(x-d/2)} & \text{, cladding} \\ A\cos\left(\kappa x - \phi\right) & \text{, core} \\ A\cos\left(\kappa d/2 + \phi\right) e^{-\xi(x+d/2)} & \text{, substrate} \end{cases} \tag{2.26}$$

It is important to note that ϕ in Equation (2.26) is not the same as in Equations (2.22) and (2.23), but rather a parameter that must be found independently. κ, σ and ξ are the wavenumbers along x inside the core, cladding and substrate.

$$\kappa = \sqrt{k^2 n_1^2 - \beta^2} \tag{2.27}$$

$$\sigma = \sqrt{\beta^2 - k^2 n_0^2} \tag{2.28}$$

$$\xi = \sqrt{\beta^2 - k^2 n_s^2} \tag{2.29}$$

Note that the above derivation only holds as long as the core has the highest refractive index. If this is not the case, the field distribution will be harmonic in the materials with lower refractive index, and the mode is radiative, not guided.

It is interesting to know how much of the total power is contained within the core relative to the cladding and substrate. This is called the power containment factor Γ_m, and is defined as

$$\Gamma_m = \frac{\int_{\text{core}} u_m^2(y)dy}{\int_{-\infty}^{\infty} u_m^2(y)dy}. \tag{2.30}$$

Importantly, the confinement factor increases for high-Δn systems and for lower-order modes[57].

The altered phase shift relative to planar-mirror waveguides implies that the bounce angles must change as well, in order to preserve self-consistency. In the relatively simple case of $n_s = n_0$, this can be demonstrated by requiring $\frac{\phi}{2} = \pi \frac{d}{\lambda} \sin(\theta) - m\frac{\pi}{2}$. This leads to the transcendent

Equations (2.31) and (2.32), and a graphical or numerical solution is necessary in order to find the allowed bounce angles. In the generalized case of $n_s \neq n_0$, the derivation is more complex[49] and will not be covered here.

$$\tan\left(\pi\frac{d}{\lambda}\sin(\theta_m) - m\frac{\pi}{2}\right) = \sqrt{\frac{\sin^2\overline{\theta}_c}{\sin^2\theta_m} - 1} \qquad \text{, TE} \tag{2.31}$$

$$\tan\left(\pi\frac{d}{\lambda}\sin(\theta_m) - m\frac{\pi}{2}\right) = \frac{-1}{\cos^2\overline{\theta}_c}\sqrt{\frac{\sin^2\overline{\theta}_c}{\sin^2\theta_m} - 1} \qquad \text{, TM} \tag{2.32}$$

While the number of TM modes is more complicated to calculate, the number of TE modes can easily be determined by assuming the highest-order mode to have a bounce angle $\theta_m \approx \overline{\theta}_c$, taking the inverse tangent and solving for m.

$$M = \left\lceil \frac{\sin\overline{\theta}_c 2d}{\lambda} \right\rceil \tag{2.33}$$

The $\lceil\rceil$ notation, similar to that of Equation (2.15), means that the number of modes must be rounded up to the nearest integer. Consequently, there will always be at least one legal mode in a planar dielectric waveguide.

Two-Dimensional Waveguides

In practice, most waveguides are designed to confine light in both the x and y directions, which is not possible for the planar geometries discussed above. This can be achieved using a number of different waveguide geometries, some of which are shown in Figure 2.4. While only strip, buried strip and ridge are relevant to the techniques used in this work, the optical fiber is included for completeness.

The strip and buried strip can be analyzed using Marcatili and Kumar's methods[49], which extend the methods used for planar mirror waveguides. However, these methods break down even for ridge waveguides, and it is necessary to use numerical methods to model these structures. This can be done using the finite element and finite difference methods, prominently featured in the COMSOL Multiphysics[1] software suite. The COMSOL software was used for designing the devices in this work[27].

Losses in Waveguides

The most widely discussed sources of loss in textbooks are those that plague optical fibers. These include Rayleigh scattering, which is on the order of 0.1 dB/km at 1550 nm in glass, and infrared absorption, on

[1] www.comsol.com

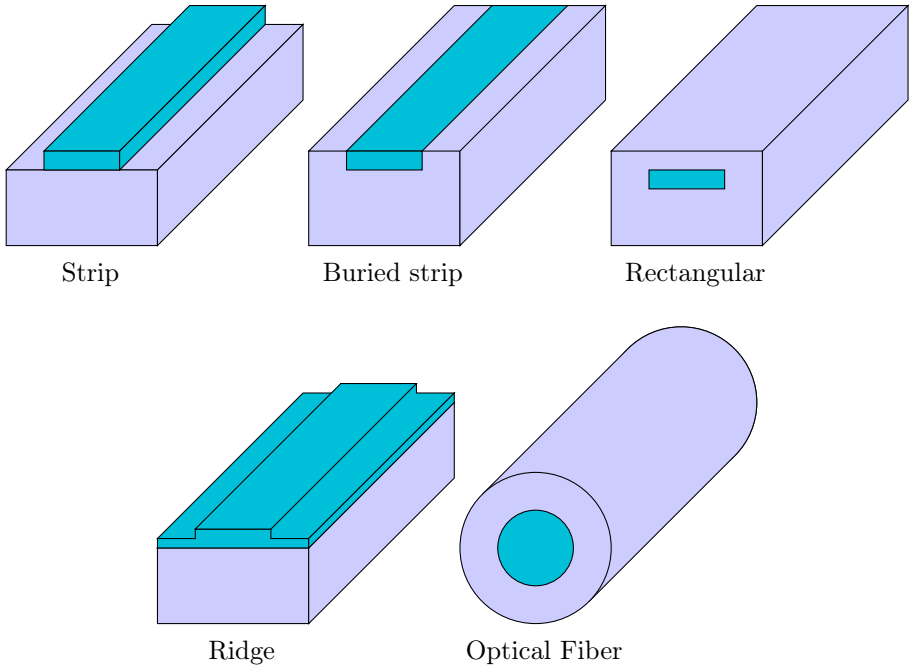


Figure 2.4: Five common 2-D waveguide geometries: Strip, buried strip, ridge, rectangular and fiber.

the same order, and in well-made silica glass fibers the losses add up to 0.15 dB/km[57].

However, scattering losses from impurities can be a serious issue. In the case of focused ion beam (FIB) milled waveguides, where a gallium beam selectively sputters away features, losses from implanted gallium atoms have been reported as high as thousands of dB/cm[17], far above what can be accepted for practical purposes. FIB typically uses acceleration voltages of up to 30 keV, however, and etching processes using lower voltage such as ICP-RIE routinely show significantly lower losses[56, 70]. Due to the lower energy of ICP-RIE, ion implantation is kept to a minimum.

Of greater concern are often scattering losses from the roughness of the waveguide itself. While sub-nm RMS roughness[53] can often be achieved on wafer surfaces following chemical-mechanical planarization, untreated PECVD grown films can be far rougher. Roughness of CVD grown films has been measured to 4 nm for 150 nm thick SiO_2, increasing for thicker films[65].

In addition to top and bottom interface roughness, the sidewall roughness of the device must not be neglected. Sidewall roughness usually arises in etching, and a great deal of effort has been put into managing it[39]. Roughness is especially problematic for thin and narrow waveguides due to low confinement leading to a stronger interaction with the rough surfaces

and sidewalls[34]. Below a width of 4 µm, transmission losses increase dramatically, reaching more than 30 dB/cm for an RMS sidewall roughness of 10 nm. However, a post-treatment of the waveguides has been shown to reduce the surface roughness to 2 nm, leading to losses of 0.8 dB/cm[35]. This procedure is based on growing an oxide layer using H_2O and O_2 at 1000 °C for 43 minutes, then stripping the oxide in HF.

2.2 Coupled Mode Theory

This section describes how an electromagnetic field can, by virtue of similarity with an allowed mode, feed power into the mode, potentially transferring itself completely to it. The central idea consists of expanding the source field $s(y)$ as a superposition of modes $u_m(y)$ and finding the amplitude of each mode[57]. Mathematically, this takes the form

$$s(y) = \sum_m a_m u_m(y) \tag{2.34}$$

$$a_m = \int_{-\infty}^{\infty} s(y) u_m(y) dy. \tag{2.35}$$

Input Coupling

The incident field can take many forms, such as a laser aimed at a waveguide facet, or a source waveguide positioned close enough to the receiving waveguide that the evanescent field overlaps the waveguide. The first case is known as butt coupling[57], and is a conceptually simple and common way to couple light into a waveguide.

Unfortunately, while the experimental setup needed for butt coupling can be very simple, achieving a high coupling coefficient can be difficult. This is mostly due to the typically very small dimensions of the waveguide core. There are in this scenario two options: Either, a tightly focused beam may be used, coupling a large amount of light into the waveguide if it hits at all. This requires great stability and precision[57], and is preferred in mass-produced setups such as fiber-to-fiber-couplers and integrated photonic devices. Figure 2.5 shows an example of a small spot not perfectly aligned with the waveguide.

The other option consists of using a larger spot, and accepting that only a fraction will excite a waveguide mode. However, when coupling into very small waveguides, the amount of accepted light may be miniscule, and it is often necessary to strike a balance between the two strategies. Furthermore, if the waveguide facet is not perfectly flat or is tilted relative to the beam, large amounts of light can be scattered. Facet quality can be ensured by polishing[28] or milling with routers[2].

Other methods for guiding light into a small device include prism coupling and grating coupling[57]. These are side coupling techniques, based on introducing the light at an angle. In prism coupling, the light undergoes total internal reflection at the bottom of the prism, which is separated by a short distance from the waveguide. The evanescent tail then couples into the waveguide. The grating coupling is based on diffracting the beam such that one diffracted component will couple into a mode.

The problem of coupling into a very small waveguide can be addressed by using a tapered waveguide[63]. The incident light now enters a large target, which then progressively narrows down to the smaller waveguide. While the wide end of the taper is massively multi-mode, the slow taper

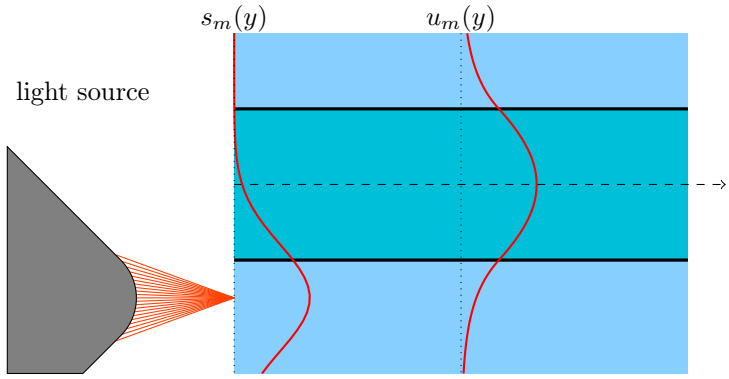


Figure 2.5: Power distributions of the exciting and excited modes in a waveguide, demonstrating the difficulties of aligning the light source.

forces the light to couple into lower-order modes. Some loss is always inherent in this process, but with properly designed tapers, even short tapers can achieve almost 100% transmission[23].

Coupled Waveguides

Another useful application of coupled modes is transferring power between adjacent waveguides. This can be used for splitting beams, feeding light into resonators or making switches by combination with electro-optical media between the waveguides[57]. A stringent analysis would be based on finding the allowed modes for the two-waveguide system as a whole. However, even in the planar case with a completely straight coupling region, considering fields in five distinct regions is a complicated process beyond the scope of this thesis. For weakly coupled waveguides, a perturbation theory based approach as in Equation (2.35) is sufficient[57], and for more complex cases software simulations will be necessary.

In a system as shown in Figure 2.6, the waveguides are identical. This is important because it means that the upper and lower modes have the same wavenumber, and are then said to be phase matched. This minimizes destructive interference, and allows the incoming mode to couple completely into the other after the coupling distance L_0[57]. If the waveguides remain adjacent, the intensity distribution will continue to switch between the two modes periodically.

This may be justified by considering two odd and even hybrid modes,

$$u_o = (u_u - u_l)/2 \tag{2.36}$$
$$u_e = (u_u + u_l)/2. \tag{2.37}$$

It obviously follows that

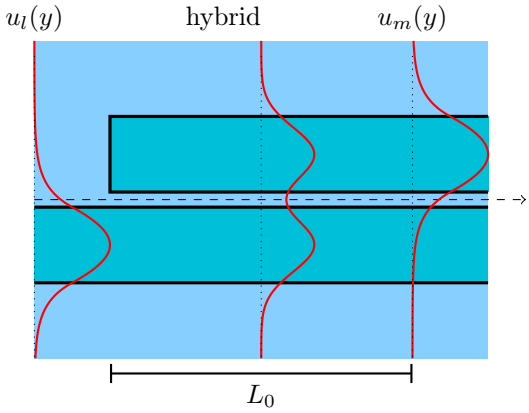


Figure 2.6: Power distributions of the exciting and excited modes in coupled parallel planar single-mode waveguides, as well as the intermediate field distribution.

$$u_u = (u_o - u_e)/2 \tag{2.38}$$
$$u_l = (u_o + u_e)/2 \tag{2.39}$$

so that the initial state u_l is a superposition of the odd and even mode. Further, it can be shown that the propagation constants β_o and β_e are not identical[26]. Thus, as the odd and even mode undergo phase shift, u_u becomes more dominant, until it is the sole existing mode after a distance $L_0 = \frac{\pi}{\beta_o - \beta_e}$.

If the waveguides are placed further apart, the coupling coefficients from Equation (2.35) will be smaller, and L_0 increases. This becomes relevant in more complex devices where the waveguides may curve apart after the coupling region. While a first approximation may assume that the coupling coefficients are zero outside of the coupling region, this is a dangerous approach as coupling may take place in the curve itself[69].

2.3 Microring Resonators

While being able to guide light is in itself interesting, more complex devices than waveguides are needed in order to manipulate light. One such device is the microring resonator. The resonator is a conceptually simple device, consisting of two adjacent waveguides, one shaped like a small loop and another, the bus waveguide, passing along it in a straight line. The light passing through the bus waveguide is able to couple into the loop in accordance with the theory outlined in Section 2.2, allowing light continually fed in to interfere with itself[5]. This causes resonances when the total phase shift in a round-trip in the ring is a multiple of 2π. This means that the requirement for resonance is

$$\lambda_{\text{res}} = n_e L/q, q \in \mathbb{N}_{>0}. \tag{2.40}$$

The field stored in the loop will couple back into the bus waveguide. At a resonance, the field coupled out of the loop will exactly cancel out the field in the waveguide, leading to complete extinction.

Functionalizing the resonator allows the refractive index of the surrounding medium to be chemically sensitive. This in turn alters the effective index n_e and changes the resonance conditions. Thus the resonance frequency can be tuned by depositing chemicals, which makes the microring resonator a viable candidate for chemical sensing[74]. Importantly, this can be used for detecting specific proteins in order to make novel, miniaturized diagnostic equipment[12].

While the term microring or ring resonator is in common use, the resonator geometry is not restricted to circles[5]. Ring resonators come in different forms. Of particular interest in this paper are racetrack resonators, which have an elongated coupling region. This is advantageous because it allows the bus waveguide and the ring to be spaced further apart as outlined in Section 2.2, which allows for easier manufacturing. Ring resonators can also be realized in photonic crystals, for example in square or hexagonal shapes as determined by the crystal structure[52].

In the simplest case, a ring resonator is placed adjacent to a single waveguide. Under ideal conditions of no loss in the resonator, this is termed an all-pass filter, as it has unity transmission over the whole spectrum and only introduces a phase shift[5]. However, balancing the losses in the waveguide and coupling into and out of it tells a different story.

Consider the system shown in Figure 2.7. Here a_1 and b_1 are the incoming and outgoing fields in the bus waveguide, and a_2 and b_2 the incoming and outgoing fields in the racetrack. The coupling between waveguide and resonator is given by k, and the self-coupling by t. The transmission through the ring is given by α, such that $a_2 = \alpha e^{i\phi} b_2$, ϕ being the phase shift introduced by the resonator. This system can be described by the scattering matrix method, as follows[75].

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} t & k \\ k^* & -t^* \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.41}$$

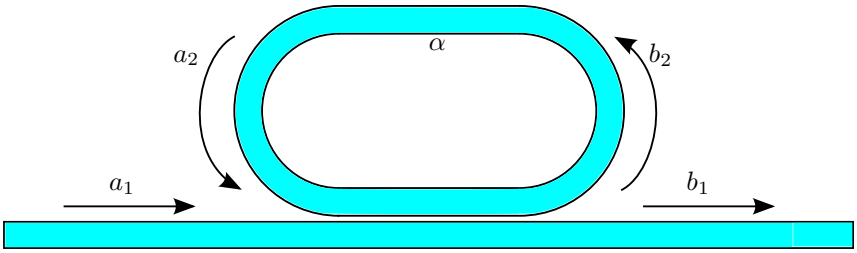


Figure 2.7: Schematic of a racetrack resonator in an all-pass filter configuration.

Considering the ratio between the incoming and outgoing power yields the following equation.

$$\left|\frac{b_1}{a_1}\right| = \frac{\alpha^2 + |t|^2 - 2\alpha\,|t|\cos\phi}{1 + \alpha^2\,|t|^2 - 2\alpha\,|t|\cos\phi} \tag{2.42}$$

An interesting feature of this is that when the self-coupling coefficient t is equal to the transmission coefficient α, the transmission drops to zero when $\phi = m2\pi$. This condition is called critical coupling[75]. It follows that in order to construct a high-quality resonator, balancing the coupling and loss is of great importance. It has been suggested that if the transmission coefficient can be controlled rapidly, this resonator setup may be used as a small and low-imprint optical switch[75].

In the more general case of non-critical coupling, the output at resonance becomes

$$\left|\frac{b_1}{a_1}\right| = \frac{(\alpha - |t|)^2}{(1 - \alpha\,|t|)^2}. \tag{2.43}$$

2.4 Silicon on Insulator

Silicon on Insulator (SOI) wafers consist of three layers. The bottom layer is a thick slab of silicon, the middle layer is SiO_2 and the top layer is silicon. Interest in the technology has been increasing over the past 20 years, and SOI wafers have been used by CPU and GPU manufacturer in the past and present[19]. In photonics, SOI is especially interesting because the oxide layer confines light in the silicon through total internal reflection.

One of the major advantages of SOI technology is that silicon micromachining techniques have become very sophisticated over the almost 60 years that silicon has been the preferred material for semiconductors. High quality CMOS fabrication equipment is widely available, and these existing production lines can be used without the complications of developing and purchasing new equipment especially for photonic components.

Furthermore, sharing processing equipment means that the prospects are good for integrating micro- and nanoelectronics with silicon photonic components. This could lead both to photonic components being used in computing, and to electronic components directly working with photonic ones, miniaturizing communications equipment[11].

There are three main ways of fabricating SOI: SIMOX, Smart Cut and PECVD.

In the SIMOX process, high dose ion implantation is used to bury an oxygen layer deep below the wafer surface[24]. A subsequent annealing step converts the oxygen doped layer to SiO_2, while a silicon layer on top remains untouched. In Smart Cut[8], a silicon wafer with an oxide capping layer has hydrogen implanted deep under the surface. Then, the oxide is bonded to another wafer, and the whole system is heated. During heating, the hydrogen creates bubbles and the wafer cracks, leaving a rough SOI wafer that must be polished. The Smart Cut method produces higher quality wafers than SIMOX, but is more expensive due to the far more complex fabrication process.

PECVD growth is an alternative to the prohibitively expensive wafers produced by the aforementioned processes. In PECVD growth, precursor gases are allowed to react and settle on the wafer surface to build films, which will be covered in more detail in Section 3.4. There are two main advantages to PECVD grown SOI: Having total control over the growth process allows samples to be made exactly according to the needs of the researchers. With commercially bought SOI, the selection is limited to that which is in stock with a vendor, prices can be very high especially if not bought in bulk and the quality may be lacking depending on the manufacturer. Furthermore, many research cleanrooms have a flat rate funding scheme where users can spend a day manufacturing their samples without paying any additional fees. In these cleanrooms, the cost of equipment and material use is covered by the host institution, which makes PECVD grown wafers free from the researchers' point of view.

Chapter 3

Equipment and Setup

3.1 Scanning Electron Microscopy

Scanning Electron Microscopy (SEM) is not a central part of this work, being used only for inspection of the structures. It is, however, included here for completeness and because it is based on the same equipment as the far more important technique of Electron Beam Lithography. SEM is one of the preferred techniques for visualizing micro- and nanostructures. This powerful technique allows for resolution far below the diffraction limit, and introduces new contrast mechanisms[54]. However, it has its own set of disadvantages. This section will explain the fundamentals of SEM. Figure 3.1 shows the Hitachi S-5500 S(T)EM used in this thesis. The T in its name indicates that it is capable of scanning tunneling electron microscopy, which is not used in this thesis.

Construction of the Microscope and Sources of Aberration

The SEM is, as the name suggests, a microscope based on the scanning of a highly focused high energy electron beam over the surface of the sample. A simple sketch of a SEM is shown in Figure 3.2. The source, or electron gun, emits a controllable stream of electrons. In older systems, this is performed using a thermionic emitter, composed of a tungsten filament or LaB_6 crystal heated to around 2800K. Newer systems use a cold field emitter, consisting of a wolfram $\langle 310 \rangle$ monocrystal tapered to a fine point. This device emits electrons even at room temperature in the presence of a strong electric field. This yields a significantly lower energy spread, reduced from around 2 in the thermionic emitter to 0.5 in the cold field emitter. The downsides are a lower overall current, higher relative current noise and drift relative to the thermionic emitter. It is also necessary to remove contaminants by strongly increasing the temperature every 6 to 8 hours[73, p. 90].

After being accelerated by an electrode in the electron source, the electron beam is narrowed down by a limiting aperture. Unfortunately, electron lenses are far from perfect, and significant spherical aberration

would otherwise be introduced by the subsequent lenses. A smaller aperture yields less spherical aberration, but reduces the overall current. The aperture needs to be shifted slightly while calibrating the SEM, but is typically not replaced by users. Spherical aberration can also be reduced by increasing the acceleration voltage.

The electrons then pass through a condenser lens, which serves to concentrate the beam. The beam is then narrowed down by yet another aperture, which is typically succeeded by another condenser lens. The beam then passes through the scanning coils, which deflect the beam to target it at a specific point on the sample surface, and an objective lens which focuses it to a point[54].

The condenser lens also contains stigmator lenses, which circularize the beam to cancel out asymmetries in the preceding lenses. If the beam is not properly circularized, it will have an elliptical shape, which introduces astigmatism in the image. This is one of the main user-correctable sources of unsharpness. Astigmatism will show as points being blurred to lines, and corners may have one sharp edge and one blurred. Going from over-focus to under-focus will reveal whether the system is astigmatic, as the blurring changes direction.

Sample Interaction

When the electron beam strikes the substrate, a number of inelastic and elastic collisions take place. Most importantly, secondary electrons are knocked loose as the incident electrons (primary electrons) strike atoms. These electrons are created throughout the interaction volume, but only the ones created closest to the surface are able to escape, as the secondary electron energy typically is lower than 50 eV[54, p. 166].

Furthermore, elastic electron-electron interactions will cause the primary electrons to be bent off, either widening the beam in forward scattering, or launching the electrons back toward the surface in backscattering. Backscattered electrons are generated throughout the whole interaction volume, shown in Figure 3.3, but not all are able to escape to the surface. However, they are able to return from further down into the sample than secondary electrons. This means that they can carry information about what lies underneath the surface, such as impurities or holes. Of particular importance is the fact that the distance they propagate is very dependent on the atomic number, as larger atoms have a higher probability of colliding with the electron. This causes higher atomic number atoms to appear brighter than low atomic number atoms, in what is called Z-contrast. SE electrons have Z contrast as well, but not as markedly.

Another useful technique is Energy-Dispersive X-ray Spectroscopy (EDS). This method relies on characteristic X-rays emitted from atoms struck by electrons, and gives information about which atoms are present. X-rays are generated far deeper into the interaction volume than electrons can escape from, and thus resolution is poor.

In general, it is easier to visualize conductive materials than isolators. This is because the electron beam charges the sample. In conductors the charge dissipates to ground through the sample holder, while in isolators it remains on the surface. This causes an unwanted electric field which turns away incident electrons, blurring the image and turning it white from the additional electrons that strike the detectors[16].

Secondary electrons that escape to the surface are detected using the SE detector. This detector is usually placed at the side of the specimen chamber. Because the secondary electrons have low energy and are ejected at a wide variety of angles, the SE detector is positively biased in order to suck the electrons in. The backscattered electrons are detected by the BSE detector, which typically is a small disk placed directly above the sample.

Figure 3.1: The Hitachi S-5500 S(T)EM installed at NTNU NanoLab.

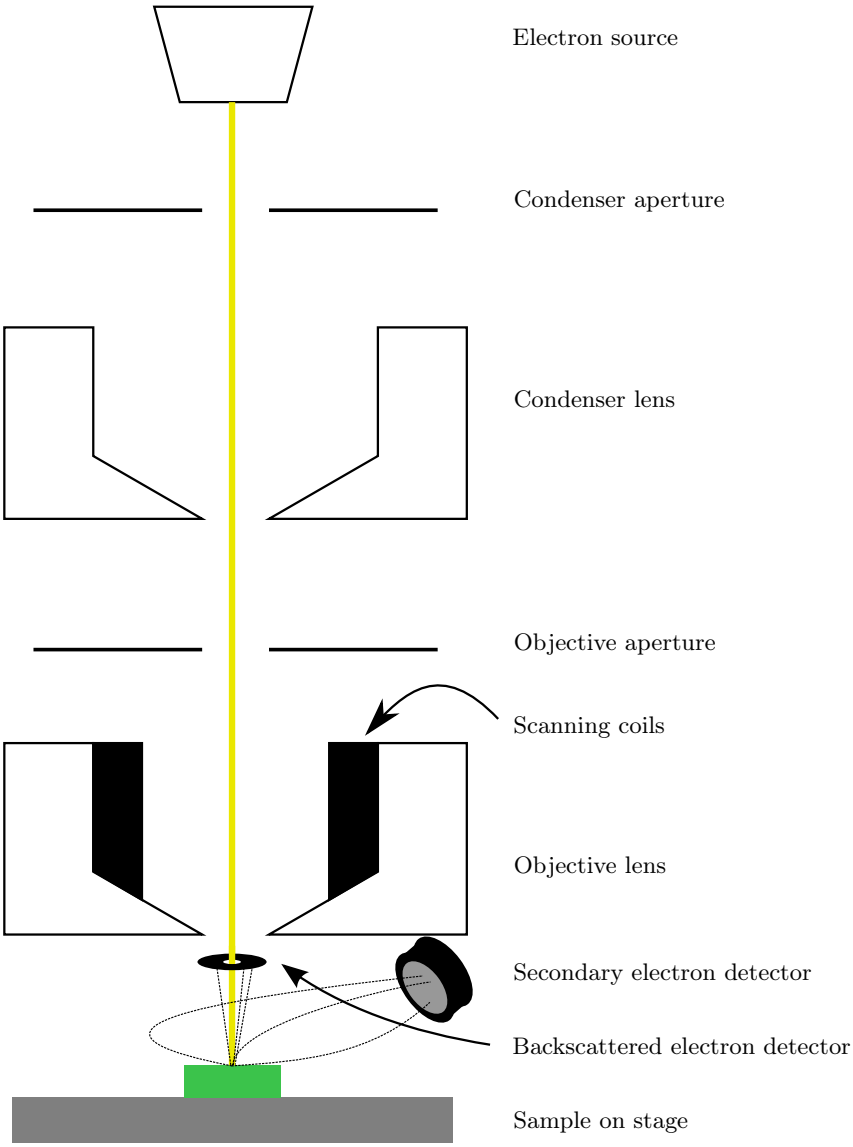


Figure 3.2: Simplified schematic of a SEM.

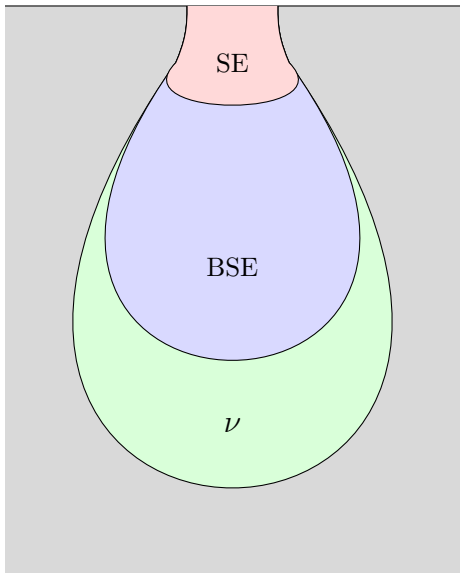


Figure 3.3: Simplified sketch of the interaction volume, labeled with the type of electrons that are able to escape from the particular part of the volume. SE electrons generated in the pink region will be able to escape, and so on. The green region is part of the interaction volume, but only generates characteristic X-rays useful for characterizing the chemical composition. Figure courtesy of Vegar Ottesen.

3.2 Electron Beam Lithography

The EBL technique is based on the same principles as SEM. As a matter of fact, most low cost EBL systems are constructed from SEMs with a retrofitted stage. The stage, retrofitted or native to the system, moves the sample in order to bring an area to be exposed under the beam. In addition to manual manipulation by the operator, it is central to the writing process, as the written area is often larger than that covered by the scanning beam. In this case it has to be broken down into smaller write fields, exposed one at a time and aligned next to each other, with a tolerance defined by operator efforts.

More expensive EBLs differ from budget models in that the stage is integrated with the machine by the manufacturer, and that the EBL can support a higher acceleration voltage than is necessary for a SEM. This allows for higher resolution and straighter sidewalls due to a smaller interaction volume in the resist layer[72, p. 128][30]. A Monte Carlo simulation demonstrating this is shown in Figures 3.4a and 3.4b. In this simulation performed using the CASINO[1] software, 200 electrons in a 5 nm wide beam strike a 270 nm thick PMMA layer on an SOI substrate. The beams have acceleration voltages of 15 kV and 30 kV. It is evident that the amount of scattering in the PMMA layer is far smaller at higher voltages. As the exposed area overlaps more closely with the interaction volume, the sidewalls are visibly straighter. In Figure 3.4c, the resist has been made thinner, reducing the scattering even more.

In EBL, a resist layer is deposited by spin coating on a clean wafer surface. The electron beam scans across the sample surface while it is repeatedly blanked and unblanked, exposing the resist layer to the electrons. Blanking means that a deflection coil redirects the beam into a plate such that it never reaches the sample.

The resist may either be positive or negative. In positive resists, the resist becomes soluble to a developer chemical when it is exposed. This happens either due to the breaking of bonds in the polymer resist, called chain scission, or due to the degeneration of compounds inhibiting dissolution[53, p, 353]. In contrast, negative resists become hardened where exposed, typically through crosslinking promoted by photoactive compounds. Photoactive compounds are named as such for historical reasons, due to the well-established technique of photolithography.

The same polymer may form the basis of both positive and negative resists, the photoactive compound being what determies the tone (positive or negative) and sensitivity. In the case of pure PMMA, there is no photoactive compound, and chain scission is the mechanism of exposure.

Contributions To Write Time

For any given beam current, the time needed to write a pattern scales proportionally with the dose that needs to be delivered. This in turn

[1] `http://www.gel.usherbrooke.ca/casino/`

is dependent on the resist sensitivity and the size of the pattern. For PMMA, the sensitivity is $50 - 500$ µC/cm^2[51], with $100 - 300$ µC/cm^2 being commonly used parameters on NTNU NanoLab's system, depending on the resist thickness.

When an area is exposed, the EBL's software rasterizes it, that is, breaks it down into pixels to be exposed individually. In this case, rather than attempting to expose the area continuously, the beam freezes over a specific point and exposes it for a predetermined amount of time. The time it takes to expose a single pixel, is termed the dwell time. The rasterization process may introduce errors when working with very small features. An example of this is shown in Figure 3.6, where a 500 nm pore as in a photonic crystal has been rasterized with a step size of 20 nm.

When the beam has just moved from one continuous area to the next, there might be instabilities caused by transient effects in the electromagnetic lenses. To account for this, a settling time may be introduced, being an interval where the beam rests upon one spot before it is unblanked.

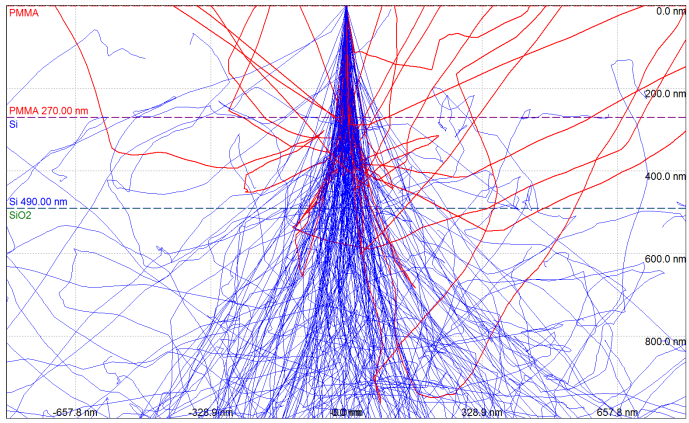
In the case where many small areas are exposed one at a time, this can be a major contribution to the writing time, and it is important to optimize in order to achieve acceptable write times. However, a too short settling time will result in exposure while the beam is unstable, yielding distorted features[4]. The beam speed is defined by the distance between features and the sum of exposure time and settling time. Raith recommends that this speed be kept below 10 mm/s, and preferably below 1 mm/s for optimal performance[4].

Proximity effects

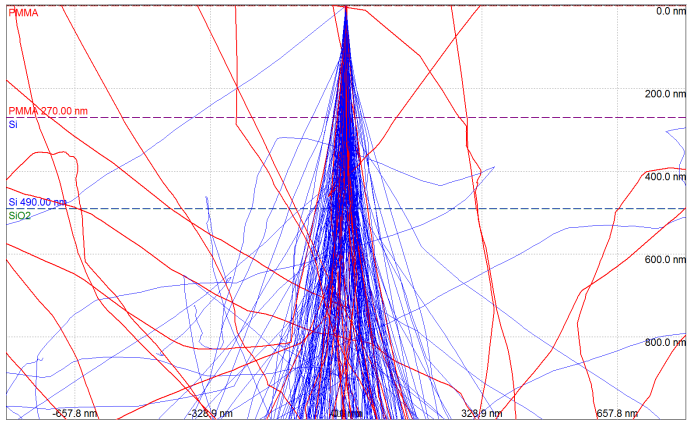
When a feature is exposed, the resist directly adjacent to it receives a non-zero dose as well. This undesired exposure occurs mostly due to electron forward scattering in the resist, very evident from Figure 3.4 which shows that forward scattering causes most of the complete exposure widening. However, backscattering from the resist can also be problematic, to a smaller degree but over a larger area than the forward scattering. Due to the effects explained in Section 3.1, the degree to which backscattering matters depends a great deal on the choice of substrate and acceleration voltage: A higher voltage or a higher Z substrate, such as a gold film instead of bare silicon, will create more backscattered electrons. Increasing the exposure dose will, of course, increase proximity effects proportionally[20].

When using negative resists the backscattering can be especially problematic, as undesired crosslinking can leave a thin, hardened resist layer on the surface, necessitating further removal steps. More economically and dependably, reworking the exposure recipe can be a better option. With positive resists, very thin exposed layers will typically not be developed unless they are strongly exposed, and the problem is not as significant. However, when two features are placed sufficiently close to one another,

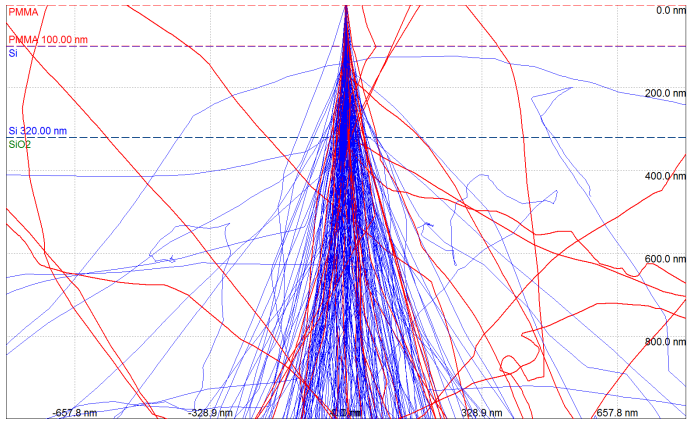
two individually underexposed regions may overlap and cause widening of the features. In the worst case scenario the features can melt together.



(a) 270 nm PMMA, 15 kV.



(b) 270 nm PMMA, 30 kV.



(c) 100 nm PMMA, 30 kV. Note the different height of the first boundary.

Figure 3.4: Monte Carlo simulations of electron beams striking PMMA on SOI. The width of the beam in the PMMA/Si interface is reduced when the resist gets thinner or the acceleration voltage increases.

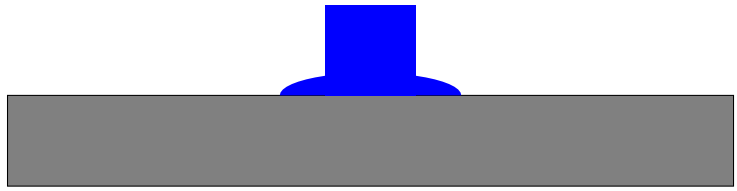


Figure 3.5: A simplified sketch of the resulting resist profile if backscattered electrons from the substrate hardens the bottom of a negative resist layer. Enough electrons have escaped from the substrate and back into the resist to make an unwanted solid layer around the feature.

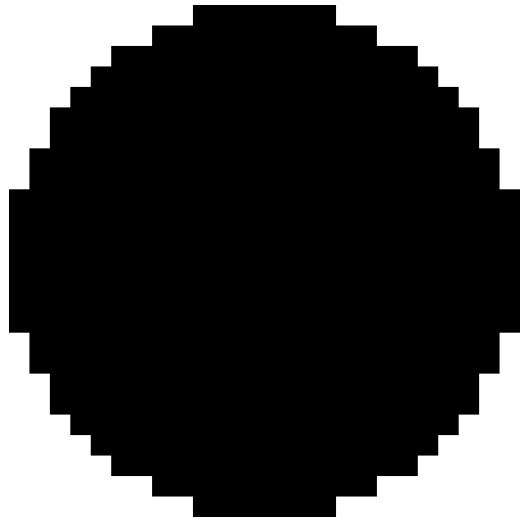


Figure 3.6: Example of a 500 nm circle rasterized with a step size of 20 nm.

3.3 Inductively Coupled Plasma Reactive Ion Etching

The Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) technique is a simple and popular etching technique[29, 31]. Among its advantages are a simple design and flexibility with regard to balancing chemical and physical (sputtering) etch mechanisms.

The ICP-RIE consists of a plasma chamber under vacuum. An example of the whole machine is shown in Figure 3.7. Process gases are introduced into the chamber through a coil separated from the plasma by a dielectric. An RF magnetic field is applied, disassociating the gas molecules and igniting the plasma. The frequency 13.56 MHz is common, as it is reserved as an industrial, scientific and medical (ISM) radio band by the International Telecommunications Union[67]. This is what leads to the term "inductively coupled plasma".

At the same time, an RF electric field is applied between the wafer chuck and a grounded electrode, accelerating the electrons and ionized atoms in opposite directions. Electrons move further due to their lower mass and ionize the wafer chuck[53]. Thus a strong DC self-bias develops, and the ions are accelerated into the wafer.

Commonly, a whole wafer is placed in the machine to undergo etching. However, many wafer holders are designed for 4 in wafers, and anything smaller would not be possible to mount. For this reason, smaller samples such as the ones used in this work must rest upon a carrier wafer. At NTNU NanoLab, this carrier wafer is usually made from sapphire, which has the chemical composition Al_2O_3. Silicon wafers are also used, but they have the disadvantage of being less inert than the sapphire. This causes them to be consumed by the etching over time, and needing frequent replacement. Unfortunately this is not widely discussed in the literature, as mass production efforts always use whole wafers that don't need carriers.

Gas flow in ICP-RIE and PECVD is typically measured in the unit sccm. This acronym stands for standard cubic centimeters per minute, and refers to the amount of gas that would fill 1 cm^3 at 1 bar and 25 °C.

Etching Action

The self-bias mechanism ensures an ion path relatively perpendicular to the wafer, making the sputter component of the etch highly directional. However, the high plasma density caused by the ICP mechanism means that many of the incident atoms will still be ionized as they hit the wafer surface. These ions are more reactive than their neutral counterparts, and will contribute with a chemical component to the etch.

This makes it possible to select etch gases appropriate to the desired substrate for improved selectivity and higher etch rate. For example, fluorine based etch chemistries such as SF_6 are well suited for etching oxides.

Figure 3.7: The Oxford Instruments Plasmalab System 100 ICP-RIE 180 installed at NTNU NanoLab.

If a more physical etch is desired, the ICP power may be reduced for a larger proportion of non-ionized atoms striking the surface. If the ICP power is switched off entirely, the system works as a regular RIE. As the RF power has an effect on the plasma density as well, tuning it will also have an effect on the chemical to physical etching ratio, although sufficiently low RF power may fail to ignite the plasma or charge the wafer

chuck.

Etching Parameters

Etch Profile

The shape of an etched hole is known as the etch profile. Etch profiles are subdivided into two types: Isotropic and anisotropic. Isotropic etches etch equally fast in all directions, while anisotropic ones etch faster in one direction. Typically, wet chemical etches are more isotropic in nature, while dry physical etches are anisotropic. For this reason, dry etching is used for submicron dimension devices[53]. Typical etch profiles are shown in Figure 3.8.

ICP-RIE, being a combination of a chemical and physical etch, can exhibit traits of both anisotropic and isotropic etching. However, directionality is strongly preferred for higher resolution, so most etch recipes are optimized for anisotropic etching. While it is possible to quantify anisotropy, as in [37], this has not been done in this work.

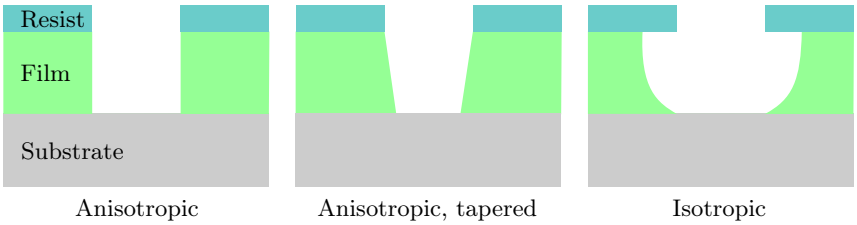


Figure 3.8: Three examples of etch profiles.

Etch Rate

The etch rate is, as implied by the name, the rate with which the surface material disappears as it undergoes etching action. In this work, it will typically be given in the unit nm/s. Due to etch selectivity, it is necessary to state the etch rate for each material to be etched.

The etch rate is dependent on among other things ICP and RF power, choice of process gases, chamber pressure, temperature and other chemicals present in the chamber.

Uniformity

Uniformity is the ability to etch with the same characteristics across the entire wafer surface[53]. This is naturally an important parameter, as features everywhere on the wafer should be processed identically. Etch uniformity may be compromised by geometry, for example wafer clamps or other features of the chamber that rest on the edge of the wafer or close

to it. These may interfere with the diffusion of reactive species, changing the chemical component from point to point on the wafer.

Furthermore, uniformity may not be preserved over very small features due to changes in aspect ratio. High aspect ratio trenches may wind up being clogged, meaning that reactive species will not easily diffuse into them and etched material may not get out.

Selectivity

Etch selectivity is an issue with both chemical and physical etches, but moreso with chemicals[53]. In the case of chemical etching, some reactive species will not react with certain materials at all, and certain crystallographic directions will etch more easily than others[38]. With wet etches such as KOH, this may be exploited to achieve well-defined features in monocrystalline materials, but with dry etches such as RIE and ICP-RIE this is not an option.

Physical etching is selective mostly due to the difference in sputter yield. Sputter yield is defined as the number of surface atoms blasted away by the incoming ions, and is dependent on the binding energy and chemistry of the etched atoms. However, selectivity to sputter etching is far lower than to chemical etching[29].

Polymer Formation

By selecting organic molecules as part of the etch chemistry, it is possible to deposit polymers, which may improve the anisotropy of the etch. Examples of such chemicals include CHF_3 and CF_4.

The mechanism for improving the etch is that the sidewalls are protected against low-energy chemical etching, while the polymer that deposits on the bottom will be sputtered away. Thus, it is possible to achieve higher aspect ratio etching or to avoid undercut. A sketch demonstrating this is shown in Figure 3.9.

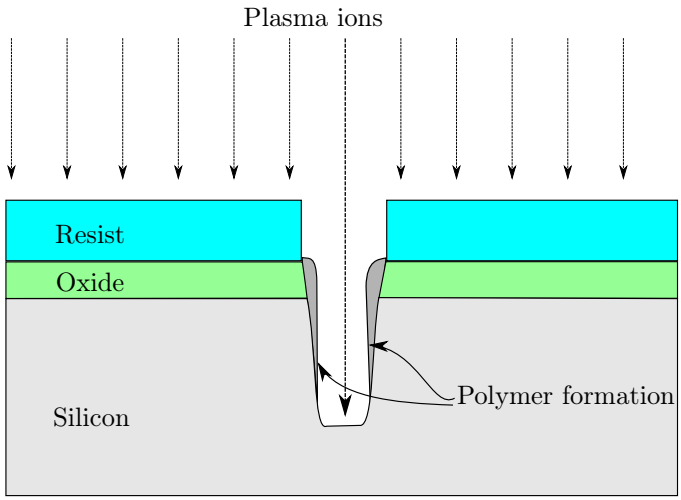


Figure 3.9: Polymer sidewall passivation. Adapted from Quirk and Serda[53].

3.4 Plasma Enhanced Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a technique for depositing material on a surface. It consists of introducing gases into a reactor chamber, allowing them to undergo chemical reactions and deposit precursors on the substrate[53]. Many modern systems are of the Plasma Enhanced CVD (PECVD) variety. NTNU NanoLab's CVD system is of this kind, shown in Figure 3.10.

In this method, the gases are disassociated by either an alternating electric field at 13.56 MHz or by a DC discharge between two electrodes. Low frequency RF fields are also commonly used, in the range of 100 kHz. The low frequency requires hundreds of volts to maintain high plasma density, and causes ion bombardment of the substrate. Conversely, RF ignites the plasma more easily, but relies on diffusion to bring the precursors to the substrate. Many systems use a combination of high and low frequency RF[68].

While older CVD systems typically used atmospheric pressure and high temperatures to drive the reactions, PECVD is able to run at lower pressure and at lower temperatures due to the high plasma density. This leads to lower substrate damage and higher quality films, but requires more expensive systems due to the added complexity[53].

Chemical Processes

The chemical pathways involved in PECVD can be extremely complicated[32], involving classical chemical reactions, photolysis and collisions between free electrons and any of the species present in the chamber. Therefore, the processes mentioned here are somewhat simplified.

It is to be noted that both processes presented here include carrier gases that do not take part in the reaction. These inert gases serve to produce a high enough chamber pressure to maintain the plasma. Lower pressures will not have a high enough plasma density, as the ionizing collisions of accelerated ions and neutral molecules do not take place as often. However, increasing the concentration of process gases may increase the growth rate dramatically, leading to uncontrolled growth and low-quality films.

Silicon

While it is possible to grow monocrystalline silicon using vapor-phase epitaxy, a technique similar in principle to CVD, this can not be achieved with most PECVD equipment due to the high temperatures and low pressures necessary. Furthermore, it is necessary to deposit on a clean, monocrystalline substrate of similar crystal structure and lattice constant as silicon. This will not be the case in this work, as the silicon will be deposited on silicon dioxide. The net chemical reaction for growing the silicon layer with PECVD is given in Reaction 3.1.

$$SiH_4\,(g) + Ar\,(g) \longrightarrow Si\,(s) + H_2\,(g) + Ar\,(g) \qquad \{3.1\}$$

Therefore, the deposited silicon will be amorphous, or devoid of crystal structure. An interesting feature of this material is that due to the imperfect crystal packing, not all silicon atoms will have all chemical bonds filled. This leads to dangling bonds, which are localized charges. These can act as strong scatterers, leading to bulk losses.[61]. This problem solves itself in the presence of hydrogen, as the atoms fill the dangling bonds easily. The resulting material is known as hydrogenated amorphous silicon (a-Si:H), and can have as low losses as 0.2 dB/cm. For practical reasons, a-Si:H will only be known as Si in this work.

While hydrogenation solves the issue of bulk losses, it introduces restrictions on the processing steps the material can undergo: Annealing the waveguides leads to out-diffusion of the hydrogen and re-introduces the dangling bonds, with losses as high as 70 dB/cm[76]. Further annealing can reduce the losses somewhat, as the silicon enters a polycrystalline phase.

Silicon Dioxide

Like silicon, SiO_2 grown by PECVD is amorphous. While the existence of crystalline SiO_2 on Si has been reported[13], such reports are well within the realm of basic physics and have received little attention. The net chemical reaction is given in Reaction 3.2

$$SiH_4\,(g) + 2\,N_2O\,(g) + N_2\,(g) \longrightarrow SiO_2\,(s) + 3\,N_2\,(g) + 2\,H_2\,(g) \qquad \{3.2\}$$

Film Quality

While the topic of thin film quality is complex, only a few aspects will be discussed here. Of greatest importance is film thickness uniformity. For a device dependent on film thickness, it is a major issue if the thickness is not the same over the entire wafer. Unfortunately, this is a question of chamber gas flow and is outside the operator's control.

Film roughness is also a potentially serious issue. Tanenbaum[65] discusses surface roughness further, noting that it increases with increasing film thickness. As mentioned in Section 2.1, roughness can be reduced by polishing treatments, but this is not available at NTNU NanoLab.

Figure 3.10: The Oxford Instruments Plasmalab System 100 PECVD installed at NTNU NanoLab.

3.5 Reflectometry

The reflectometer is an optical device used for measuring the thickness of films. A wide-spectered beam of light is directed on a surface, and the reflected beam is analyzed. Working from assumptions about which layers are present in the film, the reflectometer is able to calculate their thickness based on the intensity spectrum of the reflected light.

NTNU NanoLab's reflectometer is shown in Figure 3.11. It is rated for films between 15 nm and 70 µm thick, and measures using light in the 380 nm to 1050 nm wavelength range. However, the maximum thickness is also restricted by the opacity of the film. If light cannot penetrate it, there will not be any back-reflection, and the thickness can't be deduced.

Figure 3.11: The Filmetrics F20 reflectometer installed at NTNU NanoLab.

3.6 Optical Test Setup

The setup is to a large degree inherited from Ørnulf Nordseth's PhD work[48], with only some modifications. A diagram of the optical characterization setup is shown in Figure 3.12, and a list of the equipment used is given in Table 3.1. Figure 3.13 shows a photograph the setup.

IR light at a wavelength of 1550 nm is transmitted through a single-mode fiber and butt coupled into the sample. The fiber tip is tapered in order to function as a lens, focusing the beam to a spot between 5 and 50 µm from the tip. Another tapered fibre is positioned at the other end of the sample, butt coupling out of the waveguides. The light passes into a photodetector and the signal is amplified and shown on an oscilloscope.

The sample and the tapered fibers are mounted on separate movable stages. The fibers can be shifted in all directions with micrometer screws, as well as with a coarse adjustment screw in order to move them far away from the sample to enable safe sample handling. The sample can be moved vertically and horizontally. The sample also has a screw for controlling tilt.

The microscope is connected to the camera by a C mount, and mounted on a movable stage made by the department's mechanical workshop. The stage allows for coarse adjustment in the horizontal plane, and features a focus screw with a range of 15 mm. 5x and 20x objectives are attached to the microscope, and an ocular is available for adjusting the microscope without relying on the camera. This is necessary because the camera appears to be relatively insensitive to visible light. A high-powered 7000 lm LED flashlight was used for illuminating the samples during alignment, although this level of flux is more than is needed.

Temperature Controller

The temperature controller manages the heating and cooling capabilities of the laser diode. The temperature of the laser chassis is measured using an NTC thermistor, which is a semiconducting device with strongly temperature-dependent conductivity. The resistivity of a thermistor is given by[59]

$$R = R_0 e^{-B(\frac{1}{T_0} - \frac{1}{T})} = r_\infty e^{B/T}, \text{where} \tag{3.1}$$

$$r_\infty = R_0 e^{-B/T_0}. \tag{3.2}$$

The B parameter is given by the manufacturer and determines the electrical characteristics of the thermistor. T_0 is typically 25 °C. It is notable that the the resistivity goes up when the temperature goes down. This is the basis for the acronym NTC, which stands for Negative Temperature Coefficient. A theoretical explanation can be found in most textbooks on semiconductors, such as Solid State Electronic Devices by Streetman and Banerjee[62].

Table 3.1: Equipment used in the optical setup.

Component	Model
Continuous DFB laser	Anritsu GB-5A-016
Laser driver	Newport Model 505
Laser temp. controller	Newport Model 325
Signal generator	Hewlett Packard 33120 A
Fiber polarizer	Chiral Photonics IFP-155D-SM
Single-mode tapered fibers	Nanonics Imaging
XYZ stage	Elliot Scientific Ltd. MDE881
Microscope	Leitz Wetzlar
Objective	JEA 20/0.4
IR camera	Hamamatsu C2400
Camera driver	Hamamatsu C2400
IR photodetector	InGaAs PIN diode
Digital oscilloscope	Tektronix TDS2004B

While it is possible to both cool and heat the laser, cooling is a slower process than heating due to the fundamental rules of thermodynamics. Therefore, a sound strategy is to set the target temperature higher than the expected operating temperature without any cooling. In this way, heat dissipation into the atmosphere will be the only cooling effect, and the temperature controller will keep heating the laser in a steady state. In practice, this works by setting a target resistivity for the thermistor.

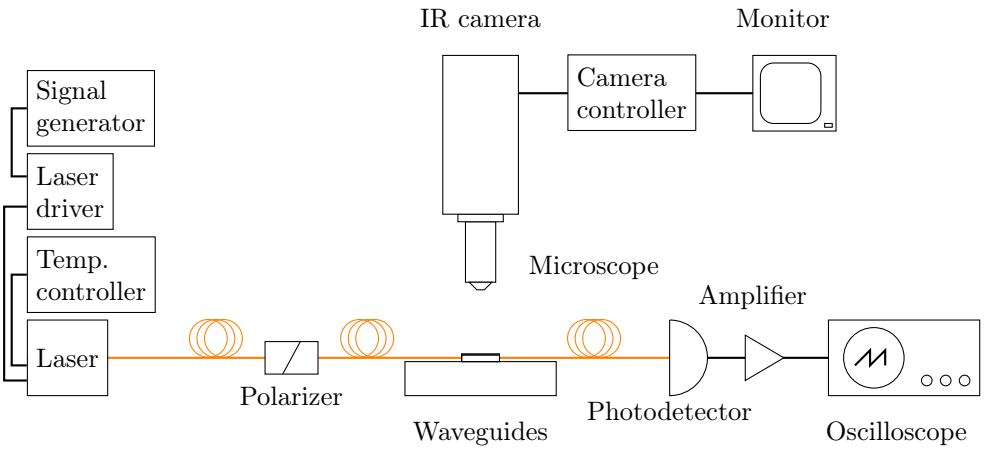


Figure 3.12: Schematic of the optical setup used in the experiments.

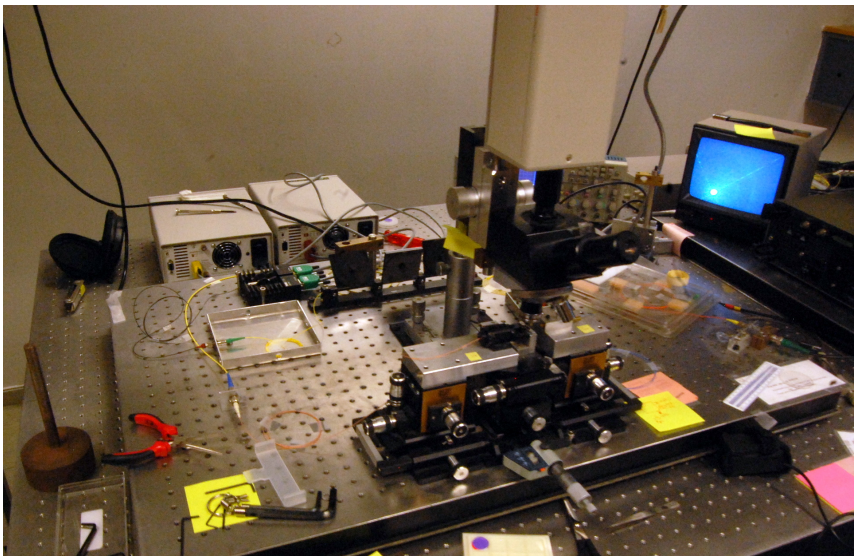


Figure 3.13: Photographic image of the optical setup.

3.7 Scriber-breaker

Breaking silicon wafers into smaller samples in the lab is often done by hand using a scriber tool. This is a stylus with a sharp diamond tip that scrapes away a line in the silicon, creating a weak spot. When torque is applied to the weak spot it breaks, quickly propagating a crack in the {100} plane.

The scriber-breaker automates this process using computerized numerical control (CNC) technology. NTNU NanoLab's Dynatex DX-III scriber shown in Figure 3.14 is able to scribe samples with a precision of around 10 µm. The breaking process also handled by the machine may introduce more errors, as the crack will sometimes deviate from the {100} plane by a few degrees. The scriber can be run either in automatic mode, useful for dicing wafers into smaller samples, or in interactive mode, for cutting an already made sample into a size suitable for the Hitachi S-5500 S(T)EM. It is also able to scribe only for a set distance into a sample, protecting features on the edge from being struck by the scriber facet. This is a very valuable feature when scribing waveguides and samples for cross-section analysis.

Figure 3.14: The Dynatex DX-III installed at NTNU NanoLab.

Chapter 4

Experiments and Results

4.1 Process Development

Materials and Standard Parameters

This section describes the materials and process parameters common to most of the performed experiments. They are included here in order to reduce unnecessary repetitiveness in the main text. This includes spin curves of custom blended resist, EBL parameters and growth and characterization of the wafers used for samples.

Spin Coating and Exposure Parameters

Table 4.1: Parameters for spin coating with 950K PMMA resists. Acceleration time does not count towards spin time.

Parameter	Value
Spin acceleration	1000 RPM/s
Spin speed	Variable, refer to text
Spin time	45 s+ acceleration time
Soft bake temperature	180 °C
Soft bake time	60 s

Resist Spin Curves

For simplifying further work in this project, it was necessary to mix custom blended EBL resist with the desired viscosity. This is important in order to precisely control the thickness of the resist layer. For this purpose, a blend was made of equal parts anisole and 950K PMMA A9[51], making A4.5. Later, it was determined that the A4.5 resist was too thick, and a thinner

Table 4.2: Parameters for EBL exposure.

Parameter	Value
EBL resist	950K PMMA
Acceleration voltage	30 kV
Beam current	100 pA
Settling time	5 ms
Area dose	Variable, refer to text
Write field size	100 µm^2
Developer	1:9 DI water:IPA
Develop time	30 s

one was produced, by mixing one part 950K PMMA A9 resist with two parts anisole. This should ideally make 950K PMMA A3, however the A9 bottle was very old and may have evaporated significantly. Furthermore, it has recently come to the author's attention that the anisole is unfiltered. Even accounting for possible deviations from the specificed deviations, neither the A4.5 or A3 blends are documented by the manufacturer[51].

For the A4.5 resist, 12 mm by 16 mm samples of polished, monocrystalline silicon were spin coated at speeds of 1000 to 7000 RPM at 1000 RPM intervals. For the A3 resist, 12 mm by 12 mm samples were spin coated at 1000 to 5000 RPM, at 1000 RPM intervals and at 2500 RPM. Acceleration was 1000 RPM/s and the spin time at the final speed was 45 s. The samples were soft baked at 180 °C for 60 s and the thickness was measured by reflectometer using a Cauchy model for the dielectric function.

In addition, point measurements were made of A2, A3.5 and A4 blends at 2000, 1500 and 4000 RPM, respectively.

Results

950K PMMA A4.5 The results of the test are summarized in Table 4.3 and Figure 4.1. After spinning at 1000 RPM, the film showed a distinctive repeated rainbow pattern after spinning had finished, indicating a gradient in the film thickness on the order of several µm. However, it appeared to have relaxed to a uniform film on its own after edge bead inspection had been performed. Edge bead is an unwanted phenomenon that occurs during spin coating, where the resist forms a ridge at the outer edges of the wafer[53].

As the edge bead volume may be significant in this case, especially for smaller samples with a high edge length to area ratio, the speed is

deemed non-viable. However, the measurement has been included here for completeness. Refer to the PMMA datasheet[51] for further information.

Table 4.3: Thickness as a function of spin speed for 950K PMMA A4.5

Spin speed [RPM]	Thickness [nm]
1000	490
2000	345
3000	285
4000	251
5000	230
6000	219
7000	212

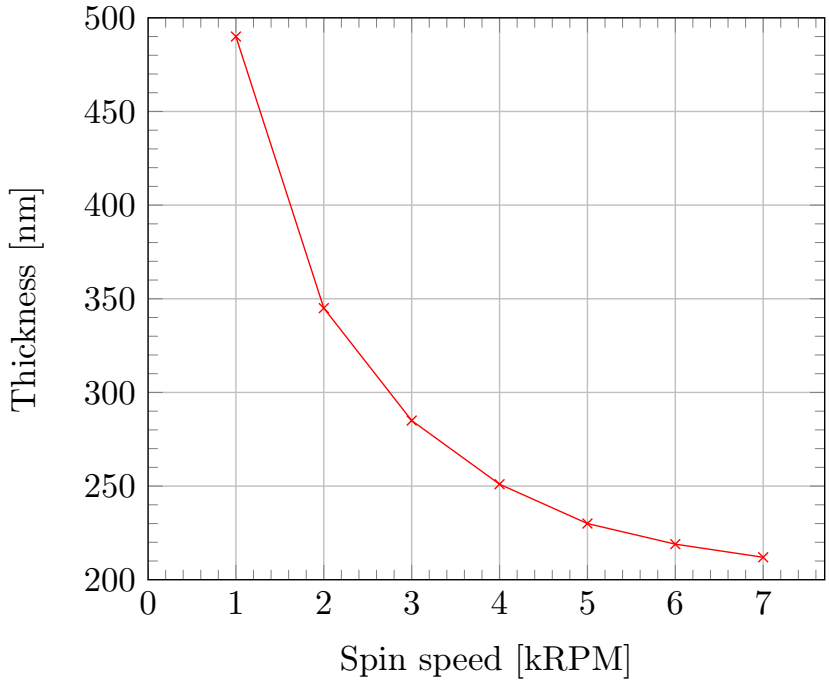


Figure 4.1: Spin curve for 950K PMMA A4.5

950K PMMA A3 The results of the test are summarized in Table 4.4 and Figure 4.2. Regrettably, plotting the thicknesses of A3 and A4.5 in the same graph would make the A3 plot difficult to read. The

entire range of thicknesses available with A3 is 53 nm, while the range for A4.5 is 278 nm.

For 1000 RPM, the film was obviously not in a stable state, as shown by a rainbow pattern even more distinct than that of the A4.5 resist, even floating around visibly, presumably due to the thinner resist. This phenomenon is likely to be dependent on sample size, and the measurement is therefore discarded, and the speed deemed not viable. This is because the edge bead can take up a significant volume, and when floating back into the center of a very small sample, it may represent a large fraction of the total amount of resist.

By comparing with the data given in the PMMA datasheet[51], it is evident that the blended resist behaves more like 950K PMMA A2 than A3. This could indicate a poorly mixed resist, however this seems unlikely as the half-full bottle was shaken more than a hundred times.

Table 4.4: Thickness as a function of spin speed for 950K PMMA A3

Spin speed [RPM]	Thickness [nm]
2000	168
2500	152
3000	138
4000	123
5000	115

Table 4.5: Thicknesses of A2, A3.5 and A4 at 2000, 1500 and 4000 RPM, respectively.

Resist	Spin speed [RPM]	Thickness [nm]
950K PMMA A2	2000	85
950K PMMA A3.5	1500	260
950K PMMA A4	4000	250

950K PMMA A2 and A4 The measured thicknesses are given in Table 4.5.

The A2 thickness is comparable to what can be read out of the graph in the datasheel[51], but the A4 resist was significantly thicker. There could be several reasons for this, as it was mixed by another cleanroom user. This illustrates the fact that bottles of chemicals made by other cleanroom users should not be trusted blindly to conform to specifications. No tabulated values exist for A3.5.

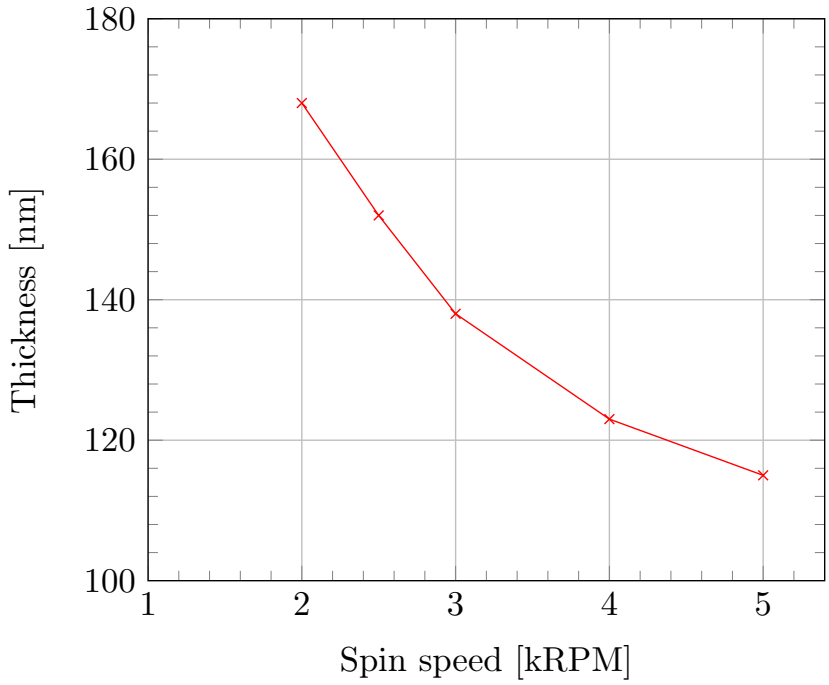


Figure 4.2: Spin curve for 950K PMMA A3

Fabricated Wafers

A stated goal of the project was to manufacture the structures on self-grown SOI. This was performed by loading silicon wafers into the Oxford Instruments PECVD and depositing SiO_2 and a-Si films of the desired thickness.

First, a chamber preconditioning step is performed on the carrier wafer in order to stabilize the growth rate. This is done by running the desired film growth recipe for 30 minutes. Then, a small sample has the desired film deposited to an expected thickness of around 200 nm. This sample is measured in a reflectometer and the growth rate is calculated. It is important that the sample material is compatible with the film, and must support film growth, not island growth or Volmer-Weber[7], and there must be a precise reflectometer recipe available. The simpler the sample is, the better, as more layers lead to more degrees of freedom in the reflectometer, and more room for error. For Si growth, both crystalline Si and a SiO_2 on Si sample were used. It is critical that the SiO_2 on Si sample is measured before deposition, to verify that the reported SiO_2 thickness is correct in the rate test measurement.

For SiO_2, the thickness is not as critical as for Si, and the chamber conditioning and rate test do not necessarily need to be performed. In-

Table 4.6: PECVD parameters for a-Si growth.

Parameter	Value
SiH_4	25 sccm
Ar	475 sccm
Pressure	1000 mTorr
RF power	7W
Temperature	250 °C

Table 4.7: PECVD parameters for a-Si growth.

Parameter	Value
SiH_4	8.5 sccm
N_2O	710 sccm
N_2	161.5 sccm
Pressure	1000 mTorr
RF power	20W
Temperature	300 °C

stead, the tabulated rates listed in the process library can be used directly, aiming for a suitable thickness. Alternatively, the film grown in the preconditioning step can be measured and used to calculate the rate.

After the growth rate has been determined the desired film can be deposited on a wafer. It is important that the wafer surface is clean and dry. To ensure this, the wafer was plasma cleaned in O_2, washed with acetone, IPA and DI water and dehydration baked at at least 150 °C for 5 minutes.

The recipes used have the parameters given in Tables 4.6 and 4.7.

Wafer 1: 1000 nm SiO_2, 270 nm Si, 152 nm PMMA From the SiO_2 preconditioning step, a growth rate of 1.2 nm/s was measured. From this, a growth time of 13 min and 53 s was decided on in order to grow 1 µm of SiO_2. A 4" wafer underwent this depositioning process.

Afterward, a Si preconditioning step was performed for 30 minutes with a sample in the chamber. To save time after the SiO_2 deposition, the machine was not allowed time to cool, and the temperature used was 300 °C. The thickness was measured to be 657 nm both in reflectometer and in cross-section SEM, yielding a rate of 0.365 nm/s. As this rate

might be unstable, a second deposition was performed only as a rate test, for 10 min and 3 s. The resulting thickness was measured in both reflectometer and cross-section SEM to 265 nm, yielding a rate of 0.439 nm/s, significantly higher than the previous one.

A Si layer was then deposited on Wafer 1 for 8 min and 20 s, aiming at 220 nm. The final layer was reflectometrically measured to 270 nm. This indicates a rate of 0.540 nm/s, significantly higher than that measured in the previous runs. The reason for this instability may be the higher temperature. Nevertheless, the wafer was kept for further use.

After cleaning, the wafer was spin coated with 950K PMMA A3 at 2500 RPM, following a 5 second spreading step at 300 RPM, which can be useful for large wafers. This should yield a 152 nm thick layer of resist, as per Table 4.4. The final wafer was scribed into 14 mm by 14 mm squares in the scriber-breaker.

Wafer 2: 1060 nm SiO_2, 205 nm Si, 50 nm SiO_2 Hardmask As the chamber had been used for SiO_2 by the last user, no preconditioning was performed. A 5 min deposition yielded 390 nm, or 1.3 nm/s, so 13 minutes was decided on as the deposition time. This yielded a 1060 nm thick layer in the center, up to 1160 nm in the edges.

For Si, a rate of 0.431 nm/s was found. Aiming at 220 nm, the wafer underwent deposition for 8 minutes and 30 s. According to reflectometric measurements, however, only 205 nm were deposited.

Following this, the hard mask layer was deposited using the same SiO_2 recipe as before. Due to the Si layer deposited in between, a new preconditioning and rate test had to be performed. The rate was measured to be 1.27 nm/s, and 42 s was selected as the depositioning time, aiming at 50 nm. Reflectometric measurements were not performed, as there is no built-in recipe for this combination of layers in the FILMeasure software.

Wafer 3: 1100 nm SiO_2, 200 nm Si This wafer was manufactured by Jens Høvik. Unfortunately, growth rates are not known as a large number of wafers were fabricated at the same time, this being only one of many.

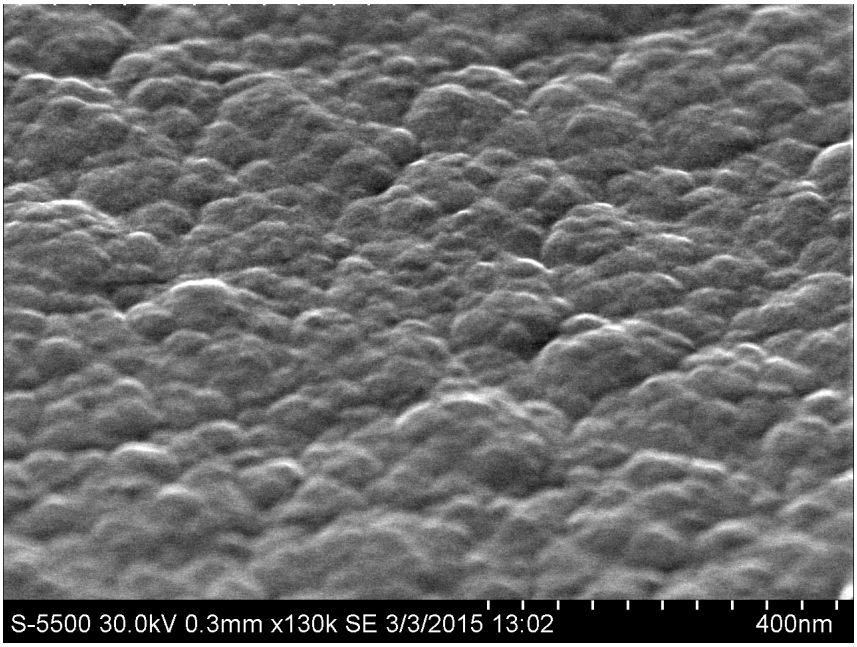


Figure 4.3: Rough surface of Wafer 1.

Initial silicon patterning and sidewall exposure

Method

A sample consisting of bare, monocrystalline silicon was prepared using the existing 950K PMMA A3.5 resist, at a thickness of 260 nm. A mask was designed featuring lines of width from 400 to 600 nm, with alignment marks in order to make identification of the individual lines easier. The mask was exposed twice, with exposure doses of 120 and 192 $\mu C/cm^2$ in order to compare the vastly different optimal doses of Vigen[69], who used 120 $\mu C/cm^2$ and Bolstad[6], who used 192 $\mu C/cm^2$. The reason for the significant difference is not known, but was observed even within Vigen's trials.

After exposure and development, the sample was etched during the ICP-RIE training course, according to the parameters given in Table 4.8. The machine used was the ICP-RIE cryo, a machine very similar to the one used in the rest of this thesis work, except with the capability to cool the sample to cryogenic temperatures. This machine was not used, however, because of other users' concerns about non-repeatability and stability. A final ellipsometric measurement was made to check for residues resist post-etching.

Table 4.8: Etching parameters for the sample.

Parameter	Value	Unit
SF_6	7.5	sccm
CHF_3	50.0	sccm
Pressure	15	mTorr
CCP power	40	W
ICP power	600	W
Temperature	20	C
Time	60	Seconds

The final sample was scribed down to a size of 5 mm-by-3 mm with the Dynatex DX-III scriber. The scribe lines crossed the developed waveguides, so that sidewall characterization would be possible using the S(T)EM's cross-section holder.

The sample was also imaged once again at a later date in order to verify the results.

Results

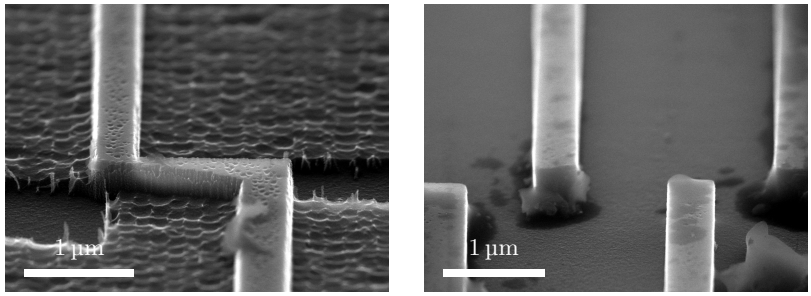
Reflectometric measurements pre-exposure in the Filmetrics F20 showed the resist thickness to be 260 nm.

It was shown that it is feasible to produce waveguides with straight sidewalls by replicating the methods developed in previous work. However, it turns out that there are complications that must be overcome, and that the process needs to be adapted for the particular needs of this work.

Figure 4.4 shows the boundary between two write fields, one for each exposure dose. The most apparent difference is the presence of a very rough layer on the sample exposed with the lower dose, with a smoother waveguide and a smoother floor underneath. In comparison, the higher exposure dose yields only the smooth waveguides and the smooth floor.

The explanation for these different structures is simply underexposure. The lower dose was obviously not sufficient to fully expose the resist layer, leaving a significant residue on the surface. During etching this layer had to be etched through before the underlying silicon could be removed. In addition the semi-developed resist is rough and lumpy, causing the underetched silicon to be roughened as well.

However, the stitching error caused double exposure of a small area where the resist was removed entirely, exposing parts of the silicon to the full etching process. This is sheer luck. There are no guarantees that the write fields will overlap in this way, but the resulting structures are very instructive.



(a) 120 µC/cm^2 (b) 192 µC/cm^2

Figure 4.4: Stitching errors for doses of 120 and 192 µC/cm^2. The structures appear to be smooth and of high quality.

Figure 4.5 shows a cross-section of a waveguide from the 192 µC/cm^2-exposed area. While the left sidewall is straight, the right sidewall appears to be isotropic. This might be due to carelessness on the part of the researchers. The sample was known to have received some rough treatment, with residual silicon dust from scribing and other sources being a potential issue. However, the straight sidewall serves as a proof of concept.

The curve at the bottom should not be a problem in the final structures as an oxide layer will be present at the 200 nm mark and will serve as an automatic etch stop. In this trial the total etched depth was found to be around 440 nm.

A useful result from this trial is an approximation of the etching recipe's selectivity. Reflectometric measurements of the residual resist layer showed that any remaining resist would be below the reflectometer's sensitivity, meaning at most 50 nm. Assuming no resist layer, a lower bound for the selectivity thus becomes the etched depth in silicon divided by the resist layer's initial thickness, or 1.69.

This result is significant, as it implies that a resist layer theoretically only 130 nm thick will be able to protect the 220 nm thick silicon completely during etching. A thinner resist is desirable, as the width of the beam increases during the passage through the superfluous PMMA layer and decreases accuracy, as shown in Figure 3.4. The desired resist thickness is below the range given in Figure 4.1, so the thinner 950K PMMA A3 resist was mixed, as documented in Section 4.1.

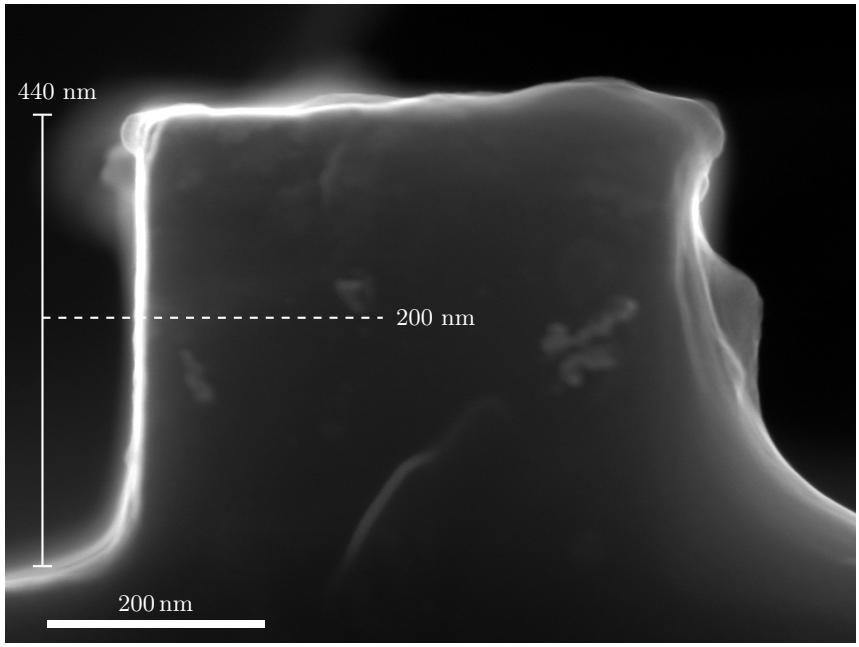


Figure 4.5: Cross-section of a waveguide exposed with 192 $\mu C/cm^2$.

The waveguide shown in Figure 4.4b is very smooth and appears to be of high quality. Therefore, repeating this degree of smoothness was the goal during the rest of the project. At one point, the resolution of the images was questioned, and the sample was inspected again. Figure 4.6 shows the resulting image. The sidewalls are quite rough, illustrating that achieving very high resolution is necessary in order to identify roughness.

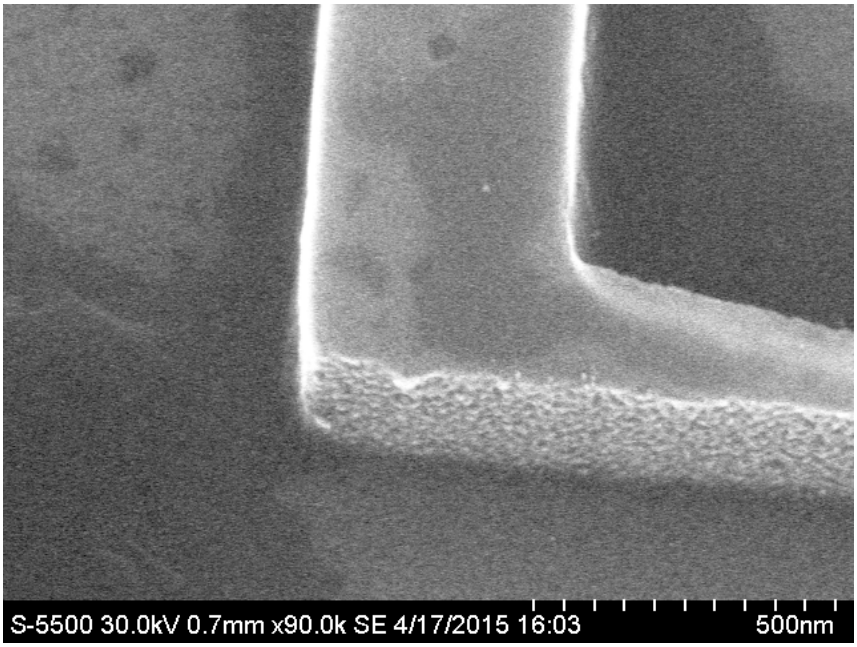


Figure 4.6: A higher-resolution image of the sample taken at a later date. Larger sidewall roughness than seen previously is evident.

Etch Recipe Comparisons

As the sidewalls seen in preliminary tests were unacceptably rough, it was necessary to find an etch recipe that would produce smoother sidewalls with a vertical etch profile. For this purpose, a number of etch recipes were tested. Sources included a folder of recipes written by Oxford Instruments and other lab users, recipes published in research papers[37] and previous master's theses[41]. Some trials also created novel etch recipes by starting with existing ones and changing single parameters, inspired by discussions with other cleanroom users or made haphazardly in order to look for highly visible changes in the structures.

Notably, one strategy that was employed was setting the ICP power to zero in order to run the etcher in RIE mode. Also, using Ion Beam Etching was considered due to the technique's predominantly physical etching mechanism and resulting anisotropic etch profile[53]. However, the instrument had significant downtime during the semester, and was not available at the time of this experiment.

Method

For ease of inspection, monocrystalline silicon was used as the etched material. The reason for monocrystalline silicon being advantageous is that the insulator layer of SOI stops the electron charge building from dissipating, as described in Section 3.1. While this may lead to some mispredictions of the etch's properties in the amorphous silicon used in the SOI samples, it is critical in order to image the sidewall defects. The difference between etching monocrystalline and amorphous silicon will be shown in Section 4.1.

The samples were spin coated with 270 nm thick 950K PMMA A4.5 by spinning at 3500 RPM. A mask consisting of several test structures including circles, lines and a lattice of pores was exposed using the exposure parameters previously determined. To ensure conformity, many of these structures were made on one piece of silicon in the same run, and the sample was scribed into several smaller ones. These were etched separately, using the parameters given in Table 4.9. For easier lookup, the table is sorted by the first column, then by the second and so on. The exception is the first eight entries, which are all based on Recipe 1 and are clustered by themselves. A sapphire wafer was used for all the etches.

Most of the experiments were performed by Jens Høvik, others by the author. The samples were inspected in the S-5500 S(T)EM. Some of the recipes were tested for a-Si-to-PMMA selectivity. Thickness measurements were performed using the Filmetrics F20 reflectometer.

Results

The experimentation succeeded in identifying a family of etch recipes that yielded very smooth sidewalls compared to the others. In particular, recipes with 12 sccm of SF_6 and 3 sccm of O_2 were highly successful.

This etch chemistry is among those recommended by Oxford Instruments. An example of the smoothest sidewalls found is shown in Figure 4.7. For comparison, Figure 4.8 shows a related etch, recipe 24, with CHF_3 constituting part of the etch chemistry. The other etch chemistries tested showed similar sidewall roughness to that shown in this figure. Pictures of the other recipes will not be published here, but are available on request.

Experimenting with the RF and ICP power also gave interesting insights. An early result was that reducing the ICP power or switching it entirely off gave a somewhat more anisotropic, although slower, etch. This is in line with existing theory,[53] as this would create a weaker plasma and make sputtering the predominant etching mechanism.

A working hypothesis was that further increasing the RF power while decreasing chamber pressure would rapidly remove reactive species and weaken the chemical components, making the etch even more anisotropic. Surprisingly, this was not found to be the case. On the contrary, the best recipe found was number 14, with lowered RF power and increased pressure.

Table 4.10 shows an overview of the quality of the etch recipes. The table is mostly empty, as the low roughness of the sidewalls was the top priority for most of the trials, and rate tests were in general not performed. Etch profile is only included if it was tested explicitly or clearly visible from images taken during SEM inspection.

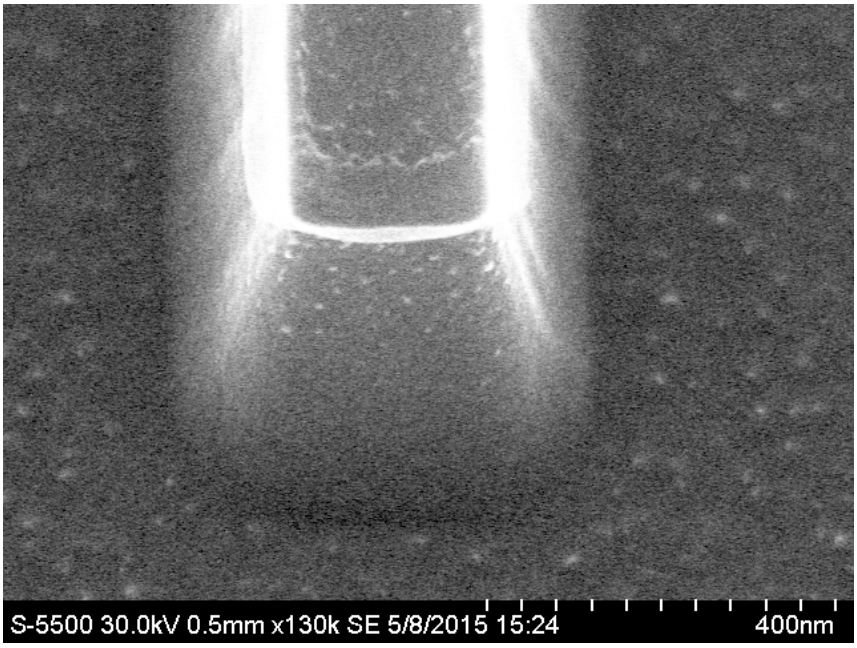


Figure 4.7: Etch number 14, showing smooth, tapered sidewalls.

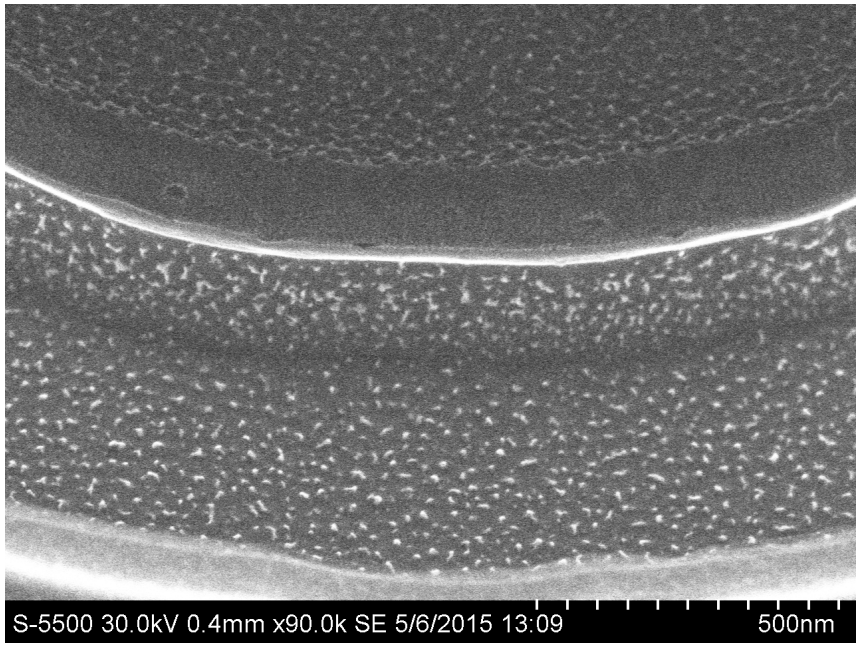


Figure 4.8: Etch number 24, showing coarser sidewalls than number 12 with the addition of 5 sccm CHF_3.

Table 4.9: List of parameters for the etch recipes that were tested on a sapphire wafer. Table temperature for all etches was 20 °C. Recipes of particular interest are highlighted.

No.	SF_6 sccm	O_2 sccm	CHF_3 sccm	RF W	ICP W	Pressure mTorr
1	7.5	0	50	40	600	15
2	3.75	0	50	40	600	15
3	7.5	0	25	40	600	15
4	7.5	2.5	50	40	600	15
5	7.5	8	50	40	600	15
6	15	0	50	40	600	15
7	7.5	0	50	100	600	15
8	7.5	0	50	100	300	15
9	12	3	0	5	0	15
10	12	3	0	10	0	15
11	12	3	0	15	0	15
12	12	3	0	20	0	10
13	12	3	0	20	0	15
14	12	3	0	20	0	25
15	12	3	0	30	0	15
16	12	3	0	40	0	5
17	12	3	0	40	0	10
18	12	3	0	40	0	15
19	12	3	0	40	200	15
20	12	3	0	40	0	20
21	12	3	0	40	0	25
22	12	3	0	40	0	40
23	12	3	0	80	0	15
24	12	3	5	40	0	15
25	12	3	10	40	0	15
26	12	4	0	40	0	15
27	12	5	0	40	0	15
28	12	6	0	40	0	15
29	12	6	5	40	200	15
30	12	6	10	40	200	15
31	14	0	35	100	0	15
32	30	12	12	100	0	15

Table 4.10: Evaluation of etch recipes. Etch rates are variable from run to run. Roughness evaluated subjectively based on SEM images on a scale from 1-3, where 1 is poor, 2 is acceptable and 3 is good. Profile is A for anisotropic, T for tapered and I for isotropic, as shown in Figure 3.8. Not all values have been measured for all recipes. For example, profile is not given for etch recipes not viewed in cross-section, as the profile is very difficult to judge from tilted imaging alone.

No.	Rough-ness	Profile	Etch rates Si [nm/s]	PMMA [nm/s]	Selectivity
1	2	A	13.3	6.7	2.0
2	1				
3	1				
4	1				
5	1				
6	1				
7	1				
8	2				
9	1				
10	1				
11	2				
12	1				
13	3				
14	3	I	5.8	1.2	4.8
15	2				
16	2				
17	2				
18	2	T	4.6	3	1.5
19	1				
20	2				
21	2				
22	2				
23	1				
24	1				
25	1				
26	2				
27	2				
28	2				
29	1				
30	1				
31	2				
32	2				

Recipe 1 Lithography Optimization

The optimization of recipe 1 was performed in two similar trials. Unfortunately, they happened at vastly different times in the project, and as such are not directly comparable. One was among the first experiments, the other among the last. Therefore, the second trial used optimizations found during later stages of the work and had as its main goal to examine the effect of using a silicon carrier wafer during etching. While varying several parameters at once is poor practice from a scientific standpoint, it must be understood that this is an engineering effort, with the quality of the resulting device being far more important than the testing of every variable.

Method

Two samples were used for cross-section testing. Sample 1 was taken from Wafer 1, with a PMMA thickness of 152 nm. Sample 2 was taken from Wafer 3 and coated with 270 nm of PMMA, as 152 nm was found to be thinner than optimal. In addition, two more samples were used for comparing the differences between etching in amorphous and monocrystalline silicon. Sample 3 was taken from Wafer 1 as well, and Sample 4 was monocrystalline, coated with 270 nm PMMA. Finally, the sample that inspired the use of Si carrier wafers is presented. This is a monocrystalline Si sample coated with 270 nm of PMMA, and is called Sample 5.

The difference between the processing of the two cross-section samples is that Sample 1 was exposed with doses between 50 $\mu C/cm^2$ and 190 $\mu C/cm^2$, while Sample 2 was exposed with 240 $\mu C/cm^2$ to 320 $\mu C/cm^2$. Also, Sample 1 was etched on a sapphire carrier, and Sample 2 on a silicon carrier.

The mask used contained long stripes that would be easy to scribe perpendicular to and examine in cross-section SEM. Furthermore, Sample 2 was patterned with waveguides and trenches of various sizes. The waveguides ranged from 500 nm to 1000 nm, and the trenches from 100 nm to 1000 nm. These were imaged and measured in SEM after the cross-section measurements verified a good etch.

Knowing the actual size of an etched feature is crucial in order to make waveguides of the correct dimensions. For example, using the wrong trench width between a waveguide and a resonator can ruin the whole device by selecting a poor coupling coefficient or even fusing the two together. The effect of changing carriers was not examined until late in the project, making Sample 2 the last test before the fabrication of waveguides made for characterization.

Samples 3 and 4 were both exposed with 180 $\mu C/cm^2$ to 260 $\mu C/cm^2$. The features examined were rings, which have the useful property of allowing the experimenter to examine sidewalls from an angle perpendicular to the feature no matter which way the sample is rotated. In contrast, a straight wall that has been rotated on the sample holder will restrict

the viewing angle, as the Hitachi S-5500 S(T)EM does not have hardware in-plane stage rotation.

All samples were etched using Recipe 1, with the parameters given in Table 4.9. Rate and selectivity tests were performed on PMMA and SOI samples.

Results

Rate and selectivity testing on a sapphire wafer revealed a PMMA etch rate of 7.1 nm/s and a Si etch rate of 14.3 nm/s. Thus, it would take only 15.4 s to etch through the target thickness of 220 nm. This is a very short etch time, and considering that it usually takes 2-3 s to ignite the plasma, a successful etch depends on an operator being seated at the ICP-RIE and counting every second of plasma. This is necessary because it always takes a few seconds before the plasma ignites, and with a very short etch time knowing how many seconds elapsed before ignition is significant. Clearly this is an issue for reproducability as the difference between under- and overetching is only a few seconds. However, the selectivity is 2, which is acceptable for our purposes.

The same tests on a silicon wafer revealed a PMMA etch rate of 7.7 nm/s and a Si etch rate of 8.3 nm/s. This yields a selectivity of approximately 1.1. While the etch time is increased to 28.6 s, the full 270 nm of resist will be necessary, and making it thinner for improved resolution is not an option.

Samples 1 and 2 Figures 4.9 to 4.12 show a few examples of the cross-sections examined. For Sample 1, it appears that while the top edge is rounded at lower doses, the profile becomes straighter at 180 µC/cm^2. The floor around the waveguide also appears to be less rough, indicating that 110 µC/cm^2 may be underexposed.

In Sample 2, shown in Figures 4.11 and 4.12, the corners are still rounded, but the higher resolution of the images reveals a sharper corner possibly hiding in the background. The rounded corners may thus be a result of mechanical damage from the scribing, and not something that remains constant over the whole waveguide. Unfortunately, this is difficult to verify, and it is even harder to determine if it is the case with the sapphire carrier etch as well. While AFM may not have high enough resolution due to tip convolution[58], tomographic FIB-SEM[25] should be able to examine the corners much more closely. However, this is a complicated, time-consuming and expensive technique which may be of minimal benefit in this case.

While it is not known with certainty if the corners are perfect or not, it is clear that the profile does not change when the dose increases by as much as 50%. Increasing the dose will however increase the necessary write time. Therefore, the lowest dose with low roughness was examined further for width measurements. This dose was 260 µC/cm^2, shown in Figure 4.13.

While some chips in the edges are apparent, these are marginally better than when using other doses.

The comparison of exposed and measured widths is shown in Figure 4.14. The trenches are found to be wider than the exposed width, and correspondingly the waveguides are narrower. Linear regression shows the width of the trenches and waveguides to be

$$w_{\text{trench}} = w_{\text{mask}} + 112 \text{ nm} \tag{4.1}$$

$$w_{\text{waveguide}} = w_{\text{mask}} - 55 \text{ nm}. \tag{4.2}$$

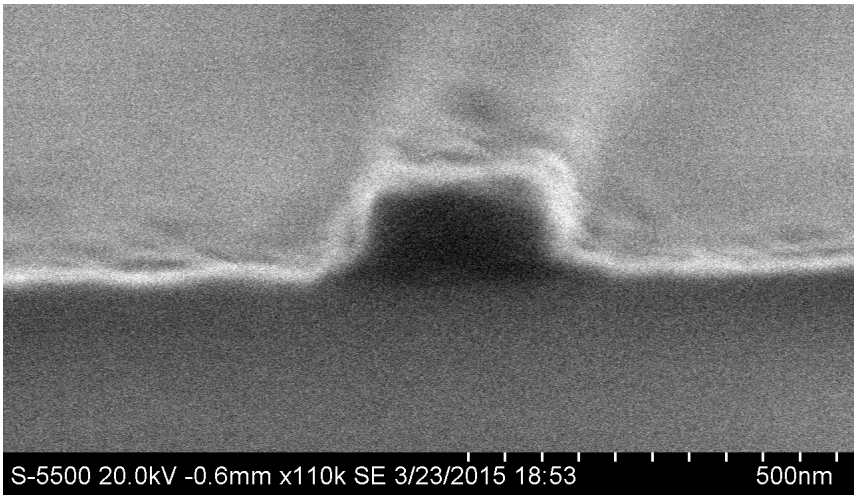


Figure 4.9: Cross-section image of waveguide etched with Recipe 1 at a dose of $110\,\mu\text{C/cm}^2$ on a sapphire carrier. Substrate is clearly rough, indicating underexposure.

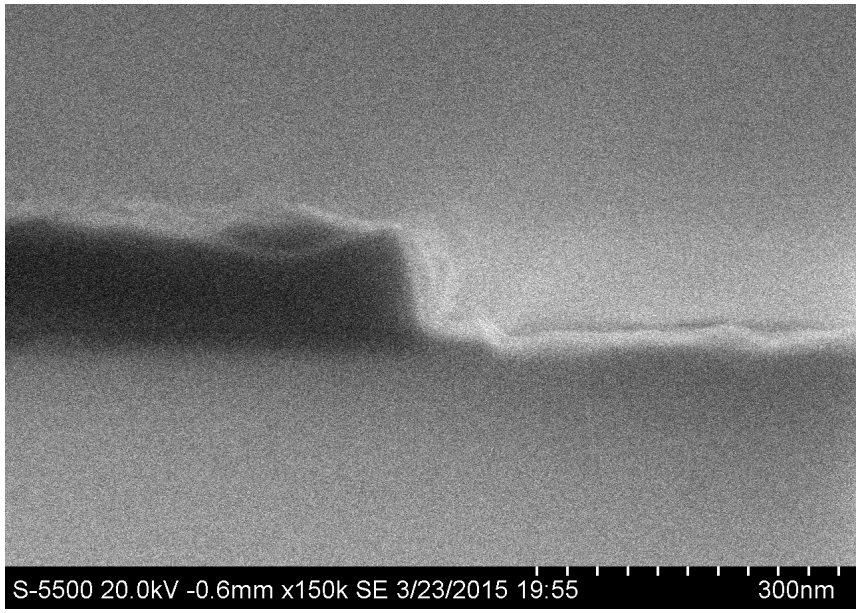


Figure 4.10: Cross-section image of nearly vertical sidewalls etched with Recipe 1 at a dose of $180\,\mu C/cm^2$ on a sapphire carrier.

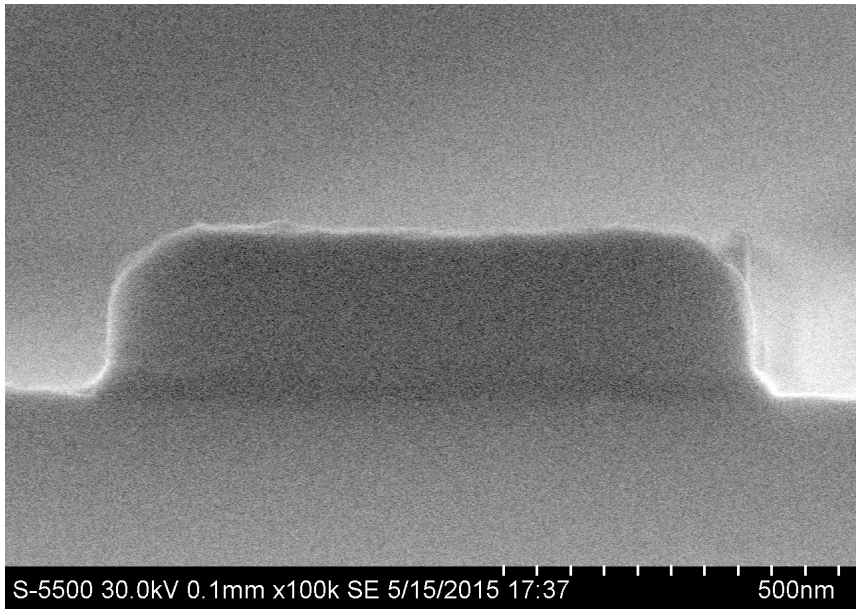


Figure 4.11: Cross-section image of nearly vertical sidewalls etched with Recipe 1 at a dose of $240\,\mu C/cm^2$ on a silicon carrier. Profile significantly better than on features etched with a sapphire carrier.

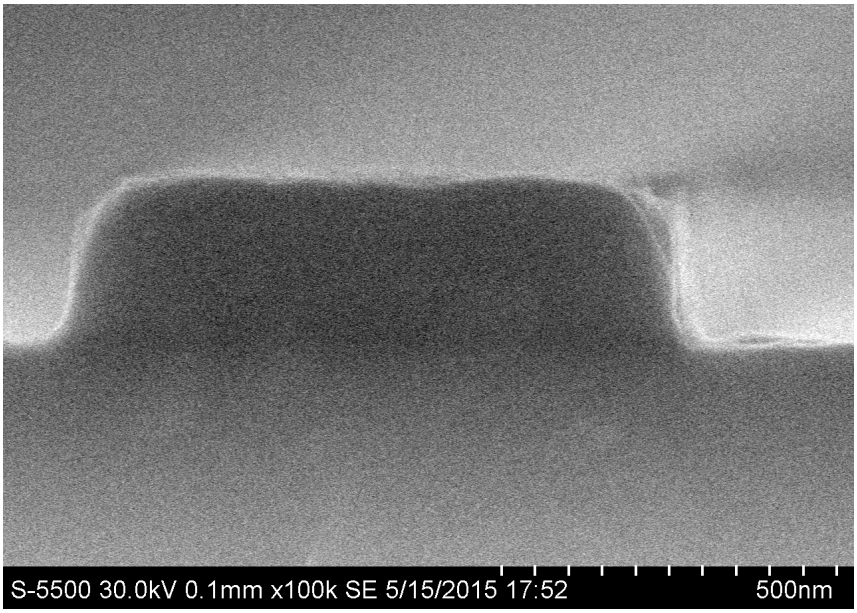


Figure 4.12: Cross-section image of nearly vertical sidewalls etched with Recipe 1 at a dose of 320 µC/cm^2 on a silicon carrier. Quality seemingly independent of dose.

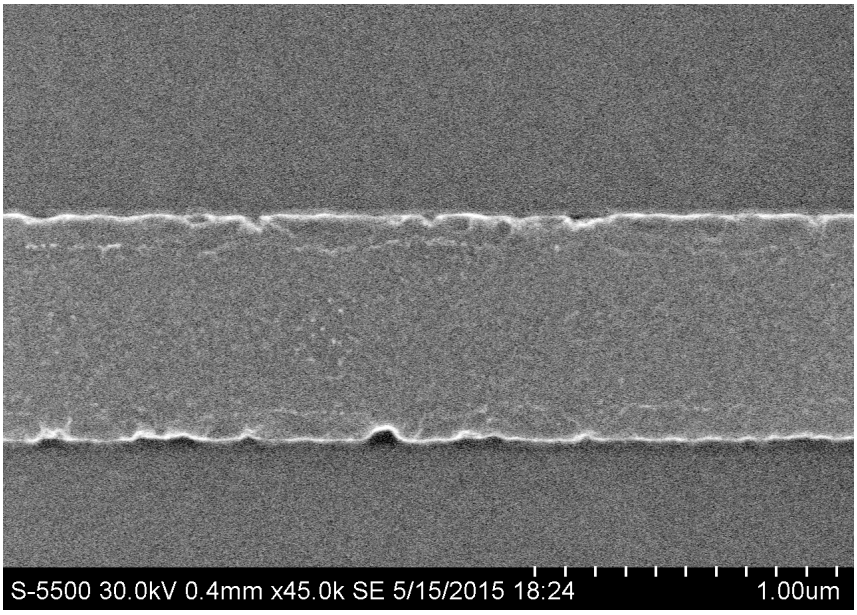


Figure 4.13: Top view of feature etched with Recipe 1 at a dose of 260 µC/cm^2 on a silicon carrier. Roughness is small compared with lower doses.

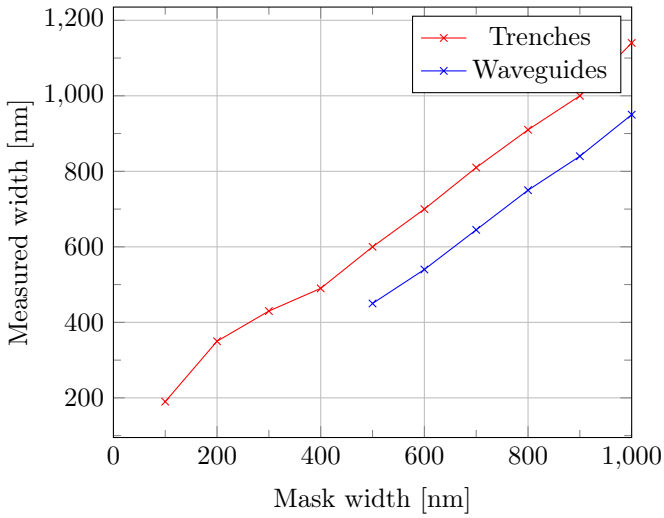


Figure 4.14: Exposed and measured widths of waveguides and trenches in Sample 2, exposed with a dose of 260 $\mu C/cm^2$ and etched on a Si carrier wafer.

Samples 3, 4 and 5 Sample 3 did not show any major changes to the etch profile at doses of 220 µC/cm^2 or larger. However, at 180 µC/cm^2 as shown in Figure 4.15 the sidewalls have large ridges jutting out, and the substrate is unevenly etched. This is a common sign of underexposed resist, as residues remain on the surface and inhibit the etch. Figure 4.16 shows much better exposure, with the outline of the etch following the intended shape without aberrations. However, in both cases the sidewalls have significant roughness.

Sample 4 showed the same issues. Figure 4.17 is far, far worse than even the worst results from Sample 3. Figure 4.18 is of similar quality to Figure 4.15, at a much higher dose. Meanwhile, the highest dose of 260 µC/cm^2 as shown in Figure 4.19 yields good results.

Comparing Samples 3 and 4, it is evident that while a higher dose is necessary when exposing a thicker resist, the end result looks similar. The roughness of the sidewalls is quite bad in both cases, giving them the appearance of a sponge. However, the features follow their intended shape without large defects.

Sample 5, shown in Figure 4.20, has no visible roughness. The sidewalls are smooth and vertical, although there is some unevenness. This unevenness seems rather periodic, and may be the result of the EBL's rasterization of the circle. Unfortunately, further characterization of etching with a silicon carrier was restricted due to time considerations. It is obvious that for improving the sidewall quality, a silicon carrier can make a huge difference.

While not widely explored in the literature, the theory presented by NTNU engineer Tron Arne Nilsen is that the silicon carrier consumes the chemical etching agent, keeping it from diffusing onto the sample and etching isotropically. Sapphire, being very inert, has no effect on the etchants. This idea is supported by the fact that the etch rate was reduced after switching to the silicon carrier. It may be worthwhile to investigate these effects more systematically as there appears to be a hole in the literature.

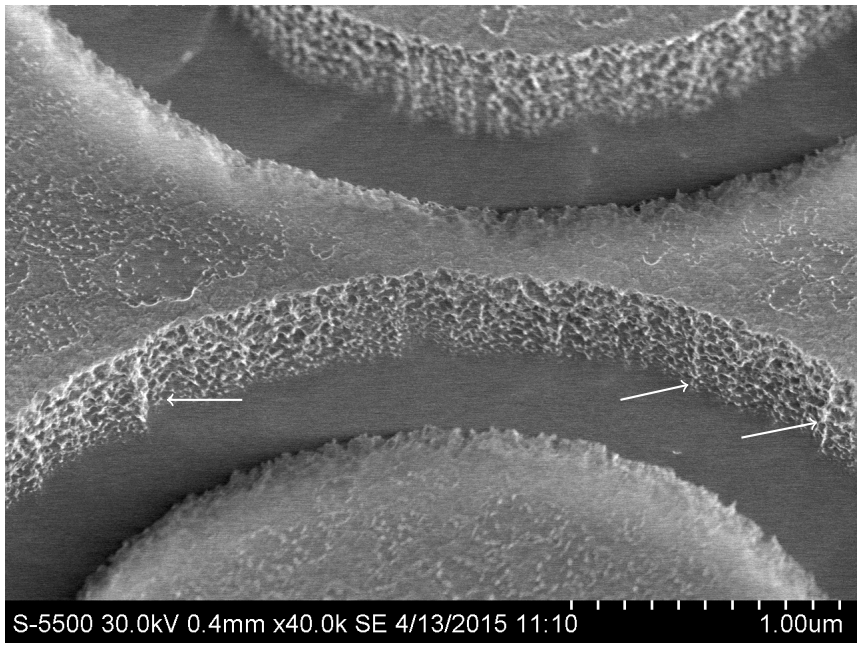


Figure 4.15: Sample 3, exposed with $180\,\mu C/cm^2$ and etched with Recipe 1. Sidewalls are rough and there is evidence of underexposure in the form of vertical ridges, highlighted by arrows.

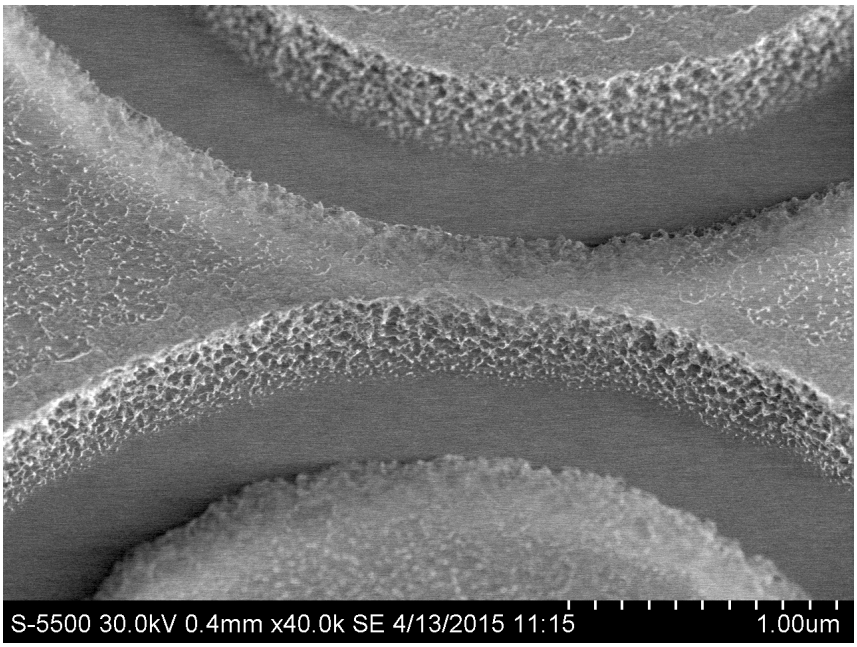


Figure 4.16: Sample 4, exposed with $260\,\mu C/cm^2$ and etched with Recipe 1. While microscopic roughness is still present, the macroscopic roughness of Figure 4.15 is gone.

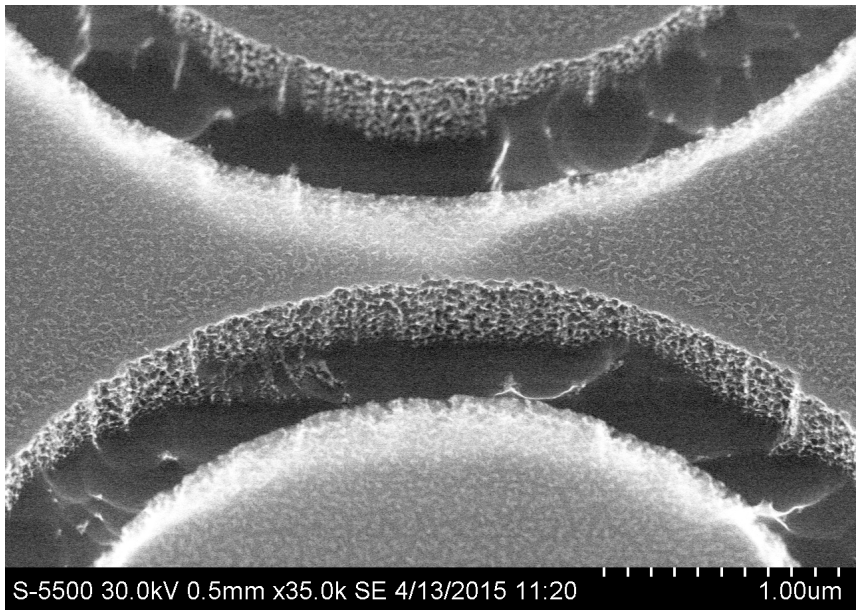


Figure 4.17: Sample 4, exposed with $200\,\mu C/cm^2$ and etched with Recipe 1. The sidewalls are uneven and the bottom of the trenches have the appearance of rough sea.

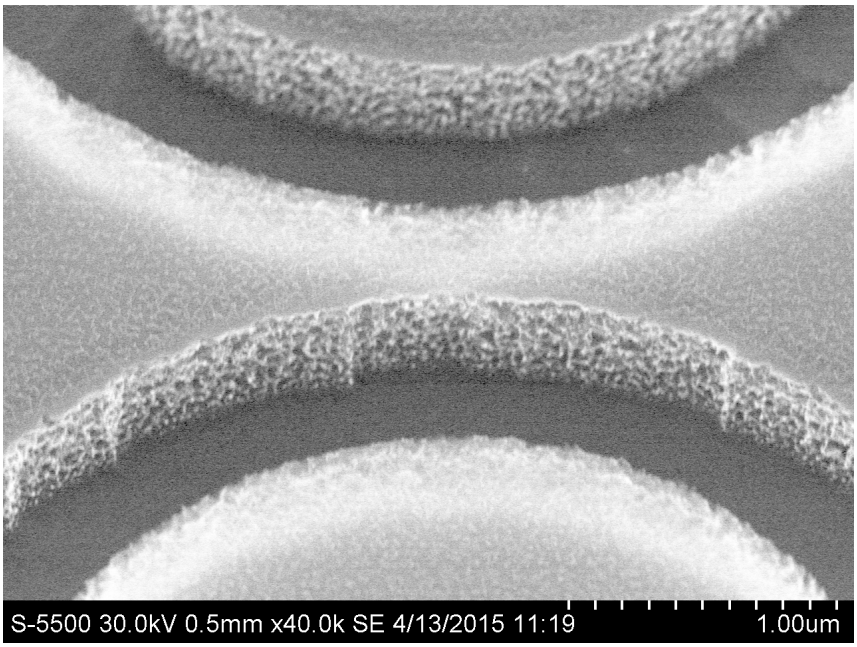


Figure 4.18: Sample 4, exposed with 240 µC/cm^2 and etched with Recipe 1. The overall quality of the etch is on the same level as for 180 µC/cm^2 on 152 nm thick resist.

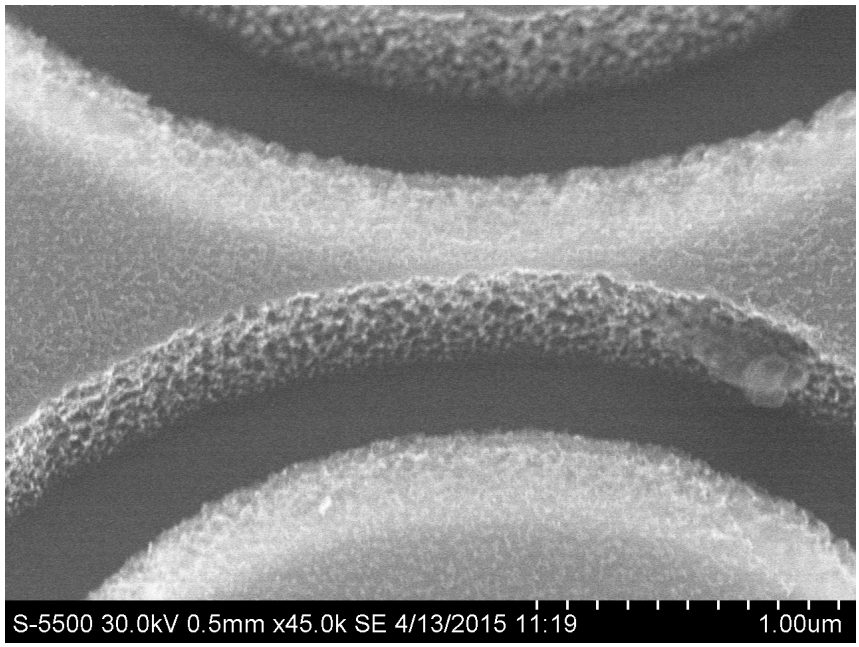


Figure 4.19: Sample 4, exposed with 260 µC/cm^2 and etched with Recipe 1. The outline of the etched area is smooth, owing to the higher exposure dose.

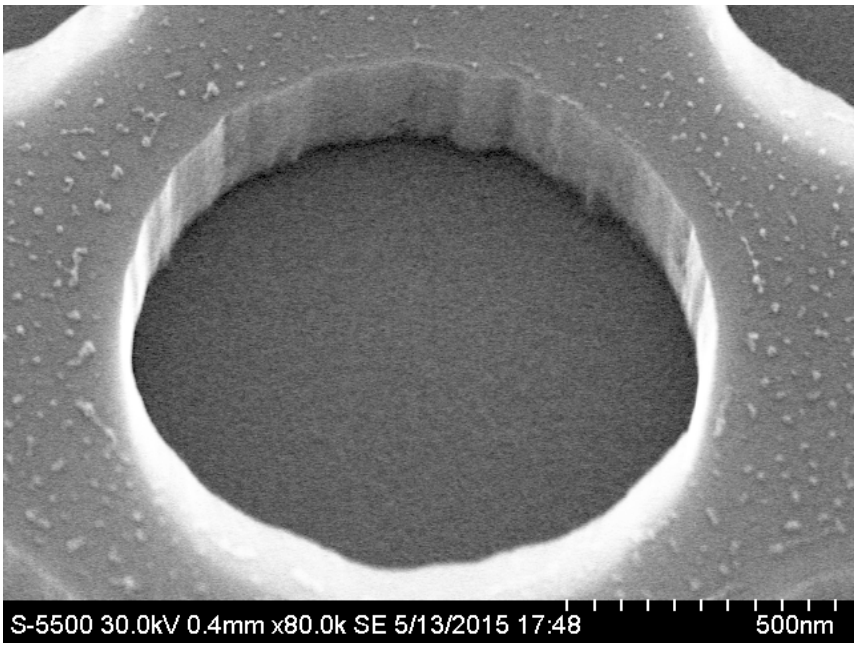


Figure 4.20: Sample 5, monocrystalline silicon exposed with 240 µC/cm^2 and etched with Recipe 1 on a silicon carrier wafer. Very smooth and vertical sidewalls.

Recipe 18 Lithography Optimization and Hardmask

Recipe 18 was found by Jens Høvik to be superior at a later stage in the project, after the initial sapphire etch experiments with Recipe 1. While only a few experiments were performed with it before Recipe 14 was developed, the results are presented here. Due to its length, this section is divided into separate parts for lithography and hardmask testing.

One technique that is commonly used for improving nanostructure quality is the hardmask[37]. In this technique, a top layer called a hardmask is deposited on the material to be etched. This top layer is usually a nitride, oxide or ceramic with a high etch selectivity to the substrate. Standard lithographical techniques are used to transfer a pattern to the hardmask. The main advantage is higher aspect ratio features and better resolution[35]. Another advantage is that the hardmask material may be able to withstand processes that would destroy polymer-based photoresists, such as KOH etching of silicon[38]. A mask that is not etched will also not be part of the etch chemistry, which can be advantageous or disadvantageous depending on the specifics of the process[53]

Method

Table 4.11: Samples used for testing Recipe 18

No.	Wafer	Resist thickness [nm]
1	W1	152
2	Monocrystalline	270
3	W3	270
4	W2	115

Lithography The samples were as described in Table 4.11. Due to the differences in thickness, the samples received different dose ranges: Sample 1 received 120 µC/cm^2 to 180 µC/cm^2 and Samples 2 and 3 received 170 µC/cm^2 to 230 µC/cm^2. The exposed mask contained lines, which were examined in cross-section SEM after scribing and breaking.

In addition, Sample 1 was exposed with rings, for viewing the sidewalls. This was not done on Sample 2 due to time constraints on the day of the experiments. Sample 3, however, was made on another day and contained waveguides ranging from 400 nm to 1000 nm in addition to the lines. The width of these waveguides was measured in SEM, between the top edges of the waveguide.

All samples were etched using Recipe 18 on a sapphire carrier, with the parameters given in Table 4.9. Rate and selectivity tests were performed on PMMA and SOI samples.

Hardmask

First, a suitable hard mask thickness had to be determined. This was done by testing the Si to SiO_2 selectivity of Recipe 18, which was the best one known at this point in the project. The test had to be performed by etching SiO_2 and PMMA samples side by side and comparing with the known PMMA/Si selectivity. It would have been better to test SiO_2 against Si directly, but due to the high expected selectivity it would have been necessary to grow a new, thicker Si sample in order to see any appreciable etching in the SiO_2. Based on the results a thickness of 50 nm was selected for Wafer 2, as mentioned in Section 4.1.

The SiO_2 etch recipe built into the ICP-RIE chiller was characterized by etching a PMMA and a SiO_2 coated sample side by side and measuring the selectivity and etch rate. The etch parameters are given in Table 4.12.

Table 4.12: Etching parameters for SiO_2 etch.

Parameter	Value
Ar	25 sccm
CHF_3	25 sccm
RF	100 W
ICP	200 W
Pressure	50 mTorr
Table temp	20 °C

Sample 4 was taken from Wafer 2. The sample was spin coated with 950K PMMA A3 at 5000 RPM, for a thickness of 115 nm. A pattern of various test structures was transferred using EBL, at doses ranging from 90 µC/cm^{2}to 150 µC/cm^2. This was done three times on the same sample.

The sample was etched for 60 s using the SiO_2 etch recipe, and the remaining PMMA layer was stripped using acetone and O_2 plasma ashing. Following this, the sample was scribed into three parts, each to be etched separately.

The Si etch rate was measured by etching a PMMA coated sample and comparing the etch rate with the known selectivity of 1.5. One was etched 10 nm, just enough to remove the Si layer, one 20 seconds more in order to hopefully remove all the hardmask, and one in between the two extremes. The purpose of this was to find the effect of overetching with a hardmask in place, where it would be possible to overetch for a long time without destroying the mask.

Samples were examined in SEM, both in cross-section and from above. Due to issues explained in the results section, the top SiO_2 layer had to be removed before viewing the samples from above.

Results

Lithography Rate and selectivity testing on a sapphire wafer revealed a PMMA etch rate of 3 nm/s and a Si etch rate of 4.6 nm/s. Thus, it would take 48 s to etch through the target thickness of 220 nm. This is a very controllable rate. The typical plasma ignition time of 2 s is negligible compared to the etch time, so it should be safe to set the etch time to 50 s, possibly including a small safety buffer of 2 s. The selectivity of 1.5 is poor and will require relatively thick resist layers.

Figure 4.21 shows the sidewall profile achieved on amorphous SOI exposed with a dose of 180 µC/cm^2. While dirty, it is clear that the sidewall is straight and close to vertical. Interestingly, the same result is achieved in monocrystalline silicon, as shown in Figure 4.22, exposed with a dose of 230 µC/cm^2.

Furthermore, the features etched with Recipe 18 can be seen in Figures 4.25 and 4.26, with 180 µC/cm^2 and 150 µC/cm^2, respectively. As seen previously, increasing the dose seems to improve the macroscopic roughness of the features.

The effect of a thicker resist, in addition to a higher required dose, can be seen by comparing the aforementioned images to Figures 4.23 and 4.24. The differences do not appear to be dramatic, and measuring the sidewalls reveals the slope to be 66° in both cases.

The width of the waveguides can be read out of Figure 4.27. Counterintuitively, the waveguides etched with a lower dose are narrower than the ones etched with a higher dose, up to a point. This is strange because the waveguide itself is not being exposed, it is the cladding that is removed in the EBL processing.

Using linear regression on the two datasets reveals the following expressions for waveguide width:

$$w_{\text{waveguide},200} = 0.93 w_{\text{mask}} - 255 \text{ nm} \tag{4.3}$$

$$w_{\text{waveguide},230} = 1.24 w_{\text{mask}} - 490 \text{ nm}. \tag{4.4}$$

In the analysis of the other etch recipes, the slope has been assumed to be equal to 1 for physical significance, and this has been very close to being true. It would be expected that the width of the final feature is simply the exposed width plus some offset. In this case, however, the linear dependence is deviating significantly from unity. If these results are to be used for making decisions on waveguide geometry, the experiment should be repeated.

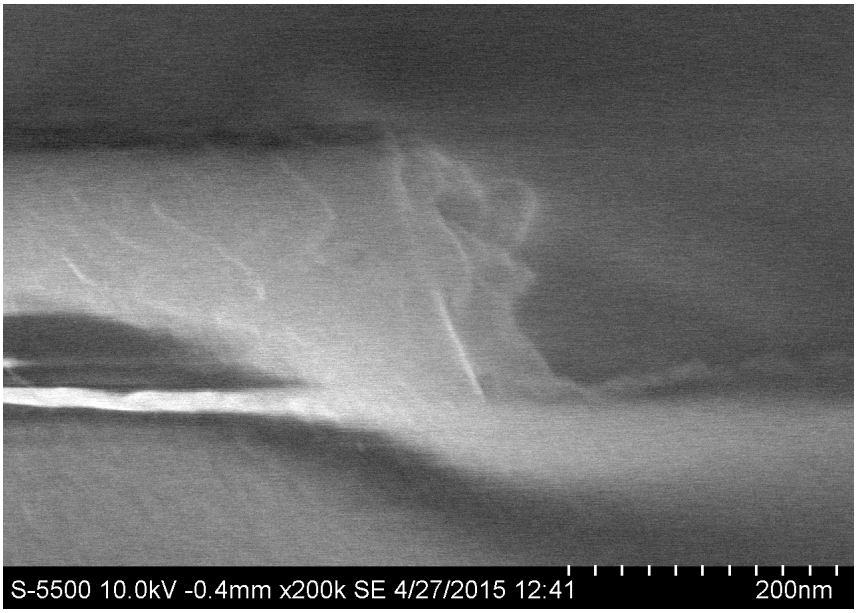


Figure 4.21: Cross-section image of slightly tapered sidewalls etched in amorphous SOI with Recipe 18 at a dose of 180 $\mu C/cm^2$ and with 270 nm thick resist.

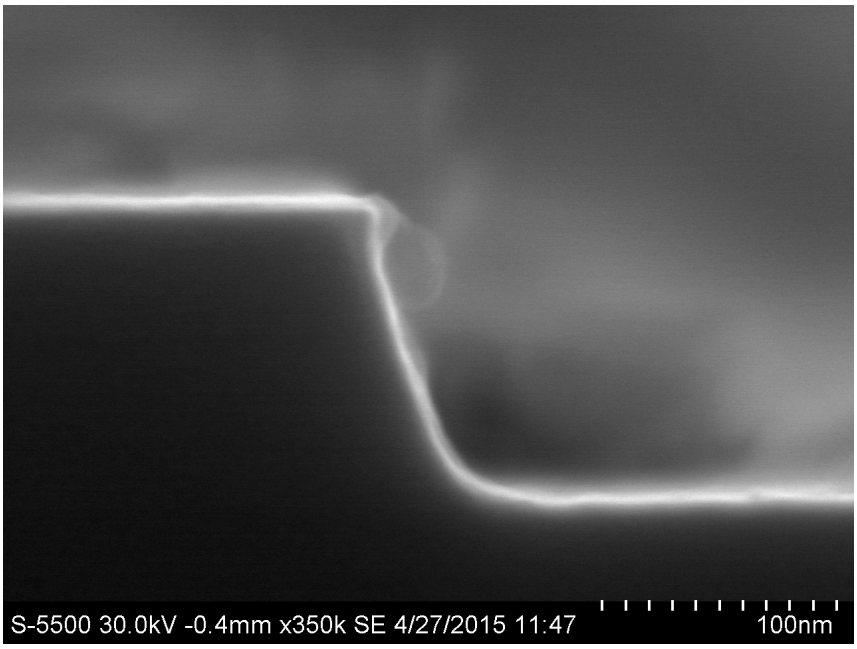


Figure 4.22: Cross-section image of slightly tapered sidewalls etched in crystalline silicon with Recipe 18 at a dose of 230 $\mu C/cm^2$.

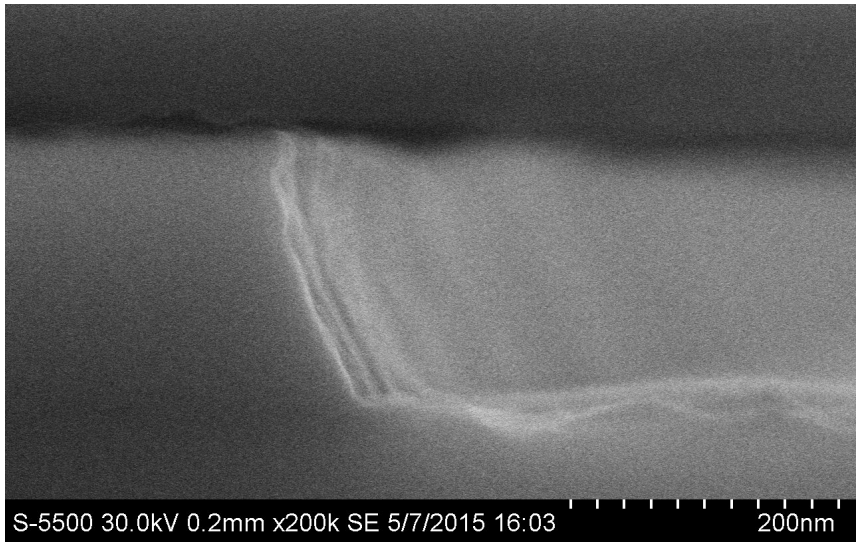


Figure 4.23: Cross-section image of slightly tapered sidewalls etched in amorphous SOI with Recipe 18 at a dose of $200\,\mu C/cm^2$ and 270 nm thick resist.

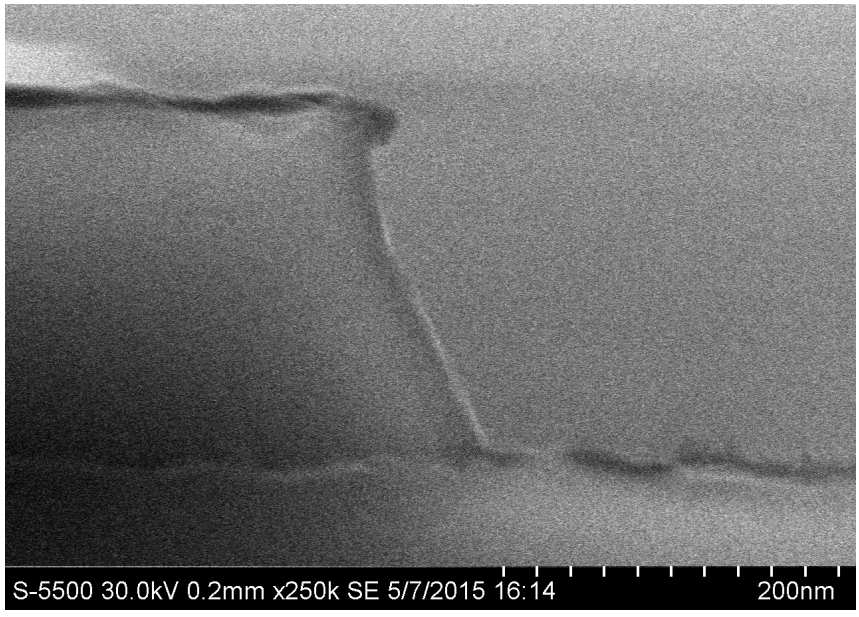


Figure 4.24: Cross-section image of slightly tapered sidewalls etched in amorphous SOI with Recipe 18 at a dose of $240\,\mu C/cm^2$ and 270 nm thick resist.

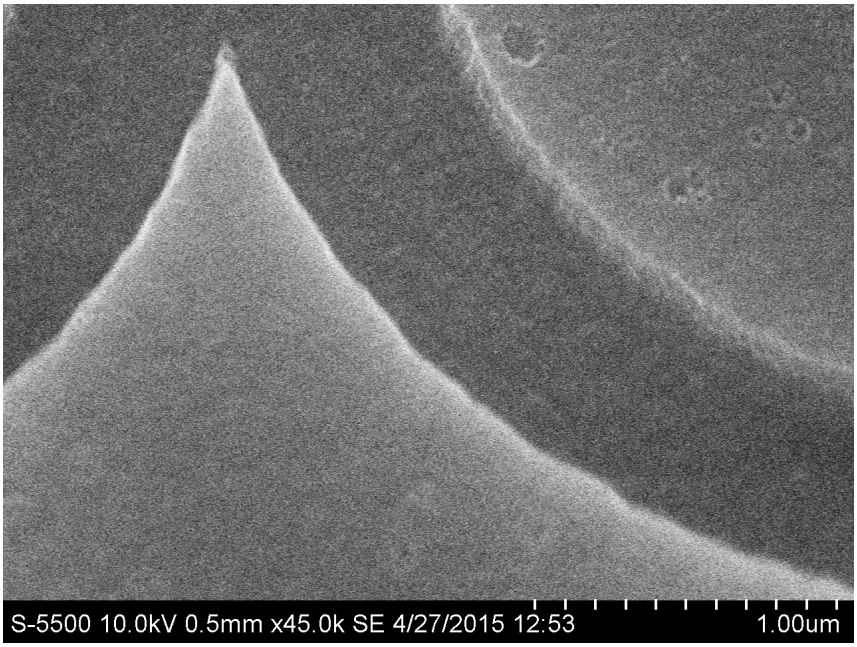


Figure 4.25: Tilted image showing a ring etched in amorphous SOI with Recipe 18 at a dose of $180\,\mu C/cm^2$. Sidewalls are visibly smooth, but the features are somewhat rough.

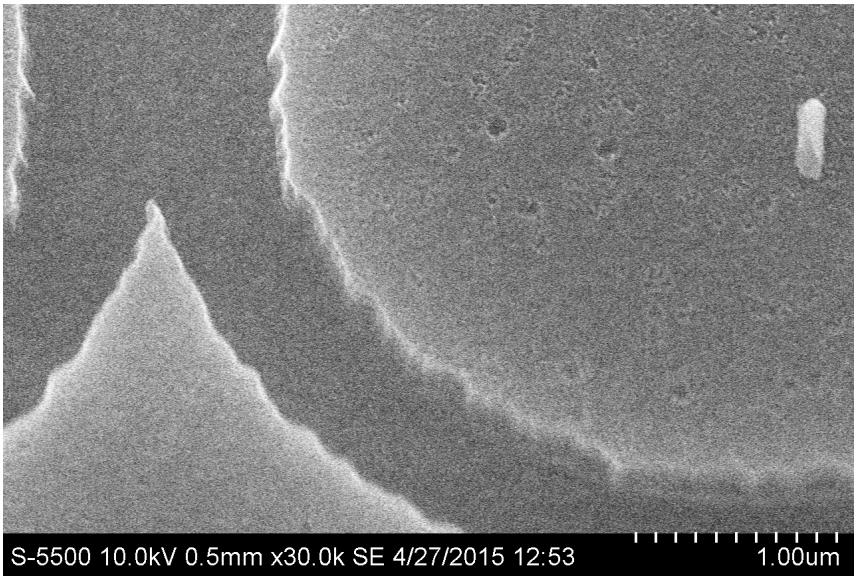


Figure 4.26: Tilted image showing a ring etched in amorphous SOI with Recipe 18 at a dose of $150\,\mu C/cm^2$. The quality of the features is much lower than with a higher dose.

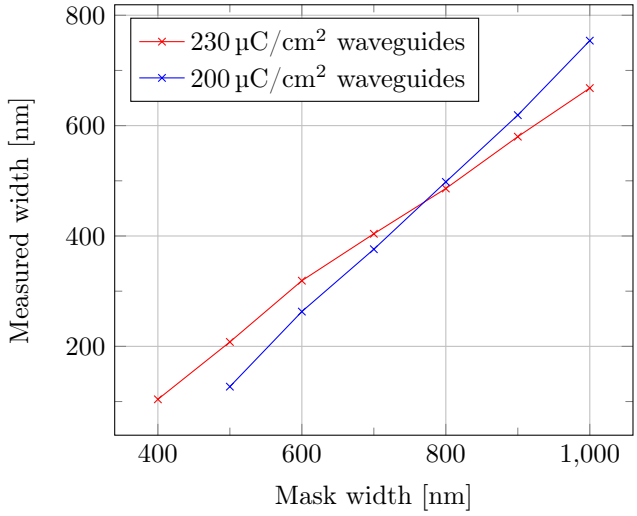


Figure 4.27: Exposed and measured widths of waveguides exposed with different doses.

Hardmask Etch characterisation of Recipe 18 revealed etch rates to be 2.4 nm/s for PMMA and 0.63 nm/s for SiO_2. This yields a selectivity of 3.8 between and PMMA and SiO_2. Recipe 18's Si to PMMA selectivity of 1.5 thus yields a Si to SiO_2 selectivity of 5.7. Thus, 50 nm of SiO_2 should be able to protect as much as 285 nm of Si.

The characterization of the SiO_2 etch recipe revealed the etch rate in SiO_2 to be 1 nm/s, and 2 nm/s in PMMA.

Sample inspection showed a remarkable amount of isotropy, shown in Figures 4.28 and 4.29 While the upper parts of the sidewalls are somewhat vertical, they are shown to widen further down. The over-etched image also shows an indentation into the underlying SiO_2 layer, clearly showing that the etch is capable of digging into the oxide.

While the undercut is less for the shorter etch time, it is still not negligible, and will add up to a total of 400 nm when counting both sides of the waveguide. Furthermore, with an additional 200 nm undercut per side during 20 seconds of extra etching, it is clear that it would not be easy to control the waveguide width.

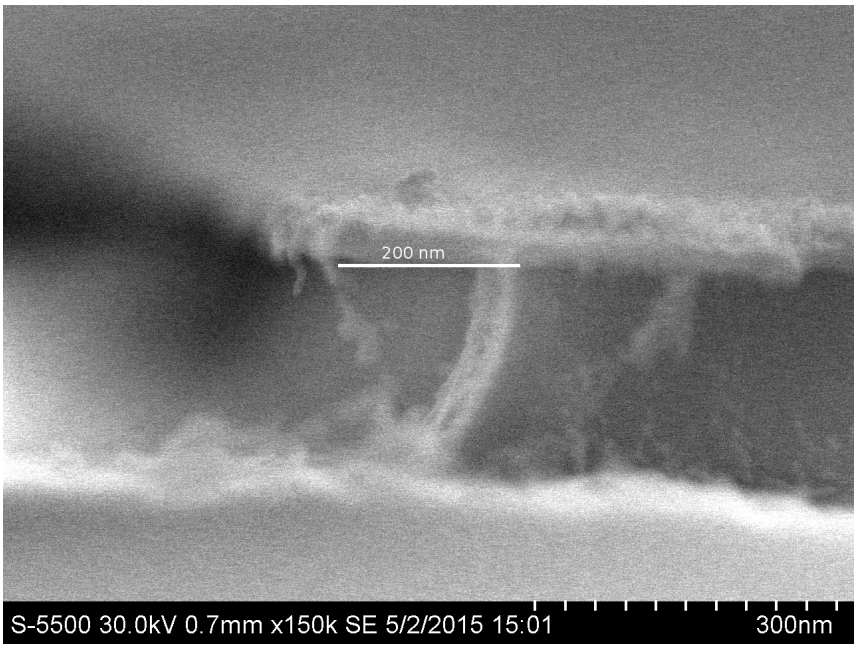


Figure 4.28: Just sufficiently etched features made with hardmask, showing less undercut than the over-etched version.

Due to the remaining oxide mask hanging over the features, getting a good look at the sidewalls from above required stripping away the oxide. The same etch recipe used for patterning the oxide was used for the etchback.

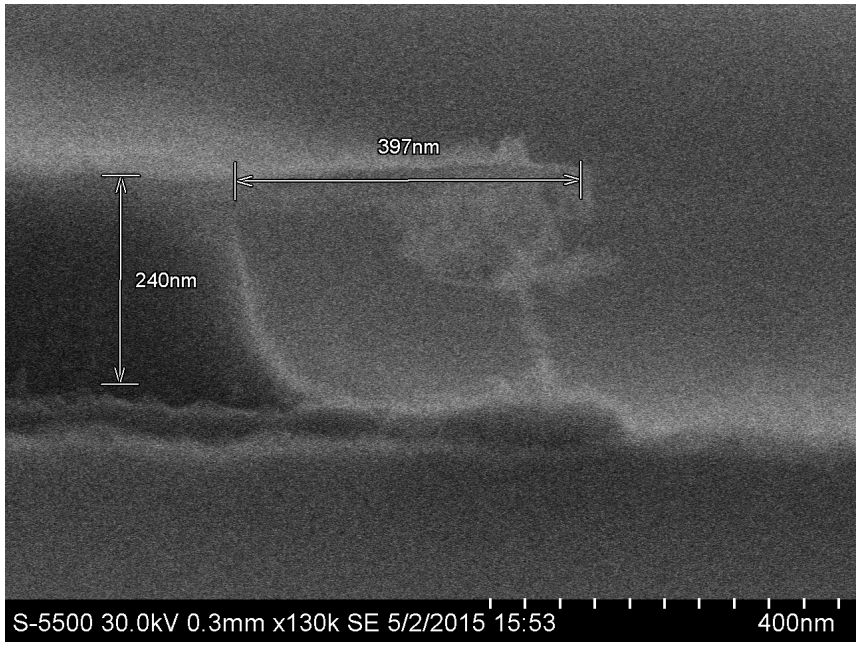


Figure 4.29: Over-etched features made with hardmask, showing dramatic undercut.

A cross feature is shown from above in Figure 4.30. This feature looks acceptable, with very straight lines and a sharp angle at the corner. However, the surfaces look very rough. This roughness is examined closer in Figure 4.31. Unfortunately, the composition of the roughness could not be examined as the EDS detector was out of order at the time of the experiment.

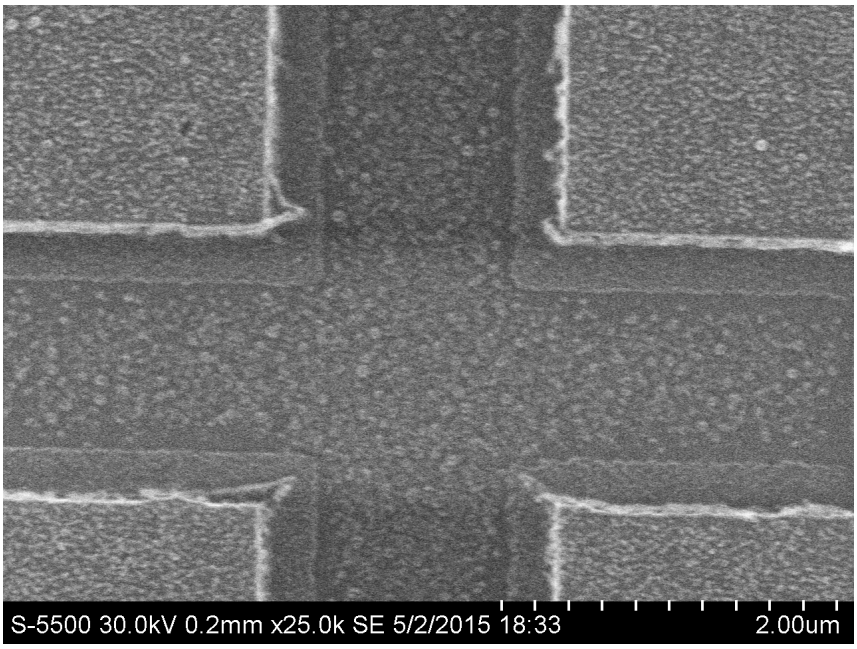


Figure 4.30: Cross etched using hardmask, after etchback.

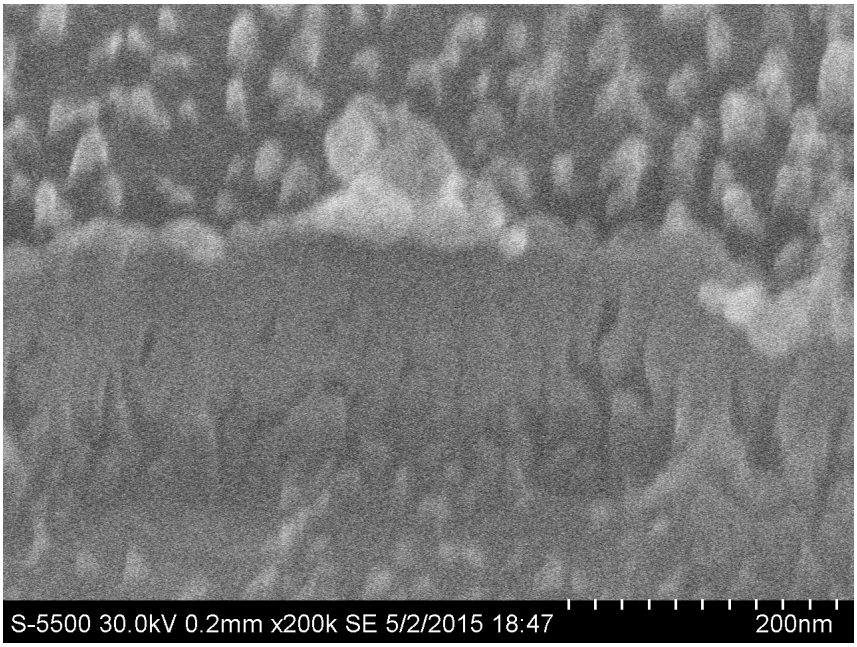


Figure 4.31: Sidewalls of cross etched using hardmask, after etchback.

Recipe 14 Lithography Optimization

Recipe 14 was discovered as an improvement upon Recipe 18 at a relatively late stage in the project. At this point, trials on monocrystalline silicon were no longer considered interesting, as it was clear that manufacturing waveguides on commercial SOI would be outside the scope of this work. Therefore, experiments were restricted to comparing different carrier wafers and doses and determining the correct dimensions to be used in the mask design.

Method

Sample 1 and Sample 2 were both prepared from Wafer 3, with 205 nm of silicon on top of the oxide. Both were spin coated with 85 nm of PMMA and exposed with doses of 100 µC/cm^2 to 180 µC/cm^2, lower than previous exposures due to the thinner resist layer. The mask contained straight lines to be examined in cross-section SEM, and arrays of waveguides and trenches of varying width. The waveguides ranged from 500 nm to 1000 nm, and the trenches from 100 nm to 1000 nm. These were imaged and measured in SEM after the cross-section measurements verified a good etch.

All samples were etched using Recipe 14, with the parameters given in Table 4.9. Rate and selectivity tests were performed on PMMA and SOI samples.

Samples with a 270 nm PMMA layer were also made, but inspection revealed these to be entirely destroyed due to a contaminated resist bottle.

Results

Rate testing with a sapphire carrier revealed an etch rate of 5.8 nm/s on Si and 1.2 nm/s on PMMA for a selectivity of 4.8. This is an absolutely astounding selectivity and a comfortably low etch rate. With a Si carrier, the Si etch rate was lowered to 2.5 nm/s and the PMMA rate to 0.85 nm/s, for a selectivity of 2.9. The lower rates and lower selectivity corresponds well to a more physical etch where the chemical species tend to disappear after the first encounter with the carrier. Even so, a selectivity of 2.9 is excellent, and allows an 85 nm thick layer of resist, as the low etch rate makes overetching unlikely.

While the sidewall profile was found to be independent of exposure dose, doses lower than 140 µC/cm^2 underexposed the resist, leaving a rough surface and low quality features. The choice of carrier wafer had a notable effect on the profile. Figure 4.32 shows the profile when a sapphire carrier was used, Figure 4.33 with a silicon carrier. While the etch has an isotropic profile with a sapphire carrier, the profile becomes markedly tapered when the material is changed.

Interestingly, Figures 4.36 and 4.37 show that the width of the features is nearly independent of the choice of carrier wafer. This implies that the source of the isotropy is not that the etch is eating into the top of

the waveguide, but rather that the bottom is being etched progressively slower. A mechanism that could be causing this is redeposition[36].

Applying linear regression to the width of the waveguides and requiring a slope of 1 yields an intersect of 190. Applying the same method to the trenches reveals an intersect of 203. Thus,

$$w_{\text{trench}} = w_{\text{mask}} + 203 \text{ nm} \tag{4.5}$$

$$w_{\text{waveguide}} = w_{\text{mask}} - 190 \text{ nm}. \tag{4.6}$$

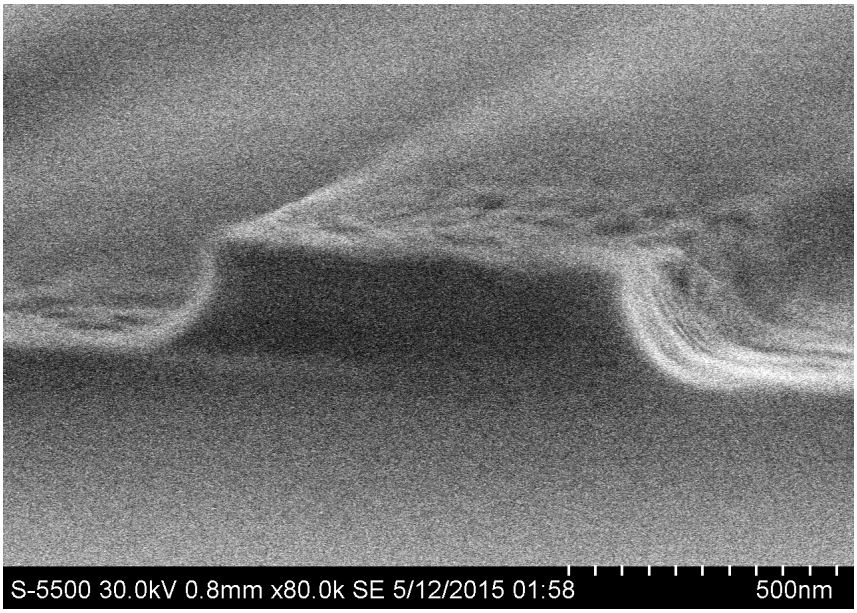


Figure 4.32: Cross-section image of waveguide etched with Recipe 14 at a dose of $180\,\mu C/cm^2$ on a sapphire carrier. Image is taken at an angle of incidence of 1° for higher resolution. The etch profile is somewhat isotropic.

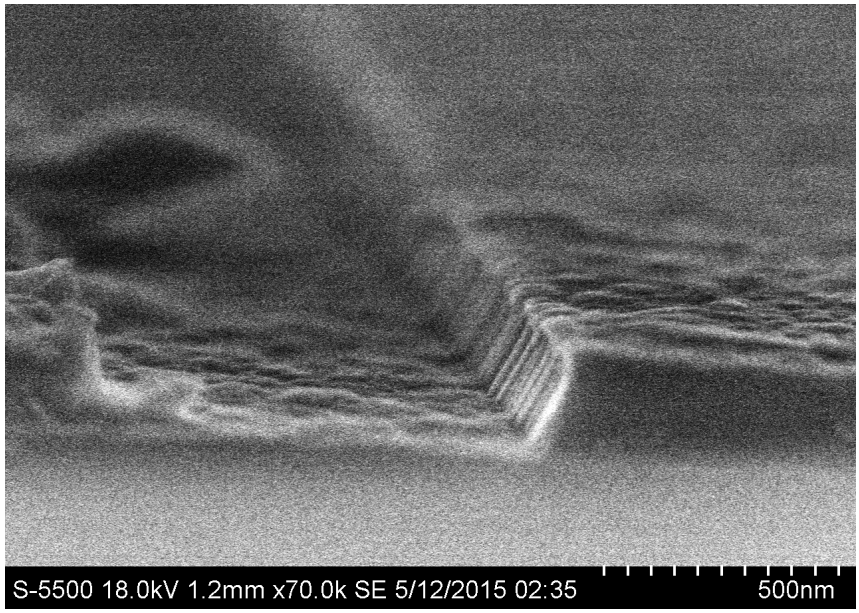


Figure 4.33: Cross-section image of waveguide etched with Recipe 14 at a dose of 180 µC/cm^2 on a silicon carrier. Image is taken at an angle of incidence of 1° for higher resolution. The etch profile is tapered, in contrast with the isotropic results achieved with a sapphire carrier.

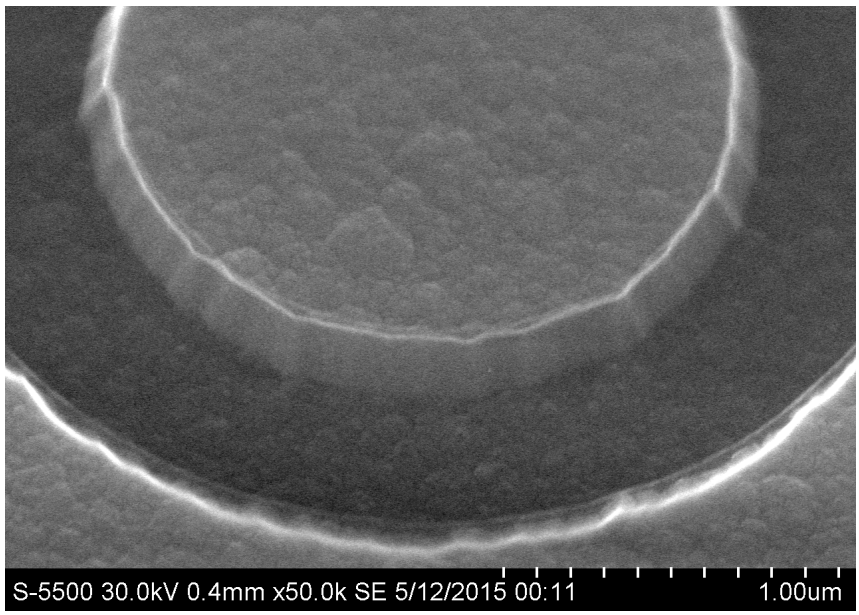


Figure 4.34: Tilted view of a ring on a sapphire carrier. Sidewalls are smooth. Exposure dose 180 µC/cm^2.

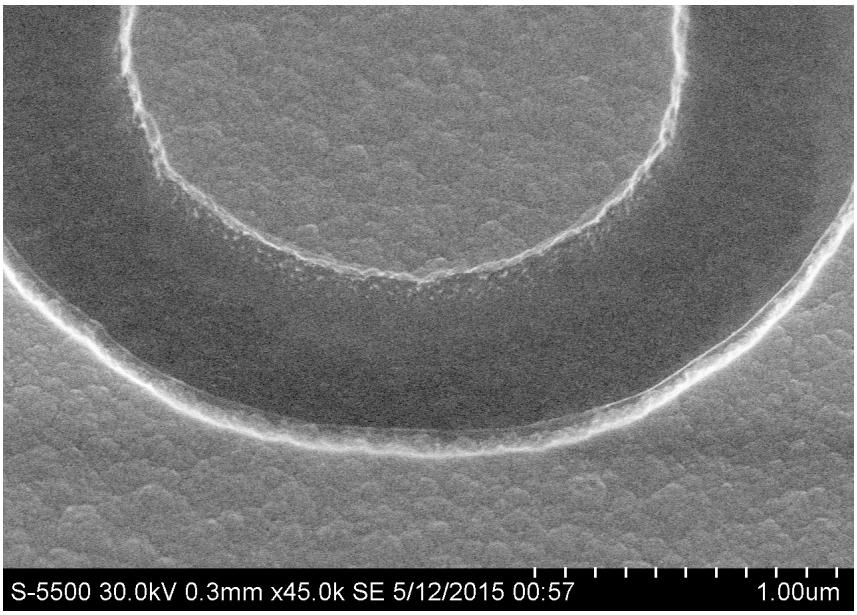


Figure 4.35: Tilted view of a ring on a silicon carrier. Sidewalls appear somewhat rougher than with the sapphire carrier. Exposure dose 180 µC/cm^2.

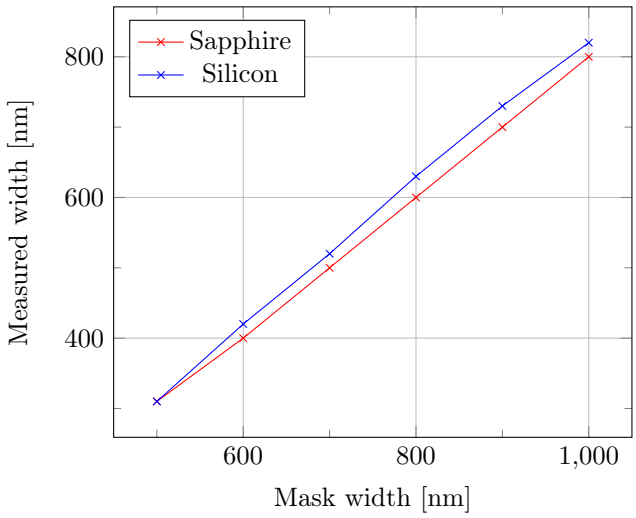


Figure 4.36: Exposed and measured widths of waveguides exposed with 180 µC/cm^2.

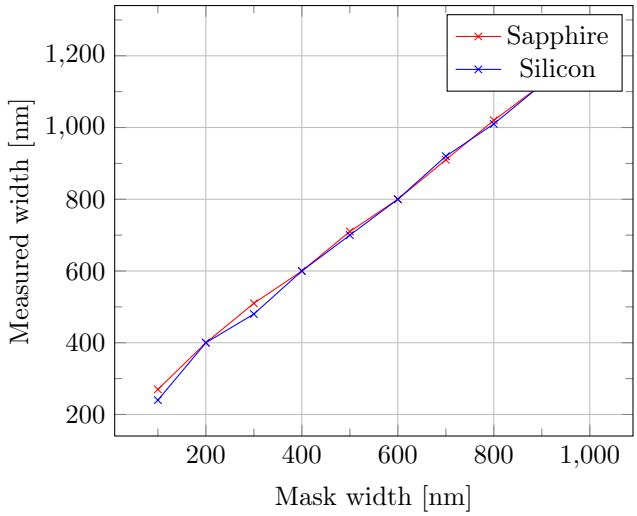


Figure 4.37: Exposed and measured widths of trenches exposed with a dose of $180\,\mu C/cm^2$.

Post-Etch Residue Examination and Removal

On many of the processed samples, the surface has been visibly covered with dirt, dust and an indeterminate particulate matter. This section examines this further and attempts to find a cleaning procedure that will overcome these problems.

Method

The first sample examined here was the one etched using recipe 32 during etch recipe comparison. It is selected here because it clearly shows the aforementioned particles on top of the unetched silicon, as well as a coarseness in the SiO_2 film. After etching, the sample was cleaned first in acetone and then in oxygen plasma for two minutes in order to remove the residual resist. The sample was inspected in the SEM.

Another sample was inspected using EDS. Unfortunately the etch recipe used on the sample has been lost, however the sample was very similar to the one presented in Figure 4.38. The EDS analysis looked for carbon, as it is the main constituent of the resist.

The third sample is a waveguide etched with recipe 1. After etching, the sample was scribed into its final waveguide dimensions and then plasma cleaned. After cleaning, it was inspected by SEM. As an additional cleaning step after the inspection, the sample was sonicated in acetone at room temperature for 10 minutes before additional inspection was performed.

Results

The two first samples are shown in Figures 4.38 and 4.39. The first obviously contains particulate matter on the non-etched areas, while the underlying SiO_2 has a grainy, but much finer structure. The same coarseness is not present on the sidewalls.

Figure 4.39 shows the EDS scan, highlighting Si and C. It is striking, but not surprising that no carbon is present in the etched area marking out the letter 'k'. After all, all resist should have been removed from this area during the development step, and the success of the subsequent etch step relies on the resist being removed. The non-etched area, however, has been covered with resist all the way through the process up until the acetone rinse and oxygen plasma clean.

More interesting is the large amount of carbon present. Apparently oxygen plasma cleaning is not enough to remove PMMA on a microscopic level, and if this turns out to be a problem another cleaning procedure should be developed.

A superior cleaning procedure has been found in the form of sonication. Figure 4.41 shows a waveguide before sonication, Figure 4.42 shows the same waveguide after. All traces of dust have been removed. The holes in the Si film presumably were not repaired by ultrasound, rather this is another part of the waveguide. The apparent increase in definition showing

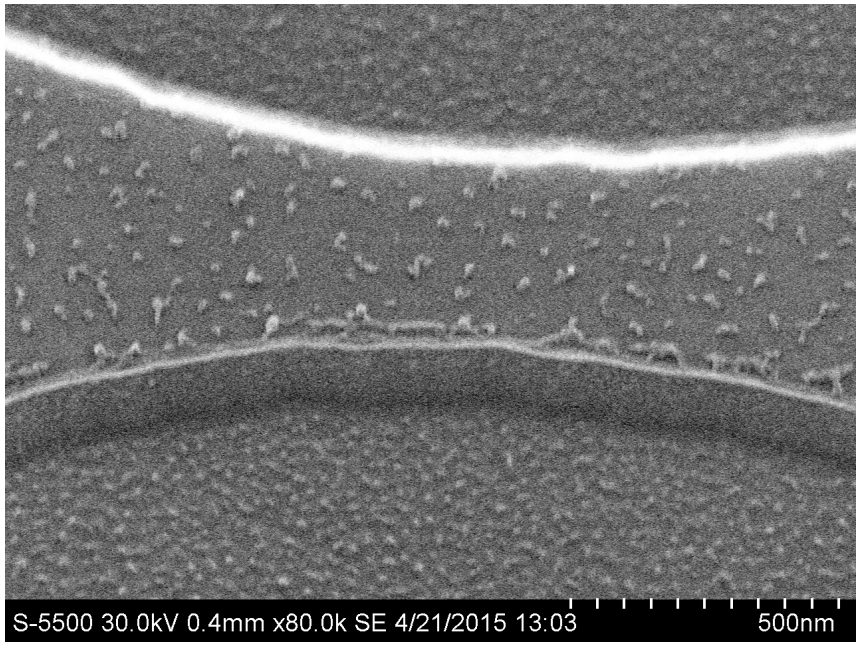


Figure 4.38: Sample etched with recipe 32. Large particles clearly visible on Si layer, smaller grains on SiO_2.

the roughness of the amorphous silicon may be due to higher resolution, which can be inconsistent unless particular care is given.

By using acetone as the sonication liquid, the PMMA should be stripped away easily. If this turns out to be insufficient at some point, PMMA residues may be removed using MicroChem's products Remover PG[55] or ACRYL STRIP[1]. However these substances are more harmful than any wet chemicals used in the current process, being based on N-methyl-2-pyrrolidone and concentrated acetic acid respectively.

Figure 4.40 confirms the effect of sonication. The EDS image clearly identifies the substrate as silicon, and only incidentally reports carbon. The amount of carbon reported in the image is very low, on the order of the typical noise levels of the EDS detector. In tests not shown here, using EDS to look for plutonium or any other rare material identified it in the same amounts as, in this case, carbon.

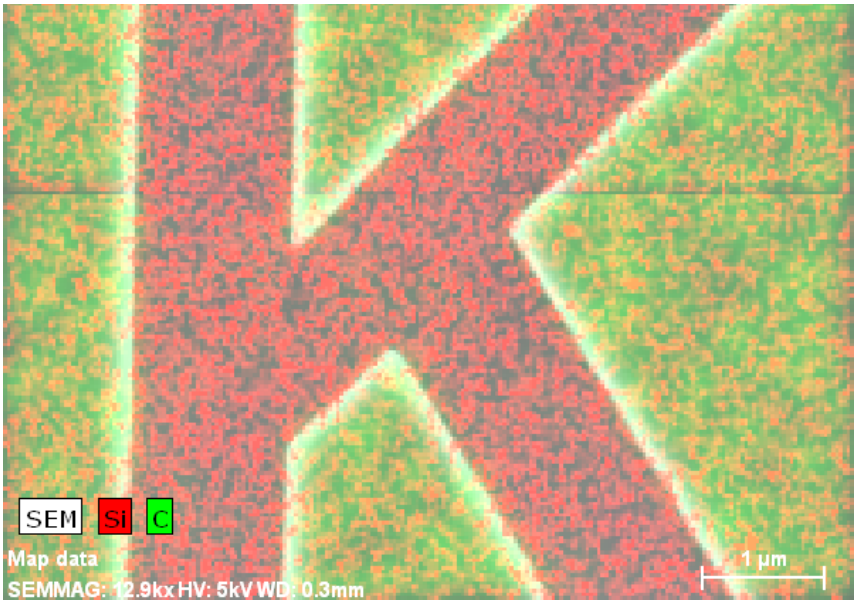


Figure 4.39: EDS image showing the letter k etched into an SOI sample. Carbon-containing residues are present in the non-etched areas, implying that resist remains.

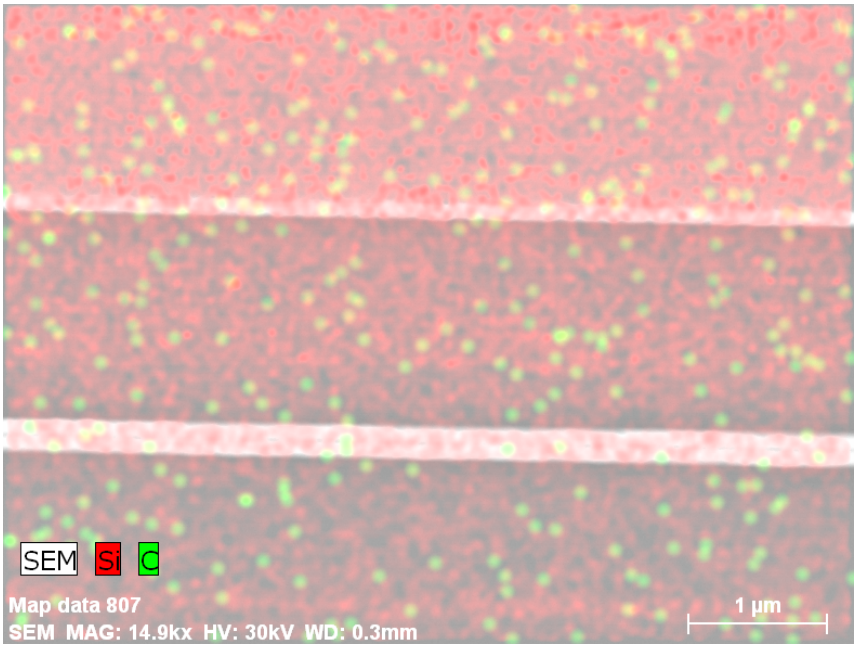


Figure 4.40: Post-sonication EDS image, showing carbon levels corresponding to typical EDS noise, independent on position in etched pattern.

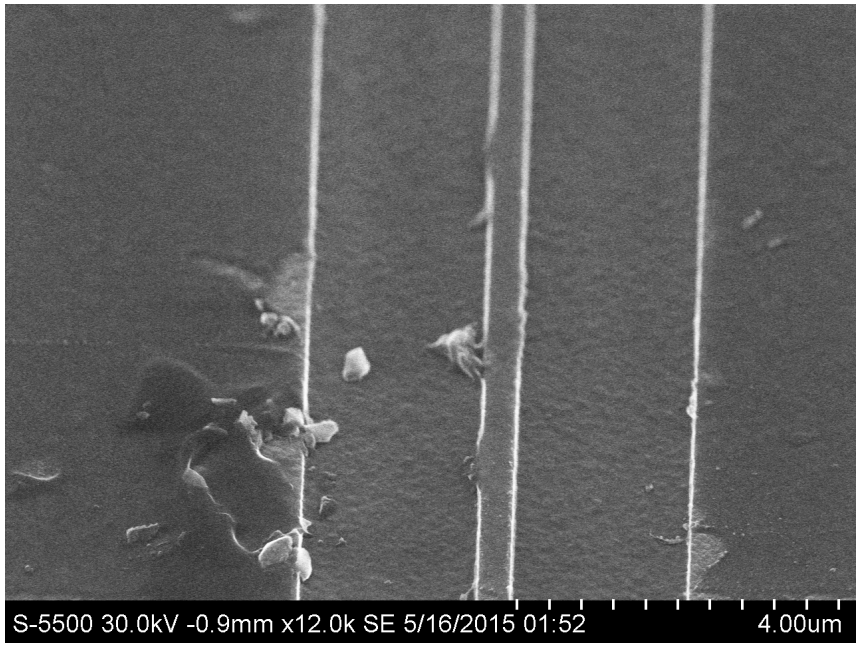


Figure 4.41: Tilted image of the waveguide, primarily showing large grains of dust from the scribing process.

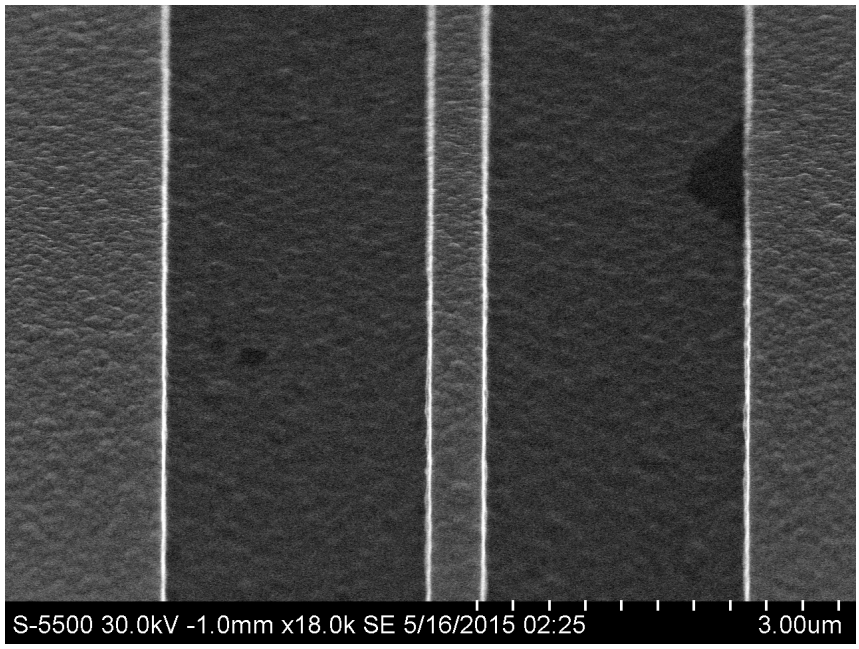


Figure 4.42: A very clean waveguide without any dust.

4.2 Fabrication and Testing of Device

Fabricating Waveguides

Method

A sample was fabricated containing a number of waveguides. It contains five simple straight waveguides, three waveguides that couple into another waveguide using a ring resonator after a few hundred µm and three containing a large S-curve, with a radius of curvature of 100 µm. The curved waveguides were designed using Autodesk AutoCAD's[1] offset feature, while the other waveguides were designed in CleWin.

The sample was taken from Wafer 3. It was coated with 250 nm PMMA and exposed with 260 µC/cm^2. Afterward, it was etched with Recipe 1 on a silicon carrier. After etching, the sample was scribed to a length of 1.2 mm and sonicated in acetone for 10 minutes. A piece of the silicon that was scribed off of the sample was also sonicated, and was examined in SEM in cross-section mode.

Results

Images of the fabricated structures are shown in Figures 4.43 and 4.44. The results are somewhat disappointing, particularly in that the silicon layer is thinner than it is supposed to. Also, the sidewalls have a very isotropic profile. While this is less than ideal, the waveguides appear to be of high quality and an attempt will be made to couple light into them.

[1] www.autodesk.com

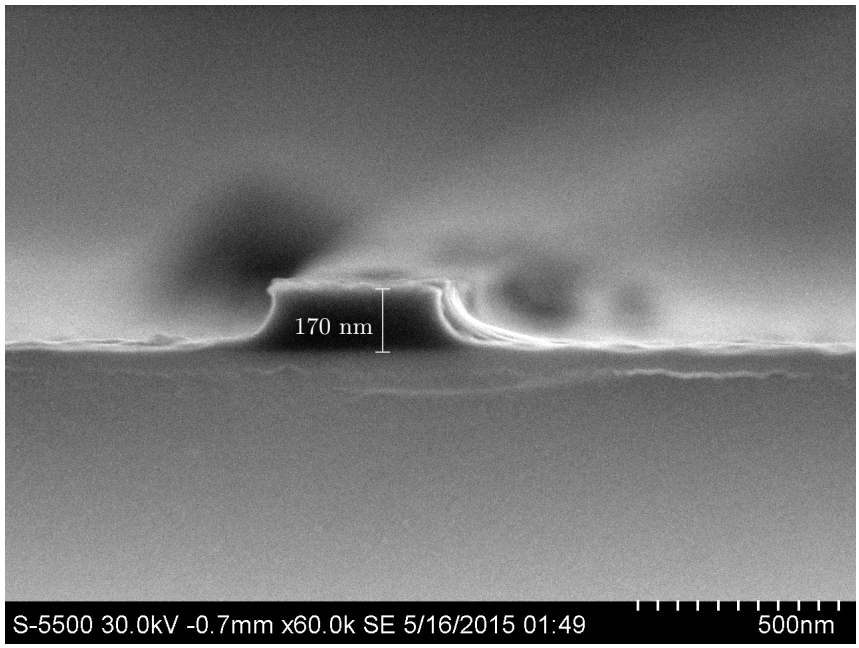


Figure 4.43: Cross-section image of a waveguide facet. The etch is more isotropic than expected and the Si is 30 nm thinner than previously measured.

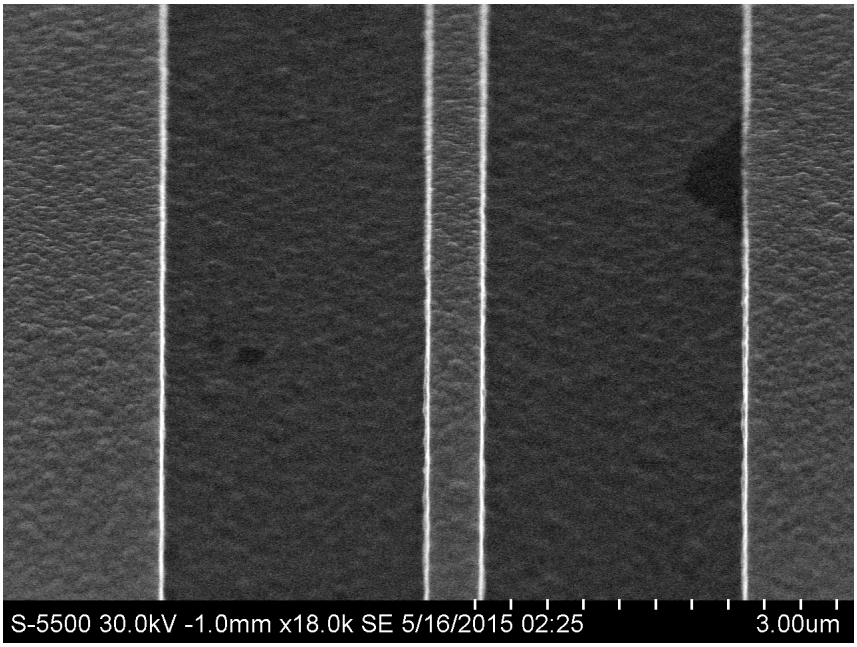


Figure 4.44: View of a waveguide from above.

Fabricating Tapered Waveguides

Following the failure to couple light into the waveguides from Section 4.2, more samples had to be prepared. In order to make a better facet for coupling light into, a larger area should be produced. This was achieved by using a thicker Si layer, and by coupling into a wider waveguide using a taper. The taper should also make the end of the waveguide more robust, potentially keeping it from flaking off during scribing and breaking.

Method

The mask from Section 4.2 was altered by adding a taper to the butt coupling end. This mask is shown in Figure 4.45. The columns of squares marks the beginning and end of the tapered region, and should be visible in the microscope of the scriber-breaker. To the left, the waveguides are 7.5 µm wide until the taper region begins, after which they narrow down to 550 nm over the course of 100 µm. These values were decided upon based on simulations by Jens Høvik.

Two samples were fabricated using the mask described above. Sample 1 was taken from Wafer 1, already coated with 150 nm of PMMA. It was exposed at a dose of 180 µC/cm^2 Sample 2 came from from Wafer 3 and was coated with 270 nm of PMMA. It was exposed at 260 µC/cm^2.

After exposure, both were etched using Recipe 14 on a Si carrier wafer. They were etched for different periods of time, due to the different thicknesses.

Results

Images of the fabricated structures are shown in Figures 4.46 to 4.48. Like with the straight waveguides, the silicon is too thin, but the etch profiles look surprisingly good. The roughness of the top surface as seen in Figure 4.46 is worrisome, but the sidewalls are generally very anisotropic, which is good.

Curiously, Sample 1 appears to have an undercut profile. This is the first appearance of this profile in this work.

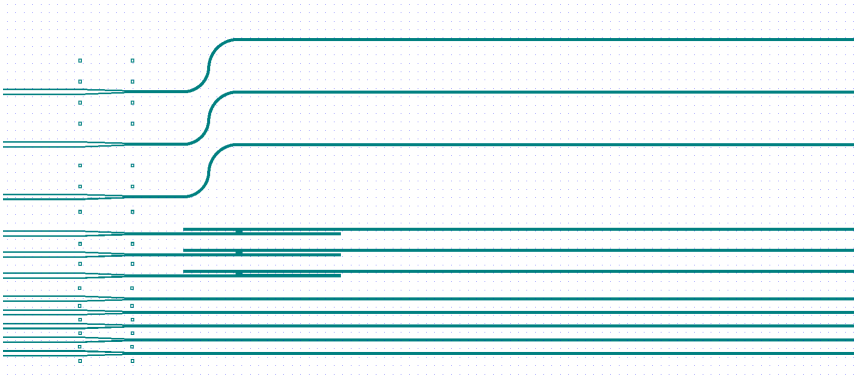


Figure 4.45: Mask featuring tapered waveguides.

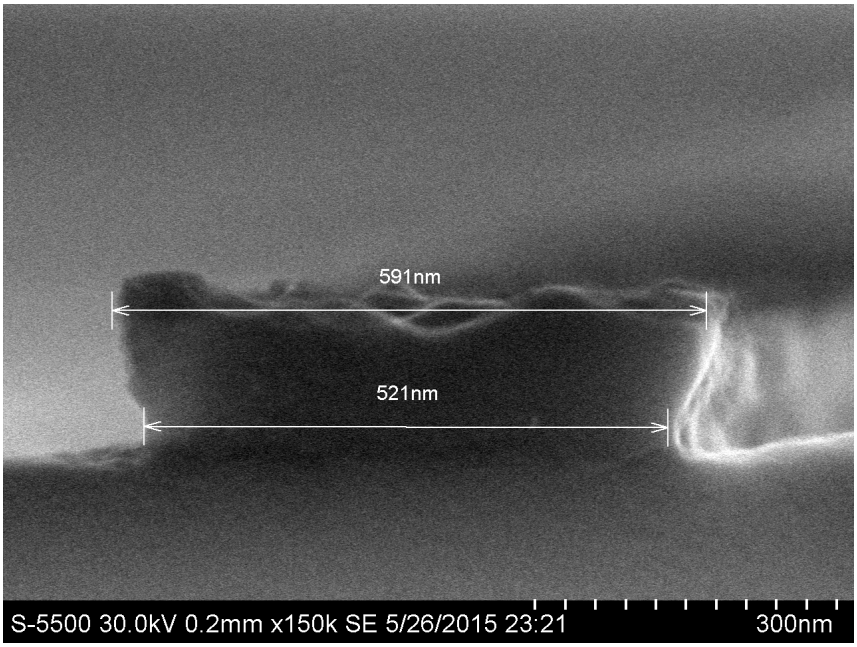


Figure 4.46: Cross-section image of a Sample 1 facet. The waveguide appears thinner than planned, has a very rough surface and has some undercut, not seen before in this work.

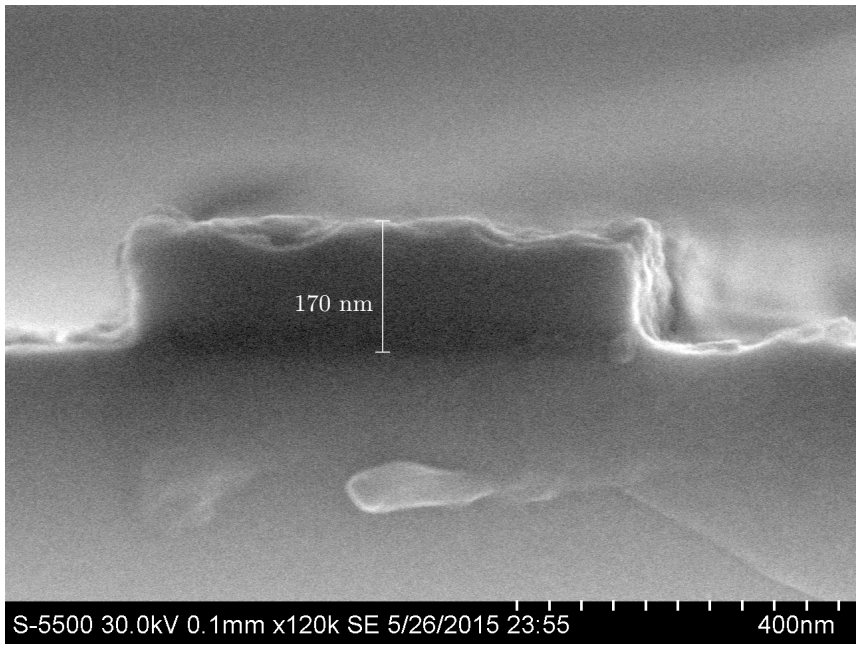


Figure 4.47: Cross-section image of a Sample 2 facet. The etch is more isotropic than expected and the Si is 30 nm thinner than previously measured.

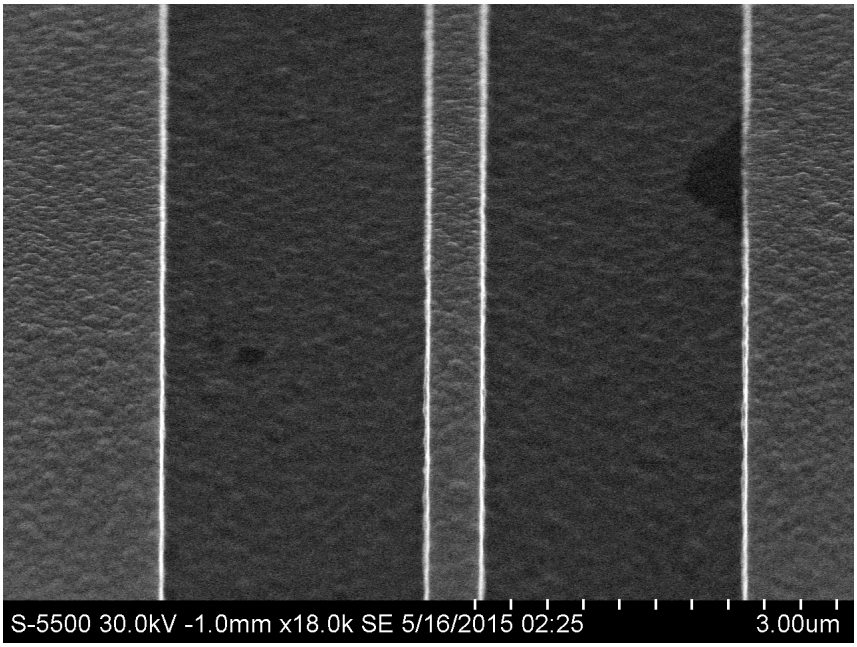


Figure 4.48: View of a waveguide from above.

Device Testing

Method

The waveguides from Section 4.2 were brought into the optics lab. Placed on carbon tape, the sample was mounted on the sample holder and inserted into the setup. At this point in time, the out-coupling fiber was not mounted on the stage, so only in-coupling was performed and characterization was done using the IR camera.

Looking through the microscope, the fiber was aligned with the waveguides. First, the fiber was brought close to the samples using the coarse adjustment screw. Then, it was brought within 50 µm using the finer adjustment screws, and aligned horizontally with the waveguide to be tested. Attempts were made to couple light into all the waveguides.

Adjusting the fiber tip in the vertical direction, an attempt was made to coarsely line it up with the top of the sample, staring closely at it from the side. The laser was enabled and set to between 40 mA and 100 mA, where the adjustment depended on whether the fiber tip was visible to the camera or not, as image chip burn-in and damage was an issue. While looking at the monitor for changes in the light pattern on the surface, minute changes were made to the positioning of the fiber tip.

In a later trial, the waveguides with tapered in-coupling regions from Section 4.2 were tested. In this trial, the out-coupling fiber had been mounted, so it was possible to make measurements based on the photodetector as well as visual data from the camera. In addition, the in and out fibers were butt coupled together directly, and the signal generator was used to modulate the laser.

Results

Microscopy did not show any coupling of light into any of the waveguides. Specks of light were clearly visible on the samples, but their locations did not match up with the known waveguides. Moving the tip vertically had a clear effect on the pattern, but unfortunately it was not systematic. Interestingly, moving the tip sufficiently far down that it was only pointing at the silicon substrate did not cause extinction of the pattern.

Although the waveguides are only 200 nm thick, it was expected that they would light up on the monitor when the beam struck them, as a sufficiently large portion of the light should couple into them. This was not observed.

However, when observing the out-coupling end of the waveguides, three streaks of light were often visible. These are shown in Figure 4.49. At first glance, these were assumed to be light escaping from the waveguides. However, moving the fiber along the sample caused the streaks to move as well, even when they weren't intersecting the waveguides. Focusing up and down revealed that the streaks were not at the same height as the waveguides, confirming that they were only light transmitted through the substrate.

Positioning the out-coupling fiber next to the far end of a waveguide did return a signal on the oscilloscope, showing the photodetector to be functioning. It was possible to cause a large spike in the strength of the signal by fine tuning the position of both fibers. The signal strength was particularly sensitive to the distance from the out coupling fiber to the waveguide. However, when moving the entire sample while keeping the fibers stationary, no change in signal strength was observed, meaning that the signal was not linked to the presence of the waveguides. Curiously, these results were gained when using the curved waveguides, with the fiber tips offset by 100 µm.

Coupling in-fiber directly to out-fiber revealed that the signal generator is functioning as well. The output of the laser when modulated by a square wave is shown in Figure 4.50. At a current of 40 mA a signal strength of 350 mV was measured at the oscilloscope. The signal amplifier was not used, as switching it on would cut the signal to 0. No effort was made to debug the amplifier, as the signal was readable without it.

Analyzing the data showed the 10%-90% rise time of the laser to be 330 µs, and the fall time to be 1.1 ms. No ringing was observed. A closer look at the rise and fall of the signal is shown in Figures 4.51 and 4.52. It is not known if the rise and fall times are due to the laser or the photodetector. This could be tested with a light source or photodetector known to be faster than the time constants measured here, but this falls outside the scope of this thesis.

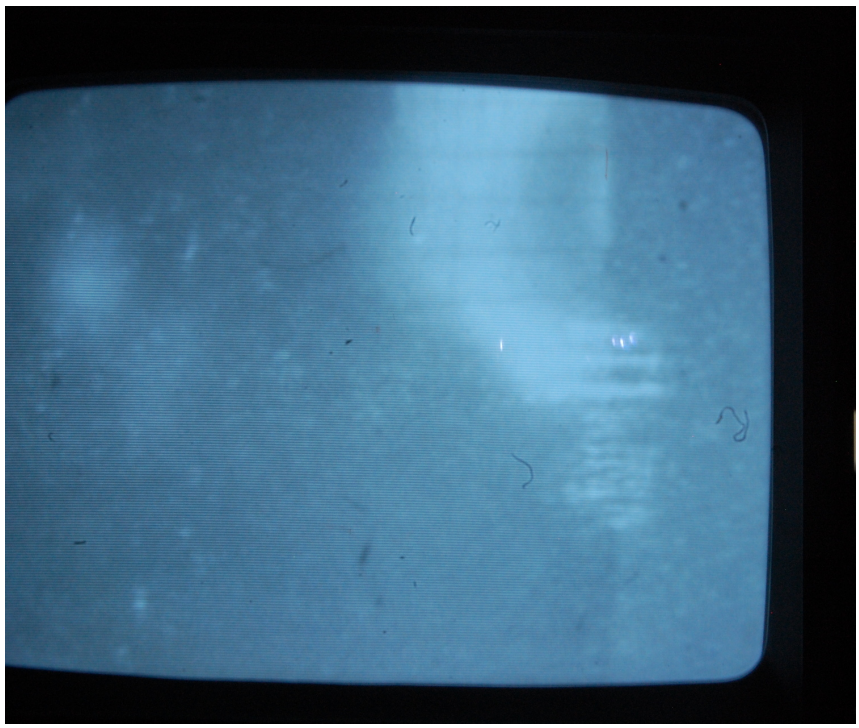


Figure 4.49: Streaks lighting up where light exits the sample. Applying a powerful flashlight to the sample causes some waveguides to be visible as well, in the top right part of the image. Waveguides must not be confused with artifacts from photographing the monitor's CRT screen.

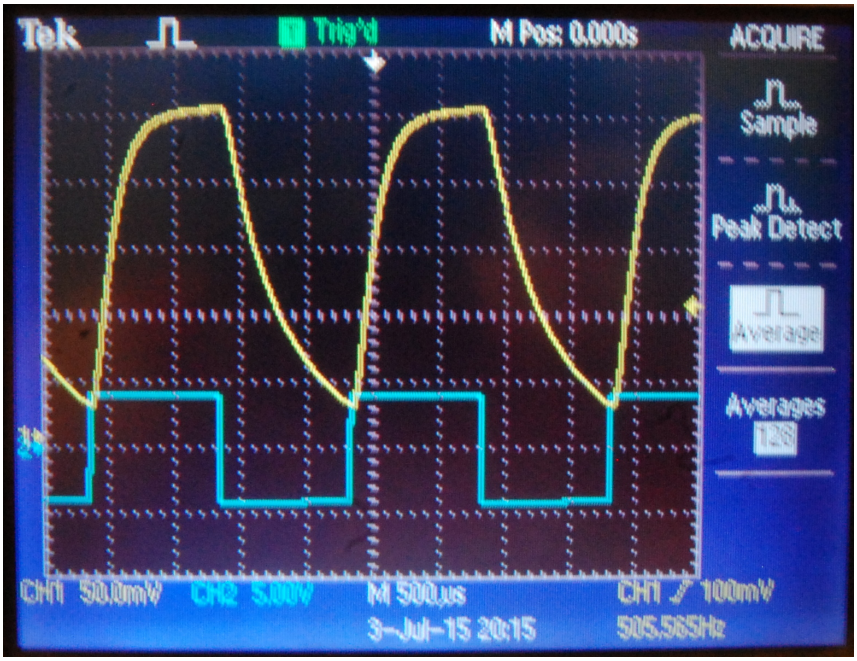


Figure 4.50: Oscilloscope showing the output of the laser when switched relatively quickly compared to its rise and fall times. At lower switching frequencies, the signal would stabilize very close to the levels shown here.

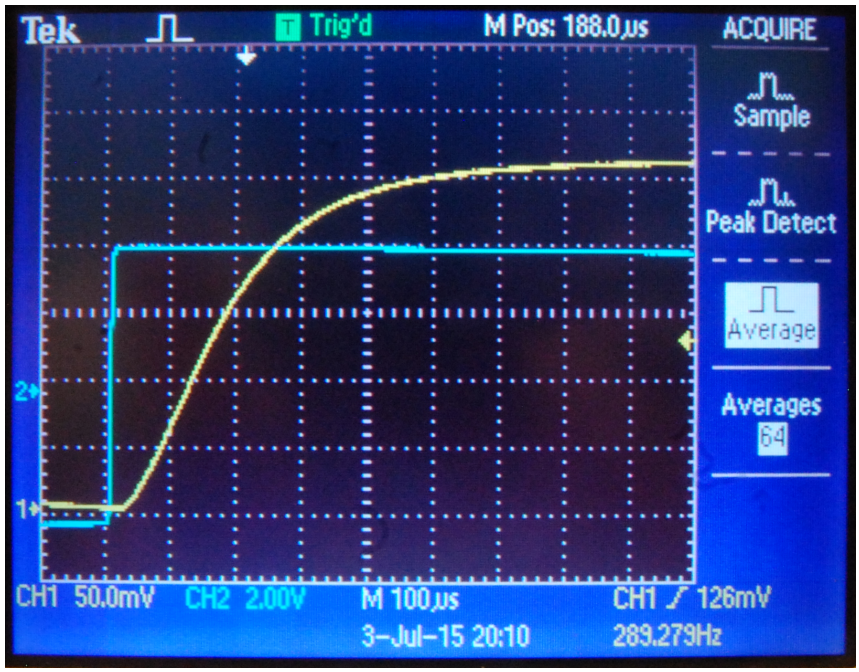


Figure 4.51: Laser transient response when switched on.

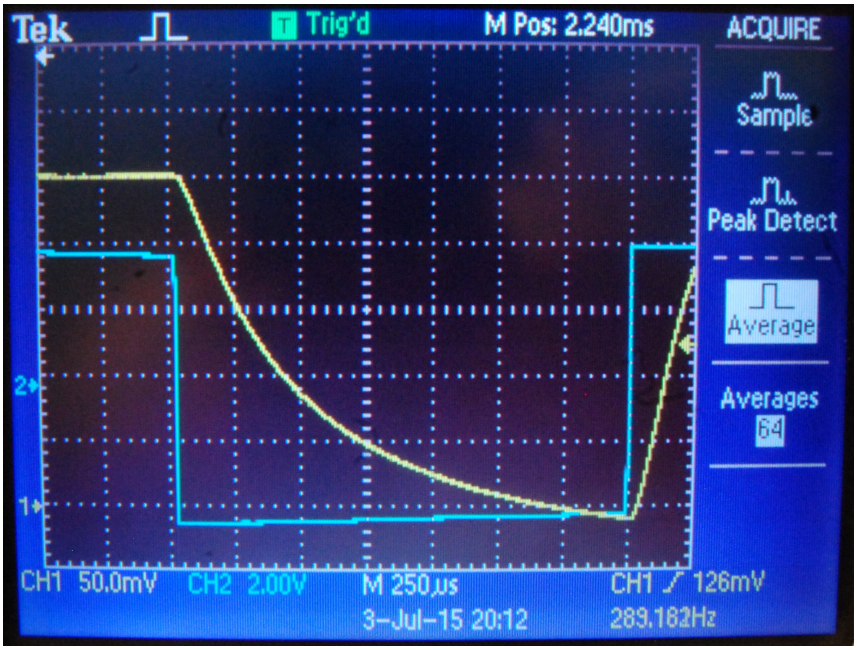


Figure 4.52: Laser transient response when switched off. Fall takes far longer than rise.

Chapter 5

Discussion

5.1 Fabrication

Substrate

The substrates used for making devices in this work were made using PECVD, as described in Sections 3.4 and 4.1. This method was previously attempted by Lorvik[41], although he abandoned the prospect very early in the project, disheartened by the observed roughness of the substrate and the commonly higher absorption coefficient as compared to crystalline silicon. Høvik[27] also made attempts to grow high-quality SOI in his master's thesis, but concluded that the fabricated material was not of high enough quality for optical structures. Nevertheless, PECVD grown SOI was used in this work.

A number of factors motivated this choice. For one, commercial SOI is very costly, easily costing up to 1000 US Dollars for a 6 in wafer[3]. In contrast with this, fabricating a wafer at NTNU NanoLab can be done in a day, with arbitrary thickness of the SiO_2 and Si layers and at no cost to the student except for the initial silicon wafers. Furthermore, the SiO_2 layer in an SOI wafer serves as an etch stop when using an etch with fair selectivity[53]. This feature is lacking in the simple silicon substrates used by Lorvik, and although he achieved excellent structures the etch stop layer might have an effect.

Furthermore, the author believes the claims of high loss to be exaggerated. Cocorullo et al.[14] have achieved losses of 0.7 dB/cm, and while this is higher than the extremely low losses achieved in monocrystalline silicon[35] it is acceptable for small devices such as sensors. For telecommunications purposes, however, maintaining the power budget[57] is important enough that the difference may be worth the extra money, depending on final device size and performance.

This makes PECVD grown SOI a very attractive platform for this project, at least in the current stage, and it is definitely worth giving it a serious try. The assumption of poor optical properties should be tested experimentally by guiding light and measuring the losses, as guided modes

may have a different behavior from the perpendicularly incident light from a reflectometer.

However, the issue of roughness is very real and must be addressed. As shown in Figure 4.3, the roughness of the silicon is significant. Unfortunately, the roughness has not been quantified using AFM measurements. Due to the 15 mm sample size restriction of NanoLab's Veeco AFM, getting a representative view of the roughness over a larger area of the wafer would be time consuming and would require measurements from multiple samples.

The scale of the roughness can be assumed to have propagated from the thick oxide layer. Tanenbaum[65] measured a roughness of 4 nm in 150 nm thick layers, and while our layer has not been measured properly, it appears to be significantly rougher.

Reducing the roughness can be achieved in a number of ways: The most direct method is to use chemical-mechanical planarization[53]. This method uses a combination of a chemically active slurry containing particles and an abrasive disc. Achieving a very smooth surface usually takes several rounds, using progressively finer slurries and abrasive discs. This method is not available at NTNU NanoLab, but may be in use by the TEM Gemini Centre. However, it is time consuming and represents many more steps in the fabrication process, which should be avoided.

Another method is to use a different method for fabricating the SiO_2. While commercial SOI is expensive, some of the benefits may be achieved at a lower cost by growing thermal SiO_2 or buying it commercially. NTNU does not have the necessary tools to grow thick thermal oxides, as this requires high-temperature furnaces or atmospheric pressure CVD. It might be possible to have a batch of wafers processed at another laboratory such as MiNaLab, or they may be bought at low cost, typically less than $30 per 4 in wafer. Based on current results, the author's recommendation is to obtain thermally oxidated silicon and only use PECVD grown amorphous silicon as the top layer.

Waveguides

The bulk of this thesis has consisted of fabricating the waveguides and this effort has been successful, taking into account the issues with the wafer quality. In particular, characterizing different etch recipes has been important. The great number of recipes tested makes it possible to analyze how the different parameters affect the end result.

At first, Recipe 1 was examined by changing one variable at a time from the original recipe and observing the results. It turns out that the changes made were far too large to draw a lot of conclusions from, but they did shed light on some processes. For one thing, reducing the CHF_3 flow did not have a major effect on the sidewall roughness. This indicates that the roughness is not simply passivating polymers, but is rather defects introduced in the silicon itself.

Polymerization does, however, appear to have serious effects on the properties of the etch, regardless of the source of the polymerizing compound. This is seen clearly in the hardmask testing of Section 4.1. The etch recipe used, Recipe 18, does not provide any CHF_3, and the mask is only SiO_2. This is in stark contrast with every other trial, where the mask was PMMA. The sudden isotropy observed in the hardmask test indicates that the PMMA mask contributes to polymerization, although probably not to the same extent as the CHF_3 would, due to the lack of strong C-F bonds. Even so, fluorine might be contributed to the polymer through SF_6, but this is only speculation. Having concluded that PMMA has a passivating effect on the etch, it becomes even more obvious that the roughness is not only polymers, as the roughness in the hardmask sample is by far the worst witnessed. It is possible that a CHF_3-containing etch would perform better with a hard mask.

Effects of RF and ICP Power

An early assumption was that reducing the ICP power and increasing RF power would be beneficial, as there would be more kinetic energy delivered to the sample, and at the same time less chemically reactive species that could attack the sidewalls haphazardly due to the lower plasma density of RIE compared to ICP-RIE. Etch Recipe 8 partially confirmed this hypothesis, as it produced sidewalls better than Recipes 2 through 7. However, Recipe 7 did not give as positive results, which might indicate that reducing ICP is more important than increasing RF.

These results were used further in the testing, with very few tested recipes using ICP. In effect, most etching was done only in RIE mode. The greatest advantage this gave, apart from the smoother sidewalls, was the lower etch rate. The aggressive etch rate of Recipe 1 made it difficult to time in practice, especially with thin resist layers. With the recipes with etch rates around 5 nm/s, it is possible to set the etch time to the calculated etch time and add two seconds for the plasma to ignite, and two more as a buffer, and accept a 10 nm overetch as inconsequential. With an etch rate of 15 nm/s, the same overetch is achieved in less than a second by inattentiveness alone.

While decreasing ICP power was found to be a good strategy for reducing roughness, making the etch more physical by increasing RF did not have the same effect. Recipe 23, being a version of Recipe 18 with higher RF power, did not show smoother sidewalls. However, decreasing the power was found to help, but only up to a point. At too low RF power, igniting and sustaining the plasma may become an issue, and the etch quality didn't improve after decreasing the RF power below 20 W.

Roughness

Unfortunately, the roughness of the sidewalls has not been eliminated. Roughness reduction is recognized for its importance in manufacturing

optical components, but most studies approach it only by reducing roughness in the etch process[40], like this thesis. While reasonably smooth waveguides can be made through etching alone, some recent research has focused on post-treatments to the structures, as mentioned in Section 2.1.

The most successful of these approaches has used two types of wet processing of the waveguides to remove rough surfaces[35]. In the most successful type, thermal oxide was grown on the sample and then, if desirable, etched away in HF. Thermal oxidation was performed at 1000 °C for 43 min. According to Brigham-Young University's thermal oxide growth time calculator[1] based on the Deal-Grove model[46, 18] this would create an oxide layer about 300 nm thick. Using the same calculator but allowing only for the dry, 1000 °C 10 min RTP process available at NanoLab, a layer of only 10 nm would be achievable. This might produce a very slight reduction in roughness, but as mentioned in Section 3.4 the heating might make the amorphous silicon itself lossy, up to the limit where the annealing causes recrystallization of the silicon. Repeated dipping between hydrogen peroxide to iteratively grow a thin native oxide and HF to remove it probably would not work either due to the thin oxide produced, and would be both time-consuming and dangerous.

The same authors also had some success with using an alkaline etch to strip away roughness, leaving only the stable {110} planes[35]. This, however, required the use of a hard mask, as resist would be peeled away immediately. Also, since there are no crystallographic planes in amorphous silicon, the stable planes would never arise and the etch might be uncontrollable. It is theoretically possible that protruding features would be etched away faster than receding ones based on surface area alone, and this effect might cause some reduction of roughness. However, this is only speculation, and the effects could be very slight. Furthermore, the method may be useful only for straight waveguides aligned with the (100) direction in the silicon. For a curved feature or a ring resonator, entirely different planes would be exposed, and the resulting features would be distorted as there is no self-limiting effect.

Etch Profiles

Looking at the results from testing Recipes 1, 14 and 18, it is clear that all three etches have their strengths and weaknesses. Recipe 1, especially when combined with a silicon carrier, offers excellent sidewall profiles with little of the porosity seen in the samples etched with a sapphire carrier. However, there is still some unevenness in the features, which manifests as notches in the waveguide when seen from above, as in Figure 4.13. The same issues are visible in Vigen's samples[69, p. 78]. The roughness issue appears to be present when using Recipe 14 as well, but possibly to a lesser degree.

Unfortunately, Recipe 14 turned out to be isotropic when using a sapphire carrier, but became far better with silicon. However, a certain flange

[1] `http://www.cleanroom.byu.edu/OxideTimeCalc.phtml`

appears on the waveguides in the latter case. Figure 4.37 reveals that the waveguides etched on sapphire and silicon are almost equal in width, with only a slight offset in favor of the silicon etched waveguides. Inspection of the raw data reveals that the difference is only on the order of 20-30 nm. Figure 4.37 is even more striking, showing no difference at all. This should come as a surprise, considering the difference in profile.

Recall from Section 3.3 that isotropy is usually a result of the etchant attacking the sidewalls and eating them away. If this were the case, the sapphire etched trenches would become wider and the waveguides narrower. As it turns out, the etch is slower near the corners, which is the opposite of the problem described above. While this could be mistaken for aspect ratio dependent etching[33], this usually takes place only at far higher aspect ratios, and does not necessarily compromise the sidewall profile.

Another explanation may be found by comparing the etch to other techniques. The problem of outward sloping profiles, also known as overcut, is characteristic of ion beam etching, particularly when etching perpendicularly to the substrate[10]. The reason for this is that atoms that are sputtered away without reacting with chemical species may redeposit on the sidewalls, and the fix in ion beam etching is to tilt the sample by, typically, 20°. In this work, the etch recipes have been aimed at being as physical as possible, with little chemical etching action. This can be compared to a poorly controlled reactive ion beam etch[10], and redeposition may occur.

However, a highly physical etch would be expected to have low selectivity between silicon and resist[53], as sputtering selectivity is only a question of bond strength. In Recipe 1, with high ICP power and a high plasma density, the selectivity is rather low even though the high plasma density is expected to create a very chemical etch. In Recipe 14 however, the selectivity is very high. It may be speculated that Recipe 14 with its relatively high pressure and low power has a significant chemical component to it, or simply has too low power to get a high sputter yield in PMMA. Unfortunately, no studies have been found on the voltage dependence of selectivity in ion beam etching, so these statements cannot be substantiated.

5.2 Coupling

The optical test setup has been confirmed to be functional. The fibers can be moved with high accuracy in close proximity to the sample without unneccesary risk of colliding the tip due to the functioning microscope setup. Also, is has been shown that the laser output is completely controllable, both manually and with a signal generator. The coupling of fiber to fiber also shows the photodetector to be in working order, meaning that the test setup should be working just fine for further use in the project, and easy to modify if found necessary.

The results from the attempts to couple light into the waveguides were negative. No light was observed by camera to enter the waveguides. The photodetector gave a response, but unfortunately this proved to be a false positive when the signal persisted after the sample was shifted sideways. However, a persistent pattern of bright spots appeared at the out-coupling end of the sample, which moved in accordance with the fiber and which was observed by focusing to originate below the sample surface.

The most likely reason for the pattern is some kind of interference pattern in light traveling through the silicon substrate. As the substrate is more than 1000 times thicker than the waveguides and approximately infinitely wide, it has a far larger area that can accept light, and will receive a much higher optical power than the actual devices. As the silcon substrate-oxide interface is perfectly flat, total internal reflection should contain the light within the substrate and keep it from disturbing the microscope images, but a powerful light beam striking the out-coupling fiber is an issue. A way to fix this is to introduce a larger S-bend in the waveguide, displacing the out-coupling fiber more than the undesirable beam widens.

Another fix is to make the waveguides L-shaped and alter the optical setup to accomodate this. A sketch of a proposed mask design is shown in Figure 5.1. The dotted lines are the proposed scribe lines. In this scheme a number of concentric waveguides are made, preferably with the same radius of curvature but different side lengths. By scribing in the suggested way, four samples are made with different properties: If one sample winds up with only waveguides too long for practical use, the opposite corner will have correspondingly shorter waveguides.

A setup for making measurements on these waveguides is shown in Figure 5.2. Here a bracket has been added to the movable stage for the out-coupling fiber, and the fiber is mounted on its end. By extending the movable stages, complete mobility of the fibers is preserved. This extension should be easy for the department's mechanical workshop to make.

While this may fix the problem of false positives, coupling into the waveguides may still be a problem. One way to fix this is to guarantee that the facets are of higher quality than they have been thus far. In this work, the waveguide facets have been made by breaking the samples, with greatly varying results. In many cases, the waveguides have been

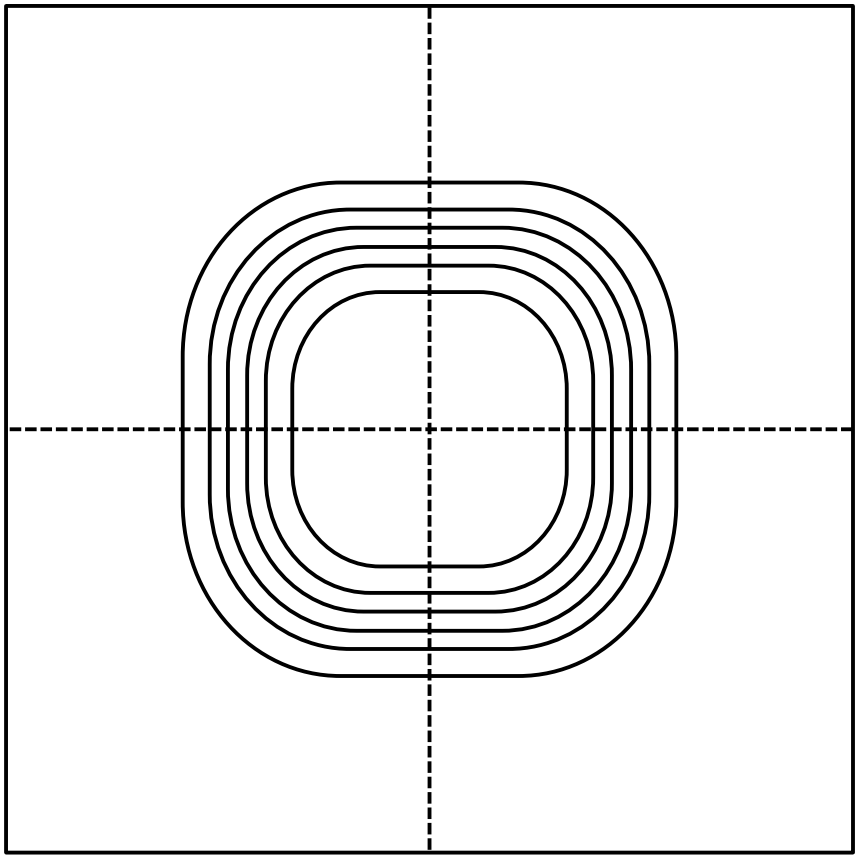


Figure 5.1: Proposed mask design for L-shaped waveguides. The concentric design guarantees that a large number of waveguides with different length are made at once, making measurements of losses easier. Furthermore, four samples will be produced from one single exposure.

terminated several micrometers from the sample edge, been broken at an angle and so forth. Using a tapered design has mitigated this, as the broader waveguides are more robust, in addition to having a larger area. However, the facets may still be rough, which is a source of problems.

This could be fixed by polishing the waveguide facets. A number of procedures are available for this: The necessary equipment exists at the TEM Gemini group at the Department of Physics. However, getting training and using it might be costly, depending on internal procedures for cross-faculty resource use. There may also be a polishing machine at the Department of Electronics and Telecommunications, which should be investigated further. Another possibility is to use FIB milling. This has been done before[42] with success.

Another approach is to switch to grating coupling[57]. In this scheme, a

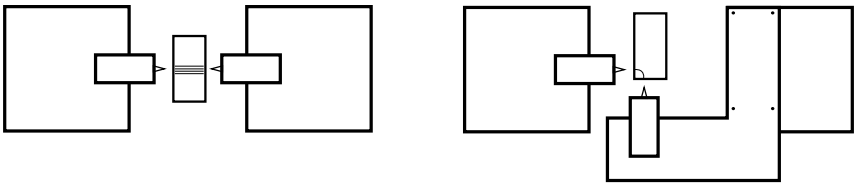


Figure 5.2: Proposed setup for measuring L-shaped waveguides. To the left is the current setup, to the right is the proposed design. The movable stage for the out-coupling fiber is modified with a bracket for mounting the fiber perpendicular to its current position.

separate lithography and etch process creates a grating on the waveguides at the points of in- and out-coupling, and the fibers are pointed at these at a specific angle. While this requires more fabrication steps, so does milling. In addition to simplifying the alignment process a great deal, it might lead to higher coupling efficiency[64]. However, grating coupling will require changes to the setup, and changes to the microscope might be necessary in order to avoid collisions with the fiber holders.

Furthermore, the camera does not appear to be of very high quality. It is a distinct possibility that light has coupled into the waveguide and been lost in the process, but that the camera has not been sensitive enough to show it.

The spot size of the tapered fiber output at focus is stated by the documentation to be between 1.7 µm and 6 µm[47]. In the best case, with a diameter of 1.7 µm, the fraction of the area overlapping a 200 nm by 550 nm waveguide is 4.8%, corresponding to an in-coupled power of 4.8 mW at maximum power if there is no reflection or loss at the surface. In the worst case, the corresponding power at perfect focus is 0.39 mW.

Switching to a tapered waveguide helps by increasing the width of the waveguide, up to the size where it is the size of the spot. In this case, the power with the smallest spot size is 15 mW, and 2.1 mW with the largest.

It is clear that the potential gains from using a tapered waveguide are large. Especially in the best case, where the spot is almost the size of its wavelength and perfect focus has been found, a significant amount of light can be coupled into the waveguide. However, it must be assumed that achieving such perfect coupling is difficult, and it is more realistic that the coupled amount of light is far lower.

Another issue that needs to be addressed is the choice of laser. As was shown in Chapter A, the laser is only barely tunable. If resonators are to be used, it is critical that the laser is tunable to their resonance frequency. As it may be quite sensitive to fabrication errors and preferably to stimulation in a sensor setup, the laser must be tunable over a wide enough range to find the resonance. At the moment this is not possible and thus a new laser should be acquired before testing of resonator devices begins.

Chapter 6

Conclusion

The goal of this work has been to optimize processes for fabricating silicon photonic components.

6.1 Electron Beam Lithography

Electron beam lithography was used for patterning the samples, and the effect of changing parameters was tested. Based on simulations and previous personal experiences, an acceleration voltage of 30 kV was selected. It was found that while underexposure must be avoided, overexposure does not appear to cause problems. Serious underexposure may result in a residual resist layer that causes severe and obvious damage. In addition, even slight underexposure will cause abnormalities in the outline of the feature. However, increasing the dose even far above the point where these issues disappear does not negatively affect device quality.

PMMA was used as the resist. For thicknesses of both 85 nm and 150 nm, a dose of 180 $\mu C/cm^2$ was found to produce good results. For the higher thickness of 270 nm, used for low-selectivity etching, 260 $\mu C/cm^2$ or higher was preferred. The size of physical features as a function of the exposed area has been documented.

6.2 Etching

A large number of etch recipes have been tested and compared, and three of them were selected for further study and optimization. These were Recipes number 1, 14 and 18 from Table 4.9. Recipe 1 and 14 were found to have the best performance in terms of etch profile and sidewall roughness.

Recipe 1 produced anisotropic etch profiles of the waveguide sidewalls. However, the sidewalls were rough and the etch rate was too high for controllable shallow etch. Recipes 14 and 18, on the other hand, had smoother sidewalls, a lower etch rate and in the case of Recipe 14 a much higher selectivity. However they also displayed a more isotropic etch profile. This

isotropy may be caused by redeposition of sputtered atoms, although this is usually only a problem in ion beam etching.

Interestingly, it was found that switching from a sapphire carrier wafer to a silicon wafer reduced the sidewall roughness and improved the etch profile of all recipes tested. This is because the sapphire is chemically inert. It thus allows a large volume of reactive chemicals to etch the sample without any sputtering effect. The silicon, on the other hand, reacts with them on impact and neutralizes them. However, using a silicon carrier reduces the selectivity of the etch.

6.3 Characterization

An optical test setup was built. It is capable of coupling light into and out of a sample and measuring the transmission. Alignment can be carefully monitored through a microscope or with a camera that works both in the infrared and visible spectrum. The incident light can be modulated with a signal generator for easier detection of coupling.

The setup has been verified to work by coupling light directly between the in- and out-coupling fibers. The laser's power and spectral characteristics have been tested as a function of current and temperature. It has been found to be practically not tunable and to have a higher spectral width than specified, however there is good control of the power output.

Attempts were made to couple 1550 nm light into the waveguides. However, it was not possible to measure any coupling either with a photodetector connected to an out-coupling fiber or with an infrared camera. The addition of a 7.5 µm wide taper for light to couple into did not help. Light passing through the substrate and stimulating the out-coupling fiber was found to be a serious issue.

6.4 Further Work

The surface roughness of the PECVD grown SOI wafers must be reduced, as they are expected to cause high losses. This can easily and affordably be accomplished by growing PECVD silicon on top of a thermally oxidated silicon wafer.

Due to the drastically improved results when using a silicon carrier wafer, it is recommended that the sapphire wafer is no longer used for etching.

Looking further into post-treatments to reduce sidewall roughness may be worthwhile. However any addition of steps to the fabrication process is undesirable, and must be weighed against the potential gains.

The reason for the failure to couple light into the waveguides has not been conclusively determined, but a number of possible solutions have been found. For making in-coupling easier, polishing the facets is an option. This can be accomplished either with FIB or mechanically. However, light transmitted through the substrate will still be an issue, which may

require additions to the experimental setup. Another possibility is to use grating coupling instead of butt coupling. Grating coupling is the solution favored by the author.

As a tunable laser is essential for characterizing resonators, it is recommended that the existing laser is replaced.

Appendix A

Laser Characterization

The Anritsu laser had to be characterized in order to find its characteristics, as the existing documentation was lacking. In particular, finding the peak frequency and whether it shifted with intensity or temperature was of great interest. A tunable laser would be ideal in order to excite the microring resonator, but there was great uncertainty about these capabilities.

Method

In order to determine the current-power and temperature-power characteristics of the laser, it was fired into a Melles Griot 13PEM001 powermeter. First, the thermistor resistivity was kept constant at 10 kΩ while the current was varied between 10 and 105 mA. Then, the current was kept constant at 50 mA while the thermistor resistivity was varied between 9 and 11 kΩ.

The spectral characteristics of the laser were determined using a Thermo Scientific Nicolet 8700 FT-IR spectrometer. The laser was aimed into the spectrometer in free air. Measurements were taken between wavenumbers of 6200/cm and 6700/cm at 0.125/cm intervals. This corresponds to the range of 1492.5 nm to 1612.9 nm with a resolution of 0.003 nm.

The experiments were performed with help from Tron Arne Nilsen.

Results

As the spectrometer works in terms of wavenumber, the raw data had to be processed to list the wavelength instead. During this processing, it turned out that MATLAB's[1] function csvwrite, which writes data to CSV files, converts numbers to a low precision datatype. This caused loss of data by removing significant decimal places, leading to nearly useless plots. The problem was solved by using the dlmwrite function, which has

[1] `http://www.mathworks.com/products/matlab/`

arbitrary precision. This information is included for the benefit of later master's students.

The by far most interesting result is the temperature dependence of the emission peak frequency. It is obvious from Figure A.1 that the laser can only be tuned approximately 1.8 nm. It can be reasonably concluded that the laser is not designed to be tunable, and is emitting at between 1549.0 nm and 1549.5 nm at the standard operating temperature of 25 °C. From Figure A.2, it is clear that the peak output wavelength is only weakly dependent on current.

A plot of the peak output wavelength as a function of temperature is shown in Figure A.3. The graph is remarkably linear, and it is noted that the wavelength increases with increasing temperature. This is to be expected for a DFB laser. When the temperature increases the Bragg gratings expand, and the resonant wavelength thus becomes longer[15]. The temperature dependence of the peak wavelength is given by

$$\lambda = 1546.662\text{nm} + 0.098\text{nm/K} \cdot T. \tag{A.1}$$

Figures A.4 and A.5 show the spectral linewidth in terms of FWHM as a function of temperature and current. As is also visible in Figure A.2, the spectrum is wider at 20 mA than at any higher current. This is presumably because the laser is operating close to threshold, as is clear from Figure A.6.

The temperature dependence is more confusing, as 25 °C has a lower FWHM than any other temperature. There appears to be a discrete step between 20.8 °C and 22.7 °C, except for the drop at 25 °C. In general, the laser's FWHM is around 12 nm at standard operating conditions. This works out to a spectral linewidth of 15 GHz, far more than the datasheet's promised maximum value of 40 MHz.

The step in the temperature dependence occurs around room temperature. This is the point at which the temperature controller switches from heating to cooling mode. As the aquisition took a few seconds, it is possible that the temperature of the cavity had not yet stabilized at the point of the measurement, and that the linewidth is a result of temperature drift.

From Equation (A.1), it is apparent that a wavelength drift of 0.15 nm would require a drift of 1.5 K. However, such a large shift in wavelength would probably introduce a larger shift in linewidth. No quantitative analysis will be given here. The temperature drift model of explanation also explains the smaller linewidth of the measurements at 25 °C. As the temperature was held constant and only the current was varied, any temperature drift would result from the increased current and not from a deliberate and large temperature change. This implies that the measurements should be repeated if a higher degree of accuracy is desired, and the laser should be allowed to stabilize for a minute or two between measurements.

Figure A.6 shows the relationship between the laser output power and the current. No lasing takes place at 10 mA, but starting at 20 mA the

relationship is linear. Linear regression shows the relationship to be as follows:

$$P = I \cdot 0.228\text{W/A} - 1.8\text{mW} \tag{A.2}$$

Similarly, Figure A.7 shows the relationship between the temperature, which is regulated by the thermistor resistivity, and the current. The dependence is shown to be relatively weak, varying by 0.5 mW within the laser's operating temperature range. The power increases with decreasing temperature, which is to be expected for diode lasers[50].

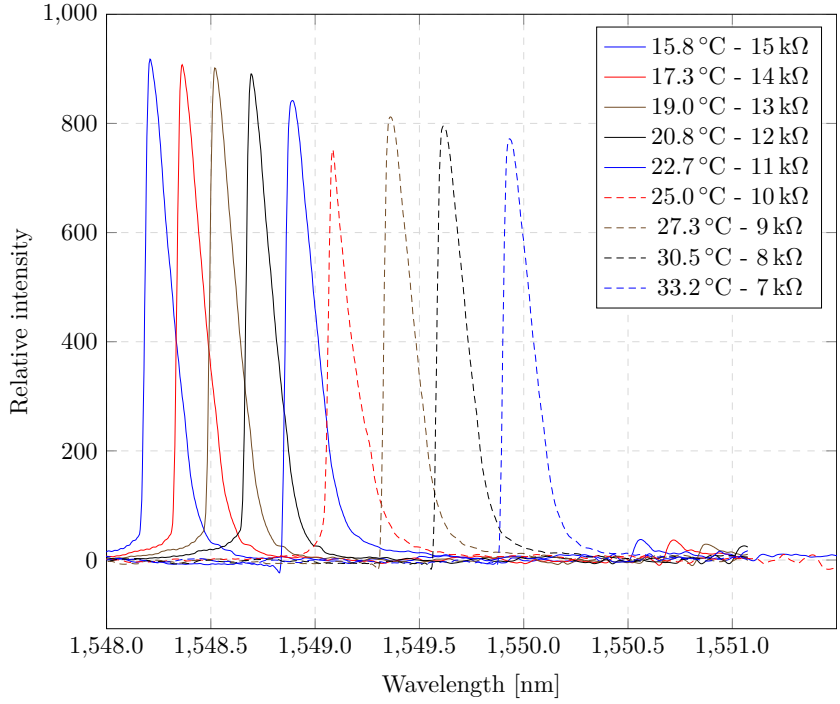


Figure A.1: Emission spectra of the laser at temperatures between 15.8 °C and 33.2 °C, controlled by adjusting the thermistor resistivity in steps of 1 kΩ.

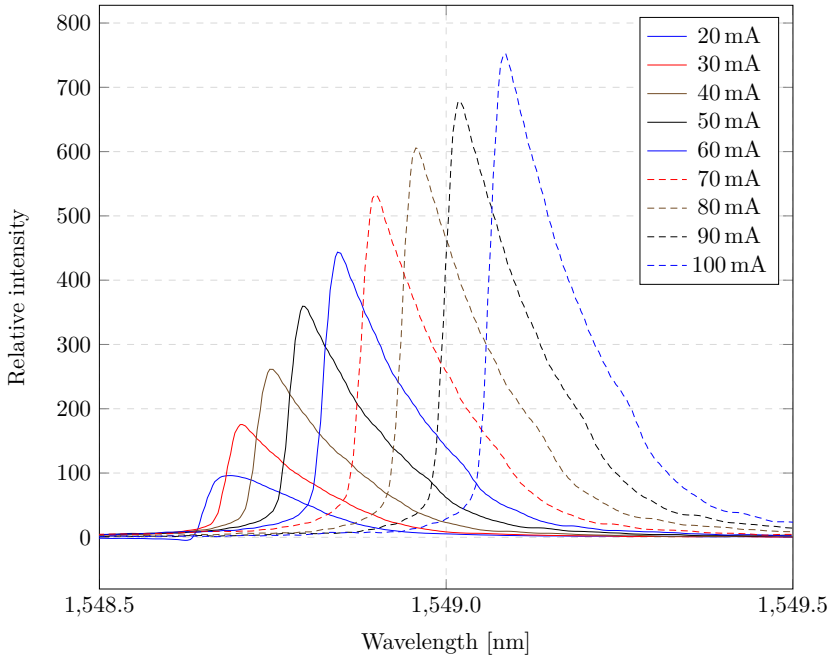


Figure A.2: Emission spectra of the laser at currents between 20 mA and 100 mA.

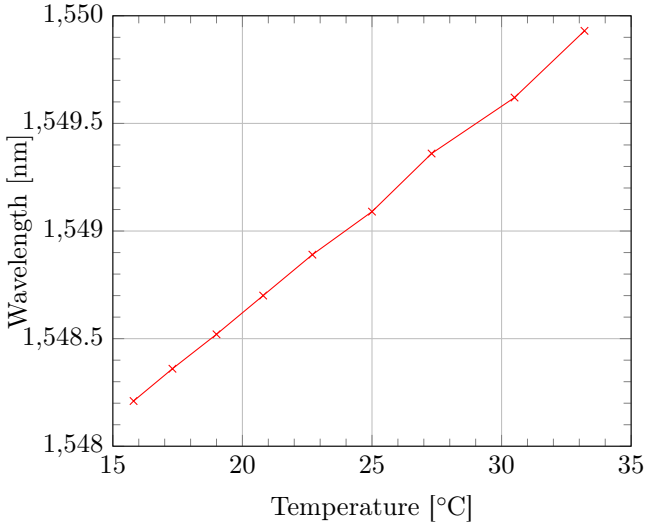


Figure A.3: Laser peak output wavelength as a function of temperature at a current of 100 mA.

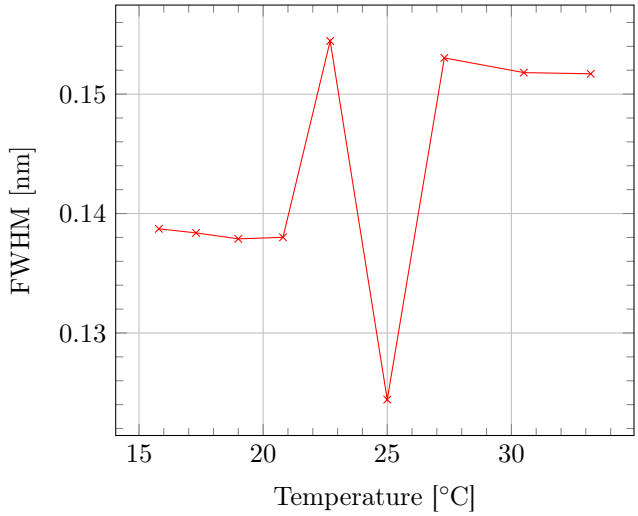


Figure A.4: Laser FWHM as a function of temperature at a current of 100 mA.

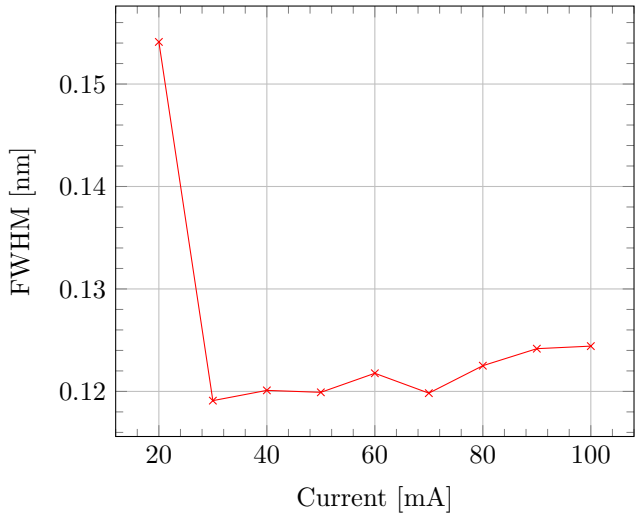


Figure A.5: Laser FWHM as a function of current at a thermistor resistivity of 10 kΩ.

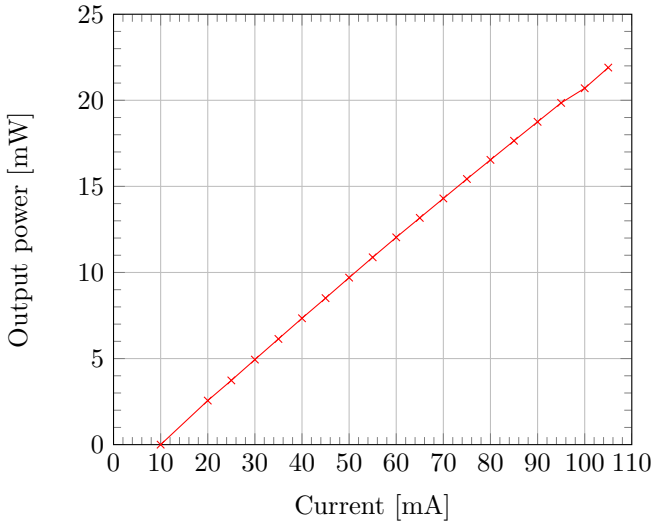


Figure A.6: Laser output power as a function of current at a thermistor resistivity of 10 kΩ.

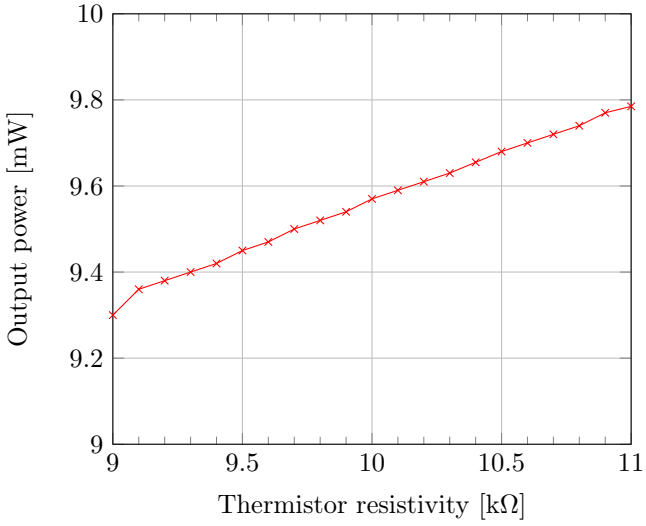


Figure A.7: Laser output power as a function of thermistor resistivity at a current of 50 mA.

Bibliography

[1] Acryl Strip. MicroChem Acryl Strip Material Safety Data Sheet, April 2001. URL http://www.princeton.edu/prism/mnfl/current-users/safety/msds/Acryl%20Strip.pdf.

[2] H. Baghsiahi, Kai Wang, W. Kandulski, R.C.A. Pitwon, and D.R. Selviah. Optical waveguide end facet roughness and optical coupling loss. *Lightwave Technology, Journal of*, 31(16):2659–2668, Aug 2013. ISSN 0733-8724. doi: 10.1109/JLT.2013.2271952.

[3] K. Baker. SOI Quote from UniversityWafer.com. Private Communication, 3 2015.

[4] Kai Müller Beckwith. EBL tricks : Improving EBL performance for writing nanostructure arrays over large areas, 2013. Internal document at NTNU NanoLab.

[5] W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. Kumar Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets. Silicon microring resonators. *Laser & Photonics Reviews*, 6(1):47–73, 2012. ISSN 1863-8899. doi: 10.1002/lpor.201100017. URL http://dx.doi.org/10.1002/lpor.201100017.

[6] T. Bolstad. Fabrication of a silicon photonic crystal biosensor. Master's thesis, NTNU, 2014.

[7] C. Bréchignac and P. Houdy. *Nanomaterials and Nanochemistry*. Springer Berlin Heidelberg, 2008. ISBN 9783540729938. URL https://books.google.no/books?id=yKOtuRjNRoYC.

[8] M Bruel. Silicon on insulator material technology. *Electronics letters*, 31(14):1201–1202, 1995.

[9] S. Burgess and M. Cargill. Using genre analysis and corpus linguistics to teach research article writing. In V. Matarese, editor, *Supporting Research Writing: Roles and Challenges in Multilingual Settings*, Chandos Information Professional Series, pages 55–71. EWoodhead Publishing, cambridge, 2012.

[10] M. A. Bösch, L. A. Coldren, and E. Good. Reactive ion beam etching of inp with cl2. *Applied Physics Letters*, 38(4):264–266, 1981.

doi: http://dx.doi.org/10.1063/1.92338. URL http://scitation.aip.org/content/aip/journal/apl/38/4/10.1063/1.92338.

[11] H John Caulfield and Shlomi Dolev. Why future supercomputing requires optics. *Nature Photonics*, 4(5):261–263, 2010.

[12] Chung-Yen Chao and L. Jay Guo. Design and optimization of microring resonators in biochemical sensing applications. *Lightwave Technology, Journal of*, 24(3):1395–1402, March 2006. ISSN 0733-8724. doi: 10.1109/JLT.2005.863333.

[13] Eun-Chel Cho, M.A. Green, J. Xia, and Richard Corkish. Evidence for crystalline silicon oxide growth on thin silicon. In *Optoelectronic and Microelectronic Materials and Devices, 2002 Conference on*, pages 421–424, Dec 2002. doi: 10.1109/COMMAD.2002.1237280.

[14] G. Cocorullo, F.G. Della Corte, R. de Rosa, Ivo Rendina, A. Rubino, and E. Terzini. Amorphous silicon-based guided-wave passive and active devices for silicon integrated optoelectronics. *Selected Topics in Quantum Electronics, IEEE Journal of*, 4(6):997–1002, Nov 1998. ISSN 1077-260X. doi: 10.1109/2944.736096.

[15] L.A. Coldren, S.W. Corzine, and M.L. Mashanovitch. *Diode Lasers and Photonic Integrated Circuits*. Wiley Series in Microwave and Optical Engineering. Wiley, 2012. ISBN 9781118148174. URL https://books.google.no/books?id=D6Ub126rtPoC.

[16] Mark P Davidson and Neal T Sullivan. Investigation of the effects of charging in sem-based cd metrology. In *Microlithography'97*, pages 226–242. International Society for Optics and Photonics, 1997.

[17] R.M. de Ridder, W.C.L. Hopman, and Feridun Ay. Focused-ion-beam processing for photonics. In *Transparent Optical Networks, 2007. ICTON '07. 9th International Conference on*, volume 2, pages 212–215, July 2007. doi: 10.1109/ICTON.2007.4296183.

[18] B. E. Deal and A. S. Grove. General relationship for the thermal oxidation of silicon. *Journal of Applied Physics*, 36(12):3770–3778, 1965. doi: http://dx.doi.org/10.1063/1.1713945. URL http://scitation.aip.org/content/aip/journal/jap/36/12/10.1063/1.1713945.

[19] K. Divakaruni and IBM. SOI CMOS Technology Through 7nm. Silicon on Insulator Technology Summit, 10 2013.

[20] E. A. Dobisz, C. R. K. Marrian, R. E. Salvino, M. A. Ancona, F. K. Perkins, and N. H. Turner. Reduction and elimination of proximity effects. *Journal of Vacuum Science & Technology B*, 11(6):2733–2740, 1993. doi: http://dx.doi.org/10.1116/1.586593. URL http://scitation.aip.org/content/avs/journal/jvstb/11/6/10.1116/1.586593.

[21] D. Dorfner, T. Zabel, T. Hürlimann, N. Hauke, L. Frandsen, U. Rant, G. Abstreiter, and J. Finley. Photonic crystal nanostructures for optical biosensing applications. *Biosensors and Bioelectronics*, 24 (12):3688 – 3692, 2009. ISSN 0956-5663. doi: http://dx.doi.org/10.1016/j.bios.2009.05.014. URL `http://www.sciencedirect.com/science/article/pii/S0956566309002632`.

[22] A. Einstein. Über einen die erzeugung und verwandlung des lichtes betreffenden heuristischen gesichtspunkt. *Annalen der Physik*, 322 (6):132–148, 1905. ISSN 1521-3889. doi: 10.1002/andp.19053220607. URL `http://dx.doi.org/10.1002/andp.19053220607`.

[23] Yunfei Fu, Tong Ye, Weijie Tang, and Tao Chu. Efficient adiabatic silicon-on-insulator waveguide taper. *Photon. Res.*, 2(3):A41–A44, Jun 2014. doi: 10.1364/PRJ.2.000A41. URL `http://www.osapublishing.org/prj/abstract.cfm?URI=prj-2-3-A41`.

[24] H. Fujioka. Method of manufacturing semiconductor on insulator, October 29 1991. URL `https://www.google.com/patents/US5061642`. US Patent 5,061,642.

[25] M.A. Groeber, B.K. Haley, M.D. Uchic, D.M. Dimiduk, and S. Ghosh. 3d reconstruction and characterization of polycrystalline microstructures using a fib–sem system. *Materials Characterization*, 57 (4–5):259 – 273, 2006. ISSN 1044-5803. doi: http://dx.doi.org/10.1016/j.matchar.2006.01.019. URL `http://www.sciencedirect.com/science/article/pii/S1044580306000623`.

[26] H.A. Haus and S. Kawakami. Coupled-mode theory of optical waveguides. *Journal of Lightwave Technology*, 5(1), 1987.

[27] J. Hovik. Photonic crystal waveguide fabrication. Master's thesis, NTNU, 2012.

[28] M. H. Ibrahim, N. M. Kassim, A. B. Mohammad, and A. S. M. Supa'At. Facet polishing technique for polymer on glass optical waveguide. *Optoelectronics And Advanced Materials-Rapid Communications*, 3(3):223–225, MAR 2009. ISSN 1842-6573.

[29] Henri Jansen, Han Gardeniers, Meint de Boer, Miko Elwenspoek, and Jan Fluitman. A survey on the reactive ion etching of silicon in microtechnology. *Journal of Micromechanics and Microengineering*, 6(1):14, 1996. URL `http://stacks.iop.org/0960-1317/6/i=1/a=002`.

[30] G. A. C. Jones, S. Blythe, and H. Ahmed. Very high voltage (500 kv) electron beam lithography for thick resists and high resolution. *Journal of Vacuum Science & Technology B*, 5(1):120–123, 1987. doi: http://dx.doi.org/10.1116/1.583844.

[31] G.T.A. Kovacs, Nadim I. Maluf, and K.E. Petersen. Bulk micromachining of silicon. *Proceedings of the IEEE*, 86(8):1536–1551, Aug 1998. ISSN 0018-9219.

[32] Mark J. Kushner. Plasma chemistry of He/O2/SiH4 and He/N2O/SiH4 mixtures for remote plasma-activated chemical-vapor deposition of silicon dioxide. *Journal of Applied Physics*, 74 (11):6538–6553, 1993. doi: http://dx.doi.org/10.1063/1.355115. URL http://scitation.aip.org/content/aip/journal/jap/74/11/10.1063/1.355115.

[33] S. L. Lai, D. Johnson, and R. Westerman. Aspect ratio dependent etching lag reduction in deep silicon etch processes. *Journal of Vacuum Science & Technology A*, 24(4):1283–1288, 2006. doi: http://dx.doi.org/10.1116/1.2172944. URL http://scitation.aip.org/content/avs/journal/jvsta/24/4/10.1116/1.2172944.

[34] Kevin K. Lee, Desmond R. Lim, Hsin-Chiao Luan, Anuradha Agarwal, James Foresi, and Lionel C. Kimerling. Effect of size and roughness on light transmission in a si/sio2 waveguide: Experiments and model. *Applied Physics Letters*, 77(11):1617–1619, 2000. doi: http://dx.doi.org/10.1063/1.1308532. URL http://scitation.aip.org/content/aip/journal/apl/77/11/10.1063/1.1308532.

[35] Kevin K. Lee, Desmond R. Lim, Lionel C. Kimerling, Jangho Shin, and Franco Cerrina. Fabrication of ultralow-loss si/sio2 waveguides by roughness reduction. *Opt. Lett.*, 26(23):1888–1890, Dec 2001. doi: 10.1364/OL.26.001888. URL http://ol.osa.org/abstract.cfm?URI=ol-26-23-1888.

[36] Robert E. Lee. Microfabrication by ion-beam etching. *Journal of Vacuum Science & Technology*, 16(2):164–170, 1979. doi: http://dx.doi.org/10.1116/1.569897. URL http://scitation.aip.org/content/avs/journal/jvst/16/2/10.1116/1.569897.

[37] Rob Legtenberg, Henri Jansen, Meint de Boer, and Miko Elwenspoek. Anisotropic reactive ion etching of silicon using SF6/O2/CHF3 gas mixtures. *Journal of The Electrochemical Society*, 142(6):2020–2028, 1995.

[38] C. Liu. *Foundation of MEMS: International Edition*. Pearson Education Limited, 2014. ISBN 9781292013985. URL https://books.google.no/books?id=NQWpBwAAQBAJ.

[39] H.-C. Liu, Y.-H. Lin, and W. Hsu. Sidewall roughness control in advanced silicon etch process. *Microsystem Technologies*, 10(1):29–34, 2003. ISSN 0946-7076. doi: 10.1007/s00542-003-0309-8. URL http://dx.doi.org/10.1007/s00542-003-0309-8.

[40] H.-C. Liu, Y.-H. Lin, and W. Hsu. Sidewall roughness control in advanced silicon etch process. *Microsystem Technologies*, 10(1):29–34, 2003. ISSN 0946-7076. doi: 10.1007/s00542-003-0309-8. URL `http://dx.doi.org/10.1007/s00542-003-0309-8`.

[41] M. Lorvik. Photonic crystal structures: Design and fabrication. Master's thesis, NTNU, 2013.

[42] MP Mack, GD Via, AC Abare, M Hansen, P Kozodoy, S Keller, JS Speck, UK Mishra, LA Coldren, and SP DenBaars. Improvement of gan-based laser diode facets by fib polishing. *Electronics Letters*, 34(13):1315–1316, 1998.

[43] S.A. Maier. *Plasmonics: Fundamentals and Applications: Fundamentals and Applications*. Springer, 2007. ISBN 9780387378251.

[44] S. Martinussen. EBL Fabrication and Ellipsometric Determination of the Optical Characteristics of Plasmonic Gold Nanostructures. Preliminary thesis, 2014.

[45] James Clerk Maxwell. *A Treatise on Electricity and Magnetism*. Clarendon Press Series, 1873.

[46] Gary E McGuire. Semiconductor materials and process technology handbook for very large scale integration(vlsi) and ultra large scale integration(ulsi). *N, Mill Rd. at Grand Ave, Park Ridge, New Jersey 07656, USA, 1988. 675*, 1988.

[47] Nanonics. Lens fiber probes, 2015. URL `http://www.nanonics.co.il/products/lens-fiber-probes`.

[48] Ørnulf Nordseth. *Ferroelectric Thin Films for Planar Photonic Device Applications :*. PhD thesis, Norwegian University of Science and Technology, Department of Electronics and Telecommunications, 2010.

[49] K. Okamoto. *Fundamentals of Optical Waveguides*. Electronics & Electrical. Elsevier, 2006. ISBN 9780125250962. URL `https://books.google.no/books?id=0SNXgnx6un4C`.

[50] Jacques I. Pankove. Temperature dependence of emission efficiency and lasing threshold in laser diodes. *Quantum Electronics, IEEE Journal of*, 4(4):119–122, Apr 1968. ISSN 0018-9197. doi: 10.1109/JQE.1968.1075062.

[51] PMMA. MicroChem PMMA & copolymer datasheet, August 2011. URL `http://www.microchem.com/pdf/PMMA_Data_Sheet.pdf`.

[52] Zexuan Qiang, Weidong Zhou, and Richard A Soref. Optical add-drop filters based on photonic crystal ring resonators. *Optics express*, 15(4):1823–1831, 2007.

[53] M. Quirk and J. Serda. *Semiconductor Manufacturing Technology*. Prentice Hall, 2001. ISBN 9780130815200.

[54] R. Reichelt and L. Reimer. *Scanning Electron Microscopy: Physics of Image Formation and Microanalysis*. Springer Series in Optical Sciences. Springer London, Limited, 2010. ISBN 9783540853176.

[55] Remover PG. MicroChem Nano™Remover PG, 2001. URL `http://www.microchem.com/pdf/removerpg.pdf`.

[56] A.G. Rickman, G.T. Reed, and Fereydoon Namavar. Silicon-on-insulator optical rib waveguide loss and mode characteristics. *Lightwave Technology, Journal of*, 12(10):1771–1776, Oct 1994. ISSN 0733-8724. doi: 10.1109/50.337489.

[57] B.E.A. Saleh and M.C. Teich. *Fundamentals of Photonics*. Wiley Series in Pure and Applied Optics. Wiley, 2013. ISBN 9781118585818.

[58] Dana L Sedin and Kathy L Rowlen. Influence of tip size on AFM roughness measurements. *Applied Surface Science*, 182(1–2): 40 – 48, 2001. ISSN 0169-4332. doi: http://dx.doi.org/10.1016/S0169-4332(01)00432-9. URL `http://www.sciencedirect.com/science/article/pii/S0169433201004329`.

[59] Vishay Semiconductor. NTC Thermistors, May 2012. URL `http://www.vishay.com/docs/29053/ntcintro.pdf`.

[60] Jasprit Singh. *Smart Electronic Materials*. Cambridge University Press, 2005. ISBN 9780511614439. Cambridge Books Online.

[61] Daniel Knight Sparacin. *Process and design techniques for low loss integrated silicon photonics*. PhD thesis, Massachusetts Institute of Technology, Department of Materials Science and Engineering, 2006.

[62] B.G. Streetman and S. Banerjee. *Solid State Electronic Devices*. Prentice-Hall series in solid state physical electronics. Pearson Prentice Hall, 2006. ISBN 9780131497269. URL `https://books.google.no/books?id=xHS8QgAACAAJ`.

[63] Anita Sure, Thomas Dillon, Janusz Murakowski, Chunchen Lin, David Pustai, and Dennis Prather. Fabrication and characterization of three-dimensional silicon tapers. *Opt. Express*, 11(26):3555–3561, Dec 2003. doi: 10.1364/OE.11.003555. URL `http://www.opticsexpress.org/abstract.cfm?URI=oe-11-26-3555`.

[64] Dirk Taillaert, Frederik Van Laere, Melanie Ayre, Wim Bogaerts, Dries Van Thourhout, Peter Bienstman, and Roel Baets. Grating couplers for coupling between optical fibers and nanophotonic waveguides. *Japanese Journal of Applied Physics*, 45(8R):6071, 2006. URL `http://stacks.iop.org/1347-4065/45/i=8R/a=6071`.

[65] David M Tanenbaum, AL Laracuente, and Alan Gallagher. Surface roughening during plasma-enhanced chemical-vapor deposition of hydrogenated amorphous silicon on crystal silicon substrates. *Physical Review B*, 56(7):4243, 1997.

[66] U.N. General Assembly, sixty-eighth session. 68/221. International Year of Light and Light-based Technologies, 2015, 2014.

[67] International Telecommunication Union. Radio regulations, 2012. URL `http://www.itu.int/pub/R-REG-RR-2012`.

[68] Evert P Van de Ven, I-Wen Connick, and Alain S Harrus. Advantages of dual frequency pecvd for deposition of ild and passivation films. In *VLSI Multilevel Interconnection Conference, 1990. Proceedings., Seventh International IEEE*, pages 194–201. IEEE, 1990.

[69] L. Vigen. Silisium racetrack resonator: Design og fabrikasjon. Master's thesis, NTNU, 2014.

[70] Yurii Vlasov and Sharee McNab. Losses in single-mode silicon-on-insulator strip waveguides and bends. *Opt. Express*, 12(8):1622–1631, Apr 2004. doi: 10.1364/OPEX.12.001622. URL `http://www.opticsexpress.org/abstract.cfm?URI=oe-12-8-1622`.

[71] Katrien De Vos, Irene Bartolozzi, Etienne Schacht, Peter Bienstman, and Roel Baets. Silicon-on-insulator microring resonator forsensitive and label-free biosensing. *Opt. Express*, 15(12):7610–7615, Jun 2007. doi: 10.1364/OE.15.007610. URL `http://www.opticsexpress.org/abstract.cfm?URI=oe-15-12-7610`.

[72] G. Wiederrecht. *Handbook of Nanofabrication*. Elsevier Science, 2010. ISBN 9780123751775.

[73] David B. Williams and C. Barry Carter. *Transmission Electron Microscopy: A Textbook for Materials Science*. Springer, 2nd edition, 2009.

[74] A. Yalcin, K.C. Popat, J.C. Aldridge, T.A. Desai, J. Hryniewicz, N. Chbouki, B.E. Little, O. King, V. Van, Sai Chu, D. Gill, M. Anthes-Washburn, M.S. Unlu, and B.B. Goldberg. Optical sensing of biomolecules using microring resonators. *Selected Topics in Quantum Electronics, IEEE Journal of*, 12(1):148–155, Jan 2006. ISSN 1077-260X. doi: 10.1109/JSTQE.2005.863003.

[75] Amnon Yariv. Critical coupling and its control in optical waveguide-ring resonator systems. *IEEE Photonics Technology Letters*, 14(4): 483–485, 2002.

[76] Shiyang Zhu, G. Q. Lo, and D. L. Kwong. Low-loss amorphous silicon wire waveguide for integrated photonics: effect of fabrication process and the thermal stability. *Opt. Express*, 18(24):25283–25291, Nov 2010. doi: 10.1364/OE.18.025283. URL `http://www.opticsexpress.org/abstract.cfm?URI=oe-18-24-25283`.