**NTNU – Trondheim**
Norwegian University of
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# Wideband Harmonically Tuned Power Amplifier Design Based on GaN Technology for use in Envelope Tracking

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# Problem Description

Assignment title: Wideband Harmonically Tuned Power Amplifier Design Based on GaN Technology for use in Envelope Tracking

In many radio systems the efficiency of the power amplifier is extremely important. When a power amplifier is driven near its maximum output power, it will generate higher order harmonic frequency components. A way to increase the efficiency of the amplifier is to tune these components to a desired outcome. In class-F and class-$F^{-1}$, also called harmonically tuned power amplifiers, the impedance of the harmonic components are tuned at the output of the amplifier. This will adjust the shape of the current and voltage, making the amplifier as efficient as possible. This is inherently a narrowbanded technique. Challenges regarding high efficiency operation will become present when designing a wideband power amplifier.

Harmonically tuned power amplifiers with static drain bias voltage will reach maximum efficiency around peak output power. In order to increase efficiency for lower input power the drain bias voltage can be decreased. The decrease of drain bias voltage will stimulate the transistor to enter compression for lower input signals, which in turn will produce harmonics. This technique is called envelope tracking.

The tasks of this assignment are:

- Study the principles of a harmonically tuned amplifier.
- Learn how to use simulation software (Keysight ADS).
- Design and simulate a power amplifier which exhibits maximum efficiency over a relatively large bandwidth.
- Make a layout of the amplifier and manufacture it.
- Measure and characterize the power amplifier.

Specifications for the PA:

| | |
|---|---|
| Center Frequency ($f_0$) | 2.2 GHz |
| Bandwidth (3 dB) | 800 MHz |
| Output Power ($P_{out}$) | $>$ 40 dBm within the bandwidth |
| Gain | $>$ 12 dB within the bandwidth |
| Input match ($S_{11}$) | $<$ -10 dB within the bandwidth |
| Efficiency | as high as possible |

Supervisor: Associate Professor Morten Olavsbråten
Issued at: Department of Electronics and Telecommunications, NTNU, Norway

# Summary

In this thesis, the design, simulation and measurements of a harmonically tuned 10 W wideband high efficiency power amplifier employing envelope tracking is presented. The simulations and design were carried out with the use of the CAD tool Keysight ADS. The optimal impedances for $f_0$, $2f_0$ and $3f_0$ were mapped for both source and load with the help of the load pull technique, and matching networks were designed to try to model the optimal impedances. The matching networks consists of microstrip transmission lines and passive components.

Simulations of the design with lossy components showed an average peak power added efficiency (PAE) of 67% from 1.8 GHz to 2.6 GHz while maintaining 40 dBm (10 W) output power. The final realized design was measured to deliver an average peak PAE of 66% from 1.8 GHz to 2.6 GHz while maintaining 40 dBm output power. The highest measured output was 41.8 dBm (15.1 W) at 1.8 GHz. For the small signal performance the gain was measured to be a maximum of 18.2 dB at 2.4 GHz and maintain 12 dB gain from 1.1 GHz to 2.65 GHz. A 3 dB bandwidth of 1.05 GHz, from 1.55 GHz to 2.6 GHz, was measured for the small signal gain. The input match ($S_{11}$) requirement in the specifications was not fulfilled as this proved to be extremely hard, if not impossible while still fulfilling the rest of the specifications. A solution to reduce $S_{11}$ is proposed at the cost of less gain and efficiency.

Microwave power amplifiers obtain maximum efficiency when operating close to the saturation point. For fixed bias amplifiers the saturation point is close to the maximum output power of the device. The saturation point is dependent on the supply voltage for the amplifier and by modulating the supply voltage high efficiency can be achieved for lower output power levels. Two schemes are used in this thesis to modulate the supply voltage, namely envelope tracking and power tracking. The strengths, weaknesses and the increase in efficiency are explored for the two methods for both two tone and 16-QAM signals. Two tone baseline measurements were taken at 1.8 GHz, 2.2 GHz and 2.6 GHz with a fixed supply voltage while the PA was close to 1 dB compression. This resulted in a PAE of 53%, 52% and 47%. Employing the tracking schemes to the amplifier resulted in a PAE of 63%, 59% and 53% for envelope tracking and 60%, 59% and 51% for power tracking. A 16-QAM baseline was established and resulted in 37%, 22% and 30% for the same frequencies as the two tone test. With the use of envelope tracking the PA was measured to have a PAE of 53%, 39% and 47%. The power tracking scheme resulted in a PAE of 48%, 32% and 39%. The measurements for the tracking schemes shows that the techniques are viable for complex modulation schemes with the use of linearization techniques.

# Sammendrag

I denne oppgaven ble design, simulasjon og målinger av en harmonisk tilpasset 10 W bredbåndet høy-effektivitets effektforsterker med implementasjon av envelope tracking utført. Simulasjonene ble utført ved hjelp av CAD programmet ADS levert av Keysight. De optimale impedansene for $f_0$, $2f_0$ og $3f_0$ ble kartlagt ved hjelp av load pull, og tilpassningsnettverk ble designet for å modellere de optimale impedansene. Tilpassningsnettverket består av microstrip transmisjonslinjer og passive kretskomponenter.

Ikke-ideelle simuleringer av designet resulterte i en gjennomsnittlig maksimal power added efficiency (PAE) på $67\%$ fra 1,8 GHz til 2,6 GHz med mer enn 40 dBm (10 W) utgangseffekt. Det endelige utlegget ble målt til å ha en gjennomsnittlig maksimal PAE på $66\%$ fra 1,8 GHz til 2,6 GHz med overkant av 40 dBm (10 W) utgangseffekt. Den høyeste leverte effekten ble målt til 41,8 dBm (15,1 W) ved 1,8 GHz. Småsignalforsterkningen ble målt til en maksimal verdi på 18,2 dB ved 2,4 GHz og opprettholdt 12 dB forsterkning fra 1,1 GHz til 2.65 GHz. En 3 dB båndbredde på 1,05 GHz fra 1,55 GHz til 2,6 GHz ble oppnådd i målinger. Kravet til inngangstilpassningen ($S_{11}$) ble ikke opprettholdt da dette viste seg å være veldig vanskelig, om ikke umulig gitt resten av spesifikasjonene. En potensiell løsning for å redusere $S_{11}$ er foreslått på bekostning av forsterkning og effektivitet.

Mikrobølge effektforsterkere når maksimal effiktivitet når utganseffekten nærmer seg metningspunktet. For forsterkere med konstant forsyningsspenning er metningspunktet nær maksimal utgangseffekt. Metningspunktet er avhengig av forsyningsspenningen og ved å modulere denne kan høy effiktivitet oppnås for lavere utgangseffekter. To forskjellige funksjoner er brukt for å modulere forsyningsspenningen til forsterkeren, nemlig envelope tracking og power tracking. Styrkene, svakhetene og økningen i effektivitet er utforsket for begge metodene for både to tone og 16-QAM signaler. Målingsgrunnlaget for to-tone testen ble gjennomført på 1,8 GHz, 2,2 GHz og 2,6 GHz med resulterende PAE målinger på $53\%$, $52\%$ og $47\%$. Ved å bruke tracking metodene på effektforsterkeren ble PAE målt til $63\%$, $59\%$ og $53\%$ for envelope tracking og $60\%$, $59\%$ og $51\%$ for power tracking. 16-QAM målingsgrunnlaget ble foretatt med statisk bias for de samme frekvensene som to-tone målingene. Disse målingene førte til en PAE på $37\%$, $22\%$ og $30\%$. Ved å bruke envelope tracking ble effektforsterkeren målt til å ha en PAE på $53\%$, $39\%$ og $47\%$. Med power tracking ble PAE målt til $48\%$, $32\%$ og $39\%$. Målingene av forsterkeren med modulert forsyningsspenning viser at metoden er effektiv med tanke på å øke effektiviteten, men lineariseringsteknikker må bli brukt får å redusere de tilførte ulinearitetene.

# Preface

This thesis is submitted in partial fulfilment with the requirements for the degree of Master of Science (MSc) at the Department of Electronics and Telecommunications, Norwegian University of Science and technology (NTNU). The work was carried out in the time period January 2015 to June 2015, under the supervision of Asc. Prof. Morten Olavsbråten, who is with the Department of Electronics and Telecommunications at NTNU.

## Acknowledgement

First and foremost I would like to thank Asc. Prof. Morten Olavsbråten for his valuable help and input with this thesis. His vast knowledge on the topic of RF power amplifiers helped me to find a good solution and motivate me to solve the problem presented. His enthusiasm combined with his willingness to give comprehensive, detailed answers to my questions were of great importance to me. A special thanks goes to all the wonderful people I have studied with here at NTNU, making these years unforgettable. I would like to thank my family and friends back in Horten for their great support during my 5 year period in Trondheim. I would also like to thank PhD cand. Dragan Mitrevski for help with troubleshooting some of the measured results. Lastly I would like to thank the people at the electronics and prototype laboratory who manufactured the microstrip PCB for the amplifier.

Trondheim, Norway, June 2015.
Richard Samuelsen

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# Abbreviations

| | | |
|---|---|---|
| AC | = | Alternating Current |
| ACPR | = | Adjacent Channel Power Ratio |
| ADS | = | Advanced Design Systems |
| CAD | = | Computer-Aided Design |
| DC | = | Direct Current |
| DUT | = | Device Under Test |
| ET | = | Envelope Tracking |
| GaAs | = | Gallium Arsenide |
| GaN | = | Gallium Nitride |
| HEMT | = | High Electron Mobility Transistor |
| IM | = | Intermodulation |
| IMD | = | Intermodulation distortion |
| OP-AMP | = | Operational Amplifier |
| PA | = | Power Amplifier |
| PAE | = | Power Added Efficiency |
| PAPR | = | Peak to Average Power Ratio |
| PCB | = | Printed Circuit Board |
| QAM | = | Quadrature Amplitude Modulation |
| RF | = | Radio Frequency |
| RFPA | = | Radio Frequency Power Amplifier |
| Si | = | Silicon |
| SOLT | = | Short, Open, Load, Through |
| TRL | = | Through, Reflect, Line |
| VNA | = | Vector Network Analyser |

Chapter 1

# Introduction

Wireless communication is very much a big part of living in the 21st century. Smartphones and notebooks are widespread and have undergone a revolution, leaving them with high performance and diverse functionality. More features and higher performance comes with a cost of increased power consumption, requiring higher battery capacity for the same battery life. The increased power consumption comes from the use of more complex modulation schemes with high peak to average power ratio making the amplifier work in several dB's back off, where the efficiency is low. In recent years focus have been shifted to reduce the physical dimensions of the portable devices, which directly affects the battery capacity negatively. Battery life and environmentally friendly efficient operation can be as important as raw performance for a personal product. Hence, efficiency has become one of the central topics in the wireless communication industry.

The power amplifier (PA) is a key component in wireless communication systems such as smartphones and notebooks. It will often be the governing component in the output stage of a transmitter from a performance point of view, and will determine system characteristics such as linearity, gain and efficiency. In many wireless systems the PA will, next to the screen, be the system component which requires the most power in a wireless device. This has become apparent in later years, especially for smartphones, with the introduction of LTE. LTE sacrifices efficiency for increased performance by using a complex modulation scheme. Increasing the efficiency of the PA for the wireless communication system will effectively increase the battery life of the devices, giving increased market value for the early adopters of the efficiency increasing techniques.

Different characteristics of the PA are important in different scenarios. High efficiency is important for more than increasing battery life, for instance in designing a base station. Increased efficiency in the base station PA will directly decrease the power dissipation, reducing the need for cooling. Complex cooling systems require large amounts of space, are expensive to design and produce, and increase the upkeep cost of the base station. On the other hand output power might be equally important for applications which rely on

long range transmission in noisy environments, and efficiency might be a secondary design goal for such a PA. A constant concern for the designers of power amplifiers are the strict linearity specifications. These are a result of the explosive growth in the number of radio systems, making the designated channels for each communication system relatively small in the frequency domain. All wireless systems must comply with the industry standard so that interference between wireless systems does not occur.

In order to accomplish high efficiency the power amplifier must be driven into nonlinear region and be subject to gain compression. This will generate harmonics of higher order, which will increase the nonlinearities. These higher order harmonics are exploited to increase the efficiency of the PA. The exploitation of harmonics has resulted in a class of amplifier known as class-F, which will be explored in this thesis. In such a design the harmonics are used to shape the drain voltage and current to minimize the overlap between their waveforms, thus reducing the power dissipation of the device and increasing efficiency. Highly efficient operation will only occur for the highest output power levels. Envelope tracking (ET) aims to increase efficiency for the PA by reducing the supply voltage as the output power is reduced and thus resulting in the PA operating at or near the highly efficient nonlinear area for a wide dynamic range of output power.

The transistor used for the power amplifier in this thesis is a Gallium nitride (GaN) high electron mobility transistor (HEMT). GaN HEMT has been commercially available for the last decade. This technology offers improved characteristics in several areas compared to the more traditional gallium arsenide (GaAs) and silicon (Si) technologies. Some improved characteristics are higher breakdown voltage and higher output power which will contribute to higher efficiency as well as less complex amplifier designs.

| | |
|---|---|
| Center Frequency ($f_0$) | 2.2 GHz |
| Bandwidth (3 dB) | 800 MHz |
| Output Power ($P_{out}$) | $>$ 40 dBm within the bandwidth |
| Gain | $>$ 12 dB within the bandwidth |
| Input match ($S_{11}$) | $<$ -10 dB within the bandwidth |
| Efficiency | as high as possible |

**Table 1.1:** Specification for the PA

## 1.1 Outline of the thesis

The following gives a brief introduction to the outline of this thesis.

- **Chapter 1, Introduction**. Consists of an introduction to the thesis and the motivation behind the work covered in the thesis.
- **Chapter 2, Theory**. Preliminary theory regarding the main topics covered in this thesis. This includes a brief introduction to basic microwave theory and an introduction to the most popular microwave power amplifier class operations. An introduction to the envelope tracking scheme is also presented.
- **Chapter 3, Design**. The process of designing a highly efficient wideband power amplifier is presented. Included in this chapter is the choice of bias voltage, ensuring stability for the amplifier, designing bias networks, a brief introduction to the load pull technique and designing a wideband matching network.
- **Chapter 4, Results**. This chapter covers the methods of how the measurements were obtained, preliminary adaptive static bias simulations and measured results for both drain tracking schemes.
- **Chapter 5, Discussion**. The results are discussed and challenges and possible sources of errors are explored. The discussion is split in three parts, one part is designated to the design while the other two are designated respectively to the simulation of the design and the measured results .
- **Chapter 6, Conclusion**. A conclusion to this thesis is given. Further topics and development for the work presented in this thesis are sketched.

Chapter 2

# Theory

The work done in this paper encloses PA design, which can be described as active two-port networks with simple input and output. Therefore some preliminary theory regarding active two-ports and amplifiers in general will be presented in this chapter.

## 2.1 S-parameters

S-parameters, or scattering parameters, are a mathematical method which allows for simplification of complex circuitry by characterizing it as a box with simple input and output. Measuring current and voltage accurately for higher frequencies is a challenging task. S-parameters are instead a measure of the incident and reflected power, which can be more easily quantified at microwave frequencies. A N-port network is shown in figure 2.1, where $V_N^+$ is the amplitude of voltage wave incident on port $N$ and $V_N^-$ is the amplitude of the reflected voltage wave from port $N$. The scattering matrix, which contain the scattering parameters, are then defined in equation 2.1 and will contain $N^2$ parameters. Each of the $N^2$ S-parameters for the N-port network will contain a complex value representing magnitude and phase [13].

$$\begin{pmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{pmatrix} = \begin{pmatrix} S_{1,1} & S_{1,2} & \cdots & S_{1,N} \\ S_{2,1} & S_{2,2} & \cdots & S_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ S_{N,1} & S_{N,2} & \cdots & S_{N,N} \end{pmatrix} \begin{pmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{pmatrix} \tag{2.1}$$

The most common use for S-parameters are the characterization of two-ports. In Figure 2.2 all the S-parameters for a 2-port network are outlined. $S_{11}$ and $S_{22}$ represents, respectively, the input and output reflection coefficients. While $S_{21}$ and $S_{12}$ represents the forward/reverse transmission coefficients. The measurements are only valid when all other ports are terminated to the characteristic impedance $Z_0$. $S_{21}$ can be viewed as the gain of the two-port, while $S_{12}$ is the reverse gain or reverse leakage [2] [8].

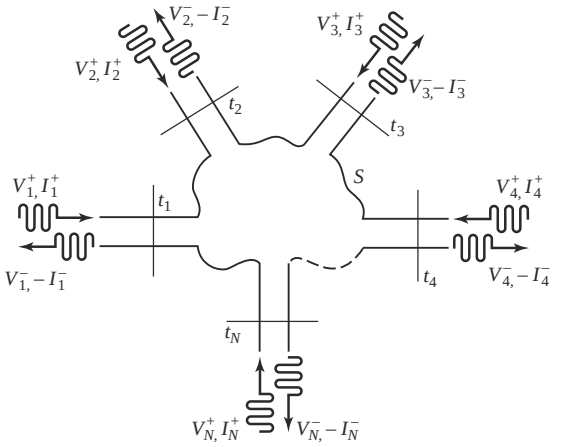



**Figure 2.1:** An arbitrary N-port network [13].

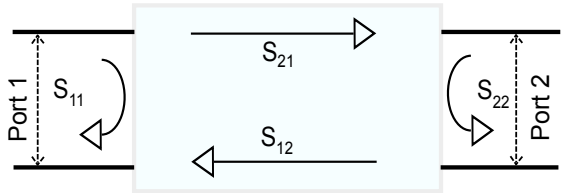



**Figure 2.2:** Scattering Parameters for a 2-port network [6].

## 2.2 Stability

Instabilities are a major concern in PA designs and can lead to unwanted amplifier behaviour like oscillation. Oscillations can result in serious degradation of performance and equipment and is crucial to avoid. Instabilities in amplifiers occur if the source or load impedances have a negative real part, or equivalently $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$ for any $\Gamma_S$ or $\Gamma_L$. Both $\Gamma_{in}$ and $\Gamma_{out}$ are dependent on the matching network, which means that the stability of the amplifier will be dependent on the matching. In addition the matching network impedance will be frequency dependent, which ultimately results in stability to be frequency dependent [2] [13].

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}, \tag{2.2}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} = \frac{Z_{out} - Z_0}{Z_{out} + Z_0}. \tag{2.3}$$

Two cases for stability can be defined:

- Conditionally stable: Conditional stability occurs when the amplifier is stable only for some source and load impedances.
- Unconditionally stable: Unconditional stability occurs when the amplifier is stable for all passive source and load impedances.

Unconditional stability occur when either equation 2.4 and 2.5 are larger than 1 for all frequencies. In addition, a greater value of $\mu$ can be said to indicate greater stability [2] [13].

$$\mu_{source} = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1, \tag{2.4}$$

$$\mu_{load} = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} > 1, \tag{2.5}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{2.6}$$

### 2.2.1 Stability Circles

Stability circles can be employed to plot the boundary between stable/unstable region in the Smith chart. This is useful to visualize the stable region of the amplifier. A brief deduction of the stability circle equations will now be presented. To find the boundary first set $\Gamma_{in}$ = 1:

$$\Gamma_{in} = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| = 1 \tag{2.7}$$

which can be rewritten as

$$|S_{11}(1 - S_{22}\Gamma_L) + S_{12}S_{21}\Gamma_L| = |1 - S_{22}\Gamma_L| \tag{2.8}$$

By using the fact that $\Delta$ is defined as the determinant of the scattering matrix, see equation 2.6, the above result can be written as follows:

$$|S_{11} - \Delta\Gamma_L| = |1 - S_{22}\Gamma_L| \tag{2.9}$$

By squaring both sides, simplifying the expression and completing the square one obtains:

$$\left| \Gamma_L - \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \tag{2.10}$$

Detailed derivation of the full expression becomes cumbersome and can be found elsewhere [13]. An equation of the form $|\Gamma - C| = R$ will represent a circle in the complex plane $\Gamma$. Equation 2.10 will therefore describe the output stability circle with a center $C_L$ and a radius $R_L$ [2][13].

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2}, \tag{2.11}$$

$$R_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right|. \tag{2.12}$$

The equations for source stability circles can be obtained by interchanging $S_{11}$ and $S_{22}$.

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2}, \tag{2.13}$$

$$R_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right|. \tag{2.14}$$

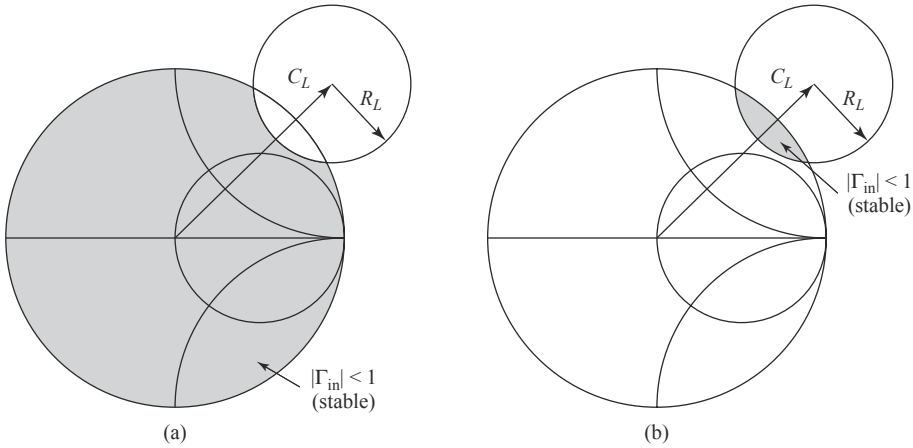



**Figure 2.3:** Stability circles on the output of a conditionally stable device **(a)** $|S_{11}| < 1$ when $Z_L = Z_0$ and **(b)** $|S_{11}| > 1$ when $Z_L = Z_0$ [13].

Figure 2.3 shows two different cases where the device is conditionally stable. For case **a**, the device is stable in the centre of the Smith chart since $|S_{11}| < 1$ when $Z_L = Z_0$. Therefore the unstable region will be inside the stability circle, while everything exterior to the stability circle will be in the stable range for $\Gamma_L$. The stable range is shaded in the figure. For case **b**, the device is unstable when $Z_L = Z_0$ because $|S_{11}| > 1$. This means that the stable region must be the area of the Smith chart that intersects with the stability circle. For an unconditionally stable device the stability circle must either completely enclose the Smith chart or be completely outside of the Smith chart and the amplifier must be stable ($|S_{11}| < 1$) in $Z_0$ [2][13].

## 2.3 Gain

Gain is the amplifiers ability to increase the power or amplitude of a signal. There are three different definitions for the gain of a power amplifier, *power gain*, *available power*

*gain* and *transducer power gain*.

Power gain is defined as the ratio of power delivered to the load to the power applied to the input of the amplifier. Which mathematically can be expressed as:

$$G = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2}. \tag{2.15}$$

As can be seen by equation 2.15 the power gain is not dependent on $\Gamma_S$, but is dependent on $\Gamma_L$. This means that the power gain is independent from the input-impedance of the amplifier. This only holds true for idealized cases as both input and output matching impedance are dependent on each other.

Available power gain is defined as the ratio of the power available from the two-port network to the power available from the source. This gain measure does not depend on $\Gamma_L$, as can be seen by:

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2(1-|\Gamma_{out}|^2)}. \tag{2.16}$$

Available power gain assumes that both source and load are conjugately matched, which means that $\Gamma_{in} = \Gamma_S^*$ and $\Gamma_{out} = \Gamma_L^*$.

The last measure is transducer power gain, which can be viewed as a combination of power gain and available gain. It is defined as the ratio of the power delivered to the load to the power available from the source. This measure is dependent on both $\Gamma_L$ and $\Gamma_S$. Transducer power gain can be expressed as

$$G_T = \frac{P_L}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_{in}\Gamma_S|^2|1-S_{22}\Gamma_L|^2}. \tag{2.17}$$

A single stage amplifier can be modelled as figure 2.4. The amplifier is based around a transistor. There are matching networks on both sides of the transistor which work to transform the input and output impedance to $Z_0$. Separate gain factors for each of these three elements can be defined. The gain of the matching networks are $G_S$ and $G_L$ for source and load respectively and are defined as

$$G_S = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}, \tag{2.18}$$

and

$$G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}|\Gamma_L|^2}. \tag{2.19}$$

The transistor gain by itself can be expressed as:

$$G_0 = |S_{21}|^2. \tag{2.20}$$

The overall transducer gain of the amplifier may then be written $G_T = G_S G_0 G_L$.

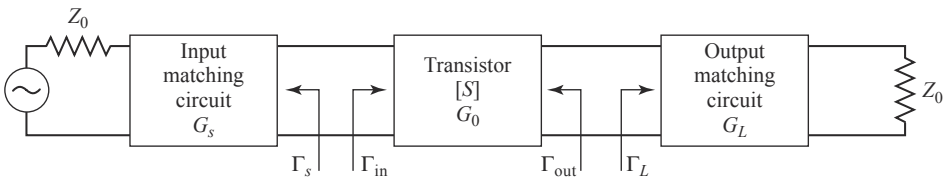



**Figure 2.4:** General transistor amplifier circuit [13].

## 2.4 Matching

The problem of properly matching an amplifier can be complex, especially if wideband matching is required. Both discrete components and transmission lines are common in matching networks, but for higher frequencies, transmission lines are more widely used. The matching network is ideally lossless, and is usually designed so that the impedance seen into the matching network is $Z_0$ to minimize reflection. In figure 2.5 an arbitrary load $Z_L$ has been matched to a transmission line with an impedance of $Z_0$. The reflections to the left of the matching network are then eliminated, however there will be multiple reflections between the matching network and the load $Z_L$ [2].

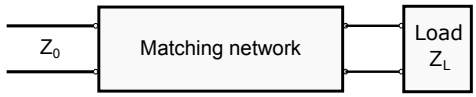



**Figure 2.5:** Network matching an arbitrary load to a transmission line [2].

From section 2.3 and equations 2.18, 2.19 and 2.20 it can be seen that when both source and load are matched to the characteristic impedance $Z_0$, the total gain of the amplifier is that of the transistor $G_0$. The source and load matching must be designed to the specific application of the amplifier. In the case of power amplifiers maximum gain and output power is desirable.

For maximum gain the matching done on the source of the amplifier will be the governing factor. From equation 2.18 it can be seen that maximum gain will be achieved when the input impedance $\Gamma_{in}$ is conjugately matched with $\Gamma_S$.

$$\Gamma_{in} = \Gamma_S^* \tag{2.21}$$

For maximum power transfer to the load, matching on the load side of the amplifier will be the most important factor. To match to maximum power, $\Gamma_L$ should be designed so that $P_{out}$ is as high as possible. Maximum power match can be found by employing load-pulling, which is explained in greater detail in chapter 3.6.

$$\Gamma_{out} \Rightarrow max(P_{out}) \tag{2.22}$$

## 2.5 Efficiency

A very important aspect of designing a power amplifier, or any electronics device today, is how efficienct it is at doing its job. A highly efficient amplifier will require less cooling and increase the time the device can run on battery power given the same output power. There are multiple ways to define efficiency for a power amplifier, but the most common are *drain efficiency* and *power added efficiency*. Drain efficiency is the RF output power divided by the DC input power, and is defined as:

$$\eta = 100 \cdot \frac{P_{OUT}}{P_{dc}}. \tag{2.23}$$

Drain efficiency does not take RF input power into account, so for a better model with respect to thermal dissipation and actual power applied to the amplifier, the RF input power needs to be included in the efficiency equation. Therefore power added efficiency (PAE), defined mathematically as:

$$PAE = 100 \cdot \frac{P_{OUT} - P_{IN}}{P_{dc}} = \eta \cdot \left(1 - \frac{1}{G}\right), \tag{2.24}$$

will be used in this paper when efficiency is referred to. In the equation for power added efficiency G denotes the gain of the device. For high gain devices the PAE and drain efficiency will virtually be the same.

## 2.6 Linearity

A linear amplifier is an amplifier whose output is proportional to the input. Nonlinearities can present itself in different ways. One way is the intermodulation distortion (IMD) products. These components are the result of applying a signal with more than one frequency component in its spectrum. To better visualize this, the output spectrum of an amplifier whose input signal consists of two different frequencies is depicted in figure 2.6. The frequency components $f_1$ and $f_2$ are the signals which are applied to the input of the amplifier. The other frequency components in the spectrum are a result of IMD. The IMD products, which have been limited to only include $5th$ order in figure 2.6, can be a serious limitation to linearity. If $f_1$ and $f_2$ are close in frequency, e.g. a spacing of 5 MHz at a center frequency of 2.4 GHz, the 3rd. order IMD products can become troublesome and hard to remove from the output spectrum.

Linearity will also be impaired by the compression of the output signal which occur due to the saturation of the transistor. In figure 2.7 an idealized amplifier response and a more realistic non-ideal response of an amplifier has been plotted. In this figure the non-ideal response is called actual response. For the lower levels of input power the actual response of the amplifier will be linear and closely be that of an ideal response, which will result in low harmonic and IM distortion. However, at lower input levels the amplifier will operate inefficiently as well as having lower output power. In order to get higher efficiency the amplifier will need to be driven harder which will force the amplifier response into

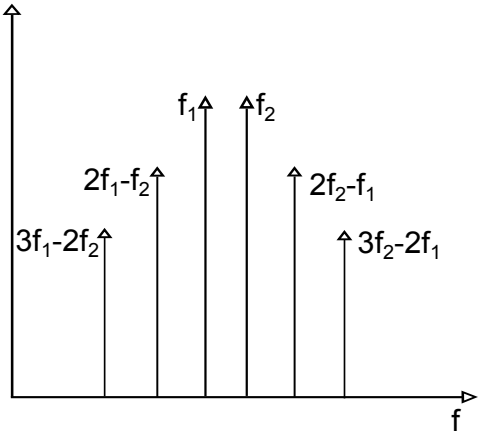



**Figure 2.6:** Output spectrum of a PA showing IMD products [1].

compression. Harmonics with the frequency $n \cdot f_0$, where n is an integer, as well as IMD products will be added to the output spectrum of the amplifier. The harmonics can be exploited for better efficiency with the design of a good output matching network. This method will be described in section 2.9. It is important to note that there is a trade off between efficiency and linearity. For good linearity performance the amplifier will be significantly inefficient without the use of advanced linearization techniques like gate tracking or predistortion [1][14].

Two common measurements for nonlinearity are the 1 dB compression point and 3rd order intercept point. The 1 dB compression point is where the input power of the amplifier is such that the output power deviates 1 dB from the ideal amplifier response and represents the amplifier driven to medium distortion. The 3rd order intercept point is a fictitious point where the linear idealized gain of the device intercepts the linear third harmonic line. In figure 2.7 both the 1 dB compression point and the 3rd order intercept point are depicted.

## 2.7 Memory effects

For an ideal nonlinear PA the gain will only be a function of the input signal. The gain response for an ideal nonlinear PA is plotted as the blue dotted line in figure 2.7. The gain of a real PA will also be given as a function of what is known as *memory effects*. Memory effects will add to the nonlinearities of a PA and will be the cause of deviation between static and dynamic characteristics. Any form of element that is capable of storing energy will introduce memory to the system. For instance, a heatsink can release heat into the device after high power operation. Another very common memory inducing element are inductors and capacitors. This can be directly seen from voltage equation for a capacitor

$$v_C(t) = \frac{1}{C} \cdot \int_{-\infty}^{t} i(t')\,\mathrm{d}t'. \tag{2.25}$$

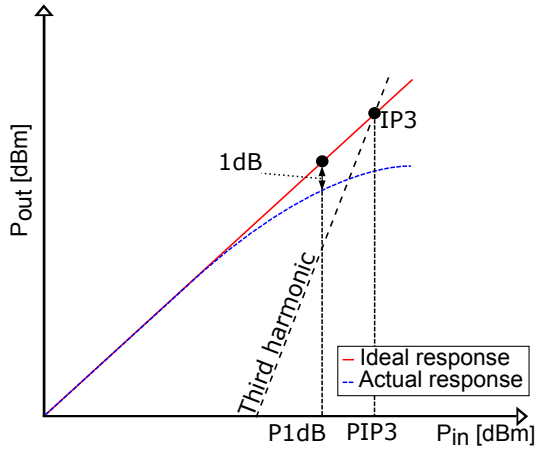



**Figure 2.7:** Amplifier response showing 1 dB compression point and 3rd order intercept point [1].

The voltage at time $t$ is proportional to all prior current values, and not just the instantaneous value [1][14]. There are other main causes for memory effects which can be characterized as:

- Modulation of supply rail
- Semiconductor trapping effects
- Dynamic thermal effects

The most common reason for memory effects and asymmetrical IM sidebands is modulation of supply rail. This can cause major linearity issues as the gain of the PA and the amount of compression will change. Modulation of the supply rail can be avoided by carefully designing the biasing network for the PA, as the reason for this modulation is that a portion of the RF signal propagates to the power supply [1][14].

The trapping effect is usually most apparent in a device if it is placed in cut-off region and then rapidly switched on into the linear region. The current can then be observed and is expected to reach steady state in a relatively fast response. Usually in a matter of picoseconds. The device may not actually reach steady state before microseconds, milliseconds or even seconds have passed. This is caused by electrons being ”trapped” in the semiconductor channel. The electrons will be released in a seemingly random fashion, which will result in nonlinearities [1][14].

Fluctuations in device temperature is widely accepted to cause nonlinear effects. The gain of the DUT will be temperature dependent and adequate cooling is therefore critical. The semiconductor device will heat up and cool off for slower envelopes causing distortion to the signal based on previous states[1][14].

## 2.8 Amplifier Classes

### 2.8.1 Class-A

A class-A amplifier is an amplifier which the operating point is chosen so that the collector/drain current flows at all times, thus a conduction angle of $360°$. It therefore operates in the linear portion of the amplifier characteristics and the signal will suffer minimal distortion. As mentioned in section 2.6 the trade off for linearity is efficient operation. This is where class-A amplifiers are inferior to the other classes. The maximum drain efficiency of a class-A amplifier with a supply voltage of $V_{DD}$ can be calculated [7]:
First, define $V_{max}$ as the peak voltage across the load $R_L$ and require the output current to be positive:

$$I_{DC} = \frac{V_{max}}{R_L} \leq \frac{V_{DD}}{R_L} \tag{2.26}$$

$V_{max}$ has to be less than the supply voltage $V_{DD}$ for anything other than idealized cases because of the non-zero saturation voltage of the transistor. The power delivered from the supply may then be written:

$$P_{supply} = V_{DD} I_{DC} = \frac{V_{DD}^2}{R_L} \tag{2.27}$$

Now assume that the signal applied to the load is a sine wave. The RMS output power supplied to the load is then:

$$P_{load} = \frac{V_{max}^2}{2R_L} \leq \frac{V_{DD}^2}{2R_L} \tag{2.28}$$

The overall efficiency can then be written as:

$$\eta = \frac{P_{load}}{P_{supply}} = \frac{V_{max}^2}{2V_{DD}^2} \leq \frac{1}{2} \tag{2.29}$$

This means that the theoretical maximum *drain efficiency* of a class-A amplifier is $50\%$ when the saturation voltage across the transistor is zero. The non-zero saturation voltage of the transistor, which can be several volts, will reduce the drain efficiency to less than $50\%$. The maximum efficiency which includes the non-zero saturation voltage can then be expressed as [7]

$$\eta_{max} = \frac{V_{DD} - V_{sat}}{2V_{DD}}. \tag{2.30}$$

### 2.8.2 Class-B

The class-B amplifier is one in which the operating point is chosen so that the amplification takes place for only half the cycle. The conduction angle is then $180°$. The drain efficiency of the class-B amplifier can be deduced similarly to that of the class-A amplifier. It is not included in this paper, but can be found in other literature [7]. The maximum drain efficiency is given by equation 2.31.

$$\eta = \frac{\pi}{4} \approx 78.5\% \tag{2.31}$$

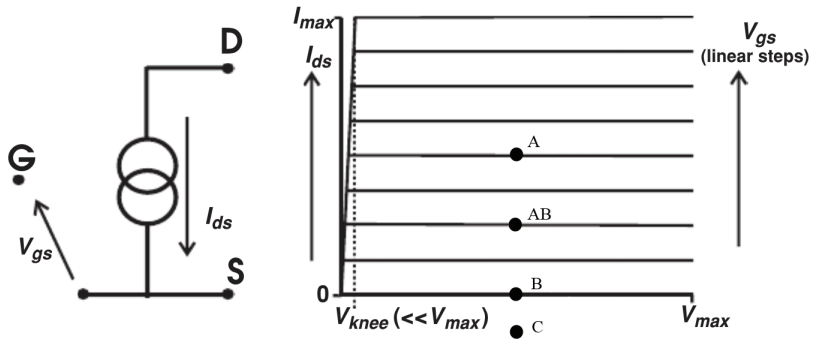



**Figure 2.8:** Operating points of the different classes [10].

Class-B operation is significantly more efficient than class-A, while still offering useful linearity[7].

### 2.8.3 Class-AB

The class-AB amplifier is a compromise between the class-A and class-B amplifier in both efficiency and linearity, and has been a popular class for RFPA designers for several generations. It has a conduction angle between $180° - 360°$ depending on the operation point chosen by the designer. The operation point governs the maximum drain efficiency which will be between $50\% - 78.5\%$ [7] [9].

### 2.8.4 Class-C

The class-C amplifier is characterised by the operating point being chosen such that the output current is zero for more than half of the input signal cycle given an input of a sine wave. This means that the conduction angle is less than $180°$. This is accomplished by biasing below the cut off region. This class of amplifiers will result in significant distortion and thus will be unsuitable for applications where linearity is an issue. Theoretical maximum drain efficiency of $100\%$ is possible, but in real life applications the efficiency is reduced to approximately $75\%$.

## 2.9 Class-F amplifier

The class-F amplifier is a reduced conduction angle amplifier with load harmonic modulation, which means that the harmonics are used to shape the intrinsic voltage and current waveforms of the transistor so that minimal overlap between the waveforms occur. This overlap between current and voltage waveforms will materialize itself as added heat and power dissipation to the transistor, which will inhibit efficient operation. The power that

is dissipated can be described mathematically as

$$P = V \cdot I. \tag{2.32}$$

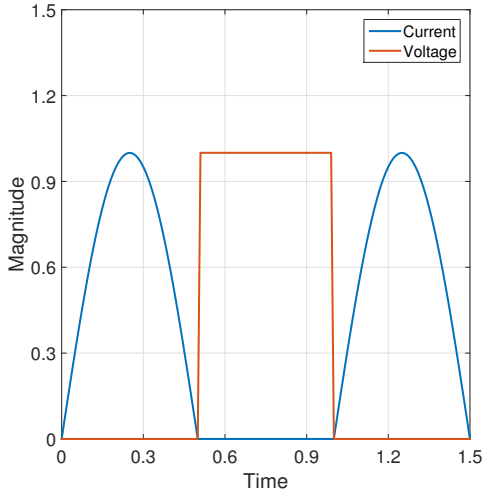



**Figure 2.9:** Ideal class-F waveforms.

An ideal class-F amplifier will have an efficiency of 100% which can be explained with figure 2.9. There will be no overlap between the current and voltage and thus no power dissipation in the transistor. In order to reach 100% efficiency $n = \infty$ harmonics need to be perfectly tuned. The harmonics used in the tuning process needs to be generated from the transistor, which means that the transistor must be driven into compression so that it can distort the signal. To be able to achieve this kind of compression and distortion the transistor needs to be biased near the cut-off region and a suitably large input signal must be applied. Therefore the transistor is usually biased in deep class-AB or class-B region. As can be seen by figure 2.9 the drain voltage waveform will be ideally square shaped, while the drain-current will be half sine wave for a class-F design. This shaping of the intrinsic waveforms is achieved by reflecting all odd order harmonic components back to the drain node on the transistor. The even order harmonics must be shorted to ground. This will remove higher order harmonics from the output spectrum and a current shape of a half sine wave will be achieved. The reflection of the higher order odd harmonics will result in a square shaped drain-voltage. Because of the non ideal transistors and limited gain as frequency increases, this is impossible to achieve. However it is common to include harmonics in the order of 3 or 4 in the matching network design process. This will increase the efficient operation of the amplifier for larger input signals [1][7].

There is also a class called the inverse class-F or class-F$^{-1}$ which is based on the exact same principle as class-F. The only difference in operation is that the voltage is now shaped to a half wave sine and the current will be square shaped. The design of the amplifier will be similar to the class-F, but the output matching network must be designed to short odd

order harmonics and reflect even order harmonics. It is important to note that the phase of the current and voltage is extremely important to be able to minimize the overlap in both class-F and class-$F^{-1}$. Too much of a phase-shift can seriously degrade the efficient operation because overlap between voltage and current will occur and power will be dissipated in the device.

## 2.10 Envelope tracking

Envelope tracking (ET) is an efficiency enhancing technique which continually adjust the supply voltage of the amplifier in order to ensure that it is working at peak efficiency. ET has become more widespread in modern times as more complex modulation schemes with a higher peak to average power ratio (PAPR) are being used. Fixed bias RF amplifiers will operate at peak efficiency only when driven into compression, which complex modulation schemes with a high PAPR will not achieve for most of the signal. ET seek to make the RF amplifier work at peak efficiency for a wide range of signal power levels. This will however introduce more distortion as well as increased system complexity.

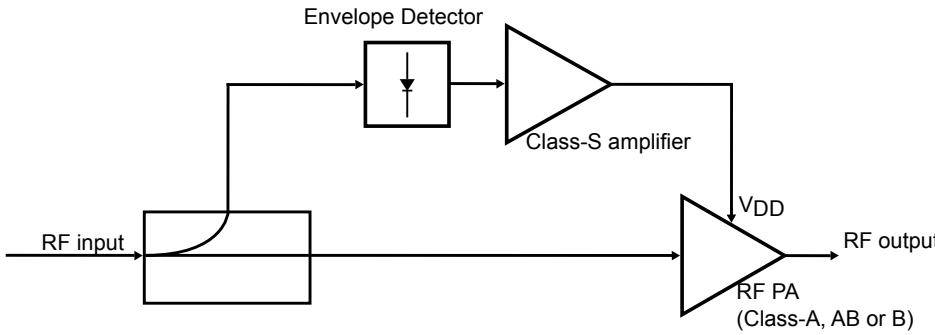



**Figure 2.10:** Schematic of a typical ET scheme employed on a RF amplifier [1] [7].

The main idea behind envelope tracking can be clarified with reference to figure 2.10. The RF input signal enters a coupler which splits the signal into two paths. One enters the RF PA and the other enters an envelope detector. The envelope detector can be made with a diode and a low pass filter. The diode ensures that only the positive part of the signal gets sent to the filter. The low pass filter extracts the low frequency components of the signal, which in this case is the signal envelope. The envelope is then amplified up to a suitable level so that it can modulate $V_{DD}$ on the main RF PA. The envelope amplifier can for instance be an audio amplifier (class-S) or an amplifier with bandwidth in the MHz region. However, the critical design point is that the envelope amplifier needs to be highly efficient. This can be seen from equation 2.33 where an approximation for the total system efficiency is the envelope amplifier efficiency times RFPA efficiency.

$$\eta_{tot} \approx \eta_{EnvAmp} \cdot \eta_{RF} \tag{2.33}$$

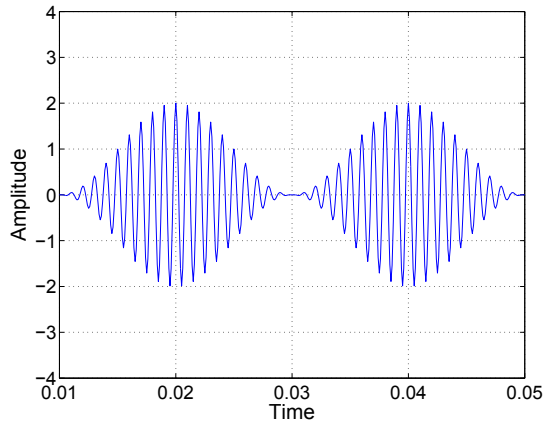



**Figure 2.11:** Waveform of a two tone signal.

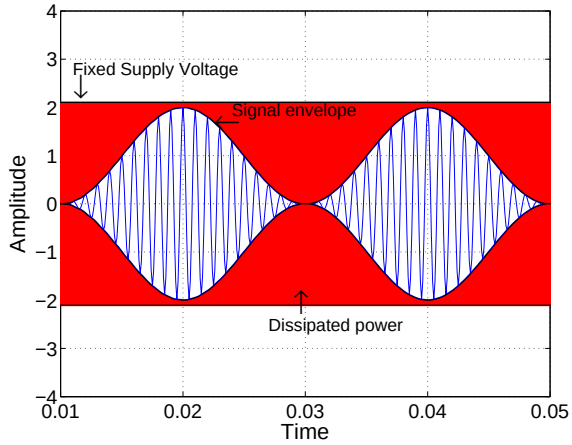



**Figure 2.12:** Power dissipation for an amplifier with static drain bias.

Now for an idealized example. Lets assume the output signal consists of the two tone signal plotted in figure 2.11. With a static drain bias voltage the dissipated power is plotted as the red area in figure 2.12. If the bias voltage now is allowed to track the envelope of the signal, the average dissipated power will be heavily reduced. This is shown in figure 2.13. One of the strengths of this technique is that the modulation of the drain voltage does not have to be very accurate. The voltage offset of the tracking function in comparison to the signal envelop decides the amount of distortion and how far into compression the envelope tracked amplifier operates. For instance, the tracking function can be made to follow the

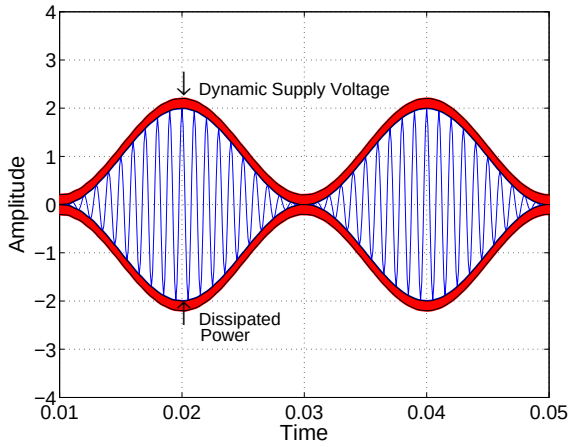



**Figure 2.13:** Power dissipation for an amplifier with dynamic drain bias.

signal envelope closely by choosing a small offset. By increasing this offset compared to the signal envelope the envelope tracked amplifier will operate with less distortion. The offset voltage is shown in figure 2.16

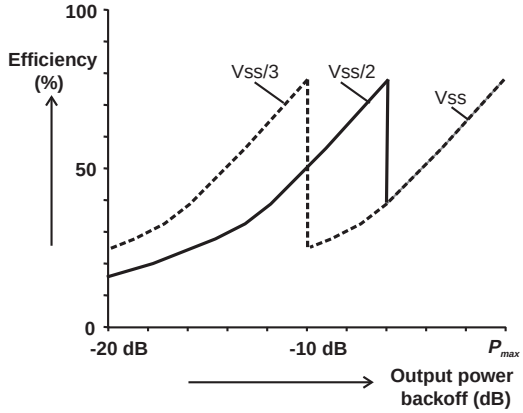



**Figure 2.14:** Efficiency for a multi level bias amplifier [1].

Figure 2.14 shows the efficiency of an ideal class-B amplifier with a simplified ET scheme versus the output power for three different drain bias voltages. The different bias voltages will all result in the same peak efficiency, but this will occur for different output power levels. By intelligently switching the bias voltage between the three levels one can achieve much higher efficiency for the low and medium powered output. For the few upper dB of

output power there will not be any bias switching and thus no increase in efficiency. A fully implemented envelope tracking scheme is based on dynamically adjusting the drain voltage for all output levels so that high efficiency can be obtained for a large output power range.

The effects of this can be seen in figure 2.15 where the drain bias voltage has been swept in equal steps for a simulated PA. The red line depicts the envelope tracking scheme tracking at 1 dB compression. This means that the amplifier will constantly be in 1 dB compression as long as envelope tracking occur. Tracking will stop at a chosen supply voltage when the output power level decreases past a set point and the amplifier will then follow the fixed bias PAE curve. This behaviour is shown as the red line following the PAE curve for the lowest supply voltage. The power tracking scheme will follow the curve for $V_{DD}/2$ up to certain power level before tracking takes place. As the output power increases the difference between the two schemes will decrease. In this figure the effects of supply tracking are evident as efficiency is increased for lower power levels. The curves for the tracking schemes are approximated from simulations and are not identical with the tracking function of a real PA. An interesting possibility of tracking different drain function arises from this figure. Tracking at different PA characteristics is possible. E.g. tracking at peak efficiency is possible and the tracking function for this will follow the PAE peak for each supply voltage. Tracking at 2 dB compression is a possibility and will result in a higher PAE compared to 1 dB. It all depends on the purpose of the amplifier. For an ideal transistor the peak of the PAE curves of each supply voltage would be identical. The reason for the increase in peak PAE as the supply voltage increases is the knee voltage of the transistor not being equal to zero. The knee voltage will be a decreasing fraction of the supply voltage as it increases and thus the peak PAE will increase.

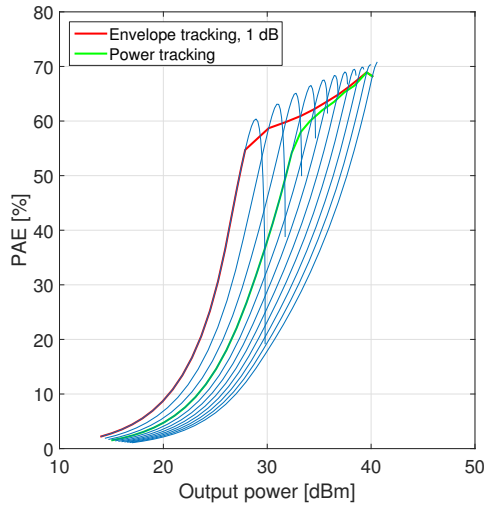



**Figure 2.15:** PAE for a simulated PA with supply voltage steps of 2 V. The red line depicts a envelope tracking scheme and the green line depicts a power tracking scheme.

Figure 2.16 shows the tracking functions for an ideal transistor. The transistor is ideal in the sense that the saturation voltage is zero. This figure shows what the necessary drain voltage, $V_D$, needs to be as a function of the RF envelope voltage $V_{RF}$ for a given tracking scheme. The envelope is defined as:

$$E = I + jQ, \tag{2.34}$$

for a signal operating with I/Q data and will consist of both negative and positive voltages. ET will track the absolute value of the envelope voltage and thus the tracking function is described as:

$$|E| = \sqrt{I^2 + Q^2}. \tag{2.35}$$

Because of the square root operation, ET will in theory require infinite bandwidth of the tracking amplifier to track perfectly. This is demanding on the tracking amplifier and therefore an alternative method of tracking was also explored and compared to ET, namely power tracking. Tracking the RF power of the amplifier can be done by using the tracking function:

$$P = |E|^2 = I^2 + Q^2. \tag{2.36}$$

This method does not require any square root operation and will only demand the bandwidth of the RF envelope to track perfectly, thus making the tracking amplifier design simpler. The drawback of this method comes in the form of less efficiency compared to ET. This can be seen from figure 2.16 where the tracking functions are plotted and the power tracking voltage is higher than the ET scheme for low output power levels. For the higher power levels the power tracking scheme will follow the ET scheme almost identically. ET will follow the ideal envelope of the transistor with a given voltage offset. This offset will govern the amount of compression and efficiency for the envelope tracking scheme. The smaller this offset is, the closer the ET will follow the RF envelope and higher efficiency will be achieved at the cost of linearity and gain. The tracking functions are not allowed to track under the RF envelope as this will result in the amplifier gain collapsing. This area is called the forbidden area in the figure. For the idealized case the envelope tracking scheme will track down to the offset voltage chosen and up to $V_{Dmax}$. The power tracking will ideally track down to $V_D/2$ and up to $V_{Dmax}$.

For the performance of the ET scheme it is extremely important that the modulated drain bias from the envelope amplifier gets properly synchronised with the RF signal. A minor unsynchronisation will contribute to signal distortion, less efficient operation and asymmetrical IM sidebands. This may be a major concern for modern radio systems as the requirements for IMD can be very strict.

## 2.11 Measurements

In the following section errors connected to measurements and methods to minimize the errors are described.

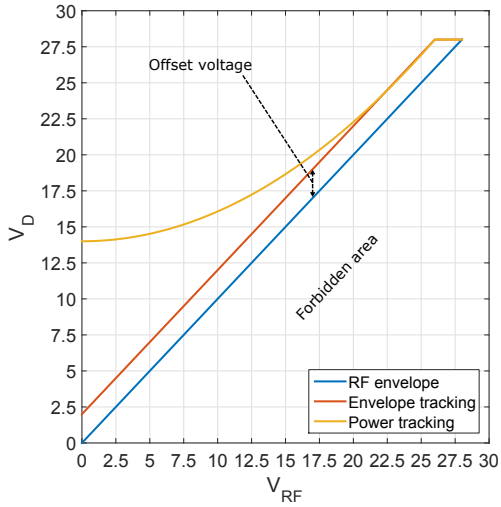



**Figure 2.16:** Tracking functions for both ET and power tracking given an ideal transistor.

### 2.11.1 Small signal measurements

A vector network analyser (VNA) was used to carry out the small signal measurements. The VNA measures the S-parameters for the device connected and consists of a transmitter, two RF-cables to connect the device under test (DUT), a receiver, an information panel and a control panel.

When conducting measurements there will always be some measuring errors. Some of the factors that contribute to measurement errors are repeatable over time, for instance loss in cables. The repeatable and predictable errors can be calibrated for and therefore mathematically eliminated. Some errors are random and cannot eliminated through calibration, for instance instrument noise. There are three types of error sources connected to measuring which concerns all types of equipment:

- Systematic errors
- Random errors
- Drift errors

*Systematic errors* are errors that are predictable and repeatable over time. These are caused by imperfections in the test setup and equipment. Common errors include signal leakage, reflection and the frequency response of cables and connectors. Systematic errors can be effectively removed by calibrating the equipment.

*Random errors* are errors that are unpredictable and non-repeatable over time. Causes for these errors can be hard to identify, but common causes are instrument noise and other noise sources. These errors cannot be calibrated for, but the impact can be reduced with

the use of averaging the measurements.

*Drift errors* are errors that occur when the external and/or internal parameters, like temperature, change after the equipment is calibrated. These errors can be minimized by having the test equipment in an environment with controlled temperature and frequent calibrations.

### 2.11.2 Measuring Power Amplifiers and use of attenuation

When measuring a high power DUT such as power amplifiers, attenuation of the output is important in order to not damage the VNA. However, attenuators will introduce a source of inaccuracy. While the attenuation will be mathematically removed from the measurements with proper calibration, the measured data will suffer in accuracy. Each time the signal passes through the attenuator it will be brought closer to the noise floor of the VNA. This is not especially troublesome for the forward gain, $S_{21}$, as the attenuation only occurs once, but will become a bigger issue for the reflected wave on the output which will be attenuated multiple times.

## 2.12 Calibration

There are two common calibration kits that are employed for VNA calibration. SOLT (short, open, load and through) and TRL (trough, reflect and line). SOLT is the most common for coaxial interface, while TRL is more common in in-fixture and on-wafer environments [12].

**SOLT** consists of well defined short, open and load of a characteristic impedance. The calibration is easy to perform and offer calibration from DC up to the upper frequency limit of the equipment. To utilize SOLT calibration the short, open and load standards are connected one by one to each port on the VNA so that the VNA can measure them. When this is done the two reference planes are then connected together with the trough component. This enables the VNA to mathematically remove systematic errors for each path. SOLT calibration does offer good repeatability given sound calibration practices from the user, as well as ease of use and good accuracy of the calibration. SOLT may also be made to user specification and therefore be able to accommodate many different user requirements [12].

**TRL** is well suited to measure devices that are not connectorized or devices that does not share the same connector type as the measuring equipment. TRL does not require well defined calibration standards as SOLT does. However, TRL requires a short through component, preferable of zero length and at the same impedance as the line standard. It does also require a highly reflective standard as well as a line at the characteristic impedance of the system. The TRL calibration is often manufactured and characterised on the same material as the DUT. In comparison to SOLT, TRL is less straightforward to use, but offer a higher degree of accuracy and repeatability of the calibration [12].

Chapter 3

# Design of the power amplifier

## 3.1 Cree CGH40010

The PA in this paper is based on the CGH40010 transistor from Cree. This is an unmatched, 10 W, gallium-nitride (GaN), high electron mobility transistor (HEMT). The transistor operates from a 28 V rail and is a general purpose transistor. Some of the features of the Cree CGH40010 includes[3]:

- Up to 6 GHz operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical $P_{SAT}$
- 65 % Efficiency at $P_{SAT}$
- 28 V operation

## 3.2 Choice of gate bias voltage

From section 2.8 and 2.9 it is clear that the transistor needs to biased in class AB or B in order to achieve harmonically tuned operation. Class AB operation was chosen to get a compromise between linearity and efficiency. According to the datasheet of the Cree CGH40100 transistor [3] a gate bias voltage of -3 V and higher will make the simulator model of the transistor conduct. Therefore a voltage sweep from -3 to -1.5 V with a 100 mV step was performed to plot the IV characteristics of the transistor. With a simple testbench in ADS, which measures the drain current versus drain voltage for each gate voltage specified, a gate voltage of $V_{GS} = -2.8V$ was found to be a good point to bias the transistor with regard to class AB operation. This bias point will result in a drain current of

$I_{DS} = 163$ mA, a voltage swing from 5 V to 28 V and $I_{DS_{max}} = 1049$ mA. The biasing point with its related simulated results are depicted in figure 3.1.

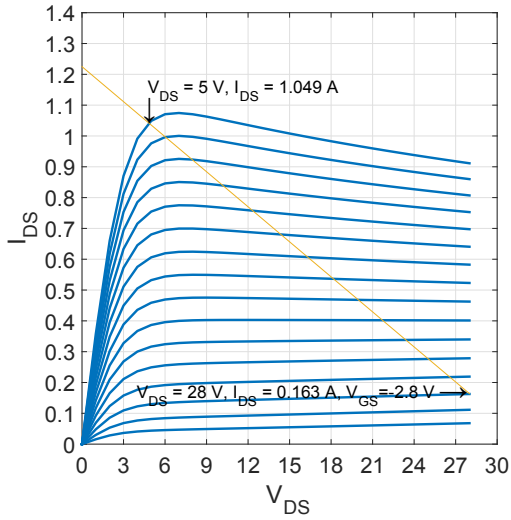



**Figure 3.1:** IV curves for the CGH40100 transistor.

## 3.3 Substrate

For this amplifier the substrate was chosen to be flame retardant 4, also known as FR4. This substrate is very popular, inexpensive, versatile and retains its electrical properties in both dry and humid conditions. In table 3.1 the substrate parameters used in the simulations are listed.

| H | Er | Mur | Cond | T | tan($\delta$) |
|---|---|---|---|---|---|
| $1.6 \cdot 10^{-3}m$ | 4.4 | 1.0 | $5.96 \cdot 10^{7}$ | $36 \cdot 10^{-6}m$ | 0.02 |

**Table 3.1:** Substrate parameters used in the simulations.

## 3.4 Stability

Now that a gate biasing point, $V_{GS}$, had been chosen, stability became an issue. In section 2.2 two methods of testing unconditional stability were introduced. $\mu$ factors, given in equations 2.4 and 2.5, with the addition of stability circles were used to ensure stable operation for all frequencies. A design goal was set to always require the $\mu$ factors to be greater than one. Two methods were utilized to provide stability in the design process.

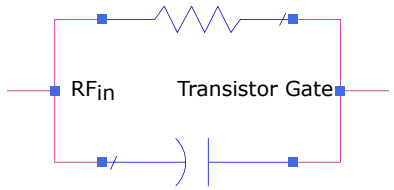



**Figure 3.2:** High pass filter stability network.

The first method is depicted in figure 3.2 and consists of a capacitor and a resistor in parallel, in series with the gate. The resistor will add attenuation for all frequencies. This helps the transistor in becoming stable, but will also introduce attenuation in the operational bandwidth of the amplifier, reducing the gain. A capacitor was added in parallel to the resistor, reducing the attenuation as frequency increases. Capacitors are components whose impedance will be dependent on both capacitance and frequency. The impedance of a capacitor can be calculated as

$$Z_C = \frac{1}{j\omega C} = \frac{1}{j2\pi f C}, \tag{3.1}$$

where $C$ is the capacitance of the capacitor and $f$ is the frequency of the signal. The equivalent series impedance of the parallel stability network presented in figure 3.2 is given as

$$Z_{eq} = \frac{Z_C Z_R}{Z_C + Z_R} = \frac{\frac{1}{j\omega C} R}{\frac{1}{j\omega C} + R} = \frac{R}{1 + j\omega C R}, \tag{3.2}$$

where $Z_R$ is the impedance of the resistor given by

$$Z_R = R. \tag{3.3}$$

From equation 3.2 it is seen that the impedance will be reduced for the high pass stabilizing network when the capacitance or the frequency increases. This is desirable as high gain in the operational frequency band is wanted for a PA. With regard to stability the reduced attenuation will not become an issue for higher frequencies as the transistor gain will decrease and therefore become inherently stable.

The frequency response of the high pass stabilizing filter topology is shown in figure 3.3. As is seen in this figure the stabilizing network will function as a high pass filter, attenuating low frequencies while allowing high frequency signals to propagate relatively uninhibited. A non ideal model including parasitic circuit elements for the capacitor was used in this simulation and the component values was R = 100 Ω and C = 1.8 pF.

The second method was to add a small resistor in series with the DC network on the gate of the transistor. This will attenuate the relatively small RF signal which travels up to the DC network and gets reflected back to the gate, which will further help with stability. It is important to note that the current drawn on the gate is very small, ideally zero, and the RF

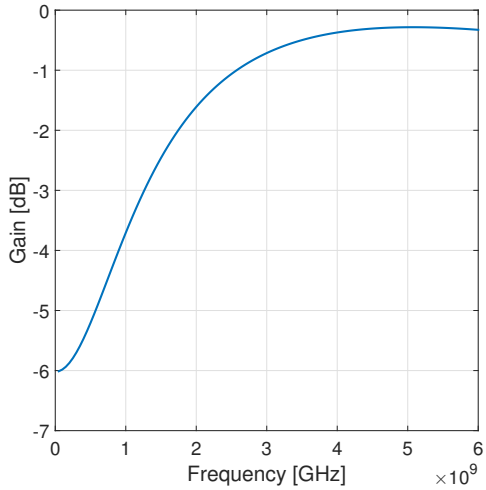


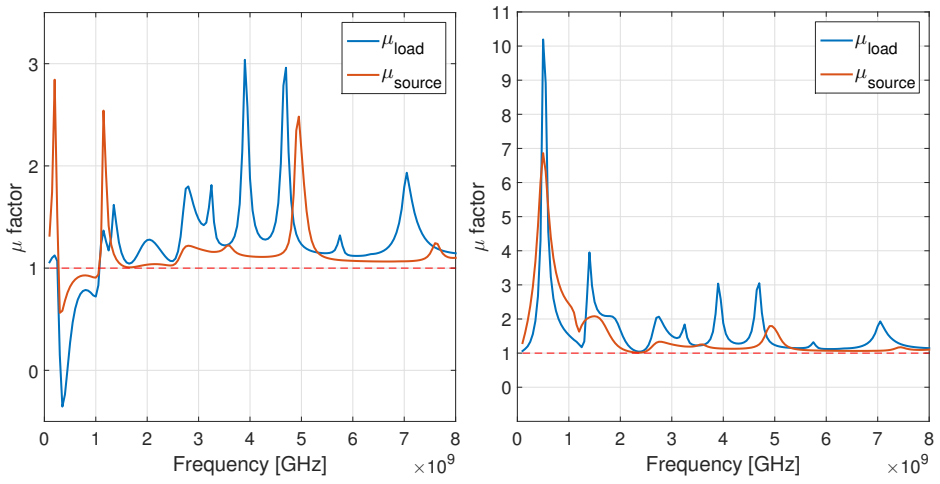

**Figure 3.3:** High pass filter stability network frequency response.

input signal should in theory not propagate into the DC network and thus the resistor in the DC network will not affect efficiency or gain in any significant way. Still, the resistor should be of small value. Ohm's law,

$$V = RI, \tag{3.4}$$

states that a current, I, passing through a resistor, R, will force there to be a voltage potential difference across this resistor. If there is a small current passing through the gate bias resistor for the realized amplifier the gate bias voltage can be changed and cause distortion or degradation of performance. The resistor was not included in the drain bias network as this will reduce the output power and efficiency. For this design the resistor was chosen to be 10 Ω. This resistor was included into the design process of the gate bias network and will be described in more detail in section 3.5.

In figure 3.4 the $\mu$ factors before and after stabilization are plotted. The red dotted line denotes the limit that ensures unconditional stability. Before any stabilization the amplifier is potentially unstable up to 1 GHz. By using the two stabilization techniques of the series gate bias resistor and the high pass filter the amplifier becomes unconditionally stable for all frequencies. A greater value of $\mu$ factors indicates a greater stability margin. Around 500 MHz the $\mu$ factors are at their highest value, which can be seen in figure 3.4b. This was a conscious design choice as the bias network decoupling capacitors which usually work in this range must be removed from the drain bias network when performing ET. When envelope tracking, the drain bias will not remain a DC voltage, but instead a low frequency AC voltage. The low frequency decoupling capacitors will form a low impedance coupling to ground and must be removed. A higher margin of the $\mu$ factors will help with keeping the PA stable even without the decoupling capacitors.




**(a)** $\mu$ factors before stabilization.

**(b)** $\mu$ factors after stabilization.

**Figure 3.4:** $\mu$ factors plotted for the amplifier before and after stabilization.

## 3.5 Bias network

The following section will first focus on designing the bias network as a wideband short before transforming the network into a wideband open circuit.

The basic idea behind a bias network is to provide the transistor with suitable DC voltage while RF signal does not propagate into the DC sources. In other words, DC should see an impedance of $Z = 0$, while any AC signal should see an impedance of $Z = \infty$. This is for an idealized case and it is impossible to achieve for any real circuit, but good approximations with a well designed bias network is possible. Since the design proposed in this paper is a wideband design the biasing network needs to be wideband reflective. The bias network designed in this paper can be described as having three main parts. A $\lambda/4$ line, a radial stub and decoupling capacitors.

The radial stub is a stub with increasing width as length increases and can be seen in the bottom right corner of figure 3.5. This figure shows the bias network as a block diagram on the left hand side. On the right hand side the inner works of the bias network block is depicted. Nodes A and B are the same points in the bias network for both the left and right side of the figure. The idea behind using the radial stub, which has much better wideband characteristics than a fixed width stub, was to tune it to such a geometry that the network could be viewed as a short from node B in figure 3.5. In figure 3.6, a Smith chart with the reflection plotted for the bias network block shown in figure 3.5 and for the entire bias network including the resistor and the $\lambda/4$ line is presented. From the blue result, which is for the bias network block without the resistor or $\lambda/4$ line, it is clear that this network shorts out the RF signal from 1.8 GHz to 2.6 GHz. This is not a perfect short and some of the RF signal will propagate past the radial stub. To attenuate the leaking RF signal further,

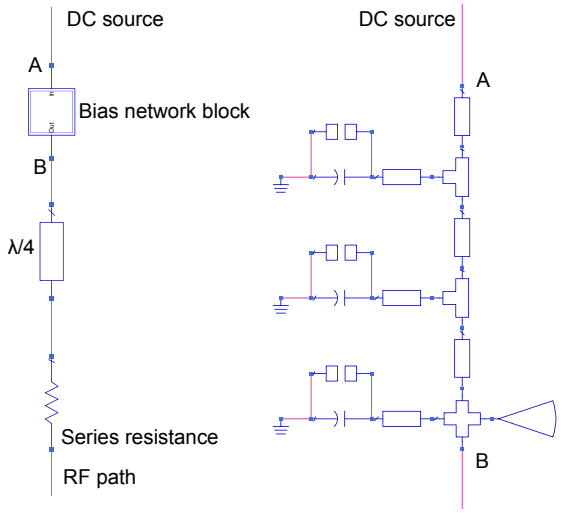



**Figure 3.5:** Bias network. On the left hand side is a block diagram of the entire bias network which is connected between the DC source and RF path. On the right hand side is the inner works of the bias network block.

three capacitors of different capacitance was connected between the DC path and ground. For the right frequency range the capacitors will act as a low impedance coupling between the DC path and ground and will effectively attenuate the RF signal. The capacitors with the lowest capacitance will be most effective at decoupling the higher frequencies and high value capacitors will decouple the lower frequencies. For this design the decoupling capacitors were chosen to be 1 pF, 1 nF and 1 $\mu$F. The value of these capacitors are not critical for the performance of the amplifier other than to help with stability. Capacitors can be added or changed for the realized amplifier if needed. It should be added that it is good practice to add the smallest capacitor closest to the RF path to minimize the total number of wavelengths travelled for the waves.

In order to transform this short circuit to an open circuit for the RF signal path a $\lambda/4$ line was added in series at the RF path node in figure 3.5. The $\lambda/4$ line is a very narrowbanded component and will be exactly $\lambda/4$ for one frequency. This line was designed to be $\lambda/4$ at 2.3 GHz. This is 100 MHz higher than the center frequency $f_0$, and the reason for this is that the transistor inherently has higher gain for lower frequencies. The $\lambda/4$ line was therefore designed slightly higher in frequency to try to negate the effects of lower gain in the upper part of the frequency band. The series gate bias resistor mentioned in section 3.4 and seen in figure 3.5 does have a physical length which will work as a transmission line. This length was taken into account when the length of the $\lambda/4$ line was determined. The simulated reflection for the entire bias network is shown in a Smith chart in figure 3.6 and colored orange. With the use of the $\lambda/4$ line the characteristics for the entire bias network have now changed to be close to an open circuit in the operational frequency band.

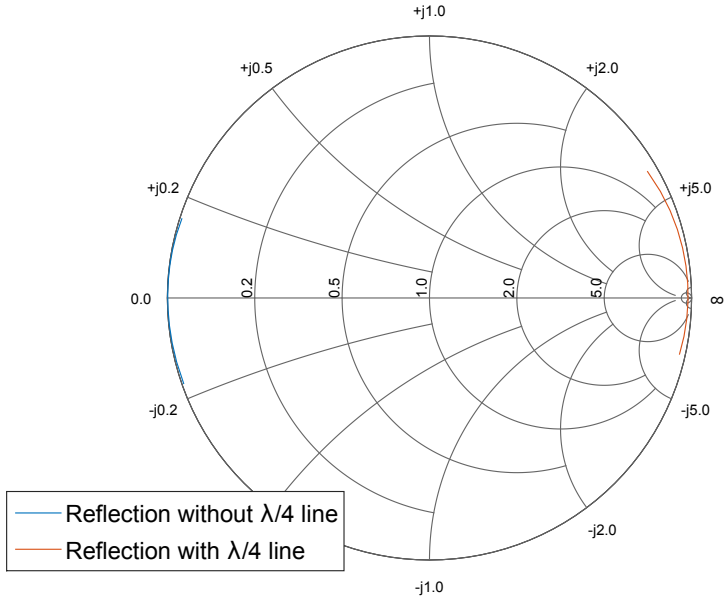



**Figure 3.6:** Reflection of the bias network. Blue colored line is the network without the $\lambda/4$ line and orange line is the network with the $\lambda/4$ line.

Simulated signal leakage and reflection for the bias network are plotted in figure 3.7. Signal leakage, seen on the right hand side of the figure, is desired to be as low as possible. The reflection from the RF path node into the RF path is desired to be as high and close to 0 dB as possible and the result is shown in the left hand side in the figure. The maximum reflection from the bias network occurs at 2.4 GHz. This is caused by the $\lambda/4$ line. This line was designed to be $\lambda/4$ at 2.3 GHz, but the length of the series resistor is not included in the simulations, resulting in a 2.4 GHz peak value. The biasing network was simulated to have an attenuation between $-30$ and $-45$ dB, and a reflection between $-0.34$ and $-0.13$ dB from $1.8 - 2.6$ GHz. These simulated results shows that the bias network is very good at reflecting over a large frequency band and is also able to suppress any RF signal which does not get reflected.

## 3.6 Load Pull and Source Pull benches

Designing a matching network for a wideband design is not a trivial task as the impedances of both the ideal matching and the matching network will change with frequency. To be able to simulate many different matching networks easily and quickly a load pull test bench made by Asc. Prof. Morten Olavsbråten was utilized. This load pull test bench can tune each impedance for $f_0$, $2f_0$ and $3f_0$ independently, making it possible to simulate all possible non-active matching networks. The reason for the limiting of the load pull bench to only include third harmonic is that the gain of the transistor becomes very low for $f > 6$

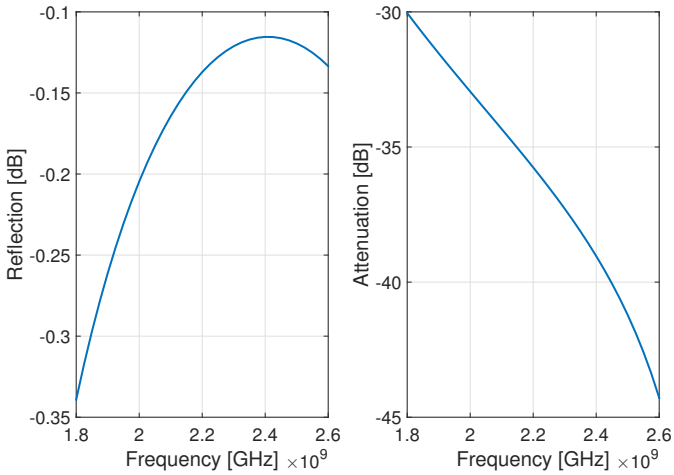



**Figure 3.7:** Both forward reflection and gain/attenuation plotted in dB for the bias network.

GHz. For frequencies higher than 1.5 GHz, which is lower than the lowest operational frequency of the amplifier, the fourth harmonic would become insignificant and add complexity to the design process. The bench interpolates between the frequencies specified and their harmonics with either cosine interpolation or linear interpolation. In this case the cosine interpolation was used. The load pull bench is designed as a component in ADS and is to be placed on the drain of the transistor without any other matching as can be seen in figure 3.8. This means that the matching the load pull bench finds will be the total impedance the transistor should be seeing after a matching network has been designed. With the use of ideal bias circuitry when finding the optimal impedances, the nonideal bias circuitry can be used as part of the matching. This will decrease the complexity of the designed matching network. The reflection for both 2nd and 3rd harmonic is limited to 0.95 to try to model the nonideal lossy behaviour of a microstrip matching network. Ideally one would want total reflection of 1, but that is impossible to achieve for a real world application.

The source pull module works in the same manner, but should be placed on the transistor gate as shown in figure 3.9. As is seen in this figure the source pull module is placed before the stabilization network. The reason for this is that the stabilization network should not be a part of the matching network and should remain unchanged after the amplifier has been made stable.

Optimal impedances should be found for the load network before the source network as the source network will be heavily dependent on the load network. The load matching is also dependent on the source network, but to a much lesser extent, and will not detune as much after the source network has been found. Because of this dependency it is favourable to optimize both load and source networks after the matches have been found.

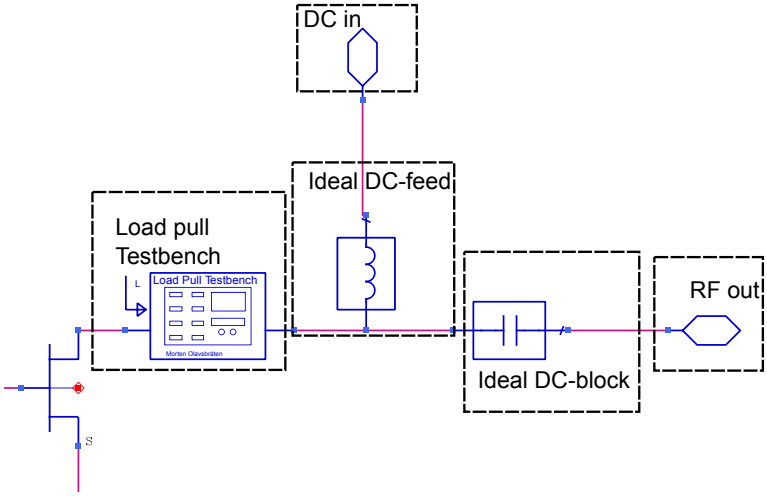



**Figure 3.8:** Method for finding the optimal load impedances.

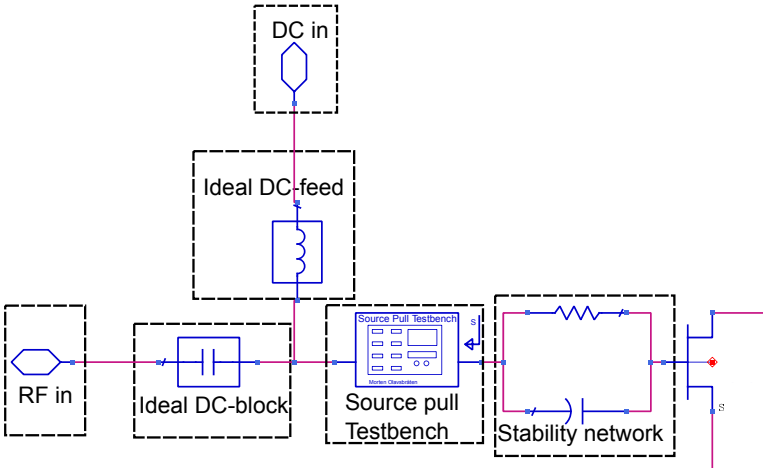



**Figure 3.9:** Method for finding the optimal source impedances. Simplified to not include the microstrip components of the stability network.

| | Source | Load | | |
|---|---|---|---|---|
| Frequency | $\Gamma_{opt}(f_0)$ | $\Gamma_{opt}(f_0)$ | $\Gamma_{opt}(2 \cdot f_0)$ | $\Gamma_{opt}(3 \cdot f_0)$ |
| 1.8 GHz | 0.63 $\angle$ -132.0 | 0.48 $\angle$ 153.1 | 0.95 $\angle$ 80.4 | 0.95 $\angle$ -40.6 |
| 1.9 GHz | 0.68 $\angle$ -121.0 | 0.49 $\angle$ 154.0 | 0.95 $\angle$ 89.2 | 0.95 $\angle$ -23.9 |
| 2.0 GHz | 0.69 $\angle$ -115.2 | 0.50 $\angle$ 155.3 | 0.95 $\angle$ 96.1 | 0.95 $\angle$ -6.4 |
| 2.1 GHz | 0.74 $\angle$ -97.7 | 0.52 $\angle$ 157.8 | 0.95 $\angle$ 107.8 | 0.95 $\angle$ 26.2 |
| 2.2 GHz | 0.74 $\angle$ -95.3 | 0.52 $\angle$ 156.1 | 0.95 $\angle$ 112.0 | 0.95 $\angle$ 27.5 |
| 2.3 GHz | 0.75 $\angle$ -87.5 | 0.53 $\angle$ 158.4 | 0.95 $\angle$ 116.4 | 0.95 $\angle$ 40.6 |
| 2.4 GHz | 0.77 $\angle$ -81.1 | 0.53 $\angle$ 160.6 | 0.95 $\angle$ 117.4 | 0.95 $\angle$ 50.8 |
| 2.5 GHz | 0.78 $\angle$ -71.6 | 0.55 $\angle$ 161.0 | 0.95 $\angle$ 125.2 | 0.95 $\angle$ 63.1 |
| 2.6 GHz | 0.79 $\angle$ -60.9 | 0.56 $\angle$ 162.6 | 0.95 $\angle$ 127.4 | 0.95 $\angle$ 75.5 |

**Table 3.2:** Simulated optimal impedances with the use of load and source pull bench.

## 3.7 Matching

Finding the optimal impedances for both source and load matching were done by using the load and source pull benches and using optimizing goals. The amplifier in this paper is designed to be a highly efficient PA and thus the goals were set to provide a power out of more than 40 dBm and as high PAE as possible. The optimal impedances found is summarized in table 3.2. To be able to match to a large frequency band the realized source and load match impedances would have to model the simulated optimal impedances. One challenge immediately arose as the impedances was turning counterclockwise in the Smith chart, seen in figure 3.10, as frequency increased. Matching to a counterclockwise impedance in the Smith chart is impossible for a passive network. This can be circumvented by using a looping topology for the matching network. This enables it to come fairly close to the ideal impedances found with the source and load pull benches at the cost of a more complex matching network. The impedances for the realized matching network is presented in figure 3.12 and 3.13 and the looping characteristics can be seen in figure 3.12 for the simulated source network.

With $\Gamma_{opt}$ mapped for both source and load a matching network could be designed. This was done by utilizing the optimizer in ADS. Goals that modelled $\Gamma_{opt}$ in table 3.2 were defined. $f_0$ for load was weighted to a greater extent than $2f_0$ and $3f_0$, since this impedance have a greater impact on the final performance of the PA. To make the matching network less complex the bias network for both drain and gate voltage was incorporated into the matching. With these goals set up in the simulator it was just a matter of trial and error of testing different topologies until a design came close to the optimal impedances.

Another challenge with realizing the matching network which needed to be addressed were that the optimal impedances for $2f_0$ and $3f_0$ were at the opposite side of the Smith chart when the frequencies are almost identical. This is seen for $2f_0$ = 5.2 GHz and $3f_0$ = 5.4 GHz. The optimal impedances for these harmonics are $0.95\angle 127.4$ and $0.95\angle -40.6$ respectively. From this it is clear that it would be an impossible task to be able to match

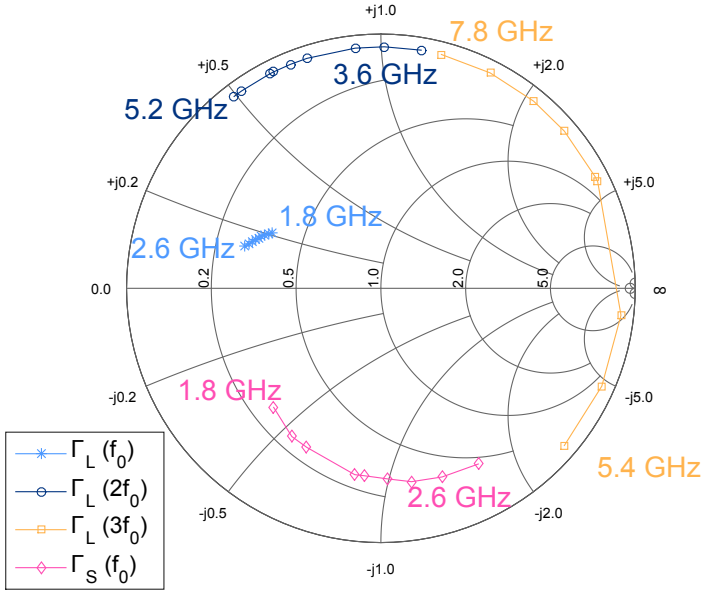



**Figure 3.10:** Optimal impedances plotted in a Smith chart for 1.8 to 2.6 GHz. All impedances move counterclockwise when frequency increases.

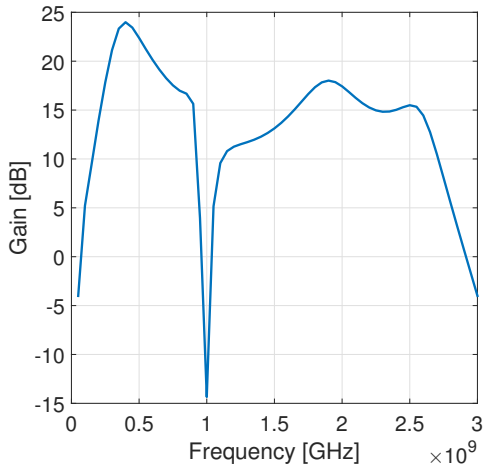



**Figure 3.11:** Small signal gain for the simulated amplifier with the modelled optimal source and load matching.

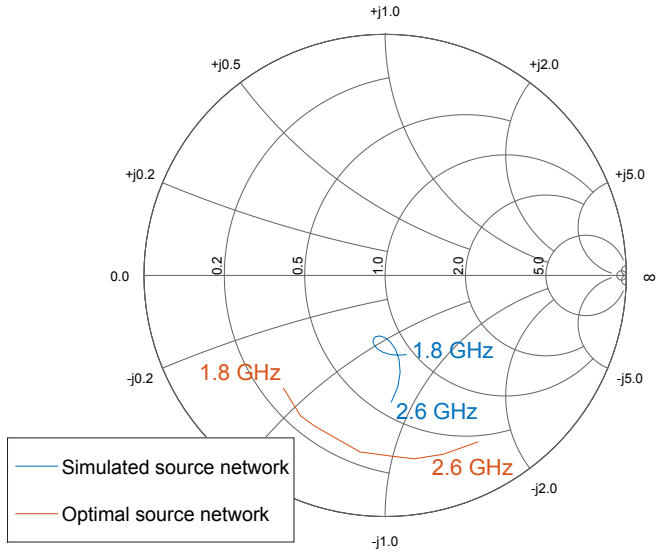



**Figure 3.12:** $\Gamma_S$ plotted for both simulated and optimal network. Blue line moves clockwise.

perfectly. Matching $2f_0$ properly is more important for the final performance than the matching of $3f_0$ and more focus and effort went into matching the second harmonic than the third.

In figure 3.12 and figure 3.13 both $\Gamma_S$ and $\Gamma_L$ for the simulated network are plotted. In the Smith chart for $\Gamma_S$ both optimal and simulated results are plotted. This is not done for $\Gamma_L$ as the Smith chart gets crowded with data and the results will be hard to read. The results must therefore be compared to that of figure 3.10. From the source matching in figure 3.12 it is clear that the matching is the closest fit at the outer extremes of the operational frequency band. The result of this is observed for the small signal gain plotted in figure 3.11 as the lowest gain in the operational band is approximately at the centre frequency. The load network shows a good match for $f_0$ and $2f_0$ compared to figure 3.10 with a very good reflection for the 2nd harmonic. However, for the 3rd harmonic the match is poor except for the lowest and highest frequencies. Matching for the 3rd harmonic was limited to be in the correct half of the Smith chart when designing the network, so that it contributes to an increase in efficiency without adding strict design goals which increase complexity.

The small signal gain of the amplifier is depicted in figure 3.11 and from this it can be seen that the 800 MHz bandwidth specification is not fulfilled. There is also a very high gain of 24 dB in the 400 MHz region. This can become very problematic when envelope tracking the amplifier as the decoupling capacitors must be removed and stability can become an issue. Steps towards reducing the gain at 400 MHz and making the 3 dB gain bandwidth wider will be presented in section 3.8.

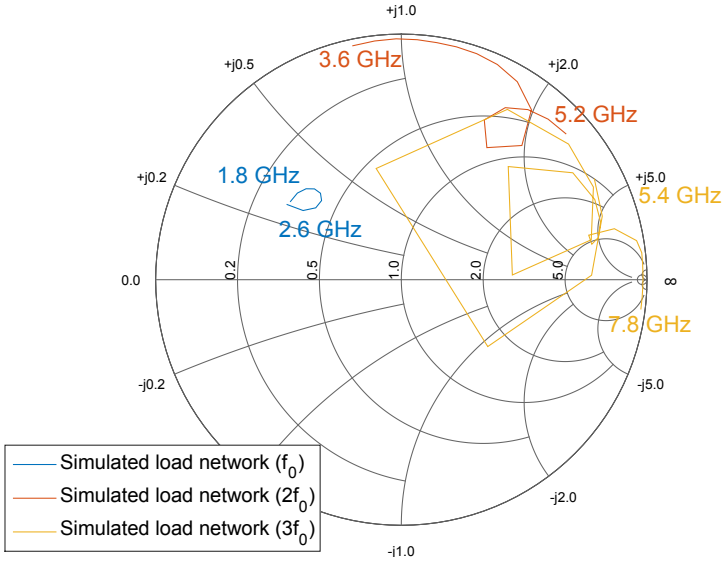



**Figure 3.13:** $\Gamma_L$ plotted for the load simulated network.

| Parameter | Goal | Frequency |
|---|---|---|
| Gain($S_{21}$) | 17 dB $\leq S_{21} \leq$ 17.5 dB | 1.8-2.6 GHz |
| $\mu$ factors | $> 1$ | 0-6 GHz |
| Input reflection($S_{11}$) | $< -10$ dB | 1.8-2.6 GHz |
| Gain($S_{21}$) | $< 10$ dB | 0-1 GHz |

**Table 3.3:** Goals used in the simulator to modify the gain of the PA.

## 3.8 Matching for larger small signal gain bandwidth

From subsection 2.4 in the theory it is clear that source matching is the major contributor to gain characteristics. To design for a larger small signal bandwidth, the same topology as found in section 3.7 was used, but some optimization goals were set in ADS to flatten the gain characteristics. The goals are summarized in table 3.3. With the help of the simulator a new match was found to give 17 dB small signal gain with a fluctuation of approximately 0.5 dB from maximum to minimum in the operational frequency band. The previous 24 dB gain peak at 400 MHz was reduced to 15 dB with the new matching network, which will help with stability. The new simulated small signal gain can be seen in figure 3.14 where it is compared to the one found with the optimal impedances. The specification for the input reflection $S_{11}$ was not fulfilled in the simulated design, but a possible solution for this will be presented in section 5.1. The Smith chart presented in figure 3.12 for the source matching network are no longer valid, but are used to show an important part of the process of designing a wideband match. By first modelling the optimal impedances found and later modifying the network to comply with specification a good wideband design can

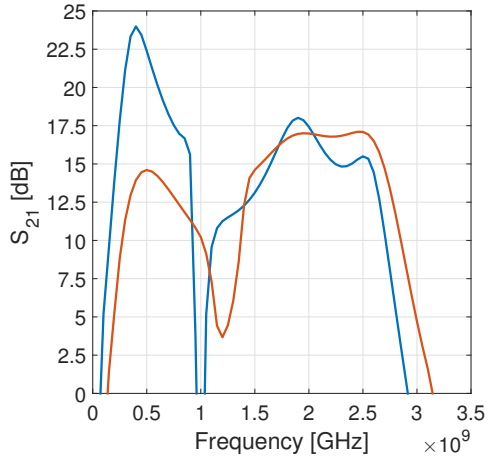



**Figure 3.14:** Small signal gain for the simulated amplifier. Blue line is the gain with simulated optimal source impedance. Orange line is the modified source network for wider 3 dB gain bandwidth.

be achieved. It is important to note that the load match will be slightly detuned by the change done on the source matching network even if the load matching network remains unchanged. This was however not found to change the simulated output power or PAE in any significant way.

Chapter 4

# Results

In this chapter the results of the measured amplifier, referred to as device under test (DUT), will be presented alongside simulated results. The results will only be briefly commented as they will be further discussed in chapter 5.

## 4.1 Method for measurements

The small signal, large signal and tracking measurements were done with different equipment setups. Both methods and the equipment used will be described in the following section.

### 4.1.1 Small signal measurement method

| Model | Manufacturer | Description |
|---|---|---|
| VNA, E8364B | Agilent Tech. | Vector analyzer for multiport measurements |
| Calibration kit, 85052D | HP Agilent | SOLT, DC to 26.5 GHz |
| Coupler, 5292 | Narda | Broadband coupler, 1-18 GHz, $-13$ dB |
| EL302Tv | TTI | Power supply |
| 374BNM | Narda | 20 W load termination, DC-18 GHz |

**Table 4.1:** Equipment used for the small signal measurements.

In order to measure the gain and reflection of the DUT a vector network analyser (VNA) was used. The test signal is sent to the input of the DUT and the DUT's output is connected to a receiver and analyzed before the results are shown on a display. The S-parameters, as mentioned in section 2.1, will describe the reflection on both input and output of the DUT as well as forward and reverse gain. Before any measurements can be obtained the VNA must be calibrated. A standardized SOLT calibration kit, which is described in section

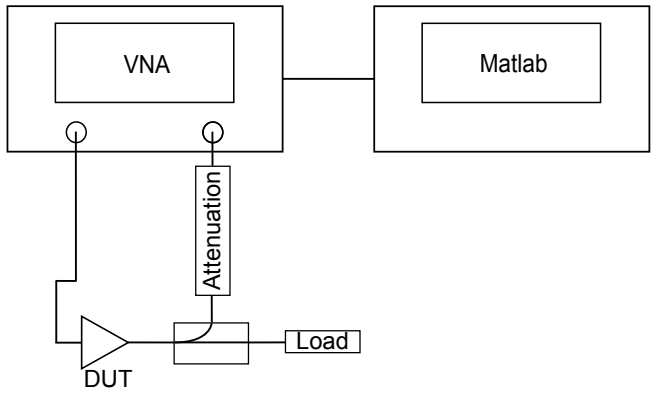



**Figure 4.1:** Small signal test bench setup.

2.12, was used in the calibration process. Attenuation on the output of the DUT was employed in order to protect the VNA from possible damage in case of DUT oscillation. This attenuator can be mathematically removed in the calibration process so that the results from the VNA are valid without any additional calculations. This is done by performing the calibration with the attenuator connected to the VNA. Attenuating the output of the DUT will however not be without problems. As mentioned in section 2.11.2, the measurements for $S_{12}$ and $S_{22}$ will not be accurate since the attenuator will bring the signal closer to the internal noise floor of the instrument. These measurements are therefore omitted in this thesis.

The attenuator used on the output of the DUT consists mostly of low power devices. The DUT has been designed to be capable of delivering in excess of 10 W and will damage the attenuator devices which are rated for a maximum of 2 W. Thus, a directional coupler was connected directly to the output of the amplifier. A directional coupler is a device that couples the incident power on its input over to a port by a set amount. This can be useful to provide another circuit or measuring equipment with a lower powered sample. The rest of the uncoupled signal propagates through the coupler. For this application the through port of the coupler was terminated with a 50 $\Omega$ termination, which is the characteristic impedance of the measuring equipment. The load termination will dissipate most of the power delivered from the amplifier. The coupler used while measuring has a coupling factor of $-13$ dB, which means that $5\%$ of the DUT's output power will propagate to the attenuator, while $95\%$ propagates to the load termination. The amplifier was then connected and biased correctly according to the $I_{drain}$ = 163 mA requirement found in section 3.2. The S-parameters were measured after some time to allow the transistor to heat up and reach steady state. Averaging with the use of 16 measurements were used in order to minimize the small fluctuations in results caused by noise. A schematic describing the test bench is depicted in figure 4.1. Equipment used and characteristics for the coupler and attenuation is summarized in table 4.1

| Model | Manufacturer | Description |
|---|---|---|
| FSQ 40 | Rohde & Schwarz | Signal analyzer |
| SMU 200A | Rohde & Schwarz | Vector Signal Generator |
| CS-144-35 | MCLI | Circulator |
| Coupler, 5292 | Narda | Broadband coupler, 1-18 GHz, $-13$ dB |
| AIM & TTI | CPX 200DP | Dual 180 W DC power supply |
| 374BNM | Narda | 20 W load termination, DC-18 GHz |
| Sucoflex cable 100 | Huber+Suhner | Signal cables for RF |

**Table 4.2:** Equipment used for the large signal test bench.

### 4.1.2 Large signal method

To be able to measure the output power and efficiency of the amplifier a large signal test bench was used. In figure 4.2 the general layout of the setup is shown and the equipment used is summarized in table 4.2. The setup has several similarities to the small signal bench described in section 4.1.1 with a few exceptions. There is now the need to measure the power consumption of the DUT. This is done by logging the current and voltage supplied by the power supply to the DUT. The use of a driver amplifier and a circulator is now a new addition to the test bench and needs explaining.

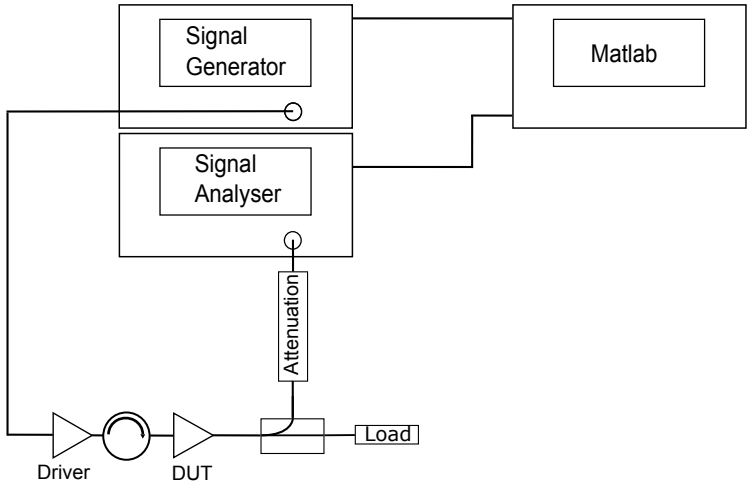



**Figure 4.2:** Large signal test bench setup.

One problem with using the SMU 200A from Rohde & Schwarz is the output power level of the signal generator as it is lacking in terms of driving the DUT into compression. To solve this a driver amplifier was introduced between the signal generator and the power amplifier. The driver amplifier is a wideband amplifier biased in class-A region to intro-

duce minimal distortion to the signal. It is based around the same 10 W transistor that the DUT is based on and offers enough gain to drive the DUT into compression.

The circulator is a passive non-reciprocal component in which RF signal entering a port will be able to propagate only to the next port. In this case it is used as an RF isolator. This is done by connecting port 1 to the driver PA, port 2 to the DUT and port 3 to a matched load. This means that the RF signal from the driver PA will propagate to the DUT where some will be reflected. Without the use of the circulator the reflected RF signal can detune the output matching of the driver amplifier and be troublesome. All the reflected RF power from the DUT will propagate to the matched load where it will be transformed into heat.

To correctly measure PAE and output power, the driver PA and attenuation for the DUT has to be characterized. Attenuation is measured with the small signal bench described in 4.1.1 as the attenuation will be the same for both small and large signals. The driver PA is characterized by measuring the output power from the circulator so that the measured output power from the circulator can be directly used as the input power on the DUT. The driver PA needs to be characterized for the same frequencies and power levels that is used to measure the DUT.

### 4.1.3 Tracking method

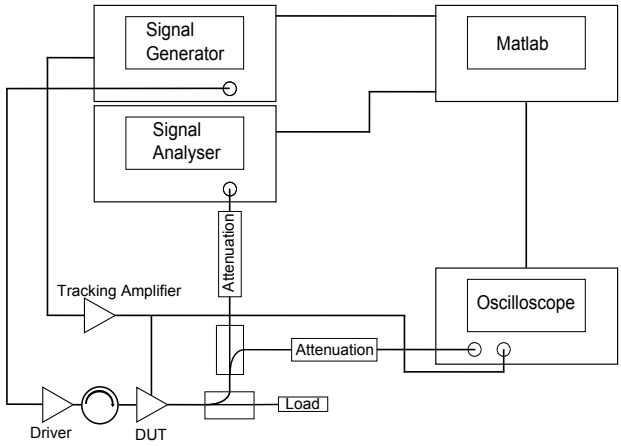



**Figure 4.3:** Tracking test bench.

The Rohde & Schwarz FSQ-40 signal generator has two built in buffers which are connected to two separate outputs. The first buffer is in this case connected to the front RF output of the signal generator while the second buffer is connected to two separate I/Q data outputs. The data uploaded to the first buffer will consist of the I/Q data for the RF test signal which will be sent to the input of the driver amplifier. The second buffer will consist of the tracking function for the drain voltage of the DUT. The tracking function is

calculated from the RF test signal with the use of

$$|E| = \sqrt{I_{RF}^2 + Q_{RF}^2}, \tag{4.1}$$

for the ET scheme and

$$P = |E|^2 = I_{RF}^2 + Q_{RF}^2, \tag{4.2}$$

for the power tracking scheme where $I_{RF}$ and $Q_{RF}$ are the I and Q data of the RF signal. Matlab was used for the calculation and uploading of the functions. The calculation is carried out before any data is uploaded to the signal generator and enables the tracking of randomly generated RF signals. The envelope data uploaded to the second buffer consists of a single floating point vector which governs the voltage on the Q data output. The signal generator does have some limitations as to what it is able to output on the I/Q data outputs. The RMS voltage of the two outputs combined cannot exceed 1 V, which effectively means that the maximum voltage that should be used by one channel is $\frac{1}{\sqrt{2}} \approx 0.7$ V. The limit of 0.7 V is not strictly necessary when only one channel is being used, but it is considered good practice to eliminate possible problems if the second channel is not set to 0 at all times. This means that the signal generator alone will not be able to deliver the necessary voltage, let alone current, required for the drain tracking. To overcome this issue a tracking amplifier made by Asc. Prof. Morten Olavsbråten was used. This tracking amplifier is a power amplifier capable of supplying voltages in the range of approximately 0 to 30 V and deliver around 1 A at full power. It is based on a two stage amplifier design where the first stage acts as a preamplifier to amplify the signal to usable levels for the second stage. The first stage consists of an operational amplifier, namely the LT1363, while the second stage is based around the LT1210 power operational amplifier, both from Linear Technology. The bandwidth of the tracking amplifier is limited to approximately 5 MHz, which will inhibit the trackers ability to track envelopes in the low MHz region as only a few harmonics will be included in the output frequency spectrum. The problems which arise from this limitation will be further explored in section 5.2.2. The tracking amplifier offers adjustable gain and it must be manually adjusted with the use of an oscilloscope to get the correct peak to peak voltage for the tracking scheme.

Measuring correct drain current for the tracker cannot be done with the usual procedure of reading the average current drawn from the lab power supply. The tracking amplifier itself will dissipate power and the current drawn from the lab power supply is no longer the drain current of the DUT. A low value resistor of 0.21 Ω is placed in series with the output of the tracking amplifier. The voltage drop can then be measured across this resistor with an oscilloscope and will be proportional to the drain current that the tracking amplifier is supplying. By measuring the voltage on the output of the tracking amplifier at the same time the instantaneous power delivered to the PA can be calculated by:

$$P_{inst} = V_{track}(t) I_{track}(t). \tag{4.3}$$

The drain voltage will now be a low frequency AC signal and the the highest value drain bias network decoupling capacitors must be removed. The capacitors will form a low

| Model | Manufacturer | Description |
|---|---|---|
| FSQ 40 | Rohde & Schwarz | Signal analyser |
| SMU 200A | Rohde & Schwarz | Vector Signal Generator |
| CS-144-35 | MCLI | Circulator |
| Coupler, 5292 | Narda | Broadband coupler, 1-18 GHz, $-13$ dB |
| MSO9254A Infiniium | Agilent | Oscilloscope |
| AIM & TTI | CPX 200DP | Dual 180 W DC power supply |
| 374BNM | Narda | 20 W load termination, DC-18 GHz |
| Sucoflex cable 100 | Huber+Suhner | Signal cables for RF |

**Table 4.3:** Equipment used for the tracking test bench.

impedance path to ground for the drain bias voltage which has to be avoided. The smallest capacitor in the drain bias network was kept intact as it will only decouple for high frequencies. Removal of the decoupling capacitors can potentially make the amplifier unstable. The tracking amplifier will provide good decoupling capabilities below 100 MHz and the DUT will ensure stability for frequencies higher than 1.8 GHz. In the frequency band between there is a possibility of oscillation, but this will not be known for certain before testing the DUT with the tracking amplifier. Focus towards increasing the stability in the 500 MHz range was made when stabilizing the DUT. This can be seen in figure 3.4b where the $\mu$-factors are at their maximum for 500 MHz. This was done to increase the chances of a stable amplifier when the decoupling capacitors in the drain bias network were desoldered.

A critical factor for the performance of drain tracking is correct timing for drain modulation. A mismatch in timing will impair both linearity and efficiency. The signal generator has the option to synchronize the two output buffers so both signals will start simultaneously, which was used when doing the measurements. However the delay paths trough the driver PA into the DUT is not the same as the delay through the tracking amplifier. This was solved effectively with Matlab by using a vector shift function that shifts the vector in a circular fashion, effectively delaying the drain function with an accuracy of one sample. To determine the best fitting amount of sample delays, the Agilent MSO9254A infiniium oscilloscope was connected to the output of the PA through a coupler and to the output of the tracking amplifier. Because of the low frequency of the tracking signal of 1 MHz the length of the cables can be ignored. With the trial and error method the correct amount of delay samples were found and is seen when both the RF envelope and tracking function synchronizes on the oscilloscope screen.

In section 2.10 a figure showing the idealized tracking function was presented. A more realistic model is presented here, and it represents the tracking functions actually used in this thesis. The envelope tracking function tracks the RF envelope from 8 V to 28 V. A lower bias than 8 V was not found to give any significant increase in PAE. The power tracking scheme was tracked between 15 V and 28 V. The offset which can be seen in the

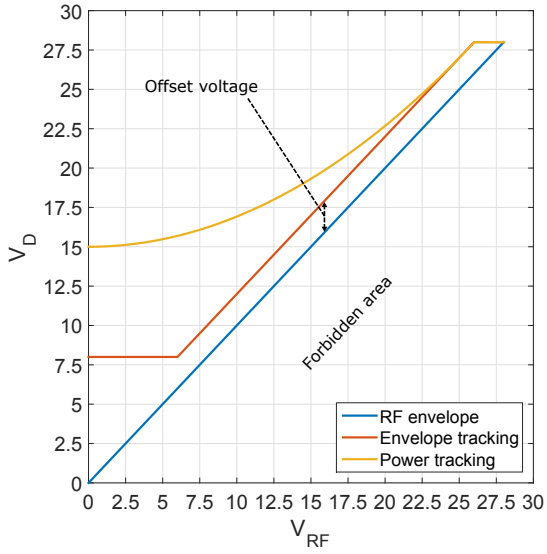



**Figure 4.4:** Approximations of the actual tracking functions for both ET and power tracking.

figure is not necessarily correct in relation to the offset used while obtaining the results in this thesis, but it shows an important property of the tracking schemes. A larger voltage offset will result in higher linearity, less efficiency and more gain. Tracking closer to the RF envelop will result in higher efficiency at the cost of added nonlinearities.

A root-raised-cosine (RRC) filter was used when measuring 16-QAM to avoid intersymbol interference (ISI). This is a frequently used filter in digital communication and is used as the send and receive filter. By using one RRC filter on both the send and receive sides the full response is that of a raised-cosine (RC) filter. The RC filter satisfies the Nyquist ISI criterion and will result in minimized ISI. The theory of RC and RRC filters fall outside the scope of this thesis, but more information can be found elsewhere [15].

## 4.2 Preliminary adaptive drain bias simulations

Envelope tracking and power tracking was not implemented in the simulator as it is more interesting to look at a realized tracking scheme. Focus therefore went into implementing the tracking schemes on realized hardware. However, simulations with static adaptive bias were carried out as this will serve as a pointer as to what to expect from the tracking schemes.

In figure 4.5 a plot showing the simulated PAE versus output power for different voltage supply levels is depicted. The drain supply voltage has been swept from 8 V to 28 V with a 2 V step. By decreasing the supply voltage for the lower output levels, efficiency can be drastically improved for a large dynamic output power range. At 30 dBm output power

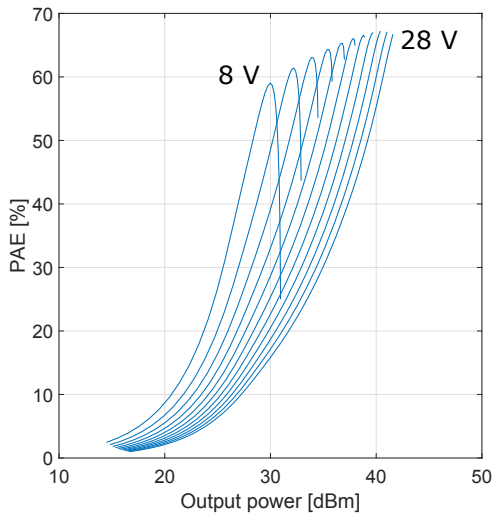



**Figure 4.5:** Simulated PAE at 1.8 GHz for the amplifier with swept supply voltage.

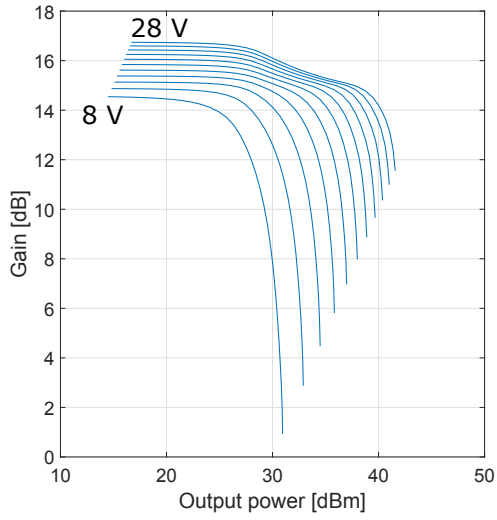



**Figure 4.6:** Both power out and PAE of the amplifier for a small set of frequencies given a one tone signal.

the PAE for the 28 V drain bias simulation is about 15 %. By lowering the drain voltage to 8 V a PAE of nearly 60 % is achieved.

Figure 4.6 depicts the power gain of the simulated DUT at 1.8 GHz. Here it is seen that the gain of the device will be dependent on the supply voltage. Gain compression will occur for lower output power levels for lower supply voltages.

## 4.3 Small signal measurements

With the use of the test bench described in 4.1.1 the small signal response of the PA was measured. In table 4.4 the small signal requirements are stated.

| | |
|---|---|
| Bandwidth (3 dB) | 800 MHz |
| Gain | $>$ 12 dB within the bandwidth |
| Input match ($S_{11}$) | $<$ -10 dB within the bandwidth |

**Table 4.4:** Small signal specification for the PA.

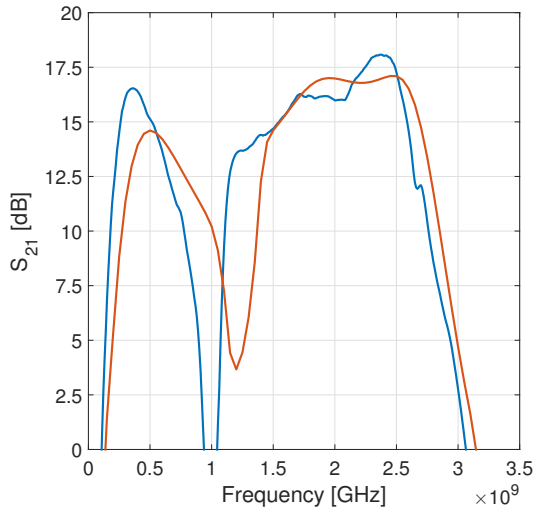



**Figure 4.7:** The measured $S_{21}$ is coloured blue. The simulated is coloured orange.

12 dB small signal gain is maintained from 1.1 GHz to 2.65 GHz with a peak of 18.2 dB at 2.35 GHz. The 3 dB bandwidth of the amplifier was measured to be 1.05 GHz from 1.55 GHz to 2.6 GHz, while the simulated 3 dB small signal bandwidth was 1.3 GHz from 1.45 GHz to 2.75 GHz. Maximum small signal gain for the simulated amplifier is achieved at 2.45 GHz with a value of 17.1 dB. In figure 4.7 the measured and simulated results are plotted. The figure shows that the gain characteristic of the simulated and

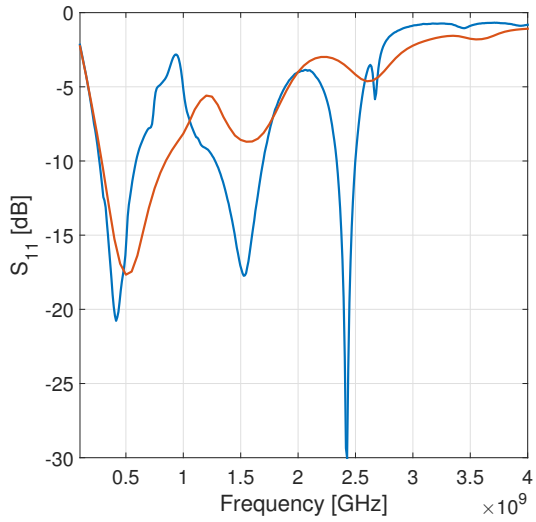



**Figure 4.8:** The measured $S_{11}$ is coloured blue. The simulated is coloured orange.

realized amplifier is well correlated except for some skewing in the frequency domain and an increase in gain at 2.1 GHz which was not present in the simulations. The simulated small signal gain shows a flat characteristic from 1.8 GHz to 2.6 GHz with fluctuations of approximately 0.5 dB from the minimum to the maximum value.

Results for the simulated and measured $S_{11}$ are depicted in figure 4.8. The measured $S_{11}$ has a global minimum at 2.4 GHz with a value of -30 dB. However with a positive or negative change of 100 MHz, $S_{11}$ changes to a value which does not fulfil specifications. The required value of $S_{11}$ from the specifications are not fulfilled for one operational frequency in the simulations, but this was a conscious design choice. A possible solution to this will be presented in section 5.1.

## 4.4 Large signal measurements

The test bench described in section 4.1.2 was used to obtain the large signal measurements. In figure 4.9 the maximum output power versus frequency is plotted. The amplifier delivers more than 10 watts, or 40 dBm, from approximately 1.50 GHz to 2.65 GHz. The output power peak is at 1.8 GHz where the amplifier delivers 41.8 dBm. These measurements were acquired with the use of one tone measurements. The one tone testbench consists of a single sine signal, which is not representative of a real world application, but offers a way to measure output power and efficiency without the intermodulation and memory effects of multi-carrier signals. Maximum PAE is plotted in figure 4.10 where a maximum value of $74\%$ is found from 1.8 GHz to 1.9 GHz and the amplifier displays good efficiency from 1.6 GHz to 2.6 GHz. The results presented so far indicates good performance for 1.6-2.6 GHz and as a result measurements will be taken for 1.8 GHz, 2.2 GHz and 2.6 GHz. These

frequencies represent the lowest frequency, the centre frequency and the highest frequency in the specified operational bandwidth of the DUT.

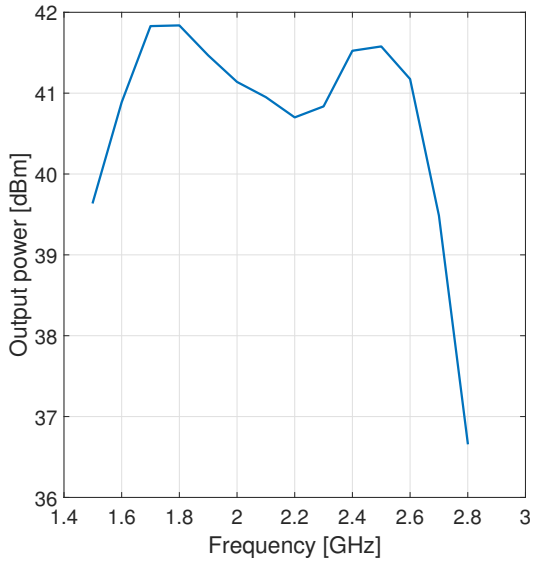



**Figure 4.9:** Maximum power out vs. frequency measured for one tone.

In figure 4.11a, the output power vs. input power is plotted for 1.8 GHz to 2.6 GHz with a step of 400 MHz. From this select few frequencies it is seen that the amplifier is capable of delivering 40 dBm without entering heavy compression. The PAE have been plotted in figure 4.11b for the same frequencies as the power output plot. Note that there have been a measuring error in the PAE measurement for 2.6 GHz and the PAE is inflated by approximately 10 percentage points.

In table 4.5 both simulated and measured output power and PAE is listed with a frequency step of 100 MHz. Note that the gain is the power gain and is measured at maximum output power and hence in heavy compression.

In figure 4.12a the measured power gain is plotted versus the output power. The amplifier can be seen delivering 40 dBm output power before entering heavy compression. Figure 4.12b shows the results for the simulated power gain. The simulated 1.8 GHz and 2.2 GHz results are well correlated with the measured gain. However, 2.6 GHz shows large differences in the simulated and measured gain.

Another interesting aspect of the large signal bench is to try to measure the memory effects associated with temperature changes. This can be done by performing a two tone test while sweeping the tone spacing and measuring the third order IMD. From section 2.7 it is known that asymmetrical sidebands indicate memory effects and by sweeping the tone spacing the RF envelope will change frequency. The frequency of the RF envelope for a

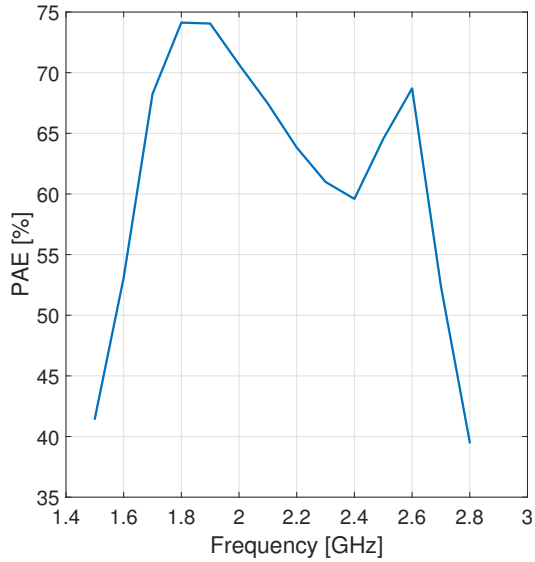
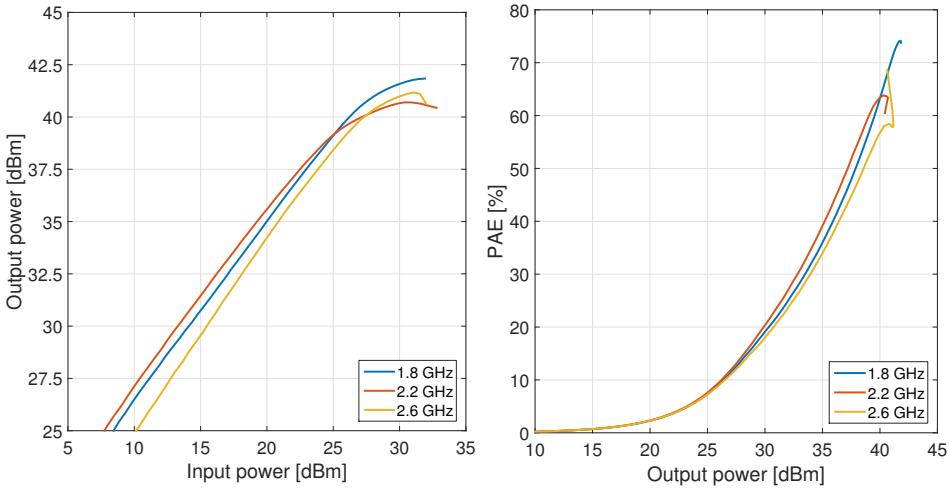



**Figure 4.10:** Maximum PAE vs. frequency measured for one tone.

| Frequency | $\eta_{pae}[\%]$ | $\eta_{pae}[\%]$* | $P_{out}[dBm]$ | $P_{out}[dBm]$* | $Gain[dB]$ | $Gain[dB]$* |
|---|---|---|---|---|---|---|
| 1.5 GHz | 41.5 | 50.8 | 39.7 | 40.9 | 10.7 | 10.9 |
| 1.6 GHz | 53.1 | 52.7 | 40.9 | 41.2 | 10.9 | 10.2 |
| 1.7 GHz | 68.2 | 58.6 | 41.8 | 41.6 | 11.4 | 11.6 |
| 1.8 GHz | 74.1 | 66.7 | 41.8 | 41.6 | 9.9 | 11.6 |
| 1.9 GHz | 74.1 | 68.6 | 41.5 | 41 | 10 | 11 |
| 2.0 GHz | 70.7 | 70.8 | 41.1 | 40.6 | 9 | 10.6 |
| 2.1 GHz | 67.5 | 69.6 | 41.0 | 40.3 | 9.3 | 10.3 |
| 2.2 GHz | 63.8 | 70.2 | 40.7 | 40.3 | 10.3 | 10.3 |
| 2.3 GHz | 61.0 | 65.2 | 40.8 | 40.2 | 11.1 | 10.2 |
| 2.4 GHz | 59.6 | 65.9 | 41.5 | 40.4 | 11.3 | 10.4 |
| 2.5 GHz | 64.5 | 64.3 | 41.6 | 40.6 | 12.6 | 10.6 |
| 2.6 GHz | 68.7 | 63.1 | 41.2 | 40.2 | 9.2 | 10.2 |
| 2.7 GHz | 52.4 | 58.1 | 39.5 | 39.3 | 8.8 | 9.3 |

**Table 4.5:** Summarized table for both simulated and measured large signal results. The gain measure is power gain. * denotes simulated results.

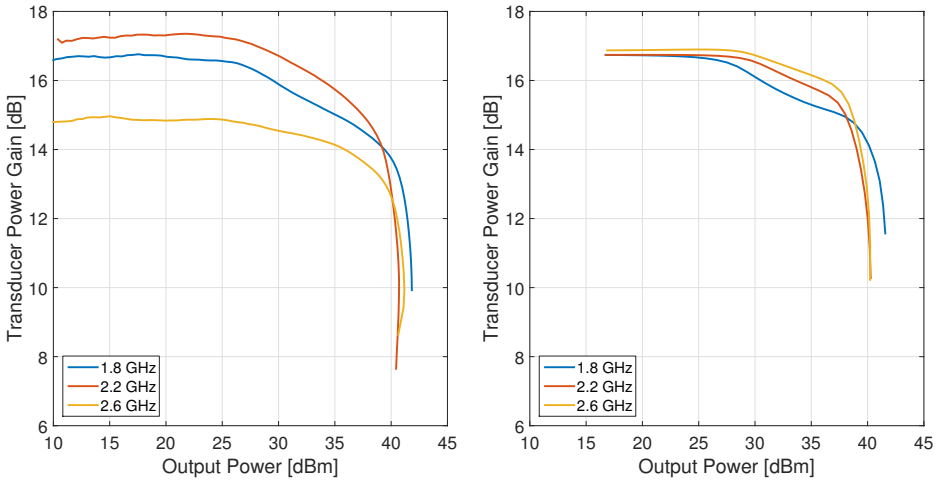
two tone signal will be equal to the tone spacing, $f_{envelope} = f_{spacing}$. The idea is that for low tone spacing the transistor will have time to heat up and cool down for a full period of the RF envelope. In figure 4.13a and 4.13b, tone spacing have been swept and both lower and higher third order IMD have been plotted with 28 V and 22 V drain bias. The results have been obtained at the 1 dB compression point for both drain bias voltages. The first tone spacing on both figures is 50 kHz. For both 28 V and 22 V results there are approximately 1.5 dB difference in high and low third order IMD for the 50 kHz measurement. When the tone spacing frequency increases, the difference in IMD decreases to become




**(a)** Power out vs. power in.

**(b)** PAE vs power in.

**Figure 4.11:** Both power out and PAE of the amplifier for a small set of frequencies given a one tone signal.

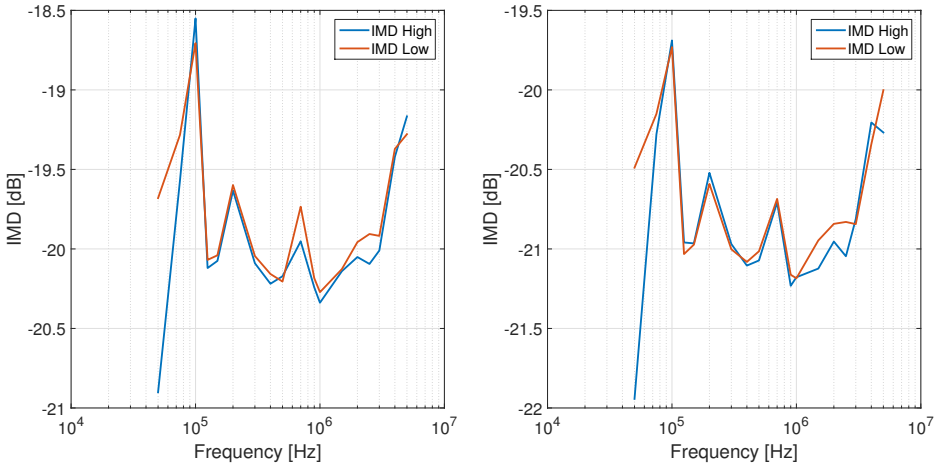



**(a)** Measured power gain.

**(b)** Simulated power gain.

**Figure 4.12:** Measured and simulated power gain.

insignificant. This indicates that there are memory effects that are temperature dependent. The results from both 28 V and 22 V drain bias shows that the amplifier's third order IMD is not dependent on drain voltage. The small difference in these two measurements can be credited to the amplifier being driven further into compression for one supply voltage than the other.




**(a)** Frequency sweep for 28 V drain bias.

**(b)** Frequency sweep for 22 V drain bias.

**Figure 4.13:** IMD versus tone spacing frequency for 28 V and 22 V drain voltage.

## 4.5 Tracking results

In table 4.5 the results for two tone tracking are listed for 1.8 GHz, 2.2 GHz and 2.6 GHz. The output power level is chosen to be at 1 dB compression for all non tracking two tone results. For correct comparison of efficiency between no tracking and tracking schemes the amplifier must deliver the same average output power in both cases.

| Frequency | Output Power | Simulated | No tracking | ET | Power tracking |
|---|---|---|---|---|---|
| 1.8 GHz | 37.9 dBm | 46 % | 53 % | 63 % | 60 % |
| 2.2 GHz | 37.4 dBm | 53 % | 52 % | 59 % | 59 % |
| 2.6 GHz | 37.4 dBm | 49 % | 47 % | 53 % | 51 % |

**Table 4.6:** PAE measurements for different tracking schemes given the same output power. Simulated results are obtained with a static drain bias of 28 V.

In table 4.7 the corresponding results for the simulated and measured IMD products are summarized.

| Frequency | Output Power | Simulated | No tracking | ET | Power tracking |
|---|---|---|---|---|---|
| 1.8 GHz | 37.9 dBm | -23.9, -23.9 | -21.0, -21.0 | -28.0, -24.0 | -38.3, -26.9 |
| 2.2 GHz | 37.4 dBm | -19.2, -19.1 | -16.8, -16.9 | -28.2, -36.9 | -32.0, -32.8 |
| 2.6 GHz | 37.4 dBm | -19.8, -19.8 | -18.5, -18.5 | -28.0, -27.8 | -36.9, -31.0 |

**Table 4.7:** Measured and simulated IMD for the DUT. Results are presented in the format of: low frequency IMD, high frequency IMD. All values are measured in dBc.

The tracking results shows a moderate increase in efficiency for all frequencies and both tracking schemes. The IMD results indicate memory effects that are caused by the intended modulation of the supply voltage as the IMD sidebands are asymmetrical. An interesting result is that the IMD products are much lower for the tracked amplifier compared to the baseline static supply voltage amplifier.

### 4.5.1 16-QAM tracking results

The following results were carried out at the very end of the master thesis and are only to be viewed as additional measurements that emphasize the previous tracking results.

QAM, or Quadrature amplitude modulation, is a modulation scheme that is common in digital and analog communication today. Hence the following results can be viewed as more realistic compared to the more synthetic one and two tone tests. The 16-QAM scheme has 16 distinct symbols which each carries 4 bits of information. The data signal in 16-QAM is made from two carrier signals which is $90^{\circ}$ out of phase, also known as in quadrature. By changing the amplitude of these two carrier signals one can change both phase and amplitude of the data signal and obtain 4 bits of information.

The results in table 4.8 were obtained with a symbol rate of 1 Msymbol/s (1 MBd), which results in a signal envelope of 1 MHz. A test vector of 10 000 randomly generated symbols were measured to ensure that accurate average data was produced.

| Frequency | Output Power | PAE | $\Delta_{PAE}$ | $\text{ACPR}_\text{L}$ | $\text{ACPR}_\text{H}$ |
|---|---|---|---|---|---|
| 1.8 GHz - No Tracking | 35.1 dBm | 37.3 % | 0 % | -41.2 dBc | -39.9 dBc |
| 1.8 GHz - Envelope Tracking | 34.1 dBm | 53.2 % | 15.9 % | -29.1 dBc | -26.7 dBc |
| 1.8 GHz - Power Tracking | 34.8 dBm | 47.8 % | 10.7 % | -29.8 dBc | -28.2 dBc |
| 2.2 GHz - No Tracking | 30.7 dBm | 22.4 % | 0 % | -41.3 dBc | -39.9 dBc |
| 2.2 GHz - Envelope Tracking | 31.2 dBm | 38.7 % | 16.3 % | -28.2 dBc | -26.2 dBc |
| 2.2 GHz - Power Tracking | 30.9 dBm | 32.1 % | 9.7 % | -29.7 dBc | -27.9 dBc |
| 2.6 GHz - No Tracking | 33.2 dBm | 29.7 % | 0 % | -42.1 dBc | -39.8 dBc |
| 2.6 GHz - Envelope Tracking | 33.2 dBm | 44.6 % | 14.9 % | -35.0 dBc | -32.8 dBc |
| 2.6 GHz - Power Tracking | 33.2 dBm | 38.9 % | 9.2 % | -38.2 dBc | -35.9 dBc |

**Table 4.8:** PAE measurements for 16-QAM.

Chapter 5

# Discussion

In this chapter both design, simulations and measurements of the power amplifier will be discussed. A possible solution to the design problem of meeting $S_{11}$ specification is presented, and challenges regarding measurements are discussed.

## 5.1 Design

The amplifier was designed in a module based process where the stabilization network, bias network and matching network were designed separately. This process allowed for validation of the amplifier components during the design with the use of ADS and provides an effective method to design an amplifier. The amplifier presented in this thesis is the second version of a wideband amplifier which was designed in a preliminary project. The amplifier designed in this thesis exhibits larger bandwidth, higher efficiency and more output power compared to the first version. Experience gained by designing the first wideband PA provided invaluable when designing a second version.

The specification for $S_{11}$ was not fulfilled in the design process. One possible solution for this is to add attenuation to the input of the amplifier. The signal entering the PA will then be attenuated for the forward transmission before being attenuated a second time for the reflected wave. Figure 5.1 shows the solution given an attenuator of 3 dB, PA gain of 10 dB, a PA $S_{11}$ of -4 dB and an input signal of 30 dBm. This method will introduce a reduction of the reflection from the PA, at the cost of gain and efficiency. The 3 dB attenuator will reduce the system $S_{11}$ with a total of 6 dB, and the system gain with 3 dB. The gain can be increased with the use of a second PA in series with the first PA. This will add cost to the total system, reduce efficiency and increase complexity. The addition of an attenuator can be a valid method of decreasing the reflection of a PA, but it must be subject to careful consideration of the trade off between gain, efficiency, cost and $S_{11}$.

Whether this design can be classified as class-F or class-F$^{-1}$ is somewhat uncertain. To be able to classify an amplifier as either of those classes, knowledge about the intrinsic

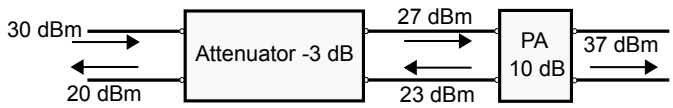



**Figure 5.1:** Possible solution to the $S_{11}$ specification.

waveforms of the current and voltage on the drain node is needed. With an internal model of the transistor, without package and wire bonding, it would be possible to determine which of the amplifier classes were achieved. Cree shares this model with only a few hand picked universities and NTNU is not one of them. However, it is safe to assume that one of these operations were achieved, as both high wideband output power and efficiency were simulated and measured. To circumvent these definitions this amplifier can be said to have achieved a harmonically tuned topology.

## 5.2 Results

### 5.2.1 Simulations

The first simulations which were carried out were ideal. Ideal in the sense that ideal transmission lines without loss, ideal DC-feed and ideal DC-block were used. The ideal DC-feed and DC-block functions, respectively, as a short and an open circuit at DC voltage levels. At AC these blocks will function as an open circuit and a short circuit respectively. This means that the bias network will introduce no loss or unwanted characteristics. This was used only to find the optimal impedances for source and load matching in table 3.2. By using ideal components in the bias network the non ideal bias network could be used as a part of the matching, which will reduce complexity of the design. For a perfectly ideal simulated design typical performance numbers are well above 80 percent PAE and 43 dBm output power. These results are not included in this thesis as they are not representative of a real world amplifier. The simulated results which are included is based on lossy, nonideal design and are more comparative in terms of performance with the realized amplifier. Microstrip transmission lines with loss and capacitor models including parasitic circuit elements were used. The bias network described in section 3.5 was used in the non-ideal simulations of the final design, and thus the results in the simulations will be more representable of a realized amplifier.

In the load pull bench made by Asc. Prof. Morten Olavsbråten, the reflection of 2nd and 3rd harmonics were chosen to be 0.95 instead of 1. For simulation purposes a full reflection of 1 would have given better results, but this will yield unrealistic performance in the simulations and thus this value was slightly reduced. When simulating the matching network a reflection coefficient of 0.95 is obtainable. This is seen in figure 3.13, where the 2nd harmonic displays good reflective properties. However, for the 3rd harmonic it is difficult to make a matching network which shows good reflective properties. This was not found, with the help of the load pull bench, to cause major loss in performance and the 3rd harmonic was limited to operate within the correct half of the Smith chart according

to optimal impedances. When the 3rd harmonic operates in the correct half of the Smith chart it will work to increase the efficiency of the amplifier.

The simulated results of the amplifier are summarized for the large signal test in table 4.5 and presented in section 4.3 for small signal results. From this it can be seen that the simulated amplifier will have very good large signal performance over a large frequency band from 1.8 GHz to 2.6 GHz. Maintaining 40 dBm output power and more than 60% PAE in the entire frequency band. The small signal gain can be seen in figure 4.7 as the red curve and depicts flat gain characteristics from 1.8 GHz to 2.6 GHz with only a 0.5 dB fluctuation from minimum value to maximum value. The PA shows a 3 dB bandwidth of 1.35 GHz from 1.4 GHz to 2.75 GHz and a gain higher than 10 dB from 1.35 GHz to 2.85 GHz. The 3 dB bandwidth of 1.35 GHz is 61% of the centre frequency of 2.2 GHz. This is an impressive result for this transistor. From these results it is clear that a wideband design had been successfully designed in a simulator environment. The measured results are expected to differ from the simulated as a simulator cannot possibly take all effects into account. The simulated design fulfilled all specifications except the specification for $S_{11}$, for which a possible solution have been presented in chapter 5.1.

The center frequency of the simulated design can be determined by looking at the peak gain at 2.5 GHz. The gain here is simulated to be 17.2 dB. By finding the upper and lower 3 dB cutoff frequency one can obtain the center frequency. This results in a center frequency of 2.1 GHz and a of bandwidth 1.3 GHz as the 3 dB high and low cutoff frequency was simulated to be 2.75 GHz and 1.45 GHz. However, one can argue for a different definition of the center frequency since the gain is almost flat and well above the specification. If one defines the center frequency as 2.2 GHz the 3 dB bandwidth becomes 1.35 GHz, from 1.4 GHz to 2.75 GHz. In any of the two definition cases above the center frequency is not a problem as the amplifier exhibits excellent performance in the specified frequency band of 1.8 GHz to 2.6 GHz.

There is however a possible problem with the gain characteristic. $S_{21}$ was simulated to be approximately 14.8 dB in the 500 MHz range. This gain was simulated to be close to 25 dB when a source matching network was designed with the optimal impedances. This was reduced with the use of the optimizer in ADS, but steps should be made to further reduce this gain. It can be troublesome and interfere with systems communicating in this frequency band. This can be solved without a PA redesign with a high pass filter prior to the PA in the signal chain or optionally just after the PA. This is however not an optimal solution as the filter will attenuate the signal to some extent, reducing the efficiency.

### 5.2.2 Measurements

There will always be some deviation of measured performance and real performance. These deviations stems from the equipment used to measure will never be able to measure perfectly, but with the use of sound calibration practices high accuracy can be obtained. The results in this thesis are believed to be representable of the real performance.

Small signal measurement results are given in section 4.3. The gain matches fairly well with the simulated result, except for some skewing in the frequency domain and a gain increase from 2.1 GHz to the upper parts of the operational frequency which was not present for the simulated design. The difference in the measured and simulated gain is believed to come from incomplete models for the microstrip transmission lines, manufacturing differences between each unit of the transistor, manufacturing differences in the FR4 substrate, tolerance of the passive circuit components, parasitics introduced while soldering and parasitic circuit elements for the capacitors and resistors. All the passive circuit components comply to the E12 series standard, which means a tolerance of $\pm 10\%$. Since the stabilizing network consists of a high pass filter, an error in the capacitor or resistor value will affect the cutoff frequency. While the capacitor models used in the simulator have included parasitics the resistors are based on an ideal model. The real resistors will include a inductive component, capacitance between the pads, and capacitance between the pads and the ground plane. A model for the resistors could be developed by measuring the S-parameters, but this is believed to not significantly improve the accuracy of the simulator. The inaccuracy of the simulations is more likely caused by the difference in each manufactured unit of the FR4 substrate and the transistor.

The peak gain was measured to be 18.2 dB, which is high for this transistor and approximately 1 dB higher than the simulated gain. It is also seen that the measured $S_{11}$ shows a better characteristic in the operational frequency band compared to the simulated results, but the specification for $S_{11}$ is still not fulfilled. With the method previously presented in section 5.1, an attenuator of 3 dB will be enough to reduce the reflection to the specified level. The peak of $S_{11}$ was measured to be -4 dB and a 6 dB reduction will place it under the -10 dB limit, but as mentioned previously it will come at a cost of less gain and efficiency. There is a large gain spike down in the 400 MHz region which was also present in the simulations. If this PA was to be commercialized the gain spike would have to be reduced as this can lead to interference between communication systems.

It is difficult to say something specific about the individual parts of the measured amplifier, like the bias network or stability network, since it is not possible to measure individual modules without destroying the PCB. But as far as the bias and stabilizing network goes it seems to be doing what it was designed to do. No oscillations occurred during measurements, even without the drain decoupling capacitors which had to be removed while performing drain tracking. This can be a result of the added focus to increase the stability in the 500 MHz region during the design phase.

The results for large signal one tone measurements are summarized in table 4.5. The amplifier provides 40 dBm from approximately 1.5 GHz to 2.65 GHz for a bandwidth of 1.15 GHz. From the simulated results an output power of 40.9 dBm was expected at 1.5 GHz, but was measured to be 39.7 dBm. The reason for this is the PA will no longer be driven into compression, as can be seen in figure 5.2, and maximum output power is not reached. This is caused by a combination of the driver PA not supplying enough power at this frequency and too much loss through the circulator. The circulator between the driver PA and the PA in this paper has a bandwidth from 2 GHz to 6 GHz. With a circulator

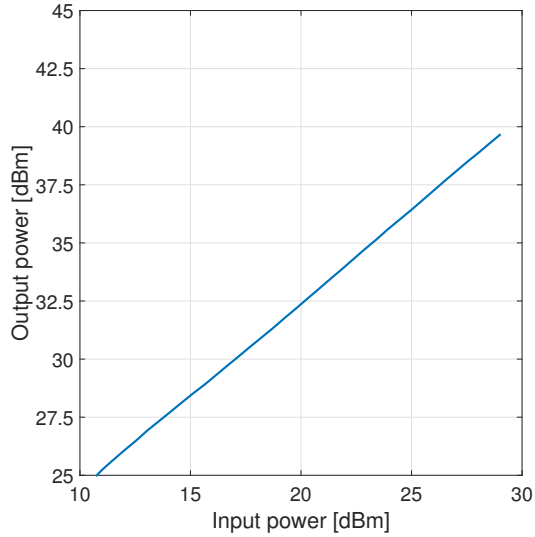



**Figure 5.2:** Measured output power for 1.5 GHz. The amplifier displays little to no gain compression.

which can operate at a lower frequency the output power for 1.5 GHz will be above 40 dBm. It would be interesting to measure the minimum frequency the amplifier can supply 40 dBm at, as the measured gain is high down to about 1.1 GHz. The measured PAE of the PA shows similar characteristics to the output power. Maximum PAE, shown in figure 4.10, is achieved at 1.8 GHz with a value of 74.1%. The measured efficiency remains high for the amplifier from 1.7 GHz to 2.6 GHz, just dipping below 60% for 2.4 GHz. At 2.6 GHz the amplifier exhibits strange behaviour for the largest input signals, and the output power and PAE in figure 4.11 can be seen breaking down. The maximum power output is measured correctly, but the PAE is artificially high at 68.7%. The correct PAE for this frequency is 58%. This behaviour of the breakdown in output power is most likely caused by the amplifier self biasing the gate voltage because of the diode connection in the transistor breaking down. The breakdown will result in heavy distortion on the output and must be avoided. One possibility is to limit the input power of the PA at this frequency to a safe non-breakdown level, effectively eliminating the possibility of a transistor breakdown.

The results measured for the one tone large signal test with the combination of small signal measurements shows a very good wideband performance. This goes to show that the matching network which is described in section 3.7 offers a good wideband match for the realized amplifier. One interesting aspect is the output power for the realized amplifier compared to the simulated amplifier. The output power is consistently higher for the realized amplifier from 1.8 GHz to 2.6 GHz. The cause of this might be that the transistor model is modelled after a minimum power that the transistor is guaranteed to deliver. A PA is one of the most expensive components of a radio system and it is therefore critical to be sure of the output power capabilities of the PA before production.

The PA was measured with the use of a two tone test to establish a baseline for the tracking results. The two tone test was carried out from 1.8 GHz to 2.6 GHz with a step off 400 MHz. Measurements were taken at 1 dB compression and showed promising PAE results without drain tracking of 53%, 52% and 47% from the lowest to highest frequency. With the same output power and frequency as the baseline the PAE increased to 63%, 59% and 53% for the envelope tracked scheme. An approximation for the system efficiency can be expressed as:

$$\eta_{tot} \approx \eta_{EnvAmp} \cdot \eta_{RF}, \tag{5.1}$$

where $\eta_{EnvAmp}$ is the tracking amplifier efficiency and $\eta_{RF}$ is the RF amplifier efficiency. Using this formula, a minimum efficiency for the tracking amplifier can be established. A PAE for the tracking amplifier of 84%, 88% and 89% will put the envelope tracked amplifier system on par with the baseline results. This is ignoring any other circuitry like control circuits or linearization techniques. There are amplifiers on the market that reach in excess of 90% efficiency and therefore it seems that ET is a viable option for increasing efficiency.

One challenge with the ET scheme is the infinite bandwidth requirement of the tracking amplifier. With the use of a power tracking scheme the tracking amplifier's bandwidth requirement gets reduced to that of the RF envelope frequency. This will make the tracking amplifier design less complex at the cost of less PAE increase compared to the ET scheme. The tracking amplifier must reach a PAE of 88%, 88% and 92% in order to be on par with the no tracking scheme. The power tracking scheme will not be as dependent on linearization compared to ET as the PA will experience less compression. With less digital signal processing (DSP) for linearization compared to ET and less complex tracking amplifier design, the power tracking scheme might come out on top in a system which employs tracking, depending on the intended use of the system.

The 3rd order IMD is summarized in table 4.7 where an interesting phenomena can be observed. With the use of the tracking schemes the absolute value of the 3rd order IMD is significantly reduced. The cause for this is unknown. Memory effects which are indicated by the asymmetrical IM sidebands are however very much present in the tracked schemes. For the power tracking scheme at 1.8 GHz there is a difference of 11.4 dB which indicate significant distortion introduced by memory effects. This cause for this might be a slight timing issue with regard to the drain voltage and the RF envelope. However, the drain function is believed to be optimally synchronized with the equipment used so this is not certainly the cause. This was not further pursued as linearity was not a focus of this thesis, but rather achieving high efficiency.
For a more realistic approach to the tracking results, 16-QAM was measured. A baseline was established for the 16-QAM by setting the output power to such a level that ACPR was measured to be -40 dBc for the fixed drain voltage amplifier. The same output power must be delivered for the drain tracked amplifier in order to directly compare performance figures. The baseline 16-QAM measurements yielded a PAE of $37.3\%$, $22.4\%$ and $29.7\%$ for 1.8 GHz, 2.2 GHz and 2.6 GHz respectively. The envelope tracking scheme resulted in a PAE of $53.2\%$, $38.7\%$ and $44.6\%$. This is a relative PAE increase between $42\%$ to $72\%$ for the envelope tracking scheme and is a significant increase in efficiency. The power

tracking scheme shows a predictably lower PAE compared to the envelope tracking. A PAE of $47.8\%$, $32.1\%$ and $38.9\%$ was measured. This results in a relative PAE increase of $28\%$, $43\%$ and $31\%$ for the power tracking scheme. An issue regarding the 1.8 GHz and 2.2 GHz measurements was that the output power of the amplifier was not the same for each scheme. Because of this the different schemes cannot be directly compared to each other at these frequencies. Nevertheless the results show great improvement going from no tracking to ET and power tracking. Envelope tracking and power tracking was expected to display a higher increase in efficiency for 16-QAM compared to the two tone test as the PAPR level is higher for 16-QAM. The requirement for the tracking amplifier efficiency becomes 70%, 59%, 67% for the ET scheme and 78%, 70% and 76% for the power tracking scheme. The efficiency requirements for the tracking amplifier has been heavily reduced from that of the two tone requirements, which further goes to support that tracking the drain voltage of the amplifier is a viable efficiency enhancement technique.

From the 16-QAM ACPR measurements in table 4.8 it is clear that the linearity suffers significantly from the tracking schemes. ACPR increases by up to 13 dB for the tracking schemes compared to the fixed bias amplifier. This was expected from the static adaptive bias results in figure 4.6 where the gain is lower for lower drain bias voltages. The answer to correcting the linearity issues associated with modulating the drain voltage is as always DSP. The digital capabilities of today's technology are extremely vast and well developed for the use in RFPA, and accurate predistortion techniques can be assumed to be applied with relative ease [1].

An interesting aspect from these measurements is that the $\text{ACPR}_\text{H}$ is always higher then the $\text{ACPR}_\text{L}$. This is most likely caused by memory effects in the PA. The asymmetry in the IM sidebands was not present for the two tone fixed bias measurements. The memory effects observed in the 16-QAM no tracking results can be caused by unintended modulation of the bias voltage [1], however this is not certain to be the cause of the asymmetric ACPR. In the case of both the tracking schemes the asymmetrical ACPR was also observed. The probable cause of this is the intentional modulation of the drain bias voltage, which will introduce memory effects as mentioned in section 2.7.

There are two issues with conducting the tracking measurements which should be addressed. The first is an issue concerning the signal generator. The output buffers run in a loop and restarts when the end of the buffer is reached. In this restarting phase the output is set to 0 for a short amount of time, but can be seen on the oscilloscope and as a decrease in output power of approximately 1 dB on the signal analyzer. If the measurement is conducted at the end of the buffer the measurement will not be accurate. This can however be avoided by taking several measurements and paying close attention to the oscilloscope while measurements are taken. The second issue is regarding the tracking amplifier and its limited bandwidth of 5 MHz. This is adequate for the power tracking scheme as the bandwidth of the tracking function is 1 MHz. With the ET scheme however the bandwidth requirement is infinite. The limited bandwidth of 5 harmonics will cause the envelope to be tracked fairly well. However, the envelope of the RF will take the shape of a half-wave sine, seen in figure 5.3, which the tracker cannot follow for the lowest envelope values.

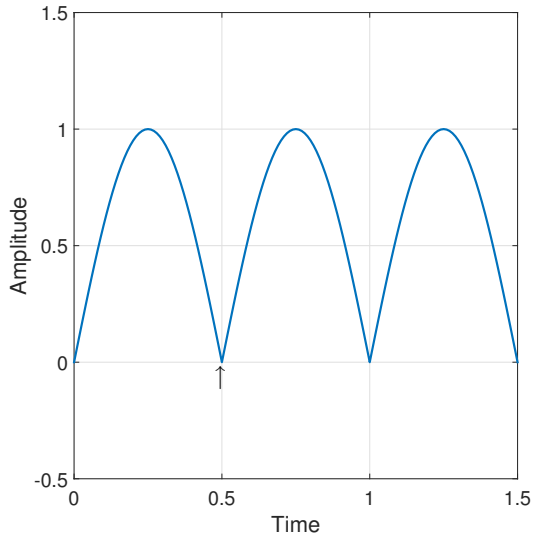



**Figure 5.3:** Ideal RF envelope for a two tone signal. The arrow denotes the problem area which makes envelope tracking require infinite bandwidth for perfect tracking.

The arrow in the figure points to the part of the RF envelope which require infinite bandwidth. This will result in the tracker voltage getting a rounder, more sine-like characteristic in this part of the envelope, instead of the sharp triangular characteristic. This will in turn result in the tracking amplifier not being able to track down to the lowest levels of the envelope. This will cause lower efficiency of the amplifier as there will be unnecessary power dissipation where the tracking function is distorted.

Chapter 6

# Conclusion

In this thesis, a wideband harmonically tuned power amplifier has been designed to have 40 dBm output power over a 800 MHz bandwidth. The amplifier was designed for a centre frequency of 2.2 GHz and as high efficiency as possible. The design was created and simulated with the use of the CAD program ADS supplied by Keysight. A wideband matching network was designed with the help of the load pull technique. This technique provided optimal load impedances which were observed to move in an anti-clockwise direction in the Smith chart. To solve this the matching network was made with a looping topology to be able to at come close to the ideal impedances. As can be seen from the results in table 6.1 this is considered a success.

| Parameter | Specification | Realized amplifier |
|---|---|---|
| Center Frequency ($f_0$) | 2.2 GHz | 2.075 GHz |
| Bandwidth (3 dB) | 800 MHz | 1.05 GHz |
| Output Power ($P_{out}$), within the bandwidth | $>$ 40 dBm | $>$ 40.8 dBm* |
| Gain, within the bandwidth | $>$ 12 dB | $>$ 15.3 dB* |
| Input match ($S_{11}$), within the bandwidth | $<$ -10 dB | $<$ -4 dB* |
| Efficiency, as high as possible | | 66%* |

**Table 6.1:** Specifications for the PA and measured realized PA. The efficiency number is based on PAE and is the average peak PAE within the bandwidth. The center frequency is calculated from the highest gain in the specified bandwidth. * denotes the results given the frequency band 1.8 GHz to 2.6 GHz.

The amplifier achieved a small signal maximum gain of 18.2 dB with 12 dB gain achieved continuously from 1.15 GHz to 2.65 GHz. The 3 dB small signal bandwidth was measured to be 1.05 GHz from 1.55 GHz to 2.6 GHz. From 1.8 GHz to 2.6 GHz the amplifier delivered in excess of 40 dBm with a maximum of 41.8 dBm. Throughout this frequency band the PAE fluctuated between 58% and 74% with a peak average of 66%. This is on

par with the simulated results which sports an average of 67%. The specification for $S_{11}$ was not met, however a possible solution to this is presented in section 5.1.

An important part of this thesis was to measure the efficiency impact the modulation of the drain voltage had on the amplifier. This was performed for two tone tests as well as 16-QAM measurements. Both power tracking and envelope tracking was performed and the strengths and weaknesses of both schemes have been explored. The two tone test results are summarized in table 4.6. With these results the tracking amplifier must reach a PAE of approximately $85\%$ for the envelope tracking scheme to be on par with the fixed bias voltage amplifier. The tracking amplifier must be even more efficient for the power tracking scheme at around $90\%$ to be on par with the fixed bias amplifier. However, for more complex modulation systems there are a higher possible efficiency increase from dynamically adjusting the drain bias voltage.

The 16-QAM measurements is summarized in table 4.8 where a large increase in PAE was obtained for the tracking schemes. Unfortunately there is no such thing as a free lunch in the world of engineering and this comes with a trade off for the linearity. The ACPR grew in excess of 10 dB and additional circuit complexity in the form of linearization techniques must be implemented to reduce the ACPR. With the more complex 16-QAM modulation the efficiency requirement for the tracking amplifier was reduced to approximately $65\%$ for the envelope tracking scheme and approximately $75\%$ for the power tracking scheme. This goes to further emphasize that supply modulation is a valid efficiency increasing technique.

Envelope tracking is an effective technique to increasing the efficiency of a PA, but comes with some challenges. The infinite bandwidth requirement of the tracking amplifier and the linearity issues spring to mind. By tracking the power of the RF signal instead of the RF envelope these issues gets partly solved. The bandwidth requirement gets reduced to that of the RF envelope. This is a big advantage over the envelope tracking scheme as the tracking amplifier design becomes less complicated. The linearity measure of a power tracked amplifier is slightly better compared to the envelope tracked amplifier. Thus the power tracked amplifier will require less linearization. The envelope tracked amplifier will offer better efficiency, but power tracking can be considered a strong contender with the trade off between efficiency, linearity, and tracking amplifier complexity. Both envelope tracking and power tracking opens a very interesting path of increasing the efficient operation of a RFPA. However, the field of power tracking a RFPA has not been extensively researched and must be said to be the more interesting scheme of the two as the decrease in efficiency compared to envelope tracking is relatively small.

## 6.1 Further Work

There are several interesting paths which can be taken for the further development of the PA. One possible path is to combine the amplifier in this thesis with digital predistortion to linearize the amplifier and get increased efficiency without the cost of increased distortion. Another linearization technique is to track the gate voltage of the transistor for constant

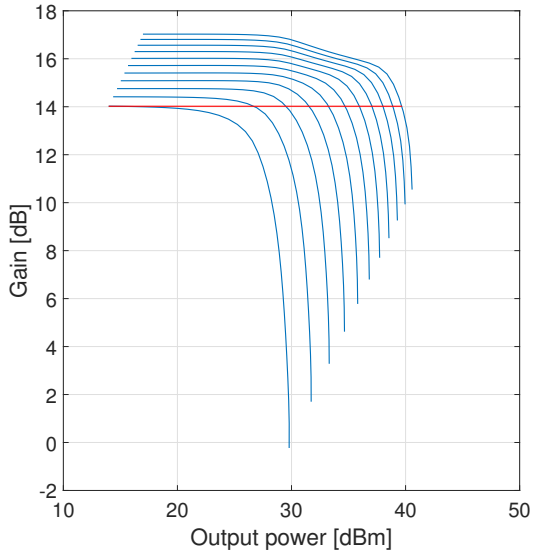



**Figure 6.1:** Simulated power gain swept for supply voltages of 8 to 28 V with a 2 V step. The lowest gain corresponds to a supply voltage of 8 V. The red line is the tracking function for constant gain of 14 dB.

gain. This, with the combination of drain tracking and predistortion would make for a very interesting further development of the PA in this thesis. A different approach to the envelope tracking scheme is the auxiliary envelope tracking (AET) technique. AET works to increase the linearity of the amplifier by superimposing a small amplitude voltage to the fixed DC supply voltage when compression of the output occur. A large improvement in third-order has been observed using this technique [16]. Another completely different take on the drain tracking scheme is to track for constant gain. The idea behind this method can be explained by figure 6.1. In this figure the red line is at a constant gain of 14 dB. By allowing the supply voltage to track this line given the output power a constant gain would be achieved, reducing the distortion of the amplifier, while still increasing the PAE of the amplifier.

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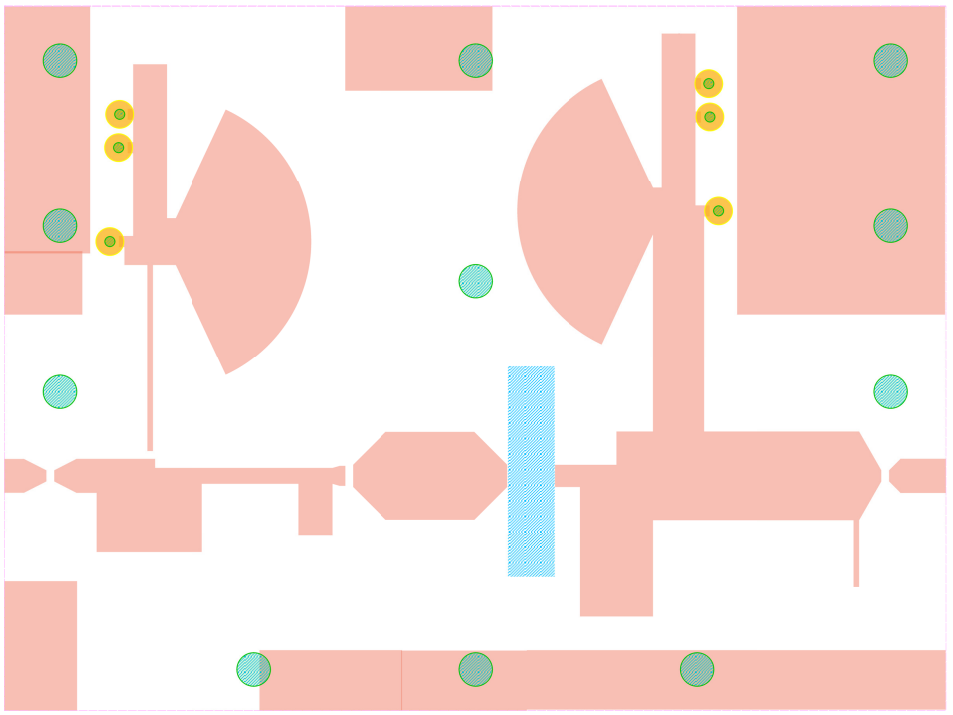
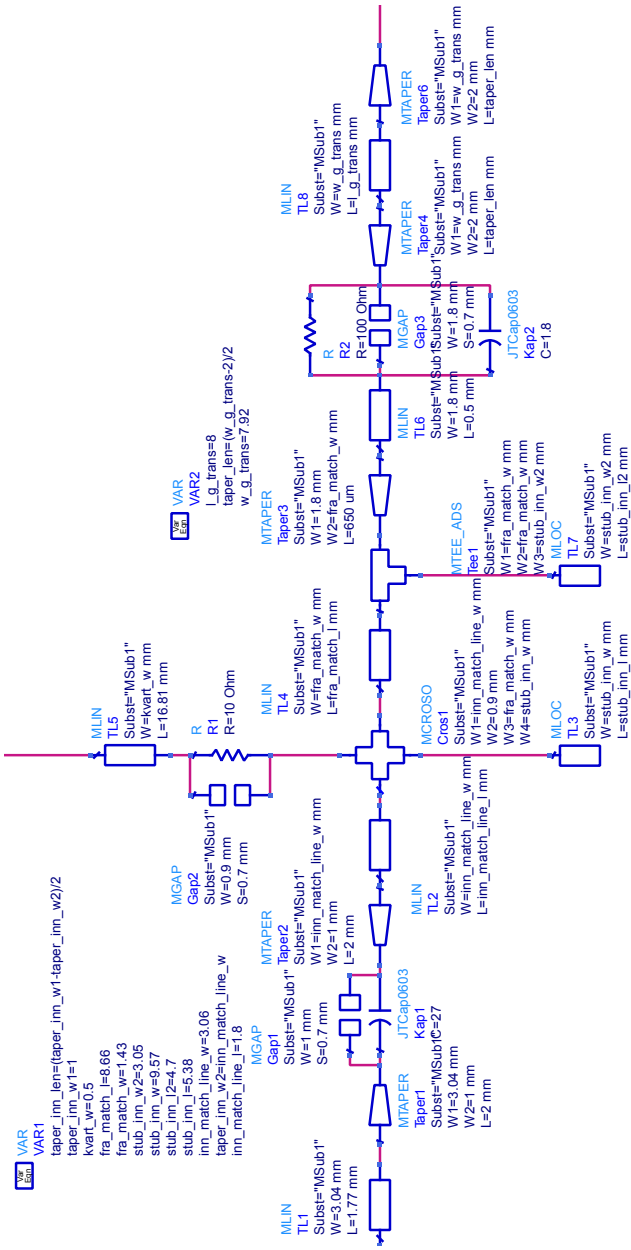
# Appendix

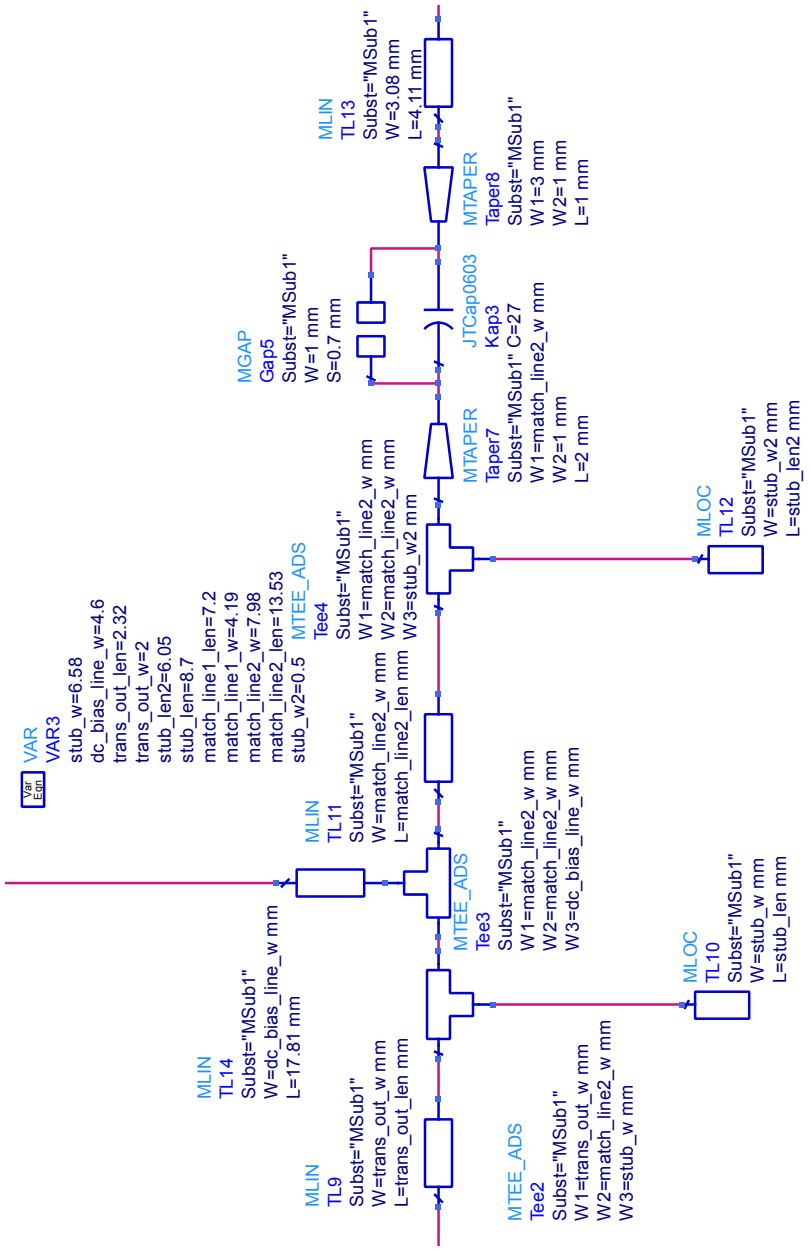
# Appendix A - Layout of the PA



# Appendix B - Schematic of the source matching network



# Appendix C - Schematic of the load matching network



# Appendix D - Schematic of the bias network