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A Fully Differential Front End Charge Sampling Amplifier for Medical Ultrasound Imaging in 28nm FD-SOI Technology

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Problem Description

Downscaling of CMOS technology provides opportunities for energy efficient electronic circuits consuming small areas. However the scaled down technology entails challenges in designing analog circuits. New analog circuits must be designed to maintain high performance in scaled down technologies with low supply voltages. The main goal of this thesis is to design a front-end LNA in 28nm FD-SOI CMOS technology for a IVUS system. The amplifier should sample and amplify the signal from a capacitive micromachined ultrasound transducer adding minimum noise and distortion. The thesis should include:

- A fully differential topology.
- Sampling at 64MHz.
- Schematic and layout design in 28nm FD-SOI CMOS technology.
- Verification of performance.
- Comparison with existing attempts.

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Supervisor: Trond Ytterdal, IET
Co-supervisor: Carsten Wulff, IET

Summary

New generations of ultrasound imaging will contain thousands of receive and transmit elements in a single probe. This leads to challenges in analog front-end circuits concerning low power, low noise, low area consumption and high linearity.

This thesis presents the design and analysis of a fully differential charge sampling amplifier, CSA, in 28nm FD-SOI CMOS technology with a capacitive micromachined ultrasonic transducer, CMUT, model as source. The proposed CSA is intended as a front-end readout LNA for IVUS systems interfaced with an ADC for high accuracy digital conversion.

The readout of the CMUT is done by connecting the two CMUT terminals to the positive and negative input nodes of the proposed CSA, reading the current from both terminals and giving a differential input signal to the CSA. This way second harmonic destortion is improved.

A capacitive parasitic extraction is done and results from simulation of the layout with parasitic extraction are presented as final results.

The proposed CSA achieves a bandwidth of 7.9MHz around a center frequency of 5MHz with a gain at centerfrequency of 14.34dB with a CMUT as source and a sampling frequency of 64MHz. High linearity of HD_2=-83dB, a relatively low power consumption of 110.6μW, an input impedance of 3.1$k\Omega$ and a noise figure, NF, of 5.79dB was achieved with an area consumption of 39.8$\times$70.3μm^2.

Sammendrag

Nye generasjoner av ultralyd avbildnings utstyr vil inneholde tusenvis av mottakere og sender komponenter inne i en ultralyd probe. Dette fører med seg utfordringer i analoge kretser vedrørende lav effekt, lav støy, lavt areal forbruk og høy linearitet.

Denne oppgaven presenterer designet av en fullt differensial ladning samplings forsterker, CSA, i 28nm FD-SOI CMOS teknologi med en kapasitiv mikromaskinert ultrasonic transduser, CMUT. Den foreslåtte CSA er tenkt som en front-end utlesnings lav-støy forsterker for et IVUS system tilkoblet en ADC for høy nøyaktighets digital konvertering.

Utlesningen fra CMUTen blir gjort ved å koble de to terminalene til CMUTen til den negative og positive inngangen til den foreslåtte CSA, slik at strømmen blir lest av fra begge terminalene og dermed gir et differensielt CSA inngangssignal. På denne måten blir andre harmonisk forvrengning forbedret.

En ekstraksjon av parasitisk kapasitanse er gjort og resultater fra simulasjoner av utlegget med disse parasittene er presentert som de endelige resultater.

Den foreslåtte CSA oppnår en båndbredde på 7.9MHz rundt en senterfrekvens på 5MHz med et gain ved senterfrekvens på 14.34dB med en CMUT som kilde og en sampling frekvens på 64MHz. Høy linearitet på HD_2=-83dB, en relativt lav effektforbruk på 110.6μW en inngangs impedanse på 3.1$k\Omega$ og en logaritmisk støy faktor på 5.79dB ble oppnådd med et areal forbruk på 39.8$\times$70.3μm^2.

Preface

First and foremost I would like to thank my supervisors Professor Trond Ytterdal and post doc. Carsten Wulff. Their deep knowledge of analog design, positive appearence and guidance along this thesis has been of great value for me and made an exiting task even more intriguing.

I would also like to thank my office companions Harald Garvik, Erlend Strandvik and Thomas Hanssen Nornes for their interest in exchanging knowledge and for a good office environment with many laughs.

Table of Contents

List of Tables

List of Figures

Abbreviations

ADC	=	Analoge to Digital Converter
CMFB	=	Common Mode Feedback
CMOS	=	Complementary Metal-Oxide-Semiconductor
CMUT	=	Capacitive Micromachined Ultrasound Transducer
CSA	=	Charge Sampling Amplifier
CT	=	Continous-Time
DR	=	Dynamic Range
DT	=	Discrete-Time
DSP	=	Digital Signal Processing
EDA	=	Electronic Design Automation
F	=	Noise Factor
FD-SOI	=	Fully Depleted Silicon On Insulator
FFT	=	Fast Fourier Transform
IVUS	=	Intravascular Ultrasound
LNA	=	Low Noise Amplifier
MEMS	=	Micro-Electro-Mechanical Systems
NF	=	Noise Figure
OpAmp	=	Operational Amplifier
SNR	=	Signal-to-Noise Ratio
SoC	=	System on a Chip
UTBB	=	Ultra-Thin Body and Burid oxide
VGA	=	Variable Gain Amplifier

Chapter 1

Introduction

Ultrasound is a popular tool for medical professionals in diagnosing and examinations inside the body. Ultrasound has the benefit over other medical imaging types in form of cost, that it can provide real-time images and it does not use ionizing radiation which may be harmful. There are several types of ultrasound techniques developed over the years like 2D-mode, Doppler ultrasonography and harmonic imaging. These techniques have different properties suited for different applications [1].

A type of ultrasound imaging technique is Intravascular ultrasound, IVUS, where a catheter with a ultrasound probe is led into the veins to be able to image the inside of the vein and locating problems such as plaque. The ultrasound transducers used for IVUS purpose need to be small and Capacitive Micromachined Ultrasound Transducers, CMUT, have proven to be a good alternative compared to the piezoelectric transducer for this purpose. CMUTs does not only have the advantage of modest size but can also be integrated on silicon in the same process as the CMOS circuitry. [2].

Modern nanoscale CMOS technology have also made it possible to implement relatively sophisticated logic in a small area. This opens the possibility to perform some of the digital processing, DSP, directly in the ultrasound probe itself which leads to less data transmission out of the probe and hence more elements can be put in the transducer array. This again gives an opportunity for 3D ultrasound imaging. [3].

Although digital circuits benefits from shrinking technology like lower power consumption, higher performance and less area consumption, analog circuitry does not have these same benefits. Nanoscale technology does often tolerate less supply voltage than larger technology. Because the relationship between signal-to-noise ratio and powerconsumtion includes voltage headroom the power consumption must be increased to maintain a certain level of accuracy [4]. This is a issue for IVUS since the power consumtion must be kept low so the temperature is held under a maximum limit. Also the intrinsic gain suffers from shrunk technology [5], [6]. This gives challenges in designing low power high performance analog circuitry like front end low noise amplifiers, LNA.

When a ultrasound echo is received at the transducer the signal may be very weak. For an analog-to-digital converter, ADC, to be able to convert it to a digital signal the received

signal needs to be amplified to a certian level without adding to much noise or distortion to the signal. The front-end LNAs performance is of utmost importance because the loss in signal here have a large impact on the rest of the system. The resulting image resolution will never be better than the signal achieved after the LNA.

There are two main methods of reading the signal from a transducer, voltage- and current readout can be realized both in continuous time or discrete time. By using discrete time i.e. doing the sampling in the pre-amplifier LNA the power consumption can be reduced compared to using a continuous time pre-amplifier LNA and sampling the signal in a subsequent block [7]. For a discrete time LNA circuit a current mode amplifier is intriguing since this will avoide the problems with linear settling which may set high demands to speed in the operational amplifier, OpAmp [8].

Further more the use of second harmonic imaging to improve the image clearity, contrast and details[1] sets high demands to low second harmonic destortion, HD2.

Sevral approaches have been made to solve the CMUT readout challenge with many different topologies like continuous time LNA [9]–[11], voltage mode sampling LNA [12] and current mode charge sampling LNA [7], [12].

In this work a the main focus has been the design of a fully-differential charge-sampling low noise amplifier in 28nm FD-SOI UTBB to see if placing the CMUT element between the two input terminals could reduce the second harmonic distortion compared to previous attempts. Complete schematic design and layout of the schematic has been made. And simulations and verification of this design has been performed using EDA tools.

1.1 Main Contributions

The main contributions in this work is the design and verification of a front-end fully-differential charge-sampling low noise amplifier for CMUT elements which contains:

- a fully-differential inverter-based amplifier with drain-to-gate feedback biasing in 28nm FD-SOI UTBB
- a discrete time CMFB circuit
- a highly linear charge sampling amplifier
- schematic and layout of the final charge sampling amplifier
- simulation and verification of layout with parasitic extraction in EDA tools

1.2 Thesis outline

The thesis is oulined as follows. Chapter 2 presents background theory used in the design. This includes general theory about transistors, amplifiers, noise, linearity and layout. In chapter 3 the design is presented with decisions explained based on theory from chapter 2 and specified goals. Chapter 4 presents verifications and results of the design. In chapter 5 the results are analyzed, discussed and compared to existing work. Finaly, in chapter 6, a conclusion is made based on the results and discussion.

Chapter 2

Theory

2.1 IVUS

IVUS is a medical imaging methology where a catheter with a ultrasound probe attached at the tip is used to see from the inside of a blood vessels. By using IVUS one could take ultrasound images from the inside of the body which in many situations are preferred to traditional ultrasound images.

Piezoelectric elements have been the preferred way to generate and detect ultrasound throughout the history. The reason is that the electric field strength needed has been to high for the capacitive mikromachined ultrasonic transducer, CMUT. However the last decades advences in microelectromechanical systems, MEMS, technology has made it possible to make CMUTs that are compatible with piezoelectric transducers. CMUTs also offers improved bandwidth, ease of fabrication of large arrays and integrations with electronics [2].

CMUTs can be produced in common CMOS prosesses and is therefore cheaper and the CMUT with its electronics can be made more compact with individual connections through wafer, therefore more transducer elements can be put in a given area. This makes CMUTs suitable for small ultrasound probes like in IVUS. CMUTs also provide wide bandwidth with a flat frequency response in the band. This gives the possibility to use imaging techniques such as harmonic imaging. Usually in harmonic imaging the transmitter frequency is set to $\frac{2}{3}$ of the senter frequency and the receiver frequency is se to $\frac{4}{3}$. This requires a flat frequency responce in a wide band and therefore CMUTs are suited. [2]. Second harmonic imaging is popular because it gives higher resolution in the resulting images than reading the receiving fundamental frequency. The reason is that tissue is nonliear and will distort the reflected signal. And so, by reading the fundamental frequency details may be lost [1].

In IVUS high-frequency and miniature probes are vital. Therefore CMUTs are well suited due to their sizes and high-frequency capabilities.

A CMUT consists of a metalized membrane, which is the top electrode, suspended above a heavily doped silicon substrate, which is the bottom electrode. The CMUT is

therefor a two-port device with the two electrodes as terminals.

In figure 2.1 the system is shown for the signal chain for one transducer. It consists of the CMUT, a RX/Tx-switch and in the receiving path a LNA and a ADC. The signal processing logic is commen for all transducers. In the transmitting path there is a power amplifier, a DAC and a waveform generator. In a transducer array used in a probe there

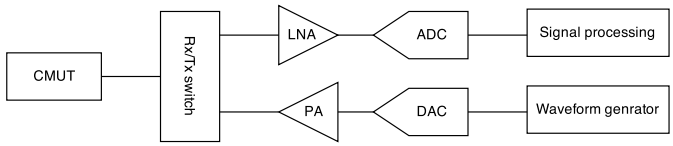


Figure 2.1: Signal path for one transducer element in a IVUS system.

might be several thousand individual transducers as shown in 2.2 with several sub-circuits for each transducer. Therefore it is important that the area consumption of each sub-circuit is small. Also the power consumption of every sub-circuit will be multiplied with the total number of transducers and therefore must be kept low to reduce the radiated heat which may heat up the blood in the veins.

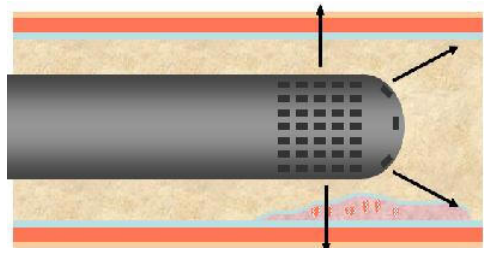


Figure 2.2: A catheter with transducers [13].

2.2 CMOS Transistors

CMOS technology is primarily developed for digital circuitry which benefits from shrunked technology due to lower supply voltage, less area consumption and less parasitics which makes power consumption lower [5]. To decrease cost from production it is desirable to design both digital and analog circuitry in the same technology so that only one technology is needed in the production process of system-of-a-chip, SoC [6].

There are some benefits of shrinking technology regarding analog circuits as well. For instance smaller gate area leads to decreased parasitic capacitance. This makes it easier to achieve higher bandwidths.

However the scaling of technology will not scale all parameters accordingly. For all practical purposes the transconductance will stay independent of technology node [14]. But the intrinsic gain of a transistor given in (2.1), decreases and the treshold voltage does

not scale down according to the supply voltage tolerated as technology is scaled down.

$$InrinsicGain = \frac{g_m}{g_{ds}} \tag{2.1}$$

Other non-idealities will, as sizes are decreased, have greater influence as well. To prevent unwanted circuit behavior after production non-idealities like high-field and short-channel effects as well as other effects like channel length modulation and mobility degradation [15] is important effects that should be considered in the design.

CMOS transistors are described by several behavior parameters. The most important parameters are threshold voltage V_{th} (2.2), drain current, I_D (2.3), transconductance g_m (2.4), drain source resitance r_{ds} (2.5), gate width W and gate length L.

$$V_{th} = V_{th-0} + \gamma(\sqrt{V_{SB} + 2\Phi_F} - \sqrt{2\Phi_F}) \tag{2.2}$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2[1 + \lambda(V_{DS} - (V_{GS} - V_{th}))] \tag{2.3}$$

$$g_m = \mu C_{ox}\frac{W}{L}(V_{gs} - V_{th}) \tag{2.4}$$

$$r_{ds} = \frac{1}{\lambda I_{D-sat}} \cong \frac{1}{\lambda I_D} \tag{2.5}$$

in equation (2.4)-(2.5) μ is the carrier mobility in bulk, C_{ox} is the gate capacitance per area, λ is the output impedance constant, γ is the body effect parameter and $2\Phi_F$ the surface inversion potential. V_{DS} is the drain-source voltage and V_{GS} the gate-source voltage.

The effective voltage $V_{eff} = V_{GS} - V_{th}$ gives an indication of the transistors trans-conductor efficiency given by (2.6)

$$\frac{g_m}{I_D} = \frac{2}{V_{eff}} \tag{2.6}$$

The ratio $\frac{g_m}{I_D}$ is valid for both strong- and weak inversion operation. The equation (2.3) is only valid in the strong inversion area where V_{eff} is relatively large. But as V_{eff} is decreased, and falls below approximately 100mV [15], to increase the trans-conductor efficiency, the transistors enters weak inversion region where equation (2.3) is no longer valid. The equation to describe the current in weak inversion is given in (2.7)

$$I_{D_{WI}} \cong I_{D_0}\left(\frac{W}{L}\right)e^{\frac{V_{eff}}{nV_T}} \tag{2.7}$$

where I_{D_0} is the current when $V_{eff} = 0$, V_T is the thermal voltage and n is the slope factor.

2.2.1 Fully Deplated Silicon on Insulator(FD-SOI)

As transistors are scaled down the channel gate area is decreased. This reduces the gate-control, making the transistor to have poorer performance. Because of this unwanted tendency fabrication plants tries to decrease gate leakage and lack of gate-control by adding additional layers in different materials under manufacturing. Production then becomes more complex and thus more expensive. UTBB FD-SOI is a technology developed to counteract this tendency [16]. It uses a thin layer of insulator under the channel, as shown in figure 2.3, which makes doping of the channel, as used in bulk CMOS, unnecessary. This gives less channel leakage and thus the channel can be made shorter, giving faster

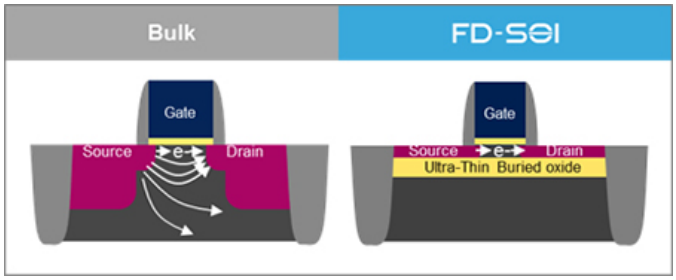


Figure 2.3: Bulk-CMOS and FD-SOI [16].

transistors. Two types of PMOS and NMOS, with different threshold voltages, are also offered by the FD-SOI technology. Low threshold voltage, LVT, transistors gives high performance and regular threshold voltage, RVT, transistors gives low power consumption.

2.2.2 Mismatch and Variability

After production transistors in a circuit may have slightly different performance than intended while design. After the manufacturing the transistor sizes and dopance may have changed because the fabrication plant cannot be perfectly accurate and so small deviations will accure. For instance the produced layout mask may have some diviation from the designed mask and also when masks are put on the top of each other they may not line up perfectly. An other sources to difference between design and manufactured circuit is scattering from well edges under ion implantation [15].

This mismatch and variability may in some circuits have great influence on performance. In circuits where two or more transistors needs to be equal or exactly scaled to each other small deviations in size may even make the circuit to not work at all if not accounted for during design. An example of such a circuit is the differential input pair. In a differential pair the output value should be zero if V_{gs} at the two input transistors are equal. If the threshold voltages differes in the two transistors equal V_{gs} will not give zero in output value because V_{eff} now differes. This leads to an offset. Also the trans-conductor effeiciency will be different at each side leading to possible distortion. The offset variation in a differetial pair is given in (2.8) [15].

$$\sigma^2(V_{OS}) = \frac{\sigma^2(\Delta I_D)}{g_m^2} = \frac{1}{WL}\left[A_{Vt0}^2 + \left(\frac{I_D}{g_m}\right)^2 A_{\kappa'}^2\right] \tag{2.8}$$

where A_{Vt0} and $A_{\kappa'}$ is proportionally constants. V_t is the threshold voltage and $\kappa' = \mu_n C_{OX}(W/L)$.

As seen from the equation (2.8) to reduce the influence of mismatch one can increase the transistor area and the tranc-conductor efficiency $\frac{g_m}{I_D}$.

Because there is no need to dope the channel in FD-SOI transistors, unlike conventional planar bulk CMOS, there will be less variation in production than conventional CMOS transistors [17]. For this reason less margin is needed in a circuit design to obtain high yield after production, and thus the ciruit can be made more current efficient and area efficient while obtaining the specifications.

2.3 Amplifier

2.3.1 Operation Amplifier

An operation amplifier, OpAmp, is an generic form of multipurpose amplifiers used mostly for small signal operations. An OpAmp can be design for many different applications and are characterized by several properties.

The gain in a single point of the $^{V_o}/_{V_i}$ characteristic is called the small signal gain, as given in (2.9). For large signals the amplifier may enter compression and this is considered in the large signal gain given in (2.10)

$$A_{ss} = \frac{\partial V_o}{\partial V_i} \tag{2.9}$$

$$A_{ls} = \frac{V_o}{V_i} \tag{2.10}$$

If the OpAmp is loaded with a capacitor the transfer function will have a low pass characteristics given by (2.11)

$$\left|A(f)\right| = \frac{G_m R_{out}}{\sqrt{(2\pi f R_{out} C_L)^2 + 1}} \tag{2.11}$$

where G_m is the transconductance, R_{out} is the output resistance and C_L is load capacitor. From (2.11) it's seen that the DC-gain becomes (2.12)

$$A_{DC} = G_m R_{out} \tag{2.12}$$

the OpAmp unity gain frequency, f_{ug}, is (2.13)

$$f_{ug} = \frac{G_m}{2\pi C_L} \tag{2.13}$$

and the -3dB bandwidth, f_{-3dB}, is given by (2.14)

$$f_{-3dB} = \frac{1}{2\pi R_{out} C_L} \tag{2.14}$$

In discrete time applications the settling time characteristics is also important. The settling time is defined as the time OpAmp uses to reach a output value within a certain accuracy compared to the correct value.

The settling time can be divided into two periodes, slew rate and linear settling [18]. The duration of the slew rate periode is dependent of the maximum current the output of the OpAmp can deliver and the load capacitance as given in equation (2.15). The slew rate is signal dependent and is therefore a non-linear effekt that may lead to distortion.

$$SR = \frac{I_{out_{max}}}{C_L} \tag{2.15}$$

The linear settling periode is dependent of the OpAmp f_{ug} and the accuracy of which the output have to settle. Linear settling is given by (2.16)

$$t_{set} = -\tau ln\left(\frac{Err}{100\%}\right) \tag{2.16}$$

where τ is the OpAmp time constant related to f_{ug} by (2.17) and Err is the accuracy in percent.

$$\tau = \frac{1}{2\pi f_{ug}} \tag{2.17}$$

2.3.2 Class of Operation

The four main classes of linear amplifier operation are class A, AB, B and C. Class A achives highest linearity, but will also have the highest power consumption since there always will be a static current to keep the transistor in active region and far from cut-off. To increase efficiency the transistors can be biased into class B. In this case the one transistor, in a push-pull configuration, will be turned off while the other is conducting. This will ideally remove the static current, but it also means that the transistors must operate in the nonlinear region between cut-off and active region which gives poor linearity. To avoid this the transistors can be biased between class A and class B called class AB. In class AB a small static current are allowed to increase linearity. Here the transistors will overlap in the region the transitors are nonlinear. This improves the linearity but at the cost of higher static current consumption. Class C means biasing the transistor lower, further than class B, which makes even lower linearity performance but also lower power consumption.

A push-pull class AB configuration like an inverter will have better slew rate performance than a class A common source configuration amplifier because there is no current source limiting the maximum peak output current.

2.3.3 Inverter

A CMOS inverter, depicted in 2.4, is a building block originally intended as a logical port. It consists of two complementary transistors, one PMOS and one NMOS, both connected in a common source configuration.

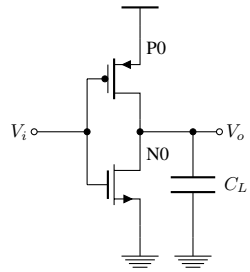


Figure 2.4: MOSFET inverter.

Because both the PMOS and the NMOS are active transistors the transconductance from both contribute to the total transconductance and the inverter will have higher total transconductance than other single stage configuration amplifiers like the common source. With twice the G_m, assuming $g_{mn} = g_{mp}$, and the same output resistance as a common source, the gain, given by (2.18), is twice a high. The unity-gain frequency also doubles with the same load (2.19). This makes inverter to have twice the trans-conductor efficiency, $\frac{g_m}{I_D}$, as a common source amplifier.

$$A_v = \frac{v_o}{v_i} = -G_m \times R_{out} = -(g_{mn} + g_{mp}) \times (r_{dsn} \| r_{dsp}) \tag{2.18}$$

$$f_{ug} = f_{-3dB} \times A_v = \frac{G_m}{2\pi C_L} = \frac{g_{mn} + g_{mp}}{2\pi C_L} \tag{2.19}$$

Biasing can be challanging with the inverter since the PMOS and NMOS will both work as active transistors but in opposite direction, they works as a push-pull configuration. The class of operation will depend on the threshold voltage and the supply voltage as shown in figure 2.5.

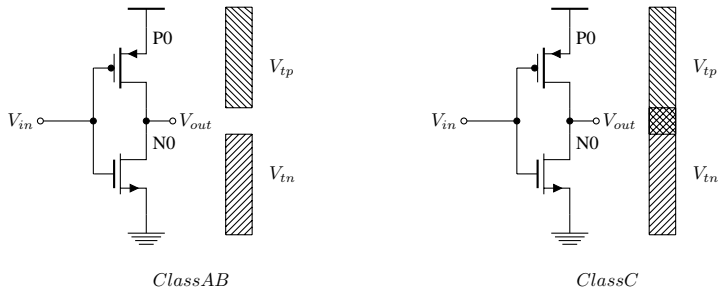


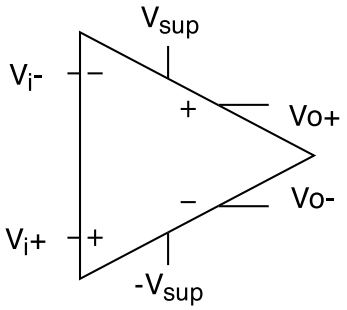
Figure 2.5: Inverter class of operation [19].

The class of operation is AB as long as $V_{sup} \geq V_{thn} + V_{thp}$ and class C if $V_{sup} < V_{thn} + V_{thp}$ as shown in figure 2.5. As one enters deeper into class AB the trans conductor efficiency increases as V_{eff} decreases and $\frac{g_m}{I_D}$ increases. A drawback by pushing the inverter far into class AB is that, to maintain the current needed to keep a sufficient slew rate at large output swings, the transitor sizes must be increased. The increased sizes will increase the parasitics in the transistors which may decrease the intrinsic cut-off frequency, f_T of the amplifier.

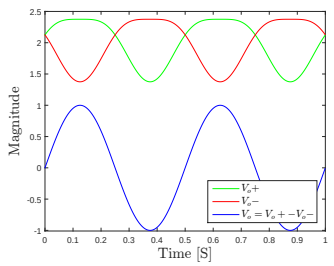
2.3.4 Fully Differential Amplifier

A fully differential amplifier is an amplifier where both input and output have two terminals as shown in figure 2.6(a). It senses the voltage differens between the input ports, multiplies this differens with the gain A and produces a differential output (2.20). If balanced input signals is applied the even order harmonic distortion, generated by the amplifier, will be canceled as seen from (2.29) where all terms with power of even order will be canceled shown in 2.6(b).

$$V_o = (V_{o+} - V_{o-}) = A(V_{i+} - V_{i-}) \tag{2.20}$$



(a) Differential amplifier.



(b) Output signals with even order distortion.

Figure 2.6: A differential amplifier and its output with even-order distortion.

The voltage of which the output signals V_o+ and V_o- swings around is called the output common mode voltage given by (2.21). In the same way there is an input common mode voltage. The common mode output voltage vary with the input common mode voltage and therefore a additionally circuit is needed called a common mode feedback. The purpose of this circuit is to keep the output common mode voltage at a specified level usually midway between the rail voltages.

$$V_{CM_o} = \frac{V_{o+} + V_{o-}}{2} \tag{2.21}$$

If the input signals is not perfectly balanced and the amplifier do not have infinitely high common mode rejection ratio, CMRR, the even order distortion is not completely canceled. CMRR is the rejection the amplifier have from a common mode input voltage variation to an output differential voltage variation. The common mode input to differential output voltage gain, A_{CM} can be added to equation (2.20) as shown in (2.22).

$$V_o = A(V_{i+} - V_{i-}) + A_{CM}\left(\frac{V_{i+} + V_{i-}}{2}\right) \tag{2.22}$$

CMRR can now be find by (2.23).

$$CMRR = \frac{A}{A_{CM}} = 20log\frac{A}{A_{CM}}dB \tag{2.23}$$

2.3.5 Biasing

An inverter as shown in figure 2.4 needs to be biased so that the point of operation on the input node is at the point where the gain, f_{ug} and linearity is at its highest. The output should also be in the middel of the rails to give maximum output swing. If both input and output point of operation is at the same voltage level a bias scheme called *drain-to-gate feedback resistor biasing* [20] shown in 2.7 can be used.

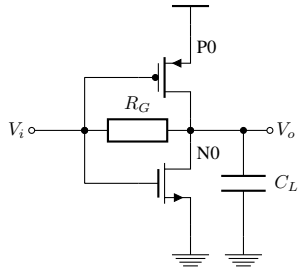


Figure 2.7: MOSFET inverter with drain-to-gate resistor feedback biasing.

In the topology the DC operating point at the input is set by the output operating point. The gate of the PMOS and NMOS are high impedance nodes at low frequencies so very little DC current flows through R_G, which makes both PMOS and NMOS to be diode connected transistors at low frequency. Therefore the transistors are self biased into active region. The biasing scheme set a limitation of the output swing because the transistors will leave the active region [21]. The minmum output voltage is given by (2.24) and the maximum voltage by (2.25).

$$V_{out_{min}} \approx \frac{V_{DD} - V_{SS}}{2} - V_{Tn} \tag{2.24}$$

$$V_{out_{max}} \approx \frac{V_{DD} - V_{SS}}{2} + V_{Tp} \tag{2.25}$$

As seen from equation (2.24) and (2.25) this topology is not suited for curcuits where the supply voltage is much larger than the threshold voltage. In modern nanoscale CMOS technology however the supply voltage is usually around 1V or lower and hence this bias scheme is suitable.

The drain-to-gate feedback resistor will lower the output resistance because it will act as a parallel connection with R_{DS} to virtual ground. A lower output resistance will lead to lower gain according to (2.18). To find the influence the drain-to-gate feedback resistor has on the gain and bandwidth some calculation can be performed. The calculations together with a small signal equivalent can be found in Appendix A.1 and the resulting equations is shown in (2.26) for gain and the transfer function in (2.27)

$$A_{DC} = -\frac{G_M R_{DS} - \frac{R_{DS}}{R_G}}{1 + \frac{R_{DS}}{R_G}} \tag{2.26}$$

$$|A_{AC}|^2 = \frac{(\omega R_{DS} C_{gd})^2 + \left(G_M R_{DS} - \frac{R_{DS}}{R_G}\right)^2}{(\omega R_{DS}(C_L + Cgd))^2 + \left(1 + \frac{R_{DS}}{R_G}\right)^2} \tag{2.27}$$

It is seen from equation (2.26) that R_G will have a great influence on the DC-gain for small values of R_G because the second term in the numerator will be subtracted from the first term and the denominator will be large. However if R_G is kept at a high value then the influence will be negligible. The frequency response is given in (2.27) and in (2.28) it is solved for a gain of one to see the influence of R_G to the f_{ug}.

$$f_{ug} = \frac{1}{2\pi}\sqrt{\frac{G_M^2}{C_L^2 + 2C_L C_{gd}} - \frac{G_M}{2R_G(C_L^2 + 2C_L C_{gd})}} \tag{2.28}$$

Equation (2.28) shows that for large values of R_G the first term under the root sign will dominate and the f_{ug} will be almost identical to the frequency without R_G. However for small values the second term will dominate and the f_{ug} will be zero. One reason is that the gain will be lower and at some point even under one.

2.3.6 Common Mode Feedback

To control the common mode voltage of a fully-differential OpAmp some circuitry is needed. This kind of circuitry is called common-mode feedback, CMFB. The CMFB circuit finds the middle voltage between the two differential signals and compare it to a desired voltage and forces the two voltages to be equal. CMFB circuits can be implemented as both continous-time circuits or as switched-capacitor circuits. Continous-time CMFB has limitations in maximum swing and are hard to design linear over a large voltage swing which again limits the OpAmp output swing. It will also, for most topologies, use static power. Switched capacitor CMFB are most suited for discret time circuits because the switching may leed to clock feedtrough glitches in the outputsignal of a continous-time

circuit. Also if large capacitors is needed in the switched capacitor CMFB the amplifier load is increased resulting in a need for higher current delivery demands from the amplifier. An example of a switched-capacitor CMFB circuit [27] is shown in 2.8.

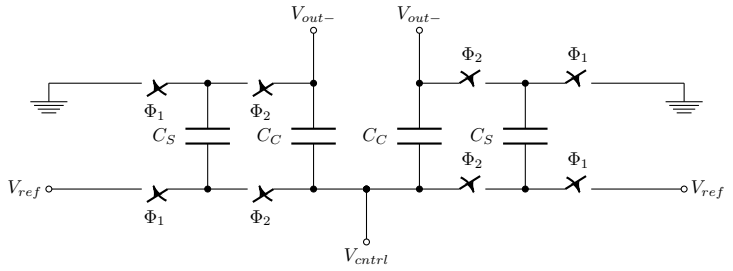


Figure 2.8: Switched-Capacitor CMFB circuit [15].

The operation is as follows. The capacitors C_C provides a AC feedback path from the amplifier output nodes to a control node in the amplifier. The common mode gain is high, but the differential gain is kept low, idealy zero. This way the common mode can be be controlled to a constant value and the CMFB circuit will have little effect on the amplifier differential gain. Since DC voltage is blocked by C_C the capacitors C_S and the switches is needed to set the CMFB DC level. C_S provides a voltage drop over C_C that gives the desired common-mode output.

2.4 Dynamic Range

An important property of an amplifier used for high accuracy applications is dynamic range, DR. DR gives the ratio between the smallest and largest signal that the amplifier can handle. In the lower end DR is limited by noise and in the upper end by linearity.

2.4.1 Linearity

In a linear amplifier the output signal should be a exact replica of the input signal only with higher amplitude. But there are limitation due to non-idealities that will change the signal somewhat on its way through the amplifier. These limitations are among others compression due to limitation in supply headroom and non-linear $^{I_o}/_{V_i}$ characteristics.

Harmonic Distortion

If a sinusoidal signal is applied to a nonlinear system, the system will generate harmonic frequency components such that the output signal will have a frequency component as the input signal, f_{in}, but also components at nf_{in} (n=2,3,4...). If the input signal of the nonlinear system is $v_{in}(t)$ and the output is $v_o(t)$, then the output signal can be expressed as the Taylor series expansion shown in (2.29) [15].

$$v_o(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) + a_4 v_{in}^4(t) + ... \tag{2.29}$$

where a_1 is the term of the fundamental frequency and a_2, a_3 and a_4 is the terms of second-, third- and fourth-order harmonic distortion.

If $v_{in}(t)$ is given by (2.30)

$$v_{in}(t) = Acos(\omega t) \tag{2.30}$$

then the output signal is approximated by (2.31)

$$\begin{aligned} V_o(t) &= a_2\frac{1}{2}A^2 + (a_1A + a_3\frac{3}{4}A^3)cos(\omega t) + a_2\frac{1}{2}A^2cos(2\omega t) + a_3\frac{1}{4}A^3cos(3\omega t) + ... \\ &= H_{D_0} + H_{D_1}cos(\omega t) + H_{D_2}cos(2\omega t) + H_{D_3}cos(3\omega t) + ... \end{aligned} \tag{2.31}$$

where H_{D_0} is the DC component and H_{D_1}, H_{D_2} and H_{D_3} are the amplitudes of the fundamental, second- and third- harmonic components. From this the second- and third-harmonic distortion ratios can be found by (2.32) and (2.33)[15]

$$HD_2 = \frac{H_{D_2}}{H_{D_1}} = \frac{a_2\frac{1}{2}A}{a_1 + a_3\frac{3}{4}A^2} \overset{\frac{3}{4}a_3A^3 \ll a_1A}{=} \left(\frac{a_2}{a_1}\right)\left(\frac{A}{2}\right) \tag{2.32}$$

$$HD_3 = \frac{H_{D_3}}{H_{D_1}} = \frac{a_3\frac{1}{4}A^2}{a_1 + a_3\frac{3}{4}A^2} \overset{\frac{3}{4}a_3A^3 \ll a_1A}{=} \left(\frac{a_3}{a_1}\right)\left(\frac{A^2}{4}\right) \tag{2.33}$$

In a fully differential system with perfectly balanced input signals, the even order terms in (2.31) will be canceled and so the evenorder distortion will be suppressed.

A measure for all the harmonics compared to the fundamental frequency is total harmonic distortion, THD. THD is the sum of all harmonics divided by the fundamental tone in decibel [15] as shown in (2.34)

$$THD = 10log\left(\frac{H_{D_2}^2 + H_{D_3}^2 + H_{D_4}^2 + ...}{H_{D_1}^2}\right) \tag{2.34}$$

Second- and Third-Order Intercept Point (IP2,IP3)

As the input signal of an amplifier increases the output signals fundamental and harmonic components will increase. The fundamental component will be much larger than the hamonics for small input signals and the harmonics will also be below the noisfloor and, hence, not be visible in the fast fourier transform, FFT, spectrum of the output signal. But as the input signal increases the harmonincs will arise above the noise floor and increase faster than the fundmental component. When the input signal gets larger the output will be limited by the maximum swing of the amplifier and so the slope will flatten out and no longer be linear. If the linear slope of the fundamental and the third harmonic component would continue infinitely they would at some point intercept as shown in 2.9. This intercept point is called Third-Order Intercept Point or IP3. The second-order intercept point is the intercept point between the fundamental and the second harmonic component. These points can be measured as terms of the input signal, IIP2 and IIP3, or as terms of the output signal, OIP2 and OIP3.

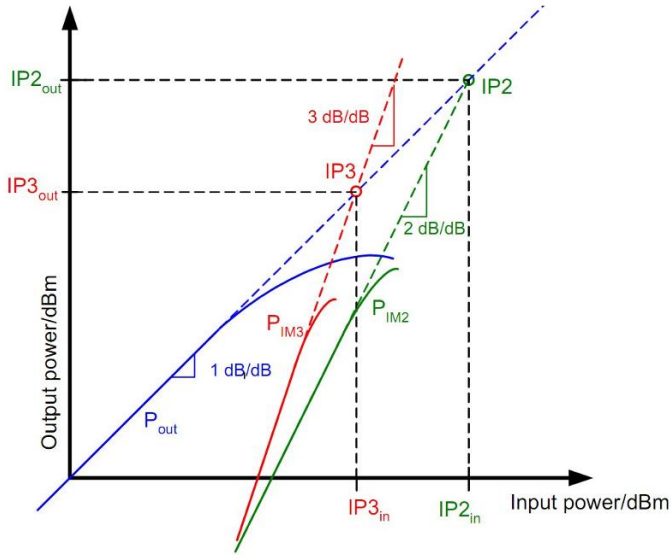


Figure 2.9: Typical $^{V_o}/_{V_i}$ relationship [22].

2.4.2 Noise

Types of Noise

The most dominant types of noise in a CMOS transistor are flicker noise and thermal noise. Thermal noise occurs due to the channel resistance. In figure 2.10 the thermal noise is modeled as a current source, $I_{tn}^2(f)$. A simple model for the thermal noise is given in expression (2.35), where T is the temperature in Kelvin, k is Boltzman's constant and g_m is the transistors transconductanse. More advanced models are obtained in [23]. The flicker noise, $V_{fn}(f)$, is given approximately by (2.36) where L is the transistor length, W the width, K is a constant dependent on device properties, f is frequency and C_{ox} is the gate capacitance per area. Flicker noise is the noise type that dominates at low frequencies [15].

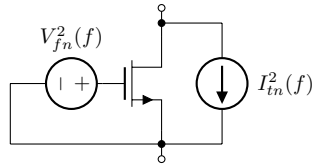


Figure 2.10: Noise model MOSFET.

$$I_{tn}^2(f) = 4kT\left(\frac{2}{3}\right)g_m \tag{2.35}$$

$$V_{fn}^2(f) = \frac{K}{WLC_{ox}f} \tag{2.36}$$

The input referred noise is given by (2.37) and is obtained by referring both noise sources of 2.10 to the gate.

$$V_i^2(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_m} + \frac{K}{WLC_{ox}f} \tag{2.37}$$

The noise in a resistor can be modeled as a current shown in figure 2.11

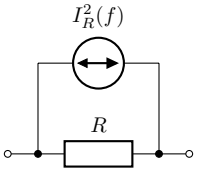


Figure 2.11: Noise model for a resistor.

and the noise current is given by equation (2.38)

$$I_R^2(f) = \frac{4kT}{R} \tag{2.38}$$

Noise Figure

Noise factor, F(f), is a measure to tell how much the signal to noise ratio, SNR, is reduced through a circuit. When calculating noise factor noise spectral density at a particular frequency, $spotnoise$, is used. Since the signal and the noise from the source both are amplified by the circuits gain, the output signal will be the input signal times the gain, and so can be replaced in the equation by a gain factor. The noise, however, is amplified, but in addition the noise from the circuit itself is added to the total output noise. The noise factor is thus the ratio of the total noise, input noise plus circuit noise, to the noise that would appear if the circuit was noiseless. If all noise is referrd to the circuit input node the expression of F(f) becomes (2.39). Noise figure, NF(f) is the noise factor, F(f), in decibel as shown in (2.40) [15].

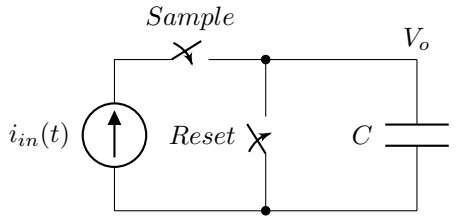
$$F(f) = \frac{V_{n_{source}}^2(f) + V_{n_{circuit}}^2(f)}{V_{n_{source}}^2(f)} = 1 + \frac{V_{n_{circuit}}^2(f)}{V_{n_{source}}^2(f)} \tag{2.39}$$

$$NF(f) = 10log_{10}[F(f)]dB = 10log_{10}\left[1 + \frac{V_{n_{circuit}}^2(f)}{V_{n_{source}}^2(f)}\right]dB \tag{2.40}$$

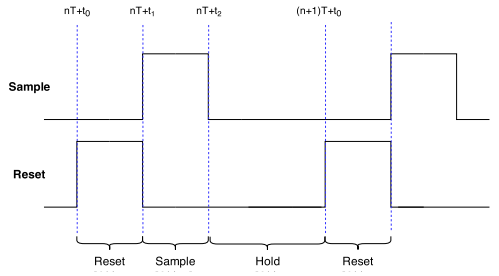
2.5 Charge Sampling

In applications when the signal from the source is a current, i.e. when the source impedance is high, a charge sampling circuit will be more suited than a voltage sampling circuit. Also, charge-sampling is a attractive alternative over voltage-sampling circuits for high speed-applications because the signal is processed in the current domain and in this way avoiding voltage settling.

A simplified charge sampling circuit is shown in figure 2.12(a). It consists of two switches and a sampling capacitor. The process is composd of three phases: charging-, holding and reset phase shown in figure 2.12(b). The operation is as follows, first the reset-switch resets the capacitor, then the sampling-switch closes and lets current flow from the source and charge the capacitor. After a specified charge time the sampling switch is opened and the charge is held until the reset switch is closed and the process is repeted. The equation for the output node is given in 2.41 for $t \in [nT + t_1, nT_{t2}]$. The frequency domain transfer function is derived in [8] and is given in equation (2.42).



(a) Charge sampling.



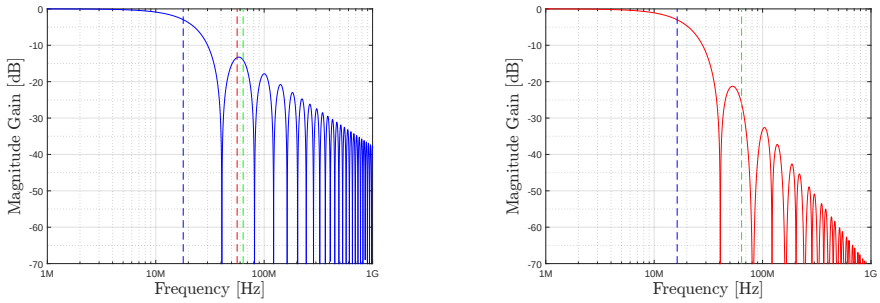
(b) Clock phases.

Figure 2.12: Charge sampling circuit and clock phases.

$$v_o(nT + t_2) = \frac{1}{C} \int_{nT+t_1}^{nT+t_2} i(t)dt \tag{2.41}$$

$$V_o(f) = \frac{\Delta t}{C} \left(\sum_{i=-\infty}^{\infty} I(f - if_s) sinc(\pi \Delta t (f - if_s)) \right) \Delta t_h sinc(\pi \Delta t_h f) \tag{2.42}$$

Figure 2.13(a) shows (2.42) plotted with normalized magnitude, i=0 and with the magnitude degrading from Δt_h is excluded. The sampling frequency, $f_s = \frac{1}{T_s}$, is set to 64MHz, chargetime is set to $0.5T_s$ and reset to $0.25T_s$. Figure 2.13(b) is the normalized plot of (2.42) with magnitude degrading including.



(a) Without magnitude degrading from hold-phase.

(b) With magnitude degrading from hold-phase.

Figure 2.13: Charge sampling transfer function.

The blue vertical lines marks the -3dB point, which is at $\frac{0.14}{\Delta t}$, the green lines marks the sampling frequency, f_s, and the red line marks the senter frequency of the first side lobe. For very high speed applications this side lobe can be used as passband. An important property of charge sampling is that the -3dB bandwidth is decided by the duration of Δt. Since the duration of Δt is not directly dependent of technology the technology can be selected to fulfill other specifications.

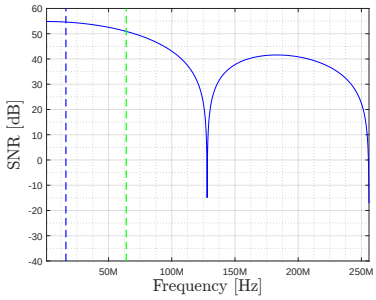
The plots in figure 2.13 is normalized and the magnitude will depend on the duration of the charge phase. If $\Delta t = 0.5$ only 50% of the signal is charged into the capacitor and so the magnitude will be 6dB lower than if all the signal had been charged into the capacitor.

A critical limitation of high-speed sampling is clock jitter. Clock jitter is the variation in rising or falling clock edges in time. If a clock edge shold rise at the time T it will, in a realized clock generator, infact rise at $T \pm \delta t$ where δt ia a small random number. The clock jitter is introduced by device noise and phase noise of oscillator [24]. This means that the sampling time is not at the exact point it was intended, and with a varying input signal, the sampled value becommes somewhat larger og smaller than the correct value. For charge sampling the signal to jitter noise ratio is given by (2.43) [25]

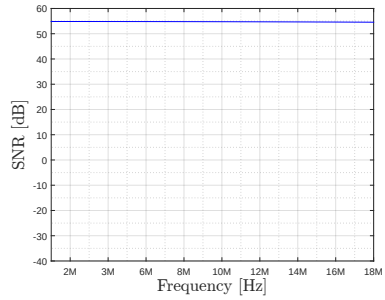
$$SNR = 10log\left(\frac{\left(sin\left(\frac{\omega\Delta t}{2}\right)\right)^2}{\left(sin\left(\frac{\omega\delta t_0}{2}\right)\right)^2 + \left(sin\left(\frac{\omega\delta t_0}{2}\right)\right)^2}\right) \tag{2.43}$$

Where δt_0 and δt_1 is the jitter error in rising and falling clock edges of the charging clock.

Figure 2.14 shows a plot of SNR versus input frequency with $\delta t_0 = \delta t_1 = 10ps$, charging periode $\Delta t = 0.5\frac{1}{f_s}$ and $f_s = 64MHz$.



(a) SNR versus input signal frequency.



(b) SNR versus frequency showing the -3dB passband.

Figure 2.14: SNR versus input signal frequency.

It is seen from figure 2.14 that the error due to jitter in a charge sampling circuit is almost independent of frequency in the passband which, for some applications, is advantageous.

The noise in charge sampling circuits is due to switches, the noise from input and the total output noise is given in equation (2.44) [8]

$$e_v^2 = \frac{kT}{C}\left(\frac{2\Delta t}{R_S C} + e^{-\frac{2\Delta t}{R_{eq}C}}\right) \tag{2.44}$$

where R_S is the source resistance, R_{eq} is the parallel connection between the source resistance and the off resistance in the reset switch, $R_{eq} = R_S||R_{off}$. If $R_{off} \gg R_S \Rightarrow R_{eq} \approx R_s$ (2.44) becommes (2.45)

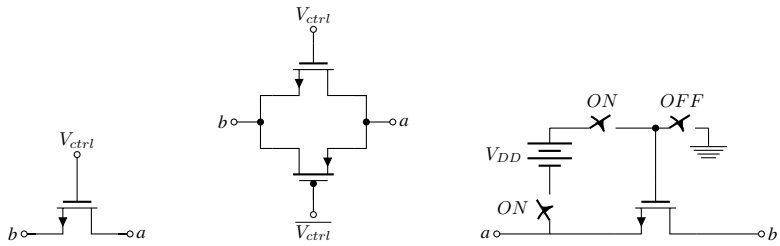
$$e_v^2 = \begin{cases} \frac{kT}{C} & \text{if} 2\Delta t \ll R_S C \\ \frac{kT}{C}\left(\frac{2\Delta t}{R_S C}\right) & \text{if} 2\Delta t \gg R_S C \end{cases} \tag{2.45}$$

which states that the noise will be near $\frac{kT}{C}$ if $2\Delta t \ll (R_S C)$ i.e. when the source impedance is high, the integration capacitor is large and the charging duration is short.

2.6 CMOS Switches

CMOS switches can be implemented as a single NMOS transitor, shown in figure 2.15(a), a transmissiongate with a NMOS and a PMOS in parallell, shown in figure 2.15(b) or as a bootstraped switch, shown in figure 2.15(c).

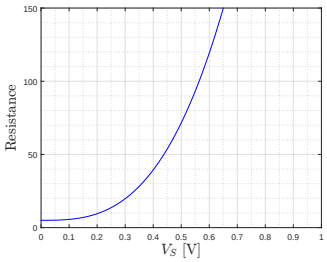
The simplest switch is a single NMOS transistor where input and output is the drain and source nodes and the control port is the gate node. The NMOS switch is limited by the voltage level at input and output. If the source node is near upper rail V_{GS} will be small and may be to low to turn the switch on. Also if the voltage level on the source node varies over a large voltage range the on-resistance, shown in figure 2.16(a) will vary which in some applications cannot be tolerated. To give the switch less variation in on-resistance a PMOS can be put in parrallel which will have lower resistance for high input and output voltage levels. But it increases complexity because a inverted version of the control signal is needed. Another drawback with transmissiongates is the increased impedance when input and output voltagelevel is halfway between the rails compared to high or low voltage levels as shown in figure 2.16(b). If the supply voltage is low the switch may even be completely off for the voltage region midway between the rails.



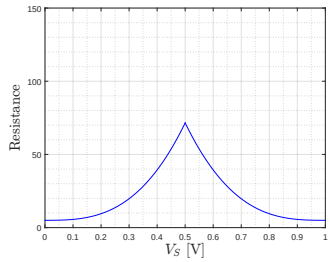
(a) NMOS switch. **(b)** Transmission gate. **(c)** Bootstrapped switch.

Figure 2.15: Three implementations of CMOS switches.

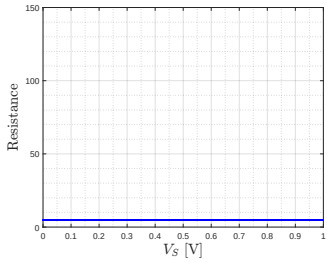
A way to improve this performance is the use of bootstrapped switches. This type off switch keeps the V_{GS} voltage constant for all voltage levels at input/output ports by the introduction of a voltage source between Source and Gate of the transistor. The common way to implement this voltage source is by a capacitor which is charge to VDD. Although constant on-resistance, a bootstrapped switch requires more transistors and a capacitor making them more complicated than other types of switches [26].



(a) NMOS switch.



(b) Transmission gate.



(c) Bootstrapped switch.

Figure 2.16: Relative resistance in the three different types of switches.

If the voltage level at the source of the switch is low and the voltage swing is low usally NMOS switches is used due to lowest complexity, lowest area and low noise performance. For nodes with large voltage swings the bootstrapped switch has the best performance due to the constant ON-reistance, but because of complexity and size transmissiongates are sometimes preferred.

An unwanted effect introduced by the use of transistor switches is charge injection. When the transistor is turned off the charge in the channel will flow out through the source and drain nodes of the transistor. The amount of channel charge in a transistor with $V_{DS} = 0$ is given by [15]

$$Q_{ch} = WLC_{OX}V_{eff} \tag{2.46}$$

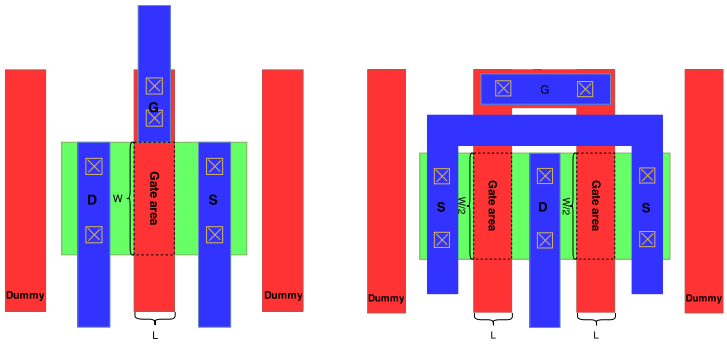
The expression in (2.46) indicates that small transitors will give less charge injection and large $V_{eff} = V_{GS} - V_{th}$ will give more charge injection. As (2.46) is dependent of V_{eff} the charge injection is dependent on the voltage level of the source node and, thus, signal dependent.

2.7 Layout

An integrated circuit is produced in several steps dependent of technology and number of layers in the prosess. To be able to build up an integrated circuit at a fabrication plant masks that blocks areas of the circuits at different stages in the process steps must be made. These mask will determind the geometry of the final chip and it's the designers responsibillity to create the geometry of these masks. The process of defining the geometry of these masks is called layout.

The masks must meet certain requirements or layout design rules which aims to compensate for the mask misalignment that may occur in production. As an example there is a rule that limits the minimum space between the drain and source contacts to the gate polysilicon. This way they will not overlap and shorts between gate and drain or source are avoided.

The rules are stricter for layout of analog circuitry than digital circuitry. The reason is that analog circuits are more sensitive to parasitics as capacitance and higher resitance in connections between layers than modeled under design. The latter can be solved by using more via connections. Also transistors for analog circuits are usually much wider than in digital circuits. Therefore the number of gate fingers are increased. To make transistors more square-shaped and compact they can be realized by using more fingers. A transitor with one finger is shown in 2.17(a) and a transistor with two fingers is shown in 2.17(b).



(a) Transistor with one gate finger. **(b)** Transistor with two fingers.

Figure 2.17: Green=active area, Red=polysilicon, Blue=Metal 1 and Yellow=Via hole.

The dummy polystrips in figure 2.17 are added to give transistors junctions equal surroundings and this way the surroundings will have less effect on the transistor performance.

If some transistors need to be matched to others, as the case for a differential pair, then the transistor should be build up with a number of unit sized transistors in parallel. These transistors should be laid out in a pattern so that production variation over the die area have the same influence on all the unit transitors. For instance if a differential pair, consisting of transistor A and B, is divided into unit transistors a pattern that give both A and B almost equal variation is by the pattern in figure 2.18.

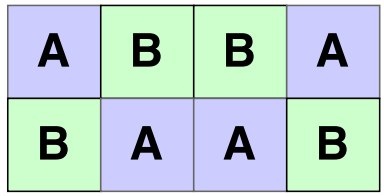


Figure 2.18: Layout pattern to give equal process variation for matched transistors.

An other advantage of using M-factor is lower series resistance and lower junction capacitance, but due to routing the parasitic capacitance will increase. Because some circuitry is very sensitive to parasitic effects it is important to locate the nodes in the circuit which is most critical for parasitics and take extra care at these nodes in the layout.

In modern design tools built-in functions that will give warnings is the layout don't meet the design rules, there are tools for checking that all design rules are fulfilled and tools to compare the layout to the schematic so that all transistors are included, that they have the right sizes and that they are correctly connected to each other. Parasitc capacitance, resistance and conductance can also be extracted from the layout to model more non-idealities that will arrise after production. This can help the designer in find bad layout choices and correct them before production.

2.8 Figure of Merit

Figure of Merit, or FoM, is a measure to be able to compare different designs in different technologies. Dependent of application the FoM should include specifications as, power consumption, bandwidth, gain, noise performance, linearity performance and area consumption. A commonly used FoM for low power, low voltage amplifiers [14] is (2.47).

$$FoM = \frac{P}{DR^2 f} \tag{2.47}$$

In design of analog integrated CMOS circuits there are trade offs so that a circuit can achieve the specifications with sevral solutions. Figure 2.19 shows the three tradeoffs power, speed and accuracy. A circuit can be made accurate and fast by increasing g_m and add capacitance. However to drive the capacitance a larger bias current is needed and, hence, high power consumption. High speed and low power can be achieved by using low capacitance and biasing the transistor in weak inversion.

For the case of low-noise front-end amplifiers important spesifications are gain bandwidth, noise factor, linearity and for IVUS ultrasound probes the area should be small. Also, like for all integrated circuits the power consumption should be kept as low as possible. In second order harmonic imaging the most critical distortion term is the second hormonic distortion and higher order distortion terms are not as important. The common way to specify the noise of a LNA is the noise faktor, F, and therefor it should be included in the FoM. The bandwidth is also important and can be tarded for power or area and

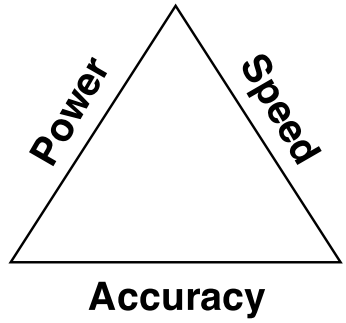


Figure 2.19: Analog CMOS IC design tradeoffs.

should be included. Therefore a suitable FoM for a LNA amplifier for second-harmonic imaging is (2.48)

$$FoM_{LNA} = \frac{P_{tot} A_{tot} HD_2 F}{BW} \tag{2.48}$$

In equation (2.48) P_{tot} is the total power consumption, A_{tot} is total area consumption, HD_2 is the second harmonic component, F is the noise factor and BW is the -3dB bandwidth. The lower value of FoM_{LNA} the better.

2.9 Computer Assisted Design

The behavior of transistors are very complex and include many higher order effects which may have great influence in a circuit design. Therefore advanced models, which tries to include as many of these effects as possible are developed through the years. As computers becommes faster and more powerfull more complex models can be used to describe transistors. Therefore modern design is done with sophisticated software, with tools to ease development and assure quality. Simulators are used to check the behavior of circuits where parasitic effects are modeled in circuit elements.

A circuit design is usually first simulated in a schematic representation. However this schematic does not take into account all parasitics and interconnects between different wires and circuit elements that is placed near each other. Therefore some effects that will occur in the fabricated circuit will not appear in the schematic simulations. After layout it is possible, with CAD tools, to extract these parasitics, but if the ciruit is large it may take some time to find areas where parasitics is causes errors. For this reason it is good practice to divide the schematic into many smaller subcircuits and do layout and simulation of these separately. This eases the search for errors and saves time.

Circuit performance may also deviate from simulated after production due to productions variations. Such variation may be mask misalignment and dopence variations. The fabrication plant can provide a statistical model for the variation and this model can be

used for example in a Monte Carlo simulation. This simulation will do a number of spesified iterations picking out random parameters from this model each iteration. The result will be an statistical model of the circut performance after production.

2.10 Existing Work

There are many exiting low noise amplifiers for CMUT readout both in voltage and current mode and in both continuous time, CT, and discrete time, DT, domain. Solutions with and without variable gain amplifiers,VGA, and in different technologies. There are several solutions like single-ended-to-differential CT VGA [10], [11], [28], solutions with single-ended-to-differential DT VGA[29], single ended CT amplifiers[21] and single ended charge sampling amplifiers [7]. These solutions are made for different CMUT sizes with different senter frequencies intended for different IVUS solutions and so have different specifications.

There are also a difference in the load for the LNAs mentioned above as not all are intended for a system with in-probe DSP.

Interesting comparative work is found in [10], [28]. [28] because it acheives the lowest FoM of the work found and [10] because it uses the same technology.

Chapter 3

Topology and Design

The goal of this work is to design a discrete-time low noise amplifier for a IVUS system. The source for the LNA is a CMUT transducer and the load is ADC in the next stage.

The design focus is to obtain low harmonic distortion and low noise performance to obtain a high resolution outputsignal. Low power consumption is also of importance to reduce the radiated heat.

In the design matlab will be used to model behavior. Cadence Virtuoso will be used for schematic and layout design and spectre for simulations.

3.1 Specifications

The goal specification are given in table 3.1

Parameters	Goal
V_{dd}	$\leq 1\ V$
V_{ss}	$0\ V$
HD_2	$<$-74dB
Center frequency, f_C	$5\ MHz$
Bandwidth (-3dB) f_{-3dB}	$5\ MHz$
Power Consumption	*Low as possibel*
Noise figure, NF	$<3\ dB$

Table 3.1: Specified goals.

The supply voltage given in table 3.1 is set to one voltage to ensure that the maximum input voltage of the ADC is not exceeded. In second harmonic imaging the important distortion term is the second harmonic. To achieve a high resolution in the digital signal used for DSP, without distortion the HD2 goal is set to -74dB. The center frequency of the intended CMUT is 5MHz obtained from the model 3.2.1. And the -3dB bandwidth of the system should be at least 100% of the center frequency which correspond to 5MHz from

2.5MHz to 7.5MHz. The bandwidth is intended to enable the use of harmonic imaging as described in section 3.2.1 in the theory. In front-end receiver LNA it is important to not add to much noise to the signal. Usally the signal-to-noise ratio, SNR, at the LNA output should not be reduced with more than 3dB compared with the SNR at the LNA input. In other words, the added noise from the LNA should be less than the source noise. Therefore the noise figure, NF, should be less than 3dB.

There is no specified gain but to have some gain the CSA will be designed to have a gain around 15dB. The gain will be adjusted to improve other specifications and my be lower or higher than 15dB in the final design.

The LNA should be fully differential and designed in 28nm UTBB FD-SOI technology.

3.2 Charge Sampling Amplifier System

The proposed charge sampling amplifier with the CMUT model is shown in figure 3.1

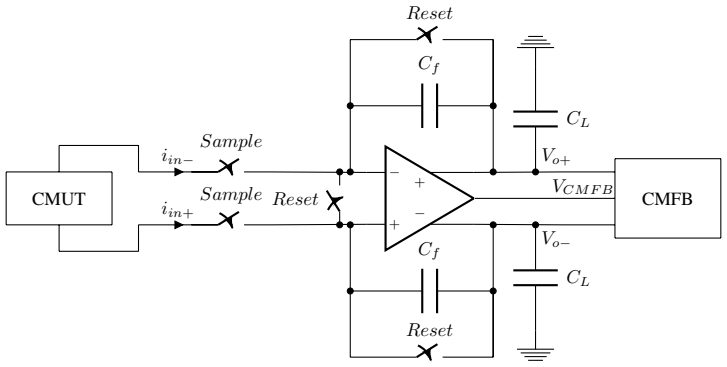


Figure 3.1: The proposed fully differential charge sampling amplifier.

It consists of the CMUT model placed between the input nodes, the sampling and reset switches, an OpAmp, a feedback capacitor, the load capacitor, which models the DAC of the proceeding SAR ADC, and a CMFB circuit. Design of all blocks will be described in following sections.

3.2.1 CMUT model

An electrical small signal equivalent circuit of a CMUT element is shown in figure 3.2

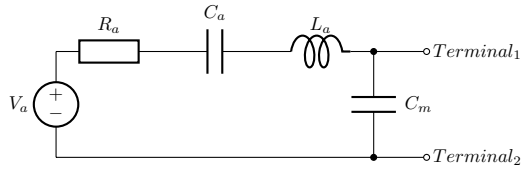


Figure 3.2: CMUT small signal model.

where R_a represents the coupling of acoustic waves between the water in front of the CMUT and the CMUT itself. C_a represents the mechanical stiffness of the mambrane and L_a represents the mass of the membrane and some of the water outside the mambrane. C_m represents the CMUT capacitance which is the capacitance measured between the two CMUT electrodes [7].

In table 3.2 the component values for the CMUT model are given [30], [31].

Component	Value
R_a	$10k\Omega$
C_a	$6.5pF$
L_a	$156\mu H$
C_m	$5.5pF$

Table 3.2: CMUT model values.

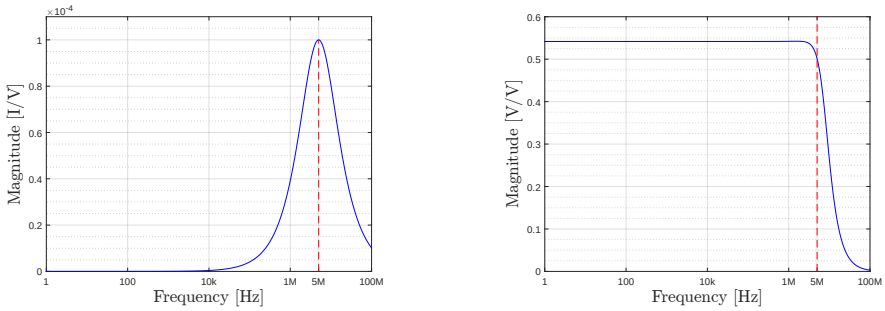
The center frequency for this CMUT model is the frequency at which the imaginary part of C_a and L_a cancels each other as shown in (3.1).

$$\left|\frac{1}{j\omega C_a}\right| = |j\omega L_a| \tag{3.1}$$

If this equation is rearranged center frequency is found in (3.2)

$$f_C = \frac{1}{2\pi}\sqrt{\frac{1}{L_a C_a}} = 4.9981MHz \approx 5MHz \tag{3.2}$$

In figure 3.3 the transfer functions of the CMUT model is plotted. 3.3(a) shows the transfer function when current mode readout circuitry is used. In ideal current mode amplifiers the input impedance is zero and so the parallel capacitor C_m is shorted and the equation is given in (3.3). In figure 3.3(b) the voltage transfer is plotted where the voltage is measured over C_m and voltage readout is assumed where the input impedance of the amplifier is infinitely high. The voltage transfer function is given in equation (3.4).



(a) CMUT current transfer function.

(b) CMUT voltage transfer function.

Figure 3.3: Transfer function of the CMUT model.

As seen from 3.3 an ideal voltage readout circuit gives an asymetric characteristic around 5MHz. Also almost half the signal is lost due to current flowing into C_m while in an ideal current readout the all the current will flow into the amplifier. The transfer function of an ideal current readout circuit shows a peak magnitude at 5MHz, where Z_{C_a} equals Z_{L_a}, and the characteristic is symmetric around the center frequency.

$$|H_I(f)| = \left|\frac{I_i(f)}{V_o(f)}\right| = \frac{2\pi f C_a}{\sqrt{(2\pi f R_a C_a)^2 + (1-(2\pi f)^2 C_a L_a)^2}} \tag{3.3}$$

$$|H_V(f)| = \left|\frac{V_i(f)}{V_o(f)}\right| = \frac{1}{\sqrt{(2\pi f R_a Cm)^2 + (1+\frac{C_m}{C_a}-(2\pi f)^2 C_m L_a)^2}} \tag{3.4}$$

The high source impedance of the CMUT at 5MHz, R_a, and the transfer function shown in 3.3 makes the current mode amplifier topology most suited as the LNA for this CMUT model and was for this reason chosen.

3.2.2 Charge Sampling Amplifier

A current mode topology was chosen for reasons discussed above. The specification also stated that the amplifier should be in discrete time domain. An attractive topology is charge sampling [8]. In addition to relaxed speed demands in the OpAmp, charge sampling lowers the requirements to the sampling switches, compared to voltage sampling, because the voltage at the input node will be almost constant. A single ended charge sampling circuit is shown in 3.4 which consists of an OpAmp, an integrating capacitor, C_f, and two switches for charging- and reset phase.

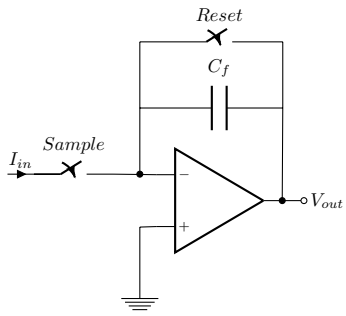


Figure 3.4: A single ended active charge sampling amplifier.

Except for the amplifier, the adjustable parameters in a charge sampling amplifier are the capacitor C_f, the sampling frequency, f_S, the charging duration, Δt_C, and the hold duration, Δt_H.

The sampling frequency is specified in the specifications to 64MHz and should not be changed.

The bandwidth is decided by Δt_C. The smaller Δt_C the higher the bandwidth. The -3dB bandwidth is given by $\frac{0.14}{\Delta t_C}$ 2.5. By setting $\Delta t_c = df_s$ and sweeping d from 0.1 to 0.75 the plot in figure 3.5 is obtained where the x-axis is d and the y-axis is the corresponding -3dB point.

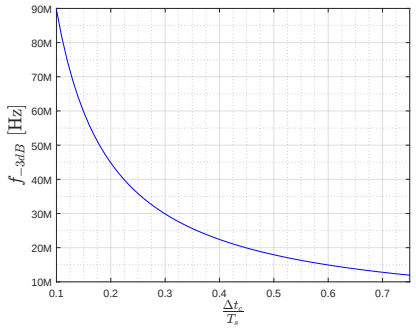


Figure 3.5: Charging duration plotet against -3dB frequency.

Although the plot in figure 3.5 suggests that all values of $\frac{\Delta t_C}{T_s}$ from 0.1 to 0.75 will give sufficient bandwidth that will not limit the transfer function of the CMUT, there also needs to be time for the hold phase and the reset phase.

It was decided to use half the clock periode for charging, $\Delta t = 0.5T_s$ because it gives sufficient bandwidth and higher transfer gain than shorter periode and still leaves sufficient time for reset and hold phases. The hold phase, Δt_h, is set to $0.25T_s$ leaving $0.25T_s$ for the reset phase, Δt_r. The control signals for the sampling switch and the reset switch is shown in figure 3.6. Another reason for using these clock periodes is that they are possible to generate from relatively low complexity logic gate circuits (Appendix E).

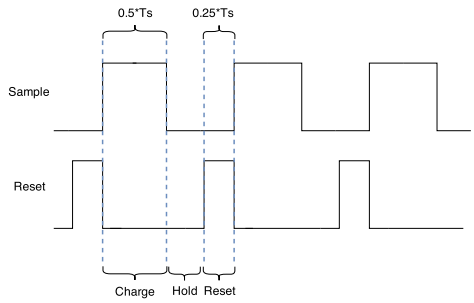


Figure 3.6: Clock phases for the charge samling amplifier.

With a charging periode of $0.5T_S$ the -3dB bandwidth becomes (3.5):

$$f_{-3dB} = \frac{0.14f_S}{0.5} = 17.92MHz \tag{3.5}$$

If the CMUT is the source of the charge sampling amplifier the output voltage is given by (3.6). The calculations are derived in Appendix B

$$V_o(f) = \frac{I_a \Delta t}{C_{eq}} sinc\left(\frac{\omega \Delta t}{2}\right) \tag{3.6}$$

In this equation I_a is the current through R_a, C_a and L_a in the CMUT and $C_{eq} = C_f * (1 + \frac{1}{A_v}) + C_m * \frac{1}{A_v}$ and A_v is the OpAmp gain. The current $I_a = \frac{V_a}{Z_a} - \frac{V_o}{A_v Z_a}$ and so the voltage transfer function from V_a to V_o is given in (3.7)

$$H(\omega) = \frac{V_o(\omega)}{V_a(\omega)} = \frac{\frac{\Delta t}{C_{eq} Z_a} sinc\left(\frac{\omega \Delta t}{2}\right)}{1 + \frac{1}{A_v} \frac{\Delta t}{C_{eq} Z_a} sinc\left(\frac{\omega \Delta t}{2}\right)} \tag{3.7}$$

In addition to charge duration transfer gain is also decided by the size of C_f as seen in (3.7). The smaller value of C_f the larger transfer gain. But C_f will also afffetct the noise characteristics and as stated in (2.44) large C_f gives low noise at the output.

The noise performance of a LNA is usally specified by its NF which is the noise from the source compared to the noise of the system in the same node. If the largest noise is at the amplifier output node a large gain will lower NF. But if the largest noise contribution is at the input node, for example the sampling switches, then lowering C_f to increase gain will not reduce NF. Since it, at this point, is not clear where the largest noise contribution will be C_f will be set to give a gain of 15dB and be adjusted during simulation to achieve small NF. By setting $A_v = \infty$ and solving (3.7) with regards to C_f the capacitor size to obtain 15dB is found in (3.8)

$$C_f = \frac{\Delta t}{10^{\frac{15}{20}} Z_a} sinc\left(\frac{5MHz \Delta t}{2}\right) \approx 135fF \tag{3.8}$$

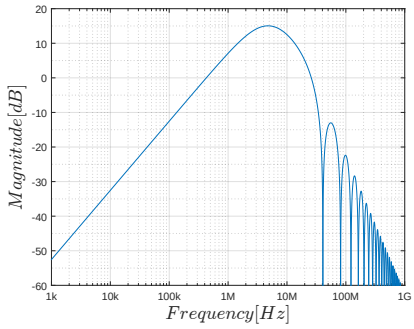


Figure 3.7: Transfer function of CMUT and CS.

The transfer function is plotted in 3.7 where $A_v = \infty$ and $C_f = 135fF$

The plot of the transfer function show that the bandwidth should be from 2MHz to 10MHz and the calculated senter frequency is about 4.9MHz.

During simulation C_f was adjusted to $200fF$ to obatin gain close to 15dB and good noise performance. The resulting clock parameters and capacitor size is listed in table 3.3

Parameter	Value
T_s	$64MHz$
Δt	$0.5T_s$
Δt_h	$0.25T_s$
C_f	$200fF$

Table 3.3: Clock signal duration and capcitor size.

3.3 Noise Analysis of CSA with CMUT load

By using the transfer gain from different nodes in the circuit equations the noise contrebutions of different circuit elements can be arrived. Figure 3.8 shows a single ended version of the circuit in charging phase with noise sources added. It is assumed that the virtual ground reset switch have very high off resistance and thus the noise current is negligible. Also it is assumed that the other reset switches contributes little because the C_f and C_L will filter the noise from the R_{OFF}.

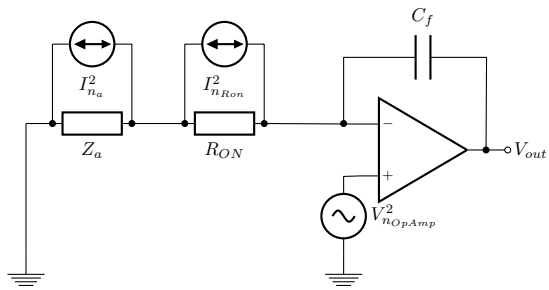


Figure 3.8: Noise Contributions in a CSA with CMUT source.

The noise referred to the output is given in (3.9)-(3.11)

$$V^2_{no_{OpAmp}}(f) = V^2_{n_{OpAmp}}(f)A^2_v(f) \tag{3.9}$$

$$V^2_{no_a}(f) = I^2_{n_a}(f)H^2_I(f) \tag{3.10}$$

$$V^2_{no_{Ron}}(f) = I^2_{n_{Ron}}(f)H^2_I(f) \tag{3.11}$$

where $H_I(f)$ is the current to voltage transfer function given by (3.12)

$$H_I(f) = \frac{\Delta t}{C_{eq}} Sinc(\frac{\omega \Delta t}{2}) \tag{3.12}$$

and $A_v(f)$ is the OpAmp transfer function. The total output referred noise is then given as

$$V^2_{no_{tot}}(f) = (I^2_{n_a}(f) + I^2_{n_{Ron}}(f)H^2_I(f) + V^2_{n_{OpAmp}}(f)A^2_v(f) \tag{3.13}$$

By using the equation for NF (2.40) with all noise referred to the output node of CSA the NF of the system is given by

$$NF(f) = 10log\left(\frac{V^2_{no_{tot}}(f)}{V^2_{no_{CMUT}}(f)}\right) = 10log\left(1 + \frac{I^2_{n_{Ron}}(f)}{I^2_a(f)} + \frac{V^2_{n_{OpAmp}}(f)A^2_v(f)}{I^2_a(f)H^2_I(f)}\right) \tag{3.14}$$

From equation (3.14) it is observed that as long as the OpAmp noise dominates NF can be decreased by increasing the CSA gain. However if the noise from the charging switch dominates increasing CSA gain will have little effect. Low impedance in the input switch is therefore vital to make sure the CMUT noise dominates.

3.4 Design Methology

The design metodology in this work is to achieve low values of FoM_{LNA}. This will be done by designing the OpAmp input transistors with high $\frac{g_m}{I_D}$ to obtain high current efficiency. Relatively large transistors will be used to lower flicker noise, because there is need for sevral capacitors the area consumption of the transitors will have lower impact on the total area as compared to a CT realization. The gain will be adjusted to reduce the OpAmp noise contrebution according to (3.14). The HD_2 will be tried minimized using fully differential designas shown in figure 3.1.

3.4.1 Operational Amplifier

For charge sampling amplifiers many types of operational amplifier can be used as core amplifier. Topologies used for this purpose in existing work are for example the folded cascode OTA [7], [12], [32] and Common source amplifier [33]. The intrinsic gain in 28nm FD-SOI technology is low and so a folded cascoded amplifier would be suited due to relative high gain caused by cascoding. It also has good speed properties because of only one high impedance node. But the cascoding transitors limits the output swing and therefore will add nonlinear components to the output signal when the swing is large. With a specified HD_2 of -74dB it is an advantage to have much ”room” for swing as possible to keep nonlinearities, caused by compression, away from the output signal.

To obtain low noise from the OpAmp a topology with few transistors is desirable. Also, a single stage amplifier with class AB push-pull will be beneficial due to low static power consumption and high slew rate capability.

An interesting topology is a single stage fully differential inverter based amplifier [34] as shown in figure 3.9

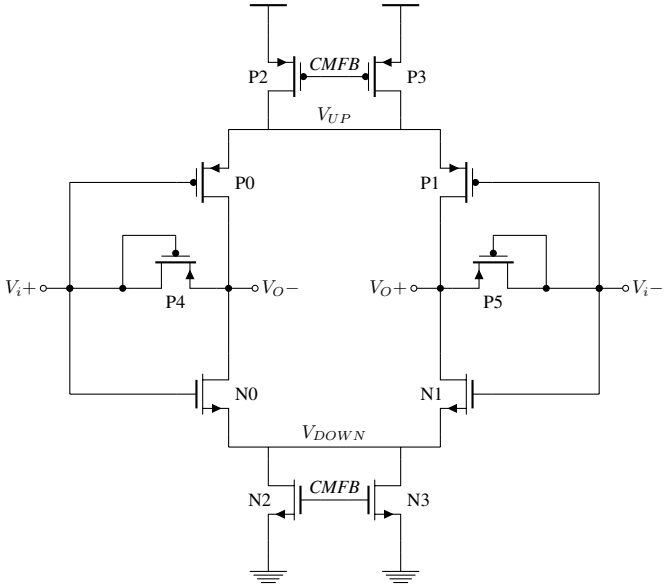


Figure 3.9: Fully Differential Inverter Based Amplifier.

In this amplifier topology transistors N0,P0 and N1,P1 constitutes two inverters. N2,N3 and P2,P3 is used to create a negative feedback loop for the common mode feedback. These four transistors operate in triode region and therefore the voltage drop over them can be very small. This way the two nodes V_{UP} and V_{DOWN} can be designed to be close to the rail voltages [34]. The gates of N2,N3 and P2,P3 will be connected to external discrete time common feedback circuit as will be described later.

The two diode connected PMOS transitors P4 and P5 are used as drain-to-gate feedback resistor biasing. A diode has very high resistance for low voltages across it. This is very suited since the purpose of this scheme is to set the DC-voltage from the output to the intput without allowing current to flow between the input and output node. Therefore a high resistance is needed.

If it's assumed that $R_g \gg r_{ds}$ in (2.26) the equation for the differential gain of the amplifier is given in (3.15)

$$A_{diff} = -(g_{m_{P0}} + g_{m_{N0}})(r_{ds_{P0}} || r_{ds_{N0}}) = -G_m R_{out} \tag{3.15}$$

which is equal to the gain of an inverter (2.18). The equation for the unity-gain frequency is also as for an inverter and given by (2.19).

If the feedback bias transistors are neglected and assumed that the amplifier is symmetrical the figure 3.10 shows the noise sources in the amplifier. The drain-to-gate feedback transitors can be neglected because the current through them will be very small as the drain and gate is connected to the gate of the input transistors and for this reason the noise contribution will be very little.

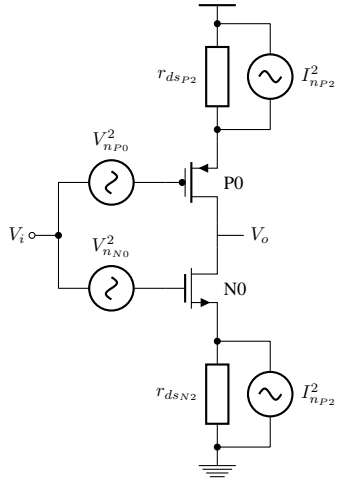


Figure 3.10: The noise model of the left half side of the OpAmp.

The input referred noise is given in (3.16)

$$e^2_{n_{in}} = \frac{(g^2_{m_{P0}} e^2_{n_{P0}}) + (g^2_{m_{N0}} e^2_{n_{N0}}) + I^2_{n_{P2}} + I^2_{n_{N2}}}{(g_{m_{P0}} + g_{m_{N0}})^2} \tag{3.16}$$

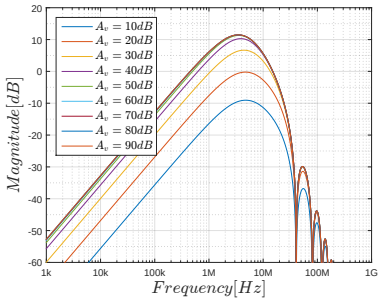
where e^2_n and I^2_n is given in (3.17) and (3.18) as explained in section 2.4.2.

$$e^2_n = \frac{K}{WLC_{ox}f} + 4kT\frac{2}{3}\frac{1}{g_m} \tag{3.17}$$

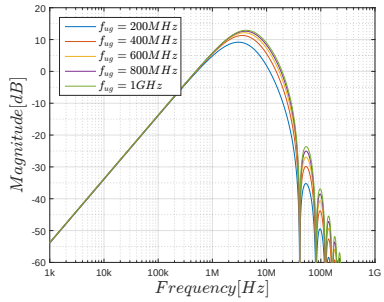
$$I^2_n = \frac{4kT}{r_{ds}} \tag{3.18}$$

From equation (3.16) it is seen that to minimize the input referred noise the transconductance of the input transistors should be high, also, to decrease flicker noise large transistor sizes is beneficial. Large resitance in P2,P3 and N2,N3 will decrease the noise contribution from these transistors which is achievable widt long channel length.

A charge sampling amplifier have the advantage of avoiding voltage settling which, for high linearity applications, may depend on many time constants to settle to a spesified value. Although the voltage settling specifications is relaxed the amplifier should be able to settle in the reset mode and the OpAmp bandwidth may influence the system transfer function. To se how the OpAmp bandwidth and gain effects the transfer function of the system equation (2.27) was used to model A_v in (3.7) by setting $g_m = 2\pi C_l f_{ug}$ and $r_{ds} = {}^{A_{DC}}/_{g_m}$ the gain and f_{ug} was swept in matlab and plotted in figure 3.11.



(a) System transfer function for different OpAmp gain.



(b) System transfer function for different f_{ug}.

Figure 3.11: Influence of nonidealities in OpAmp.

The f_{ug} was seen in 3.11(b) to have influence on the center frequency by lowering it for lower values of f_{ug}. It was found that even if the center frequency dropped to approximately 3.5MHz with a f_{ug} of 450MHz the 5MHz point was just 0.5dB lower than the magnitude at center and the bandwidth was sufficient at 1.5MHz to 7.55MHz arround 3.5MHz in the model. As the f_{ug} had to be several tens of GHz to get the center at approximately 5MHz, 450MHz was chosen because the magnitude at 5MHz diviated little from center and the bandwidth was sufficient.

From figure 3.11 it was seen that the gain had less influence on center frequency and only gave a gain error for the small signal model. As long as there is some gain in the OpAmp and it's linear the gain will have lttle affect on the system. However higher gain gives more feedback through C_f that will help linearize the circuit. It was seen that for gain of about 50dB the gain error is relatively small and will have marginal effect on the system transfer function. Therefore the gain was set to $300^V/_V \approx 50dB$.

The slew rate of the amplifier must be so high that under charging there will not accure any slewing. Slewing will affect the linearity because it is a signal dependent effect. The signal may be as high that the output will reach the rail. Assuming that the output is swinging arround $\frac{VDD-VSS}{2}$ the maximum amplitude, and thus maximum voltage step is 500mV with a 1V supply. The time duration of which the output needs to reach this level is the charging periode of $0.5T_S$. The minimum slewrate is therefore (3.19)

$$SR = \frac{\Delta V}{\Delta t} = \frac{(\frac{VDD-VSS}{2})}{0.5T_S} = 64V/\mu s \tag{3.19}$$

However in the reset phase the amplifier must be able to drive the load from the maximum value down to zero in half the time and so the SR should be $128V/\mu s$.

The load for the OpAmp will be the SAR ADC input capacitance C_{ADC} which is 650fF and the feedback capacitor C_f. The total load capacitance C_L becomes 850fF.

The g_m needed to get a f_{ug} of 450MHz with a load of 850fF is

$$G_m = 2\pi f_{ug} C_L = 2.4mS \tag{3.20}$$

the current needed for a slew rate of $128V/\mu s$ is

$$SR_{MAX} = \frac{I_D}{C_L} \Rightarrow I_D = SR_{MAX} * C_L = 108.8\mu A \tag{3.21}$$

The output resistance becomes

$$R_{out} = \frac{A_v}{G_m} \approx 125k\Omega \tag{3.22}$$

To find the sizes of the input transistors a software tool called $MosDesigner$ developed by Prof. Trond Ytterdal was used. This tools uses the values g_m, $\frac{g_m}{I_D}$, $\frac{g_m}{g_{ds}}$ and V_{ds} as input and returns transistors sizes and point of operation by running the optimizer in cadance in the background.

The g_m for the input pmos and nmos becomes $1.2mS$ if it assumed that both have the same transconductance. This gives a $\frac{g_m}{I_D}$ in each input transistor of

$$\frac{g_m}{I_{D_1}} = \frac{2g_m}{I_D} = 22.06 \tag{3.23}$$

The intrinsic gain is given by (2.1). r_{ds} is, if $r_{ds_n} = r_{ds_p}$, two times R_{out}. The intrinsic gain of the input transistors therefore becomes

$$\frac{g_m}{g_{ds}} = g_m r_{ds} = 300 \tag{3.24}$$

Although the biasing transistors, P2,P3 and N2,N3, will have some voltage across them this was neglected because this voltage will be small. The V_{ds} input in the *MosDesigner* was therefore set to 0.5V assuming that the voltage drop over the nmos and the pmos are equal.

The biasing transistors, P2,P3 and N2,N3, is sized to not limit the current, to have low V_{ds} and high r_{ds} to lower noise as stated in equation (3.16). Also relatively large size is used to minimize the influence of mismatch.

The two bias transistors P4 and P5 should have high r_{DS} and also low parasitic capacitance between drain to source and gate to source. Therfore a small transistor could be used. However a small transistor will be influenced by mismatch more than a large transistor. Therefore pmos with minimum sizes for use of two fingers was diode connected and simulated. It was found that by doubling length and width gave about a hundred times larger resistance at low V_{DS} voltages and half the resistance spread in mismatch runs and less than double the parasitic capcitance. Therfore this size was used. The resulting sizes of the OpAmp after MosDesigner and tweeking in the schematics is given in table 3.4.

Transistor	W (μm)	L (nm)
$N0$	13.56	160
$N1$	13.56	160
$N2$	16	220
$N3$	16	220
$P0$	46.68	160
$P1$	46.68	160
$P2$	40	220
$P3$	40	220
$P4$	0.34	60
$P5$	0.34	60

Table 3.4: Sizes of transistors in the OpAmp.

The resulting resistance in P4 and P5 became $88.87G\Omega$ for low V_{DS} wich gives $R_G \gg r_{ds}$ and so it can be neglected in the small signal calculations.

The resulting OpAmp specifications with the values used in table 3.4 was a $f_{ug} = 470MHz$, gain of $287^V/_V = 49.15dB$ and a current consumption of $110.4\mu A$. The $\frac{g_m}{I_D}$ became 23.1 for the PMOS input transistors and 21.6 for the NMOS transistors.

3.4.2 Common Mode Feedback Circuit

The CMFB circuit used in this work is based on [27] but changed some to work with the implemented OpAmp. A discrete time CMFB circuit was desirable to obtain high output swing which is benefical for high linearity.

The implemented CMFB circuit is shown in figure 3.12

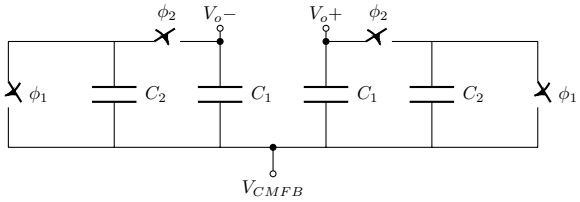


Figure 3.12: Schematic of the CMFB circuit used in this work.

In the charging phase both capacitors are connected to the output and will find the common mode voltage of the output in the V_{CMFB} node according to

$$V_{CMFB} = \frac{Z_{C_{RH}} V_{O-} + Z_{C_{LH}} * V_{O+}}{Z_{C_{RH}} + Z_{C_{RH}}} \tag{3.25}$$

where $Z_{c_{RH}} = \frac{1}{j\omega(C_1+C_2)}$ on the right hand side and $Z_{c_{LH}}$ on the left hand. The capacitance at both side are equal and therefore the $V_{CMFB} = (V_{o+} + V_{o-})/2$. The

ϕ_2 clock phase is equal to the charge phase. In the hold phase the output should not change at all and the common mode should be held constant. Therefore some a part of the capacitance, C_2, is disconnected and reset under the holding and reset phase. C_2 will be reconnected again under the charging phase and some charge will be drawn from C_1 so that capacitance will be charged up by the OpAmp output again.

This way the CMFB always will feedback the common mode voltage back to transistors P2,P3 and N2,N3 in the OpAmp. The transistors P2,P3 and N2,N3 have inverting gain and will decrease the common mode if it is high and increase it if it is low. Hence the CMFB will work almost as a diode connected inverter. The common voltage will strive to be in the middle between the rails and, unlike other CMFB circuits, this circuit cannot controll the common mode to an arbitrary, specified, voltage level. But as the largest swing is obtained for a common mode voltage of $\frac{V_{DD}}{2}$ this circuit will provide large OpAmp output voltage swing.

C_1 is sized to 50fF and C_2 to 150fF. So in the charging phase the total capacitance on each output node is 200fF.

3.4.3 Switches

There where used two types of switches in this work. The switches in the CMFB circuit are implemented as transmission gates with a PMOS and a NMOS in parallel and the switches in the charge sampling circuit is implemented as NMOS switches. The important requirement to switches is on and off resistance and linearity. The switches in the CMFB circuit is sized so that they does not dominate the settling. The highest on resistance of the switch is $1.62k\Omega$ and the lowest off resistance is approximatly 80M.

The switches used for charging and reset consists high voltage IO nmos transitors. The reason is that when the charging switches is turned off the node connected to the CMUT will go from a low impedance node to a high impedance node and so the voltage may exceed the 1V tolerance of the low voltage transistors for a large input signal. The same types of switches is used for reset of C_f because they proved to give higher system linearity and since the input switches uses high voltage transistors a 1.8V clock signal is needed anyway. The higher linearity is most likely due to that the voltage level on the source and drain is further from the on gate voltage than it would be for low voltage switch. Also for this reason it is sufficient with only a nmos transistor and a transmission gate is not needed.

To not influence the charge transfer from the CMUT to the integrating capacitor the charging switch on-resistance is set low to 924.4Ω and to make assure that little charge leaks through the switch when off, the off resitance is $16.41G\Omega$. The reset switches for resetting the integrating capacitors are equal to the charging switches. The reset switch to clamp the virtual ground nodes together under reset must not let charge flow between the two nodes under charging phase and so the off resistance needed to be large. The on resistance is $2.5k\Omega$ and the off resitance is $116G\Omega$.

The sizes of the switches is listed in table 3.5

Switch	Transistor	W (μm)	L (μm)	R_{ON}	R_{OFF}
CMFB Switches	Nmos	0.45	0.03	$1.6k\Omega$	$80M\Omega$
	Pmos	0.45	0.03	$1.6k\Omega$	$80M\Omega$
Charging Switches	Nmos	1	0.15	924.4Ω	$16.41G\Omega$
Reset Switches	Nmos	1	0.15	924.4Ω	$16.41G\Omega$
Clamping Switches	Nmos	0.5	0.3	$2.5k\Omega$	$116G\Omega$

Table 3.5: Sizes of transistors in switches.

3.5 Layout

To extract parasitics like cross-connections and parasitic capacitance to the substrate a layout of the charge sampling amplifier circuit was done. The circuit was divided into subcircuits and layout where done on OpAmp, CMFB circuit and switches separately and then connected together to save time in debugging and fulfilling design rule check. The transitors of the OpAmp is laid out using m-factor of 20 and 2 fingers and by placing the two opposing transitors like P0 and P1 in one area according to the pattern in figure 3.13. This way the mismatch and prosess variation over the area will distribute evenly over all the transistors so that both sides of the OpAmp will be as equal as possible. The transistors P0,P2 and N0, N1 and N2,N3 and P2,P3 are all placed this way.

P0	P1	P1	P0	P0
P1	P0	P0	P1	P1
P1	P0	P0	P1	P1
P0	P1	P1	P0	P0
P0	P1	P1	P0	P0
P1	P0	P0	P1	P1
P1	P0	P0	P1	P1
P0	P1	P1	P0	P0

Figure 3.13: Layout pattern of the OpAmp transistors.

The capacitors are made as MoM capacitors and to use less area four metal layers, M1, M2, M3 and M4 are used. The capacitors are generated by a script developed by Carsten Wulff [30] and are made up from sevral unit capacitors shown in figure 3.14 with overlapping metals in M1, M2, M3 and M4.

The focus in the layout design where on achieving little parasitic cross-connections. This was achieved by routing long parallel wires in different metal layers and with some

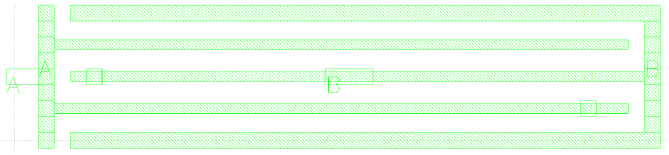


Figure 3.14: Picture of one unit capacitor.

space especially wires connected to the input nodes of the OpAmp. The high gain of the OpAmp will amplify small induced voltages in these two nodes to large voltages at the output nodes which may influence the linearity performance. The full layout is shown in figure 3.15 and the final layout size was $39.8 \times 70.3 \mu m^2$.

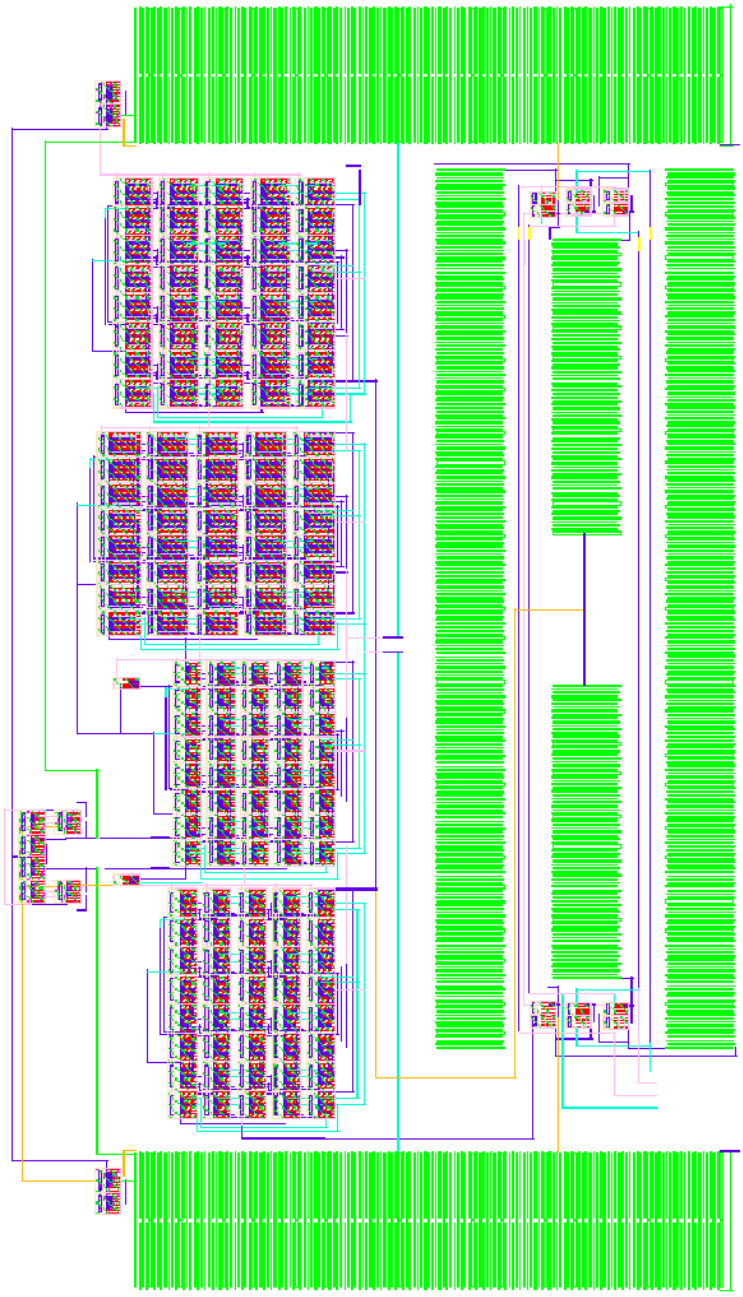


Figure 3.15: Picture of the circuit layout.

Chapter 4

Results

In this chapter the simulated results for the proposed design are presented. The testbench used where set up in Cadence Virtuoso ADE-XL environment and the simulator used where Spectre and Spectre RF. To give as realistic results as possible the presented results are obtained from the Post-Layout circuit with extracted parasitic capacitance.

In this chapter some discussions is also made but more detailed discussions is found in Chapter 5.

4.1 Test Setup

The testbench consits of the CMUT model shown in figure 3.2, the proposed charge sampling amplifier as explained in section 3.2, ideal clock and voltage sources, capacitor loads, a voltage-controlled voltage-source and a verilogA sample-and-hold, S/H, block. The testbench schematic is shown in figur C.1 in Appendix C.

To find realistic rise and fall time for the ideal clocks an inverters fall and rise time was measured. The inverter had transistors of W=160nm and L=30nm and was loaded with another inverter. The measured time was 50ps and thus 50ps was used in the ideal switches.

The load capacitors are 650fF and models the DAC capcitance array of a SAR-ADC.

To measure the differential output voltage, V_o, an ideal voltage controlled voltage source was used with a gain of 1 to subtract V_{o-} from V_{o+} giving $V_o = V_{o+} - V_{o-}$.

The S/H block was used to perform noise and ac analysis in stady state using *Periodic Steady State*, PSS, *Periodic noise*, Pnoise and *Periodic ac*, Pac, analysis. Spectre RF is set up to report the continuous-time behavior and so the idealized S/H is added to get the discrete time behavior. A detailed description is beyond the scope of this investigation and the interested reader can consult [35]. The S/H verilogA code is given in Appendix D and is the same as described in [35].

4.1.1 Small Signal Analysis

The small signal analysis where done with PSS and Pac. The PSS finds a steady state operating point by running a transient of which an ac analysis can be done.

The results is given as the differential output voltage and the input source used is the voltage source V_a in the CMUT model.

4.1.2 Large Signal Analysis

To simulate the large signal performance a transient analysis and *Quasi Periodic Steady State*, QPSS, analysis where used.

The linearity performance where measured by QPSS and confirmed by transient analysis. The power consumption was measured by averaging the current consumption from both voltage domains separatly, calculating power and adding them togheter.

The input impedance was meassured in the charge phase by dividing the differential input voltage on the differential input current.

4.2 Frequency Response

Figure 4.1 shows the small signal transfer function of the proposed CSA in the typical corner with the CMUT model as signal source.

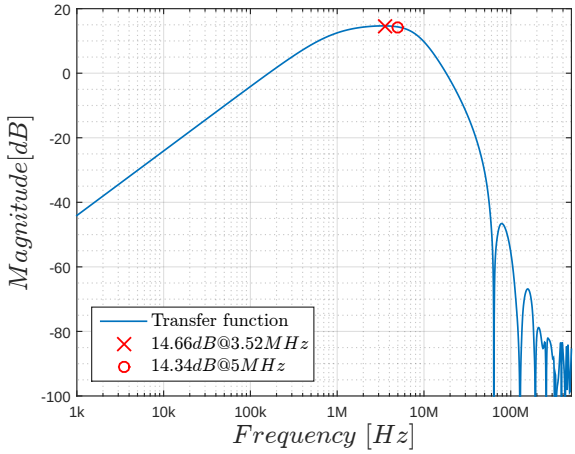


Figure 4.1: Resulting transfer function of the CSA with CMUT model as source.

The highest achieved gain was found at 3.52MHz but the magnitude at 5MHz was only 0.32dB below. The -3dB bandwidth was measured to be from 0.774MHz to 8.68MHz giving a total bandwitdh of 7.91MHz. The voltage gain of 14.34dB is measured from the acoustic source, V_a of the CMUT model shown in figure 3.2.

It was observed that the transfer gain is higher than the calculated gain in equation (3.7). The reason is due to the parallel capacitor C_m and will be discussed in chapter 5.

It is also seen from figure (4.1) that the sidelobes is lower than the observed from the figure 3.7 with ideal OpAmp. The reason is the low-pass charachteristics of the OpAmp transfer function which limits the CSA transfer function in the higher end.

4.3 Biasing Verification

As the CMUTis placed between the input nodes of the the CSA it was interesting to see if the point of operation is held constant over time. The Drain-to-Gate feedback biasing should ensure a stable operating point but if a current flows through it the generated voltage may upset the point of operation.

To ensure that the point of operation is held constant over a relatively long periode of time a 250μs transient simulation was run.

It was found that the point of operation was held constant during the entire simulation. A small transient in the beginning lasting about 250ns was observed before the point of operation was set and held constant.

The DC current through the feedback biasing transistors was also found to be very small and dominated by noise.

4.4 Noise Analysis

The noise performance was simulated in Pnoise and confirmed by transient noise analysis. The noise figure was calculated with spot noise and plot against frequency as shown in figure 4.2. In Pnoise fullspectrum sideband was used and in the PSS the number of output harmonics was set to 5. It where found that increasing number of harmonics from 5 to 50 gave less than 1% increase in input referred noise and the simulation time increased considerably and so number of harmonics was set to 5. V_a was used as *Input Source Port* and the outputs of the ideal S/H, N_{out} and P_{out}, as *output nodes*. The noise was confirmed by integrating the noise power in the frequency band from 2.5MHz to 7.5MHz in both Pnoise and in the CSA output spectrum of a transient run.

It's seen from the plot that NF is 5.79dB at 5MHz. And the noise figure ranges from 5.99dB at 2.5MHz to 7.25dB at 7.5MHz which is the specified bandwidth. The high NF at the higher end of the bandwidth became 1.25 dB higher than the lower end. The reason is that the bandwidth in the OpAmp limits the bandwidth of the system transfer function and thus the gain is not symmetric around the senter frequency and falls of faster in the higher end as was seen in figure 4.1.

The Pnoise analysis can also provide a list containing the circuit elements that contributes with most noise at the output node. The noise from the 10 largest contributers are listed in table 4.1 where the noise is integrated from 2.5MHz to 7.5MHz.

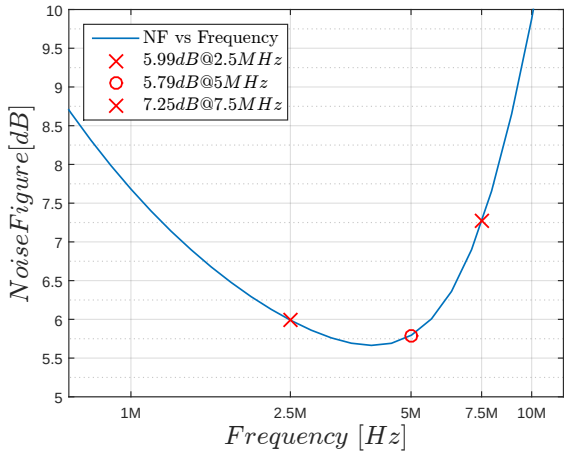


Figure 4.2: The noise figure plotted against frequency

Sub Circuit	Transistor	Contribution	Noise Type
CMUT	R_a	25.24%	rn
Sampling switch +	N	18.92%	Thermal
Sampling switch -	N	18.92%	Thermal
OpAmp	$N0$	10.8%	Flicker
	$N1$	10.8%	Flicker
	$P0$	4.4%	Thermal
	$P1$	4.4%	Thermal
Reset switch -	N	2.14%	Thermal
Reset switch +	N	2.14%	Thermal
Reset switch virtual	N	1.9%	Thermal

Table 4.1: The noise contributions from different circuit elements.

It where found that, after R_a, the input switches where the main noise contributers and so increasing the transfer gain will not give large NF enhancement, according to (3.14), because the main noise arises at the input node.

The noise from OpAmp PMOS input transistors where mainly thermal noise, however in the NMOS input transistors flicker noise dominated. The relatively large size of the PMOS input transistors suppresses the flicker noise according to (2.36).

The SNR was not specified as a goal but it was measured with a -20dB input signal and was found to be 62.16dB, in the frequency band from 2.5MHz to 7.5MHz, at the output node of the CSA with a signal amplitude of -5.59dB.

4.5 Mismatch Performance

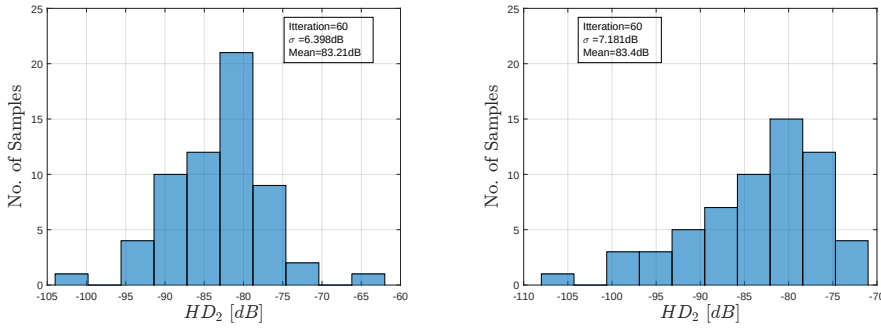
To simulate the mismatch performance of the proposed CSA a Monte Carlo analysis was performed with 60 iterations and it was run with Latin Hypercube sampling method. Monte Carlo was run both from pre and post layout but only when significant differences occurs the pre layout results are presented. Otherwise post layout results are presented.

The mismatch performance in the post layout circuit is given in table 4.2 with mean values, μ, and standard deviation, σ. For linearity simulation an input frequency of 5MHz with an amplitude of 100mV is used which corresponds to a differential, $(V_{out+} - V_{out-})$, output amplitude of 521mV. The simulations was run in the typical process corner.

Parameter	μ	σ	$\lvert\frac{\sigma}{\mu}\rvert[\%]$
BW	$7.896MHz$	$1.26kHz$	0.016
NF	$5.8dB$	$0.011dB$	0.19
$Gain$	$14.34dB$	$0.018dB$	0.13
$Offset, V_o$	$1.137m$	$0.802m$	70.53
$Offset, V_{o+}$	$512.9m$	$0.504m$	0.1
$Offset, V_{o-}$	$512.0m$	$0.584m$	0.11
HD_2	$-83.4dB$	$7.181dB$	8.61
HD_3	$-51.96dB$	$0.138dB$	0.27
Z_{in}	$3.10k\Omega$	$0.16k\Omega$	5.16
$Power$	$110.6\mu W$	$0.512\mu W$	0.46

Table 4.2: Mismatch performance.

Figure 4.3 shows the histograms of the distribution of resulting HD_2 from the Monte Carlo run.



(a) Schematic.

(b) Layout.

Figure 4.3: HD2 Monte Carlo result after 60 iterations.

The plot shows relatively large spread in second harmonic distortion over Monte Carlo iterations both for the schematic before the layout was performed and also in post layout simulations. The layout, figure 4.3(b), showed a larger spread than the schematic, figure 4.3(b), but the mean value is almost equal and just a bit better for the layout with -83.4dB compared to schematic -83.21dB. The standard deviation for the layout simulatin is 7.181dB and for the schematic 6.398dB.

The offset is measured with the differential output signal $V_{out} = V_{out+} - V_{out-}$. It seen that σ is relatively high compared to the mean value. A histogram of the DC offset is shown in figure 4.4

From the histogram it is seen that the majority of the samples is below 1.5mV.

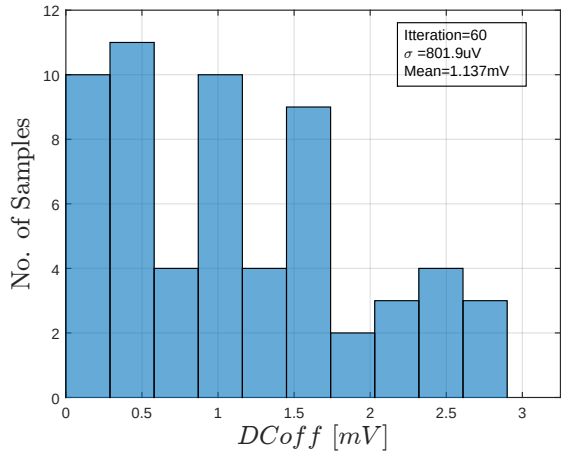


Figure 4.4: Monte Carlo result of differential output offset.

4.6 IIP2 and IIP3

The $^{V_o}/_{V_i}$ characteristics plotted in figure 4.5 is obtained from a single Monte Carlo QPSS run where the input amplitude is swept from -50dB to 0dB and the frequency was set to 5MHz. Figure 4.5 shows the output fundamental frequency magnitude in blue, the second harmonic magnitude in red and third harmonic in black plotted against input amplitude.

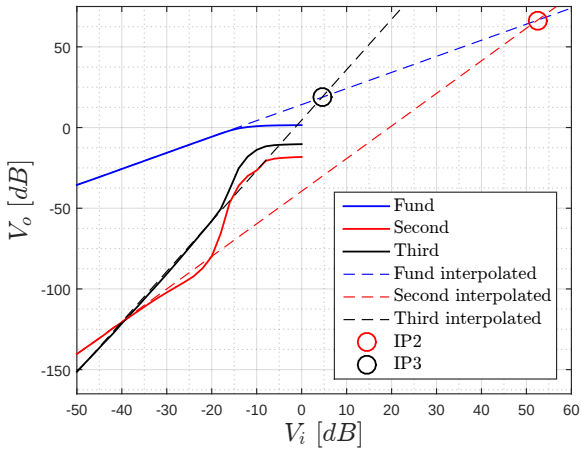


Figure 4.5: Plot of the input output characteristics.

All three graphs was interpolated in MatLab to find the IIP2 and IIP3 points. They where found at 52.45dB and 4.53dB respectively and the corresponding OIP2 and OIP3 at 66.51dB and 18.75dB. The last part of the second- and third harmonic graphs is not considered in the interpolating because the harmonic components increases much faster here because the output starts entering compression. The slope of the second harmonics is 2.02 and the third harmonics 3.13 which is close to the theoretical slopes for second and third harmonic distortion [36] as seen in figure 2.9 in section 2.4.1.

4.7 Process Variation Performance

Different dies will have different properties after manufacturing due to process variations. This is modeled in Cadence Virtuoso with different corner settings. The corners contains settings for temperature, capacitance, resistance and transistor charactheristics. Because the proposed CSA is intended for IVUS the temperature variations will be small because the body temperature is relatively constant. To simulate with some margin the temperature used where from $0°C$ to $60°C$.

In the simulations the highest deviations from the typical performance was found to be for Mos-fast-fast, Mff, and Mos-slow-slow, Mff in the high and low temperature corners. Mff means that PMOS and NMOS is faster than typical and Mss that they are slower than typical.

A nominal simulations where done in the corner simulations. Because there is no mismatch of transistors the HD_2 is very low, at -88.9dB. But the corners will still indicate how the linearity performance is affected by different process variations.

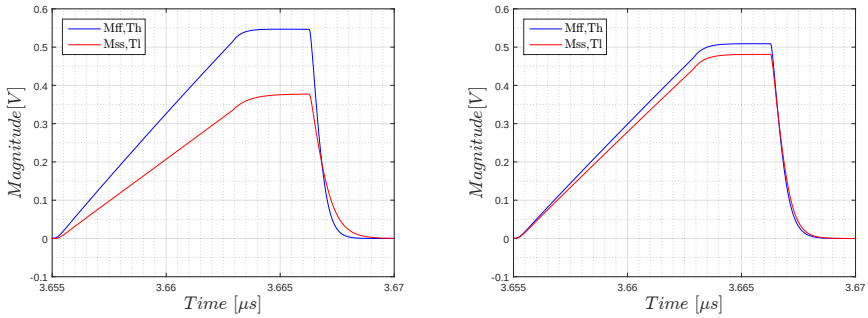
The resulting parameters of the Mss, Mff with both high and low temperature and Typical corners is shown in table 4.3.

Parameter	Mff,Th	Mff,Tl	Mss,Th	Mss,Tl	$Typical$
BW	7.95MHz	7.9MHz	7.89MHz	7.86MHz	7.9MHz
NF	6.04dB	5.12dB	6.61dB	5.74dB	5.79dB
$Gain$	15.5dB	14.48dB	14.15dB	12.73dB	14.34dB
$Offset$	0.95m	0.96m	0.96m	0.97m	0.96m
HD_2	-86.1dB	-87.1dB	-90.1dB	-84.4dB	-88.9dB
HD_3	-49.1dB	-49.2dB	-53.2dB	-46.7dB	-51.21dB
$Power$	178.3μW	98.1μW	129.3μW	66.2μW	110.7μW

Table 4.3: Performance of process variations.

The low current consumption in the Mss,Tl corner gives low transfer gain and the OpAmp f_{ug} is decreased leading to lower settling performance. The output will no longer settle to a constant value in the hold phase as seen in figure 4.6(a). This figure show the output of the CSA in the Mff,Th and the Mss,Tl corner. One reason is that there is not enough bandwidth to handle the sharp edge when the sampling switch is turned off. The Mff,Th has better settling performance due to higher current consumption.

Figure 4.6(b) shows the same corners only with the supply voltage adjusted.



(a) Before VDD adjustment.

(b) After VDD adjustment.

Figure 4.6: CSA output signal over corners.

The result of adjusting supply voltage is more evenly performance over corners. The performance of the five corners with adjusted VDD is shown in table 4.4.

Parameter	Mff,Th	Mff,Tl	Mss,Th	Mss,Tl	$Typical$
VDD	0.975V	1.025V	1.025V	1.005V	1V
BW	7.92MHz	7.93MHz	7.91MHz	7.9MHz	7.9MHz
NF	6.11dB	4.99dB	6.54dB	5.47dB	5.79dB
$Gain$	14.96dB	15.28dB	14.7dB	14.54dB	14.34dB
$Offset$	0.95m	0.97m	0.96m	0.97m	0.96m
HD_2	-87.6dB	-88.9dB	-89.9dB	-88.7dB	-88.9dB
HD_3	-50.3dB	-51.2dB	-53.7dB	-51.7dB	-51.21dB
$Power$	146.0μW	126.2μW	158.1μW	112.6μW	110.7μW

Table 4.4: Performance of process variations with adjusted supply voltage.

All parameters have less variations over corners with VDD adjustment except NF. However, even if the variation is slightly higher the highest NF is lowered 0.1dB and the NF is improved for all four corners except Mff,Th. It is also observed that the variation over temperature is larger than variation over transistor characteristics. And since the temperature variations in a human body is small it is reasonable to assume that variation in performance will be lower when used in IVUS applications.

The results implies that calibration of the supply in an application is needed to achieve higher performance over corners.

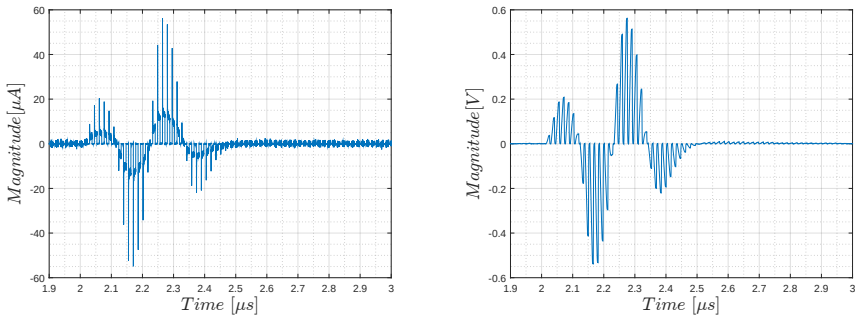
4.8 Ultrasound Pulse Test

The circuit is attended as an ultrasound imaging front-end. In IVUS applications a short-time pulse is usually used to create a broad-band signal spectrum which is transmitted into the body through a tranducer and an echo is received. The echo signal strength is measured and in the DSP and a image is generated.

To test the circuit performance of such a signal a circuit consisting of two CMUT models was used to model a signal transferred from a CMUT and the echo received back. The spectrum of the signal obtained on the receiver CMUTs terminals and the signal obtained after the LNA should have equal shape with higher magnitude in the latter signal.

The testbench, schematic of the two connected CMUTs, the input waveform and waveform out of the transmitting CMUT can be found in Appendix C.1.

The signal obtained on the input and output of the CSA is shown in figure 4.7. Figure 4.7(a) shows the output current of the CMUT which also is the CSA input current. The corresponding CSA output voltage is shown in 4.7(b).



(a) The current signal obtained at the CSA input.

(b) The voltage at the CSA output.

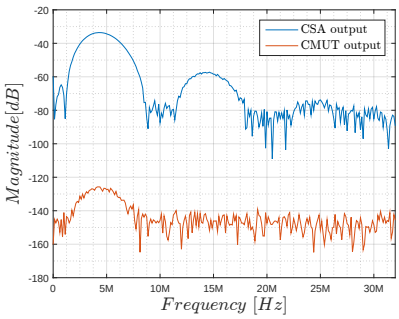
Figure 4.7: Input and output ultrasound signal.

The magnitude of the input current is approximately $14\mu A$ and the magnitude of the output $562mV$ which gives a transimpedance of 40143Ω. This corresponds quite good with the calculations of $\frac{\Delta t}{C_{eq}}$=39063Ω from equation (3.6) in section 3.2.2.

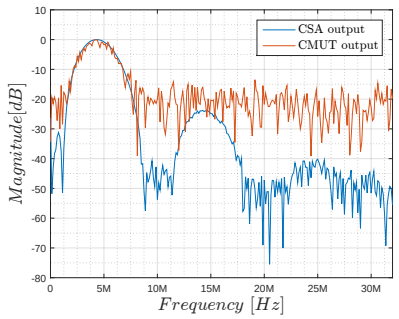
The high spikes observed in the input current occurs when the charging switches opens becuase charge will flow from C_m to C_f to equalizing the difference between them.

In figure 4.8 the spectrums of the CSA input current and output voltage is plotted. There where used 512 samples with a sampling frequency of 64MHz. The input current was sampled from $1.506\mu s$ to $9.506\mu s$ and the voltage from $1.51\mu s$ to $9.51\mu s$. The difference in sampling time is because that the output is most interesting in the holding phase where it can be used in proceeding circuits and not under the charging phase and at this instance the input current is zero.

Figure 4.8(a) shows the spectrums plotted together and 4.8(b) shows the same spectrums only with normalized magnitude.



(a) Spectrum of the input current and output voltage of the CSA.

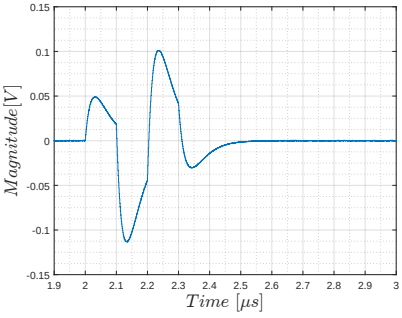


(b) Normalized plot of the frequency spectrum.

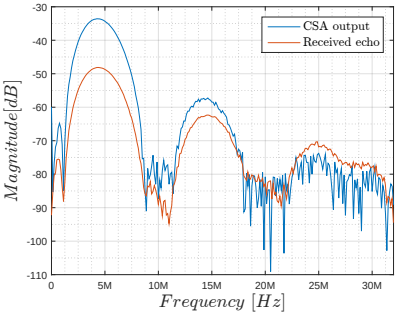
Figure 4.8: The normalized signal spectrums of CSA input and output ultrasound signal.

The short time puls and the low signal magnitude of the input current made it hard to lower the noise floor to obtain details of the spectrum at high frequencies. But it is seen that the main lobe of the CSA input current and the output voltage is very simular which indicates high linearity in the CSA.

To see the CSA influence on the received echo obtained at the transducer, at the acoustic source, V_a, in the CMUT model shown in figure 3.2, the received echo is plotted in figure 4.9(a). This waveform will also be shaped through the CMUT but the spectrum main lobe should be fairly equal to the main lobe of the CSA output because the received echo already is shaped by one CMUT. The spectrums of the received echo and CSA output voltage are plotted togheter in 4.9(b).



(a) The received echo waveform.

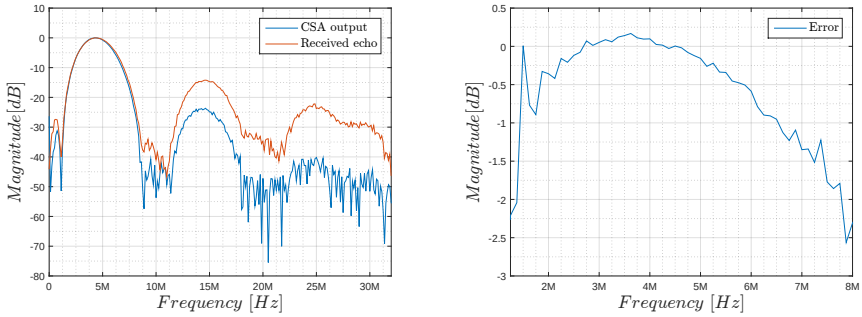


(b) The spectrum of the echo waveform and the CSA output voltage.

Figure 4.9: The received echo waveform.

It is seen that the main lobe is simular and the gain at center frequency is 14.54dB which is equal to the gain measured in the small signal analysis. It is also observed that the gain degrades as frequency increases as expected from the calculated and measured transfer function.

The two spectrums from 4.9(b) is normalized in 4.10(a) and in 4.10(b) and the normalized echo spectrum is subtracted from the CSA output spectrum to se the difference in spectrums in the main lobe.



(a) Normalized spectrums of received echo and CSA output.

(b) The difference between the spectrums.

Figure 4.10: Comparison of the echo spectrum and the CSA output spectrum.

It is seen that the error is higher at the right side of the center frequency. This may be caused by non idealties in the OpAmp, making the transfer function of the CSA to have center frequency a bit lower than the CMUT and that the frequency response fall off faster in the left half of the main lobe.

4.9 Results Summary

The results from the post layout simulations are summarized in table 4.5. The mean value of the monte carlo simulation in the typical process corner are used. For comparison the specifications is also stated in the table.

Parameter	Results	Goals
f_s	$64MHz$	$64MHz$
BW	$7.896MHz$	$5MHz$
NF	$5.8dB$	$< 3dB$
$Gain$	$14.34dB$	-
HD_2	$-83.4dB$	$< -74dB$
$Load$	$2 \times 650fF$	$2 \times 650fF$
$Size$	$39.8 \times 70.3\mu m^2$	-
$ImputImpedance(max)$	$3.17k\Omega$	-
$Power$	$110.6\mu W$	$Minimize$

Table 4.5: Final results for the CSA.

The results shows all specifications except NF is achieved. The physical size was measured on the layout shown in 3.15 as a rectangle that enclosed everything in the layout. The input impedance was measured in the charging periode with sampling switches open at 5MHz input signal.

Chapter 5

Discussion

In this chapter the results and observations will be discussed and compared to design methodology and theory.

5.1 Frequency Response

The frequency response was found to give a center frequency of 3.52MHz as expected from section 3.4.1 where the f_{ug} of the OpAmp was set to give a center frequency of 3.5MHz. The bandwidth was in section 3.4.1 calculated to be between 1.5MHz to 7.55MHz and in the simulated post layout design the bandwidth became 0.774MHz to 8.68MHz. The reason for the 30% increase in bandwidth may be that the switch impedance and input Miller capacitance not where considered in the calculation of the input current. The Miller capacitance will decrease the capacitance seen from the acoustic source V_a giving broader bandwidth of the frequency response.

The measured small signal gain was found to be higher than the calculated gain in section 3.4.1.

Inside the CMUT model,shown in figure 3.2, when the CSA input switch turns off the current from V_a flows down through the large capacitor C_m. The current then charges C_m during the holding and reset phases. When the switch is turned on again all the current from V_a flows into the CSA together with the charge stored in C_m. Therefore the charge from V_a in both charge periode, hold periode and reset periode is delivered to CSA under the charging periode. The charge during hold and reset phase is thus not lost and the total charge put into C_f during charge periode is twice as high and thus the output voltage of the CSA is twice as high as calculated in equation (3.7).

The gain obtained from calculations, with OpAmp limitations added and C_f=200fF, was 8.83dB. Considering twice the output voltage by adding 6dB gives 14.83dB which is fairly equal the simulated gain of 14.34dB.

5.2 Noise

The noise factor at 5.79dB was found to not meet the specified noise goal. It was tried, on the schematic, to increase the transfer gain of the CSA by lowering C_f. It was found that maximum NF was at $C_f = 100fF$ but the improvement was only 0.1dB compared with the NF obtained with $C_f = 200fF$.

The reason is that the input switches contributed with over half the noise in the CSA with $C_f = 200fF$, not including R_a in the CMUT, and since this noise appeared at the input the noise factor did not decrease significant by increasing the transfer gain. Increasing gain also decreases SNR because the input signal must be lowered to maintain same linearity. Although SNR was not a specified goal it will influence signal resolution.

To lower NF further the R_{ON} of the input switches should be decreased making R_{ON} low compared to R_a.

The high NF in the upper end off the bandwidth is most likely due to lower gain. The right side of the pass-band falls off faster than the left side, making the gain at 7.5MHz to be lower than the gain at 2.5MHz and thus, making the OpAmp noise more dominant. However, this is not confirmed. It was seen in the opposite side of the pass band that, the frequency with the same gain as the one found at 7.5MHz, the NF was almost equal only a bit higher most likely due to more flicker noise. This makes the assumption reasonable.

5.3 Mismatch Performance

The mismatch performance of the circuit was fairly good. The reason is the relatively large transistor sizes which according to equation (2.8) gives less mismatch.

The most critical parameter was found to be HD_2 and Offset which is very dependent on the matching of the input transistors. However the HD_2 had a mean value of -83.4dB and only 4 of 60 iterations where higher than -75dB with all 60 iterations under -70dB.

A mean differential offset of 1.14m was found satisfactory considering the theoretical maximum swing of $\pm$VDD. The offset of the two output nodes of approximately 513mV was also found reasonably good although it will limit the maximum positive swing on each output nodes with 13mV. This limits 26mV peak-to-peak voltage on each output nodes if it is assumed that the voltage is symmetrical around the point of operation and therefore lowering maximun differential peak-to-peak swing with 52mV compared to ideal.

5.4 IIP2 and IIP3

From figure 4.5 it is seen that the harmonic distortion slopes is increased drastically when the input magnitude is higher than approximately -20dB. The output of the CSA will from this point start to close in on the voltage obtained in the V_{UP} and V_{DOWN} nodes in the OpAmp shown in figure 3.9. This means that the OpAmp is entering the compression region and the distortion increases. The proposed CSA therefore will have poorer linearity performance for higher output magnitudes than about -5.66dB and to obtain the specified HD_2 higher output swings should be avoided.

The interpolated lines is calculated from the region where the OpAmp compression not yet has occurred.

5.5 Process Variation

The results showed that the proposed CSA is more vulnerable for process variations than mismatch. The power consumption, gain and NF varied especially much over process corners as shown in table 4.3. The variations was compensated to some degree by adjusting the supply voltage, VDD, as shown in table 4.4 but still there where large variations. The highest NF over corners was 6.54dB which is 0.75dB higher than the typical corner.

However, all other parameters satisfies the specified goals for all corners. And as mentioned in the results the temperature inside a human body will be fearly constant making the CSA performance to vary less.

Adjusting the supply demands calibrations of different manufactured circuits and may need additional circuitry for this purpose.

Even though the 28nm FD-SOI transistors is rated for 1V the increased supply voltage should not be a problem. In the OpAmp there are four transistors connected in series so the voltage over each one is less than VDD. Also some voltage will drop over the biasing transistors P2,P3 and N2,N3 so the output shoud not reach rail voltage and thus increased supply voltage of 50mV should not be harmfull for input transistors in proceeding circuits rated for 1V.

5.6 Ultrasound Pulse Test

The ultrasound pulse simulation showed that the distortion from the CSA was almost absent. The spectrum in the band of interest was almost identical for the signal obtained at the CMUT terminals and the CSA output. It was seen, however, that the main lobe in the spectrum of the received echo had a small error in the right side of the main lobe. The reason is probably a combination of non-idealities in the OpAmp and non-zero input impedance.

5.7 Operating point

The operating point was found to not vary over time. The Drain-to-Gate feedback resistor worked as intended and held the point of operation at the input equal that of the output. The output point of operation is held almost in the middel between the rail due to the CMFB ciruit which forces the output common mode to be almost in the middel between the rails due to the negative gain through P2,P3 and N2,N3 which works simular to a diode connected inverter. The reason the output nodes is not exactly in the middle of the rails is because the resistance in all transistors are not excatly equal.

5.8 Comperison with existing work

To compare the proposed CSAs performance to exisiting work the FoM stated in equation (2.48) is used. This gives the power efficiency of the CSA compared to other front end LNAs design for IVUS applications. Four existing works was compared only one of which is in DT and three in CT. The comparison is done in table 5.1

Parameter	This work	[10]	[28]	[29]	[37]
$f_s[MHz]$	64MHz	CT	CT	30MHz	CT
$NF[dB]$	5.79	9.26	2.98	2.87*	3
$HD2[dB]$	-83.4	-48.7	-56.6	-61	-65**
$Power[\mu W]$	110.6	16	67.2	140	80
$BW[MHz]$	7.896	8.3	11.3	4	10
$Size[\mu m^2]$	2798	150	375	17876	8000
$Technology$	28nm	28nm	65nm	0.18μm	65nm
$FoM_{LNA}[fJ*(\mu m)^2]$	0.679	32.9	9.7	962.4	40.4

*IRN was $8nV/sqrtHz$(NF calculated assuming CMUT as source)
** HD_2 given by [38]

Table 5.1: Comparison with existing work.

The FoM_{LNA} of the proposed CSA is lower than for the other compared work. The main reason is the the low HD_2 which is far lower than for [10], [28] and [29]. Also the work presented in this rapport only has one gain setting while the work compared all have variable gain which may add noise, complexity and power consumption. The area and power consumption is higher than [10] and [28] wich both are single ended to differential amplifiers in CT. [10] is an interesting comparison since it's in the same technology and also have higher NF than 3dB.

5.9 Topology

The topology chosen was done considering the relatively high source impedance. By using a fully differential topology and biasing by Drain-to-Gate Feedback resistor high second harmonic suppression was achieved. The second harmonic term was much lower than observed in single ended input LNAs used for CMUT applications for example [28] or [12]. However the charging switches contributed with a fear amount of noise making NF lowerthan about 5.75dB hard to reach. A continuous time realization of a low input impedance fully differential current mode amplifier might give better NF performance. However in terms of FoM_{LNA} given by equation (2.48) the proposed CSA has a high overal performance.

5.10 Layout

The main focus in the layout design was to achieve low parasitic connection between devices and wiring. Therefore there is relatively much space between lines and devices leading to larger area consumption than necessary. Post layout simulations did not revealed any problematic cross connections and thus the layout could be designed more compact.

Chapter 6

Conclusion

In this work a charge sampling amplifier, CSA, with a Capacitive Micromachined Ultrasonic Transducer, CMUT, model as source has been designed in 28nm FD-SOI CMOS technology and analysed. The proposed CSA was intended as a front-end readout LNA, sensing signals from a CMUT transducer generated from a ultrasound echos, and providing a amplified version for a high accuracy ADC to convert them to digital values.

In the design the focus was mainly on achieving high accuracy by low noise figure and high linearity while consuming low power. Therfore an theoretical model for transfer function and noise was used under design.

The proposed CSA achieved a bandwidth of 7.9MHz around a center frequency of 5MHz with a gain at center frequency of 14.34dB and a input impedance of $3.1k\Omega$. High linearity of $HD_2 = -83dB$ and a relatively low power consumption of $110.6\mu W$ was achieved with an area consumption of $39.8\times70.3\mu m^2$. The noise figure, NF, of 5.79dB was higher than the specifications but considering all parameters the proposed CSA performed well compared to other existing LNA implementations for CMUT signal readout.

A capacitive parasitic extraction where done and results from simulation of the layout with paracitic extraction are presented as final results. Simulations of mismatch and process variation are performed to find the performance of manufacturing variations and enviroment influence. The proposed CSA performed relatively well on mismatch due to the use of large transistors. Over processs corners however there where more variation and NF, power consumption and gain was somewhat effected. It was found that the variation could be confined by adjusting the supply voltage by approxematly $\pm$50mV.

To simulate the influence the CSA had on a ultrasound signal two CMUT models was used together with the proposed CSA to model the signal chain from a transmitted signal to the signal delivered to an ADC. The CSA was found to perform well in this setting.

Although the noise figure was higher than the specified goal the proposed CSA had a good overall performance something a FoM_{LNA} of $0.7fJ(\mu m)^2$ indicates.

6.1 Further Work

There where found some issues which should be addressed further. The main issue is the NF which should be improved. It was found that the main noise source was the input switches and so these should be redesigned to enhance NF. Also all other compared works have variable gain to ensure that the output signal of the LNA is within a range that the ADC can handle. The proposed CSA does not have variable gain and this should be implemented if the CSA sholuld by used in a realized application. Variable gain can be implemented by varying the charge duration but this will increase the complexity of clock generating circuitry. Another solution is by using a capacitive array where capacitors of different sizes can be connected and disconnected to give an adjustable value of C_f.

The layout also have potential for improvement. It was seen in the layout that there where much unused space between subcircuits and capacitors and therefore it should be possible to decrease area by reshaping capacitors and putting sub-circuits closer together. Also before the layout is tape-out ready work as parasitic extraction of resistance and inductance and ESD protection should be done.

Also the load used was a passive capacitance, but the circuit should be simulated with a realized ADC as load which may influence the performance.

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Appendix A

Calculations

A.1 Drain-to-Source Feedback Resistor Biasing

Figure A.1 shows a small signal equivalent of the circuit 2.7.

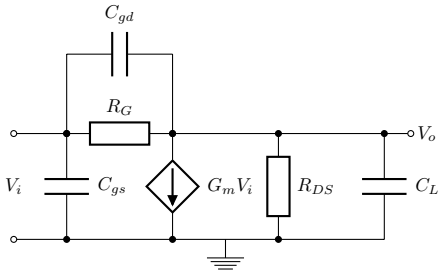


Figure A.1: MOSFET inverter with feedback biasing resistor.

Following is the calculation of the transfer function to the inverter with drain-to-gate feedback resistor.

$$I_{gd} = \frac{V_o - V_i}{Z_{gd}} \tag{A.1}$$

$$I_G = \frac{V_o - V_i}{Z_G} \tag{A.2}$$

$$I_{gs} = \frac{V_i}{Z_{gs}} \tag{A.3}$$

$$I_{g_m} = G_m V_i \tag{A.4}$$

$$I_L = -\frac{V_o}{Z_L} \tag{A.5}$$

$$I_{DS} = -\frac{V_o}{Z_{ds}} \tag{A.6}$$

$$I_o = I_{g_m} + I_G + I_{gd} \tag{A.7}$$

$$\begin{aligned} V_o &= -I_o Z_o = -(I_{g_m} + I_G + I_{gd})(Z_{ds} || Z_L) && \text{(A.8)} \\ &= -(G_m V_i + \frac{V_o - V_i}{Z_G} + \frac{V_o - V_i}{Z_{gd}}) * \frac{Z_{ds} Z_L}{Z_{DS} + Z_L} && \text{(A.9)} \end{aligned}$$

by rearranging (A.8)

$$\begin{aligned} \frac{V_o}{V_i} &= -\frac{G_m Z_G Z_{gd} - Z_{gd} - Z_G}{\frac{Z_{DS}+Z_L}{Z_{DS} Z_L} * Z_G Z_{gd}} && \text{(A.10)} \\ &= -\frac{G_m R_G \frac{1}{j\omega C_{gd}} - \frac{1}{j\omega C_{gd}} - R_G}{\frac{R_{DS} + \frac{1}{j\omega C_L}}{\frac{R_{DS}}{j\omega C_L}} * \frac{R_G}{j\omega C_{gd}} + \frac{1}{j\omega C_{gd}} + R_G} && \text{(A.11)} \\ &= -\frac{-j\omega R_{DS} C_{gd} + (G_m R_{DS} - \frac{R_{DS}}{R_G})}{j\omega R_{DS}(C_L + C_{gd}) + (1 + \frac{R_{DS}}{R_G})} && \text{(A.12)} \end{aligned}$$

which, if only the magnitude is considered, becomes:

$$|A_{AC}|^2 = \frac{(\omega R_{DS} C_{gd})^2 + \left(G_M R_{DS} - \frac{R_{DS}}{R_G}\right)^2}{(\omega R_{DS}(C_L + Cgd))^2 + \left(1 + \frac{R_{DS}}{R_G}\right)^2} \tag{A.13}$$

and by setting the frequency equal to zero and take the squareroot the DC gain is given by:

$$A_{DC} = -\frac{G_M R_{DS} - \frac{R_{DS}}{R_G}}{1 + \frac{R_{DS}}{R_G}} \tag{A.14}$$

The unity gain frequency is found by setting (A.13) equal 1 and solving for $\omega = 2\pi f$ and is given by:

$$f_{ug} = \frac{1}{2\pi} \sqrt{\frac{G_M^2}{C_L^2 + 2C_L C_{gd}} - \frac{G_M}{2R_G(C_L^2 + 2C_L C_{gd})}} \tag{A.15}$$

Appendix B

Transfer function calculation of charge sampler with CMUT model

Calculations of the charge sampling amplifier with the CMUT model as source. The voltage source is the acoustic source of he CMUT, V_a shown in 3.2. C_{eq} is the equivalent input capacitance of the charge sampling amplifier given by $C_f(1+\frac{1}{A_v}+\frac{C_m}{A_v})$ where A_v is the OpAmp open loop DC gain.

$$V_{out}(nT+t_2) = -\frac{1}{C_{eq}}\int_{nT+t_1}^{nT+t_2} I_{in(t)dt} \tag{B.1}$$

$$= -\frac{1}{C_{eq}}\int_{nT+t_1}^{nT+t_2} I_a sin(\omega t)dt \tag{B.2}$$

$$= -\frac{I_a}{C_{eq}}\left[\frac{-cos(\omega t)}{\omega}\right]_{nT+t_1}^{nT+t_2} \tag{B.3}$$

$$= -\frac{I_a}{C_{eq}}\left(\frac{cos(\omega(nT+t_2))-cos(\omega(nT+t_1))}{\omega}\right) \tag{B.4}$$

$$= -\frac{I_a}{C_{eq}}\left(-\frac{2sin(\frac{\omega}{2}(t_1-t_2))sin(\omega(nT+\frac{t_1+t_2}{2}))}{\omega}\right) \tag{B.5}$$

$$= -\frac{I_a}{C_{eq}}\left(\frac{sin(\frac{\omega}{2}(t_1-t_2))sin(\omega(nT+\frac{t_1+t_2}{2}))}{\frac{\omega}{2}}\right) \tag{B.6}$$

$$\overset{\Delta t = t_2 - t_1}{=} -\frac{I_a\Delta t}{C_{eq}}\frac{sin(\frac{\omega}{2}(\Delta t))}{\frac{\omega}{2}\Delta t}sin(\omega(nT+\frac{t_1+t_2}{2})) \tag{B.7}$$

$$= -\frac{I_a\Delta t}{C_{eq}}sinc(\frac{\omega}{2}(\Delta t))sin(\omega(nT+\frac{t_1+t_2}{2})) \tag{B.8}$$

The fourier transform magnitude of the equation above is given in

$$|V_o(\omega)| = |\mathcal{F}\{V_{out}(t)\}| \tag{B.9}$$

$$= \frac{V_a(\omega) - \frac{V_0(\omega)}{A_v}}{Z_a} \frac{\Delta t}{C_{eq}} sinc\left(\frac{\omega \Delta t}{2}\right) \tag{B.10}$$

where $I_a = (V_a - V_o/A_v)/Z_a$ and Za is the acoustic elements in the CMUT, $R_a, C_a and L_a$. By solving equation (B.9) the transfer function is found as

$$H(\omega) = \frac{V_o(\omega)}{V_a(\omega)} = \frac{\frac{\Delta t}{C_{eq} Z_a} sinc\left(\frac{\omega \Delta t}{2}\right)}{1 + \frac{1}{A_v} \frac{\Delta t}{C_{eq} Z_a} sinc\left(\frac{\omega \Delta t}{2}\right)} \tag{B.11}$$

Appendix C

Testbench

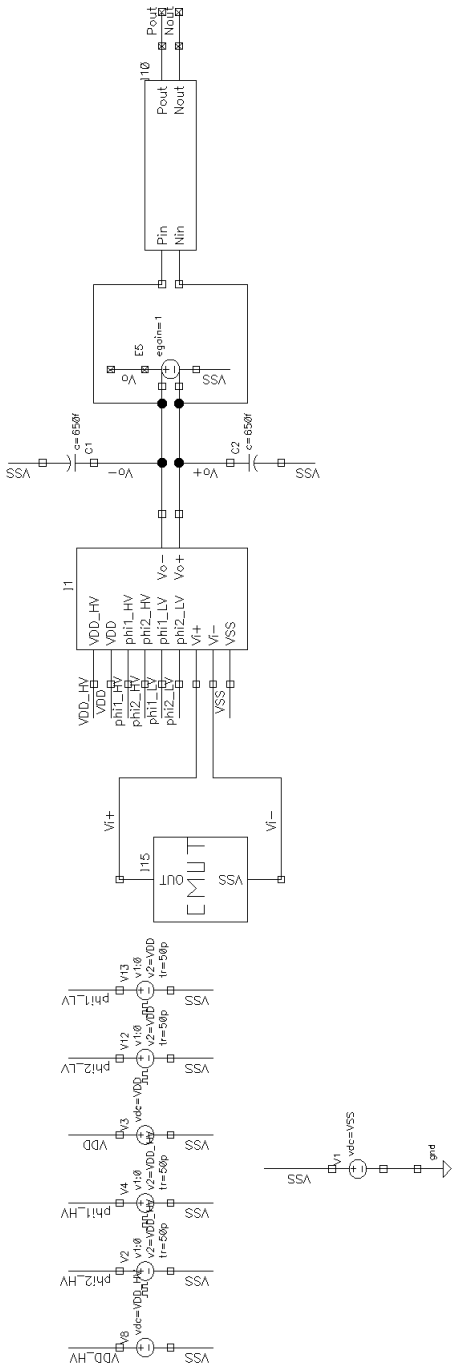


Figure C.1: The testbench used under simulations.

C.1 Ultrasound Pulse model and Waveforms

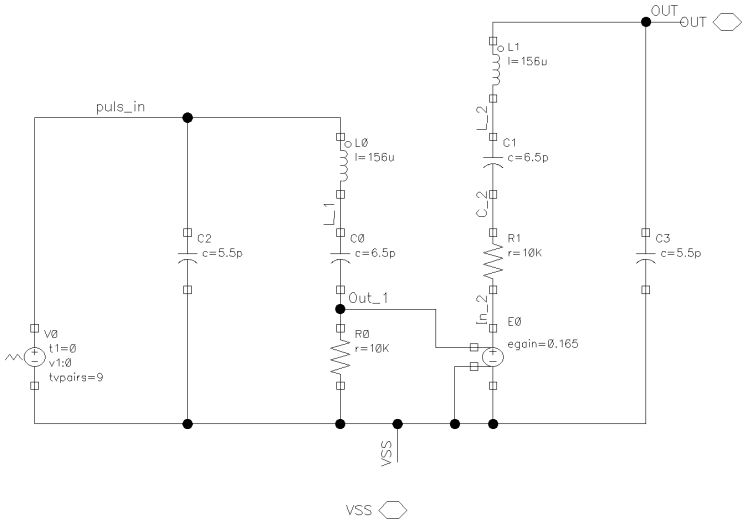
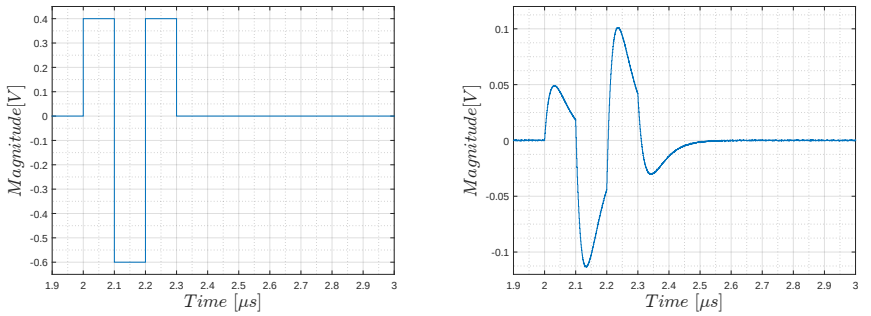


Figure C.2: Ultrasound Pulse model



(a) Waveform at the ”pulse_in” node

(b) Received echo: Waveform at the ”In_2” node

Figure C.3: Waveforms in ultrasound pulse model

Figure C.4 shows the spectrum of the transmitted waveform shown in figure C.3(a) and the received waveform shown in figure C.3(b).

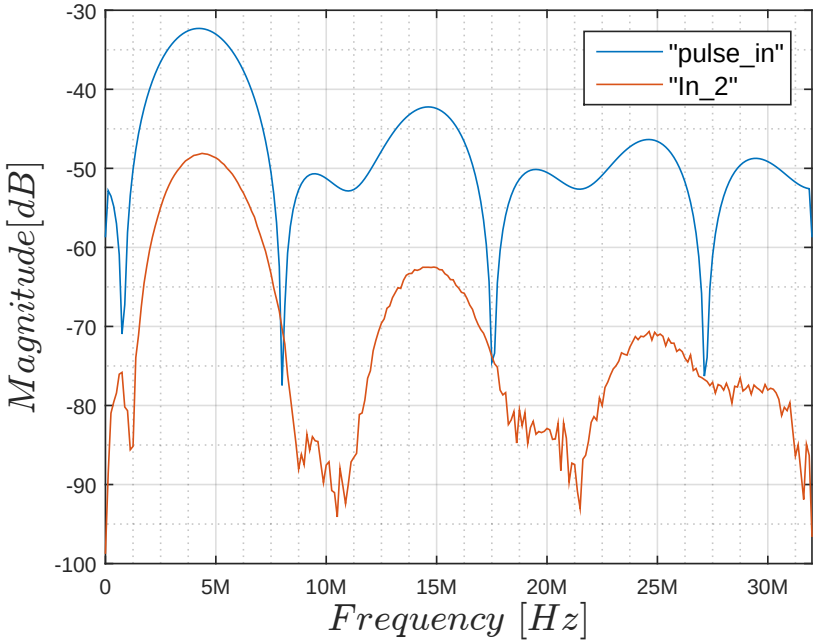


Figure C.4: Spectrum comperison of the transmitted signal at node ”pulse_in” and signal at ”In_2” nodes.

Appendix D

VerilogA Sample and Hold

```
//Periodic Sample & Hold

`include "discipline.h"
`include "constants.h"

module sh_ideal(Pout,Nout,Pin,Nin);
input Pin, Nin;
output Pout, Nout;
electrical Pin, Nin, Pout, Nout;
parameter real period=1 from (0:inf);
parameter real tdelay=0 from (0:inf);
parameter real aperture=period/100 from (0:period/2);
parameter real tc=aperture/10 from (0:aperture);

integer n;
real tstart, tstop;
electrical hold;

analog begin

//Determine the point where theaperture begins
n= ($abstime - tdelay + aperture) / period + 0.5;
tstart = n*period + tdelay;
@(timer(tstart));

//Determine the time where the aperture ends
n = ($abstime - tdelay)/period + 0.0;
tstop = n*period + tdelay;
```

```
@(timer(tstop));

//Implement switch with effective series resistance of 1 Ohm
if (($abstime > tstop - aperture) && ($abstime <= tstop))
I(hold) <+ V(hold) - V(Pin, Nin);
else
I(hold) <+ 1.0e-12 * V(hold);

//Implement capacitor with an effective capacitance of tc
I(hold) <+ tc * ddt(V(hold));

//Buffer output
V(Pout, Nout) <+ V(hold);

//Control time tightly during aperture and loosely otherwise
if (($abstime >= tstop - aperture) && ($abstime < tstop)) begin
$bound_step(tc);
end else begin
$bound_step(period/5);
end
end
endmodule
```

Appendix E

Clock Phase Logic

A possible circuit solution for generating the 25% duty cycle reset phase and the charging phase is shown in figure E.1. In figure E.1 A is the reset phase, B is the charge phase and Phi is the 50% duty cycle main clock. This circuit is not implemented in this work.

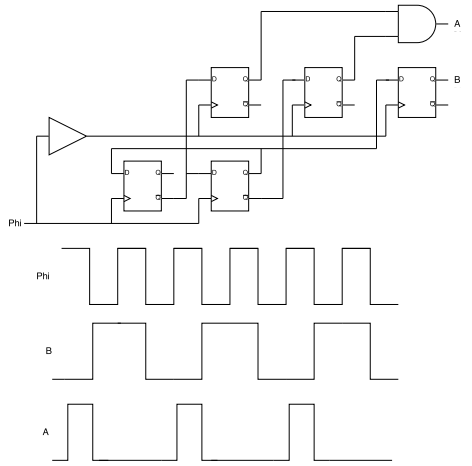


Figure E.1: A possible circuit implementation to generate reset and charge phases.