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Ultra low voltage combinatorial logic building blocks

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Preface

This document is a report of a Master's thesis in electrical engineering performed at NTNU, as part of the study program *Electronics Systems Design and Innovation*. The project was performed during the autumn semester of 2014. This project was inspired by the research paper *Modular Layout-friendly Cell Library Design Applied for Subthreshold CMOS* [1], and the project description was specified with the aid of Prof. Snorre Aunet, Prof. Trond Ytterdal and P.H.D-stip. Ali A. Vatanjou. This thesis was written for NTNUs Department of Electronics and Telecommunications.

It is assumed that the reader of this document has basic knowledge about electrical engineering, specifically within the fields of digital design and implementation.

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Abstract

In this project the three logical gates inverter, 2-input NAND and 2-input NOR was created. Each gate was implemented with two different topologies. All gates created were able to operate with a supply voltage below the transistors threshold voltage. Due to this, the gates created in this project can be called sub-threshold logical gates. To ensure that all voltages were sub-threshold a brief investigation of the transistors were performed, to determine some of the transistor characteristics.

All gates were created at a schematic level and they were tested with both DC and transient analyses. The analyses were performed on different transistor sizes and with different supply voltages, to uncover how transistor gate sizes and supply voltage affects the logical gates. The different gate topologies were compared to each other, and a body biased gate was compared to unbiased gates.

The results from the simulations performed showed that it is possible to make logical gates operate at sub-threshold voltages. The ultra low voltage caused the gates to be prone to noise, process variations, have a large gate area and large delay. Using alternative gate topologies and different gate sizes can mitigate delay and process variations, but will also take up a larger gate area and consume more energy. By using body biasing the gate area and energy consumption could be decreased without affecting gate balance, noise margins and process variations.

The main method for testing the devices in this project has been to run large parametric analyses covering a wide variety of transistor sizes and supply voltages. This method have resulted in a thorough, but time consuming investigation. Because of this the scope of this project was limited to theoretical schematic analyses, and layout with parametric extractions were not included.

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H.S.

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1. Introduction

As technology is entering the era of the Internet Of Things (IOT) the need for ultra low power hardware is increasing. Many everyday items such as power switches, light bulbs, blinds, thermometers and appliances can now be controlled over the Internet from smart phones and tablets. In order to achieve this, these items have integrated processors with TCP/IP compatibility. Some items harvest the extra energy needed to operate a processor from the power grid, others are depending on battery power. To extend the lifetime of the battery, the hardware must consume as little power as possible.

A strategy for making hardware consume less power is to enable *sleep mode*. In *sleep mode* most of the device is shut off, and will therefore consume only a small amount of power. The device is periodically woken up from *sleep mode* to do its tasks, before it goes back to *sleeping*. A thermometer for example hanging outside a building, sends the temperature to a receiver inside the house. Measurements does not need to be taken more than once every minute, or maybe even once every hour. The parts of the thermometer that measures temperature and sends it to the receiver needs to be active at very short periods. The rest of the time, the device can stay in *sleep mode*.

The main objective of a sleep mode circuit is to consume as little power as possible. Speed and performance are secondary compared to power consumption. An easy way to reduce the power consumption, is to reduce the circuits supply voltage. Reducing the voltage below the transistors threshold voltage (sub-threshold) will greatly reduce the power consumption, but will also reduce the performance of the circuit [2]. However, for nodes in the Internet of Things that spends most of its time in sleep mode, performance is not as important as a low power consumption.

To create sub-threshold circuits basic building blocks are needed. Sub-threshold has been around for some decades[3], but it is mostly used for analog purposes. The basic building blocks needed for digital circuits is still in an early stage. This project contributes to further investigate and develop basic logic gates that are able to operate at sub-threshold voltages.

1.1 Project description and specification

In this project logical gates were made with transistors from the *cmos32lp* 28nm FD-SOI library provided by Circuits Multi Projets (CMP). The gates were able to operate at sub-threshold voltages. They were built using both traditional and alternative topologies. The performance of the topologies were compared to each other. The 28nm gates were also compared to similar gates made with NTNUs 65nm CMOS technology. The project is titled: **Ultra low voltage combinatorial logic building blocks**

Here are the project specifications:

- By using cells from the *cmos32lp* library, the following gates were created:
 - 2T Inverter
 - 4T Inverter
 - 4T NAND
 - 8T NAND
 - 4T NOR
 - 8T NOR
- All gates were able to operate at sub-threshold voltages
- The performance of the different topologies were be compared to each other based on the following metrics:
 - Gate balance
 - Noise margins
 - Power
 - Delay
 - Process variations
- How body/ bulk biasing affects the metrics above were investigated.

1.2 Purpose and scope of the project

The purpose of this project was to acquire a library of standard logical cells that were able to operate at sub-threshold voltages, and provide documentation on the performance of these cells. This library consists of the logical gates listed above. This project gives an indication on how different gate topologies and manufacturing processes affects the performance of the cells. The cells created and the simulation results are intended as a contribution to further development of sub-threshold logic.

In this project the characteristics of the transistors *nfet_b* and *pfet_b* from the *cmos32lp* library were investigated. Based upon this investigation, the schematics of the logical cells were created. Test benches were created to test the metrics in the list above for different transistor gate dimensions. The results were used to decide final sizes for all the logical gates. All circuits were created using the EDA tool *Cadence Virtuoso*, and all simulations were done using *Spectre*. Graphs and tables were evaluated using *Excel*.

1.3 Goal and expected results

The main goal in this project was to push the voltage as low as possible. The logical gates had to be able to operate at satisfactory level, but reduction of supply voltage was prioritized before performance. It has been speculated in that the lowest practical voltage is 100mV[4]. Of course this statement was put to the test, and most simulations in this project were performed in the 100mV area.

“..to allow for some tolerance to process and design margins, operation at VDD 100 mV may prove a practical lower bound.”

— *Nowak, IBM, 02*

Some research has been done on how 4T NAND2 compares to 8T NAND2. According to the paper *Modular Layout-friendly Cell Library Design Applied for Subthreshold CMOS* [1], an 8T topology will have reduced speed compared to a 4T topology, but the average power consumption will stay almost the same. The 8T NAND will have a lower statistical variation, and can be a tool mitigating the effects of process variations.

1.4 Word list

σ Standard deviation

2T 2 Transistor

4T 4 Transistor

8T 8 Transistor

GB *Good Balance*

L Length of the transistor gate

Mean Arithmetic mean/ Average value.

NAND2 2 input NAND gate

NOR2 2 input NOR gate

PDP Power Delay Product

SP_x X-coordinate of the Switching Point

V_{DD} Positive supply voltage.

VNM Noise margin

VNM_H Higher Noise margin

VNM_L Lower Noise margin

V_{TH} Threshold voltage

W Width of the transistor gate

1.5 Structure of this document

In this report the following chapters are included:

- **Chapter 1** gives an introduction and a presentation of the main topics of this report
- **Chapter 2** is some theoretical background specific for this project
- **Part I: Investigate the transistor characteristics, contains the investigation of the transistors**
 - **Chapter 3** presents the method for testing the transistors
 - **Chapter 4** contains simulation results of the inverters
 - **Chapter 5** is a discussion of the results presented in chapter 4
- **Part II: Schematic design of the logical gates, contains the description on creation and testing of the logical cells at schematic level**
 - **Chapter 6** presents the creation of the schematics of the logical cells and the test benches
 - **Chapter 7** contains simulation results of the logical cells on schematic level
 - **Chapter 8** is a discussion of the results presented in chapter 7 and the method presented in chapter 6
- **Chapter 9** presents a conclusion of the work done
- **Appendix A** contains the schematics of gates and test benches
- **Appendix B** contains tables of some of the simulation results

2. Theory background

2.1 Logic gate topologies

Here are the topologies that used in this project.

- 2 transistor inverter: figure 2.1.
- 4 transistor inverter: figure 2.2.
- 4 transistor NAND2: figure 2.3.
- 8 transistor NAND2: figure 2.4.
- 4 transistor NOR2: figure 2.5.
- 8 transistor NOR2: figure 2.6.

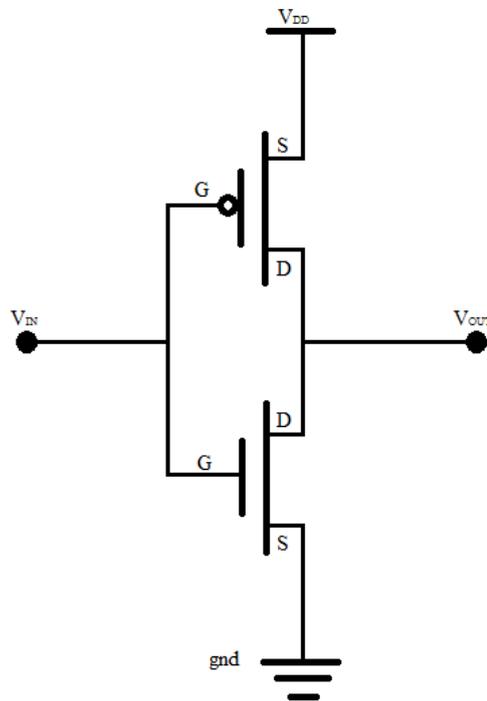


Figure 2.1: 2 transistor inverter. Schematic

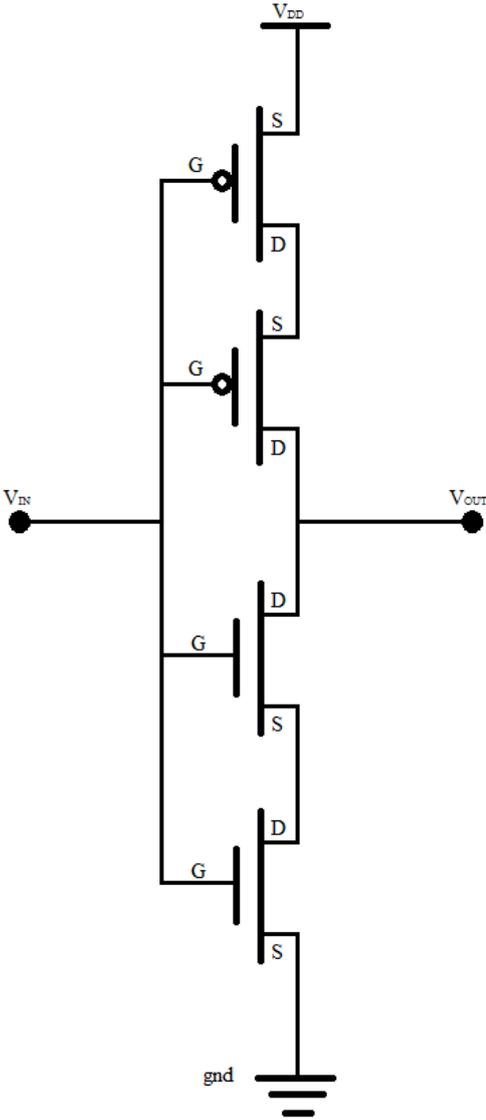


Figure 2.2: 4 transistor inverter. Schematic

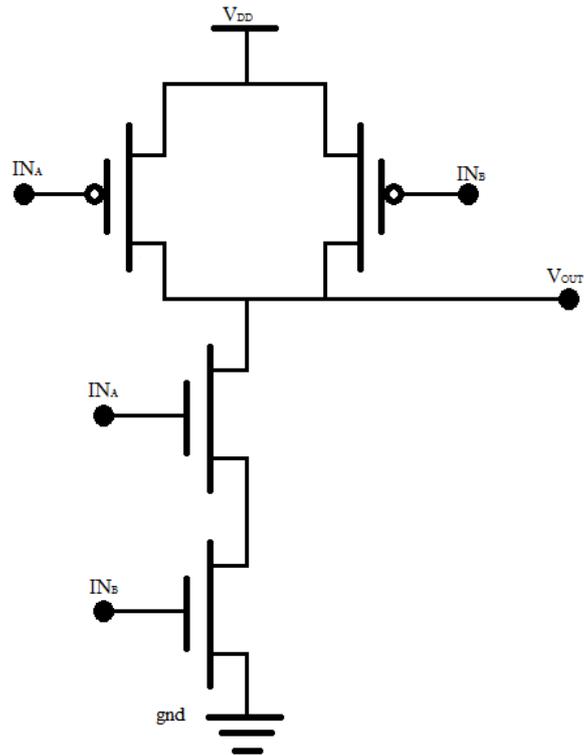


Figure 2.3: 4 transistor NAND2 gate. Schematic

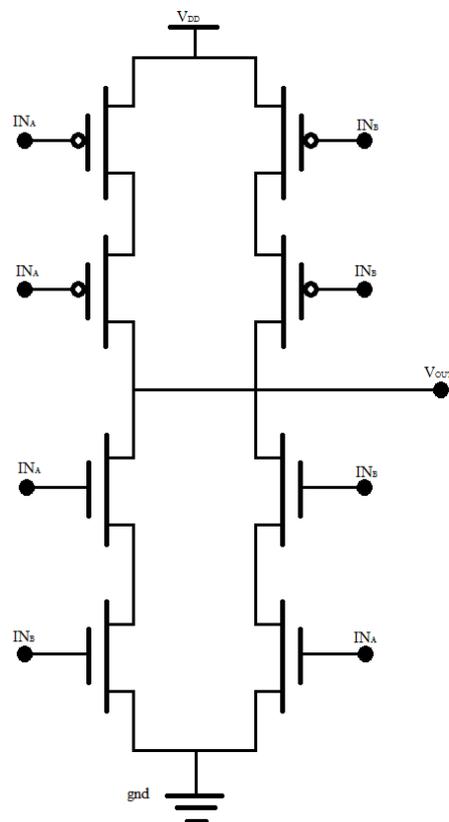


Figure 2.4: 8 transistor NAND2 gate. Schematic

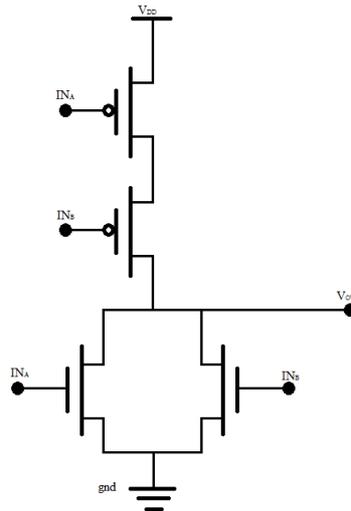


Figure 2.5: 4 transistor NOR2 gate. Schematic

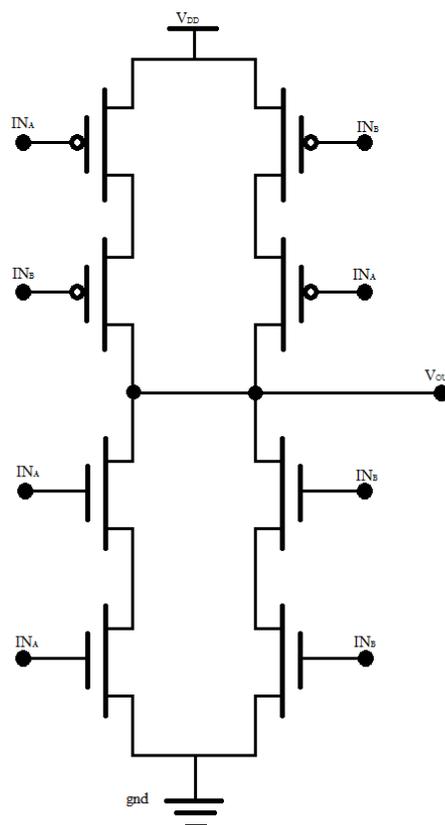


Figure 2.6: 8 transistor NOR2 gate. Schematic

2.2 Sub-threshold current

When a transistor have a drain source voltage lower than the transistors threshold voltage ($V_{DS} < V_{TH}$) while still bein forward biased the effects of drifts are reduced, and the equilibrium of the depletion region is mainly maintained by diffusion. In this stat a current going from the drain to the source called the sub-threshold current (I_{ST}) is dominant }. The sub-threshold current is given by the formula [2][5].

$$I \approx I_{ST} = I_0 \frac{W}{L} e^{\frac{(V_{GS}-V_{TH})}{nv_t}} \left(1 - e^{-\frac{V_{DS}}{v_t}} \right) \quad (2.1)$$

I_0 is the sub-threshold current when $V_{GS} = V_{TH}$. The sub-threshold factor is referred to as n . Both I_0 and n are decided by the technology used. The variable v_t is the thermal voltage given by $\frac{kT}{q}$ (k is Boltzmann's constant, and q is the charge of an electron). W/L is the ratio between the width and length of the transistor [2].

Due to this I_{ST} it is possible for logical gates to operate with a V_{DD} below V_{TH} .

2.3 Metrics

2.3.1 Gate balance

Noise Margin

To establish at what point a logical gate switches logical state, the transfer characteristics of the gate must be explored. When a gate switchtes from "1" to "0", the gain can be found by taking the derivative of the output curve. The points V_{OH} is the highest output that is recognized as a logical "1", while V_{OL} is the lowest output that is recognized as a logical "0". V_{IH} is the lowest input that is recognized as a logical "1", and V_{IL} is the highest input that is recognized as a logical "0". The area between V_{IH} and V_{IL} is a region where it is undefined whether the input is "1" or "0", and is called the *Undefined region*. The area between V_{OH} and V_{IH} is a logical "1" and the area between V_{OL} and V_{IL} is a logical "0".

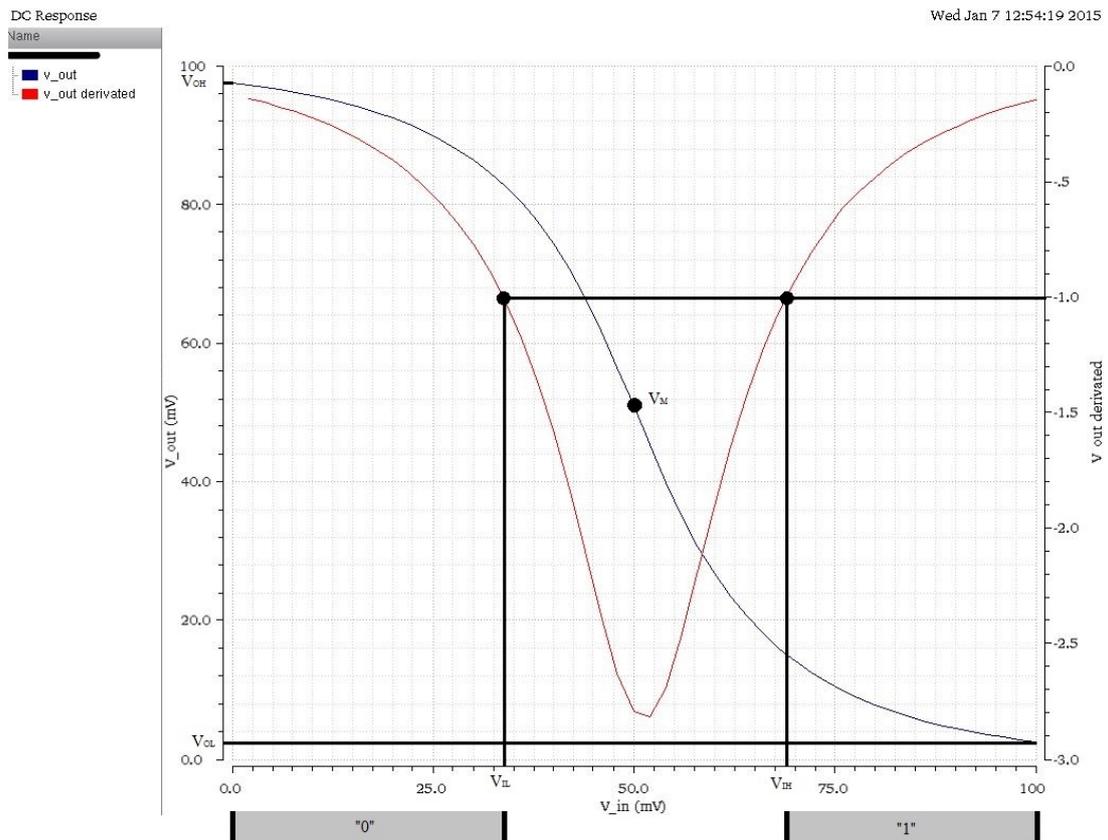


Figure 2.7: Transfer characteristic of an inverters output, and the derivative of the output. V_{OH} , V_{OL} , V_{IH} and V_{IL} are marked. $V_{DD} = 100mV$

The area between V_{OH} and V_{IH} , and the area between V_{OL} and V_{IL} are also a measurement of how large noise signals a logical gate can be exposed to. These areas are often referred to as noise margins. The high noise margin (VNM_H) is the region between V_{OH} and V_{IH} . The low noise margin (VNM_L) is the region between V_{OL} and V_{IL} . These relationships are described in the formulas 2.2 and 2.3, and illustrated in figure 2.8 [6].

$$VNM_H = V_{OH} - V_{IH} \quad (2.2)$$

$$VNM_L = V_{IL} - V_{OL} \quad (2.3)$$

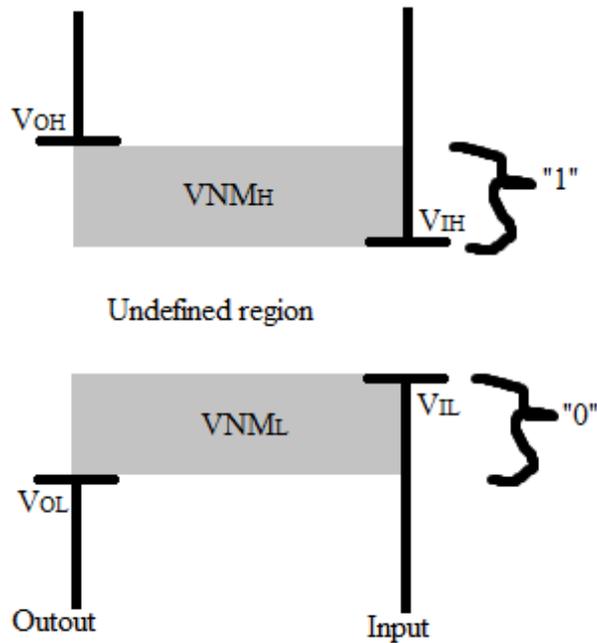


Figure 2.8: Illustration of noise margins

Switching point

The switching point of a logical gate is the point where the output value is equal to $\frac{v_{dd}}{2}$. In figure 2.7, this point is referred to as V_M . Below is an image of a DC-characteristics of an inverter. The v_{dd} and $\frac{v_{dd}}{2}$ are marked along the y-axis. The switching point is marked with SP , where the output is equal to $\frac{v_{dd}}{2}$. The value of the input voltage at the switching point is marked as $SP(x)$ along the x-axis. This input voltage is the x-coordinate of the switching point and will be referred to as " SP_x ".

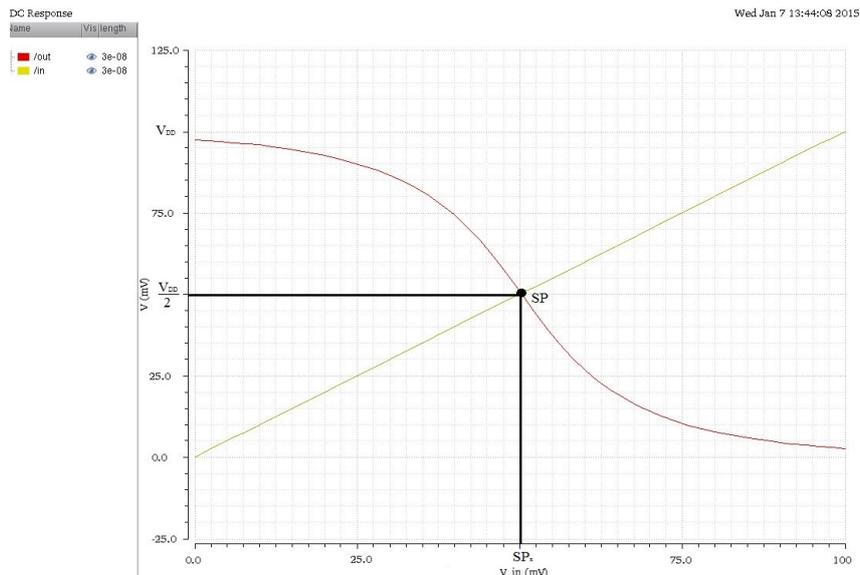


Figure 2.9: Transfer characteristic of an inverter with *perfect balance*. SP and SP_x are marked. $V_{DD} = 100mV$

The SP_x is a measure of how the gate is balanced. If the gate is perfectly balanced, the input voltage and output voltage are equal at the switching point, and both are equal to $\frac{v_{dd}}{2}$. When this is true, the gate is the most robust against noise. The further away from $\frac{v_{dd}}{2}$ SP_x is, the more prone to noise is the gate. In figure 2.9, noise pulses at the input needs to be at least 50mV, in order to make the inverter change state. In the image below 2.10 a noise pulse of only 25mV can make the inverter change state from 1 to 0.

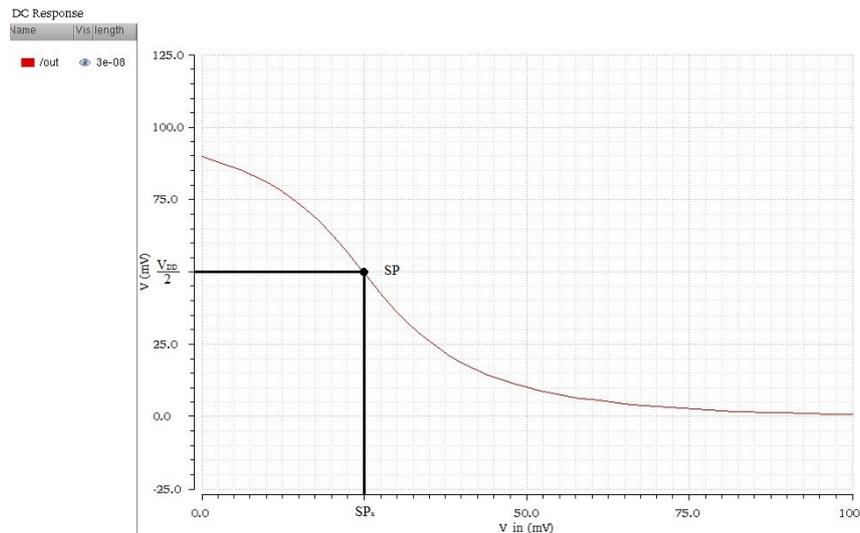


Figure 2.10: Transfer characteristic of an *unbalanced* inverter. SP and SP_x are marked. $V_{DD} = 100mV$

In the ideal situation $SP_x = \frac{v_{dd}}{2}$. However a logical gate might be fully functional with some deviation of SP_x . In this report different grades of balance will be used to determine the quality of the logical gate. They are given in the table below:

| Grade of balance | Range of SP_x |
|------------------|---|
| Perfect balance | $\frac{v_{dd}}{2}$ |
| Good Balance | $\frac{v_{dd}}{2} \cdot 45\%$ to $\frac{v_{dd}}{2} \cdot 55\%$ |
| Balanced | $\frac{v_{dd}}{2} \cdot 40\%$ to $\frac{v_{dd}}{2} \cdot 60\%$ |
| Unbalanced | under $\frac{v_{dd}}{2} \cdot 40\%$ or over $\frac{v_{dd}}{2} \cdot 60\%$ |

Both noise margins and switching point are ways to measure the balance of a logical gate. Both methods are used in this project. In order to measure the switching point and noise margins, transfer characteristics similar to the one in figure 2.9 must be created. For an inverter, this is done by simply increasing the input voltage from *gnd* to V_{DD} . For a 2 input NAND gate (NAND2) this can be done either by connecting the two inputs together (inverter coupling) and then increase the common input from *gnd* to V_{DD} . Or it could be done by connecting one input to V_{DD} while increasing the other input from *gnd* to V_{DD} . A similar approach can be used on the 2 input NOR gate (NOR2). It can be inverter coupled, or one input can be connected to *gnd* while the other input is increased from *gnd* to V_{DD} .

2.3.2 Power

In logical gates the power consumed is the sum of the static power dissipation and the dynamic or switching power dissipation. This can be estimated with the formula 2.4, where the static power consumption (P_{DC}) is given in formula 2.5, and the dynamic power consumption (P_{dyn}) is given in formula 2.6. In the estimations V_{DD} is the supply voltage, I_{DDQ} is the leakage current, C_{out} is the load capacitance, and f is the switching frequency of the device [6].

$$P = P_{DC} + P_{dyn} \quad (2.4)$$

$$P_{DC} = V_{DD} \cdot I_{DDQ} \quad (2.5)$$

$$P_{dyn} = C_{out} \cdot V_{DD}^2 \cdot f \quad (2.6)$$

By combining formula 2.5 and 2.6 the total power dissipation can be found. This is done in formula 2.7 [6].

$$P = V_{DD}I_{DDQ} + C_{out}V_{DD}^2f \quad (2.7)$$

The EDA tool Cadence Virtuoso can measure the power consumed by a circuit more accurate than the estimation above. The estimation gives an indication on how the power consumption is, however the EDA tools measurements are more correct and were therefore used in this project. In order to do this, power needs to be saved as an output. By using the Cadence calculator, the average power consumed in a simulation can be calculated. The power obtained from the calculator is the the combined static and dynamic power, so it will not give an accurate indication whether it is the switching or the leakage that produces the majority of the power consumption. The total power will help to indicate which circuits uses the most power, and can be used together with the delay to create a power delay product.

2.3.3 Delay

The delay of the circuits is a measure of the speed. Delay determine at what frequencies the logical gates are able to operate. In this project the delay was measured while the circuits were operating at maximum speed. To achieve this, 3-staged ring oscillators were created. The generation of the ring oscillators is described further in chapter 3. The delay were measured across one gate in the ring oscillator. Below is a figure of the input signal and output signal of the device. The delay between two flanks can be measured with the EDA tool. It measures the time between a falling or rising edge at the input at $\frac{V_{DD}}{2}$, and the matching edge at the output at $\frac{V_{DD}}{2}$.

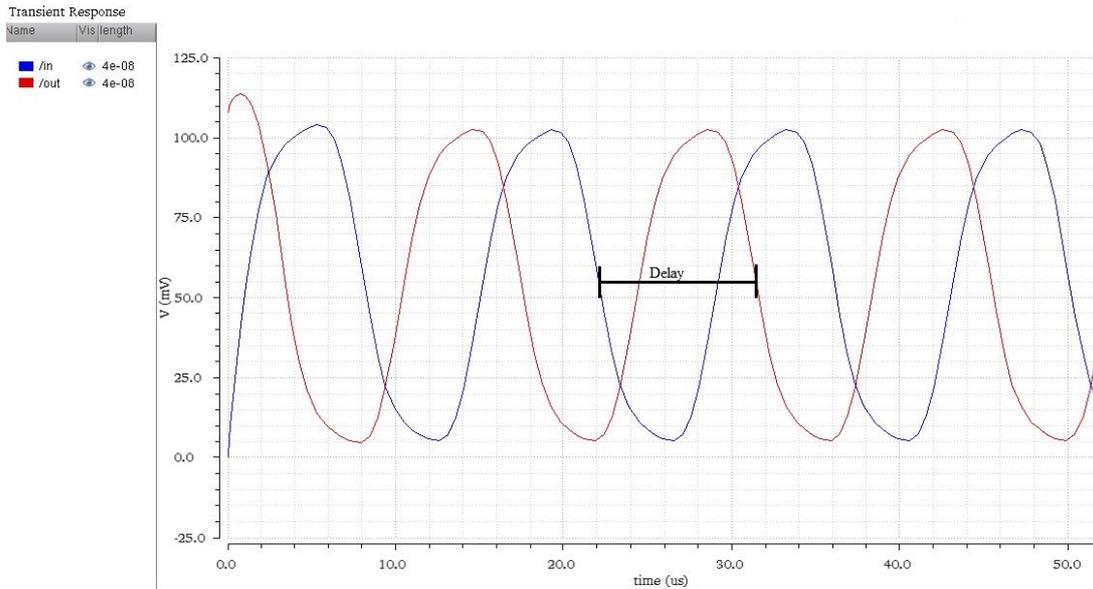


Figure 2.11: Input and output of a ring oscillator. Delay is marked. $V_{DD} = 108mV$

2.3.4 Power delay product

To decide when a circuit is operating at the most energy efficient point, the power delay product (PDP) is usually calculated[3]. To do this a ring oscillator is used to find the power and delay of the circuit at varying supply voltage. The voltage and delay are multiplied together and the power delay product is found (formula 2.8 and figure 2.12).

$$PDP(J) = Power(W) \cdot Delay(s) \quad (2.8)$$

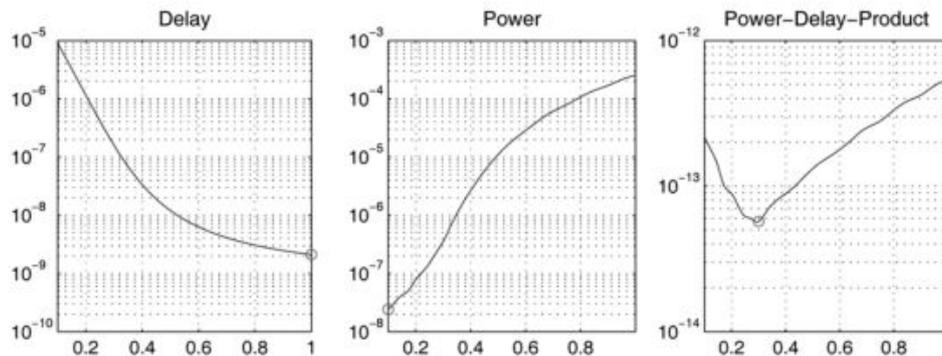


Figure 2.12: Power, Delay, and Power Delay Product. The circle indicates the lowest point. Transactions on Circuits and Systems, Nov. 2007.[7]

2.3.5 Process variations

The manufacturing process of integrated circuits may produce some variations between each sample. Even though all circuits in a batch have the same layout, there will be some differences, which will affect the yield. These variations can be simulated using a Monte Carlo simulation. The Monte Carlo will exert random instabilities to the circuit and measure the mean and standard deviation.

The Pelgrom model shows how standard deviation of mismatch between two devices is related to the transistor gate area. The model is presented below in equation 2.9. The formula presents the standard deviation σ of a model parameter ΔP . A_P is a process dependent constant, in this case the *area proportionality constant for a constant P*. W is the transistor gate width, while L is the gate length. S_P is how the model parameter varies with spacing, and D_x is the distance between the transistors[8].

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \quad (2.9)$$

Formula 2.9 show that process specific constants (A_P), layout specific constants (S_P and D_x), and the gate area (WL) affects the process variations in terms of standard deviation (σ). The constants specific for process and layout might be difficult to change, width and length are however much more easy to manipulate. The process variations are reduced by increasing the transistor gate size. This is illustrated in a simplified version of Pelgroms mismatch model in equation 2.10.

$$\sigma(\Delta P) \approx A_P \frac{1}{\sqrt{WL}} \quad (2.10)$$

Part I

Investigate the transistor characteristics

3. Procedure for transistor investigations

In this chapter the proces of investigating the transistors is described. The transistors used are the *nfet_b* and the *pfet_b* from the CMP provided FD-SOI library *cmos32lp*. These transistors were used in all the logical gates in this project. The simulations performed here provided transistor characteristics that were be used for consturction of the logical gates.

3.1 Areas of operation

To determine the different regions of operation, the drain current I_D was measured as the Drain-Source voltage V_{DS} changed [5]. The Gate-Source voltage V_{GS} and the Bulk-Source V_{GS} voltage were 0V. The transistor cells used were the 4 terminal FETs *nfet_b* and *pfet_b*. The dimensions used were the minmum values $Width = 200nm$ and $Length = 30nm$. The setup of the test benches used are presented in figures 3.1 and 3.2. The results are presented in figures 4.1 and 4.2 in chapter 4.

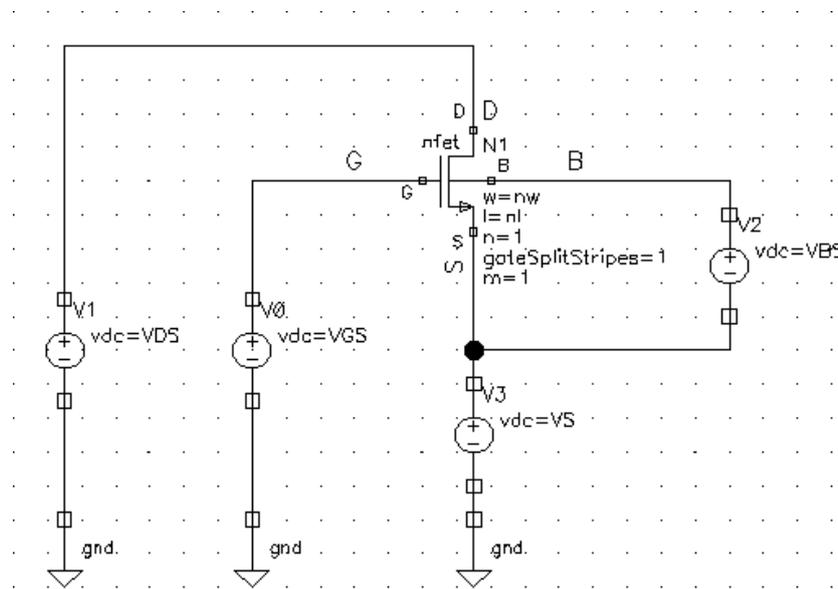


Figure 3.1: Nfet testbench schematic. $Width = 200nm$. $Length = 30nm$.

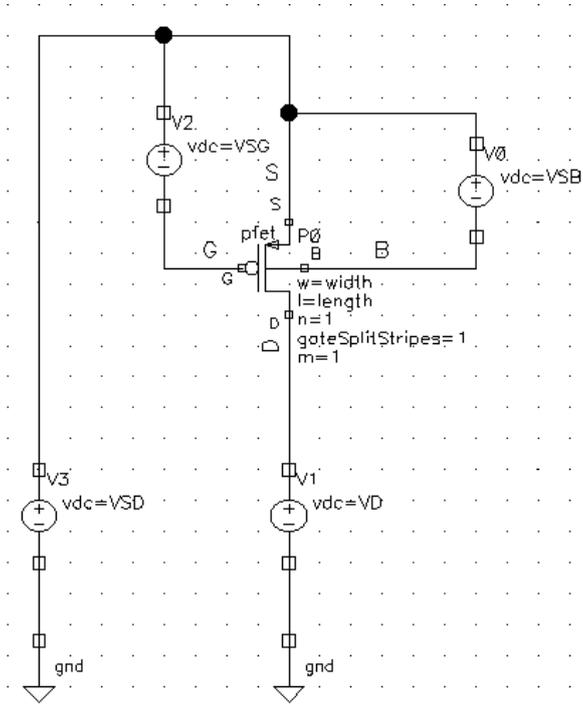


Figure 3.2: Pfet testbench schematic. *Width* = 200nm. *Length* = 30nm.

3.2 Finding the threshold voltage

The threshold voltage V_{th} can be extrapolated from the V_{GS} vs I_D plot of the transistors [5]. To do this the drain current I_D was measured while the gate source voltage V_{GS} was increased from 0V to 1V. The transistor must be in the triode region during this simulation. It can be seen in table 5.1 in chapter 4 that the V_{DS} must be below 80mV for the *nfet* and below 100mV for the *pfet*. In the simulation performed here, V_{DS} was 50mV. The testbenches used for these simulations were the same as figure 3.1 and 3.2. The bulk was connected to the source, so V_{BS} was 0V. The results of the simulations can be found in figures 4.3 and 4.4 in chapter 4.

The extrapolation were done by drawing a tangent where I_{DS} curve approximates a straight line. The tangent intersects the line $I_{DS} = 0A$. At this intersection $V_{GS} = V_{th}$. Figure 3.3 shows the I_D as a solid black line starting in origo, and the tangent is the dotted line. V_{th} is where the tangent intersect $I_D = 0V$. The approximations of V_{th} were done in figures 4.5 and 4.6, and the results are presented in table 4.1.

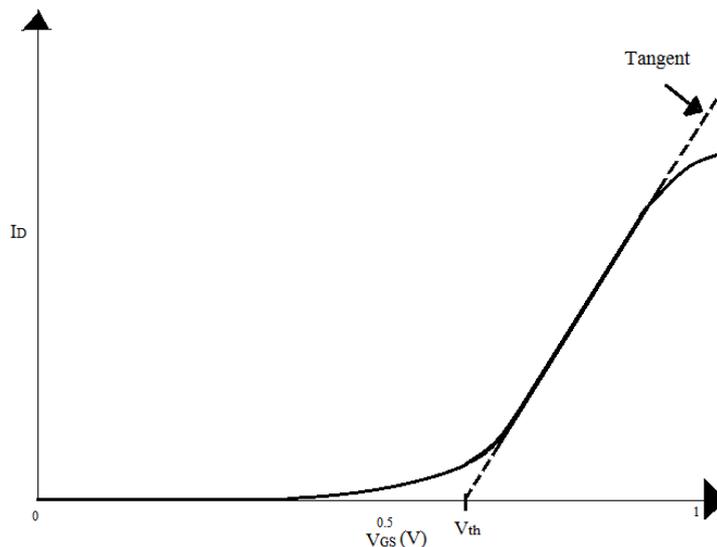


Figure 3.3: Illustration of how to extrapolate V_{th} from a V_{GS} vs I_D plot.

The EDA tool *Cadence virtuos* can also be used to find transistor characteristics using *spectre*. By saving DC operating points during simulations, the transistor characteristics can be found using a result browser. This was done and, the results are compared to the extrapolated values, in table 4.1.

3.3 Body biasing

How the bulk source voltage (V_{BS}) impacts the threshold voltage is also investigated. This was done by performing a parametric analysis of the V_{GS} versus I_D plot with varying V_{BS} . The results can be found in figures 4.7 and 4.8 in chapter 4. The DC operating points were saved, and presented in table 4.2.

4. Results from transistor simulations

In this chapter the results of the simulations performed on the *nfet_b* and *bfet_b* from the *cmos32lp* library. The tests are described in chapter 3. The results are further discussed in chapter 5.

Below in figure 4.1 is the $V_{DS} - I_{DS}$ characteristic of the *nfet_b*. The figure shows how the Drain-Source current (I_{DS}) is affected by an increasing Drain-Source voltage (V_{DS}). Both the gate and the bulk of the transistor are short circuited to the source, so the Gate-Source voltage (V_{GS}) and the Bulk-Source voltage (V_{BS}) are 0V. The transistors gate dimensions are the minimum values (Width = 200nm, Length = 30nm).

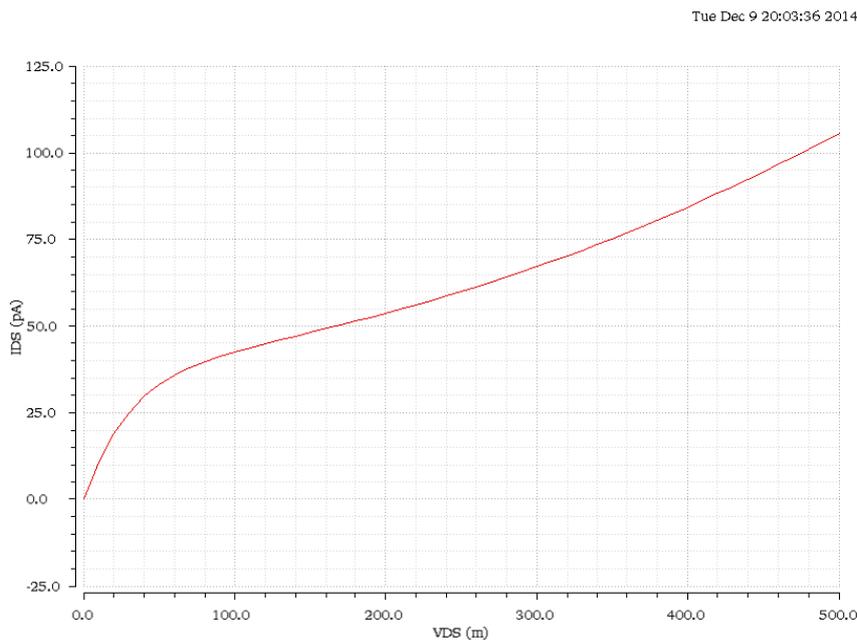


Figure 4.1: $V_{DS} - I_{DS}$ -plot of the *nfet_b* cell from the *cmos32lp* library. $V_{GS} = 0V$. $V_{BS} = 0V$. *Width* = 200nm. *Length* = 30nm.

Below in figure 4.2 is the $V_{SD} - I_{DS}$ characteristic of the *pfet_b*. The figure shows how the Drain-Source current (I_{DS}) is affected by an increasing Source-Drain voltage (V_{SD}). Both the gate and the bulk of the transistor are short circuited to the source, so the Source-Gate voltage (V_{SG}) and the Source-Bulk voltage (V_{SB}) are 0V. The transistors gate dimensions are the minimum values (Width = 200nm, Length = 30nm).

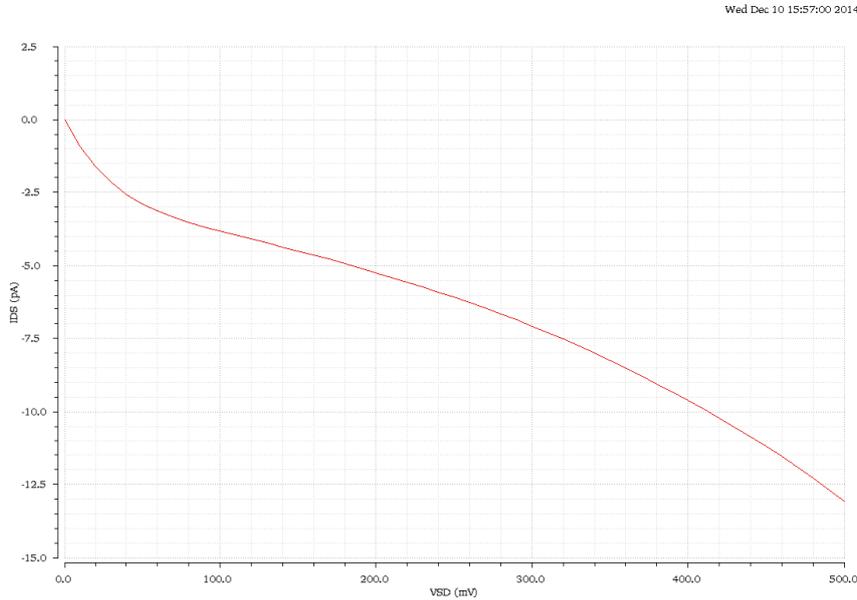


Figure 4.2: $V_{SD} - I_{DS}$ -plot of the *pfet_b* cell from the *cmos32lp* library.
 $V_{SG} = 0V$. $V_{SB} = 0V$. Width = 200nm. Length = 30nm.

Figure 4.3 shows the $V_{GS} - I_{DS}$ characteristic of the *nfet_b*. The graph shows the relationship between the Gate-Source voltage (V_{GS}) and the Drain-Source current (I_{DS}), while the Drain-Source voltage (V_{DS}) is 50mV. The bulk is connected to source so the Bulk-Source voltage (V_{BS}) is 0V. The transistors gate dimensions are the minimum values (Width = 200nm, Length = 30nm).

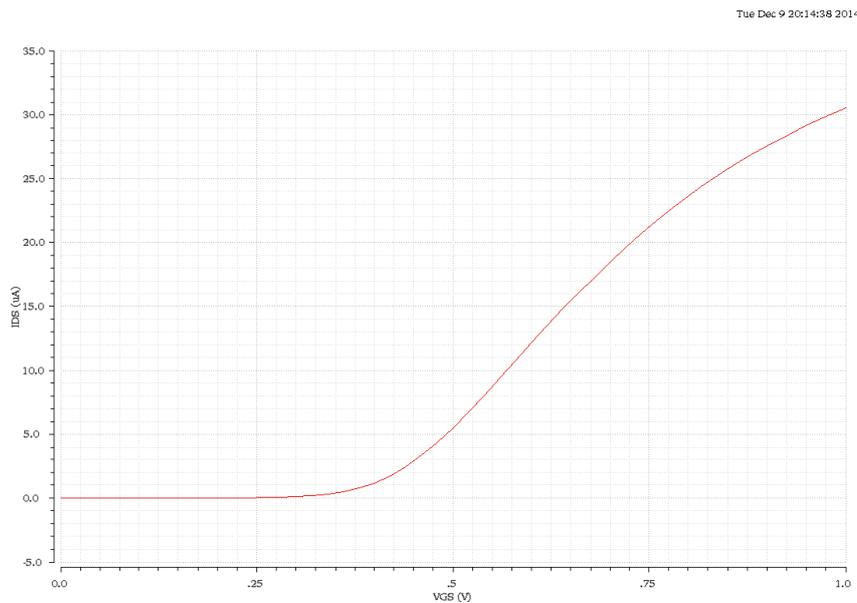


Figure 4.3: $V_{GS} - I_{DS}$ -plot of the *nfet_b* cell from the *cmos32lp* library.
 $V_{DS} = 50mV$. $V_{BS} = 0V$. Width = 200nm. Length = 30nm.

Figure 4.4 shows the $V_{SG} - I_{DS}$ characteristic of the *pfet_b*.

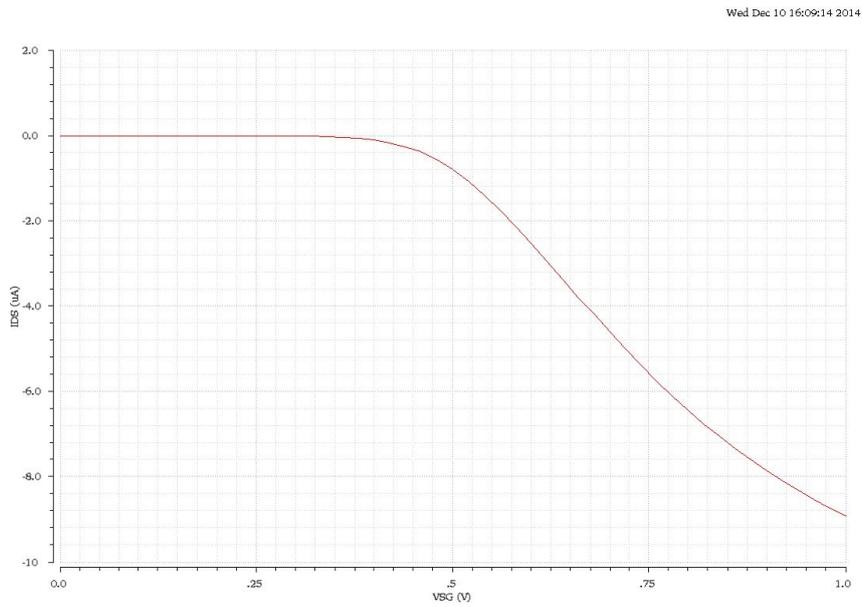


Figure 4.4: $V_{SG} - I_{DS}$ -plot of the *pfet_b* cell from the *cmos32lp* library. $V_{SD} = 50mV$. $V_{SB} = 0V$. $Width = 200nm$. $Length = 30nm$.

Approximate threshold voltage can be found by extrapolation. This is done and presented in figures 4.5 and 4.6.

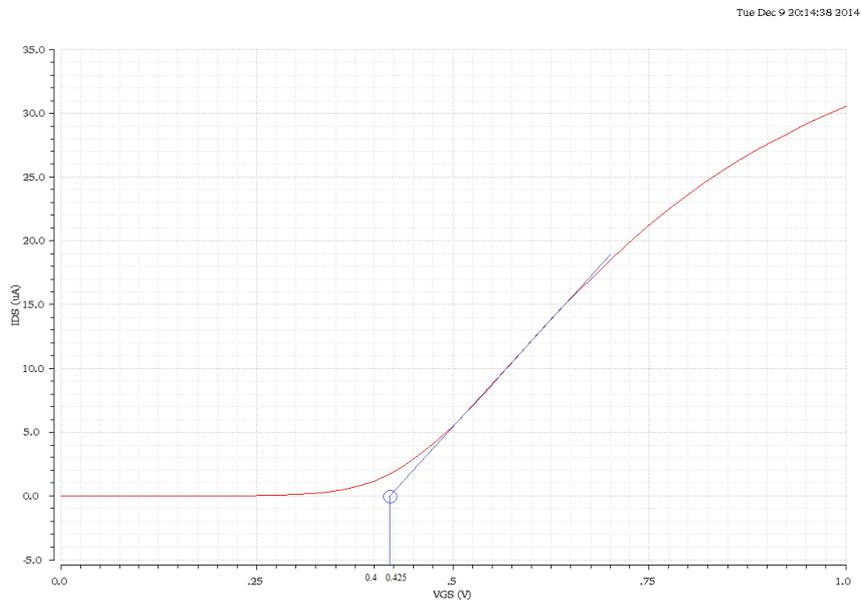


Figure 4.5: Extrapolated threshold voltage from the $V_{GS} - I_{DS}$ -plot of the *nfet_b* cell from the *cmos32lp* library. $V_{DS} = 50mV$. $V_{BS} = 0V$. $Width = 200nm$. $Length = 30nm$.

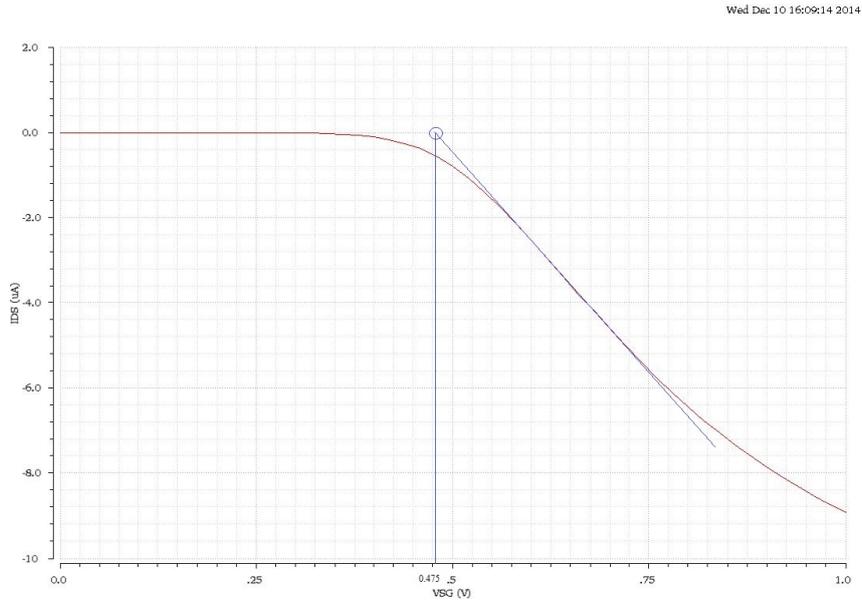


Figure 4.6: Extrapolated threshold voltage from the $V_{SG} - I_{DS}$ -plot of the *pfet_b* cell from the *cmos32lp* library. $V_{SD} = 50mV$. $V_{SB}=0V$.
 $Width = 200nm$. $Length = 30nm$.

The threshold voltage acquired by saving DC operation points is presented in the table below, together with the extrapolated threshold voltage:

| nfet V_{th} (V) Extrapolated | nfet V_{th} (V) DC operation point | pfet V_{th} (V) Extrapolated | pfet V_{th} (V) DC operation point |
|--|--|--|--|
| ~ 420m | 402m | ~ 477m | 458m |

Table 4.1: The threshold voltages of the *nfet_b* and the *pfet_b* acquired from extrapolation and DC operation point.

Here is the $V_{GS} - I_{DS}$ characteristics of the *nfet_b*, with varying bulk source voltage:

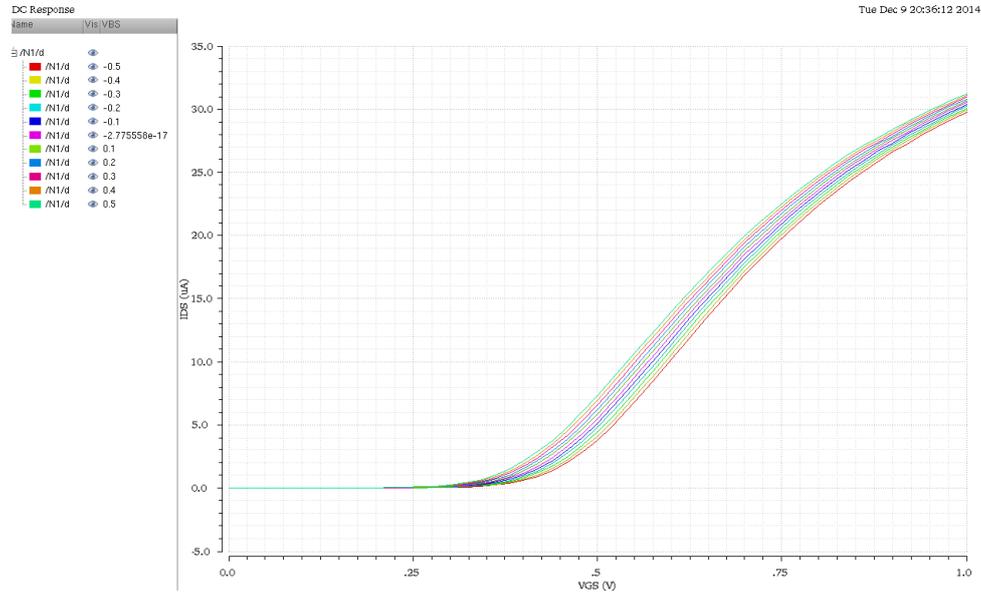


Figure 4.7: $V_{GS} - I_{DS}$ -plot of the *nfet_b* cell from the *cmos32lp* library. $V_{DS} = 50mV$. $Width = 200nm$. $Length = 30nm$.

Here is the $V_{SG} - I_{DS}$ characteristics of the *pfet_b*, with varying source-bulk voltage:

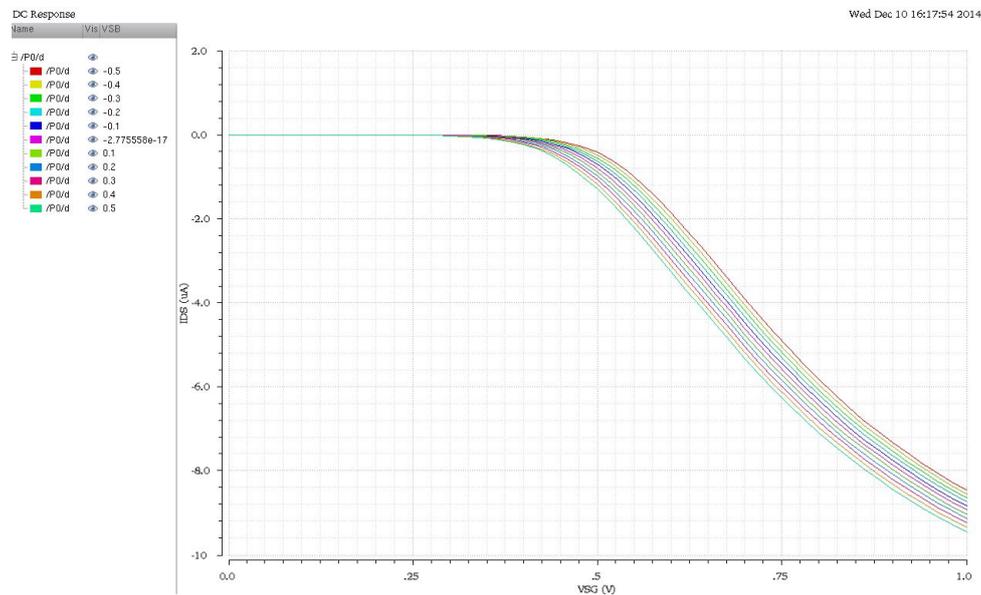


Figure 4.8: $V_{SG} - I_{DS}$ -plot of the *pfet_b* cell from the *cmos32lp* library. $V_{SD} = 50mV$. $Width = 200nm$. $Length = 30nm$.

Here is a table of the threshold voltages of the *nfet_b* and the *pfet_b*, as the bulk voltage varies.

| V_{BS} (V) | nfet V_{th} (V) | pfet V_{th} (V) |
|--------------|-------------------|-------------------|
| -500m | 434m | 423m |
| -400m | 428m | 430m |
| -300m | 422m | 437m |
| -200m | 415m | 444m |
| -100m | 409m | 451m |
| 0 | 402m | 458m |
| 100m | 396m | 465m |
| 200m | 390m | 472m |
| 300m | 383m | 478m |
| 400m | 377m | 485m |
| 500m | 370m | 492m |

Table 4.2: The threshold voltage of the *nfet_b* and the *pfet_b* cell from the *cmos32lp* library, with varying bulk-source voltage. $V_{DS} = 50mV$ for the *nfet_b*. $V_{SD} = 50mV$ for the *pfet_b*. *Width* = 200nm. *Length* = 30nm.

5. Discussion of the transistor simulation results

5.1 Identifying the sub-threshold area

The graphs in figures 4.1 and 4.2 shows how the Drain-Source current I_D is related to the Drain-Source voltage V_{DS} . From this relationship we can identify the different regions of operations (Large signal characteristics) [5]. These characteristics are given in the table below.

| Device | Triode region ΔV_{DS} | Active region ΔV_{DS} | Short-channel effects region ΔV_{DS} |
|---------------|----------------------------------|----------------------------------|---|
| <i>nfet_b</i> | 0V - 80mV | 80mV - 260mV | 260mV < |
| <i>pfet_b</i> | 0V - 100mV | 100mV - 310mV | 310mV < |

Table 5.1: Transistor large signal characteristics.

To find the different regions of inversion, the relationship between I_D and the Gate-Source voltage (V_{GS}) must be plotted while the transistor is in the triode region. This is done, and the results are displayed in figures 4.3 and 4.4. In these tests $V_{DS} = 50mV$. By extrapolation an approximate threshold voltage can be estimated. This is done in figures 4.5 and 4.6. The EDA tool (Cadence Virtuoso) is able to estimate the threshold voltage as well by saving DC operation points. The threshold voltages of the devices are presented in table 4.1. The estimated values are larger than the values obtained from the design tool, but they are quite close to each other. This indicates that the design tool gives reliable DC operation points, and can be used to measure the threshold voltage further in this project.

Table 4.2 shows how body biasing can influence the threshold voltage of the devices. Applying a voltage to the bulk of the *nfet* higher than the source, will reduce the threshold voltage and make it in CMOS terms "stronger". A lower voltage will make the threshold voltage increase, and make it "weaker". In this project, the source of *nfet* will usually be *gnd*. So a positive voltage at the bulk of the *nfet* will make it stronger, while a negative voltage will make it weaker. For the *pfet* a voltage at the bulk higher than the source will make the threshold voltage higher. While a bulk voltage lower than the source will give a lower threshold voltage. The source of *pfet* will usually be *vdd*. So a bulk voltage higher than *vdd* will give a weaker *pfet*, while a bulk voltage lower than *vdd* will make it stronger.

In this project, the aim is to generate logical gates that are operational in the weak inversion region (sub-threshold), with as low supply voltage as possible. Supply voltages close to 400mV will be near threshold, since it is close to the threshold voltage of the *nfet_b*. So in order to be sub-threshold all supply voltages needs to be deeper into the weak inversion region. As a starting point, supply voltages in the area 85mV – 105mV were investigated. The maximum of

105mV ensures that the gates are truly sub-threshold. When the supply voltage is below 85mV both the *nfet* and *pfet* devices are in the triode region, and making the gates operate might prove difficult. However, the supply voltage may end up outside these boundaries at a later state if needed.

Part II

Schematic design of the logical gates

6. Schematic design procedure

6.1 2T Inverter

A 2T Inverter was created by using the two transistors *nfet.b* and *pfet.b*. The Inverter was constructed with the 3 inputs *in*, *bulk_pfet* and *bulk_nfet*, and one output *out*. The source of the *nfet.b* was connected to the ground net (*gnd!*). The source of the *pfet.b* was connected to the supply voltage net *vdd!*. The schematic of the inverter is presented in figure 6.1.

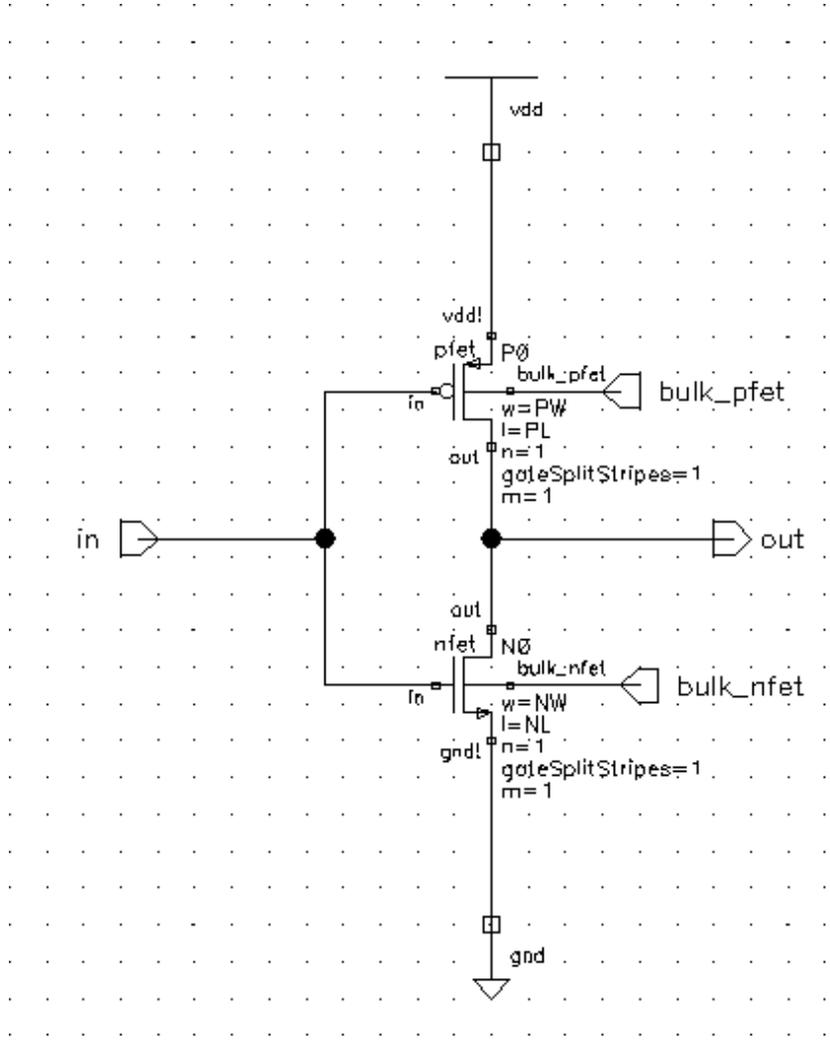


Figure 6.1: Schematic of the 2T Inverter

6.2 4T Inverter

The 4T Inverter was created by using two of each of the transistors *nfet_b* and *pfet_b*. The Inverter has the 3 inputs *in*, *bulk_pfet* and *bulk_nfet*, and one output *out*. The source of the lower *nfet* was connected to the ground net (*gnd!*). The source of the top *pfet* was connected to the supply voltage net *vdd!*. The schematic of the inverter is presented in figure 6.2.

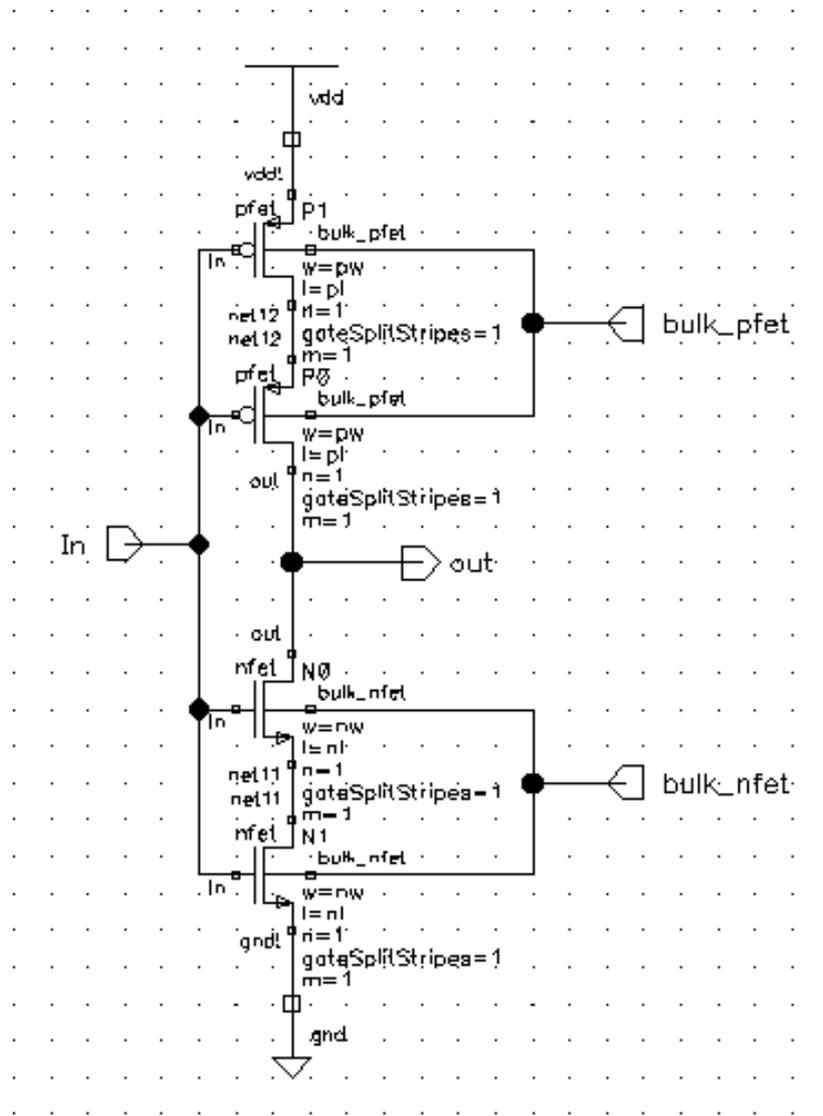


Figure 6.2: Schematic of the 4T Inverter

6.3 4T NAND2

The 4T NAND2 gate was created by using two of each of the transistors *nfet_b* and *pfet_b*. The gate was designed with the 4 inputs *in_A*, *in_B*, *bulk_pfet* and *bulk_nfet*, and one output *out*. The source of the lower *nfet* was connected to the ground net (*gnd!*). The source of the two *pfets* were connected to the supply voltage net *vdd!*. The schematic is presented in figure 6.3

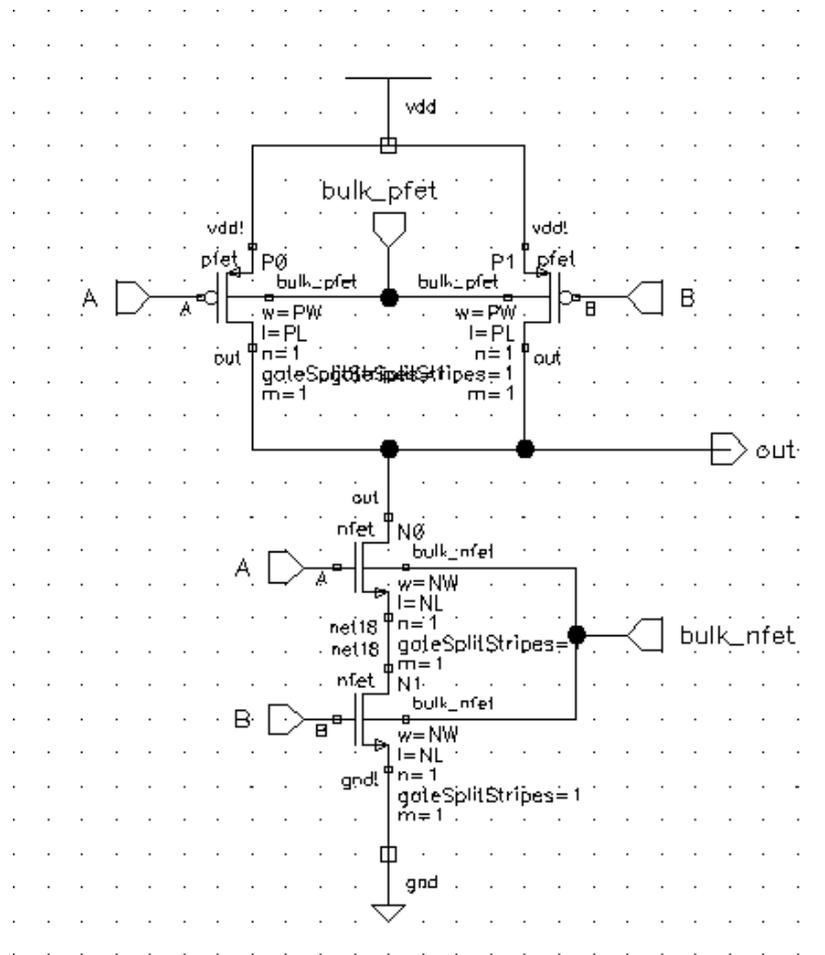


Figure 6.3: Schematic of the 4T NAND2 gate

6.4 8T NAND2

The 8T NAND2 gate was created by using four of each of the transistors *nfet_b* and *pfet_b*. The gate was constructed with the 4 inputs *in_A*, *in_B*, *bulk_pfet* and *bulk_nfet*, and one output *out*. The source of the two lower *nfets* were connected to the ground net (*gnd!*). The source of the two upper *pfets* were connected to the supply voltage net *vdd!*. The schematic is presented in figure 6.4

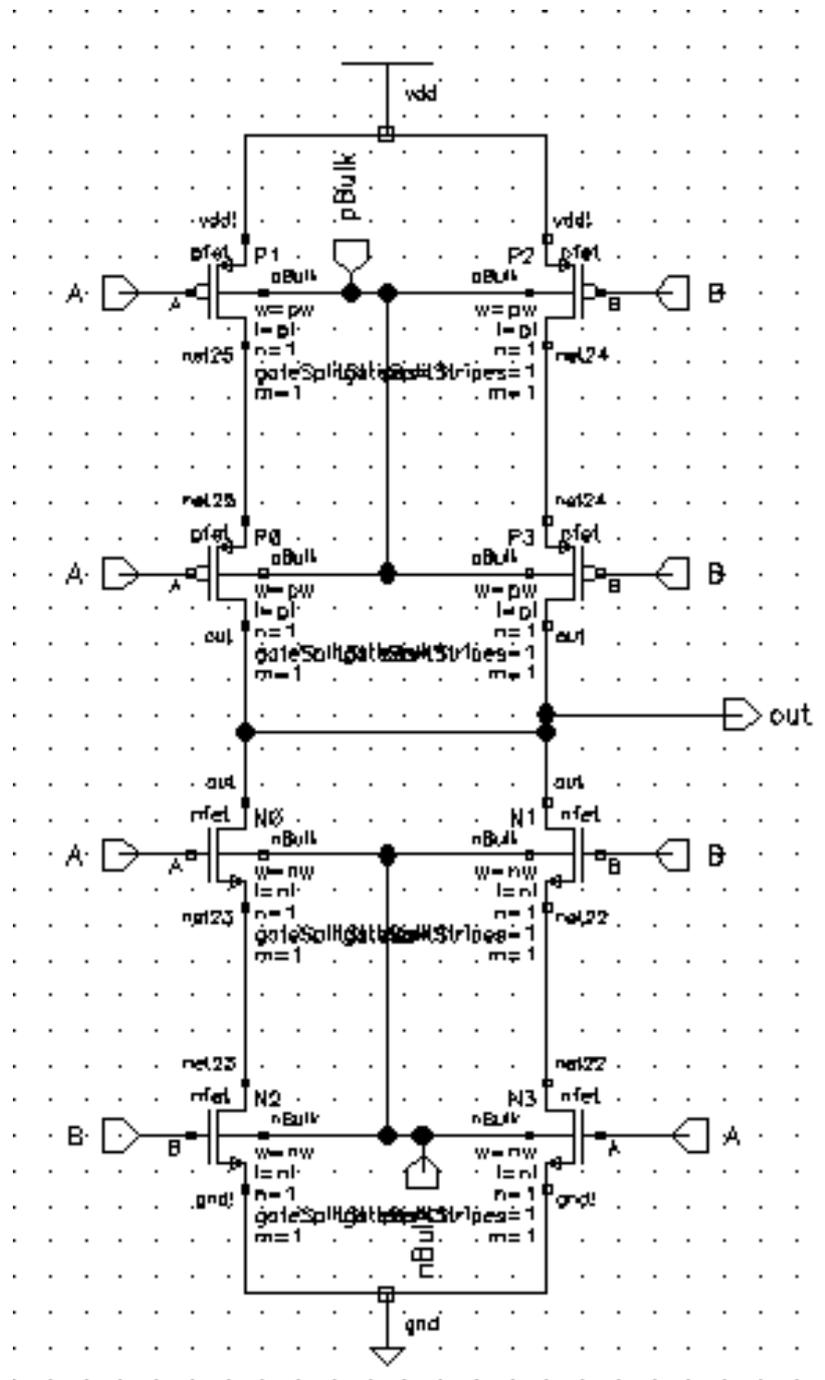


Figure 6.4: Schematic of the 8T NAND2 gate

6.5 4T NOR2

The 4T NOR2 gate was created by using two of each of the transistors *nfet_b* and *pfet_b*. The gate was designed with the 4 inputs *in_A*, *in_B*, *bulk_pfet* and *bulk_nfet*, and one output *out*. The source of the two *nfets* were connected to the ground net (*gnd!*). The source of the top *pfet* was connected to the supply voltage net *vdd!*. The schematic is presented in figure 6.5

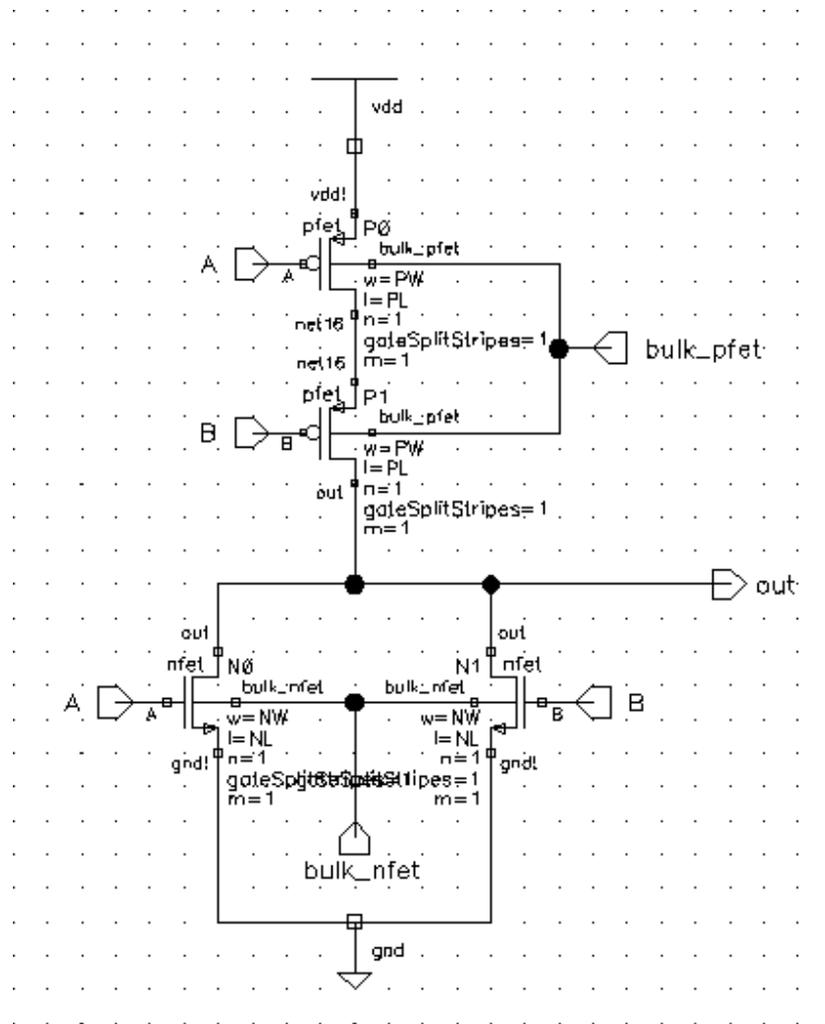


Figure 6.5: Schematic of the 4T NOR2 gate

6.6 8T NOR2

The 8T NOR2 gate was created by using four of each of the transistors *nfet_b* and *pfet_b*. The gate was constructed with the 4 inputs *in_A*, *in_B*, *bulk_pfet* and *bulk_nfet*, and one output *out*. The source of the two lower *nfets* were connected to the ground net (*gnd!*). The source of the two upper *pfets* were connected to the supply voltage net *vdd!*. The schematic is presented in figure 6.6

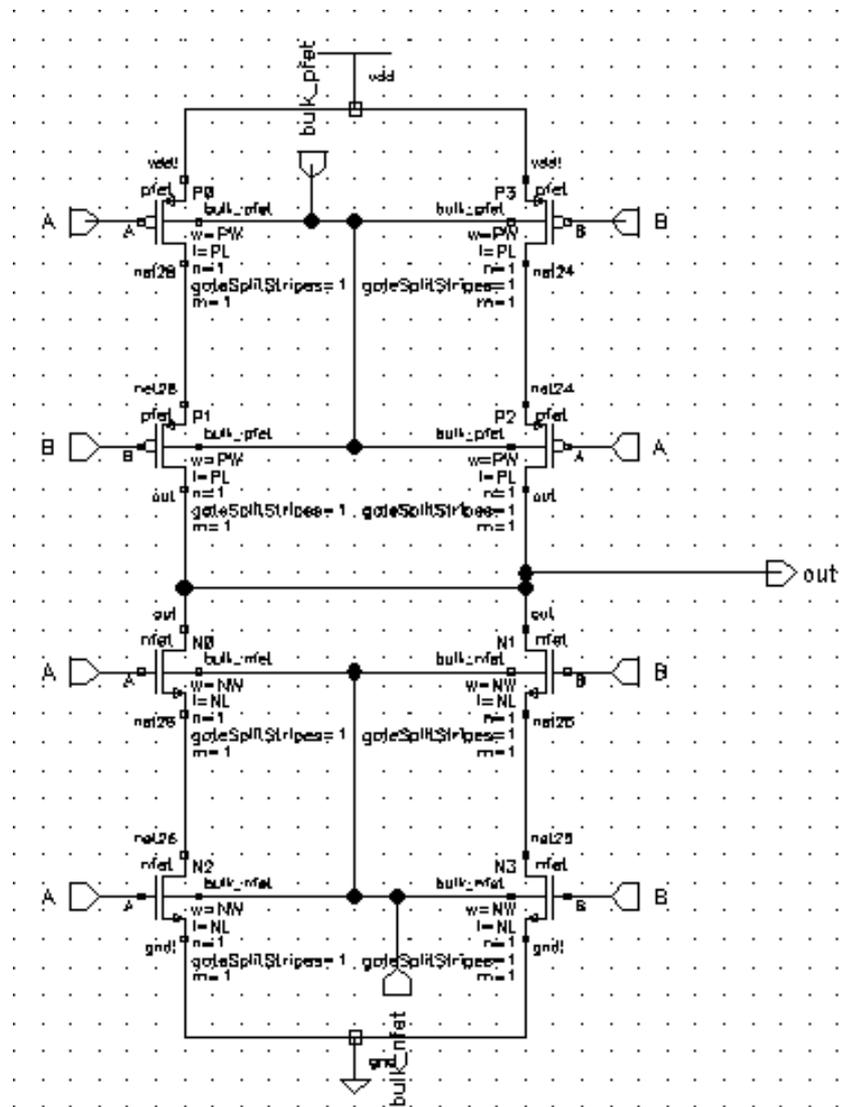


Figure 6.6: Schematic of the 8T NOR2 gate

6.7 Test benches

6.7.1 Gate balance

Switching point

To test for gate balance, the testbench in figure 6.7, 6.8 and 6.9 were created. They were used to perform a DC analysis on the inverters, NAND2 gates and NOR2 gates respectively. In the DC analysis the input voltage was increased from $0V$ to V_{DD} . The input voltage was V_{in} for the inverters, in_A for the NAND2 gates and NOR2 gates. The in_B voltage was set to be equal to V_{DD} for the NAND2 gates, while it was set to $0V$ for the NOR2 gates. This setup generated the transfer characteristics of the output signal of the logical gates. This output signal was measured and the value of SP_x was calculated using the *cross* function in *spectre*.

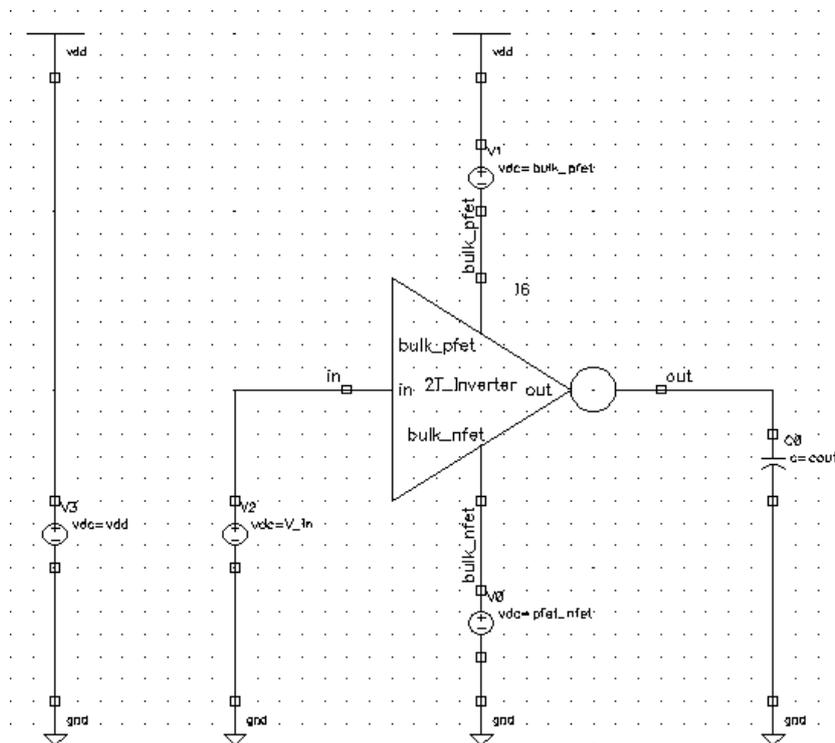


Figure 6.7: Schematic of the inverter test bench

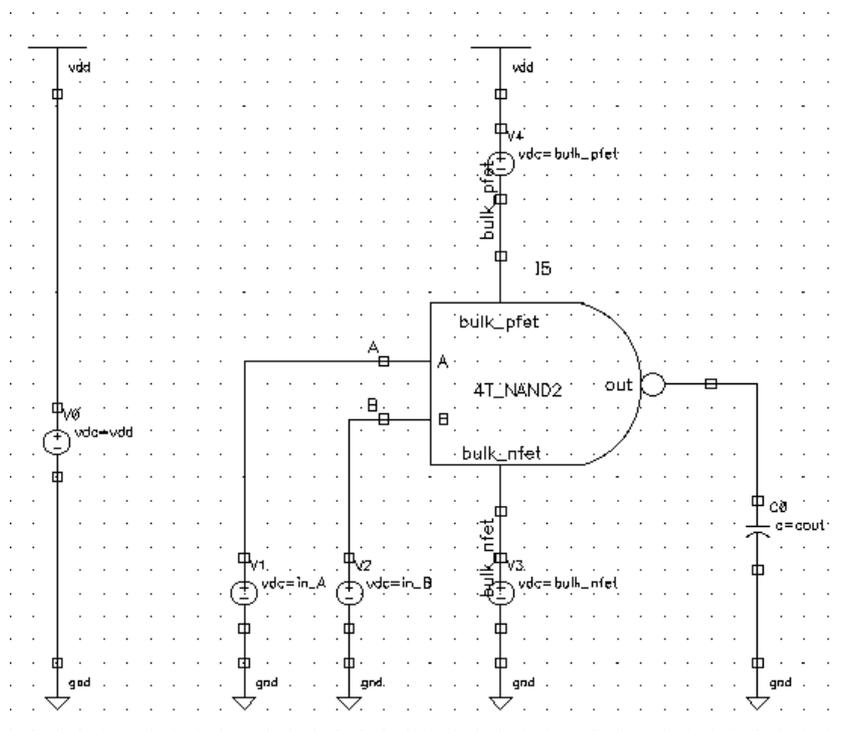


Figure 6.8: Schematic of the test bench for the NAND2 gates

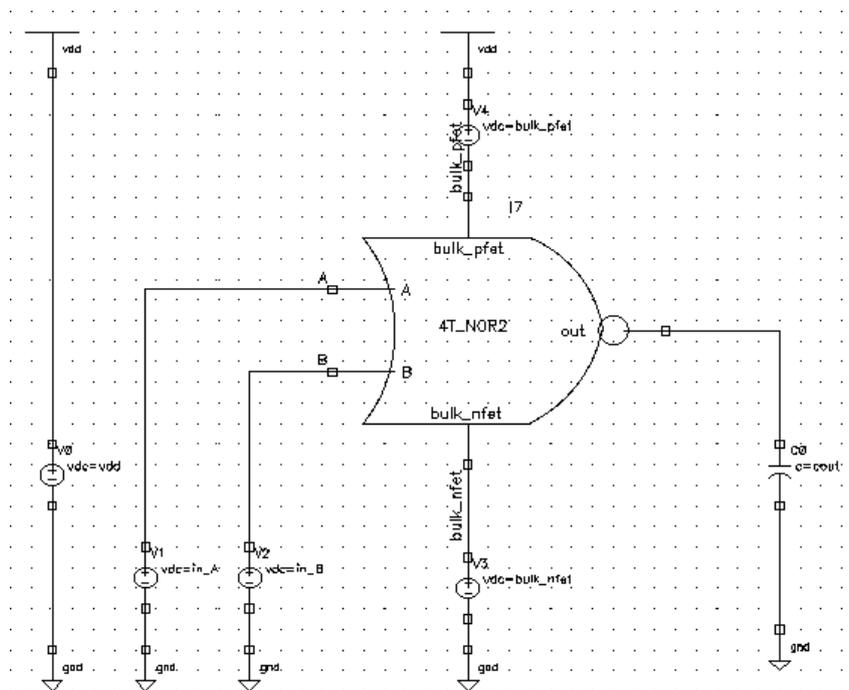


Figure 6.9: Schematic of the test bench for the NOR2 gates

The tests were performed several times with the transistor gate sizes presented in table 6.1. This process was a parametric analysis. The tests were performed with supply voltages spanning from 85mV to 105mV with 5mV intervals. All test results that had an SP_x between 40% and 60% of V_{DD} were stored for further processing.

| | Minimum size (m) | Maximum size (m) | step size (m) |
|-----------------------------|------------------|------------------|---------------|
| Nfet and Pfet length | 30n | 40n | 5n |
| Nfet width | 200n | 800n | 50n |
| Pfet width | 200n | 2.5 μ | 50n |

Table 6.1: Transistor sizes used in parametric analysis

Table 6.2 presents the value of SP_x at 40% and 60% of V_{DD} , with a V_{DD} spanning from 85mV to 105mV with steps of 5mV. The values in table 6.2 are the minimum and maximum values for SP_x that will be included in the further evaluation.

| V_{DD} (mV) | Ideal SP_X (mV) ($\frac{V_{DD}}{2}$) | Minimum SP_X (mV) ($V_{DD} \cdot 40\%$) | Maximum SP_X (mV) ($V_{DD} \cdot 60\%$) |
|---------------|---|--|--|
| 105m | 52.5 | 42 | 63 |
| 100m | 50 | 40 | 60 |
| 95m | 47.5 | 38 | 57 |
| 90m | 45 | 36 | 54 |
| 85m | 42.5 | 34 | 51 |

Table 6.2: Supply voltages used for the parametric analysis, and the range of results that will be evaluated

Certain sets of transistor gate sizes were extracted from the results of the parametric analysis. To investigate how transistor gate size and size ratio influence other metrics such as power, delay and process variations, the sets with the lowest area, largest area, and lowest ratio between $pfet$ and $nfet$ were extracted and presented in chapter 7.1.1.

6.7.2 Noise margin

The noise margins were measured by using the same test benches that were used to find the switching point. DC analyses were used to find the transfer characteristics of the outputs, and the derivative of the outputs were calculated. The minimum and maximum values of the outputs were also measured. The derivative of the outputs and the minimum and maximum values of the outputs were used to find the lower and higher noise margins as described in chapter 2.3.1. These analyses were performed on all the transistor sizes in table 6.1, with $V_{DD} = 100mV$. The results of can be found in chapter 7.1.1.

6.8 Power and delay

To test power and delay ring oscillators were created by connecting three logical gates in series. The NAND2 gates and the NOR2 gates were inverter coupled. These ring oscillators are presented in figures 6.10, 6.11 and 6.12. The oscillation in the ring oscillators were started by using *initial conditions*. Transient analyses were performed to test power, delay and minimum V_{DD} .

6.8.1 Power delay product

To test for the power delay product (PDP) the transistor sizes that produced lowest gate area and *good balance* were used. Average power consumption and delay was measured. The delay was measured at $\frac{V_{DD}}{2}$ on the 55th falling edges of the output and the input of one device. The power measurement was measuring the average power consumption of the whole circuit. The inverter and NAND2 tests ran for 3ms and were performed with V_{DD} spanning from 85mV to 130mV with intervals of 5mV. The NOR2 tests ran with voltages spanning from 90mV to 130mV with intervals of 5mV. The results were used to generate the power, delay and power delay product graphs in chapter 7.2.1.

6.8.2 Lowest V_{DD}

To find the lowest supply voltage that supported stable oscillations in the ring oscillator the delay was measured at 45% of V_{DD} at the 55th falling edge. Then simulations were performed with the the transistor gate sizes in table 6.1 with increasing V_{DD} starting from 70mV for the inverters and the NAND2 gates. The NOR2 gates used the transistor sizes in table 6.3. Simulations that returned the delay had oscillations, while simulations where the oscillations had decayed returned simulation error. The lowest supply voltage was found by looking after the simulation with the lowest V_{DD} and still returned a delay.

| | Minimum size (m) | Maximum size (m) | step size (m) |
|-----------------------------|------------------|------------------|---------------|
| Nfet and Pfet length | 30n | 40n | 5n |
| Nfet width | 200n | 800n | 50n |
| Pfet width | 200n | 4 μ | 50n |

Table 6.3: Transistor sizes used to find minimum V_{DD} of the NOR2 gates

A similar approach was used to find the lowest V_{DD} that supported oscillations between 25% and 75% of V_{DD} , and 5% and 95% of V_{DD} . Instead of measuring the delay at 45% of V_{DD} the delay was measured at 25%, 75%, 5% and 95%. Then the lowest supply voltages was found by running simulations with the transistor gate sizes in table 6.1 for the inverters and the NAND2 gates, and the sizes in table 6.3 for the NOR2 gates. The simulations were run with increasing V_{DD} until both 25% and 75%, or 5% and 95%, returned a delay instead of *simulation error*. The results of these simulations are presented in chapter 7.2.2.

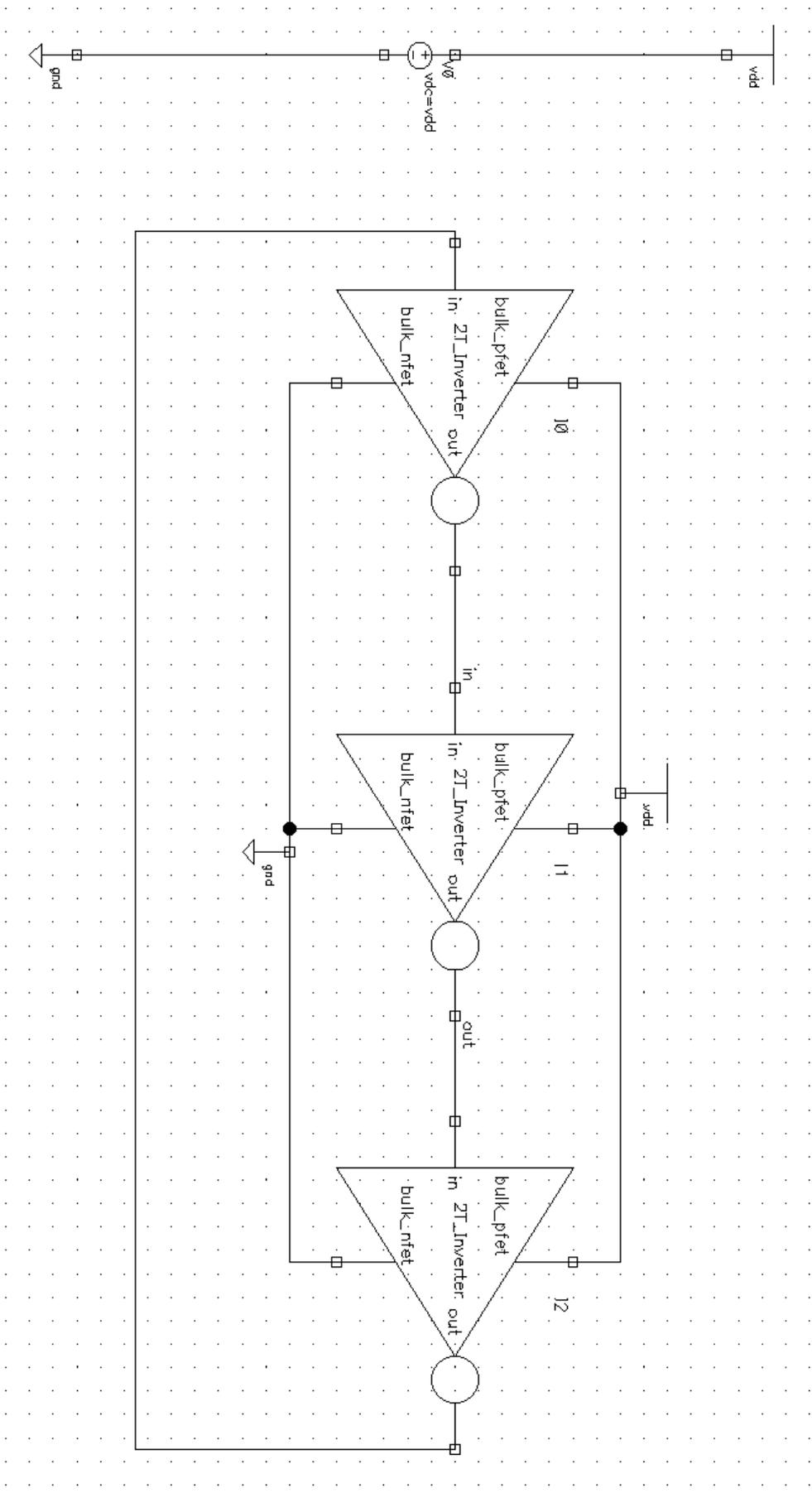


Figure 6.10: Schematic of the inverter test bench

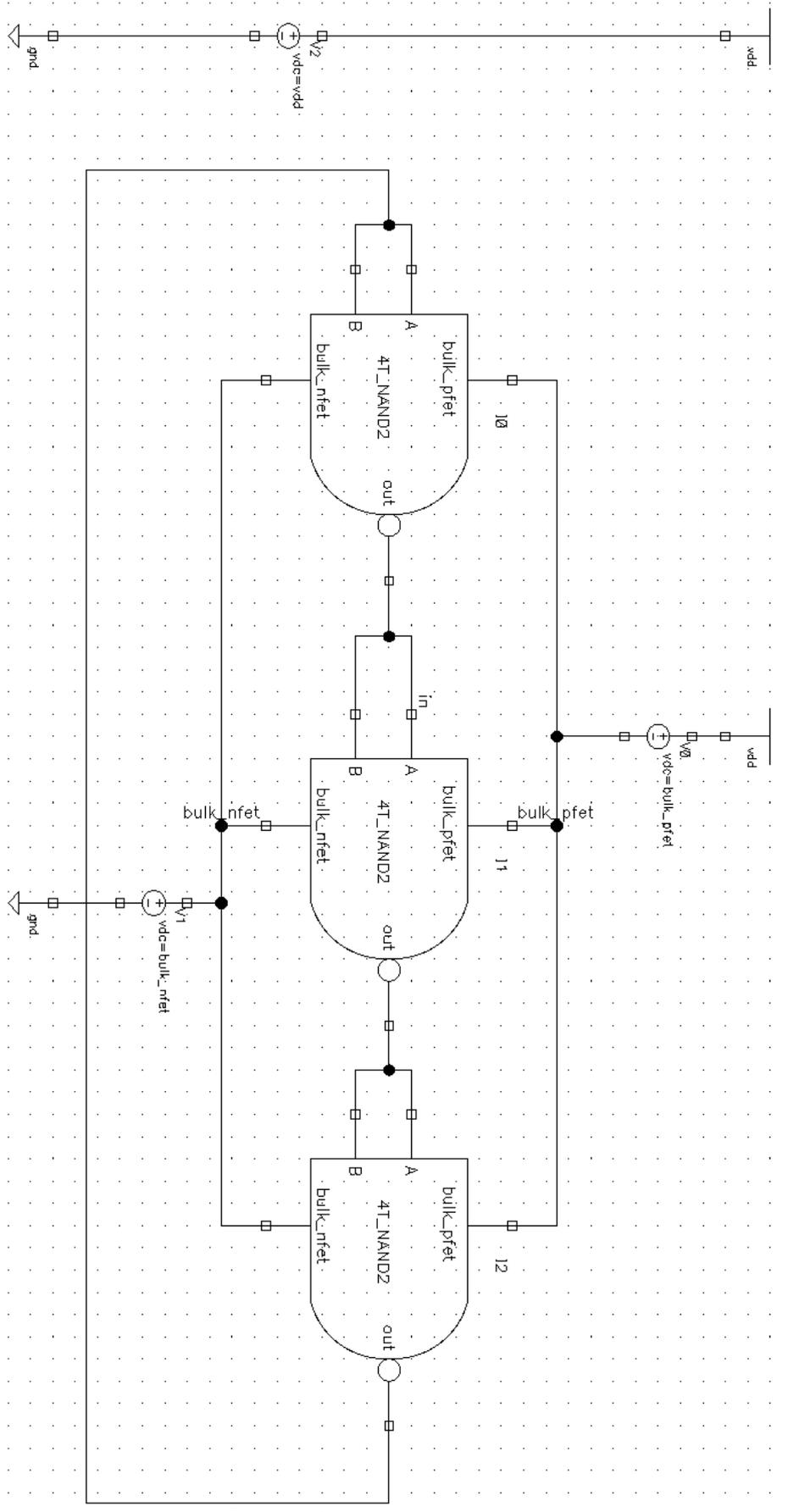


Figure 6.11: Schematic of the test bench for the NAND2 gates

6.9 Process variation

Monte Carlo analyses were performed to investigate how the DC characteristics SP_x and noise margins would vary in a manufacturing process. Monte Carlo was run with 200 samples and typical corners with $V_{DD} = 100mV$. The test benches were the same as used previously (figures 6.7, 6.8 and 6.9). The transistor sizes used for the Monte Carlo analysis were the following:

- The sets with the lowest gate area and having *good balance* (Low area & GB).
- The sets with the largest gate area and having *good balance* (Large area & GB).
- The sets with the lowest ratio between the width of the *pfet* and the *nfet* (Low size ratio)
- The sets with the lowest ratio between the higher and lower noise margins (Low VNM ratio).
- The sets with the lowest supply voltage and the power delay product in the ring oscillator (Low V_{DD} & low PDP).

The results of the Monte Carlo analyses are presented in chapter 7.3

6.10 Deciding a final size

The transistor size sets that went through the Monte Carlo analyses were the sets that had best results according to the following criteria: Transistor gate size and size ratio, noise margins and low supply voltage. These sets were further compared to each other. Therefore both DC and transient analyses were performed on all the sets. The DC analysis measured SP_x , higher and lower noise margins at $V_{DD} = 100mV$. The transient analyses measured power and delay in the ring oscillator at $V_{DD} = 100mV$. The power was the average power in the whole circuit, while delay was measured at $\frac{V_{DD}}{2}$ on the 55th falling edge. The minimum V_{DD} for stable oscillations, oscillations between 25% and 75%, and oscillations between 5% and 95% of V_{DD} .

The results from these simulations were used to decide upon a final size for each device. The criteria for the final size was to have as low V_{DD} as possible, while still being *balanced*. Results of this can be found in chapter 7.4.

6.11 Body biasing

To test the effects of body biasing the voltage source connected to the bulk of the *nfet* and the *pfet* of the NAND2 gate in testbench 6.8 were utilized. The 8T NAND2 gate was used for these tests. First the bulk of the *nfet* was increased from -100mV to 100mV with steps of 100mV. The Output and input was measured. Afterwards the same was done with the bulk of the *pfet*.

Afterwards was the procedure described in 6.7.1 and 6.7.2 repeated for the 8T NAND2 gate with the bulk of the *nfet* at -100mV, and the bulk of the *pfet* connected to *gnd* ($bulk_nfet = -100mV$, $bulk_pfet = 100mV$). The supply voltage was 100mV for this parametric analysis. The results with the lowest gate area, lowest size ratio, largest gate area and lowest VNM ratio while having an SP_x between 40% and 60% of V_{DD} were identified and presented in chapter 7.5.

The power, delay, and power delay product of the body biased 8T NAND2 gate was found by using the ring oscillator in figure 6.11. To achieve body biasing the bulk of the *nfet* was -100mV, and the bulk of the *pfet* was connected to *gnd* ($bulk_nfet = -100mV$, $bulk_pfet = 100mV$). The procedure was similar to the one described in 6.8.1.

To find the process variations of the body biased 8T NAND2 gate, a similar approach to the one described in 6.9 was used. It was only performed on the size set *Low VNM ratio*. To achieve body biasing the bulk of the *nfet* was -100mV, and the bulk of the *pfet* was connected to *gnd* ($bulk_nfet = -100mV$, $bulk_pfet = 100mV$).

The final step of the investigation of the body biased 8T NAND2 was to summarize the DC and transient characteristics of the gate. The tests performed in 6.10 was performed on the body biased 8T NAND2 gate. The results were compared to the 4T NAND2 and the regular 8T NAND2 gate in chapter 7.5.

7. Results of the schematic design

7.1 Gate Balance

7.1.1 Switching point

This chapter presents the results obtained from the DC analysis of the inverters, NAND2 gates and NOR2 gates. Included are the sets of transistor gate sizes that gave the best results according to the following criterias; lowest gate area, largest gate area, and lowest ratio. The results are presented in tables. All the results have a transfer characteristic that is between the borders presented in figure 7.1.

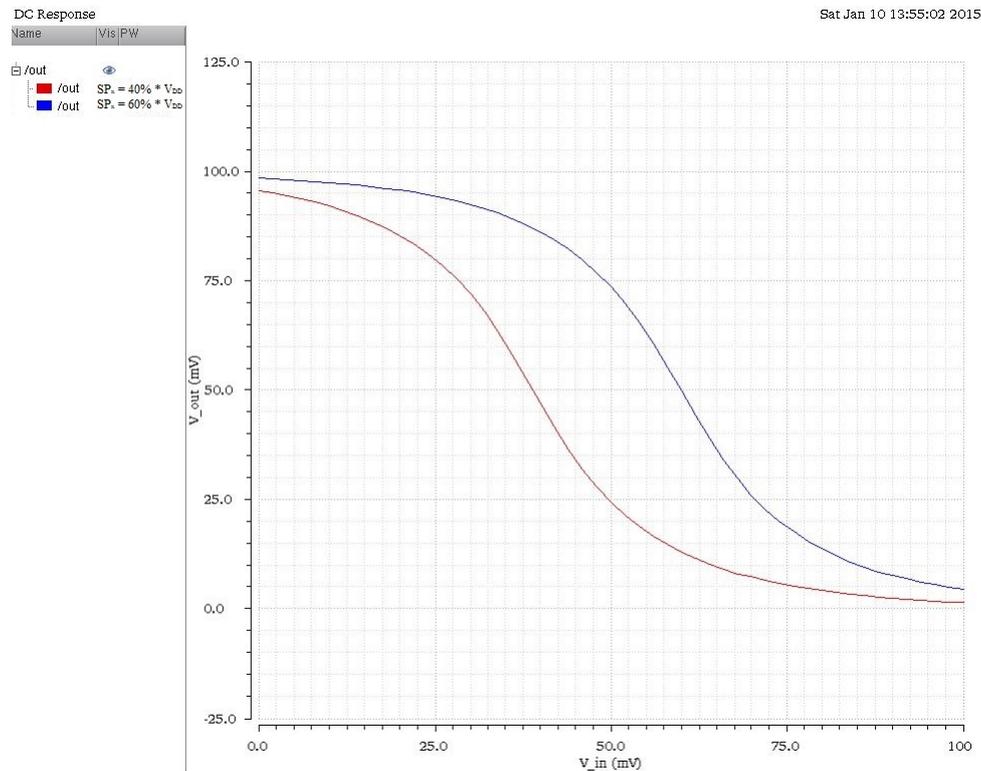


Figure 7.1: Upper and lower threshold for the transfer characteristics of the sets of transistor gate sizes presented in tables 7.2, 7.3, 7.4, 7.5 and 7.6 with $V_{DD} = 100mV$

Tables 7.2, 7.3, 7.4, 7.5 and 7.6 are constructed in the same order. The first column presents which device is tested. The next three columns gives the length (L) and the width (W) of the transistor gates. The next column sums up the gate area of one *nfet* and one *pfet*. Note that the real gate area will be larger than the ones listed in the tables for devices containing more than two transistors. The Ratio column gives the ratio between the width of the *pfet* gate and the *nfet* gate. The last column contains the value of the x-coordinate of the Switching Point

(SP_x). In these simulations the supply voltage was 100mV.

Table 7.1 presents the criterias for *balanced*, *good balance* and *perfect balance* at different supply voltages.

| V_{DD} (mV) | Perfect balance (mV) $(\frac{V_{DD}}{2})$ | Good balance (mV) $(V_{DD} \cdot 45\%)$ to $(V_{DD} \cdot 55\%)$ | Balanced (mV) $(V_{DD} \cdot 40\%)$ to $(V_{DD} \cdot 46\%)$ |
|---------------|--|---|---|
| 85 | 42.5 | 38.25 to 46.75 | 34 to 51 |
| 90 | 45 | 40.5 to 49.5 | 36 to 54 |
| 95 | 47.5 | 42.75 to 52.25 | 38 to 57 |
| 100 | 50 | 45 to 55 | 40 to 60 |
| 105 | 52.5 | 47.25 to 57.75 | 42 to 63 |

Table 7.1: Limits for balance quality at supply voltages from 85mV to 105mV

In table 7.2 are the sets of transistor gate sizes that gives the lowest gate area of one *nfet* and one *pfet* while beeing *balanced*. Table 7.3 presents the sets that have *good balance* and the lowest gate area.

| Device | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Area (fm^2) | Ratio ($\frac{m}{m}$) | SP_x (mV) |
|-------------|------------------|-----------|----------------|----------------|---------------------------|----------------------------|----------------|
| 2T inverter | 100 | 30.0 | 200 | 700 | 27.0 | 3.50 | 42.9 |
| 4T inverter | 100 | 30.0 | 200 | 700 | 27.0 | 3.50 | 42.7 |
| 4T NAND2 | 100 | 30.0 | 200 | 500 | 21.0 | 2.50 | 41.1 |
| 8T NAND2 | 100 | 30.0 | 200 | 1450 | 49.5 | 7.25 | 40.7 |
| 4T NOR2 | 100 | 30.0 | 200 | 1150 | 40.5 | 5.75 | 44.6 |
| 8T NOR2 | 100 | 30.0 | 200 | 450 | 19.5 | 2.25 | 47.6 |

Table 7.2: The sets of transistor gate sizes that give the smallest gate area. Devices are 2T and 4T Inverter, 4T and 8T NAND2, and 4T NOR2 and 8T NOR2. $V_{DD} = 100mV$

| Device | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Area (fm^2) | Ratio ($\frac{m}{m}$) | SP_x (mV) |
|-------------|------------------|-----------|----------------|----------------|---------------------------|----------------------------|----------------|
| 2T inverter | 100 | 30.0 | 200 | 800 | 30.0 | 4.00 | 46.2 |
| 4T inverter | 100 | 30.0 | 200 | 800 | 30.0 | 4.00 | 46.0 |
| 4T NAND2 | 100 | 30.0 | 200 | 600 | 24.0 | 3.00 | 47.1 |
| 8T NAND2 | 100 | 30.0 | 200 | 1750 | 58.5 | 8.75 | 45.6 |
| 4T NOR2 | 100 | 30.0 | 200 | 1300 | 45.0 | 6.50 | 48.1 |
| 8T NOR2 | 100 | 30.0 | 200 | 450 | 19.5 | 2.25 | 47.6 |

Table 7.3: The sets of transistor gate sizes that give the smallest gate area and has *good balance*. Devices are 2T and 4T Inverter, 4T and 8T NAND2, and 4T NOR2 and 8T NOR2. $V_{DD} = 100mV$

Table 7.4 presents the gate sizes that gives the larges gate area while still beeing *balanced*. Table 7.5 presents the gate sizes that gives the larges gate area while having *good balance*.

| Device | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Area (fm ²) | Ratio ($\frac{m}{m}$) | SP _x (mV) |
|-------------|------------------|-----------|----------------|----------------|----------------------------|----------------------------|-------------------------|
| 2T inverter | 100 | 40.0 | 350 | 2500 | 114 | 7.14 | 41.7 |
| 4T inverter | 100 | 40.0 | 300 | 2500 | 112 | 8.33 | 44.0 |
| 4T NAND2 | 100 | 40.0 | 500 | 2500 | 120 | 5.00 | 40.7 |
| 8T NAND2 | 100 | 35.0 | 200 | 2500 | 94.5 | 12.5 | 40.4 |
| 4T NOR2 | 100.0 | 35.0 | 250 | 2500 | 96.3 | 10.0 | 46.5 |
| 8T NOR2 | 100 | 40.0 | 700 | 2500 | 128 | 3.57 | 44.8 |

Table 7.4: The sets of transistor gate sizes that give the largest gate area and beeing *balanced*. Devices are 2T and 4T Inverter, 4T and 8T NAND2, and 4T NOR2 and 8T NOR2. $V_{DD} = 100mV$

| Device | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Area (fm ²) | Ratio ($\frac{m}{m}$) | SP _x (mV) |
|-------------|------------------|-----------|----------------|----------------|----------------------------|----------------------------|-------------------------|
| 2T inverter | 100 | 40.0 | 200 | 2500 | 108 | 12.5 | 51.5 |
| 4T inverter | 100 | 40.0 | 250 | 2500 | 110 | 10.0 | 47.2 |
| 4T NAND2 | 100 | 40.0 | 400 | 2500 | 116 | 6.25 | 45.3 |
| 8T NAND2 | 100 | 30.0 | 250 | 2500 | 82.5 | 10.0 | 49.5 |
| 4T NOR2 | 100 | 35.0 | 200 | 2450 | 92.8 | 12.3 | 51.2 |
| 8T NOR2 | 100 | 40.0 | 600 | 2500 | 124 | 4.17 | 48.1 |

Table 7.5: The sets of transistor gate sizes that give the largest gate area and having *good balance*. Devices are 2T and 4T Inverter, 4T and 8T NAND2, and 4T NOR2 and 8T NOR2. $V_{DD} = 100mV$

Table 7.6 contains the set of ransistor gate sizes with the lowest gate ratio between the width of the *pfet* and the *nfet*.

| Device | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Area (fm ²) | Ratio ($\frac{m}{m}$) | SP _x (mV) |
|-------------|------------------|-----------|----------------|----------------|----------------------------|----------------------------|-------------------------|
| 2T inverter | 100 | 30.0 | 800 | 2000 | 84.0 | 2.50 | 40.0 |
| 4T inverter | 100 | 30.0 | 800 | 2050 | 85.5 | 2.56 | 40.3 |
| 4T NAND2 | 100 | 30.0 | 800 | 1450 | 67.5 | 1.81 | 40.0 |
| 8T NAND2 | 100 | 30.0 | 300 | 2050 | 70.5 | 6.83 | 40.0 |
| 4T NOR2 | 100 | 30.0 | 450 | 2400 | 85.5 | 5.33 | 44.6 |
| 8T NOR2 | 100 | 30.0 | 800 | 1200 | 60.0 | 1.50 | 44.8 |

Table 7.6: Lowest ratio between the width of the *pfet* and the *nfet* at 100mV. Devices are 2T and 4T Inverter, 4T and 8T NAND2, and 4T and 8T NOR2. $V_{DD} = 100mV$

Noise margin

In table 7.7 are the sets of gate sizes with the ratio between the lower and higher noise margins closest to 1. Table 7.8 contains the set of transistor sizes that give the largest mean noise margin. In the two tables below, the first column gives which device is tested. The next three columns contain the transistor sizes, VNM_H is the higher noise margin while VNM_L is the lower noise margin. The next column contains the mean size of the noise margin. The last column presents the size of the undefined region.

| Device | L (nm) | W nfet (nm) | W pfet (nm) | VNM_H (mV) | VNM_L (mV) | Mean VNM (mV) | Undefined region (ΔmV) |
|-------------|--------|-------------|-------------|--------------|--------------|---------------|----------------------------------|
| 2T inverter | 40.0 | 200 | 2150 | 31.9 | 31.8 | 31.9 | 36.3 |
| 4T inverter | 35.0 | 200 | 2200 | 32.1 | 32.2 | 32.2 | 35.7 |
| 4T NAND2 | 30.0 | 600 | 1750 | 26.9 | 27.0 | 27.0 | 46.1 |
| 8T NAND2 | 30.0 | 200 | 2200 | 27.3 | 27.2 | 27.3 | 45.5 |
| 4T NOR2 | 30.0 | 250 | 1450 | 26.9 | 26.9 | 26.9 | 46.2 |
| 8T NOR2 | 40.0 | 400 | 1600 | 29.5 | 29.5 | 29.5 | 41.0 |

Table 7.7: The sets of transistor gate sizes that have the lowest ratio between the higher and lower noise margins at 100mV. Devices are 2T and 4T Inverter, 4T and 8T NAND2, and 4T NOR2 and 8T NOR2. $V_{DD} = 100mV$

| Device | L (nm) | W nfet (nm) | W pfet (nm) | VNM_H (mV) | VNM_L (mV) | Mean VNM (mV) | Undefined region (ΔmV) |
|-------------|--------|-------------|-------------|--------------|--------------|---------------|----------------------------------|
| 2T inverter | 40.0 | 200 | 2300 | 30.9 | 32.9 | 31.9 | 36.2 |
| 4T inverter | 40.0 | 200 | 2200 | 32.1 | 32.2 | 32.1 | 35.7 |
| 4T NAND2 | 40.0 | 450 | 2450 | 36.8 | 23.0 | 29.9 | 40.2 |
| 8T NAND2 | 35.0 | 200 | 2500 | 37.8 | 20.6 | 29.2 | 41.6 |
| 4T NOR2 | 40.0 | 200 | 2500 | 32.1 | 26.2 | 29.2 | 41.7 |
| 8T NOR2 | 40.0 | 550 | 2450 | 27.6 | 31.9 | 29.7 | 40.5 |

Table 7.8: The sets of transistor gate sizes that have the highest average noise margins at 100mV. Devices are 2T and 4T Inverter, 4T and 8T NAND2, and 4T NOR2 and 8T NOR2. $V_{DD} = 100mV$

The following figures illustrates how the noise margin is affected by changes in the supply voltage. The figures presents the mean noise margins and the relative mean noise margins. The mean is the average of the lower and higher noise margins. while the relative mean is the average divided by the supply voltage multiplied by 100%. The transistor gate sizes for the devices are the same as in table 7.7.

Inverter

Figure 7.2 presents the mean noise margin for the 2T and 4T inverters, and figure 7.3 presents the relative mean noise margin.

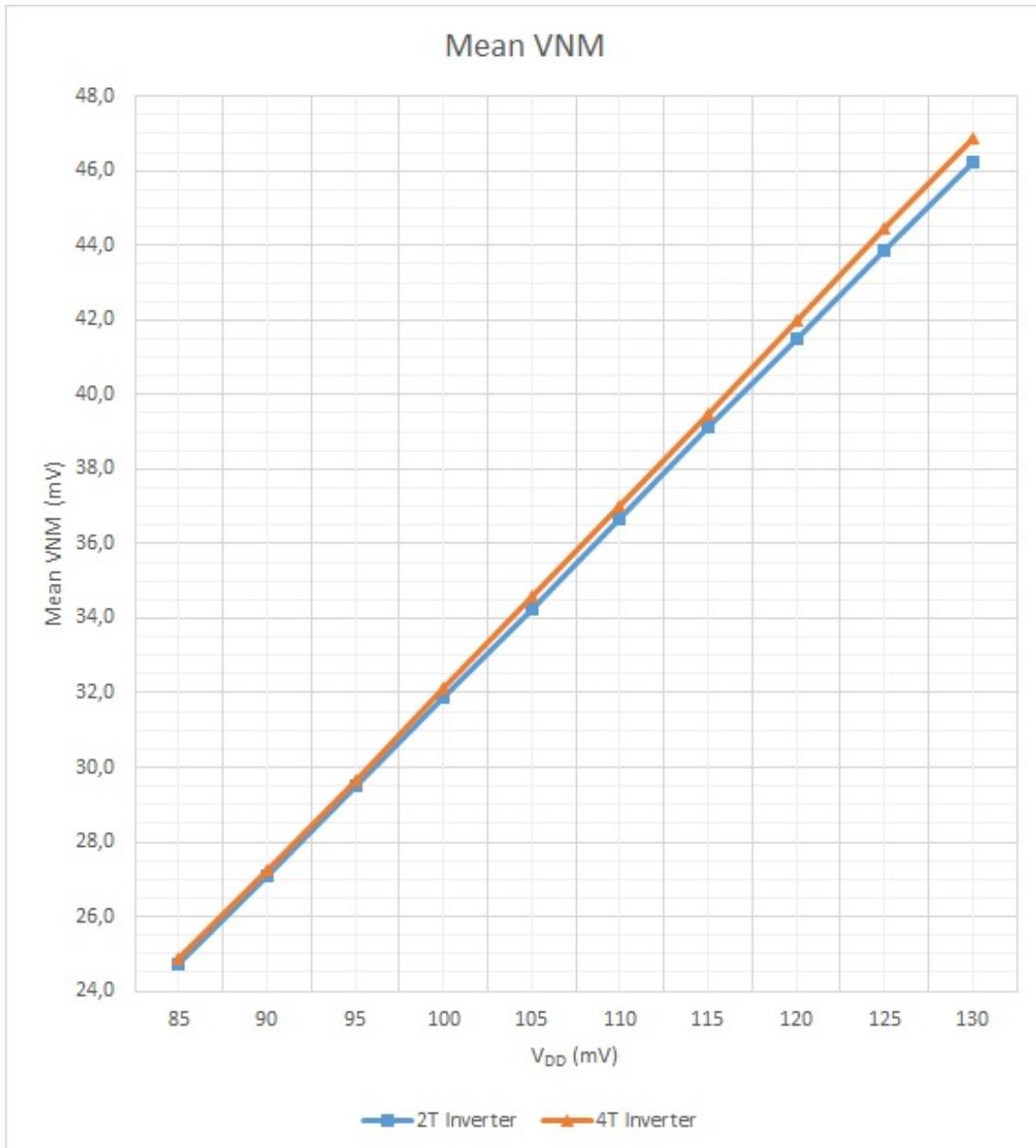


Figure 7.2: The mean noise margin in a 2T and a 4T Inverter at increasing supply voltage.

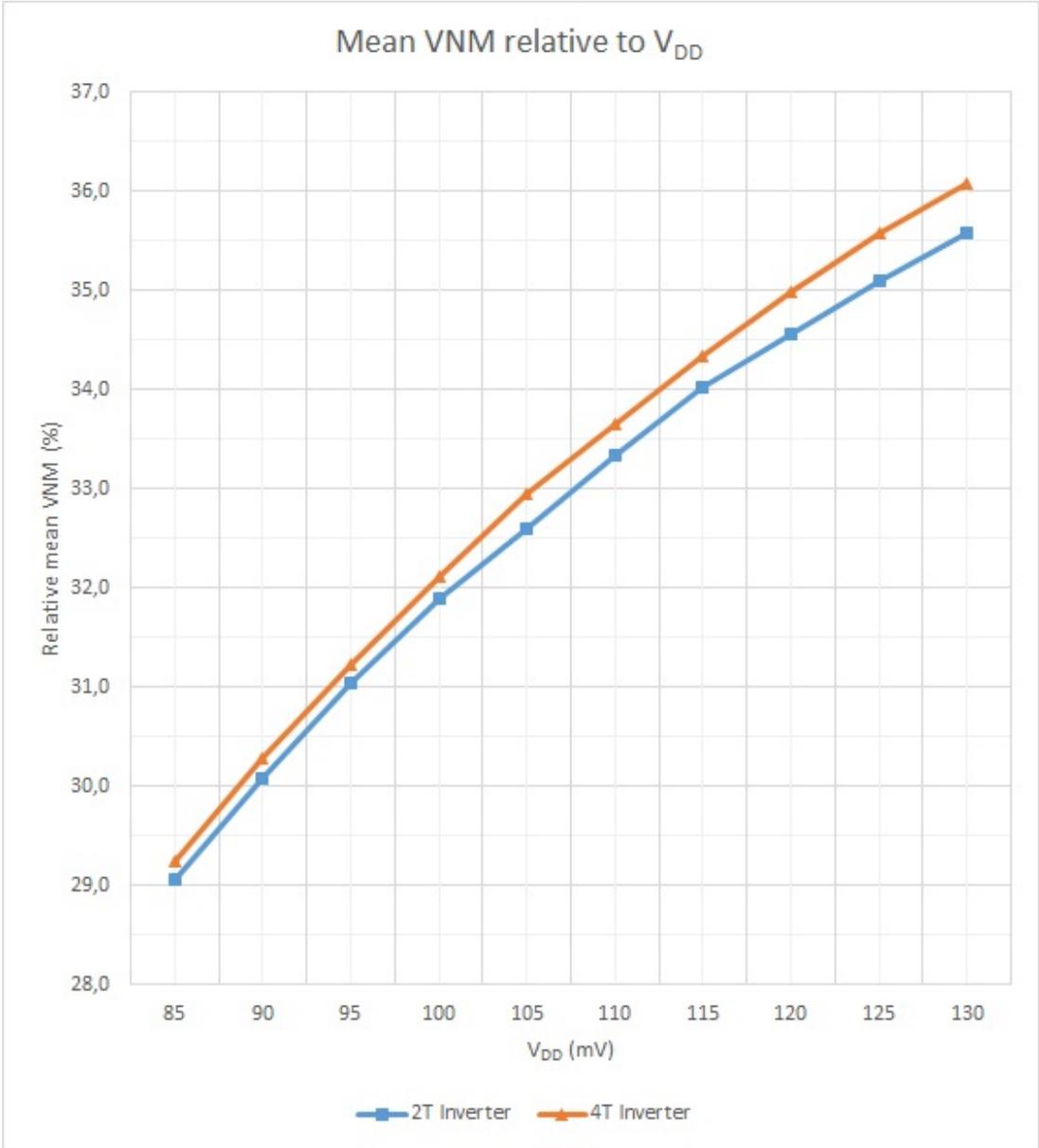


Figure 7.3: The mean noise margin relative to V_{DD} . Devices are 2T and 4T inverters

NAND2

Figure 7.4 presents the mean noise margin for the 4T and 8T NAND2 gates, and figure 7.5 presents the relative mean noise margin.

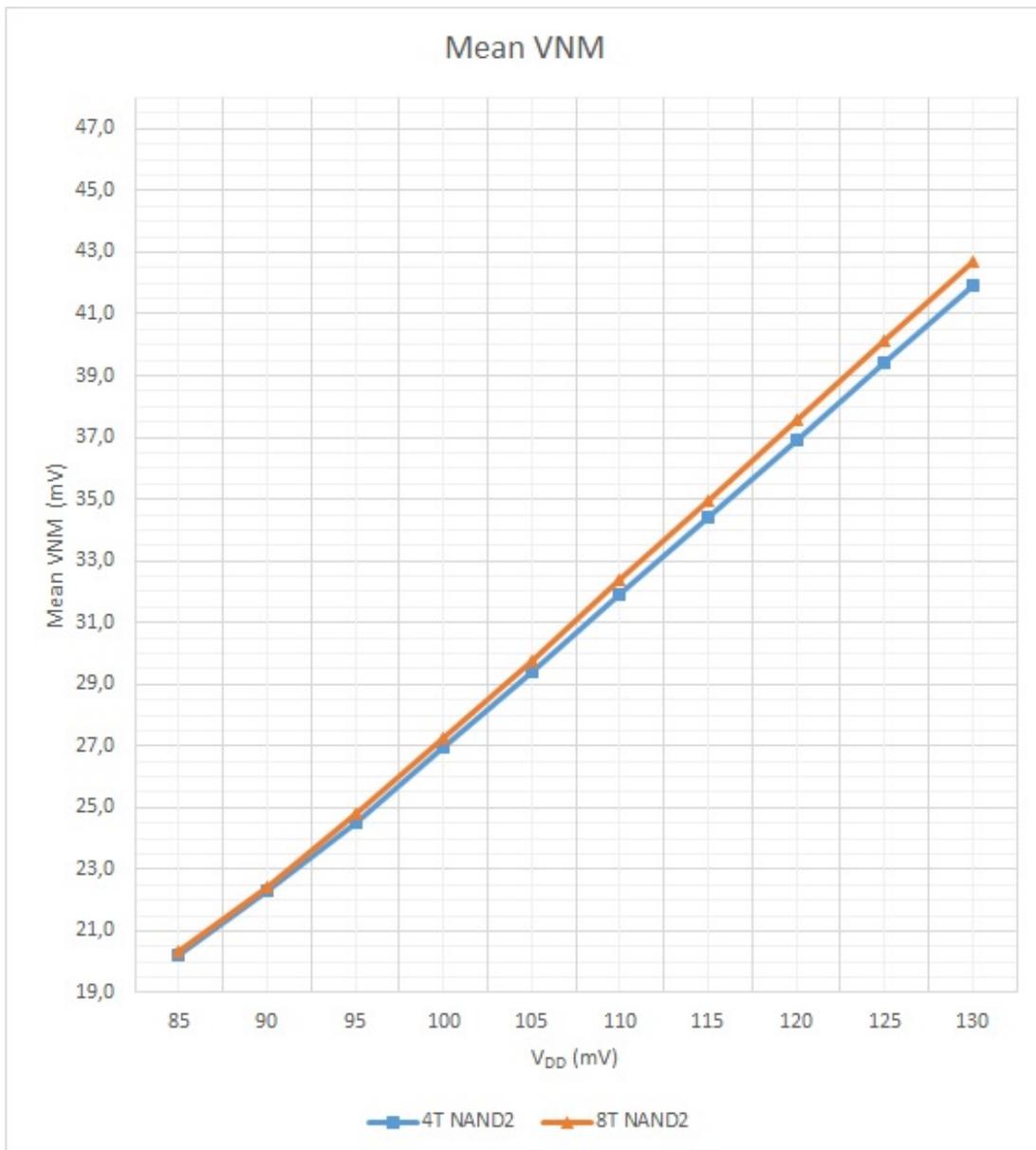


Figure 7.4: The mean noise margin in a 4T and a 8T NAND2 gate at increasing supply voltage.

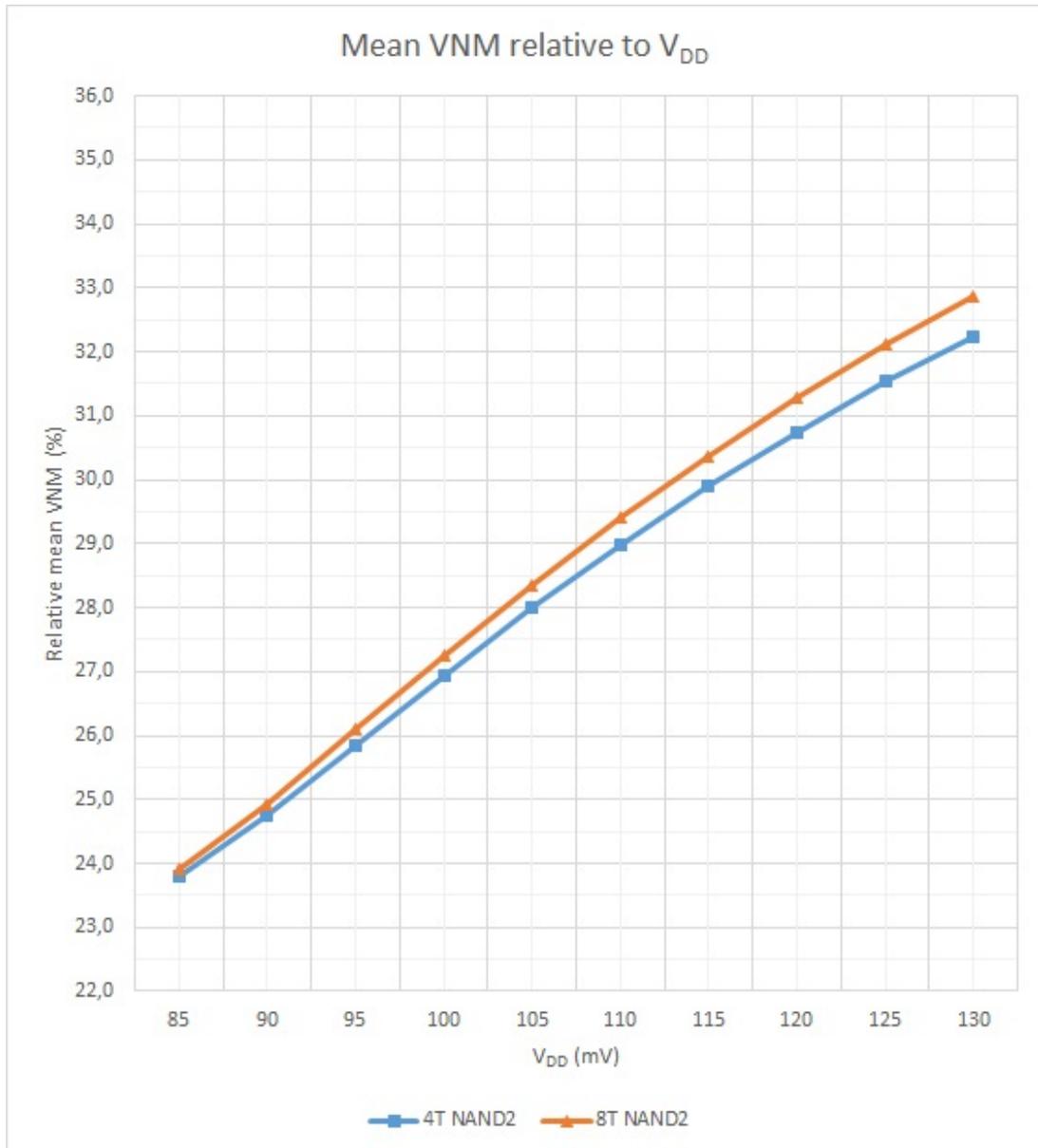


Figure 7.5: The mean noise margin relative to V_{DD} . Devices are 4T and 8T NAND2 gates.

NOR2

Figure 7.6 presents the mean noise margin for the 4T and 8T NAND2 gates, and figure 7.7 presents the relative mean noise margin.

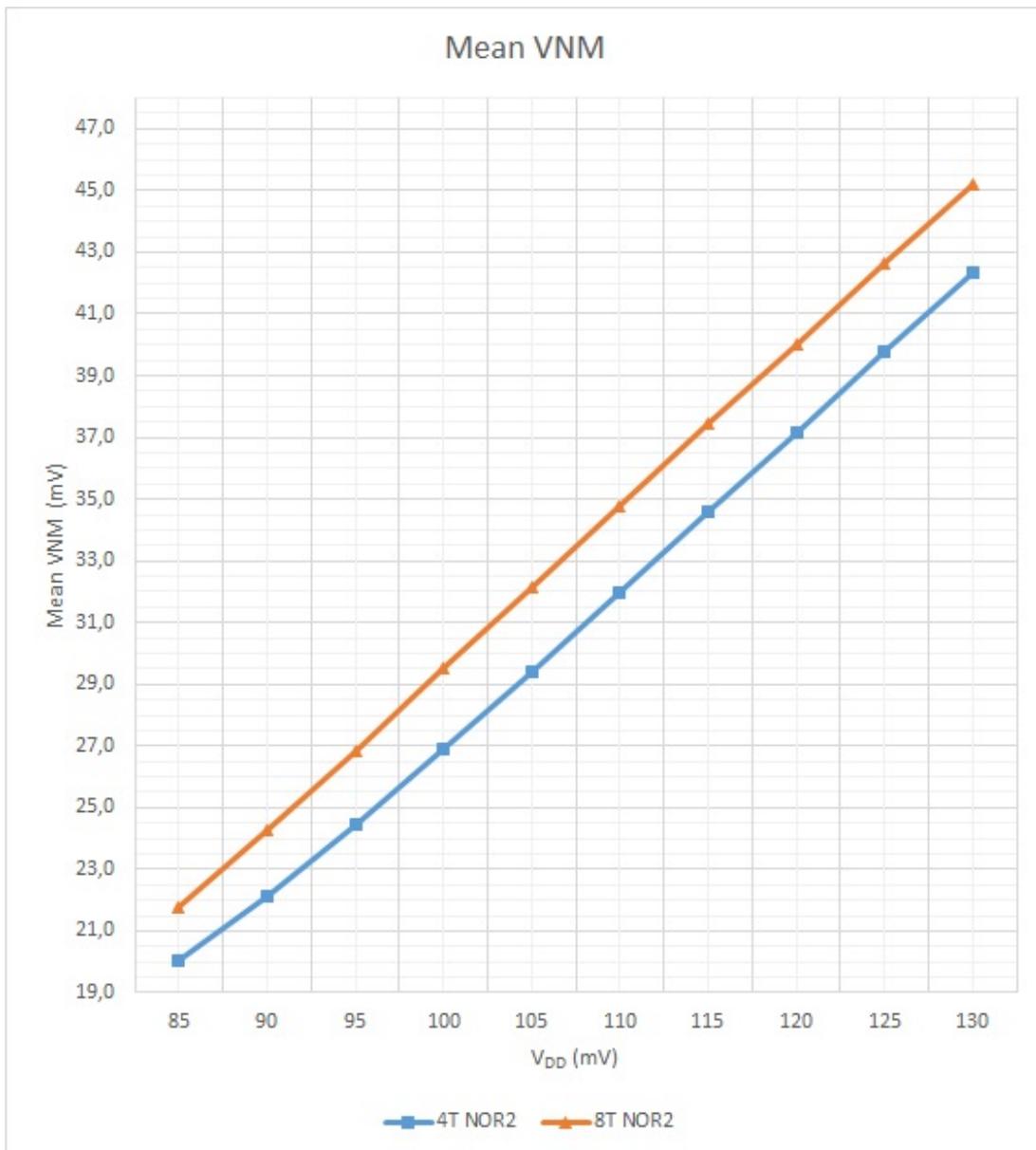


Figure 7.6: The mean noise margin in a 4T and a 8T NAND2 gate at increasing supply voltage.

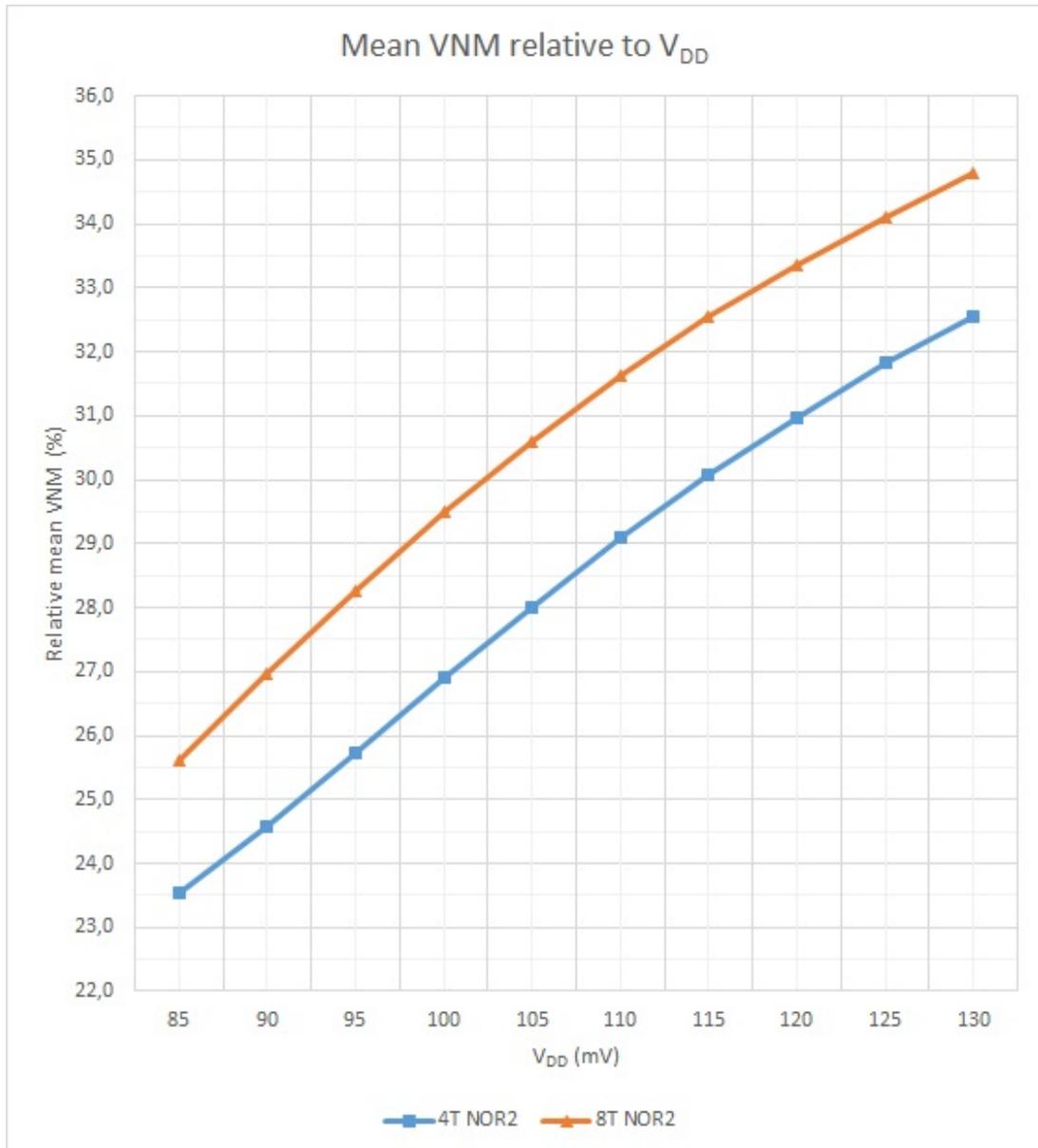


Figure 7.7: The mean noise margin relative to V_{DD} . Devices are 4T and 8T inverters.

7.2 Power and delay

7.2.1 Power delay product

In this chapter the power, delay and power delay product of the logical gates are presented graphically. Each graph contains two devices of the same type, but with different topology. The transistor gate sizes are low area and *good balance*, the same as in table 7.3.

The delay graphs show how the delay relates to an increasing V_{DD} . V_{DD} is increasing from 85mV to 130mV with a step size of 5mV. The power graphs show how the power consumption in the device is related to V_{DD} . The power delay product (PDP) is power and delay multiplied together. The graphs with PDP shows how it behaves with an increasing V_{DD} .

Inverter

Figure 7.8 shows the power in the 2T and 4T inverters. Figure 7.9 shows the delay in the inverters, while figure 7.10 presents the power delay product.

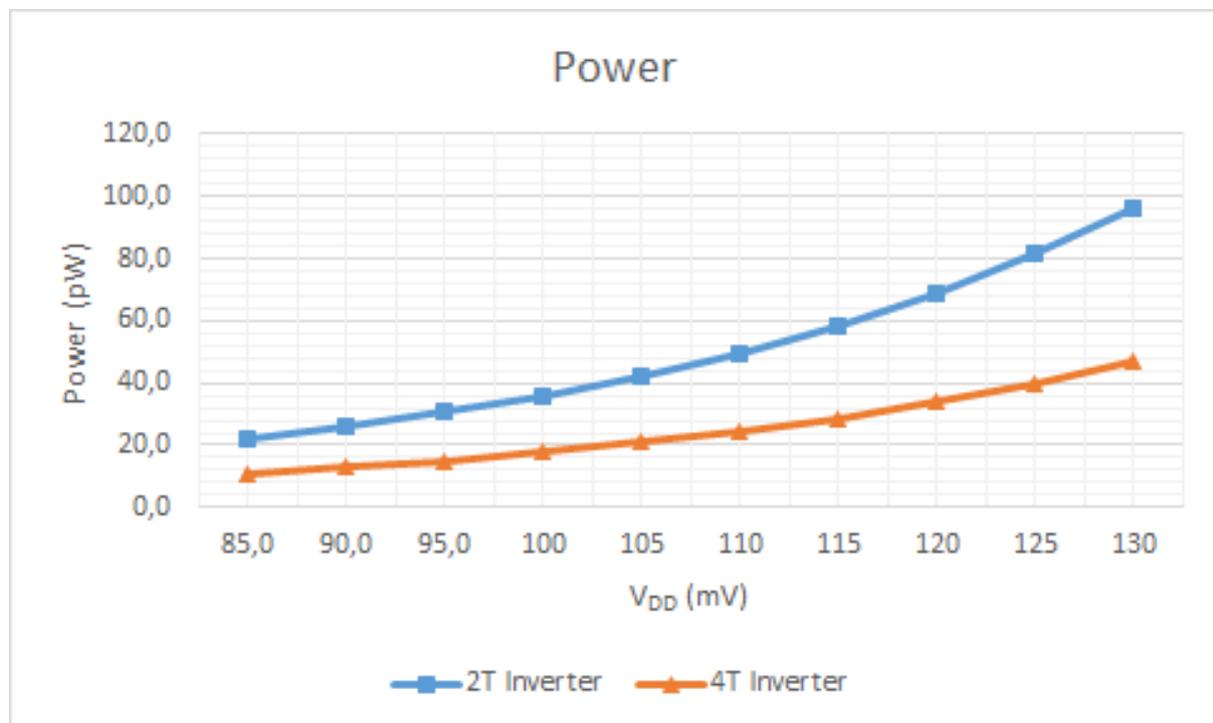


Figure 7.8: The power consumption in the ring oscillators constructed of 2T and 4T inverters. V_{DD} was increased from 85mV to 130mV.

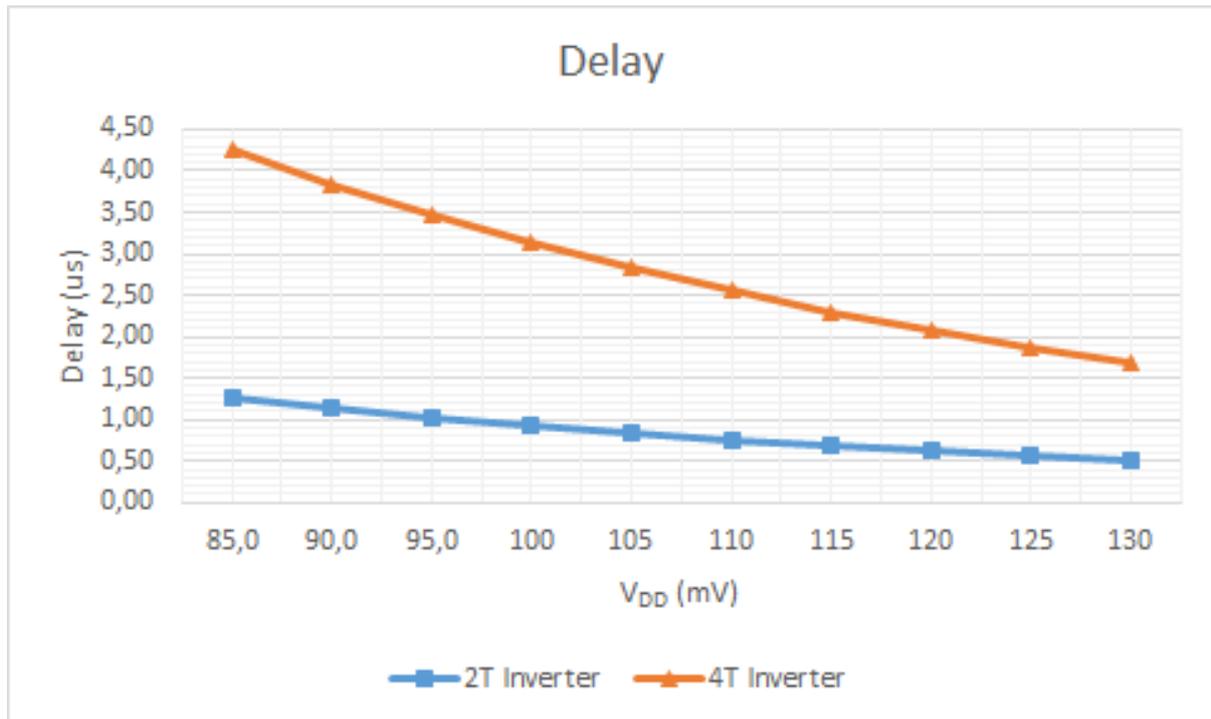


Figure 7.9: The delay in the ring oscillators constructed of 2T and 4T inverters. V_{DD} was increased from 85mV to 130mV.

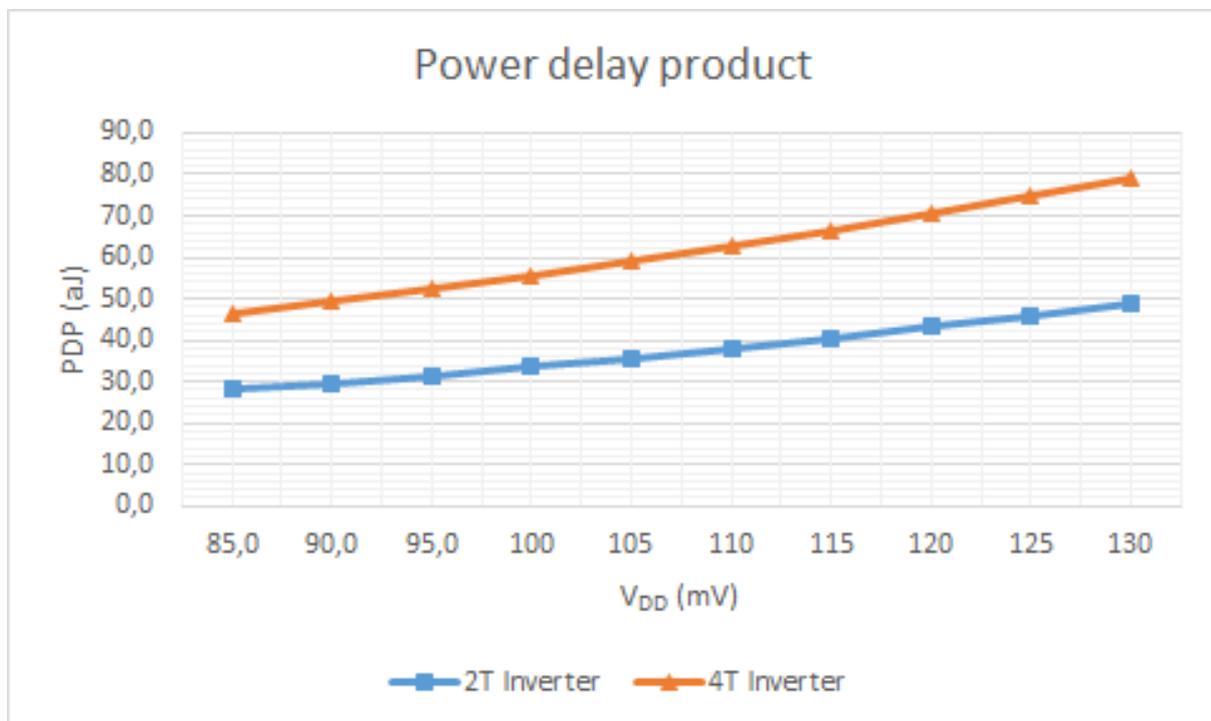


Figure 7.10: The power delay product in the ring oscillators constructed of 2T and 4T inverters. V_{DD} was increased from 85mV to 130mV.

NAND2

Figure 7.11 shows the power in the 4T and 8T NAND2 gates. Figure 7.12 shows the delay in the NAND2 gates, while figure 7.13 presents the power delay product.

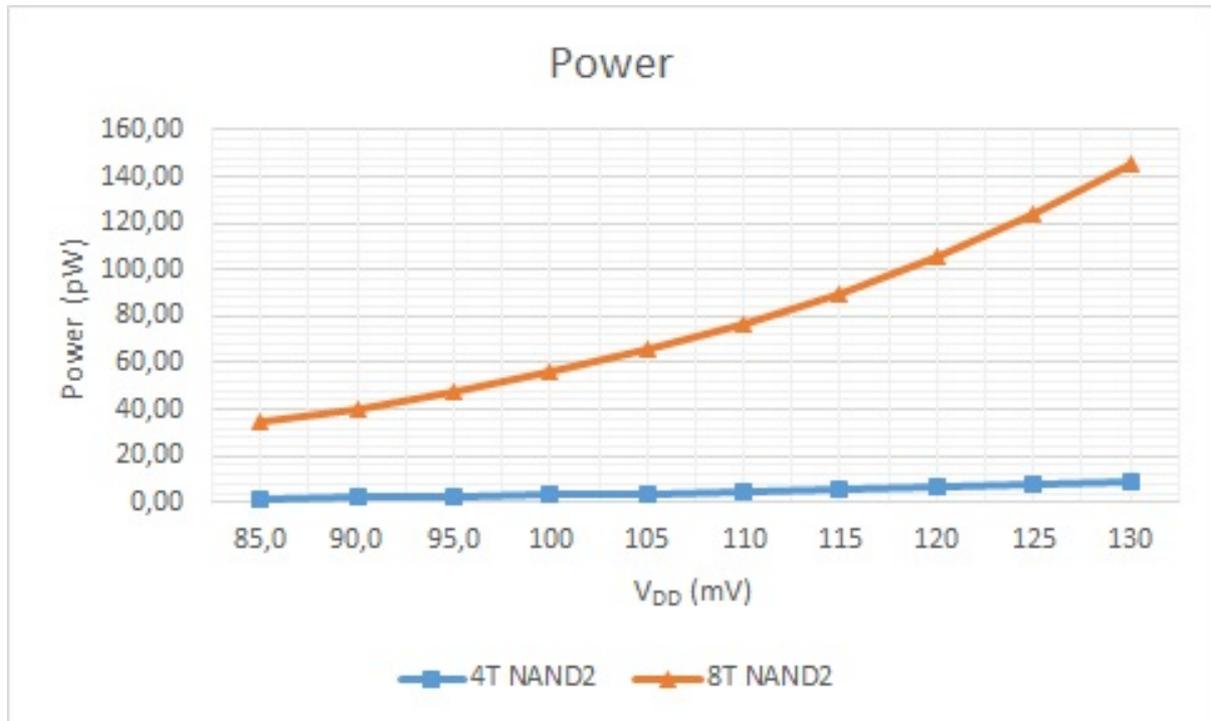


Figure 7.11: The power consumption in the ring oscillators constructed of 4T and 8T NAND2 gates. V_{DD} was increased from 85mV to 130mV.

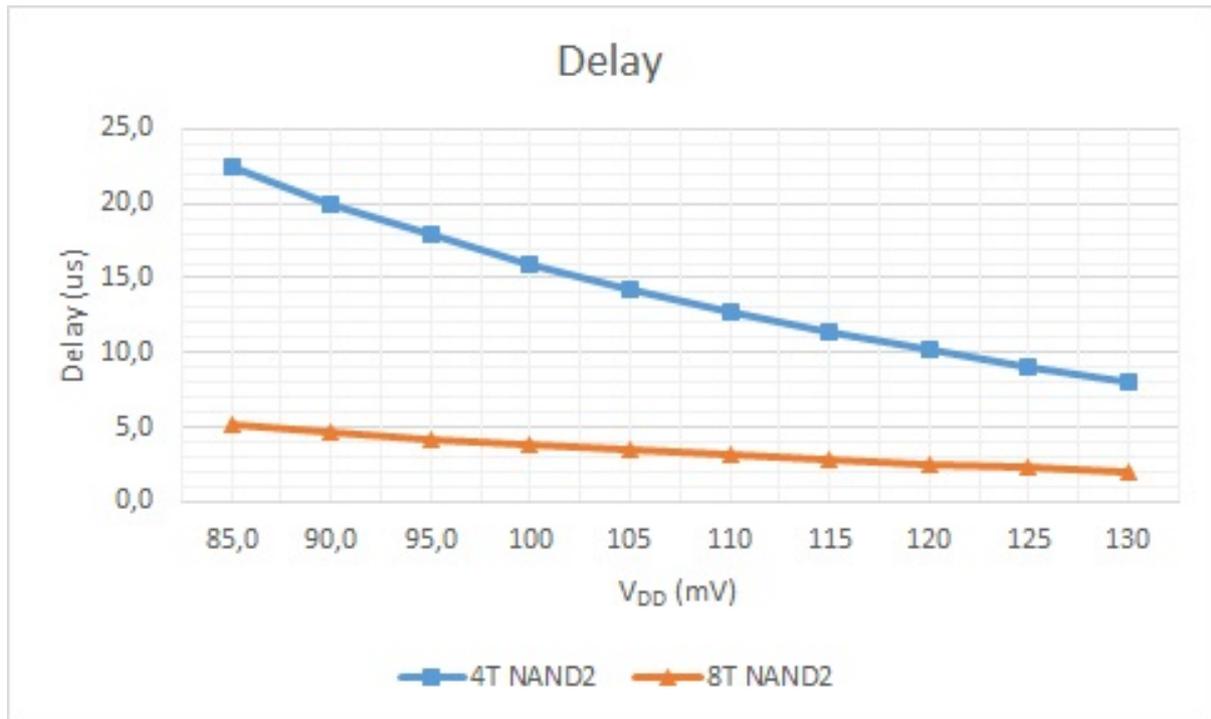


Figure 7.12: The delay in the ring oscillators constructed of 4T and 8T NAND2 gates. V_{DD} was increased from 85mV to 130mV.

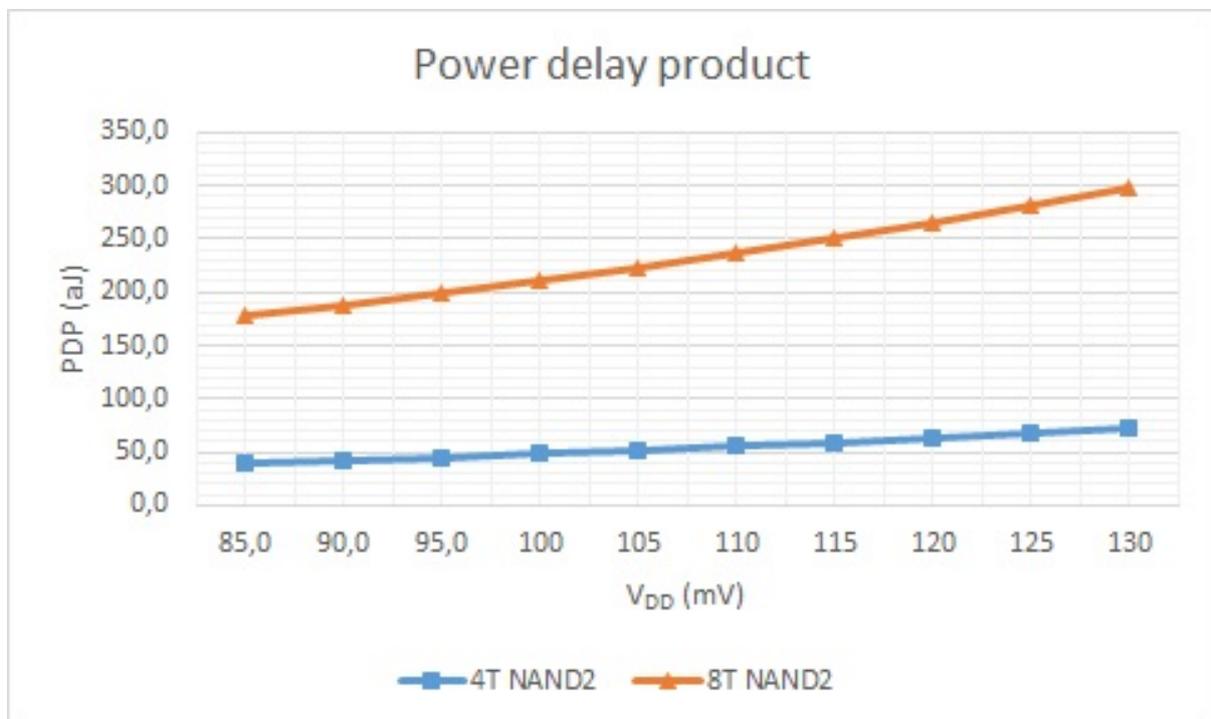


Figure 7.13: The power delay product in the ring oscillators constructed of 4T and 8T NAND2 gates. V_{DD} was increased from 85mV to 130mV.

NOR2

Figure 7.14 shows the power in the 4T and 8T NOR2 gates. Figure 7.15 shows the delay in the NAND2 gates, while figure 7.16 presents the power delay product.

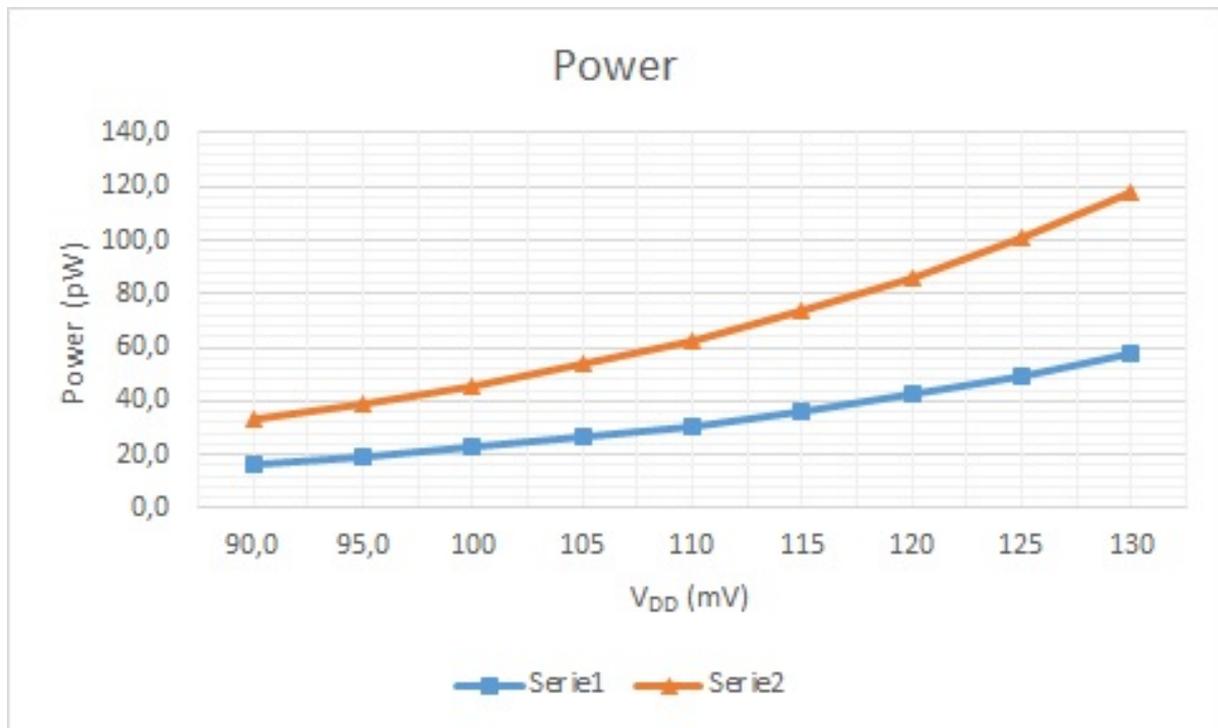


Figure 7.14: The power consumption in the ring oscillators constructed of 4T and 8T NOR2 gates. V_{DD} was increased from 90mV to 130mV.

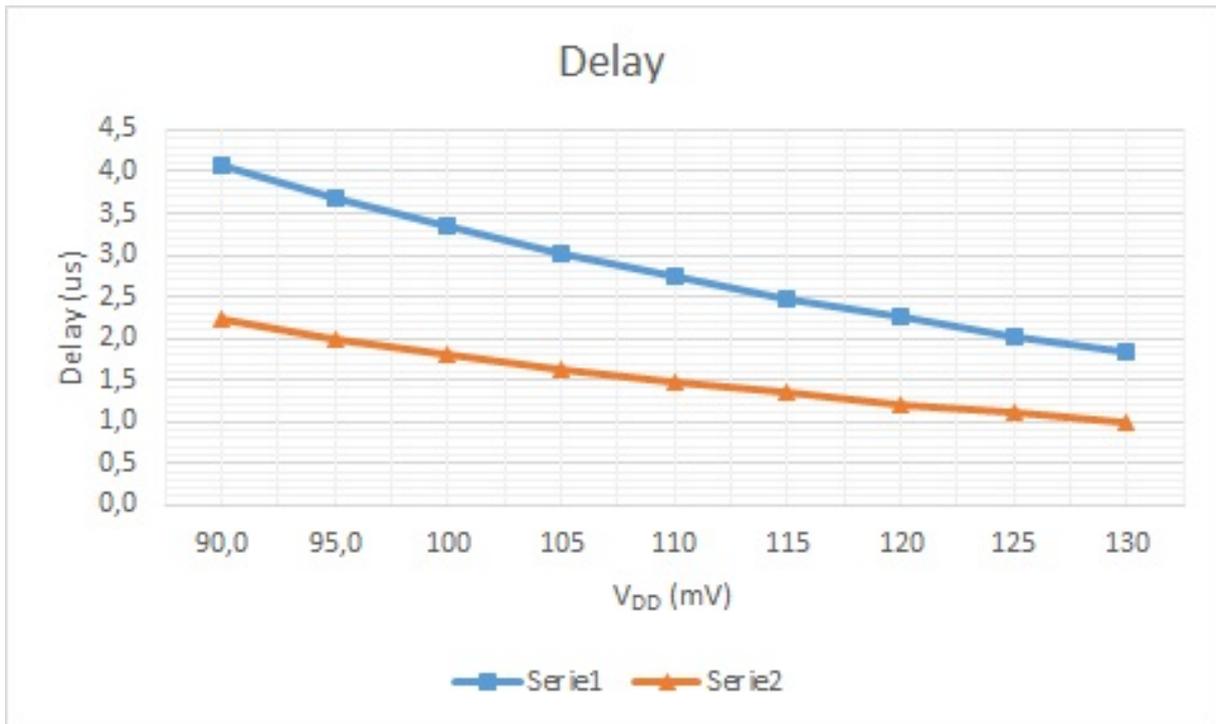


Figure 7.15: The delay in the ring oscillators constructed of 4T and 8T NOR2 gates. V_{DD} was increased from 90mV to 130mV.

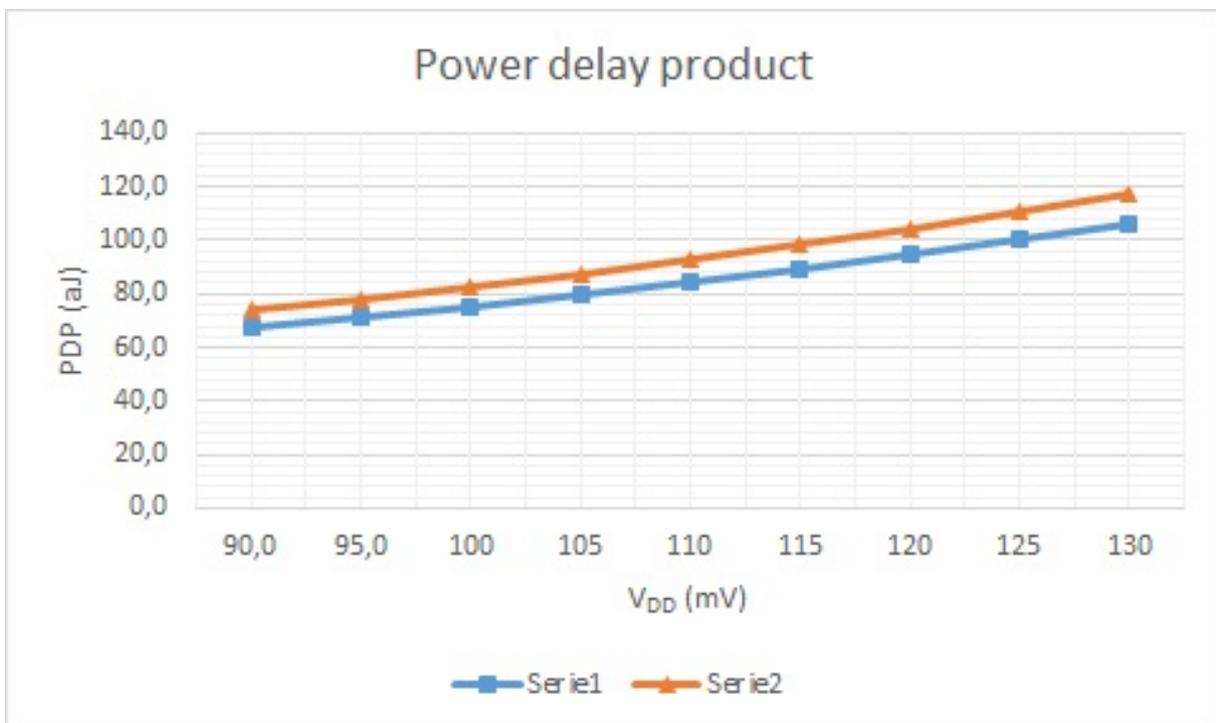


Figure 7.16: The power delay product in the ring oscillators constructed of 4T and 8T NOR2 gates. V_{DD} was increased from 90mV to 130mV

7.2.2 Minimum supply voltage

Below in table 7.9 are the lowest supply voltages that supports stable oscillations, oscillations between 25% and 75% of V_{DD} , and 5% and 95% of V_{DD} in the ring oscillator. Figure 7.17 illustrates this.

| Device | VDD (mV) stable | VDD (mV) 25% - 75% | VDD (mV) 5% - 95% |
|-------------|--------------------|-----------------------|----------------------|
| 2T Inverter | 73 | 79 | 108 |
| 4T Inverter | 71 | 78 | 104 |
| | | | |
| 4T NAND2 | 73 | 78 | 105 |
| 8T NAND2 | 73 | 78 | 104 |
| | | | |
| 4T NOR2 | 75 | 86 | 115 |
| 8T NOR2 | 72 | 78 | 104 |

Table 7.9: The minimum supply voltage in the ring oscillators constructed of the logical gates.

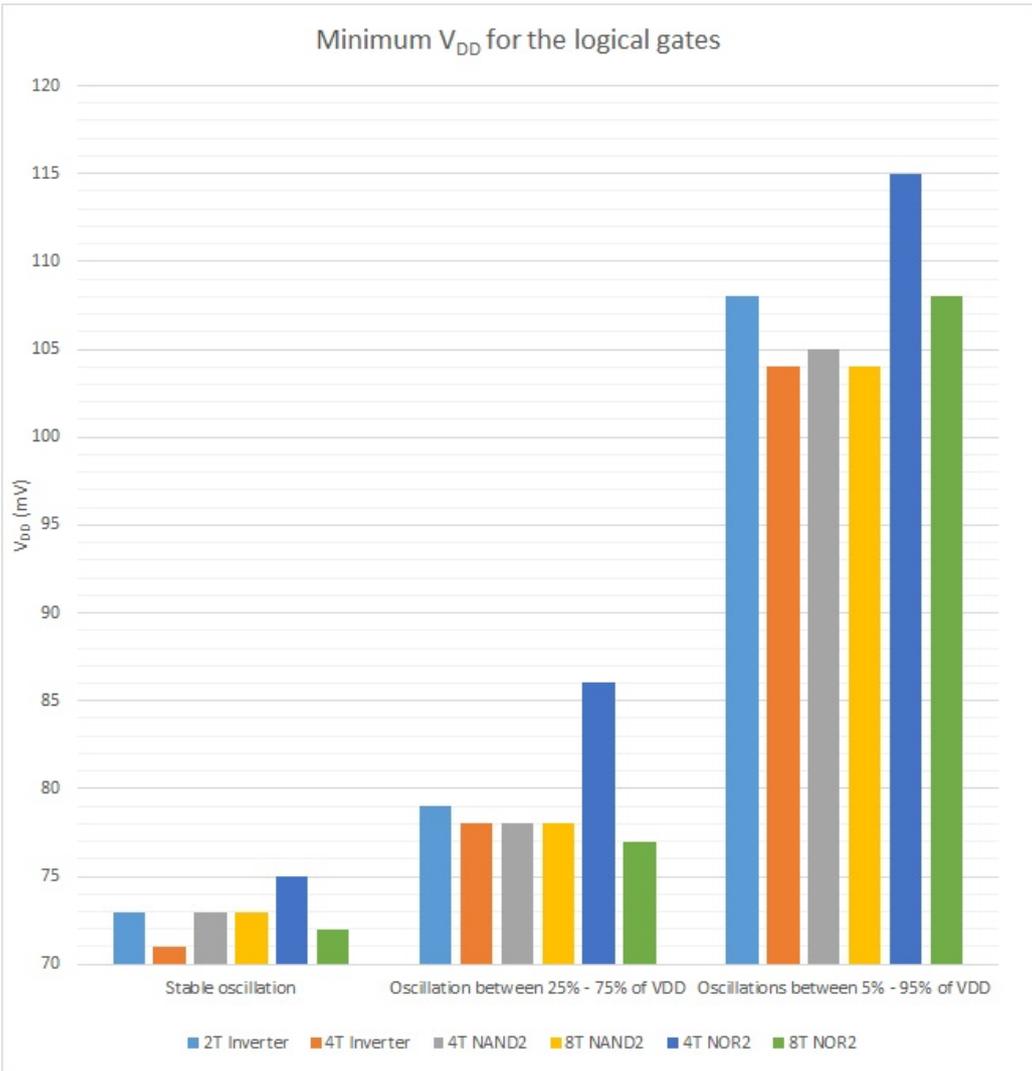


Figure 7.17: The minimum supply voltage in the ring oscillators constructed of the logical gates

Here are the sets of transistor gate sizes that have the lowest power consumption and lowest delay at stable oscillations, oscillations between 25% and 75% of V_{DD} , and 5% and 95% of V_{DD} in a ring oscillator. The tables below are constructed in the following manner. The first column contains a description of how the signal is oscillating (stable oscillations, oscillations between 25% and 75% of V_{DD} or 5% and 95% of V_{DD}). The next column contains the supply voltage. The next three columns list the transistor gate dimensions (Length, Width $nfet$ and Width $pfet$). The delay column contains the average delay. The last column contains the average power consumption.

Inverter

Table 7.10 contains the sets of transistor gate sizes that give the lowest supply voltages and lowest power in the ring oscillator. Table 7.11 presents the sets with the lowest supply voltage and lowest delay. Table 7.12 presents the sets with the lowest supply voltage and lowest power delay product.

| Device | Oscillation | V_{DD} (mV) | L (nm) | W $nfet$ (nm) | W $pfet$ (nm) | Mean delay (μs) | Power (pW) | PDP (aj) |
|-------------|------------------------------------|------------------|-----------|------------------|------------------|---------------------------|---------------|-------------|
| 2T inverter | Stable | 73.0 | 40.0 | 250 | 2150 | 20.8 | 2.06 | 42.1 |
| 2T inverter | Between 25% and 75% of V_{DD} | 79.0 | 40.0 | 200 | 2250 | 18.1 | 2.98 | 53.8 |
| 2T inverter | Between 5% and 95% of V_{DD} | 108 | 40.0 | 200 | 2150 | 9.32 | 8.35 | 77.8 |
| 4T inverter | Stable | 71.0 | 40.0 | 200 | 2000 | 72.7 | 1.04 | 75.5 |
| 4T inverter | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 200 | 1950 | 59.8 | 1.32 | 78.9 |
| 4T inverter | Between 5% and 95% of V_{DD} | 104 | 40.0 | 200 | 1950 | 32.9 | 3.37 | 111 |

Table 7.10: The sets of transistor gate sizes that use the lowest supply voltage and have the lowest power consumption. Devices are 2T and 4T Inverters

| Device | Oscillation | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Mean delay (μ s) | Power (pW) | PDP (aj) |
|-------------|------------------------------------|------------------|-----------|----------------|----------------|--------------------------|---------------|-------------|
| 2T inverter | Stable | 73.0 | 40.0 | 200 | 1700 | 19.7 | 2.73 | 53.9 |
| 2T inverter | Between 25% and 75% of V_{DD} | 79.0 | 40.0 | 200 | 2250 | 18.1 | 2.98 | 53.8 |
| 2T inverter | Between 5% and 95% of V_{DD} | 108 | 40.0 | 200 | 2150 | 9.32 | 8.35 | 77.8 |
| 4T inverter | Stable | 71.0 | 40.0 | 250 | 2350 | 70.0 | 1.28 | 89.3 |
| 4T inverter | Between 25% and 75% of V_{DD} | 79.0 | 40.0 | 250 | 2450 | 58.6 | 1.68 | 98.3 |
| 4T inverter | Between 5% and 95% of V_{DD} | 104 | 40.0 | 200 | 2450 | 32.2 | 4.29 | 138 |

Table 7.11: The sets of transistor gate sizes that uses the lowest supply voltage and have the lowest delay. Devices are 2T and 4T Inverters

| Device | Oscillation | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Mean delay (μ s) | Power (pW) | PDP (aj) |
|-------------|------------------------------------|------------------|-----------|----------------|----------------|--------------------------|---------------|-------------|
| 2T inverter | Stable | 73.0 | 40.0 | 250 | 2150 | 20.8 | 2.06 | 42.1 |
| 2T inverter | Between 25% and 75% of V_{DD} | 79.0 | 40.0 | 200 | 2250 | 18.1 | 2.98 | 53.8 |
| 2T inverter | Between 5% and 95% of V_{DD} | 108 | 40.0 | 200 | 2150 | 9.32 | 8.35 | 77.8 |
| 4T inverter | Stable | 71.0 | 40.0 | 200 | 2000 | 72.7 | 1.04 | 75.5 |
| 4T inverter | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 200 | 1950 | 59.8 | 1.32 | 78.9 |
| 4T inverter | Between 5% and 95% of V_{DD} | 104 | 40.0 | 200 | 1950 | 32.9 | 3.37 | 111 |

Table 7.12: The sets of transistor gate sizes that use the lowest supply voltage and have the lowest power delay product. Devices are 2T and 4T Inverters

NAND2

Table 7.13 containst the sets of transistor gate sizes that gives the lowest supply voltages and lowest power in the ring oscillator. Table 7.14 presents the sets with the lowest supply voltage and lowest delay. Table 7.15 presents the sets with the lowest supply voltage and lowest power delay product.

| Device | Oscillation | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Mean delay (μ s) | Power (pW) | PDP (aj) |
|----------|------------------------------------|------------------|-----------|----------------|----------------|--------------------------|---------------|-------------|
| 4T NAND2 | Stable | 73.0 | 40.0 | 200 | 700 | 30.5 | 1.24 | 37.8 |
| 4T NAND2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 450 | 1400 | 22.9 | 3.40 | 77.9 |
| 4T NAND2 | Between 5% and 95% of V_{DD} | 106 | 40.0 | 300 | 950 | 13.1 | 6.11 | 79.9 |
| 8T NAND2 | Stable | 73.0 | 40.0 | 300 | 1950 | 62.1 | 2.70 | 168 |
| 8T NAND2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 200 | 1950 | 59.8 | 2.94 | 176 |
| 8T NAND2 | Between 5% and 95% of V_{DD} | 104 | 40.0 | 200 | 1950 | 32.9 | 6.75 | 222 |

Table 7.13: The sets of transistor gate sizes that uses the lowest supply voltage and have the lowest power consumption.

| Device | Oscillation | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Mean delay (μ s) | Power (pW) | PDP (aj) |
|----------|------------------------------------|------------------|-----------|----------------|----------------|--------------------------|---------------|-------------|
| 4T NAND2 | Stable | 73.0 | 40.0 | 750 | 2200 | 24.3 | 4.72 | 115 |
| 4T NAND2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 800 | 2400 | 21.7 | 6.12 | 133 |
| 4T NAND2 | Between 5% and 95% of V_{DD} | 106 | 40.0 | 750 | 2150 | 11.4 | 15.4 | 176 |
| 8T NAND2 | Stable | 73.0 | 40.0 | 300 | 2100 | 59.3 | 2.82 | 167 |
| 8T NAND2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 250 | 2450 | 58.6 | 3.36 | 197 |
| 8T NAND2 | Between 5% and 95% of V_{DD} | 108 | 40.0 | 250 | 2450 | 32.2 | 8.59 | 277 |

Table 7.14: The sets of transistor gate sizes that uses the lowest supply voltage and have the lowest delay.

| Device | Oscillation | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Mean delay (μ s) | Power (pW) | PDP (aj) |
|----------|------------------------------------|------------------|-----------|----------------|----------------|--------------------------|---------------|-------------|
| 4T NAND2 | Stable | 73.0 | 40.0 | 200 | 700 | 30.5 | 1.24 | 37.8 |
| 4T NAND2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 450 | 1400 | 22.9 | 3.40 | 77.9 |
| 4T NAND2 | Between 5% and 95% of V_{DD} | 106 | 40.0 | 300 | 950 | 13.1 | 6.11 | 79.9 |
| 8T NAND2 | Stable | 73.0 | 40.0 | 300 | 2000 | 60.3 | 2.74 | 165 |
| 8T NAND2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 200 | 1950 | 59.8 | 2.94 | 176 |
| 8T NAND2 | Between 5% and 95% of V_{DD} | 104 | 40.0 | 200 | 1950 | 32.9 | 6.75 | 222 |

Table 7.15: The sets of transistor gate sizes that uses the lowest supply voltage and have the lowest power delay product.

NOR2

Table 7.16 containst the sets of transistor gate sizes that gives the lowest supply voltages and lowest power in the ring oscillator. Table 7.17 presents the sets with the lowest supply voltage and lowest delay. Table 7.18 presents the sets with the lowest supply voltage and lowest power delay product.

| Device | Oscillation | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Mean delay (μ s) | Power (pW) | PDP (aJ) |
|---------|------------------------------------|------------------|-----------|----------------|----------------|--------------------------|---------------|-------------|
| 4T NOR2 | Stable | 75.0 | 35.0 | 200 | 3100 | 22.0 | 8.79 | 193 |
| 4T NOR2 | Between 25% and 75% of V_{DD} | 86.0 | 35.0 | 200 | 3750 | 11.9 | 13.8 | 165 |
| 4T NOR2 | Between 5% and 95% of V_{DD} | 115 | 35.0 | 200 | 3950 | 6.48 | 38.8 | 251 |
| 8T NOR2 | Stable | 72.0 | 40.0 | 200 | 1550 | 65.2 | 1.87 | 122 |
| 8T NOR2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 200 | 1950 | 59.8 | 2.64 | 158 |
| 8T NOR2 | Between 5% and 95% of V_{DD} | 104 | 40.0 | 200 | 1950 | 32.9 | 6.74 | 222 |

Table 7.16: The sets of transistor gate sizes that uses the lowest supply voltage and have the lowest power consumption.

| Device | Oscillation | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Mean delay (μ s) | Power (pW) | PDP (aj) |
|---------|------------------------------------|------------------|-----------|----------------|----------------|--------------------------|---------------|-------------|
| 4T NOR2 | Stable | 75.0 | 35.0 | 200 | 3550 | 15.0 | 9.50 | 142 |
| 4T NOR2 | Between 25% and 75% of V_{DD} | 86.0 | 35.0 | 200 | 3750 | 11.9 | 13.8 | 165 |
| 4T NOR2 | Between 5% and 95% of V_{DD} | 115 | 35.0 | 200 | 3950 | 6.48 | 38.8 | 251 |
| 8T NOR2 | Stable | 72.0 | 40.0 | 300 | 2350 | 63.3 | 2.90 | 184 |
| 8T NOR2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 200 | 2000 | 60.3 | 2.68 | 161 |
| 8T NOR2 | Between 5% and 95% of V_{DD} | 104 | 40.0 | 250 | 2500 | 31.8 | 8.67 | 276 |

Table 7.17: The sets of transistor gate sizes that uses the lowest supply voltage and have the lowest delay.

| Device | Oscillation | V_{DD} (mV) | L (nm) | W nfet (nm) | W pfet (nm) | Mean delay (μ s) | Power (pW) | PDP (aj) |
|---------|------------------------------------|------------------|-----------|----------------|----------------|--------------------------|---------------|-------------|
| 4T NOR2 | Stable | 75.0 | 35.0 | 200 | 3450 | 15.1 | 9.35 | 141 |
| 4T NOR2 | Between 25% and 75% of V_{DD} | 86.0 | 35.0 | 200 | 3750 | 11.9 | 13.8 | 165 |
| 4T NOR2 | Between 5% and 95% of V_{DD} | 115 | 35.0 | 200 | 3950 | 6.48 | 38.8 | 251 |
| 8T NOR2 | Stable | 72.0 | 40.0 | 200 | 1550 | 65.2 | 1.87 | 122 |
| 8T NOR2 | Between 25% and 75% of V_{DD} | 78.0 | 40.0 | 200 | 1950 | 59.8 | 2.64 | 158 |
| 8T NOR2 | Between 5% and 95% of V_{DD} | 104 | 40.0 | 200 | 1950 | 32.9 | 6.74 | 222 |

Table 7.18: The sets of transistor gate sizes that uses the lowest supply voltage and have the lowest delay.

7.3 Robustness

Monte Carlo analyses were performed on the following sets of transistor gate sizes.

- The sets with the lowest gate area and having *good balance* (Low area & GB, table 7.3).
- The sets with the largest gate area and having *good balance* (Large area & GB, table 7.5).
- The sets with the lowest ratio between the width of the *pfet* and the *nfet* (Low size ratio, table 7.6)
- The sets with the lowest ratio between the higher and lower noise margins (Low VNM ratio, table 7.7).
- The sets with the lowest supply voltage and the power delay product in the ring oscillator (Low V_{DD} & low PDP, table 7.12, 7.15 and 7.18).

Inverter

Table presents the different sets of transistor gate sizes from the 2T and 4T inverters. The first column gives the device. The next column states the names of the size sets. The next three columns presents the gate sizes. The area column gives the total gate area for the device, while the ratio column gives the size ratio between the *pfet* and the *nfet*.

| Device | Size set name | L (nm) | W nfet (nm) | W pfet (nm) | Area fm^2 | Ratio ($\frac{m}{m}$) |
|-------------|------------------------|--------|-------------|-------------|--------------------|-------------------------|
| 2T Inverter | Low area & GB | 30.0 | 200 | 800 | 30.0 | 4.00 |
| 2T Inverter | Low size ratio | 30.0 | 800 | 2150 | 88.5 | 2.69 |
| 2T Inverter | Low VNM ratio | 40.0 | 200 | 2150 | 94.0 | 10.8 |
| 2T Inverter | Low V_{DD} & low PDP | 40.0 | 200 | 2150 | 94.0 | 10.8 |
| 2T Inverter | Large area & GB | 40.0 | 200 | 2500 | 108 | 12.5 |
| | | | | | | |
| 4T Inverter | Low area & GB | 30.0 | 200 | 800 | 60.0 | 4.00 |
| 4T Inverter | Low size ratio | 30.0 | 800 | 2050 | 171 | 2.56 |
| 4T Inverter | Low VNM ratio | 35.0 | 200 | 2200 | 168 | 11.0 |
| 4T Inverter | Low V_{DD} & low PDP | 40.0 | 200 | 1950 | 172 | 9.75 |
| 4T Inverter | Large area & GB | 40.0 | 250 | 2500 | 220 | 10.0 |

Table 7.19: Names of transistor gate size sets. Devices are 2T and 4T Inverters.

Table 7.20 contains the results of the Monte Carlo analysis of the 2T and 4T inverters. Here are the mean value and the standard deviation of SP_x , the lower and the higher noise margin (VNM_L and VNM_H). Test was performed with 200 samples, and all samples passed (100% yield).

| Device | Size set name | Mean SP_x (mV) | σ SP_x (mV) | Mean VNM_L (mV) | σ VNM_L (mV) | Mean VNM_H (mV) | σ VNM_H (mV) |
|-------------|------------------------|------------------|----------------------|-------------------|-----------------------|-------------------|-----------------------|
| 2T Inverter | Low area & GB | 44.8 | 9.67 | 26.2 | 8.35 | 32.6 | 7.59 |
| 2T Inverter | Low size ratio | 40.8 | 5.12 | 22.5 | 3.87 | 36.3 | 3.87 |
| 2T Inverter | Low VNM ratio | 47.8 | 7.57 | 30.7 | 6.80 | 32.6 | 6.67 |
| 2T Inverter | Low V_{DD} & low PDP | 47.8 | 7.57 | 30.7 | 6.80 | 32.6 | 6.67 |
| 2T Inverter | Large area GB | 50.5 | 7.52 | 33.1 | 6.62 | 30.2 | 6.78 |
| 4T Inverter | Low area & GB | 47.0 | 7.59 | 31.5 | 6.14 | 28.4 | 6.76 |
| 4T Inverter | Low size ratio | 40.6 | 4.21 | 36.8 | 3.04 | 22.7 | 3.72 |
| 4T Inverter | Low VNM ratio | 49.9 | 5.93 | 31.1 | 5.27 | 32.9 | 5.36 |
| 4T Inverter | Low V_{DD} & low PDP | 43.8 | 5.49 | 36.5 | 4.61 | 27.4 | 5.12 |
| 4T Inverter | Large area & GB | 48.2 | 5.41 | 32.6 | 4.77 | 31.4 | 4.93 |

Table 7.20: Results from the Monte Carlo simulations of the 2T and the 4T Inverters.

Figure 7.18 shows the relative process variations of SP_x for the inverters. Here the standard deviation of SP_x is divided by the mean value ($\frac{\sigma}{Mean}$). The figures show the relative process variation for each of the size sets in table 7.19 for the 2T and 4T inverters.

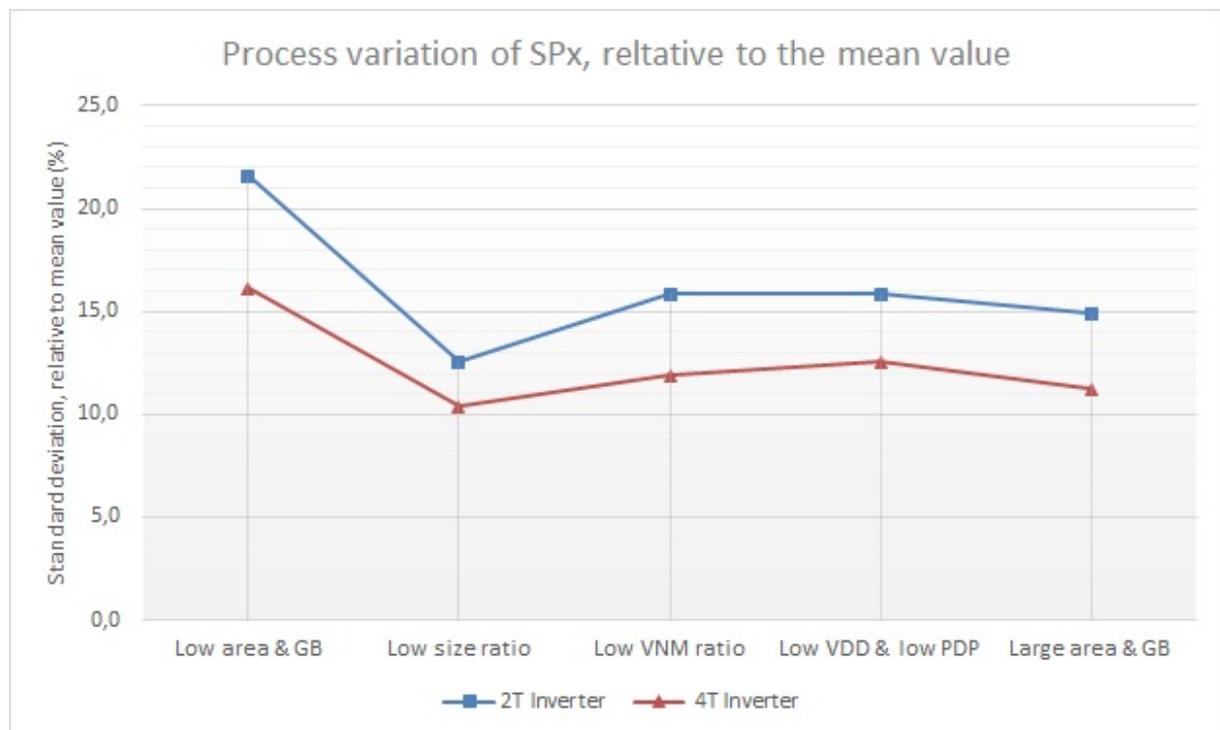


Figure 7.18: The relative process variation of SP_x for the 2T and the 4T inverters.

NAND2

Table 7.21 presents the sets of transistor gate sizes that were used for the Monte Carlo analyses of the 4T and the 8T NAND2 gates.

| Device | Size set name | L (nm) | W nfet (nm) | W pfet (nm) | Area fm ² | Ratio ($\frac{m}{m}$) |
|----------|------------------------|--------|-------------|-------------|----------------------|-------------------------|
| 4T NAND2 | Low area & GB | 30.0 | 200 | 600 | 48.0 | 3.00 |
| 4T NAND2 | Low size ratio | 30.0 | 800 | 1450 | 135 | 1.81 |
| 4T NAND2 | Low VNM ratio | 40.0 | 600 | 1750 | 141 | 2.92 |
| 4T NAND2 | Low V_{DD} & low PDP | 40.0 | 300 | 950 | 100 | 3.17 |
| 4T NAND2 | Large area & GB | 40.0 | 400 | 2500 | 232 | 6.25 |
| | | | | | | |
| 8T NAND2 | Low area & GB | 30.0 | 200 | 1750 | 234 | 8.75 |
| 8T NAND2 | Low size ratio | 30.0 | 300 | 2050 | 282 | 6.83 |
| 8T NAND2 | Low VNM ratio | 30.0 | 200 | 2200 | 288 | 11.0 |
| 8T NAND2 | Low V_{DD} & low PDP | 40.0 | 200 | 1950 | 344 | 9.75 |
| 8T NAND2 | Large area & GB | 30.0 | 250 | 2500 | 330 | 10.0 |

Table 7.21: Names of transistor gate size sets. Devices are 4T and 8T NAND2 gates.

Table 7.22 contains the results of the Monte Carlo analysis of the 4T and 8T NAND2 gates. Here are the mean value and the standard deviation of SP_x , the lower and the higher noise margin (VMN_L and VMN_H). Test was performed with 200 samples, and all samples passed (100% yield).

| Device | Size set name | Mean SP_x (mV) | σ SP_x (mV) | Mean VMN_L (mV) | σ VMN_L (mV) | Mean VMN_H (mV) | σ VMN_H (mV) |
|----------|------------------------|------------------|----------------------|-------------------|-----------------------|-------------------|-----------------------|
| 4T NAND2 | Low area & GB | 48.4 | 10.2 | 24.1 | 7.89 | 29.1 | 7.83 |
| 4T NAND2 | Low size ratio | 40.5 | 5.56 | 18.6 | 4.81 | 35.7 | 3.92 |
| 4T NAND2 | Low VNM ratio | 52.4 | 6.00 | 27.0 | 4.55 | 26.4 | 4.95 |
| 4T NAND2 | Low V_{DD} & low PDP | 31.1 | 6.81 | 13.9 | 6.49 | 44.4 | 4.01 |
| 4T NAND2 | Large area & GB | 45.7 | 5.52 | 25.4 | 4.79 | 33.9 | 4.60 |
| | | | | | | | |
| 8T NAND2 | Low area & GB | 45.7 | 6.43 | 22.8 | 5.34 | 31.8 | 4.95 |
| 8T NAND2 | Low size ratio | 40.1 | 5.35 | 18.6 | 4.69 | 36.1 | 3.76 |
| 8T NAND2 | Low VNM ratio | 51.8 | 5.29 | 27.0 | 4.93 | 26.9 | 5.29 |
| 8T NAND2 | Low V_{DD} & low pdp | 48.6 | 6.41 | 255 | 5.16 | 29.5 | 5.12 |
| 8T NAND2 | Large area & GB | 49.6 | 5.76 | 25.6 | 4.59 | 28.8 | 4.66 |

Table 7.22: Results from the Monte Carlo simulations of the 4T and the 8T NAND2 gates.

Figure 7.19 shows the relative process variations of SP_x for the NAND2 gates. Here the standard deviation of SP_x is divided by the mean value ($\frac{\sigma}{Mean}$). The figures shows the relative process variation for each of the size sets in table 7.21 for the 4T and 8T NAND2 gates.

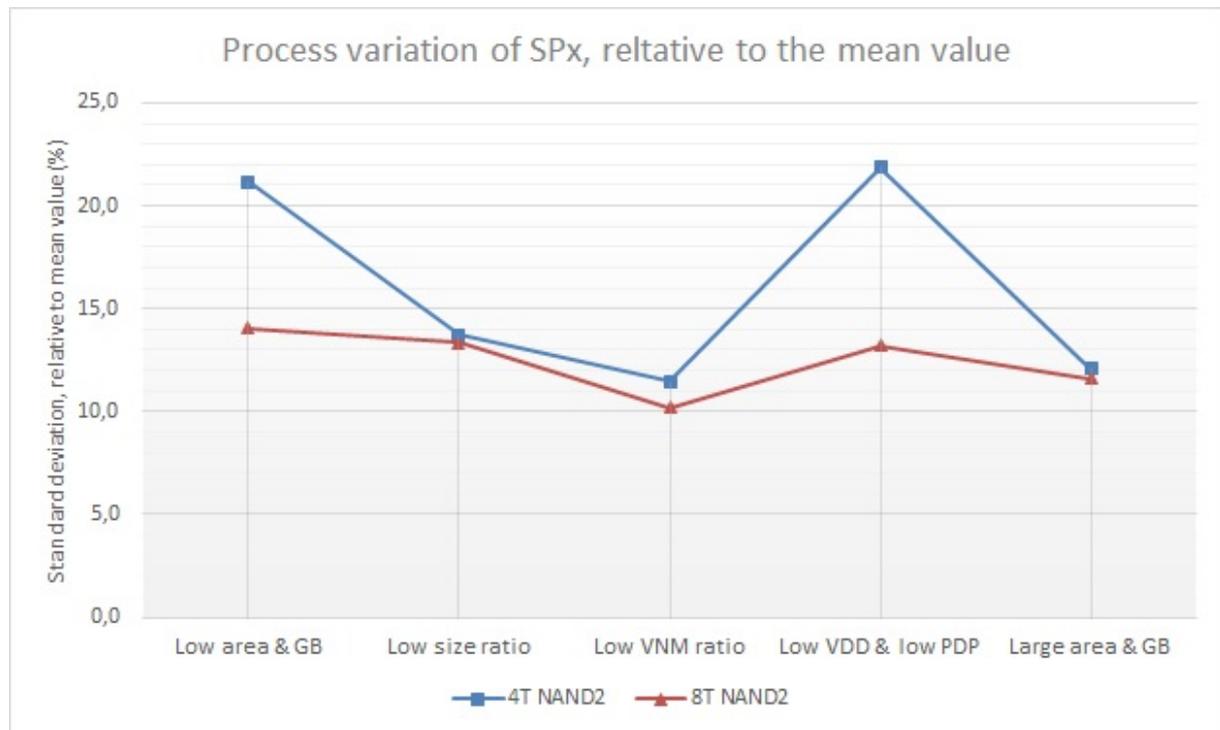


Figure 7.19: The relative process variation of SP_x for the 4T and the 8T NAND2 gates.

NOR2

Table 7.23 presents the sets of transistor gate sizes that were used for the Monte Carlo analyses of the 4T and the 8T NOR2 gates.

| Device | Size set name | L (nm) | W nfet (nm) | W pfet (nm) | Area fm^2 | Ratio ($\frac{m}{m}$) |
|---------|------------------------|--------|-------------|-------------|--------------------|-------------------------|
| 4T NOR2 | Low area & GB | 30.0 | 200 | 1300 | 90.0 | 6.50 |
| 4T NOR2 | Low size ratio | 30.0 | 450 | 2400 | 171 | 5.33 |
| 4T NOR2 | Low VNM ratio | 30.0 | 250 | 1450 | 102 | 5.80 |
| 4T NOR2 | Low V_{DD} & low PDP | 40.0 | 200 | 3750 | 316 | 18.8 |
| 4T NOR2 | Large area & GB | 35.0 | 200 | 2450 | 186 | 12.3 |
| 8T NOR2 | Low area & GB | 30.0 | 200 | 450 | 78 | 2.25 |
| 8T NOR2 | Low size ratio | 30.0 | 800 | 1200 | 240 | 1.50 |
| 8T NOR2 | Low VNM ratio | 40.0 | 400 | 1600 | 320 | 4.00 |
| 8T NOR2 | Low V_{DD} & low PDP | 40.0 | 200 | 1950 | 344 | 9.75 |
| 8T NOR2 | Large area & GB | 40.0 | 600 | 2500 | 496 | 4.17 |

Table 7.23: Names of transistor gate size sets. Devices are 4T and 8T NOR2 gates.

Table 7.24 contains the results of the Monte Carlo analysis of the 4T and 8T NOR2 gates. Here are the mean value and the standard deviation of SP_x , the lower and the higher noise margin (VMN_L and VMN_H). Test was performed with 200 samples, and all samples passed (100% yield).

| Device | Size set name | Mean SP_x (mV) | σ SP_x (mV) | Mean VNM_L (mV) | σ VNM_L (mV) | Mean VNM_H (mV) | σ VNM_H (mV) |
|---------|------------------------|------------------|----------------------|-------------------|-----------------------|-------------------|-----------------------|
| 4T NOR2 | Low area & GB | 47.3 | 9.69 | 28.0 | 7.91 | 24.9 | 7.03 |
| 4T NOR2 | Low size ratio | 44.2 | 6.59 | 25.6 | 5.59 | 27.2 | 4.65 |
| 4T NOR2 | Low VNM ratio | 44.9 | 8.79 | 26.0 | 7.35 | 26.5 | 6.15 |
| 4T NOR2 | Low V_{DD} & low PDP | 51.5 | 7.45 | 33.5 | 6.31 | 25.7 | 6.24 |
| 4T NOR2 | Large area & GB | 50.6 | 8.27 | 31.9 | 6.88 | 25.0 | 6.65 |
| 8T NOR2 | Low area & GB | 48.8 | 7.94 | 29.2 | 6.43 | 24.4 | 6.16 |
| 8T NOR2 | Low size ratio | 45.2 | 4.25 | 26.3 | 3.60 | 27.1 | 3.18 |
| 8T NOR2 | Low VNM ratio | 47.4 | 4.31 | 29.9 | 3.79 | 28.9 | 3.58 |
| 8T NOR2 | Low V_{DD} & low PDP | 66.7 | 5.67 | 45.3 | 3.61 | 13.4 | 5.16 |
| 8T NOR2 | Large area & GB | 48.5 | 3.51 | 30.9 | 3.06 | 28.2 | 2.95 |

Table 7.24: Results from the Monte Carlo simulations of the 4T and the 8T NOR2 gates.

Figure 7.20 shows the relative process variations of SP_x for the NOR2 gates. Here the standard deviation of SP_x is divided by the mean value ($\frac{\sigma}{Mean}$). The figures shows the relative process variation for each of the size sets in table 7.23 for the 4T and 8T NOR2 gates.

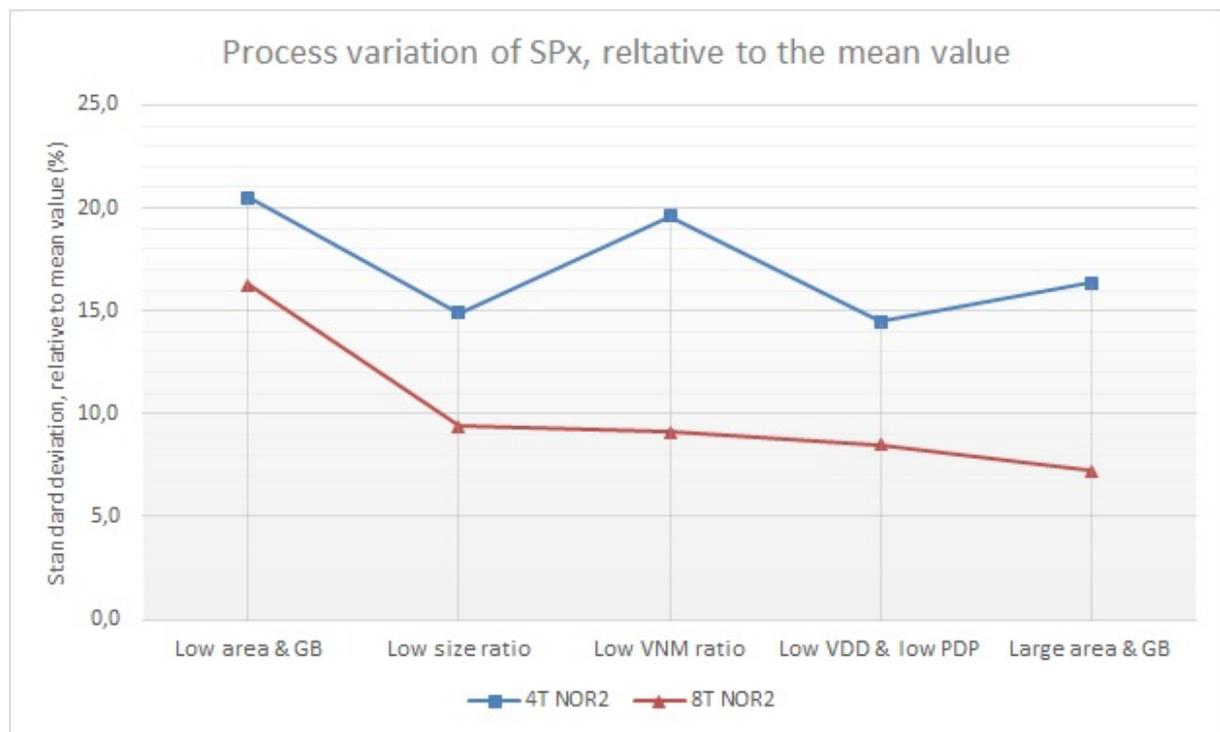


Figure 7.20: The relative process variation of SP_x for the 4T and the 8T NOR2 gates.

7.4 Deciding final sizes

7.4.1 Summary

Here the summary of the results for the DC and transient analyses performed on the different sets of gate sizes for the different logical gates. The results are presented in both tables and figures. The tables with DC results presents area, size ratio, higher and lower noise margins, mean noise margins, ratio between the higher and lower noise margins and the process variation of SP_x relative to the mean value. The tables with the transient results presents the lowest supply voltages that supports stable oscillations, oscillations between 25% and 75% of V_{DD} , and between 5% and 95% of V_{DD} . They also presents power, delay and power delay product obtained at a supply voltage of 100mV in the ring oscillator.

The figures presents the following metrics: Area, size ratio, balance, noise margins, lowest V_{DD} , delay, power and power delay product. The values in the figures are results relative to the set *low area & good balance*. In the figures area represents the total gate area. Size ratio is the ratio between the width of the *pfet* and the *nfet*. Balance represents the absolute value of the difference between SP_x and $\frac{V_{DD}}{2}$. The lower the value of the balance, the closer SP_x is to $\frac{V_{DD}}{2}$. Noise margin in the figure is the mean value of the noise margins. The process variations are the process variations of SP_x relative to the mean value in the Monte Carlo analyses. The lowest V_{DD} represents the lowest supply voltage that gives oscillations between 5% and 95% of V_{DD} . The delay, power and PDP are the delay, power and power delay product obtained at 100mV in the ring oscillator.

Inverter

Table 7.25 presents the results from the DC analyses of the different transistor size sets for the inverters.

| Device | Size set name | SP_x (mV) | VNM_L (mV) | VNM_H (mV) | Mean VNM (mV) | VNM ratio ($\frac{V}{V}$) | Relative σ of SP_x (mV) |
|-------------|------------------------|----------------|-----------------|-----------------|------------------|--------------------------------|-------------------------------------|
| 2T Inverter | Low area & GB | 46.2 | 27.5 | 32.1 | 29.8 | 1.17 | 21.6 |
| 2T Inverter | Low size ratio | 41.5 | 23.3 | 35.9 | 29.6 | 1.54 | 12.6 |
| 2T Inverter | Low VNM ratio | 48.9 | 31.8 | 31.9 | 31.9 | 1.00 | 15.8 |
| 2T Inverter | Low V_{DD} & low PDP | 48.9 | 31.8 | 31.9 | 31.9 | 1.00 | 15.8 |
| 2T Inverter | Large area & GB | 51.5 | 34.2 | 29.5 | 31.9 | 0.863 | 14.9 |
| 4T Inverter | Low area & GB | 45.9 | 27.6 | 32.6 | 30.1 | 1.18 | 16.1 |
| 4T Inverter | Low size ratio | 40.3 | 22.4 | 37.2 | 29.8 | 1.66 | 10.4 |
| 4T Inverter | Low VNM ratio | 48.9 | 32.2 | 32.1 | 32.1 | 1.00 | 11.9 |
| 4T Inverter | Low V_{DD} & low PDP | 42.8 | 26.5 | 37.5 | 32.0 | 1.41 | 12.5 |
| 4T Inverter | Large area & GB | 47.2 | 30.6 | 33.6 | 32.1 | 1.10 | 11.2 |

Table 7.25: Summary of the DC properties of the different transistor gate size sets of the 2T and the 4T inverters.

Table 7.26 presents the results from the transient analyses of the different transistor size sets for the inverters.

| Device | Size set name | V_{DD} at Stable (mV) | V_{DD} at 25% -75% (mV) | V_{DD} at 5% - 95% (mV) | Delay (μs) | Power (pW) | PDP (aJ) |
|-------------|------------------------|-------------------------------|---------------------------------|---------------------------------|----------------------|---------------|-------------|
| 2T Inverter | Low area & GB | 82.0 | 91.0 | 127.0 | 0.935 | 35.96 | 33.6 |
| 2T Inverter | Low size ratio | 83.0 | 96.0 | 135.0 | 0.715 | 131.10 | 93.8 |
| 2T Inverter | Low VNM ratio | 73.0 | 80.0 | 108.0 | 11.2 | 6.23 | 69.5 |
| 2T Inverter | Low V_{DD} & low PDP | 73.0 | 80.0 | 108.0 | 11.2 | 6.23 | 69.5 |
| 2T Inverter | Large area & GB | 73.0 | 80.0 | 110.0 | 11.8 | 6.74 | 79.5 |
| 4T Inverter | Low area & GB | 79.0 | 87.0 | 117 | 3.13 | 17.8 | 55.5 |
| 4T Inverter | Low size ratio | 81.0 | 92.0 | 124 | 2.32 | 62.8 | 146 |
| 4T Inverter | Low VNM ratio | 76.0 | 85.0 | 118 | 14.4 | 8.42 | 121 |
| 4T Inverter | Low V_{DD} & low PDP | 71.0 | 78.0 | 104 | 36.0 | 2.91 | 105 |
| 4T Inverter | Large area & GB | 71.0 | 78.0 | 104 | 35.5 | 3.75 | 133 |

Table 7.26: Summary of the results of the transient analyses of the different transistor gate size sets of the 2T and the 4T inverters.

Figures 7.21 and 7.22 presents the metrics of the different sets of transistor gate sizes for the 2T and 4T inverters respectively. The values in the figures are relative to the *low area & good balance* sets.

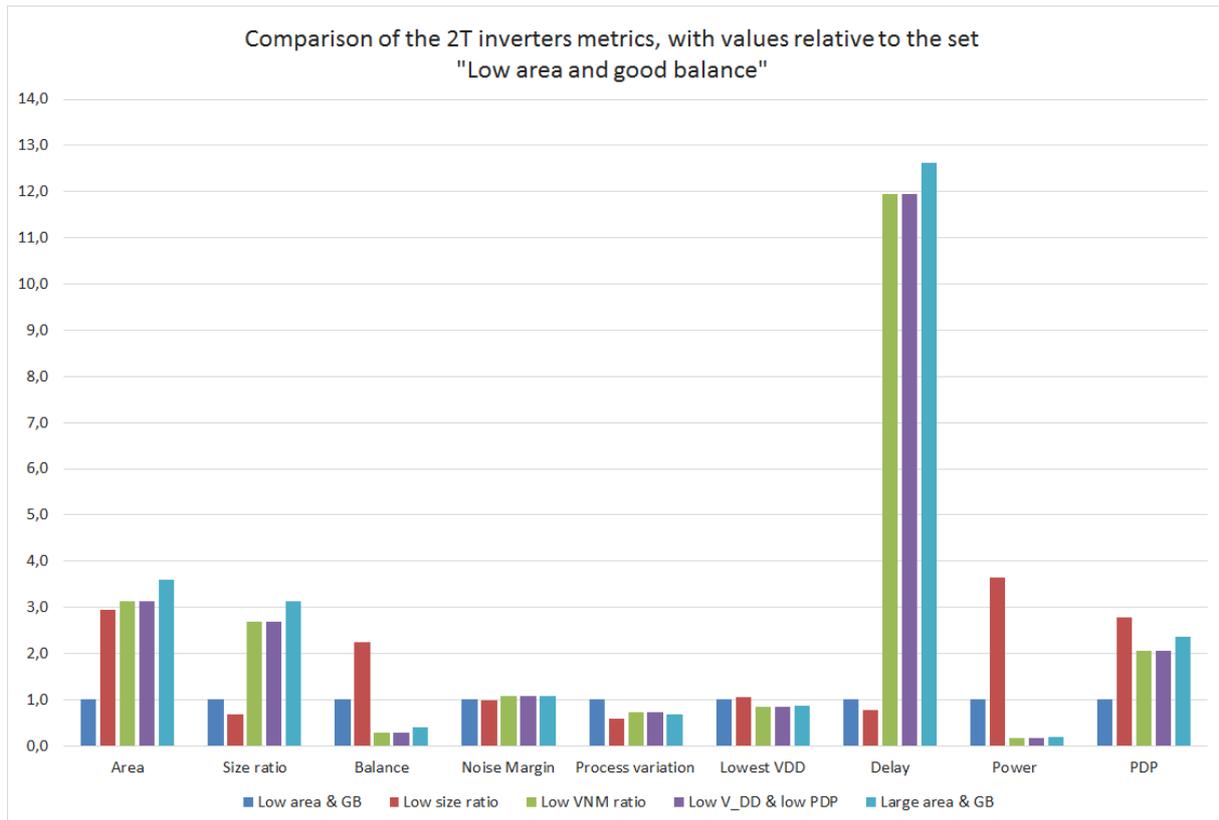


Figure 7.21: Comparison of the relative metrics of the 2T inverter.

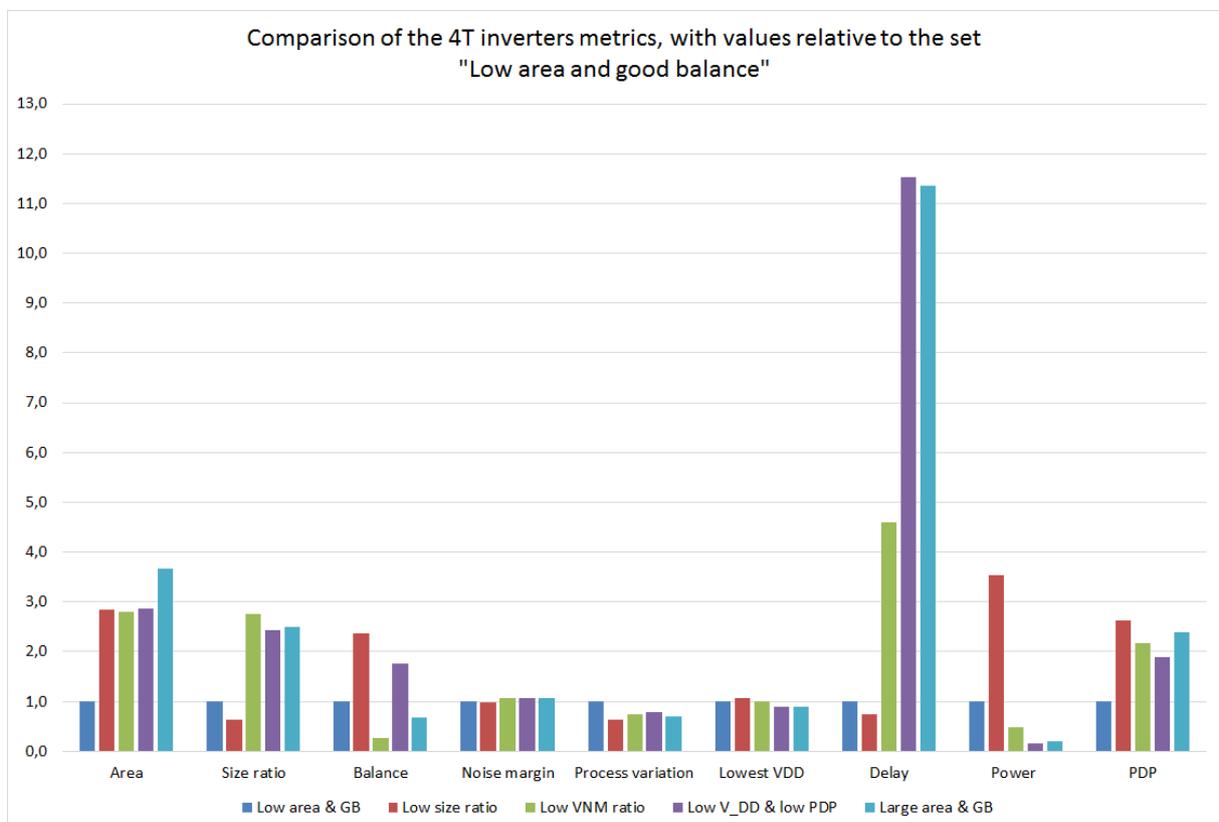


Figure 7.22: Comparison of the relative metrics of the 4T inverter.

NAND2

Table 7.27 presents the results from the DC analyses of the different transistor size sets for the NAND2 gates.

| Device | Size set name | SP_x (mV) | VNM_L (mV) | VNM_H (mV) | Mean VNM (mV) | VNM ratio ($\frac{V}{V}$) | Relative σ of SP_x (mV) |
|----------|------------------------|----------------|-----------------|-----------------|------------------|--------------------------------|-------------------------------------|
| 4T NAND2 | Low area & GB | 47.1 | 23.7 | 30.8 | 27.3 | 1.30 | 21.1 |
| 4T NAND2 | Low size ratio | 40.0 | 18.3 | 36.2 | 27.3 | 1.97 | 13.7 |
| 4T NAND2 | Low VNM ratio | 51.9 | 26.9 | 27.0 | 27.0 | 1.00 | 11.4 |
| 4T NAND2 | Low V_{DD} & low PDP | 30.6 | 12.8 | 45.6 | 29.2 | 3.57 | 21.9 |
| 4T NAND2 | Large area & GB | 45.3 | 25.2 | 34.4 | 29.8 | 1.36 | 12.1 |
| 8T NAND2 | Low area & GB | 45.6 | 23.0 | 32.2 | 27.6 | 1.40 | 14.1 |
| 8T NAND2 | Low size ratio | 40.0 | 18.7 | 36.4 | 27.6 | 1.95 | 13.3 |
| 8T NAND2 | Low VNM ratio | 51.6 | 27.3 | 27.2 | 27.3 | 1.00 | 10.2 |
| 8T NAND2 | Low V_{DD} & low PDP | 27.2 | 10.1 | 47.9 | 29.0 | 4.77 | 13.2 |
| 8T NAND2 | Large area & GB | 49.5 | 25.8 | 29.0 | 27.4 | 1.13 | 11.6 |

Table 7.27: Summary of the DC properties of the different transistor gate size sets of the 4T and the 8T NAND2 gates.

Table 7.28 presents the results from the transient analyses of the different transistor size sets for the NAND2 gates.

| Device | Size set name | V_{DD} at Stable (mV) | V_{DD} at 25% -75% (mV) | V_{DD} at 5% - 95% (mV) | Delay (μ s) | Power (pW) | PDP (aJ) |
|----------|------------------------|-------------------------------|---------------------------------|---------------------------------|---------------------|---------------|-------------|
| 4T NAND2 | Low area & GB | 85.0 | 87.0 | 139 | 1.82 | 27.7 | 50.3 |
| 4T NAND2 | Low size ratio | 82.0 | 86.0 | 130 | 1.29 | 104 | 135 |
| 4T NAND2 | Low VNM ratio | 88.0 | 107.0 | 146 | 1.48 | 96.9 | 143 |
| 4T NAND2 | Low V_{DD} & low PDP | 74.0 | 79.0 | 106 | 14.8 | 4.91 | 72.8 |
| 4T NAND2 | Large area & GB | 76.0 | 89.0 | 124 | 10.4 | 22.1 | 230 |
| 8T NAND2 | Low area & GB | 84.0 | 97.0 | 134 | 3.78 | 55.7 | 210 |
| 8T NAND2 | Low size ratio | 82.0 | 92.0 | 128 | 3.28 | 76.4 | 251 |
| 8T NAND2 | Low VNM ratio | 88.0 | 105 | 134 | 4.15 | 62.0 | 257 |
| 8T NAND2 | Low V_{DD} & low PDP | 72.0 | 78.0 | 104 | 5.83 | 36.0 | 210 |
| 8T NAND2 | Large area & GB | 88.0 | 102 | 140 | 3.90 | 75.4 | 294 |

Table 7.28: Summary of the results of the transient analyses of the different transistor gate size sets of the 4T and the 8T NAND2 gates.

Figures 7.23 and 7.24 presents the metrics of the different sets of transistor gate sizes for the 4T and 8T NAND2 gates respectively. The values in the figures are relative to the *low area & good balance* sets.

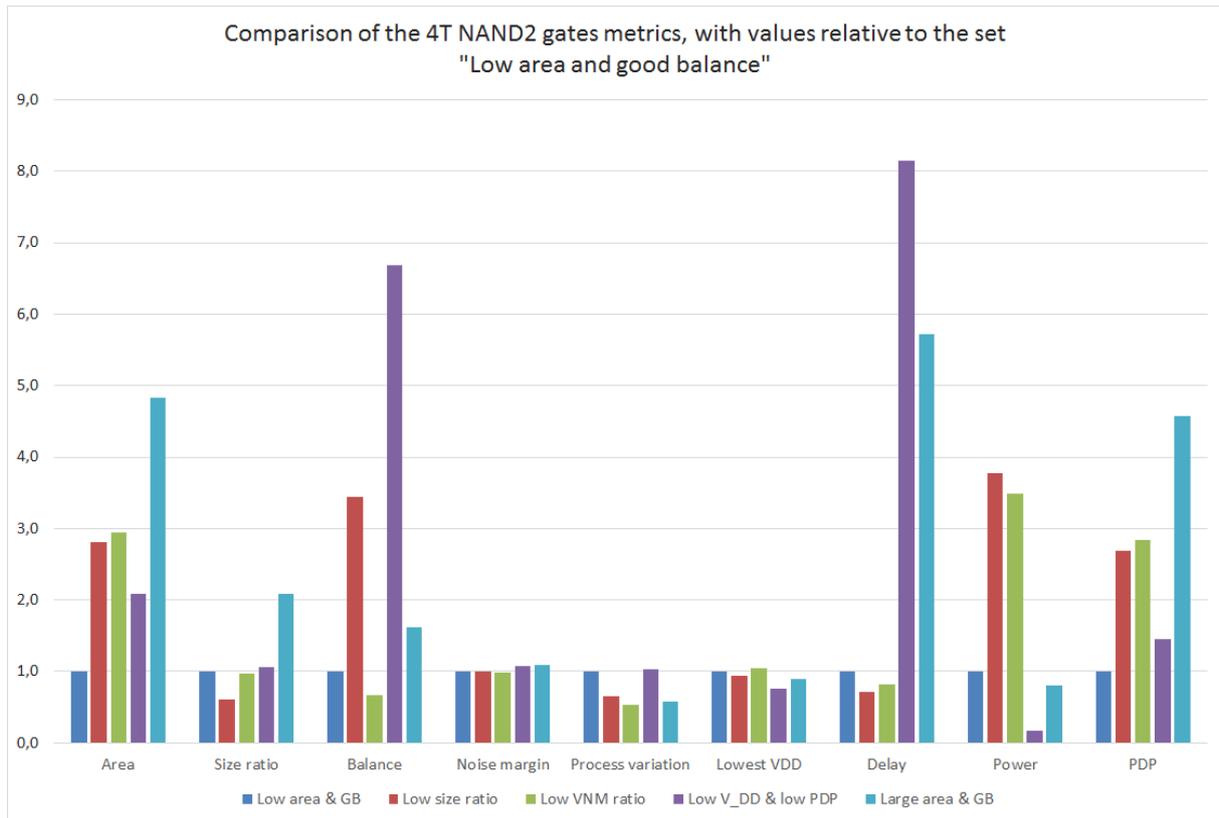


Figure 7.23: Comparison of the relative metrics of the 4T NAND2 gate.

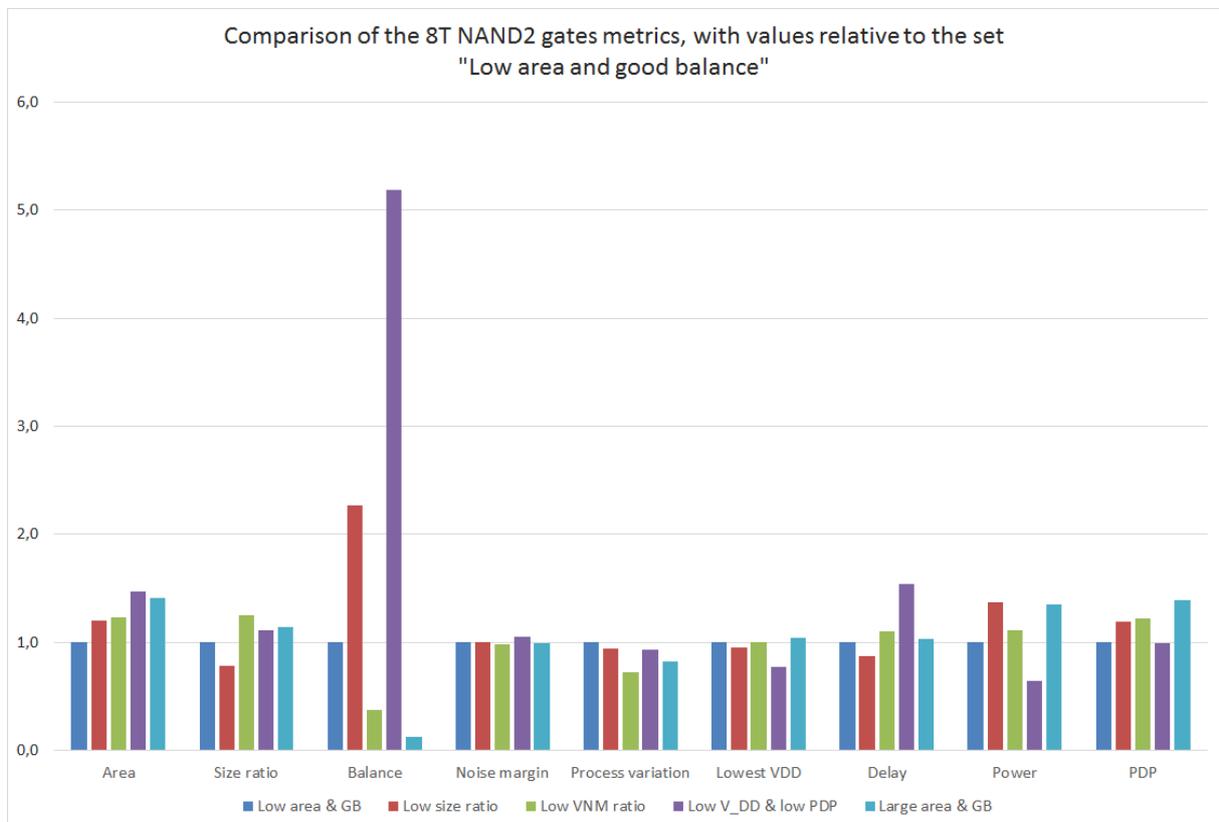


Figure 7.24: Comparison of the relative metrics of the 8T NAND2 gate.

NOR2

Table 7.29 presents the results from the DC analyses of the different transistor size sets for the NOR2 gates.

| Device | Size set name | SP_x (mV) | VNM_L (mV) | VNM_H (mV) | Mean VNM (mV) | VNM ratio ($\frac{V}{V}$) | Relative σ of SP_x (mV) |
|---------|------------------------|----------------|-----------------|-----------------|------------------|--------------------------------|-------------------------------------|
| 4T NOR2 | Low area & GB | 48.1 | 25.3 | 29.0 | 27.2 | 1.15 | 20.5 |
| 4T NOR2 | Low size ratio | 44.6 | 27.5 | 26.1 | 26.8 | 0.948 | 14.9 |
| 4T NOR2 | Low VNM ratio | 45.6 | 26.9 | 26.9 | 26.9 | 1.00 | 19.6 |
| 4T NOR2 | Low V_{DD} & low PDP | 52.0 | 25.8 | 34.1 | 30.0 | 1.32 | 14.5 |
| 4T NOR2 | Large area & GB | 51.2 | 25.2 | 32.7 | 28.9 | 1.30 | 16.3 |
| 8T NOR2 | Low area & GB | 47.6 | 28.5 | 25.8 | 27.1 | 0.904 | 16.3 |
| 8T NOR2 | Low size ratio | 44.8 | 26.1 | 27.5 | 26.8 | 1.05 | 9.40 |
| 8T NOR2 | Low VNM ratio | 46.9 | 29.5 | 29.5 | 29.5 | 1.00 | 9.10 |
| 8T NOR2 | Low V_{DD} & low PDP | 65.7 | 45.0 | 14.3 | 29.6 | 0.318 | 8.50 |
| 8T NOR2 | Large area & GB | 48.1 | 30.6 | 28.6 | 29.6 | 0.932 | 7.23 |

Table 7.29: Summary of the DC properties of the different transistor gate size sets of the 4T and the 8T NOR2 gates.

Table 7.30 presents the results from the transient analyses of the different transistor size sets for the NOR2 gates.

| Device | Size set name | V_{DD} at Stable (mV) | V_{DD} at 25% -75% (mV) | V_{DD} at 5% - 95% (mV) | Delay (μs) | Power (pW) | PDP (aJ) |
|---------|------------------------|-------------------------------|---------------------------------|---------------------------------|----------------------|---------------|-------------|
| 4T NOR2 | Low area & GB | 88.0 | 105 | 142 | 1.81 | 45.7 | 82.6 |
| 4T NOR2 | Low size ratio | 90.0 | 109 | 147 | 1.58 | 97.1 | 153 |
| 4T NOR2 | Low VNM ratio | 89.0 | 109 | 146 | 1.72 | 54.1 | 93.0 |
| 4T NOR2 | Low V_{DD} & low PDP | 77.0 | 91.0 | 121 | 23.9 | 7.92 | 189 |
| 4T NOR2 | Large area & GB | 81.0 | 95.0 | 128 | 7.71 | 17.3 | 133 |
| 8T NOR2 | Low area & GB | 87.0 | 104 | 137 | 3.34 | 22.5 | 75.1 |
| 8T NOR2 | Low size ratio | 89.0 | 107 | 142 | 2.42 | 87.6 | 212 |
| 8T NOR2 | Low VNM ratio | 80.0 | 96.0 | 125 | 27.5 | 7.07 | 194 |
| 8T NOR2 | Low V_{DD} & low PDP | 71.0 | 79.0 | 104 | 36.0 | 5.83 | 210 |
| 8T NOR2 | Large area & GB | 79.0 | 94.0 | 123 | 26.6 | 11.2 | 297 |

Table 7.30: Summary of the results of the transient analyses of the different transistor gate size sets of the 4T and the 8T NOR2 gates.

Figures 7.25 and 7.26 presents the metrics of the different sets of transistor gate sizes for the 4T and 8T NOR2 gates respectively. The values in the figures are relative to the *low area & good balance* sets.

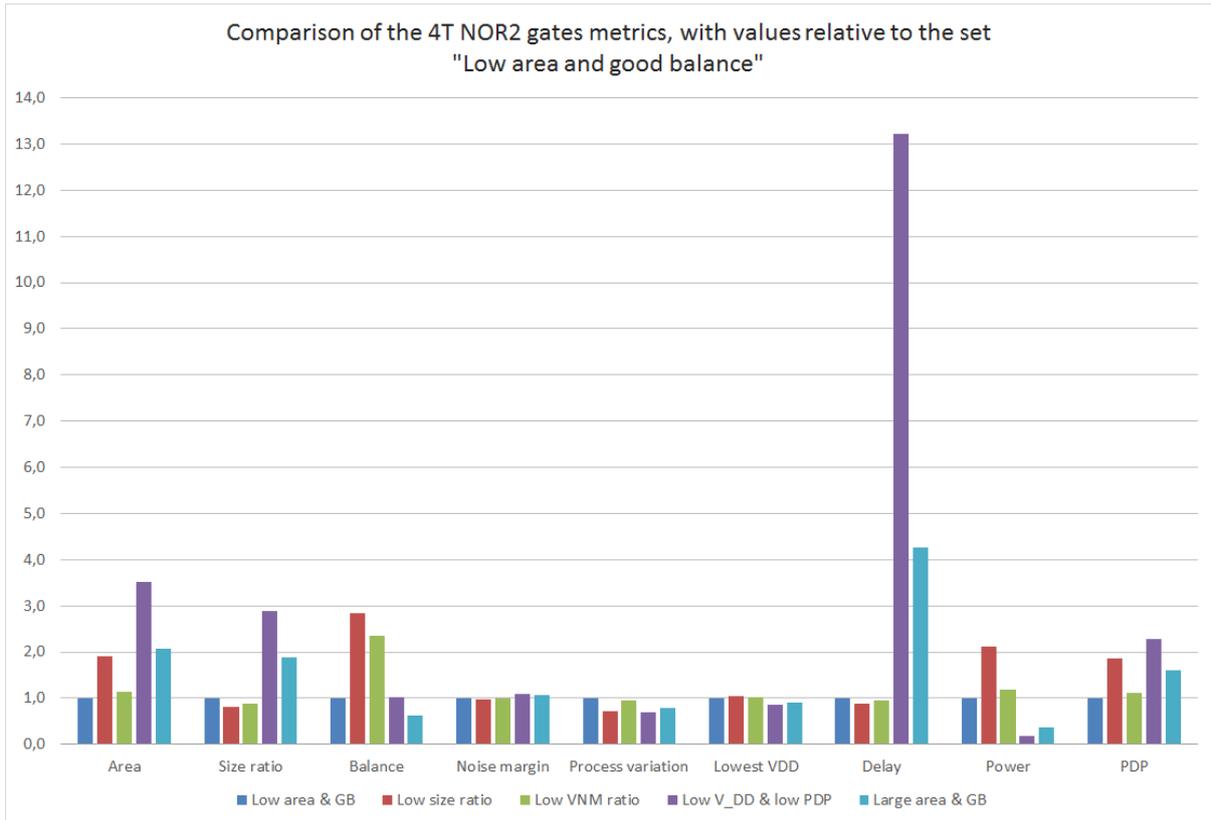


Figure 7.25: Comparison of the relative metrics of the 4T NOR2 gate

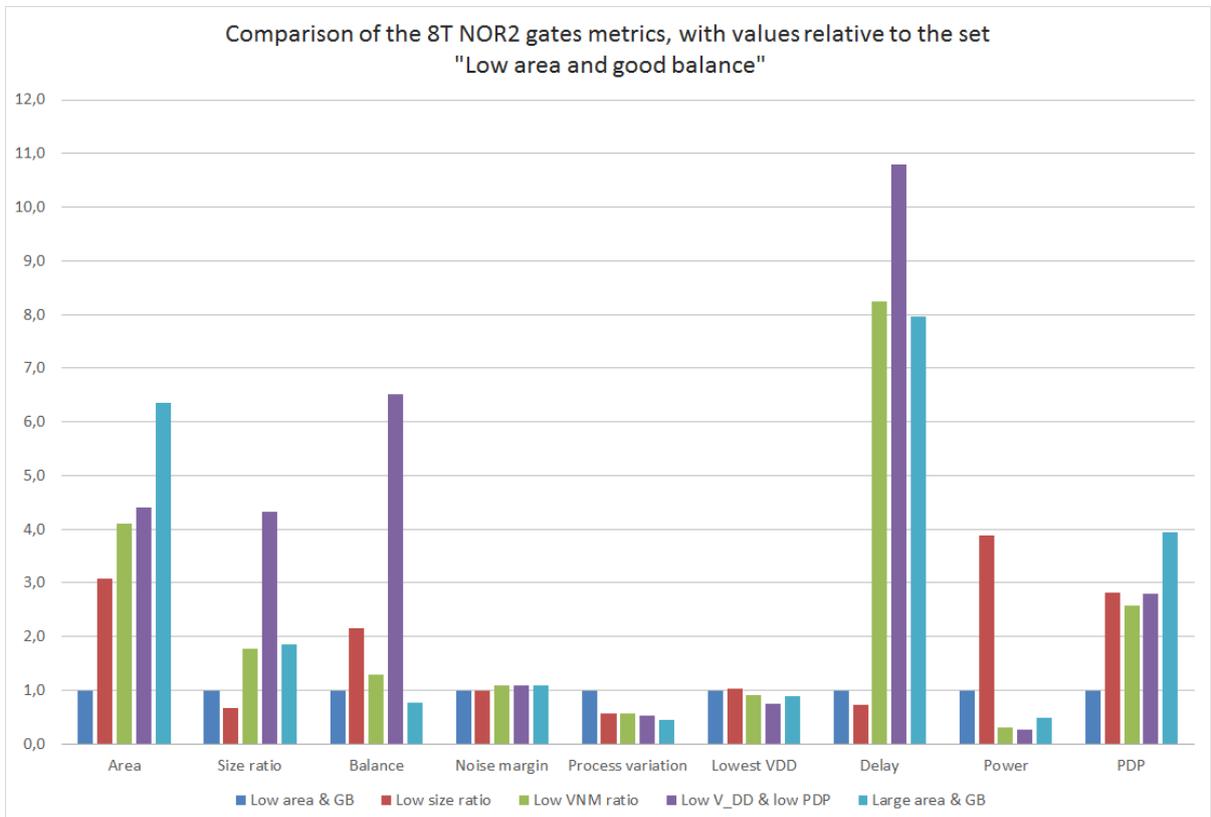


Figure 7.26: Comparison of the relative metrics of the 8T NOR2 gate

7.4.2 Final sizes

Table 7.31 presents the transistor gate size sets that were decided to be the final sizes for the different logical gates.

| Device | Size set name | L (nm) | W nfet (nm) | W pfet (nm) | Area fm ² | Ratio ($\frac{m}{m}$) |
|-------------|---------------|--------|-------------|-------------|----------------------|-------------------------|
| 2T Inverter | Low VNM ratio | 40.0 | 200 | 2150 | 94.0 | 10.8 |
| 4T Inverter | Low VNM ratio | 35.0 | 200 | 2200 | 168 | 11.0 |
| 4T NAND2 | Low VNM ratio | 30.0 | 600 | 1750 | 141 | 2.92 |
| 8T NAND2 | Low VNM ratio | 30.0 | 200 | 2200 | 288 | 11.0 |
| 4T NOR2 | Low VNM ratio | 30.0 | 250 | 1450 | 102 | 5.80 |
| 8T NOR2 | Low VNM ratio | 40.0 | 400 | 1600 | 320 | 4.00 |

Table 7.31: The final sets of transistor gate sizes.

Table 7.32 presents the results from the DC analyses of the final sizes of the different logical gates.

| Device | SP _x (mV) | VNM _L (mV) | VNM _H (mV) | Mean VNM (mV) | VNM ratio ($\frac{V}{V}$) | Relative σ of SP _x (mV) |
|-------------|----------------------|-----------------------|-----------------------|---------------|-----------------------------|---|
| 2T Inverter | 48.9 | 31.8 | 31.9 | 31.9 | 1.00 | 15.8 |
| 4T Inverter | 48.9 | 32.2 | 32.1 | 32.1 | 1.00 | 11.9 |
| 4T NAND2 | 51.9 | 26.9 | 27.0 | 27.0 | 1.00 | 11.4 |
| 8T NAND2 | 51.6 | 27.3 | 27.2 | 27.3 | 1.00 | 10.2 |
| 4T NOR2 | 45.6 | 26.9 | 26.9 | 26.9 | 1.00 | 19.6 |
| 8T NOR2 | 46.9 | 29.5 | 29.5 | 29.5 | 1.00 | 9.10 |

Table 7.32: The results of the DC analyses of the final sets of transistor gate sizes.

Table 7.33 presents the results from the transient analyses of the final sizes of the different logical gates.

| Device | V _{DD} at Stable (mV) | V _{DD} at 25% -75% (mV) | V _{DD} at 5% - 95% (mV) | Delay (μ s) | Power (pW) | PDP (aJ) |
|-------------|--------------------------------|----------------------------------|----------------------------------|------------------|------------|----------|
| 2T Inverter | 73.0 | 80.0 | 108.0 | 11.2 | 6.23 | 69.5 |
| 4T Inverter | 76.0 | 85.0 | 118 | 14.4 | 8.42 | 121 |
| 4T NAND2 | 88.0 | 107.0 | 146 | 1.48 | 96.9 | 143 |
| 8T NAND2 | 88.0 | 105 | 134 | 4.15 | 62.0 | 257 |
| 4T NOR2 | 89.0 | 109 | 146 | 1.72 | 54.1 | 93.0 |
| 8T NOR2 | 80.0 | 96.0 | 125 | 27.5 | 7.07 | 194 |

Table 7.33: The results of the transient analyses of the final sets of transistor gate sizes.

Figure 7.27 presents the metrics of the final sizes of the logical gates. The values are relative to the 2T inverter.

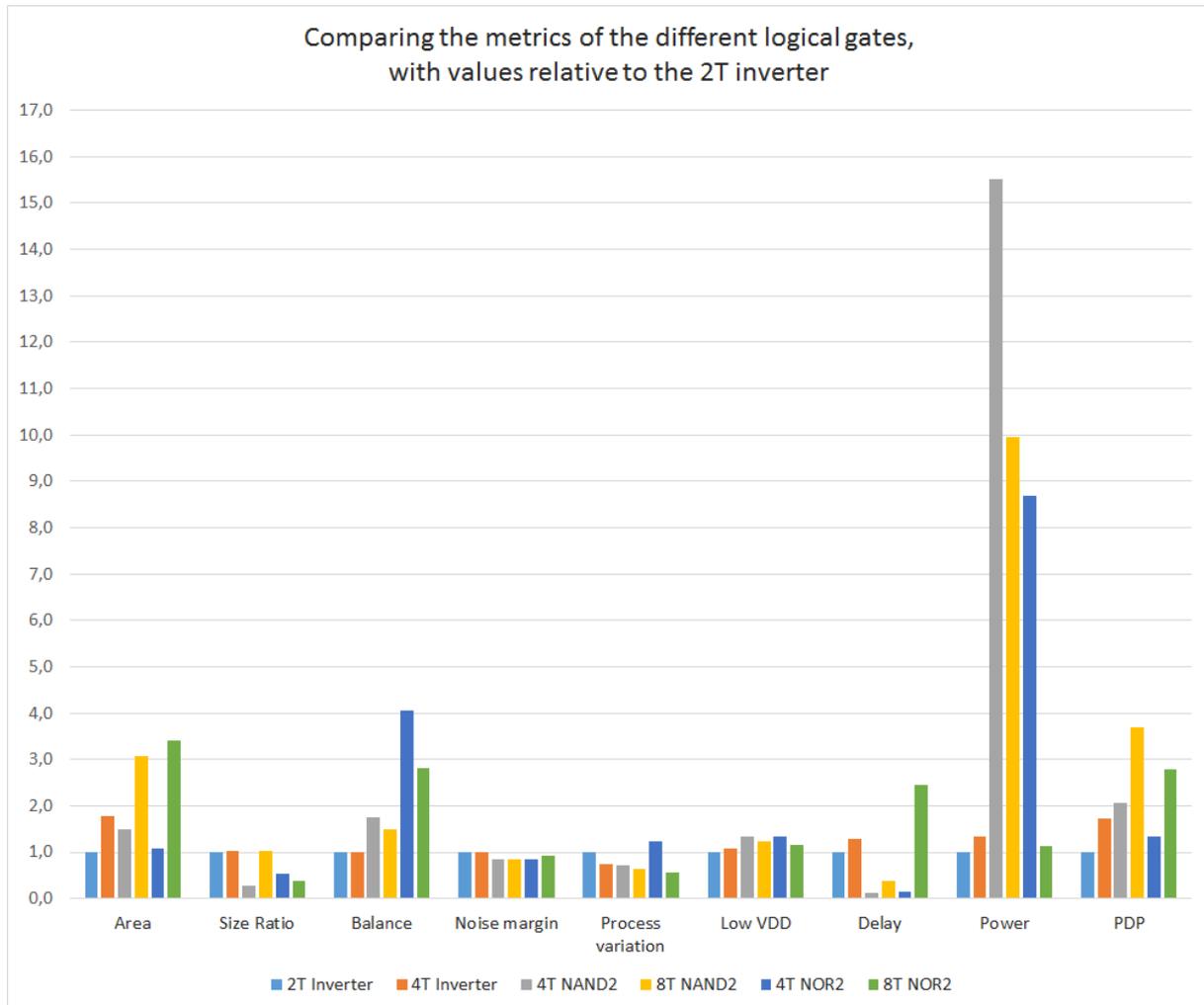


Figure 7.27: Comparison of the final transistor gate size sets of the different logical gates. Values are relative to the 2T inverter.

7.5 Effects of body biasing

Figures 7.28 and 7.29 presents how body biasing the *nfet* and the *pfet* respectively affects the transfer characteristics of the output of the 8T NAND2 gate.

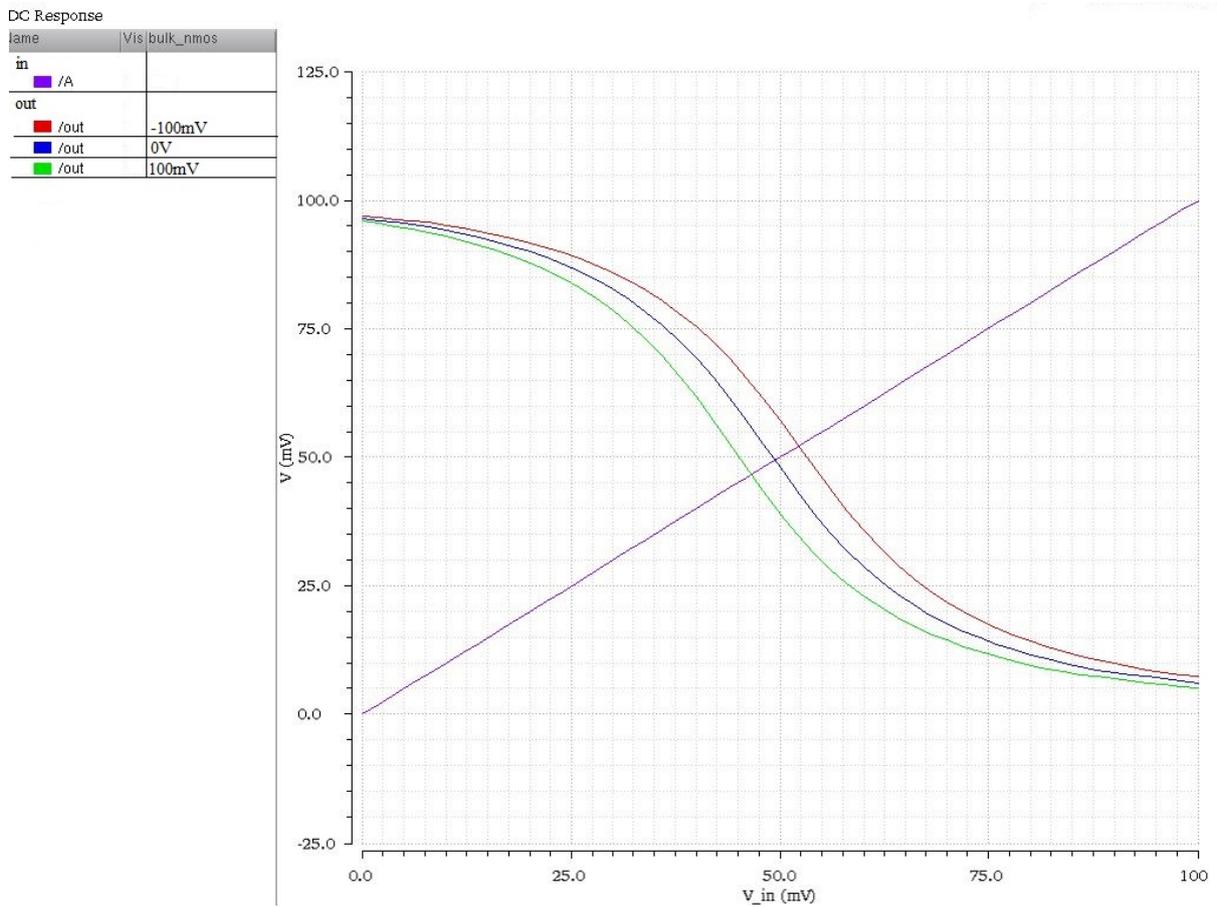


Figure 7.28: Body biasing the *nfet* in a 8T NAND2 gate. $L = 30\text{nm}$, $W_{nfet} = 200\text{nm}$, $W_{pfet} = 2000\text{nm}$

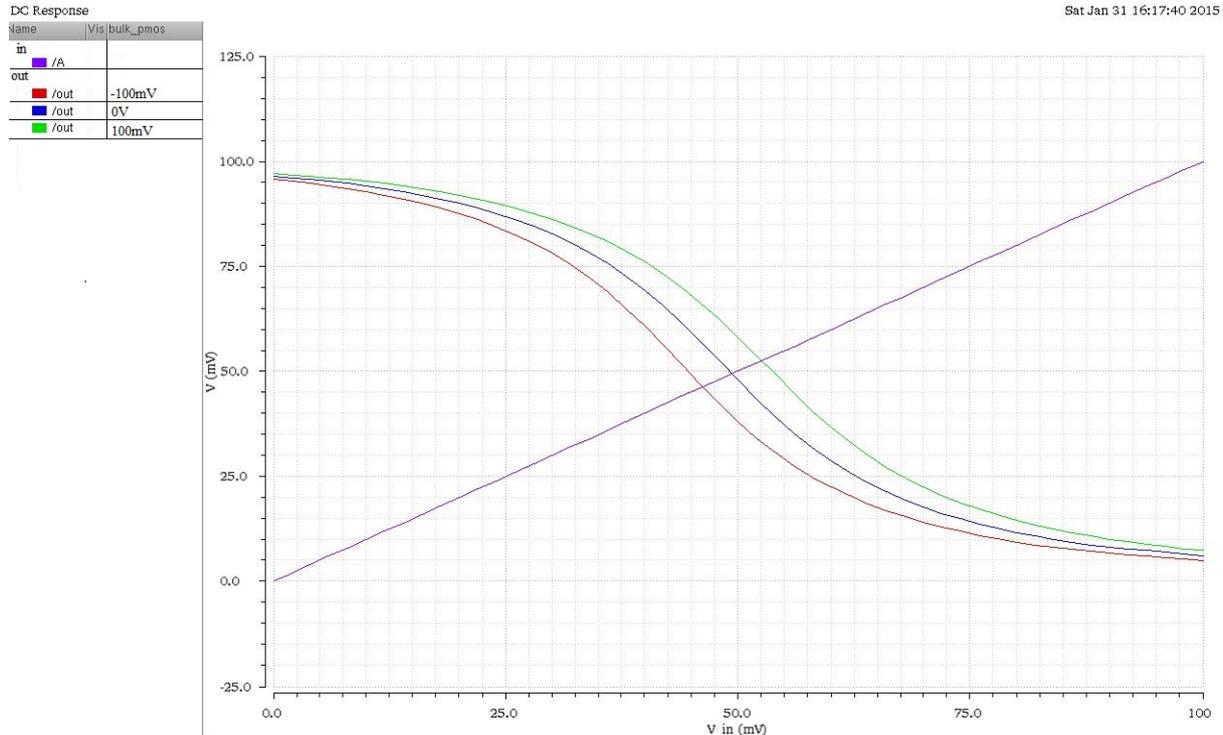


Figure 7.29: Body biasing the *pfet* in a 8T NAND2 gate. $L = 30\text{nm}$, $W_{\text{nfet}} = 200\text{nm}$, $W_{\text{pfet}} = 2000\text{nm}$

Figure 7.30 presents how body biasing both the *nfet* and the *pfet* affects the transfer characteristics of the output of the 8T NAND2 gate.

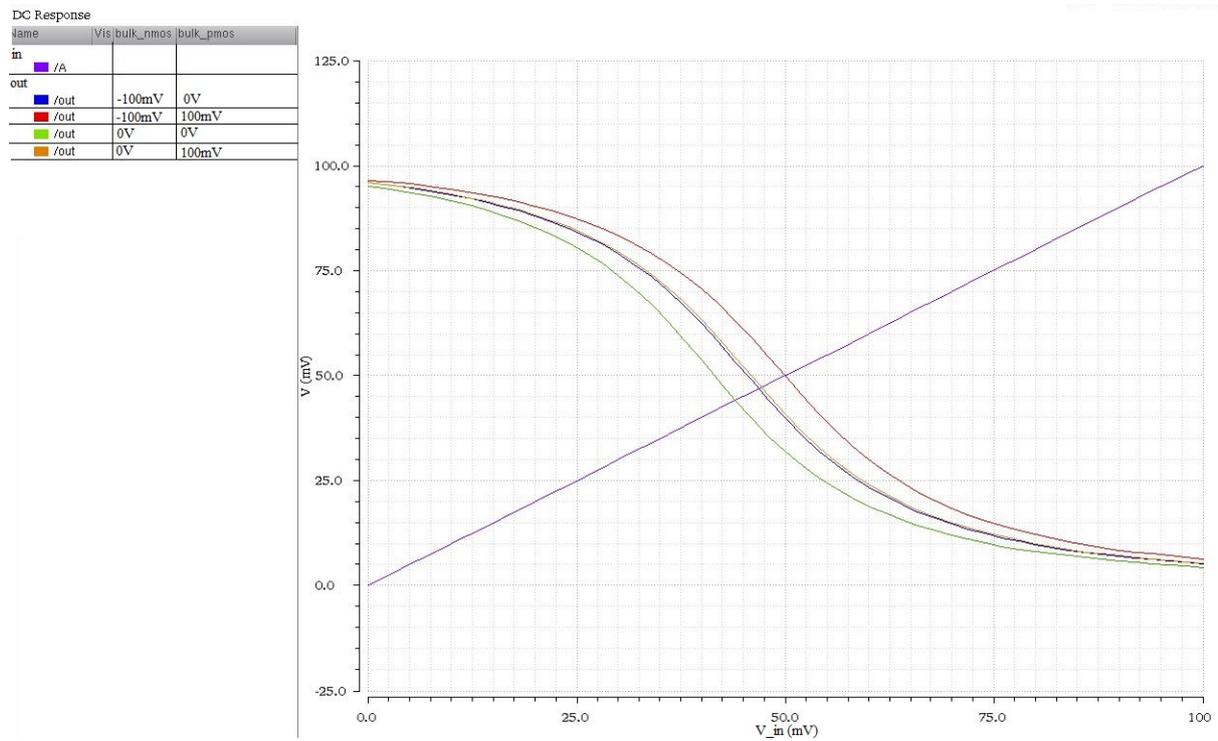


Figure 7.30: Body biasing both the *nfet* and the *pfet* in a 8T NAND2 gate. $L = 30\text{nm}$, $W_{\text{nfet}} = 200\text{nm}$, $W_{\text{pfet}} = 1500\text{nm}$

The table 7.34 presents the different sets of transistor gate sizes for the body biased 8T NAND2 gate that gives the lowest area, lowest size ratio, lowest VNM ratio and largest gate area.

| Size set name | L (nm) | WN (nm) | WP (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) | VNM _L (mV) | VNM _H (mV) | Mean VNM (mV) | VNM ratio ($\frac{V}{V}$) |
|-----------------|--------|---------|---------|-------------------------|------------------------------|----------------------|-----------------------|-----------------------|---------------|-----------------------------|
| Low area | 30.0 | 200 | 1050 | 150 | 5.25 | 40.1 | 18.8 | 36.4 | 27.6 | 1.94 |
| Low area & GB | 30.0 | 200 | 1300 | 180 | 6.50 | 46.0 | 23.3 | 31.9 | 27.6 | 1.37 |
| Low size ratio | 30.0 | 450 | 2150 | 312 | 4.78 | 40.1 | 18.8 | 36.4 | 27.6 | 1.94 |
| Low VNM ratio | 30.0 | 250 | 1950 | 264 | 7.80 | 51.6 | 27.2 | 27.3 | 27.3 | 1.00 |
| Large area | 40.0 | 200 | 2500 | 432 | 12.50 | 40.0 | 21.3 | 39.0 | 30.1 | 1.83 |
| Large area & GB | 35.0 | 200 | 2500 | 378 | 12.50 | 48.6 | 27.0 | 31.0 | 29.0 | 1.15 |

Table 7.34: The different sets of transistor gate sizes for the 8T NAND2 gate using body biasing.

Figures 7.31, 7.32 and 7.33 shows how the power, delay and power delay products for the different NAND2 gates varies with increasing supply voltages.

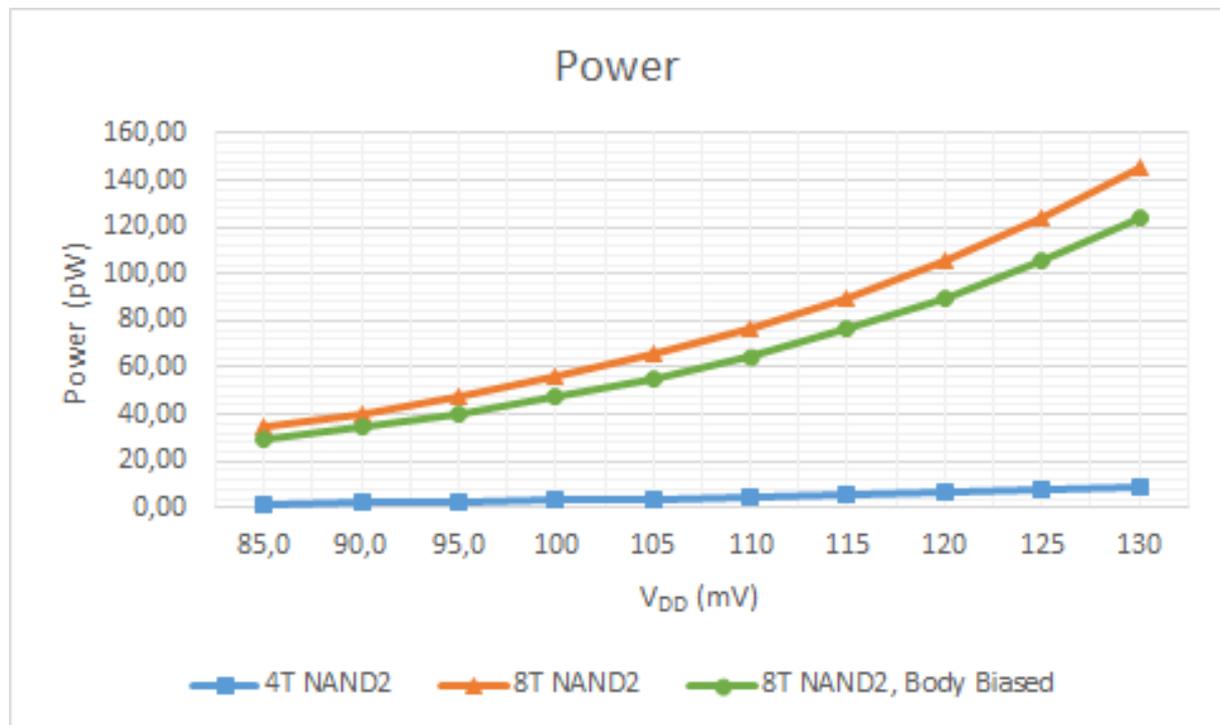


Figure 7.31: The power consumption in the ring oscillators constructed of the NAND2 gates. V_{DD} was increased from 85mV to 130mV.

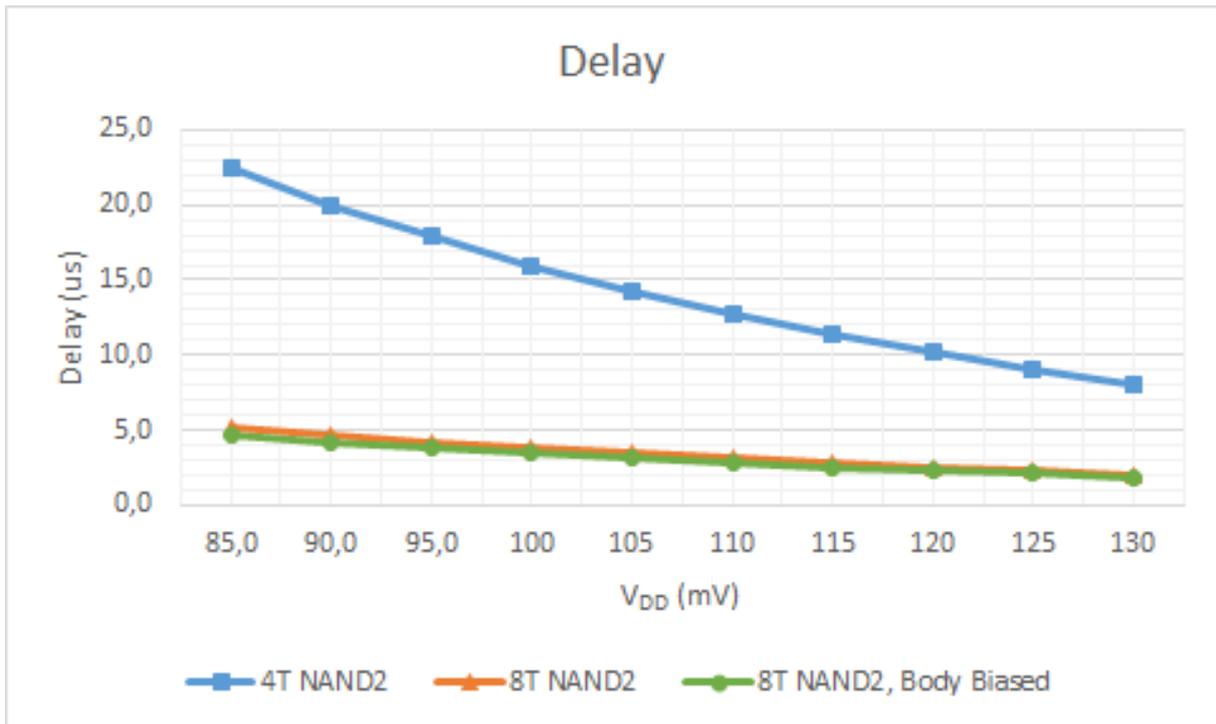


Figure 7.32: The delay in the ring oscillators constructed of the NAND2 gates. V_{DD} was increased from 85mV to 130mV.

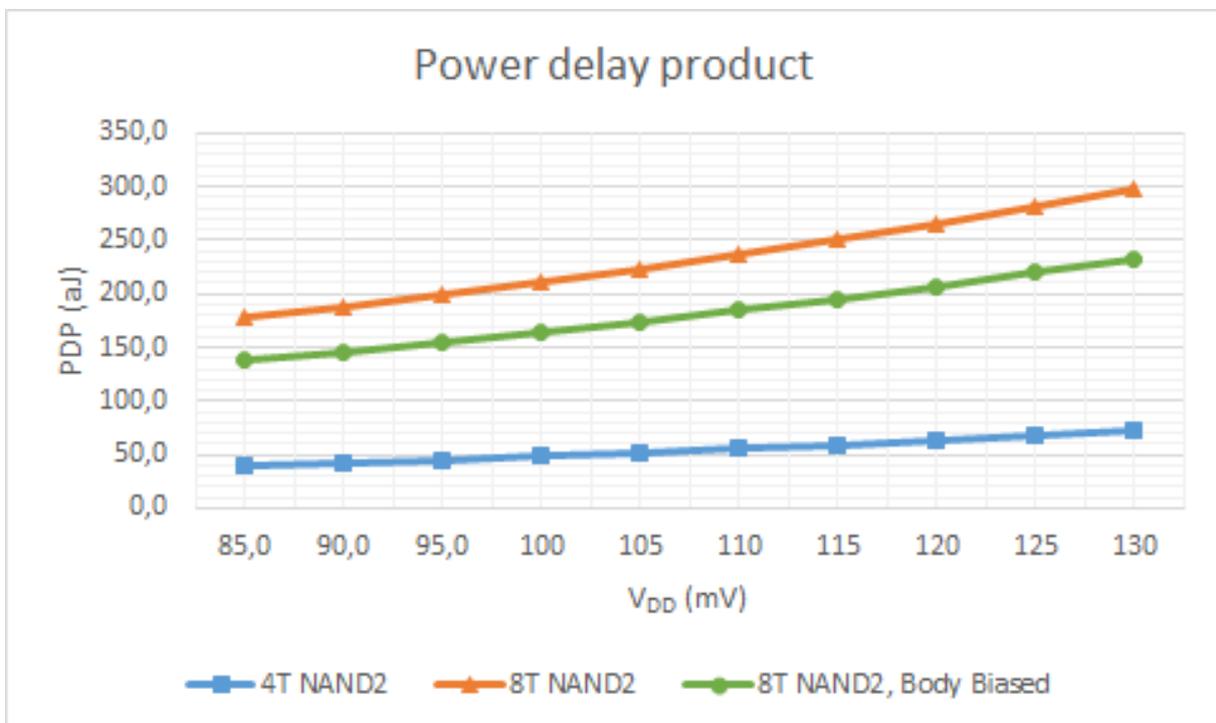


Figure 7.33: The power delay product in the ring oscillators constructed of the NAND2 gates. V_{DD} was increased from 85mV to 130mV.

Table 7.35 shows the transistor gate sizes for the set *low VNM ratio* for the different NAND2 gates.

| Device | Size set name | L (nm) | W nfet (nm) | W pfet (nm) | Area fm^2 | Size ratio ($\frac{m}{m}$) |
|-----------------------|---------------|--------|-------------|-------------|--------------------|------------------------------|
| 4T NAND2 | Low VNM ratio | 30.0 | 600 | 1750 | 141 | 2.92 |
| 8T NAND2 | Low VNM ratio | 30.0 | 200 | 2200 | 288 | 11.0 |
| 8T NAND2. Body Biased | Low VNM ratio | 30.0 | 250 | 1950 | 264 | 7.80 |

Table 7.35: Transistor gate dimensions for the different NAND2 gates.

Table 7.36 shows the process variations for the set *low VNM ratio* for the different NAND2 gates.

| Device | Mean SP_x (mV) | σ SP_x (mV) | Mean VNM_L (mV) | σ VNM_L (mV) | Mean VNM_H (mV) | σ VNM_H (mV) |
|-------------|-------------------------|-----------------------------|--------------------------|------------------------------|--------------------------|------------------------------|
| 4T NAND2 | 51.5 | 6.29 | 29.6 | 5.12 | 28.9 | 5.50 |
| 8T NAND2 | 51.8 | 5.29 | 27.0 | 4.93 | 26.9 | 5.29 |
| 8T NAND2 BB | 51.7 | 5.86 | 27.0 | 4.55 | 27.0 | 4.84 |

Table 7.36: Results from the Monte Carlo simulations of the different NAND2 gates.

Table 7.37 shows the results of the DC analyses for the set *low VNM ratio* for the different NAND2 gates.

| Device | SP_x (mV) | VNM_L (mV) | VNM_H (mV) | Mean VNM (mV) | VNM ratio ($\frac{V}{V}$) | Relative σ of SP_x (mV) |
|-------------|--------------------|---------------------|---------------------|---------------|-----------------------------|---|
| 4T NAND2 | 51.9 | 26.9 | 27.0 | 27.0 | 1.00 | 11.4 |
| 8T NAND2 | 51.6 | 27.3 | 27.2 | 27.3 | 1.00 | 10.2 |
| 8T NAND2 BB | 51.6 | 27.2 | 27.3 | 27.3 | 1.00 | 11.3 |

Table 7.37: Summary of the DC properties of the different NAND2 gates.

Table 7.38 shows the results of the transient analyses for the set *low VNM ratio* for the different NAND2 gates.

| Device | V_{DD} at Stable (mV) | V_{DD} at 25% -75% (mV) | V_{DD} at 5% - 95% (mV) | Delay (μs) | Power (pW) | PDP (aJ) |
|-------------|-------------------------|---------------------------|---------------------------|-------------------------|------------|----------|
| 4T NAND2 | 79.0 | 97.0 | 134 | 20.4 | 7.69 | 157 |
| 8T NAND2 | 88.0 | 105 | 134 | 4.15 | 62.0 | 257 |
| 8T NAND2 BB | 87 | 104 | 143 | 3.60 | 65.7 | 237 |

Table 7.38: Summary of the results of the transient analyses of the different NAND2 gates.

Figure 7.34 shows the different metrics for the set *low VNM ratio* for the different NAND2 gates. The metrics in this figure are the same as in chapter 7.4.1, and the values are relative to the 4T NAND2 gate.

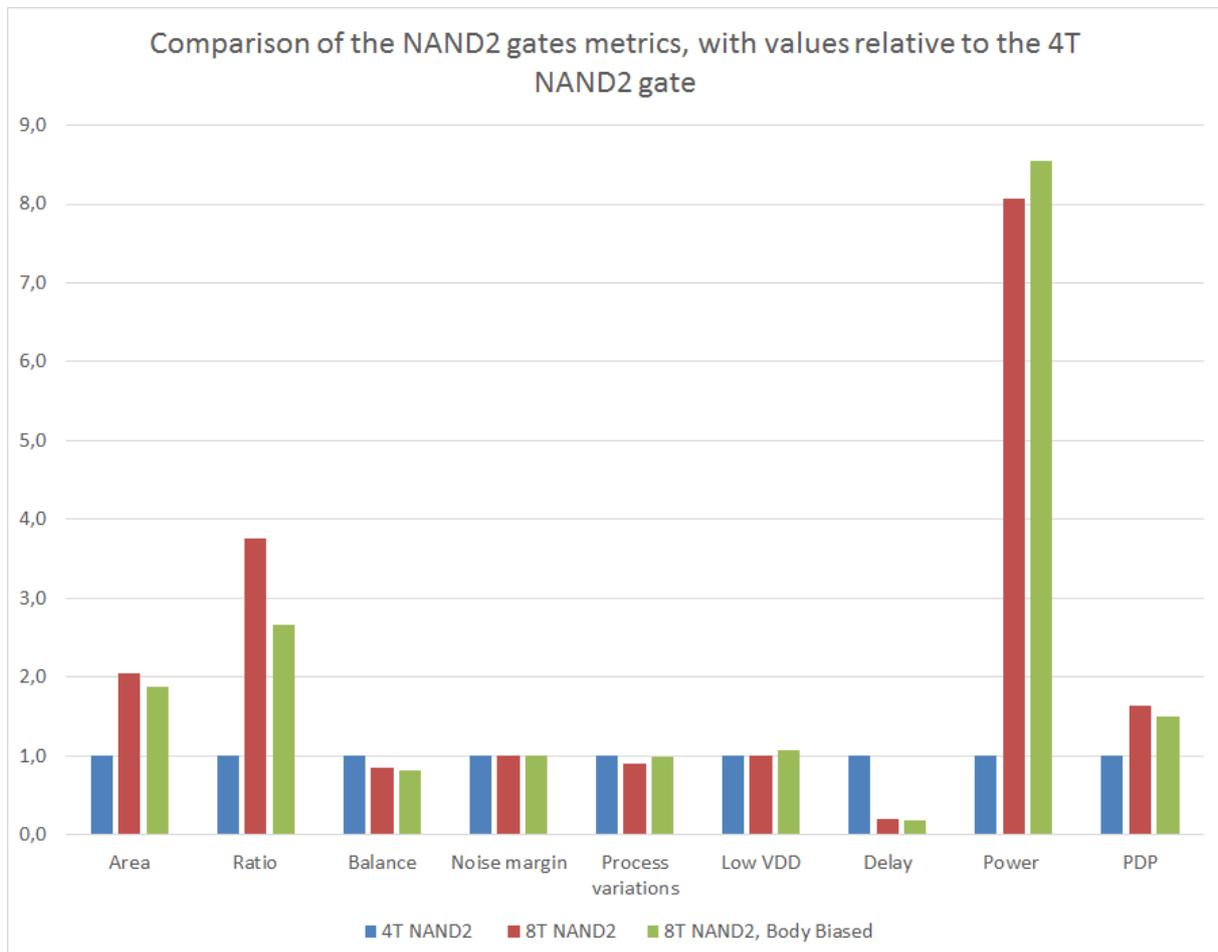


Figure 7.34: Comparison of the relative metrics for the different NAND2 gates

8. Discussion

8.1 Gate balance

8.1.1 Switching point

The tables in chapter 7.1.1 presents the sets of transistor gate sizes that have the lowest and largest transistor gate area, and lowest size ratio between the *pfet* and the *nfet*. They do also satisfy the condition of having an SP_x between 40% and 60% of V_{DD} . The results was used to investigate how gate size, and size ratio affected noise margins, power, delay, supply voltage and process variations. However, first some general tendencies of transistor gate sizing will be discussed here

Low area

The sets of transistor gate sizes that gives the lowest area are presented in tables 7.2 and 7.3. When it comes to gate area, the 2T inverter and the 4T inverter are similar in gate dimensions. The dimensions that give the lowest gate area are the same for both inverters. They achieve *balance* with gate length of 30nm, an *nfet* width of 200nm and a *pfet* width of 700. This gives a size ratio between the widths of $3.5\frac{m}{m}$ and a total gate area of respectively 27fm^2 and 54fm^2 . By increasing the widths to 800nm, both inverters have *good balance*. This gives a ratio of $4\frac{m}{m}$ and a total gate area of respectively 30fm^2 and 60fm^2

The two NAND2 gates have a larger difference in gate dimensions. The 4T NAND2 gate achieves *good balance* with a gate area of 24fm^2 and a ratio of $3\frac{m}{m}$, while the 8T NAND2 gate needed an area of 117fm^2 and a ratio of $8.75\frac{m}{m}$. The 4T were able to achieve *good balance* with a much lower gate area than the 8T NAND2 gate.

For the NOR 2 gates, the opposite was true. The 8T NOR2 was able to achieve *good balance* with a total gate area of 39fm^2 and a ratio of $2.25\frac{m}{m}$. The 4T NOR2 gate needed a gate area of 45fm^2 and a ratio of $6.5\frac{m}{m}$ to have *good balance*.

Large area

The tables 7.4 and 7.5 presents the the sets of transistor gate sizes that give the largest gate area. Again, the inverter had similar sizes. The 2T inverter achieved the largest gate area that also had *good balance* with an area of 108fm^2 and a ratio of $12.5\frac{m}{m}$, while the 4T inverter had an area of 110fm^2 and a ratio of $10.5\frac{m}{m}$. The 4T NAND2 performed better than the 8T NAND2 in terms of achieving the largest area. The 4T was able to get an area of 116fm^2 and a ratio of $6.25\frac{m}{m}$ while having *good balance*. The 8T NAND2 gate achieved an area of 82.5fm^2 and a ratio of $10\frac{m}{m}$. The situation was again the opposite for the NOR2 gates. The 8T NOR2 gate had a larger area of 124fm^2 and a ratio of $4.17\frac{m}{m}$, and *good balance*. The 4T NOR2 only achieved an area of 92.8fm^2 and a ratio of $12.3\frac{m}{m}$.

Low size ratio

As a rule of thumb, the gate size of the *pfet* should be double the size of the *nfet* to obtain a well balanced device. The results in chapter 7.1.1 shows that this ratio might have to be increased at sub-threshold supply voltages. The inverters obtain *balance* with a size ratio of approximately 2,5 which is not so far away from the situations with super-threshold supply voltages. The 4T NAND2 gate and the 8T NOR2 gate achieved *balance* with a size ratio below 2, while the 8T NAND2 gate and the 4T NOR2 gate however, had a ratio above 5.

8.1.2 Noise margin

All the results in chapter 7.1 have an SP_x between 40% and 60% of V_{DD} . This ensures that all the results have a transfer characteristic that is somewhat balanced. To further discuss gate balance, noise margin is a more suitable tool. This is because it identifies how large area of the output signal is a logical state ("1" or "0") or the undefined region. All sets of transistor gate sizes in table 7.7 have a ratio between the lower and higher noise margins of 1. This means that the logical "1" and "0" have equal size on the transfer characteristics and will produce an SP_x close to $\frac{V_{DD}}{2}$. The additional information the noise margins provide is how large noise signals are needed to push the device from a defined logical state to the undefined region.

Inverter

The 2T and 4T inverters have quite similar noise margins. For supply voltages close to $100mV$ they are both below $\frac{1}{3}$ of V_{DD} . Noise signals with an amplitude of $33mV$ can influence the inverters at $V_{DD} = 100mV$. This makes the inverters prone to noise. The 4T inverter has a slightly higher noise margin than the 2T inverter, however the difference is so small that it will not make any difference in most cases. When it comes to order of magnitude, they are equal. At V_{DD} above $108mV$ both the inverters will have mean noise margins above $\frac{1}{3}$ of V_{DD} , and be slightly less prone to noise signals.

NAND2

The 4T and 8T NAND2 gates also have quite similar noise margins. The 8T device has a slightly higher mean noise margin than the 4T NAND2 gate. The mean noise margins for the 4T and the 8T NAND2 gates are below $\frac{1}{3}$ of V_{DD} with V_{DD} close to $100mV$. Both the 4T and the 8T NAND2 gate have a noise margin right below $\frac{1}{3}$ of V_{DD} at $V_{DD} = 130mV$. Even though there is a slight difference in noise margins they are both prone to noise signals at supply voltages in the area $85mV$ to $130mV$.

NOR2

The noise margins of the 4T and 8T NOR2 gates are similar to the Inverters and NAND2 gates in terms of magnitude. The difference from the NAND2 gate is that the traditional 4T topology has a lower mean noise margin than the 8T topology. For V_{DD} close to $100mV$ the noise margins are below $\frac{1}{3}$ of V_{DD} . For the 4T NOR2 gate, the mean noise margin is below $\frac{1}{3}$ for $V_{DD} = 130mV$, while it is above $\frac{1}{3}$ for $V_{DD} = 118mV$ for the 8T NOR2 gate. This means that both NOR2 gates are prone to noise at voltages close to $100mV$.

8.2 Power and delay

8.2.1 PDP

The results of the ring oscillators provides power delay products of each device. This indicates at which V_{DD} least energy is consumed. The power delay product graphs show that the lower

the supply voltage goes, the lower the PDP goes. This is because the power is reduced at a higher rate than the delay is increased as V_{DD} is reduced. For the 2T Inverter the delay is increased from $500ns$ to $1.25us$ when V_{DD} is reduced from $130mV$ to $85mV$. The power is reduced from $94pW$ to $24pW$ for the same change in V_{DD} . The change in delay is $\frac{3}{5}$ of max delay while the change in power is $\frac{7}{9}$ of max power. Due to this, the V_{DD} that gives the lowest energy consumption is the lowest. In order to find the most energy efficient device, the supply voltage must be as low as possible.

8.2.2 Minimum supply voltage

The lowest V_{DD} that support oscillations in the ring oscillator are in the area of $71mV$ to $73mV$. These values are good compared to the goal of $100mV$, however these oscillations have maximum amplitude between 45% and 55% of V_{DD} , which makes them useless for most logical operations. Oscillations between 25% and 75% of V_{DD} , and 5% and 95% of V_{DD} are more likely able to support regular operation of a logical gate. Oscillations between 25% and 75% of V_{DD} are achieved with V_{DD} spanning from $77mV$ (8T NOR2) to $86mV$ (4T NOR2). If the circumstances allows operations with oscillations of this magnitude, the supply voltage can be reduced below $100mV$. If the oscillations of at least 5% and 95% of V_{DD} is required, the supply voltage must be the area $104mV$ to $115mV$, which is also quite close to $100mV$.

The traditional topologies (2T Inverter, 4T NAND2 and 4T NOR2) have a higher V_{DD} and a lower power delay product than the new topologies (4T Inverter, 8T NAND2 and 8T NOR2). So even though the new topologies can have a slightly lower V_{DD} they are less energy effective than the traditional topologies. This is because the traditional gates have a lower delay than the new ones.

8.3 Robustness

Based on the Monte Carlo analysis presented in chapter 7.3 relationships between transistor gate sizing and process variations can be identified. Common for all gates in this project is that the process variations was decreased when the transistor gate area was increased. Another relationship that might be observed is that a low size ratio between the width of the *pfet* and the *nfet* also lowered the process variations. However, the sets with low size ratio also had a large total gate area, so the low process variation for low ratio might just be a bi-effect of a large area.

The Monte Carlo analyses uncovered another important result. The new topologies (4T inverter, 8T NAND2 and 8T NOR2) had lower process variations than the traditional topologies (2T inverter, 4T NAND2 and 4T NOR2). The new topologies had double the amount of transistors compared to the traditional topologies, and therefore also a larger total gate area. The larger gate area was probably the cause of the lower process variations. One anomaly however, is the case of *low area & good balance* for the NOR2 gates. The 4T NOR2 gate had a total gate area of $90fm^2$ while the 8T NOR2 gate had a total gate area of $78fm^2$. In table 7.24 it can be seen that the process variations for the 8T NOR2 was lower than for the 4T NOR2, while the mean values were almost equal. The main difference from these two situations is that the 8T NOR2 had the lowest transistor width ratio.

The robustness of logical gates at sub-threshold voltages can be increased by increasing the total gate area and reduce the ratio between the sizes of the *pfet* and the *nfet*. The use of the new topologies presented in this project can even further increase the robustness.

8.4 Deciding final sizes

8.4.1 Summary

In chapter 7.4.1 the results of the DC analyses and the transient analyses are summarized for the different sets of transistor size sets from chapter 7.1.1. Here are the results further discussed. The figures 7.21, 7.22, 7.23, 7.24, 7.25 and 7.26 shows that there are trade-offs between the different metrics used in this project. There are some general tendencies for all the gates.

Gate balance is affected by the area of the transistor gates. The gate balance was increased as the total gate area and the size ratio between the *pfet* and the *nfet* were increased. This indicates that the unbalance between the strength of *nfet* and *pfet* transistors is larger at sub-threshold voltages than at super-threshold voltages.

The gate area had little influence on the mean noise margins. The mean noise margins were almost equal for all the different sizes of transistor gate sizes. This means that manipulating the transistor dimensions will not influence the size of the *undefined region* in a large degree at sub-threshold voltages. The most effective method for reducing the size of the *undefined region* is to increase the supply voltage.

The robustness of the logical gates are affected by the transistor sizes. Common for all the devices is that the process variations were decreased as the transistor gate area was increased.

The size of the transistor gate lengths had the largest influences on the results from the transient analyses. A larger length decreased the supply voltage needed to support stable operation, and also reduce the power consumption. The delay will however increase, as the length increases. The widths of the transistor gates do also have an effect on the supply voltage, power and delay. A larger width will reduce the delay, and increase the power consumption. Low gate width will reduce the power consumption, but increase the delay. A low gate length will increase the power consumption and lower the delay. This indicates maybe the most prominent trade-off, low delay gives large power, and a large delay gives low power. To help decide what is most energy effective, the power delay product is calculated. The figures in chapter 7.4.1 shows that the lowest power delay product is achieved with the size set *low area & good balance*.

It is important to note that the power delay products in chapter 7.4.1 were measured with $V_{DD} = 100mV$. So the set *low V_{DD} & low PDP* has a lower PDP at the lowest supply voltages it achieves. However the sets *low area & good balance* had a lower PDP at 100mV than the sets *low V_{DD} & low PDP* had at the lowest V_{DD} for the inverters and NOR2 gates. For the NAND2 gates, the lowest PDP was achieved by the sets *low V_{DD} & low PDP* at the lowest supply voltages. In table 8.1 below this is shown.

| Set | Device | V_{DD} (mV) | PDP (aJ) |
|------------------------|-------------|---------------|----------|
| Low V_{DD} & low PDP | 2T inverter | 73 | 42,1 |
| Low area & GB | 2T inverter | 100 | 33,6 |
| Low V_{DD} & low PDP | 4T inverter | 71 | 75,5 |
| Low area & GB | 4T inverter | 100 | 55,5 |
| Low V_{DD} & low PDP | 4T NAND2 | 73 | 37,8 |
| Low area & GB | 4T NAND2 | 100 | 50,3 |
| Low V_{DD} & low PDP | 8T NAND2 | 73 | 165 |
| Low area & GB | 8T NAND2 | 100 | 210 |
| Low V_{DD} & low PDP | 4T NOR2 | 75 | 141 |
| Low area & GB | 4T NOR2 | 100 | 82,6 |
| Low V_{DD} & low PDP | 8T NOR2 | 72 | 122 |
| Low area & GB | 8T NOR2 | 100 | 75,1 |

Table 8.1: Comparison of the power delay product.

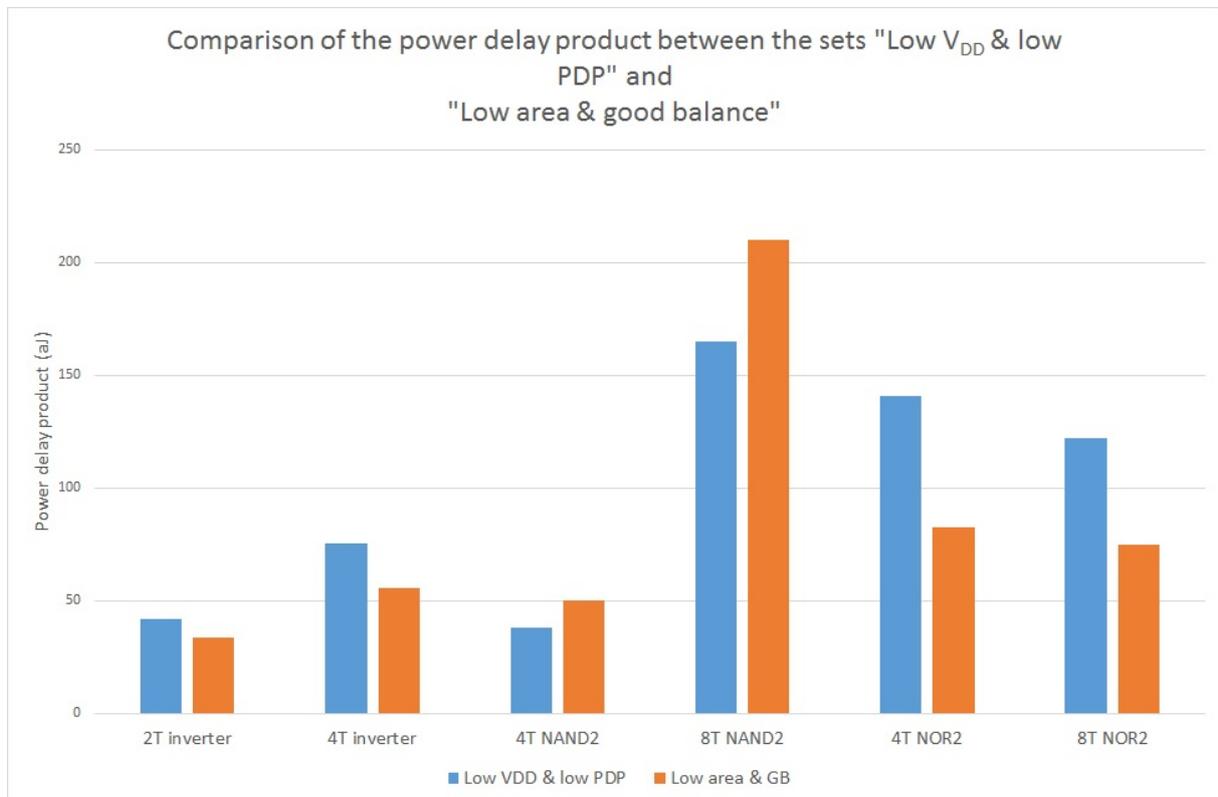


Figure 8.1: Comparison of the power delay product.

8.4.2 Final sizes

One of the main goals of this project was to create logical gates that were able to operate at a low V_{DD} . The results that supported the lowest V_{DD} in the ring oscillators were too unbalanced to satisfy the requirement of having an SP_x between 40% and 60% of V_{DD} . In a noiseless environment the sets with the lowest V_{DD} would have been a good choice due to low supply voltage, low PDP and decent robustness.

Instead was the set *Low VNM ratio* chosen for all the devices. This is because it is a set that have good results in the DC analyses. It has *good balance* and low process variations. When it comes to the transient analyses the performance was more average. It was not the set that was most energy efficient, but have a decent performance relative to the lowest V_{DD} and PDP. It was amongst the sets that were least prone to noise and variations in the manufacturing process. This makes it a set that is likely to function properly in a practical implementation, but still have a relative low V_{DD} , and was therefor chosen to be the final set.

8.4.3 Comparing topologies

The figure 7.27 in chapter 7.4.2 indicates the main differences between the traditional topologies (2T inverter, 4T NAND2 and 4T NOR2) and the new topologies (4T inverter, 8T NAND2 and 8T NOR2). The new topologies have a larger area, this is not surprising since they have double the amount of transistors. The new topologies achieved a little better gate balance than the traditional ones, but the mean noise margins were almost the same. The lowest V_{DD} were also quite similar for all devices. When it comes to process variations, the new topologies performed better than the traditional ones. Power and delay, were a little inconsistent for the different devices, but the power delay product was lowest for the traditional topologies.

The new topologies tested in this project give better performance in terms of gate balance and process variations compared to the traditional topologies. They are however, less energy effective and have a larger transistor gate area.

8.5 Effects of body biasing

The two figures 7.28 and 7.29 in chapter 7.5 shows how biasing the bulks of the *nfet* and the *pfet* affects the gate balance. Reverse biasing the bulk increased the transistors threshold voltage making the transistors *weaker*. Forward biasing the bulk, did the opposite, lowering the threshold voltage and making the transistors stronger. In sub-threshold the *nfet* is stronger than the *pfet*. To reduce this unbalance the *nfet* needs to be reverse biased, while the *pfet* must be forward biased. Figure 7.30 shows how this body bias configuration was used to balance an 8T NAND2 gate.

By forward biasing the *pfet* with 100mV, and reverse biasing the *nfet* with 100mV the sets size ratios in table 7.34 were created. The requirements to SP_x were the same, but they were achieved with lower ratio between the widths of the *pfet* and the *nfet*.

The figures 7.31, 7.32 and 7.33 shows how the body biasing affected power, delay and the power delay product in the ring oscillator with the transistor gate size set *low area & good*

balance. For this size set, the power and the delay was slightly reduced, resulting in a reduction of the power delay product compared to the unbiased 8T NAND2 gate.

Tables 7.35, 7.36, 7.37, 7.38 and figure 7.34 presents the results of the DC and transient analyses for the 8T NAND2 gate with body biasing compared to the other NAND 2 gates. The body biased 8T NAND2 gate performed relatively similar to the unbiased 8T NAND2 gate. The main differences were that the body biased version had a smaller gate area and a lower gate size ratio, and a lower power delay product.

The main benefits of body biasing the 8T NAND2 gate is that it will take less area and consume less energy while still performing quite similar to an unbiased gate in terms of balance, noise margins and process variations.

8.6 Evaluation of the method

8.6.1 Constructing the logical gates

All gates were created in Cadence Virtuoso with schematics and symbols. They were created according to the theoretical schematics in chapter 2.1 with extra inputs to the bulks of the *nfet* and *pfet*. Few problems were encountered during the construction of the gates, and the work was performed in a time effective manner.

8.6.2 Testing the logical gates

The test benches used to test the logical gates were created in Cadence Virtuoso with schematics. The tool used for testing the gates was ADE XL. Construction of the test benches and the setup of the tests were done with few problems.

The main method for testing the logical gates in this project was to run large parametric analyses with different transistor gate dimensions. The results of these analyses have been post processed using excel to identify the largest and lowest values. This method has made sure that many results have been included and examined. This has resulted in a thorough investigation, that have been very time consuming, which limited the scope of this project. The large analyses ensured that all results within the test parameters were investigated and included in the post evaluation.

8.6.3 Sources of errors

In this project many transistor gate sizes was tested at different supply voltages in both DC and transient analyses. The problem with this large tests was actually the amount of test results produced. Even though all results were available, to identify important results was at time somewhat confusing and difficult. There might still be results that need more attention hidden in the maze of all the test results. When faced with such a mass of raw data, the chance for human error is present.

Another source of errors are that important results might be outside the parameters of the tests. Since much time and effort was used on the results within the test parameters, the boundaries of the tests them self was not investigated in dept. Transistor sizes and voltages

outside the boundaries presented in chapter 6 were unfortunately not investigated.

All tests performed in this project was solely based on schematic design. An effect of this is that all test results are theoretical values lacking the parasitic parameters that will be added with a practical implementation. If layouts were made, the tests results would have given a more realistic representation on how the logical gates had performed.

The test benches used for the DC analyses of the NAND2 gates and the NOR2 gates only investigated the the case when one output changed from "0" to "1" while the other input was connected to V_{DD} and gnd respectively. The case of an inverter coupled NAND2 or NOR2 was not investigated. The test benches for the transient analyses only considered the inverter coupled case. Some important sets of transistor sizes might have been found if the other cases were tested.

8.6.4 What could have been done differently

The majority of the time spent on this project have been used to run large simulations and post process the results. This have limited the investigation to schematic analyses within rigid test parameters. If fewer devices were investigated with less parametric analyses, more time would probably have been available for investigating other tests and creating layouts. Other areas of investigation could have been rise time and fall time, DC analyses of inverter coupled NAND2 and NOR2, ring oscillators without inverter coupled NAND2 and NOR2 gates, ring oscillators with more than 3 devices, and of course layout with parametric extractions.

Layout would especially be included if this project were to be repeated. A parametric extraction could have provided valuable information about how a practical implementation would have behaved.

9. Conclusion

9.1 What were done

In this project the three logical gates Inverter, 2-input NAND and 2-input NOR were constructed in Cadence Virtuoso. Each gate was constructed with two different topologies. All gates were able to operate with a supply voltage below the transistors threshold voltage, and can therefore be referred to as sub-threshold logical gates. All gates were tested with DC and transient analyses and the following metrics were measured; Area, balance, noise margin, process variations, supply voltage, power, delay and energy. Based on this, the different topologies for each gate were compared to each other.

9.2 Comparing results to task specification

All gates that the task specification described were constructed, and they were able to operate at sub-threshold voltages. They were also tested according to the metrics described in the project specification. One of the main goals in this project was to push the supply voltage as low as possible. Nowaks statement of 100mV being the practical lower limit for V_{DD} was challenged[4]. Gates able to operate at V_{DD} close to 80mV were created. These gates however, were unbalanced and prone to noise. Logical gates with satisfactory tolerance for noise and process variations were able to operate with a V_{DD} between 108mV and 146mV.

The new gate topologies were compared to the traditional ones. The new topologies had a larger transistor gate area, were more robust towards process variations, but were less energy effective. This result is quite similar to the results found with the same gate topologies and the 65nm library[1].

The effect of body biasing were tested. The results showed that the gate area, and energy consumption could be decreased without influencing the other metrics, by the use of body biasing.

9.3 Conclusion

Creating sub-threshold logic is possible. The low V_{DD} will reduce the performance of the gates in terms of gate area, noise margins, robustness towards process variations and delay. Different gate topologies, different transistor gate dimensions and bulk biasing can mitigate some of these trade-offs.

The benefits of the new topologies tested in this project (4T Inverter, 8T NAND2 and 8T NOR2) is that they can mitigate process variations and increase gate balance. The negative properties of the new topologies are that they consume more energy and occupies a larger gate area than the traditional gates (2T inverter, 4T NAND2 and 4T NOR2). The gates that had the largest benefit of the new topology were the inverter and the NOR2 gate. The traditional 4T topology of the NAND2 had better performance than the new 8T topology.

The focus of this project has been to do in dept investigations on the theoretical characteristics of the different logical gates. Large amounts of tests have been performed, and lots of test results have been post processed to ensure that the most important results were identified and further investigated.

9.4 Further work

The natural next stage of this project will be to create layouts based upon the final transistor sizes. A layout can take the theoretical values found here and investigate how a practical implementation would behave. After layouts have been created the construction of larger logical structures can begin. For implementation in a *sleep mode* circuit, a real time counter would be interesting to create.

A. Schematics

A.1 Test bench nfet

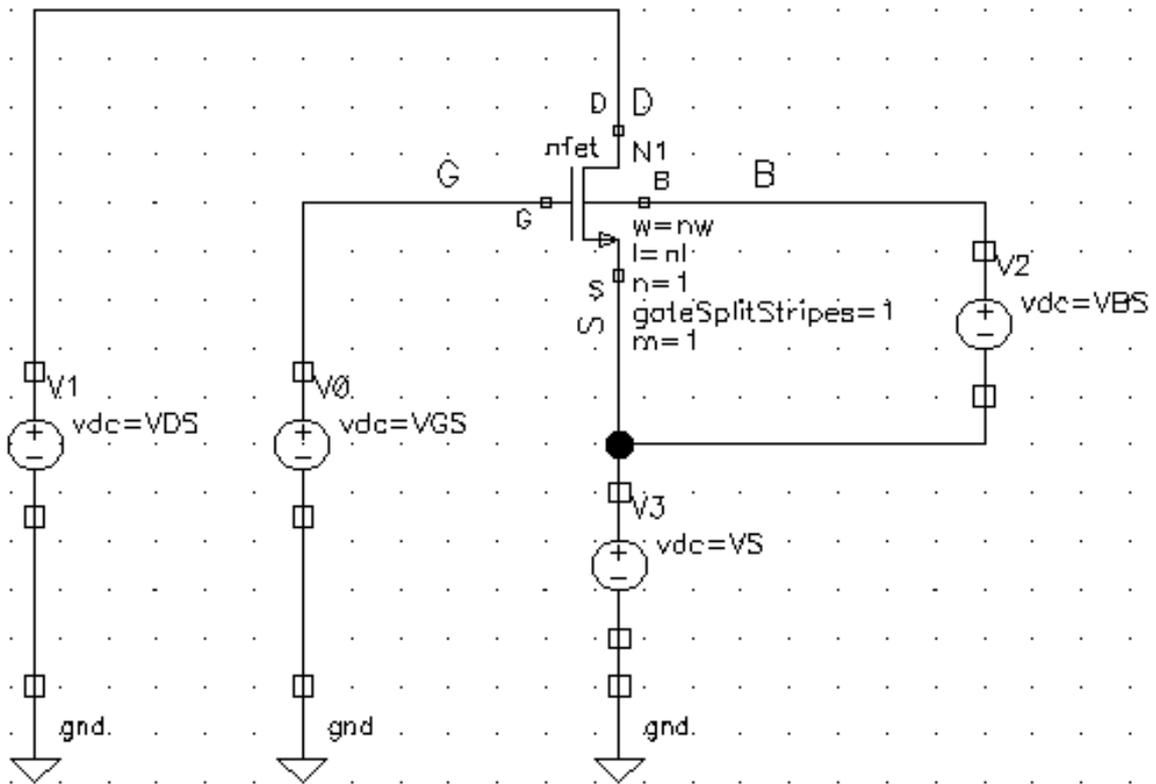


Figure A.1: Nfet testbench schematic

A.2 Testbench pfet

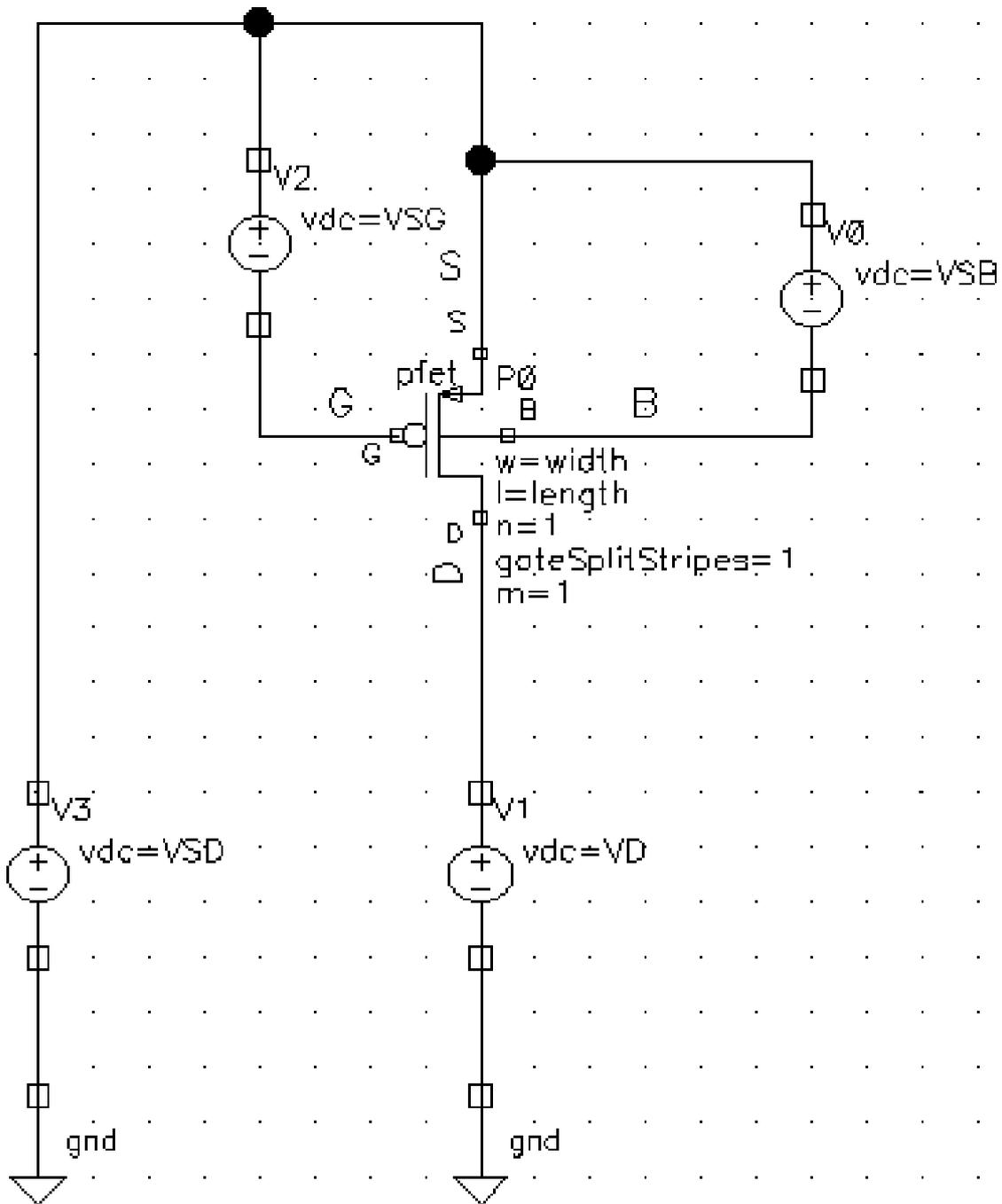


Figure A.2: Pfet testbench schematic

A.3 2 Transistor inverter schematic

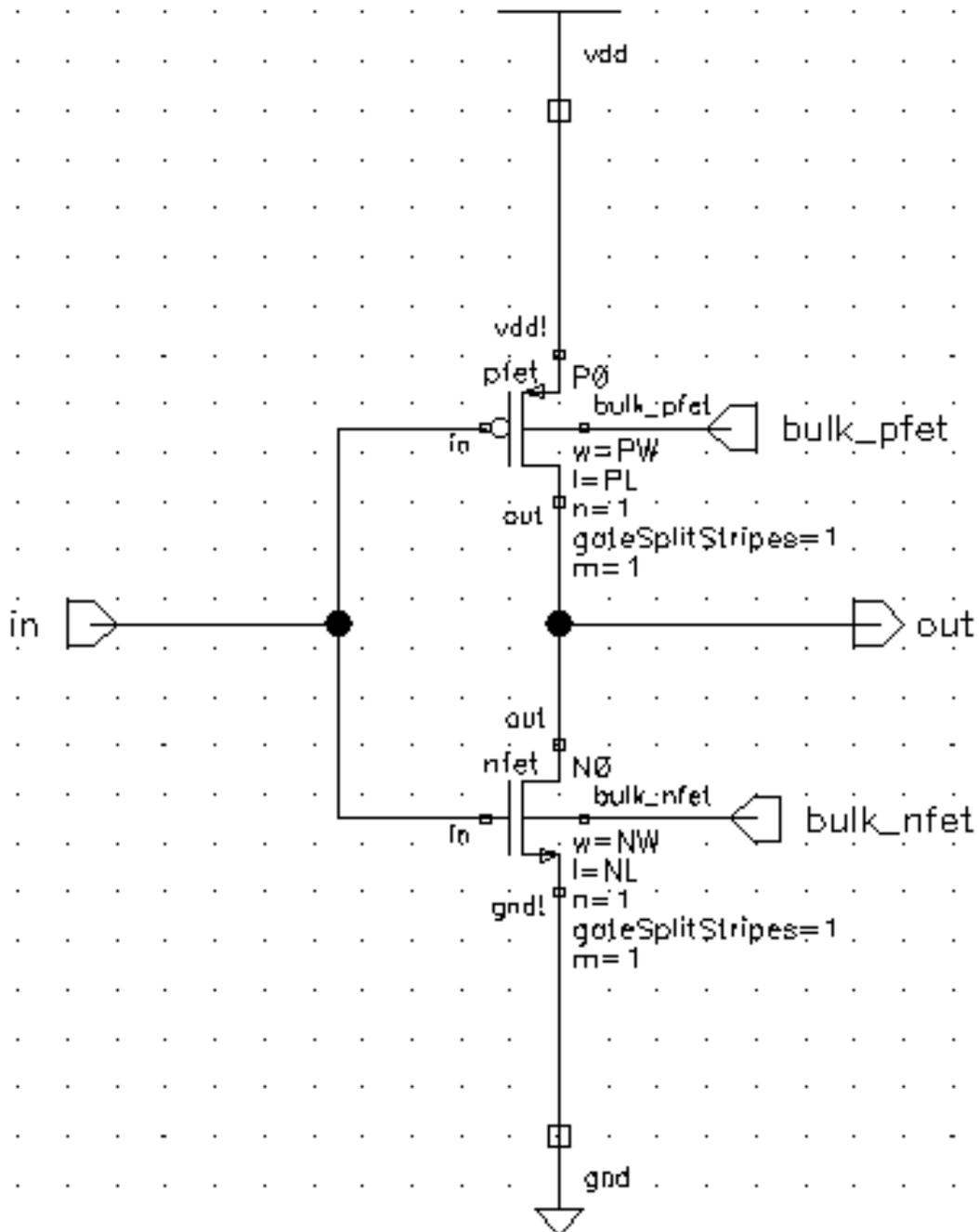


Figure A.3: 2 Transistor inverter schematic

A.4 2 Transistor inverter symbol

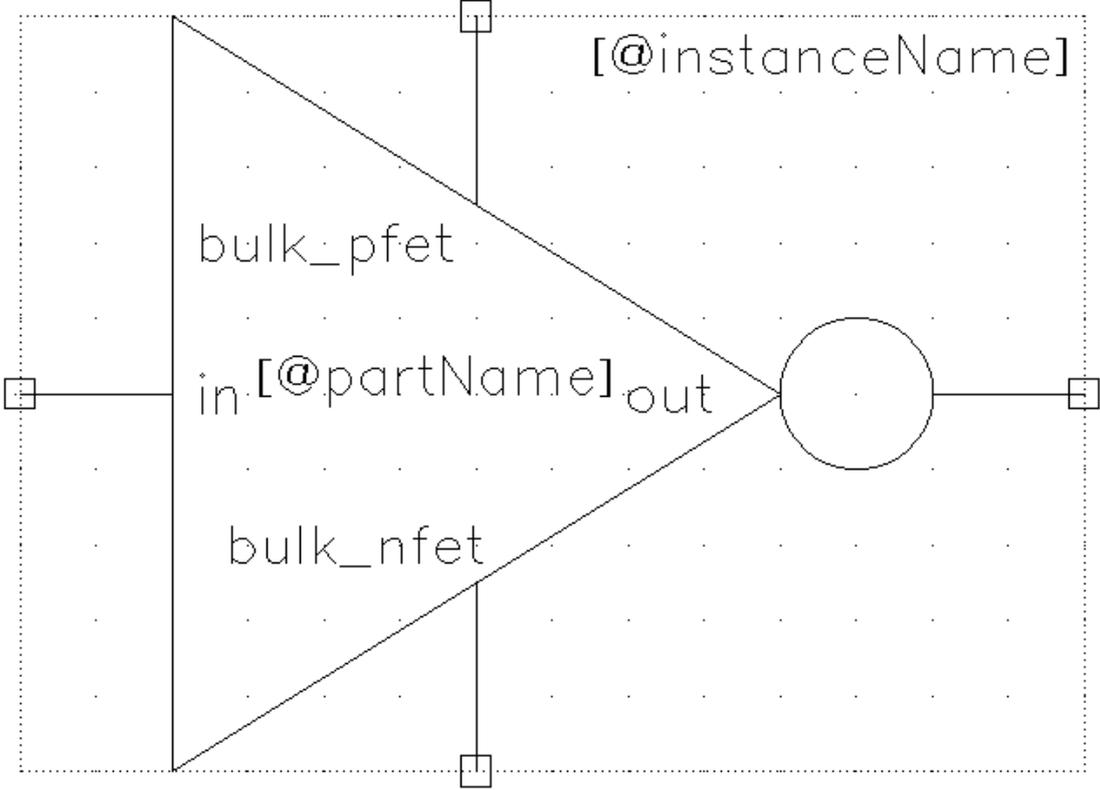


Figure A.4: 2 Transistor inverter symbol

A.5 2 Transistor inverter test bench

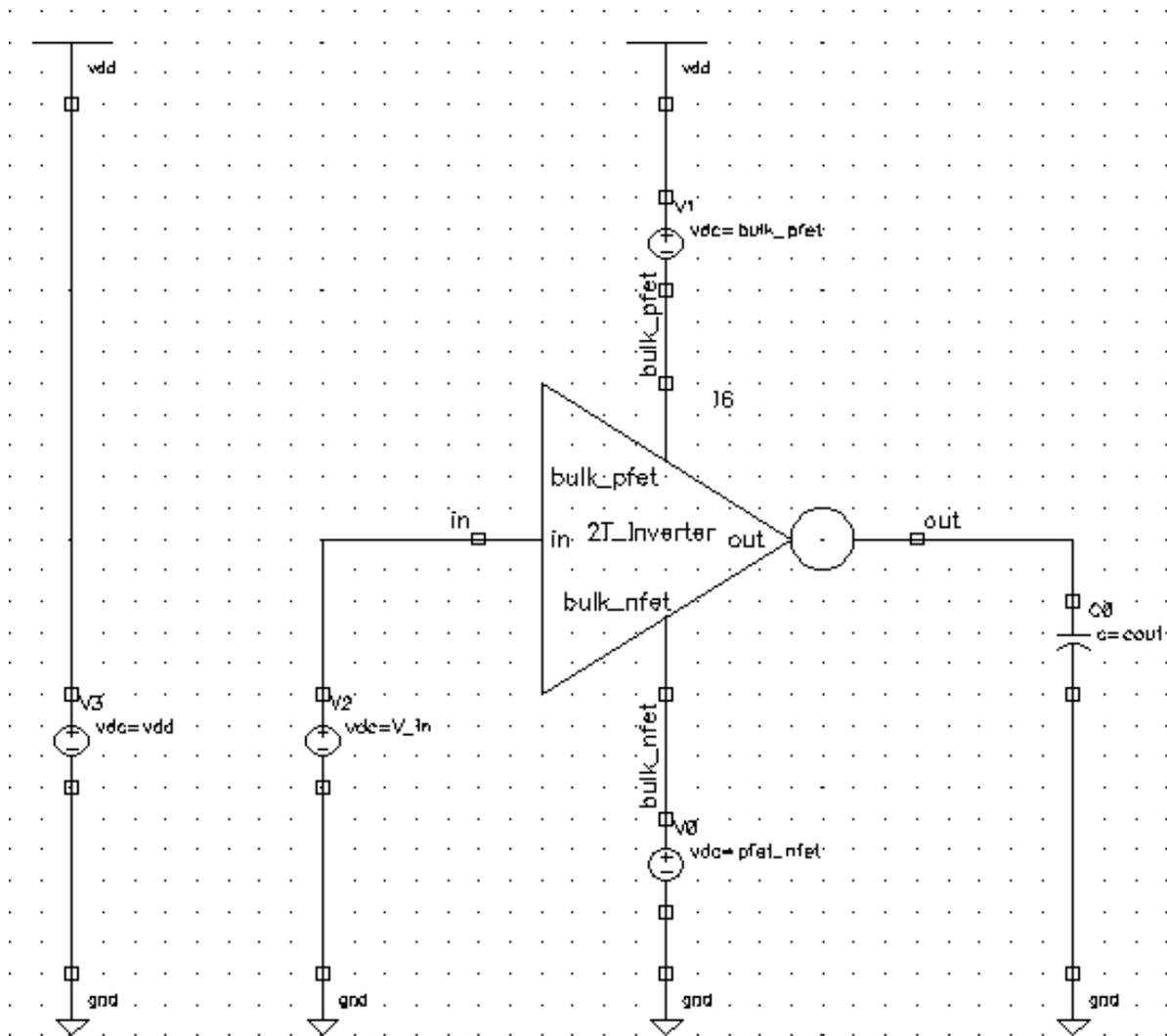


Figure A.5: 2 Transistor inverter test bench

A.6 2 Transistor inverter ring oscillator

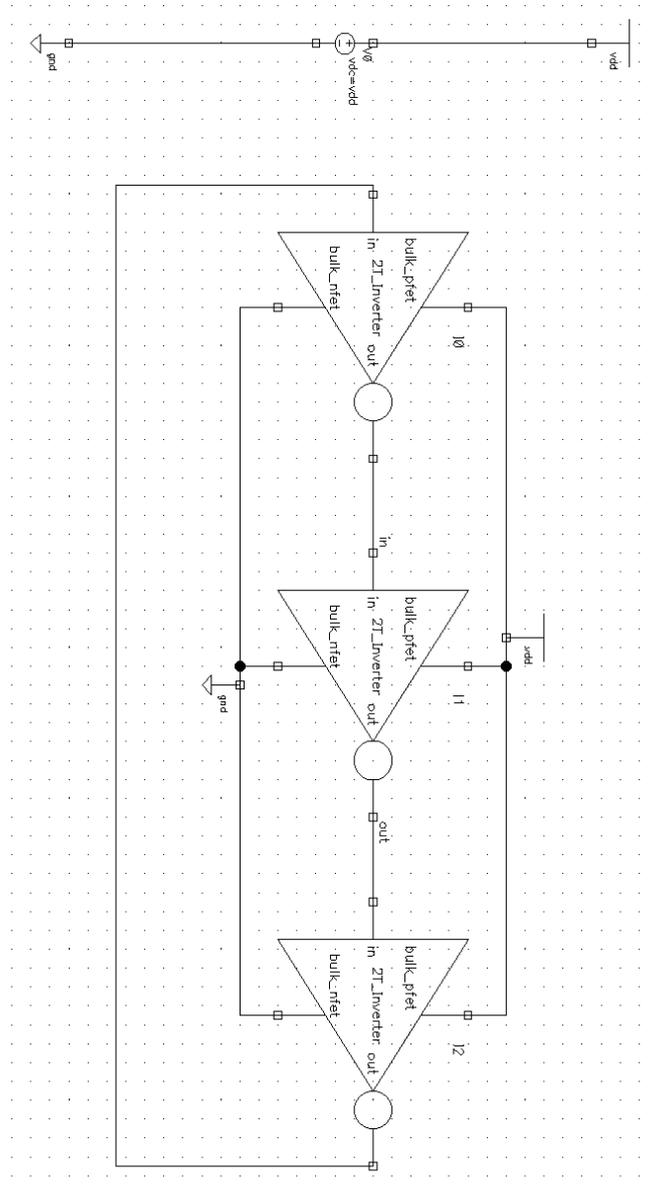


Figure A.6: 2 Transistor inverter ring oscillator

A.7 4 Transistor inverter schematic

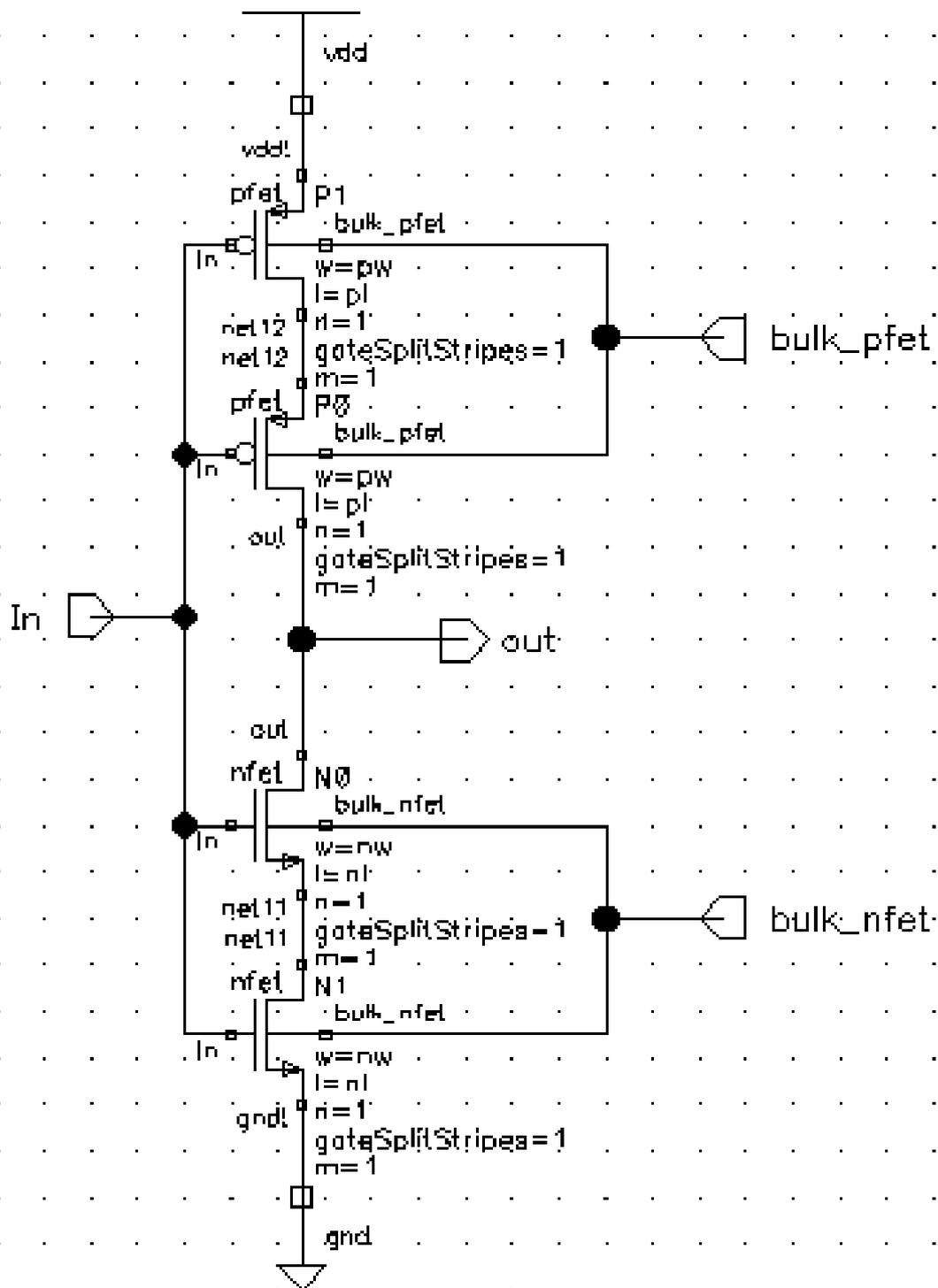


Figure A.7: 4 Transistor inverter schematic

A.8 4 Transistor inverter symbol

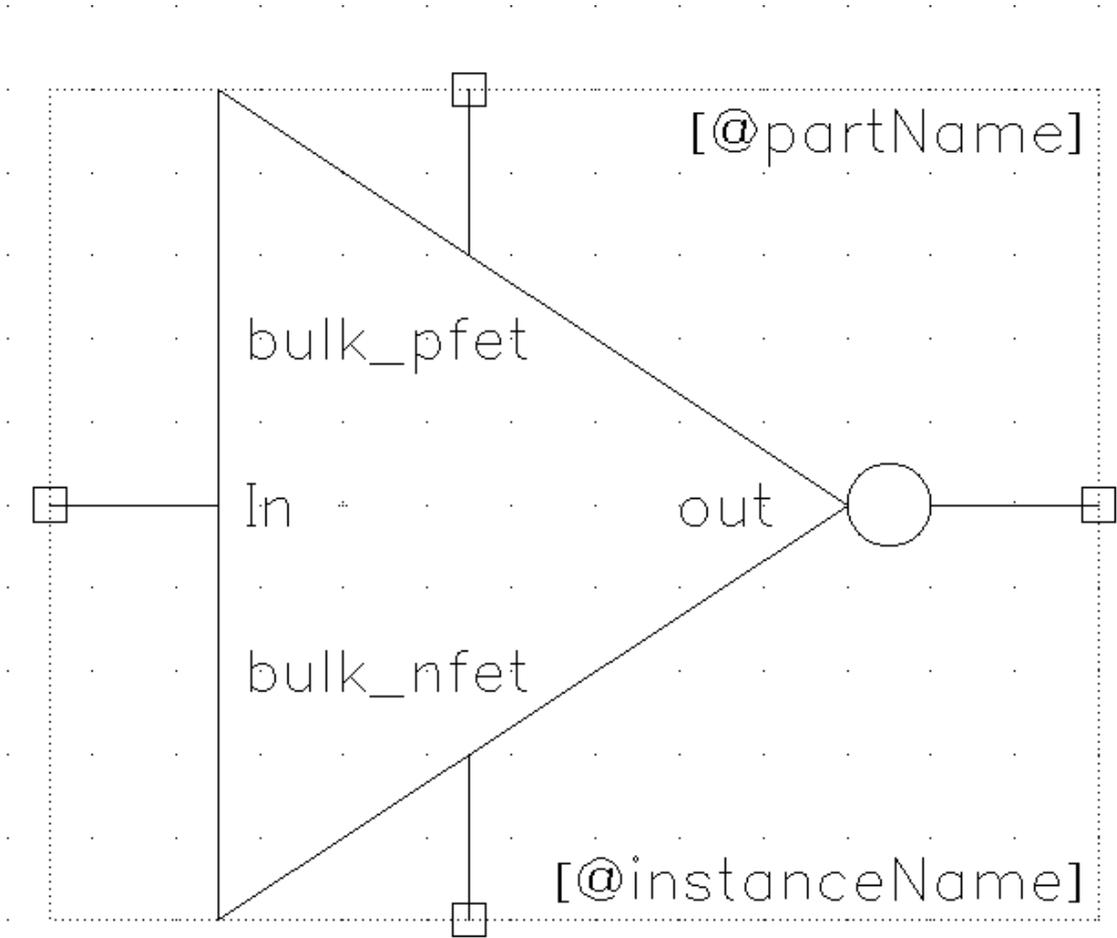


Figure A.8: 4 Transistor inverter symbol

A.9 4 Transistor inverter test bench

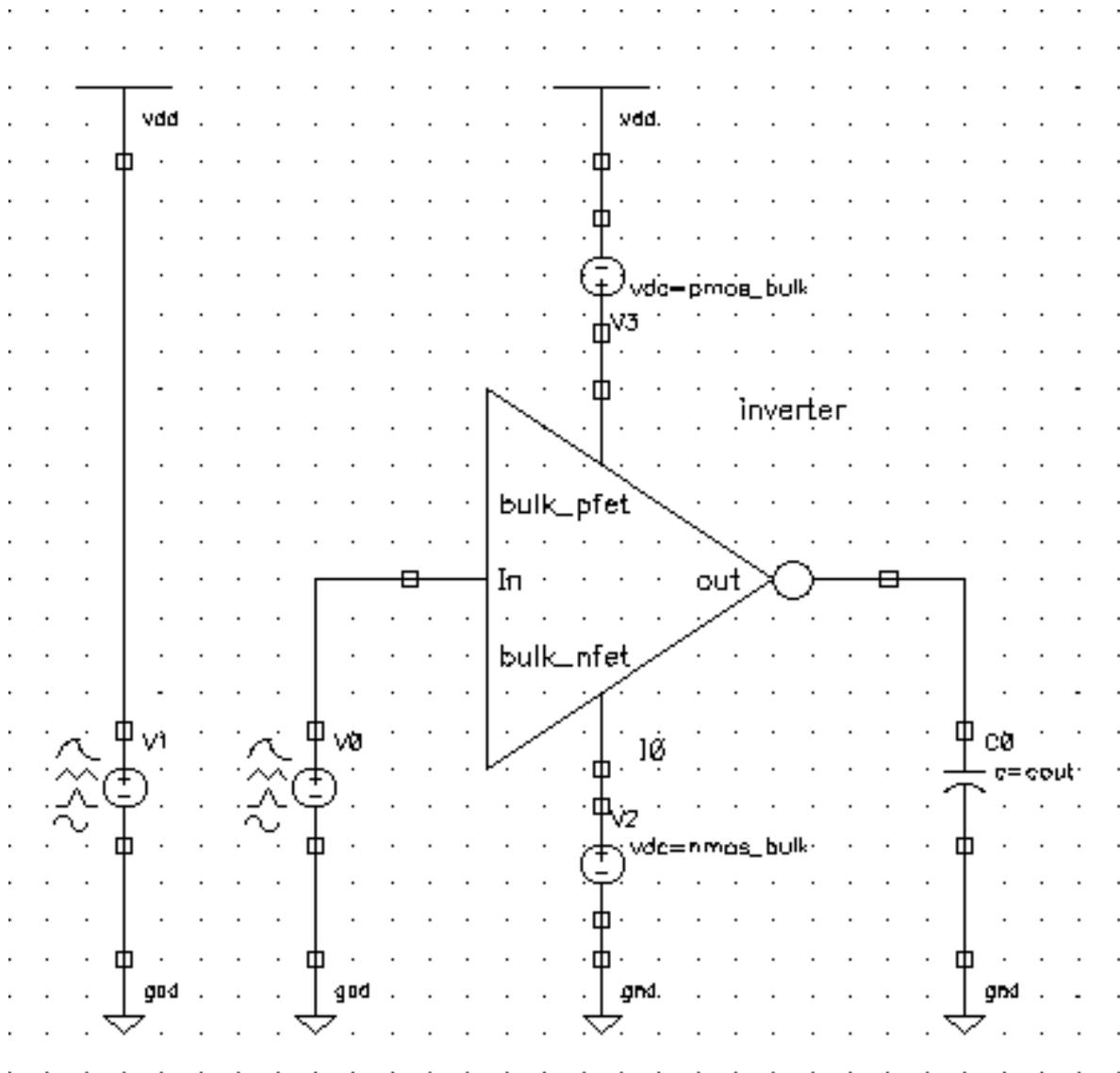


Figure A.9: 4 Transistor inverter test bench

A.10 4 Transistor inverter ring oscillator

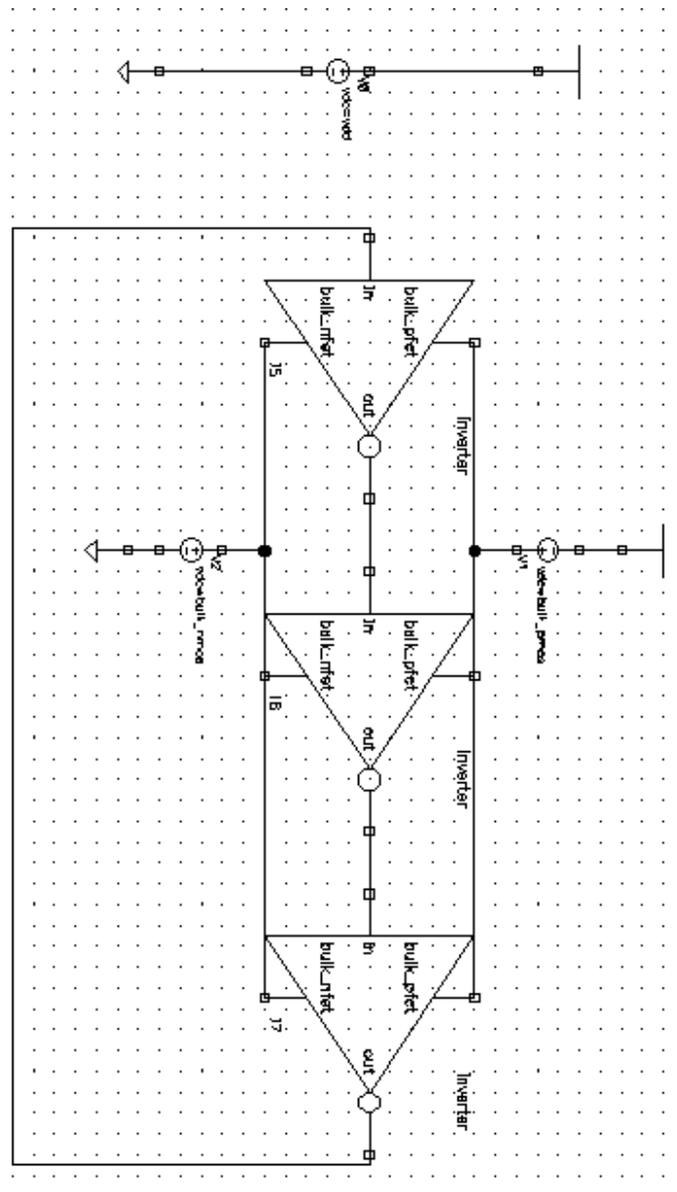


Figure A.10: 4 Transistor inverter ring oscillator

A.11 4 Transistor NAND2 gate schematic

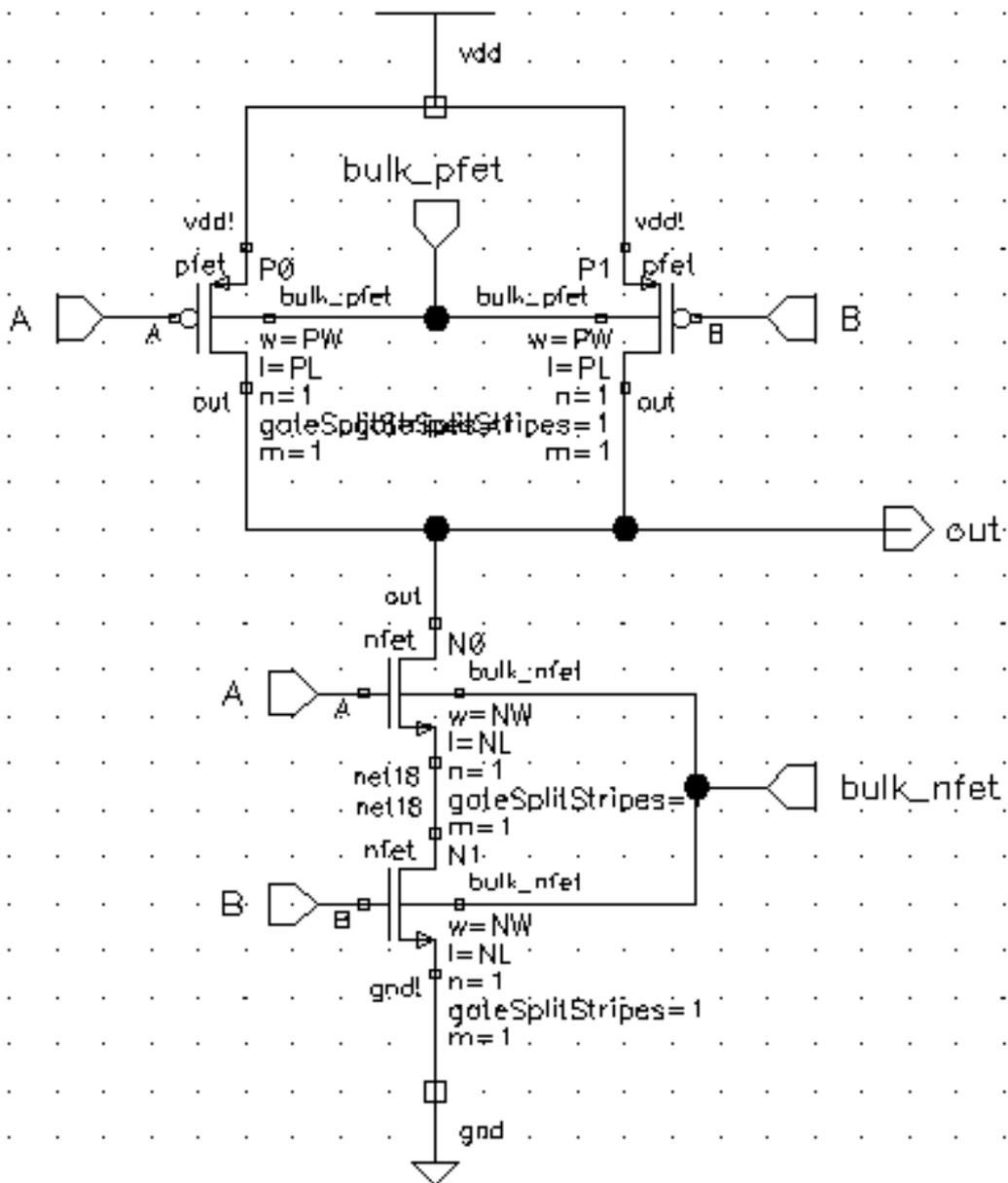


Figure A.11: 4 Transistor NAND2 gate schematic

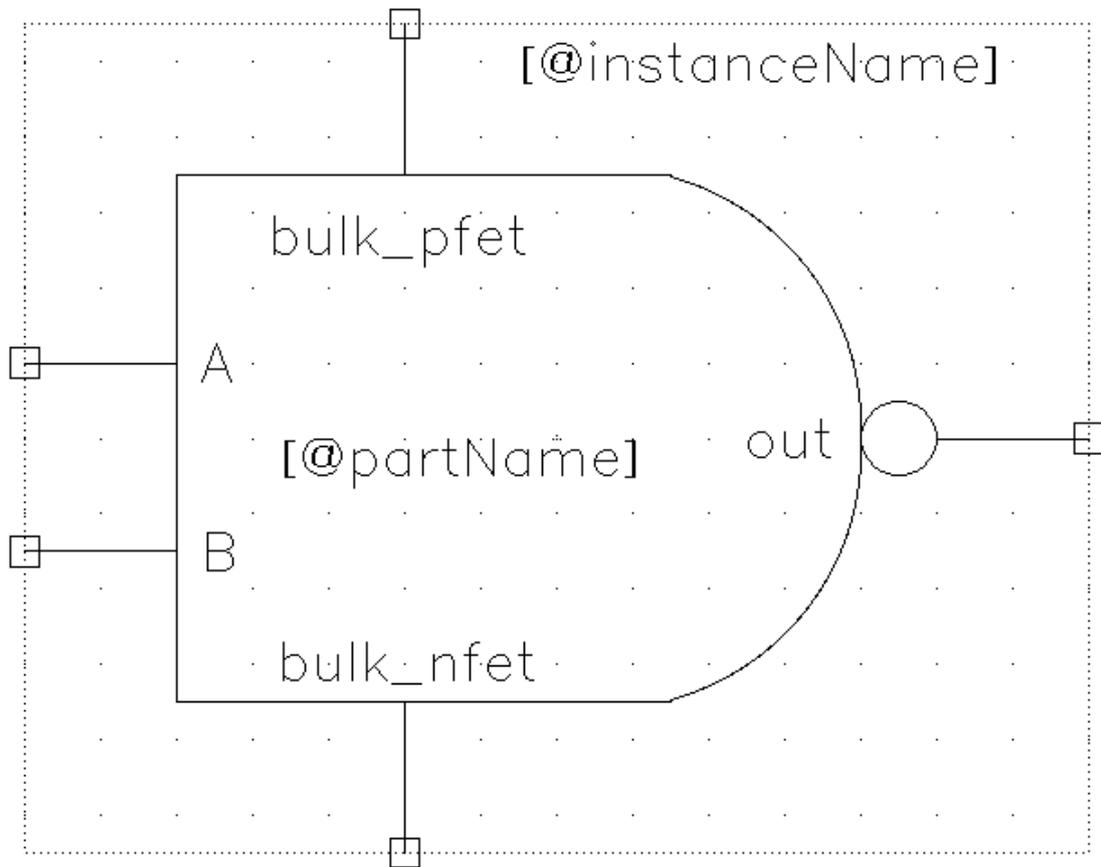
A.12 4 Transistor NAND2 gate symbol

Figure A.12: 4 Transistor NAND2 gate symbol

A.13 4 Transistor NAND2 gate test bench

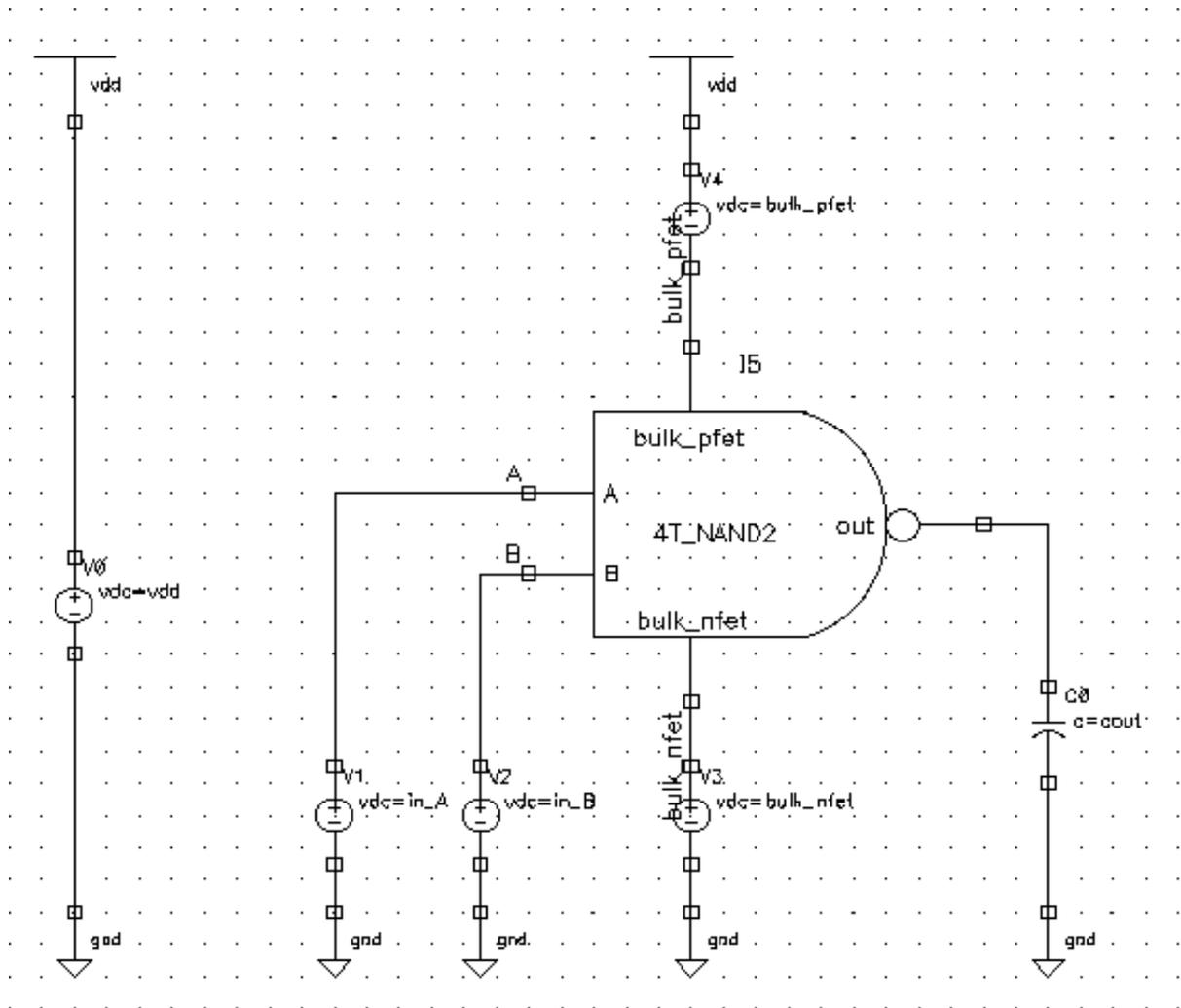


Figure A.13: 4 Transistor NAND2 gate test bench

A.14 4 Transistor NAND2 gate ring oscillator

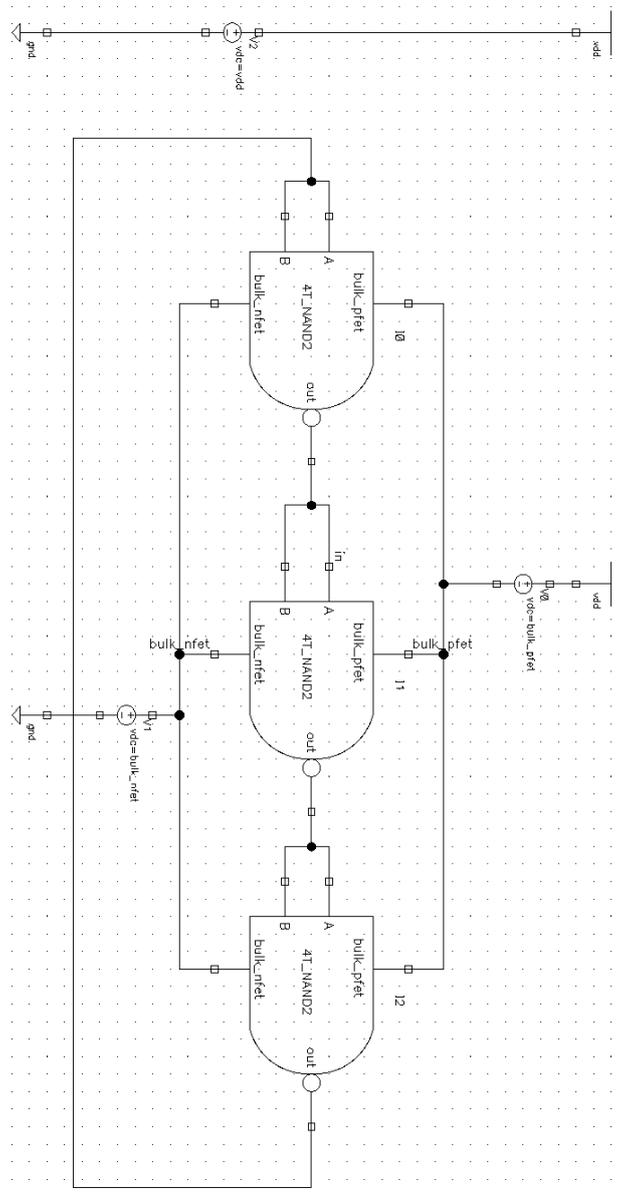


Figure A.14: 4 Transistor NAND2 gater ring oscillator

A.15 8 Transistor NAND2 gate schematic

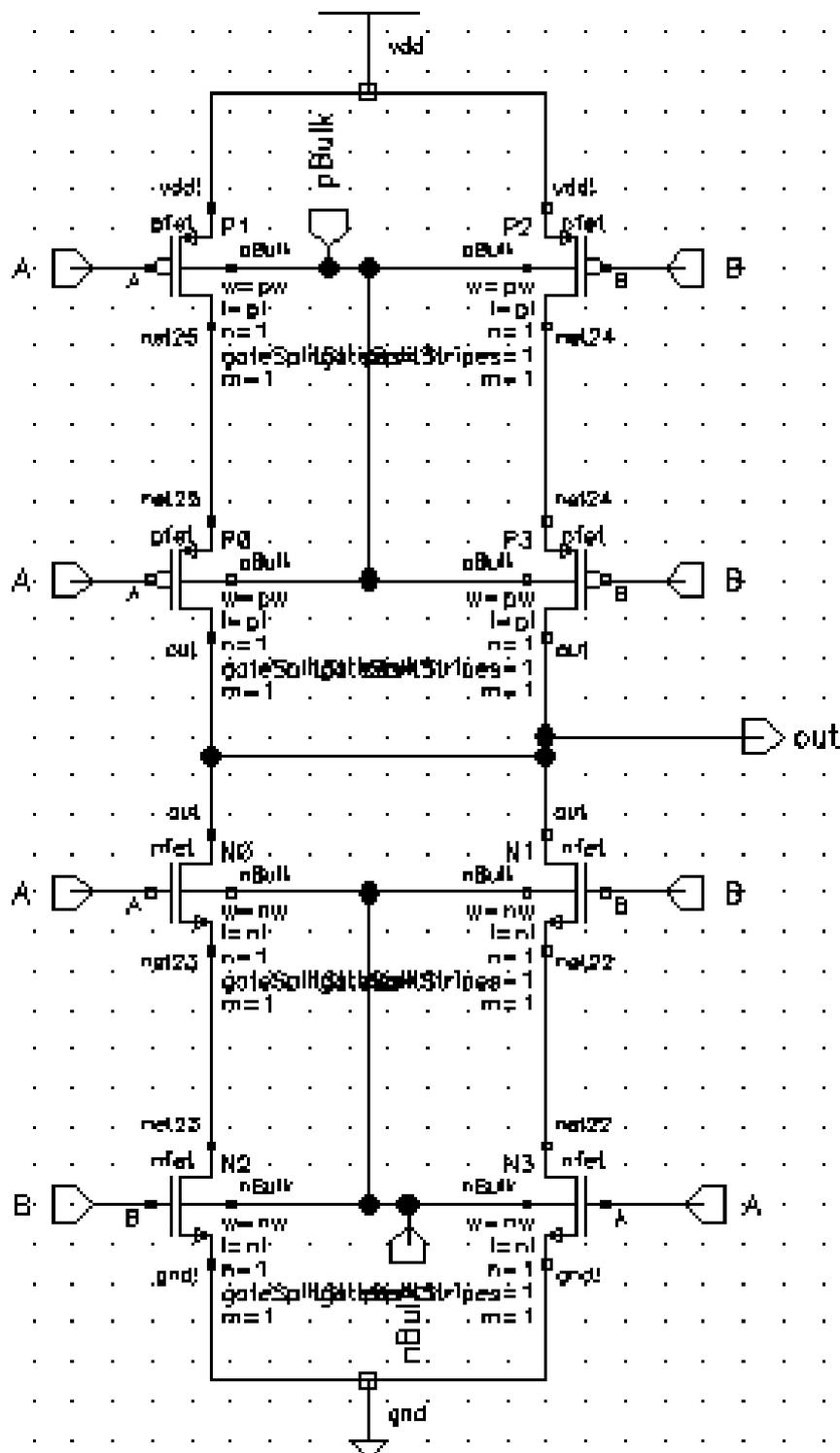


Figure A.15: 8 Transistor NAND2 gate schematic

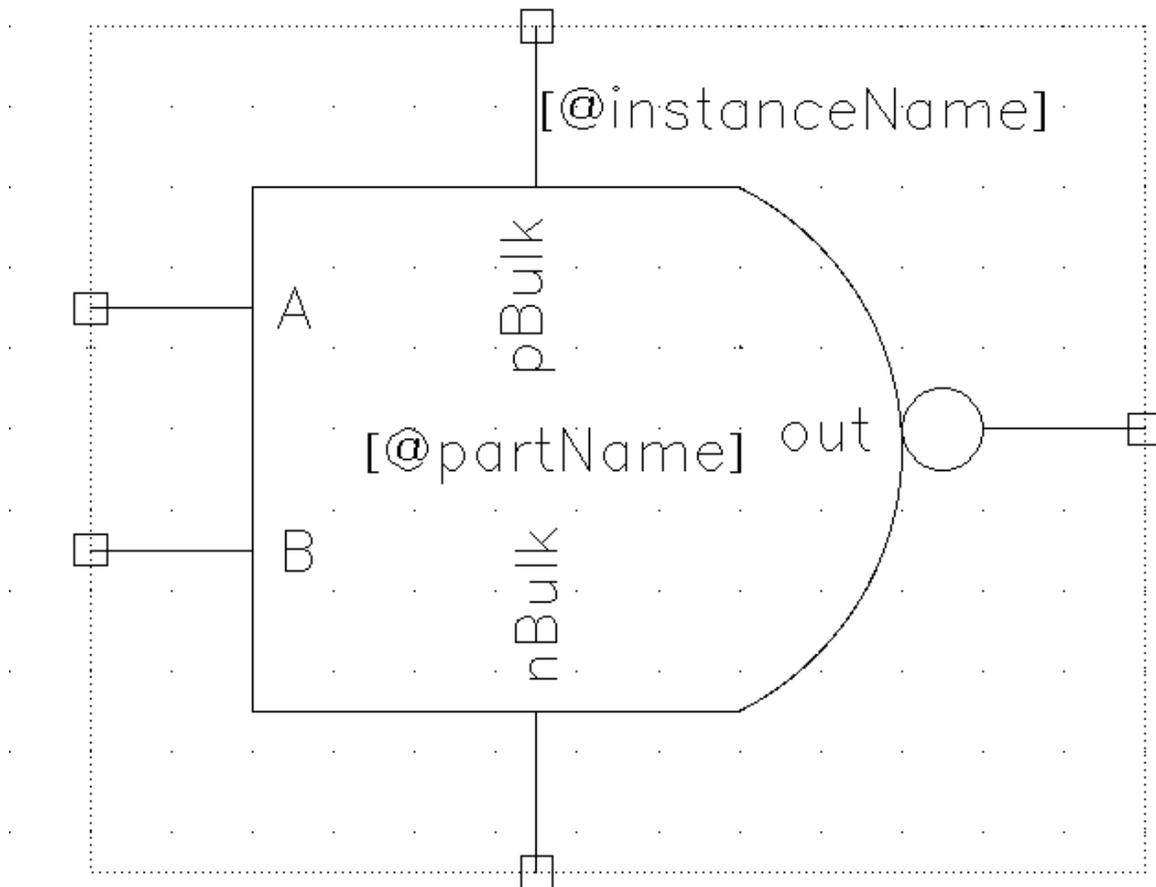
A.16 8 Transistor NAND2 gate symbol

Figure A.16: 8 Transistor NAND2 gate symbol

A.17 8 Transistor NAND2 gate test bench

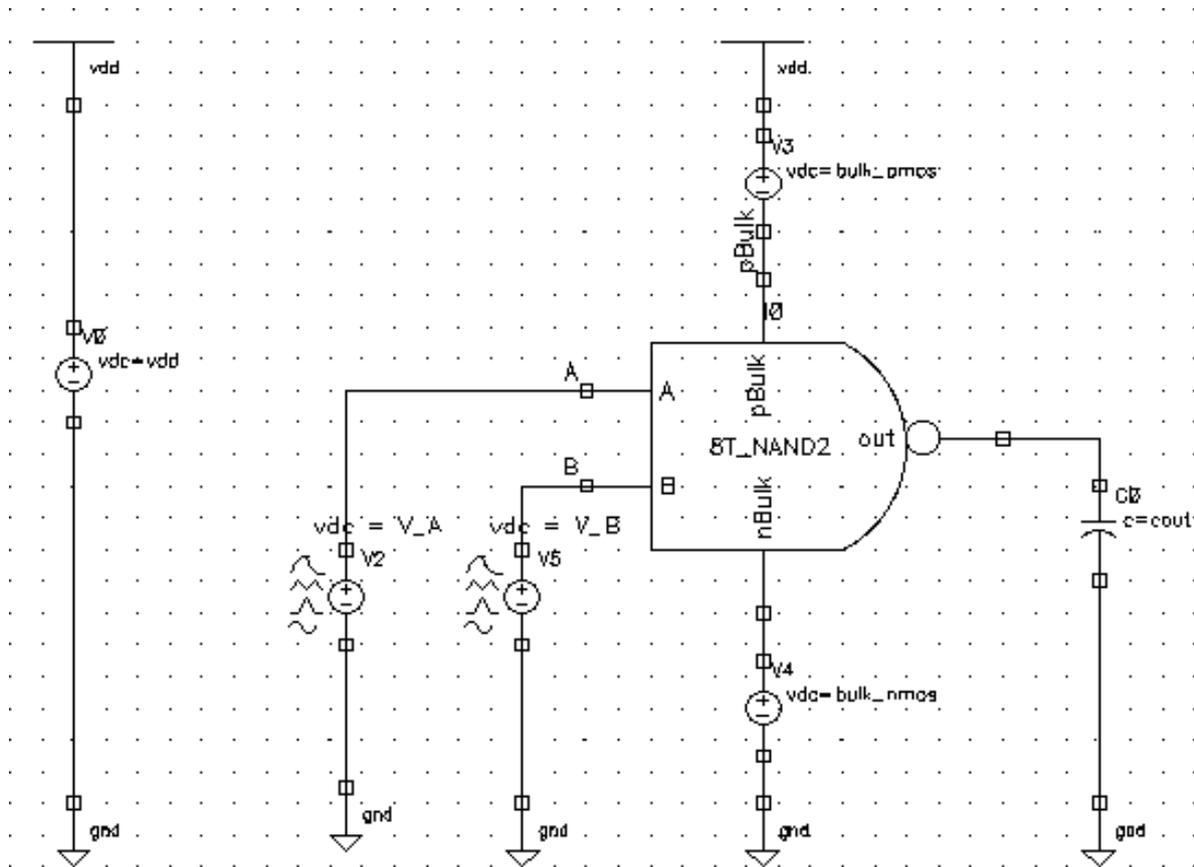


Figure A.17: 8 Transistor NAND2 gate test bench

A.18 8 Transistor NAND2 gate ring oscillator

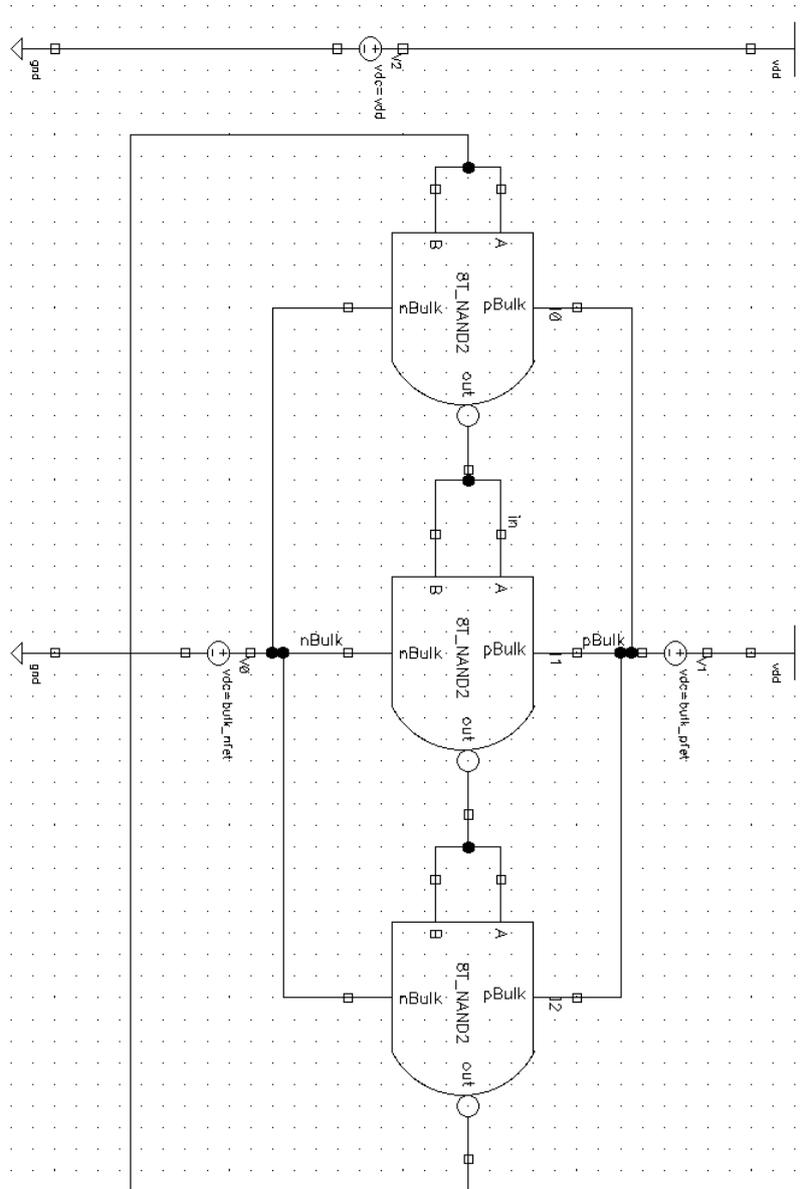


Figure A.18: 8Transistor NAND2 gater ring oscillator

A.19 4 Transistor NOR2 gate schematic

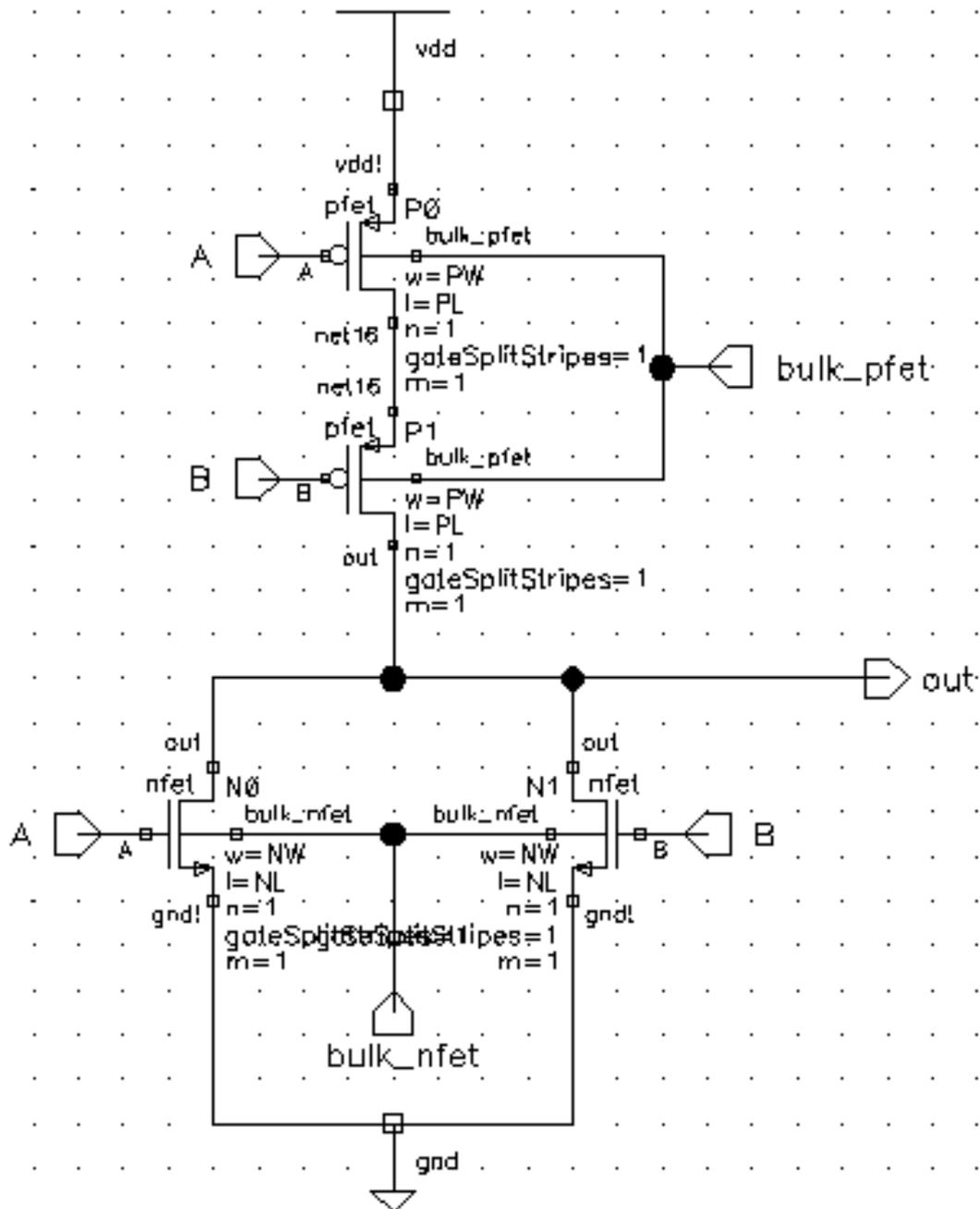


Figure A.19: 4 Transistor NOR2 gate schematic

A.20 4 Transistor NOR2 gate symbol

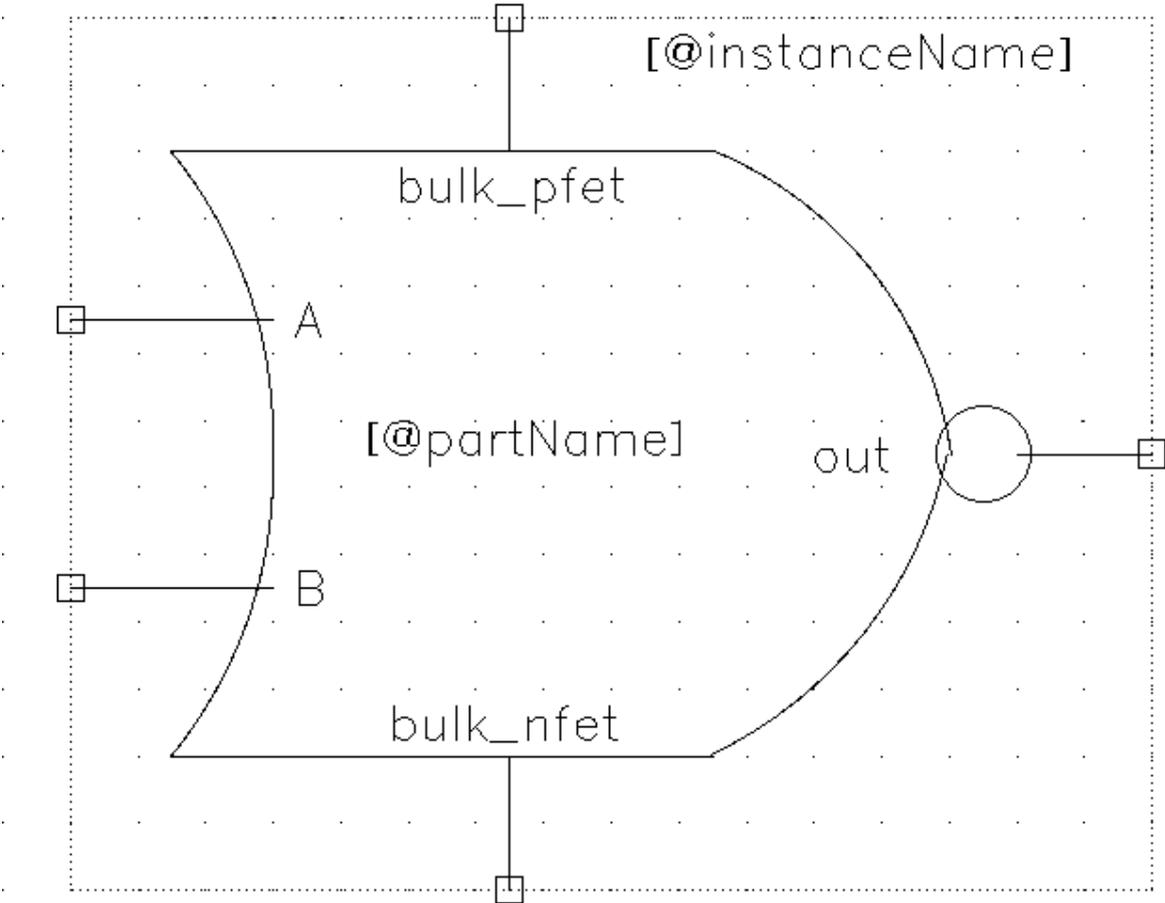


Figure A.20: 4 Transistor NOR2 gate symbol

A.21 4 Transistor NOR2 gate test bench

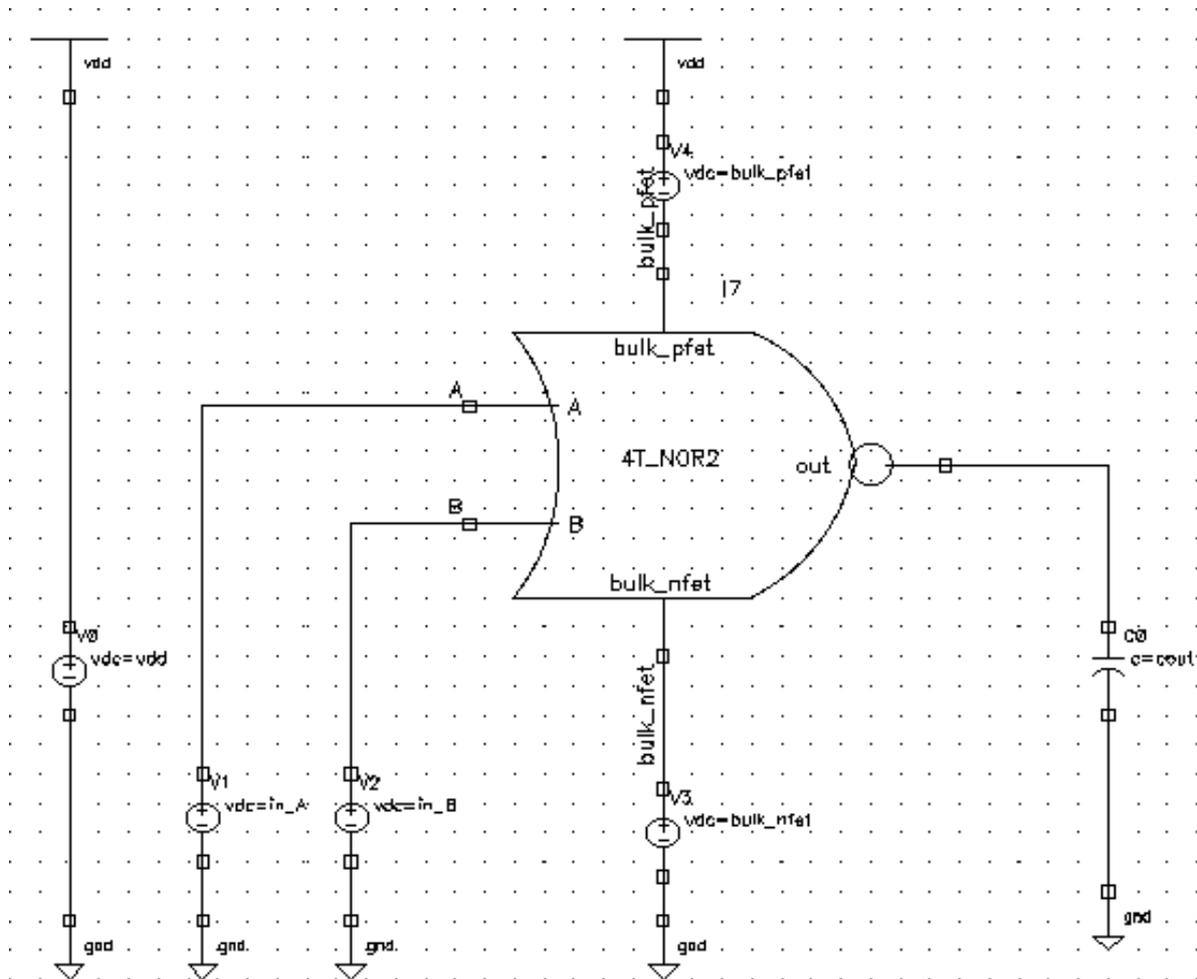


Figure A.21: 4 Transistor NOR2 gate test bench

A.22 4 Transistor NOR2 gate ring oscillator

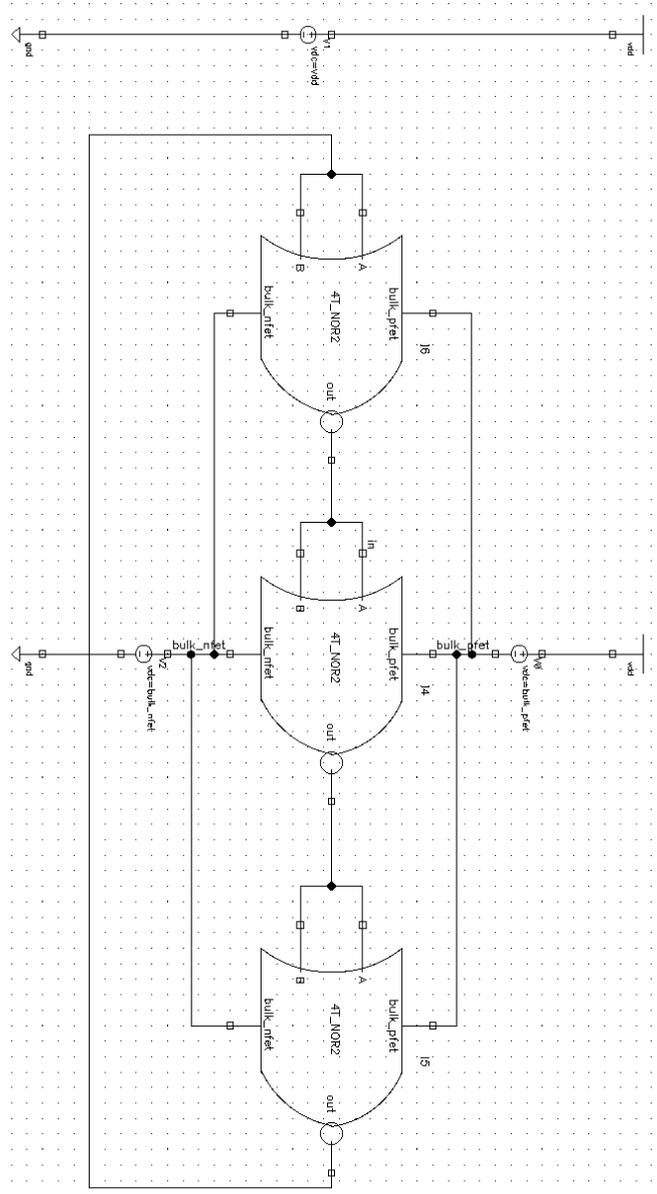


Figure A.22: 4 Transistor NOR2 gater ring oscillator

A.23 8 Transistor NOR2 gate schematic

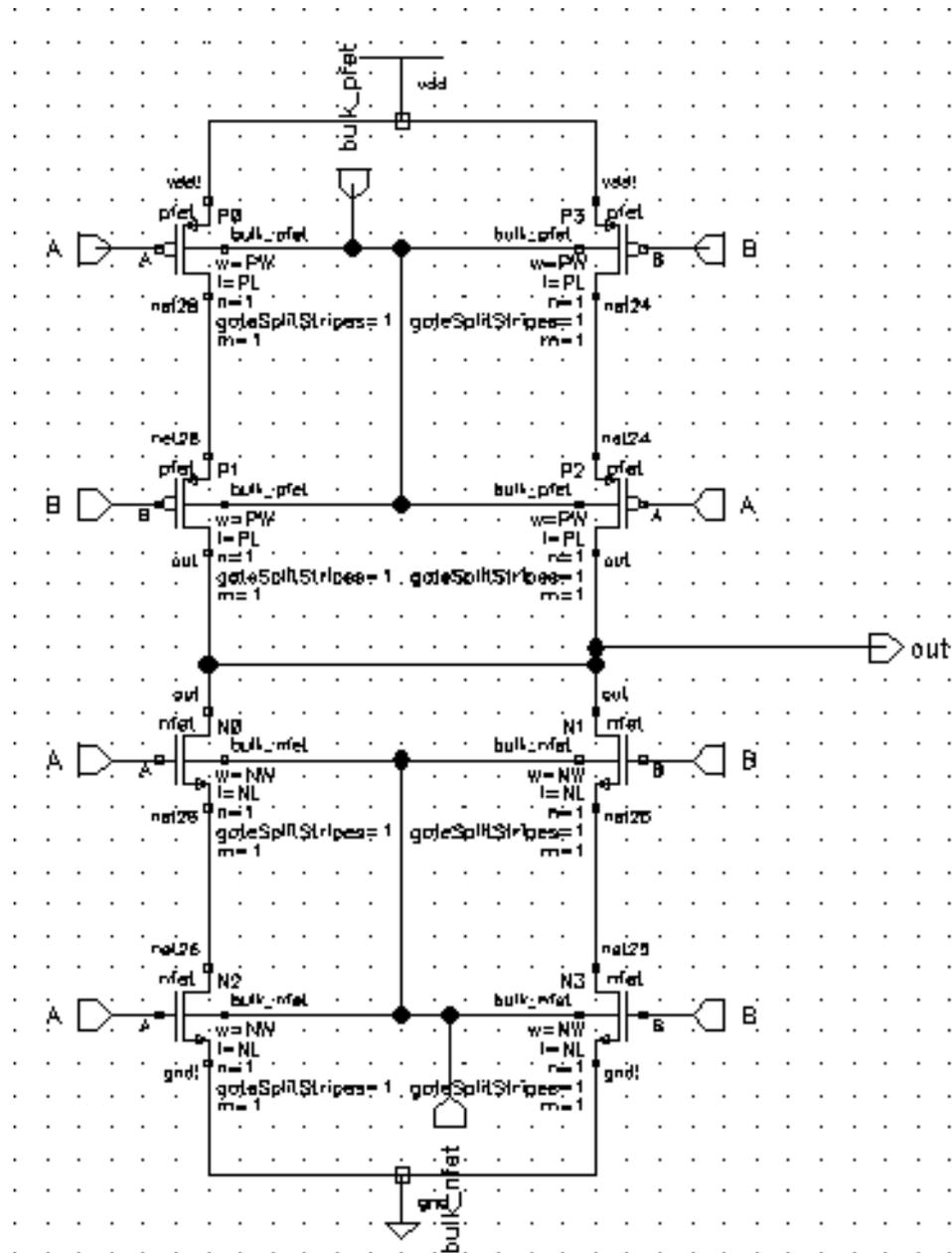


Figure A.23: 8 Transistor NOR2 gate schematic

A.24 8 Transistor NOR2 gate symbol

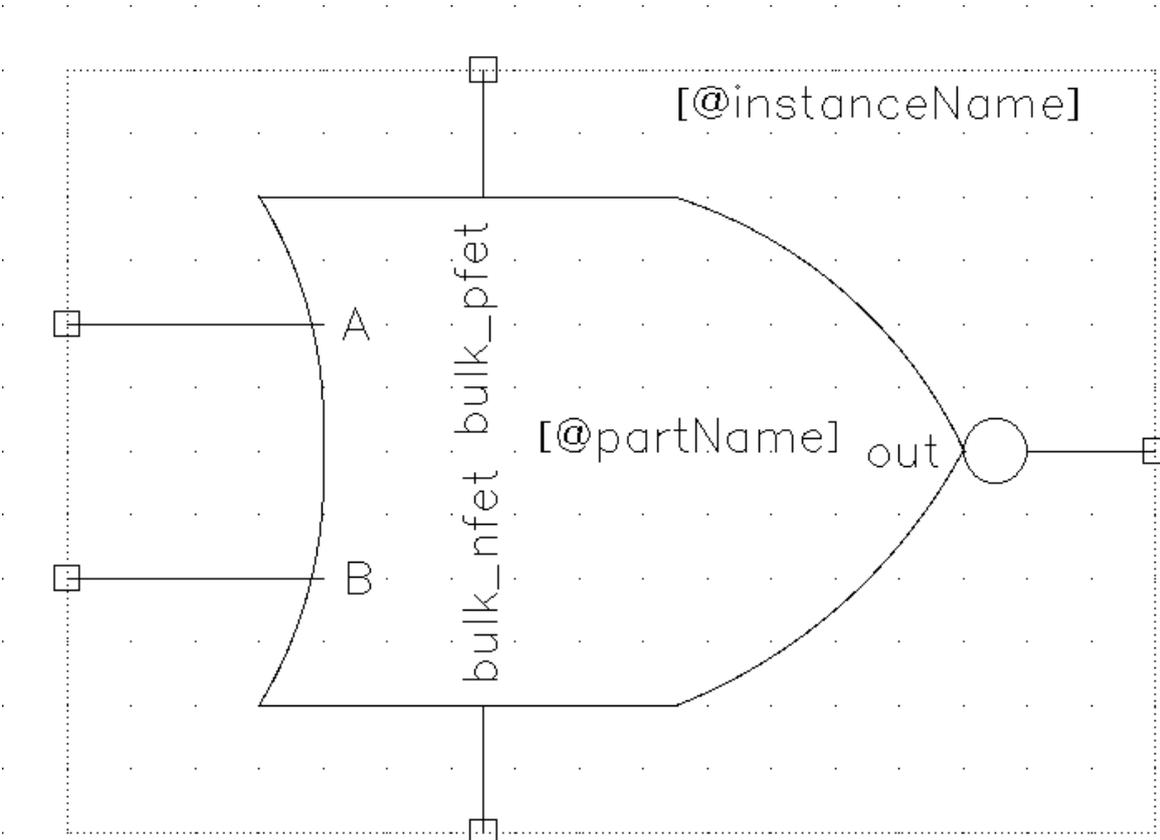


Figure A.24: 8 Transistor NOR2 gate symbol

A.25 8 Transistor NOR2 gate test bench

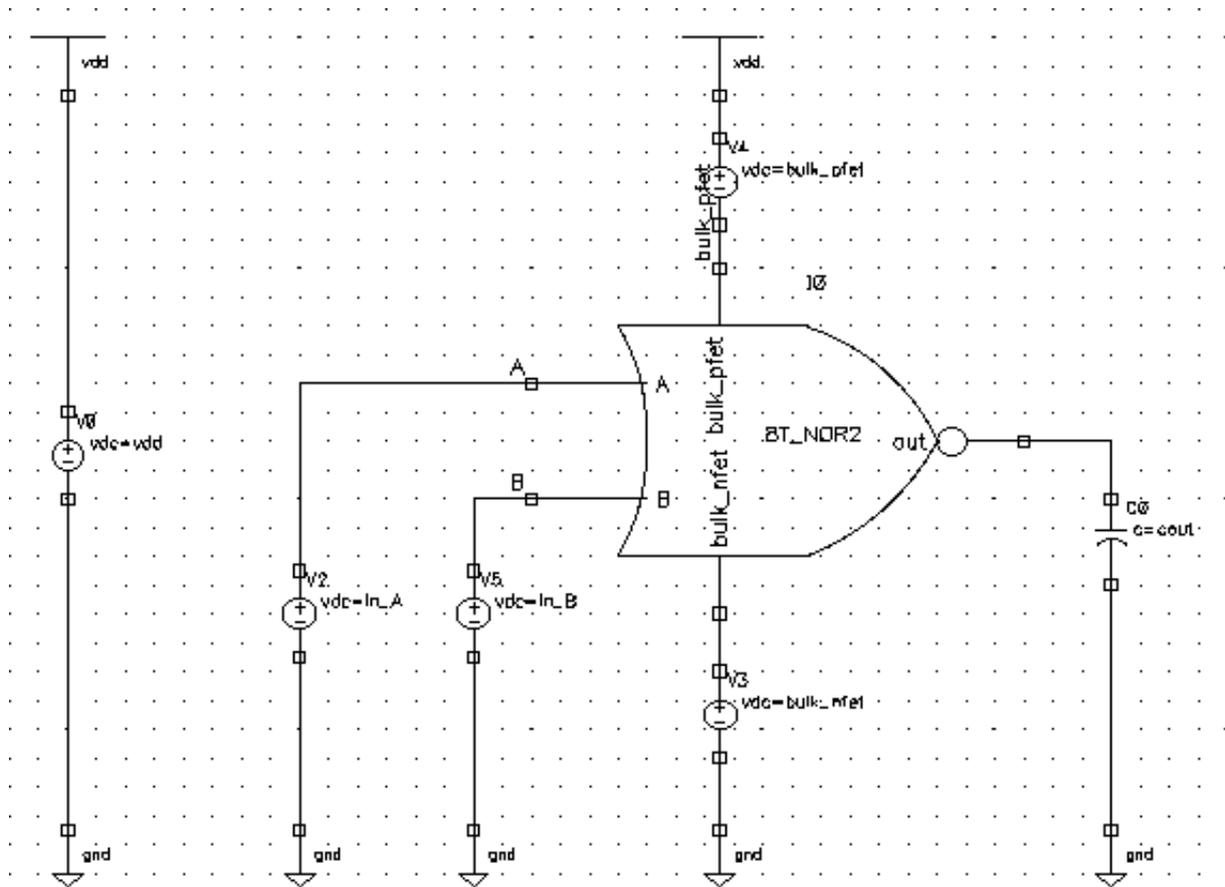


Figure A.25: 8 Transistor NOR2 gate test bench

A.26 8 Transistor NOR2 gate ring oscillator

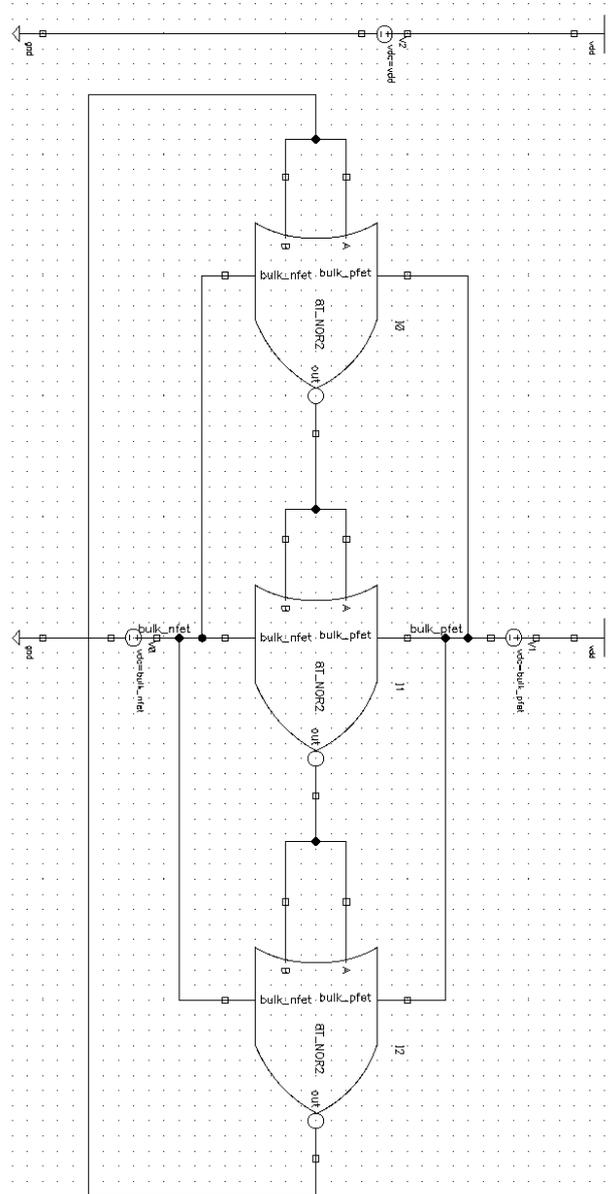


Figure A.26: 8TransistorNOR2 gater ring oscillator

B. Tables

B.1 Gate balance

Table B.1: The SP_x of the 2T Inverter at 100mV. Results from the parametric DC analysis.

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100 | 145 | 30.0 | 200 | 650 | 25.5 | 3.25 | 41.0 |
| 100 | 160 | 30.0 | 200 | 700 | 27.0 | 3.50 | 42.9 |
| 100 | 175 | 30.0 | 200 | 750 | 28.5 | 3.75 | 44.6 |
| 100 | 190 | 30.0 | 200 | 800 | 30.0 | 4.00 | 46.2 |
| 100 | 205 | 30.0 | 200 | 850 | 31.5 | 4.25 | 47.7 |
| 100 | 220 | 30.0 | 200 | 900 | 33.0 | 4.50 | 49.1 |
| 100 | 235 | 30.0 | 200 | 950 | 34.5 | 4.75 | 50.3 |
| 100 | 236 | 35.0 | 200 | 950 | 40.3 | 4.75 | 40.2 |
| 100 | 250 | 30.0 | 200 | 1000 | 36.0 | 5.00 | 51.5 |
| 100 | 251 | 35.0 | 200 | 1000 | 42.0 | 5.00 | 41.2 |
| 100 | 265 | 30.0 | 200 | 1050 | 37.5 | 5.25 | 52.7 |
| 100 | 266 | 35.0 | 200 | 1050 | 43.8 | 5.25 | 42.2 |
| 100 | 280 | 30.0 | 200 | 1100 | 39.0 | 5.50 | 53.7 |
| 100 | 281 | 35.0 | 200 | 1100 | 45.5 | 5.50 | 43.2 |
| 100 | 295 | 30.0 | 200 | 1150 | 40.5 | 5.75 | 54.7 |
| 100 | 296 | 35.0 | 200 | 1150 | 47.3 | 5.75 | 44.1 |
| 100 | 310 | 30.0 | 200 | 1200 | 42.0 | 6.00 | 55.7 |
| 100 | 311 | 35.0 | 200 | 1200 | 49.0 | 6.00 | 44.9 |
| 100 | 325 | 30.0 | 200 | 1250 | 43.5 | 6.25 | 56.6 |
| 100 | 326 | 35.0 | 200 | 1250 | 50.8 | 6.25 | 45.7 |
| 100 | 340 | 30.0 | 200 | 1300 | 45.0 | 6.50 | 57.5 |
| 100 | 341 | 35.0 | 200 | 1300 | 52.5 | 6.50 | 46.5 |
| 100 | 355 | 30.0 | 200 | 1350 | 46.5 | 6.75 | 58.3 |
| 100 | 356 | 35.0 | 200 | 1350 | 54.3 | 6.75 | 47.3 |
| 100 | 357 | 40.0 | 200 | 1350 | 62.0 | 6.75 | 40.4 |
| 100 | 370 | 30.0 | 200 | 1400 | 48.0 | 7.00 | 59.1 |
| 100 | 371 | 35.0 | 200 | 1400 | 56.0 | 7.00 | 48.0 |
| 100 | 372 | 40.0 | 200 | 1400 | 64.0 | 7.00 | 41.1 |
| 100 | 385 | 30.0 | 200 | 1450 | 49.5 | 7.25 | 59.9 |
| 100 | 386 | 35.0 | 200 | 1450 | 57.8 | 7.25 | 48.7 |
| 100 | 387 | 40.0 | 200 | 1450 | 66.0 | 7.25 | 41.8 |
| 100 | 401 | 35.0 | 200 | 1500 | 59.5 | 7.50 | 49.3 |
| 100 | 402 | 40.0 | 200 | 1500 | 68.0 | 7.50 | 42.4 |

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Table B.1 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100 | 416 | 35.0 | 200 | 1550 | 61.3 | 7.75 | 50.0 |
| 100 | 417 | 40.0 | 200 | 1550 | 70.0 | 7.75 | 43.0 |
| 100 | 431 | 35.0 | 200 | 1600 | 63.0 | 8.00 | 50.6 |
| 100 | 432 | 40.0 | 200 | 1600 | 72.0 | 8.00 | 43.6 |
| 100 | 446 | 35.0 | 200 | 1650 | 64.8 | 8.25 | 51.2 |
| 100 | 447 | 40.0 | 200 | 1650 | 74.0 | 8.25 | 44.1 |
| 100 | 461 | 35.0 | 200 | 1700 | 66.5 | 8.50 | 51.8 |
| 100 | 462 | 40.0 | 200 | 1700 | 76.0 | 8.50 | 44.7 |
| 100 | 476 | 35.0 | 200 | 1750 | 68.3 | 8.75 | 52.3 |
| 100 | 477 | 40.0 | 200 | 1750 | 78.0 | 8.75 | 45.2 |
| 100 | 491 | 35.0 | 200 | 1800 | 70.0 | 9.00 | 52.9 |
| 100 | 492 | 40.0 | 200 | 1800 | 80.0 | 9.00 | 45.7 |
| 100 | 506 | 35.0 | 200 | 1850 | 71.8 | 9.25 | 53.4 |
| 100 | 507 | 40.0 | 200 | 1850 | 82.0 | 9.25 | 46.2 |
| 100 | 521 | 35.0 | 200 | 1900 | 73.5 | 9.50 | 53.9 |
| 100 | 522 | 40.0 | 200 | 1900 | 84.0 | 9.50 | 46.7 |
| 100 | 536 | 35.0 | 200 | 1950 | 75.3 | 9.75 | 54.4 |
| 100 | 537 | 40.0 | 200 | 1950 | 86.0 | 9.75 | 47.1 |
| 100 | 551 | 35.0 | 200 | 2000 | 77.0 | 10.00 | 54.9 |
| 100 | 552 | 40.0 | 200 | 2000 | 88.0 | 10.00 | 47.6 |
| 100 | 566 | 35.0 | 200 | 2050 | 78.8 | 10.25 | 55.3 |
| 100 | 567 | 40.0 | 200 | 2050 | 90.0 | 10.25 | 48.0 |
| 100 | 581 | 35.0 | 200 | 2100 | 80.5 | 10.50 | 55.8 |
| 100 | 582 | 40.0 | 200 | 2100 | 92.0 | 10.50 | 48.4 |
| 100 | 596 | 35.0 | 200 | 2150 | 82.3 | 10.75 | 56.2 |
| 100 | 597 | 40.0 | 200 | 2150 | 94.0 | 10.75 | 48.9 |
| 100 | 611 | 35.0 | 200 | 2200 | 84.0 | 11.00 | 56.7 |
| 100 | 612 | 40.0 | 200 | 2200 | 96.0 | 11.00 | 49.3 |
| 100 | 626 | 35.0 | 200 | 2250 | 85.8 | 11.25 | 57.1 |
| 100 | 627 | 40.0 | 200 | 2250 | 98.0 | 11.25 | 49.7 |
| 100 | 641 | 35.0 | 200 | 2300 | 87.5 | 11.50 | 57.5 |
| 100 | 642 | 40.0 | 200 | 2300 | 100.0 | 11.50 | 50.1 |
| 100 | 656 | 35.0 | 200 | 2350 | 89.3 | 11.75 | 57.9 |
| 100 | 657 | 40.0 | 200 | 2350 | 102.0 | 11.75 | 50.4 |
| 100 | 671 | 35.0 | 200 | 2400 | 91.0 | 12.00 | 58.3 |
| 100 | 672 | 40.0 | 200 | 2400 | 104.0 | 12.00 | 50.8 |
| 100 | 686 | 35.0 | 200 | 2450 | 92.8 | 12.25 | 58.7 |
| 100 | 687 | 40.0 | 200 | 2450 | 106.0 | 12.25 | 51.2 |
| 100 | 701 | 35.0 | 200 | 2500 | 94.5 | 12.50 | 59.1 |
| 100 | 702 | 40.0 | 200 | 2500 | 108.0 | 12.50 | 51.5 |
| 100 | 880 | 30.0 | 250 | 750 | 30.0 | 3.00 | 40.3 |
| 100 | 895 | 30.0 | 250 | 800 | 31.5 | 3.20 | 41.8 |
| 100 | 910 | 30.0 | 250 | 850 | 33.0 | 3.40 | 43.3 |
| 100 | 925 | 30.0 | 250 | 900 | 34.5 | 3.60 | 44.7 |
| 100 | 940 | 30.0 | 250 | 950 | 36.0 | 3.80 | 46.0 |
| 100 | 955 | 30.0 | 250 | 1000 | 37.5 | 4.00 | 47.2 |

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Table B.1 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100 | 970 | 30.0 | 250 | 1050 | 39.0 | 4.20 | 48.3 |
| 100 | 985 | 30.0 | 250 | 1100 | 40.5 | 4.40 | 49.3 |
| 100 | 1000 | 30.0 | 250 | 1150 | 42.0 | 4.60 | 50.4 |
| 100 | 1015 | 30.0 | 250 | 1200 | 43.5 | 4.80 | 51.3 |
| 100 | 1016 | 35.0 | 250 | 1200 | 50.8 | 4.80 | 40.8 |
| 100 | 1030 | 30.0 | 250 | 1250 | 45.0 | 5.00 | 52.2 |
| 100 | 1031 | 35.0 | 250 | 1250 | 52.5 | 5.00 | 41.6 |
| 100 | 1045 | 30.0 | 250 | 1300 | 46.5 | 5.20 | 53.1 |
| 100 | 1046 | 35.0 | 250 | 1300 | 54.3 | 5.20 | 42.4 |
| 100 | 1060 | 30.0 | 250 | 1350 | 48.0 | 5.40 | 53.9 |
| 100 | 1061 | 35.0 | 250 | 1350 | 56.0 | 5.40 | 43.1 |
| 100 | 1075 | 30.0 | 250 | 1400 | 49.5 | 5.60 | 54.8 |
| 100 | 1076 | 35.0 | 250 | 1400 | 57.8 | 5.60 | 43.9 |
| 100 | 1090 | 30.0 | 250 | 1450 | 51.0 | 5.80 | 55.5 |
| 100 | 1091 | 35.0 | 250 | 1450 | 59.5 | 5.80 | 44.5 |
| 100 | 1105 | 30.0 | 250 | 1500 | 52.5 | 6.00 | 56.3 |
| 100 | 1106 | 35.0 | 250 | 1500 | 61.3 | 6.00 | 45.2 |
| 100 | 1120 | 30.0 | 250 | 1550 | 54.0 | 6.20 | 57.0 |
| 100 | 1121 | 35.0 | 250 | 1550 | 63.0 | 6.20 | 45.8 |
| 100 | 1135 | 30.0 | 250 | 1600 | 55.5 | 6.40 | 57.7 |
| 100 | 1136 | 35.0 | 250 | 1600 | 64.8 | 6.40 | 46.5 |
| 100 | 1150 | 30.0 | 250 | 1650 | 57.0 | 6.60 | 58.3 |
| 100 | 1151 | 35.0 | 250 | 1650 | 66.5 | 6.60 | 47.1 |
| 100 | 1152 | 40.0 | 250 | 1650 | 76.0 | 6.60 | 40.1 |
| 100 | 1165 | 30.0 | 250 | 1700 | 58.5 | 6.80 | 59.0 |
| 100 | 1166 | 35.0 | 250 | 1700 | 68.3 | 6.80 | 47.6 |
| 100 | 1167 | 40.0 | 250 | 1700 | 78.0 | 6.80 | 40.7 |
| 100 | 1180 | 30.0 | 250 | 1750 | 60.0 | 7.00 | 59.6 |
| 100 | 1181 | 35.0 | 250 | 1750 | 70.0 | 7.00 | 48.2 |
| 100 | 1182 | 40.0 | 250 | 1750 | 80.0 | 7.00 | 41.2 |
| 100 | 1196 | 35.0 | 250 | 1800 | 71.8 | 7.20 | 48.7 |
| 100 | 1197 | 40.0 | 250 | 1800 | 82.0 | 7.20 | 41.7 |
| 100 | 1211 | 35.0 | 250 | 1850 | 73.5 | 7.40 | 49.3 |
| 100 | 1212 | 40.0 | 250 | 1850 | 84.0 | 7.40 | 42.2 |
| 100 | 1226 | 35.0 | 250 | 1900 | 75.3 | 7.60 | 49.8 |
| 100 | 1227 | 40.0 | 250 | 1900 | 86.0 | 7.60 | 42.7 |
| 100 | 1241 | 35.0 | 250 | 1950 | 77.0 | 7.80 | 50.3 |
| 100 | 1242 | 40.0 | 250 | 1950 | 88.0 | 7.80 | 43.2 |
| 100 | 1256 | 35.0 | 250 | 2000 | 78.8 | 8.00 | 50.8 |
| 100 | 1257 | 40.0 | 250 | 2000 | 90.0 | 8.00 | 43.6 |
| 100 | 1271 | 35.0 | 250 | 2050 | 80.5 | 8.20 | 51.2 |
| 100 | 1272 | 40.0 | 250 | 2050 | 92.0 | 8.20 | 44.0 |
| 100 | 1286 | 35.0 | 250 | 2100 | 82.3 | 8.40 | 51.7 |
| 100 | 1287 | 40.0 | 250 | 2100 | 94.0 | 8.40 | 44.5 |
| 100 | 1301 | 35.0 | 250 | 2150 | 84.0 | 8.60 | 52.1 |
| 100 | 1302 | 40.0 | 250 | 2150 | 96.0 | 8.60 | 44.9 |

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Table B.1 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100 | 1316 | 35.0 | 250 | 2200 | 85.8 | 8.80 | 52.6 |
| 100 | 1317 | 40.0 | 250 | 2200 | 98.0 | 8.80 | 45.3 |
| 100 | 1331 | 35.0 | 250 | 2250 | 87.5 | 9.00 | 53.0 |
| 100 | 1332 | 40.0 | 250 | 2250 | 100.0 | 9.00 | 45.7 |
| 100 | 1346 | 35.0 | 250 | 2300 | 89.3 | 9.20 | 53.4 |
| 100 | 1347 | 40.0 | 250 | 2300 | 102.0 | 9.20 | 46.1 |
| 100 | 1361 | 35.0 | 250 | 2350 | 91.0 | 9.40 | 53.8 |
| 100 | 1362 | 40.0 | 250 | 2350 | 104.0 | 9.40 | 46.5 |
| 100 | 1376 | 35.0 | 250 | 2400 | 92.8 | 9.60 | 54.2 |
| 100 | 1377 | 40.0 | 250 | 2400 | 106.0 | 9.60 | 46.8 |
| 100 | 1391 | 35.0 | 250 | 2450 | 94.5 | 9.80 | 54.6 |
| 100 | 1392 | 40.0 | 250 | 2450 | 108.0 | 9.80 | 47.2 |
| 100 | 1406 | 35.0 | 250 | 2500 | 96.3 | 10.00 | 55.0 |
| 100 | 1407 | 40.0 | 250 | 2500 | 110.0 | 10.00 | 47.6 |
| 100 | 1630 | 30.0 | 300 | 900 | 36.0 | 3.00 | 41.1 |
| 100 | 1645 | 30.0 | 300 | 950 | 37.5 | 3.17 | 42.4 |
| 100 | 1660 | 30.0 | 300 | 1000 | 39.0 | 3.33 | 43.6 |
| 100 | 1675 | 30.0 | 300 | 1050 | 40.5 | 3.50 | 44.7 |
| 100 | 1690 | 30.0 | 300 | 1100 | 42.0 | 3.67 | 45.8 |
| 100 | 1705 | 30.0 | 300 | 1150 | 43.5 | 3.83 | 46.8 |
| 100 | 1720 | 30.0 | 300 | 1200 | 45.0 | 4.00 | 47.8 |
| 100 | 1735 | 30.0 | 300 | 1250 | 46.5 | 4.17 | 48.7 |
| 100 | 1750 | 30.0 | 300 | 1300 | 48.0 | 4.33 | 49.6 |
| 100 | 1765 | 30.0 | 300 | 1350 | 49.5 | 4.50 | 50.4 |
| 100 | 1780 | 30.0 | 300 | 1400 | 51.0 | 4.67 | 51.2 |
| 100 | 1781 | 35.0 | 300 | 1400 | 59.5 | 4.67 | 40.5 |
| 100 | 1795 | 30.0 | 300 | 1450 | 52.5 | 4.83 | 52.0 |
| 100 | 1796 | 35.0 | 300 | 1450 | 61.3 | 4.83 | 41.2 |
| 100 | 1810 | 30.0 | 300 | 1500 | 54.0 | 5.00 | 52.7 |
| 100 | 1811 | 35.0 | 300 | 1500 | 63.0 | 5.00 | 41.9 |
| 100 | 1825 | 30.0 | 300 | 1550 | 55.5 | 5.17 | 53.4 |
| 100 | 1826 | 35.0 | 300 | 1550 | 64.8 | 5.17 | 42.5 |
| 100 | 1840 | 30.0 | 300 | 1600 | 57.0 | 5.33 | 54.1 |
| 100 | 1841 | 35.0 | 300 | 1600 | 66.5 | 5.33 | 43.1 |
| 100 | 1855 | 30.0 | 300 | 1650 | 58.5 | 5.50 | 54.8 |
| 100 | 1856 | 35.0 | 300 | 1650 | 68.3 | 5.50 | 43.7 |
| 100 | 1870 | 30.0 | 300 | 1700 | 60.0 | 5.67 | 55.4 |
| 100 | 1871 | 35.0 | 300 | 1700 | 70.0 | 5.67 | 44.3 |
| 100 | 1885 | 30.0 | 300 | 1750 | 61.5 | 5.83 | 56.0 |
| 100 | 1886 | 35.0 | 300 | 1750 | 71.8 | 5.83 | 44.9 |
| 100 | 1900 | 30.0 | 300 | 1800 | 63.0 | 6.00 | 56.6 |
| 100 | 1901 | 35.0 | 300 | 1800 | 73.5 | 6.00 | 45.4 |
| 100 | 1915 | 30.0 | 300 | 1850 | 64.5 | 6.17 | 57.2 |
| 100 | 1916 | 35.0 | 300 | 1850 | 75.3 | 6.17 | 45.9 |
| 100 | 1930 | 30.0 | 300 | 1900 | 66.0 | 6.33 | 57.8 |
| 100 | 1931 | 35.0 | 300 | 1900 | 77.0 | 6.33 | 46.4 |

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Table B.1 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100 | 1945 | 30.0 | 300 | 1950 | 67.5 | 6.50 | 58.3 |
| 100 | 1946 | 35.0 | 300 | 1950 | 78.8 | 6.50 | 46.9 |
| 100 | 1960 | 30.0 | 300 | 2000 | 69.0 | 6.67 | 58.9 |
| 100 | 1961 | 35.0 | 300 | 2000 | 80.5 | 6.67 | 47.4 |
| 100 | 1962 | 40.0 | 300 | 2000 | 92.0 | 6.67 | 40.4 |
| 100 | 1975 | 30.0 | 300 | 2050 | 70.5 | 6.83 | 59.4 |
| 100 | 1976 | 35.0 | 300 | 2050 | 82.3 | 6.83 | 47.9 |
| 100 | 1977 | 40.0 | 300 | 2050 | 94.0 | 6.83 | 40.8 |
| 100 | 1990 | 30.0 | 300 | 2100 | 72.0 | 7.00 | 59.9 |
| 100 | 1991 | 35.0 | 300 | 2100 | 84.0 | 7.00 | 48.3 |
| 100 | 1992 | 40.0 | 300 | 2100 | 96.0 | 7.00 | 41.3 |
| 100 | 2006 | 35.0 | 300 | 2150 | 85.8 | 7.17 | 48.8 |
| 100 | 2007 | 40.0 | 300 | 2150 | 98.0 | 7.17 | 41.7 |
| 100 | 2021 | 35.0 | 300 | 2200 | 87.5 | 7.33 | 49.2 |
| 100 | 2022 | 40.0 | 300 | 2200 | 100.0 | 7.33 | 42.1 |
| 100 | 2036 | 35.0 | 300 | 2250 | 89.3 | 7.50 | 49.6 |
| 100 | 2037 | 40.0 | 300 | 2250 | 102.0 | 7.50 | 42.5 |
| 100 | 2051 | 35.0 | 300 | 2300 | 91.0 | 7.67 | 50.1 |
| 100 | 2052 | 40.0 | 300 | 2300 | 104.0 | 7.67 | 42.9 |
| 100 | 2066 | 35.0 | 300 | 2350 | 92.8 | 7.83 | 50.5 |
| 100 | 2067 | 40.0 | 300 | 2350 | 106.0 | 7.83 | 43.3 |
| 100 | 2081 | 35.0 | 300 | 2400 | 94.5 | 8.00 | 50.9 |
| 100 | 2082 | 40.0 | 300 | 2400 | 108.0 | 8.00 | 43.6 |
| 100 | 2096 | 35.0 | 300 | 2450 | 96.3 | 8.17 | 51.2 |
| 100 | 2097 | 40.0 | 300 | 2450 | 110.0 | 8.17 | 44.0 |
| 100 | 2111 | 35.0 | 300 | 2500 | 98.0 | 8.33 | 51.6 |
| 100 | 2112 | 40.0 | 300 | 2500 | 112.0 | 8.33 | 44.4 |
| 100 | 2365 | 30.0 | 350 | 1000 | 40.5 | 2.86 | 40.6 |
| 100 | 2380 | 30.0 | 350 | 1050 | 42.0 | 3.00 | 41.7 |

Table B.2: The SP_x of the 4T Inverter at 100mV. Results from the parametric DC analysis.

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|----------------|
| 100.0 | 145 | 30.0 | 200 | 650 | 25.5 | 3.25 | 40.8 |
| 100.0 | 160 | 30.0 | 200 | 700 | 27.0 | 3.50 | 42.7 |
| 100.0 | 175 | 30.0 | 200 | 750 | 28.5 | 3.75 | 44.4 |
| 100.0 | 190 | 30.0 | 200 | 800 | 30.0 | 4.00 | 46.0 |
| 100.0 | 205 | 30.0 | 200 | 850 | 31.5 | 4.25 | 47.4 |
| 100.0 | 220 | 30.0 | 200 | 900 | 33.0 | 4.50 | 48.8 |
| 100.0 | 235 | 30.0 | 200 | 950 | 34.5 | 4.75 | 50.1 |
| 100.0 | 250 | 30.0 | 200 | 1000 | 36.0 | 5.00 | 51.3 |
| 100.0 | 251 | 35.0 | 200 | 1000 | 42.0 | 5.00 | 40.9 |
| 100.0 | 265 | 30.0 | 200 | 1050 | 37.5 | 5.25 | 52.4 |
| 100.0 | 266 | 35.0 | 200 | 1050 | 43.8 | 5.25 | 41.9 |
| 100.0 | 280 | 30.0 | 200 | 1100 | 39.0 | 5.50 | 53.5 |
| 100.0 | 281 | 35.0 | 200 | 1100 | 45.5 | 5.50 | 42.8 |
| 100.0 | 295 | 30.0 | 200 | 1150 | 40.5 | 5.75 | 54.5 |
| 100.0 | 296 | 35.0 | 200 | 1150 | 47.3 | 5.75 | 43.7 |
| 100.0 | 310 | 30.0 | 200 | 1200 | 42.0 | 6.00 | 55.4 |
| 100.0 | 311 | 35.0 | 200 | 1200 | 49.0 | 6.00 | 44.6 |
| 100.0 | 325 | 30.0 | 200 | 1250 | 43.5 | 6.25 | 56.4 |
| 100.0 | 326 | 35.0 | 200 | 1250 | 50.8 | 6.25 | 45.4 |
| 100.0 | 340 | 30.0 | 200 | 1300 | 45.0 | 6.50 | 57.2 |
| 100.0 | 341 | 35.0 | 200 | 1300 | 52.5 | 6.50 | 46.2 |
| 100.0 | 355 | 30.0 | 200 | 1350 | 46.5 | 6.75 | 58.1 |
| 100.0 | 356 | 35.0 | 200 | 1350 | 54.3 | 6.75 | 46.9 |
| 100.0 | 357 | 40.0 | 200 | 1350 | 62.0 | 6.75 | 40.1 |
| 100.0 | 370 | 30.0 | 200 | 1400 | 48.0 | 7.00 | 58.9 |
| 100.0 | 371 | 35.0 | 200 | 1400 | 56.0 | 7.00 | 47.6 |
| 100.0 | 372 | 40.0 | 200 | 1400 | 64.0 | 7.00 | 40.8 |
| 100.0 | 385 | 30.0 | 200 | 1450 | 49.5 | 7.25 | 59.6 |
| 100.0 | 386 | 35.0 | 200 | 1450 | 57.8 | 7.25 | 48.3 |
| 100.0 | 387 | 40.0 | 200 | 1450 | 66.0 | 7.25 | 41.4 |
| 100.0 | 401 | 35.0 | 200 | 1500 | 59.5 | 7.50 | 49.0 |
| 100.0 | 402 | 40.0 | 200 | 1500 | 68.0 | 7.50 | 42.0 |
| 100.0 | 416 | 35.0 | 200 | 1550 | 61.3 | 7.75 | 49.6 |
| 100.0 | 417 | 40.0 | 200 | 1550 | 70.0 | 7.75 | 42.6 |
| 100.0 | 431 | 35.0 | 200 | 1600 | 63.0 | 8.00 | 50.2 |
| 100.0 | 432 | 40.0 | 200 | 1600 | 72.0 | 8.00 | 43.2 |
| 100.0 | 446 | 35.0 | 200 | 1650 | 64.8 | 8.25 | 50.8 |
| 100.0 | 447 | 40.0 | 200 | 1650 | 74.0 | 8.25 | 43.8 |
| 100.0 | 461 | 35.0 | 200 | 1700 | 66.5 | 8.50 | 51.4 |
| 100.0 | 462 | 40.0 | 200 | 1700 | 76.0 | 8.50 | 44.3 |
| 100.0 | 476 | 35.0 | 200 | 1750 | 68.3 | 8.75 | 52.0 |
| 100.0 | 477 | 40.0 | 200 | 1750 | 78.0 | 8.75 | 44.8 |
| 100.0 | 491 | 35.0 | 200 | 1800 | 70.0 | 9.00 | 52.5 |
| 100.0 | 492 | 40.0 | 200 | 1800 | 80.0 | 9.00 | 45.3 |
| 100.0 | 506 | 35.0 | 200 | 1850 | 71.8 | 9.25 | 53.0 |

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Table B.2 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100.0 | 507 | 40.0 | 200 | 1850 | 82.0 | 9.25 | 45.8 |
| 100.0 | 521 | 35.0 | 200 | 1900 | 73.5 | 9.50 | 53.5 |
| 100.0 | 522 | 40.0 | 200 | 1900 | 84.0 | 9.50 | 46.3 |
| 100.0 | 536 | 35.0 | 200 | 1950 | 75.3 | 9.75 | 54.0 |
| 100.0 | 537 | 40.0 | 200 | 1950 | 86.0 | 9.75 | 46.8 |
| 100.0 | 551 | 35.0 | 200 | 2000 | 77.0 | 10.00 | 54.5 |
| 100.0 | 552 | 40.0 | 200 | 2000 | 88.0 | 10.00 | 47.2 |
| 100.0 | 566 | 35.0 | 200 | 2050 | 78.8 | 10.25 | 55.0 |
| 100.0 | 567 | 40.0 | 200 | 2050 | 90.0 | 10.25 | 47.7 |
| 100.0 | 581 | 35.0 | 200 | 2100 | 80.5 | 10.50 | 55.4 |
| 100.0 | 582 | 40.0 | 200 | 2100 | 92.0 | 10.50 | 48.1 |
| 100.0 | 596 | 35.0 | 200 | 2150 | 82.3 | 10.75 | 55.9 |
| 100.0 | 597 | 40.0 | 200 | 2150 | 94.0 | 10.75 | 48.5 |
| 100.0 | 611 | 35.0 | 200 | 2200 | 84.0 | 11.00 | 56.3 |
| 100.0 | 612 | 40.0 | 200 | 2200 | 96.0 | 11.00 | 48.9 |
| 100.0 | 626 | 35.0 | 200 | 2250 | 85.8 | 11.25 | 56.8 |
| 100.0 | 627 | 40.0 | 200 | 2250 | 98.0 | 11.25 | 49.3 |
| 100.0 | 641 | 35.0 | 200 | 2300 | 87.5 | 11.50 | 57.2 |
| 100.0 | 642 | 40.0 | 200 | 2300 | 100.0 | 11.50 | 49.7 |
| 100.0 | 656 | 35.0 | 200 | 2350 | 89.3 | 11.75 | 57.6 |
| 100.0 | 657 | 40.0 | 200 | 2350 | 102.0 | 11.75 | 50.1 |
| 100.0 | 671 | 35.0 | 200 | 2400 | 91.0 | 12.00 | 58.0 |
| 100.0 | 672 | 40.0 | 200 | 2400 | 104.0 | 12.00 | 50.5 |
| 100.0 | 686 | 35.0 | 200 | 2450 | 92.8 | 12.25 | 58.4 |
| 100.0 | 687 | 40.0 | 200 | 2450 | 106.0 | 12.25 | 50.8 |
| 100.0 | 701 | 35.0 | 200 | 2500 | 94.5 | 12.50 | 58.7 |
| 100.0 | 702 | 40.0 | 200 | 2500 | 108.0 | 12.50 | 51.2 |
| 100.0 | 880 | 30.0 | 250 | 750 | 30.0 | 3.00 | 40.0 |
| 100.0 | 895 | 30.0 | 250 | 800 | 31.5 | 3.20 | 41.6 |
| 100.0 | 910 | 30.0 | 250 | 850 | 33.0 | 3.40 | 43.1 |
| 100.0 | 925 | 30.0 | 250 | 900 | 34.5 | 3.60 | 44.4 |
| 100.0 | 940 | 30.0 | 250 | 950 | 36.0 | 3.80 | 45.7 |
| 100.0 | 955 | 30.0 | 250 | 1000 | 37.5 | 4.00 | 46.9 |
| 100.0 | 970 | 30.0 | 250 | 1050 | 39.0 | 4.20 | 48.0 |
| 100.0 | 985 | 30.0 | 250 | 1100 | 40.5 | 4.40 | 49.1 |
| 100.0 | 1000 | 30.0 | 250 | 1150 | 42.0 | 4.60 | 50.1 |
| 100.0 | 1015 | 30.0 | 250 | 1200 | 43.5 | 4.80 | 51.1 |
| 100.0 | 1016 | 35.0 | 250 | 1200 | 50.8 | 4.80 | 40.5 |
| 100.0 | 1030 | 30.0 | 250 | 1250 | 45.0 | 5.00 | 52.0 |
| 100.0 | 1031 | 35.0 | 250 | 1250 | 52.5 | 5.00 | 41.3 |
| 100.0 | 1045 | 30.0 | 250 | 1300 | 46.5 | 5.20 | 52.9 |
| 100.0 | 1046 | 35.0 | 250 | 1300 | 54.3 | 5.20 | 42.1 |
| 100.0 | 1060 | 30.0 | 250 | 1350 | 48.0 | 5.40 | 53.7 |
| 100.0 | 1061 | 35.0 | 250 | 1350 | 56.0 | 5.40 | 42.8 |
| 100.0 | 1075 | 30.0 | 250 | 1400 | 49.5 | 5.60 | 54.5 |
| 100.0 | 1076 | 35.0 | 250 | 1400 | 57.8 | 5.60 | 43.5 |

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Table B.2 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100.0 | 1090 | 30.0 | 250 | 1450 | 51.0 | 5.80 | 55.3 |
| 100.0 | 1091 | 35.0 | 250 | 1450 | 59.5 | 5.80 | 44.2 |
| 100.0 | 1105 | 30.0 | 250 | 1500 | 52.5 | 6.00 | 56.0 |
| 100.0 | 1106 | 35.0 | 250 | 1500 | 61.3 | 6.00 | 44.9 |
| 100.0 | 1120 | 30.0 | 250 | 1550 | 54.0 | 6.20 | 56.7 |
| 100.0 | 1121 | 35.0 | 250 | 1550 | 63.0 | 6.20 | 45.5 |
| 100.0 | 1135 | 30.0 | 250 | 1600 | 55.5 | 6.40 | 57.4 |
| 100.0 | 1136 | 35.0 | 250 | 1600 | 64.8 | 6.40 | 46.1 |
| 100.0 | 1150 | 30.0 | 250 | 1650 | 57.0 | 6.60 | 58.1 |
| 100.0 | 1151 | 35.0 | 250 | 1650 | 66.5 | 6.60 | 46.7 |
| 100.0 | 1165 | 30.0 | 250 | 1700 | 58.5 | 6.80 | 58.7 |
| 100.0 | 1166 | 35.0 | 250 | 1700 | 68.3 | 6.80 | 47.3 |
| 100.0 | 1167 | 40.0 | 250 | 1700 | 78.0 | 6.80 | 40.3 |
| 100.0 | 1180 | 30.0 | 250 | 1750 | 60.0 | 7.00 | 59.3 |
| 100.0 | 1181 | 35.0 | 250 | 1750 | 70.0 | 7.00 | 47.9 |
| 100.0 | 1182 | 40.0 | 250 | 1750 | 80.0 | 7.00 | 40.9 |
| 100.0 | 1195 | 30.0 | 250 | 1800 | 61.5 | 7.20 | 59.9 |
| 100.0 | 1196 | 35.0 | 250 | 1800 | 71.8 | 7.20 | 48.4 |
| 100.0 | 1197 | 40.0 | 250 | 1800 | 82.0 | 7.20 | 41.4 |
| 100.0 | 1211 | 35.0 | 250 | 1850 | 73.5 | 7.40 | 48.9 |
| 100.0 | 1212 | 40.0 | 250 | 1850 | 84.0 | 7.40 | 41.8 |
| 100.0 | 1226 | 35.0 | 250 | 1900 | 75.3 | 7.60 | 49.4 |
| 100.0 | 1227 | 40.0 | 250 | 1900 | 86.0 | 7.60 | 42.3 |
| 100.0 | 1241 | 35.0 | 250 | 1950 | 77.0 | 7.80 | 49.9 |
| 100.0 | 1242 | 40.0 | 250 | 1950 | 88.0 | 7.80 | 42.8 |
| 100.0 | 1256 | 35.0 | 250 | 2000 | 78.8 | 8.00 | 50.4 |
| 100.0 | 1257 | 40.0 | 250 | 2000 | 90.0 | 8.00 | 43.2 |
| 100.0 | 1271 | 35.0 | 250 | 2050 | 80.5 | 8.20 | 50.9 |
| 100.0 | 1272 | 40.0 | 250 | 2050 | 92.0 | 8.20 | 43.7 |
| 100.0 | 1286 | 35.0 | 250 | 2100 | 82.3 | 8.40 | 51.3 |
| 100.0 | 1287 | 40.0 | 250 | 2100 | 94.0 | 8.40 | 44.1 |
| 100.0 | 1301 | 35.0 | 250 | 2150 | 84.0 | 8.60 | 51.8 |
| 100.0 | 1302 | 40.0 | 250 | 2150 | 96.0 | 8.60 | 44.5 |
| 100.0 | 1316 | 35.0 | 250 | 2200 | 85.8 | 8.80 | 52.2 |
| 100.0 | 1317 | 40.0 | 250 | 2200 | 98.0 | 8.80 | 44.9 |
| 100.0 | 1331 | 35.0 | 250 | 2250 | 87.5 | 9.00 | 52.6 |
| 100.0 | 1332 | 40.0 | 250 | 2250 | 100.0 | 9.00 | 45.3 |
| 100.0 | 1346 | 35.0 | 250 | 2300 | 89.3 | 9.20 | 53.1 |
| 100.0 | 1347 | 40.0 | 250 | 2300 | 102.0 | 9.20 | 45.7 |
| 100.0 | 1361 | 35.0 | 250 | 2350 | 91.0 | 9.40 | 53.5 |
| 100.0 | 1362 | 40.0 | 250 | 2350 | 104.0 | 9.40 | 46.1 |
| 100.0 | 1376 | 35.0 | 250 | 2400 | 92.8 | 9.60 | 53.8 |
| 100.0 | 1377 | 40.0 | 250 | 2400 | 106.0 | 9.60 | 46.5 |
| 100.0 | 1391 | 35.0 | 250 | 2450 | 94.5 | 9.80 | 54.2 |
| 100.0 | 1392 | 40.0 | 250 | 2450 | 108.0 | 9.80 | 46.9 |
| 100.0 | 1406 | 35.0 | 250 | 2500 | 96.3 | 10.00 | 54.6 |

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Table B.2 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100.0 | 1407 | 40.0 | 250 | 2500 | 110.0 | 10.00 | 47.2 |
| 100.0 | 1630 | 30.0 | 300 | 900 | 36.0 | 3.00 | 40.9 |
| 100.0 | 1645 | 30.0 | 300 | 950 | 37.5 | 3.17 | 42.2 |
| 100.0 | 1660 | 30.0 | 300 | 1000 | 39.0 | 3.33 | 43.3 |
| 100.0 | 1675 | 30.0 | 300 | 1050 | 40.5 | 3.50 | 44.5 |
| 100.0 | 1690 | 30.0 | 300 | 1100 | 42.0 | 3.67 | 45.5 |
| 100.0 | 1705 | 30.0 | 300 | 1150 | 43.5 | 3.83 | 46.6 |
| 100.0 | 1720 | 30.0 | 300 | 1200 | 45.0 | 4.00 | 47.5 |
| 100.0 | 1735 | 30.0 | 300 | 1250 | 46.5 | 4.17 | 48.4 |
| 100.0 | 1750 | 30.0 | 300 | 1300 | 48.0 | 4.33 | 49.3 |
| 100.0 | 1765 | 30.0 | 300 | 1350 | 49.5 | 4.50 | 50.1 |
| 100.0 | 1780 | 30.0 | 300 | 1400 | 51.0 | 4.67 | 50.9 |
| 100.0 | 1781 | 35.0 | 300 | 1400 | 59.5 | 4.67 | 40.2 |
| 100.0 | 1795 | 30.0 | 300 | 1450 | 52.5 | 4.83 | 51.7 |
| 100.0 | 1796 | 35.0 | 300 | 1450 | 61.3 | 4.83 | 40.9 |
| 100.0 | 1810 | 30.0 | 300 | 1500 | 54.0 | 5.00 | 52.5 |
| 100.0 | 1811 | 35.0 | 300 | 1500 | 63.0 | 5.00 | 41.5 |
| 100.0 | 1825 | 30.0 | 300 | 1550 | 55.5 | 5.17 | 53.2 |
| 100.0 | 1826 | 35.0 | 300 | 1550 | 64.8 | 5.17 | 42.2 |
| 100.0 | 1840 | 30.0 | 300 | 1600 | 57.0 | 5.33 | 53.8 |
| 100.0 | 1841 | 35.0 | 300 | 1600 | 66.5 | 5.33 | 42.8 |
| 100.0 | 1855 | 30.0 | 300 | 1650 | 58.5 | 5.50 | 54.5 |
| 100.0 | 1856 | 35.0 | 300 | 1650 | 68.3 | 5.50 | 43.4 |
| 100.0 | 1870 | 30.0 | 300 | 1700 | 60.0 | 5.67 | 55.1 |
| 100.0 | 1871 | 35.0 | 300 | 1700 | 70.0 | 5.67 | 44.0 |
| 100.0 | 1885 | 30.0 | 300 | 1750 | 61.5 | 5.83 | 55.8 |
| 100.0 | 1886 | 35.0 | 300 | 1750 | 71.8 | 5.83 | 44.5 |
| 100.0 | 1900 | 30.0 | 300 | 1800 | 63.0 | 6.00 | 56.4 |
| 100.0 | 1901 | 35.0 | 300 | 1800 | 73.5 | 6.00 | 45.1 |
| 100.0 | 1915 | 30.0 | 300 | 1850 | 64.5 | 6.17 | 57.0 |
| 100.0 | 1916 | 35.0 | 300 | 1850 | 75.3 | 6.17 | 45.6 |
| 100.0 | 1930 | 30.0 | 300 | 1900 | 66.0 | 6.33 | 57.5 |
| 100.0 | 1931 | 35.0 | 300 | 1900 | 77.0 | 6.33 | 46.1 |
| 100.0 | 1945 | 30.0 | 300 | 1950 | 67.5 | 6.50 | 58.1 |
| 100.0 | 1946 | 35.0 | 300 | 1950 | 78.8 | 6.50 | 46.6 |
| 100.0 | 1960 | 30.0 | 300 | 2000 | 69.0 | 6.67 | 58.6 |
| 100.0 | 1961 | 35.0 | 300 | 2000 | 80.5 | 6.67 | 47.1 |
| 100.0 | 1962 | 40.0 | 300 | 2000 | 92.0 | 6.67 | 40.0 |
| 100.0 | 1975 | 30.0 | 300 | 2050 | 70.5 | 6.83 | 59.1 |
| 100.0 | 1976 | 35.0 | 300 | 2050 | 82.3 | 6.83 | 47.5 |
| 100.0 | 1977 | 40.0 | 300 | 2050 | 94.0 | 6.83 | 40.5 |
| 100.0 | 1990 | 30.0 | 300 | 2100 | 72.0 | 7.00 | 59.6 |
| 100.0 | 1991 | 35.0 | 300 | 2100 | 84.0 | 7.00 | 48.0 |
| 100.0 | 1992 | 40.0 | 300 | 2100 | 96.0 | 7.00 | 40.9 |
| 100.0 | 2006 | 35.0 | 300 | 2150 | 85.8 | 7.17 | 48.4 |
| 100.0 | 2007 | 40.0 | 300 | 2150 | 98.0 | 7.17 | 41.3 |

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Table B.2 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100.0 | 2021 | 35.0 | 300 | 2200 | 87.5 | 7.33 | 48.9 |
| 100.0 | 2022 | 40.0 | 300 | 2200 | 100.0 | 7.33 | 41.7 |
| 100.0 | 2036 | 35.0 | 300 | 2250 | 89.3 | 7.50 | 49.3 |
| 100.0 | 2037 | 40.0 | 300 | 2250 | 102.0 | 7.50 | 42.1 |
| 100.0 | 2051 | 35.0 | 300 | 2300 | 91.0 | 7.67 | 49.7 |
| 100.0 | 2052 | 40.0 | 300 | 2300 | 104.0 | 7.67 | 42.5 |
| 100.0 | 2066 | 35.0 | 300 | 2350 | 92.8 | 7.83 | 50.1 |
| 100.0 | 2067 | 40.0 | 300 | 2350 | 106.0 | 7.83 | 42.9 |
| 100.0 | 2081 | 35.0 | 300 | 2400 | 94.5 | 8.00 | 50.5 |
| 100.0 | 2082 | 40.0 | 300 | 2400 | 108.0 | 8.00 | 43.3 |
| 100.0 | 2096 | 35.0 | 300 | 2450 | 96.3 | 8.17 | 50.9 |
| 100.0 | 2097 | 40.0 | 300 | 2450 | 110.0 | 8.17 | 43.6 |
| 100.0 | 2111 | 35.0 | 300 | 2500 | 98.0 | 8.33 | 51.3 |
| 100.0 | 2112 | 40.0 | 300 | 2500 | 112.0 | 8.33 | 44.0 |
| 100.0 | 2365 | 30.0 | 350 | 1000 | 40.5 | 2.86 | 40.4 |
| 100.0 | 2380 | 30.0 | 350 | 1050 | 42.0 | 3.00 | 41.5 |
| 100.0 | 2395 | 30.0 | 350 | 1100 | 43.5 | 3.14 | 42.6 |

Table B.3: The SP_x of the 4T NAND2 at 100mV. Results from the parametric DC analysis.

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|----------------|
| 100 | 34 | 30.0 | 200 | 500 | 21.0 | 2.50 | 41.1 |
| 100 | 39 | 30.0 | 200 | 550 | 22.5 | 2.75 | 44.3 |
| 100 | 44 | 30.0 | 200 | 600 | 24.0 | 3.00 | 47.1 |
| 100 | 49 | 30.0 | 200 | 650 | 25.5 | 3.25 | 49.7 |
| 100 | 54 | 30.0 | 200 | 700 | 27.0 | 3.50 | 52.1 |
| 100 | 59 | 30.0 | 200 | 750 | 28.5 | 3.75 | 54.3 |
| 100 | 64 | 30.0 | 200 | 800 | 30.0 | 4.00 | 56.4 |
| 100 | 69 | 30.0 | 200 | 850 | 31.5 | 4.25 | 58.3 |
| 100 | 279 | 30.0 | 250 | 600 | 25.5 | 2.40 | 41.8 |
| 100 | 284 | 30.0 | 250 | 650 | 27.0 | 2.60 | 44.3 |
| 100 | 289 | 30.0 | 250 | 700 | 28.5 | 2.80 | 46.6 |
| 100 | 294 | 30.0 | 250 | 750 | 30.0 | 3.00 | 48.8 |
| 100 | 299 | 30.0 | 250 | 800 | 31.5 | 3.20 | 50.8 |
| 100 | 304 | 30.0 | 250 | 850 | 33.0 | 3.40 | 52.6 |
| 100 | 309 | 30.0 | 250 | 900 | 34.5 | 3.60 | 54.4 |
| 100 | 314 | 30.0 | 250 | 950 | 36.0 | 3.80 | 56.1 |
| 100 | 319 | 30.0 | 250 | 1000 | 37.5 | 4.00 | 57.6 |
| 100 | 324 | 30.0 | 250 | 1050 | 39.0 | 4.20 | 59.1 |
| 100 | 519 | 30.0 | 300 | 650 | 28.5 | 2.17 | 40.0 |
| 100 | 524 | 30.0 | 300 | 700 | 30.0 | 2.33 | 42.3 |
| 100 | 529 | 30.0 | 300 | 750 | 31.5 | 2.50 | 44.4 |
| 100 | 534 | 30.0 | 300 | 800 | 33.0 | 2.67 | 46.3 |
| 100 | 539 | 30.0 | 300 | 850 | 34.5 | 2.83 | 48.2 |
| 100 | 544 | 30.0 | 300 | 900 | 36.0 | 3.00 | 49.9 |
| 100 | 549 | 30.0 | 300 | 950 | 37.5 | 3.17 | 51.5 |
| 100 | 554 | 30.0 | 300 | 1000 | 39.0 | 3.33 | 53.0 |
| 100 | 559 | 30.0 | 300 | 1050 | 40.5 | 3.50 | 54.5 |
| 100 | 564 | 30.0 | 300 | 1100 | 42.0 | 3.67 | 55.9 |
| 100 | 569 | 30.0 | 300 | 1150 | 43.5 | 3.83 | 57.2 |
| 100 | 574 | 30.0 | 300 | 1200 | 45.0 | 4.00 | 58.5 |
| 100 | 579 | 30.0 | 300 | 1250 | 46.5 | 4.17 | 59.7 |
| 100 | 764 | 30.0 | 350 | 750 | 33.0 | 2.14 | 40.7 |
| 100 | 769 | 30.0 | 350 | 800 | 34.5 | 2.29 | 42.7 |
| 100 | 774 | 30.0 | 350 | 850 | 36.0 | 2.43 | 44.5 |
| 100 | 779 | 30.0 | 350 | 900 | 37.5 | 2.57 | 46.1 |
| 100 | 784 | 30.0 | 350 | 950 | 39.0 | 2.71 | 47.7 |
| 100 | 789 | 30.0 | 350 | 1000 | 40.5 | 2.86 | 49.2 |
| 100 | 794 | 30.0 | 350 | 1050 | 42.0 | 3.00 | 50.7 |
| 100 | 799 | 30.0 | 350 | 1100 | 43.5 | 3.14 | 52.0 |
| 100 | 804 | 30.0 | 350 | 1150 | 45.0 | 3.29 | 53.3 |
| 100 | 809 | 30.0 | 350 | 1200 | 46.5 | 3.43 | 54.6 |
| 100 | 814 | 30.0 | 350 | 1250 | 48.0 | 3.57 | 55.7 |
| 100 | 819 | 30.0 | 350 | 1300 | 49.5 | 3.71 | 56.9 |
| 100 | 824 | 30.0 | 350 | 1350 | 51.0 | 3.86 | 58.0 |
| 100 | 829 | 30.0 | 350 | 1400 | 52.5 | 4.00 | 59.1 |

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Table B.3 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100 | 1009 | 30.0 | 400 | 850 | 37.5 | 2.13 | 41.3 |
| 100 | 1014 | 30.0 | 400 | 900 | 39.0 | 2.25 | 43.0 |
| 100 | 1019 | 30.0 | 400 | 950 | 40.5 | 2.38 | 44.5 |
| 100 | 1024 | 30.0 | 400 | 1000 | 42.0 | 2.50 | 46.0 |
| 100 | 1029 | 30.0 | 400 | 1050 | 43.5 | 2.63 | 47.4 |
| 100 | 1034 | 30.0 | 400 | 1100 | 45.0 | 2.75 | 48.8 |
| 100 | 1039 | 30.0 | 400 | 1150 | 46.5 | 2.88 | 50.0 |
| 100 | 1044 | 30.0 | 400 | 1200 | 48.0 | 3.00 | 51.2 |
| 100 | 1049 | 30.0 | 400 | 1250 | 49.5 | 3.13 | 52.4 |
| 100 | 1054 | 30.0 | 400 | 1300 | 51.0 | 3.25 | 53.5 |
| 100 | 1059 | 30.0 | 400 | 1350 | 52.5 | 3.38 | 54.6 |
| 100 | 1064 | 30.0 | 400 | 1400 | 54.0 | 3.50 | 55.7 |
| 100 | 1069 | 30.0 | 400 | 1450 | 55.5 | 3.63 | 56.7 |
| 100 | 1074 | 30.0 | 400 | 1500 | 57.0 | 3.75 | 57.6 |
| 100 | 1079 | 30.0 | 400 | 1550 | 58.5 | 3.88 | 58.6 |
| 100 | 1084 | 30.0 | 400 | 1600 | 60.0 | 4.00 | 59.5 |
| 100 | 1249 | 30.0 | 450 | 900 | 40.5 | 2.00 | 40.2 |
| 100 | 1254 | 30.0 | 450 | 950 | 42.0 | 2.11 | 41.8 |
| 100 | 1259 | 30.0 | 450 | 1000 | 43.5 | 2.22 | 43.2 |
| 100 | 1264 | 30.0 | 450 | 1050 | 45.0 | 2.33 | 44.6 |
| 100 | 1269 | 30.0 | 450 | 1100 | 46.5 | 2.44 | 45.9 |
| 100 | 1274 | 30.0 | 450 | 1150 | 48.0 | 2.56 | 47.2 |
| 100 | 1279 | 30.0 | 450 | 1200 | 49.5 | 2.67 | 48.4 |
| 100 | 1284 | 30.0 | 450 | 1250 | 51.0 | 2.78 | 49.5 |
| 100 | 1289 | 30.0 | 450 | 1300 | 52.5 | 2.89 | 50.6 |
| 100 | 1294 | 30.0 | 450 | 1350 | 54.0 | 3.00 | 51.7 |
| 100 | 1299 | 30.0 | 450 | 1400 | 55.5 | 3.11 | 52.7 |
| 100 | 1304 | 30.0 | 450 | 1450 | 57.0 | 3.22 | 53.7 |
| 100 | 1309 | 30.0 | 450 | 1500 | 58.5 | 3.33 | 54.7 |
| 100 | 1314 | 30.0 | 450 | 1550 | 60.0 | 3.44 | 55.6 |
| 100 | 1319 | 30.0 | 450 | 1600 | 61.5 | 3.56 | 56.5 |
| 100 | 1324 | 30.0 | 450 | 1650 | 63.0 | 3.67 | 57.4 |
| 100 | 1329 | 30.0 | 450 | 1700 | 64.5 | 3.78 | 58.2 |
| 100 | 1334 | 30.0 | 450 | 1750 | 66.0 | 3.89 | 59.0 |
| 100 | 1339 | 30.0 | 450 | 1800 | 67.5 | 4.00 | 59.8 |
| 100 | 1494 | 30.0 | 500 | 1000 | 45.0 | 2.00 | 40.8 |
| 100 | 1499 | 30.0 | 500 | 1050 | 46.5 | 2.10 | 42.1 |
| 100 | 1504 | 30.0 | 500 | 1100 | 48.0 | 2.20 | 43.4 |
| 100 | 1509 | 30.0 | 500 | 1150 | 49.5 | 2.30 | 44.7 |
| 100 | 1514 | 30.0 | 500 | 1200 | 51.0 | 2.40 | 45.9 |
| 100 | 1519 | 30.0 | 500 | 1250 | 52.5 | 2.50 | 47.0 |
| 100 | 1524 | 30.0 | 500 | 1300 | 54.0 | 2.60 | 48.1 |
| 100 | 1529 | 30.0 | 500 | 1350 | 55.5 | 2.70 | 49.1 |
| 100 | 1534 | 30.0 | 500 | 1400 | 57.0 | 2.80 | 50.1 |
| 100 | 1539 | 30.0 | 500 | 1450 | 58.5 | 2.90 | 51.1 |
| 100 | 1544 | 30.0 | 500 | 1500 | 60.0 | 3.00 | 52.1 |

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Table B.3 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100 | 1549 | 30.0 | 500 | 1550 | 61.5 | 3.10 | 53.0 |
| 100 | 1554 | 30.0 | 500 | 1600 | 63.0 | 3.20 | 53.9 |
| 100 | 1559 | 30.0 | 500 | 1650 | 64.5 | 3.30 | 54.7 |
| 100 | 1564 | 30.0 | 500 | 1700 | 66.0 | 3.40 | 55.6 |
| 100 | 1569 | 30.0 | 500 | 1750 | 67.5 | 3.50 | 56.4 |
| 100 | 1574 | 30.0 | 500 | 1800 | 69.0 | 3.60 | 57.2 |
| 100 | 1579 | 30.0 | 500 | 1850 | 70.5 | 3.70 | 57.9 |
| 100 | 1584 | 30.0 | 500 | 1900 | 72.0 | 3.80 | 58.7 |
| 100 | 1589 | 30.0 | 500 | 1950 | 73.5 | 3.90 | 59.4 |
| 100 | 1739 | 30.0 | 550 | 1100 | 49.5 | 2.00 | 41.2 |
| 100 | 1744 | 30.0 | 550 | 1150 | 51.0 | 2.09 | 42.4 |
| 100 | 1749 | 30.0 | 550 | 1200 | 52.5 | 2.18 | 43.6 |
| 100 | 1754 | 30.0 | 550 | 1250 | 54.0 | 2.27 | 44.7 |
| 100 | 1759 | 30.0 | 550 | 1300 | 55.5 | 2.36 | 45.8 |
| 100 | 1764 | 30.0 | 550 | 1350 | 57.0 | 2.45 | 46.9 |
| 100 | 1769 | 30.0 | 550 | 1400 | 58.5 | 2.55 | 47.9 |
| 100 | 1774 | 30.0 | 550 | 1450 | 60.0 | 2.64 | 48.8 |
| 100 | 1779 | 30.0 | 550 | 1500 | 61.5 | 2.73 | 49.7 |
| 100 | 1784 | 30.0 | 550 | 1550 | 63.0 | 2.82 | 50.7 |
| 100 | 1789 | 30.0 | 550 | 1600 | 64.5 | 2.91 | 51.5 |
| 100 | 1794 | 30.0 | 550 | 1650 | 66.0 | 3.00 | 52.4 |
| 100 | 1799 | 30.0 | 550 | 1700 | 67.5 | 3.09 | 53.2 |
| 100 | 1804 | 30.0 | 550 | 1750 | 69.0 | 3.18 | 54.0 |
| 100 | 1809 | 30.0 | 550 | 1800 | 70.5 | 3.27 | 54.8 |
| 100 | 1814 | 30.0 | 550 | 1850 | 72.0 | 3.36 | 55.5 |
| 100 | 1819 | 30.0 | 550 | 1900 | 73.5 | 3.45 | 56.3 |
| 100 | 1824 | 30.0 | 550 | 1950 | 75.0 | 3.55 | 57.0 |
| 100 | 1829 | 30.0 | 550 | 2000 | 76.5 | 3.64 | 57.7 |
| 100 | 1834 | 30.0 | 550 | 2050 | 78.0 | 3.73 | 58.4 |
| 100 | 1839 | 30.0 | 550 | 2100 | 79.5 | 3.82 | 59.1 |
| 100 | 1844 | 30.0 | 550 | 2150 | 81.0 | 3.91 | 59.7 |
| 100 | 1979 | 30.0 | 600 | 1150 | 52.5 | 1.92 | 40.4 |
| 100 | 1984 | 30.0 | 600 | 1200 | 54.0 | 2.00 | 41.6 |
| 100 | 1989 | 30.0 | 600 | 1250 | 55.5 | 2.08 | 42.7 |
| 100 | 1994 | 30.0 | 600 | 1300 | 57.0 | 2.17 | 43.8 |
| 100 | 1999 | 30.0 | 600 | 1350 | 58.5 | 2.25 | 44.8 |
| 100 | 2004 | 30.0 | 600 | 1400 | 60.0 | 2.33 | 45.8 |
| 100 | 2009 | 30.0 | 600 | 1450 | 61.5 | 2.42 | 46.7 |
| 100 | 2014 | 30.0 | 600 | 1500 | 63.0 | 2.50 | 47.7 |
| 100 | 2019 | 30.0 | 600 | 1550 | 64.5 | 2.58 | 48.6 |
| 100 | 2024 | 30.0 | 600 | 1600 | 66.0 | 2.67 | 49.4 |
| 100 | 2029 | 30.0 | 600 | 1650 | 67.5 | 2.75 | 50.3 |
| 100 | 2034 | 30.0 | 600 | 1700 | 69.0 | 2.83 | 51.1 |
| 100 | 2039 | 30.0 | 600 | 1750 | 70.5 | 2.92 | 51.9 |
| 100 | 2044 | 30.0 | 600 | 1800 | 72.0 | 3.00 | 52.6 |
| 100 | 2049 | 30.0 | 600 | 1850 | 73.5 | 3.08 | 53.4 |

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Table B.3 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100 | 2054 | 30.0 | 600 | 1900 | 75.0 | 3.17 | 54.1 |
| 100 | 2059 | 30.0 | 600 | 1950 | 76.5 | 3.25 | 54.8 |
| 100 | 2064 | 30.0 | 600 | 2000 | 78.0 | 3.33 | 55.5 |
| 100 | 2069 | 30.0 | 600 | 2050 | 79.5 | 3.42 | 56.2 |
| 100 | 2074 | 30.0 | 600 | 2100 | 81.0 | 3.50 | 56.8 |
| 100 | 2079 | 30.0 | 600 | 2150 | 82.5 | 3.58 | 57.5 |
| 100 | 2084 | 30.0 | 600 | 2200 | 84.0 | 3.67 | 58.1 |
| 100 | 2089 | 30.0 | 600 | 2250 | 85.5 | 3.75 | 58.7 |
| 100 | 2094 | 30.0 | 600 | 2300 | 87.0 | 3.83 | 59.4 |
| 100 | 2099 | 30.0 | 600 | 2350 | 88.5 | 3.92 | 60.0 |
| 100 | 2224 | 30.0 | 650 | 1250 | 57.0 | 1.92 | 40.9 |
| 100 | 2229 | 30.0 | 650 | 1300 | 58.5 | 2.00 | 41.9 |
| 100 | 2234 | 30.0 | 650 | 1350 | 60.0 | 2.08 | 42.9 |
| 100 | 2239 | 30.0 | 650 | 1400 | 61.5 | 2.15 | 43.9 |
| 100 | 2244 | 30.0 | 650 | 1450 | 63.0 | 2.23 | 44.9 |
| 100 | 2249 | 30.0 | 650 | 1500 | 64.5 | 2.31 | 45.8 |
| 100 | 2254 | 30.0 | 650 | 1550 | 66.0 | 2.38 | 46.6 |
| 100 | 2259 | 30.0 | 650 | 1600 | 67.5 | 2.46 | 47.5 |
| 100 | 2264 | 30.0 | 650 | 1650 | 69.0 | 2.54 | 48.3 |
| 100 | 2269 | 30.0 | 650 | 1700 | 70.5 | 2.62 | 49.1 |
| 100 | 2274 | 30.0 | 650 | 1750 | 72.0 | 2.69 | 49.9 |
| 100 | 2279 | 30.0 | 650 | 1800 | 73.5 | 2.77 | 50.7 |
| 100 | 2284 | 30.0 | 650 | 1850 | 75.0 | 2.85 | 51.4 |
| 100 | 2289 | 30.0 | 650 | 1900 | 76.5 | 2.92 | 52.1 |
| 100 | 2294 | 30.0 | 650 | 1950 | 78.0 | 3.00 | 52.8 |
| 100 | 2299 | 30.0 | 650 | 2000 | 79.5 | 3.08 | 53.5 |
| 100 | 2304 | 30.0 | 650 | 2050 | 81.0 | 3.15 | 54.2 |
| 100 | 2309 | 30.0 | 650 | 2100 | 82.5 | 3.23 | 54.8 |
| 100 | 2314 | 30.0 | 650 | 2150 | 84.0 | 3.31 | 55.5 |
| 100 | 2319 | 30.0 | 650 | 2200 | 85.5 | 3.38 | 56.1 |
| 100 | 2324 | 30.0 | 650 | 2250 | 87.0 | 3.46 | 56.7 |
| 100 | 2329 | 30.0 | 650 | 2300 | 88.5 | 3.54 | 57.3 |
| 100 | 2334 | 30.0 | 650 | 2350 | 90.0 | 3.62 | 57.9 |
| 100 | 2339 | 30.0 | 650 | 2400 | 91.5 | 3.69 | 58.5 |
| 100 | 2344 | 30.0 | 650 | 2450 | 93.0 | 3.77 | 59.1 |
| 100 | 2349 | 30.0 | 650 | 2500 | 94.5 | 3.85 | 59.6 |
| 100 | 2464 | 30.0 | 700 | 1300 | 60.0 | 1.86 | 40.2 |
| 100 | 2469 | 30.0 | 700 | 1350 | 61.5 | 1.93 | 41.2 |
| 100 | 2474 | 30.0 | 700 | 1400 | 63.0 | 2.00 | 42.2 |
| 100 | 2479 | 30.0 | 700 | 1450 | 64.5 | 2.07 | 43.1 |
| 100 | 2484 | 30.0 | 700 | 1500 | 66.0 | 2.14 | 44.0 |
| 100 | 2489 | 30.0 | 700 | 1550 | 67.5 | 2.21 | 44.9 |
| 100 | 2494 | 30.0 | 700 | 1600 | 69.0 | 2.29 | 45.7 |
| 100 | 2499 | 30.0 | 700 | 1650 | 70.5 | 2.36 | 46.6 |
| 100 | 2504 | 30.0 | 700 | 1700 | 72.0 | 2.43 | 47.4 |
| 100 | 2509 | 30.0 | 700 | 1750 | 73.5 | 2.50 | 48.1 |

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Table B.3 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100 | 2514 | 30.0 | 700 | 1800 | 75.0 | 2.57 | 48.9 |
| 100 | 2519 | 30.0 | 700 | 1850 | 76.5 | 2.64 | 49.6 |
| 100 | 2524 | 30.0 | 700 | 1900 | 78.0 | 2.71 | 50.3 |
| 100 | 2529 | 30.0 | 700 | 1950 | 79.5 | 2.79 | 51.0 |
| 100 | 2534 | 30.0 | 700 | 2000 | 81.0 | 2.86 | 51.7 |
| 100 | 2539 | 30.0 | 700 | 2050 | 82.5 | 2.93 | 52.4 |
| 100 | 2544 | 30.0 | 700 | 2100 | 84.0 | 3.00 | 53.0 |
| 100 | 2549 | 30.0 | 700 | 2150 | 85.5 | 3.07 | 53.6 |
| 100 | 2554 | 30.0 | 700 | 2200 | 87.0 | 3.14 | 54.3 |
| 100 | 2559 | 30.0 | 700 | 2250 | 88.5 | 3.21 | 54.9 |
| 100 | 2564 | 30.0 | 700 | 2300 | 90.0 | 3.29 | 55.5 |
| 100 | 2569 | 30.0 | 700 | 2350 | 91.5 | 3.36 | 56.0 |
| 100 | 2574 | 30.0 | 700 | 2400 | 93.0 | 3.43 | 56.6 |
| 100 | 2579 | 30.0 | 700 | 2450 | 94.5 | 3.50 | 57.2 |
| 100 | 2584 | 30.0 | 700 | 2500 | 96.0 | 3.57 | 57.7 |
| 100 | 2709 | 30.0 | 750 | 1400 | 64.5 | 1.87 | 40.6 |
| 100 | 2714 | 30.0 | 750 | 1450 | 66.0 | 1.93 | 41.5 |

Table B.4: The SP_x of the 8T NAND2 at 100mV. Results from the parametric DC analysis.

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|----------------|
| 100.0 | 385 | 30.0 | 200 | 1450 | 49.5 | 7.25 | 40.7 |
| 100.0 | 400 | 30.0 | 200 | 1500 | 51.0 | 7.50 | 41.6 |
| 100.0 | 415 | 30.0 | 200 | 1550 | 52.5 | 7.75 | 42.4 |
| 100.0 | 430 | 30.0 | 200 | 1600 | 54.0 | 8.00 | 43.3 |
| 100.0 | 445 | 30.0 | 200 | 1650 | 55.5 | 8.25 | 44.1 |
| 100.0 | 460 | 30.0 | 200 | 1700 | 57.0 | 8.50 | 44.9 |
| 100.0 | 475 | 30.0 | 200 | 1750 | 58.5 | 8.75 | 45.6 |
| 100.0 | 490 | 30.0 | 200 | 1800 | 60.0 | 9.00 | 46.4 |
| 100.0 | 505 | 30.0 | 200 | 1850 | 61.5 | 9.25 | 47.1 |
| 100.0 | 520 | 30.0 | 200 | 1900 | 63.0 | 9.50 | 47.8 |
| 100.0 | 535 | 30.0 | 200 | 1950 | 64.5 | 9.75 | 48.5 |
| 100.0 | 550 | 30.0 | 200 | 2000 | 66.0 | 10.00 | 49.1 |
| 100.0 | 565 | 30.0 | 200 | 2050 | 67.5 | 10.25 | 49.8 |
| 100.0 | 580 | 30.0 | 200 | 2100 | 69.0 | 10.50 | 50.4 |
| 100.0 | 595 | 30.0 | 200 | 2150 | 70.5 | 10.75 | 51.0 |
| 100.0 | 610 | 30.0 | 200 | 2200 | 72.0 | 11.00 | 51.6 |
| 100.0 | 625 | 30.0 | 200 | 2250 | 73.5 | 11.25 | 52.2 |
| 100.0 | 640 | 30.0 | 200 | 2300 | 75.0 | 11.50 | 52.8 |
| 100.0 | 655 | 30.0 | 200 | 2350 | 76.5 | 11.75 | 53.4 |
| 100.0 | 670 | 30.0 | 200 | 2400 | 78.0 | 12.00 | 54.0 |
| 100.0 | 685 | 30.0 | 200 | 2450 | 79.5 | 12.25 | 54.5 |
| 100.0 | 700 | 30.0 | 200 | 2500 | 81.0 | 12.50 | 55.0 |
| 100.0 | 701 | 35.0 | 200 | 2500 | 94.5 | 12.50 | 40.4 |
| 100.0 | 1180 | 30.0 | 250 | 1750 | 60.0 | 7.00 | 40.3 |
| 100.0 | 1195 | 30.0 | 250 | 1800 | 61.5 | 7.20 | 41.0 |
| 100.0 | 1210 | 30.0 | 250 | 1850 | 63.0 | 7.40 | 41.7 |
| 100.0 | 1225 | 30.0 | 250 | 1900 | 64.5 | 7.60 | 42.4 |
| 100.0 | 1240 | 30.0 | 250 | 1950 | 66.0 | 7.80 | 43.1 |
| 100.0 | 1255 | 30.0 | 250 | 2000 | 67.5 | 8.00 | 43.7 |
| 100.0 | 1270 | 30.0 | 250 | 2050 | 69.0 | 8.20 | 44.3 |
| 100.0 | 1285 | 30.0 | 250 | 2100 | 70.5 | 8.40 | 45.0 |
| 100.0 | 1300 | 30.0 | 250 | 2150 | 72.0 | 8.60 | 45.6 |
| 100.0 | 1315 | 30.0 | 250 | 2200 | 73.5 | 8.80 | 46.2 |
| 100.0 | 1330 | 30.0 | 250 | 2250 | 75.0 | 9.00 | 46.7 |
| 100.0 | 1345 | 30.0 | 250 | 2300 | 76.5 | 9.20 | 47.3 |
| 100.0 | 1360 | 30.0 | 250 | 2350 | 78.0 | 9.40 | 47.9 |
| 100.0 | 1375 | 30.0 | 250 | 2400 | 79.5 | 9.60 | 48.4 |
| 100.0 | 1390 | 30.0 | 250 | 2450 | 81.0 | 9.80 | 48.9 |
| 100.0 | 1405 | 30.0 | 250 | 2500 | 82.5 | 10.00 | 49.5 |
| 100.0 | 1975 | 30.0 | 300 | 2050 | 70.5 | 6.83 | 40.0 |
| 100.0 | 1990 | 30.0 | 300 | 2100 | 72.0 | 7.00 | 40.6 |
| 100.0 | 2005 | 30.0 | 300 | 2150 | 73.5 | 7.17 | 41.2 |
| 100.0 | 2020 | 30.0 | 300 | 2200 | 75.0 | 7.33 | 41.8 |
| 100.0 | 2035 | 30.0 | 300 | 2250 | 76.5 | 7.50 | 42.4 |
| 100.0 | 2050 | 30.0 | 300 | 2300 | 78.0 | 7.67 | 42.9 |

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Table B.4 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100.0 | 2065 | 30.0 | 300 | 2350 | 79.5 | 7.83 | 43.5 |
| 100.0 | 2080 | 30.0 | 300 | 2400 | 81.0 | 8.00 | 44.0 |
| 100.0 | 2095 | 30.0 | 300 | 2450 | 82.5 | 8.17 | 44.5 |
| 100.0 | 2110 | 30.0 | 300 | 2500 | 84.0 | 8.33 | 45.0 |
| 100.0 | 2785 | 30.0 | 350 | 2400 | 82.5 | 6.86 | 40.4 |
| 100.0 | 2800 | 30.0 | 350 | 2450 | 84.0 | 7.00 | 40.9 |
| 100.0 | 2815 | 30.0 | 350 | 2500 | 85.5 | 7.14 | 41.4 |

Table B.5: The SP_x of the 4T NOR2 at 100mV. Results from the parametric DC analysis.

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|----------------|
| 100.0 | 84 | 30.0 | 200 | 1000 | 36.0 | 5.00 | 40.3 |
| 100.0 | 89 | 30.0 | 200 | 1050 | 37.5 | 5.25 | 41.8 |
| 100.0 | 94 | 30.0 | 200 | 1100 | 39.0 | 5.50 | 43.2 |
| 100.0 | 99 | 30.0 | 200 | 1150 | 40.5 | 5.75 | 44.6 |
| 100.0 | 104 | 30.0 | 200 | 1200 | 42.0 | 6.00 | 45.8 |
| 100.0 | 109 | 30.0 | 200 | 1250 | 43.5 | 6.25 | 47.0 |
| 100.0 | 114 | 30.0 | 200 | 1300 | 45.0 | 6.50 | 48.1 |
| 100.0 | 119 | 30.0 | 200 | 1350 | 46.5 | 6.75 | 49.2 |
| 100.0 | 124 | 30.0 | 200 | 1400 | 48.0 | 7.00 | 50.2 |
| 100.0 | 129 | 30.0 | 200 | 1450 | 49.5 | 7.25 | 51.2 |
| 100.0 | 134 | 30.0 | 200 | 1500 | 51.0 | 7.50 | 52.1 |
| 100.0 | 139 | 30.0 | 200 | 1550 | 52.5 | 7.75 | 53.0 |
| 100.0 | 144 | 30.0 | 200 | 1600 | 54.0 | 8.00 | 53.8 |
| 100.0 | 149 | 30.0 | 200 | 1650 | 55.5 | 8.25 | 54.6 |
| 100.0 | 154 | 30.0 | 200 | 1700 | 57.0 | 8.50 | 55.4 |
| 100.0 | 159 | 30.0 | 200 | 1750 | 58.5 | 8.75 | 56.2 |
| 100.0 | 164 | 30.0 | 200 | 1800 | 60.0 | 9.00 | 56.9 |
| 100.0 | 169 | 30.0 | 200 | 1850 | 61.5 | 9.25 | 57.6 |
| 100.0 | 174 | 30.0 | 200 | 1900 | 63.0 | 9.50 | 58.3 |
| 100.0 | 179 | 30.0 | 200 | 1950 | 64.5 | 9.75 | 59.0 |
| 100.0 | 184 | 30.0 | 200 | 2000 | 66.0 | 10.00 | 59.6 |
| 100.0 | 339 | 30.0 | 250 | 1200 | 43.5 | 4.80 | 40.0 |
| 100.0 | 344 | 30.0 | 250 | 1250 | 45.0 | 5.00 | 41.2 |
| 100.0 | 349 | 30.0 | 250 | 1300 | 46.5 | 5.20 | 42.4 |
| 100.0 | 354 | 30.0 | 250 | 1350 | 48.0 | 5.40 | 43.5 |
| 100.0 | 359 | 30.0 | 250 | 1400 | 49.5 | 5.60 | 44.6 |
| 100.0 | 364 | 30.0 | 250 | 1450 | 51.0 | 5.80 | 45.6 |
| 100.0 | 369 | 30.0 | 250 | 1500 | 52.5 | 6.00 | 46.5 |
| 100.0 | 374 | 30.0 | 250 | 1550 | 54.0 | 6.20 | 47.4 |
| 100.0 | 379 | 30.0 | 250 | 1600 | 55.5 | 6.40 | 48.3 |
| 100.0 | 384 | 30.0 | 250 | 1650 | 57.0 | 6.60 | 49.2 |
| 100.0 | 389 | 30.0 | 250 | 1700 | 58.5 | 6.80 | 50.0 |
| 100.0 | 394 | 30.0 | 250 | 1750 | 60.0 | 7.00 | 50.8 |
| 100.0 | 399 | 30.0 | 250 | 1800 | 61.5 | 7.20 | 51.5 |
| 100.0 | 404 | 30.0 | 250 | 1850 | 63.0 | 7.40 | 52.2 |
| 100.0 | 409 | 30.0 | 250 | 1900 | 64.5 | 7.60 | 52.9 |
| 100.0 | 414 | 30.0 | 250 | 1950 | 66.0 | 7.80 | 53.6 |
| 100.0 | 419 | 30.0 | 250 | 2000 | 67.5 | 8.00 | 54.3 |
| 100.0 | 424 | 30.0 | 250 | 2050 | 69.0 | 8.20 | 54.9 |
| 100.0 | 429 | 30.0 | 250 | 2100 | 70.5 | 8.40 | 55.5 |
| 100.0 | 434 | 30.0 | 250 | 2150 | 72.0 | 8.60 | 56.1 |
| 100.0 | 439 | 30.0 | 250 | 2200 | 73.5 | 8.80 | 56.7 |
| 100.0 | 444 | 30.0 | 250 | 2250 | 75.0 | 9.00 | 57.3 |
| 100.0 | 449 | 30.0 | 250 | 2300 | 76.5 | 9.20 | 57.9 |
| 100.0 | 454 | 30.0 | 250 | 2350 | 78.0 | 9.40 | 58.4 |

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Table B.5 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100.0 | 459 | 30.0 | 250 | 2400 | 79.5 | 9.60 | 58.9 |
| 100.0 | 464 | 30.0 | 250 | 2450 | 81.0 | 9.80 | 59.4 |
| 100.0 | 469 | 30.0 | 250 | 2500 | 82.5 | 10.00 | 59.9 |
| 100.0 | 599 | 30.0 | 300 | 1450 | 52.5 | 4.83 | 40.9 |
| 100.0 | 604 | 30.0 | 300 | 1500 | 54.0 | 5.00 | 41.9 |
| 100.0 | 609 | 30.0 | 300 | 1550 | 55.5 | 5.17 | 42.8 |
| 100.0 | 614 | 30.0 | 300 | 1600 | 57.0 | 5.33 | 43.7 |
| 100.0 | 619 | 30.0 | 300 | 1650 | 58.5 | 5.50 | 44.6 |
| 100.0 | 624 | 30.0 | 300 | 1700 | 60.0 | 5.67 | 45.4 |
| 100.0 | 629 | 30.0 | 300 | 1750 | 61.5 | 5.83 | 46.2 |
| 100.0 | 634 | 30.0 | 300 | 1800 | 63.0 | 6.00 | 47.0 |
| 100.0 | 639 | 30.0 | 300 | 1850 | 64.5 | 6.17 | 47.7 |
| 100.0 | 644 | 30.0 | 300 | 1900 | 66.0 | 6.33 | 48.5 |
| 100.0 | 649 | 30.0 | 300 | 1950 | 67.5 | 6.50 | 49.2 |
| 100.0 | 654 | 30.0 | 300 | 2000 | 69.0 | 6.67 | 49.8 |
| 100.0 | 659 | 30.0 | 300 | 2050 | 70.5 | 6.83 | 50.5 |
| 100.0 | 664 | 30.0 | 300 | 2100 | 72.0 | 7.00 | 51.1 |
| 100.0 | 669 | 30.0 | 300 | 2150 | 73.5 | 7.17 | 51.7 |
| 100.0 | 674 | 30.0 | 300 | 2200 | 75.0 | 7.33 | 52.3 |
| 100.0 | 679 | 30.0 | 300 | 2250 | 76.5 | 7.50 | 52.9 |
| 100.0 | 684 | 30.0 | 300 | 2300 | 78.0 | 7.67 | 53.5 |
| 100.0 | 689 | 30.0 | 300 | 2350 | 79.5 | 7.83 | 54.0 |
| 100.0 | 694 | 30.0 | 300 | 2400 | 81.0 | 8.00 | 54.6 |
| 100.0 | 699 | 30.0 | 300 | 2450 | 82.5 | 8.17 | 55.1 |
| 100.0 | 704 | 30.0 | 300 | 2500 | 84.0 | 8.33 | 55.6 |
| 100.0 | 854 | 30.0 | 350 | 1650 | 60.0 | 4.71 | 40.6 |
| 100.0 | 859 | 30.0 | 350 | 1700 | 61.5 | 4.86 | 41.5 |
| 100.0 | 864 | 30.0 | 350 | 1750 | 63.0 | 5.00 | 42.3 |
| 100.0 | 869 | 30.0 | 350 | 1800 | 64.5 | 5.14 | 43.1 |
| 100.0 | 874 | 30.0 | 350 | 1850 | 66.0 | 5.29 | 43.9 |
| 100.0 | 879 | 30.0 | 350 | 1900 | 67.5 | 5.43 | 44.6 |
| 100.0 | 884 | 30.0 | 350 | 1950 | 69.0 | 5.57 | 45.3 |
| 100.0 | 889 | 30.0 | 350 | 2000 | 70.5 | 5.71 | 46.0 |
| 100.0 | 894 | 30.0 | 350 | 2050 | 72.0 | 5.86 | 46.7 |
| 100.0 | 899 | 30.0 | 350 | 2100 | 73.5 | 6.00 | 47.3 |
| 100.0 | 904 | 30.0 | 350 | 2150 | 75.0 | 6.14 | 48.0 |
| 100.0 | 909 | 30.0 | 350 | 2200 | 76.5 | 6.29 | 48.6 |
| 100.0 | 914 | 30.0 | 350 | 2250 | 78.0 | 6.43 | 49.2 |
| 100.0 | 919 | 30.0 | 350 | 2300 | 79.5 | 6.57 | 49.7 |
| 100.0 | 924 | 30.0 | 350 | 2350 | 81.0 | 6.71 | 50.3 |
| 100.0 | 929 | 30.0 | 350 | 2400 | 82.5 | 6.86 | 50.8 |
| 100.0 | 934 | 30.0 | 350 | 2450 | 84.0 | 7.00 | 51.4 |
| 100.0 | 939 | 30.0 | 350 | 2500 | 85.5 | 7.14 | 51.9 |
| 100.0 | 1109 | 30.0 | 400 | 1850 | 67.5 | 4.63 | 40.4 |
| 100.0 | 1114 | 30.0 | 400 | 1900 | 69.0 | 4.75 | 41.2 |
| 100.0 | 1119 | 30.0 | 400 | 1950 | 70.5 | 4.88 | 41.9 |

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Table B.5 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100.0 | 1124 | 30.0 | 400 | 2000 | 72.0 | 5.00 | 42.6 |
| 100.0 | 1129 | 30.0 | 400 | 2050 | 73.5 | 5.13 | 43.3 |
| 100.0 | 1134 | 30.0 | 400 | 2100 | 75.0 | 5.25 | 44.0 |
| 100.0 | 1139 | 30.0 | 400 | 2150 | 76.5 | 5.38 | 44.6 |
| 100.0 | 1144 | 30.0 | 400 | 2200 | 78.0 | 5.50 | 45.2 |
| 100.0 | 1149 | 30.0 | 400 | 2250 | 79.5 | 5.63 | 45.8 |
| 100.0 | 1154 | 30.0 | 400 | 2300 | 81.0 | 5.75 | 46.4 |
| 100.0 | 1159 | 30.0 | 400 | 2350 | 82.5 | 5.88 | 47.0 |
| 100.0 | 1164 | 30.0 | 400 | 2400 | 84.0 | 6.00 | 47.6 |
| 100.0 | 1169 | 30.0 | 400 | 2450 | 85.5 | 6.13 | 48.1 |
| 100.0 | 1174 | 30.0 | 400 | 2500 | 87.0 | 6.25 | 48.6 |
| 100.0 | 1364 | 30.0 | 450 | 2050 | 75.0 | 4.56 | 40.3 |
| 100.0 | 1369 | 30.0 | 450 | 2100 | 76.5 | 4.67 | 41.0 |
| 100.0 | 1374 | 30.0 | 450 | 2150 | 78.0 | 4.78 | 41.6 |
| 100.0 | 1379 | 30.0 | 450 | 2200 | 79.5 | 4.89 | 42.3 |
| 100.0 | 1384 | 30.0 | 450 | 2250 | 81.0 | 5.00 | 42.9 |
| 100.0 | 1389 | 30.0 | 450 | 2300 | 82.5 | 5.11 | 43.5 |
| 100.0 | 1394 | 30.0 | 450 | 2350 | 84.0 | 5.22 | 44.1 |
| 100.0 | 1399 | 30.0 | 450 | 2400 | 85.5 | 5.33 | 44.6 |
| 100.0 | 1404 | 30.0 | 450 | 2450 | 87.0 | 5.44 | 45.2 |
| 100.0 | 1409 | 30.0 | 450 | 2500 | 88.5 | 5.56 | 45.7 |
| 100.0 | 1619 | 30.0 | 500 | 2250 | 82.5 | 4.50 | 40.2 |
| 100.0 | 1624 | 30.0 | 500 | 2300 | 84.0 | 4.60 | 40.8 |
| 100.0 | 1629 | 30.0 | 500 | 2350 | 85.5 | 4.70 | 41.4 |
| 100.0 | 1634 | 30.0 | 500 | 2400 | 87.0 | 4.80 | 42.0 |
| 100.0 | 1639 | 30.0 | 500 | 2450 | 88.5 | 4.90 | 42.5 |
| 100.0 | 1644 | 30.0 | 500 | 2500 | 90.0 | 5.00 | 43.1 |
| 100.0 | 1874 | 30.0 | 550 | 2450 | 90.0 | 4.45 | 40.1 |
| 100.0 | 1879 | 30.0 | 550 | 2500 | 91.5 | 4.55 | 40.6 |
| 100.0 | 3194 | 35.0 | 200 | 1550 | 61.3 | 7.75 | 40.0 |
| 100.0 | 3199 | 35.0 | 200 | 1600 | 63.0 | 8.00 | 40.9 |
| 100.0 | 3204 | 35.0 | 200 | 1650 | 64.8 | 8.25 | 41.6 |
| 100.0 | 3209 | 35.0 | 200 | 1700 | 66.5 | 8.50 | 42.4 |
| 100.0 | 3214 | 35.0 | 200 | 1750 | 68.3 | 8.75 | 43.1 |
| 100.0 | 3219 | 35.0 | 200 | 1800 | 70.0 | 9.00 | 43.8 |
| 100.0 | 3224 | 35.0 | 200 | 1850 | 71.8 | 9.25 | 44.5 |
| 100.0 | 3229 | 35.0 | 200 | 1900 | 73.5 | 9.50 | 45.1 |
| 100.0 | 3234 | 35.0 | 200 | 1950 | 75.3 | 9.75 | 45.8 |
| 100.0 | 3239 | 35.0 | 200 | 2000 | 77.0 | 10.00 | 46.4 |
| 100.0 | 3244 | 35.0 | 200 | 2050 | 78.8 | 10.25 | 47.0 |
| 100.0 | 3249 | 35.0 | 200 | 2100 | 80.5 | 10.50 | 47.6 |
| 100.0 | 3254 | 35.0 | 200 | 2150 | 82.3 | 10.75 | 48.1 |
| 100.0 | 3259 | 35.0 | 200 | 2200 | 84.0 | 11.00 | 48.7 |
| 100.0 | 3264 | 35.0 | 200 | 2250 | 85.8 | 11.25 | 49.2 |
| 100.0 | 3269 | 35.0 | 200 | 2300 | 87.5 | 11.50 | 49.7 |
| 100.0 | 3274 | 35.0 | 200 | 2350 | 89.3 | 11.75 | 50.2 |

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Table B.5 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100.0 | 3279 | 35.0 | 200 | 2400 | 91.0 | 12.00 | 50.7 |
| 100.0 | 3284 | 35.0 | 200 | 2450 | 92.8 | 12.25 | 51.2 |
| 100.0 | 3289 | 35.0 | 200 | 2500 | 94.5 | 12.50 | 51.6 |
| 100.0 | 3469 | 35.0 | 250 | 1950 | 77.0 | 7.80 | 40.4 |
| 100.0 | 3474 | 35.0 | 250 | 2000 | 78.8 | 8.00 | 41.1 |
| 100.0 | 3479 | 35.0 | 250 | 2050 | 80.5 | 8.20 | 41.7 |
| 100.0 | 3484 | 35.0 | 250 | 2100 | 82.3 | 8.40 | 42.3 |
| 100.0 | 3489 | 35.0 | 250 | 2150 | 84.0 | 8.60 | 42.9 |
| 100.0 | 3494 | 35.0 | 250 | 2200 | 85.8 | 8.80 | 43.4 |
| 100.0 | 3499 | 35.0 | 250 | 2250 | 87.5 | 9.00 | 44.0 |
| 100.0 | 3504 | 35.0 | 250 | 2300 | 89.3 | 9.20 | 44.5 |
| 100.0 | 3509 | 35.0 | 250 | 2350 | 91.0 | 9.40 | 45.0 |
| 100.0 | 3514 | 35.0 | 250 | 2400 | 92.8 | 9.60 | 45.5 |
| 100.0 | 3519 | 35.0 | 250 | 2450 | 94.5 | 9.80 | 46.0 |
| 100.0 | 3524 | 35.0 | 250 | 2500 | 96.3 | 10.00 | 46.5 |
| 100.0 | 3739 | 35.0 | 300 | 2300 | 91.0 | 7.67 | 40.2 |
| 100.0 | 3744 | 35.0 | 300 | 2350 | 92.8 | 7.83 | 40.7 |
| 100.0 | 3749 | 35.0 | 300 | 2400 | 94.5 | 8.00 | 41.2 |
| 100.0 | 3754 | 35.0 | 300 | 2450 | 96.3 | 8.17 | 41.7 |
| 100.0 | 3759 | 35.0 | 300 | 2500 | 98.0 | 8.33 | 42.2 |
| 100.0 | 6314 | 40.0 | 200 | 2200 | 96.0 | 11.00 | 40.2 |
| 100.0 | 6319 | 40.0 | 200 | 2250 | 98.0 | 11.25 | 40.7 |
| 100.0 | 6324 | 40.0 | 200 | 2300 | 100.0 | 11.50 | 41.2 |
| 100.0 | 6329 | 40.0 | 200 | 2350 | 102.0 | 11.75 | 41.7 |
| 100.0 | 6334 | 40.0 | 200 | 2400 | 104.0 | 12.00 | 42.2 |
| 100.0 | 6339 | 40.0 | 200 | 2450 | 106.0 | 12.25 | 42.7 |
| 100.0 | 6344 | 40.0 | 200 | 2500 | 108.0 | 12.50 | 43.1 |

Table B.6: The SP_x of the 8T NOR2 at 100mV. Results from the parametric DC analysis.

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|----------------|
| 100.0 | 5512 | 30.0 | 200 | 400 | 18.0 | 2.00 | 43.1 |
| 100.0 | 5515 | 30.0 | 200 | 450 | 19.5 | 2.25 | 47.6 |
| 100.0 | 5518 | 30.0 | 200 | 500 | 21.0 | 2.50 | 51.4 |
| 100.0 | 5519 | 35.0 | 200 | 500 | 24.5 | 2.50 | 40.4 |
| 100.0 | 5521 | 30.0 | 200 | 550 | 22.5 | 2.75 | 54.6 |
| 100.0 | 5522 | 35.0 | 200 | 550 | 26.3 | 2.75 | 43.3 |
| 100.0 | 5524 | 30.0 | 200 | 600 | 24.0 | 3.00 | 57.4 |
| 100.0 | 5525 | 35.0 | 200 | 600 | 28.0 | 3.00 | 45.9 |
| 100.0 | 5527 | 30.0 | 200 | 650 | 25.5 | 3.25 | 60.0 |
| 100.0 | 5528 | 35.0 | 200 | 650 | 29.8 | 3.25 | 48.1 |
| 100.0 | 5529 | 40.0 | 200 | 650 | 34.0 | 3.25 | 40.5 |
| 100.0 | 5531 | 35.0 | 200 | 700 | 31.5 | 3.50 | 50.2 |
| 100.0 | 5532 | 40.0 | 200 | 700 | 36.0 | 3.50 | 42.5 |
| 100.0 | 5534 | 35.0 | 200 | 750 | 33.3 | 3.75 | 52.0 |
| 100.0 | 5535 | 40.0 | 200 | 750 | 38.0 | 3.75 | 44.2 |
| 100.0 | 5537 | 35.0 | 200 | 800 | 35.0 | 4.00 | 53.7 |
| 100.0 | 5538 | 40.0 | 200 | 800 | 40.0 | 4.00 | 45.8 |
| 100.0 | 5540 | 35.0 | 200 | 850 | 36.8 | 4.25 | 55.3 |
| 100.0 | 5541 | 40.0 | 200 | 850 | 42.0 | 4.25 | 47.3 |
| 100.0 | 5543 | 35.0 | 200 | 900 | 38.5 | 4.50 | 56.7 |
| 100.0 | 5544 | 40.0 | 200 | 900 | 44.0 | 4.50 | 48.7 |
| 100.0 | 5546 | 35.0 | 200 | 950 | 40.3 | 4.75 | 58.1 |
| 100.0 | 5547 | 40.0 | 200 | 950 | 46.0 | 4.75 | 50.0 |
| 100.0 | 5549 | 35.0 | 200 | 1000 | 42.0 | 5.00 | 59.3 |
| 100.0 | 5550 | 40.0 | 200 | 1000 | 48.0 | 5.00 | 51.2 |
| 100.0 | 5553 | 40.0 | 200 | 1050 | 50.0 | 5.25 | 52.3 |
| 100.0 | 5556 | 40.0 | 200 | 1100 | 52.0 | 5.50 | 53.4 |
| 100.0 | 5559 | 40.0 | 200 | 1150 | 54.0 | 5.75 | 54.4 |
| 100.0 | 5562 | 40.0 | 200 | 1200 | 56.0 | 6.00 | 55.3 |
| 100.0 | 5565 | 40.0 | 200 | 1250 | 58.0 | 6.25 | 56.3 |
| 100.0 | 5568 | 40.0 | 200 | 1300 | 60.0 | 6.50 | 57.1 |
| 100.0 | 5571 | 40.0 | 200 | 1350 | 62.0 | 6.75 | 57.9 |
| 100.0 | 5574 | 40.0 | 200 | 1400 | 64.0 | 7.00 | 58.7 |
| 100.0 | 5577 | 40.0 | 200 | 1450 | 66.0 | 7.25 | 59.5 |
| 100.0 | 5656 | 30.0 | 250 | 450 | 21.0 | 1.80 | 41.9 |
| 100.0 | 5659 | 30.0 | 250 | 500 | 22.5 | 2.00 | 45.8 |
| 100.0 | 5662 | 30.0 | 250 | 550 | 24.0 | 2.20 | 49.1 |
| 100.0 | 5665 | 30.0 | 250 | 600 | 25.5 | 2.40 | 52.0 |
| 100.0 | 5666 | 35.0 | 250 | 600 | 29.8 | 2.40 | 40.5 |
| 100.0 | 5668 | 30.0 | 250 | 650 | 27.0 | 2.60 | 54.6 |
| 100.0 | 5669 | 35.0 | 250 | 650 | 31.5 | 2.60 | 42.9 |
| 100.0 | 5671 | 30.0 | 250 | 700 | 28.5 | 2.80 | 56.9 |
| 100.0 | 5672 | 35.0 | 250 | 700 | 33.3 | 2.80 | 45.0 |
| 100.0 | 5674 | 30.0 | 250 | 750 | 30.0 | 3.00 | 59.0 |
| 100.0 | 5675 | 35.0 | 250 | 750 | 35.0 | 3.00 | 46.9 |

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Table B.6 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100.0 | 5678 | 35.0 | 250 | 800 | 36.8 | 3.20 | 48.6 |
| 100.0 | 5679 | 40.0 | 250 | 800 | 42.0 | 3.20 | 40.7 |
| 100.0 | 5681 | 35.0 | 250 | 850 | 38.5 | 3.40 | 50.2 |
| 100.0 | 5682 | 40.0 | 250 | 850 | 44.0 | 3.40 | 42.3 |
| 100.0 | 5684 | 35.0 | 250 | 900 | 40.3 | 3.60 | 51.7 |
| 100.0 | 5685 | 40.0 | 250 | 900 | 46.0 | 3.60 | 43.7 |
| 100.0 | 5687 | 35.0 | 250 | 950 | 42.0 | 3.80 | 53.1 |
| 100.0 | 5688 | 40.0 | 250 | 950 | 48.0 | 3.80 | 45.0 |
| 100.0 | 5690 | 35.0 | 250 | 1000 | 43.8 | 4.00 | 54.4 |
| 100.0 | 5691 | 40.0 | 250 | 1000 | 50.0 | 4.00 | 46.3 |
| 100.0 | 5693 | 35.0 | 250 | 1050 | 45.5 | 4.20 | 55.6 |
| 100.0 | 5694 | 40.0 | 250 | 1050 | 52.0 | 4.20 | 47.4 |
| 100.0 | 5696 | 35.0 | 250 | 1100 | 47.3 | 4.40 | 56.7 |
| 100.0 | 5697 | 40.0 | 250 | 1100 | 54.0 | 4.40 | 48.5 |
| 100.0 | 5699 | 35.0 | 250 | 1150 | 49.0 | 4.60 | 57.8 |
| 100.0 | 5700 | 40.0 | 250 | 1150 | 56.0 | 4.60 | 49.6 |
| 100.0 | 5702 | 35.0 | 250 | 1200 | 50.8 | 4.80 | 58.8 |
| 100.0 | 5703 | 40.0 | 250 | 1200 | 58.0 | 4.80 | 50.5 |
| 100.0 | 5705 | 35.0 | 250 | 1250 | 52.5 | 5.00 | 59.8 |
| 100.0 | 5706 | 40.0 | 250 | 1250 | 60.0 | 5.00 | 51.5 |
| 100.0 | 5709 | 40.0 | 250 | 1300 | 62.0 | 5.20 | 52.4 |
| 100.0 | 5712 | 40.0 | 250 | 1350 | 64.0 | 5.40 | 53.2 |
| 100.0 | 5715 | 40.0 | 250 | 1400 | 66.0 | 5.60 | 54.0 |
| 100.0 | 5718 | 40.0 | 250 | 1450 | 68.0 | 5.80 | 54.8 |
| 100.0 | 5721 | 40.0 | 250 | 1500 | 70.0 | 6.00 | 55.5 |
| 100.0 | 5724 | 40.0 | 250 | 1550 | 72.0 | 6.20 | 56.2 |
| 100.0 | 5727 | 40.0 | 250 | 1600 | 74.0 | 6.40 | 56.9 |
| 100.0 | 5730 | 40.0 | 250 | 1650 | 76.0 | 6.60 | 57.6 |
| 100.0 | 5733 | 40.0 | 250 | 1700 | 78.0 | 6.80 | 58.2 |
| 100.0 | 5736 | 40.0 | 250 | 1750 | 80.0 | 7.00 | 58.8 |
| 100.0 | 5739 | 40.0 | 250 | 1800 | 82.0 | 7.20 | 59.4 |
| 100.0 | 5742 | 40.0 | 250 | 1850 | 84.0 | 7.40 | 60.0 |
| 100.0 | 5800 | 30.0 | 300 | 500 | 24.0 | 1.67 | 41.1 |
| 100.0 | 5803 | 30.0 | 300 | 550 | 25.5 | 1.83 | 44.5 |
| 100.0 | 5806 | 30.0 | 300 | 600 | 27.0 | 2.00 | 47.5 |
| 100.0 | 5809 | 30.0 | 300 | 650 | 28.5 | 2.17 | 50.2 |
| 100.0 | 5812 | 30.0 | 300 | 700 | 30.0 | 2.33 | 52.5 |
| 100.0 | 5813 | 35.0 | 300 | 700 | 35.0 | 2.33 | 40.6 |
| 100.0 | 5815 | 30.0 | 300 | 750 | 31.5 | 2.50 | 54.7 |
| 100.0 | 5816 | 35.0 | 300 | 750 | 36.8 | 2.50 | 42.6 |
| 100.0 | 5818 | 30.0 | 300 | 800 | 33.0 | 2.67 | 56.6 |
| 100.0 | 5819 | 35.0 | 300 | 800 | 38.5 | 2.67 | 44.4 |
| 100.0 | 5821 | 30.0 | 300 | 850 | 34.5 | 2.83 | 58.4 |
| 100.0 | 5822 | 35.0 | 300 | 850 | 40.3 | 2.83 | 46.0 |
| 100.0 | 5825 | 35.0 | 300 | 900 | 42.0 | 3.00 | 47.6 |
| 100.0 | 5828 | 35.0 | 300 | 950 | 43.8 | 3.17 | 49.0 |

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Table B.6 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100.0 | 5829 | 40.0 | 300 | 950 | 50.0 | 3.17 | 40.9 |
| 100.0 | 5831 | 35.0 | 300 | 1000 | 45.5 | 3.33 | 50.3 |
| 100.0 | 5832 | 40.0 | 300 | 1000 | 52.0 | 3.33 | 42.2 |
| 100.0 | 5834 | 35.0 | 300 | 1050 | 47.3 | 3.50 | 51.5 |
| 100.0 | 5835 | 40.0 | 300 | 1050 | 54.0 | 3.50 | 43.4 |
| 100.0 | 5837 | 35.0 | 300 | 1100 | 49.0 | 3.67 | 52.7 |
| 100.0 | 5838 | 40.0 | 300 | 1100 | 56.0 | 3.67 | 44.5 |
| 100.0 | 5840 | 35.0 | 300 | 1150 | 50.8 | 3.83 | 53.8 |
| 100.0 | 5841 | 40.0 | 300 | 1150 | 58.0 | 3.83 | 45.5 |
| 100.0 | 5843 | 35.0 | 300 | 1200 | 52.5 | 4.00 | 54.8 |
| 100.0 | 5844 | 40.0 | 300 | 1200 | 60.0 | 4.00 | 46.6 |
| 100.0 | 5846 | 35.0 | 300 | 1250 | 54.3 | 4.17 | 55.8 |
| 100.0 | 5847 | 40.0 | 300 | 1250 | 62.0 | 4.17 | 47.5 |
| 100.0 | 5849 | 35.0 | 300 | 1300 | 56.0 | 4.33 | 56.8 |
| 100.0 | 5850 | 40.0 | 300 | 1300 | 64.0 | 4.33 | 48.4 |
| 100.0 | 5852 | 35.0 | 300 | 1350 | 57.8 | 4.50 | 57.7 |
| 100.0 | 5853 | 40.0 | 300 | 1350 | 66.0 | 4.50 | 49.3 |
| 100.0 | 5855 | 35.0 | 300 | 1400 | 59.5 | 4.67 | 58.5 |
| 100.0 | 5856 | 40.0 | 300 | 1400 | 68.0 | 4.67 | 50.1 |
| 100.0 | 5858 | 35.0 | 300 | 1450 | 61.3 | 4.83 | 59.3 |
| 100.0 | 5859 | 40.0 | 300 | 1450 | 70.0 | 4.83 | 50.9 |
| 100.0 | 5862 | 40.0 | 300 | 1500 | 72.0 | 5.00 | 51.6 |
| 100.0 | 5865 | 40.0 | 300 | 1550 | 74.0 | 5.17 | 52.4 |
| 100.0 | 5868 | 40.0 | 300 | 1600 | 76.0 | 5.33 | 53.1 |
| 100.0 | 5871 | 40.0 | 300 | 1650 | 78.0 | 5.50 | 53.7 |
| 100.0 | 5874 | 40.0 | 300 | 1700 | 80.0 | 5.67 | 54.4 |
| 100.0 | 5877 | 40.0 | 300 | 1750 | 82.0 | 5.83 | 55.0 |
| 100.0 | 5880 | 40.0 | 300 | 1800 | 84.0 | 6.00 | 55.6 |
| 100.0 | 5883 | 40.0 | 300 | 1850 | 86.0 | 6.17 | 56.2 |
| 100.0 | 5886 | 40.0 | 300 | 1900 | 88.0 | 6.33 | 56.8 |
| 100.0 | 5889 | 40.0 | 300 | 1950 | 90.0 | 6.50 | 57.3 |
| 100.0 | 5892 | 40.0 | 300 | 2000 | 92.0 | 6.67 | 57.9 |
| 100.0 | 5895 | 40.0 | 300 | 2050 | 94.0 | 6.83 | 58.4 |
| 100.0 | 5898 | 40.0 | 300 | 2100 | 96.0 | 7.00 | 58.9 |
| 100.0 | 5901 | 40.0 | 300 | 2150 | 98.0 | 7.17 | 59.4 |
| 100.0 | 5904 | 40.0 | 300 | 2200 | 100.0 | 7.33 | 59.9 |
| 100.0 | 5944 | 30.0 | 350 | 550 | 27.0 | 1.57 | 40.6 |
| 100.0 | 5947 | 30.0 | 350 | 600 | 28.5 | 1.71 | 43.6 |
| 100.0 | 5950 | 30.0 | 350 | 650 | 30.0 | 1.86 | 46.3 |
| 100.0 | 5953 | 30.0 | 350 | 700 | 31.5 | 2.00 | 48.8 |
| 100.0 | 5956 | 30.0 | 350 | 750 | 33.0 | 2.14 | 50.9 |
| 100.0 | 5959 | 30.0 | 350 | 800 | 34.5 | 2.29 | 52.9 |
| 100.0 | 5960 | 35.0 | 350 | 800 | 40.3 | 2.29 | 40.7 |
| 100.0 | 5962 | 30.0 | 350 | 850 | 36.0 | 2.43 | 54.8 |
| 100.0 | 5963 | 35.0 | 350 | 850 | 42.0 | 2.43 | 42.4 |
| 100.0 | 5965 | 30.0 | 350 | 900 | 37.5 | 2.57 | 56.4 |

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Table B.6 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm^2) | Size ratio ($\frac{m}{m}$) | SP_x (mV) |
|------------------|-------|-----------|------------|------------|---------------------------|---------------------------------|----------------|
| 100.0 | 5966 | 35.0 | 350 | 900 | 43.8 | 2.57 | 44.0 |
| 100.0 | 5968 | 30.0 | 350 | 950 | 39.0 | 2.71 | 58.0 |
| 100.0 | 5969 | 35.0 | 350 | 950 | 45.5 | 2.71 | 45.4 |
| 100.0 | 5971 | 30.0 | 350 | 1000 | 40.5 | 2.86 | 59.4 |
| 100.0 | 5972 | 35.0 | 350 | 1000 | 47.3 | 2.86 | 46.8 |
| 100.0 | 5975 | 35.0 | 350 | 1050 | 49.0 | 3.00 | 48.0 |
| 100.0 | 5978 | 35.0 | 350 | 1100 | 50.8 | 3.14 | 49.2 |
| 100.0 | 5979 | 40.0 | 350 | 1100 | 58.0 | 3.14 | 41.0 |
| 100.0 | 5981 | 35.0 | 350 | 1150 | 52.5 | 3.29 | 50.3 |
| 100.0 | 5982 | 40.0 | 350 | 1150 | 60.0 | 3.29 | 42.1 |
| 100.0 | 5984 | 35.0 | 350 | 1200 | 54.3 | 3.43 | 51.4 |
| 100.0 | 5985 | 40.0 | 350 | 1200 | 62.0 | 3.43 | 43.1 |
| 100.0 | 5987 | 35.0 | 350 | 1250 | 56.0 | 3.57 | 52.4 |
| 100.0 | 5988 | 40.0 | 350 | 1250 | 64.0 | 3.57 | 44.1 |
| 100.0 | 5990 | 35.0 | 350 | 1300 | 57.8 | 3.71 | 53.4 |
| 100.0 | 5991 | 40.0 | 350 | 1300 | 66.0 | 3.71 | 45.0 |
| 100.0 | 5993 | 35.0 | 350 | 1350 | 59.5 | 3.86 | 54.3 |
| 100.0 | 5994 | 40.0 | 350 | 1350 | 68.0 | 3.86 | 45.9 |
| 100.0 | 5996 | 35.0 | 350 | 1400 | 61.3 | 4.00 | 55.1 |
| 100.0 | 5997 | 40.0 | 350 | 1400 | 70.0 | 4.00 | 46.8 |
| 100.0 | 5999 | 35.0 | 350 | 1450 | 63.0 | 4.14 | 56.0 |
| 100.0 | 6000 | 40.0 | 350 | 1450 | 72.0 | 4.14 | 47.6 |
| 100.0 | 6002 | 35.0 | 350 | 1500 | 64.8 | 4.29 | 56.8 |
| 100.0 | 6003 | 40.0 | 350 | 1500 | 74.0 | 4.29 | 48.3 |
| 100.0 | 6005 | 35.0 | 350 | 1550 | 66.5 | 4.43 | 57.5 |
| 100.0 | 6006 | 40.0 | 350 | 1550 | 76.0 | 4.43 | 49.1 |
| 100.0 | 6008 | 35.0 | 350 | 1600 | 68.3 | 4.57 | 58.3 |
| 100.0 | 6009 | 40.0 | 350 | 1600 | 78.0 | 4.57 | 49.8 |
| 100.0 | 6011 | 35.0 | 350 | 1650 | 70.0 | 4.71 | 59.0 |
| 100.0 | 6012 | 40.0 | 350 | 1650 | 80.0 | 4.71 | 50.5 |
| 100.0 | 6014 | 35.0 | 350 | 1700 | 71.8 | 4.86 | 59.7 |
| 100.0 | 6015 | 40.0 | 350 | 1700 | 82.0 | 4.86 | 51.1 |
| 100.0 | 6018 | 40.0 | 350 | 1750 | 84.0 | 5.00 | 51.8 |
| 100.0 | 6021 | 40.0 | 350 | 1800 | 86.0 | 5.14 | 52.4 |
| 100.0 | 6024 | 40.0 | 350 | 1850 | 88.0 | 5.29 | 53.0 |
| 100.0 | 6027 | 40.0 | 350 | 1900 | 90.0 | 5.43 | 53.6 |
| 100.0 | 6030 | 40.0 | 350 | 1950 | 92.0 | 5.57 | 54.1 |
| 100.0 | 6033 | 40.0 | 350 | 2000 | 94.0 | 5.71 | 54.7 |
| 100.0 | 6036 | 40.0 | 350 | 2050 | 96.0 | 5.86 | 55.2 |
| 100.0 | 6039 | 40.0 | 350 | 2100 | 98.0 | 6.00 | 55.7 |
| 100.0 | 6042 | 40.0 | 350 | 2150 | 100.0 | 6.14 | 56.2 |
| 100.0 | 6045 | 40.0 | 350 | 2200 | 102.0 | 6.29 | 56.7 |
| 100.0 | 6048 | 40.0 | 350 | 2250 | 104.0 | 6.43 | 57.2 |
| 100.0 | 6051 | 40.0 | 350 | 2300 | 106.0 | 6.57 | 57.6 |
| 100.0 | 6054 | 40.0 | 350 | 2350 | 108.0 | 6.71 | 58.1 |
| 100.0 | 6057 | 40.0 | 350 | 2400 | 110.0 | 6.86 | 58.5 |

Continued on next page

Table B.6 – *Continued from previous page*

| V_{DD} (mV) | Point | L (nm) | NW (nm) | PW (nm) | Area (fm ²) | Size ratio ($\frac{m}{m}$) | SP _x (mV) |
|------------------|-------|-----------|------------|------------|----------------------------|---------------------------------|-------------------------|
| 100.0 | 6060 | 40.0 | 350 | 2450 | 112.0 | 7.00 | 59.0 |
| 100.0 | 6063 | 40.0 | 350 | 2500 | 114.0 | 7.14 | 59.4 |
| 100.0 | 6088 | 30.0 | 400 | 600 | 30.0 | 1.50 | 40.2 |
| 100.0 | 6091 | 30.0 | 400 | 650 | 31.5 | 1.63 | 43.0 |
| 100.0 | 6094 | 30.0 | 400 | 700 | 33.0 | 1.75 | 45.4 |
| 100.0 | 6097 | 30.0 | 400 | 750 | 34.5 | 1.88 | 47.7 |
| 100.0 | 6100 | 30.0 | 400 | 800 | 36.0 | 2.00 | 49.7 |
| 100.0 | 6103 | 30.0 | 400 | 850 | 37.5 | 2.13 | 51.5 |
| 100.0 | 6106 | 30.0 | 400 | 900 | 39.0 | 2.25 | 53.2 |
| 100.0 | 6107 | 35.0 | 400 | 900 | 45.5 | 2.25 | 40.8 |
| 100.0 | 6109 | 30.0 | 400 | 950 | 40.5 | 2.38 | 54.8 |
| 100.0 | 6110 | 35.0 | 400 | 950 | 47.3 | 2.38 | 42.3 |
| 100.0 | 6112 | 30.0 | 400 | 1000 | 42.0 | 2.50 | 56.3 |
| 100.0 | 6113 | 35.0 | 400 | 1000 | 49.0 | 2.50 | 43.7 |
| 100.0 | 6115 | 30.0 | 400 | 1050 | 43.5 | 2.63 | 57.7 |
| 100.0 | 6116 | 35.0 | 400 | 1050 | 50.8 | 2.63 | 45.0 |
| 100.0 | 6118 | 30.0 | 400 | 1100 | 45.0 | 2.75 | 59.0 |

B.2 Gate balance

Table B.7: The power and delay in the ring oscillator constructed of three 2T inverters. Results of transient analyses

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 73.0 | 40.0 | 200 | 1700 | | | 19.7 | 2.73 |
| 73.0 | 40.0 | 200 | 1750 | | | 19.8 | 2.76 |
| 73.0 | 40.0 | 200 | 1800 | | | 19.8 | 2.70 |
| 73.0 | 40.0 | 200 | 1850 | | | 19.8 | 2.79 |
| 73.0 | 40.0 | 200 | 1900 | | | 19.9 | 2.85 |
| 73.0 | 40.0 | 200 | 1950 | | | 20.0 | 2.82 |
| 73.0 | 40.0 | 200 | 2000 | | | 20.0 | 2.66 |
| 73.0 | 40.0 | 200 | 2050 | | | 20.1 | 2.63 |
| 73.0 | 40.0 | 200 | 2100 | | | 20.2 | 3.14 |
| 73.0 | 40.0 | 200 | 2150 | | | 20.2 | 2.16 |
| 73.0 | 40.0 | 200 | 2200 | | | 20.3 | 2.19 |
| 73.0 | 40.0 | 200 | 2250 | | | 20.4 | 2.12 |
| 73.0 | 40.0 | 200 | 2300 | | | 20.4 | 2.22 |
| 73.0 | 40.0 | 200 | 2350 | | | 20.5 | 2.60 |
| 73.0 | 40.0 | 200 | 2400 | | | 20.6 | 2.25 |
| 73.0 | 40.0 | 200 | 2450 | | | 20.6 | 2.28 |
| 73.0 | 40.0 | 200 | 2500 | | | 20.7 | 2.31 |
| 73.0 | 40.0 | 250 | 2100 | | | 20.8 | 2.09 |
| 73.0 | 40.0 | 250 | 2150 | | | 20.8 | 2.06 |
| 73.0 | 40.0 | 250 | 2200 | | | 20.9 | 2.34 |
| 73.0 | 40.0 | 250 | 2250 | | | 21.0 | 2.37 |
| 73.0 | 40.0 | 250 | 2300 | | | 21.3 | 2.40 |
| 73.0 | 40.0 | 250 | 2350 | | | 21.3 | 2.42 |
| 73.0 | 40.0 | 250 | 2400 | | | 21.4 | 2.45 |
| 73.0 | 40.0 | 250 | 2450 | | | 21.7 | 2.48 |
| 73.0 | 40.0 | 250 | 2500 | | | 21.7 | 2.50 |
| 73.0 | 40.0 | 300 | 2500 | | | 22.1 | 2.53 |
| 79.0 | 40.0 | 200 | 2250 | 18.2 | 18.0 | 18.1 | 2.98 |
| 79.0 | 40.0 | 200 | 2300 | 18.4 | 18.4 | 18.4 | 3.01 |
| 79.0 | 40.0 | 200 | 2350 | 18.5 | 18.4 | 18.5 | 3.05 |
| 79.0 | 40.0 | 200 | 2400 | 18.6 | 18.6 | 18.6 | 3.08 |
| 108 | 40.0 | 200 | 2150 | 9.32 | 9.32 | 9.32 | 8.35 |
| 108 | 40.0 | 200 | 2200 | 9.40 | 9.40 | 9.40 | 8.45 |

Table B.8: The power and delay in the ring oscillator constructed of three 4T inverters. Results of transient analyses

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 71.0 | 40.0 | 200 | 2000 | | | 72.7 | 1.04 |
| 71.0 | 40.0 | 200 | 2050 | | | 73.1 | 1.05 |
| 71.0 | 40.0 | 200 | 2100 | | | 74.1 | 1.07 |
| 71.0 | 40.0 | 200 | 2150 | | | 74.5 | 1.08 |
| 71.0 | 40.0 | 200 | 2200 | | | 75.0 | 1.09 |
| 71.0 | 40.0 | 200 | 2250 | | | 75.9 | 1.11 |
| 71.0 | 40.0 | 200 | 2300 | | | 76.5 | 1.12 |
| 71.0 | 40.0 | 200 | 2350 | | | 77.0 | 1.13 |
| 71.0 | 40.0 | 200 | 2400 | | | 77.1 | 1.15 |
| 71.0 | 40.0 | 200 | 2450 | | | 78.9 | 1.16 |
| 71.0 | 40.0 | 200 | 2500 | | | 79.3 | 1.17 |
| 71.0 | 40.0 | 250 | 2100 | | | 71.3 | 1.20 |
| 71.0 | 40.0 | 250 | 2150 | | | 72.0 | 1.21 |
| 71.0 | 40.0 | 250 | 2200 | | | 71.6 | 1.23 |
| 71.0 | 40.0 | 250 | 2250 | | | 70.7 | 1.25 |
| 71.0 | 40.0 | 250 | 2300 | | | 70.6 | 1.26 |
| 71.0 | 40.0 | 250 | 2350 | | | 70.0 | 1.28 |
| 71.0 | 40.0 | 250 | 2400 | | | 70.7 | 1.29 |
| 71.0 | 40.0 | 250 | 2450 | | | 70.9 | 1.30 |
| 71.0 | 40.0 | 250 | 2500 | | | 71.0 | 1.32 |
| 71.0 | 40.0 | 300 | 2500 | | | 78.6 | 1.45 |
| 78.0 | 40.0 | 200 | 1950 | 59.8 | 59.8 | 59.8 | 1.32 |
| 78.0 | 40.0 | 200 | 2000 | 60.3 | 60.3 | 60.3 | 1.34 |
| 78.0 | 40.0 | 200 | 2050 | 60.9 | 60.9 | 60.9 | 1.36 |
| 78.0 | 40.0 | 200 | 2100 | 61.4 | 61.4 | 61.4 | 1.37 |
| 78.0 | 40.0 | 200 | 2150 | 61.9 | 61.9 | 61.9 | 1.39 |
| 78.0 | 40.0 | 200 | 2200 | 62.4 | 62.4 | 62.4 | 1.41 |
| 78.0 | 40.0 | 200 | 2250 | 62.9 | 62.9 | 62.9 | 1.43 |
| 78.0 | 40.0 | 200 | 2300 | 63.4 | 63.4 | 63.4 | 1.44 |
| 78.0 | 40.0 | 200 | 2350 | 63.9 | 63.9 | 63.9 | 1.46 |
| 78.0 | 40.0 | 200 | 2400 | 64.4 | 64.4 | 64.4 | 1.47 |
| 78.0 | 40.0 | 200 | 2450 | 65.0 | 65.0 | 65.0 | 1.49 |
| 78.0 | 40.0 | 200 | 2500 | 65.5 | 65.5 | 65.5 | 1.51 |
| 78.0 | 40.0 | 250 | 2450 | 58.6 | 58.6 | 58.6 | 1.68 |
| 78.0 | 40.0 | 250 | 2500 | 59.0 | 59.0 | 59.0 | 1.70 |
| 104.0 | 40.0 | 200 | 1950 | 32.6 | 33.3 | 32.9 | 3.37 |
| 104.0 | 40.0 | 200 | 2000 | 33.3 | 32.5 | 32.9 | 3.42 |
| 104.0 | 40.0 | 200 | 2050 | 33.6 | 32.8 | 33.2 | 3.46 |
| 104.0 | 40.0 | 250 | 2450 | 31.9 | 32.5 | 32.2 | 4.29 |
| 104.0 | 40.0 | 250 | 2500 | 31.9 | 32.5 | 32.2 | 4.34 |

Table B.9: The power and delay in the ring oscillator constructed of three 4T NAND2 gates. Results of transient analyses

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 73.0 | 40.0 | 200 | 750 | | | 30.4 | 1.30 |
| 73.0 | 40.0 | 200 | 700 | | | 30.5 | 1.24 |
| 73.0 | 40.0 | 200 | 800 | | | 31.2 | 1.34 |
| 73.0 | 40.0 | 200 | 850 | | | 31.9 | 1.39 |
| 73.0 | 40.0 | 250 | 850 | | | 28.9 | 1.57 |
| 73.0 | 40.0 | 250 | 900 | | | 29.2 | 1.62 |
| 73.0 | 40.0 | 250 | 950 | | | 29.6 | 1.67 |
| 73.0 | 40.0 | 250 | 1000 | | | 29.9 | 1.72 |
| 73.0 | 40.0 | 250 | 1050 | | | 30.3 | 1.77 |
| 73.0 | 40.0 | 250 | 1100 | | | 30.4 | 1.81 |
| 73.0 | 40.0 | 300 | 950 | | | 27.6 | 1.85 |
| 73.0 | 40.0 | 300 | 1000 | | | 27.8 | 1.90 |
| 73.0 | 40.0 | 300 | 1050 | | | 28.1 | 1.96 |
| 73.0 | 40.0 | 300 | 1100 | | | 28.4 | 2.01 |
| 73.0 | 40.0 | 300 | 1150 | | | 28.8 | 2.06 |
| 73.0 | 40.0 | 300 | 1200 | | | 28.9 | 2.10 |
| 73.0 | 40.0 | 300 | 1250 | | | 29.4 | 2.15 |
| 73.0 | 40.0 | 300 | 1300 | | | 29.6 | 2.19 |
| 73.0 | 40.0 | 350 | 1100 | | | 26.9 | 2.18 |
| 73.0 | 40.0 | 350 | 1150 | | | 27.1 | 2.23 |
| 73.0 | 40.0 | 350 | 1200 | | | 27.3 | 2.29 |
| 73.0 | 40.0 | 350 | 1250 | | | 27.6 | 2.34 |
| 73.0 | 40.0 | 350 | 1300 | | | 27.9 | 2.39 |
| 73.0 | 40.0 | 350 | 1350 | | | 28.1 | 2.44 |
| 73.0 | 40.0 | 350 | 1400 | | | 28.3 | 2.48 |
| 73.0 | 40.0 | 350 | 1450 | | | 28.7 | 2.53 |
| 73.0 | 40.0 | 350 | 1500 | | | 29.2 | 2.57 |
| 73.0 | 40.0 | 350 | 1550 | | | 29.4 | 2.62 |
| 73.0 | 40.0 | 400 | 1250 | | | 26.3 | 2.51 |
| 73.0 | 40.0 | 400 | 1300 | | | 26.6 | 2.57 |
| 73.0 | 40.0 | 400 | 1350 | | | 26.7 | 2.62 |
| 73.0 | 40.0 | 400 | 1400 | | | 27.0 | 2.67 |
| 73.0 | 40.0 | 400 | 1450 | | | 27.2 | 2.72 |
| 73.0 | 40.0 | 400 | 1500 | | | 27.6 | 2.77 |
| 73.0 | 40.0 | 400 | 1550 | | | 27.7 | 2.82 |
| 73.0 | 40.0 | 400 | 1600 | | | 28.1 | 2.86 |
| 73.0 | 40.0 | 400 | 1650 | | | 28.4 | 2.91 |
| 73.0 | 40.0 | 400 | 1700 | | | 28.8 | 2.95 |
| 73.0 | 40.0 | 400 | 1750 | | | 29.7 | 3.00 |
| 73.0 | 40.0 | 400 | 1800 | | | 76.7 | 3.04 |
| 73.0 | 40.0 | 450 | 1400 | | | 25.9 | 2.84 |
| 73.0 | 40.0 | 450 | 1450 | | | 26.2 | 2.90 |
| 73.0 | 40.0 | 450 | 1500 | | | 26.2 | 2.95 |
| 73.0 | 40.0 | 450 | 1550 | | | 26.6 | 3.00 |

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Table B.9 – *Continued from previous page*

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 73.0 | 40.0 | 450 | 1600 | | | 26.8 | 3.05 |
| 73.0 | 40.0 | 450 | 1650 | | | 27.0 | 3.10 |
| 73.0 | 40.0 | 450 | 1700 | | | 27.2 | 3.15 |
| 73.0 | 40.0 | 450 | 1750 | | | 27.5 | 3.20 |
| 73.0 | 40.0 | 450 | 1800 | | | 28.0 | 3.25 |
| 73.0 | 40.0 | 450 | 1850 | | | 28.0 | 3.29 |
| 73.0 | 40.0 | 450 | 1900 | | | 28.2 | 3.34 |
| 73.0 | 40.0 | 450 | 1950 | | | 28.7 | 3.38 |
| 73.0 | 40.0 | 450 | 2000 | | | 29.0 | 3.42 |
| 73.0 | 40.0 | 450 | 1350 | | | 63.5 | 2.79 |
| 73.0 | 40.0 | 500 | 1550 | | | 25.4 | 3.17 |
| 73.0 | 40.0 | 500 | 1500 | | | 25.4 | 3.12 |
| 73.0 | 40.0 | 500 | 2250 | | | 25.6 | 3.85 |
| 73.0 | 40.0 | 500 | 1600 | | | 26.0 | 3.23 |
| 73.0 | 40.0 | 500 | 1650 | | | 26.1 | 3.28 |
| 73.0 | 40.0 | 500 | 1700 | | | 26.3 | 3.33 |
| 73.0 | 40.0 | 500 | 1750 | | | 26.4 | 3.39 |
| 73.0 | 40.0 | 500 | 1800 | | | 26.6 | 3.44 |
| 73.0 | 40.0 | 500 | 1850 | | | 26.7 | 3.49 |
| 73.0 | 40.0 | 500 | 1900 | | | 27.1 | 3.53 |
| 73.0 | 40.0 | 500 | 1950 | | | 27.4 | 3.58 |
| 73.0 | 40.0 | 500 | 2050 | | | 27.6 | 3.67 |
| 73.0 | 40.0 | 500 | 2000 | | | 27.7 | 3.63 |
| 73.0 | 40.0 | 500 | 2100 | | | 28.0 | 3.72 |
| 73.0 | 40.0 | 500 | 2200 | | | 28.4 | 3.80 |
| 73.0 | 40.0 | 500 | 2150 | | | 28.5 | 3.76 |
| 73.0 | 40.0 | 550 | 1650 | | | 25.1 | 3.45 |
| 73.0 | 40.0 | 550 | 1700 | | | 25.5 | 3.51 |
| 73.0 | 40.0 | 550 | 1750 | | | 25.6 | 3.56 |
| 73.0 | 40.0 | 550 | 1850 | | | 25.8 | 3.67 |
| 73.0 | 40.0 | 550 | 1800 | | | 25.8 | 3.61 |
| 73.0 | 40.0 | 550 | 1900 | | | 26.0 | 3.72 |
| 73.0 | 40.0 | 550 | 1950 | | | 26.3 | 3.77 |
| 73.0 | 40.0 | 550 | 2000 | | | 26.4 | 3.82 |
| 73.0 | 40.0 | 550 | 2050 | | | 26.6 | 3.87 |
| 73.0 | 40.0 | 550 | 2100 | | | 27.0 | 3.92 |
| 73.0 | 40.0 | 550 | 2150 | | | 27.1 | 3.96 |
| 73.0 | 40.0 | 550 | 2250 | | | 27.4 | 4.05 |
| 73.0 | 40.0 | 550 | 2200 | | | 27.4 | 4.01 |
| 73.0 | 40.0 | 550 | 2300 | | | 27.7 | 4.10 |
| 73.0 | 40.0 | 550 | 2400 | | | 28.1 | 4.19 |
| 73.0 | 40.0 | 550 | 2350 | | | 28.2 | 4.14 |
| 73.0 | 40.0 | 550 | 2450 | | | 28.7 | 4.23 |
| 73.0 | 40.0 | 600 | 1800 | | | 24.9 | 3.78 |
| 73.0 | 40.0 | 600 | 1850 | | | 25.1 | 3.84 |
| 73.0 | 40.0 | 600 | 1900 | | | 25.3 | 3.89 |

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Table B.9 – *Continued from previous page*

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 73.0 | 40.0 | 600 | 1950 | | | 25.3 | 3.95 |
| 73.0 | 40.0 | 600 | 2000 | | | 25.5 | 4.00 |
| 73.0 | 40.0 | 600 | 2050 | | | 25.7 | 4.05 |
| 73.0 | 40.0 | 600 | 2100 | | | 25.9 | 4.10 |
| 73.0 | 40.0 | 600 | 2150 | | | 26.2 | 4.15 |
| 73.0 | 40.0 | 600 | 2200 | | | 26.3 | 4.20 |
| 73.0 | 40.0 | 600 | 2250 | | | 26.4 | 4.25 |
| 73.0 | 40.0 | 600 | 2300 | | | 26.5 | 4.30 |
| 73.0 | 40.0 | 600 | 2350 | | | 26.8 | 4.34 |
| 73.0 | 40.0 | 600 | 2450 | | | 27.2 | 4.44 |
| 73.0 | 40.0 | 600 | 2400 | | | 27.3 | 4.39 |
| 73.0 | 40.0 | 600 | 2500 | | | 27.5 | 4.48 |
| 73.0 | 40.0 | 650 | 1900 | | | 24.6 | 4.06 |
| 73.0 | 40.0 | 650 | 1950 | | | 24.6 | 4.11 |
| 73.0 | 40.0 | 650 | 2050 | | | 24.9 | 4.23 |
| 73.0 | 40.0 | 650 | 2000 | | | 25.1 | 4.17 |
| 73.0 | 40.0 | 650 | 2100 | | | 25.3 | 4.28 |
| 73.0 | 40.0 | 650 | 2200 | | | 25.5 | 4.38 |
| 73.0 | 40.0 | 650 | 2150 | | | 25.5 | 4.33 |
| 73.0 | 40.0 | 650 | 2250 | | | 25.7 | 4.43 |
| 73.0 | 40.0 | 650 | 2300 | | | 25.9 | 4.49 |
| 73.0 | 40.0 | 650 | 2350 | | | 26.1 | 4.53 |
| 73.0 | 40.0 | 650 | 2400 | | | 26.2 | 4.58 |
| 73.0 | 40.0 | 650 | 2450 | | | 26.4 | 4.63 |
| 73.0 | 40.0 | 650 | 2500 | | | 26.4 | 4.68 |
| 73.0 | 40.0 | 700 | 2050 | | | 24.6 | 4.39 |
| 73.0 | 40.0 | 700 | 2100 | | | 24.7 | 4.45 |
| 73.0 | 40.0 | 700 | 2200 | | | 24.8 | 4.56 |
| 73.0 | 40.0 | 700 | 2150 | | | 25.1 | 4.50 |
| 73.0 | 40.0 | 700 | 2300 | | | 25.1 | 4.66 |
| 73.0 | 40.0 | 700 | 2250 | | | 25.2 | 4.61 |
| 73.0 | 40.0 | 700 | 2350 | | | 25.4 | 4.72 |
| 73.0 | 40.0 | 700 | 2400 | | | 25.6 | 4.77 |
| 73.0 | 40.0 | 700 | 2450 | | | 25.7 | 4.82 |
| 73.0 | 40.0 | 700 | 2500 | | | 25.8 | 4.87 |
| 73.0 | 40.0 | 750 | 2200 | | | 24.3 | 4.72 |
| 73.0 | 40.0 | 750 | 2250 | | | 24.6 | 4.78 |
| 73.0 | 40.0 | 750 | 2300 | | | 24.8 | 4.84 |
| 73.0 | 40.0 | 750 | 2350 | | | 24.8 | 4.89 |
| 73.0 | 40.0 | 750 | 2400 | | | 24.9 | 4.94 |
| 73.0 | 40.0 | 750 | 2450 | | | 25.0 | 5.00 |
| 73.0 | 40.0 | 750 | 2500 | | | 25.1 | 5.05 |
| 73.0 | 40.0 | 750 | 2150 | | | 60.1 | 4.67 |
| 73.0 | 40.0 | 800 | 2400 | | | 24.4 | 5.11 |
| 73.0 | 40.0 | 800 | 2350 | | | 24.5 | 5.06 |
| 73.0 | 40.0 | 800 | 2450 | | | 24.5 | 5.17 |

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Table B.9 – *Continued from previous page*

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 73.0 | 40.0 | 800 | 2300 | | | 24.8 | 5.00 |
| 73.0 | 40.0 | 800 | 2500 | | | 24.9 | 5.22 |
| 78.0 | 40.0 | 450 | 1400 | 22.6 | 23.2 | 22.88 | 3.40 |
| 78.0 | 40.0 | 500 | 1550 | 22.5 | 23.0 | 22.745 | 3.80 |
| 78.0 | 40.0 | 550 | 1700 | 22.5 | 22.6 | 22.545 | 4.20 |
| 78.0 | 40.0 | 550 | 1750 | 22.9 | 22.6 | 22.76 | 4.27 |
| 78.0 | 40.0 | 600 | 1850 | 22.3 | 22.1 | 22.155 | 4.60 |
| 78.0 | 40.0 | 650 | 2000 | 22.2 | 22.2 | 22.19 | 5.00 |
| 78.0 | 40.0 | 700 | 2150 | 21.6 | 21.9 | 21.735 | 5.39 |
| 78.0 | 40.0 | 750 | 2350 | 22.1 | 21.7 | 21.885 | 5.86 |
| 78.0 | 40.0 | 750 | 2300 | 21.9 | 21.9 | 21.915 | 5.79 |
| 78.0 | 40.0 | 800 | 2400 | 21.7 | 21.8 | 21.73 | 6.12 |
| 78.0 | 40.0 | 800 | 2450 | 21.8 | 21.8 | 21.825 | 6.19 |
| 78.0 | 40.0 | 800 | 2500 | 22.0 | 21.9 | 21.935 | 6.26 |
| 106 | 40.0 | 300 | 950 | 13.3 | 12.9 | 13.1 | 6.11 |
| 106 | 40.0 | 350 | 1050 | 12.5 | 12.4 | 12.5 | 7.02 |
| 106 | 40.0 | 400 | 1200 | 12.2 | 12.5 | 12.3 | 8.12 |
| 106 | 40.0 | 450 | 1350 | 12.3 | 12.0 | 12.1 | 9.21 |
| 106 | 40.0 | 500 | 1450 | 12.0 | 11.7 | 11.8 | 10.1 |
| 106 | 40.0 | 500 | 1500 | 12.1 | 12.0 | 12.1 | 10.3 |
| 106 | 40.0 | 550 | 1600 | 11.7 | 12.0 | 11.8 | 11.2 |
| 106 | 40.0 | 550 | 1650 | 12.0 | 11.7 | 11.9 | 11.4 |
| 106 | 40.0 | 600 | 1800 | 11.5 | 11.8 | 11.7 | 12.5 |
| 106 | 40.0 | 600 | 1750 | 11.7 | 11.8 | 11.7 | 12.3 |
| 106 | 40.0 | 650 | 1900 | 11.7 | 11.6 | 11.7 | 13.4 |
| 106 | 40.0 | 700 | 2000 | 11.5 | 11.6 | 11.5 | 14.3 |
| 106 | 40.0 | 700 | 2050 | 11.6 | 11.5 | 11.6 | 14.5 |
| 106 | 40.0 | 700 | 1950 | 11.5 | 11.7 | 11.6 | 14.1 |
| 106 | 40.0 | 700 | 2100 | 11.9 | 11.7 | 11.8 | 14.7 |
| 106 | 40.0 | 750 | 2150 | 11.5 | 11.3 | 11.4 | 15.4 |
| 106 | 40.0 | 750 | 2200 | 11.4 | 11.7 | 11.5 | 15.6 |
| 106 | 40.0 | 750 | 2250 | 11.8 | 11.6 | 11.7 | 15.8 |
| 106 | 40.0 | 800 | 2300 | 11.3 | 11.6 | 11.4 | 16.5 |
| 106 | 40.0 | 800 | 2250 | 11.4 | 11.5 | 11.5 | 16.3 |
| 106 | 40.0 | 800 | 2350 | 11.5 | 11.5 | 11.5 | 16.7 |
| 106 | 40.0 | 800 | 2400 | 11.6 | 11.6 | 11.6 | 16.9 |

Table B.10: The power and delay in the ring oscillator constructed of three 8T NAND2 gates. Results of transient analyses

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 73.0 | 40.0 | 300 | 1950 | | | 62.1 | 2.70 |
| 73.0 | 40.0 | 300 | 2000 | | | 60.3 | 2.74 |
| 73.0 | 40.0 | 300 | 2050 | | | 59.5 | 2.78 |
| 73.0 | 40.0 | 300 | 2100 | | | 59.3 | 2.82 |
| 73.0 | 40.0 | 300 | 2150 | | | 59.6 | 2.86 |
| 73.0 | 40.0 | 300 | 2200 | | | 59.9 | 2.90 |
| 73.0 | 40.0 | 300 | 2250 | | | 60.0 | 2.93 |
| 78.0 | 40.0 | 200 | 1950 | 59.8 | 59.8 | 59.8 | 2.64 |
| 78.0 | 40.0 | 250 | 2450 | 58.6 | 58.6 | 58.6 | 3.36 |
| 78.0 | 40.0 | 250 | 2500 | 59.0 | 59.0 | 59.0 | 3.39 |
| 104 | 40.0 | 200 | 1950 | 33.3 | 32.6 | 32.9 | 6.75 |
| 104 | 40.0 | 250 | 2450 | 32.5 | 31.9 | 32.2 | 8.59 |
| 104 | 40.0 | 250 | 2500 | 32.5 | 32.7 | 32.6 | 8.68 |

Table B.11: The power and delay in the ring oscillator constructed of three 4T NOR2 gates. Results of transient analyses

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 75.0 | 35.0 | 200 | 3100 | | | 22.0 | 8.79 |
| 75.0 | 35.0 | 200 | 3150 | | | 22.2 | 8.87 |
| 75.0 | 35.0 | 200 | 3400 | | | 15.6 | 9.27 |
| 75.0 | 35.0 | 200 | 3450 | | | 15.1 | 9.35 |
| 75.0 | 35.0 | 200 | 3500 | | | 15.3 | 9.43 |
| 75.0 | 35.0 | 200 | 3550 | | | 15.0 | 9.50 |
| 75.0 | 35.0 | 200 | 3600 | | | 15.1 | 9.58 |
| 75.0 | 35.0 | 200 | 3650 | | | 15.0 | 9.65 |
| 75.0 | 35.0 | 200 | 3700 | | | 15.2 | 9.73 |
| 75.0 | 35.0 | 200 | 3750 | | | 15.2 | 9.80 |
| 75.0 | 35.0 | 200 | 3800 | | | 15.2 | 9.87 |
| 75.0 | 35.0 | 200 | 3850 | | | 15.3 | 9.95 |
| 75.0 | 35.0 | 200 | 3900 | | | 15.3 | 10.0 |
| 75.0 | 35.0 | 200 | 3950 | | | 15.4 | 10.1 |
| 75.0 | 35.0 | 200 | 4000 | | | 15.5 | 10.2 |
| 75.0 | 35.0 | 250 | 3900 | | | 21.9 | 11.2 |
| 75.0 | 35.0 | 250 | 3950 | | | 21.7 | 11.3 |
| 86.0 | 35.0 | 200 | 3750 | 12.0 | 11.9 | 11.9 | 13.8 |
| 86.0 | 35.0 | 200 | 3800 | 12.0 | 12.0 | 12.0 | 13.9 |
| 86.0 | 35.0 | 200 | 3850 | 12.1 | 12.2 | 12.1 | 14.0 |
| 86.0 | 35.0 | 200 | 3900 | 12.1 | 12.1 | 12.1 | 14.1 |
| 86.0 | 35.0 | 200 | 3950 | 12.2 | 12.3 | 12.2 | 14.2 |
| 86.0 | 35.0 | 200 | 4000 | 12.3 | 12.2 | 12.2 | 14.3 |
| 115 | 35.0 | 200 | 3950 | 6.42 | 6.53 | 6.48 | 38.8 |

Table B.12: The power and delay in the ring oscillator constructed of three 8T NOR2 gates. Results of transient analyses

| V_{DD} (mV) | L (nm) | NW (nm) | PW (nm) | delay_Low (μ s) | delay_high (μ s) | Mean delay (μ s) | power (pW) |
|------------------|-----------|------------|------------|-------------------------|--------------------------|--------------------------|---------------|
| 73.0 | 40.0 | 300 | 1950 | | | 62.1 | 2.70 |
| 73.0 | 40.0 | 300 | 2000 | | | 60.3 | 2.74 |
| 73.0 | 40.0 | 300 | 2050 | | | 59.5 | 2.78 |
| 73.0 | 40.0 | 300 | 2100 | | | 59.3 | 2.82 |
| 73.0 | 40.0 | 300 | 2150 | | | 59.6 | 2.86 |
| 73.0 | 40.0 | 300 | 2200 | | | 59.9 | 2.90 |
| 73.0 | 40.0 | 300 | 2250 | | | 60.0 | 2.93 |
| 78.0 | 40.0 | 200 | 1950 | 59.8 | 59.8 | 59.8 | 2.64 |
| 78.0 | 40.0 | 250 | 2450 | 58.6 | 58.6 | 58.6 | 3.36 |
| 78.0 | 40.0 | 250 | 2500 | 59.0 | 59.0 | 59.0 | 3.39 |
| 104 | 40.0 | 200 | 1950 | 33.3 | 32.6 | 32.9 | 6.75 |
| 104 | 40.0 | 250 | 2450 | 32.5 | 31.9 | 32.2 | 8.59 |
| 104 | 40.0 | 250 | 2500 | 32.5 | 32.7 | 32.6 | 8.68 |

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