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A 65nm CMOS Front-end LNA for Medical Ultrasound Imaging with Feedback Employing Noise and Distortion Cancellation

Jon Håvard Eriksrød

Electronics Engineering
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Supervisor: Trond Ytterdal, IET

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

MASTER THESIS

Circuit and System Design

A 65nm CMOS Front-end LNA for Medical Ultrasound Imaging with Feedback Employing Noise and Distortion Cancellation

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Abstract

A high performance $67.2\mu W$ low power front-end Low Noise Amplifier (LNA) for ultrasound applications is proposed. The amplifier utilizes a balun based on a common-gate (CG) and a common-source (CS) combination. The CS-amplifier performs error correction, and thus cancels distortion and noise from the CG-amplifier. The proposed design introduces a GM-boosted CG-amplifier for further linearization and HD2-supression. Furthermore, a programmable-gain scheme has been introduced. The amplifier is tailored towards a capacitive micro machined ultrasonic transducer (CMUT), with an impedance of $10k\angle -60°$ at a center of frequency 5MHz.

Layout for the amplifier is created, and the LNA is design and simulated under 65nm CMOS including layout effects. Consequently, achieving a noise figure (NF) of only 2.98dB with a total power consumption of only $67.2\mu W$, with an input impedance of $3.8k\Omega$.

The final design sports a dynamic range (DR) of 50.35dB. Total harmonic distortion is simulated to -62.43dB with an IM3 of -41.47dB and HD2 of -56.63dB.

Sammendrag

En 65nm CMOS lavstøyforsterke for medisinsk ultralyd er foreslått. Forsterkeren nytter seg av en balun topologi bestående av et felles-source (CS) og et felles-gate (CG) trinn. Et CS-trinn utfører feil korreksjon av CG-trinnet. Følgelig blir både forvrengning og termisk/fliker-støy som har sitt opphavet i CG-transistoren kansellert, og den totale ytinga er uavhengig av CG-trinnet. Den foreslåtte forsterkeren nytter et GM-boostet CG-trinn for økt HD2-undertrykking. Videre er programmerbar forsterking introdusert. Forsterkeren er skreddersyd capacitive micro machined ultrasonic transducer (CMUT), med en impedans ved $10k\angle -60°$ ved en senterfrekvens av 5MHz.

Et 65nm utlegg er laget og forsterkaren er simulert med tilleggseffekter fra utlegget. Det oppnåes en støyfigur ved 2.98dB ved eit total strœmforbruk ved $67.2\mu W$. Videre blir det simulerte dynamisk område lik 50.35dB, med en total harmonisk forvrenging lik -62.43dB, og dessuten en IM3 ved -41.47dB og HD2 ved -56.63dB.

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Acknowledgements

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Moreover, i would like to express my deepest gratitude to both new and old classmates. Finally, P.B. Andersen for making noise predominantly interesting.

"May your TROUBLES be middle-sized so that you can find them" - Bob Pease

CHAPTER 1

Introduction

The main objective for this thesis is a low noise low power medical ultrasound front-end amplifier for CMUT. The proposed amplifier is based on a CGCS-Balun, but includes a gm-boosted CG-stage as HD2 suppression. The amplifier employs thermal/flicker-noise and distortion cancellation. Moreover, a programmable gain scheme is proposed.

1.1 Motivation

Ultrasonic-imaging plays an important role in todays modern medicine. Contrary to X-ray imaging, ultrasound medical imaging has an impeccable safety record, it is cost efficient and has the ability to perform real time imaging.

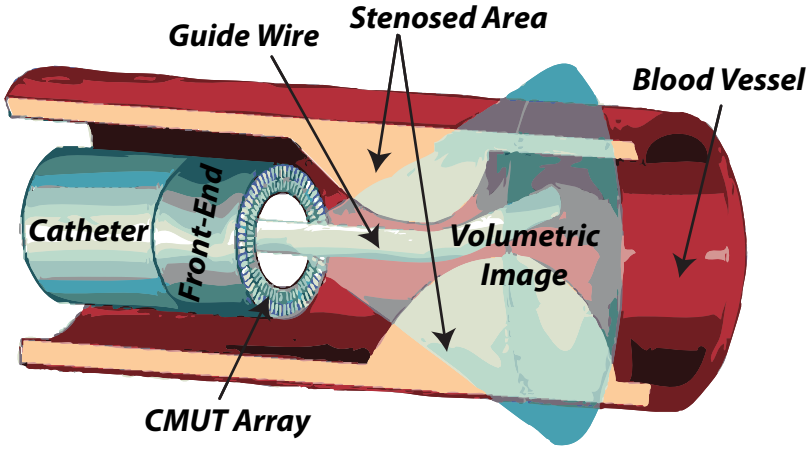


FIGURE 1.1: A graphical illustration of an intravascular ultrasound catheter.

Intravascular ultrasound (IVUS) is an imaging technique for internal body imaging. The most significant human health benefit of such technology is to visualize

plaque in arteries as in figure 1.1, courtesy of [1]. The accumulation of plague in the arterial wall over time can lead to stenosis of the artery leading to angina, or heart attack if there is a complete block in the coronary arteries. A physician will numb the groin area with a local anesthetic. A short hollow plastic tube or an introducer sheath is then inserted in the artery groin. An ultrasound catheter is then feed into the sheath, following the artery to the heart. Once the catheter is in the coronary artery, a series of cross-sectional images of the artery produced.

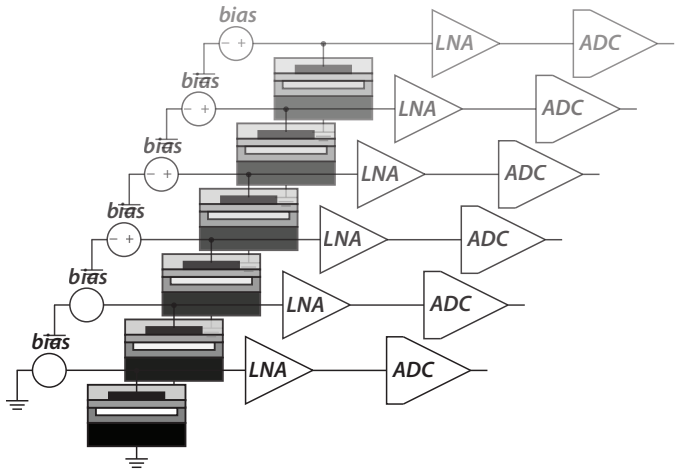


FIGURE 1.2: Block representation of an ultrasonic receiver chain array.

Ultrasonic imaging employs the use of high-frequency sound waves for depicting soft tissues. A transducer sends out a high frequency burst, which is subsequently reflected off of the body structure. A Low noise amplifier (LNA) receives and amplifies the reflected signal for further processing. Generally the front-end amplifier will be piggybacked by a high-resolution A/D-Converter for futher signal processing. Capacitive Micro machined Ultrasonic Transducers (CMUT) are easily integrate with CMOS and performes almost as good as piezoelectric transducers [2]. Moreover, CMUTS has the ability to perform when immersed in a medium, and therefore a good candidate for IVUS.

The front-end being analog limits the systems overall performance like signal-to-noise ratio, linearity and bits of resolution. Noise generated by the amplifier limits the dynamic range of the A/D-Converter, and distortion limits the maximum signal swing. Cosequently, the degradation of the total system performance is determined by the noise generated by the amplifier, and is given as Noise Figure (NF).

Figuratively representation of the catheter is seen in figure 1.1 and schematically in figure 1.2. The hollow catheter consists of a CMUT array connected to an array of analog front-ends with converters. Current production catheters do not include the A/Ds inside of the catheter. Area continues to decline in downscaled CMOS, and energy consumption rapidly decreases. It is therefor conceivable that a complete system including CMUTs, amplifiers and A/Ds may be implemented on a single chip sometime in the future.

Current state of the art front-ends use a transimpedance amplifier (TIA) [2]. TIA amplifiers are suitable for CMUT applications since they have low input impedance and overall good performance. Low front-end input-impedance improves performance of CMUTs as implied in [3]. A typical TIA based reciver chain consists of a TIA, Current feedback Amplifier (CFA) and Buffer [4]. Example [2] has a low Noise Figure (NF) of $1.8dB$, with a poor Dynamic Range (DR) of just $28dB$ and a total power consumption of $9.9mW$. Hence, the main problem with this type of approach is the sheer power consumption.

This project focuses on the use of noise cancelation using a Balun-LNA topology for reduced input referred noise. The Balun-LNA is a fairly uncommon topology for ultrasonic front end applications, but widely used for radio applications.

1.2 Main Contributions

- High performance ultrasound amplifier with very low power consumption of only $67.2\mu W$ has been introduced..
- A radio-frequency CGCS-Balun amplifier has been implemented for ultrasound applications.
- One introduces a GM-boosted CG-amplifier for further linearization and HD2-supression.
- A programmable-gain scheme has been introduced.
- Derived and proven that the CGCS Balun-LNA can cancel flicker-noise.

1.3 Thesis Outline

An ultrasound LNA is design and devised with a comprehensive design methodology. This thesis is organized in the following manner. Chapter 2, presents the relevant background theory in order to be able to analyze and comprehend the design. Chapter 3, focuses on ultrasound sensors and amplifiers. The proposed design is analyzed in chapter 4, including small-signal analysis and distortion/noise cancellation. Chapter 5 details and gives a comprehensive design methodology based on the theoretical analysis. Chapter 6 presents the final design including the layout, values based on the theoretical analysis is also given. The results for the final design are then given in chapter 7. Chapter 8 discuses the results, finally concluding in chapter 9.

CHAPTER 2

Theory

The following chapter will give the fundamental background theory for this thesis in brief. The thesis emphasizes on low noise and low power consumption. Consequently, the theory will focus on noise and low noise techniques.

2.1 Noise

The following section presents noise sources commonly present in a CMOS technology. There are several noise sources present in CMOS solid-state circuit, including temperature dependent thermal noise in resistors and transistors, frequency dependent flicker noise and bias dependent shot noise. Noise is random fluctuations in the signal, and it is by its nature non-deterministic and cannot be predicted.

2.1.1 Thermal noise

Thermal noise occurs due to random thermal movement in charge carriers in a conductor. Thermal noise is a natural occurrence and is proportional to absolute temperature. It occurs in all resistors and conductors, regardless of operating conditions. The noise characteristics appears as uniformly distributed over the spectrum, or approximately white [5].

Thermal noise can be modeled by using a noiseless resistor in combination with a noise source, as in figure 2.1. Thermal noise is given by equation 2.1 and 2.2, hence thermal noise is directly proportional to temperature T (Kelvin). Where K is the Boltzmann constant and R the resistance.

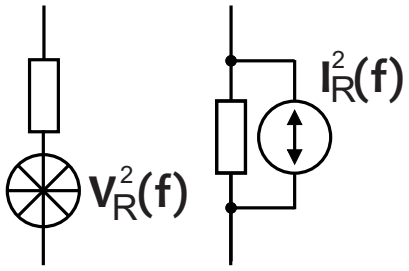


FIGURE 2.1: Thermal noise modeled for a resistor. Thermal noise as voltage (left) and as a current (right)

$$V_R^2(f) = 4kTR \tag{2.1}$$

$$I_R^2(f) = \frac{4kT}{R} \tag{2.2}$$

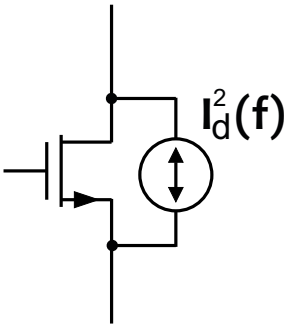


FIGURE 2.2: Thermal noise modeled for a mos transistor.

$$I_d^2(f) = 4kT\frac{2}{3}g_m \tag{2.3}$$

Thermal noise is generated in a MOSFET transistor due to the channel resistance. The following noise can be modeled by a noise current source in parallel with the transistor, as seen in figure 4.5. In the active region one cannot simply assume that channel resistance is uniform. The channel resistance is thereby obtained by integrating a portion of the channel. Thus, thermal noise in a transistor given by equation 2.3 [5].

2.1.2 Flicker noise

Low frequency noise in MOSFET circuits is commonly dominated by flicker noise. The exact nature of flicker noise is a phenomenon not fully understood. One believes that flicker noise occurs due to carriers being trapped in the channel for a random amount of time, thus creating random fluctuation in the channel [5].

The flicker noise can be referred to gate (figure 2.3) as a voltage, expressed as:

$$V_g^2(f) = \frac{K}{WLfC_{ox}} \tag{2.4}$$

Flicker noise is dependent on the device constant K, physical size of the transistor WL (Width Length), gate capacitance Cox and frequency f. From equation 2.4 one sees that flicker noise decreases with increased frequency (f) , and that it is inversely proportional to the transistor area (WL).

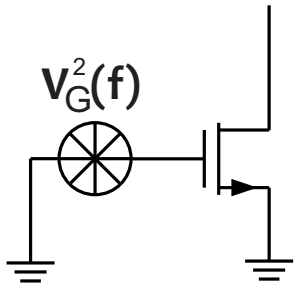


FIGURE 2.3: Flicker noise model for a MOS transistor.

One can model flicker noise as a noise voltage source at gate, as seen in figure 2.3

2.1.3 Shot noise

Shot Noise is present when a transistor is operating in the sub-threshold region, and will dominate over thermal noise. Shot noise occurs due to fluctuation in current across a potential barrier, like a pn-junction. The fluctuation occurs because of non-continuous bias supply, making bursts of current due to individual flow of carriers. Shot noise is often neglected for a MOS transistor as only gate dc leakage contributes. [5]

2.2 Noise Figure

Noise factor F is a figure of merit for a systems noise performance. Noise figure NF is Noise factor expressed in decibel. Thus, $N_F = 10\log(F)$. Noise factor could be viewed as a measurement of deterioration of the signal-to-noise ratio (SNR) between the input and the output of a system, and expressed as equation 2.5. When a system is thought to be noisy, the output noise will increase greater than the output signal thus degrading SNR [6].

$$F = \frac{S_{input}/N_{input}}{S_{output}/N_{output}} \geq 1 \tag{2.5}$$

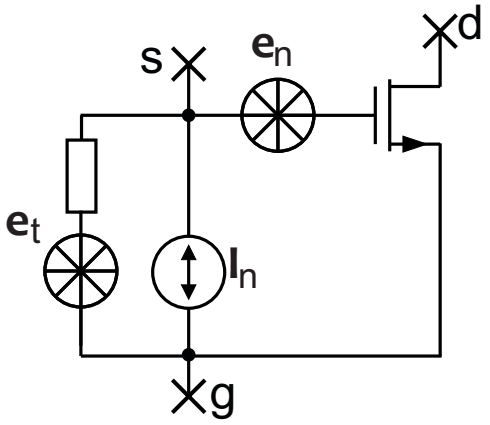


FIGURE 2.4: Noise sources for a device.

One assumes an ideal noise free device with two external noise sources 2.4 , which has the same noise output as an actual device. Noise figure is thereby a figure of merit with respect to source impedance. Noise factor F may be defined as 2.6 [7].

$$F = 1 + \frac{Input\ referred\ noise\ for\ the\ device}{Noise\ gennerated\ by\ R_s} \tag{2.6}$$

2.3 Nonlinear Distortion

A non-linear system distorts the signal and adds unwanted multiples of the fundamental frequency. Linearity of a system can be defined by several metrics. One defines the metrics used to classify the amplifier. The output signal is directly

proportional to the input signal for an ideal linear system. A general nonlinear system can be modeled as a Taylor series in terms of input signal, assuming that the system is memoryless and time invariant [6].

$$V_o = \alpha_0 + \alpha_1 V_i + \alpha_2 V_i^2 + \alpha_3 V_i^3 + ... + \alpha_n V_i^n \tag{2.7}$$

2.3.1 Harmonics

Nonlinearities in the amplifier add overtones to the spectrum. Number of harmonics is limited by the bandwidth of the system [6]. A single frequency component as a sine wave is feeding an amplifier:

$$V_i = V_m \cos(\omega_0 t) \tag{2.8}$$

Consequently, by inserting it into the Taylor expression the following can be obtained:

$$\begin{aligned} V_o &= \alpha_0 + \alpha_1 V_m \cos(\omega_0 t) + \alpha_2 V_m^2 \cos^2(\omega_0 t) + \alpha_3 V_m^3 \cos^3(\omega_0 t) + ... \\ &= \alpha_0 + \frac{\alpha_2 V_m^2}{2} + \left(\alpha_1 V_m + \frac{3\alpha_3 V_m^3}{4}\right)\cos(\omega_0 t) + \frac{\alpha_2 V_m^2}{2}\cos(2\omega_0 t) + \frac{\alpha_3 V_m^3}{4}\cos(3\omega_0 t) \end{aligned} \tag{2.9}$$

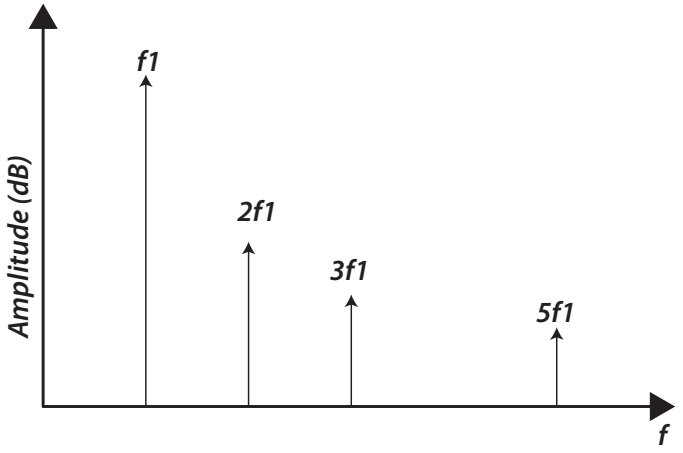


FIGURE 2.5: Single-tone spectrum where leftmost is fundamental, and then 2nd 3nd etc.

Figure 2.5 shows the single-tone spectrum of an arbitrary amplifier. One defines HD_2 as equation 2.10 and HD_3 as equation 2.11 [5].

$$\mathrm{HD}_2 = \frac{\text{Amplitude of Second Harmonic}}{\text{Amplitude of Fundamental}} = \frac{\alpha_2}{\alpha_1}\frac{V_m}{2} \tag{2.10}$$

$$\mathrm{HD}_3 = \frac{\text{Amplitude of Third Harmonic}}{\text{Amplitude of Fundamental}} = \frac{\alpha_3}{\alpha_1}\frac{V_m^2}{4} \tag{2.11}$$

2.3.2 Intermodulation Product

Intermodulation distortion (IM) is caused by nonlinearities of an amplifier, and specifies the degree of amplifiers linearity. Two frequency components are applied to an amplifier. Intermodulation between each frequency component forms additional frequencies. These additional components are the sum and difference between the fundamental frequencies, and multiples of those sum and difference frequencies [6].

Two signals are applied at different frequencies:

$$V_i = V_m[\cos(\omega_1 t) + \cos(\omega_2 t)] \tag{2.12}$$

By inserting it into the Taylor expression, the following can be obtaine:

$$\begin{aligned}
V_o &= \alpha_0 + \alpha_1 V_m[\cos(\omega_1 t) + \cos(\omega_2 t)] + \alpha_2 V_m^2[\cos(\omega_1 t) + \cos(\omega_2 t)]^2 \\
&\quad + \alpha_3 V_m^3[\cos(\omega_1 t) + \cos(\omega_2 t)]^3 + ... \\
&= \alpha_0 + \alpha_1 V_m \cos(\omega_1 t) + \alpha_1 V_m \cos(\omega_2 t) + \frac{1}{2}\alpha_2 V_m^2(1 + \cos(2\omega_1 t)) \\
&\quad + \frac{1}{2}\alpha_2 V_m^2(1 + \cos(2\omega_2 t)) + \alpha_2 V_m^2 \cos((\omega_1 - \omega_2)t) + \alpha_2 V_m^2 \cos((\omega_1 + \omega_2)t) \\
&\quad + \alpha_3 V_m^3 \left(\frac{3}{4}cos(\omega_1 t) + \frac{1}{4}cos(3\omega_1 t)\right) + \alpha_3 V_m^3 \left(\frac{3}{4}cos(\omega_2 t)\right. \\
&\quad \left. + \frac{1}{4}cos(3\omega_2 t)\right) + \alpha_3 V_m^3 \left[\frac{3}{2}cos(\omega_2 t) + \frac{3}{4}cos((2\omega_1 - \omega_2)t) + \frac{3}{4}cos((2\omega_1 + \right. \\
&\quad \left. \omega_2)t)\right] + \alpha_3 V_m^3 \left[\frac{3}{2}cos(\omega_1 t) + \frac{3}{4}cos((2\omega_2 - \omega_1)t) + \frac{3}{4}cos((2\omega_2 + \omega_1)t)\right]
\end{aligned} \tag{2.13}$$

From equation 2.13, intermodulation products appear at frequencies $n\omega_1 \pm m\omega_w$ and illustrated in figure 4.7 [5].

Figure 4.7 shows the two-tone spectrum of an arbitrary amplifier. The fundamental tones are denoted f_1 and f_2. Consequently, giving the secound intermodulation

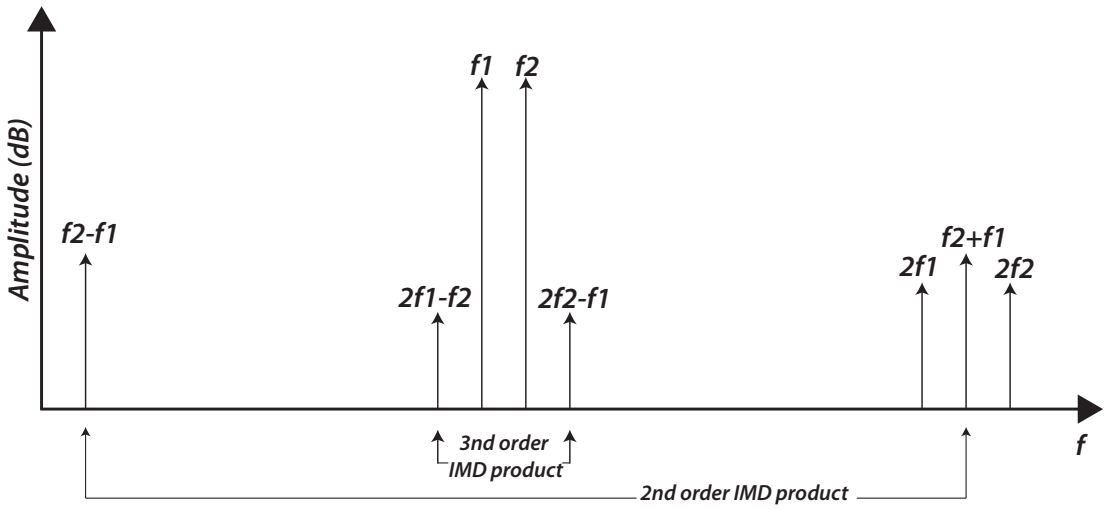


FIGURE 2.6: Two-Tone spectrum and intermodulated spurs

product (IM2) as $f_2 - f_1$ & $f_2 + f_1$ and third intermodulation product (IM3) as $2f_1 - f_2$ & $2f_2 - f_1$. One defines IM_2 and IM_3 as:

$$\mathrm{IM}_2 = \frac{\text{Amplitude of Second Intermodulation product}}{\text{Amplitude of Fundamental}} \Rightarrow 2\mathrm{HD}_2 = \frac{\alpha_2}{\alpha_1} V_m \quad (2.14)$$

$$\mathrm{IM}_3 = \frac{\text{Amplitude of Third Intermodulation product}}{\text{Amplitude of Fundamental}} \Rightarrow 3\mathrm{HD}_3 = \frac{\alpha_3}{\alpha_1} \frac{3V_m^2}{4} \quad (2.15)$$

2.4 Dynamic Range

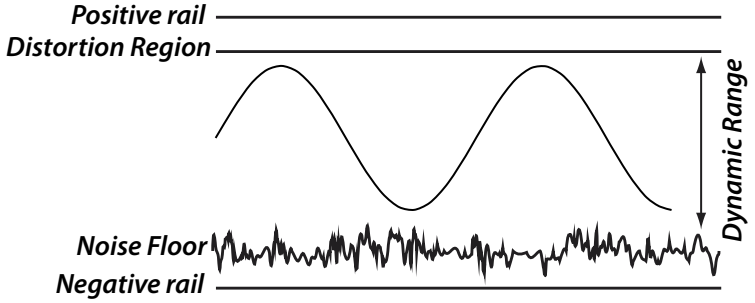


FIGURE 2.7: Dynamic Range

Dynamic Range describes the ratio between the largest and smallest signal an amplifier or a system can process. The smallest signal is determined by the noise floor of the amplifier, lesser signals are drowned out by the noise. The largest signal is given by amplifier distortion. Consequently, large dynamic range is vital

for high quality, high resolution amplifiers. By assuming that the dynamic range is limited by the supply voltage and the noise floor, the following could be written:

$$D_R = \frac{V_{pp}/2}{V_{n_{rms}}} = \frac{\eta V_{DD}}{2V_{n_{rms}}} \tag{2.16}$$

$V_{n_{rms}}$ is the RMS-value of the noise, η is the voltage efficiency and V_{pp} is the maximum peak-to-peak of the signal. Front-end amplifiers for IVUS-applications should sport a dynamic range of better than 40dB [2].

2.5 Power-Supply Rejection Ratio

The power supply rejection is a measurement of changes in the output due to changes in the supply voltage. A change in the supply voltage alters the output voltage and introduces an error at the output as equation 2.17.

$$\mathrm{PSRR}_{dB} = 20 \log \left(\frac{\delta V_{dd}}{\delta V_o} \right) \tag{2.17}$$

2.6 Layout

The section explains in brief, basic terminology and the manufacturing of a wafer for an arbitrary down-scaled CMOS-technology.

Photolithography uses light to transfer a pattern (mask out) from a mask to a light-sensitive chemical on the substrate. A number of chemical treatments are then applied that either engraves the exposure pattern into, or enables new materials to be made underneath the photo resists in the desired pattern.

Optical proximity correction (OPC) is a photolithography enhancement technique that compensate for image errors due to diffraction or process effects. Sharp edges and edge placement is difficult to obtain, and OPC corrects that by adding more material to problem areas on the mask. Figure 2.8 exemplifies the problem. A nice bend with sharp edges is drawn in a layout-tool (Black). Rounding of the corners occurs under the photolithographic process, and is shown without OPC (dark grey). OPC adds additional polygons to problem areas (Light-gray) making the bend look more like the original one after etching.

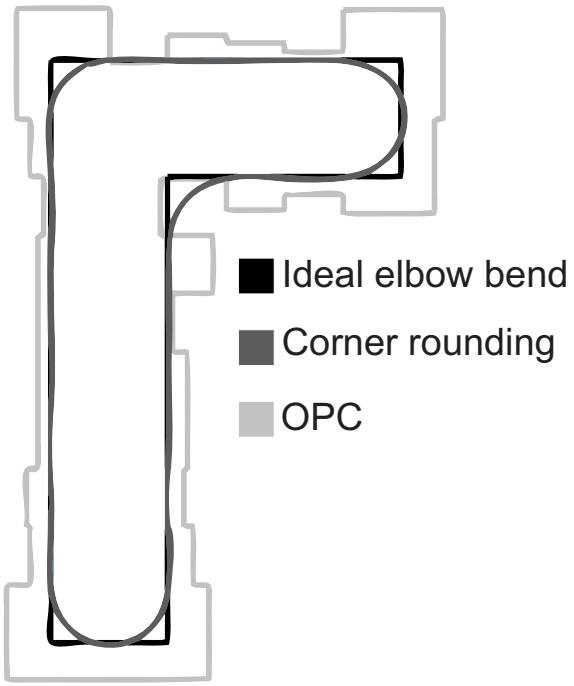


FIGURE 2.8: Ideal 90° elbow bend, when transferred to wafer corner rounding occurs and OPC adds extra material

Reactive-ion etching Reactive-ion etching (RIE) is a photolithographic etching technology that uses chemically reactive plasma to remove material deposited on wafers.

Two components with identical physical layout never have the exact same electrical properties. Mismatch is generally a problem for differential circuits, but not limited to. Mismatch is either random or systematic.

2.6.1 Random mismatch

Random mismatch occurs due to process variation. A complete elimination of random mismatch is impossible. However, mismatch could be reduced by increasing the area of the device. Process variation are often manifestations of statistical variation, and could be expressed as [5]:

$$\sigma = \frac{\kappa}{\sqrt{WL}} \tag{2.18}$$

Where κ is a process dependent parameter, and WL is the aera of the device (Width Length).

2.6.2 Systematic mismatch

Systematic mismatch often arises from imperfect balancing of a circuit, and could be eliminated by redesigning the circuit.

2.6.2.1 Pinching/Corner Rounding

Pinching, Corner Rounding and non-uniformities can be corrected by OPC when the distance is within $\approx 3\lambda$. Pinching could possibly have devastatingly effects on crucial layers such as poly. Mismatch and gate leakage can be aggravated by poly pinching. Gate leakages can potentially have a bigger impact on yield than mismatch. Poly patters going in the same direction with a fixed pitch, requires less OPC. Moreover, high poly density degrades RIE loading. [8]

2.6.2.2 Well Proximity Effect

The threshold voltage for a device is dependent on the distance from the edge of the well mask to the channel. Threshold is increased when the device is too close to resist edge, due to dopant ions scattering off resist sidewall into active area during well implants [9]. The effect of WPE could be reduced by increasing the distance from gate to the well edge. Distance greater than 2μm greatly reduces WPE. However, a better strategy is to use extended well patterns [8].

2.6.2.3 Shallow Trench Isolation

A function of which prevents electrical current leakage between neighboring semiconductor device components. The oxide isolation trench for a device produces channel stress, and thus affects both the threshold voltage and mobility. The effect is inversely proportional to distance between each trench and the channel. One can reduce the effect of STI by using a pair of fingers (two gates) for each device [8].

CHAPTER 3

Ultrasound Front-End

3.1 Ultrasound front-end

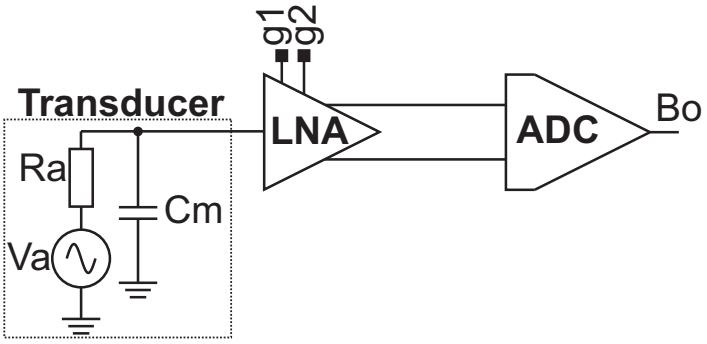


FIGURE 3.1: Block representation of the suggested LPLN receiver architecture, for the ultrasound imaging.

Low Noise-Amplifier (LNA) is a key building block in front-end amplifiers for high quality instrumentational systems. The primary function for a LNA is to amplify very weak signals whilst not adding undesirable noise.

The received ultrasound pulse is delicate and need further signal conditioning before the received signal gets digitized. The low noise amplifier increases the signal power of the transducer signal, so that the signal does not get drowned in noise from the A/D-Converter.

3.2 Ultrasound transducers

An ultrasound transducer is an electromechanical device that converts ultrasound to voltage and vice versa. The most common types are Piezoelectric transducers

and Capacitive Micromachined Ultrasonic Transducer (CMUT).

3.2.1 Capacitive Micromachined Ultrasonic Transducers

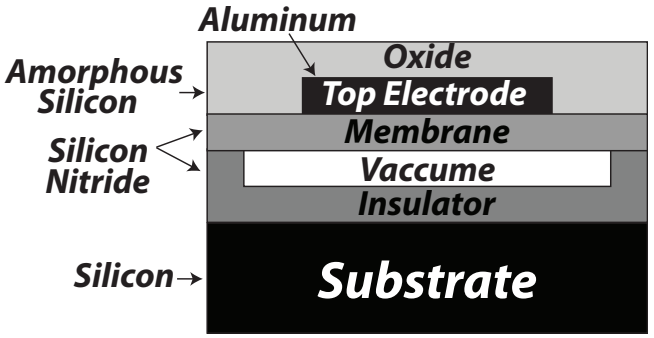


FIGURE 3.2: Side cut view of a single CMUT-cell

Capacitive Micromachined Ultrasonic Transducers (CMUT) are, as seen in figure 3.2 a capacitor-cell consisting of a thin membrane suspended over a thin cavity, fabricated under a standard CMOS technology. The membrane is coated with a thin metal layer and thus formes a variable capacitor in respect to the back plate. When the electrodes are biased with a high-voltage (30v), the membrane is attracted toward the substrate by the electrostatic force. By applying an AC-voltage the membrane will vibrate. When pressure is applied to the biased membrane, one effectivly alters the distance between the two electrodes, consequently, changing the capacitance. Thus, allowing one to use CMUT as the sending-element as well as the receiving-element. The amplitude is determined by capacitance of the cell, bias voltage and the frequency of the incident wave. As previoulsy stated, CMUTS are fabricated in a standard CMOS technology, making them very cost efficient. Moreover, CMUTs sports high yield. CMUTs generally achieves better impedance matching to the propagation medium than piezoelectric transducers. Thus, achieving higher fractional bandwidth. [3]

3.2.1.1 Electrical characterization

The electrical characteristics of a single CMUT as a receiving element can be simplified [4], and looked upon under resonance as an impedance of $10k\angle -60°$.

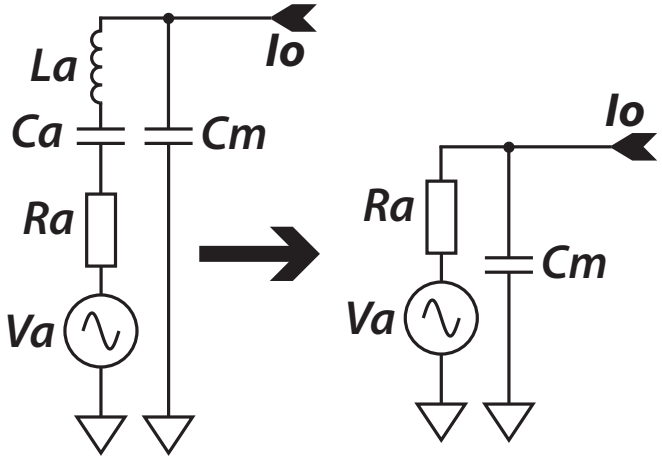
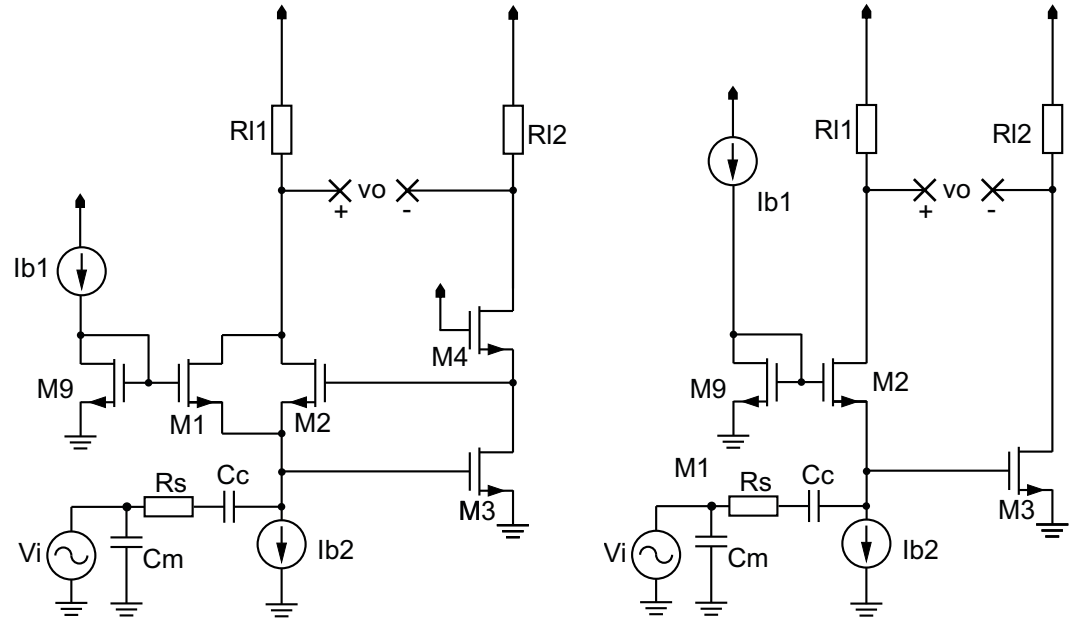


FIGURE 3.3: Electrical equivalent circuit for a CMUT at resonance. Simplified circuit (right)

CHAPTER 4

The Balun-LNA

4.1 The Balun-LNA



(a) The proposed CGCS Balun-LNA, here shown without programmable gain

(b) Conventional CGCS Balun-LNA

FIGURE 4.1: The CGCS-Balun LNA

The proposed CGCS Balun-LNA [figure 4.1(a)] employs feedback by partly gm-boosting the CG-Stage by the CS-stage. The conventional CGCS-LNA [10] [figure 4.1(b)] achieves decent HD_2 suppression [11], since the CS-amplifier will performs error-correction on the CG-amplifier. However, further improvements are possible. The proposed CGCS-Balun-LNA achieves significant improvement in HD_2 suppression, which are later presented.

Moreover, one will later prove that the linearity of the CGCS-Balun-LNA is independent of the CG-Amplifier. Consequently, other linearity parameters could possibly also be improved by adding feedback to the CS-amplifier.

The amplifier in figure 4.1(a), consists of a non inverting common gate-amplifier and an inverting common source-amplifier and performes single-to-differential conversion. Thermal noise due to transistor $M1$ and $M2$ could be modelled as a current source in parallel. Flicker noise from the same devices could also be modelled, but as voltage sources at the respected gates. Thus, generating noise voltages in anti-phase, over the surge impedance (R_s) and over the load impedance (R_{L1}). The noise voltage $V_n R_s$ will be amplified and phase shifted by a CS-amplifier. Consequently, the noise at the positiv output (Vn_{op}) and the negative output (Vn_{on}) are in phase. One could therefore cancel thermal noise entirely from M1 and M2, if the noises correlates and are of the same magnitude. The amplifier is design towards a source impedance (R_s) of $10k\angle -60°$.

$M2$ looks to be gm-boosted by the CS-amplifier. However, the main objective is to enhance the linearity of the CS-amplifier by using $M2$ as feedback, and not to increase the gain. $M3$ is biased by the quiescent current flowing trough the CG-Amplifier and $M2$ is biased by the CS-amplifier. Thus, creating somewhat of a circular dependency between the two amplifying stages (V_{op}, V_{on}). One tries to counteract the dependency with $M1$. $M1$ is an amplifying element, but its primary function is to controll the operation point of the CS-amplifier, somewhat independently of the CG-amplifier.

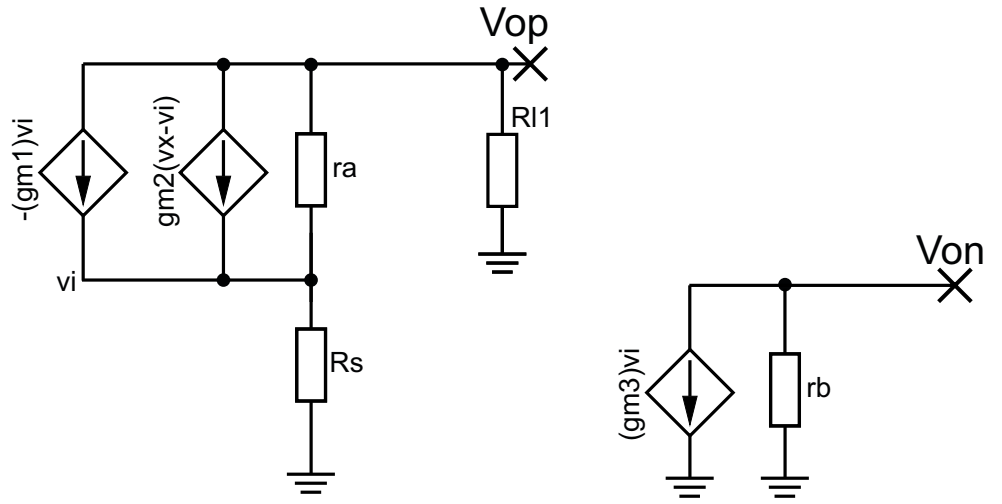
4.2 Small Signal Analysis

Note that the channel resistance: $r_a = R_{ds1} \| R_{ds2}$. By assuming that $R_{L2} << R_{ds3}$ thus giving $r_b = R_{L2} \| R_{ds3} \approx R_{L2}$.

According to figure 4.2(a), the input voltage V_i is given by the sum of the drop over r_a and R_{L1}, thus giving:

$$V_i = \frac{r_a + R_{L1}}{R_s[r_a(r_b g_{m3} g_{m2} + g_{m1} + g_{m2}) + 1] + R_{L1} + r_a} \tag{4.1}$$

The expression is simplefied by assuming that $g_{m1} << g_{m2}$ and $r_a(r_b g_{m3} g_{m2} + g_{m1} + g_{m2}) >> 1$. One later finds an expression for noise cancellation (given by



(a) Common-gate stage (b) Common-Source stage

FIGURE 4.2: Simplified noise analysis of the proposed design, where In is thermal noise from the CG stage.

equation 4.15), and the following could be obtained:

$$V_i \approx \frac{r_a + R_{L1}}{r_a[R_{L1}g_{m2} + g_{m2}R_s + 1] + R_{L1}} \tag{4.2}$$

4.2.1 V_{out}^-

Gain for a common source amplifier could be written as: $V_{out}^- = -g_{m3}r_bV_i$. Including the feedback by M_2 the amplification could be written as:

$$V_{A_v}^- = \frac{-g_{m3}r_b(r_a + R_{L1})}{r_a[R_{L1}g_{m2} + g_{m1}R_s + 1] + R_{L1}} \tag{4.3}$$

Again, inserting the noise cancellation term into g_{m3} (given by equation 4.15), the following could be written. Also note that $r_b = R_{L2} \| R_{ds3} \approx R_{L2}$.

$$V_{A_v}^- = -\frac{R_{L1}(r_a + R_{L1})}{R_s(r_a[R_{L1}g_{m2} + g_{m1}R_s] + R_s)} \tag{4.4}$$

4.2.2 V_{out}^+

The input voltage V_i was given by eqaution 4.2 and the gain could be obtained by multiplying it with the output impedance. Common-gate small signal gain could

therefore be written as:

$$V_{A_v}^{+} = \frac{[r_a(r_b g_{m3} g_{m2} + g_{m1} + g_{m2}) + 1]R_{L1}}{R_s[r_a(r_b g_{m3} g_{m2} + g_{m1} + g_{m2}) + 1] + R_{L1} + r_a} \tag{4.5}$$

Investigating the denominator, one sees that the surge impedance R_s governed by the gm-boosting and is more significant. Consequently, one could assume the following: $R_s[r_a(r_b g_{m3} g_{m2} + g_{m1} + g_{m2}) + 1] >> R_{L1} + r_a$. The simplification yields the following:

$$V_{A_v}^{+} \approx \frac{R_{L1}}{R_s} \tag{4.6}$$

4.2.3 Small Signal Gain

The gain for the CG-stage and the CS-stage was given by equation 4.5 and 4.4. Total small signal gain could be obtained by differentiating the outputs. Thus, giving:

$$V_{A_v}^{\text{diff}} = \frac{R_{L1}}{R_s}\left(1 + \frac{r_a + R_{L1}}{r_a[R_{L1} g_{m2} + g_{m1} R_s] + R_s}\right) \tag{4.7}$$

4.2.4 Input impedance

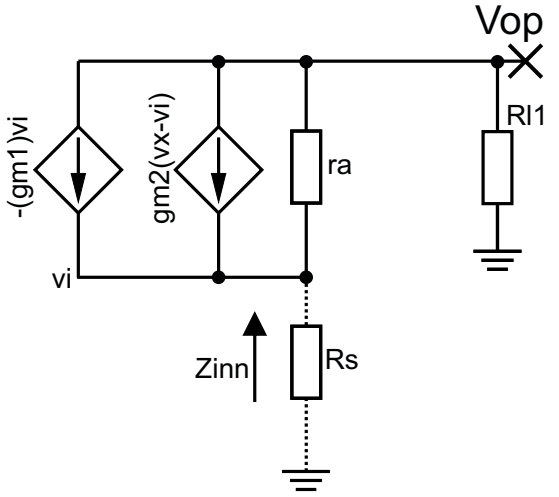


FIGURE 4.3: Small signal analysis neglecting R_s

The input impedance of the Balun-LNA is approximated as the input impedance of the CG-stage, for low frequencies.

$$Z_i = Z_{iCG} \| Z_{iCS} \approx Z_{iCG} \tag{4.8}$$

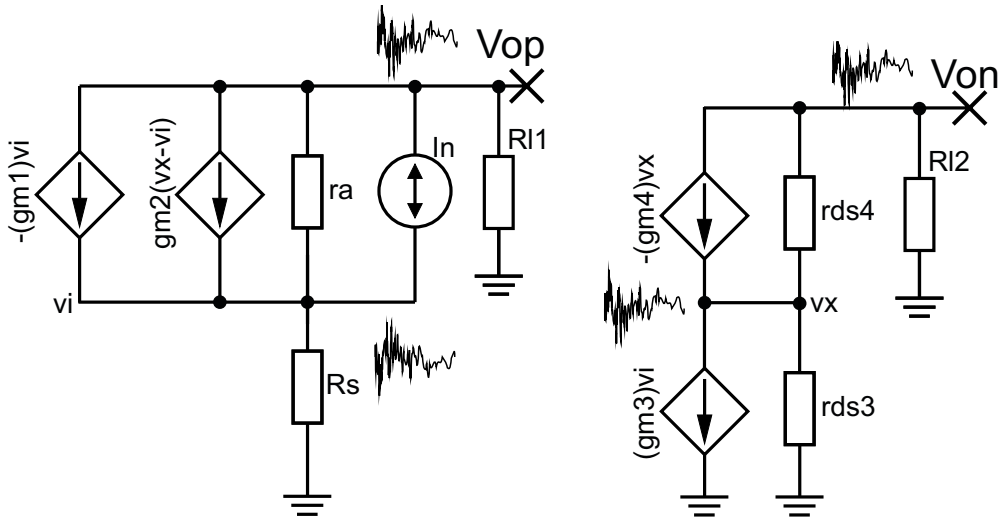
The input voltage over R_s was given by equation 4.2. Moreover, the input impedance looking into V_i can be obtained by setting R_s=0. [**?**]

$$Z_i = \frac{r_a + R_{L1}}{r_a(r_b g_{m3} g_{m2} + g_{m1} + g_{m2}) + 1} \tag{4.9}$$

4.3 Noise and Distortion Analysis

The following section deals with the criteria, which must be fulfilled for achieving perfect noise and distortion cancellation. Later, linearity expressions for a single stage will be derived.

4.3.1 Thermal-Noise Cancellation



(a) Common-gate stage (b) Common-Source stage

FIGURE 4.4: Simplified noise analysis of the proposed design, where In is thermal noise from the CG stage.

r_{ds4} and r_a are neglected in this simplified analysis. The current flowing through the transconductances g_{m1} and g_{m2} and the noise current I_n is the same as flowing

through R_s, denoted I_x. Looking at 4.4, one could claim that the current could be expressed as:

$$I_x = \frac{(1 + g_{m4}r_{ds3})I_n}{R_s[g_{m1}(1 + g_{m4}r_{ds3}) - g_{m2}(1 + g_{m3}r_{ds3} + g_{m4}r_{ds3})] + 1 + g_{m4}r_{ds3}} \tag{4.10}$$

The voltage at the input could therefore be expressed $V_i = R_s I_x$ giving:

$$V_i = \frac{(1 + g_{m4}r_{ds3})I_n R_s}{R_s[g_{m1}(1 + g_{m4}r_{ds3}) - g_{m2}(1 + g_{m3}r_{ds3} + g_{m4}r_{ds3})] + 1 + g_{m4}r_{ds3}} \tag{4.11}$$

V_i is amplified by the CS-amplifier, and since r_{ds4} is neglected, the transfer function could be given as: $V_{on} = -g_{m4}g_{m3}r_{ds3}R_{L2}V_i$, consequently:

$$V_{on} = -\frac{g_{m4}g_{m3}r_{ds3}R_{L2}I_n R_s}{R_s[g_{m1}(1 + g_{m4}r_{ds3}) - g_{m2}(1 + g_{m3}r_{ds3} + g_{m4}r_{ds3})] + 1 + g_{m4}r_{ds3}} \tag{4.12}$$

The current flowing through R_s is the same as the current flowing through R_{L1}. Thus, the output could be expressed as $V_{op} = I_x R_{L1}$, giving:

$$V_{op} = \frac{R_{L1}I_n(1 + g_{m4}r_{ds3})}{R_s[g_{m1}(1 + g_{m4}r_{ds3}) - g_{m2}(1 + g_{m3}r_{ds3} + g_{m4}r_{ds3})] + 1 + g_{m4}r_{ds3}} \tag{4.13}$$

Differentiating the two outputs given by equation 4.13 and 4.12 and solving for R_s, yields:

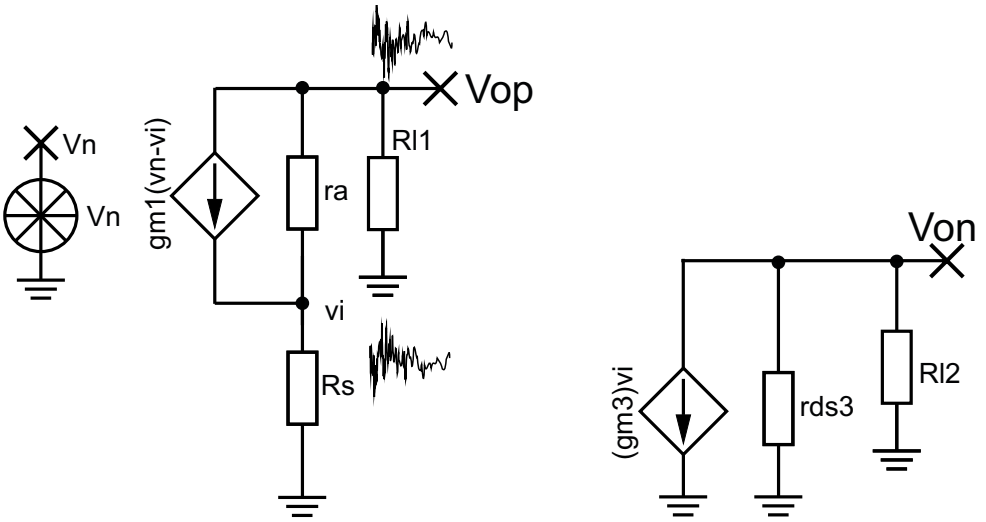
$$V_{op} - V_{on} \rightarrow R_s = \frac{R_{L1}(1 + g_{m4}r_{ds3})}{g_{m4}g_{m3}r_{ds3}R_{L2}} \tag{4.14}$$

By assuming that $1 << g_{m4}r_{ds3}$, one could rewrite the expression as:

$$R_s \approx \frac{R_{L1}}{g_{m3}R_{L2}} \tag{4.15}$$

4.3.2 Flicker-Noise Cancellation

Flicker-noise can be modeled as previously done in chapter 2.1.2, as a noise voltage source at the gate. Moreover, it will be shown that the topology has the ability to not only cancel thermal-noise, but also flicker-noise produced by the CG-stage.



(a) Common-gate stage

(b) Common-Source stage

Flicker noise is as previously stated inversely proportional to device area and frequency. Thus noise constraints due to flicker-noise could easily be solved by sizing area. With the following in mind, one takes the liberty and conducts a very simplified analysis. Firstly, one omits the gm-boosting of M_2 and the cascoding transistor M_4. Secondly, one assumes that M_1 and M_2 is the same device. Lastly, channel resistance of M_3 is ignored.

The voltage over R_s, due to V_n could be expressed as:

$$V_i = -\frac{g_{m1} r_a V_n}{R_s(1 + g_{m1} r_a) + R_{L1} + r_a} R_s \tag{4.16}$$

The same current that passes through R_s passes also through R_{L1} in anti-phase, ie $V_{op} = -R_{L1} I_i$, thus:

$$V_{op} = \frac{g_{m1} r_a V_n}{R_s(1 + g_{m1} r_a) + R_{L1} + r_a} R_{L1} \tag{4.17}$$

Amplification by the common-gate stage can be given as $V_{on} = -V_i(g_{m3} R_{L2})$, inserting the expression for the noise voltage (equation 4.16) at the input:

$$V_{on} = \frac{g_{m1} r_a V_n}{R_s(1 + g_{m1} r_a) + R_{L1} + r_a} R_s g_{m3} R_{L2} \tag{4.18}$$

Differentiating the output yields:

$$V_{op} - V_{on} \to R_s \approx \frac{R_{L1}}{g_{m3} R_{L2}} \tag{4.19}$$

Flicker-noise from CG-stage can be cancelled if the following yields true. Furthermore, by comparing the expression for flicker-noise cancellation (4.18) with the expression one previously obtained for thermal-noise (4.15), one gets the exact same conditions. The analysis conditions where not exactly the same, but the analysis gives an indication for which direction to turn the knobs.

4.3.3 Distortion Cancellation

One assumes that non-ideal behaviour could be modeled as a current that is dependent on the gate-source voltage.

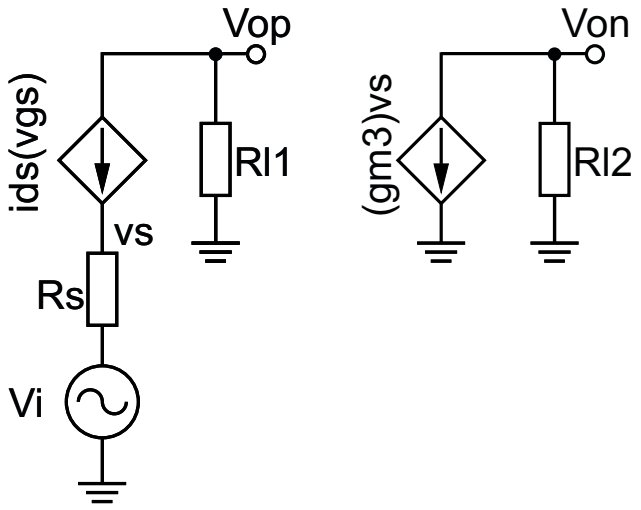


FIGURE 4.5: Dynamic Range

Distortion could be expressed as a Taylor-series as given by equation 2.7. Thus, the non-linear source voltage (V_s) could be written as a Taylor-series of the input signal (V_{in}):

$$V_s = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3 + ... + \alpha_n V_{in}^n = V_{in} + V_d \tag{4.20}$$

Where α represents the Taylor coefficients and V_d contains all of the nonlinear behaviour [**?**]. The negative output voltage (V_{on}) is the source voltage (V_s) amplified by a CS-amplifier, giving:

$$V_{on} = -g_{m3} R_{L2} V_s = -g_{m2} R_{L2} [V_s + V_d] \tag{4.21}$$

In termes of distortion, (V_{op}) is given by the load and the non-ideal behavioural current (I_{ds}) and inserting equation 4.20, yields:

$$V_{op} = R_{L1}I_{In} = (V_i - V_s)\frac{R_{L1}}{R_s} = [V_{in} - (V_{in} + V_d)]\frac{R_{L1}}{R_s} \tag{4.22}$$

Differentiating the outputs yields:

$$V_{op} - V_{on} = 0 \rightarrow -(V_s + V_s + V_d)\frac{R_{L1}}{R_s} + (V_s + V_d)R_{L2} + g_{m2} \tag{4.23}$$

Inserting the condition for noise cancellation given in equation 4.15 and inserting into 4.23, the output could be written as:

$$V_o = R_{L2}g_{m3}V_s \tag{4.24}$$

Consequently, all of the non-linear elements are removed from the output. Thus, the differentiated output is only dependent on the CS-amplifier in terms of distortion and noise.

4.3.4 Common-Source Linearity

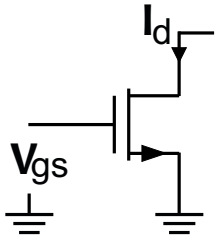


FIGURE 4.6: Commoun-source amplifier, without load.

The distortion for a CS-stage could be analyzed by using the square-law model (equation 4.25) . However, the square-law model does not take short-channel devices into account [12].
The Square-law model for MOS transistor can be written as:

$$I_d = \mu_0 C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 \tag{4.25}$$

Harmonic distortion could be looked upon as a Taylor-series as one saw in chapter 2.3.1 . The first order coefficient can be expressed as follows:

$$\alpha_1 = \frac{\delta I_d}{\delta V_{gs}}\bigg|_{V_{gs}=V_{gsq}} = \mu_0 C_{ox}\frac{W}{L}(V_{gs}-V_t)\bigg|_{V_{gs}=V_{gsq}} = \mu_0 C_{ox}\frac{W}{L}V_{eff} = \frac{2I_d}{V_{eff}} = g_m \tag{4.26}$$

And the second order coefficient can be expressed as:

$$\alpha_2 = \frac{1}{2}\frac{\delta^2 I_d}{\delta V_{gs}^2}\bigg|_{V_{gs}=V_{gsq}} = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}V_{eff} = \frac{I_d}{V_{eff}^2} = \frac{1}{2}g'_m \tag{4.27}$$

$$\alpha_3 = \frac{1}{6}\frac{\delta^3 I_d}{\delta V_{gs}^3}\bigg|_{V_{gs}=V_{gsq}} = 0 \tag{4.28}$$

The definition of HD2 was given in equation 2.10 and by inserting equation 4.26 and 4.27 yields:

$$\mathrm{HD}_2 = \frac{1}{4}\frac{V_m}{V_{eff}} \tag{4.29}$$

One sees from the equation, that second harmonic distortion is minimized by increasing the overdrive voltage. However, using higher overdrive voltage will increase the power consumption and worsening the efficiency of the stage. The following analysis implies the usage of long channel devices. Consequently, the gate length of a common source amplifier should be maximized.

One has derived an expression for which must be fulfilled in order to obtain proper noise cancellation for the proposed topology. One has also seen that the balun-toplogy has the ability to cancel harmonic distortion and other non-idealities from the CG-stage. Consequently, the proposed design is theoretically only dependent on the CS-stage. However, the theoretical analysis has not taken parasitic capacitances into account, nor does it consider phase-error between the two stages. Since the linearity of the topology was dependent on the CS-stage, distortion metrics for a CS-stage was derived.

4.4 Noise Sources

Thermal noise and flicker noise was defined in theory section 2.1.1 and 2.1.2. The noise sources are assumed to be uncorrelated, and are looked upon independently from each other. One will derive an expression for Noise Figure for the amplifier. An expression for each noise source is independently derived, and referred to at the

output of both amplifier stages. The noise figure was defined in theory chapter **??**. Small-signal analysis with respect to noise for the Balun-LNA, was most

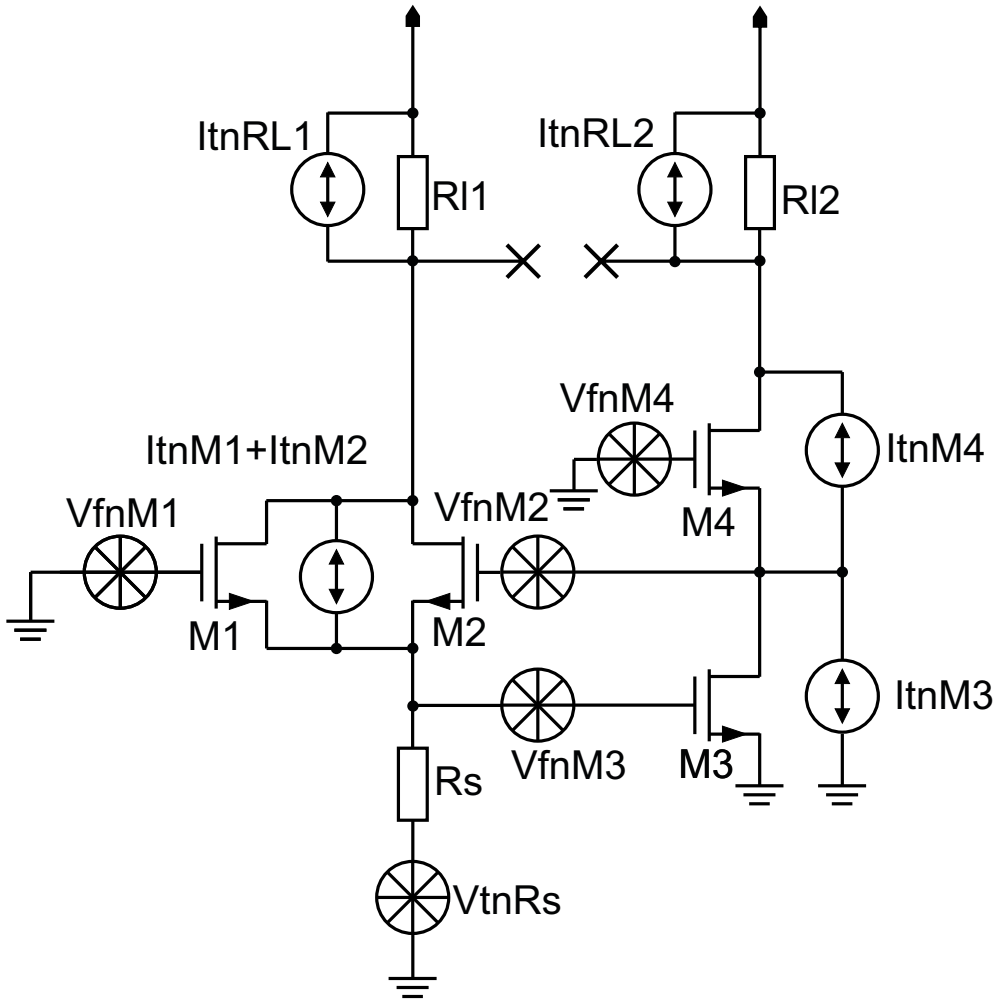


FIGURE 4.7: Noise sources present due to thermal and flicker noise for the proposed design.

thoroughly done in the premaster project [13]. The focus is therefore shifted away from small signal analysis. Superficial expressions for the noise sources are found under appendix B.1.

4.4.1 Noise power

$\beta = R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}$

Flicker-Noise from $M1$

$$V^{+2}_{fnm1} = \left(\frac{g_{m1} r_a R_{L1}}{\beta}\right)^2 \frac{\kappa}{W_1 L_1 C_{ox} f} \tag{4.30}$$

$$V^{-2}_{fnm1} = \left(\frac{g_{m3} g_{m1} r_a R_s R_{L2}}{\beta}\right)^2 \frac{\kappa}{W_1 L_1 C_{ox} f} \tag{4.31}$$

Flicker-Noise from $M2$

$$V^{+2}_{fnm2} = \left(\frac{g_{m2} r_a R_{L1}}{\beta}\right)^2 \frac{\kappa}{W_2 L_2 C_{ox} f} \tag{4.32}$$

$$V^{-2}_{fnm2} = \left(\frac{g_{m3} g_{m2} r_a R_s R_{L2}}{\beta}\right)^2 \frac{\kappa}{W_2 L_2 C_{ox} f} \tag{4.33}$$

Flicker-Noise from $M3$

$$V^{+2}_{fnm3} = \left(\frac{g_{m3} r_a R_{L1} R_{L2}}{\beta}\right)^2 \frac{\kappa}{W_3 L_3 C_{ox} f} \tag{4.34}$$

$$V^{-2}_{fnm3} = -\left(\frac{g_{m3}(g_{m2} R_s r_a + g_{m1} R_s r_a + R_s + r_a + R_{L1}) R_{L2}}{\beta}\right)^2 \frac{\kappa}{W_3 L_3 C_{ox} f} \tag{4.35}$$

Thermal-Noise from $M1$ ***and*** $M2$

$$V^{+2}_{tnm12} = (g_{m1} + g_{m2}) 4kT\gamma \left(\frac{R_{L1} r_a}{\beta}\right)^2 \tag{4.36}$$

$$V^{-2}_{tnm12} = (g_{m1} + g_{m2}) 4kT\gamma \left(\frac{g_{m3} r_a R_s R_{L2}}{\beta}\right)^2 \tag{4.37}$$

Thermal-Noise from $M3$

$$V^{+2}_{tnm3} = 4kT g_{m3} \gamma \left(\frac{g_{m2} r_a R_{L1} R_{L2}}{\beta}\right)^2 \tag{4.38}$$

$$V^{-2}_{tnm3} = 4kT g_{m3} \gamma \left(\frac{(g_{m2} R_s r_a + g_{m1} R_s r_a + R_s + r_a + R_{L1}) R_{L2}}{\beta}\right)^2 \tag{4.39}$$

Thermal-Noise from R_{L2}

$$V^{+2}_{tnrl2} = 4kTR_{L2}\left(\frac{g_{m2}r_aR_{L1}}{\beta}\right)^2 \tag{4.40}$$

$$V^{-2}_{tnrl2} = 4kTR_{L2}\left(\frac{g_{m2}R_sr_a + g_{m1}R_sr_a + R_s + r_a + R_{L1}}{\beta}\right)^2 \tag{4.41}$$

Thermal-Noise from R_{L1}

$$V^{+2}_{tnrl1} = 4kTR_{L1}\left(\frac{g_{m2}r_a}{\beta}\right)^2 \tag{4.42}$$

$$V^{-2}_{tnrl1} = \frac{4kT}{R_{L1}}\left(\frac{r_aR_sR_{L2}}{\beta}\right)^2 \tag{4.43}$$

Thermal-Noise from R_s

Thermal noise from R_s, differentiated and $V^{diff^2}_{tnRs} = V^{+2}_{tnRs} - V^{-2}_{tnRs}$.

$$V^{diff^2}_{tnRs} = 4kTR_s\left(\frac{R_{L1}(g_{m2}r_aR_{L2}g_{m3} + 1 + g_{m1}r_a + g_{m2}r_a) + g_{m3}R_{L2}(R_{L1} + r_a)}{\beta}\right)^2 \tag{4.44}$$

4.4.2 Noise Factor

The Total noise power at the differential output is the sum of all the noise contributions, assuming the noises are uncorrelated. Thermal Noise from both M_1 and M_2, could be modeled as a noise current in parallel, as one did in chapter 2.2. Thus, cancelling thermal noise at the differential output produced by both M_1 and M_2. Therefore, one assumes perfect noise cancellation and neglects thermal noise from M_1 and M_2. Consequently, each output could be expressed as:

$$V^{+2}_{n} = V^{+2}_{fnm1} + V^{+2}_{fnm2} + V^{+2}_{fnm3} + V^{+2}_{tnm3} + V^{+2}_{tnrl2} + V^{+2}_{tnrl1} \tag{4.45}$$

$$V^{-2}_{n} = V^{-2}_{fnm1} + V^{-2}_{fnm2} + V^{-2}_{fnm3} + V^{-2}_{tnm3} + V^{-2}_{tnrl2} + V^{-2}_{tnrl1} \tag{4.46}$$

The Noise Factor could be written as:

$$F = \frac{V^{diff^2}_{tnRs} + V^{+2}_{n} + V^{-2}_{n}}{V^{diff^2}_{tnRs}} = 1 + \frac{V^{+2}_{n} + V^{-2}_{n}}{V^{diff^2}_{tnRs}} \tag{4.47}$$

Noise Power at the positive differential output (V^{+2}) was given by equation: 4.30, 4.32, 4.34, 4.38, 4.40 and 4.42 and the negative noise powers (V^{-2}) by equation: 4.31, 4.33, 4.35, 4.39, 4.41 and 4.43. Thus, by summing and inserting into 4.47, the following could be obtained:

Note that $\alpha = R_{L1}(g_{m2}r_aR_{L2}g_{m3} + 1 + g_{m1}r_a + g_{m2}r_a) + g_{m3}R_{L2}(R_{L1} + r_a)$, in order to make a more appealing expression.

$$\begin{aligned} F = 1 + \left(\frac{1}{4kTR_s\alpha^2}\right) \Bigg[\Bigg(& \frac{\kappa g_{m3}^2}{W_3L_3C_{ox}f} \\ & + 4kT(g_{m3}\gamma R_{L2}^2 + \gamma R_{L2}g_{m2}^2 + \frac{g_{m2}^2}{R_{L1}}) \Bigg) (r_aR_{L1})^2 + \frac{4kT}{R_{L1}}(r_aR_sR_{L2})^2 + (R_s[1 \\ & + g_{m2} + g_{m1}r_a] + r_a + R_{L1})^2 \left(\frac{(g_{m3}R_{L2})^2\kappa}{W_3L_3C_{ox}f} + 4kTR_{L2}(1 + \gamma g_{m3}R_{L2}) \right) \Bigg] \end{aligned} \tag{4.48}$$

CHAPTER 5

Design Methodology

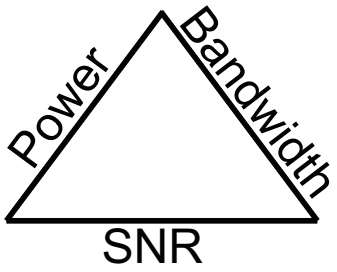


FIGURE 5.1: Drawbacks for analog design

Analog circuit performance is determined and quantified by power consumption, speed and accuracy. The metrics has a circular dependency to each other as in figure 5.1, and there is always a trade-off between the different metrics [14].

5.1 Figure of Merit

In order to quantify the performance of the circuit, one defines a Figure of Merit (FOM) in relation to the different performance metrics of the design. Bog standard FOM for an A/D converter is given as:

$$\text{FOM} = \frac{P}{\text{DR}^2 \times f} \tag{5.1}$$

Where DR is Dynamic Range, P os power consumption and f is maximum convertible frequency. However, the FOM defined in equation 5.1 does not take important design metrics into account. Consequently, one defines a FOM tailored towards LNA design.

$$\text{FOM} = \frac{P \times F^2}{\text{DR}^2 \times B \times A_v} \tag{5.2}$$

The new definition is given by equation 5.2, where DR is the Dynamic Range, P is power consumption, B is Bandwidth, A_v is the voltage gain and F the is noise factor.

5.2 g_m/I_d

The proposed design is predominantly geared towards power efficiency. The power efficiency of an amplifier relates to the device efficiency, which is governed by g_m/I_d. An increased V_{gs} increases g_m thus reducing g_m/I_d (equation 5.3). Consequently, V_{gs} should be minimized in order to maximize g_m/I_d.

$$g_m/I_d = \frac{V_{eff}}{1/2 \times V_{eff}^2} = \frac{2}{V_{eff}} = \frac{2}{V_{gs} - V_{th}} \tag{5.3}$$

Device thermal noise is proportional to V_{gs}, from equation 5.3 and 2.3. HD_2 is inversely proportional to V_{gs} (equation 4.29). Therefore, choosing V_{gs} is a fairly non-trivial procedure and exemplifies the different tradeoffs which must be taken into account for an analog circuit.

5.3 Amplifier Design

It has previously been proven that the performance of the amplifier is independent of the Common-Gate stage, as one previously saw in the theoretical analysis in chapter: 4.3.1, 4.3.2 and 4.3.3, therefore, relaxing constraints on both noise and distortion performance of the CG-amplifier. The design methodology for the proposed design is therefore governed by the foregoing theortical analysis. The CG-amplifier is therefore analyzed and designed independently of the CS-stage. Linearity and noise is neglected, and only bandwidth requirements and gain are taken into account.

5.3.1 Common-Gate

R_s is determined by the output impedance of the CMUT, and modeled as one previously did in theory chapter 3.2.1.1. The bandwidth for the amplifier could

be approximated as a parallel RC-filter, thus giving:

$$R_{L1} = \frac{1}{\omega C_t} \tag{5.4}$$

The gain for the CG-stage could be approximated as:

$$A_{cg} = \frac{R_{L1}}{R_s} \tag{5.5}$$

Flicker noise should ideally be cancelled. However, one should size the area of the devices so that the noise corner is under the band of interest, thus, relaxing correction strains on the CG-stage.

5.3.2 Bias

M_2 is self-biased by the CS-amplifier. M_1 supplies bias current to the M_3 and governs V_{gs}. The power efficiency is given by g_m/I_d-ratio as given in chapter 5.3. The drain current could be approximated by equation 5.6b, and g_m could be determined in order to achieve sufficient power efficiency.

5.3.3 Common-Source

The drain-current can be expressed for the Common-source stage, by the square-law model (equation 4.25). The drain current for the CS-stage can therefore be expressed as:

$$I_d = \frac{1}{2} g_{m3} V_{eff} \tag{5.6a}$$

$$I_d = \frac{1}{2} \frac{V_{dd}}{R_{L2}} \tag{5.6b}$$

Equation 5.6b is derived by assuming $I_d = \frac{V_{dd}-V_o}{R_{L2}} = \frac{V_{dd}-V_{dd}/2}{R_{L2}}$

The power consumption for an arbitrary mosfet device could be expressed as:

$$P_d = \frac{1}{2} g_{m3} \frac{V_{pp}}{\eta_v} V_{eff} \tag{5.7}$$

The voltage efficiency for the device is expressed as η_v. Moreover, the theoretical maximum efficiency for a class-A amplifier is 25% [6].

A square-law device only produces HD2 as one saw earlier. Since distortion was only dependent on the CG-stage, one will express power consumption relative to HD2. V_m was previously defined as the input signal for a Taylor representation of distortion.

$$V_{eff} = \frac{1}{4}\frac{V_m}{\mathrm{HD}_2} \tag{5.8}$$

Transconductance is easiest determined by the load capacitance in relation to the unity gain frequency.

$$g_m = \omega_u C_t \tag{5.9a}$$

$$C_t = C_l + C_{db} + C_p \tag{5.9b}$$

Combining equation 5.15a, 5.10, 5.8 and 5.9a yields:

$$P_d = \frac{1}{8}V_{pp}\frac{V_m}{\mathrm{HD}_2}\frac{\omega_u C_t}{\eta_v} \tag{5.10}$$

The equation will give a quick estimate over the amplifier's power consumption, one will later use it to determine other design variables. Moreover, the equation does not include noise and distortion cancellation conditions.

The load resistance (R_{L2}) is then determined by manipulating equation 5.6b:

$$R_{L2} = \frac{1}{2}\frac{V_{dd}}{I_d} = 4\frac{\mathrm{HD}_2}{V_m}\frac{V_{dd}}{\omega_u C_t} \tag{5.11}$$

One will now introduce the requirement to carry out noise cancellation, which was given by equation 4.15. The gain for the CG-stage could be simplified and approximated as $A_{cg} = \frac{R_{L1}}{R_s}$. Thereupon, the cancellation term could be expressed as:

$$g_{m3} = \frac{A_{cg}}{R_{L2}} \tag{5.12}$$

The transconductance g_{m3} is then iterated according to expression 5.12 and not from the unity gain requirements. One should expect a healthy growth in transconductance due to the iteration. The power consumption should ultimately be limited by the load (R_{L2}) and should remain somewhat unchanged after iteration.

However, the common mode voltage is likely to be skewed towards ground, therefore increasing the total power consumption for the CS-amplifier.

Noise factor was given by equation 4.48. The expression being unwieldy could be manipulated by neglecting the gm-boosting of M_2 ($M_{2vgs} = 0$) and thus setting $V^{+2}_{tnrl2} = V^{-2}_{tnrl1} = V^{+2}_{tnm3} = V^{+2}_{fnm3} = 0$. The following approach yields:

$$F = 1 + \left(\frac{1}{4kTR_s\alpha^2}\right)\left[4kT\left(R_{L1}g_{m2}r_a + R_{L2} + \gamma g_{m3}R_{L2}^2\right) + \frac{(g_{m3}R_{L2})^2\kappa}{W_3L_3C_{ox}f}\right] \quad (5.13)$$

The noise from R_s was previously written as $V^{diff^2}A_{balun}$ and was given by equation 4.44. The first part of the equation corresponds to the gain of the CG-stage, whilst the later refers to the gain of the CS-stage. Assuming that both stages have the same magnitude of gain and by using the simplified gain expression for the CG-stage, total gain for the Balun-LNA could be written as $A_{balun} = 2A_{cg} = \frac{2R_{L1}}{R_s}$ Moreover, equation 5.12 is manipulated and inserted. Consequently, α could be rewritten as $\alpha = R_{L1}(g_{m2}r_aR_{L2}g_{m3}+1+g_{m1}r_a+g_{m2}r_a)+g_{m3}R_{L2}(R_{L1}+r_a) = 2R_{L1}$. The following yields:

$$F = 1 + \left(\frac{1}{4kTR_sR_{L1}^2}\right)\left[4kT\left(R_{L1}g_{m2}r_a + R_{L2} + \gamma g_{m3}R_{L2}^2\right) + \frac{A_{cg}^2\kappa}{W_3L_3C_{ox}f}\right] \quad (5.14)$$

Thermal noise and flicker noise is phased out, and the previous assumptions done for equation 5.14 are assumed to be applicable. It is seen that R_{L1} should be set large, and R_{L2} should be sat small in order to minima the noise factor. Flicker noise is frequency and area dependent, and could be minimized by sizing the area of M_3. The size of the transconductance of M_3 is relatively large due to the cancellation term (equation 4.15). Moreover, it is therefore likely that thermal noise of M3 will dominate the noise figure. The noise sources and their relations to the noise factor will be exemplified in the results chapter.

5.4 Design Approach

Equation 5.4 R_{L1} is determined by bandwidth and the load capacitance. The amplifier is loaded with an ADC with a input capacitance of $256f$F. Furthermore, it is assumed that an extra parasitic capacitance of $10f$F is to be placed in parallel

with the load. The cutoff frequency ω_{-3dB} is given as 11.5MHz. Additionally, R_s is fixed to 10k.

$$R_{L1} = \frac{1}{\omega C_t} = \frac{1}{2\pi \times 11.5 \times 10^6 \times 266 \times 10^{-15}} \approx 53k\Omega \tag{5.15a}$$

$$A_{Cg} = \frac{R_{L1}}{R_s} \approx 5.3\times \tag{5.15b}$$

$$P_d = \frac{1}{8} V_{pp} \frac{V_m}{\text{HD}_2} \frac{\omega_u C_t}{\eta_v} \approx \frac{800mV}{8} \times \frac{25mV}{\text{-40dB}} \times \frac{2\pi \times 40 \times 10^6 \times 266 \times 10^{-15}}{25\%} \approx 67\mu W \tag{5.15c}$$

$$R_{L2} = \frac{1}{2} \frac{V_{dd}^2}{P_d} = \frac{1}{2} \times \frac{1}{67\mu W} \approx 7.5k\Omega \tag{5.15d}$$

$$g_{m3} = \frac{A_{cg}}{R_{L2}} \approx \frac{5.3}{7.5k\Omega} \approx 706\mu S \tag{5.15e}$$

V_{pp} is the peak to peak of the output, which should be rail-to-rail but chosen lower due to non-zero saturation voltages, thus $V_{pp} = 0.8V$. V_m is the input signal from the Taylor series from equation 2.13, one assumes $V_m = 25mV$. C_t was determined by the A/D Converter as one did for the CG-stage, $256fF$ and HD_2 was specified as greater than -40dB from the thesis outline. R_{L2} could be related to the idle current as one did in equation 5.6b, and found in equation 5.15d.

5.4.1 Power vs Noise

The method described in the foregoing paragraph yields excellent results as one will later see. However, a substantial amount of energy could be saved by easing the noise cancellation term. All of the design parameter are fixed, whilst R_{L2} is swept over conceivable values. The transconductance of M_3 is plotted and both simulated and calculated by equation 5.15d in figure 5.1. Moreover, the noise figure is plotted with only noise contributions from R_{L1}, R_{L2}, M_1 ,M_2 and M_3.

Consequently, one sees in figure 5.1 that one could deviate from the noise cancellation term, save power and still achieve a superb noise figure. $R_{L2} = 7.5k\Omega$ has a difference in calculated and simulated transconductance of $\Delta = 9.7\mu$. This gives a Noise figure of 1.89dB. However, when $R_{L2} = 14k\Omega$, one gets a differance of $\Delta = 262.9\mu$, which corresponds to a Noise figure of 2.15dB.

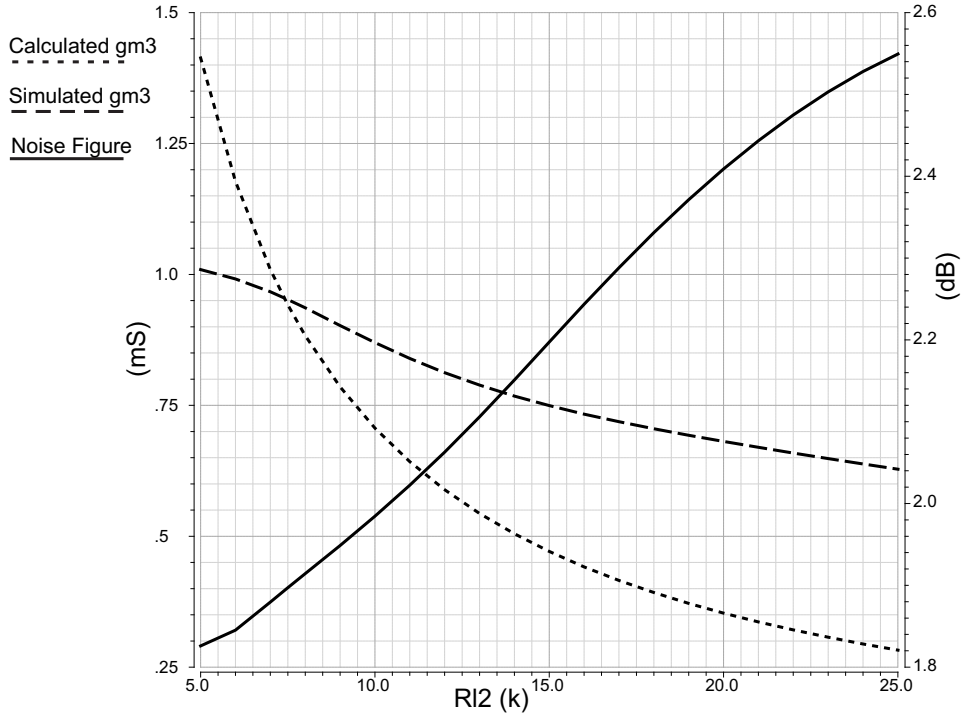


FIGURE 5.2: Noise figure with noise only from R_{L1},R˙L2 M_1 ,M_2 and M_3, and drain current of M_3 plotted with respect to R_{L2}.

One should however notice that the plot does not entirely correlates the preceded findings one did in equation 5.15. This is because the plot includes the biasing resistor denoted as I_{b2} in figure 5.4, which comes in parallel with R_s and thus lowering g_{m3}. $I_{b2} = 27k\Omega$, including $g_{m3} = \frac{R_{L1}}{R_{L2}(R_s \| R_b)} \approx 968.4\mu S$.

The expression for the noise factor given by equation 5.14 is still to ungainly as a design equation. $\frac{\kappa}{C_{ox}}$ is simulated and found to be $\frac{\kappa}{C_{ox}} \approx 1.82 \times 10^{-10}$. The other design variables are given by equation 5.15. One assumes that M_3 has an large area, like $\frac{15\mu m}{0.1\mu m}$. Thus, giving:

$$F = 1 + \left(\frac{1}{4kTR_sA_{cg}^2}\right)\left[4kT\left(R_{L1} + R_{L2} + \gamma A_{cg}R_{L2}\right) + \frac{A_{cg}^2\kappa}{W_3L_3C_{ox}f}\right] \quad (5.16)$$

If $R_{L2} = 7.5k\Omega$ then $F \approx 1.47$ and when $R_{L2} = 14k\Omega$ $F \approx 1.53$

Comparing the theoretical findings with all the assumption one did with the simulated results, one sees that degradation of Noise Factor primarily is due to increased thermal noise from increasing R_{L2}.

TABLE 5.1: Noise figure with noise only from R_{L1},R˙L2 M_1 ,M_2 and M_3, and drain current of M_3 plotted with respect to R_{L2}.

R_{L2}	Simulated	Calculated
$7.5k\Omega$	1.88dB	1.67dB
$14k\Omega$	2.13dB	1.85dB

5.4.2 Figure of Merit

Previous mathematical endeavors have made it possible to calculate a simplified design FOM. The FOM design equation only looks at thermal noise, and assumes perfect noise cancellation. Moreover, the gain for LNA is approximated as $2 \times A_{cg}$, and the power consumption as $P_{total} = \frac{1}{2R_{L1}} + \frac{1}{2R_{L2}}$. Furthermore, the DR of the amplifier is assumed to be limited only by distortion. Thus by inserting equation 5.14 into 5.2, the following could be approximated:

$$\text{FOM} \approx \frac{1}{4} \times \frac{(R_{L1} + R_{L2})(R_{L1}^2 + R_s R_{L1} + R_s R_{L2} + \gamma R_{L1} R_{L2})^2}{R_{L1}^6 D_R^2 R_{L2} \times B} \tag{5.17}$$

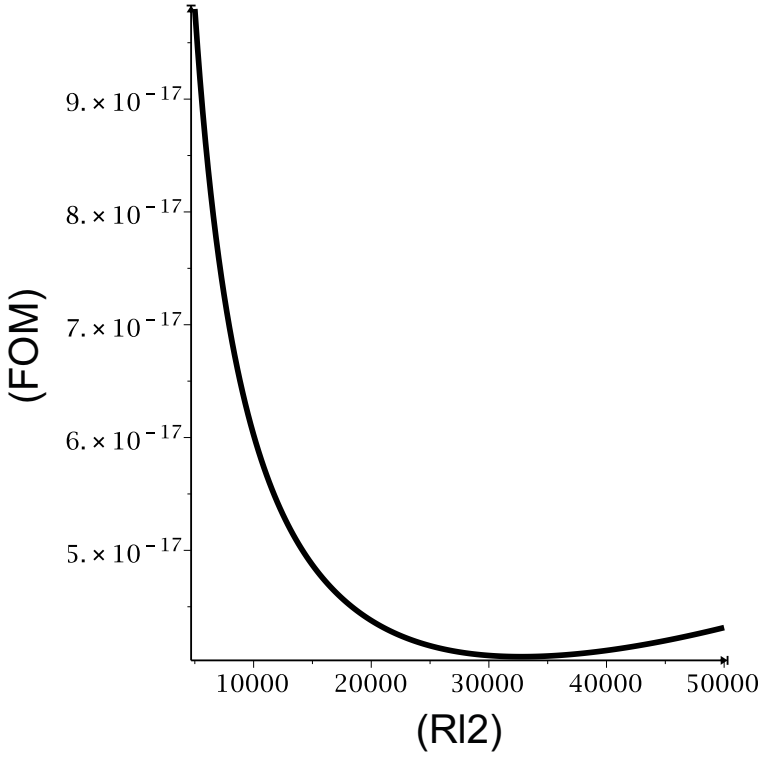


FIGURE 5.3: FOM definition from equation 5.17, is plotted vs R_{L2}

The following is kept constant at: B=16MHz, DR=-40dB, $R_{L1} = 53k\Omega$, $R_s = 10k\Omega$ and $\gamma = 2/3$.

The FOM definition from equation 5.17, is plotted vs. R_{L2}. Figure 5.3 shows a tendency towards a sweet-spot for the FOM optimization. It is likely that such a region exists. Nontheless, it is highly unlikely that the sweet-spot is given entirely by the approximated FOM equation. The main problem is that the noise factor expression assumes perfect cancellation. Even so, perfect noise cancellation only occurs for one value of R_{L2}. It is therefore likely that the real minima is somewhat shifted towards left. Likewise altering R_{L2} will skew the common mode voltage thus making the power consumption estimate somewhat generous. FOM is dictated entirely by power consumption until right around $R_{L2} = 35k\Omega$. As R_{L2} grows, thermal noise from the same resistor starts to pose a major contribution, and thus governs FOM. However, it is improbable that the actual FOM is limited by thermal noise from R_{L2}, but rather the amount one can deviate from the noise cancellation term.

5.5 Programmable-Gain

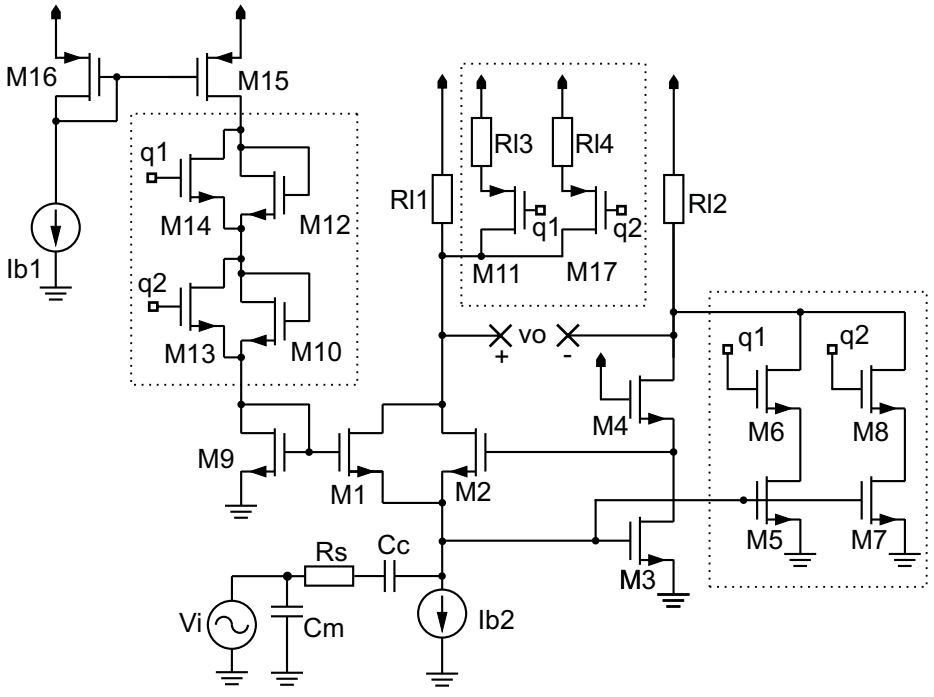


FIGURE 5.4: Noise sources present due to thermal and flicker noise for the proposed design.

The complete design in figure 5.4 proposes a digital stepwise gain control. The gain is controlled by setting two digital pins q_1 and q_2. The gain is mainly controlled by

altering the load of the CG-amplifier (R_{L1}). The load is altered switching resistors in parallel with the load. R_{L3} and R_{L4} are controlled by M_{11} M_{12}.

However, the CS-amplifier is biased by the quiescent current flowing through the CG-amplifier. Thus, V_{gs} for CS-amplifier is increased when R_{L1} is reduced, causing the positive output (V_{op}) to be pulled towards ground. The transconductance of the CS-amplifier is altered in order to counteract the operational changes introduced by the gain control. The alteration of the transconductance is done by using several transistors in parallel that are controlled by switching the cascoding transistors. The transconductance of the CS-stage is given by g_{m3} , g_{m5} and g_{m7}, and altered by switching M_6 and M_8.

Cancellation was dependent on R_{L1}/g_{m3} it is therefore desirable that the two are reduced at the same rate. In order to combat the degradation of NF, one therefore alters the current mirror reducing the biasing voltage of $M1$. A reduction in the bias voltage further reduces the biasing voltage for the CS-amplifier thus reducing the transconductance of the CS-amplifier. This provides a significant improvement in noise figure. $V_{gs_{m3}}$ is altered by manipulating the current flowing in the biasing branch. M_{14} and M_{13} switches M_{12} and M_{10} which are diode-coupled with an impedance of $1/g_m$. M_{12} and M_{10} are sized different so that adequate $V_{gs_{m3}}$.

CHAPTER 6

Design and Layout

The following chapter presents the final design and values based on the theoretical analysis. Furthermore, the layout for the design is presented.

6.1 Schematic

The amplifier is firstly implemented in a CMOS technology on a schematically level. The amplifier is designed according to the design methodology presented in chapter 5.3. The design parameters were firstly calculated based on the theoretical analysis given. Furthermore, the amplifier is then FOM optimized by trading noise performance with power, as one given in figure 5.3. The stages are biased as well as optimized by iterating the parameters.

The final component parameters for the design are given. Critical device parameters are given in table 6.1, whilst more arbitrary and iteration obtained devices are given by 6.2. Passive components although critical are denoted on the schematic, given by figure 6.1.

TABLE 6.1: Transistor parameters for the amplifier.

Device	Description	g_m/I_d	W (μm)	L (μm)	Mfing	I_d (μA)
M_1	CG bias	24.79	12	0.18	6	9.5
M_2	CG boosted	30.1	0.9	0.18	1	0.033
M_3	CS Input	22.4	10	0.1	5	18.75
M_4	Cascode CS	3	10	0.18	5	$-\|\|-$
M_5	Switched CS Input	22.3	8	0.1	4	14.55
M_6	Switched Cascode CS	3.1	4	0.18	2	$-\|\|-$
M_7	Switched CS Input	22.4	6	0.1	3	10.46
M_8	Switched Cascode CS	3.1	4	0.18	2	$-\|\|-$

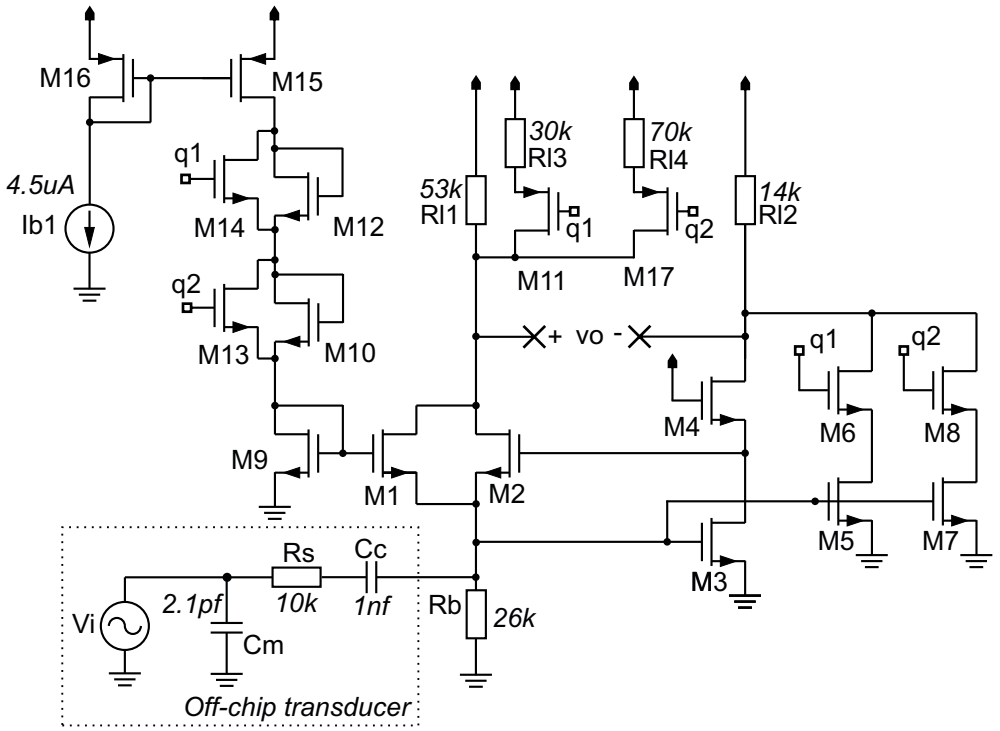


FIGURE 6.1: Schematic with passive component values

TABLE 6.2: Transistor parameters for the amplifier.

Device	Description	g_m/I_d	W (μm)	L (μm)	Mfing	M	I_d (μA)
M_9	Current-Mirror 1/2 (M_1)	7.6	0.18	0.18	1	1	1.57
M_{12}	Diode-Coupled	-	0.18	0.18	1	2	-
M_{10}	Diode-Coupled	-	0.18	0.18	1	1	-
M_{11}	Switch	-	0.18	0.18	1	1	-
M_{17}	Switch	-	0.18	0.18	1	1	-
M_{13}	Switch	-	0.18	0.18	1	2	-
M_{14}	Switch	-	0.18	0.18	1	2	-
M_{15}	Current-Mirror (1/2)	16	4	0.1	2	1	4.5
M_{16}	Current-Mirror (2/2)	16	1	0.1	2	1	9.9

6.2 Layout

The design is transferred to layout when the amplifier performers as desired on a schematic-level. Layout introduces resistive loss and parasitic capacitances, mismatch as well as other non-idealities. The layout is then further iterated in order to combat previous effects.

6.2.1 Pad Ring

The bond ring is used for connecting bond wires between die (wafer) and the package. The bond wire will introduce approximately an inductance of 1nH, which is a general rule of thumb. The pad by itself will have a capacitance to ground of approximately 1pF. Each pin has therefore a shunt capacitance and a series inductor.

6.2.2 Layout

The layout of the proposed design is shown in figure 6.2. Two metal layers are used where M1 is going vertical and M2 horizontal. This should ideally be the other way around since thats the common practice. However, one chooses to do so because it required less routing.

Critical layers should only propagate in one direction, preferably with a constant pitch as given in chapter 2.6.2.1. In the design, poly only flows in the vertical direction. The pitch however is not constant throughout. Partly because of the number of different device size and thus number of fingers, and part make an easier design. Gates are made of poly, and number of finger corresponds to number of gates.

The entire design uses device known as Lewyn-structures. Lewyn-structures [8] use a partial guard ring. Substrate contacts are situated along both sides in a vertical fashion of the device. This design approach greatly reduces threshold variations due to WPE as discussed in chapter 2.6.2.2. However, in order to actually avoid WPE the well distance from gate should be greater than 2μm. Two devices with a different distance that is less than 2μm to the well, will have different threshold voltages (V_{th}) and therefore difficult to match. The left top corner of the layout under the load resistors sports a P-channel current mirror. The following current mirror does not have a well distance greater than 2μm. However, one will later see in chapter 7 that mismatch does not appear to be an issue for noise cancellation. The same applies to the two P-channel switches situated in the center, just below the equal load resistors. The switches operate in either cutoff or saturation, and since $V_{eff} < V_{dd}$ making WPE negligible.

The amplifying devices of the design are quite large, and a general rule of thumb is to add an extra finger for every 2μm of the length. Meaning that a device with a width of 12μm should have 6 fingers. The thumb finger rule combatant what is known as STI (chapter 2.6.2.3), which causes leakage and alteration of the threshold voltage. Moreover, multifinger devices could possibly have less parasitic capacitance.

Devices of equal physical size will be distorted in an equal fashion due to process variations. Consequently, matched devices should have the same gate length. Moreover, number of fingers should also be equal for a matched pair. The current mirror in figure 5.4 and at layout 6.2, consists of transistor M_9 and M_1. M_1 is heavily saturated, and relies on a large ratio in order to achieve a sufficient bias current. Since one are not interested in burning, unnecessary effect in the copying branch. Because of the large ratio M_1 is multi finger device and M_9 single finger. Notwithstanding, as previously stated, one will later see in chapter 7 that mismatch does not appear to be an issue for the proposed design.

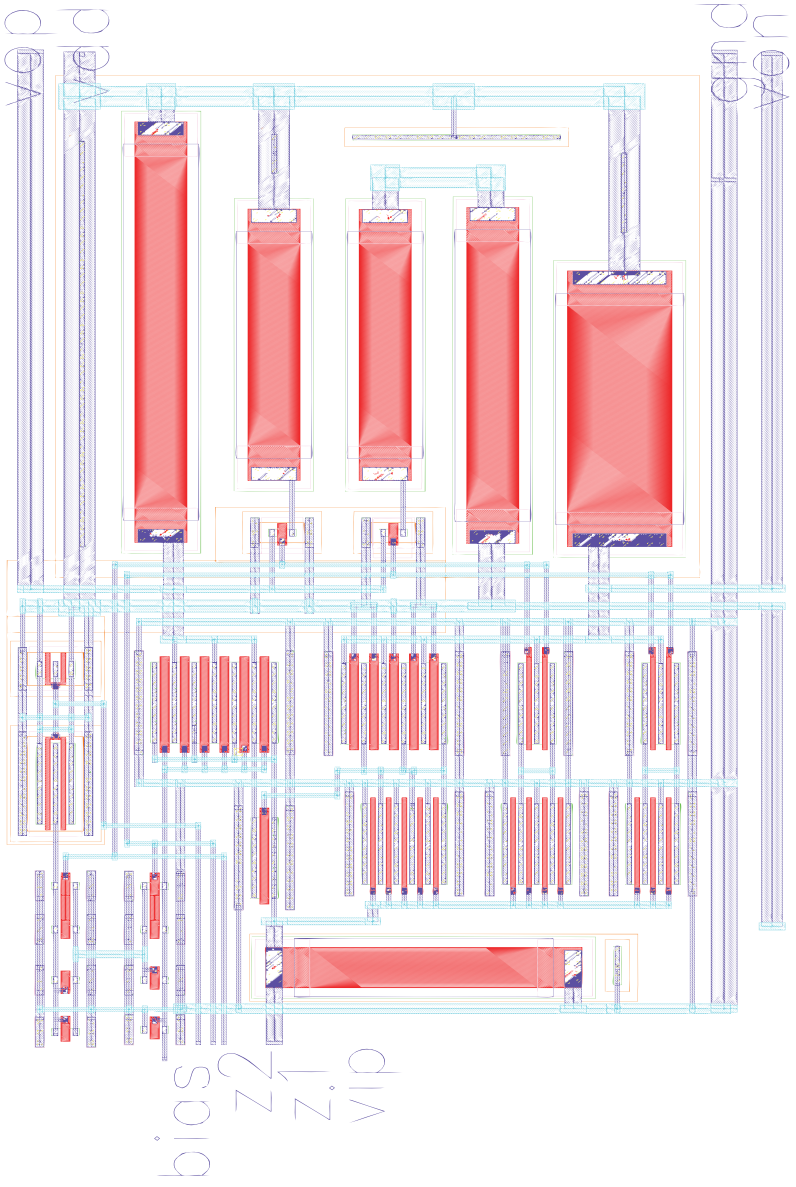


FIGURE 6.2: Complete layout for the proposed design.

CHAPTER 7

Results

The following chapter presents the results for the proposed design. All of the results include parasitic capacitances and resistances extraction from the layout. Firstly, one starts by explaining the different test benches and methodology. The chapter then continues by presenting the final results and, an yield estimate is given.

7.1 Test Setup

The theory is verified using state-of-the-art simulation tools and vice versa. The topology was carefully examined with a thoroughgoing design mythology. Firstly the transistors are biased using a DC-analysis, and verified that they are operating under thought conditions. Iterations may be necessary in order to get correlation between theory and simulated results. The frequency response is then found by performing an AC-analysis.

The results are obtained from a number of test benches given in the appendix (CUNT) summary of the test benches as well as what they do are given in the following table:

TABLE 7.1: The different design goals, as well as the respected test benches and analysis.

Goal	Analysis
Operation point	DC
Power Consumption	DC/AC
Bandwidth ω_{-3dB}	AC
Noise Figure	SP
Input Impedance	SP
Large Signal Gain	PSS
HD_2	PSS
IM_3	QPSS
SNR/DR	Tran
PSRR	Xf

7.1.1 Large-Signal Analysis

The Single-Tone test and its metrics was elaborated upon in chapter 2.3.1. ***Periodic Steady State*** (PSS) is a large signal analysis, which finds the steady state response of the circuit. Executing such an analysis linearizes the circuit about a time varying operation point. PSS is mainly used to find HD_2. The findings are validated by taking a Fast Fourier transform of an transient analysis (small signal), and then applying the definitions given in chapter 2.3.1. Moreover, PSS is also used to determined large signal gain for the amplifier. ***Quasi Periodic Steady State*** analysis is a multi-frequency PSS, and works in a similar manner. IM_3 was defined in chapter 2.3.2 and obtained by performing a QPSS analysis.

7.1.2 Small-Signal Analysis

Transient analysis is a time dependen analysis. Coherent sampling forces an integer of input cycles within the sampling window. Thus, assures that the signal power of the FFT is contained within one bin. The results are exported, and use by an external script. Performing an FFT of the exported results, one is able to determined SNR, DR, HD2 and ENOB. SNR and HD_2 is validated by single-tone test, and DR and ENOB through an windowing FFT.

Scatter parameters or S-parameters are a small signal steady state analysis. S-parameters are used to extract the VSWR, which again is used to determine the input impedance $Z_{inn} = \frac{Z_L}{\text{VSWR}}$ [6]. The noise factor could also be found by

using S-parameters. Noise factor is obtained by using a small signal s-parameter analysis. To verify the simulated noise factor and to find out how the simulator comes about with the noise factor, additional simulations were done. One could claim that $F = \frac{\text{Total noise for the amplifier}}{\text{Noise generated by } R_s}$. Thus, the F from the simulator was verified by using another type of simulator.

XF is a transfer function analysis, and linearizes the circuit about the DC operation point. The analysis computes the transfer function from every independent source to the output of the circuit. Power supply rejection ratio was previously defined in chapter 2.5, as a measurement for output error in respect to power supply changes.

7.2 Results Overview

The amplifier is simulated as one previously described in subchapter 7.1. The specifications is given for the thesis and is shown for the amplifier in table 7.3. A test tone of either 5.17578125MHz or the preceding tone including 5.27578125MHz is applied to the amplifier with amplitude of 50mV.

The amplifier is either fixed loaded or dynamic loaded dependent on the analysis. Steady state analyses and/or two-tone tests uses fixed loads of 256fF. For more realistic results and implementation, the amplifier is loaded by a sampling A/D converter running at 50Msps. The amplifiers output is therefore either loaded with 256fF or floating, at 50MHz.

The results are plotted in appendix: FFT with fixed load in figure B.1 , FFT with dynamic load in figure B.2 , PSS in figure B.3, QPSS in figure B.4, VSWR in figure B.5, Bandwidth in figure B.6 and NF in figure B.7.

Table 7.2: Simulated results overview for the proposed design

Parameter	Fixed Load	Dynamic Load	
Power	67.2*	-	μW
Gain	14.9*	15.1*	dB
BW	11.32*	11.32*	MH_Z
NF	2.98	-	dB
NF_{min}	2.39	-	dB
SNR	74.06	61.17	dB
Enob	8.07	5.7	b
DR	50.35	36.31	dB
HD_2	- 56.63	- 36.37	dB
IM_3	- 41.47	**	dB
THD	62.43	60.52	b
PSRR	2.6	-	dB
Z_{inn}	3k8	3k8	Ω
Area	375	-	$\mu^2 m$

* Dependent on gain setting (g_1 and g_2), referring to table 7.7

** Transient with Coherent Sampling theorem therefore no two-tone test is available.

TABLE 7.3: Amplifier Specification

Power	<100	μW
Gain	>10	dB
BW	>10	MH_Z
NF	<3	dB
SNR	>50	dB
DR	>40	dB
HD_2	<-40	dB
IM_3	<-40	dB
Z_{inn}	¡5k	Ω

7.2.1 Noise Behaviour

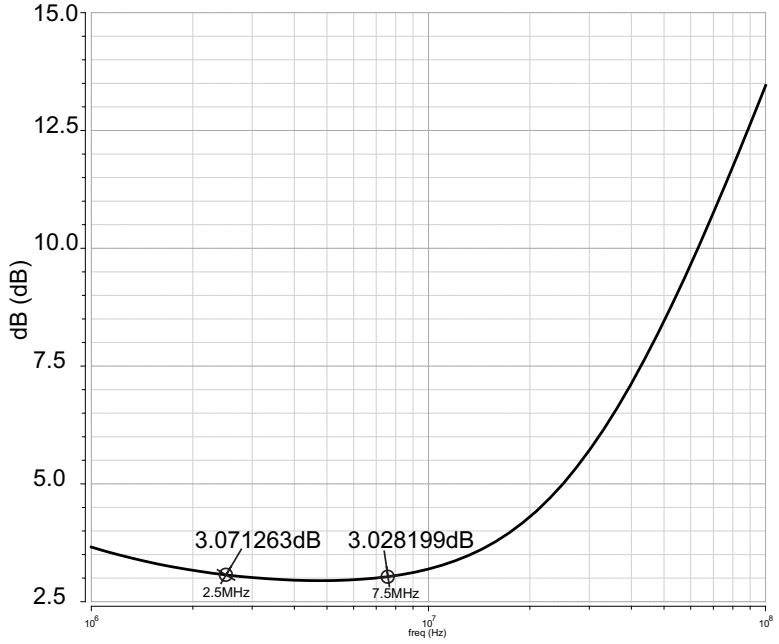


FIGURE 7.1: Noise Figure plotted for the amplifier

The noise factor is simulated with extracted parasitics as previously explained in subchapter 7.1.2. Noise factor as a function of frequency is plotted in figure 7.1. The amplifier has a 100% bandwidth at 5MHz. The figure sports NF of 2.98dB with a minima at $\approx$ 5MHz. NF raises ever so slightly from center to the endpoints, which is given by the bandwidth span at 2.5MHz to 7.5MHz. Noise figure near the endpoints exceeds the specification ever so slightly with a Δ of only 0.07.

7.3 Yield Estimate

The yield is determined by mismatch and process variation as ubiquitously described in the layout chapter. A series of runs are executed. Each run uses randomly generated yield/mismatch variables according to statistical-distribution. The desired simulations are then performed on the basis of the acquired yield/mismatch variables. The results of each run is evaluated against the target goal.

Table 7.4 shows 60 random Monte Carlo runs for the proposed design. The Monte Carlo runs include mismatch and process variations. Moreover, the runs are performed on a layout-level. Consequently, parasitic capacitance and resistance from the layout are extracted and added to the original schematic.

TABLE 7.4: 60 Monte Carlo runs with mismatches and process variations, performed on the layout.

Goal	MIN	MAX	MEAN	σ
Bandwith ω_{-3dB}	11.11MH$_z$	11.56MH$_z$	11.3MH$_z$	75.09k
Noise Figure at 5MH$_z$	2.942dB	3.024dB	2.982dB	17.73m
ENOB*	6.351b	7.817b	7.313b	415.7m
HD$_2$	-40.52dB	-78.62dB	-51.8dB	7.25
IM$_3$	-38.17dB	-52.39dB	-42.48dB	3.154
VCM$_p$	495.5mV	537.5mV	516mV	9.602m
VCM$_n$	285mV	450mV	378.9mV	41.87m

*ENOB found by fast Fourier transform with windowing.

TABLE 7.5: 10 Monte Carlo runs with only mismatches, performed on the layout.

Goal	MIN	MAX	MEAN	σ
HD$_2$	-40.52dB	-81.53dB	-54.12dB	13.01

7.4 HD_2-Suppression

The introduction of the gm-boosted device (M_2) as feedback provides superb HD_2-Suppression. The conventional CGCS-Balun achieves a typical HD_2 of $\approx$ -40dB [11]. However, the proposed design acquires an HD_2 of $\approx$ -56dB, after layout. Figure 7.2, shows g_{m3} and HD_2 plotted vs. the width of M_2. Note that the HD_2 is plotted and simulated on a schematically-level and does not take parasitics into account. Consequently, the circuit after layout is not optimized towards second harmonic suppression, and should be iterated for further enhancement of second harmonic suppression.

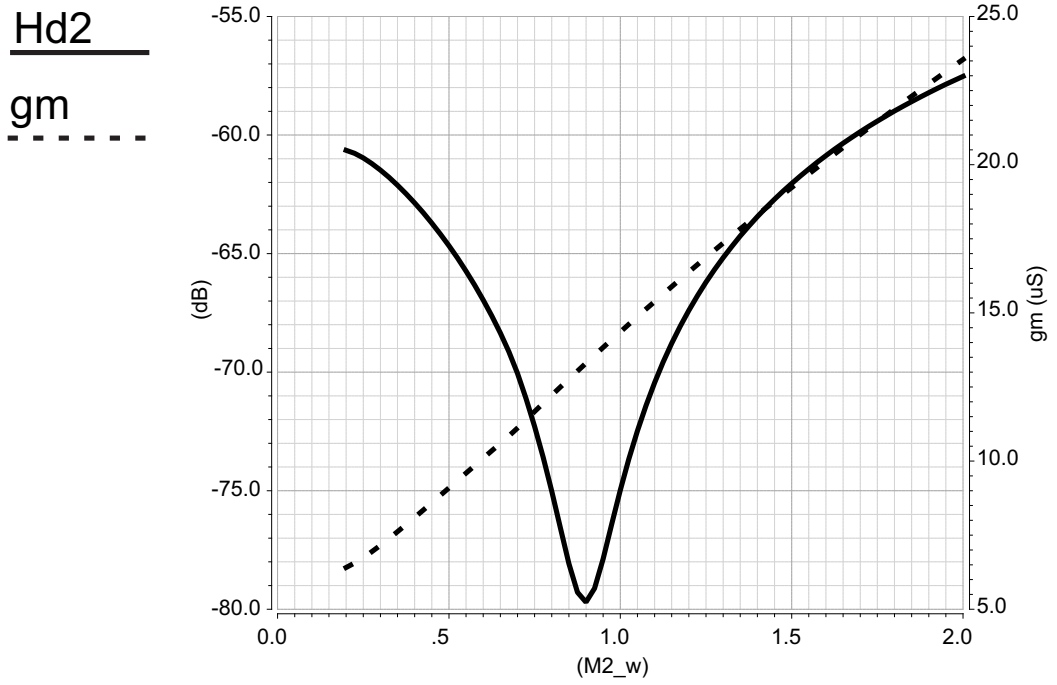


FIGURE 7.2: HD_2-Suppression

The proposed and the conventional CGCS-Balun-LNA was shown in figure 4.1, and are compared in table 7.6.

TABLE 7.6: HD_2/IM_3-Suppression for conventional and proposed CGCS-Balun.

		Proposed		
Parameter	Conventional	Schematic	Layout	
HD_2	-53.91	-79.8	-56.63	dB
IM_3	-40.15	-40.38	-41.47	dB

7.5 Programmable-gain

Bandwidth and Noise Figure is plotted with the different gain-settings for the amplifier in appendix figure: B.6 and B.7.

Table 7.7: Programmable-gain

g_1	g_2	Gain [dB]	NF [dB]	NF_{min} [dB]	BW [MHz]	Power [μw]	Z_{inn} [kΩ]
1	1	14.34	2.98	2.39	11.32	67.2	3k80
0	1	12.68	3.295	2.63	19.46	50.2	1k80
1	0	9.16	4.21	2.87	25.69	39.9	1k50
0	0	7.53	4.244	3.47	38.36	35.5	1k25

All of the above results were given with an input signal of 50mV. One wishes probably to reduce the gain because of increased input signal. An input signal of 100mV is therefore applied to the amplifier in table 7.8.

Table 7.8: Programmable-gain with 100mV amplitude applied to the amplifier.

g_1	g_2	SNR	ENOB
1	1	71.16dB	5.5b
0	1	71.24dB	4.4b
1	0	74.97dB	5.8b
0	0	71.16dB	5.5b

Table 7.9: Alterations in the amplifier specifications because of the programmable gain.

g_1	g_2	g_m* [μS]	$\frac{R_{L1}}{(R_s \times R_{L2})}$ [μS]	$V_{gs_{m1}}$	$V_{gs_{m3}}$
1	1	878	504	0.257v	0.224v
0	1	697	287	0.225v	0.229v
1	0	665	182	0.113v	0.219v
0	0	562	143	0.079v	0.239v

CHAPTER 8

Discussion

This chapter discusses and compares the previously obtained results with the design methodology.

The final design satisfies the design parameter provided for the thesis.

8.1 Resoultion

Enob for the amplifier with a fixed load is 8b as reported in table 7.2. However, an average enob of 7.3b was given in by the yield estimate (table 7.4). The dissimilarity in enob can probably be explained, by the results being obtained differently. The lesser enob of 7.3b was found by a windowing FFT. The window weights the samples so that the signal power is partly within an FFT-bin. Coherent sampling on the other hand is more accurate, and ensures that the total signal power is within each bin. Hence 8b from coherent sampling is believed to be a more accurate result.

The amplifier is loaded with a sampling A/D converter with 256fF input. Comparing the FFT plot of the amplifier statically loaded in figure B.1 vs dynamically loaded in figure B.2. One sees that the second harmonic spur is quite larger when loaded with an AD. The A/D converter without the amplifier already has a significant second harmonic distortion. And is presumably the cause of the increased HD_2. The amplifier is an LP-filter, and one could move the cutoff frequency further down by adding additional load capacitance to the amplifier.

HD_2 was found to be -56.63dB with a fixed load and - 36.37dB when loaded by an A/D converter, both is well within specifications. HD_2-Suppression could be

additionally optimized at a layout level for aggrandized results. Although one do experiences issues with maintaining outermost HD_2- suppression. The fluctuation in HD_2 is apparently due to mismatch, from table 7.5.

IM_3 suppression is sadly not maintained under -40dB through all of the mismatch runs. However, an average of -42.48dB and standard deviation of 3.154.

8.2 FOM

One defined a FOM in order to better optimize the design in terms of the different tradeoffs encountered in analog design. FOM was given by equation 5.2, inserting the simulated results previously obtained, one could calculate FOM to 4.2×10^{-17}. The following simulated results corresponds to the theoretical FOM one plotted in figure 5.3. From the figure one sees that a R_{L2} of 14k gives a FOM of 5×10^{-17}. The theoretical plot assumes perfect cancellation and cancellation declines with increased R_{L2}. Best FOM is therefore not necessarily obtained at 32k, and is probably somewhere around the final design.

8.3 Small-Signal

Bandwidth was conditioned by the common-gate stage. Bandwidth of 11.3MHz surpasses the requirement of 100% relative bandwidth at 5MHz, and conforms to the estimated bandwidth of 11.5MHz given by the design methodology in equation 5.15. Yield estimates sports a standard deviation of 75k, the lowest cutoff frequency is found to be 11.11MHz. The difference between the estimated and the simulated bandwidth is probably because of the parasitic capacitances, as well as errors introduced due to simplification of the analysis.

8.4 Noise figure

Noise figure of 2.98dB is just within specifications. The noise figure is thoroughly neglected whilst attaining specifications and simultaneously increasing efficiency.

Better noise figure could easily be obtained for other more noise sensitive applications, by degrading FOM. That was elaborated upon in the design methodology, chapter 5.4.2. Yield estimated noise figure gives a peak of 3.024dB at center, with a standard deviation of 17.73m. It is believed to be sufficient and within a reasonable discrepancy. Band of interests spans from 2.5MHz to 7.5MHz with a noise figure exceeding the specifications ever so slightly in figure 7.1. However, the results are acceptable with a deflection of only 0.07dB.

8.5 PSRR

The design achieves a poor PSRR of 2.7dB. PSRR is generally not a problem for differential circuits as both sides uses the same valued loads, transistors etc. However, this is not the case for the Balun-LNA. The amplifier is lopsided in terms of both load and transconductance of both stages, note that $R_{L1} \approx 3.5R_{L2}$. PSRR could be improved by the use of a regulator, since PSRR for the circuit would be given by the regulator and not the amplifier.

8.6 Programmable-Gain

The results for the variable gain was given in table 7.7. The proposed programmable-gain scheme alters the load. Moreover, noise and distortion cancellation is dependent on R_{L1}, as ubiquitously shown in chapter 4.3.1. Therefore, a reduction in R_{L1} tarnishes both distortion and noise cancellation.

Noise figure decreases with gain, as seen in table 7.7. The problem is exemplified in table 7.9. g_m* is simmulated g_{m3} for the circuit, whilst $\frac{R_{L1}}{(R_s \times R_{L2})}$ is the calculated g_{m3} given by the noise cancellation term of equation 4.15. Moreover, a small difference between the two is attainable and desirable for FOM optimization as shown in chapter 5.4.2. Consequently, NF is decreased because of the increased difference.

The programmable gain works by choking the gain. However, it is reasonable to believe that one desires a reduction in gain because of increased input voltage (increased fundamental). Therefore, one could have poorer noise characteristics and still achieve adequate SNR. On the other hand, increasing the input signal or

V_m does increase HD_2, from equation 4.29. The decreased linearity of CS, because of increased V_m is likely the cause of the degradation of enob one sees in table 7.8. Better manners to introduce variable gain would example be the attenuate the input signals swing whilst maintain gain. The attenuation could easily be implemented in front of the amplifier, and capacitive ladder would be the most excellent of choices.

Naturally, the bandwidth is increased because of the reduction of the load seen in equation 5.15. The input impedance for the Balun-LNA was given by equation 4.9, and decreasing the load decreases the input impedance.

8.7 Mismatch

Yield was estimated based on Monte Carlo runs and given in table 7.4. Although some of the samples are outside of the given specification, deviations are within reasonable expected limits. The culprits are believed to be mismatch because of careless implementation of both the current mirrors.

Current mirror consisting of $M15$ and $M16$ has a g_m/I_d of 16, and should be further saturated with a g_m/I_d of typically around 5. Moreover, the current mirror has a well distance less than 2μm (chapter 6.2.2) and both devices has different well distance. It is great possibility that the mirror is a fault source for the deviation in yield given in table 7.4.

To further avoid mismatch in a current mirror, should both devices have an equal amount of fingers. However, this is not the case for the current mirror consisting of $M1$ and $M9$. Because of the lavish current ratio in the mirror, equal finger ratios are not possible. Presumably, giving the origin of the deviation shown in the yield estimate.

CHAPTER 9

Conclusion

A design of a $sub-70\mu W$, $sub-3dB$ noise figure amplifier for ultrasound imaging applications has been proposed. The amplifier is tuned towards low power and low noise. The amplifier is optimized to be loaded with a high-resolution A/D-converter. The design is based on the CGCS-Balun, but also employs HD_2-suppression by gm-boosting the CG-stage of the amplifier, achieving a superior HD_2, when compared to a conventional CGCS-Balun. Programmable-gain architecture has also been proposed.

The topology is theoretical analyzed, and an expression for the noise factor has been derived. An expression for thermal/flicker-noise cancellation has been derived. Distortion originating from the CG-stage has been analyzed. Moreover, it is proven that the performance of the topology is independent of the CG-stage, assuming perfect cancellation. A comprehensive theoretical design methodology has been coined on the analysis. Furthermore, a Figure-of-Merit optimized towards low noise and low power consumption has been defined. The amplifier is designed and optimized based on the Figure-of-Merit. Recent published works was then compared based on the Figure-of-Merit.

A 65nm CMOS layout based on Lewyn structures has been created for the amplifier, and paracitics and restive loss from the layout has been extracted to schematic. Results are given with the following layout effects.

The final design surpasses all of the specifications given by table 7.3.

The amplifier achieves a power consumption of $67.2\mu W$, a dynamic range of 50.35dB, Noise figure of 2.98dB, HD_2 of -56dB at layout. Yield was estimated based on Monte Carlo simulations, and the design sports although at times very varying, excellent results within the provided specification.

9.1 Comparison with recent published works

TABLE 9.1: Comparison with recent published works

The proposed design is compared with recent published ultrasound front-end amplifiers in table 9.1. FOM definition was given by equation 5.2 and is calculated for the amplifiers for easier comparing.

	Power $[mW]$	Gain $[dB]$	BW $[MHz]$	NF $[dB]$	DR $[dB]$	FOM
[15]	20.3	20.5	100	4.9	-	$1.79 \times 10^{-13} **$
[16]	-	77.5	7.5	3.7	-	-
[4]	18.7	-	100	3.2	51	$6.48 \times 10^{-16} *$
[2]	9.9	-	20	1.8	28	$1.79 \times 10^{-13} *$
This Work	0.072	14.35	11.32	2.98	50.35	4.2×10^{-17}

*One assumes a gain of 20dB.
**One assumes a dynamic Range of 40dB.

9.2 Future Work

The suggested programmable-gain scheme suffers from poor linearity, and should be redesign in order achieve sufficient linearity. Attenuation the input with a capacitive ladder would be the easiest solution. However, power consumption would be constantly high. The layout has a few rookie mistakes, and the area could possibly be made even smaller. The design should also be further optimized in terms of mismatch, which was previously detailed in the discussion.

APPENDIX A

Noise Sources

A.1 Noise Sources

An expedient noise analysis for the circuit could be executed by neglecting the cascoding transistor M_4. Futhermore $R_{L2} = R_{L2}||R_{ds3}$ and $R_a = r_{ds1}||r_{ds2}$

Flicker noise from M1

$$V_{fnm1}^{+} = \left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m1} r_a R_{L1} V_{fm1} \quad \text{(A.1)}$$

$$V_{fnm1}^{-} = -\left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m3} g_{m1} r_a R_s R_{L2} V_{fm1} \quad \text{(A.2)}$$

Flicker noise from M2

$$V_{fnm2}^{+} = -\left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m2} r_a R_{L1} V_{fm2} \quad \text{(A.3)}$$

$$V_{fnm2}^{-} = -\left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m3} g_{m2} r_a R_s R_{L2} V_{fm2} \quad \text{(A.4)}$$

Flicker noise from M3

$$V_{fnm3}^{+} = \left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m3} r_a R_{L1} R_{L2} V_{fm3} \quad \text{(A.5)}$$

$$V_{fnm3}^{-} = -\left(\frac{g_{m3} V_{fm3}(g_{m2} R_s r_a + g_{m1} R_s r_a + R_s + r_a + R_{L1}) R_{L2}}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) \quad \text{(A.6)}$$

Thermal Noise from M3

$$V^{+}_{tnm3} = \left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m2} r_a R_{L1} R_{L2} I_{tm3} \quad \text{(A.7)}$$

$$V^{-}_{tnm3} = -\left(\frac{I_{tm3}(g_{m2}R_s r_a + g_{m1}R_s r_a + R_s + r_a + R_{L1})R_{L2}}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) \quad \text{(A.8)}$$

Thermal Noise from M1 and M2

$$V^{+}_{tnm3} = -\left(\frac{2}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) R_{L1} r_a I_{tm12} \quad \text{(A.9)}$$

$$V^{-}_{tnm3} = \left(\frac{2}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m3} r_a R_s R_{L2} I_{tm12} \quad \text{(A.10)}$$

Thermal Noise from R_{L2}

$$V^{+}_{tnrl2} = \left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m2} r_a R_{L1} R_{L2} I_{tRL2} \quad \text{(A.11)}$$

$$V^{-}_{tnrl2} = -\left(\frac{I_{tRL2}(g_{m2}R_s r_a + g_{m1}R_s r_a + R_s + r_a + R_{L1})R_{L2}}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) \quad \text{(A.12)}$$

Thermal Noise from R_{L1}

$$V^{+}_{tnrl1} = -\left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m2} r_a R_{L1} I_{tRL1} \quad \text{(A.13)}$$

$$V^{-}_{tnrl1} = -\left(\frac{1}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) g_{m3} r_a R_s R_{L2} I_{tRL1} \quad \text{(A.14)}$$

Thermal Noise from R_s

$$V^{+}_{tnRs} = -\left(\frac{g_{m3}R_{L2}(R_{L1} + r_a)V_{nrs}}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) \quad \text{(A.15)}$$

$$V^{-}_{tnRs} = -\left(\frac{R_{L1}(g_{m2}r_a R_{L2} g_{m3} + 1 + g_{m1}r_a + g_{m2}r_a)V_{nrs}}{R_s[1 + r_a(g_{m1} + g_{m2} + g_{m3}g_{m2}R_{L2})] + R_{L1}} \right) \quad \text{(A.16)}$$

APPENDIX B

Results

B.1 Results

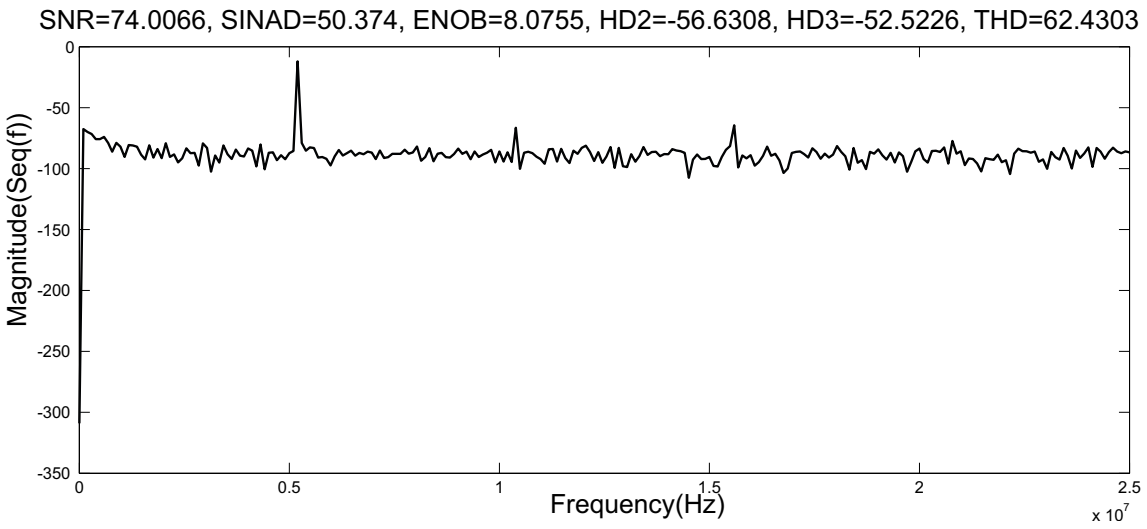


FIGURE B.1: FFT of transient analysis with coherent sampling, at fixed loads of 256fF. $fin \approx 5.1$MHz, 50mV amplitude

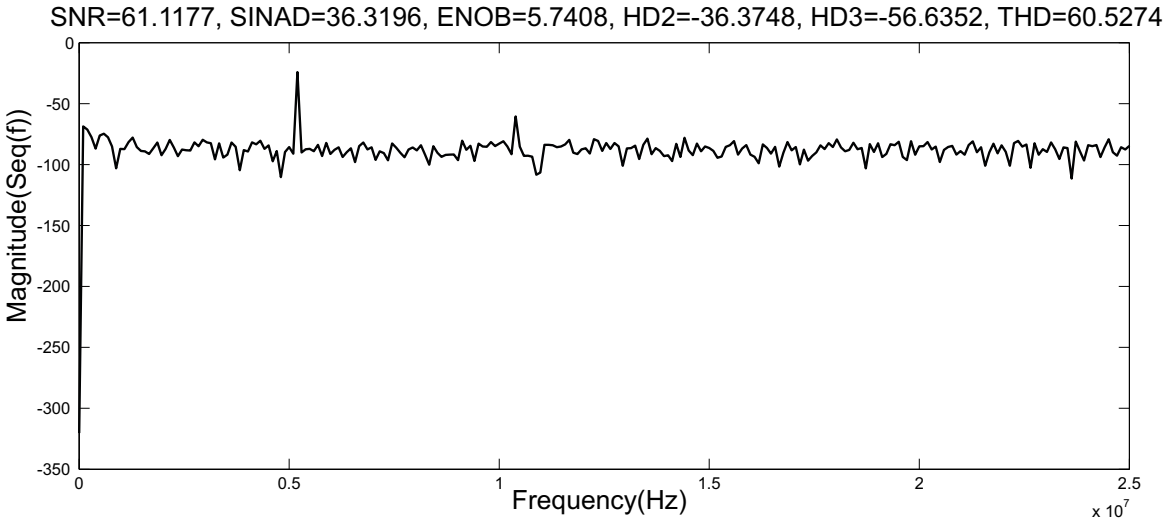


FIGURE B.2: FFT of transient analysis with coherent sampling, loaded with an A/D-converter. $fin \approx 5.1$MHz, 50mV amplitude

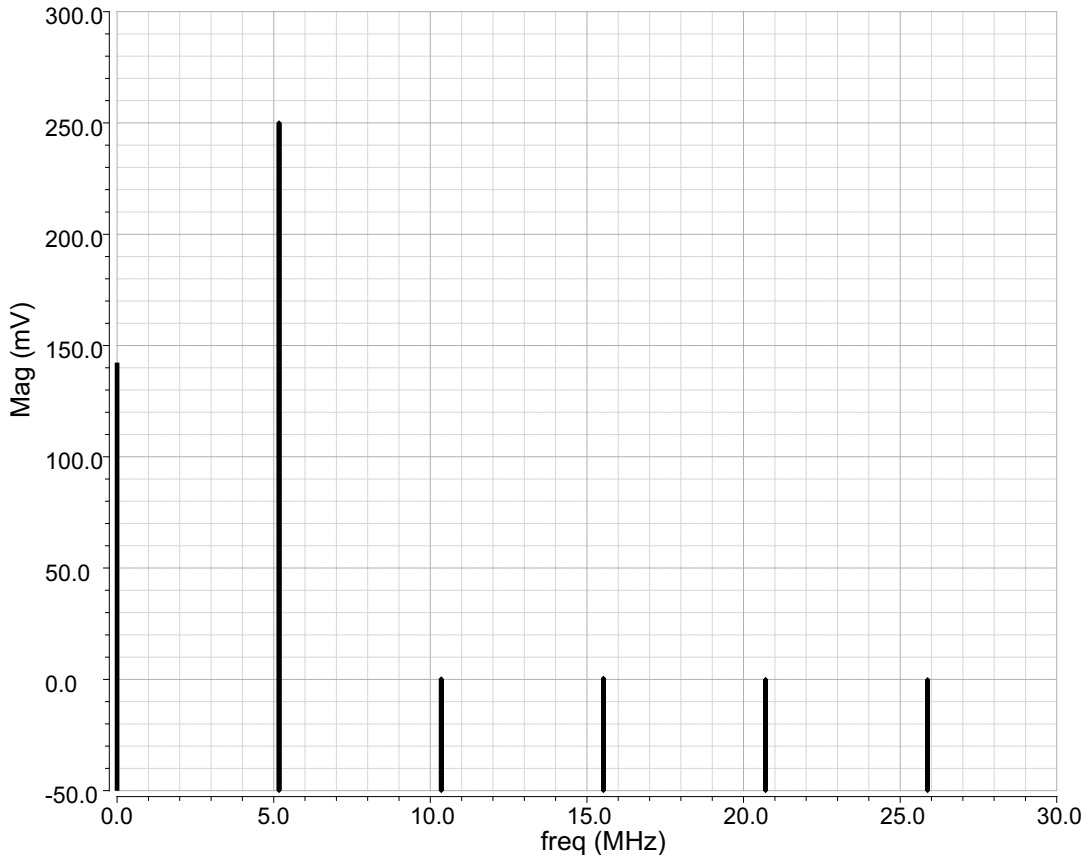


FIGURE B.3: PSS Single-Tone test at fixed loads of 256fF. $fin \approx 5.1$MHz, 50mV amplitud

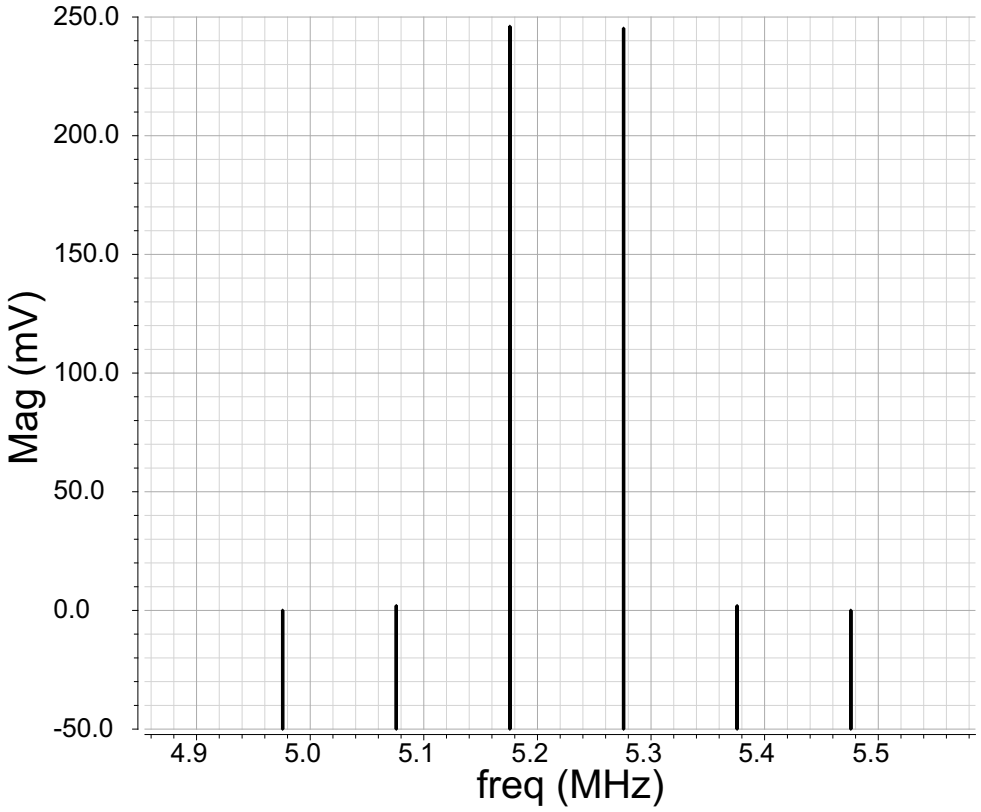


FIGURE B.4: QPSS Two-Tone test at fixed loads of 256fF. $fin \approx$ 5.17578125MHz and 5.27578125MHz, 50mV amplitud

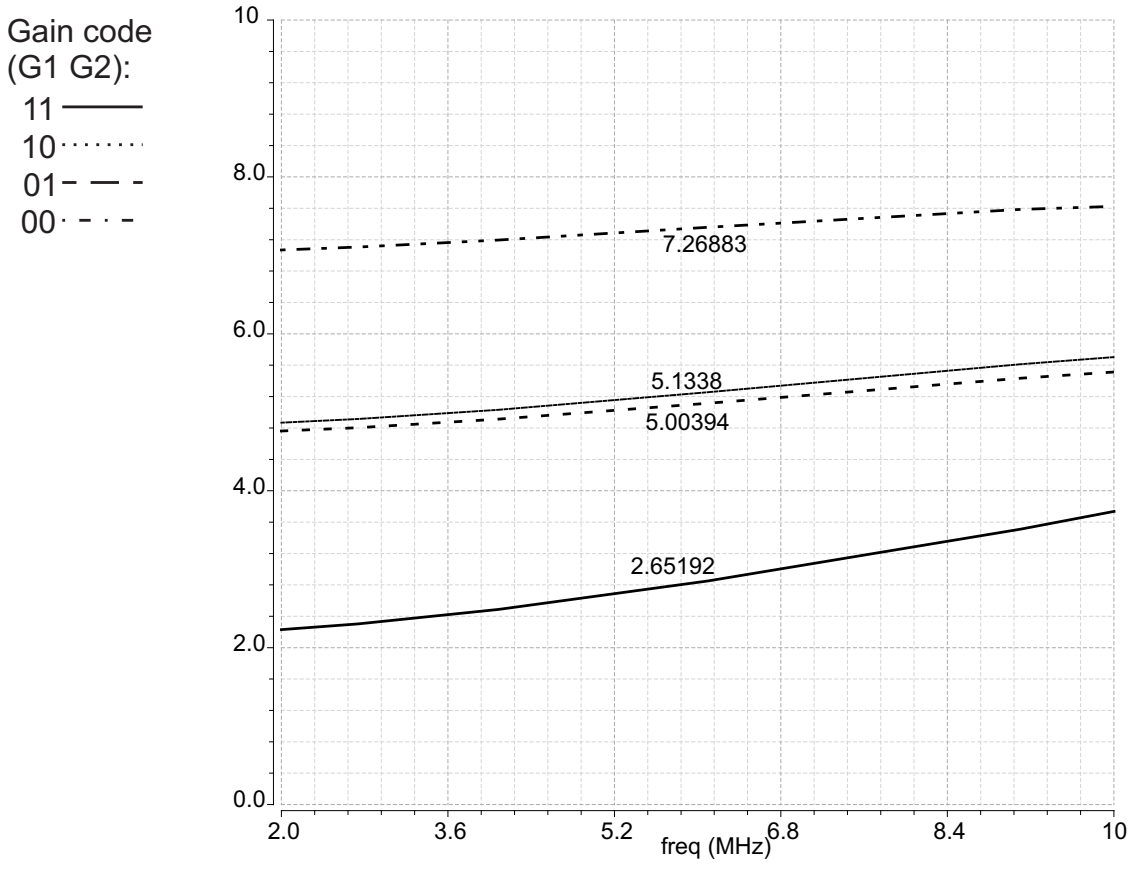


FIGURE B.5: VSWR plotted and given numerically at 5MHz.

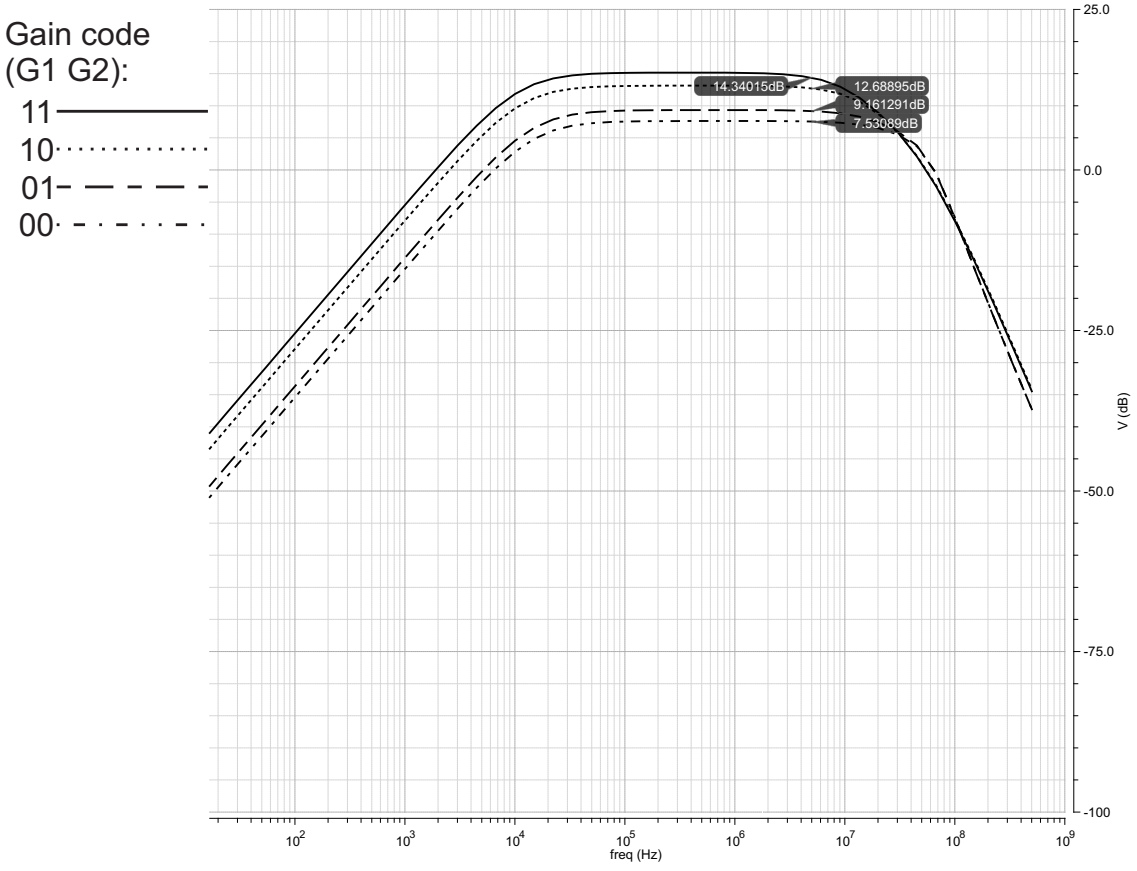


FIGURE B.6: Bandwidth plotted for the respected gain codes, gain highlighted at 5MHz.

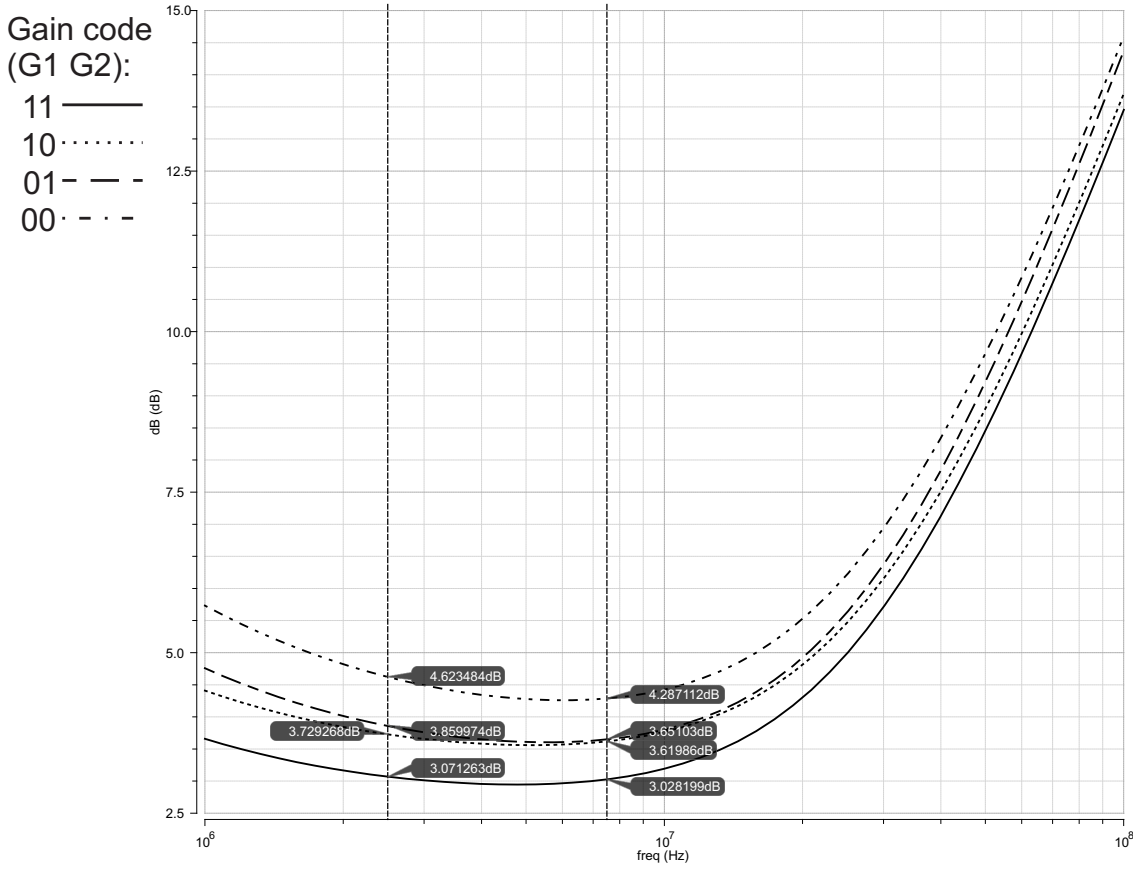


FIGURE B.7: The Noise Factor plotted for the respected gain codes, highlighted frequency corresponds to the endpoints of 5MHz center with 100%-bandwidth.

APPENDIX C

Paper Submission

A 65nm CMOS Front-end LNA for Medical Ultrasound Imaging with Feedback Employing Noise and Distortion Cancellation

J. Håvard Eriksrød and Trond Ytterdal
Department of Electronics and Telecommunication,
Norwegian University of Science and Technology - NTNU
N-7491 Trondheim, Norway
post@heriksro.org - ytterdal@iet.ntnu.no

***Abstract*—A 70μW low power front-end Low Noise Amplifier (LNA) for ultrasound applications is proposed. The amplifier utilizes a balun based on a common-gate (CG) and a common-source (CS) combination. The CS-amplifier performs error correction, and thus cancels distortion and noise from the CG-amplifier. The amplifier is optimized towards low noise and low power consumption, and is a capacitive micro machined ultrasonic transducer (CMUT) tailored LNA. The LNA is design and simulated under 65nm CMOS technology, achieving a noise figure (NF) of only 2.87dB with a total power consumption of only 70μW. The amplifier is tuned towards an CMUT impedance of $10k\angle -60^{\circ}$ at a center of frequency 5MHz, with a input impedance of 3.2$k\Omega$. Moreover, sporting a dynamic range (DR) of 40.57dB.**

I. Introduction

Contrary to X-ray imaging, ultrasound medical imaging has an impeccable safety record, it is cost efficient and has the ability to perform real time imaging. Capacitive Micro machined Ultrasonic Transducer (CMUT) easily integrate with CMOS and performes almost as good as piezoelectric transducers [1].

The receiving end of an ultrasound system consists of a transducer and a front-end amplifier. Generally the front-end amplifier will be piggybacked by a high-resolution A/D-Converter for futher signal processing. It is therefore conceivable that a complete system including CMUTs, amplifiers and A/Ds may be implemented on a single chip sometime in the future. The front-end being analog limits the systems overall performance like signal-to-noise ratio, linearity and bits of resolution. Noise generated by the amplifier limits the dynamic range of the A/D-Converter, and distortion limits the maximum signal swing. Cosequently, the degradation of the total system performance is determined by the noise generated by the amplifier, and is given as Noise Figure (NF). Current state of the art front-end uses a transimpedance amplifier (TIA). TIA amplifiers are suitable for CMUT applications since they have low input impedance and overall good performance. Low front-end input-impedance improves performance of CMUTs as implied in [7]. A typical TIA based reciver chain consists of a TIA, Current feedback Amplifier (CFA) and Buffer [2]. Example [1] has a low Noise Figure (NF) of $1.8dB$, with a poor Dynamic Range (DR) of just $28dB$ and a total power consumption of $9.9mW$. Hench, the main problem with this type of approach is the sheer power consumption.

This paper proposes a $sub-100\mu W$, $sub-3dB$ low power low noise front end, with noise and distortion cancelling for CMUT applications. The proposed design is based on a CGCS Balun-LNA, with switchable gain and gm-boosting [5]. The CGCS-LNA is a well know and a heavily researched topology in the RF-world.

The paper is organized as follows: Section II describes the proposed design in detail, including small signal analysis. In Section III noise/distortion cancelling conditions and noise figure for the proposed topology are derived. Simulated results and discussion will be presented Section IV, ending with a brief conclusion in section V.

II. Circuit Description

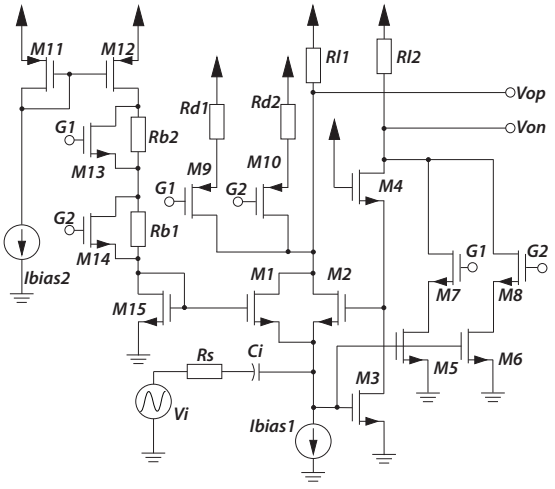


Fig. 1. Complete schematic of the proposed design

The amplifier consists of a non inverting common gate-amplifier and an inverting common source-amplifier and thus performes single-to-differential conversion. Thermal noise due to transistor $M1$ and $M2$ could be modelled as a current source

in parallel. Thus, generating noise voltages in anti-phase, over the surge impedance (R_s) and over the load impedance (R_{L1}). The noise voltage V_nR_s will be amplified and phase shifted by a CS-amplifier. Consequently, the noise at positiv output (Vn_{op}) and the negative output (Vn_{on}) is in phase. One could therefore cancel thermal noise entirely from M1 and M2, if the noises correlates and are of the same magnitude. The conditions for proper noise cancellation is derived in section III-A. The amplifier is design towards a source impedance (R_s) of $10k\Omega$.

The area of $M1$ and $M2$ are chosen relatively large mainly to get the noise corner (1/f) under band of interest. Thus, relaxing the reliance of $M2$. The input impedance $Z_{in} \propto \frac{W}{L}$ (equation 4) Consequently, making a trade off between flicker noise/bandwith and input impedance. $M2$ looks to be gm-boosted by the CS-amplifier, however the main objective is to enhance the linearity of the CS-amplifier by using $M2$ as feedback, and not to increase the gain.

$M3$ is biased by the quiescent current flowing trough the CG-Amplifier and $M2$ is biased by the CS-amplifier. Thus, creating somewhat of a circular dependency between the two amplifying stages (V_{op}, V_{on}). One tries to counteract the dependency with $M1$. $M1$ is an amplifying element but its primary function is to controll the operation point of the CS-amplifier, somewhat independently of the CG-amplifier. The proposed design is lopsided on the output in terms of common-mode and gain, which can be troublesome for some designs. Moreover, one has successfully simulated the amplifier, piggybacked by a state-of-the-art A/D-Converter [6] in discrete time, with $2x256fF$ load capacitance. The digitized signal was then filtered by a low order FIR low pass filter, with a cutoff frequency (f_{fc}) of $2f_{in}$. Consequently, sporting results on par with that of table IV. Chopper stabilized common mode has successfully been implemented for the amplifier. Chopper stabilizing is a feasible solution if one need likewise common-mode. However, this was not necessary as our receiver chain only consists of the amplifier piggybacked by an A/D-Converter IV.

A. Small Signal Parameters

One neglects the body effect and the channel resistance of $M3$ and $M4$ in order to make the small signal analysis less strenuous. Note that $r_a = r_{ds1}||r_{ds2}$.

Small-signal voltage gain at the positive output (V_{op}) could be given as:

$$A_{vop} = \frac{R_{L1}[g_{m4}(1 + r_a[g_{m2} + g_{m1}]) + g_{m2}g_{m3}r_a]}{R_s(g_{m2}g_{m3}r_a + g_{m4}[1 + r_a(g_{m1} + g_{m2})]) + g_{m4}(R_{L1} + r_a)} \quad (1)$$

The small-signal voltage gain at the negative output (V_{on}) could be given as:

$$A_{von} = -\frac{R_{L2}[g_{m4}g_{m3}(r_a + R_{L1})]}{R_s(g_{m2}g_{m3}r_a + g_{m4}[1 + r_a(g_{m1} + g_{m2})]) + g_{m4}(R_{L1} + r_a)} \quad (2)$$

The amplifier performs single to differential conversion, the gain is therefore the two outputs differentiated.

$$A_{balun} = A_{vop} - (-A_{von}) \quad (3)$$

The input impedance as:

$$Z_{in} = \frac{g_{m4}(R_{L1} + r_a)}{r_a[g_{m2}g_{m3} + g_{m4}(g_{m1} + g_{m2})] + g_{m4}} \quad (4)$$

Hench the toplogy has a lesser input impedance when compared to a normal CG-amplifier.

B. Programmable-gain

The complete design in figure 1 proposes a digital stepwise gain control. The gain is controlled by setting two digital pins g_1 and g_2. The gain is mainly controlled by altering the load of the CG-amplifier (R_{L1}). However, the CS-amplifier is biased by the quiescent current flowing trough the CG-amplifier. Thus, V_{gs} for CS-amplifier is increased when R_{L1} is reduced, causing the postive output (V_{op}) to be pulled towards ground. The transconductance of the CS-amplifier is alterd in order to counteract for the operational changes introduced by the gain controll. The alteration of the transconductance is done by using several transistors in parallel, that are controlled by switching the cascoding transistors. Moreover, noise and distortion cancellation is dependent on R_{L1}, as shown in equation 8 . Therefore, a reduction in R_{L1} tarnishes both distortion and noise cancellation. However, it is reasonable to believe that one desires a reduction in gain because of increased input voltage. Therefore, one could have poorer noise characteristics and still achieve adequate DR.

Canellation was dependent on R_{L1}/g_{m3} it is therefore desirable that the two are reduced at the same rate. In order to combat the degradation of NF, one therefore alters the current mirror reducing the biasing voltage of $M1$. A reduction in the bias voltage further reduces the biasing voltage for the cs-amplifier. Thus, reducing the transconductance of the CS-amplifier.This provides a significant improvement in noise figure.

TABLE I. PROGRAMMABLE-GAIN

g_1	g_2	Gain [dB]	NF [dB]	NF_{min} [dB]	BW [MHz]	Power[μw]
1	1	13	2.87	2.14	11.5	53
0	1	10.8	3.47	2.42	18.76	62
1	0	9.7	4.17	2.3	16.2	64
0	0	7.4	4.54	3	27.5	68

III. NOISE/DISTORTION

One assumes that the thermal noise generated by $M1$ and $M2$ are uncorrelated. Consequently, thermal noise could be added and seen as one noise current source, in parallel with the transistors. By neglecting the channel resistance (rds) and the body effect, a far less cumbersome noise cancelling analysis could be performed.

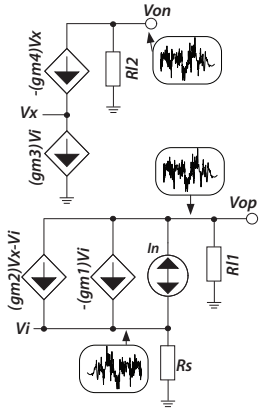


Fig. 2. Simplified noise analyses of thermal noise.

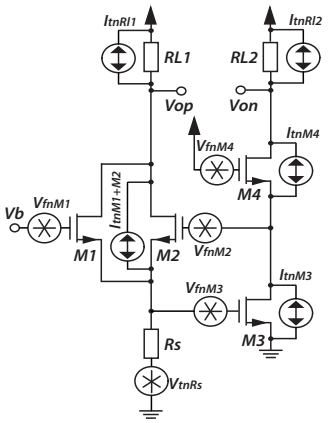


Fig. 3. Noise sources present in a Balun-LNA.

A. Noise cancelling

First, one assumes that the current passing through Rs namely I_{rs}, could be written as:

$$I_{rs} = \frac{g_{m4} i_n}{g_{m4} + R_s(g_{m1}g_{m2} + g_{m1}g_{m4})} \tag{5}$$

The positive output voltage $Vop = -I_{rs}R_{L1}$, thus:

$$V_{op} = -\frac{g_{m4} i_n R_{L1}}{g_{m4} + R_s(g_{m1}g_{m2} + g_{m1}g_{m4})} \tag{6}$$

The negative output is the voltage at the input, $V_i = I_{rs}R_S$ amplified by the CS-amplifier, giving:

$$V_{on} = -\frac{g_{m4}g_{m2} i_n Rs R_{L2}}{g_{m4} + R_s(g_{m1}g_{m2} + g_{m1}g_{m4})} \tag{7}$$

Differentiating Vop and Von gives:

$$V_{op} - V_{op} \rightarrow R_s = \frac{R_{L1}}{g_{m2}R_{L2}} \tag{8}$$

Thermal noise from $M1$ and $M2$ is cancelled if equation 8 yields true. One sees that noise cancellation is only dependent on the load resistance and the transconductance of g_{m3}

B. Noise sources

Noise sources includes thermal noise from transistors and resistors, as well as flicker noise from transistors. One assumes that all of the noise sources are uncorrelated. Consequently, each noise source is viewed independently and then summed. One also neglects the body effect and the channel resistance (rds). One assumes perfect noise cancellation and that thermal noise from both M1 and M2($I_{tn}(M1 + M2)$) are completely cancelled out. Moreover, one neglects channel resistance (rds) and the body effect.

$$F = \frac{1}{4kTR_s(R_{L1}[g_{m4}(g_{m1}+g_{m2}) + g_{m2}g_{m3}] + g_{m3}g_{m4}R_{L2})^2} \left(R_{L1}^2\left[g_{m4}^2\left[g_{m1}^2\frac{\kappa}{W_1L_1C_{ox}f} + g_{m2}^2\left(\frac{\kappa}{W_2L_2C_{ox}f} + \frac{\kappa}{W_4L_4C_{ox}f}\right)\right] + (g_{m2}g_{m3})^2\frac{\kappa}{W_3L_3C_{ox}f} + g_{m2}^2 4kT\gamma(g_{m3}+g_{m4})\right] + R_{L2}^2\left[\left(\frac{\kappa}{W_3L_3C_{ox}f}g_{m3}^2 + 4kT\gamma g_{m3}\right)g_{m4}^2(R_s^2(g_{m1}+g_{m2})^2+1) + \left(\frac{\kappa}{W_4L_4C_{ox}f}g_{m4}^2 + 4kT\gamma g_{m4}\right)(g_{m2}g_{m3}R_s)^2 + \left(\frac{\kappa}{W_1L_1C_{ox}f} + g_{m2}^2\frac{\kappa}{W_2L_2C_{ox}f}\right)(R_s g_{m4}g_{m3}g_{m1})^2\right] + 8kT(R_{L1}+R_{L2})[g_{m4}(1+R_s(g_{m1}+g_{m2})) + R_s g_{m2}g_{m3}]^2\right) \tag{9}$$

Where κ is a process dependent parameter, k is the boltzman constant, f is frequency, Temperature(K°) T, C_{ox} is the oxide capacitance, W_n width for transistor n , L_n gate length for transistor n, $\gamma = 2/3$ and the noise factor is given as $N_f = 10\log(F)$.

C. Distortion cancelling

One assumes that non-ideal behaviour could be modeled as a current that is dependent on the gate-source voltage. In order to derive a less ungainly expression one neglects the cascoding transistor M4 for the CS-amplifier, and does the same simplifications one did in the proof for noise cancelling. The non-linear source voltage (V_s), could be written as a

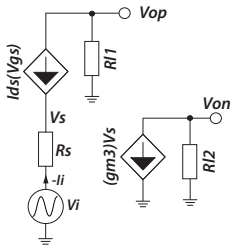


Fig. 4. Simplified small signal distortion analyses.

Taylor-series of the input signal (V_{in}):

$$V_s = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3 + ... + \alpha_n V_{in}^n = V_{in} + V_d \quad (10)$$

where α represents the Taylor coefficients, and V_d contains all of the nonlinear behaviour [5]. The negative output voltage (V_{on}) is the source voltage (V_s) amplified by a CS-amplifier, giving:

$$V_{on} = -g_{m3} R_{L2} V_s = -g_{m2} R_{L2} [V_s + V_d] \quad (11)$$

In termes of distortion, (V_{op}) is given by the load and the non-ideal behavioural current (I_{ds}) and inserting equation 10, yields:

$$V_{op} = R_{L1} I_{In} = (V_i - V_s)\frac{R_{L1}}{R_s} = [V_{in} - (V_{in} + V_d)]\frac{R_{L1}}{R_s} \quad (12)$$

Differentiating the outputs yields:

$$V_{op} - V_{on} = 0 \rightarrow -(V_s + V_s + V_d)\frac{R_{L1}}{R_s} + (V_s + V_d) R_{L2} + g_{m2} \quad (13)$$

Inserting equation 8 into 13, the output could be written as:

$$V_o = R_{L2} g_{m3} V_s \quad (14)$$

Consequently, all of the non-linear elements are removed from the output. Thus, the differentiated output is only dependent on the CS-amplifier in terms of distortion and noise.

IV. Results and Discussion

The amplifier (shown in figure 1) is implemented in a 65nm CMOS technology from STM, and simulated using state-of-the-art EDA-tools from Cadence. However, one should note that the results has not taken parasitic capacitance into account. The amplifiers positive (V_{op}) output and the negative (V_{on}) output are each loaded with $256fF$. A CMUT at resonance can be molded as a resistor with a capacitance in parallel [2]. The circuit is simulated with the CMUT having a impedance of $10k\angle -60°$, center frequency of 5MHz and an amplitude of 25mV. One sees that power consumption (table I) increases when the gain is reduced, which is somewhat counterintuitive and toilsome to justify. However, the worst case total power consumption is $< 140x$ that of [1]. The input impedance was found to be $3.2k\Omega$ and could be reduced by reducing the size of transistor $M1$ and $M2$. A reduction will not tarnish noise/distortion cancellation. However, bandwidth and gain would potentially suffer.

TABLE II. Simulated results for the proposed design

$Power$	53*	μW
$Gain$	13*	dB
BW	11.5*	MH_Z
NF	2.87*	dB
NF_{min}	2.14*	dB
$Enob$	6.74	b
DR	40.57	dB
HD_2	-43.52	dB
IM_3	-38.14	dB
$VSWR$	3.23	

* Dependent on gain setting (g_1 and g_2), referring to table I

V. Conclusion

A design of a $sub - 100\mu W$, $sub - 3dB$ noise figure amplifier for ultrasound imaging applications has been proposed. The amplifier is tuned towards low power and low noise. The amplifier is optimized to be loaded with a high-resolution A/D-converter. The amplifier is implementeted and simulated in 65nm CMOS technology. Moreover, achieving a DR of 40.57dB, NF of 2.87dB with a power consumption of $< 70\mu W$. Comparing the proposed design with recent published front-end amplifiers, shows a huge improvement in power consumption.

TABLE III. Comparison with recent published works

	Power $[mW]$	Gain $[dB]$	BW $[MHz]$	NF $[dB]$	DR $[dB]$
[4]	20.3	20.5	100	4.9	-
[3]	-	77.5	7.5	3.7	-
[2]	18.7		100	3.2	51
[1]	9.9		20	1.8	28
This Work	0.068	13	11.5	2.87	40.57

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