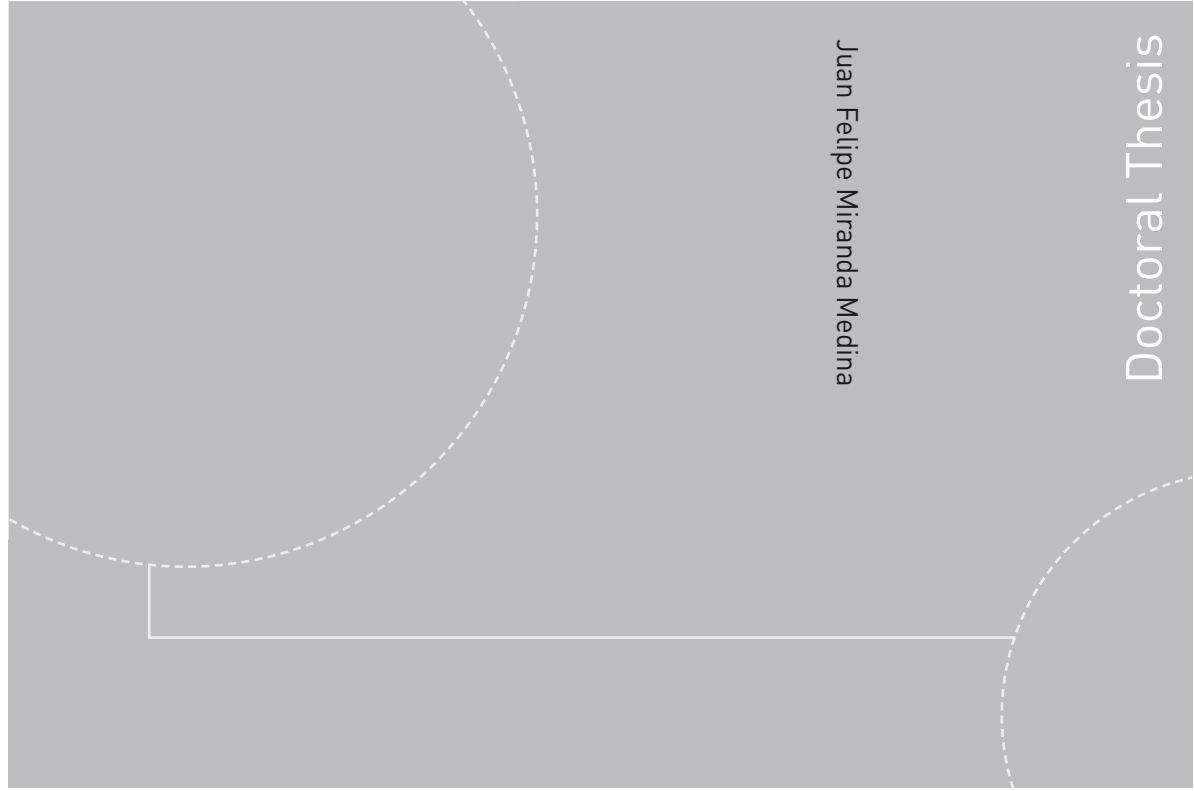


ISBN 978-82-471-3867-0 (printed version)
ISBN 978-82-471-3868-7 (electronic version)
ISSN 1503-8181



Juan Felipe Miranda Medina

Doctoral Thesis

Doctoral theses at NTNU, 2012:277

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 **NTNU – Trondheim**
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Thesis for the degree of Philosophiae Doctor

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ISSN 1503-8181

52698

Doctoral theses at NTNU, 2012:277



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*We shall not cease from exploration,
and the end of all our exploring will be
to arrive where we started and know
the place for the first time.*

T. S. Eliot

Abstract

Spectrum is an indispensable and scarce resource in modern communication systems. Reduced hardware complexity is therefore traded for bandwidth-efficient modulation that increases the signal's peak-to-average power ratio (PAPR).

For applications requiring high linearity amplification at microwave frequencies, class-A and -AB power amplifiers have been the traditional choice. However, due to the large PAPR of the modulated signals, they must be operated at several decibels back-off to comply with linearity requirements. Though class-A/AB amplifiers offer descent efficiency at peak envelope power, efficiency decays rapidly with input power back-off. The designer is seemingly left with an inevitable linearity–efficiency trade-off. Though there are several alternatives around the problem, in the context of point-to-point radios the challenge is to find low-cost, reliable solutions that are independent of carrier frequency and manage large bandwidths (e.g., 40 MHz) for moderate output powers (i.e., not larger than 10 W).

It is therefore that *dynamic biasing*—the joint variation of input and output biases following envelope power—is attractive. Following envelope power instead of envelope amplitude and varying also the input bias makes DB substantially different from envelope tracking (ET). Varying the output and input biases as first and second order polynomials of the input power, the bias bandwidth can be controlled to be only twice and four times the RF bandwidth, respectively. Bias bandwidth in a typical ET system would be at least twice as large.

This dissertation specifically addresses the problem finding the polynomial coefficients for bias variation, first through simulation methods, and then through direct measurement on different technologies (an MMIC HBT transistor, a discrete GaAs amplifier, and a discrete GaN amplifier). The dynamic biasing problem is formulated mathematically and solved using random search optimization, for which a multi-objective cost function and a linearity measure—different from least square error—are introduced. The effect of output matching on the linearity of the amplifier, and the inclusion of digital predistortion without affecting bias bandwidth are also considered.

The results from this research study show that dynamic variation of the input bias alone can significantly improve linearity—a low-complexity, low-cost solution due to the low current levels at the input—. The largest benefits in efficiency are certainly obtained from output bias variation. Though it may adversely affect linearity if used alone, in many cases full dynamic bias (both at input and output)

is a win-win combination both in regards to linearity and efficiency. The technique is also attractive because the transistor can be biased higher at peak power if the PAPR of the signal is large, and hence higher average output power can be obtained than with static biasing.

Preface

This work was developed in the Radio Group of the Department of Electronics and Telecommunications, in the Norwegian University of Science and Technology (NTNU). It was carried out under the supervision of Associate Professor Morten Olavsbråten, and the co-supervision of Karl Martin Gjertsen, Chief Technologist at Ceragon. It was funded by the Norwegian Research Council through the project “Smidig, Trådløs Infrastruktur”, with project number 176923.

Acknowledgments

I would like to thank professor Morten Olavsbråten, for his support and guidance all along this project. His profound insight, knowledge and good will to guide me and encourage me have been vital in this process of swimming in deeper waters. Just as important has been the insight that my cosupervisor, Karl Martin Gjertsen, contributed with all along. His patience in our written dialogs, his experience, his critical eye, and creative thinking inspired me to dig willingly into the benefits that the method here presented can provide. Both of them were excellent guides to the new world of RF power amplifiers. I also appreciate the positive and pleasant academic interaction with Marius Ubostad, Walter Caharija, Terje Mathiesen, and Dragan Mitrevski. I must particularly thank Dragan for his encouragement and eagerness in the process of showing me to the L^AT_EXworld, and for kindly proofreading this work carefully. For the chance of pursuing this PhD am I most grateful to Mikael Gidlund, who encouraged me to apply, was a good reference, and a good supervisor and guide while I was finishing my master thesis in Sweden.

My experience in Norway would not have come along is it was not for the love and patience I received from my parents and family from early on. The principle of trying as hard as one can and not giving up, and to do things with joy brought me to beautiful Scandinavia. I whole heartedly thank Jessica Vargas, for her love, joy and patience all along the way, for being willing to share with me the simpleness of the every day, for having been partners in this wild, delightful process. I also thank deeply my Norwegian friends who welcomed a foreign and taught him their language and manners, and shared with me the delight of a new interaction, music, art, simple chats and philosophy. Memories from simple gatherings I cherish, your different personalities and dialects, your values of respect for the other, independence and helpfulness, and your vital pursuit of what lies ahead. I am also most thankful to my Latin friends who day to day make me feel at home, hablando en español and treating each other with such closeness as if we had grown up together. My last thankful thoughts are dedicated to Life, for being as mysterious and complexly simple as it is. For having apples hanging from trees and pulling them down from its center, for being That that we shall never fully know, but always shall sense as if we did.

... I do not seem to be able to turn to the next page without pronouncing your names: Federico, Carlos Roberto, David, Freddy, Alfredo, Tati, Virginia, Sara, Jos, Bety, Habib, Cecitar, Sonia, Jorge, Helmuth, Carlos Bellatn, Carolina,

Brenda, Daniel, Manuel, Efran, Emilia, Edith, Jessica Chani, Patricia, Ebert, Vidis, Mauricio, Tatiana Machicao, Olof, Mikael, Claes, Nils Arne, Sissel, Jrn, Anne Lise, Anna, Max, Jonas, Maclau, Miolinho, Matias, Mariela, Daniel Reinoso, Elena, Edgard, Giorgos, Cecilie, Jen, Indre, Sandra, Rampa, Eleni, Marcelinha, Jordan, Saul, Robert, Lilian, Oscar, Branda, Father Alf, Joyce, Einar, Lizeth, Claudia, Mercedes, Diana, los Herrera, los Miranda, los Medina, Yonne, Lone, Leif, Hanne, Anders Palma, Anders den Kule, Andreas, Andreas Schille, Jarib, Esperanza, Sandra, Mara, Lucerito, Felipe, Brian, Pablo, Luciano, Ada, Carlos y Mara, Andrea Asuncin, Antonio, Flavia, Piotr, Ania, Renz Chirinos, Renzo Balln, Marco Huanca, Walter Valderrama, Walter Caharija, Vesna, Ahmed, Lux, Kun, Sara Boulosa, Li Xin, Lee, Robert, Sick, Hctor, Miguel, Cristhian, Roderick, Juan III, Cristina, Corina, Chelita, Blanquita, Teresa, Tiwinza and Preciosa. I hug you all.

Juan F. Miranda Medina
Trondheim, July 2012

Publications and contributions

Publications

- I. **J. F. Miranda**, M. Olavsbråten, K. M. Gjertsen, “Biasing an HBT MMIC transistor for efficiency and output power enhancement,” in *Integrated Non-linear Microwave and Millimetre-wave Circuits (INMMiC)*, Dublin, Ireland, 2012.
- II. **J. F. Miranda**, K. M. Gjertsen, M. Olavsbråten, “Optimization Theory Applied to Dynamic Biasing for Power Amplifier Performance Enhancement,” in *IEEE Topical Conference on RF/microwave Power Amplifiers*, Santa Clara, CA, USA, 2012.
- III. **J. F. Miranda** and M. Olavsbråten, “Dynamic Biasing for Linear and Efficient Microwave Amplification,” in *IEEE Topical Symposium on Power Amplifiers for Wireless Communications*, Arizona, USA, 2010.
- IV. **J. F. Miranda**, M. Olavsbråten, K. M. Gjertsen, “First and second order polynomial functions for bandwidth reduction of dynamic biasing signals,” in *IEEE International Conference on Wireless Information Technology and Systems (ICWITS)*, Honolulu, HI, 2010.
- V. W. Caharija, **J. F. Miranda**, M. Olavsbråten, K. M. Gjertsen, “A cost-based path search algorithm for enhanced design with Dynamic Bias,” in *17th Telecommunications forum TELFOR*, Belgrade, Serbia, 2009.
- VI. **J. F. Miranda**, W. Caharija, M. Olavsbråten, K. M. Gjertsen, “Dual dynamic biasing with input power precompensation for class-A/AB enhancement,” in *17th Telecommunications forum TELFOR*, Belgrade, Serbia, 2009.

Conference presentations

- I. **J. F. Miranda**, M. Olavsbråten, “Dynamic Biasing for class A/AB Power Amplifiers” in *4th MC Meeting and Workshop of COST IC0803*, Aveiro, Portugal, 2010.

II. **J. F. Miranda**, M. Olavsbråten, “Dynamic biasing for class A/AB power amplifiers” in *VERDIKT Conference*, Lillehammer, Norway, 2009.

Note: regarding publication V., the main author was at that time a master student under the supervision of Morten Olavsbråten and me. My contribution was to discuss with the main author the specifications for the algorithm that the paper describes, to verify its performance, and to review the writing of the paper.

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Nomenclature

Abbreviations and acronyms

ACPR3-L	Adjacent channel power ratio of the lower channel
ACPR3-U	Adjacent channel power ratio of the upper channel
ACPR5-L	Alternate channel power ratio of the lower channel
ACPR5-U	Alternate channel power ratio of the upper channel
AGT	Auxiliary gate tracking
AM/AM	Amplitude-to-amplitude distortion
AM/PM	Amplitude-to-phase distortion
ARS	Adaptive random search
Auxiliary envelope tracking	AET
BJT	Bipolar junction transistor
DB	Dynamic biasing
DGB	Dynamic gate biasing
DPD	Digital predistortion
DPD	Digital predistortion
DSP	Digital signal processor
DUT	Device under test
EER	Envelope elimination and restoration
ET	Envelope tracking
EVM	Error vector magnitude

FET Field effect transistor
FET Field-effect transistor
FPGA Field programmable gate array
HBT Heterojunction bipolar transistors
HEMT High-electron-mobility transistor
I–V plane Current–voltage characteristic curves
IM Intermodulation
IM3 Third-order intermodulation distortion
IM3 Third-order intermodulation distortion
IM5 Fifth-order intermodulation distortion
IMD Intermodulation distortion
LDMOS Laterally diffused metal-oxide-silicon
LS Least squares
LS Least squares
LUT Look-up table
LUT Look-up table
MESFET Metal semiconductor field effect transistor
MI Monotonically increasing
MOSFET Metal-oxide-silicon field effect transistor
OBO Output power back-off
PA Power amplifier
PAE Power added efficiency
PAPR Peak-to-average power ratio
PDF Probability density function
RC Resistor-capacitor
RRC Root-raised-cosine

RS Random search

UHF Ultra high frequency

VHF Very high frequency

Mathematical symbols

\hat{S} Nonlinear system that is a model of S

Ψ Probability density function

C_i i th complex coeff. of the polynomial model $\hat{S}\{\cdot\}$

f_c Carrier (or center) frequency

f_c Carrier frequency

I_D Drain bias current.

$I_{D,\max}$ Maximum drain current for reliable operation

L Measure of nonlinear distortion

P Measure of average dissipated power

p Input power.

$p(t)$ Instantaneous power of $x(t)$

P_0 Output power

P_{dis} Dissipated power

$S\{\cdot\}$ Nonlinear system

V_D Drain bias voltage.

V_G Gate bias voltage.

$V_{D,\max}$ Upper limit for drain bias voltage-sweep.

$V_{D,\min}$ Lower limit for drain bias voltage-sweep.

$V_{G,\max}$ Upper limit for gate bias voltage-sweep.

$V_{G,\min}$ Lower limit for gate bias voltage-sweep.

$X(t)$ Band-pass input signal

$x(t)$ Low-pass input signal

$Y(t)$ Band-pass output signal

$y(t)$ Low-pass output signal

Chapter 1

Introduction

1.1 Motivation

The deployment of wireless communication has increased tremendously in the past few decades. Since the spectrum is a limited resource, it must be distributed efficiently among communication providers. This requires that a very large fraction of the RF spectral power is contained within the allocated bandwidth, which is accomplished by means of pulse shaping filters which significantly increase envelope variations (i.e., higher peak-to-average power ratio, PAPR). The power amplifier (PA)—located right before the transmitter antenna—is therefore challenged twice: its output must be linear to comply with spectral mask requirements; but it must also be efficient so that feeding power is not wasted and large heat removal hardware is avoided.

There are already a number of solutions to improve the linearity–efficiency tradeoff. They can be roughly classified into two main categories: linearization systems (e.g., feedforward, feedback, predistortion) and efficiency enhancement systems [2]. The latter are based on controlling operating conditions of the active cells (i.e., bias voltages and load impedances) so that high efficiency is maintained along varying output power levels. Popular forms of these techniques are, for example, envelope elimination and restoration (EER), envelope tracking (ET) and load modulation (a special case of which is the Doherty Amplifier) [4–8].

This PhD is financed by the Norwegian Research Council (*Forskningsrådet*) in collaboration with Nera Networks AS through the *Smidig, Trådløs Infrastruktur* project (nr. 176923), and is therefore mainly oriented towards point-to-point radio technology. There are certain requirements for these radio transmitters that are worth naming:

1. Wireless infrastructure covers a decade of frequency (4 GHz to 40 GHz), so the transmitter technology must be as independent of the carrier frequency as possible.
2. The bandwidth can be as high as 50 MHz, so oversampling at the digital side

comes at a cost.

3. The output power for radio infrastructure is rather modest, not significantly above 1 W. Efficient operation is important since it allows small sized radio hardware, but it is not as crucial as for base station amplifiers delivering 100 W.
4. The aim is to produce commercial products, so cost and reliability are priorities.

Class-A amplifiers are ideally perfectly linear, assuming an ideal transconductance function. Even if the transconductance is nonlinear the bias point can be fine-tuned to locate a “sweet spot” that yields a linear class-AB amplifier [9]. Though the maximum efficiency of an ideal class-A amplifier is 50 %, its average efficiency is inversely proportional to the PAPR, and can be as low as 5 % for a PAPR of 10 dB [10]. This is a consequence of the power back-off required for linear amplification given high variations in the signal’s envelope.

A promising solution that is hereafter referred to as dynamic biasing (DB), is to jointly vary the input and output bias of a Class-A/AB amplifier with the envelope of the RF input signal. In this way high DC power is provided when the input envelope is at its peak, but low DC power is fed for low envelope amplitudes. This principle is independent of the carrier frequency, can potentially manage high bandwidths, and provides linearity with a significant improvement in efficiency. From the implementation point of view the technique is attractive because it can be applied to conventional RF linear amplification topologies by readily substituting the static supply for a dynamic one [11].

There are nonetheless certain issues that must be dealt with carefully when manipulating the bias. It is precisely the need for a different design methodology to apply dynamic biasing to RF power amplifiers that gives rise to this research project.

1.2 The approach to bias variation

It has been more than thirty years since the invention of ET, a method for efficiency enhancement for class-B amplifiers. Class-B amplifiers have the property that the DC current varies in proportion to the required output current. Therefore, efficiency in back-off can be enhanced by varying the drain bias voltage according to the envelope power of the input signal [2]. Envelope tracking has been used in several different applications ranging from base station amplifiers [12],[13], to handset amplifiers in mobile telephone units [14].

The simplest way to implement ET would be to use an envelope detector at the input of the PA connected to a linear amplifier—the bias source—that feeds the PA with varying voltage and high current. However, there are some issues in this apparent simplicity that are subject of current research.

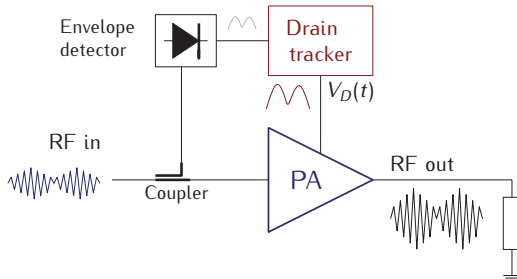


Figure 1.1: Simplified envelope tracking system.

1.2.1 Design of an efficient bias supply

The concern for supply efficiency arises because the overall amplifier system efficiency is given by the product of the power supply efficiency and the PA efficiency. In addition, depending on the output power expected from the amplifier, the current demand at the drain of the PA can be high.

On the other hand, the bandwidth of the envelope is several times the RF bandwidth. While in WCDMA applications the RF bandwidth can be smaller than 5 MHz, in point-to-point radios it can span decades of megahertz [15]. Manufacturing a source that follows rapid envelope variations and that provides the required current is not trivial. The most common solutions are to use switching supplies based on class-S architectures; vary the voltage in fixed voltage steps; or to combine a switching and a linear amplifier, so that the latter amplifies the highest frequency components that contain less power [10],[7],[16].

1.2.2 Shaping the bias function

The approach to the problem that actually concerns this work is how to limit the bandwidth of the drain bias signal to alleviate the requirements for the supply. A possibility is to digitally filter the drain waveform [17],[18]. The drawback is that memory effects will be introduced into the PA, hence a high-order digital predistortion (DPD) with memory will be necessary to meet linearity requirements, which increases the implementation cost. This work instead proposes varying the drain voltage as a polynomial function of the input power, making the bandwidth proportional to the order of the polynomial.

How the drain voltage is modulated has also an impact on the performance of the system. For example, Nemati et al. [19] varied independently the drain voltage and input power in different 1-GHz LDMOS switch-mode amplifier topologies with a maximum output power close to 40 dBm. The purpose was to determine the maximum PAE point for each constant output power contour. By joining these points and interpolating they extracted dependences of the drain voltage, input power and input phase on the output power level. Results showed 16 % more points

in PAE compared to EER and reduced envelope and RF bandwidth requirements. Hoversten et al. report a similar study for a 40-W class-A LDMOS amplifier [20]. In this case the maximum PAE curve is extracted and filtered in the drain-voltage–input-envelope-voltage space to avoid inflections that increase bandwidth. Linearity is further improved by means of an adaptive DPD algorithm. Rautio et al. [21] fed a 16-QAM 1-MHz signal into a 0.5-W PA, and chose 3 different paths in the drain-voltage–input-envelope-voltage space: 1. Drain voltage proportional to input-envelope. 2. Constant gain. 3. Maximum drain efficiency. The comparison showed that the paths could differ from each other up to 3.4 points in Error Vector Magnitude (EVM), 33° in amplitude-to-phase distortion (AM/PM), and 4 percentage points in PAE. The conclusion from the literature is that carefully designed drain modulation can positively impact efficiency, linearity and gain. This last point is important because gain drops with the input power should be avoided, else a buffer amplifier would have to be added before the PA to obtain the same output power.

Dynamic biasing poses the same problem as ET applied to class-A/AB amplifiers adding one dimension: the gate voltage. While it becomes more difficult to find biasing functions for the gate and drain working in synchrony, the gate supply can be modulated at higher bandwidths than the drain with less hardware complexity. That is because the efficiency of the gate converter has a smaller impact on overall system efficiency, since the currents at the gate are small—in field effect transistors (FET) the gate current is in the order of a few microamperes.

It has been theoretically proven that the PAE of a class-A PA driven by a modulated signal can be increased by a factor of 8 by using synchronized continuous gate and drain bias variation [22]. The study considered both synchronized and individual variation of gate and drain bias in continuous and step-like fashion using the ideal and the Saleh model. A signal with multicarrier phase modulation and large PAPR was used at an output power back-off (OBO) of 10 dB. For the specific case of the Saleh model with continuous gate and drain variation the class-A and -B biased transistor yielded 3.3 % and 10.8 % PAE respectively; while the PAE was of 8.8 % for ET, and 24 % for DB. Though this study is most relevant to demonstrate the improvements that DB can bring, it does not address how the bias should change with the envelope of the input signal. On the other hand, Colantonio et al. derived equations for the gate and drain bias variations as a function of the envelope for a simplified transistor model [23]. The device is modeled as a voltage controlled current source. The knee voltage is taken to be constant and the input and output resistances are considered, together with the gate-source and drain-source capacitances. The simulated results show that the system provides better ACPR for high average RF input power compared to the static case. The assumption of constant drain-source capacitance and transconductance with bias does certainly not apply to several transistor technologies. One of the aims of this work is to go deeper in the problem of finding suitable bias functions in a three dimensional space formed by the input voltage, output voltage and the input

envelope/power; by means of both graphic methods and optimization algorithms.

1.2.3 Predistorting a variable bias system

If digital predistortion is applied to a low bandwidth bias waveform, its bandwidth will be expanded due to the nonlinearity of the predistorting function. This work presents linearity measures that can be used for memoryless polynomial predistortion that aim for minimum distortion at the adjacent and alternate channels. The possibility of having gate/drain biasing that depends on the original (unpredistorted) signal while the predistorted signal is input to the PA is also discussed.

1.2.4 Load and source impedance selection

Given a transistor technology, the classic load-pull design procedure is to choose a class of operation and bias point according to the intended application. The optimum load is next found by means of a load-pull sweep for maximum output power/gain/PAE, or a trade-off point between the three. So can the source impedance be swept for maximum gain, and finally some extra rounds of load/-source impedance tuning might be required due to feedback within the device [24].

In a dynamic bias system the bias will vary between class-A and -B, while the source and load impedances presented to the transistor are fixed. Unfortunately, some internal parameters of the transistor, such as the drain-source capacitance, are sensitive to bias variations, especially to the gate [25],[18]. The load line will hence change with the bias, and so will the optimum load and source impedances for each bias point along the bias path.

The question is how to choose the source and load impedances in addition to the bias functions for the system to provide optimum performance—in terms of output power, efficiency, or linearity—together with a high gain at all input power levels despite the mismatch from bias variation.

The problem therefore becomes a set of five variables without considering harmonic tuning:

1. Input power to tune the load and source impedances.
2. Gate voltage as a function of the envelope voltage/power.
3. Drain voltage as a function of the envelope voltage/power.
4. Source impedance at the fundamental frequency
5. Load impedance at the fundamental frequency

The determination of the source and load impedances is addressed in the design of the pHEMT amplifier in Chapter 3.

1.3 Overview, scope and contributions

Chapter 2 includes a theoretical review that puts dynamic biasing in perspective. It outlines the main techniques used for linearity and efficiency enhancement in modern amplifier design, and describes both dominant and emerging transistor and semiconductor technologies in today's market.

Chapter 3 theoretically analyzes the implications of biasing as a function of input envelope power instead of input envelope amplitude using an idealized transistor model. Next, the design of a pHEMT MMIC amplifier for dynamic biasing is discussed step by step. Graphical methods are introduced to describe the amplifier's behavior using quasi-static characterization, as well as a point-search algorithm to find a sequence of (input power, input bias voltage, output bias voltage) points that constitute the biasing functions at input and output, without making assumptions on a particular shape (e.g., linear variation with envelope amplitude). In addition, it presents a comparison of the response of HBT and pHEMT transistors to different bias functions, and deepens on the idea of using first and second order polynomials for the bias functions, to be able to control the bandwidth of the signals.

The possibility of searching heuristically to find *optimal* bias trajectories is explored in Chapter 4. An algorithm is proposed based on representing the bias function search as a constrained optimization theory problem. The derivation of the constraints, and a multi-objective error function, together with measures for linearity and dissipated power is explained. (The linearity measure is different from the classical least squares measure, it aims to minimize third and fifth order distortions.)

Finally, Chapter 5 introduces a full automatized experimental setup that allows to apply dynamic biasing to different transistor technologies. Dynamic biasing is tested on a discrete pHEMT GaAs amplifier, a discrete pHEMT GaN amplifier, and on an MMIC HBT transistor. The principles of the methodology from Chapters 3 and 4 are extended to optimize the amplifier's performance in terms of power added efficiency and adjacent and alternate channel ratios, without having to rely on simulation data.

The research methodology is based on circuit simulations in Agilent ADS, load-pull measurements, nonlinear optimization in MATLAB, and measurement of several devices with modulated signals using a "custom-made" measurement setup. The transistor technologies studied include discrete GaN HEMT, discrete and MMIC GaAs pHEMT transistors, and HBT transistors in MMIC.

The manufacturing of the bias supplies was oriented towards providing low distortion with frequency and load variations within an adequate bandwidth (5 MHz), as well as an accurate measurement of the instantaneous current for efficiency calculations. The efficiency of the bias supplies is not addressed in this work, as it is a research problem on its own right [26],[5],[4]. Instead, is set on the concept of varying bias with power to limit the bandwidth of the bias waveforms. A discussion

about the different applications and advantages of using dynamic gate biasing, dynamic drain biasing or both, and the impact on linearity, PAE and output power is presented in Chapter 6, which is rounded up with ideas that hopefully will awaken interest for future research.

Chapter 2

Dynamic biasing in perspective

This chapter presents a theoretical framework to put into perspective the research done in this work on dynamic biasing. Different transistor materials and technologies are reviewed, as well as modern efficiency and linearity enhancement methods. The aim is to highlight the strengths, limitations, and application area of each topic.

2.1 Semiconductor technologies

A transistor is a semiconductor device in which the output current can be controlled as a function of the input voltage (e.g., field effect transistor, FET) or current (e.g., bipolar junction transistor, BJT). Transistors can be used to build amplifiers, oscillators and mixers at different frequencies and operating bandwidths for a variety of applications. This section focuses on the use of transistors in the context of high power RF amplifiers only.

2.1.1 Output power in microwave PAs

For microwave PAs, high output power and gain are important properties that are more difficult to obtain than in low frequency applications. For a transistor to yield high output power at RF, the following conditions must be met without introducing excessive resistive or capacitive parasitics [25]:

1. *Maximize the channel current.* In FETs, channel current can be increased by increasing the gate width. This will alter device parasitics such as gate-to-source capacitance and the gate resistance, and the maximum operating frequency will be reduced. Higher gate resistance leads to lower gain for a power FET device. To allow for adequate current and obtain good thermal properties, power devices are designed as a number of cells connected in parallel often interconnected by air bridges. The cell structure will nevertheless introduce inductive and capacitive parasitics. Since one gate segment

can ruin the whole device, the manufacturing of the gate must be flawless, which becomes easier with a longer gate. This will unfortunately lead to reduced transconductance and increased capacitance, resulting in further gain diminishment.

2. *Maximize the breakdown voltage.* The gate-to-drain breakdown voltage establishes a fundamental limit to the power capability of the device. It can be maximized by optimizing the ohmic contact technology, using a recessed-gate structure, and leaving adequate space between gate and drain. It is also heavily dependent on the semiconductor materials that build the transistor [24].
3. *Maintain good heat-dissipation properties.* The DC-to-RF efficiency of a power amplifier in practice is rarely greater than 50%. A power device must dissipate 1.5 to 4 times its RF output power as heat in the presence of other chips that also emanate heat. The chip must be designed carefully to minimize its thermal resistance. Bipolar devices are subject to thermal instability (thermal runaway for BJTs, and thermal collapse for HBTs).

2.1.2 Comparing semiconductor materials

The current semiconductor market holds mature material technologies such as silicon (Si) and gallium arsenide (GaAs). Silicon-based MOSFET (metal-oxide-silicon field effect transistor) and LDMOS (laterally diffused metal-oxide-silicon) transistors are especially useful for high power applications at the VHF (very high frequency) and UHF (ultra high frequency) bands [27]. GaAs-based MESFET (metal semiconductor field effect transistor) and HEMT (high-electron-mobility transistor) cover a very wide range of frequency bands and power levels [28],[29]; from handheld devices to base stations. Heterojunction bipolar transistors (HBT) made of both Si and GaAs are also popular in today's market.

Silicon LDMOS covered approximately 90% of the high-power RF amplification market for base stations up to 2005 in the frequency range around 2 GHz. The remaining 10% was addressed by GaAs pHEMT technology. However, this equilibrium has been disrupted by the introduction of wide bandgap materials and related RF devices such as silicon SiC MESFETs and GaN HEMTs [30].

Table 2.1 compares some important physical properties of Si, GaAs, SiC, and GaN. The larger bandgap of SiC and GaN translates directly into a much larger breakdown field, which in turn implies a much higher breakdown voltage. Though GaAs possesses the highest electron mobility, the higher saturated velocity of GaN and SiC make them better for high frequency power operation. In addition, the larger thermal conductivity of SiC and GaN enables lower temperature rise due to self heating [31]. SiC has a clear advantage over GaN in thermal conductivity, but the AlGaIn/GaN heterojunction which can be grown in the GaN HEMT devices enables superior current handling capability even compared to lateral SiC devices

Table 2.1: Comparison of the physical properties of Si, GaAs, SiC, and GaN.

Properties	Si	GaAs	4HSiC	GaN
Bandgap (eV)	1.11	1.43	3.26	3.42
Breakdown Field (10^6 V/cm)	0.25	0.35	3.5	3.5
Saturated Velocity (10^7 cm/sec)	1.0	1.0	2.0	1.5
Electron Mobility ($\text{cm}^2/\text{V}\cdot\text{sec}$)	1350	6000	800	1000
Hole Mobility ($\text{cm}^2/\text{V}\cdot\text{sec}$)	450	330	120	300
Thermal Conductivity (W/cm-K)	1.5	0.46	4.9	1.7
Relative Dielectric Constant	11.8	12.8	9.7	9

[32]. Moreover, GaN can be epitaxially grown on SiC, taking advantage of its higher thermal conductivity. Though SiC is a wide bandgap material, its poor electron transport capability hinders its use in very high frequency amplifiers. SiC has also been limited by expensive, small and low-quality substrate wafers. The capability of handling higher breakdown voltages and providing high current density makes GaN specially suited for high power applications. Larger powers can be handled in a small die, and the large breakdown voltage results in a larger output impedance. A smaller die reduces the parasitic capacitance, which together with a larger output impedance makes it suitable for broadband, switching, and bias modulated amplifier designs.

There are, however, still some problems in the production of FETs based on III-V wide bandgap compounds mainly due to trapping centers related to surface, material, and/or interface states. Some of the observed effects are threshold voltage shift, current collapse, reduction of short channel effect, light sensitivity, transconductance frequency dispersion, gate-lag and drain-lag transients, and limited microwave power output [33]. There is much ongoing research on wide bandgap materials, but cost and reliability continue to favor GaAs and Si in several commercial applications.

2.2 Transistor types

2.2.1 MESFET

MESFETs are most commonly fabricated on a GaAs substrate. First, a semi-insulating buffer layer is grown on a semi-insulating GaAs substrate. Then, an n -doped epitaxial layer is grown to realize the FET's active channel. The source and drain ohmic contacts are connected to the channel, as well as the Schottky-barrier gate. When the gate-to-source voltage (v_{gs}) is held constant and the drain-to-source voltage (v_{ds}) is gradually increased from zero, the drain current varies linearly with v_{ds} , since a depletion region is formed that progressively becomes wider, "strangling" carrier flow. When the channel is shut due to full depletion,

carriers move at saturation velocity and the drain current is held constant even if v_{ds} is further increased. This saturation mode of operation is used when biasing power amplifiers. The width of the channel can also be directly controlled by varying the v_{gs} voltage [25].

GaAs MESFETs possess higher mobility than Si devices, and are capable of efficient operation at higher frequencies. They have lower break-down voltages compared to MOSFETs or JFETs, and usually work in depletion mode, that is, with negative gate voltage. They suffer of poor linearity because the input capacitance varies with voltage, and the output capacitance is also bias and frequency dependent [27].

The superior mobility and high breakdown voltage of SiC in high power applications gives SiC MESFETs a high frequency response comparable to that of GaAs MESFETs, and breakdown voltages double that of LDMOS. This results in a power density of 10 W/mm^{-1} , ten times that of a GaAs MESFET [27]. Chen [34] reports an S-band 4H-SiC MESFET with a pulsed (300 us, 10 %) output power of 250 W at 2 GHz, a gain of 10.5 dB, and a PAE of 30 %.

2.2.2 HEMT

The HEMT differs from the MESFET in that the channel is formed by a heterojunction instead of a epitaxial layer. The heterojunction consists of an n -doped AlGaAs Schottky layer, an undoped AlGaAs spacer, and an undoped GaAs buffer. The discontinuity in the band gaps of AlGaAs and GaAs causes a thin layer of electrons (“two-dimensional electron gas” or “2-DEG”) to form below the gate at the interface of the AlGaAs and GaAs buffer layers. The GaAs buffer contributes to a relatively high breakdown voltage [27].

Since the channel is not doped, impurity scattering is minimized yielding high electron mobilities, which results in high-frequency response and low noise figure. The charge density of the 2-DEG layer is controlled by the gate voltage. Though it may be insufficient for high power applications, the charge density can be increased by using several heterojunctions [25]. Since these are fabricated with advanced epitaxial technologies, the cost of the HEMT is higher than that of the MESFET.

Pseudomorphic HEMT (pHEMT)

The pHEMT employs a thin $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel because InAs has a wider bandgap than GaAs, though the lattice constant mismatch limits the content of In up to 22 %. With an increase in bandgap discontinuity, the number of carriers in the 2-DEG will also be increased, resulting in higher current density. pHEMTs provide high efficiency and reliability, and are usable in frequencies as high as 80 GHz [27].

Despite the interest in GaN HEMTs, research is still being done on GaAs pHEMTs. Powell et al. [35] reported an MMIC GaAs pHEMT with single-tone drain efficiency over 65 %, and bandwidth greater than 30 % in X-band operation.

Using waveform engineering, a GaAs pHEMT wideband PA with an an output power of 0.5 W, 5 GHz to 10 GHz operation and 55-% single-tone PAE was built [36].

GaN HEMT

AlGaIn/GaN HEMTs are fabricated on either Si or SiC substrates due to the lack of native GaN substrates [31]. The choice of substrate determines important properties that have a direct impact on device performance and reliability. GaN HEMTs offer ten times higher power density and wider bandwidths due to higher input and output impedances, which they maintain at high frequency operation (up to 12 GHz). LDMOS performance, on the other hand, drops as the operation frequency exceeds 3 GHz, and GaAs suffers from low power though it has the potential for high frequency operation. An added benefit of GaN is its lower output capacitance and “on” resistance which allows for a better realization of drain-modulation and switching-mode amplifiers [37]. An interesting study reports a W-band MMIC amplifier in 0.12-um GaN HEMT technology with an output power of 25.4dBm at 76.5 GHz with continuous wave operation [38]. Output powers of 8 W at 10 GHz with 30-% drain efficiency have been demonstrated [27].

2.2.3 HBT

HBTs have played a major role in power amplification for microwave and millimeter-wave applications such as handset phones and wireless local area networks [39]. HBT operation is essentially the same as that of a BJT. It has the same $n-p-n$ structure, but a heterojunction is used at the base-emitter junction, instead of a $p-n$ junction. The heterojunction employs dissimilar semiconductor materials to provide an energy barrier between emitter and base. Thus heavy base doping is possible, minimizing the base resistance and maximizing the maximum operation frequency. They are mostly available in IC technologies, and though they can be realized in III-V technologies, SiGe HBTs offer high performance at lower cost. HBTs have lower parasitic resistances, and lower fringing capacitance. Power HBTs can be fabricated by paralleling a number of devices having long, narrow emitters [25]. In addition, HBTs appear to require less power back-off for linear amplification; they combine good linearity performance at an input power level appropriate for good PAE. There have been great improvements in their high frequency characteristics and reliability [40].

AlGaAs/GaAs HBTs are capable of producing several watts and are widely used in wireless handsets and in MMIC circuits at frequencies up to X band. The use of InP in an HBT further enhances mobility, and therefore improves high frequency response. Higher gain and efficiency are possible due to lower turn-on and knee voltages. The InP in the collector increases the breakdown voltage for higher output power [27].

InGaP HBTs have superior reliability in comparison to the widely used AlGaAs. In addition due to the minimum conduction band offset between InGaP in the emitter and GaAs in the base, InGaP HBTs have improved uniformity of current gain with changes in applied current and operating temperature. These factors account for the high power density, high efficiency, and superior linearity of InGaP HBTs compared to AlGaAs HBTs or even GaAs MESFETs at similar frequencies [41],[42]. Triquint offers an InGaP HBT process, where the emitter is made of InGaAs/n+, GaAs/InGaP, the base of p+ GaAs, the collector of n- GaAs, and the sub-collector of n+GaAs Substrate. The maximum operation frequency is of 65 GHz with a base-emitter voltage of 1.15V, with a collector-to-base breakdown voltage of the common emitter of 24 V for a standard cell of $3\text{ um} \times 3\text{ um} \times 30\text{ um}$ [43].

2.3 MMIC

Monolithic microwave integrated circuits (MMICs) are fabricated from a single piece of semiconductor material. Both high-performance microwave transistors and low-loss passive components and lines are grown over the same substrate, avoiding the need for interconnecting wires that would introduce parasitics. Given that the foundry provides adequate models for its components, the design process becomes repeatable within the tolerances of the MMIC process. This is of great importance, since it eliminates the need for tedious revisions of the board layout, and empirical adjustments in component values. Nevertheless, the fabrication process is very time-consuming and costly, and often the correct functionality of the circuit can not be tested until the whole of the processing is complete [44].

The dimension of MMIC transistors is in the order of microns, and they weigh an order of magnitude less than their equivalent hybrid MICs, which makes them suitable to mobile electronic applications. MMICs cover from microwave- to millimeter-wave frequencies, and are used in mobile phones, wireless local-area networks (WLANs), Global Positioning System (GPS) receivers at the low GHz end; up to earth observation radiometers and security scanners up in the hundreds of gigahertz end. Optical-fiber, satellite communications, point-to-point links, automotive industry with vehicle identification, and military applications are also inside the MMIC market. Since the reliability is well understood for Si and GaAs, these processes qualify for space-borne applications [44].

This work includes simulation and measurements for two different MMIC processes by Triquint: the TQPED 0.5 um E/D pHEMT process [3] (only the enhancement mode transistor was used), and the TQHBT3 InGaP HBT process [43]. The processes include two thick and one thin global metal interconnect layers encapsulated in a high performance interlayer dielectric. Thick metal interconnects are used for adequate thermal management, together with high-density high-value capacitors, and precision nichrome resistors. The HBT transistor is built with a

carbon-doped base and a 3- μm width InGaP emitter, with good performance and reliability; while the pHEMT transistor uses a 0.5 micron optical gate for both enhancement and depletion modes.

2.4 Efficiency enhancement

2.4.1 Doherty amplifiers

The Doherty amplifier is becoming widely deployed in current communication systems, though it was first proposed in 1936 for use in high-power broadcast transmitters, where it continues to be used due to its relative simplicity of implementation and convenience for high-power systems [45].

Two or more amplifiers are combined so that the system operates efficiently with envelope-varying signals. The efficiency gains can be as high as two or three times that of a conventional class-B PA when operating below peak envelope power. The linearity achieved by the Doherty system is reliant on the linearity of the amplifiers used in its implementation.

The Doherty amplifier is based on amplifiers connected in parallel. Let us take the case of two amplifiers, PA1 and PA2. The first one, PA1, is usually biased as a class-AB amplifier with a quarter-wave line at its output, while the second one, PA2, can be in deep class-AB, -B or -C mode [46]. PA2 can be switched on and off depending on the envelope level at the input. Both amplifiers have their outputs connected to the load R_L . A typical configuration is shown in Figure 2.1. For low input power levels PA1 is operating as a linear amplifier, while PA2 is switched off. When the input power reaches a certain threshold, usually at 6-dB back-off from the peak envelope power (PEP), PA1 comes into saturation. Above that threshold PA2 will be switched on and begins operating as a linear amplifier. Then, the voltage at the load is given by

$$V_L = R_L(I_1 + I_2) \quad (2.1)$$

where I_1 and I_2 are the currents at the output of amplifiers PA1 and PA2, respectively. The impedance at the output of the quarter-line in the branch of PA1, is given by V_L/I_1 , and is greater than R_L . Therefore the Doherty system is in itself a load modulation system. Once the input power has reached the PEP, both PA1 and PA2 will have reached saturation, and the efficiency of the system is at its maximum.

The Doherty system can be an excellent choice for some applications. Its efficiency rivals that of alternative techniques, including envelope tracking. It is simple to implement, does not place high demands on the RF power devices, and does not require an envelope modulator as in EER or ET. Nevertheless, the need for quarter-wave lines and accurate phase alignment between the amplifier-paths restricts the system to single frequency operation, and can also limit the band-

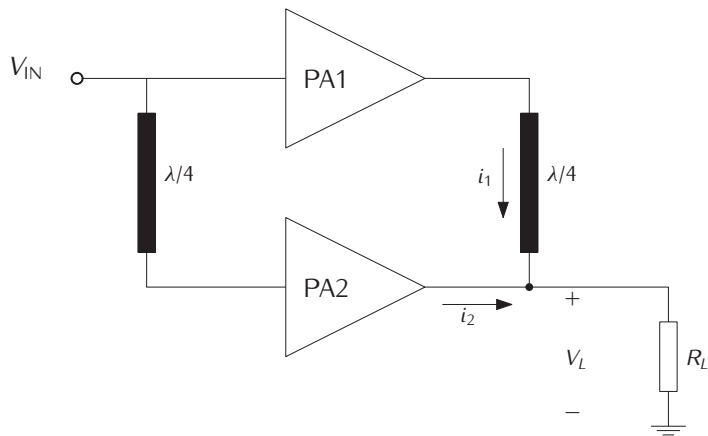


Figure 2.1: A typical Doherty amplification system [1].

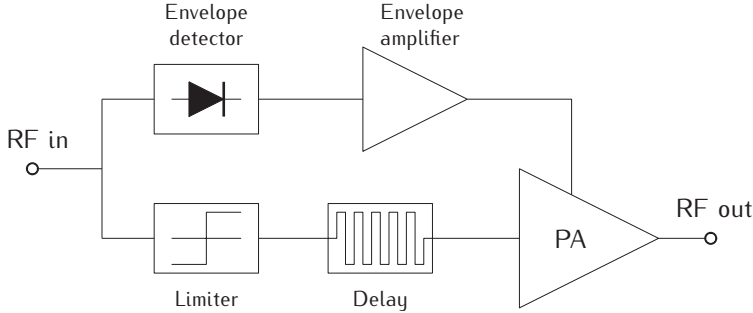


Figure 2.2: A simplified envelope elimination and restoration system [2].

width. Linearity performance is relatively poor, so the Doherty system requires the addition of a linearization scheme. In modern implementations a DSP controls the drive and bias to the two PAs for precise control and higher linearity [27]. Finally, the PAs used in the system must be able to cope with variable resistive load impedances. These properties make it unsuitable for point-to-point radios operating in a variety of bandwidths and carrier frequencies.

2.4.2 Envelope Elimination and Restoration

Envelope elimination and restoration (EER), also known as the Kahn technique, enables switching amplifiers to operate with envelope-varying signals. The input signal passes first through an amplifier with a very high gain so as to generate a squared waveform containing only the phase of the original signal. Such an amplifier is commonly referred to as the limiter. This phase-only signal will be the input to the amplifier. On the other hand, an exact scaled replica of the envelope is fed into the bias of the switching amplifier, so that the output contains both phase and envelope information. The simplified mechanism is illustrated in Figure 2.2.

Though the technique is attractive because of the high efficiency inherent to switching amplifiers, it is very sensible to time misalignment between the bias and the RF signal, and to distortions in the bias signal due to imperfect envelope amplification (i.e., the envelope amplifier must be highly linear). When the RF signal is large in bandwidth, the high frequency components will be distorted due to the limited frequency response of the envelope amplifier. Recall from Chapter 1 that the envelope amplifier must be highly efficient so that the system's overall efficiency remains high, so in practice the efficiency/linearity trade-off has been moved from the RF-amplifier to the envelope amplifier.

2.4.3 Envelope Tracking

Class-B amplifiers have the convenient property that the drain current varies with the envelope of the input signal. By varying only the drain bias voltage with the envelope of the input signal, the amplifier can ideally achieve a class-B efficiency regardless of the level of the input envelope, while holding a flat gain (Figure 2.3).

The knee voltage, the nonlinear transconductance, the variation of the drain-to-source capacitance with bias, among other factors, impair the ideal performance of the amplifier. The purpose of varying the drain bias is to supply only as much voltage as required to amplify the instantaneous envelope amplitude, therefore identical reproduction of the envelope is not indispensable as in EER. Nevertheless, the bandwidth of the bias signal at the drain is still of concern. An alternative is to filter it and compensate the memory effects at the predistorter [17],[18].

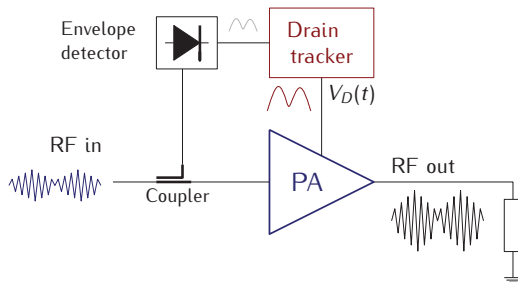


Figure 2.3: Simplified envelope tracking system.

2.4.4 Linear amplification with nonlinear components

Linear amplification with nonlinear components (LINC) is an outphasing amplification technique that dates back to the 1930s. Consider an RF input signal,

$$x(t) = A(t) \cos(w_0 t + \phi(t)) \quad (2.2)$$

with envelope $A(t)$ and phase $\phi(t)$ that varies in time around the carrier frequency w_0 . As illustrated in Figure 2.4, the signal can be split in two signals of constant envelope [2],

$$x_1(t) = V_0 \cos(w_0 t + \phi(t) + \theta(t)) \quad (2.3)$$

$$x_2(t) = V_0 \cos(w_0 t + \phi(t) - \theta(t)), \quad (2.4)$$

where $2\theta(t)$ is the phase difference between $x_1(t)$ and $x_2(t)$ that varies with the envelope $A(t)$:

$$\theta(t) = \cos^{-1} \left(\frac{A(t)}{V_0} \right). \quad (2.5)$$

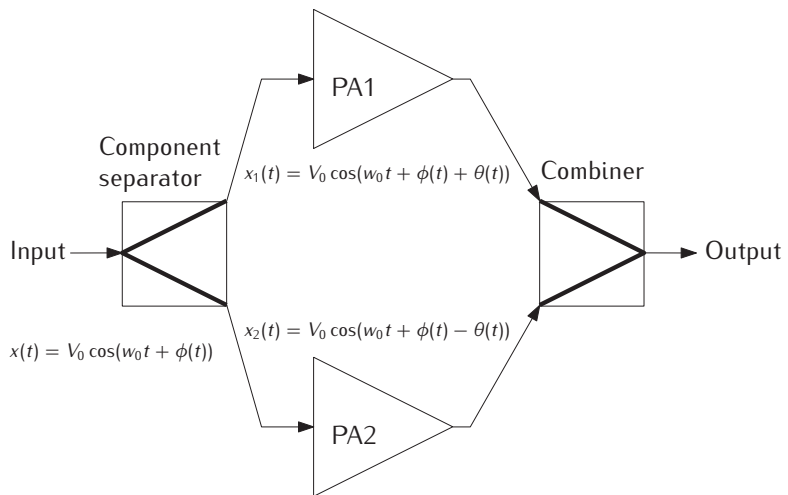


Figure 2.4: Schematic of a LINC transmitter [2].

This approach is advantageous in that the amplifiers can be operated efficiently due to the constant-envelope input, and that the linearity of the output is insensitive to the nonlinearities of the individual amplifiers. Nevertheless, the linearity of the LINC transmitter is sensitive to the imbalances between the two PA branches, the quadrature error of the in-phase/quadrature (I/Q) modulator, and the quantization noise of the DSP [47].

The phase of the output current is that of the vector sum of the two PA-output voltages. If the out-of-phase signals are directly summed in a non-hybrid combiner, each of the amplifiers will be “seeing” a reactive load impedance, in which case the current drawn from the PAs is proportional to the transmitter-output voltage. Then the efficiency will depend on the input power as in a class-B PA. The Chireix technique uses shunt reactances on the inputs to the combiner to tune-out the drain reactances at a particular amplitude. Though the efficiency at high and low amplitudes may be degraded, the average efficiency can be maximized for any signal [48]. This technique is seldom used at microwave frequencies because of the non-ideal behavior of the amplifier as a voltage source.

The PAs can be isolated from the reactive loads using hybrid combining, presenting resistive loads to both amplifiers at all input envelope levels. Since both amplifiers operate at maximum output power all of the time, the efficiency characteristic will be similar to that of a class-A, though the efficiency at peak envelope power will be much higher.

2.5 Linearity enhancement

2.5.1 Feedback

In feedback linearization, a fraction of the output signal is compared to the input signal, and the resulting error signal is the input to the PA. As Figure 2.5 shows, the term “compared” in this case means subtracted, and the comparison can be done in terms of RF amplitude, envelope, envelope and phase, or I and Q components. For detailed figures of different variants of the feedback systems refer to Kenington [2], or to Raab et al. [49].

RF feedback

A portion of the RF output is compared to the RF input without any detection or down-conversion. Since large feedback delays result in instability, and gain loss at RF is expensive, RF feedback in discrete circuits is usually restricted to HF and lower VHF frequencies. It can be applied within MMIC devices, however, well into the microwave region. Though it can reduce intermodulation distortion (IMD) by 10 dB, even better suppression is possible at a fixed power level [27].

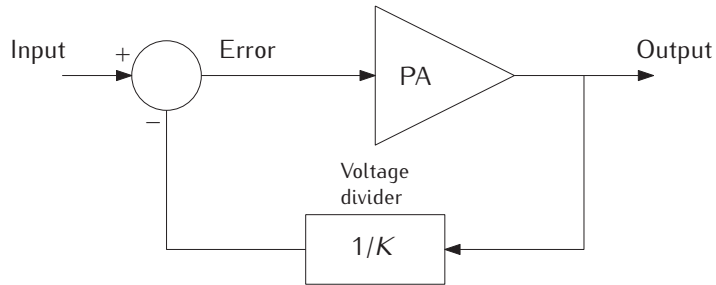


Figure 2.5: The principle of feedback linearization (from Kenington [2]).

Envelope feedback

This approach corrects for in-band distortion, and can be implemented at system level, or at an amplifier level. Since only the envelopes of the input and output signals are compared, it is effective only if AM/AM nonlinearity is the dominant source of distortion in the PA. Therefore its use is generally restricted to relatively linear class-A or -AB amplifiers.

Polar-loop feedback

By adding a phase-locked loop branch to the system, the input/output phase difference can be corrected. Limiters can be used to detect the phase of the signals at IF level, or alternatively the envelope and phase modulated signals can be supplied and compared at baseband. The main disadvantage of this approach is that different bandwidths are required for the amplitude and phase feedback paths. In general, the phase bandwidth must be five to ten times the envelope bandwidth.

Cartesian feedback

Two identical feedback loops operate for the I and Q channels. While the output signal is demodulated to obtain its I and Q components, these are available for the input signal at the digital end of the system. Reported results mention a reduction in ACPR greater than 35 dB for a nonlinear class-C for the IS-136 standard.

Limitations

Though feedback has been successfully applied to audio amplifiers, some of its limitations can become impractical at RF frequencies [2]:

- Larger bandwidths are involved.
- The cycle-time for the feedback loop is smaller.

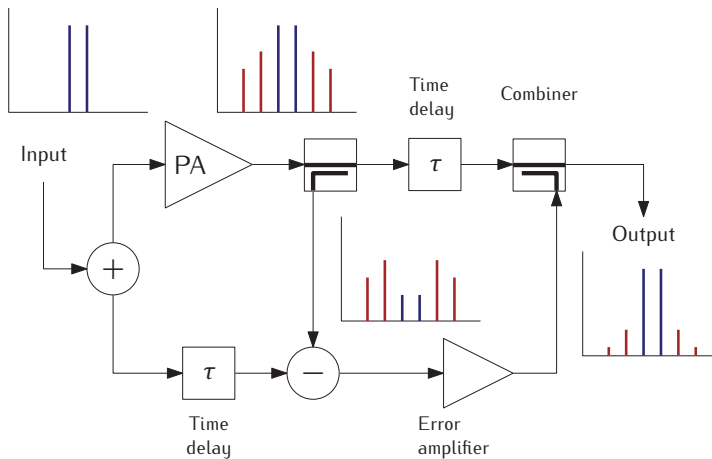


Figure 2.6: A basic feedforward amplifying system (from Kenington [2]).

- The forward path gain is more expensive to achieve due to the inherent low gain and high cost of RF power devices.
- Linearity requirements can be much greater (e.g., $\text{IMD} \leq 70$ dBc).

Finally, if only small amounts of feedback can be applied to individual power stages to maintain an adequate gain, the resulting linearization effect will be proportionately less.

2.5.2 Feedforward

Feedforward achieves linearization by adding an error amplifier in parallel to the RF PA (Figure 2.6). The error amplifier is fed with a small portion of the output of the RF PA, subtracted by a fraction of the input signal to the RF PA, so that it only amplifies the distortion products from the RF amplifier. The output of the error amplifier is then added 180° out of phase to the output of the RF PA so as to ideally cancel all the distortion products [2].

For a 30-dB reduction in distortion, the amplitude mismatch is approximately ± 0.27 dB, while the phase mismatch is around $\pm 1.7^\circ$. The limiting factor is nearly always the bandwidth over which a given accuracy can be obtained [49].

The two largest hurdles to wideband performance are delay mismatch and unwanted frequency dependence of the circuit elements [50]. These limitations can be overcome using an adaptive architecture such as the one proposed by Smith and Cavers [50]. They achieve a reduction of 40 dB of 3rd order intermodulation products (IM3) over a 40-MHz range, and a reduction of 25 dB or more over an 80-MHz range. Suzuki and Narahashi [51] report a 120-MHz operation bandwidth

for an ACPR of -45 dB for a W-CDMA signal for 39-dBm output power. Though feedforward can be implemented entirely with analog circuitry, digital processing can be used to track parameter changes in the main PA and other circuitry to enhance the bandwidth of the system [52]. Typical values of IM3 cancellation for manufactured equipment are around 25 dB to 35 dB [53],[54].

A distortion free error amplifier is also critical for performance. Additional feedforward loops can be added to linearize the error amplifier if necessary. Using several loops makes the system more robust in case one of the error amplifiers fail, and the component in the loops require a lower power rating [2]. Using digital and analog techniques in an adaptive architecture to correct gain and phase (i.e., an automatic control scheme) will not only enhance the system's bandwidth, but will also compensate for changes of device characteristics with time and temperature [49].

The efficiency of a feedforward system may therefore be only 10 to 15 percent for typical multicarrier signals [49]: for an output coupler with a 10 dB coupling factor, 90 % of the main PA's output reaches the load (0.46 dB gain drop), and the error amplifier must produce 10 times the distortion power of the main amplifier. In addition, the PAPR of the error signal is much higher than that of the main signal, and several dB back-off might be required to achieve the desired linearity.

The main advantages of feedforward are that the gain is not reduced, and that the gain-bandwidth is conserved within the band of interest. Stability is not such an issue as it is for feedback systems, since the basic feedforward configuration is unconditionally stable. Only cost limits the number of stages [2]. A disadvantage is that the matching between the circuit components in amplitude and phase must be very high over the bandwidth of interest. Tracking device characteristics, as well as adding loops to reduce the distortion of the error amplifier adds extra complexity, size, and cost; and the efficiency of the system will be modest.

2.5.3 Digital predistortion

Most modern transmitters utilize either a DSP (digital signal processor) or an FPGA (field programmable gate array) for the bit encoding, digital modulation, pulse shape filtering, among other tasks, as these devices have become cheaper and more power efficient [2]. In digital predistortion (DPD), the digitally modulated signal is modified by an inverting complex function either at baseband, IF or RF level so as to compensate for the nonlinear distortion of the PA. The output of a PA with an ideal DPD would have constant gain and phase shift respect to the input envelope level; the calculations for the DPD signal are carried out by the DSP.

The inverting complex function can be implemented using a look-up table (LUT), or a set of mathematical functions, such as polynomials. The LUT can be indexed by the envelope of the input signal, or by its I and Q components, which yields a better performance at the expense of a higher number of table values and

slower convergence [48]. The use of polynomials for DPD is also practical because the maximum order of the polynomial set controls the computational complexity and the bandwidth of the DPD signal.

If desired, thermal and electric memory effects can also be corrected with DPD. They are usually extracted and represented by Volterra kernels or reduced complexity memory polynomials. This will however require higher complexity for the characterization of the PA, the inversion of the PAs response, and the computation of each sample of the DPD signal. The linearization process can be adaptive so that either the values of the LUT are refreshed, or the parameters of the predistortion function are recalculated with each new set of input samples to the PA [55]. In addition, crest factor reduction can also be added so that the amplifier is driven harder, allowing more efficient amplification.

The results obtained from predistortion without memory might be modest in comparison to those of a feedforward transmitter, what is attractive is the simplicity of implementation, since DPD relies on the signal processor. For the case of point-to-point radios very high order predistortion may not be affordable, nevertheless DPD is practical since the principle is independent of the carrier frequency, and can be used for signals of different bandwidth. As the bandwidth increases, though, the order of the nonlinearity that the predistorter can correct will decrease.

2.6 Summary

The context of this research project is in the field point-to-point radios with bandwidths as high as 40 MHz and carrier frequencies between 4 GHz to 40 GHz. The goal is not to study an amplification system and test it along the full frequency range, but to propose an amplification solution that neither depends heavily on the center frequency, nor on specific signal characteristics such as bandwidth, or envelope variability.

As explained in sections 2.1 and 2.2, there are several available substrates and transistor types in the market. GaAs pHEMT, GaN HEMT and GaAs HBT are rather representative in the sense that they cover a wide range of output power capacity and bias voltages. Furthermore, the intrinsic properties of the materials are rather different, making it interesting to study their response to bias variation.

Section 2.4 reviewed several efficiency enhancement methods. Doherty amplifiers can provide substantial improvements in efficiency, but due to the need for quarter-wave lines or line components they can not operate flexibly along varying center frequencies as required in point-to-point radios. Envelope elimination and restoration can offer very high efficiencies, but the successful manufacturing of a switching amplifier above a few gigahertz is not trivial. The implementation of a “perfectly linear” envelope amplifier at high bandwidths can also be a considerable challenge. In that sense envelope tracking and dynamic biasing represent a good

compromise, since the envelope amplifier is not dependent of the center frequency, only the biasing functions for the gate and drain need to be modified according to the amplifier, which can be done digitally. Nevertheless, the limitation of the bandwidth of the drain bias must be handled with care.

When it comes to linearity, feedback offers linearity improvement at the expense of high gain losses and potential instability. Though feedforward has strong linearization capabilities, it offers only modest overall efficiency, and the need for several loops to compensate for the non-ideal error amplifier increase hardware complexity. In addition, the tuning of the main path and the error path is different for every device and frequency of operation. Though linear amplification with nonlinear components can offer as high efficiency as that of the two amplifiers that compose the system, the combiner makes the efficiency decay as a class-A or at best class-B amplifier; not to mention the dependency on frequency. If an inductor and a capacitor are used as proposed by Chirieux, the efficiency enhancement will work only for signals with moderate envelope variation. With digital predistortion, on the other hand, only modest linearity improvements can be attained (approx. 10 to 25 dB), depending on the complexity of the algorithm. What is appealing is that DPD can be simple to implement provided that the DSP or FPGA has enough computational power and bandwidth. Though the available bandwidth imposes a limit on the order of the predistorter, the procedure for the extraction of the polynomial coefficients is exactly the same regardless of the center frequency and system bandwidth.

The chapters that follow describe methods based on simulation and measurement to apply dynamic biasing to different transistor technologies: an InGaP HBT transistor, discrete and MMIC GaAs pHEMT amplifiers, and a discrete GaN HEMT amplifier.

Chapter 3

A case study of dynamic biasing

3.1 Introduction

The two previous chapters have put into context the relevance and application of dynamic biasing, as well as the challenges around it. This chapter opens with a general picture of dynamic biasing. A simple theoretical framework is developed assuming a transistor with constant transconductance and an ideal strongly non-linear response. The resulting drain current, efficiency and gain characteristics from these equations highlight the implications of varying the bias as a function of power instead of envelope voltage or constant class-A bias. The design case of a GaAs pHEMT MMIC amplifier is reviewed, highlighting the impact of the bias point to which the amplifier is matched in the behavior of small-signal gain. After describing a primer characterization method based on single-tone simulations, an algorithm is presented based on joining different bias points to minimize parameters such as gain variation and phase variation; and maximize efficiency. The output of the algorithm is compared in simulation against continuous bias functions for a modulated input signal.

3.2 A general picture

As explained in Chapter 1, this work develops around point-to-point radios, so the amplifying system is driven by modulated signals with highly variable envelopes. High efficiency is desired, but compliance with linearity standards such as the spectral mask is important. The amplifier is driven at moderate compression levels (i.e., 1, or 2 dB) as opposed to base station envelope tracking PAs that are driven at heavy compression to reach peak efficiency at each drain bias voltage level [12],[56].

Figure 3.1 presents a simplified description of the dynamic biasing system. The baseband signal is digitally generated at the modulator; if desired digital predistortion can be applied. The upconverted signal is fed into the RF amplifier.

The bias waveforms are also generated at the digital end with normalized voltage levels (for example ± 1 V) and input into the gate/drain trackers. They have a direct dependence on the original baseband signal, and must be synchronized with the RF input. The drain tracker operates as an adjustable voltage amplifier that feeds the RF PA with the necessary bias current. The current levels at the gate are insignificant, so the gate amplifier is simply a voltage amplifier. An efficient construction of the drain tracker—still subject of current research [26],[5]—is out of the scope of this work. Experiments have been carried out for different amplifier technologies as explained later on, but the main goal when designing the trackers was to make them linear within a reasonable bandwidth, and usable for different devices.

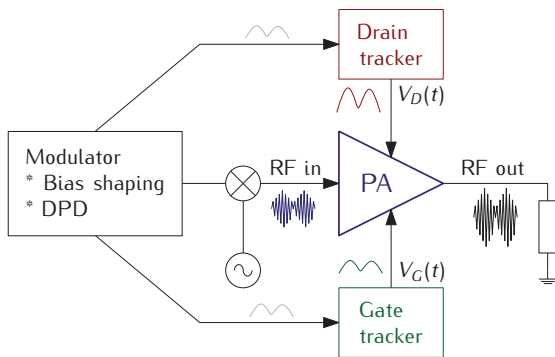


Figure 3.1: Simplified block diagram of a dynamic biasing system.

3.3 A theoretical insight into bias variation

3.3.1 Introduction

The following section aims to explain the implications of having gate and drain bias varying with the input power instead of the envelope of the input signal for the simplest transistor model possible [9]: one with perfectly linear transconductance when the gate voltage is between the threshold voltage and smaller than the saturation voltage, and with hard clipping outside that range. (The threshold gate voltage and drain knee voltage are assumed to be zero.) If the transistor was matched for maximum output power and biased as a class-A for maximum envelope level, and both gate and drain biases varied from this class-A bias point towards zero as the envelope amplitude decreased, the average drain efficiency would be 50%, and the gain would be perfectly flat all along the power range [22]. This is depicted in Figure 3.2.

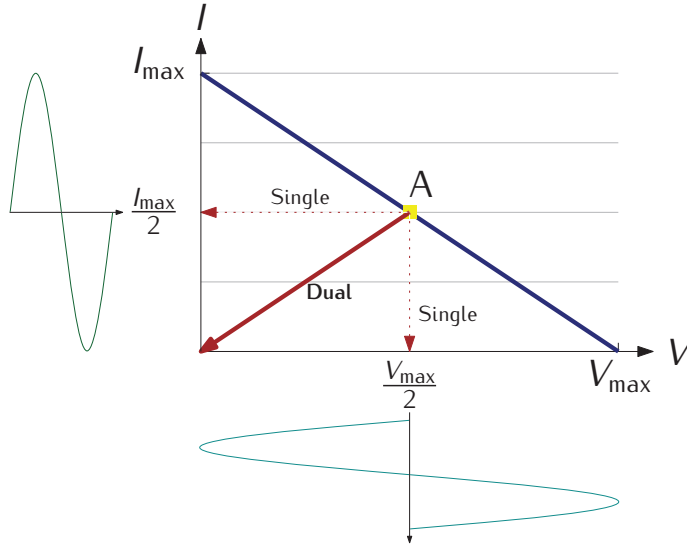


Figure 3.2: Dynamic biasing applied to an idealized transistor following envelope amplitude. Variable V (x-axis) represents the collector/drain voltage, while I represents the collector/drain current. The transistor is biased in class A condition at maximum envelope amplitude, i.e., $(V, I) = (V_{\max}/2, I_{\max}/2)$. The thick diagonal arrow shows how varying both gate and drain biases ensures class-A operation along the envelope amplitude range. The horizontal and vertical arrows illustrate drain-only and gain-only bias variation, respectively.

Nevertheless, equations show how varying the gate bias with input power between threshold voltage and saturation changes the conduction angle from 180° to 360° —between class A and class B operation. This implies that the average drain efficiency is greater than 50%, but the gain response is not perfectly flat (the gain of a class-B PA is 6 dB below that of a class-A for such an ideal transistor). It also shows that varying the drain voltage between knee voltage and class-A drain voltage would lead to clipping of the drain AC waveform at the lowest output power range, since the drain bias must always be greater than the AC drain voltage to avoid clipping, and the latter is determined by the conduction angle and the input envelope level. The idea that the optimum matching might be slightly different than the maximum-output-power class-A matching is illustrated when the gate bias is varied quadratically with input power. The possible benefits from clipping the drain bias waveform are also discussed. Finally, calculations for high order QAM signals are presented to highlight the efficiency improvements attainable.

3.3.2 Why bias depending on power instead of envelope

Let us consider a modulated signal in its baseband equivalent (complex) form:

$$\tilde{v} = v \exp j\varphi = v_i + jv_q. \quad (3.1)$$

The signal's envelope would then be

$$|\tilde{v}| = v = \sqrt{v_i^2 + v_q^2}. \quad (3.2)$$

Equations (3.1) and (3.2) are very different in form. Even if \tilde{v} is limited to a finite bandwidth B (i.e., the RF bandwidth), the bandwidth of v will in theory be infinite, since the square root function has an infinite Taylor series expansion [57]. In practice, most of the spectral power is concentrated in a finite bandwidth. Hanington, for example, proposed a minimum switching frequency of 10 MHz for a switching drain tracker if the RF bandwidth B was 1.22 MHz [58]. If the tracker can not cope with the bandwidth of its input signal the result will be reduced system efficiency, and most likely nonlinear distortion. Linear filtering of the input to the tracker can reduce the bias bandwidth, but it also introduces memory effects [11, 18, 59].

The power of the low-pass signal, however,

$$p = \tilde{v}\tilde{v}^* = v_i^2 + v_q^2 \quad (3.3)$$

will have a bandwidth of only $2B$. If the bias was taken to vary as a function of power instead, one could have a much greater control over the bandwidth. Since most functions can be represented by Taylor series, a Q th-order polynomial function of the power \tilde{p} will have a bandwidth equal to $2QB$. By choosing a first order polynomial variation of the drain with the input power, the drain bias bandwidth can be held to twice the RF bandwidth. By the same principle, a quadratic bias variation in the gate, will lead to a bandwidth of four times the RF bandwidth, which can still be manageable due to the low current flowing into the gate. These bias functions, written mathematically in (3.4), shall be employed from now on when referring to polynomial bias variation unless otherwise specified.

$$V_G(p) = g_2p^2 + g_1p + g_0, \quad (3.4)$$

$$V_D(p) = d_1p + d_0. \quad (3.5)$$

The next subsections present equations for the ideal transistor considering a linear dependence of the drain bias with the input power, and both a linear and a quadratic dependence of the gate bias with the input power.

3.3.3 The idealized transistor

There are three main quantities in this analysis: gate voltage (V_g), drain voltage (V_d), and drain current (I_d). The gate voltage is assumed to have two components

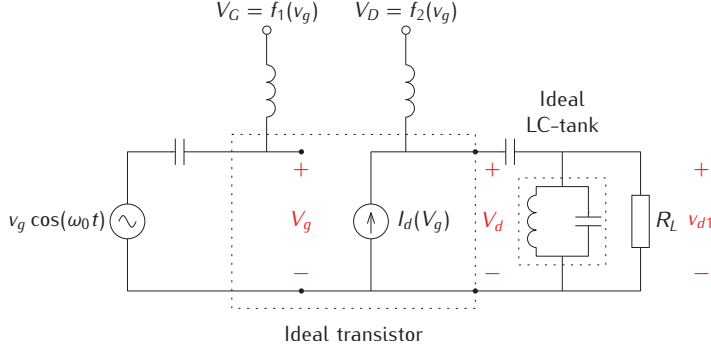


Figure 3.3: Ideal transistor model. The input is a single-tone signal with envelope amplitude v_g ; the input power is proportional to the square of the envelope $|v_g|^2$. The gate bias (V_G) and drain bias (V_D) can be functions of the amplitude v_g , or equivalently of the input power. The ideal LC-tank filter shorts all the harmonic components of the current I_d arising from the transconductance function (3.8). Therefore the voltage at the load R_L is purely sinusoidal with amplitude v_{d1} .

only: one at the fundamental frequency ω_0 with envelope amplitude v_g —the input to the PA—and the DC gate bias voltage V_G , so that

$$V_g = v_g \cos(\omega_0 t) + V_G \quad (3.6)$$

where t is time. The product $\omega_0 t$ from now on will be represented by the angle θ . Both gate and drain biases can be considered to vary as a function of the envelope, $V_G(v_g)$ and $V_D(v_g)$, or equivalently as functions of the input power p which is itself a function of the envelope ($p \propto |v_g|^2$). Figure 3.3 illustrates these variables in an idealized amplifier built upon a transistor with zero knee voltage and zero output conductance.

The transconductance is the dependence of the drain current I_d on V_g and V_d . Since I_d is less sensitive to V_d at the saturation region of operation [25], we consider the current to depend only on the gate voltage. Due to the inherent nonlinearity of the transconductance, the current can be composed of infinitely many harmonics:

$$I_d = I_{DC} + i_1 \cos \theta + i_2 \cos 2\theta + i_3 \cos 3\theta + \dots \quad (3.7)$$

For simplicity, the transconductance function will be assumed to be a hard non-linear characteristic, given by (3.8) [9].

$$I_d = \begin{cases} 0 & \text{if } V_g \leq 0 \\ \lambda V_g & \text{if } 0 < V_g \leq V_{g,\max} \\ I_{d,\max} & \text{if } V_g > V_{g,\max} \end{cases} \quad (3.8)$$

where λ is the proportionality transconductance factor. Despite the transconductance being perfectly linear in the range $0 < V_g \leq V_{g,\max}$, the drain current I_d will have infinitely many harmonic components outside that range, as in (3.7).

As shown in Figure 3.3, another important assumption is that there is an ideal LC-tank or “harmonic trap” at the output, parallel to the load. It shorts all the harmonics so that only the fundamental current component i_1 circulates through the load. Therefore, the voltage seen at the drain terminal is of the form

$$V_d = -v_d \cos \theta + V_D(v_g) \quad (3.9)$$

where $V_D(v_g)$ is the drain bias voltage that is dependent on the input signal’s amplitude, and the drain RF component is given by

$$v_d = R_L i_1 \quad (3.10)$$

where R_L is the purely resistive load presented to the amplifier. Then, the RF output power at the fundamental can be calculated as

$$P_{RF} = \frac{1}{2} R_L i_1^2 \quad (3.11)$$

Class A at full drive

We shall now consider the case of a class-A amplifier biased statically for maximum output power. Let (V_{GA}, V_{DA}) be the bias point of an ideal class-A amplifier, where V_{GA} is chosen so that

$$I_{DA} = I_{d,\max}/2 \quad (3.12)$$

and V_{DA} fulfills

$$V_{DA} = V_{d,\max}/2 \quad (3.13)$$

where $V_{d,\max}$ is the maximum drain voltage before breakdown. For a maximum input drive $v_g = V_{g,\max}/2$, V_g will swing from 0 to $V_{g,\max}$. A load resistor R_L is selected so that the total drain voltage, $V_d = -I_d R_L$, swings from 0 to $V_{d,\max}$:

$$R_{LA} = V_{d,\max}/I_{d,\max} . \quad (3.14)$$

The RF output power is then given by

$$P_{RF_{\max,A}} = \frac{1}{2} v_d i_d = \frac{1}{2} V_{DA} I_{DA} . \quad (3.15)$$

Since the DC power fed into the PA is

$$P_{DC,A} = V_{DA} I_{DA} , \quad (3.16)$$

the drain efficiency is defined as

$$\eta = P_{RF}/P_{DC} \quad (3.17)$$

which for the case of a class-A yields 1/2.

If the input envelope v_g was reduced from the maximum v_g^* by a fraction k

$$v_g = \frac{v_g^*}{k} \quad (3.18)$$

and the bias was held constant at (V_{GA}, V_{DA}) , the DC power consumption would still be $1/2V_{DA}I_{DA}$, while the output power would decrease proportionally to k^2 . The drain efficiency would therefore decrease quadratically with the back-off k :

$$\eta_A = \frac{1}{2k^2}. \quad (3.19)$$

If however the bias signals $V_G(v_g), V_D(v_g)$ varied proportionally with v_g (i.e., starting at 0 and up to V_{GA} and V_{DA} , respectively), the amplifier would operate in linear class-A mode even with an increase in the back-off k . Therefore the drain efficiency and the gain would be constant for all input envelope levels. If a constant knee voltage and a constant drain-to-source resistance were added to the model, the bias would have to change linearly, instead of proportionally, as shown by Colantonio [23]. As explained already in Section 3.3.2, this would require higher bias bandwidth than if the bias followed the input power. It will soon be shown that varying the bias with respect to power drives the amplifier into class-AB mode, even if the starting point is a class-A amplifier.

3.3.4 Reduced conduction angle

From now on we consider the gate bias V_G to be in the interval $[0, V_{g,\max}/2]$. If the input envelope increases up to a level v_g^* so large that $\max(V_g) = V_{g,\max}$, and at the same time $V_G < V_{g,\max}/2$, clipping occurs at the lower end of I_d (see (3.8)), and the transistor is said to operate in reduced conduction mode. The angle α for which the transistor operates linearly is called the conduction angle. It is defined so that

$$V_G + v_g \cos(\alpha/2) = 0 \quad (3.20)$$

and therefore

$$\alpha = 2 \cos^{-1} \left(\frac{-V_G}{v_g} \right). \quad (3.21)$$

In general, for an amplifier with a conduction angle α , the quiescent current I_D and the AC component i_d will be given by

$$I_D = \lambda V_G \quad (3.22)$$

$$i_d = \lambda v_g \quad (3.23)$$

where λ is the proportionality transconductance factor defined in (3.8). Then, the DC and fundamental components of the drain current, I_{DC} and i_1 respectively,

can be calculated using the Fourier transform:

$$\begin{aligned} I_{DC} &= \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} (I_D + i_d \cos \theta) d\theta \\ &= \frac{1}{2\pi} I_D \alpha + 2i_d \sin(\alpha/2). \end{aligned} \quad (3.24)$$

The component at the fundamental is given by:

$$\begin{aligned} i_1 &= \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} (I_D + i_d \cos \theta) \cos \theta d\theta \\ &= \frac{2}{\pi} I_D \sin(\alpha/2) + \frac{i_d}{2\pi} \alpha + \frac{i_d}{2\pi} \sin \alpha \end{aligned} \quad (3.25)$$

3.3.5 Relations for the variation of bias with input power

Assume that an output impedance has been selected for maximum output power for a class-A PA. Let the input envelope amplitude of the single-tone gate voltage (i.e., fundamental gate voltage) be reduced by a factor k , where $k > 1$, so that

$$v_g = V_{GA}/k. \quad (3.26)$$

Substituting (3.26) in (3.6) we get

$$V_G = V_G(k) + V_{GA}/k \cos(\theta). \quad (3.27)$$

The gate bias shall be varied linearly or quadratically with the input power from 0 up to the class-A bias point, V_{GA} . That is to say that $V_G(p)$ varies with the input power p , which is proportional to v_g^2 . When the back-off k tends to infinity, V_G tends to 0; and when there is no back-off (i.e., $k = 1$), $V_G = V_{GA}$. That is

$$V_G \propto p \propto \left(\frac{1}{k^2}\right)^m, \quad m = 1, \text{ or } 2. \quad (3.28)$$

Using this relation, one can show for the case of proportional ($m = 1$) and quadratic ($m = 2$) variation that

$$V_G = \frac{V_{GA}}{(k^2)^m}, \quad \text{for } m = 1, 2 \quad (3.29)$$

Since the gate bias voltage V_G varies as a function of the input power instead of the input envelope, the amplifier is biased in class-AB to -B mode for any $k > 1$, and the conduction angle α varies between π and 2π . Replacing (3.29) in (3.20) we obtain the expression for the conduction angle:

$$\cos(\alpha/2) = -1/(k)^{2m-1}, \quad \text{for } m = 1, 2. \quad (3.30)$$

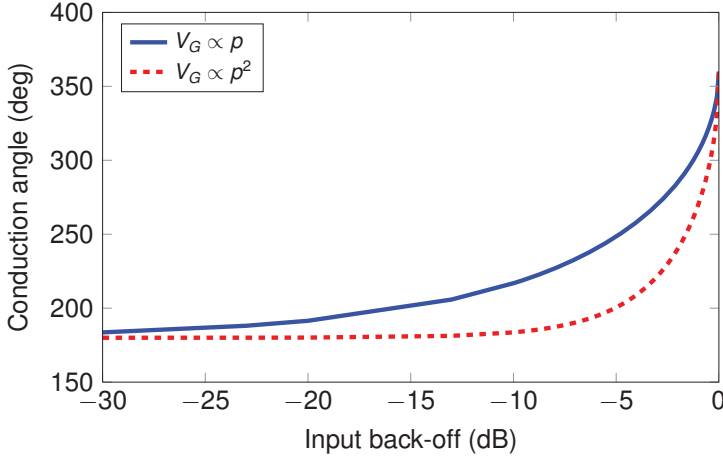


Figure 3.4: Conduction angle vs. input power back-off for the gate bias proportional to (1) input power $V_G \propto p$, (2) the square of the input power $V_G \propto p^2$.

Figure 3.4 shows the conduction angle α as a function of the input power back-off ($10 \log(1/k^2)$). In this figure and in those that follow; the drain current, gate voltage, drain voltage and load resistance are all normalized respect to their static-bias class-A counterpart [9].

Replacing (3.29) and (3.26) in (3.24), the DC drain current component can be shown to be given by:

$$I_{DC} = \frac{1}{2\pi} \frac{\alpha I_{DA}}{(k^2)^m} + \frac{1}{\pi} \frac{I_{DA}}{k} \sin(\alpha/2) \quad (3.31)$$

where α is defined in (3.30).

Replacing (3.29), (3.26), in (3.25), the drain current component at the fundamental is found to be given by:

$$i_1 = \frac{2}{\pi} \frac{I_{DA}}{(k^2)^m} \sin(\alpha/2) + \frac{I_{DA}}{2\pi k} (\alpha + \sin \alpha) \quad (3.32)$$

Figure 3.5 shows both the DC and fundamental drain current components. Since the RF output power can be calculated from (3.11), it only remains to calculate the drain efficiency in order to calculate the DC power, which depends on the drain bias.

The drain bias voltage function is a straight-line, and for both cases the function was fitted empirically using numerical simulation based on the equations presented so far. For the case of a proportional variation of gate bias with input power (i.e., $m = 1$), the load resistance R_L was chosen to be the same than that of the class-A

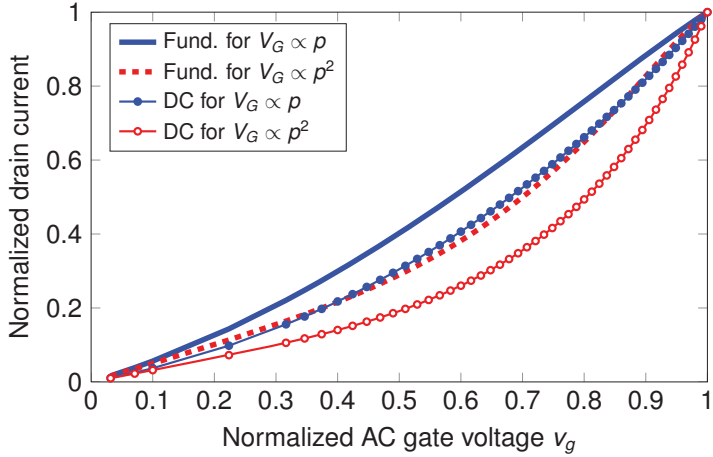


Figure 3.5: Normalized fundamental and DC components of the drain current vs. normalized AC gate voltage (v_g) when the gate bias is proportional to (1) the input power $V_G \propto p$ (2) the square of the input power ($V_G \propto p^2$). A maximum AC gate voltage of $v_g = 1$ with a gate bias voltage of $V_G = 1$ produce a maximum drain current swing from 0 to 2 in scalar current units (a drain current of 1 corresponds to half of the saturation drain current for the transistor).

amplifier. That is,

$$R_L = R_{LA} \quad (3.33)$$

$$= V_{d,\max}/V_{d,\max}. \quad (3.34)$$

Since we assume perfect short terminations for all harmonic frequencies at the load, only the fundamental current component i_1 circulates through R_L . Therefore the straight line $V_D(k^2)$ is chosen so that:

1. The distance between V_D and v_d is minimal (maximizes efficiency).
2. $V_D \geq |v_d|$ for all k (avoids clipping of the drain voltage V_d at the lower end).
3. When there is no back-off, $V_D(k^2 = 1) = V_{DA}$.

For the case of varying V_G quadratically with input power, $V_D(p)$ can be traced as a straight line very near to v_d satisfying conditions 1 and 2 if only $V_D(k^2 = 1) = 1.02V_{DA}$. The load resistance was therefore reduced by a factor of 1.02, so that condition 3 was satisfied. This implies a reduction in RF output power of $10 \log(1.02)$, but allows V_D to follow v_d much closer, which results in higher efficiency. The RF output power at the fundamental and the drain efficiency can be

calculated using (3.11) and (3.17), respectively, keeping in mind that

$$R_L = \begin{cases} R_{LA} & \text{for } m = 1 \\ R_{LA}/1.02 & \text{for } m = 2. \end{cases} \quad (3.35)$$

Figure 3.6 shows both V_D and v_d as a function of the normalized input power. Notice how the straight line function of V_D for the quadratic case follows v_d much closer. The improvement in efficiency that this brings is reflected in Figure 3.7, though both cases perform far better than a class-A with static bias in this regard. Figure 3.8 illustrates how the improvements in efficiency come at the expense of output power. As Figure 3.9 shows, both amplifiers vary 6 dB in their gain, because of the transition from class-A to class-B with increasing back-off.

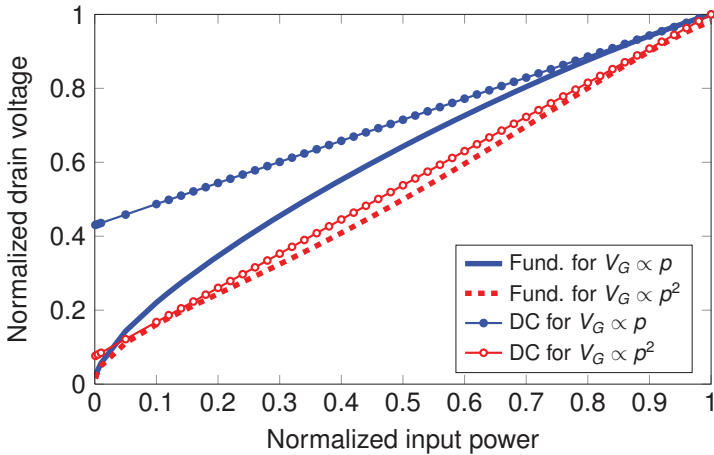


Figure 3.6: Fundamental and DC components of the normalized drain voltage vs. the normalized input power p when the gate bias is proportional to (1) the input power ($V_G \propto p$) (2) the square of the input power ($V_G \propto p^2$). The maximum input power $p = 1$ produces a maximum drain current swing from 0 to 2 and a maximum drain voltage swing from 0 to 2 when the transistor is biased as a class-A for maximum output power (a drain voltage of 1 corresponds to half of the transistor's maximum drain voltage before breakdown). The DC drain voltage is greater than the fundamental drain voltage along the whole input power range to avoid clipping of the drain voltage waveform.

To emphasize on the substantial efficiency improvements obtained by varying the bias with power, two modulated signals, a 16-QAM and a 128-QAM with 0.22 roll-off factor, were applied to the two dynamic biasing cases. The probability density function of the 16-QAM signal is shown in Figure 3.10. The PAPR of the 16-QAM signal is 6.5 dB, but is susceptible to variations depending on the order of

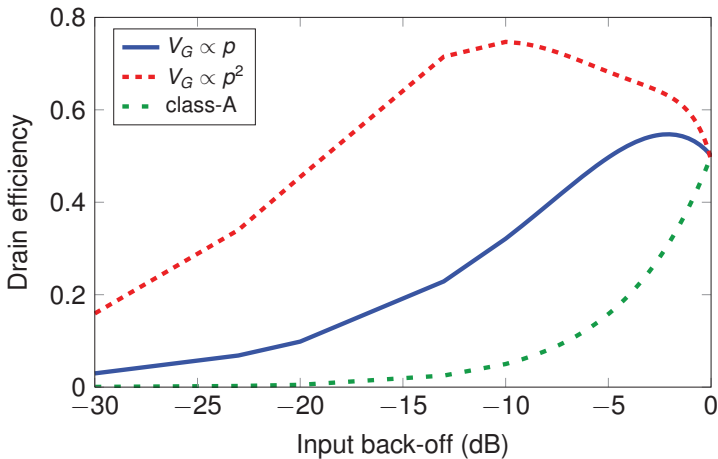


Figure 3.7: Drain efficiency comparing class-A static biasing with linear and quadratic variation of the gate bias with input power vs. input power back-off.

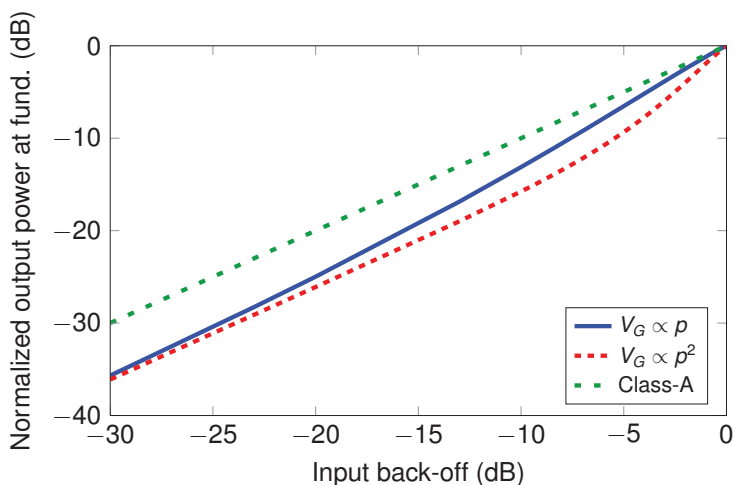


Figure 3.8: Normalized output power at the fundamental vs. input back-off for (1) gate bias proportional to the input power, (2) gate bias proportional to the square of the input power, (3) fixed class-A bias for maximum output power. The output power of cases (1) and (2) is relative to that of case (3) at 0-dB input back-off.

the RRC filter and the number of symbols used in the simulation. Table 3.1 shows the average drain efficiencies and average gains compared to class A operation. Varying the gate bias proportionally to p can yield almost 4 times as much drain

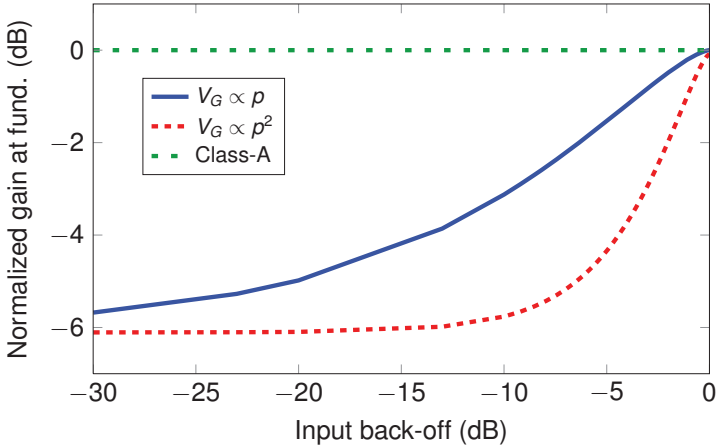


Figure 3.9: Normalized gain at the fundamental vs. input back-off for (1) gate bias proportional to the input power, (2) gate bias proportional to the square of the input power, (3) fixed class-A bias for maximum output power. The gain of cases (1) and (2) is relative to that of case (3) at 0-dB input back-off.

efficiency as the class-A case, while varying it proportionally to p^2 can yield six times as much drain efficiency as a class-A. The efficiency improvements come at the cost of some decibels in gain. In fact, the reduced gain for when the the gate bias is proportional to p^2 is expected from Figure 3.9.

Finally, Figure 3.11 shows how the DC drain current varies respect to the drain bias voltage V_D . One could imagine Figure 3.11 overlapped over an I–V plane (i.e., the current–voltage characteristic curves of the transistor), showing how the DC components of the drain current and drain voltage actually look like respect to each other.

Table 3.1: Comparison of the average drain efficiency and average gain of the dynamically biased transistor to class-A biasing for two different modulated signals: 16-QAM and 128-QAM. (The average gain is relative to class-A gain.)

Case	PAE (%)		Gain (dB)	
	16-QAM	128-QAM	16-QAM	128-QAM
$V_D \propto p, V_G \propto p$	40.5	39.7	-2.1	-2.2
$V_D \propto p, V_G \propto p^2$	67.8	67.4	-4.6	-4.6
Class-A	12.3	11.8	0	0

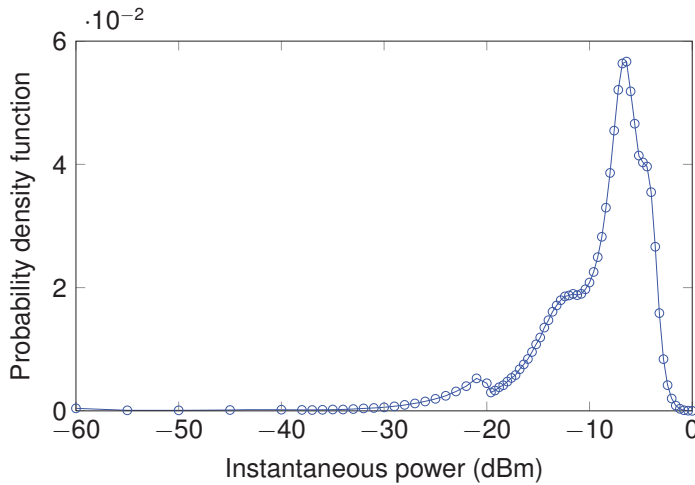


Figure 3.10: Probability density function of a typical 16-QAM signal. The roll-off factor of the RRC filter is 0.22, with a filter delay of 20 symbols, and an oversampling factor of 8. More than 10000 symbols were simulated.

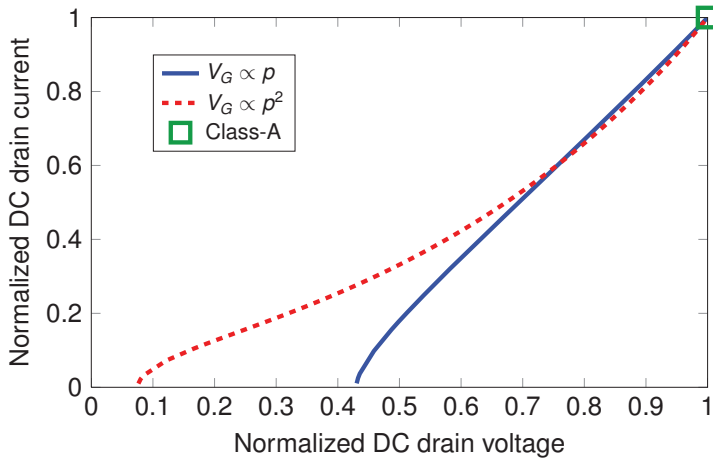


Figure 3.11: Normalized DC component of the drain current vs. normalized drain bias voltage V_D for (1) gate bias proportional to the input power, (2) gate bias proportional to the square of the input power, (3) fixed class-A bias for maximum output power. Both the DC drain current and the drain bias voltage in cases (1) and (2) are normalized respect to those of case (3).

3.3.6 Clip the envelope, or clip the bias?

This section discusses how varying the drain bias with input power may lead to clipping of the RF drain waveform, and how clipping the drain bias waveform instead, can lead to high efficiency without causing nonlinear distortion. A class-B amplifier with different drain biasing functions is used as an example, in order to isolate the effect of drain bias variation from that of gate bias variation.

Clipping of the RF envelope and nonlinear distortion

In dynamic biasing, it is the variation of the drain bias that brings the largest efficiency improvement. The closer the drain bias (V_D) is to the RF envelope at the drain (v_d), the higher the efficiency.

For this reason a low drain bias voltage at zero input envelope ($v_g = 0$) is desirable—to optimize efficiency at large input power back-off—. On the other hand if $V_D < v_d$ for any input amplitude v_g , the drain RF waveform will be clipped, which will lower the power at the fundamental, and increase distortion power at the harmonics.

Current variation in a class-B amplifier

Consider a class-B amplifier with static gate bias (i.e., $V_G = 0$ and thus $I_D = 0$ for all values of v_g). Then, from (3.21), we have that $\alpha = \pi$, which substituted into (3.25) together with (3.22) and (3.23) yields

$$i_1 = \left[\frac{\lambda}{2} \right] v_g. \quad (3.36)$$

Equation (3.36) states that the RF current at the fundamental, i_1 , is proportional to the input amplitude (or envelope) v_g . The load resistor, R_L , is the proportionality factor between the amplitude of the drain RF voltage, v_d , and the fundamental current component, i_1 (see (3.10)). Consequently, the RF amplitude at the drain is proportional to the input amplitude, $v_d \propto v_g$, for a class-B amplifier.

Adding dynamic drain biasing to the class-B PA

The case of having the drain bias varying proportionally to the input envelope is illustrated in Figure 3.12, curve “---”. Since $V_D = v_d$ along the whole v_g -range, no clipping occurs. Figure 3.12 shows three other cases where the bias varies with input power instead (—, —, and —). For the first one, —, the drain bias starts so low that clipping will clearly occur for $v_g < 0.18$. The next case, —, remedies the clipping problem by starting the bias at a higher value ($V_D(v_g = 0) = 0.22$), but the downside is the wide V_D - v_d gap along the input envelope range that diminishes average efficiency.

The last case (—), presents an interesting alternative with the the bias waveform clipped intentionally at its higher end; the bias follows the envelope closer along the whole envelope range without clipping the RF drain waveform. The clipped drain bias waveform actually comes closest to the straight envelope line (---) near the middle of the envelope amplitude range. The input envelope voltage at which the bias is clipped, as well as the starting bias point (the bias $V_{D,\min}$ when the input envelope v_g is zero) may be tuned to maximize efficiency at the average input envelope for a modulated signal, thus enhancing average PA efficiency.

This shows that upper-clipping the drain bias when it varies with power may improve both linearity and efficiency (compared to — and —).

Generating “clipped bias”

There are two options:

1. To include a hard clipping function after the polynomial function at the digital end, where the normalized bias waveforms are generated.
2. To regulate the bias of the drain tracker so that it saturates at the drain bias threshold from which we wish clipping to occur.

In this work the first option is used, as it does not represent any extra complexity at the digital side, and can be directly controlled from the computer without touching the hardware.

Implications on bias bandwidth

As soon as the drain bias waveform is clipped, its bandwidth becomes infinite in theory. The amount of power at harmonic frequencies depends on how frequently the clipping effect happens, and how much of the V_D waveform is clipped. Since the initial purpose was especially to constrain the drain bias bandwidth to twice the RF bandwidth, one might wonder what is the point of biasing following power.

Unlike most ET systems, in applications that use class-A/AB PAs for high linearity, the amplifier is not driven near saturation at every point of the bias vs. input power curve. Even if some of the harmonics of a perfectly clipped signal are filtered away at the tracker’s output, the bias V_D will not clip the RF drain voltage v_d as long as $V_D > v_d$.

The potential distortion introduced by clipping the bias increases as the drain clipping level decreases (i.e., lower clipping threshold, more nonlinear distortion). It is also possible that the tracker’s bandwidth limitations produce a large delay at the output when the input power is near the peak, in which case memory effects are introduced. However, for the drain tracker at hand, rounded “bias corners” were observed instead of hard clipping, but the tracker followed the instantaneous input power waveform in time. It is therefore that ACPR3 levels below -50 dB could be achieved for the GaN transistor using bias clipping (Section 5.4.2).

Summary: clipping the drain bias

If the bias tracks the input power starting from a very low bias value, compression can be generated even at low and medium input power levels. Clipping the drain bias can help achieve higher average efficiency without generating nonlinear distortion from clipping the envelope of the RF signal at the drain. The clipping effect can be implemented digitally as a hard clipping function after the polynomial function for the bias. If the PA is not driven hard into saturation along the power range, and if the clipping does not start from a very low bias level, it does not matter if the tracker rounds off the edges of the hard-clipped bias function, as long as it has enough bandwidth to follow the input power signal without a significant delay, and as long as there is an adequate margin between the drain bias and the drain RF envelope (so that saturation from limited drain biasing is avoided along the power range). A demonstration of the usefulness of the technique is given in Chapter 5 for the GaAs and GaN transistors, where high improvements in linearity compared to static bias and other dynamic biasing cases are achieved using bias clipping mainly at the drain.

3.3.7 Summary and discussion

The effects of varying the drain and gate bias as a function of the input power, as compared to varying them as a function of the input envelope have been studied using an ideal transistor model. This case illustrated how the selection of the bias function can result in a trade-off between efficiency and output power, and showed that the resistive load can be adjusted to the biasing functions to obtain the desired voltage swing for maximum output power. Much higher efficiencies were obtained at back-off compared to a static-bias ideal class-A amplifier, specially for the quadratic input power bias variation. Nevertheless, the 6-dB gain ripple is a consequence of the bias-transition from class-A to class-AB with power back-off, arising from the choice of varying the gate bias from the threshold voltage (0 V) up to the class-A value ($V_{g,max}/2$).

In this analysis the transistor is considered as a linear voltage-controlled current source, provided that the gate voltage is within a range (greater than zero, less than the saturation voltage). In practice, however, the transconductance is a nonlinear function dependent on the bias point; and the transistor's internal capacitances and resistances are also bias-dependent to a certain extent. The bias variation will affect the temperature of the device, which will also have an impact on its output capabilities, and might introduce memory effects.

An issue of concern might be the apparently inescapable 6-dB gain ripple introduced by varying the bias with input power. Fortunately, some of the non-ideal characteristics mentioned before can actually have a positive influence in the reduction of gain variation [9]:

- *A nonlinear transconductance*: If the transconductance function has a cubic

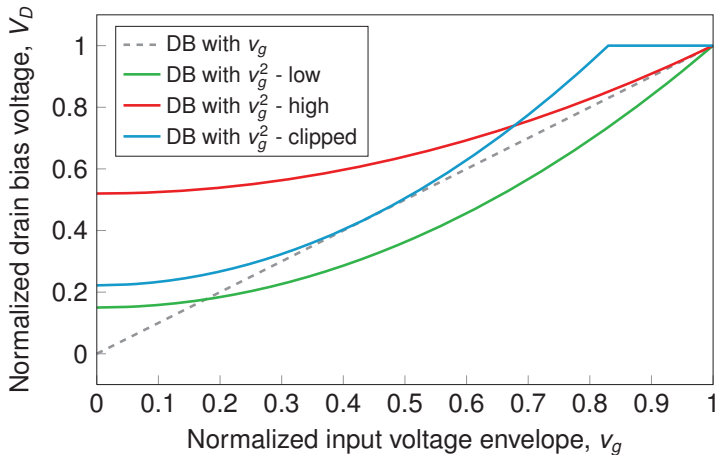


Figure 3.12: Four cases of dynamic drain biasing for an ideal class-B amplifier with fixed gate bias. For an input envelope amplitude v_g , and an input power (proportional to the square of the input envelope, $p \propto v_g^2$), the drain bias V_D is varied (1) proportionally to the input envelope (---), (2) linearly with input power for a low minimum drain bias (—), (3) linearly with input power for a high minimum drain bias (—), (4) linearly with input power, and with hard clipping (—). Case (1) is the reference. Case (2) generates nonlinear power from clipping the RF drain signal because V_D is smaller than the amplitude of the drain RF signal. Case (3) corrects the failure, but due to the high starting bias the average efficiency is diminished. Case (4) allows higher average efficiency without clipping the RF envelope at the drain.

form instead of a linear one between threshold and saturation voltages, the class-A response can suffer from premature gain compression. For fixed bias, in the midrange class AB region, a bias condition can be found that has a more linear characteristic over a wider dynamic range than even a class A mode. The same applies to dynamic biasing. Linearity over a specified dynamic range of input signal can be optimized by carefully choosing the operating mode and the RF load resistor.

- *The dependence of transconductance on bias:* Since for many device technologies the transconductance depends on the bias point, a higher transconductance at lower input power levels can compensate for the gain difference.
- *Harnessing the right harmonic components:* nonlinearities of the right kind on the input might be harnessed to reduce the heavy drive requirements of sinusoidal signals. The I–V characteristic of the BJTs input diode junction does that to some extent, and the reduction in class B power gain may be

as little as 2 dB. With FETs this could be done by adding some second harmonic from the output to the input drive signal.

It must also be considered that the results presented in this section consider the gate bias to vary all the way from the threshold voltage up to class-A level. Reducing the gate bias variation range will in turn reduce the conduction angle variation, and thus the gain ripple.

These considerations imply that the selection of an appropriate load, and of the biasing functions are dependent on the device, and of course on the application. The impossibility of solving the problem with a purely mathematically deterministic approach motivated the design methods that are presented later in this work.

Experimental results presented later in Chapter 5 will show that power added efficiencies twice or three times that of a statically biased PA can be obtained with dynamic biasing, with comparable linearity levels. For some average output power levels, linearity might even be better with dynamic biasing, while still yielding significant benefits in efficiency.

3.4 Designing a MMIC pHEMT power amplifier

The usual procedure for designing a class-A/AB amplifier is: given a transistor technology, choose a transistor size, and view its I–V characteristics to select a suitable bias point and class depending on the application. After the bias point is chosen the transistor is stabilized by adding lossy components or negative feedback, and then one can choose the input and output impedances for the transistor and design the matching network. This was precisely what was done with the pHEMT transistor, in a first attempt to build an amplifier driven by dynamic bias. The goal was to design an amplifier in enhancement pHEMT MMIC technology provided by Triquint with a peak output power of 30 dBm, operating at a frequency of 6 GHz, with a 20 MHz bandwidth, and a minimum gain of 10 dB. The characteristics for the pHEMT transistor are shown in Table 3.2.

The transistor was designed to operate at the bias point

$$(V_G, I_D, V_D) = (0.75 \text{ V}, 0.32 \text{ A}, 8 \text{ V}) \quad (3.37)$$

Table 3.2: Current and voltage specifications of the pHEMT transistor, as provided by the manufacturer [3].

Description	Parameter	Value	Unit
Maximum channel current per gate unit length	I_{\max}	320	mA/mm
Breakdown D-G voltage	BV_{dg}	15 min, 18typ	V

as a maximum gain amplifier. The maximum current of the transistor is given by

$$I_{\text{ch,max}} = n_{\text{fingers}} w_{\text{finger}} I_{\text{max}} \quad (3.38)$$

where n_{fingers} and w_{finger} are the number of fingers and the width of each finger, respectively. By choosing a width of 240 μm with 9 fingers we obtain a maximum current of 691.2 mA, which considering a knee voltage V_{knee} of 2 V and a maximum drain voltage V_{max} of 18 V yields a maximum output power of

$$P_{\text{max}} = \frac{1}{8}(V_{\text{max}} - V_{\text{knee}})I_{\text{max}} = 31.4 \text{ dBm} \quad (3.39)$$

The schematic of the pHEMT amplifier is included in Appendix D. There are two inductors with a shunt capacitor in between at the drain that work together as an RF-choke. They provide high impedance to the RF signal but at the same time ensure that the resonance frequency is at least two or three times the operating frequency. The resistor-capacitor (RC) network ensures unconditional small-signal stability at all frequencies for the selected bias point, though the loss of the shunt inductors at the input also contributes significantly to stability. The output matching network was deliberately chosen to be low-pass to filter away the harmonic components.

Graphical approaches are widely used in the envelope tracking literature in order to find suitable bias paths for the drain voltage as a function of the input and output power (an extension of such an approach to include the gate bias was presented by the author, together with Caharija et al. [60]). Nevertheless, plotting constant-S₂₁ (small-signal gain) contours in the I–V plane can give us a practical “first glance” at the variation of gain with bias (Figure 3.13). From Figure 3.13, we note that the S₂₁ contours follow closely the constant-gate-bias lines (—). This implies that varying the drain dynamically will maintain the small-signal gain constant along the bias path as long as the gate is fixed. The red continuous line in Figure 3.13 shows a bias path where both gate and drain vary proportionally with the input power, and in that case since 5 contours are traversed, there would be a 2.5-dB small-signal gain-drop along the bias path. Being able to vary the gate bias is important for further efficiency enhancement, but if there is a large gain drop along the bias path, efficiency would come at the expense of high nonlinear distortion.

In order to shift the S₂₁-contours diagonally upwards, one can design the matching for a lower bias point as shown in Figure 3.14. The new design bias point was chosen to be $(V_G, V_D) = (0.65 \text{ V}, 4 \text{ V})$. The principle is that the transconductance is an increasing function of the transistor’s current. As the gate bias increases the gain increases as well. The gain at the new lower design bias point \otimes will be lower, but as one traverses the diagonal bias path (red thick line) the impedance mismatch will increase in turn, which should compensate the natural tendency of the transistor to have a higher gain in this region. Figure 3.14 shows the S₂₁-contours bending diagonally upwards, following closer the biasing path so the S₂₁-variation is only 1.5 dB along the path.

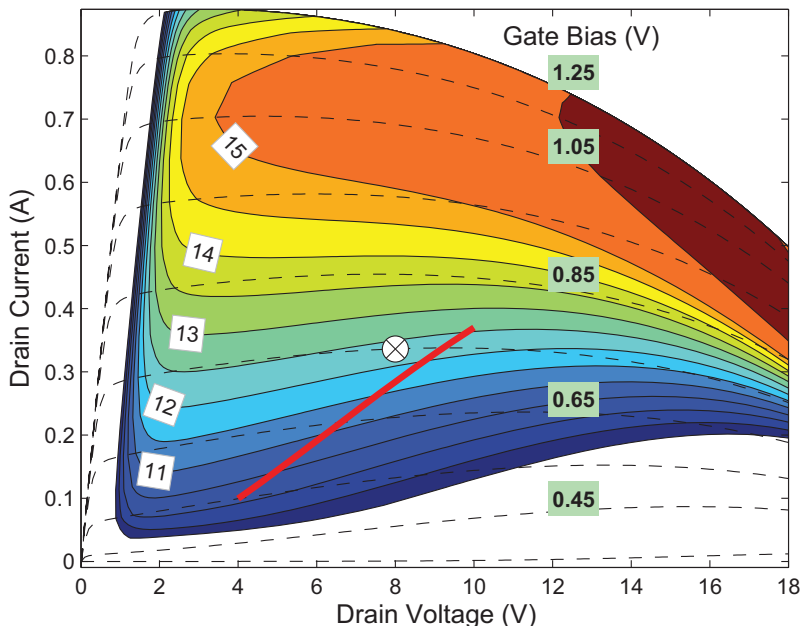


Figure 3.13: Small-signal gain contours in the I–V plane for an amplifier designed at bias point \otimes : $(V_G, V_D) = (0.75 \text{ V}, 8 \text{ V})$. Since the S21-contours are almost parallel to the constant gate bias lines (–), there is a large (2.5-dB) gain variation for a typical biasing path with gate and drain biases varying proportionally to the input power (red thick line).

3.5 Characterizing an amplifier to use it with dynamic bias

The initial characterization of the PA is based on *quasi-static modeling*. For a single-tone input signal, the input power is swept at different bias points, and for each input power value output parameters are recorded (e.g., output power, phase-shift, PAE). Such a procedure is not uncommon within envelope tracking practitioners [19, 61, 62]. It provides a simple framework to select suitable biasing functions based on gain and phase responses (among other output parameters), and reduces computational time and complexity with respect to full envelope simulation.

Yet there are a number of effects that the model does not consider; the first one to be addressed shall be temperature. Thermal resistance in small devices, such as the MMIC HBT transistor deployed in Section 4.5.2, can generate thermal effects in bandwidths as large as 0.1 MHz, or 1 MHz. If the modulated signal had

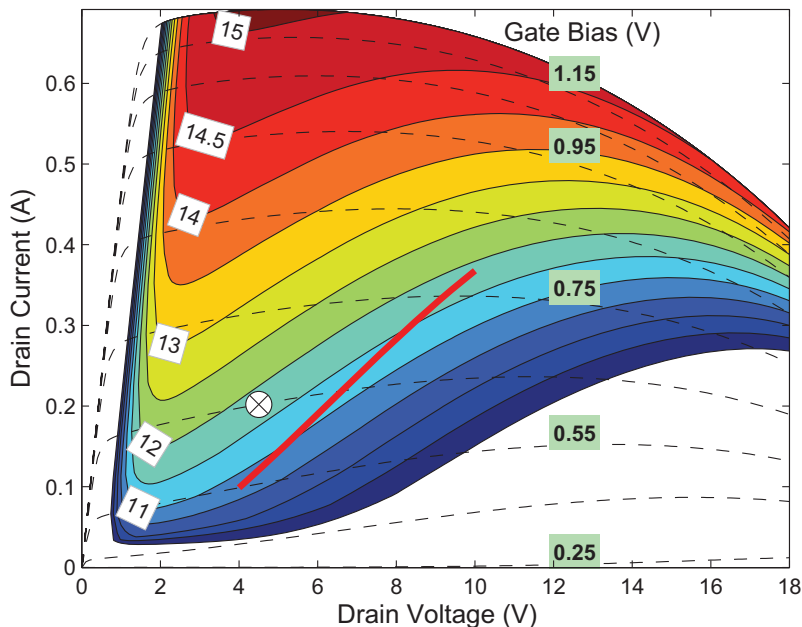


Figure 3.14: Small-signal gain (S_{21}) contours in the I - V plane for an amplifier designed at bias point \otimes : $(V_G, V_D) = (0.65 \text{ V}, 4.5 \text{ V})$. For a typical biasing path with gate and drain biases varying proportionally to the input power (red thick line) there is only 1.5-dB gain variation because the S_{21} -contours are shifted diagonally upwards.

a 1-MHz bandwidth, the temperature of the transistor would be moved up and down by dynamic biasing, close to the behavior predicted by quasi-static modeling. Large devices, for example a 100-W GaN PA, will exhibit a longer thermal time constant and therefore may be more adequately characterized by using quasi-static modeling together with pulsed measurements of the RF and gate/drain biases [63]. This is because high temperatures at the amplifier will reduce its output power capacity. It would hence be incorrect to assume reduced output power (extracted from static biasing single-tone measurements) if the bias will be “moved” dynamically to a high region so fast that the transistor’s channel temperature will not follow. In consequence, the bandwidth of the modulated signal compared to that of the thermal effects, as well as the probability distribution function of the signal must be taken into account. Other effects not considered by quasi-static modeling are narrow bandwidth bias circuit effects, narrow bandwidth RF input and output matching effects, finite bandwidth at the tracker and tracker-PA time misalign-

ment [61].

The purpose of quasi-static modeling is to choose biasing functions that yield the desired linearity and efficiency trade-offs taking into account the probability density function of the modulated signal intended for the amplifier. Accuracy must be sufficient to choose “the optimum bias function” and discard the others, but is not expected to be so high as to match results that one would obtain by running the amplifier with dynamic biasing and a modulated signal. Once suitable gate and drain bias functions are found, a simulation using a more complex model that considers memory and temperature effects shall be run. Another advantage with the method is that the same algorithms used to select biasing paths from quasi-static data can be applied directly to find biasing paths from measurements with a modulated signal, as shown later in Chapter 5.

Using single-tone measurements to extract the model, three independent variables are swept: the input power p , the gate voltage V_G , and the drain voltage V_D , with the sweeping ranges being $[p_{\min}, p_{\max}]$, $[V_{G,\min}, V_{G,\max}]$, and $[V_{D,\min}, V_{D,\max}]$, respectively. A set of output variables is recorded: output power, phase shift and dissipated power. The impedance at the load is $50\ \Omega$. Table 3.3 shows the values used for the sweep of the input variables.

Table 3.3: Values for the 1-tone sweep of the input variables.

Variable	Unit	Symbol	Minimum	Maximum	Step
Input power	dBm	p	-30	24	0.5 (min)
Gate voltage	V	V_G	0.53	0.81	0.02
Drain voltage	V	V_D	1.5	8.5	0.5

3.6 A point-search algorithm to find a biasing path

The goal of the point-search algorithm is to find a discrete sequence of bias points related to input or output power, such that the amplifier is operating efficiently and linearly along the sequence [64]. This sequence can be thought of as a look-up table (LUT) in digital predistortion. Continuous biasing functions can be later extracted from it.

Since the input power, and gate and drain voltages were varied in steps as explained in Section 3.5, what we have are Q different combinations of points $\mathbf{P}_k : (V_G(k), V_D(k), p(k))$, where $k = 1, \dots, Q$. The algorithm is explained in simple terms in Algorithm 3.1.

Algorithm 3.1: Description of the point-search algorithm.

- 1 Sort the Q points according to their output power level.
 - 2 Divide them into N groups in steps of Δp_o according to their output power so that the first group includes points with p_o from $p_{o,\min}$ to $p_{o,\min} + \Delta p_o$, and the last one from $p_{o,\min} + (N - 1)\Delta p_o$ to $p_{o,\min} + N\Delta p_o$. Each group has Q_n points.
 - 3 Find a starting point \mathbf{P}_1 from the Q_1 points in the first group applying the starting-point-constraints.
 - 4 **for** $n \leftarrow 2$ **to** N **do**
 - 5 Discard points with bias or input power smaller than that of the last point in the path: \mathbf{P}_{n-1} .
 - 6 Calculate the cost J for each of the points that are left.
 - 7 Choose \mathbf{P}_n to be the one with lower cost.
 - 8 **end**
-

3.6.1 Input, output and parameters of the algorithm

The inputs for the point-search algorithm are 4-dimensional matrices for output power p_o , phase-shift $\Delta\phi$, power-added efficiency (η), second harmonic component in dBc (h_2), and third harmonic component in dBc (h_3). All matrices are generated from the single-tone simulations/measurements described in Section 3.5. The output of the algorithm is a sequence of N elements of the form $\mathbf{P}_k : (V_G(k), V_D(k), p(k))$. The following parameters are required:

- Output power range in dB (in this case 20 dB)
- Cost function weights: $(w_\alpha, w_\beta, w_\gamma, w_\delta, w_\epsilon, w_\zeta)$.
- Distance-normalization coefficients to calculate the distance from one point to the next one in the output sequence $(V_{G,\text{norm}}, V_{D,\text{norm}}, p_{\text{norm}})$.
- Class-A or -AB reference bias point to compare the performance of the dynamic bias path with.
- Minimum acceptable gain value to select the starting point, G_{\min} .
- Maximum acceptable phase-shift to select the starting point, $\Delta\phi_{\max}$.
- Maximum acceptable second and third harmonic levels to select the starting point, $h_{2,\max}$ and $h_{3,\max}$, respectively.
- Output power interval in dB, Δp_o . It is used to divide the Q sorted points into groups of different output power levels.

3.6.2 Starting point selection

The first point, \mathbf{P}_1 , is chosen among the Q_1 points in the first group using the following method:

1. Use the bounds in Table 3.3 to limit the range of the starting point.
2. Discard points with transducer gain lower than G_{\min} . This limit should be close to the minimum gain the amplifier exhibits in its linear region.
3. Discard points with phase-shift greater than $\Delta\phi_{\max}$.
4. Discard points with second and third harmonic levels greater than $h_{2,\max}$ and $h_{3,\max}$, respectively.
5. From the points left, choose the one with highest PAE.

3.6.3 Calculating the cost

As explained in Algorithm 3.1, the cost J is used to determine the next point in the sequence \mathbf{P}_k . The cost J is computed as a linear combination of cost coefficients:

$$J = w_\alpha\alpha_{\text{norm}} + w_\beta\beta_{\text{norm}} + w_\gamma\gamma_{\text{norm}} + w_\delta\delta_{\text{norm}} + w_\epsilon\epsilon_{\text{norm}} + w_\zeta\zeta_{\text{norm}} \quad (3.40)$$

where the weights are normalized so that

$$w_\alpha + w_\beta + w_\gamma + w_\delta + w_\epsilon + w_{\text{dist}} = 1. \quad (3.41)$$

The cost coefficients are defined in equations (3.42) to (3.47). Variable α corresponds to the average PAE coefficient in percent, β to the gain-flatness index in decibels, γ to the phase-shift-flatness index in degrees, δ to the average power at the second harmonic in decibels, ϵ to the average power at the third harmonic in decibels, and ζ to the normalized distance between the current point and the previous one. The expression $[i]$ indicates a discrete sequence with index i .

$$\alpha = -\frac{1}{n} \sum_{i=1}^n \eta[i] \quad (3.42)$$

$$\beta = \sum_{i=2}^n |G[i] - G[i-1]| \quad (3.43)$$

$$\gamma = \sum_{i=2}^n |\phi[i] - \phi[i-1]| \quad (3.44)$$

$$\delta = \frac{1}{n} \sum_{i=1}^n h_2[i] \quad (3.45)$$

$$\epsilon = \frac{1}{n} \sum_{i=1}^n h_3[i] \quad (3.46)$$

$$\varsigma^2 = \left(\frac{V_G[n] - V_G[n-1]}{V_{G,\text{norm}}} \right)^2 + \left(\frac{V_D[n] - V_D[n-1]}{V_{D,\text{norm}}} \right)^2 + \left(\frac{p[n] - p[n-1]}{p_{\text{norm}}} \right)^2 \quad (3.47)$$

The weight w_α corresponds to PAE, w_β to gain-flatness, w_γ to phase-shift, w_δ to the average second harmonic level, w_ϵ to the average third harmonic level and w_ς to the distance between bias points. Since the output sequence yielded by the algorithm strongly depends on the set of weights and normalization distances, some suggested initial coefficients are presented in Table 3.4.

Table 3.4: Proposed initial coefficients for the point-search algorithm.

Coefficient	Proposed initial value
$w_\alpha, w_\beta, w_\gamma, w_\delta, w_\epsilon, w_\varsigma$	1/6
$V_{G,\text{norm}}$	$V_{G,\text{max}}$ from HB sweep
$V_{D,\text{norm}}$	$V_{D,\text{max}}$ from HB sweep
p_{norm}	p_{max} from HB sweep

3.6.4 Results

The results presented in this section correspond to five different runs of the algorithm with 5 different weight-combinations representing extreme cases, plus the static bias case, as described in Table 3.5.

Table 3.5: Cases and weight combinations for which the point-search algorithm was tested.

Case	Description
Maximum PAE	$w_\alpha = 1$, all other weights equal zero.
Minimum gain variation	$w_\beta = 1$, all other weights equal zero.
Minimum phase-shift variation	$w_\gamma = 1$, all other weights equal zero.
Minimum third harmonic	$w_\epsilon = 1$, all other weights equal zero.
“Tuned”	all weights equal 1/6.
Class-A	fixed bias point $(V_G, V_D) = (0.71 \text{ V}, 9 \text{ V})$.

The results for gain, PAE, phase-shift and third harmonic level are shown in figures 3.15 to 3.18, respectively. The maximum-PAE path has the highest efficiency of all, but has also a very high third harmonic, rapidly varying phase and a gain drop from 11 dB to 6 dB, which makes it useless for practical purposes. Even if the gain was linearized, the power loss could only be compensated for by a

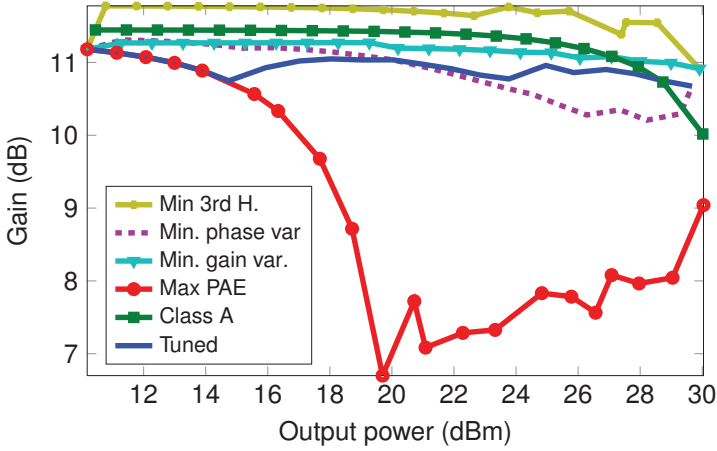


Figure 3.15: Gain vs. output power for the 6 different cases in Table 3.5.

boosting amplifier. The “tuned” path still provides a significant PAE improvement with respect to the class-A PA and has lower third harmonic compared to the maximum PAE path. It is relatively flat in gain and phase-shift: in Figure 3.15 the gain is steady between 10.5 and 11 dB, and the phase varies between 84° and 86° only, as shown in Figure 3.17. The path for flat phase has similar characteristics. Alternatively, the path for gain flatness has a phase-shift close to that of the class-A PA up to 27 dBm of output power. After that threshold, the phase-shift increases steeply in class A operation, while the best gain flatness path holds the gain and phase constant with a lower third harmonic level than the class A mode. In this case DB acts more as a linearization mechanism than as an efficiency enhancement method.

Figure 3.19 shows the trajectories of the paths in the I–V plane. Each marker accounts for a 1dB increase of output power, giving a sense of how fast the bias changes with output power. Note that while several paths tend to have an abrupt current increase at high output power values, the “tuned” path continues to show a moderate increase both in drain current and drain voltage. Finally, Figure 3.20 shows the gate and drain biases as a function of the output power for the “tuned” path. It suggests that the $V_G(p_o)$ and $V_D(p_o)$ functions could be conveniently approximated by low-order polynomials.

3.6.5 Summary

The point-search algorithm is a useful tool to find a biasing path for an unknown transistor. Some limitations would be the large number of input parameters it requires, and that it returns a discrete sequence relating the bias to the input or output power. In practice, however, these relations are continuous. When

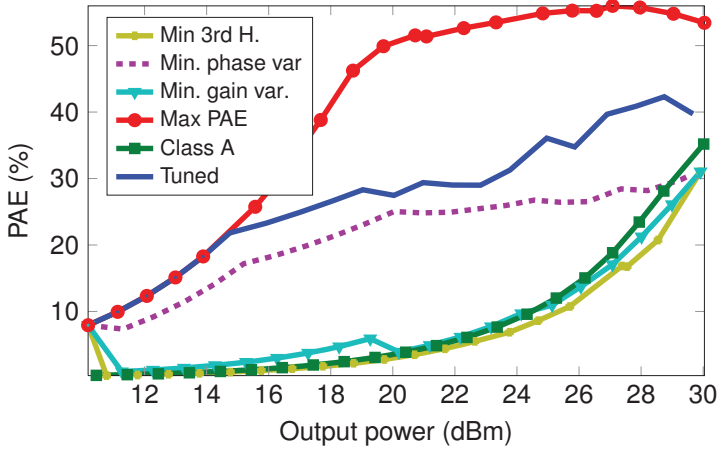


Figure 3.16: PAE vs. output power for the 6 different cases in Table 3.5.

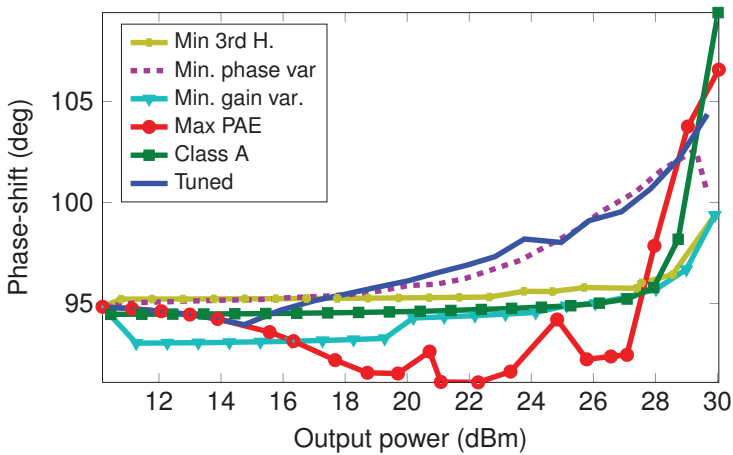


Figure 3.17: Phase-shift vs. output power for the 6 different cases in Table 3.5.

providing the algorithm with reasonable values, it returned a path that would yield much higher efficiency for a wide range of output power, compared to class A operation, while maintaining the gain and phase variations at low levels. The “tuned path” will be used in the next section, and its performance compared to other continuous paths for a modulated input signal.

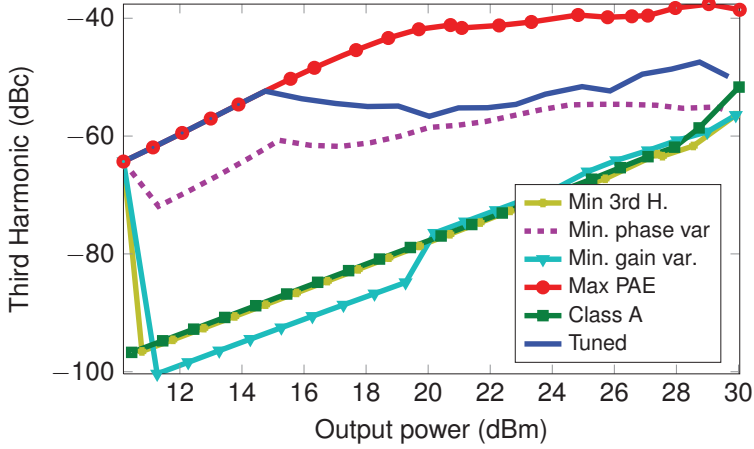


Figure 3.18: Third harmonic vs. output power for the 6 different cases in Table 3.5. The low 3rd harmonic power values are due to a low-pass filter matching network at the output of the pHEMT amplifier—if a two-tone signal was the input to the PA and the third-order intermodulation (IM3) was measured, an increase in the range of 10 dB to 20 dB would be expected.

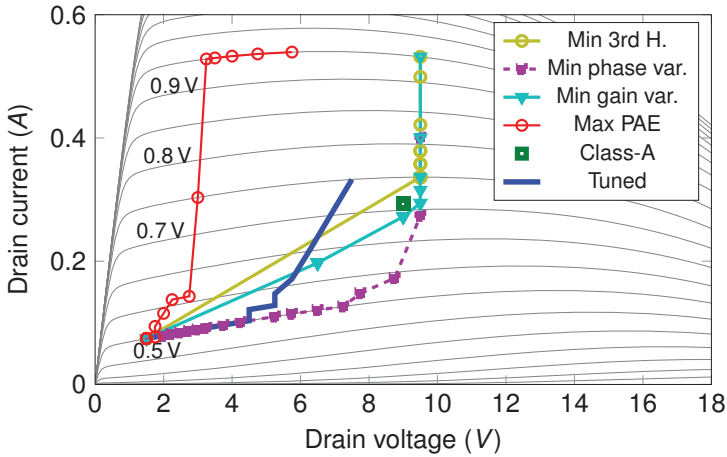


Figure 3.19: Dynamic biasing paths in the I-V plane.

3.7 Continuous bias variation for the pHEMT

In this section, the bias functions are modeled as polynomials depending on input power, as in (3.4). The amplifier's response is tested for gate polynomials of 0th, 1st

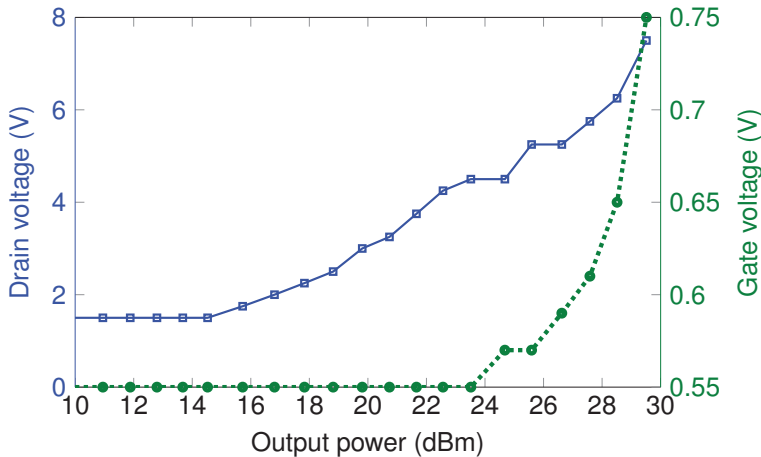


Figure 3.20: Drain and gate bias functions vs. output power for the “tuned” path shown in Figure 3.19.

and 2nd degrees, and for drain polynomials of 0th and 1st degree. Results for the static bias case, and for an interpolated version of the “tuned path” (Section 3.6) are also presented. The effect of adding dynamic gate bias (DGB), often overlooked in other studies, is also investigated by comparing dynamic against static gate biasing [65],[66].

The use of polynomial bias functions of input power, $V_G(p)$ and $V_D(p)$, makes it possible to find an optimum trade-off between efficiency, bias bandwidth, linearity and system complexity. Compared to varying the bias with the input envelope, biasing as a function of power may reduce the bandwidth of the bias, and even yield a higher average efficiency at the expense of a slightly lower average gain (Section 3.3).

Several constant, linear, and quadratic functions were tested for gate and drain in MATLAB. Their equations were extracted by joining a “starting” bias point (V_{g1}, V_{d1}) with an initial input power p_1 , to a “landing” bias point (V_{g2}, V_{d2}) corresponding to an input power of p_2 . A condition was derived for the quadratic function’s coefficients to ensure that the function is always monotonically increasing, since this will avoid that the bias enters undesirable regions in the I–V plane. Two different sets of coefficients were then used at the upper and lower bounds of the condition to cover the full range of possibilities.

Using the single-tone discrete data, the performance of each of the paths was compared in terms of output power, PAE, gain and phase-shift using cubic interpolation. It was observed that gain varied largely with input power (e.g., 2 dB or more) when the gate bias was fixed and the drain bias varied. When both gate and drain biases were dynamic, the gain variation was less than 1 dB. As expected,

PAE at the lower power range was highly dependent on the choice of the initial bias point. Lower V_{g1} and V_{d1} voltages resulted in higher PAE at p_1 , and affected PAE up to approximately 6 dB back-off from peak input power (it is (V_{g2}, V_{d2}) that affects PAE most at the higher power range). The lowest feasible value for the drain bias is limited by the transistor’s knee voltage, while the lowest value for the gate bias is limited by the pinch-off or threshold voltage. Figure 3.21 shows all of the (V_G, V_D) trajectories in the I–V plane including an interpolation of the “tuned path” (thick, black trace). The “tuned path” was interpolated using a third order polynomial for the drain bias, and a second order polynomial for the gate bias.

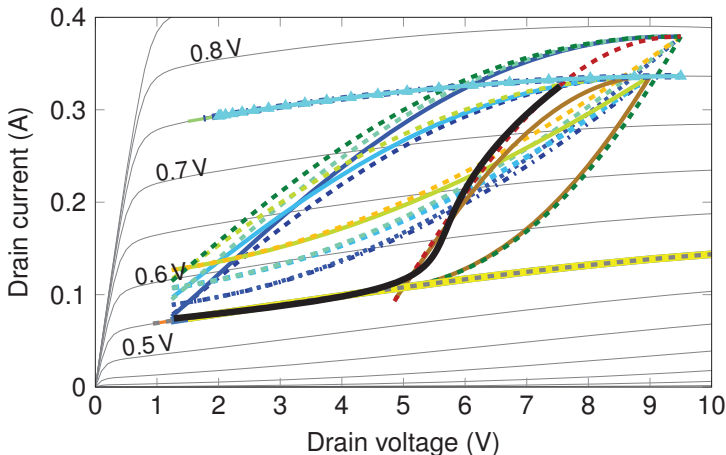


Figure 3.21: Different dynamic biasing paths in the I–V plane.

3.7.1 Test with a modulated signal

Only some of the path-combinations tested in the previous section were selected for this stage; prioritizing PAE, gain flatness, and phase variation in that order. The paths were then simulated with a 16-QAM modulated signal with a symbol rate of 20 MHz. The baseband signal was root-raised-cosine filtered with a roll-off factor of 0.35 and a 5-symbol delay, yielding an RF bandwidth $B_{\text{RF}} = 20(1 + 0.35) = 27$ MHz. The resulting PAE, gain, and ACPR are shown in Table 3.3.

From Table 3.6 it is clear that the tuned path presents the lowest ACPR levels, which is accordant with the expectations, since the algorithm took into account not only gain flatness, but also second and third harmonics. Nevertheless, the highest PAE was obtained for $N_G = 2$ and $N_D = 1$ using the same starting and landing points as the tuned path. Using a first-order polynomial for the drain has the advantage that that the drain bias bandwidth is only twice the RF bandwidth, in this case 54 MHz. Because of the low currents at the gate, the gate bandwidth

Table 3.6: Comparison of ACPR, PAE and gain for different DB paths. The average output power is fixed to 25 dBm.

N_G	N_D	(V_{G1}, V_{D1}) (V, V)	(V_{G2}, V_{D2}) (V, V)	ACPR-Low (dB)	ACPR-Up (dB)	PAE (%)	Gain (dB)
2	3	(0.55,1.5)	(0.75,7.5)	- 39.6	- 38.5	39.2	10.9
2	1	(0.57, 1.5)	(0.75,9)	- 37.4	- 34.8	50.5	10.7
		(0.55,1.5)	(0.75,7.5)	- 37.7	- 34.4	54.2	10.2
		(0.55,1.5)	(0.75,9)	- 38.2	- 35.1	50.6	10.6
0	1	(0.55, 1.5)	(0.55,10)	- 33.3	- 32.9	42.1	9.6
	2	(0.75, 2)	(0.75,9.5)	- 28.2	- 27.4	42.3	10.1
0	0	(0.71,9)	(0.71,9)	- 40.4	- 40.1	11.9	11.2

is much less critical. Fixing the gate, the ACPR may be moderate even in deep class-AB, but using DGB instead can yield 5 extra PAE points. Likewise, linearity may be a bit better for a traditional class-A, but 42 PAE points are gained with DB, not to mention that ACPR can be further reduced by means of memoryless DPD.

Figure 3.22 shows the spectrum for the different paths tested with the modulated signal.

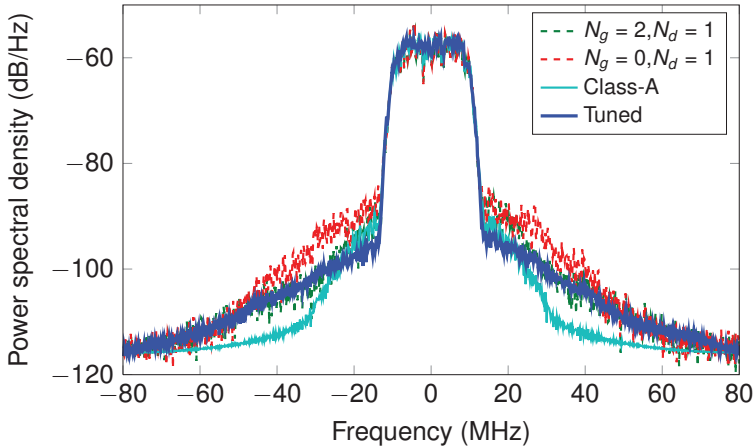


Figure 3.22: Power spectral density for the most important biasing paths from Table 3.6.

3.7.2 Summary of the results with a 16-QAM signal

Using polynomial functions of the input power, results from simulation with a modulated signal showed an increase of 40 points in PAE with an increment of 3 dB in ACPR compared to a class-A amplifier. Such a system would require a drain bandwidth of only two times the RF signal bandwidth, which is only a fraction of that used in standard envelope tracking. The interpolation of the path yielded by the point-search algorithm gave the best linearity result, at the expense of slightly reduced PAE, and a higher bandwidth requirement for the drain bias signal (six times the bandwidth of the RF signal, as the drain polynomial was of third order).

Chapter 4

Optimization theory applied to dynamic biasing

In Chapter 3 it was explained that the gate bias (V_G) and the drain bias (V_D) can be controlled by the input power (p) using low-order polynomial functions:

$$V_G(p) = g_2 p^2 + g_1 p + g_0, \quad (4.1)$$

$$V_D(p) = d_1 p + d_0. \quad (4.2)$$

Let the vector of bias polynomial coefficients (β) be defined as

$$\beta = [g_2, g_1, g_0, d_1, d_0]. \quad (4.3)$$

This chapter deals with the problem of finding an optimum set of bias coefficients, β^* , that achieves a good compromise between linearity and average dissipated power, using constrained optimization theory. The amplifier is initially characterized using the single-tone sweep, as described in Section 3.5. The method is applied to the pHEMT transistor described in Chapter 3 [67], and to an unmatched HBT MMIC transistor with a maximum output power of 20.5 dBm when the drain bias is fixed at 5 V [68].

Simulating with a root-raised cosine filtered 16-QAM signal with 6.5-dB PAPR, the random search algorithm yielded some solutions with average PAE greater than 40% (Table 4.1), and others with a balanced trade-off with twice as high PAE, and nearly the same linearity level, compared to class A operation.

Finally, different nonlinearity measures that can also be used to identify the coefficients of a digital memoryless polynomial predistorter are presented and discussed. The concept of merging predistortion and dynamic biasing without increasing bias bandwidth is explained.

4.1 General statement of the problem

The goal of the optimization process is to minimize two quantities: the power dissipated by the amplifier, and the nonlinearity, quantified as the in-band nonlinear

distortion. Therefore, the global error function, written for simplicity as $J(\boldsymbol{\beta})$, is actually composed of two subfunctions or measures: $P(\boldsymbol{\beta}, p)$ for dissipated power, and $L(\boldsymbol{\beta}, p)$ for nonlinearity. Both measures are defined in sections 4.3.1 and 4.3.2 of this chapter. The variable to optimize is the set of polynomial coefficients in $\boldsymbol{\beta}$ (see (4.1)–(4.3)). Mathematically, we wish to find a global optimum $\boldsymbol{\beta}^*$ such that

$$J(\boldsymbol{\beta}^*) < J(\boldsymbol{\beta}), \forall \boldsymbol{\beta} \in \Omega \quad (4.4)$$

where Ω is the search space delimited by the constraints. In practice, depending on the optimization problem and on the error function, it might be unlikely that the global optimum is found. Good local optimum solutions $\boldsymbol{\beta}_s$ can nonetheless be found such that $J(\boldsymbol{\beta}_s) < J(\boldsymbol{\beta}), \forall \boldsymbol{\beta} \in \Omega_s$, where $\Omega_s \in \Omega$.

4.2 Determination of constraints

Two types of constraints were used. The bound constraints, $\boldsymbol{\beta}_{\text{lb}}$ and $\boldsymbol{\beta}_{\text{ub}}$, are lower and upper bound limits on the values of the elements of $\boldsymbol{\beta}$. That is,

$$\boldsymbol{\beta}_{\text{lb}} \leq \boldsymbol{\beta} \leq \boldsymbol{\beta}_{\text{ub}}. \quad (4.5)$$

Linear constraints are bounded linear combinations of the elements of $\boldsymbol{\beta}$. They have the form

$$\mathbf{A}\boldsymbol{\beta} \leq \mathbf{b} \quad (4.6)$$

where \mathbf{b} is a vector with N_c elements— N_c being the number of linear constraints—and \mathbf{A} is an N_c -by-5 matrix, since there are five elements in $\boldsymbol{\beta}$. Both types of constraints are derived based on the following criteria for $V_G(p)$ and $V_D(p)$:

- I. $V_G(p)$, and $V_D(p)$ must be monotonically increasing (MI).
- II. There are upper and lower bounds for the values of V_G , V_D , and p , given by the minimum and maximum values in the single-tone characterization for each variable (see Section 3.5). That is

$$V_{G,\min} \leq V_G(p) \leq V_{G,\max} \quad (4.7)$$

$$V_{D,\min} \leq V_D(p) \leq V_{D,\max} \quad (4.8)$$

The derivation of the constraints, explained in detail in Appendix A, yielded the following expressions:

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & p_{\max} & 1 \\ p_{\max}^2 & p_{\max} & 1 & 0 & 0 \end{bmatrix} \quad (4.9)$$

$$\mathbf{b} = [V_{D,\max} \quad V_{G,\max}]^T \quad (4.10)$$

$$\beta_{\text{lb}} = [0 \quad 0 \quad V_{G,\text{min}} \quad 0 \quad V_{D,\text{min}}]^\top \quad (4.11)$$

$$\beta_{\text{ub}} = \left[\frac{\Delta V_G}{p_{\text{max}}^2} \quad \frac{\Delta V_G}{p_{\text{max}}} \quad V_{G,\text{max}} \quad \frac{\Delta V_D}{p_{\text{max}}} \quad V_{D,\text{max}} \right]^\top \quad (4.12)$$

$$\Delta V_G = V_{G,\text{max}} - V_{G,\text{min}} \quad (4.13)$$

$$\Delta V_D = V_{D,\text{max}} - V_{D,\text{min}} \quad (4.14)$$

4.3 Structure of the error function

The purpose of dynamic bias optimization is to find a set of coefficients, β^* , so that the amplification system yields both adequate linearity, and low dissipated power. The set of coefficients β^* corresponds to a suitable local (or ideally to the global) minimum of the error function. Since this is a multivariable optimization problem with two optimization goals, the error function J was chosen to be of the form:

$$J = \exp\left(\frac{L - L_0}{L_1 - L_0}\right) + \exp\left(\frac{P - P_0}{P_1 - P_0}\right), \quad (4.15)$$

where L is the measure for nonlinearity and P the measure for dissipated power. The threshold values for measures L and P — (L_0, L_1) and (P_0, P_1) , respectively—are chosen so that

$$L_1 > L_0 \quad (4.16)$$

$$P_1 > P_0. \quad (4.17)$$

Since the structure of both terms in the error function J is the same, let us temporarily consider only the first one. When variable L increases until it equals L_0 , the exponential term yields an error of 1. The difference $L_1 - L_0$ determines the rate of increase of the error once the lowest threshold L_0 is exceeded. The same applies to variable P . Figure 4.1 represents graphically this idea for arbitrarily chosen values of (L_0, L_1) , and (P_0, P_1) .

4.3.1 Measuring nonlinearity

Consider a nonlinear system $S\{\cdot\}$ that maps the low-pass signal $x(t)$ into a low-pass output signal $y(t)$, i.e., $y(t) = S\{x(t)\}$. Let us assume that the system can be suitably modeled by a memoryless complex polynomial system, $\hat{y}(t) = \hat{S}\{x(t)\}$, and $\hat{y}(t) \approx y(t)$, so that

$$\hat{y}(t) = x(t) \sum_{i=0}^{N/2} C_{2i} |x(t)|^{2i}, \quad (4.18)$$

where N is the order of the complex polynomial, $x(t)$ is the input voltage to the amplifier, and $C_{2i+1} = 0$, for all i from 0 to $N/2 - 1$. Assuming a matched load at

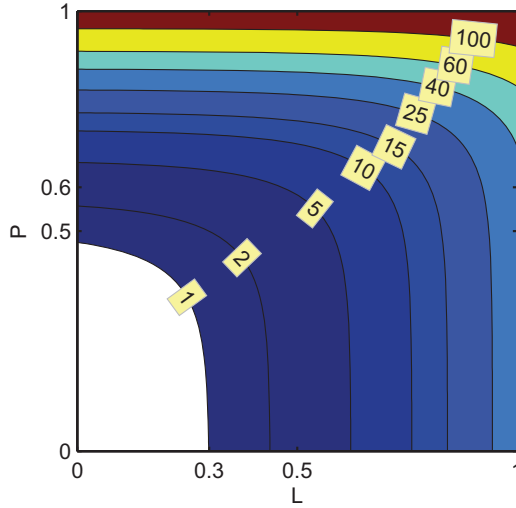


Figure 4.1: An example of the contours of the error function used for multivariable optimization defined in (4.15). In this example $(L_0, L_1) = (0.3, 0.5)$, and $(P_0, P_1) = (0.5, 0.6)$. By choosing different values of the difference $L_1 - L_0$ or $P_1 - P_0$ we can control how steep the contours become in the direction of L or P . For the set of chosen values the rate at which the error increases along the P -axis is greater, and since in this illustration $L_0 < P_0$, the cost at $(L = 0.3, P = 0)$ is higher than the cost at $(L = 0, P = 0.3)$.

all frequencies, with a $1-\Omega$ impedance, the time-average nonlinear power is given by

$$P_0 = \int |\hat{y}(t)|^2 dt = \int p(t)^{i+j+1} \sum_{i=0}^{N/2} \sum_{j=0}^{N/2} C_{2i} C_{2j}^* dt \quad (4.19)$$

where $p(t)$ is the instantaneous input power, $p(t) = |x(t)|^2$. For $N = 4$, we obtain

$$P_0 = |C_4|^2 w_5 + 2\Re\{C_4 C_2^*\} w_4 + (|C_2|^2 + 2\Re\{C_4 C_0^*\}) w_3 + 2\Re\{C_2 C_0^*\} w_2 + |C_0|^2 w_1 \quad (4.20)$$

where

$$w_j = \int p(t)^j dt. \quad (4.21)$$

The linear power, $P_{0,\text{linear}}$, is given by

$$P_{0,\text{linear}} = |C_0|^2 w_1. \quad (4.22)$$

If we defined the nonlinearity measure L as $P_0 - |C_0|^2 w_1$, its minimization could yield negative values from the $2\Re\{C_i C_j^*\}$ terms. Considering the worst case, we

replace terms of the form $2\Re\{C_i C_j^*\}$ in (4.20) with $2|C_i||C_j|$, which yields

$$P_{0,\max} = |C_4|^2 w_5 + 2|C_4 C_2| w_4 + (|C_2|^2 + 2|C_4 C_0|) w_3 + 2|C_2 C_0| w_2 + |C_0|^2 w_1. \quad (4.23)$$

Let the nonlinearity measure, subfunction L , be defined as the ratio of maximum in-band nonlinear distortion power to the linear power at the desired channel, $P_{0,\text{linear}}$. That is

$$L = (\max(P_{0,\max}) - P_{0,\text{linear}}) / P_{0,\text{linear}}. \quad (4.24)$$

Replacing (4.22) and (4.23) in (4.24) we finally obtain

$$L = \frac{|C_4|^2 w_5 + 2|C_4 C_2| w_4 + (|C_2|^2 + 2|C_4 C_0|) w_3 + 2|C_2 C_0| w_2}{|C_0|^2 w_1}. \quad (4.25)$$

Subfunction L is a consistent measure of nonlinearity; minimizing it reduces the power in the nonlinear distortion cross-terms, and favors a high gain at the fundamental, $|C_0|^2$. This is useful since it is not only important that the gain varies smoothly, but also that it is always above a threshold to avoid the need for a high-power input stage.

A note on in-band and out-of-band components in power

It might be tempting to consider *exclusively* terms of the form

$$p(t)^{i+j+1} \left(\sum_{i=0}^{N/2} \sum_{j=0}^{N/2} C_{2i} C_{2j}^* \right) \quad (4.26)$$

for which $i + j + 1$ is odd, as those corresponding to the in-band average output power in (4.19). However, the fact that the nonlinear system is assumed to be a polynomial of odd-order terms only, i.e., $C_{2i+1} = 0$, and that equations are formulated for low-pass equivalent signals (i.e., with spectrum centered around zero frequency) instead of passband signals, ensures that only in-band terms will be present at the output of the odd-order low-pass equivalent complex system defined in (4.18). Consequently, all of the terms in (4.19) must be included without caring if the sum of $i + j + 1$ is odd or even.

As an example, consider the following. A low-pass equivalent signal, $x(t)$, has its spectrum centered around frequency zero. An RF signal $X(t)$, or passband signal, constructed from $x(t)$ by upconversion,

$$X(t) = \Re \{ x(t) e^{j2\pi f_c t} \} \quad (4.27)$$

will be centered around frequency f_c . If $x(t)$ was the low-pass equivalent of a two-tone signal

$$x(t) = a e^{-j\alpha/2t} + b e^{j\alpha/2t} \quad (4.28)$$

with frequency spacing α , and $y(t)$ a third-order nonlinearity of the form

$$y(t) = |x(t)|^2 x(t) \quad (4.29)$$

$y(t)$ would contain the third order intermodulation (IM) components at frequencies $-3\alpha/2$ and $3\alpha/2$, and distortion components at the original frequencies $-\alpha/2$ and $\alpha/2$. Nevertheless, since no carrier frequency is considered in the expression, it would not contain any harmonic components of the first or second tones. Thus if the power of $y(t)$, $|y(t)|^2$ was calculated, only in-band components would be present in the calculation.

If the two-tone passband signal, $U(t)$, of the form

$$U(t) = A \cos(f_c - \alpha/2)t + B \cos(f_c + \alpha/2)t \quad (4.30)$$

is the input to the third-order passband nonlinearity, $V(t) = U(t)^3$, IM components will be present at the output around center frequency f_c , $(f_c - 3\alpha/2, f_c + 3\alpha/2)$, and at the original frequencies, $(f_c - \alpha/2, f_c + \alpha/2)$, as well as harmonic and third order components around the frequency $3f_c$, $(3f_c - \alpha/2, f_c + \alpha/2, 3f_c - 3\alpha/2, f_c + 3\alpha/2)$. The last set of frequency components corresponds to out-of-band third-order distortion.

In conclusion, a nonlinear system that consists of the weighted sum of odd-order powers of the input signal will have some out of band components if it is a band-pass system. If the system is low-pass (therefore the input is also a low-pass signal), all of the IM components will be in-band.

4.3.2 Measuring the dissipated power

The proposed measure for dissipated power is simply the average of the dissipated power considering the probability distribution function (PDF) $\Psi(p)$ of the modulated signal

$$P = \int_0^{p_{\max}} P_{\text{dis}} \Psi(p) dp. \quad (4.31)$$

If one heavily prioritized minimizing dissipated power over linearity, so that the error given by the exponential linearity term was small compared to that of the dissipated power term, it might happen that the optimized solution β^* yields impractically low gain levels. This is because it was the linearity term that ensured a high gain through the factor $|C_0|^2 w_1$ (see (4.25)). This was indeed observed with the HBT transistor, motivating the use of a modified dissipated power measure that includes the output power P_0 :

$$P = \frac{\int_0^{p_{\max}} P_{\text{dis}} \Psi(p) dp}{\int_0^{p_{\max}} P_0 \Psi(p) dp} \quad (4.32)$$

4.4 Choice of optimization method

Since the amplifier's output is only measured at some points (p_i, V_{Gi}, V_{Di}) in the subspace $p \in [0, p_{\max}]$, $V_G \in [V_{G,\min}, V_{G,\max}]$, $V_D \in [V_{D,\min}, V_{D,\max}]$, the error function J can only be computed within this subspace. Gradient methods tend to violate constraints, but can be used by setting $J \rightarrow \infty$ whenever p , $V_G(p)$ or $V_D(p)$ are out of range. Their drawback is that they tend to converge rapidly towards the nearest local solution, which is usually far from the optimum [69]. An alternative is to use random search optimization, as explained by Baba [70].

The principle of random search is to add random vectors to the current optimum solution. If the addition respects the constraints, its error function is computed. If the error function is lower than that of the current optimum solution, the new vector will overwrite the current optimum solution. If not, a new random vector is generated, and the process is repeated. The amplitude of the random vector coefficients can be scaled (i.e., adaptive random search, ARS), and the scaling can be shrunk exponentially in time to narrow the search [71]. The list of input and output variables, the parameters, and a detailed description of the algorithm used is given in Appendix B.

Despite its simplicity, this method is robust in that it may converge to the global optimum, and it can be applied to discontinuous and noisy error and constraint functions [69]. Intelligently choosing the search range, and its exponential contraction in time, one has the possibility of searching in very wide or narrow regions in the search space around the initial solution. When tested in the context of polynomial system identification, the method yielded an estimation accuracy very near to that of least squares optimization.

4.5 Results

The dynamic bias system was optimized for a 16-QAM modulated signal with root-raised-cosine (RRC) filtering with a roll-off factor of 0.22. In order to obtain a set of values for optimization parameter p , the PDF of the QAM signal was calculated around 25 evenly spaced values in the range $[0, p_{\max}]$. Several optimization tests were performed varying the values for the initial solution β_0 , number of iterations N , search range σ , and the search range contraction vector λ . For each of the different cases in tables 4.1 and 4.2, the input power was adjusted so that the output power was approximately the same for all cases. To allow room for experimentation, some optimizations were carried out without using the constraints, but all of the solutions which yielded best performance complied with the constraints. Even if the constraints are not to be used they provide a very useful reference point to choose the search range scaling factors in vector σ .

As explained in Section 4.5.1, after optimal biasing functions are identified using single-tone data, a new set of simulations are run using Agilent's ADS circuit

simulator using real-time virtual dynamic biasing, with a model that includes thermal effects (see Table 4.1).

4.5.1 pHEMT MMIC amplifier

Since the PA had an output power of 30 dBm at 20 dBm input power with 2 dB compression ($V_G = 0.75$ V, $V_D = 7.5$ V) and the 16-QAM signal has a PAPR of approximately 6 dB, the reference output power was chosen to be 25 dBm.

This subsection reports two optimized results for two different initial solutions, $\beta_{0,0}$ and $\beta_{0,1}$. The initial solution $\beta_{0,0}$ was calculated joining the points (0, 0.53, 1.5) and (0.1, 0.75, 7.5), while $\beta_{0,1}$, deliberately chosen to be inefficient and nonlinear, joins the points (0, 0.79, 8) and (0.1, 0.81, 9). Both cases refer to the (p, V_G, V_D) coordinates. In Table 4.1, “case 0” corresponds to $\beta_{0,0}$, while “case 1” and “case 2” are the results from two different optimizations of $\beta_{0,0}$ and $\beta_{0,1}$. “Case A” presents data for the case of the static bias class-A amplifier biased at $(V_g, V_d) = (0.75V, 7.5V)$.

Table 4.1 compares results obtained from harmonic balance single-tone simulation to those obtained from envelope simulation with the 16-QAM modulated signal, and it clearly shows an agreement between the two methods. Relevant solutions were found for both efficient and inefficient initial solutions. “Case 2”, however, was obtained optimizing only for linearity, hence the lower PAE. Figure 4.2 shows the location of the dynamic bias paths from Table 4.1 in the I–V plane, and figures 4.3–4.6 describe the performance of the DB system according to single-tone simulation data. Note from Figure 4.3 that the path optimized for linearity, “case 2”, has flatter gain than the pure class-A amplifier. Figure 4.4 and 4.6 show that while “case 0” ranks highest in PAE, all DB solutions outperform the class-A amplifier by far in PAE and dissipated power.

Table 4.1: Comparison of ACPR, PAE, and gain for different DB paths, for the pHEMT amplifier for an output power of 25 dBm.

Case	Modulated signal				Single-tone		
	ACPRL (dB)	ACPRU (dB)	PAE (%)	Gain (dB)	PAE (%)	Gain (dB)	P_d (W)
0	-38.0	-33.9	46.6	10.3	44.7	10.1	0.3
1	-39.7	-37.0	28.8	11.0	26.1	11.1	0.8
2	-35.5	-38.9	41.7	10.6	37.7	10.9	0.4
A	-36.2	-36.4	12.6	11.8	17.4	11.8	1.9

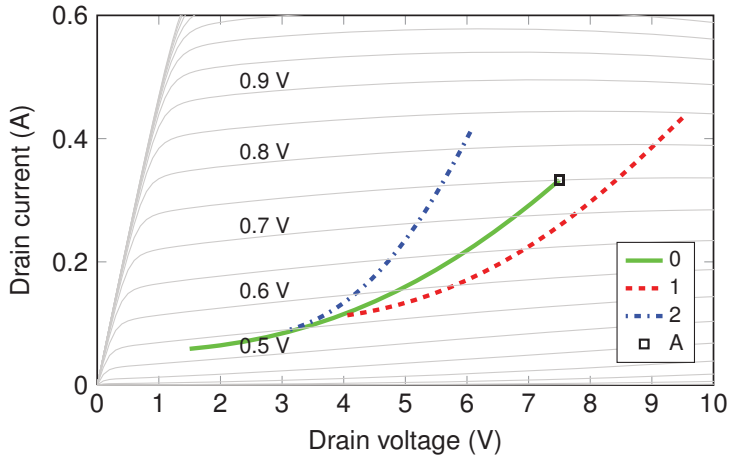


Figure 4.2: Trajectories in the I–V plane followed by the unoptimized and optimized solutions as described in Table 4.1.

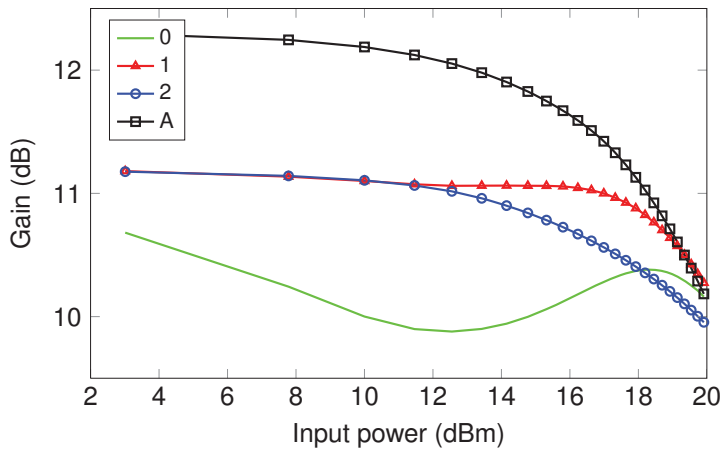


Figure 4.3: Gain as a function of input power for each of the cases in Table 4.1.

4.5.2 HBT MMIC transistor

An HBT transistor manufactured by the Triquint foundry was also used to test the optimization method. The transistor has an emitter composed of three fingers, each with a width of 3 μm , and a length of 50 μm , which yields an emitter area of 450 μm^2 . Since the manufacturer specifies a maximum junction current density of

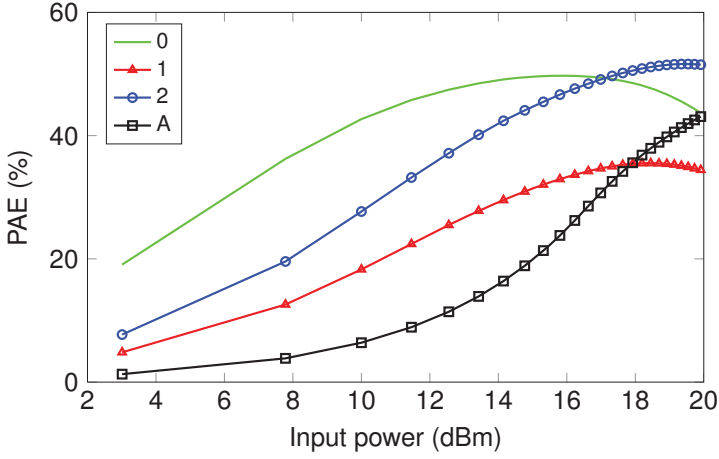


Figure 4.4: PAE as a function of input power for each of the cases in Table 4.1.

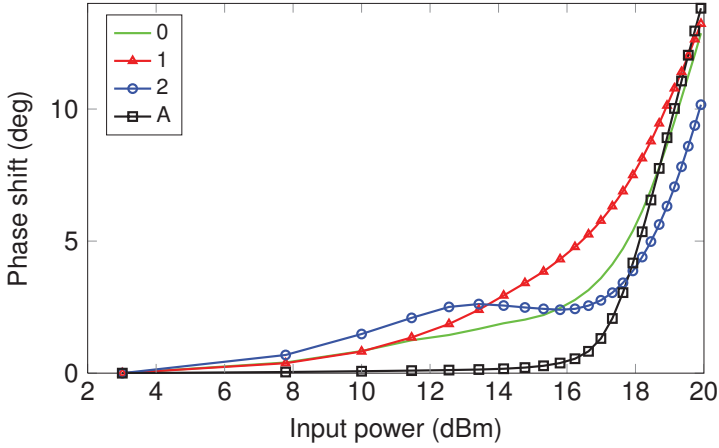


Figure 4.5: Phase shift as a function of input power for each of the cases in Table 4.1.

20 kA/cm² [43], the maximum current I_{\max} that the transistor can handle is

$$I_{\max} = \text{emitter area} \times \text{max. junction current density} \quad (4.33)$$

$$= 90 \text{ mA} . \quad (4.34)$$

The unmatched HBT transistor used for simulation was much more linear than the pHEMT transistor, but due to the lack of matching it is also expected that lower PAE is achieved. Table 4.2 presents the results for the modulated signal only.

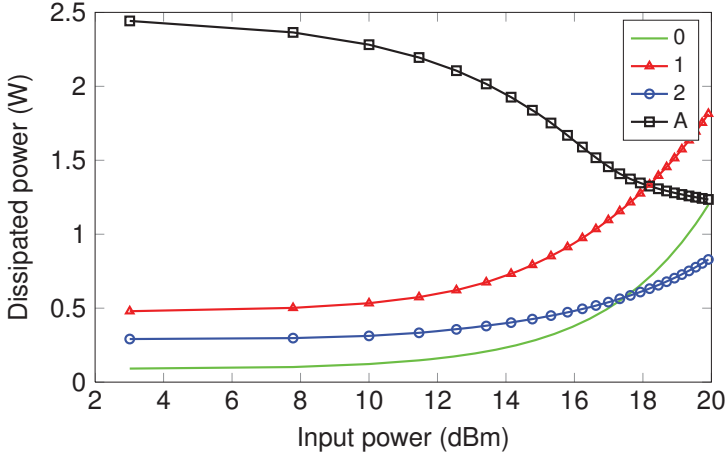


Figure 4.6: Dissipated power as a function of input power for each of the cases in Table 4.1.

Cases “1” and “2” correspond to optimized results using the adaptive random search algorithm, while “PS” stands for “point-search”. It is a solution obtained from interpolating the results obtained by the point-search algorithm described in Chapter 3. Case “A” is for the class-A amplifier, which was used as a reference to determine an output power reference level of 14.8 dBm.

Figure 4.7 shows the DB paths and the class-A point in the I–V plane. The contours and values in white boxes describe the small-signal gain of the HBT, as in figures 3.13 and 3.14. One can see that there is a wide region where the gain is between 19 dB and 20 dB, which is good for high linearity, where the base current is between 360 μ A and 480 μ A. If one, however, wishes to obtain higher efficiency one must go lower in bias, but this coincides with a rapid variation between 17 dB and 19 dB in small-signal gain. The results for single-tone characterization shown in figures 4.8 to 4.11 are consistent with these observations. Case “2” is attractive from a linearity point of view, since there is only a 4-dB increase in ACPR respect to the class-A case, but the average PAE is doubled. The point search algorithm yielded a fairly good result with PAE of 38%, and case “1” matches this feat but with lower ACPR. The highest PAE obtained with optimization is more than three times that of the class-A amplifier alone. From the different optimization solutions it was seen that the phase variation in the HBT could be less than one degree, which explains the lower ACPR compared to the pHEMT amplifier.

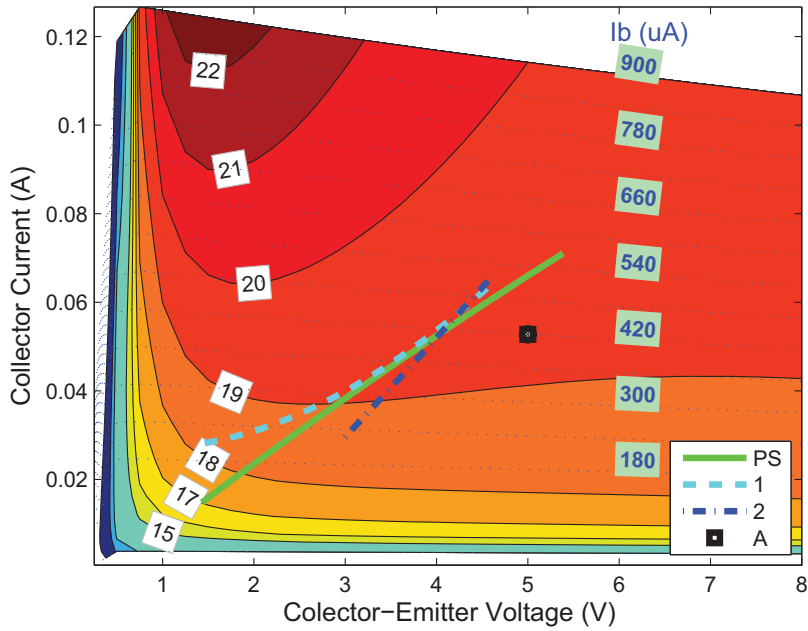


Figure 4.7: Optimized dynamic bias paths in the I-V plane for the HBT transistor.

Table 4.2: Comparison for the different dynamic biasing paths for the HBT transistor in terms of ACPR, PAE and gain, for an output power of 14.8 dBm.

Case	Modulated signal			Gain (dB)	P_{dis} (mW)	P_0 (dBm)
	ACPRL (dB)	ACPRU (dB)	PAE (%)			
PS	-34.4	-34.1	38.6	17.5	48.3	14.85
1	-35.0	-37.4	38.3	17.9	48.6	14.82
2	-47.0	-47.1	22.4	19.0	105.0	14.83
A	-51.7	-50.4	11.3	19.3	237.1	14.83

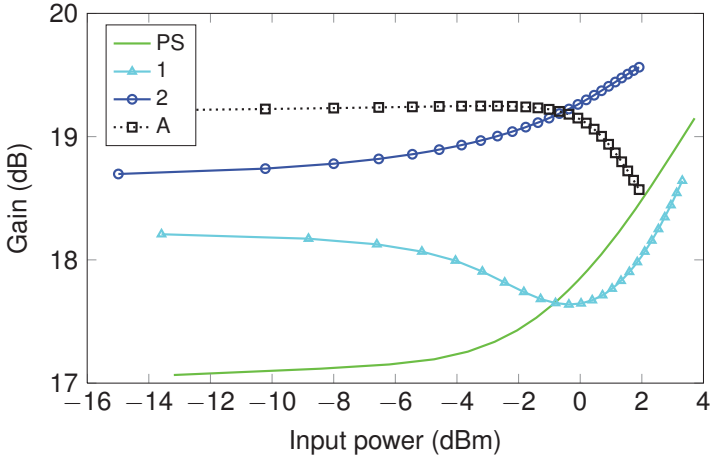


Figure 4.8: Gain as a function of input power for each of the cases in Table 4.2.

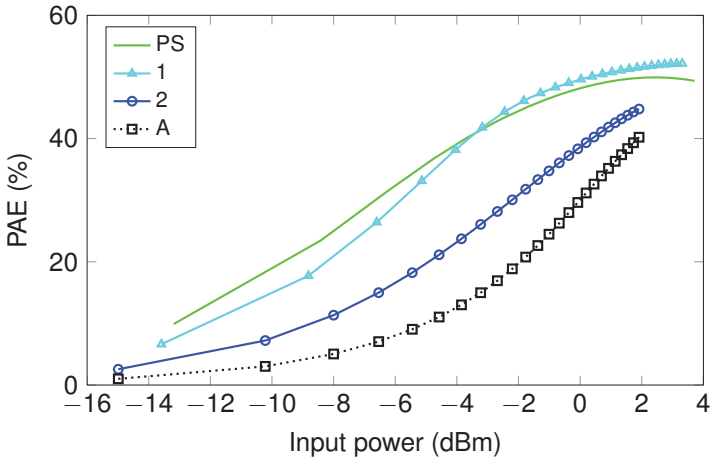


Figure 4.9: PAE as a function of input power for each of the cases in Table 4.2.

4.6 Dynamic biasing and DPD

Digital predistortion (DPD) has become a popular linearization method in digital communication systems, as it can be implemented in a several different ways—e.g., look-up tables, memoryless polynomials, neural networks—with different degrees of complexity. It requires no additional hardware, since the algorithms are implemented in a digital signal processor or FPGA unit [55].

DPD can be readily combined with dynamic bias because the two are independen-

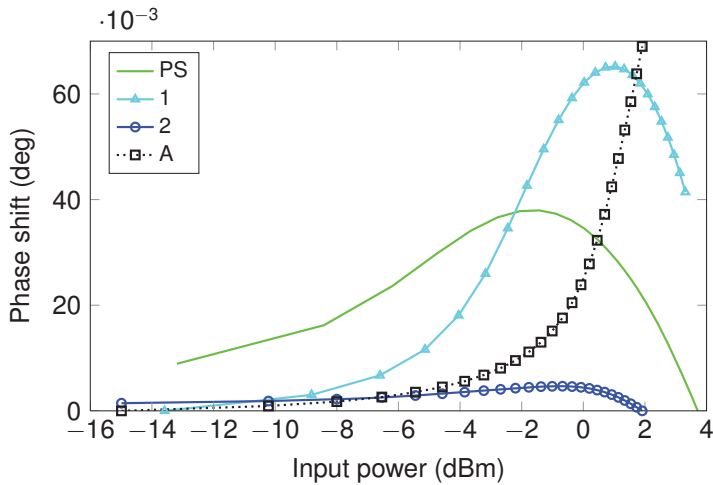


Figure 4.10: Phase shift as a function of input power for each of the cases in Table 4.2.

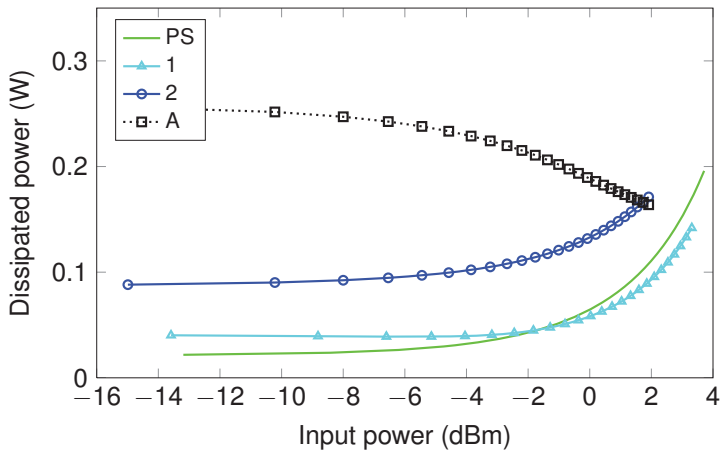


Figure 4.11: Dissipated power as a function of input power for each of the cases in Table 4.2.

dent of carrier frequency, and can be used for signals of different bandwidth. As the bandwidth of the modulated signal increases, though, the order of the nonlinearity that the predistorter can correct will decrease.

If DPD is combined with ET, the bias source will have to track the envelope of the predistorted signal which has much higher bandwidth, thus setting a very high demand on the bandwidth of the envelope amplifier. What is usually done is

to filter the envelope of the predistorted signal before applying it to the tracker. Though this may constrain the bias bandwidth to be even smaller than that of the RF signal, more complex DPD algorithms that include memory mitigation will have to be used to compensate for the filtering.

This same problem applies to dynamic biasing, where bias varies as a function of input power. To go around it the architecture shown in Figure 4.12 is proposed. Both the drain and the gate bias depend on the power of the original modulated signal, and the parameters of the predistorter are estimated so as to invert the amplitude and phase-shift distortion characteristics of the PA. In a statically biased amplifier, a first estimation of the coefficients of an amplitude memoryless polynomial DPD can be obtained by modeling the input voltage of the PA vs. the output voltage of the PA, so as to obtain the shape of the inverse function. With the solution proposed in Figure 4.12, an iterative algorithm would be required to partially cancel distortion from the amplifier.

Another possibility would be to have the gate bias depend on the input signal to the PA, that is the predistorted signal, while the drain bias depends on the power of the modulated signal. This is consistent with regular PA operation even without DPD, as the gate bias normally controls the input of the transistor, while the drain bias controls the voltage seen at the output. The feasibility to implement this architecture would depend on the bandwidth that the gate tracker is capable of handling, so it is indirectly limited by the order of the polynomial predistorter, and by the bandwidth of the modulated signal.

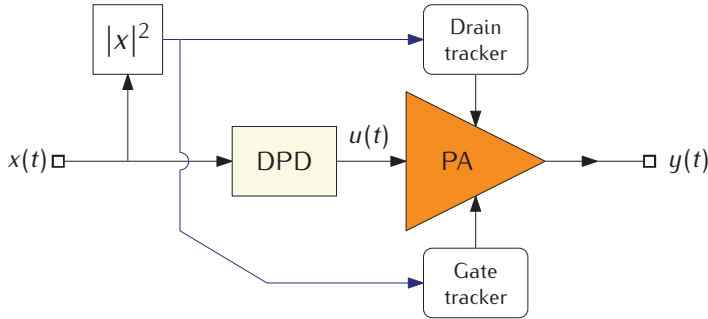


Figure 4.12: Digital predistortion with dynamic biasing. The gate and drain bias depend on the power of the modulated signal, while the DPD signal is upconverted and applied to the power amplifier.

4.7 A different measure for nonlinearity

In this work, memoryless predistortion in its Cartesian form is preferred over look-up tables and memoryless polar predistortion; the reason being faster convergence,

reduced number of parameters, and that the bandwidth of the predistorted signal will equal the bandwidth of the RF signal times the order of the predistortion polynomial (i.e., the order of the DPD polynomial controls the bandwidth of the predistorted signal).

Section 4.3.1 described a measure for nonlinearity that focused on reducing nonlinear power at the adjacent and alternate channels by modeling the low-pass equivalent of the PA as a fifth order complex memoryless polynomial. The same concept can be applied to the DPD-PA chain, as Figure 4.13 illustrates. The

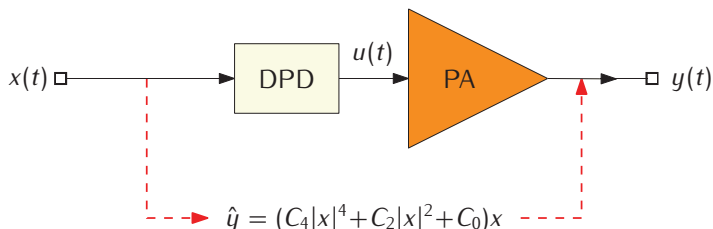


Figure 4.13: System composed of a digital predistorter followed by a power amplifier modeled as a 5th order memoryless complex polynomial.

system's output $y(t)$ is approximated by

$$\hat{y}(t) = x(t) [C_4|x(t)|^4 + C_2|x(t)|^2 + C_0] . \quad (4.35)$$

Consequently, measure L , defined in (4.25), can be used to identify the coefficients a_j of the predistorter. The predistorter's output, $u(t)$, is of the form

$$u(t) = x(t) \sum_{j=0}^{M/2} a_{2j} |x(t)|^{2j} \quad (4.36)$$

where $x(t)$ is the low-pass equivalent input signal, and M the order of the predistorter. One can safely set even-order coefficients to zero, that is $a_{2j+1} = 0$, so that only in-band components are considered.

The nonlinearity measure L was most useful for bias function optimization, but it presents a limitation: it does not consider the phase difference between the set of C_i coefficients ($i = 0, 2, 4$). That is because terms of the form $2\Re\{C_i C_j^*\}$ are substituted by $2|C_i||C_j|$ to prevent L from becoming negative. The nonlinear power could be thus redefined as the average least squares error of the 5th order simplified nonlinear system. Define the an error signal

$$e(t) = \hat{y}(t) - gx(t) \quad (4.37)$$

where g is the “target” complex gain for the DPD-PA system. Replacing (4.35) in (4.37) we obtain

$$e(t) = x(t) [C_4|x(t)|^4 + C_2|x(t)|^2] + (C_0 - g)x(t) . \quad (4.38)$$

Then the average nonlinear error power can be defined as

$$E = \frac{1}{T} \int_0^T e(t)e^*(t) dt. \quad (4.39)$$

An immediately noticeable advantage is that E does not have the possibility of being negative. Replacing (4.38) in (4.39) yields

$$E = |C_4|^2 w_5 + 2\Re\{C_4 C_2^*\} w_4 + (2\Re\{C_4(C_0 - g)^*\} + |C_2|^2) w_3 + 2\Re\{C_2(C_0 - g)^*\} w_2 + |C_0 - g|^2 w_1 \quad (4.40)$$

where the weights w_j are defined as before,

$$w_j = 1/T \int_0^T (|x(t)|^2)^j dt. \quad (4.41)$$

Yet another advantage comes to mind when looking at (4.40): the phase difference between the pair of coefficients C_i and C_j is taken into account, making it possible to compensate for phase-shift distortion (also known as memoryless AM/PM distortion).

Two interesting values of g can be chosen. Selecting $g = C_0$ in (4.40), we can define $E_0 = E(g = C_0)$, which yields

$$E_0 = |C_4|^2 w_5 + 2\Re\{C_4 C_2^*\} w_4 + |C_2|^2 w_3. \quad (4.42)$$

The structure of (4.42) is much simpler than that of (4.25). Another interesting possibility is to define the target gain $g = \hat{g}_{yx}$ as an odd first-order least squares fit of $y(t)$ in terms of $x(t)$ (i.e., only one least squares coefficient is estimated), that is

$$\hat{g}_{yx} = \frac{1/T \int_0^T \hat{y}(t)x^*(t) dt}{1/T \int_0^T x(t)x^*(t) dt}. \quad (4.43)$$

Equation (4.42) can also be viewed as the cross-correlation of $y(t)$ and $x(t)$ divided by the variance (or the power) of the zero-mean complex signal $x(t)$. Replacing (4.35) in (4.43) we obtain

$$g = C_4 w_3 / w_1 + C_2 w_2 / w_1 + C_0. \quad (4.44)$$

By substituting (4.44) in (4.40) and simplifying, we get

$$E_{yx} = |C_4|^2 \left(w_5 - \frac{w_3^2}{w_1} \right) + |C_2|^2 \left(w_3 - \frac{w_2^2}{w_1} \right) + 2\Re\{C_4 C_2^*\} \left(w_4 - \frac{w_3 w_2}{w_1} \right). \quad (4.45)$$

Intuitively, some advantage is expected from choosing $g = \hat{g}_{yx}$ as given by (4.45), since \hat{g}_{yx} represents a purely linear relation between $x(t)$ and $y(t)$, and

is therefore overall “closer” to all values of the y/x function than $g = C_0$ is. It might be that it takes fewer iterations to find a DPD solution, or that better nonlinearity compensation can be achieved with the same polynomial order M , especially when combining DPD with dynamic bias, where the selection of the predistorter’s coefficients alters the amplifier’s response. The downside is that \hat{g}_{yx} is smaller than $g = C_0$.

4.7.1 A theoretical example with DPD

In this subsection, different nonlinearity measures are used to optimize the coefficients of a digital predistorter. The model for the amplifier is the simplest possible: a third-order baseband polynomial with real coefficients, so that only AM/AM distortion is considered. The performance of the DPD–PA system for each measure is evaluated in terms of EVM, adjacent-band distortion, and gain.

The amplifier

The amplifier’s response, $y(t)$, to a complex input, $u(t)$, is given by

$$y(t) = \begin{cases} u(t) (\alpha_2 |u(t)|^2 + \alpha_0) & \text{if } u(t) \leq x_{\text{sat}} \\ u(t)/|u(t)|x_{\text{sat}} & \text{if } u(t) > x_{\text{sat}} \end{cases} \quad (4.46)$$

where $u(t)$ is the output of the predistorter, x_{sat} is the saturation input voltage for the amplifier, and α_2 and α_0 are the third order and first order complex coefficients, respectively.

In our example, the amplifier’s small signal gain is set to one (i.e., $\alpha_0 = 1$), and $x_{\text{sat}} = 1.5$. The third-order coefficient was calculated so that $|y(t)| = 1$ when $|u(t)| = x_{\text{sat}}$. That is

$$\alpha_2 = \frac{x_{\text{sat}} - 1}{x_{\text{sat}}^3}. \quad (4.47)$$

Figure 4.14 shows the amplifier’s voltage response.

The nonlinearity measures

The measures that are used in this comparison are the following:

$$E_L = \frac{|C_4|^2 w_5 + 2|C_4 C_2| w_4 + (|C_2|^2 + 2|C_4 C_0|) w_3 + 2|C_2 C_0| w_2}{|C_0|^2 w_1} \quad (4.48)$$

$$E_0 = |C_4|^2 w_5 + 2\Re\{C_4 C_2^*\} w_4 + |C_2|^2 w_3 + |C_0 - g|^2 w_1 \quad (4.49)$$

$$E_{yx} = |C_4|^2 \left(w_5 - \frac{w_3^2}{w_1} \right) + |C_2|^2 \left(w_3 - \frac{w_2^2}{w_1} \right) + 2\Re\{C_4 C_2^*\} \left(w_4 - \frac{w_3 w_2}{w_1} \right) \quad (4.50)$$

$$E_{0\text{-LS}} = \int (\hat{y}(t) - C_0 x(t)) (\hat{y}^*(t) - C_0^* x^*(t)) dt \quad (4.51)$$

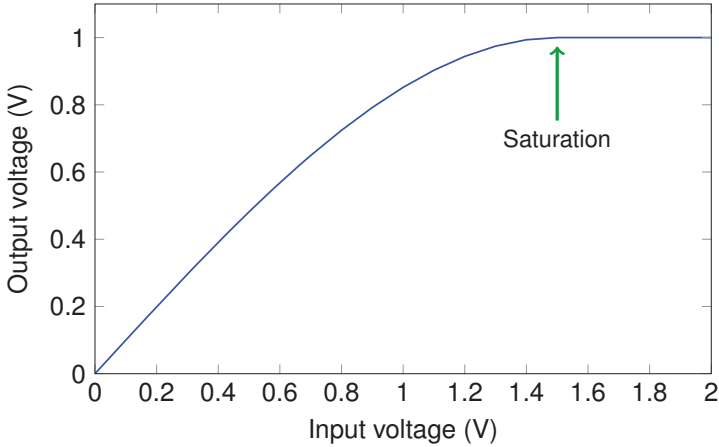


Figure 4.14: Output voltage vs. input voltage for the third-order polynomial amplifier defined in (4.46). The saturation voltage x_{sat} is 1.5 V, and the coefficients α_2 and α_0 are set to 0.1481 and 1, respectively.

$$E_{\text{LS}} = \int (y(t) - C_0 x(t)) (y^*(t) - C_0^* x^*(t)) dt \quad (4.52)$$

Equations (4.48),(4.50),(4.51) and (4.52) were defined in Section 4.3.1 and in the first part of this section. Equation (4.49), however, is the same expression given in (4.42) plus a linear term, $|C_0 - g|^2 w_1$, which is the last term in (4.40). The impact of this new term will become clear in the results. The classical least squares error (LS) is defined in (4.52), while (4.51) is the LS error computed as a function of $\hat{y}(t)$ instead of $y(t)$.

Methodology

The test signal is the 16-QAM signal used in Section 4.5 with a PAPR of approximately 6.5 dB—the PDF of the signal is shown in Figure 3.10. The target system gain g is set to be equal to the amplifier’s small-signal gain, α_0 (one, in this example). The signal is scaled so as to vary the peak voltage level, x_{max} , between α_0 and x_{sat} (1 and 1.5, respectively), in steps of 0.05. The DPD coefficients are optimized for each value of x_{max} and for each nonlinearity measure (see (4.48) to (4.52)). EVM, distortion power and average power gain are recorded for all of these cases. The first-order coefficient of the predistorter is set to one (as $\alpha_0 = 1$ and the target gain is $g = 1$); only the third- and fifth-order coefficients are optimized using MATLAB’s line-search solver.

The first criterion to evaluate performance is EVM (in decibels), defined as

$$\text{EVM} = 10 \log \left(\frac{\sum_{k=0}^{N_s} \|\tilde{y}[k] - g_{yx}\tilde{x}[k]\|^2}{\sum_{k=0}^{N_s} \|g_{yx}\tilde{x}[k]\|^2} \right) \quad (4.53)$$

where N_s denotes the number of symbols, $\tilde{x}[k]$ is the k th complex symbol of the original signal (before RRC filtering), and $\tilde{y}[k]$ is the k th symbol of the demodulated signal (at the output of the amplifier, after RRC filtering and downsampling). The scaling factor g_{yx} is identical to \hat{g}_{yx} , defined in (4.43), except that $y(t)$ is used in the cross-correlation instead of $\hat{y}(t)$. The symbol $\|\cdot\|$ refers to the norm operator, $\|x[k]\|^2 = \Re\{x[k]\}^2 + \Im\{x[k]\}^2$.

The second criterion to evaluate performance is referred to as “distortion power”, which is actually the sum of the power in the upper and lower adjacent channels, compared to the power in the desired channel. Note that the measurement bandwidth is twice the symbol rate (SR), so the channels are centered at $2\text{SR} + r$ and $-2\text{SR} + r$, respectively. (This measure is also deployed in Chapter 5. See Section 5.1.3.) For a two-tone signal, distortion power would be equivalent to the sum of the upper and lower IM3 and IM5 powers, divided by the total power contained in the two tones.

Results of the DPD optimization

The instantaneous gain response of the DPD-PA system for x_{\max} fixed to 1.5 V is shown in Figure 4.15. Figure 4.16 shows EVM, average power gain and distortion power as a function of the peak input voltage, x_{\max} .

In Figure 4.15, x_{\max} is fixed to 1.5 V, which means that the peak voltage of the predistorted signal reaches saturation. The amplifier’s response without DPD (blue curve) decays smoothly. The LS curve (E_{LS}) exhibits a high gain with a flat response, while the curve corresponding to $E_{0\text{-LS}}$ also exhibits a high gain but with a higher ripple. The gain characteristic for E_{yx} is also rippled, and smaller than all the others almost all along the x_{\max} -range. The overall gain of the modified function, $E_{0+\delta g}$, is slightly below that of E_{LS} and $E_{0\text{-LS}}$, but it is nicely shaped.

The LS error, E_{LS} , yields the lowest EVM for most of the values of x_{\max} . At $x_{\max} = 1$, the predistorter is not driven into saturation, and is therefore most effective. For that peak level, all the error functions except E_L perform alike.

Nevertheless, E_L , the measure proposed in Section 4.3.1, performs better than the others in terms of distortion when x_{\max} is above 1.15 V. The modified measure $E_{0+\delta g}$ follows E_{LS} and $E_{0\text{-LS}}$ tightly in the average gain plot, and it is second best in EVM after E_{LS} . The E_{yx} function competes with E_{LS} , $E_{0\text{-LS}}$ and $E_{0+\delta g}$ for lowest distortion power when x_{\max} is below 1.13 V—it performs quite well when it comes to EVM too—but above that threshold its performance worsens and the loss in average gain becomes notorious.

After this careful examination of figures 4.15 and 4.16, let us explain what has been observed. Because the LS error takes into account all the terms that

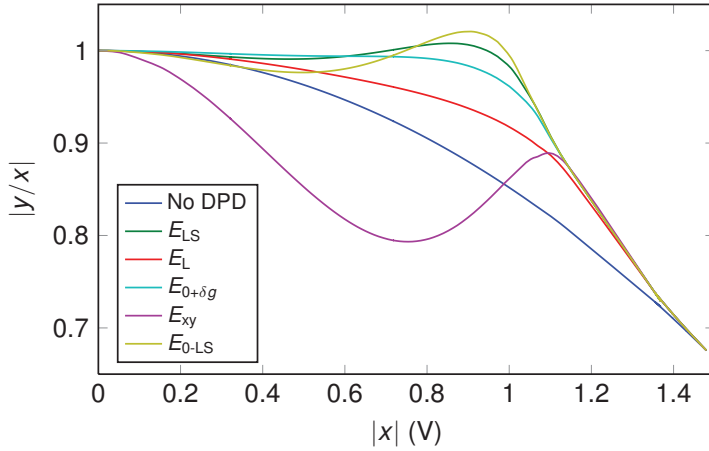


Figure 4.15: Instantaneous gain vs. instantaneous input voltage for the unpredistorted PA, and for the PA with DPD optimized for each of the measures presented in (4.48) to (4.52). The peak input voltage, x_{\max} , is fixed to 1.5 V.

contribute to different orders of nonlinear distortion, it is not surprising that it yields the lowest EVM. Since the other measures consider third and fifth order distortions, LS is not as dominant when it comes to lowest distortion power. When E_L was derived in Section 4.3.1, it was mentioned that the terms $2\Re\{C_i C_j\}$ were replaced with $2|C_i||C_j|$ to avoid negative values for E_L , and to consider the worst-case distortion power (see Section 4.3.1). That is also why there are noticeable jumps in the EVM, average gain, and distortion power curves for E_L ; because the $|\cdot|$ operator acts as a maximizing function, and is therefore discontinuous. Initially, function E_0 which is identical in structure to E_{yx} (compare (4.42) to (4.45)), was used instead of $E_{0+\delta g}$. As expected, E_0 and E_{yx} yielded almost exactly the same results. Measure E_0 was derived from (4.40) by setting $g = C_0$, which canceled the terms containing $C_0 - g$. Nevertheless, while value g is a fixed parameter, the estimated small-signal gain C_0 varies with the DPD coefficients even if the first-order DPD coefficient is fixed, and therefore the difference $C_0 - g$ changes in every iteration. That is because C_0 , C_2 and C_4 are a 5th order approximation of the DPD-PA system. If the PA is a third-order polynomial, and the DPD is a fifth-order polynomial, the composed system has an order of 15. If the input signal to the DPD has its peak above x_{sat} , then the order of the composed DPD-PA nonlinearity is even higher. In any case, a fifth order approximation results in a non-negligible error in the estimation of C_0 . Therefore, by canceling the terms that contain $C_0 - g$, the optimization process is in a sense "blinded". It becomes impossible to know at every iteration, if the system's gain is equal to the target gain. It is therefore that E_{yx} showed an uneven gain response and

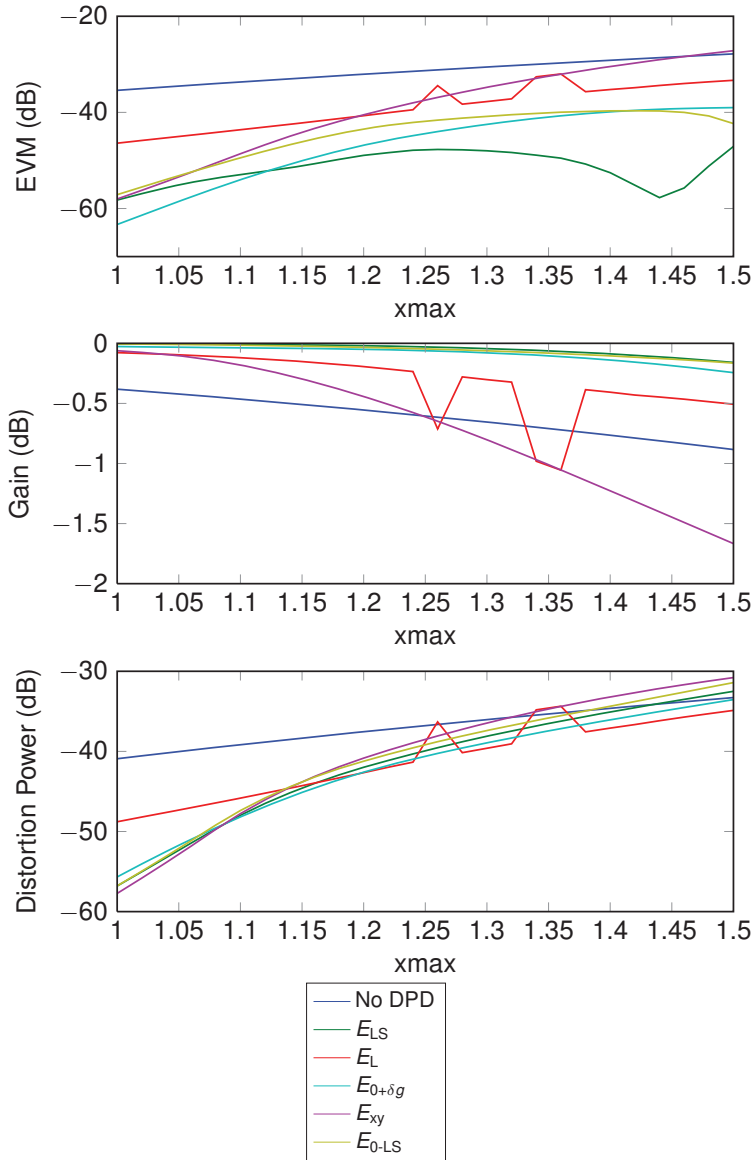


Figure 4.16: Error vector magnitude, distortion power and average gain vs. peak input voltage for the undistorted PA, and for the PA with DPD optimized for each of the measures presented in (4.48) to (4.52).

drops in average power gain. The results for $E_{0+\delta g}$ show that by adding the term $|C_0 - g|^2 w_1$, performance comparable to that of LS can be obtained.

Summary

The purpose of this section has been to present different possible nonlinearity measures that are variations of the typical least squares error. Though performance was in general best with the DPD optimized for least squares, some of the proposed measures can yield comparable results in distortion power and EVM. These measures can be used for the optimization of bias functions in regards to dynamic biasing, and for DPD optimization. Their simplified structure should make it possible to find an algorithm that requires less computational complexity than least squares.

4.8 Summary

This chapter has dealt with the formulation of dynamic biasing as an optimization problem. The constraints that were derived are useful to limit the search space, and define the search ranges for each dimension in β . The measure for dissipated power considers the output power to ensure an adequate average gain. A nonlinearity measure was presented, quite different from the usual least squares measure, that bears a physical meaning: minimize the maximum in-band distortion power relative to the in-band power. The exponential structure that unites the nonlinearity and dissipated power measures makes it possible to find regions for a good compromise between linearity and dissipated power.

Though the class-A sets a high reference point for linearity, in the case of the pHEMT one of the solutions yielded an ACPR even lower than the class A mode. This shows the potential of dynamic biasing as a linearization method. From the different cases it is clear that PAE can be even more than three times as high with optimized dynamic biasing.

Alternative measures for nonlinearity have been presented based on the concept of reducing distortion power at the adjacent and alternate channels. These measures have a simple structure and take into account the phase of the nonlinear distortion coefficients. By means of a simulation example, it was shown that performance comparable to that of least squares is attainable.

In the next chapter, the optimization method based on random search is extended so that it runs based on experimental data only, and the optimization results obtained in this chapter are validated.

Chapter 5

Measurement of different device technologies

This chapter presents experimental results that validate and extend the methodology described in Chapter 3 and Chapter 4 to measurement-based optimization.

Three devices were measured: the HBT MMIC transistor (chapters 3 and 4), a 10-W GaN amplifier, and a 2-W GaAs amplifier. A number of bias functions were tested on each device aiming either at enhancing efficiency, linearity, or output power; or to find a suitable trade-off between the three. For the GaN and GaAs amplifiers, the bias functions were found using random search based on purely experimental data, and included the possibility of clipping the bias waveforms. For the HBT transistor, the main bias functions were found in Chapter 4 using optimization based on single-tone data.

The chapter begins by explaining the automated measurement setup, and the modifications to the optimization method from Chapter 4. Some necessary terminology (such as “auxiliary envelope tracking”) is explained before presenting the experimental results. A detailed summary of the results closes the chapter, together with conclusions about the performance of each device for the different dynamic bias biasing configurations (i.e., only dynamic gate biasing, only dynamic drain biasing, dynamic gate and drain biasing, and static biasing).

Table 5.1 highlights some important characteristics of the devices that were tested.

5.1 Methodology

The details around the implementation of dynamic biasing and the measurement system for the different amplifiers are next described.

Table 5.1: Specifications (as provided by the manufacturer) and design characteristics of the three measured devices. (1) GaN: values correspond to the saturation output power at $V_D = 28$ V, $I_D = 200$ mA. (2) GaAs: values correspond to 1-dB compression. (3) HBT $3 \times 3 \mu\text{m} \times 50 \mu\text{m}$ transistor: values correspond to linear operation (i.e., below 1-dB compression); matching for maximum output power is assumed. Notation: f_c is the center frequency, I_D the drain bias current, $I_{D,\text{max}}$ is the maximum drain current for reliable operation. Subindexes *spec* and *op* refer to data specified by the manufacturer, and to values at which the device actually operates in the measurement results, respectively. Hence, $I_{D,\text{op}}$ is the biasing current in static biasing conditions.

	<i>Specifications</i>			<i>Design</i>				
	Output power (dBm)	PAE (%)	Gain (dB)	$I_{D,\text{spec}}$ (mA)	$f_{c,\text{spec}}$ (GHz)	$I_{D,\text{max}}$ (mA)	$I_{D,\text{op}}$ (mA)	$f_{c,\text{op}}$ (GHz)
HBT	20	33	19–21	55	1.9	90	55	1.9
GaAs	33	50	14	350	1.8	1150	100	2.4
GaN	41	62	13.8	200	2.0	1500	160	2.4

5.1.1 Measurement setup

The measurement setup is automated, as shown in Figure 5.1. The RF and bias waveforms are generated from the computer and uploaded into the Rohde & Schwarz SMU200A signal generator. The RF signal is output through the A port of the signal generator, while the bias signals are output through the B port using the I/Q outputs at the back, with a maximum amplitude of ± 1 V. The gate and drain trackers amplify and offset these signals to the levels required by the device under test (DUT).

The instantaneous drain bias voltage and drain bias current are measured with the Agilent MSO9254A oscilloscope. The Rohde & Schwarz FSQ40 signal analyzer, connected to the output of the amplifier, measures the power at the fundamental, adjacent and neighbor channels; as well as the I and Q components of the output signal around the fundamental (i.e., the gain and phase-shift characteristics).

The bias is fed in to the HBT transistor through bias tees at the base and the collector. Since two prototypes of the drain tracker were built, one of them was used as a constant current source by setting a large resistor at its output (10 k Ω).

The gate and drain trackers were directly connected to the biasing networks included in the GaAs and GaN amplifiers. The shunt capacitors between DC and ground were removed, as the trackers themselves provided the low output impedance required for stable biasing [63]. Without these capacitors the amplifiers may be unstable if connected to a DC power supply, therefore the trackers were also used for static bias measurements.

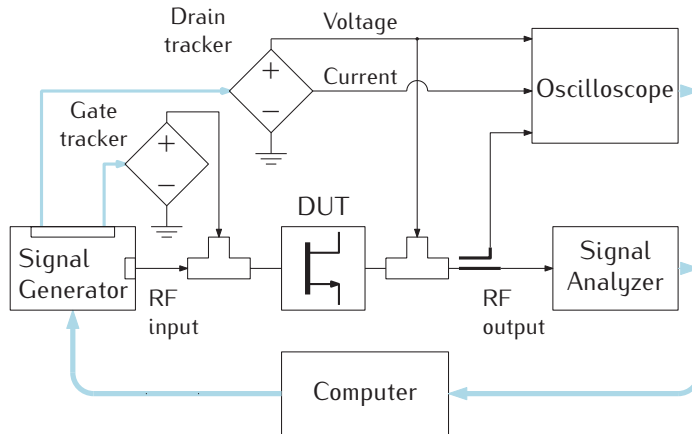


Figure 5.1: Simplified diagram of the measurement setup used to test dynamic biasing on the HBT, GaAs and GaN devices. A buffer amplifier was used with the GaN amplifier.

The dynamic bias sources

Building a highly efficient wide bandwidth bias source is a subject of current research, as it is a complex task, and is out of the scope of this work. The bias sources that were built for this measurement system were linear amplifier solutions based on operational amplifiers (op-amp) [72],[73] and a 1.1-A current feedback amplifier to provide the large currents required at the drain [74]. For the schematics for the gate and drain trackers refer to Appendix C. Because the gate bias functions can also be quadratic with input power, the operational bandwidth of the gate tracker must be twice that of the drain tracker. That is why different op-amps are used for the gate and the drain, with different gain bandwidth and slew rate specifications.

The drain tracker design was challenging because of the difficulties involved in the drain bias current measurement. Two drain tracker prototypes were thus built. The specifications for the gate and second prototype of the drain tracker are summarized in Table 5.2. The voltage at the trackers' input from the signal generator is effectively in the range of -0.35 V to 0.35 V , so the trackers' circuitry includes gain and offset mechanisms to output gate and drain voltages at the levels required by the DUT (a single-tone signal can be used for voltage range calibration). The output of the drain tracker ranges from 1 V to 29.5 V , and is limited by the DC input voltage ($\pm 18\text{ V}$). If the peak output voltage is 28 V , however, the minimum output voltage will then be 8 V (Table 5.2, maximum voltage swing). This limitation is imposed by the slew rate of the op-amp at the maximum frequency (5 MHz).

To measure the instantaneous bias current at the drain, the simplest would be

to set a small resistor at the output of the drain tracker, and measure the voltages drop across the resistor using two oscilloscope probes. Unfortunately common mode error would render the measurement inaccurate. That is why two different drain trackers were constructed. The first one used a transformer to split the DC component from the AC component of the drain bias waveform. The transform acted as a bandpass filter with a passband between 0.05 MHz to 5 MHz. The main problem was that for output voltages greater than 8 V, the transformer would cause nonlinear distortion. The second prototype utilizes a 2- Ω resistor at the output to measure the current. The resistor is included in an op-amp feedback loop to prevent the voltage bias from swinging with the current (Figure C.4). The Agilent N2792A differential probe was used to measure the voltage drop across the resistor. Refer to Appendix C for more details.

The test signal

The test signal is a 16-QAM signal, filtered with a root-raised cosine (RCC) filter with 0.22 roll-off factor, and a symbol rate of 1 MHz. The signal is pseudorandom, with 1024 symbols and a peak-to-average power ratio of 6.5 dB. If the desired channel is defined as a 1-MHz channel centered around the carrier frequency, the upper and lower adjacent channels are 1-MHz channels centered 1.22 MHz to the the right and left of the desired channel, respectively; and the upper and lower alternate channels are centered 2.44 MHz to the right and left of the desired channel, respectively. For the sake of simplicity, the adjacent channel power ratio is referred to as ACPR3, and the alternate channel power ratio as ACPR5, analogously to the “IM3” and “IM5” denomination for third and fifth order intermodulation products for two-tone signals. The adjacent channel power ratio of the lower/upper channel is represented as ACPR3-L/U, while the alternate channel power ratio of the lower/upper channel is represented as ACPR5-L/U.

Table 5.2: Specifications for the gate tracker, and the second prototype of the drain tracker. The maximum operation frequency is f_{\max} .

Specification	Gate	Drain	Unit
Maximum voltage input to the tracker	± 0.35	± 1	V
f_{\max}	4.5	5	MHz
Output voltage range	-3 to 0	1 to 29.5	V
Maximum voltage swing	2	20	V
Maximum output current	0.25	1	A
Voltage variation with load (50 Ω to 200 Ω)	0.5	0.5	dB
Voltage variation with frequency (DC to f_{\max})	1	1	dB

5.1.2 Sources of measurement error

The cable losses from cables and connectors was compensated with power measurements using a power meter. There is, however, some uncertainty on the input power to the amplifier depending on the response of the signal generator, and on the linearity of the buffer PA (for the GaN PA), which affects the measurement of the average gain for modulated signals. The measurement on average gain is thus limited to the accuracy of the SMU200A signal generator.

The power at the main channel and adjacent and alternate channels was measured using the integration bandwidth method [75]. According to the characteristics of the modulated signal, and to the span and sweep time settings for the signal analyzer, the repeatability error for the power measurements with 95-% confidence was estimated to be ± 0.3 dB.

The current measurements were calibrated by measuring the instantaneous drain and current waveforms at different fixed resistors with known values ($50\ \Omega$, $100\ \Omega$, and $200\ \Omega$). The differential probe provides 60 dB of common mode rejection rate, but the remaining common error can affect the current measurement. The impact on the calculation of PAE was estimated to be no greater than 3 %.

5.1.3 Optimization of the bias functions

Random search optimization is used, as in Chapter 4, to experiment with different biasing functions for each device.

There are many similarities with the method presented in Chapter 4. Random search is again used to solve the optimization problems, and the bias functions are once again formulated as polynomial functions of the input power (see (4.1)). In this chapter we add the possibility of clipping the gate/drain bias waveforms at the higher and lower ends, and to choose at which input power level relative to the peak will the upper/lower clipping occur (e.g., Figure 5.6). This expands the degrees of freedom of the optimization problem from five to ten, though in some cases only one degree of freedom is optimized while the others are fixed. In most of the cases, the “pure” polynomial expressions from (4.1) are used, but drain clipping at the higher end, however, will be shown to be useful for the GaAs and GaN amplifiers.

For the HBT, the optimization was carried out from simulation data as described in Section 4.5.2. The nonlinearity measure, (4.25), is presented again for the sake of convenience:

$$L = \frac{|C_4|^2 w_5 + 2|C_4 C_2| w_4 + (|C_2|^2 + 2|C_4 C_0|) w_3 + 2|C_2 C_0| w_2}{|C_0|^2 w_1}. \quad (5.1)$$

Nonlinearity measure L enjoys an aesthetic appeal in its simplicity. It aims at minimizing third and fifth order in-band distortions while maximizing linear channel power. A similar measure for nonlinearity is used for the measurement-based

optimization of GaAs and GaN transistors. Given a RRC filter with a roll-off factor α , and a modulated signal with symbol rate SR, the nonlinear power (P_{NL35}) is defined as the power in a bandwidth of 2SR that is $\text{SR} + \alpha$ away from the center of the desired channel. The nonlinearity measure is defined as the ratio of P_{NL35} to the power in the desired channel over bandwidth SR, P_{channel} . That is

$$L = \frac{P_{\text{NL35}}}{P_{\text{channel}}} \text{ for GaN and GaAs amplifiers.} \quad (5.2)$$

In a physical sense, this is approximately equivalent to measuring the sum of adjacent channel power and the alternate channel power divided by the power in the desired channel.

For the HBT, the biasing paths resulting from the optimization algorithm described in Chapter 4, are used as a starting point for other cases, i.e., dynamic gate bias with static drain bias, and dynamic biasing for maximum output power. For the GaAs and GaN pHEMTs, random search is also used, but applied directly upon measurement data. Instead of using a joint error function as in (4.15) to optimize two subfunctions, namely linearity and dissipated power, only one quantity is optimized at the time, while limit constraints are set on the other one. For example, if the goal is to linearize, then measure L is minimized, and constraints are set on the minimum possible values of PAE and gain. If the goal is to reduce power consumption, then the optimizer seeks to maximize PAE, and constraints are set for linearity L and the gain. Though the measure for power consumption for the HBT was the average dissipated power divided by the average output power, PAE is the power-consumption measure to maximize for the GaAs and GaN amplifiers, and it is also used for performance comparison.

5.1.4 Performance comparison

Regardless of the device being measured, the amplifier's performance with dynamic bias is always compared against a reference point—the performance with static bias operation at the design bias point—. The comparison is in terms of ACPR3, ACPR5 (for the GaAs and GaN transistors), gain, and PAE. The amplifier is driven to the same output power in both cases.

In some cases, overlapped gain curves are presented to clarify how dynamic biasing improved or failed to improve linearity. When continuous gain curves are shown for measurements with the modulated signal, they are actually polynomial fits of 9th order from the measured gain response. This is done because the gain data points can present strong spreading spanning even several decibels, which would make the comparison of gain/phase response confusing.

It is important to clarify that it is solely with illustrative or explanatory purposes that gain or phase responses are used. The preference for a set of bias functions over another is based on the variable being optimized (i.e., measure L or PAE), not on the gain or phase variations over the power range, as was the case of the point-search algorithm in Chapter 3.

5.1.5 Auxiliary envelope tracking for linearization

In the experiments carried out with the GaAs and GaN transistors, sections 5.3.3 and 5.4.3 emulate a technique denominated auxiliary envelope tracking (AET), first presented by Yusoff and the Centre for High Frequency Engineering at Cardiff University [76],[77].

AET varies the drain bias voltage—as in envelope tracking (ET)—, but the fundamental difference between conventional ET and AET is the mechanism of generating the drain modulated bias signals. In AET, the DC and AC components of the drain bias signal are generated separately, and then combined to form the full drain bias signal that is applied to the PA. In ET, the amplification of both DC and AC components of the bias signal is handled by the envelope amplifier, or tracker unit.

The AET system provides a reduced-range tracking supply; the amplitude range of the AC component of the drain bias signal is small compared to the DC component, especially for signals with high crest factor. This allows AET to be efficiently implemented with low cost and low complexity, resulting in high overall system efficiency. An RF broadband transformer can be used as a combiner, and the envelope amplifier can be a transistor in source-follower configuration. Thus another important difference with ET is that the drain bias does not follow the envelope down to the lowest levels.

AET in itself is a linearity enhancement mechanism, and is not intended to be combined with predistortion or other linearization techniques. There are two principles on which linearization through AET may be achieved.

- *The “gain expansion” characteristic of GaN devices.* Yusoff states that for a GaN device, the power gain increases exponentially with drain bias voltage, assuming a fixed quiescent current [76]. Hence for a higher drain bias both small-signal and saturation gain are higher, which can be used to flatten the gain response with appropriate selection of the drain bias.
- *Reducing compression through higher biasing.* In general, if the drain bias is increased in a device when the input envelope (or power) is near compression, the clipping of the load voltage waveform will be reduced, reducing nonlinear distortion. However, bias can not be increased indefinitely because of excessive heat accumulation at the transistor, and if the load waveform reaches breakdown, there may be irreversible changes in the device’s properties. In both cases the device may be permanently damaged. The advantage with high-PAPR modulated signals is that input power peaks occur infrequently, so that bias could be increased over normal operation for short periods of time for peak amplification only, as verified from the results in Section 5.2.3.

To round up the discussion: AET is a linearity enhancement method that can also lead to efficiency enhancement. The AC drain bias voltage that swings on the fixed DC level can be thought of as a small *perturbation*. In the context of

this work the perturbation follows the power of the input signal. Linearization can be achieved by setting the DC level at the “usual” fixed bias level, which implies that higher voltage is applied at high input power peaks, thus linearizing near compression. This work is not concerned with the physical separation of AC and DC bias components, but on the linearization principle mentioned before. Different AET cases were tried on the GaAs and GaN amplifiers, and the results are presented in sections 5.3.3 and 5.4.3. A similar experimental study was carried out for the HBT transistor (Section 5.2.3). The test cases include testing AET on its own, and combining it with dynamic gate biasing to improve performance further. Also, for the GaN amplifier, a similar terminology, auxiliary gate tracking (AGT), is used to refer to small perturbations on a constant DC gate bias voltage that are mainly used to linearize the GaN amplifier when operating in deep AB and B modes (Section 5.4.1, Section 5.4.3).

A note on the terminology to be used throughout the chapter:

- *Auxiliary gate tracking* refers to dynamic gate biasing with small voltage variations that results in the PA operating at the same quiescent current level as in static bias mode near compression.
- *Envelope tracking* refers to dynamic drain biasing with static gate biasing, following *input power*, unless specified otherwise.
- *Auxiliary envelope tracking* refers to envelope tracking with reduced voltage swing (i.e., not going all the way down towards the knee voltage).
- *Dynamic biasing* refers to full tracking at both gate and drain as a function of input power.

5.1.6 More terminology

The terms gate bias and drain bias are used by default, but depending on the context they may apply to the base and collector biases of the HBT transistor, respectively. The drain/collector bias current is represented as I_D/I_C . The drain/collector bias voltage as V_D/V_C , and the gate bias voltage/base bias current is represented as V_G/I_B . When presenting measurements for a modulated signal, the term output power (for example in a figure label) refers to the average output power level, unless specified otherwise.

5.2 HBT

This section presents measurements for the 20.5-dBm HBT transistor utilized in Section 4.5.2, where an optimization algorithm based on single-tone simulation data using random search (RS) was used to find two biasing functions—labeled

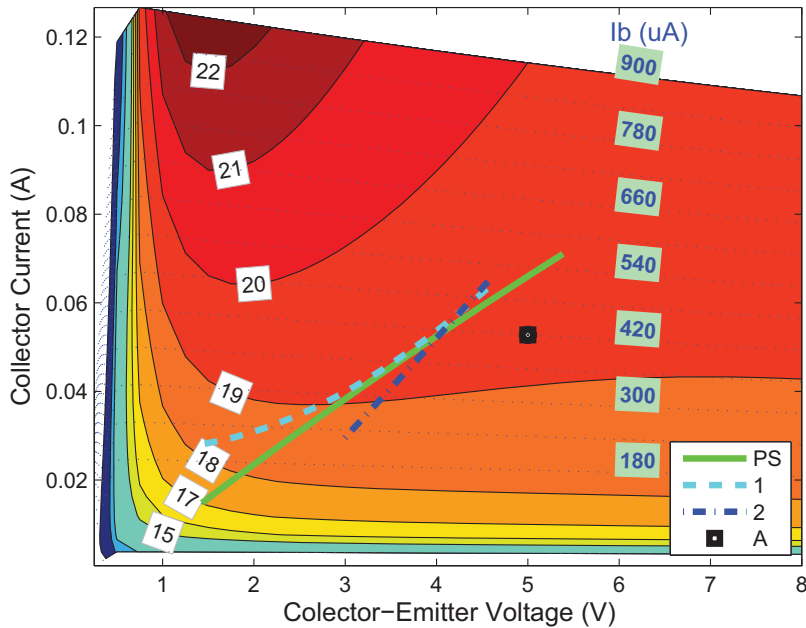


Figure 5.2: Optimized dynamic bias paths in the I–V plane for the HBT transistor.

“1” and “2”—. These functions were compared against a solution from the point-search algorithm described in Section 3.6 labeled “PS”, and against the class-A static bias case, labeled “A”. The four bias paths as shown in Figure 4.7 are presented again in Figure 5.2 for the sake of convenience.

Section 5.2.1 presents a comparison of measured and simulated results in terms of ACPR3 and PAE for the four paths. In subsection 5.2.2, solution “2” is used to bias dynamically the base with the drain bias fixed to 5 V; while in subsection 5.2.3, maximum output power—higher than that attainable with static bias—is achieved using full dynamic biasing [68].

5.2.1 Measurement of the biasing paths obtained through optimization and simulation

Figure 5.3 highlights the good agreement between measured and simulated results for ACPR and PAE for the different biasing paths. Path “2” doubles class-A efficiency with a slight diminishment in linearity, while “PS” and “1” are thrice as efficient, at the expense of some dBs in ACPR.

These results are of high value because they validate the methodology to select the biasing functions used throughout chapters 3 and 4, which was based on quasi-

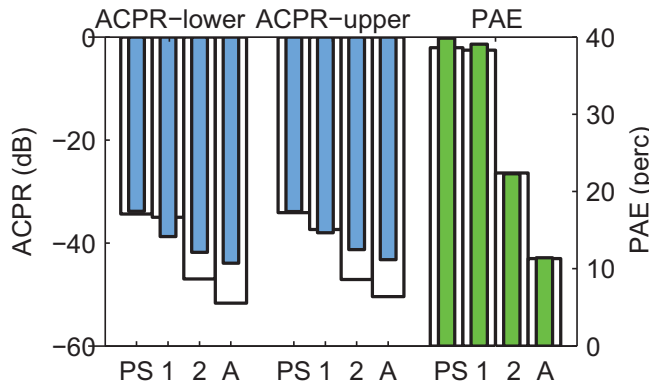


Figure 5.3: HBT transistor at 14.8-dBm average output power: comparison of simulated and measured (lower and upper) ACPR3 and PAE for the four biasing cases shown in Figure 5.2. Case “PS” corresponds to the bias functions found with the point-search algorithm (Section 3.6), while cases “1” and “2” were found using random search optimization as described in Chapter 4.

static modeling from single-tone simulations.

As discussed in Section 3.5, the thermal time constant of the HBT device is small enough to reach 1-MHz frequencies, given that the symbol rate is also 1 MHz, the fact that the single-tone simulations took self-heating into account contributed to the accuracy in the selection of the bias paths. The simulated results in Figure 5.3 come from a new simulation for the selected test cases with dynamic biasing. The simulation does consider memory and includes a model for self-heating effects.

There are some discrepancies around simulated and measured data for ACPR3 that are mainly attributed to the nonlinear behavior of the collector tracker. The tracker uses a high-frequency transformer to split the DC and AC components of the collector biasing signal, but is sensible to nonlinear effects as the amplitude of the AC component increases. (That was actually why another tracker prototype was built.) Small differences in measured vs. simulated ACPR3 are also observed for static bias, case “A”, because the tracker was connected for all biasing cases. What is most valuable is that the simulated data correctly predicts the tendency in ACPR3, particularly respect to static bias operation (case “A”). For PAE, measured and simulated results match extremely well.

Another set of measurements was carried out for an output power of 16 dBm for the same biasing cases. Once again paths “PS” and “1” present the highest PAE; 40.1 % and 42.9 %, respectively; and ACPR3 is below -37.0 dB for both of them. Case “2” beats static biasing with an ACPR3 of -42.9 dB compared to -42.2 dB, and a PAE of 32.0 % compared to 14.8 %. That means that with dynamic biasing

we can improve PAE by 15 points with slightly better ACPR3, or win 28 extra PAE-points at the cost of a 4-dB degradation in ACPR3.

5.2.2 Dynamic variation of the base bias only

By using the same base bias function as in solution “2”, and keeping the collector bias fixed to 5 V, we obtain the results in Figure 5.4. The figure shows that when the average output power is 16.0 dBm, ACPR3 is the same for dynamic base biasing and for static biasing, but PAE is 13 points higher for dynamic base biasing. There is a “sweet-spot” at an output power of 16.9 dBm, where the highest ACPR3 is -42.19 dB and the PAE is 34.4%. Comparing dynamic base biasing against class A for a constant ACPR3 level of -42 dB, we have that PAE increases from 14.8% to 34.4% with dynamic base biasing—a 20-point advantage—while the average output power is almost 1 dB higher with dynamic base biasing. Since the transistor was not measured in class A operation at exactly the same output power, it is difficult to say what would be the benefit in ACPR3 at 16.9 dBm, where the sweet-spot occurs. At the highest average output power level ACPR3 can be half that of the class-A case, while PAE is 8 points higher. Dynamic base biasing alone can therefore give an advantage both in ACPR3 and PAE along the average output power range.

5.2.3 Dynamic biasing for maximum output power

In this scenario, the base current varies linearly between 240 μ A to 520 μ A, while V_C varies between 2 V to 7 V. The input power is increased in steps of 1 dB. What is interesting in Figure 5.5 is how high the output power is for DB at the last point in the curve. It reaches in fact the 1-dB static single-tone compression point, 21 dBm. In class A mode, the PA is driven with $I_B = 520$ μ A, and $V_C = 7$ V. For an output power of 19.8 dBm it yields almost the same ACPR level as DB at 19.5 dBm, while the PAE is 5.7 points lower. When the input power for the class-A was increased to obtain an output power of 20.30 dBm to compare it with DB, the transistor burned out. This illustrates another feature of dynamic biasing: the capacity of driving the transistor to higher output power levels given that the PAPR of the modulated signal is “large”. In this case, the maximum average output power that could be obtained with dynamic biasing was 1.3 dB higher than with static biasing.

5.2.4 Discussion

The beauty of this experiment is that it shows how the simulation and optimization carried out in Chapter 4 achieved its goal:

1. To find biasing paths for different purposes (e.g., maximum PAE enhancement, “1”, or best possible linearity together with PAE enhancement, “2”).

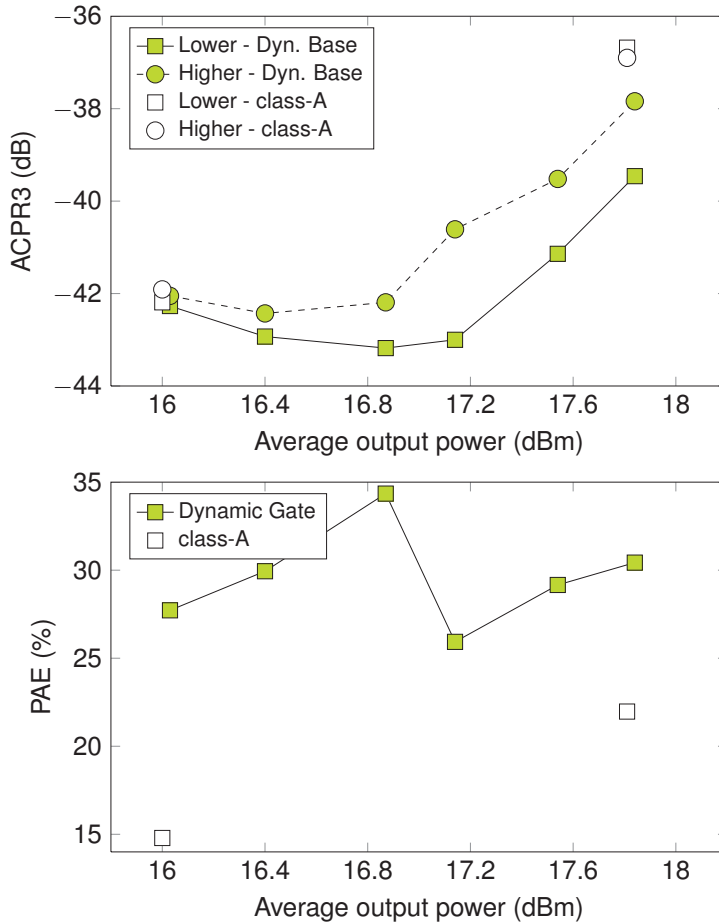


Figure 5.4: HBT transistor: comparison of ACPR and PAE for dynamic base biasing with a collector bias fixed at 5V against the class-A. The average input power is increased in 0.5 dB for each point in the dynamic base biasing curves.

2. To provide an estimate of ACPR3 and average PAE (or dissipated power) that is consistent with measured data, especially compared to the static bias case.

Regarding the bias paths obtained through optimization, Figure 5.3 showed that solution “2” is a good bet if we are after linearity levels close to class-A performance with twice as much efficiency. If the priority is to enhance PAE as much as possible even at the expense of linearity, then both “PS” and “1” are suitable, though “1” presented nearly 5 dB less distortion than “PS” at the lowest output power level.

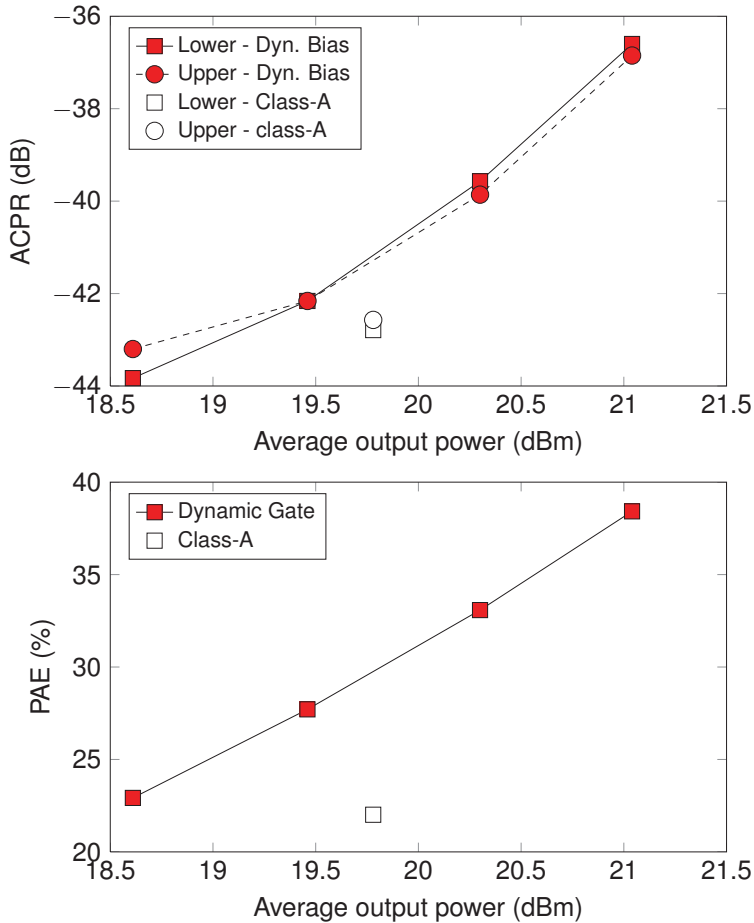


Figure 5.5: HBT transistor: Comparison of ACPR3 and PAE for dynamic bias for maximum output power against the static bias case.

Section 5.2.2 showed that dynamic base biasing alone can improve PAE by as much as 13 points and that at high output powers, ACPR3 can be maintained below that of class A and still win 8 points in PAE. The advantage of such a solution is that it can manage higher RF bandwidths, since the current at the base is low compared to the current at the collector, which in turn reduces the circuit complexity, and therefore the implementation cost.

Another exciting result was using dynamic biasing to drive the HBT transistor as hard as possible. The maximum average output power achieved with dynamic biasing was 21 dBm. That is very high considering that the 1-dB compression

point for continuous wave is also 21 dBm, and that the PAPR of the test signal was 6.5 dB. With static bias, the transistor could be driven only 1.3 dB below this power level. A study of the impact that such hard operation would have on the transistor’s lifetime could be subject for future work.

5.3 GaAs pHEMT

A 2-W GaAs power amplifier using the FPD2000AS AlGaAs/InGaAs pHEMT transistor by RFMD was measured [78]. Static bias measurements for the amplifier in class AB with a drain bias current of 100 mA are compared to dynamic biasing in different scenarios. The first one is envelope tracking, where the drain bias is varied first linearly as a function of input power, and then clipping is applied as shown in Figure 5.6. The other scenario is auxiliary envelope tracking (AET), described in Section 5.1.5. Yusoff et al. studied AET for a 2-tone signal [76]. The envelope of the signal, that is, the bias stirring signal, was emulated using a sinusoidal signal, so the drain bias was actually varied as a function of input power—as has been done throughout this work. To observe the impact that adding dynamic gate biasing has in third and fifth order distortions and in PAE, both ET and AET are tested with static and dynamic gate voltage. The measurements were taken for an average output power values of 28, 29 and 30 dBm.

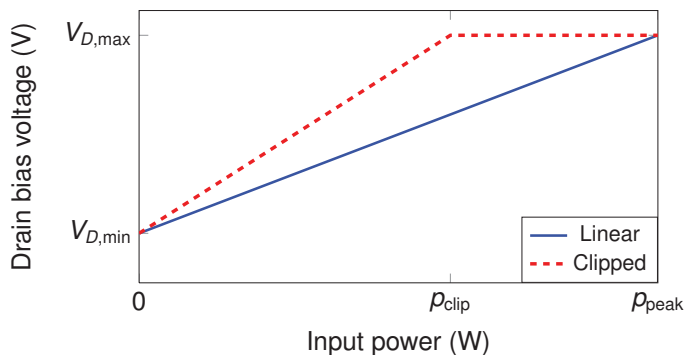


Figure 5.6: Drain bias voltage vs. normalized input power with upper clipping of the drain bias waveform. Variable p_{peak} is the peak input power, p_{clip} , the input power level at which the drain voltage is clipped; V_{min} and V_{max} are the minimum and maximum drain bias voltages, respectively.

5.3.1 Dynamic gate bias

The motivation for experimenting with dynamic gate bias only, while holding the drain bias fixed becomes clear from Figure 5.7. Increasing the gate bias voltage

to allow higher drain bias currents increases the gain of the transistor because transconductance is increasing with the bias current. This applies even at power levels close to peak envelope power and can be used to “smoothen out” compression by making $V_G(p)$ a parabola facing upwards as shown in Figure 5.8.

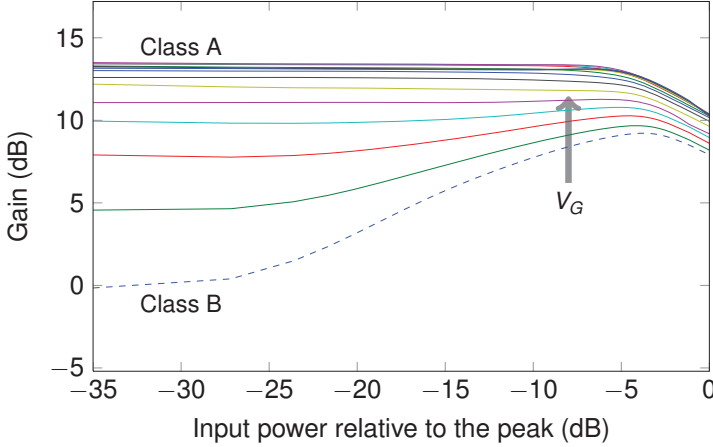


Figure 5.7: GaAs amplifier: fit of the gain vs. relative input power sweeping the static gate bias, V_G , with the drain bias fixed at $V_D = 10$ V. The lowest V_G value corresponds to class B operation ($I_D = 20$ mA) and the highest values to class A operation ($I_D = 500$ mA). The maximum drain current $I_{D,\max} = 1150$ mA. The input signal is the QAM signal from Section 5.1.1 with a peak input power of 23.8 dBm and an average input power of 17.1 dBm.

Table 5.3 shows the result of testing the gate bias path in Figure 5.8 with a static drain bias of 10 V, for average output powers of 28 dBm and 29 dBm. There are three main scenarios to consider:

1. *Constant 28-dBm average output power*, which yields a 6-dB improvement in ACPR3, and a 4-point increase in PAE.
2. *Constant average output power of 29 dBm*, for which ACPR3 improves by a little more than 3 dB, the gain increases 0.5 dB, and the PAE maintains the same level.
3. *Constant ACPR3 at -42 dBm*, for which we observe a 1-dB increase in average output power, and 11 extra points in PAE.

5.3.2 Envelope tracking and dynamic gate bias

When using envelope tracking, i.e., varying only the drain bias as a function of power, the gain can be dragged to unsuitably low levels if the minimum voltage of

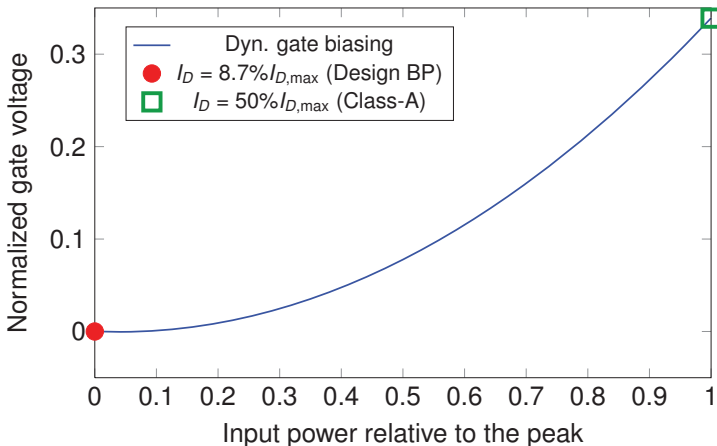


Figure 5.8: An example of dynamic biasing at the gate with the drain bias voltage fixed to 10 V. The device operates at its design bias point at zero relative input power, and reaches class A operation at a relative input power of 1. ($I_{D,\max}$: maximum drain current.)

the drain bias, $V_{D,\min}$ (Figure 5.6) is too low. This is illustrated in Figure 5.9.

For the lowest curves, those with $V_{D,\min} \leq 3.8$ V, the RF drain voltage waveform is clipped hard because the drain bias varies as a quadratic function of the RF envelope. For the upper curves, the drain bias voltage variation is very small, which means that the transistor's average efficiency is reduced, so its temperature is higher at low input power levels. Since $V_{D,\max}$ is fixed, one would expect all of the curves to converge when the input power relative to the peak is 0 dB, however the curves for $V_{D,\min} \leq 4.6$ V never reach the same point as the other curves. This behavior is attributed to memory effects resulting from the heavy clipping at large input power back-off.

Table 5.3: GaAs transistor: comparison of dynamic gate biasing with static gate biasing for an average output power of 28 dBm and 29 dBm. The drain bias for both cases is fixed at 10 V. The input is a 16-QAM modulated signal. (ACPR3-L/U: lower/upper ACPR3. ACPR5-L/U: lower/upper ACPR5.)

	Po (dBm)	Gain (dB)	ACPR3-L (dB)	ACPR3-U (dB)	ACPR5-L (dB)	ACPR5-U (dB)	PAE (%)
Static	28.1	12.0	-42.3	-42.7	-71.4	-71.6	32.2
	29.1	11.8	-38.7	-39.1	-62.1	-61.7	43.1
Dyn.G	27.9	12.3	-48.6	-48.2	-64.4	-64.4	36.9
	29.1	12.3	-42.5	-42.8	-61.4	-60.7	43.9

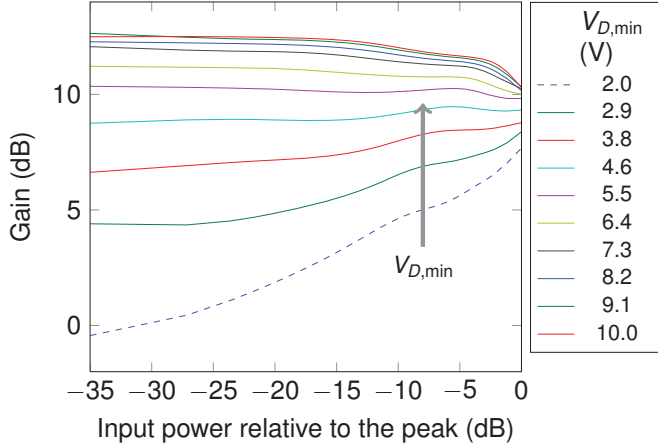


Figure 5.9: GaAs amplifier: fit of the gain vs. relative input power sweeping the minimum ET voltage, $V_{D,\min}$, from 2 V to 10 V without clipping V_D ($p_{\text{clip}} = p_{\text{peak}}$). At 0-dB relative input power the drain bias is 10 V for all curves, thus ideally all of the curves would intersect at peak input power. The gate voltage is fixed for a current of 100 mA, and the input signal is the 16-QAM signal from Section 5.1.1. The peak input power is 23.3 dBm, and the average input power is 16.6 dBm.

Another parameter that can be used in the drain bias waveform is p_{clip} , the input power level relative to the peak at which the drain bias voltage reaches its maximum. If the input power increases above that level, the drain bias remains unchanged at the maximum. Figure 5.10 shows how higher gains can be achieved at higher input power levels by adding clipping to the drain voltage waveform. Because the drain bias varies from 2 V to 10 V for all cases, the gain is very low at low input power levels.

Figures 5.9 and 5.10 were measured from a device that burned out due to inadequate cooling. A new device with similar characteristics—except for a slightly higher gain—was soldered to the PA hardware. Taking similar measurements to those from figures 5.9 and 5.10, it was decided to vary the drain bias voltage from 4.9 V to 10 V, and to set p_{clip} to $0.65p_{\text{peak}}$ for measurements with average output powers of 29 dBm and 30 dBm. Figure 5.11 presents the results for the different cases for ET, with static and dynamic gate biasing.

For the lowest output power level, 28 dBm, there is a 3-dB linearity improvement combining ET with dynamic gate biasing (\diamond) respect to only using ET (\blacksquare). The improvement respect to the static biased class-AB (\ominus) is of 1.3 dB in ACPR3, and the gain is the same. Using ET with fixed gate yields 25 extra PAE points respect to the class-AB, while using ET with dynamic gate yields 19 extra PAE points. Using dynamic gate maintains ACPR5 at the same level as for the class-

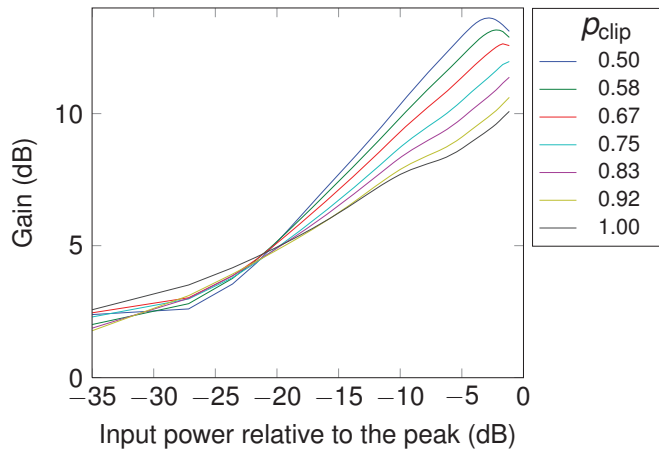


Figure 5.10: GaAs amplifier: fit of the gain vs. input power relative to the peak (p_{peak}). The power at which the drain bias voltage is clipped is swept, p_{clip} , is swept from $0.5p_{\text{peak}}$ to $1.0p_{\text{peak}}$. The drain bias voltage varies from 2 V to 10 V for all curves. The gate bias voltage is fixed for a current of 100 mA. The input is the 16-QAM signal from Section 5.1.1. The peak input power is 23.3 dBm, and the average input power is 16.6 dBm.

AB, approximately -60 dB, while using only ET deteriorates ACPR5 by a little more than 1 dB.

When the average output power is increased to 29 dBm, nonlinear distortion becomes very high for ET (\blacksquare) with ACPR3 reaching almost -34 dB, and adding dynamic gate biasing (\blacklozenge) does not reduce the distortion. It is then that clipping the drain bias waveform comes in handy, since ACPR3 for ET with drain bias clipping becomes lower than that of the static bias case both for fixed and dynamic gate biasing (\blacktriangle and \blacklozenge , respectively). The PAE is also the same for both of these cases (58.6%) which means 20.5 extra points in PAE compared to static biasing (\ominus).

For the maximum output power, 30 dBm, ET with drain bias clipping and dynamic gate biasing (\blacklozenge) yields a maximum ACPR3 of -38.6 dB with a PAE of 61%, that is 16 points higher than that of the static biased class-AB amplifier (\ominus) with more than 1-dB improvement in ACPR3.

Comparing for a constant ACPR3 of approximately -41.7 dB, ET with dynamic gate bias and clipping at the drain bias (\blacklozenge) achieves 1 dB higher average output power (29 dBm), and 15 extra PAE points (58.7%) than the static bias case (\ominus). Using ET and dynamic gate biasing, ACPR3 can be improved by 1 dB to 2 dB. For the same output power level it can improve efficiency by more than 20 points. That is especially clear at the lower output power levels (i.e., 28 dBm

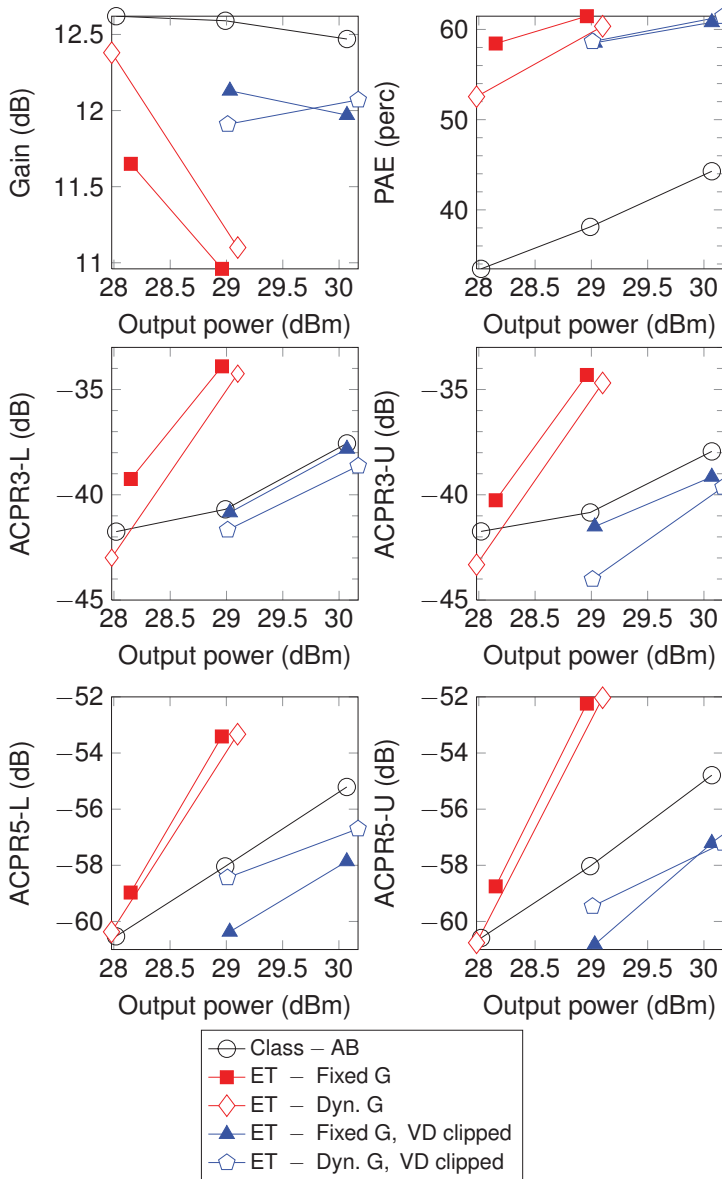


Figure 5.11: GaAs amplifier: comparison of the different envelope tracking cases in terms of gain, lower/upper ACPR3 (ACPR3-L/U), lower/upper ACPR5 (ACPR5-L/U) and PAE for different average output power levels.

and 29 dBm) (-■- -◇-).

5.3.3 Auxiliary envelope tracking

For auxiliary envelope tracking, the drain bias voltage varies in two different ranges: between 8 and 11 V, and between 7 to 12 V. Both cases were measured with static and dynamic gate bias, for average output power levels of 28 dBm, 29 dBm and 30 dBm (Figure 5.12).

For an average output power of 28 dBm, ACPR3 improves by 2.25 dB with AET from 8 V to 11 V and fixed gate (-◇-) respect to the static bias class-AB case (-○-). For AET from 7 V to 12 V with fixed gate (-▲-) it is almost 5 dB better. There is a 4.5 to 6-point improvement in PAE for both cases.

For an output power of 29 dBm there is a 1.5-dB improvement for AET from 8 V to 11 V with fixed gate bias (-◇-). Adding dynamic gate bias ACPR3 can be 3 dB better than the static-bias PA (■). However, AET from 7 V to 12 V with fixed gate bias is the best (-▲-), since ACPR3 is approximately 4 dB better than the static-bias PA. The improvement in PAE is again modest: between 5 to 7 points for all cases.

For an output power of 30 dBm, AET from 8 V to 11 V (-◇-) reaches -38 dB in ACPR3, the same result as with ET with dynamic gate biasing and clipping of the drain bias voltage (refer to Figure 5.11, -◇-). Though the -◇- case of ET in Figure 5.11 yielded higher PAE by 11 points, PAE for all AET cases is still 5 points better than with static bias. With fixed gate bias and AET from 7 V to 12 V (-▲-) ACPR3 is 1.3 dB better than AET from 8 V to 11 V (-◇-), which is almost 2 dB better than the static bias case (-◇-). Using dynamic gate in conjunction with AET from 7 V to 12 V (-◇-) the best result in linearity was achieved: an ACPR3 of -42 dB, which is a 4.5 dB improvement in ACPR3 respect to the static case, with a 6-point higher PAE (50%).

Comparing based on an ACPR3-level of approximately -42 dB, using AET from 7 V to 12 V with dynamic gate (-◇-) we achieve a 2-dB increase in average output power, and 17 extra points in PAE than with the static class-AB (-○-).

ACPR5 changed very little for each of the cases in each output power level, though solution 2 using AET from 8 V to 11 V with dynamic gate bias (□) improved ACPR5 by 4 dB at the expense of 2 dB in ACPR3 for an average output power of 29 dBm.

Summarizing, for the three different average output power levels, using AET from 8 V to 11 V can improve ACPR3 by 1 dB to 2 dB, and AET from 7 V to 12 V is in turn 1 dB to 2 dB better than AET from 8 V to 11 V.

For ACPR3, adding dynamic gate had in some cases almost unnoticeable impact, though for an output power of 29 dBm and using AET from 8 V to 11 V, the ACPR3-improvement was of 2 dB compared to having the gate bias fixed. For AET from 7 V to 12 V, at the maximum average output power, dynamic gate bias did count, as ACPR3 was reduced to -42 dB, an improvement greater than 2.6 dB

compared to having the gate bias fixed, which is 4 dB better than having static bias.

5.3.4 Overall comparison

Table 5.4 presents a ranking for the best and second best biasing options for each of the output parameters: gain, PAE, ACPR3 and ACPR5. The following conclusions are drawn from the table, as well as from figures 5.11 and 5.12, and Table 5.3.

- Class-AB with static biasing possesses high gain by itself. AET 7–12V yields the highest gain. Dynamic gate biasing can add some tenths of a dB in gain, while ET had some tenths of a decibel less gain than the static biasing case.
- The highest PAE levels are attainable with ET. Though dynamic gate increases the drain bias current near compression, it does not diminish PAE noticeably.
- The lowest ACPR3 is achieved with AET 7-12V, and then with AET 8-11V. Though the linearity achieved by combining ET with dynamic gate biasing at an output power of 30 dBm was as high as -39.2 dB, AET 7–12V with dynamic gate biasing can still improve ACPR3 by 3 dB. This improvement only occurs if dynamic instead of static gate biasing is used with AET from 7 V to 12 V.
- In many cases dynamic gate biasing can be used to reduce the fifth order distortion for the different average output power levels.
- Though using dynamic gate biasing together with static drain biasing only does not make it to the top of the ranking, one can reduce ACPR3 by a little more than 3 dB. This gain in linearity can be used to drive the PA harder and achieve 1 dB more in average output power, and thus increase PAE by more than 10 %.

5.4 GaN pHEMT

This section presents measurements of a power amplifier built around a pHEMT GaN transistor—the CGH40010, by Cree [79]. The PA is designed to operate at a frequency of 2.1 GHz, and has a saturated output power of 40.2 dBm (with a 200-mA bias current). The small-signal gain is 17.4 dB, while the gain at the saturation power is 14.2 dB. These values were measured for a continuous-wave input signal. The recommended drain bias voltage is 28 V and the drain tracker’s maximum voltage is almost 30 V, but the transistor has a break-down voltage of 120 V so it could actually be biased much higher. The matching of the amplifier

was designed for static bias operation for high output power, high gain, and high PAE. A photo of the amplifier is included in Appendix D.

5.4.1 Dynamic gate biasing

Dynamic gate biasing refers to varying the gate bias voltage as a function of the input power. This work considers only linear or quadratic gate biasing functions. However, when the gate bias is optimized one can distinguish between varying the gate bias in its three degrees of freedom (if it is a quadratic function) or to constrain the optimization so that near compression the bias current equals the bias current with static bias. The gate voltage variation becomes then a small “perturbation” or correction that can be added to the original static biasing gate voltage, and this will be called from now on auxiliary gate tracking (AGT).

Table 5.4: GaAs amplifier: ranking of the best biasing paths for each of the output parameters (gain, PAE, ACPR3, and ACPR5) and for different average output power levels P_0 (ACPR3 and ACPR5 are actually the worst ACPR values for a given biasing path).

P_0 (dBm)	Best	Gain (dB)		
		2nd Best		
28	AET 7–12 V - Dyn. G	13.14	AET 7–12 V - Fixed G	12.62
29	AET 7–12 V - Dyn. G	12.92	AET 7–12 V - Fixed G	12.62
30	AET 7–12 V - Dyn. G	12.69	Class-AB	12.47
		PAE (perc)		
		2nd Best		
28	ET Fixed G	58.44	ET Dyn. G	52.55
29	ET Fixed G	61.47	ET Dyn. G	60.35
30	ET Dyn. G, V_D clipped	61.45	ET Fixed G	60.79
		ACPR3 (dB)		
		2nd Best		
28	AET 7–12 V - Fixed G	-46.7	AET 8–11 V - Fixed G	-44.0
29	AET 7–12 V - Fixed G	-44.5	AET 8–11 V - Dyn. G1	-43.6
30	AET 7–12 V - Dyn. G	-42.0	AET 7–12 V - Fixed G	-39.8
			ET Fixed G, V_D clipped	-39.2
		ACPR5 (dB)		
		2nd Best		
28	AET 7–12 V - Dyn. G	-62.8	ET Dyn. G	-60.4
29	AET 8–11 V - Dyn. G	-61.4	ET Fixed G, V_D clipped	-60.4
30	ET Fixed G, V_D clipped	-57.2	ET Dyn. G, V_D clipped	-56.7

Full dynamic gate biasing

This subsection presents two different cases; the drain bias is fixed to 28 V in both of them:

- Full dynamic gate biasing compared to static class AB with $I_D = 160$ mA.
- AGT for deep class AB and class B operation.

In order to understand what dynamic gate biasing alone can do for the GaN PA, it would be useful to know how gain responds to gate bias variation. For the GaAs PA, as explained in Section 5.3.1, a gate bias function of the form of Figure 5.8 was effective at improving linearity. With this kind of function, the gate bias voltage, and thus the drain bias current, increases when the input power moves towards peak values. Ideally, taking a single-tone input power sweep for varying gate bias could help us see how the PA would react to bias current increase at peak input power, but the temperature increase due to higher dissipated power would limit the output power capability of the device. Gain increase near peak input power due to an increase in gate bias could therefore be hidden by thermal effects. Pulsed single-tone measurements, especially at high input power levels, would be appropriate. Since the required equipment is not available, the QAM signal described in Section 5.1.1 is used instead of a single-tone power sweep. Because the signal has a large PAPR (6.5 dB), i.e., power peaks come shortly and infrequently, power reduction due to thermal effects will be less than if non-pulsed static bias single-tone measurements were used.

Figure 5.13 shows the effect of increasing the gate bias voltage with fixed drain bias, using constant average input power for the QAM signal. The gain does not increase as much with gate bias as it does for the GaAs PA (Figure 5.7). If the gate bias function starts from the gate bias voltage the amplifier was designed to work with at low input power levels (\ominus , $I_D = 160$ mA), there is most likely little linearization that can be done near compression or at input power back-off by varying gate bias only, since the gain characteristic at the design bias point is almost flat. It is nonetheless possible that gate variation evens out phase-shifts arising from input power variations (i.e., AM/PM distortion).

In order to evaluate possible improvements in linearity, several optimizations for minimum ACPR3 and ACPR5 were run for dynamic gate biasing. In all of them the average gain was at least 0.5-dB smaller than at static bias operation. For the solutions that yielded an output power only 0.5-dB less than that of static class AB, the reduction in ACPR3 was never greater than 1 dB, and PAE was one or two points lower. Table 5.5 compares the class-AB case against one such solution, while Figure 5.14 shows the amplifier's gain curve when biased in static class-AB mode at its design quiescent current (160 mA).

Figure 5.15 shows the gain responses of the dynamic gate solution from Table 5.5, and of the class-AB amplifier in static bias. For the design bias point, the gain increase with increasing gate bias at compression is not large enough to

reduce nonlinear distortion significantly (Figure 5.13). The only way to even out the gain response is to reduce the overall gain, so the modest reductions in ACPR3 and ACPR5 come at the expense of reduced output power. There is therefore little to gain in linearity from dynamic gate biasing alone if the amplifier is operating as a class-AB at $I_D = 160$ mA. Nevertheless, Figure 5.13 shows that gate linearization could be used if the amplifier was biased deeper into class AB operation. In that case, output power would be reduced, but an improvement in efficiency could be attained, so dynamic gate biasing would be used as an efficiency enhancement method instead.

Auxiliary gate tracking for deep class-AB and class-B operation

When the GaN PA is biased statically in class B, there is a large gain drop at lower input powers (Figure 5.16). A maximum gain of 15.0 dB is attained at an input back-off of 4 dB, and the gain is greater than 14 dB for an input back-off a little larger than 10 dB. When the back-off is at 25 dB, however, there is a 7-dB reduction in gain, which gives dynamic gate biasing (or AGT) room for linearization.

From Figure 5.13 one might expect the gain drop to be compensated by having a high current at low input powers that decreases and “lands” in a class-B as we come near compression (i.e., the bias current level when the input back-off is 0 dB is the same as that of the static bias case). Figure 5.17 shows how such gate bias trajectory would look like.

Figure 5.18 shows a comparison of the performance of the PA with static bias against dynamic gate biasing using functions similar to the one shown in Figure 5.17. Both QAM and 2-tone signals are used as inputs. The gate biasing was optimized separately for each of the two cases. For the QAM input signal, the gain decay for the lowest input power is only 1.1 dB, and this translates to an improvement of 10 dB to 12 dB in ACPR5, and for the 2-tone signal the 5th order intermodulation power is reduced by 7 dB to 8 dB. For the QAM input signal, ACPR3 was correspondingly reduced by 2.1 dB to 2.5 dB. Using dynamic gate biasing for linearization increased the gain by a few tenths of a decibel in both cases. That is in agreement with Figure 5.16 since the gain is “straightened up” at the low input power level range only.

Table 5.5: GaN transistor: comparison of the performance of the class-AB amplifier biased with 160 mA against dynamic gate biasing. The drain bias is fixed at 28 V.

	Po (dBm)	Gain (dB)	ACPR3-L (dB)	ACPR3-U (dB)	ACPR5-L (dB)	ACPR5-U (dB)	PAE (%)
Class-AB	36.3	16.2	-41.7	-41.4	-61.2	-61.2	40.0
Dyn. gate	35.7	15.6	-43.3	-43.0	-63.3	-62.7	38.9

Figure 5.19 presents a similar comparison for the statically biased PA at a fixed drain bias current of 35 mA and 60 mA. For the 60 mA case the ACPR3 is improved by 5 dB, and ACPR5 by 7 dB. For the 35 mA case there is a 5 dB to 6 dB improvement in ACPR3, and more than 10 dB improvement in ACPR5. PAE and gain remain unaffected in both cases.

Dynamic gate biasing, or its particular form called auxiliary gate tracking, has therefore been shown to be extremely useful as a linearization method to operate the GaN amplifier in deep class-AB or -B modes near compression since it compensates the large gain drops occurring at the lower input power range.

Summary

Dynamic gate biasing alone does not linearize significantly when the PA is biased at its design bias point ($I_D = 160$ mA). If the amplifier is biased in deep class-AB or -B, however, varying the gate bias with the lower input power range can improve ACPR3 and ACPR5 by as much as 5 dB and 10 dB, respectively, without affecting PAE or gain.

5.4.2 Envelope tracking and dynamic gate bias

There are four biasing cases compared in Figure 5.20: static biasing at class-AB mode, ET with static gate biasing, ET with dynamic gate biasing optimized for linearity, and ET with dynamic gate biasing optimized for efficiency.

Figure 5.20 shows that the static bias class-AB amplifier ($-\circ-$) has the highest gain in the whole average output power range. The PA driven with ET and static gate bias ($-\square-$) yields the best PAE in the lower power range, but as output power increases compression increases strongly and gain becomes poor. The two solutions of ET combined with dynamic gate biasing—one optimized for linearity ($-\blacklozenge-$) and the other for PAE ($-\blacklozenge-$)—offer a gain of approximately 14 dB between 36 dBm to 38 dBm output power.

For an output power of 36 dBm, ET with dynamic gate optimized for linearity ($-\blacklozenge-$) reaches the best linearity levels with -52 dB in ACPR3, still maintaining ACPR5 low (-64 dB) and with a PAE of 52%—16 points higher than with static bias. For ET with dynamic gate optimized for PAE ($-\blacklozenge-$) ACPR3 is at -40 dB for 36 dBm average output power, and the PAE is 60% (23 points higher than with static bias). The difference in ACPR3 between the two solutions is less than 4 dB when the average output power is 38 dBm, but the solution optimized for PAE yields 71% in PAE, while the one optimized for linearity yields 63%, and static bias yields only 47.5%.

Summary

ET with fixed gate bias can yield PAE levels as high as 70% at the expense of higher nonlinear distortion and lower gain, and therefore is suitable for average

output power levels up to 36 dBm. Very high linearity levels can be achieved if ET is combined with dynamic gate biasing: ACPR3 can be as low as -52 dB with ACPR5 below -63 dB), and PAE can be 16 points higher than with static bias; the gain will be reduced by a couple of decibels. Optimizing the bias for the highest possible PAE can increase PAE by 23 to 24 points (both for 36 dBm and 38 dBm in output power) and still yield adequate ACPR3 levels (-40 dB, approximately). It is clear that for ET, dynamic gate biasing does make a difference in performance.

5.4.3 Auxiliary envelope tracking

AET can be simplistically described as varying the drain bias of the PA slightly up and down around the fixed drain bias voltage the PA was designed to operate with (Section 5.1.5). Since the drain tracker for the GaN transistor is limited to a peak voltage of 28 V, the fixed bias reference voltage for the GaN PA is considered to be 25 V (for comparison purposes). Another solution considered to circumvent the 28 V dynamic bias limit was to use clipping at the drain bias waveform.

AET at normal class-AB operation

For the PA operating at a 160-mA drain bias current, there are altogether four different cases to compare:

1. Class-AB with $V_D = 25$ V and $I_D = 160$ mA
2. AET with an average V_D ($V_{D,avg}$) of 25 V and $I_D = 160$ mA
3. AET with clipped V_D and $I_D = 160$ mA
4. AET with clipped V_D and dynamic gate biasing

Applying dynamic gate biasing to case 2 made no difference except improving ACPR5 by 1 dB. Driving the PA with static biasing and $V_D = 28$ V instead of 25 V increased the gain 0.4 dB and reduced the PAE by 5 points at an average output power of 39 dBm. Since these changes are minor these two cases are not included in the final comparison shown in Figure 5.21.

Figure 5.21 shows that the ACPR3 improvement due to AET (\square) compared to static biasing (\circ) is almost 6 dB for an output power of 35.8 dB, and 4 dB for an output power of 36.6 dB. In this output power range ACPR5 improves almost 2 dB with AET, and PAE is almost 2 points higher. When the average output power is increased to 38.8 dBm there is only a 1.5-dB improvement in ACPR3 using AET without clipping at the drain bias.

When the gate voltage is fixed and V_D is clipped (\diamond) ACPR3 is 3.5 dB better than with static biasing (\circ) and 1.7 dB better than with AET with no clipping (\square). ACPR5, however, is 3.2 dB to 3.4 dB worse than with static biasing,

and 1.8 dB to 2.0 dB worse than AET with no clipping. Adding dynamic gate biasing at the highest output power level (\otimes at 38.9 dBm) solves the problem: ACPR5 becomes 2 dB better compared to static bias ($-\circ-$), and yet the 4-dB improvement in ACPR3 from adding AET is preserved.

AET at deep-class-AB operation

This last case considers biasing the amplifier in deep AB mode with $V_D = 25$ V. In Figure 5.22 static biasing is compared to static drain biasing with dynamic gate, AET with the gate biasing varying linearly with input power, and AET with gate biasing varying quadratically with input power.

As one moves from class-AB towards a class-B, it is expected that the gain is reduced and that PAE increases. This agrees with the results of Figure 5.22, which show a 1-dB lower gain for the statically biased PA at 35 mA quiescent current, compared to static bias at a 160 mA quiescent current, and a 4-point higher PAE. The amplifier in deep AB mode, however, presents much higher third and fifth order distortions—6 dB and 8 dB to 10 dB, respectively. That is due to the large gain drops at low input power levels for this GaN transistor when biased statically in deep class AB or class B mode.

Compared to static biasing for a 35 mA quiescent current, AGT alone improves ACPR3 by almost 7 dB, and ACPR5 by more than 11 dB; since it corrects a 5-dB gain drop that occurs at the low input power range. Combining AGT and AET can improve ACPR3 by 4 dB to 5.5 dB, depending on whether the gate bias varies linearly or quadratically with input power. With a linear gate bias variation on input power ACPR3 is only 0.7 dB worse; while ACPR5 and PAE remain mostly unchanged.

Summary

At a drain bias current of 160 mA, and for an output power range of 35.5 dBm to 38.9 dBm, AET is useful in linearizing 3rd and 5th in-band distortions for low to medium power levels. For high output power levels it is desirable to increase the peak drain bias voltage to avoid compression. Though this was not possible due to the peak voltage limit of the drain tracker, using clipping at the drain bias waveform still yielded a 2-dB improvement in ACPR3 compared to AET without clipping. Combining AET with clipping and dynamic gate biasing was best since then ACPR5 was also improved, making it 2 dB lower than with static bias and retaining the 3.5-dB improvement in ACPR3.

For a lower average output power (35.5 dB), results also show how dynamic gate biasing allows the transistor to be biased low as a deep class AB maintaining the same PAE, while noticeably improving linearity by straightening the gain response at the lower input power range—ACPR3 levels were tenths of dB shy from -50 dB, and ACPR5 was as low as -62.8 dB combining AET with dynamic gate bias. Nevertheless, dynamic gate biasing alone could correct both ACPR3 and ACPR5

by 7 dB and 11 dB respectively. Varying the gate linearly with the input power in combination with AET can be almost as effective as quadratic variation, having the advantage of reduced computational or circuit complexity and reduced bias bandwidth, since the square of the input power need not be computed.

5.5 General summary

5.5.1 About the method

Chapter 3 and Chapter 4 approached the problem of finding biasing functions using quasi-static modeling based on single-tone data. In Chapter 3 a point-search algorithm was used to find the biasing functions as a discrete sequence of points. In Chapter 4 the biasing functions were expressed as first and second order polynomials of input power, for the drain and gate, respectively, and the coefficients were found using random search optimization.

In this chapter, a full measurement setup to experiment with dynamic biasing was presented. The setup allowed the optimization of the biasing functions based solely on measurement data for difference devices technologies: an HBT MMIC transistor, a discrete GaAs pHEMT amplifier, and a discrete GaN pHEMT amplifier. The signal the amplifier is intended to work with was used as the input signal—in this case, a 16-QAM signal with 1-MHz symbol rate. Only one variable was optimized at the time: either adjacent plus alternate channel distortion was minimized, or average PAE was maximized. Depending on the variable being optimized, other variables (such as minimum average gain) were used as constraints. The random search optimizer from Chapter 4 was used again as a solver, and the biasing functions, as in Chapter 4, were treated as polynomials of input power, but the possibility of clipping the bias waveforms at either end was added (in total there were 10 degrees of freedom to optimize, but the methodology made it possible to reduce the number of optimized variables as desired). The gate/base and drain/collector trackers were built with a frequency response up to 5 MHz.

5.5.2 About the results

An important contribution of this chapter (Section 5.2.1) is to have validated the quasi-static model used for the HBT MMIC transistor in Chapter 4. Good agreement of measured and simulated results was observed. The results for PAE matched extremely well, and though some small differences were observed in ACPR3, the optimization based on simulation from Chapter 4, successfully selected the bias functions that yielded minimum ACPR3 distortion. That was very clear especially when comparing the dynamic biasing results against static bias operation.

Though there were many different kinds of experiments carried out for each device, some general conclusions can be drawn from the results:

- *Dynamic gate biasing* alone can be very effective as a linearization method (e.g., HBT transistor, Figure 5.4, sweetspot at an output power of 16.8 dBm). If the transconductance increases significantly with gate bias (as with the GaAs PA), it might even be possible to linearize at compression (Figure 5.12, 2-dB improvement from \ominus respect to \blacktriangle). Dynamic gate biasing can also be used to even out gain-drops or gain/phase ripples caused by dynamic drain biasing (GaN PA, e.g., Figure 5.16, Figure 5.19), or specially to improve ACPR5 levels (GaAs amplifier, Figure 5.12, 4-dB improvement from \diamond to \square). PAE was in general not affected significantly, a few PAE points may be won or lost.
- *Dynamic drain biasing* is used for efficiency enhancement. In some cases there might be little to win by combining it with dynamic gate biasing, since it may happen that linearity is not deteriorated significantly compared to static bias operation, or that the addition of dynamic gate bias yields little benefit in terms of ACPR3 and/or ACPR5 improvement. For the HBT, PAE was more than tripled for an output power of 14.8 dBm (+28 PAE-points, Figure 5.3), and there was an increase of 16 PAE-points comparing the maximum output powers with dynamic and static bias (Figure 5.5). For the GaAs PA PAE increased by 25 and 15 points for average output powers of 28 dBm and 30 dBm, respectively (Figure 5.11). The GaN PA had an increase in PAE of 23 (almost a factor of two) and 24 points (71.4%) at average output powers of 36 dBm and 38 dBm, respectively (Figure 5.20).
- *Dynamic biasing for maximum output power*, based on driving the drain bias higher at peak input power than in static bias operation, can serve to purposes: (1) Linearization, since clipping of the drain envelope voltage waveform will be reduced due to higher biasing (2) “Squeezing out” as much output power from the transistor as possible. Measurements on the HBT clearly illustrate the latter, since a 21-dBm output power was obtained with dynamic biasing, where as the transistor surrendered to breakdown effects with static biasing, in an attempt to reach an output power almost 1 dB lower (Figure 5.5). (It is not possible to know from these experiments if continuous dynamic biasing pushing the device so hard would reduce its reliability and lifetime.) The breakdown voltage for the GaN transistor, which exceeds 100 V, is far from the reach of the drain tracker. Nevertheless a 4-dB improvement in ACPR3 was possible by increasing the average drain bias voltage using clipping (Figure 5.21). For the GaAs transistor, 12 V is the absolute maximum drain bias voltage, not recommended for continuous operation. Though the transistor was not driven into breakdown, biasing at 12 V at peak power yielded 17 extra PAE-points for an output power of 30 dBm, compared to static biasing for 28-dBm output power, with 0.2-dB improvement in ACPR3, and the same average gain. So even if the input power is not driven so high as to press the transistor to its maximum output

power, the benefit of higher drain/collector bias is clearly seen in linearity and gain.

The results from the measurements in this chapter enforce a strong statement: biasing dynamically—and intelligently choosing whether to do it at the gate, at the drain, or both—can lead to performance enhancement for linearity, PAE, and output power without having to trade one for the other.

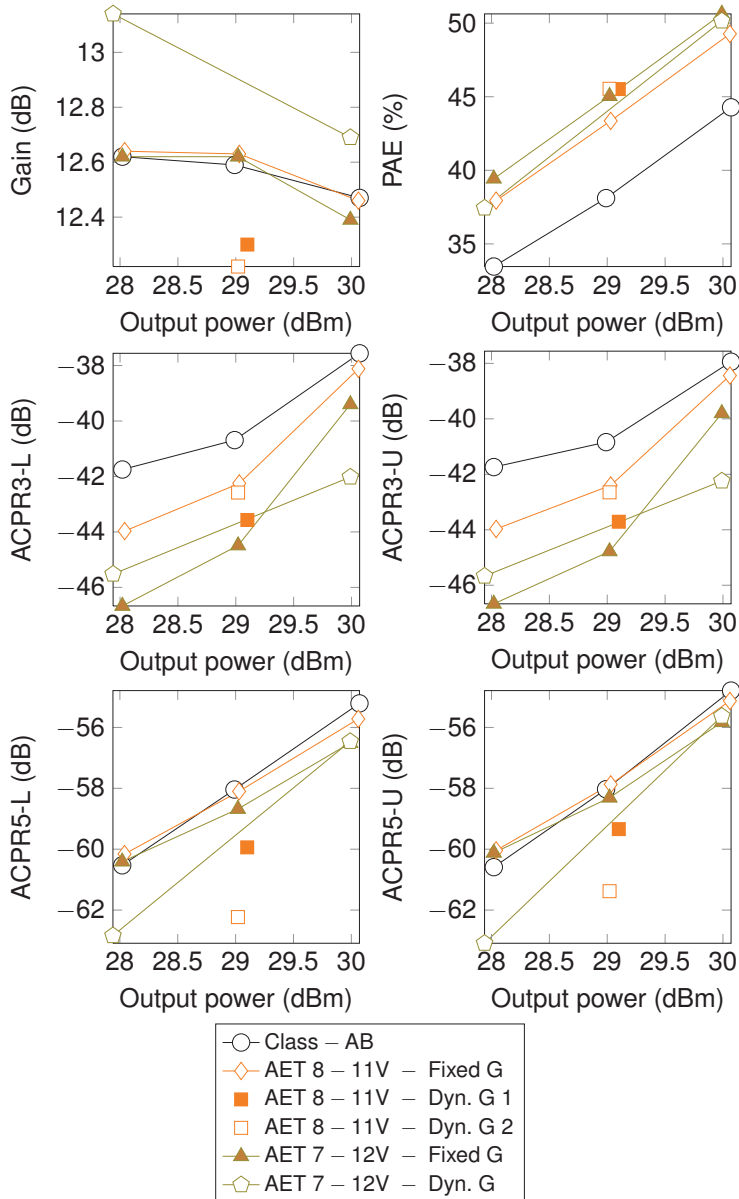


Figure 5.12: GaAs amplifier: comparison of the different auxiliary envelope tracking cases in terms of gain, lower/upper ACPR3 (ACPR3-L/U), lower/upper ACPR5 (ACPR5-L/U) and PAE for different average output power levels.

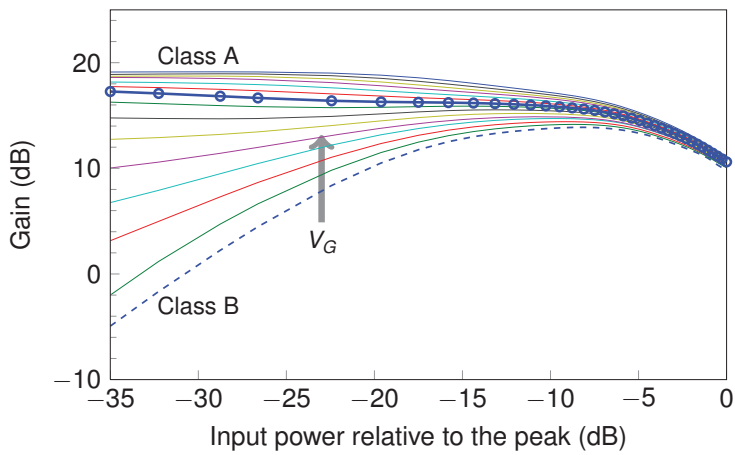


Figure 5.13: GaN transistor: fit of gain vs. relative input power for constant gate bias sweep (V_D is fixed to 28 V). The gate voltage V_G is swept linearly from class B operation ($1\%I_{D,max}$) to high class AB operation ($35\%I_{D,max}$). The $\text{---}\circ\text{---}$ curve corresponds to the 160-mA quiescent current the PA was designed for. The QAM input signal, described in Section 5.1.1, has a peak input power of 31.8 dBm, and the average input power is 25.1 dBm.

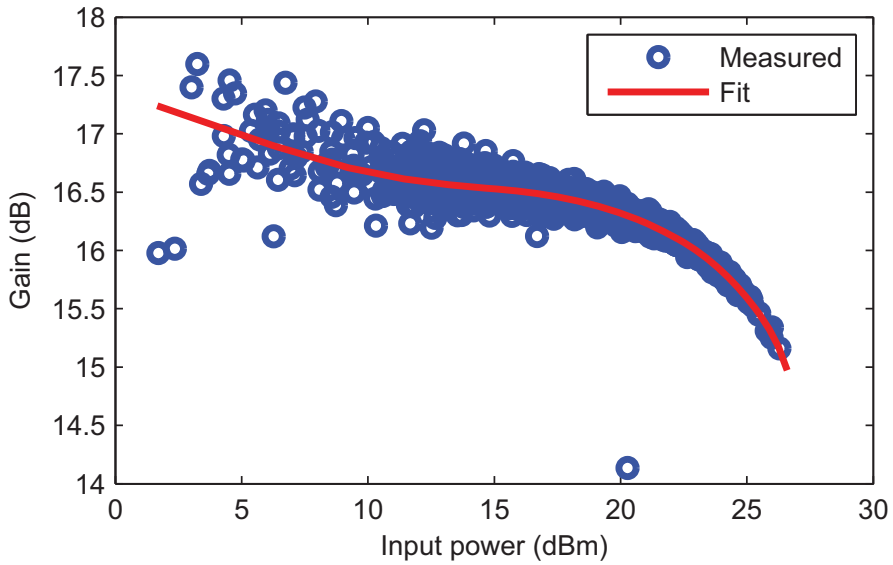


Figure 5.14: GaN transistor: gain response of the amplifier biased statically in class AB with a bias current of 160 mA and a drain bias voltage of 28 V (o measured data points, — polynomial fit from the measured data points.).

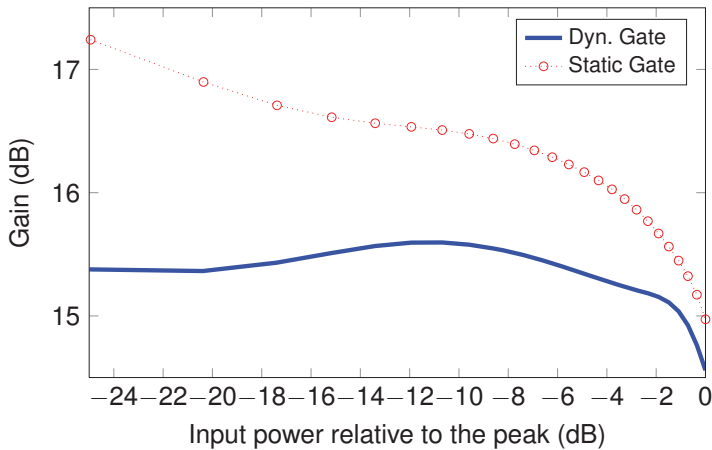


Figure 5.15: GaN transistor: gain-comparison of the class-AB amplifier with static gate biasing ($I_D = 160$ mA) and dynamic gate biasing. The drain bias is fixed to 28 V.

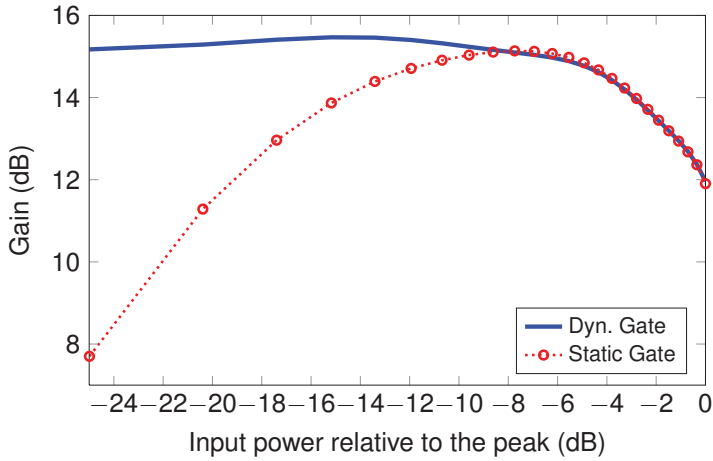


Figure 5.16: GaN transistor: Comparison of the gain response for the GaN PA biased in class B mode for an output power of 38.8 dBm: (1) static biasing for a drain bias current of 10 mA ($\cdots\circ\cdots$) (2) Auxiliary gate tracking for a drain bias current of 10 mA at 0 dB relative input power (—). The drain bias is fixed to 28 V. The gain curves are polynomial fits from the measured data.

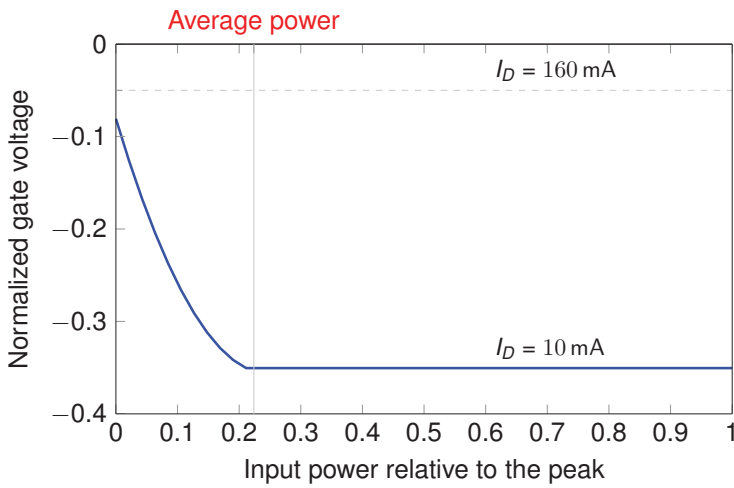


Figure 5.17: GaN transistor with auxiliary gate tracking: gate bias voltage vs. input power to compensate for the gain drop shown in the dotted curve in Figure 5.16. The gray mark in the x-axis shows the relative average input power. The y-axis to the right shows the static bias current that corresponds to the gate bias voltage.

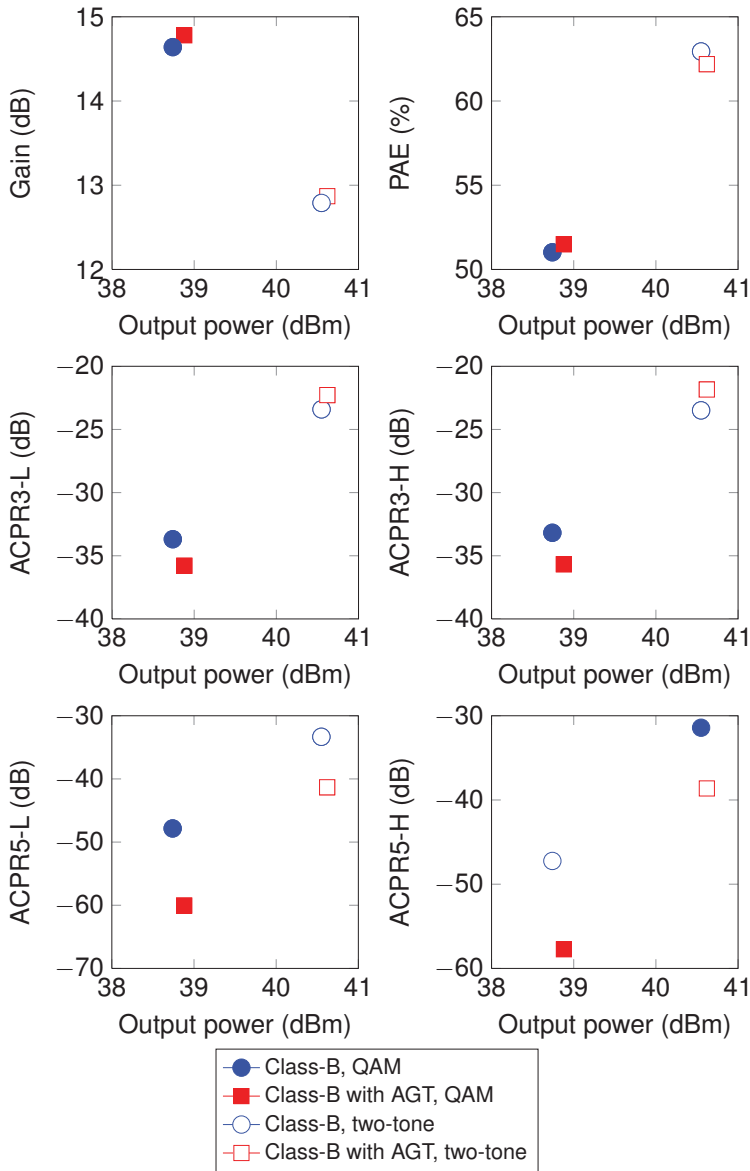


Figure 5.18: GaN transistor: comparison of the performance of the PA driven as a class-B with static bias, and with auxiliary gate tracking with QAM and two-tone signals.

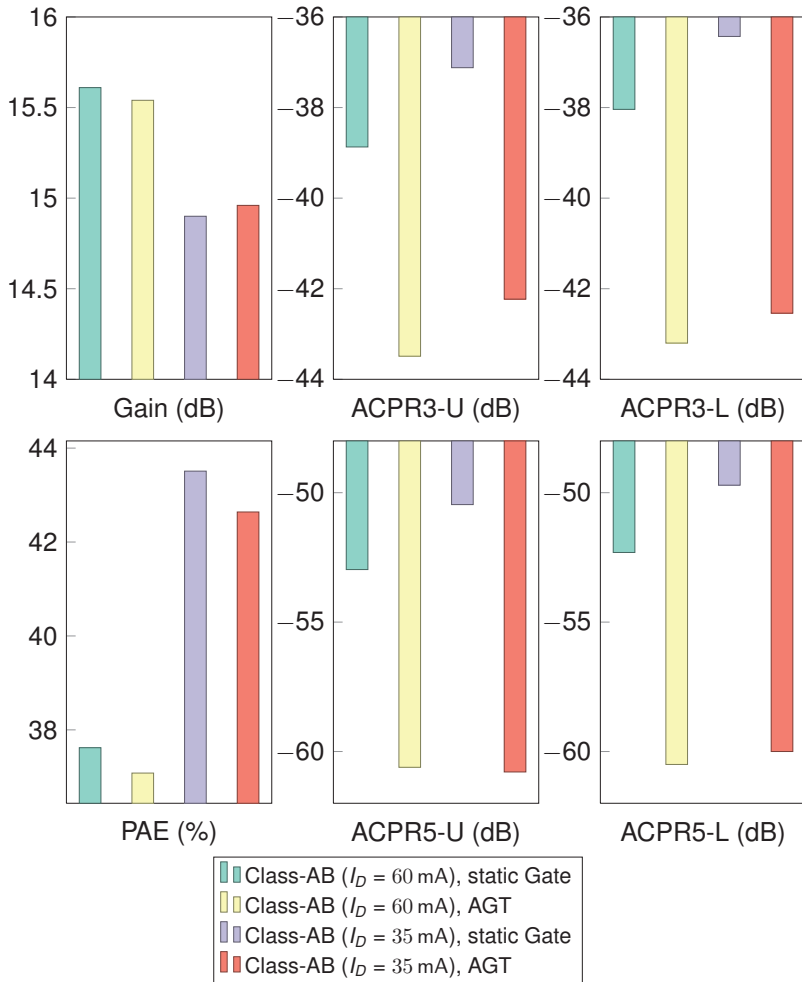


Figure 5.19: GaN transistor: comparison of the performance of the PA biased in deep class-AB mode with a bias current of 35 mA with static and dynamic gate biasing (AGT), and with a bias current of 60 mA with static and dynamic gate biasing. The drain bias is fixed to 28 V, and the average output power is in the range 36.2 dBm to 36.6 dBm.

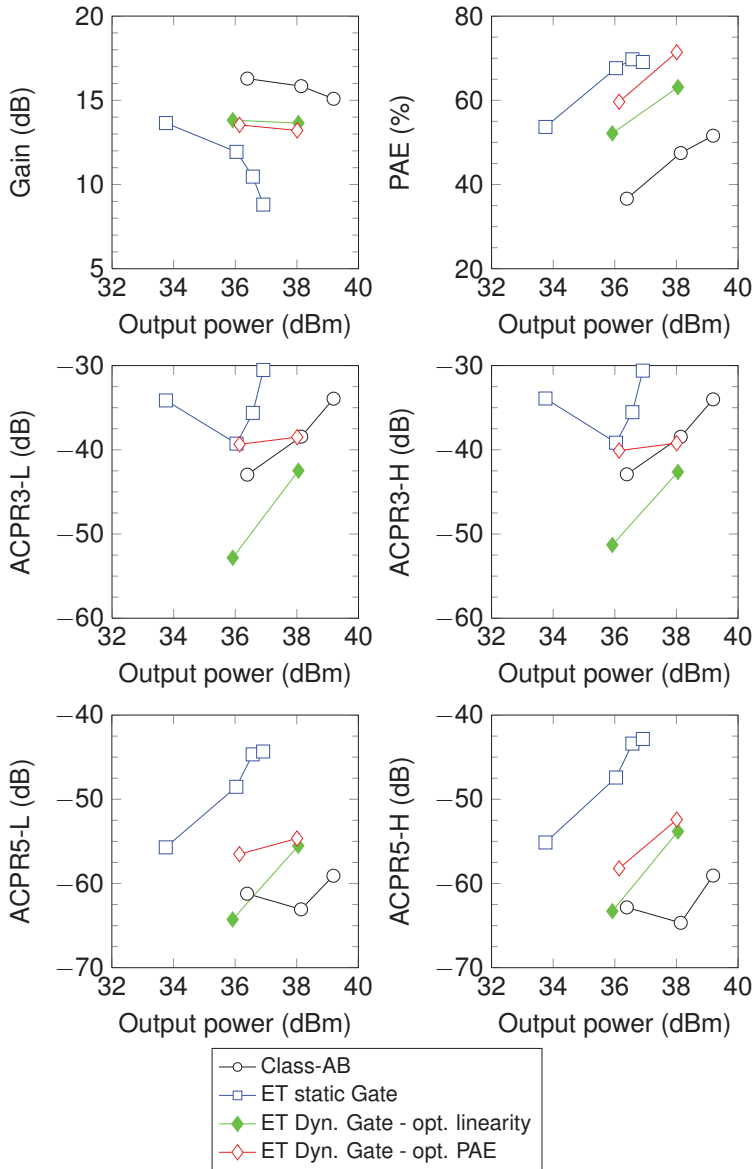


Figure 5.20: GaN transistor: comparison of four biasing cases: static biasing, ET with static gate biasing, ET with dynamic gate biasing optimized for linearity, and ET with dynamic gate biasing optimized for PAE for different average output power levels.

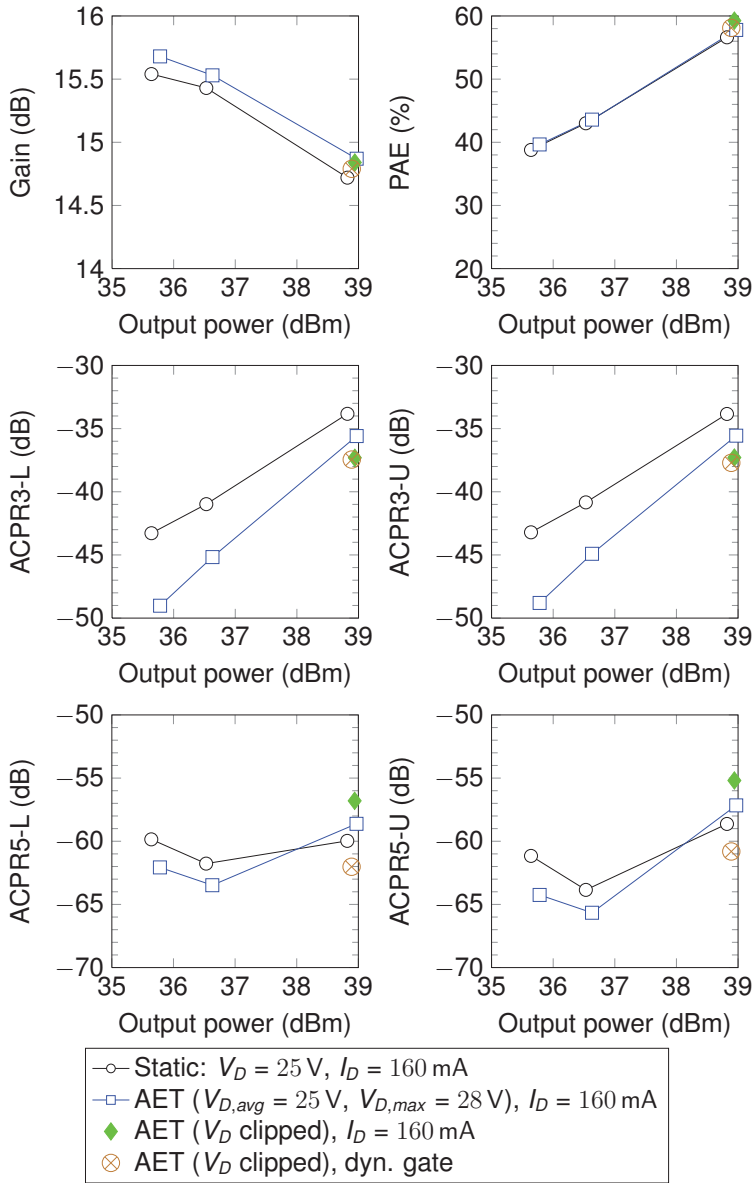


Figure 5.21: GaN transistor: comparison of four biasing cases for different average output power levels: static biasing \circ -, AET with fixed gate bias \square -, AET with clipping at the drain and fixed gate bias \blacklozenge -, AET with clipping at the drain and dynamic gate bias \otimes .

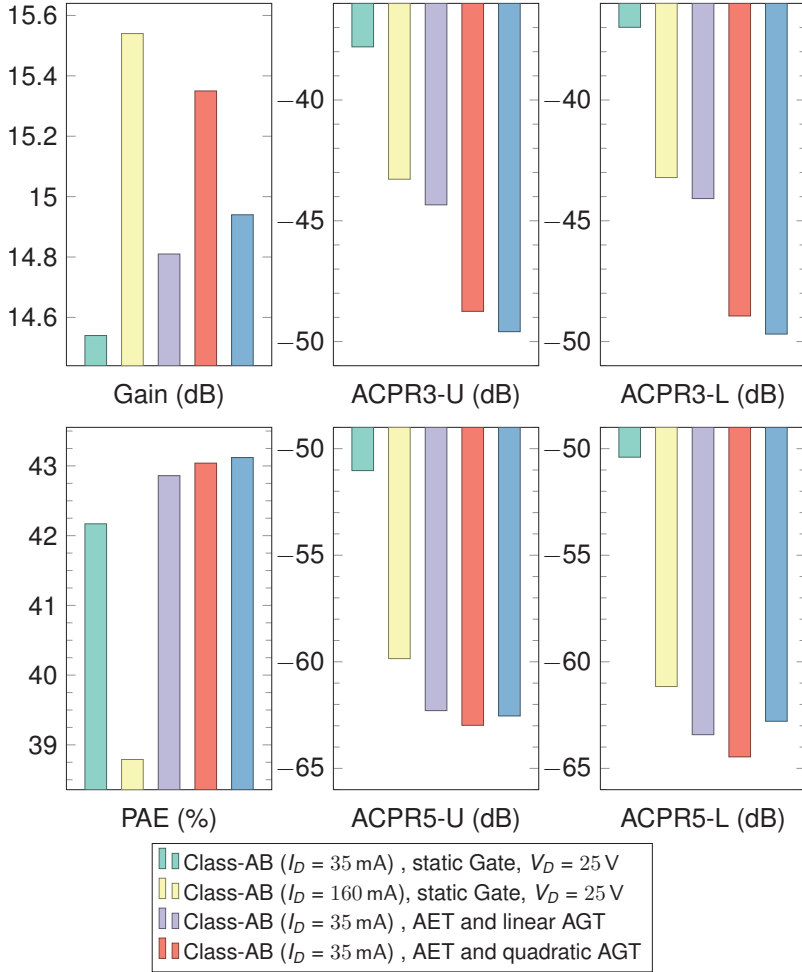


Figure 5.22: Comparison of the PA performance operating in deep AB mode for (1) Drain bias fixed to 25 V and fixed gate bias for $I_D = 35$ mA (2) Drain bias fixed to 25 V and fixed gate bias for $I_D = 160$ mA (3) Drain bias fixed to 25 V and AGT for $I_D = 35$ mA (3) AET with AGT linearly varying with input power for $I_D = 35$ mA (4) AET with AGT varying quadratically with input power for $I_D = 35$ mA. The deep class-AB for $I_D = 35$ mA has an average output power of 35.1 dBm, while for all other cases the output power is in the range 35.4 dBm to 35.6 dBm.

Chapter 6

Conclusions and perspective towards the future

Throughout this dissertation, dynamic biasing has been presented as a solution to the linearity–efficiency trade-off arising from modulated signals with large crest factors. Dynamic biasing is especially suitable for point-to-point radios, which operate with bandwidths spanning decades of megahertz and output powers below 10 W, where low-cost, reliability and independence of carrier frequency is desired.

What follows is the condensed story of the process and reasoning behind this research study, arriving at fruitful conclusions, next posing questions that are yet to be dealt with.

6.1 A tale with end unwritten

6.1.1 Starting from scratch

In 1999, it was theoretically proven that simultaneous variation of gate and drain biases with envelope would lead to improved PA efficiency [22]. A number of questions arise: how much benefit in efficiency will such a scheme yield for different device technologies and class of operation? how to deal with the bandwidth limitations of the bias supplies? will linearity be worse or better compared to static bias operation? will the selection of the optimum output matching be different from what traditional PA design theory dictates? can such a scheme be combined with other linearization methods such as predistortion? All of these questions were an incentive to pursue research in this direction.

Envelope tracking, usually used with class-B amplifiers, has already been around for some decades. It is common in ET that drain bias V_D and input envelope voltage v_i are paired up so that maximum efficiency is reached at each (v_i, V_D) combination, even if the amplifier is driven several decibels into compression. In point-to-point radios efficiency is important, but there are strict regulations on linearity. Adding the gate bias into the picture makes the problem three-dimensional

(input power, gate bias voltage, and drain bias voltage) and adequate bias solutions are no longer easy to extract by means of graphical methods (e.g., contour plots).

6.1.2 Searching in a multidimensional space

The reasoning then was to find a more systematic approach using three-dimensional matrices of output power, phase shift, power added efficiency, and even second and third harmonic levels based on single-tone sweeps. A point-search algorithm was devised (Section 3.6) that would allow the search for bias functions without any particular shape, assuming only a dependence on input power. (A good example is the pHEMT “tuned path”, as presented by Caharija et al. [64].) The method was applied in simulation to an MMIC pHEMT amplifier and an MMIC HBT transistor. Being aware of how bias variation as a polynomial of power would potentially have low bandwidth, the discrete sequence of bias points yielded by the algorithm were transformed to continuous curves by interpolation. Then, for the case of the pHEMT, the continuous curves were compared to simple first and second order polynomials dependent on input power for the drain bias, and gate bias, respectively. A simulation with dynamic biasing with a modulated signal was carried out for many of these trajectories. The conclusion was that low-order polynomials could yield very satisfactory efficiency levels, and comparable linearity levels to the bias functions found with the point-search method.

6.1.3 Parabolas and straight lines

The next step was to find a systematical approach towards the new target; to find the coefficients for the gate and drain bias polynomials. There were several expectancies for the new method compared to the point-search algorithm:

- It should find polynomials of a given degree, instead of a sequence of points.
- The number of optimization parameters must be reduced (e.g., weights for the gain ripple, second and third harmonic components; required by the point-search algorithm).
- It should take into account the probability density function of the modulated signal the amplification system is intended for.
- It should use a clear optimization metric for linearity (as opposed to gain ripple, phase variation, and second and third harmonic levels from single-tone data, which do not relate directly to performance parameters such as ACPR, or EVM).

It is so that the method presented in Chapter 4 came to be. The goals were clear: to optimize efficiency and linearity. This time the gain vs. input power curve

was to be modeled as a polynomial, and there was to be only one nonlinearity measure: a function of the polynomial fit of the input and the output, weighted by the PDF of the modulated signal (see (4.25)). Efficiency would be measured as the average dissipated power by the average output power, and the two optimization goals would be integrated in a global multi-objective optimization function (refer to (4.15)). The advantage of the function lies in its simplicity, as it is oriented more towards finding “spots” in which both linearity and efficiency are “better than” certain threshold levels. Aiming for the absolute optimal linearity–efficiency combination would make the optimization problem much larger, which would increase the computational time, and may require a more complex solver.

Another achievement was to formulate the optimization problem in a simple mathematical fashion: constraint functions were derived assuming that the bias functions would be monotonically increasing. The last step would be to find an adequate solver. MATLAB offers several, but they are based on gradient methods that tend to violate constraints and settle for the first local solution. Random search was chosen instead, for it is a simple stochastic optimization method that may find the global optimum in some non-convex optimization problems [69]. Some variations of the concept allow the search range to be narrowed as the number of iteration increases.

Having formulated dynamic biasing as an optimization problem as a whole, different solutions were found for the MMIC pHEMT amplifier and the MMIC HBT transistor, with different trade-offs between linearity and efficiency.

6.1.4 A slight deviation towards the ideal

Let us first visualize an ideal transistor, one with perfectly linear transconductance between zero and maximum drain current, and zero-knee turn-on region. It is known that if a class-A amplifier was built on such a device, operation could be held in class A mode even at reduced envelope levels. The requirement would be that the drain and gate biases varied proportionally to the envelope (ergo, drain efficiency would be 50 % for all power levels). But what is one to expect if the bias followed 1st and 2nd order polynomials of the input power?

A simple theoretical analysis (Section 3.3.1) showed that even with an ideal device, biasing dynamically with input power p would produce gain ripple because the conduction angle changes with p . If the gate bias went from the threshold voltage—ideally zero—up to class A mode, the conduction angle would vary between 180° to 360° . That is, the amplifier would change from class A to class B operation, the gain response would vary 6 dB along with input power, and drain efficiency would be between 50 % to 78.5 %.

To avoid clipping of the envelope voltage at the drain, drain bias can no longer start from zero up to class A, and even an output matching different from class A operation may be required, depending on the gate bias function, to maximize efficiency. Another alternative to avoid distortion from envelope clipping, would

be to clip the upper part of the drain bias signal. The power at which clipping begins, together with the minimum drain bias voltage would allow the bias to track very near to the envelope signal, especially at the signal's average output power. This would increase efficiency, and avoid nonlinear distortion from clipping.

In practice, as confirmed by the experimental results, the gain response can be shaped so as to avoid gain drop along the power range, and performance can actually improve both in linearity and efficiency. One reason is that the gate bias needs not move all the way down to the threshold voltage (conduction angle variation would then be reduced), but another cause is that non-ideal effects can actually act to our favor: transconductance nonlinearity, the dependence of transconductance on bias, and harmonic component reflection can contribute to reduce the gain difference due to a reduction in conduction angle [9].

The analysis makes one thing clear: biasing as a function of power will reduce bias bandwidth, but the bias functions and the output matching must be carefully chosen, as they will have an impact in linearity, output power and efficiency.

6.1.5 Measure to be sure

It would not be until Chapter 5 that an experiment with the HBT transistor, driven with a modulated signal and by *real* dynamic bias sources, would confirm the validity of the method. There was excellent agreement between simulation and measurement results regarding power added efficiency, and though there were differences in ACPR3, the tendency was the same: relative to static class A operation, the method found paths that would yield higher or lower ACPR3 levels.

But then again there were limitations. The single-tone characterization data, used for optimization in chapters 3 and 4, would be more reliable if pulsed-measurement characterization was used. Then dynamic effects from the amplifier—thermal loading, charge storage, and other memory effects—would be separated from static behavior [80]. In the case of envelope tracking, holding the bias current fixed and pulsing RF and drain bias is the closest to ET conditions [63]. But adding dynamic gate biasing as an independent variable, however, means that both gate and drain biases would have to be pulsed from a reference bias point to each of the (V_G, V_D) test bias points, since thermal load varies with bias current. The selection of the reference bias point would have had an impact on the measurement results [81].

A more empirical approach was therefore taken. The construction of a drain bias supply that allowed for an accurate measurement of the drain bias current proved to be a challenge. Once overcome, it was possible to harvest new, reliable results based directly on the application of dynamic bias to a given amplifier or transistor, using the modulated signal it was intended to work for. Every part of the process was stirred from the computer: the shaping of the RF and bias signals, their uploading to the signal generator, the ACPR and output power measurements from the signal analyzer, and the measurement of bias current and voltage from

the oscilloscope to compute PAE. Three devices were measured: the 20-dBm HBT MMIC transistor characterized in simulation, a discrete 2-W GaAs amplifier, and a discrete 10-W GaN amplifier. Different dynamic biasing cases were tried on the three amplifiers, which can be summarized in the four following cases:

1. *Fixed drain bias with dynamic gate bias*, where the gate bias is used mainly for linearization
2. *Fixed gate bias with dynamic drain bias*, where the drain bias will work purely as an efficiency enhancement mechanism, probably at the expense of linearity
3. *Gate and drain dynamic biasing for high efficiency, or high linearity*, depending on the settings of the random search optimizer. This case can be seen as envelope tracking (for high efficiency) accompanied of dynamic gate biasing (for improved linearity).
4. *Dynamic biasing for maximum output power*, in which the drain/collector bias is higher than it would be with static bias in order to drive the transistor harder.

Some important conclusions can be drawn from these experimental studies:

- *Dynamic gate biasing* alone can be an effective linearization method. If the transconductance increases significantly with gate bias (as with the GaAs PA), it might even be possible to linearize at compression. Dynamic gate biasing can also be used to even out gain-drops or gain/phase ripples caused by dynamic drain biasing (particularly noticeable with the GaN amplifier), or specially to improve ACPR5 levels. In general it does not affect PAE significantly, a few PAE points may be won or lost.
- *Dynamic drain biasing* is used for efficiency enhancement. In some cases there might be little to win by combining it with dynamic gate biasing; either because linearity is not deteriorated significantly compared to static bias operation, or because the improvement in ACPR3 and/or ACPR5 is so modest that it does not justify the addition of dynamic gate bias. The improvement in PAE respect to static biasing is in the order of 15–30 percent points, depending on the amplifier’s average output power.
- *High dynamic biasing for maximum output power*, based on driving the drain bias higher at peak input power than in static bias operation, can serve to purposes: (1) Linearization, since clipping of the drain envelope voltage waveform will be reduced due to higher biasing (2) To drive hard the amplifier, to gain as much output power from it as possible (as done with the HBT transistor). The effect of the latter on the device’s lifetime and reliability can be a subject of further study. When biasing high for linearization (i.e.,

with auxiliary envelope tracking), ACPR3 distortion can be maintained at the same level as with static biasing operation, but higher output power and higher PAE can be attained. So even if the input power is not driven so high as to press the transistor to its maximum output power, the benefit of higher drain/collector biasing is clearly seen in linearity and gain.

6.2 Continuing to walk

This dissertation has demonstrated that dynamic biasing will improve efficiency with similar, or better linearity levels for today's popular transistor technologies. Nonetheless, a number of unanswered questions remain that can serve as inspiration to future research.

6.2.1 Selection of output impedance at fundamental and harmonic frequencies

The effect that output matching can have on the gain response with dynamic biasing was addressed in Chapter 3 (Figure 3.13, and Figure 3.14). It would be interesting to develop a more comprehensive method, based on theoretical conclusions and experimental observation, to select an optimum load impedance at fundamental and harmonic frequencies for a dynamically biased PA. There is an interdependence in the problem, as the output impedance will affect the optimization of the bias functions, but it is for a given bias point and power level that output impedance must be optimized. Parameters such as drain–source capacitance, drain–gate capacitance, and transconductance may exhibit strong dependence on bias. To the knowledge of the author, studies of the kind have only been carried out for envelope tracking [61],[82]. The addition of gate bias into the matching problem makes it even more interesting. A combination that could also be worth studying is load modulation [83] with dynamic biasing.

6.2.2 Pulsed measurements for the quasi-static model

Although it is possible to select biasing functions from direct measurements with modulated signals (Section 5.1), it is often desirable to have a reliable model for simulation. The quasi-static model used for simulation in this work relied on single-tone power sweeps for different constant-gate–constant-drain bias combinations (Section 3.5). Thermal effects in small devices, such as the HBT and pHEMT MMICs, can go up to frequencies of 0.1 MHz to 1 MHz [80]. Because this is not far from the bandwidth of the bias signals applied to these transistors, the model is reasonably accurate. Nonetheless, for larger devices with larger thermal time constants, pulsed-RF/pulsed-DC measurements will be more suitable [63]. The width of the pulse would be related to the proportion between the bias bandwidth

and the inverse of the thermal time constant. Also, the reference bias point will affect the pulsed measurements, and would depend on the selection of the bias functions, so an iterative procedure would most likely be necessary.

6.2.3 Biasing and driving the device for maximum output power

Utilizing the device to its full capacity is always desired. Biasing higher at the drain at high input power is particularly attractive to get as much power out of the transistor as possible, and can also be used to linearize at compression by reducing clipping of the RF output waveform. Knowledge of the physical construction of the transistor could be used to determine how high can drain bias and RF input power go for maximum output power operation without damaging the device, depending on the probability density function of the modulated signal, as well as the impact that hard driving may have on the device's lifetime and reliability.

6.2.4 Digital predistortion with dynamic biasing

To begin with, it would be exciting to combine digital predistortion with dynamic biasing as explained in Chapter 4. The proposed linearity measure has the advantage of aiming for minimum 3rd and 5th order distortions, which are priorities to comply with the spectral mask. Low-order memory polynomials for memory effect mitigation would also be an interesting possibility [84], as this method offers faster convergence and smaller memory requirements compared to look-up table memory predistortion [85].

6.3 Arriving where we started

The journey towards efficiency enhancement of the well known linear class-A and class-AB amplifiers will surely continue. This dissertation hopes to have awakened interest in dynamic biasing as a promising alternative by exposing different aspects related to bias variation, showing the improvements that one can expect for small and large devices, for HEMTs or HBTs.

Bias variation can yield an advantage in linearity, efficiency, and output power; and one thing is sure: every stage of the amplifier design process can be reengineered towards that ultimate goal.

Appendices

Appendix A

Derivation of constraints for random search optimization.

As mentioned in Section 4.2, two types of constraints were used. The bound constraints, β_{lb} and β_{ub} , are lower and upper bound limits on the values of the elements of β . That is,

$$\beta_{\text{lb}} < \beta < \beta_{\text{ub}}. \quad (\text{A.1})$$

Linear constraints are bounded linear combinations of the elements of β , such that

$$\mathbf{A}\beta \leq \mathbf{b} \quad (\text{A.2})$$

where \mathbf{b} is a vector with N_c elements— N_c being the number of linear constraints—and \mathbf{A} is an N_c by 5 matrix, since there are five elements in β .

The criteria to derive the constraints are the following:

- I. $V_G(p)$, and $V_D(p)$ must be monotonically increasing (MI) to avoid that the bias suddenly enters regions of extremely low or high drain currents.
- II. There are upper and lower bounds for the values of V_G , V_D , and p , given by the minimum and maximum values in the single-tone characterization for each variable (see Section 3.5). That is

$$V_{G,\text{min}} \leq V_G(p) \leq V_{G,\text{max}} \quad (\text{A.3})$$

$$V_{D,\text{min}} \leq V_D(p) \leq V_{D,\text{max}} \quad (\text{A.4})$$

Because $\beta = [g_2, g_1, g_0, d_1, d_0]$, where g_2 , g_1 and g_0 define the parabolic function $V_G(p)$; and d_1 and d_0 define the straight line for $V_D(p)$, the analysis for the constraints of g_i and d_i coefficients is taken separately.

A.1 Constraints for the drain voltage coefficients

Since

$$V_D(p) = d_1p + d_0 \quad (\text{A.5})$$

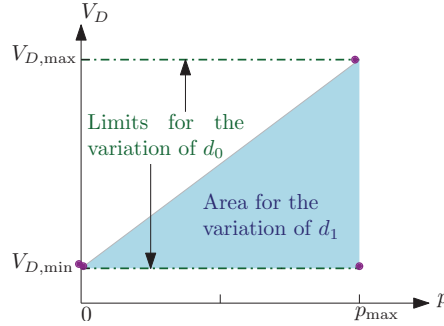


Figure A.1: Illustration of the different reference point and ranges for the determination of the constraints of the coefficients d_1 and d_0 .

is a straight line, for it to be MI it is enough that

$$d_1 \geq 0. \quad (\text{A.6})$$

From (A.5) it is clear that for d_0 to be at its maximum, V_D must also be at its maximum, while d_1 and p are at their minimum, which would imply that $p = 0$ and $d_1 = 0$ given (A.6). Then we have that

$$d_0 \leq V_{D,\max}. \quad (\text{A.7})$$

The upper bound for d_1 is found joining the points $(0, V_{D,\min})$ and $(p_{\max}, V_{D,\max})$ —see the dots in marrenta in Figure A.1—and is given by

$$d_1 \leq (V_{D,\max} - V_{D,\min})/p_{\max}. \quad (\text{A.8})$$

From eq A.4, and knowing that $d_1 \geq 0$ we know that if $V_D \geq V_{D,\min}$ for the minimum value of p (i.e. 0), $V_D \geq V_{D,\min}$ for all other values of p . Therefore we have that

$$d_0 \geq V_{D,\min}. \quad (\text{A.9})$$

This is equivalent to saying that the lower and upper bounds for d_0 are found joining $(0, V_{D,\min})$ to $(p_{\max}, V_{D,\min})$ and $(0, V_{D,\max})$ to $(p_{\max}, V_{D,\max})$, while the maximum of d_1 is found by joining the points $(0, V_{D,\min})$ and $(p_{\max}, V_{D,\max})$, as shown in Figure A.1.

A.2 Constraints for the gate voltage coefficients

Figure A.2 illustrates the reference points and ranges used to derive the constraints for g_2 , g_1 and g_0 . Using the same argument as in the previous section, we have that

$$V_{G,\min} \leq g_0 \leq V_{G,\max} \quad (\text{A.10})$$

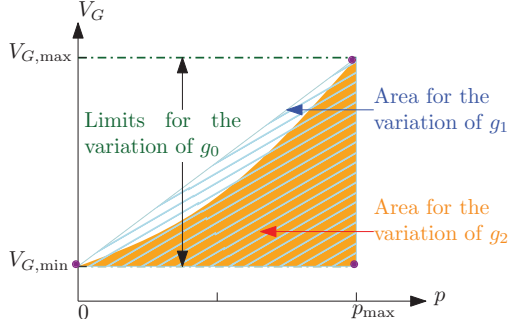


Figure A.2: Illustration of the different reference point and ranges for the determination of the constraints of the coefficients g_2 , g_1 and g_0 .

For the inflection point p^* of the function $V_G(p)$, it is by definition true that

$$dV_G(p^*)/dp = 0. \quad (\text{A.11})$$

For $V_G(p)$ to be MI in the interval $[0, p_{\max}]$, p^* must lie outside that interval. That is:

$$p^* \leq 0, \text{ or } p^* \geq p_{\max}. \quad (\text{A.12})$$

The inflection point p^* can be found from

$$\frac{dV_G}{dp}(p^*) = 2g_2p^* + g_1 = 0. \quad (\text{A.13})$$

Replacing (A.13) in (A.12) yields two possibilities;

$$g_1 \geq 0 \quad (\text{A.14})$$

or

$$-\frac{g_1}{2g_2} \geq p_{\max} \quad (\text{A.15})$$

Equation A.15 implies that a possible solution is that g_2 is negative (the parabol opens downwards), and then g_1 will have to be positive. However, a parabol that opens upwards will have lower bias consumption, and therefore yield higher efficiency, so only the case

$$g_2 \geq 0 \quad (\text{A.16})$$

is considered. Hence, (A.14) will yield the lower bound for g_1 . Just as in the previous section, the upper bounds for g_2 and g_1 are found by joining the points $(0, V_{G,\min})$ and $(p_{\max}, V_{G,\max})$ —see the dots in magenta in Figure A.2—. Because both g_2 and g_1 are positive, the coefficient g_2 is at its maximum when g_1 is zero,

and g_1 is maximum when g_2 is zero. This together with the fact that V_G is bounded is all that is needed to find the remaining constraints.

Equations A.17 to A.22 summarize the linear and bound constraints.

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & p_{\max} & 1 \\ p_{\max}^2 & p_{\max} & 1 & 0 & 0 \end{bmatrix}, \quad (\text{A.17})$$

$$\mathbf{b} = [V_{D,\max} \quad V_{G,\max}]^T \quad (\text{A.18})$$

$$\boldsymbol{\beta}_{\text{lb}} = [0 \quad 0 \quad V_{G,\min} \quad 0 \quad V_{D,\min}]^T \quad (\text{A.19})$$

$$\boldsymbol{\beta}_{\text{ub}} = \left[\frac{\Delta V_G}{p_{\max}^2} \quad \frac{\Delta V_G}{p_{\max}} \quad V_{G,\max} \quad \frac{\Delta V_D}{p_{\max}} \quad V_{D,\max} \right]^T \quad (\text{A.20})$$

$$\Delta V_G = V_{G,\max} - V_{G,\min}, \quad (\text{A.21})$$

$$\Delta V_D = V_{D,\max} - V_{D,\min} \quad (\text{A.22})$$

such that $\boldsymbol{\beta}_{\text{lb}} \leq \boldsymbol{\beta} \leq \boldsymbol{\beta}_{\text{ub}}$, and $\mathbf{A}\boldsymbol{\beta} \leq \mathbf{b}$.

Appendix B

Description of the Adaptive Random Search algorithm

The input and output variables, the constraints, and the stop criteria for the adaptive random search (ARS) algorithm are defined in Table B.1. Algorithm B.1 explains the principle of ARS. Given an error function $J(\boldsymbol{\beta})$, and given the estimate of the optimum in iteration n , $\boldsymbol{\beta}^*$, try an update $\boldsymbol{\beta}_{\text{try}} = \boldsymbol{\beta}^* + \boldsymbol{\sigma} \circ \mathbf{u}$, where \circ denotes an element-to-element product, and \mathbf{u} is a vector of random numbers with uniform distribution in the interval $[-0.5, 0.5]$. The elements of vector $\boldsymbol{\sigma}$ are scaling factors for each element in \mathbf{u} to control the search range along each dimension of $\boldsymbol{\beta}^*$. If $\boldsymbol{\beta}_{\text{try}}$ satisfies the constraints, compute its error function, and if it is lower than the error function of the current optimum $\boldsymbol{\beta}^*$, update the optimum to be $\boldsymbol{\beta}_{\text{try}}$. Else, generate another random vector and repeat the process. The stop criteria used for this case is the classic stop criteria used in optimization theory; such as the variation of the error function in each iteration, the variation of the optimized variable in each iteration, the level of the error function, and the number of iterations. The search range in each iteration can be reduced by scaling each element σ_i in $\boldsymbol{\sigma}$ by a factor λ_i in the search range contraction vector $\boldsymbol{\lambda}$.¹

¹ The element-by-element product of any two vectors \mathbf{a} and \mathbf{b} , each with M elements is defined by $\mathbf{a} \circ \mathbf{b}$, so that

$$(\mathbf{a} \circ \mathbf{b})_i = a_i b_i, \text{ for } i = 1, \dots, M$$

Table B.1: Input, output, constraints, and parameters for the adaptive random search algorithm; β_n denotes the solution of the optimizer at iteration n .

Type	Variable	Description
Input	β_0	Initial solution vector with M elements
Output	β^*	Optimized solution vector with M elements
Constraints	\mathbf{A}	Linear constraint matrix
	\mathbf{b}	Linear constraint vector: $\mathbf{A}\beta_{\text{try}} \leq \mathbf{b}$
	β_{lb}	Lower bound constraint vector
Parameters	β_{ub}	Upper bound constraint vector: $\beta_{\text{lb}} \leq \beta_n \leq \beta_{\text{ub}}$
	N	Number of iterations
	σ	Search range vector
	λ	Search range contraction vector
Stop criteria	β_{tol}	Stop if $ \beta_n - \beta_{n-1} < \beta_{\text{tol}}$
	J_{tol}	Stop if $ J(\beta_n) - J(\beta_{n-1}) < \Delta J_{\text{tol}}$
	ΔJ_{tol}	Stop if $J(\beta_n) < J_{\text{tol}}$

Algorithm B.1: Description of the adaptive random search algorithm (ARS)

```

input :  $\beta_0$ 
output:  $\beta^*$ 
1 parameters :  $N, \sigma, \lambda$ 
2 constraints :  $\mathbf{A}, \mathbf{b}, \beta_{\text{lb}}, \beta_{\text{ub}}$ 
3 stop criteria :  $\beta_{\text{tol}}, J_{\text{tol}}, \Delta J_{\text{tol}}$ 
4  $n \leftarrow 1$ 
5  $\beta^* \leftarrow \beta_0$ 
6  $J \leftarrow J(\beta_0)$ 
7 while  $n < N$ , and stop criteria not met do
8   Generate  $\mathbf{u}$ , a vector with  $M$  uniformly distributed numbers so that
    $u_k \in [-1/2, 1/2], k = 1, \dots, M$ 
9    $\beta_{\text{try}} \leftarrow \beta^* + \sigma \circ \mathbf{u}$ 
10  if  $\beta_{\text{try}}$  satisfies constraints:  $\mathbf{A}\beta_{\text{try}} \leq \mathbf{b}$ , and  $\beta_{\text{lb}} \leq \beta_{\text{try}} \leq \beta_{\text{ub}}$  then
11   Compute  $J_{\text{try}} \leftarrow J(\beta_{\text{try}})$ 
12   if  $J_{\text{try}} < J$  then
13      $\beta^* \leftarrow \beta_{\text{try}}$ 
14      $J \leftarrow J_{\text{try}}$ 
15   end
16 end
17  $\sigma \leftarrow \lambda \circ \sigma$ 
18  $n = n + 1$ 
19 end

```

Appendix C

Schematics of the gate and drain trackers

The trackers are the bias sources used to bias the power amplifier dynamically. This section presents circuit schematics for both gate and drain trackers. As explained in Section 5.1.1, the trackers that were built for this measurement system are based on linear amplification: they were constructed using operational amplifiers (op-amps)—specifically the LT1363 [72] and LM6172 [73]—and a 1.1-A current feedback amplifier to provide the large currents required at the drain (LT1210) [74]. This section presents the schematic of the gate and drain trackers.

The sources have gain and offset mechanisms to adjust the gate and drain biases to the required levels. The gate tracker outputs a negative voltage, since it is used to bias pHEMT transistors. A typical output voltage level would be a minimum of -3 V with a 1-V voltage swing. For the drain tracker the maximum output voltage of 29.5 V with a 18-V swing is limited by the absolute maximum $\pm 18\text{ V}$ biasing of the op-amps and the current feedback amplifier, as well as the slew-rate at maximum frequency (5 MHz). The drain tracker has a maximum average output current capability of 1 A. Since the gate bias functions can also be quadratic, the operational bandwidth of the gate tracker must be twice that of the drain tracker. That is why different op-amps are used for the gate [72] and the drain [73], with different gain bandwidth and slew rate specifications.

The measurement setup for the bias sources is built around the signal generator. Port A of the generator will output the RF signal that is the input to the PA, while the I and Q outputs at the back of the generator from port B will output the gate and drain normalized bias waveforms, respectively. The I and Q outputs can vary between $\pm 1\text{ V}$, but since the amplitude of the I and Q signals together should be smaller than one, they vary in practice only between $\pm 0.7\text{ V}$. The voltage amplitude into the trackers is half of that, since the tracker's input impedance is $50\ \Omega$, and the output impedance of the I/Q ports of the generator is also $50\ \Omega$. Only negative voltages are used at the gate tracker, since it is designed for depletion-mode pHEMT transistors.

The output from the gate tracker in Figure C.1 is connected to the gate bias of the power amplifier. In the case of the drain tracker, a current feedback amplifier that provides variable gain at the first stage (Figure C.2) is connected to a second stage consisting of op-amps and the current measurement system.

Two different prototypes were designed and manufactured to measure the current accurately. The first one (Figure C.3) has the DC bias component added separately to the dynamic drain bias component (i.e., the actual bias waveform) at the output of a high frequency large bandwidth transformer. The advantage with such an approach is that it greatly reduces common mode error in the current measurement since the DC and dynamic bias current components are measured separately. Unfortunately, for high output voltages the transformer's hysteresis can severely distort the drain bias signal at the output. This design was used to drive the HBT MMIC transistor, since the maximum collector bias is only 7 V [43]. The transformer in addition acts as a high-pass filter that attenuates frequency components below 50 kHz. Since the symbol rate of the test signal was 1 MHz, the error in the current measurement is small. The second drain tracker uses a 2- Ω resistor at the output of the op-amp system (Figure C.4). The instantaneous current is proportional to the voltage drop through the resistor.

The differential probe N2792A by Agilent [86] was used to measure the voltage difference at the ends of the resistor with high common mode error rejection. The probe provides a common mode rejection rate of -60 dB at 1 MHz, together with low input capacitance to minimize circuit loading [87]. The small voltage swing with bias current due to the resistor at the output is compensated by including the resistor in the op-amp feedback loop. The advantage of this second approach using a resistor and a differential probe compared to using a transformer, is that there are no high-pass filtering or nonlinear distortion effects, as was the case with the transformer. The downside is slightly higher common mode error.

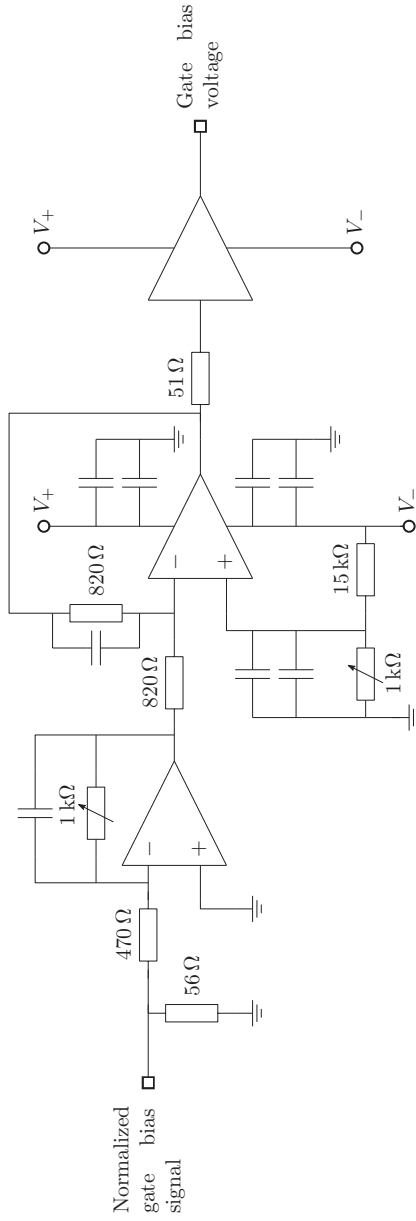


Figure C.1: Schematic of the gate tracker for dynamic biasing of an RF power amplifier. The first stage provides adjustable voltage gain, and the second stage, included for offset adjustment, gives a 20-mA output current. The third stage is the current buffer connected for a gain of one. The maximum output current is 250 mA.

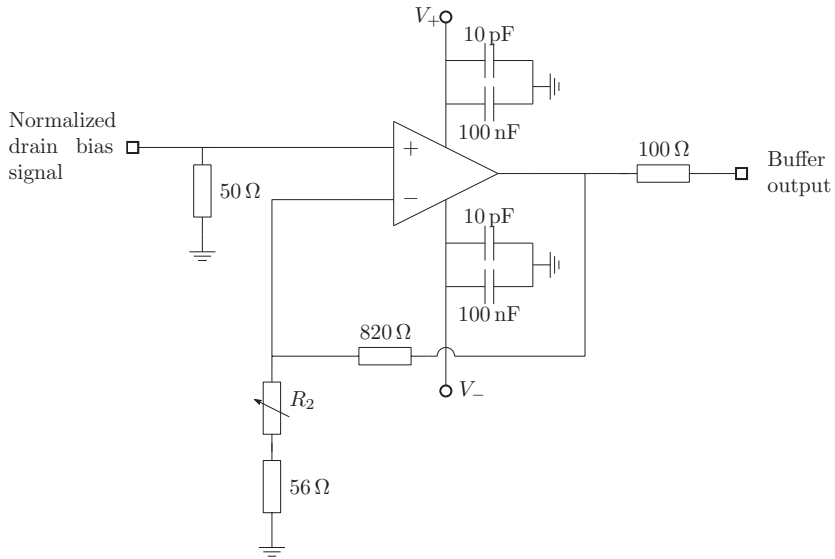


Figure C.2: Schematic of the voltage amplifier circuit based on the current feedback amplifier for the drain. Resistor R_2 makes it possible to adjust the gain.

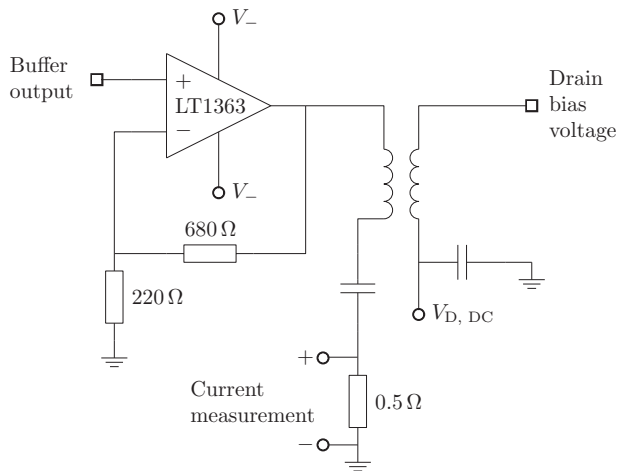


Figure C.3: Second stage of the drain tracker. A high frequency transformer is used for current measurement. The DC and AC components of the drain bias signals are input separately. The LT1363 is in charge of supplying high current. The maximum output current of the tracker is 1 A.

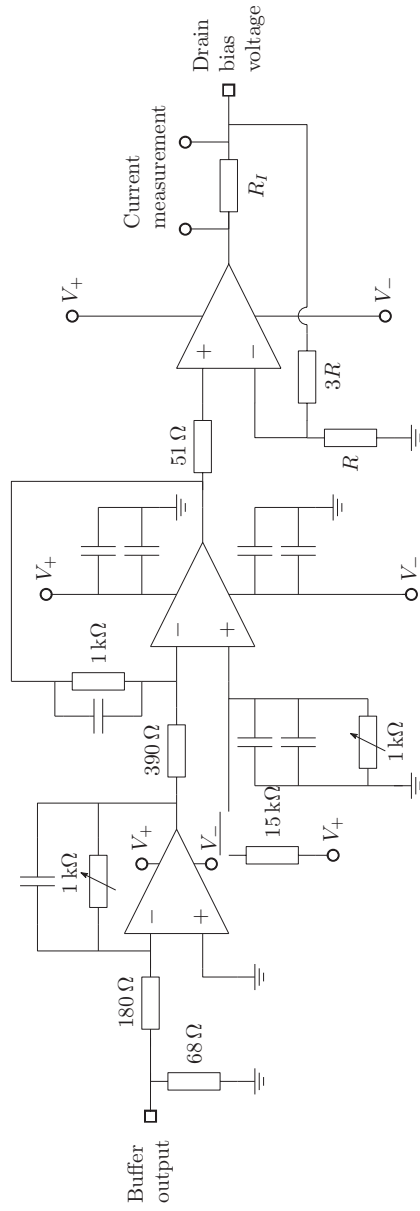


Figure C.4: Second stage of the drain tracker using a $2\text{-}\Omega$ resistor and a differential probe for current measurement. The first gain is used for gain adjustment, the second stage for offset adjustment, while the third stage with $4\times$ gain is a high current buffer. The maximum output current is 1 A . Some extra shunt capacitors parallel to the DC feed of the tracker were not included for the sake of clarity.

Appendix D

Schematics and layouts of the simulated and measured power amplifiers

The characteristics of the devices on which the amplifiers are constructed can be read from Table 5.1.

D.1 pHEMT MMIC amplifier

The schematic of the 30-dBm MMIC GaAs pHEMT amplifier is shown in Figure D.1. The two inductors and the capacitor at the drain work as an RF-choke. They provide high impedance to the RF signal but at the same time ensure that the resonance frequency is at least two or three times the operating frequency. The resistor-capacitor (RC) network ensures unconditional small-signal stability at all frequencies for the selected bias point, though the loss of the shunt inductors at the input also contribute significantly to stability. The output matching network was deliberately chosen to be low-pass to reject the harmonic components.

D.2 Discrete 33-dBm GaAs pHEMT amplifier

Figure D.2 presents a photo of the discrete GaAs PA measured in Chapter 5. The amplifier was designed for static bias class AB operation by a former member of the Radio Group at the university.

D.3 Discrete 41-dBm GaN pHEMT amplifier

Figure D.3 presents a photo of the discrete GaN PA measured in Chapter 5. The amplifier was designed for static bias class AB operation by a member of the Radio

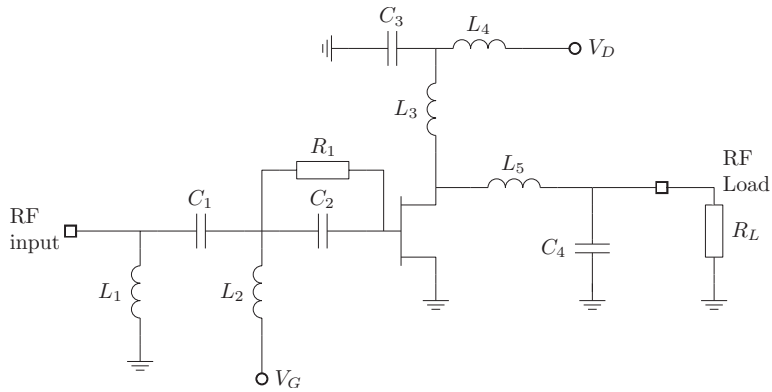


Figure D.1: Schematic of the pHEMT MMIC amplifier described in Chapter 3.

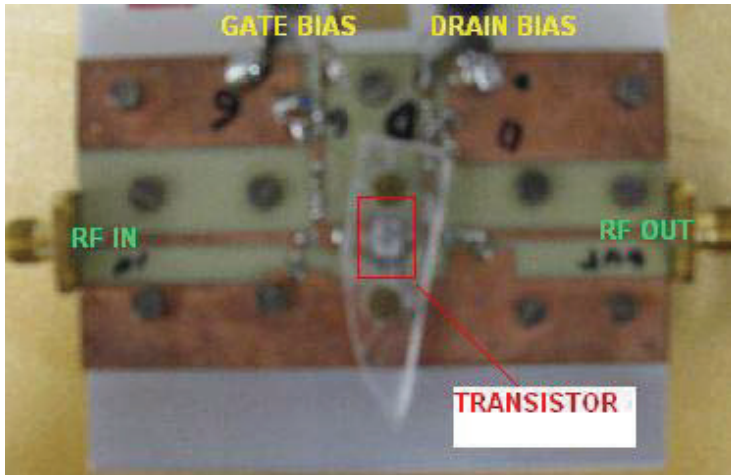


Figure D.2: Photo of the discrete 33-dBm GaAs PA measured in Section 5.3.

Group at the university, and is matched for high output power, high gain and PAE.

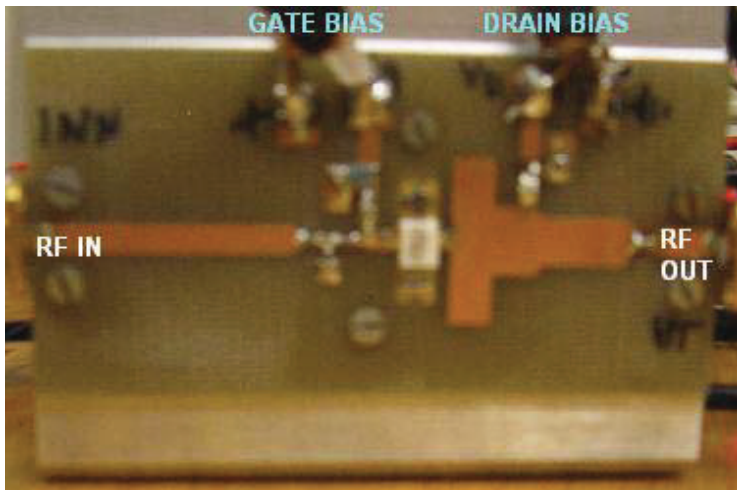


Figure D.3: Photo of the discrete 41-dBm GaN PA measured in Section 5.4.

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