

# Spec

The objective of this project is to model and design a 50MS/s, 9-bit pipelined ADC in a 3D CMOS technology.

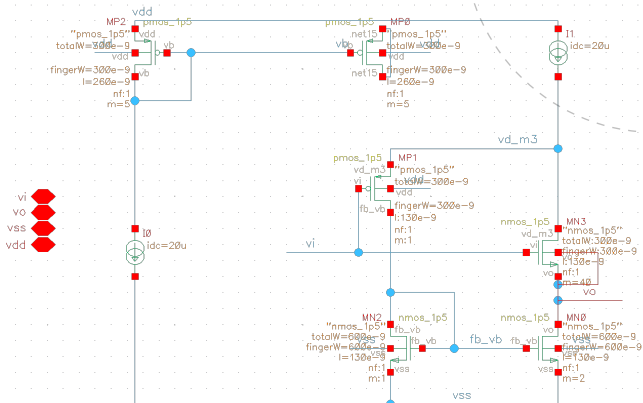
The project consists of the following tasks:

- Perform a literature survey of pipelined ADCs to establish current-state-of-the-art
- Analyze and compare published work
- Develop a behavioral model of the ADC and use the model for deriving specifications of the individual blocks
- Study the characteristics of the 3D CMOS technology
- Design the ADC at transistor level and characterize the performance by simulations
- Perform part of the layout to enable characterization of TSV parasitics and back-annotate to schematics simulations
- Input voltage:  $\pm 100mV$

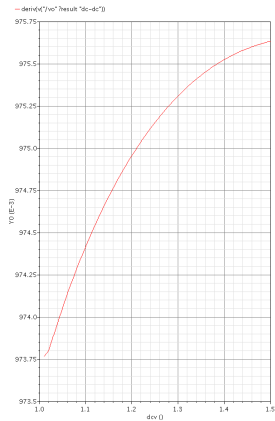
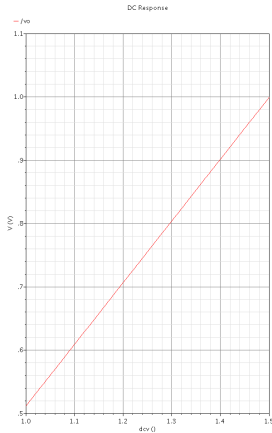
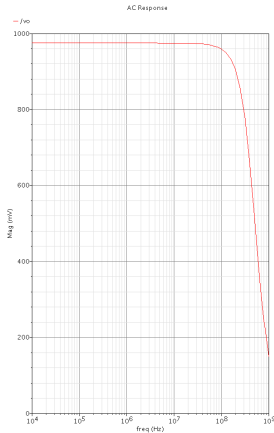


NTNU  
Norwegian University of  
Science and Technology

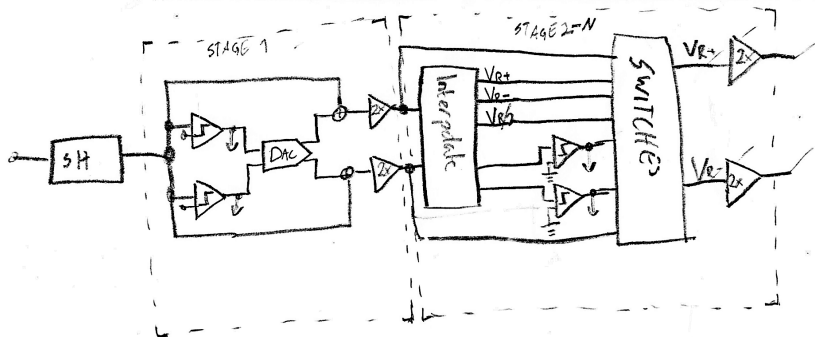
# Buffer



# Buffer results



# Topology



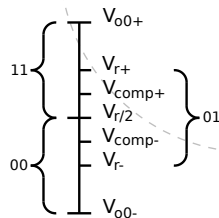
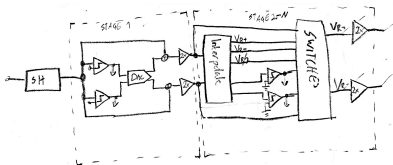
$$V_{o+,stage1} = 2(V_i - V_{Qh}) \quad (1)$$

$$V_{o-,stage1} = 2(V_i - V_{Ql}) \quad (2)$$



NTNU  
Norwegian University of  
Science and Technology

## Stage 2-N



$$V_{comp+} = \frac{5}{8}(V_{o0+} + V_{o0-}) \quad (3)$$

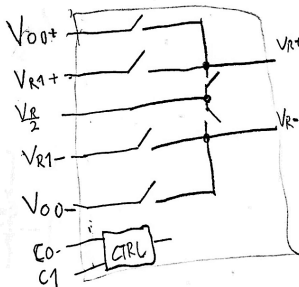
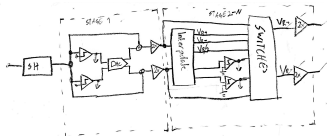
$$V_{comp-} = \frac{3}{8}(V_{o0+} + V_{o0-}) \quad (4)$$

$V_{o,stage2+}$	$V_{o,stage2-}$	code
$2 \cdot \frac{V_{o0+} - V_{o0-}}{2}$	$2 \cdot V_{o0-}$	00
$\frac{3}{4}(V_{o0+} + V_{o0-})$	$\frac{1}{4}(V_{o0+} + V_{o0-})$	01
$2 \cdot V_{o0+}$	$2 \cdot \frac{V_{o0+} - V_{o0-}}{2}$	11



NTNU  
Norwegian University of  
Science and Technology

# Switches



NTNU  
Norwegian University of  
Science and Technology