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Design of a wideband 10W GaN power amplifier

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Master of Science in Electronics
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Problem Description

In the companies developing radio equipment for wireless services and a number of universities and research centres, there is considerable activity around the theme of Power Amplifiers (PA). PA has substantial economic and technical importance because it accounts for a significant portion of the costs in both development and production of radio equipment, and is a very critical component in today's wireless world. In portable devices, it is the PA that drains the battery the most, and both the handheld and base station equipment (infrastructure) PA has to satisfy many stringent requirements. Technically good PA solutions offer a great competitive advantage.

The main topic of this thesis is to design, using a large signal model from Cree, a broadband PA.

The tasks will be to:
- Study the principles of Class B amplifier design.
- Study principles of broadband techniques.
- Learn to use the microwave simulation program (ADS).
- Simulate and design a discrete power amplifiers based on large signal model from Cree, which fulfil the specifications.
- Simulate the amplifier's characteristics (efficiency, linearity, etc.).
- Create a prototype of amplifier
- Measuring amplifier properties (bandwidth, AMAM / AMPM, efficiency etc)

Preliminary specification (10W GaN transistor from Cree)
Bandwidth: 1.5 - 3.0 GHz
Bandwidth ripple: < 1dB
Gain within the band: > 10dB
Output Power, PSAT: > 10W
Input reflection, S11: <-10dB
Efficiency: Large as possible over the whole band

Assignment given: 28. January 2011
Supervisor: Morten Olavsbråten, IET

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Thesis for the degree of Master of Science

Trondheim, July 2011

Norwegian University of Science and Technology

Faculty of Information Technology, Mathematics

and Electrical Engineering

Department of Electronics and Telecommunications

Preface

This master's thesis has been prepared by Muhammed Hakan Yilmaz during the spring of 2011 at the Norwegian University of Science and Technology. The assignment was given by the Department of Electronics and Telecommunications. The work has been interesting and challenging. I would like to thank my supervisor Associate Professor Morten Olavsbråten at Department of Electronics and Telecommunications with NTNU for all his invaluable assistance and guidance during this master's thesis. Further I would like to thank his Phd student Dragan Mitrevski for his continuous help during design and measurement in the laboratory. Also I am grateful for the guidance in ADS from Terje Mathiesen at the beginning of this thesis work.

Trondheim 5/7-2011

Muhammed Hakan Yilmaz

Abstract

There is a growing interest in transistors based on Gallium Nitride in recent years upon development of new technologies. This master thesis presents the design of a wideband power amplifier operating in the bandwidth of 1.5 – 3 GHz based on a 10W GaN-HEMT from Cree. In this paper, relevant amplifier theory, detailed descriptions of design, fabrication and measurement processes are also presented. The amplifier design was done using a large signal model from Cree in Advanced Design System. Measurement results show good accordance with simulation results for the amplifier. Typical deviations from the ideal case are however evident and various factors contributing this result are discussed in this thesis. For better correlation of simulation and measurements, accuracy of passive component models and compensation of the voltage drop in power measurement are both considered in design process. In 1 dB compression point for the fabricated amplifier, 41.43 dB of output power, efficiency (PAE) of 68.27% is achieved. Furthermore, gain is measured to be above 10 dB over the bandwidth of 2.2 GHz in small-signal measurements

Contents

Figures

Tables

Abbreviatons

ADS Advanced Design System

BFOM Baliga's figure of merit

CW Continuous Wave

DUT Device Under Test

ESR Equivalent series resistance

FET Field Effect Transistor

FM Frequency Modulation

GaAs Gallium Arsenide

GaN Gallium Nitride

HEMT High Electron Mobility Transistor

LNA Low Noise Amplifier

NF Noise Figure

NPO Negative Positive Zero

PA Power Amplifier

PAE Power Added Efficiency

RF Radio Frequency

1. Introduction

RF Power Amplifier is an integral part of modern wireless infrastructure. For a given amplifier, in order to meet the specific requirements, new and innovative transistor technologies must be implemented since the new wireless communication systems are increasing in numbers, thus these requirements have become tougher to achieve. The key features while designing an amplifier are wide bandwidth, improved efficiency, high output power, reliability, good thermal performance and gain of the amplifier.

High power and frequency applications require transistors based on semiconductor materials with both large breakdown voltage and high electron velocity. Development of a variety of these technologies such as SiC MESFETs, GaAs heterojunction bipolar transistor, GaAs metal-semiconductor field effect transistor (MESFETS) and Gallium nitride high-electron mobility transistor (GaN) are introduced for this purpose [1]. Gallium nitride based transistors have excellence over the conventional materials and the performance comparison of this type of transistors with other materials is studied further down.

One of the most significant features of GaN is the high power density. This allows not only the production of smaller device with same output power, but also provides much higher impedance. Higher impedance enables users to match it to the system much easier, eliminating the extra cost and complexity needed for other conventional elements such as GaAs. In addition to this, high-voltage properties reduce the need of voltage conversion, leading to higher efficiency operation which in return results in power saving and reduced costs for cooling the system [1]. On the other hand, high frequency operation of GaN device adds an advantage for the bandwidth requirements as well.

The design is done by simulations based on a large signal model from Cree in Advanced Design System (ADS) and an implementation based on this design is made. Further, measurements were carried out in the laboratory with the fabricated amplifier.

The task is structured such that it starts with a chapter explaining theory about amplifiers briefly. Further discussion covers the methods for design, fabrication and measurement processes. Measurement results, discussion and conclusion are also presented at the end of this thesis.

2. Theory

This part contains several theoretical aspects for this project. The theory is elaborated categorically through following chapters below.

- **RF Amplifiers** Introduction chapter for basic principles of RF amplifiers and some important parameters in the RF PA structure.

- **Amplifier Classes** Further analysis on some common power amplifiers with a focus on Class B and Class AB modes, comparison of the PA modes in terms of efficiency, linearity, usage is explained.

- **Design Guide** In this section, explanation of different components that were used in the task is given.

- **Design theory in ADS** Further theory explanation of bias network, stabilization and matching networks and implementation of these in ADS is given.

- **Calibration** Different error types and calibration standards in order to minimize these errors are outlined in this section.

2.1 RF Amplifier

A technical definition for RF PA might be a circuit that is consuming DC power circuit in order to deliver maximum RF/microwave output power. It consists of the transistor and matching parts for the input and output required for impedance transformation and biasing networks which are discussed later in the chapter.

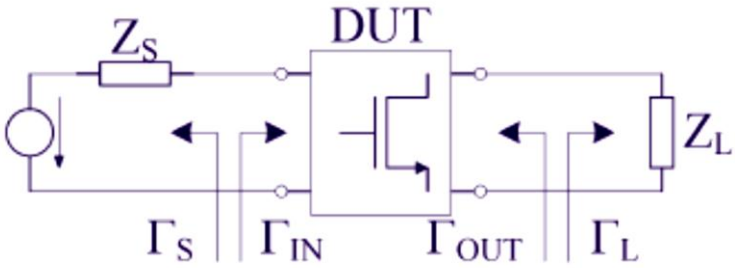

Figure 2.1: Power amplifier basic schematic

2.1.1 Transistor.

This active device is used to have an amplified input signal at the output depending on the specific requirements for the amplifier design. The Cree transistor model used in this thesis allows having a broadband solution and operates from a 28 Volt rail with high efficiency.

2.1.2 Matching Networks

These networks are designed for impedance transformation, typically between the transistor and 50 Ohm terminations on the input/output of amplifier. They might be designed with lumped elements, quarter wave transformers or micro strip stubs. Generally, input matching side provides for the maximum power transfer, which occurs according to complex conjugate theorem and gives low input return loss [2]. On the other hand, output matching network is designed according to requirements and matching the device to the output side is not always the case. For instance, loss of half the power happens on maximum power transfer and high efficiency cannot be ensured [3].

2.1.3 Biasing network and stability

Active device, in this thesis which is transistor, requires DC-bias in order to operate in the active region. Appropriate bias point is one of the most critical aspects in PA design. The bias network not only defines the PA performance over RF drive, but also does over temperature, and presented with two DC voltage supplies connected to the active device through microstrip lines as shown later in this paper [4].

Stabilization circuit is also required to prevent the PA from entering oscillation. Negative impedance seen looking into the ports of either input or output results in oscillation. Instability can damage and even destroy the active device, thus oscillations in RF may take form in the lower frequency side of the desired bandwidth and can be avoided with decreasing the gain in low frequencies.

2.1.4 Important parameters in PA design

The diagram below shows the PA for the reduced conduction angle analysis and based on harmonic termination assumption which is depicted as parallel resonant circuit. In this circuit, drain voltage to generate maximum voltage swing depends on the load resistor R_L but not the harmonics of load since the resonant circuit is used for shortage of harmonics, hence harmonics does not generate any voltage. This circuit will be the reference for further discussion of the important parameters in this chapter.

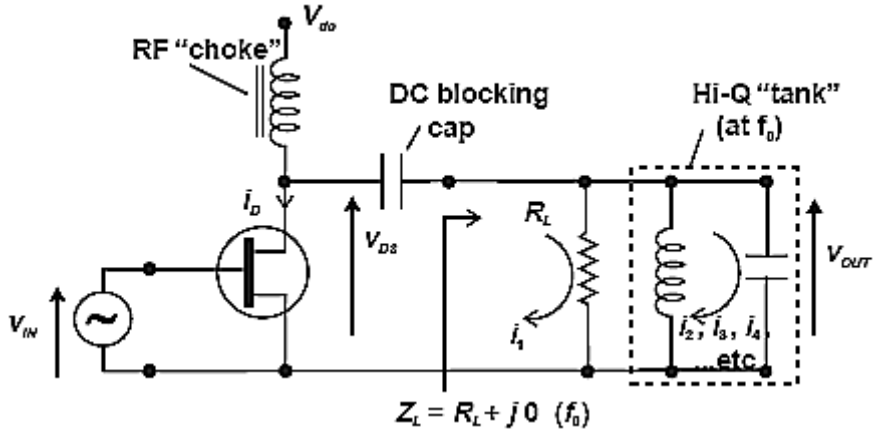

Figure 2.2: Class AB amplifier [5]

Drain Efficiency

As stated before, PA is a DC power consuming device; hence the amplifier efficiency is one of the important parameters that are to be considered. This efficiency is the ratio for FET devices clearly; its appellation is given as a result of DC input power at the drain port [6]. It is defined as the ability of converting the DC power to the RF power at the output:

$$\eta = \frac{P_{OUT}}{P_{DC}} \tag{2.1}$$

However, Power Added Efficiency, PAE, takes into account the required RF drive power defined as P_{IN} and gives more accurate amplifier efficiency, which is illustrated below:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{2.2}$$

In practice, the drain efficiency is slightly more than the power added efficiency, considering the given input RF power. Applications with amplifiers having infinite gains will have equal drain and power added efficiency. For the specific case of this thesis work, the gain of the amplifier is at a finite value of dB and the drain efficiency is typically higher than PAE.

DC supply power used in formulas above can be written as:

$$P_{DC} = V_{DC}.I_{DC} \tag{2.3}$$

Note that, DC power depends on the voltage and current at the drain port in accordance with the fact that $I_D \gg I_G$.

1 dB compression point

At low-level input signals, an amplifier has a constant gain and linear behavior. However, as the input levels increases, amplifier gets saturated and the output signal will no longer increase proportionally with the input signal. The input power level where the amplifier has a 1 dB less linear gain due to saturation is defined as 1 dB compression point and it is considered as an important parameter for the linearity of a PA.

2.2 Amplifier Classes

Power Amplifiers are generally divided into two main categories: linear and non-linear amplifiers [7]. These two categorized amplifiers can be distinguished because of their linearity, efficiency and circuit topologies. Linear amplifiers tend to preserve the waveform shape of the input signal at the output, while nonlinear amplifiers has inevitable distortion in the signal and are suitable for constant envelope signals such as FM, CW. Amplifier classes have unique bias levels for their objectives and has their own trade-offs [4]. The most common linear amplifier classes are A, B, AB; while class A being the most linear of all amplifier types. The main nonlinear amplifier classes are C, D, E, F, G, H and S [7]. Some linear PA class theories and the reduced conduction angle analyses are discussed further down.

2.2.1 Class A

In this class, transistor is biased in the exact mid-point of the linear range so that the current at the output flows during the entire cycle of the input signal, and the drive signal is kept within certain values so that the transistor will not fall into cutoff or saturation region thus conduction angle of the transistor being 360 ˚. Since the transistor always conducts, there is no necessity for turn-on region, resulting of improved charging storage. Class A amplifiers also extends to have a better high frequency performance compared to other type of power amplifiers and less evident high-order harmonics as it is shown later in this thesis. The quiescent point of this class is shown at the Figure 2.3 below and the amplifier clearly operates in the linear region, so the signal distorted minimally. Because the efficiency of this class is %50 theoretically, the class A power amplifiers are mainly used in applications with low-power levels, requiring high gain. Hence, class A amplifiers will have major effect on high power applications through its power consuming property. This is the main disadvantage of this type amplifier, as it costs significantly more to generate power supply at high power levels. On the other hand, these types of amplifiers are the most linear and the least complex compared to other type of power amplifiers.

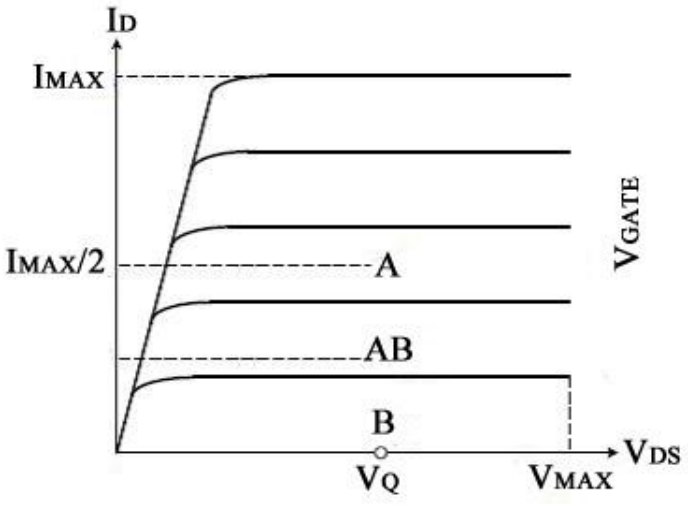

Figure 2.3: Bias points for common PA modes

2.2.2 Reduced Conduction Angle Analysis

Conduction angle is defined as the fraction of the wave period in which the given active device is conducting, knowing the fact that a full cycle of a sinusoidal waveform can be considered as 360˚. For instance, in Class-A PAs this angle is 360 ˚ as explained before, since the transistor is conducting during the entire cycle. For basic reference, bias points and corresponding conduction angles for common PA modes are given in table 2.1 below.

Table 2.1: Reduced Conduction Angle for some PA modes

Mode	Bias Point	Quiescent Point	Conduction Angle
A	**0.5**	**0.5**	**2π**
B	**0**	**0**	**π**
AB	**0-0.5**	**0-0.5**	**π-2 π**
C	**< 0**	**0**	**0-π**

Reducing the conduction angle, one can predict useful improvement in efficiency and the concept behind this process is analyzed using figure 2.4. For this analysis, it is illustrated that the conduction angle can be reduced by moving the device bias point toward cut-off from Class-A condition shown in Table 2.1. Looking at this figure, an adequate portion of RF

drive will cause the input voltage V_g fall below the threshold voltage which is given as V_t in this figure and as a result of this some part of the current is cut off. In order for the current to be able to swing up to maximum saturation point (I_{MAX}), RF drive level must be increased in relation to Class-A condition and the device is assumed to be transconductive [5]. The quiescent voltage point for this process is depicted in figure 2.4 below as V_q.

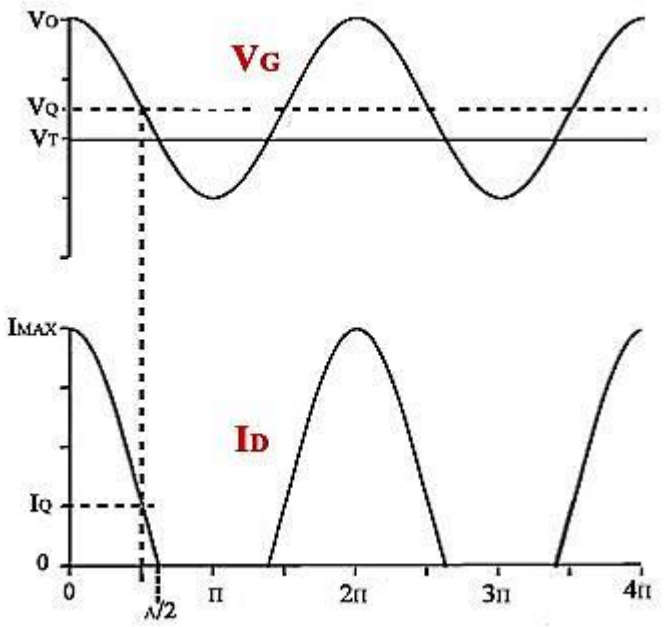

Figure 2.4: Reduced conduction angle waveforms

Input signal voltage needed for the maximum swing and quiescent bias point are represented as V_S and V_q respectively. The relation between these are given in (2.4) as V_q is a normalized quantity in this formula and defined according to (2.5).

$$V_S = 1 - V_q \tag{2.4}$$

$$V_t = 0, V_o = 1 \tag{2.5}$$

According to (2.4), alteration of bias point results in increased signal voltage so that maximum current swing can be achieved. In order for the device to be turned on, voltage at the output needs to be above zero as another assumption being made in [5].

An apparent result of reduced conduction angle is decreased DC power; however studying Fourier analysis of drain current waveform as a function of α (conduction angle) which can be found in [5] is needed to see the overall picture of fundamental component clearly. In addition to fundamental component, there will be harmonics generated.

Different components can be found by solving the integration of I_D and given by (2.6).

$$I_n = \frac{1}{2\pi} \int_{\frac{-\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{max}}{1-\cos(\alpha/2)} (\cos(\theta) - \cos(\alpha/2))\cos(n\theta) d\theta \tag{2.6}$$

The resulting fundamental and DC component from Fourier analysis are given in (2.7) and (2.8)

$$I_{DC} = \frac{I_{max}}{2\pi} \frac{2.\sin(\alpha/2) - \alpha.\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{2.7}$$

$$I_1 = \frac{I_{max}}{2\pi} \frac{2.\sin(\alpha/2) - \alpha.\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{2.8}$$

Integral solution of DC current component in (2.7) is found by letting n=0 and for 1st harmonic in (2.8) n = 1 and so on. Examining the result from the integral of (2.6) more precisely up to n=5 is shown in Figure 2.5 below.

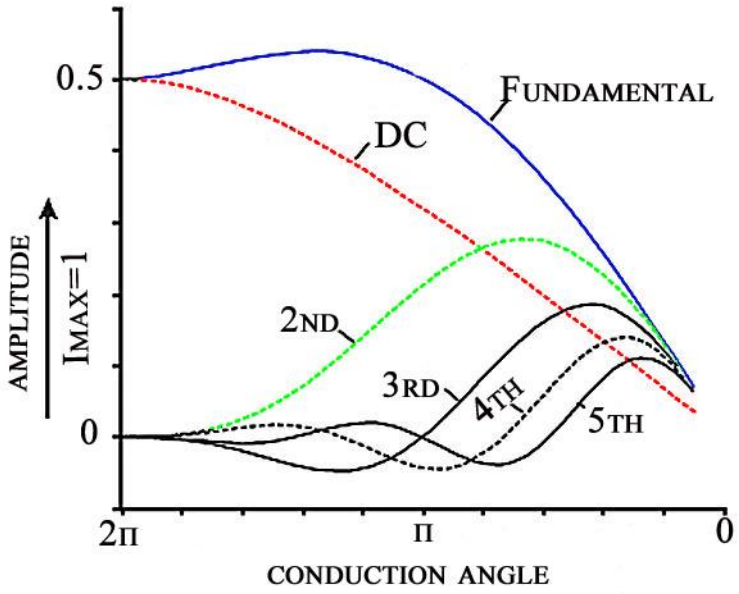

Figure 2.5: Fourier components of I_D

According to Figure 2.5, it is obvious that most PA contains second harmonic component, some having significant 3rd for instance in the case of Class-C, leading to a complex voltage analysis. Therefore, the assumption of short circuited harmonics is preferred for simplicity. Another conclusion from the figure above is that for Class-A and Class-B PAs, fundamental component is equal.

Using this assumption shows that harmonics generate no voltage for this analysis, the below figure represents the output power and efficiency results for different conduction angles. Thus the fundamental power at the output can be calculated according to (2.9). It is also noted that efficiency tends to get higher as the conduction angle goes to zero in figure 2.6.

$$P_{OUT} = \frac{V_{DC}}{\sqrt{2}} \cdot \frac{I_1}{\sqrt{2}} \tag{2.9}$$

DC supply power in this formula is given by (2.3) before in Drain Efficiency section. Hence using the formulas given in (2.7), (2.8) and (2.9), efficiency can be calculated and is plotted below in figure 2.6 as a function of conduction angle.

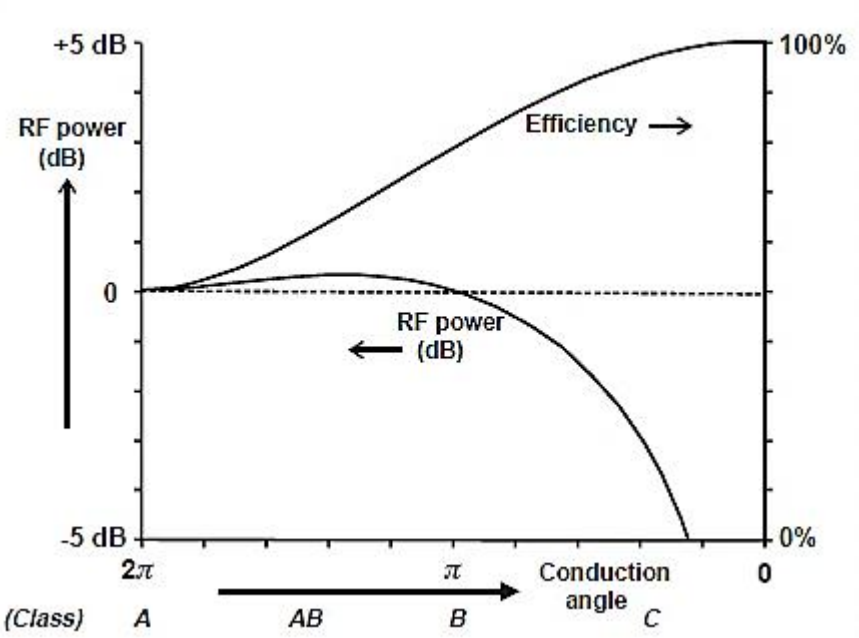

Figure 2.6: Efficiency as a function of conduction angle

As it is clearly seen in the figure, reducing conduction angle gives better efficiency, which is defined as the ratio of fundamental output power to the DC supply power. For instance, efficiency for a class A power amplifier is at 50%, while it increases substantially with reducing conduction angle and reaches to 78.5% for a class B amplifier.

2.2.3 Class B

In class B amplifiers, the conduction angle is 180˚, meaning the transistor conducts either positive or negative half cycle of the input signal, independent of drive level. Analogously, DC bias applied to device determines the class operation; quiescent point at cutoff for this class is shown in figure 2.3. The device is assumed to be linear beyond threshold voltage and harmonics are shorted at the output, hence fundamental load is resistive according to the assumptions while defining class B amplifier. For an ideal case of class B PA, the efficiency is improved to 78.5% compared to class A, however the trade-off for this improvement is less linearity, since class B amplifier have harmonic contents in the amplified signal which is explained briefly below. The harmonic components for this type of amplifier can be seen in Figure 2.5.

The results from the Fourier explanation for class B are:

$$I_{DC}(ClassB) = \frac{I_{MAX}}{\pi} \tag{2.11}$$

Similarly, dc component for Class-A can be derived using (2.12):

$$I_{DC}(ClassA) = \frac{I_{MAX}}{2} \tag{2.12}$$

This result denotes a reduction by a factor of $\pi/2$, considering the equal fundamental component is equal for both classes. This reduction factor leads to increased efficiency of 78.5% since the efficiency given by (2.2) is a function of DC component. Further analysis on figure 2.5 shows that linearity is decreased reasonably compared to Class-A. Hence, close harmonic components for this class amplifier appear and need to be terminated. On the other hand, for an ideal case odd harmonics are equal to zero.

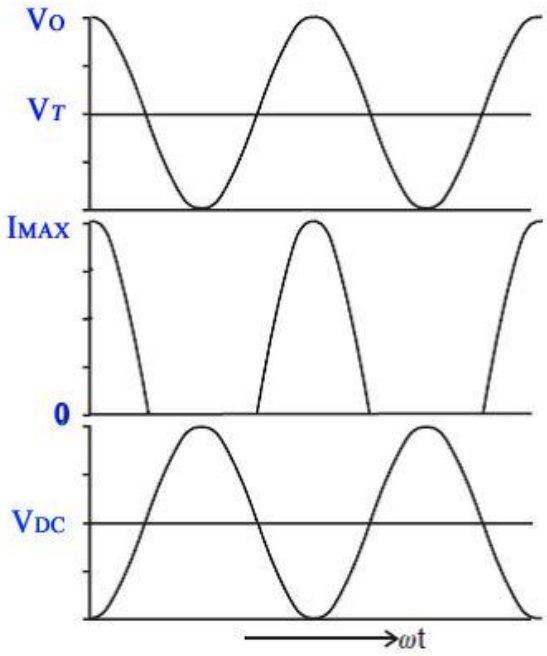

Figure 2.7: Class B waveforms

2.2.4 Class AB

A class AB amplifier is a nonlinear amplifier, a compromise between class B and class A regarding to efficiency and linearity parameters and operates between two edges defined for these two amplifiers. For ideal case, an operating class AB mode is biased to a quiescent point, which is in the region between the cutoff point and the bias point of class A. It has a quiescent drain current of between 0.1 and 0.2 I_{DSS} [8]. Efficiency is improved compared to class A PA, but still less than 78.5% by virtue of conduction angle in this class is between 180 and 360, considering the fact that the efficiency is linked with the conduction angle since the fundamental current is a function of it by (2.11). Unlike class B amplifier, the conduction

angle for a class AB amplifier being a function of drive level results in distortion of amplitude modulated signals at their peak power level [9]. Applications with class-AB often utilize wider dynamic range than the two linear PA discussed above. The reason is in fact the diversity of source that causes the gain compression in these mentioned PAs.

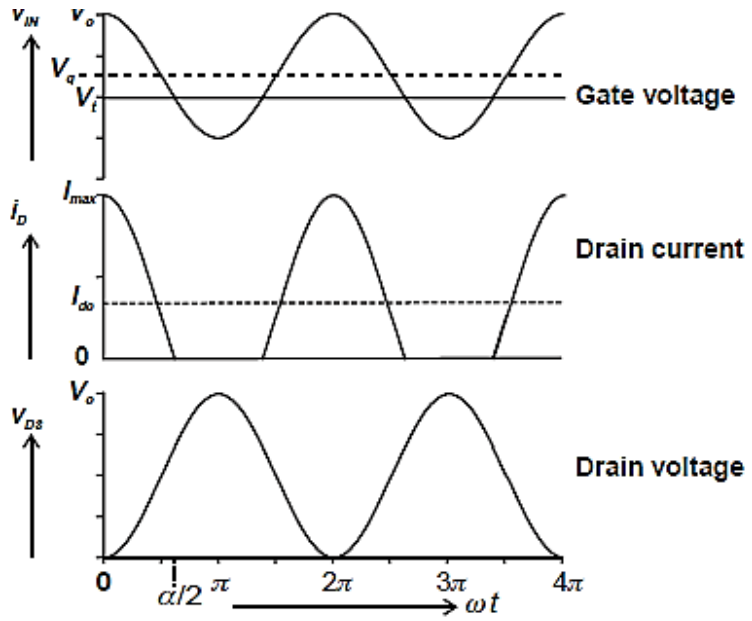

Figure 2.8: Class AB waveforms

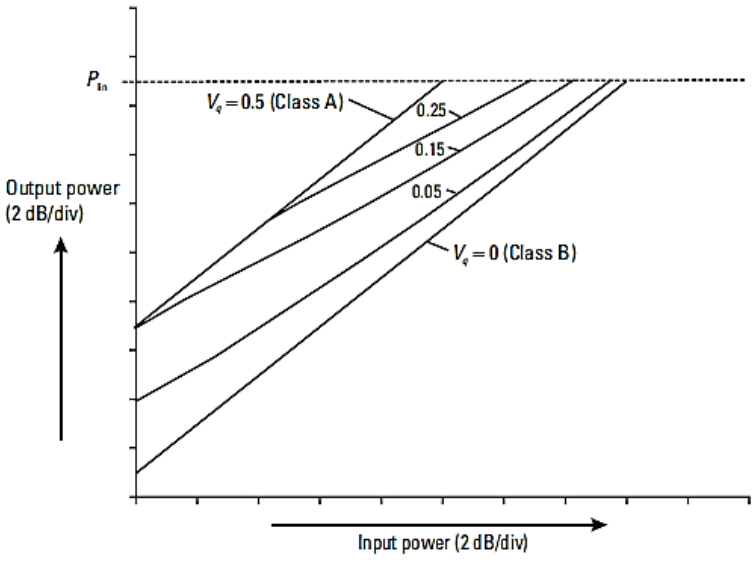

Figure 2.9: Class AB gain characteristics [10]

For further linearity observation a figure of linearity for different PA modes, which obviously indicates the gain compression for class-AB mode, is given above in Figure 2.9. This gain compression, however, arises from a different source than a class A amplifier which

experience this reduction of gain in saturation region. As a design criterion, quiescent bias voltages of 0.25, 0.15 and 0.05 in the figure correspond to class AB condition. As it is shown in figures above for class AB waveforms, truncated input signal causes odd degree harmonics which is not a desirable effect in power amplifier design. The nonlinearity of class AB mode observed for low input levels in Figure 2.9 is caused by another kind of distortion which needs to be considered elaborately [10].

2.3 Design Components

2.3.1 Cree transistor

The active device used in this thesis is a 10W Gallium nitride based High electron mobility GaN-HEMT transistor from Cree (CGH4010F), a large signal model and has following features [11].

- 28 V Operation
- Up to 6 GHz operation availability
- Small signal gain of 16 dB at 2.0 GHz
- Small signal gain of 14 dB at 4.0 GHz
- Saturated Power of 13 W and 65 % Efficiency at this level

It is used in variety of RF and microwave applications, such as Broadband amplifiers (a requirement for this thesis), cellular infrastructure and test instruments. Its capability of high gain and efficiency makes it ideal for linear amplifier circuit designs. Thanks to wide bandgap of GaN, power density of the material is 10 to 20 times higher than GaAs-based devices. Hence the GaN components are much smaller and exhibiting low capacitance characteristics [12]. The following table shows the comparison of Power Electronic materials with GaN material.

Table 2.2: Comparison of High Power Materials [1]

Material	μ	ε	Eg	BFOM ratio	JEM ratio	Tmax
Si	**1300**	**11.4**	**1.1**	**1.0**	**1.0**	**300 C**
GaAs	**5000**	**13.1**	**1.4**	**9.6**	**3.5**	**300 C**
SiC	**260**	**9.7**	**2.9**	**3.1**	**60**	**600 C**
GaN	**1500**	**9.5**	**3.4**	**24.6**	**80**	**700 C**

Results of these material properties let GaN exhibit performance superior to other competing materials listed above. Some of these performance advantages of GaN, with important ones highlighted are given in Table 2.2.

Table 2.3: Performance analysis of GaN material [1]

Need	Enabling Feature	Performance Advantage
High Power/Unit Width	Wide Bandgap, High Field	Easy to Match
High Linearity	HEMT Topology	Optimum Band Allocation
High Voltage Operation	High Breakdown Field	Reduce Step Down
High Frequency	High Electron Velocity	Bandwidth
High Efficiency	High Operating Voltage	Power Saving, Reduced Cooling
Low Noise	High Gain	High DR receivers
Thermal Management	SiC Substrate	High Power Devices with Reduced Cooling Needs
High Temperature Operation	Wide Bandgap	Reliable, Rugged, Reduced Cooling
Technology Leverage	Direct Bandgap Enabler for Lighting	Driving Force for Technology/ Low Cost

2.3.2 Microstrip

The type of the transmission lines and stubs used for this thesis is microstrip, built on FR-4 substrate. It is defined as MSUB component, length and widths of microstrip lines in this thesis are calculated through LineCalc tool in ADS design. For this thesis, specifications given for parameters defined compatibly with the configuration of Figure 2.10 can be seen below.

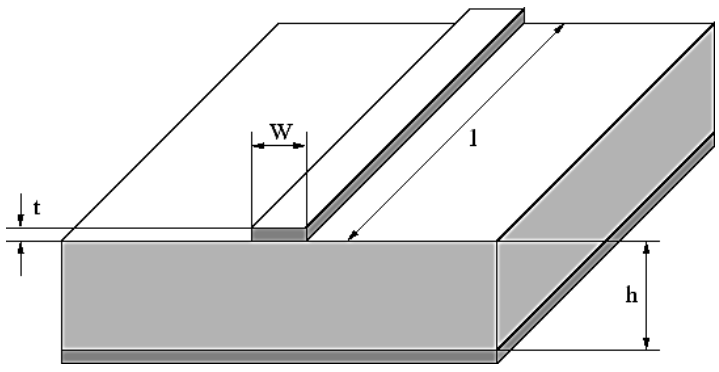

Figure 2.10: Microstrip line model [13]

- h = 1.6 mm (Substrate thickness)
- $\varepsilon_r = 4.3$ (Relative dielectric constant)
- t = 35 um (Conductor thickness)
- tanD = 0.02 (Dielectric loss tangent)
- Mur = 1 (Relative permeability)

2.3.3 Capacitor

For this thesis, The JTI0603 component from S-Series R14S capacitors of Johanson is used. These types of capacitors provide a capability that was unavailable previously: Very-high Q factor and NPO temperature-characteristics. The simulation has been made with the capacitance values provided in the Johanson manufacturer webpage and datasheets. ESR, capacitor's parasitic reactance and Quality factor are important parameters regarding to chip capacitors for high frequency applications. Q factor can be found by dividing capacitor reactance with ESR value. Since both reactance and ESR depends on the working frequency, Q factor is also a function of frequency [14].

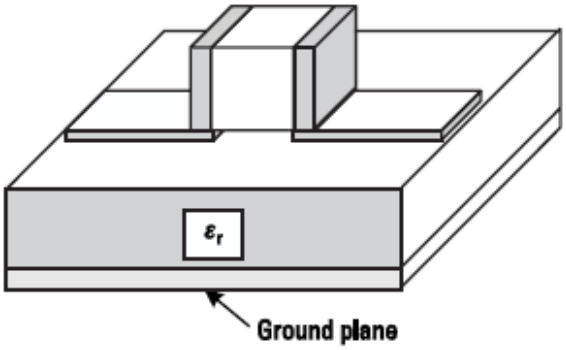

Figure 2.11: Series mounting of a chip capacitor in microstrip [13]

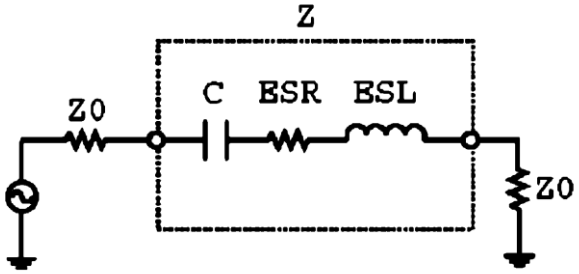

Figure 2.12: EC representation of a capacitor model [13]

A ceramic multilayer capacitor can be modeled with a basic RLC circuit with 50Ω reference impedance shown above in Figure 12, which is justifiable in RF frequencies. In this model, C represents the approximate capacitance of the component, while L and R stand for inductance and resistance, considered for propagation delay and losses in the component respectively. Studying the model above shows that ESL, Effective Series Inductance, is an important Figure of Merit for the first resonance of the capacitor and has its value around 1 nH, while ESR resistance is 0.1 Ohm for most capacitors and it's a turning point for High Power circuit designs and filters with high Q factor [15].

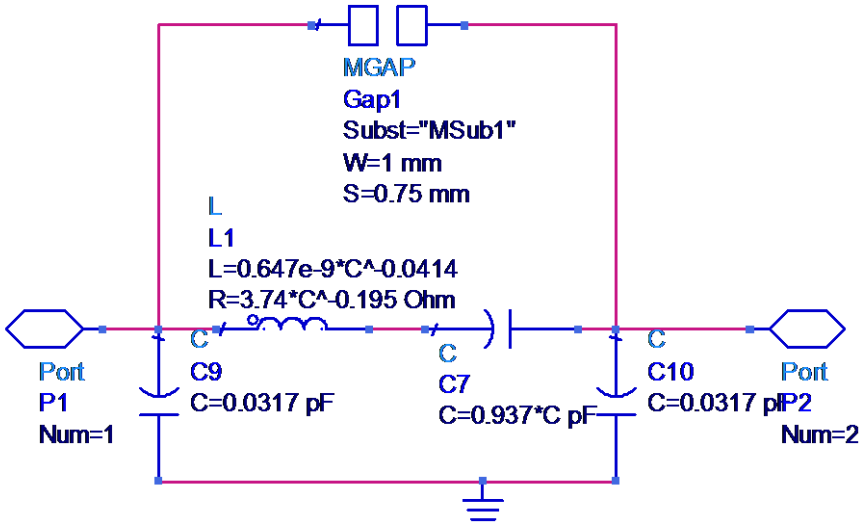

Figure 2.13: ADS representation of capacitor model CapJT used in the design

2.3.4 Resistor

The resistor used in this thesis work is a surface-mounted metal-film resistor from RK73 series of KOA in 0603 image size. These types of resistors generally have a tolerance of ±1% and can handle high power levels.

2.4 Design Theory in ADS

2.4.1 Bias-Network

Bias network is used for transmitting desired voltage and current to the amplifier. A bias line is a component that should have high impedance so as not to load down the main line. Using transmission type of bias lines, there is one frequency where it precisely looks like high impedance, which is 2.25 GHz for this thesis work. Basic concept of the bias network is shown in Figure 2.2. Power supply is applied through RF choke which blocks RF from reaching DC supply as it has high impedance at the fundamental frequency (2.25 GHz). However, biasing may be realized using microstrip components such as $\lambda/4$ lines and stubs which will be elaborated later in this thesis. The main idea of the bias network is blocking RF from preventing DC whilst supplying power supply and blocking all harmonic components. Since the power amplifier designed for this thesis is required to be broadband, microstrip butterfly stub is preferred for its large bandwidth of stop-band ability through its adjustable wings [16]. The bias circuit is simulated and results are shown in figure 2.14.

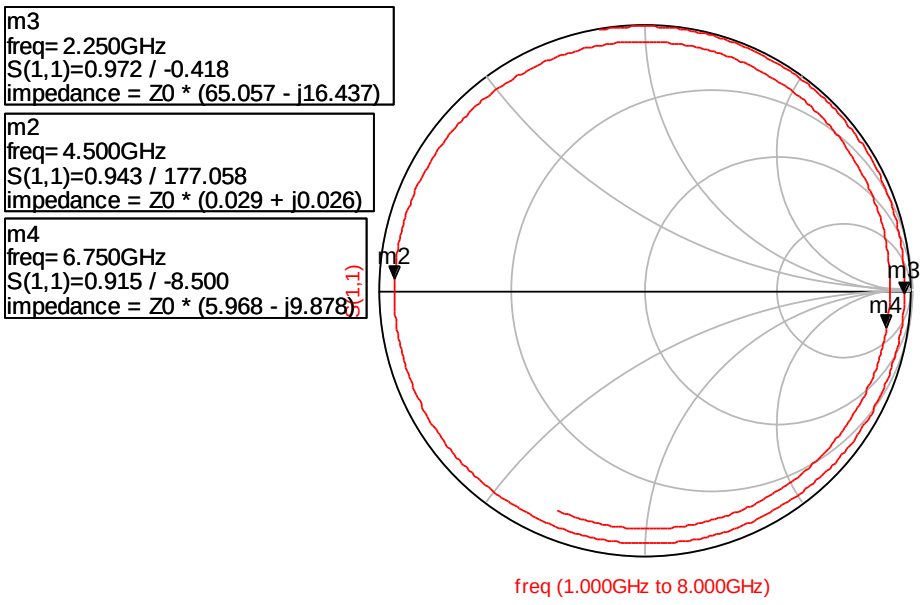

Figure 2.14: Resulting impedance values of center frequency component, its relevant second and third harmonics in bias network

Furthermore, bias circuit for the amplifier consists of a quarter-wave line and a butterfly stub. The principle of bias network designed for this thesis will be illustrated further in ADS Design chapter in detail. The main idea of this bias circuit is to have RF open in the node where RF signal is being fed while having RF short in the second harmonic component which corresponds to marker m2 in figure 2.14. Marker m4 indicates open circuit for third harmonic component.

Stability factors

As it is said before in this paper, stability is one of the most important criteria's that should be considered in amplifier design. In two-port systems, oscillations occur when resistance at the input or output ports are negative. This can be determined calculating two parameters defined below [17].

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$K = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{12}S_{21}\right|}$$

A two-port network can have any value of Rollett's stability factor K, which is calculated using a set of S parameters at the working frequency, and value of Δ parameter that is chosen out of some other parameters as reference in this paper; however most transistor are either unconditionally stable or conditionally stable regarding stability. These two stability conditions and necessary and sufficient conditions are explained below:

- Unconditional Stability. A network if, for all passive load and source impedances, input and output impedances (Z_{in} and Z_{out}) present positive resistance, is defined as unconditionally stable network, hence no oscillations occur. This can be verified if $K < 1$ and $\left|\Delta\right| < 1$ condition is hold.
- Conditional Stability. A network that has passive load and source impedances which can cause oscillations due to negative input or output impedances as a result of mismatch [18] and can be verified when $K < 1$ and $\left|\Delta\right| < 1$.

Stability test must be evaluated at all frequencies in which oscillations can occur and the stability parameters are calculated in ADS using the design guide provided as SP_NF_GainMatchK.

Below figure shows the simulation results from the GaN transistor without stabilization network and stability factors are clearly less than one at some frequencies which may result in oscillations, hence the device needs to be stabilized. Note that, mu_load and mu_source are the stability parameters in ADS that needs to be more than one for unconditional stability case.

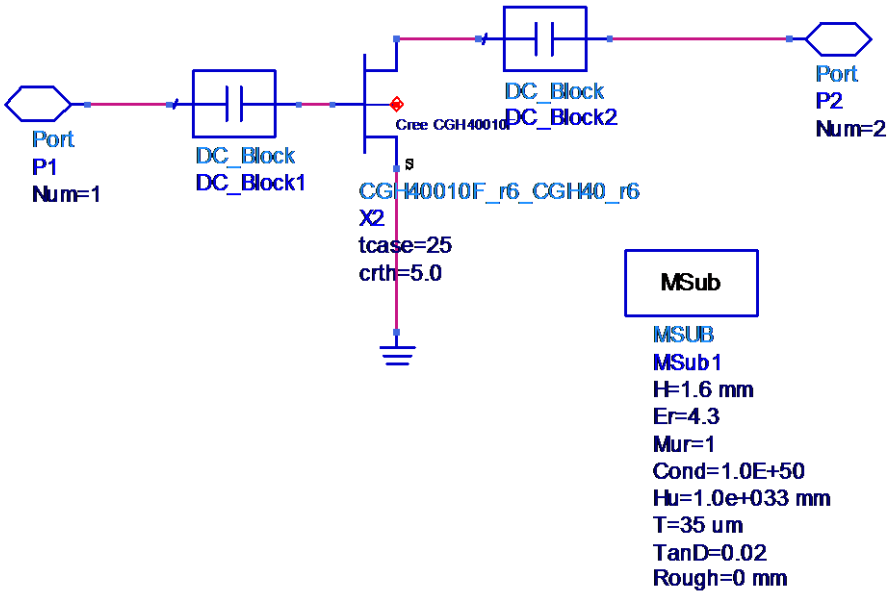

Figure 2.15: Simulation of the device without stability network

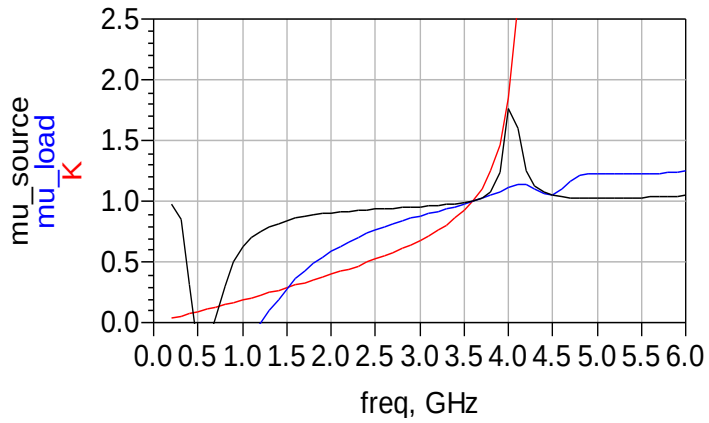

Figure 2.16: Stability factors from simulation results of the design in Figure 2.15

2.4.2 Stability circuits

Unconditional Stability can be ensured by adding a stability network to the device. A stability network may be composed of series or parallel loading with RC-RL circuits or series and parallel feedback at the input or output of the active device and depends on the application and amplifier type. For instance, in the case of a LNA, resistive stability network at the input may cause NF reduction; however for PA applications, resistive loss may be introduced at the input of transistor as noise figure does not need to be considered. In order to get the desired stability, combination of these networks might be needed [19].

Two stabilization networks, which are explained below, are evaluated in order to stabilize the circuit and the results from simulations of these networks respectively are given in the Figures 2.17 and 2.18.

- Parallel RC circuit. Composed of a resistor and a capacitor in parallel, this circuit acts like a High Pass Filter and introduces loss, stability for low frequency components ($f < \frac{1}{2\pi fC}$) while passing high frequencies unattenuated. The reason is in fact that the reactance of the capacitor is high at these lossy frequencies, hence capacitor behaves like open circuit for input signal driven at these frequencies. The result of this circuit is indicated by blue line. This circuit is used in this amplifier design in order to introduce loss for low frequency side of the bandwidth since the result found in figure 2.16 indicates this to stabilize the device.

- Series RC circuit. Composed of a resistor and a capacitor in series, this circuit introduces losses at high frequencies $f > \frac{1}{2\pi fC}$ and it is illustrated with the plot of S(2,1) in figure 2.18 represented by red line.

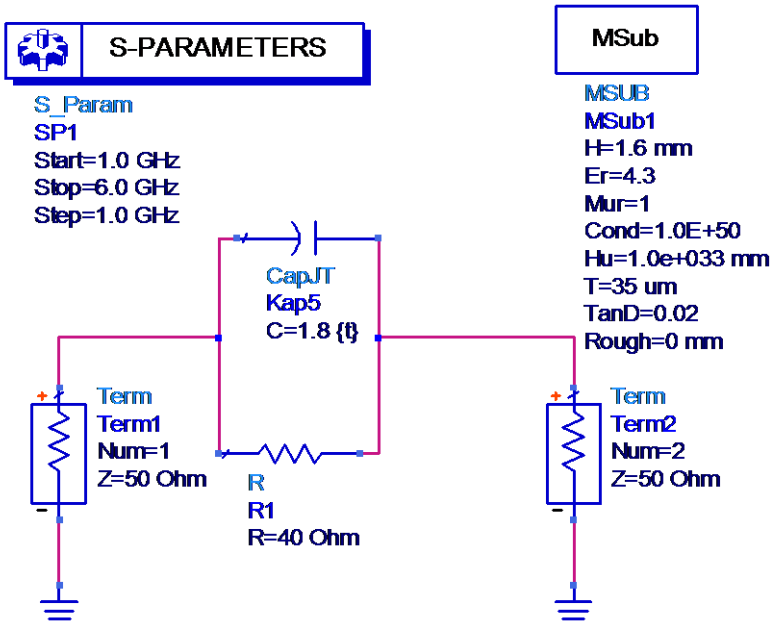

Figure 2.17: Parallel RC circuit design in order to maintain stability within band

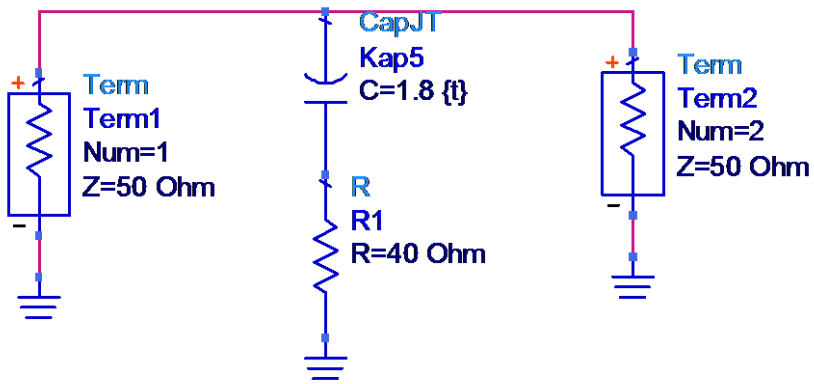

Figure 2.18: Series RC circuit design in order to maintain stability within band

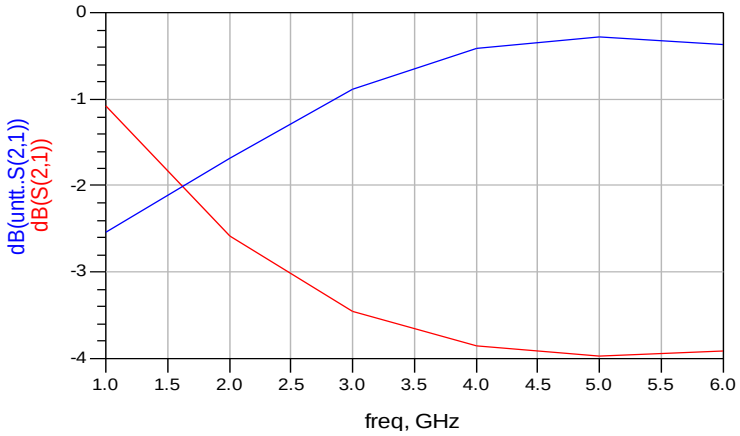

Figure 2.19: Simulation results of stability networks in figure 2.17 and figure 2.18

2.4.3 Matching

Gain Match

Maximum transfer of power from the source to the transistor and from transistor to the load takes place when there is conjugate matching at both the input and the output. At this case, source delivers all its available power to the output [20].

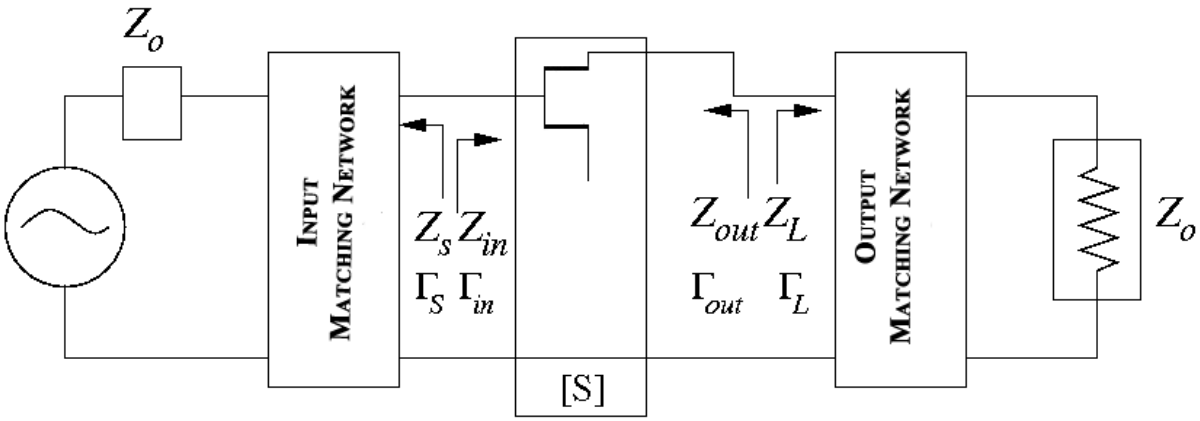

Figure 2.20: Block diagram of amplifier with matching networks

Two conditions of conjugate matching are defined as:

$$\Gamma_{in} = \Gamma_S^*$$

$$\Gamma_{out} = \Gamma_L^*$$

The first definition of reflection coefficients affiliation provides maximum power transfer from the input matching network to the transistor. Similarly, the second definition provides this transfer from the transistor to the output matching network.

Gain match versus power match

In figure 2.21, the comparison of two matching condition applied to a power amplifier is given. The solid line represents the response of a conjugate match at the output, while the dashed line indicates an amplifier matched for maximum output power. A and B represents maximum linear power and 1 dB compression points respectively for an amplifier with conjugate matched output network. For power matched amplifier these points are referred by A' and B' points. This figure shows that maximum power delivered and 1 dBc is 2 dB higher in the power match case compared to the amplifier designed for S_{22} match. For power amplifiers, power match is favored as it yields higher output power and 1 dBc point and it typically gives 0.5-4 dB better results eliminating the extra cost [5].

In most power amplifier applications, input matching networks are designed and fixed at a good gain match at the frequency range and power match is achieved using load-pull measurements at the output side.

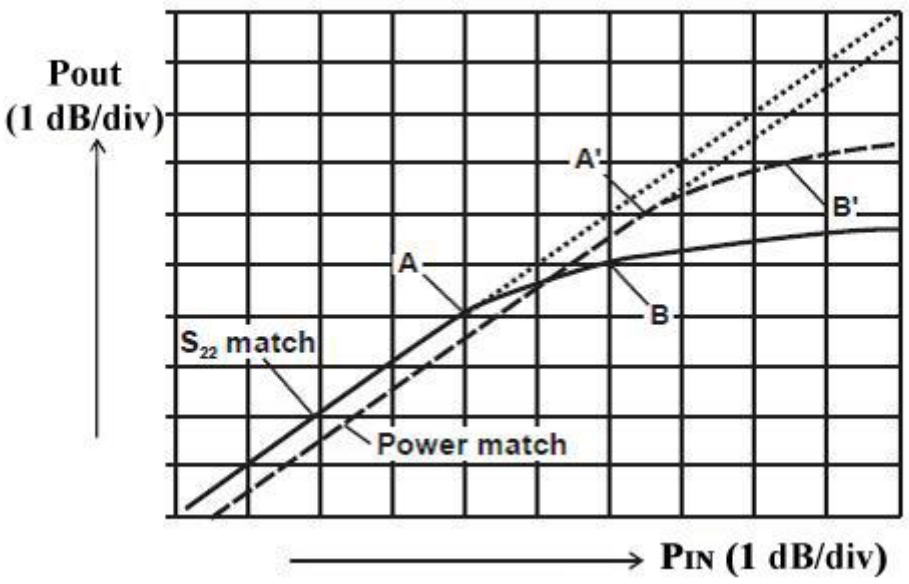

Figure 2.21: Gain matching versus power match at 1 dB compression point

Load Pull

Load pull simulations can be done in ADS using HB1Tone_LoadPull design guide with a large-signal / non-linear model of transistor. For this thesis, a large signal model CGH40010F from Cree is used. Figure 2.22 and 2.23 shows the simulation setup from this design guide and resulting load-pull contours for output power and PAE as a function of load impedance. In figure 2.23, each contours indicates the set of impedances corresponding to a constant output power or PAE.

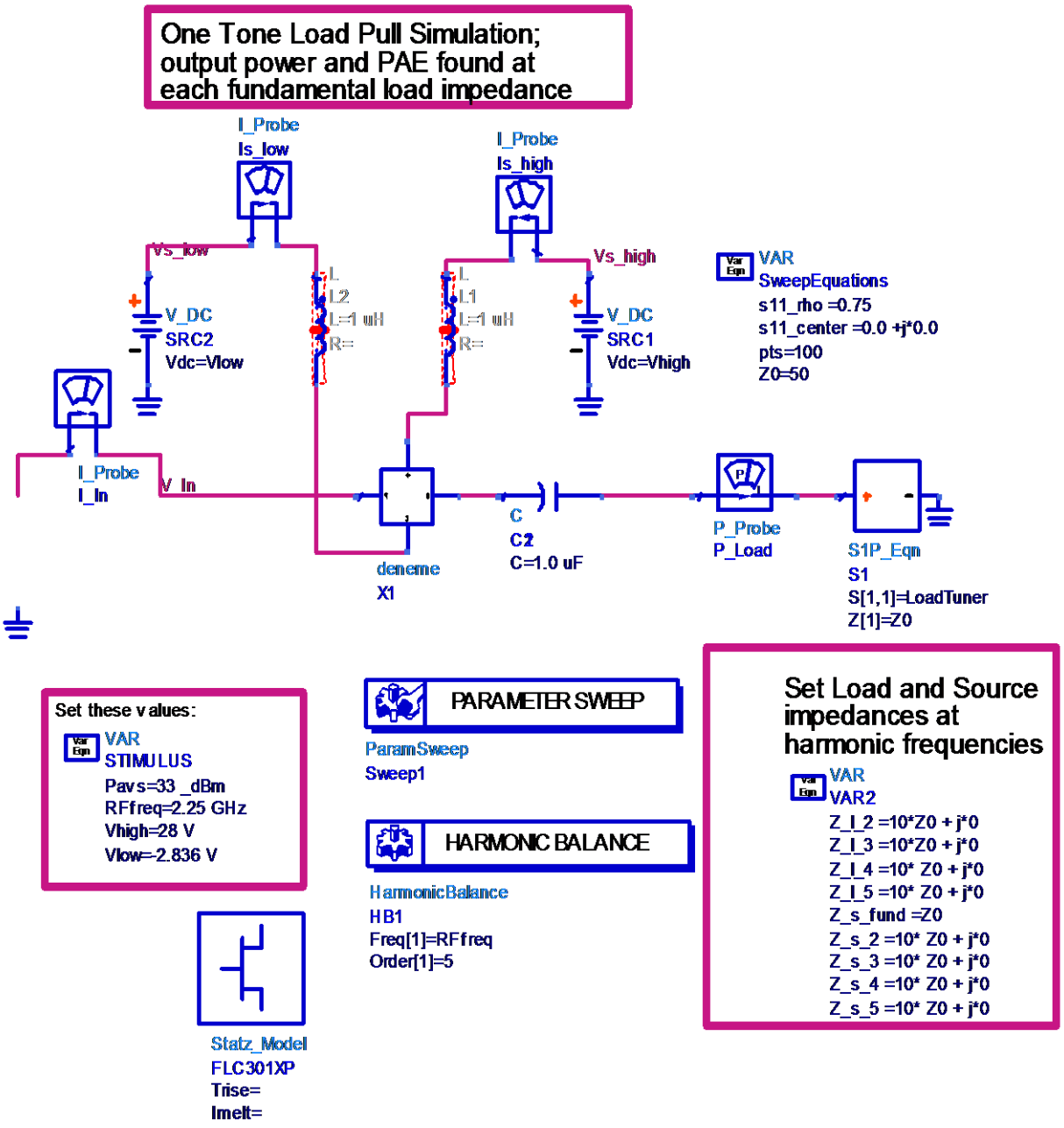

Figure 2.22: Circuit of design guide HB1Tone_LoadPull for 1-tone analysis

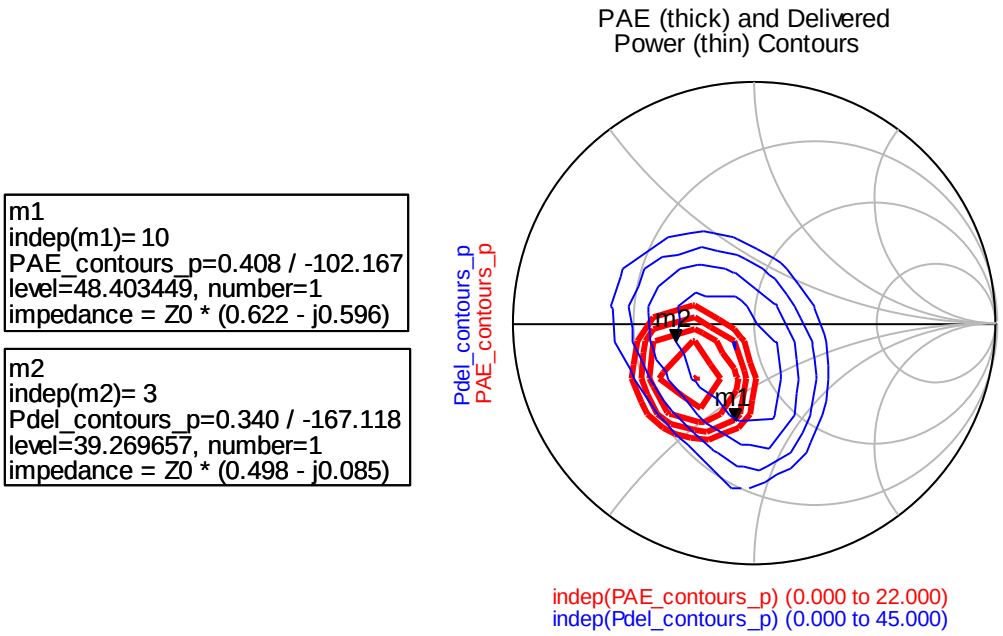

Figure 2.23: Resulting PAE and delivered power contours drawn in Smith Chart

The above load-pull circuit uses harmonic balance simulation in ADS. This iterative simulation calculates the response of large signal circuits driven by either single or multiple sources and tries to find a stationary solution for the non-linear system in the frequency domain [21]. Following flow chart shows the process of this harmonic balance simulation.

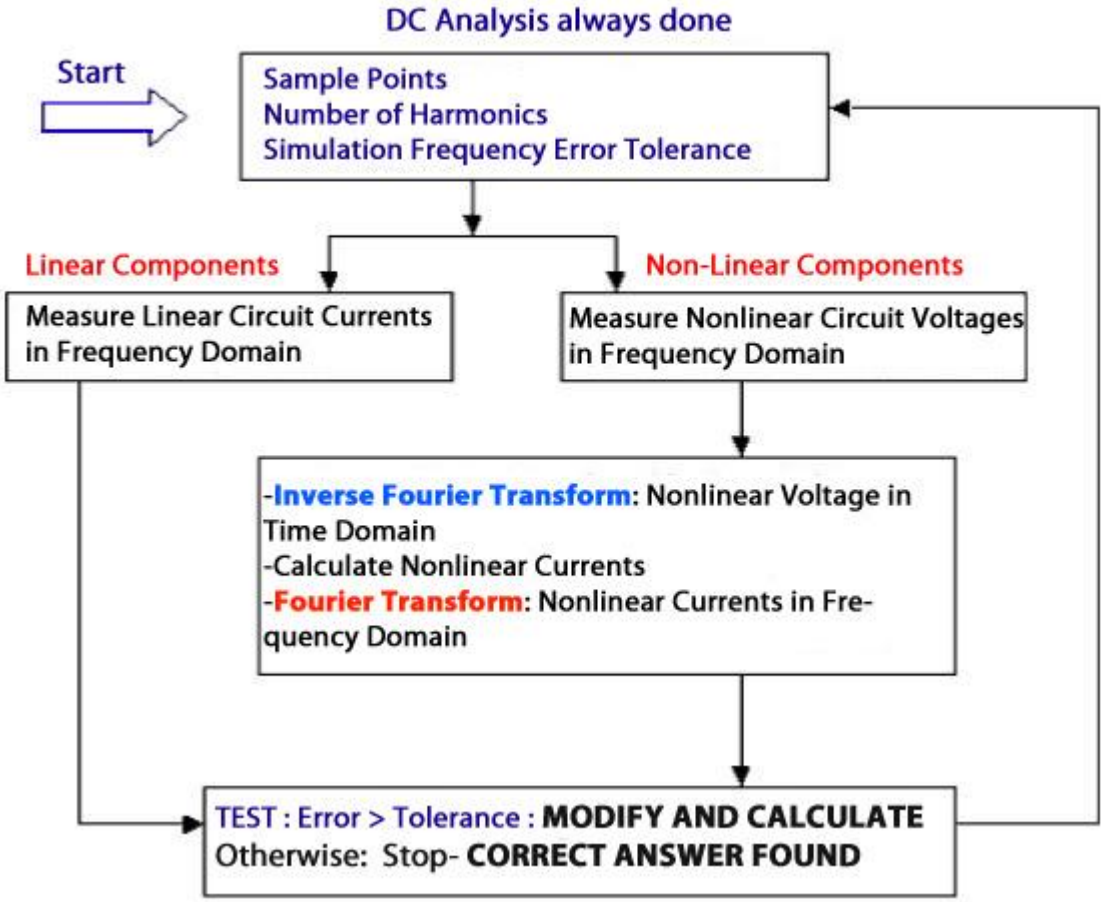

Figure 2.24: Flow diagram of Harmonic Balance simulation in ADS [21]

2.5 Calibration

Measurement with network analyzer

To ensure that the measurement results made in the laboratory are as accurate as possible, there is a need for test equipment correction. For a network analyzer measurable errors are divided into three different categories [22]:

• Systematic errors
• Random errors
• Drift errors

Systematic errors that occur on imperfect test equipment or setup can be described with calibration and discarded mathematically while taking measurements if they are stable in time.

These systematic errors can be modeled as it is shown in Figure 2.24 and consist of six different types of systematic error. In total, this model characterize errors for both forward and reverse direction, it is subject to twelve errors.

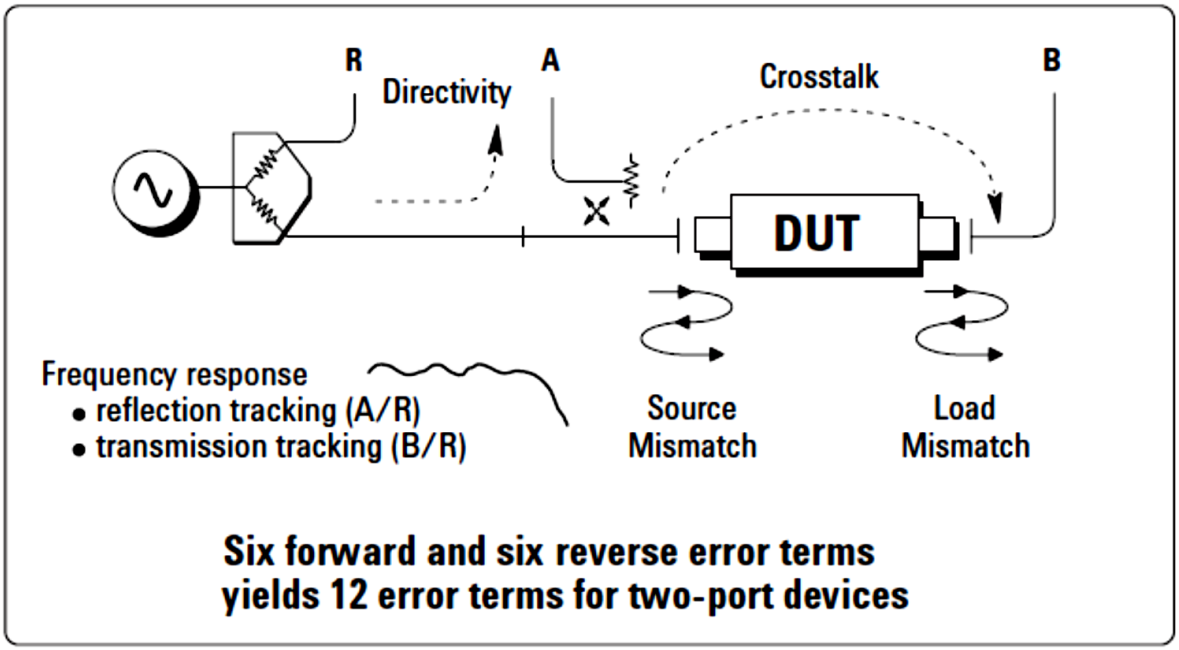

Figure 2.25: Systematic errors

Random errors are not stable in time; hence they cannot be discarded through calibration. Some random error sources such as noise generated within the equipment can be minimized by taking several measurements and increasing power level.

Drift errors are mainly caused by change in temperature and can be eliminated by calibrating the equipment iteratively. Placing the test equipment in a stable temperature like $+25^{\circ}C \pm 5^{\circ}C$ yields better accuracy in measurements [22].

2.5.1 One port calibration

This calibration includes measuring the three known calibration standards knowns as short, open and load. The data taken from these measurements are used for solving number of equations which can deduce the systematic errors on equipment and discard them while measuring for reflection. Systematic errors which can be removed with one-port calibration are shown in Figure 2.25.

2.5.2 Two port calibration

A two-port calibration (Short-Open-Load-Through) includes measurement with and additional “through” component. In short, when 7 measurements are done, three (Short-Open- Load) for each port and an additional through calibration, a two port calibration is done. Data obtained from these measurements are then used to solve the equations for

relevant S-parameters, thus systematic errors can be discarded. Figure 2.25 gives an overview of the errors removed through different calibration methods and general properties of these methods. Measurements in laboratory for the power amplifier designed for this thesis, full two-port calibrated test equipment were used. Properties of this calibration such as highest accuracy, etc. are illustrated in figure 2.26.

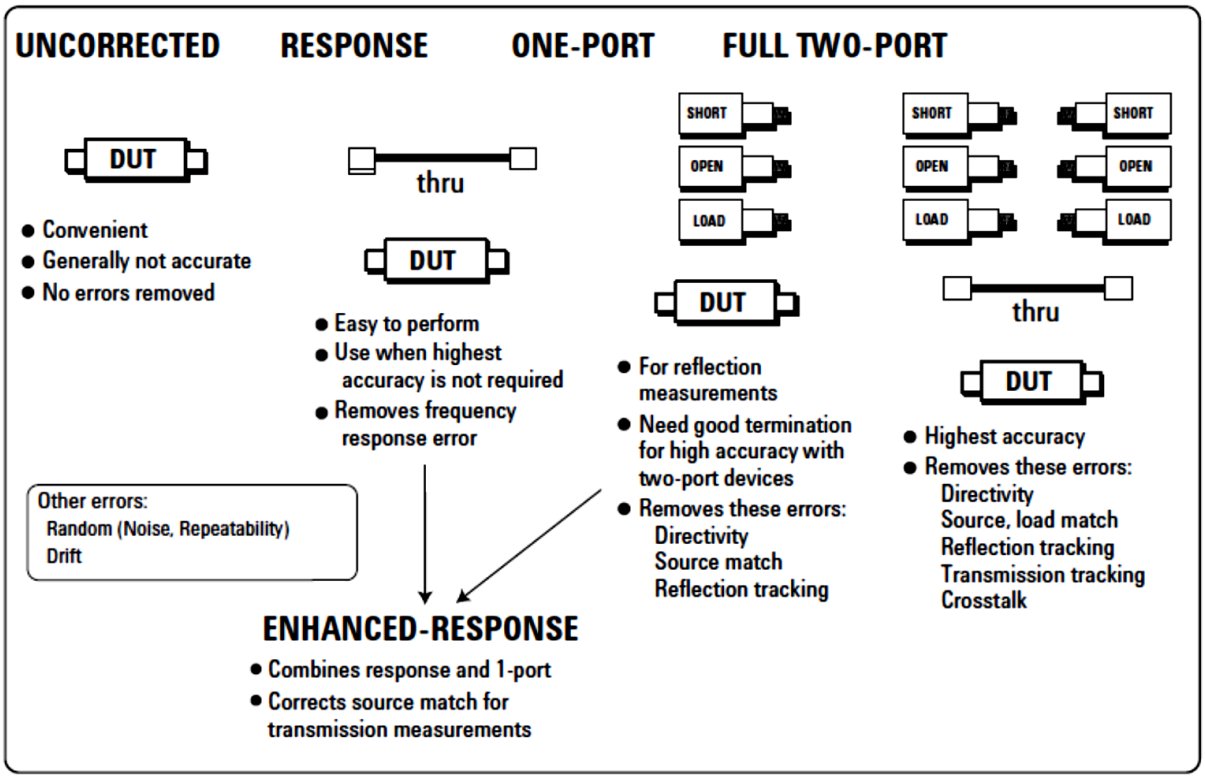

Figure 2.26: Different type of errors and calibration standards in order to remove them [22]

3. DESIGN IN ADS

3.1 Bias point selection

The amplifier designed in this thesis work is biased on just above of no-load threshold current. The corresponding bias point is set on design guide FET IV Gm PowerCalcs as -2.96V which gave a quiescent current of 84.3 mA and finally IV curves are derived. Drain is set to the normal operating voltage of 28V for the transistor [11]. Circuit used in this design guide and simulation results of IV curves are shown in figure 3.1

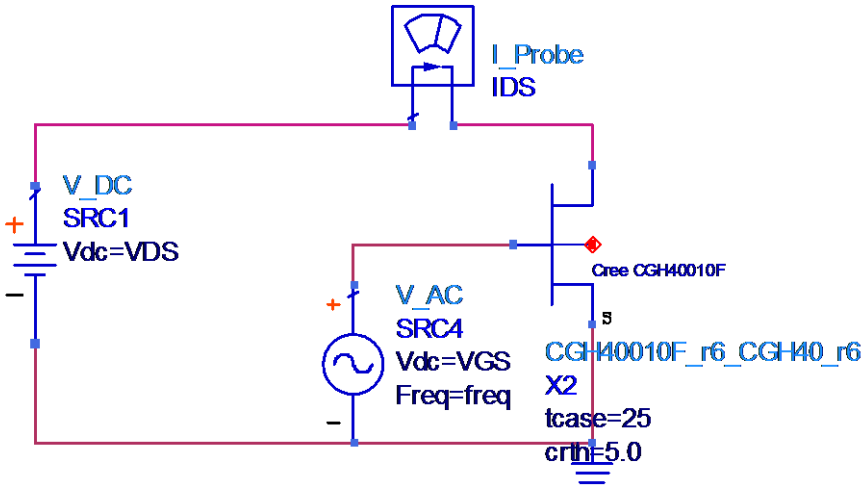

Figure 3.1: Circuit for IV curve generation in FET_IV_Gm_PowerCalcs design guide

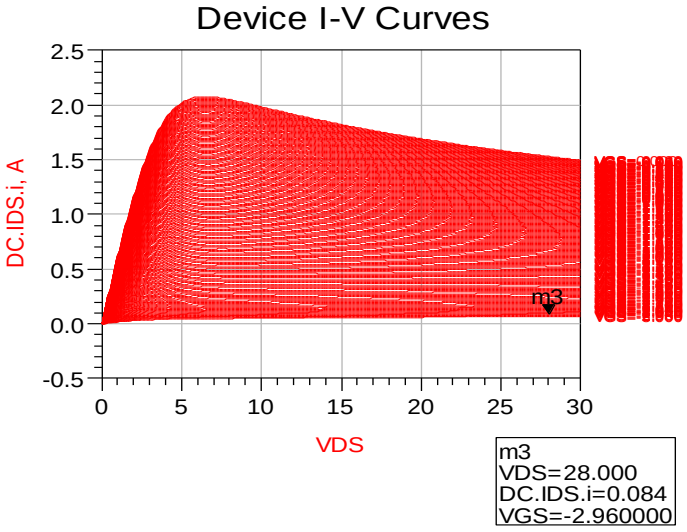

Figure 3.2: IV curves simulation results for given circuit in Figure 3.1

3.2 Bias circuit

Bias circuit discussed earlier in the previous chapter is realized on microstrip substrate. The circuit in figure 3.4 is simulated in ADS from 1 to 6 GHz and simulation results obtained in a Smith chart as it is illustrated before in this thesis in Figure 2.14. In the bias circuit design, physical parameters are calculated in Linecalc tool for frequency of f_0 and in microstrip components of MLIN and MBSTUB these results are defined. In the circuit, initial values of quarter-wave line and radius of stub are calculated as 18.5 mm. Results from a full-wave calculation is shown in figure 3.3.

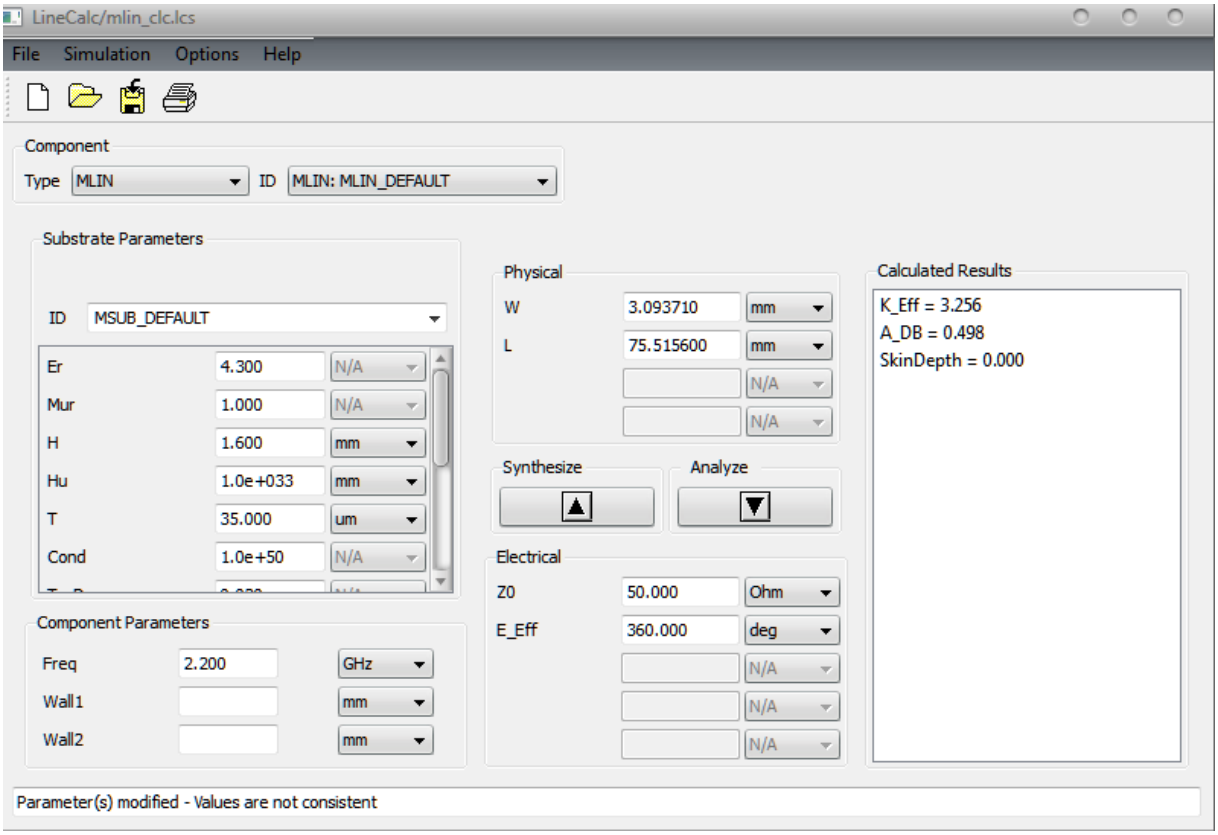

Figure 3.3: Calculation of physical parameters for the substrate using Linecalc tool in ADS

For f_0, MBSTUB will transform RF open circuit to the RF short circuit in its left node. Similarly, MLIN will transform this RF short circuit in its right node to the RF open circuit in its left node. This gives a total of a full rotation in the Smith chart (360) and open circuit for f_0 in the left node of quarter-wave line MLIN which is illustrated in figure 2.14 in this thesis previously. Impedance found in f_0 is equal to 3355 kΩ and shown in figure 3.5.

For $2f_0$, MBSTUB will transform RF open to RF open since at this frequency, lambda is double and transformation of the stub is now equal to a full rotation Smith chart. This RF open will be transformed to RF short with the quarter-wave line.

Similarly, for $3f_0$ MBSTUB will transform RF open circuit to the RF short in its left node. This transform equals to 540 degree rotation in Smith chart. MLIN then will rotate this RF short quarter wave in Smith chart resulting RF open in its left node.

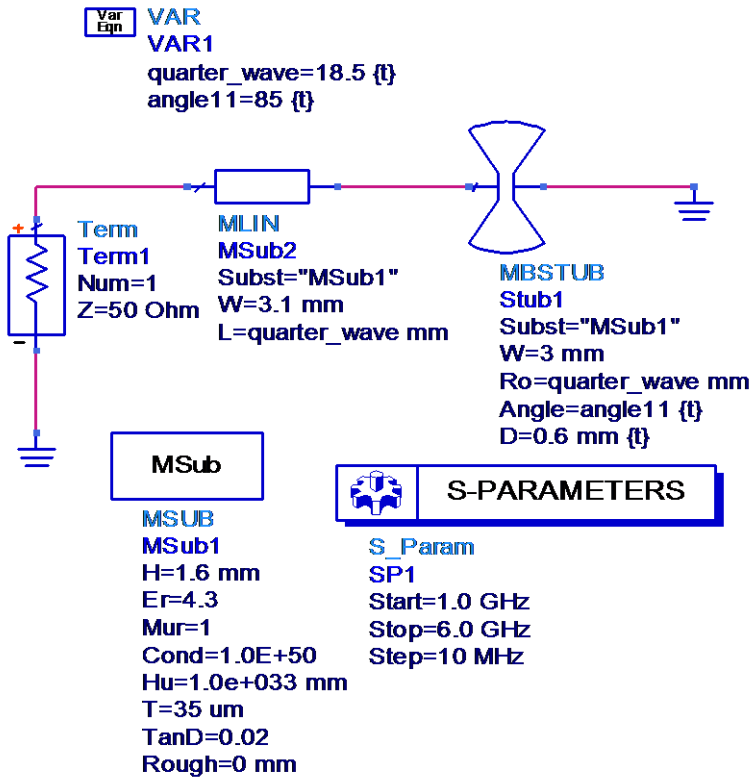

Figure 3.4: Design of bias network with a quarter wave and stub

Table 3.1: Some substrate parameters and physical diameters calculated in Linecalc for Zo = 50, electrical efficiency of 360 degree

Substrate Parameters					**Physical parameters**	
Er	Mur	H	T	Cond	Width	Length
4.3	1	1.6 mm	35	1.0e + 50	3.1 mm	75.5 mm

Furthermore, for $2f_0$ and $3f_0$ the left node of quarter-wave line indicates short circuit and open circuit respectively. As a result of the simulation, impedance in $2f_0$ is achieved as zero impedance known as short circuit and is given in figure 3.5. As it is indicates, open circuit at $3f_0$ will result in an impedance at this frequency, however this value is equal to 577Ω which is much lower than the high impedance seen in f_0 and discarded in this simulation as it is defined from 1 to 6 GHz. $3f_0$ which is 6.75 GHz does not fall into design bandwidth of the amplifier.

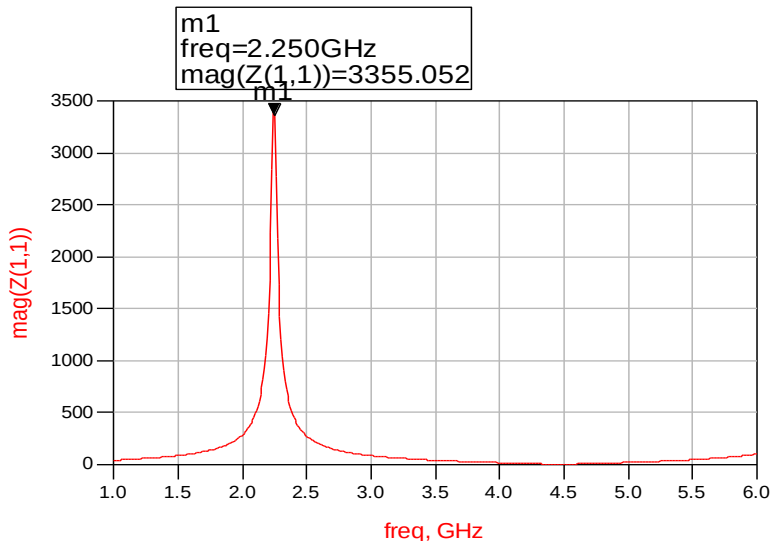

Figure 3.5: Resulting high impedance value for center frequency from simulation of design in Figure 3.4

3.3 Stabilization of the device

Result from simulations for stability was presented in figure 2.16 in previous chapter. This figure indicates that at low frequencies, gain tends to be higher thus leading to stability problems within this frequency range. In order to overcome this stability issue, a parallel connected RC circuit is attached to the gate side of the transistor. As a starting point, ideal components were used and capacitor value is set to a relatively small value. Resistance is tuned to a value so that the device is stable in the frequency range of 0-6 GHz.

As next step of the design, real components are replaced with ideal components. A capacitor model derived from CapJT library designed by Morten Olavsbråten is used which is shown in Design Components section in this thesis before. Capacitance was tuned to any value within the range of available Johanson capacitors in the laboratory and resistance value was set to nearest E-12 value. Several combinations of available capacitor and resistor values were tried to achieve unconditional stability within the defined frequency range.

In the design, a 39Ω resistor in parallel with a 1.8 pF are used in order to get stability over the whole band, thus mu factor is found to be 2.45 around the center frequency of 2.25 GHz and slightly above one within low frequency side of the band, which corresponds to a relatively large margin needed for unconditionally stable case. Following figures shows gain within the band without matching included in the design and stability factor as a function of frequency respectively.

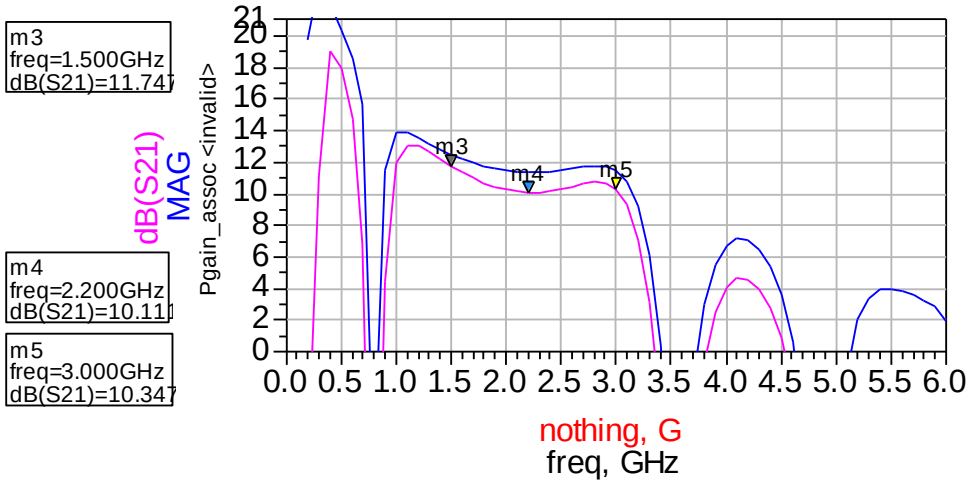

Figure 3.6: Gain characteristics within band

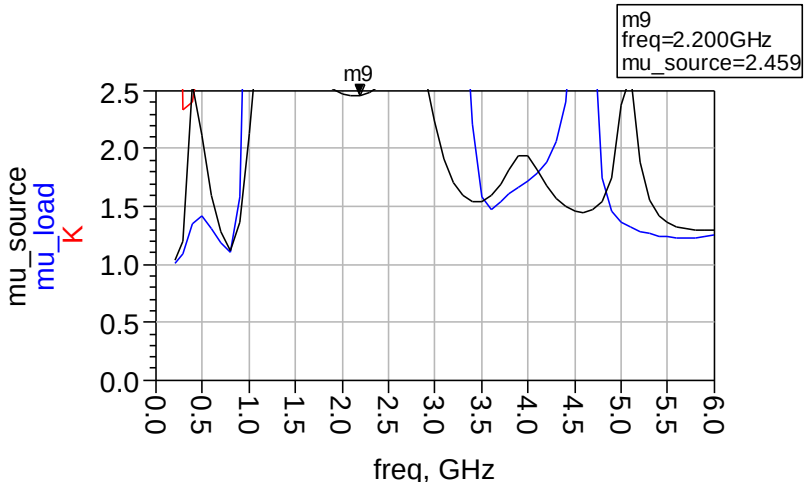

Figure 3.7: Stability factors as a function of frequency

3.4 Matching networks

In ideal case, the concept that is being followed while designing the input and output matching network is that, small-signal simulations in ADS implemented to optimize for gain and return loss for input and output sides, on the other hand large-signal simulations in ADS is used for output power and efficiency optimization.

As a starting point, SP_NF_GainMatchK design guide were used to see the stability factors and the small-signal gain performance of the device within the whole band. In order to design both input and output matching networks, Smith Chart utility in ADS were used with load and source reflection coefficient values for simultaneous conjugate matching which were achieved from the design guide simulation results as it is shown in figure 3.8 below.

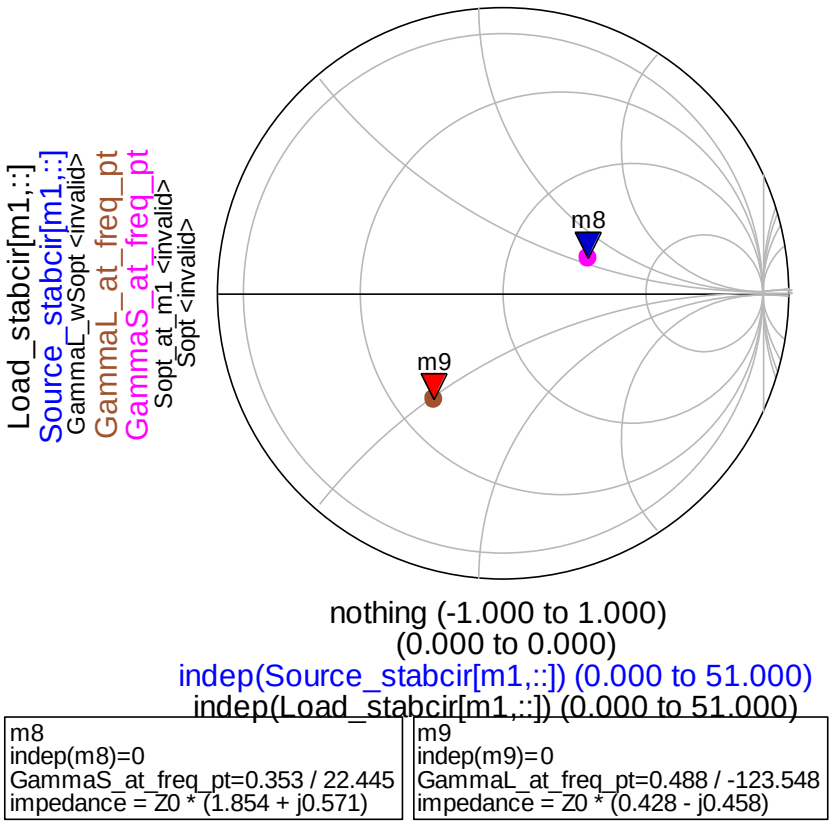

Figure 3.8: Source and Load reflection coefficients without matching

In fact, input side of the network does not exhibit perfect match by looking at Smith Chart above. Furthermore, matching for the impedance value which is shown as GammaS in figure 3.8 was implemented with an open stub and a transmission line. As a result of this implementation a better performance was achieved. In order to reduce the component losses within the whole network, line in the input matching network was deducted in this step, since the length of this line was around 1 mm and this value could be discarded.

For output matching network, similar topology has been followed. At first, the design was made with an open stub and a line. Lengths of these two components were obtained in Smith Chart tool in ADS and optimized for the specifications of gain, return loss while maintaining the unconditional stability within the band. Results of this single stub matching for output side did not exhibit optimal performance, hence using an extra stub and line which is known as double stub matching yielded much better performance as this topology is preferred in broadband designs [8]. For optimization, three goals were defined in design which is shown in Figure 3.9 according to given specifications. However, in this step, instead of conventional open stub, open-end effect stub defined as MLEF in ADS was used. The reason behind this is that this component has a superior bandwidth capability and is preferred in broadband

amplifier designs. Full circuit design for this simulation is shown in 3.10. However, microstrip width tapers of 0.5 mm and 0.7 mm length were placed in both sides of the transistor in order to get better (S1,1) in the final design of this thesis which is shown in part A in this thesis.

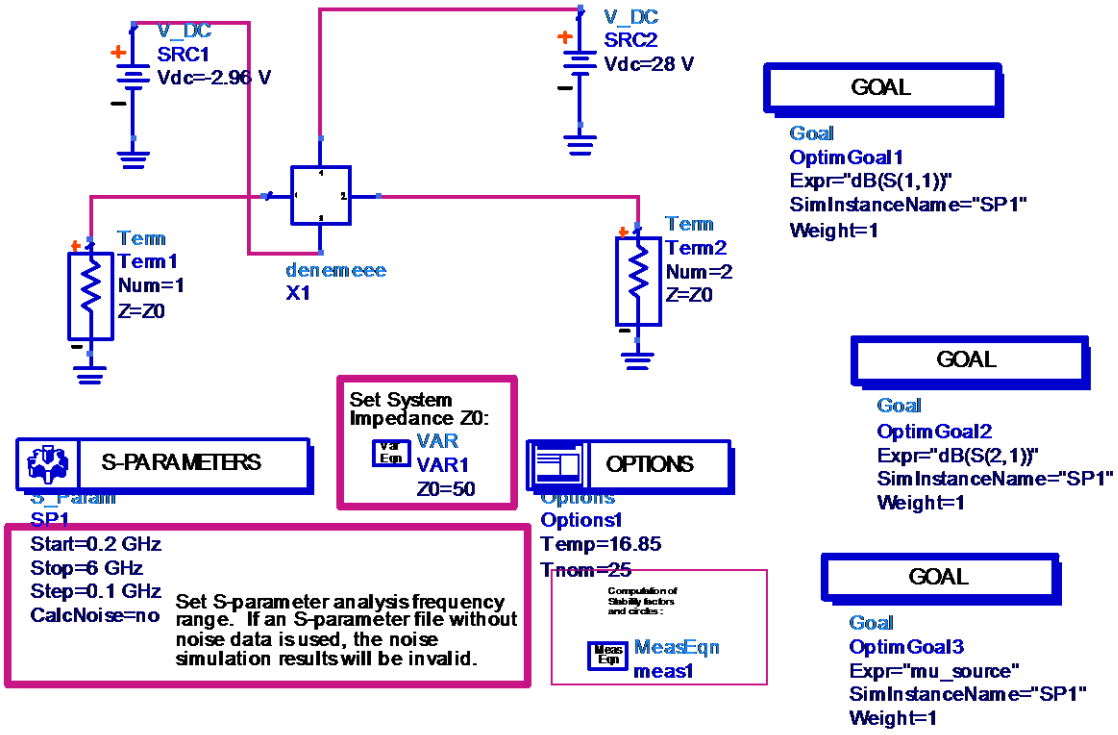

Figure 3.9: Design guide used for small-signal simulations with defined goals

Requirements that were set in the frequency band 1.5-3 GHz for the optimization objectives defined as goals in the design is given in Table 3.2 below.

Table 3.2: Definitions for optimization goals in small-signal simulation

Parameter	Goal
S11	<-10 dB
S21	>13 dB
mu_source	>1

Having established the small-signal parameters required, the next stage is to simulate the amplifier under design guide HB1TonePAE_Pswp. It is a one tone harmonic balance simulation and takes one input frequency which in this thesis work is 2.25 GHz. Similarly, in this stage, optimization goals such as Power Added Efficiency which is as high as possible according to specifications and Fundamental Output Power are defined in the design. Requirements for these goals are given in Table 3.3. Design guide used in this simulation is shown in Figure 3.11.

Table 3.3: Definitions for optimization goals in large-signal simulation

Parameter	Goal
PAE1	>60
Pfc1	>10

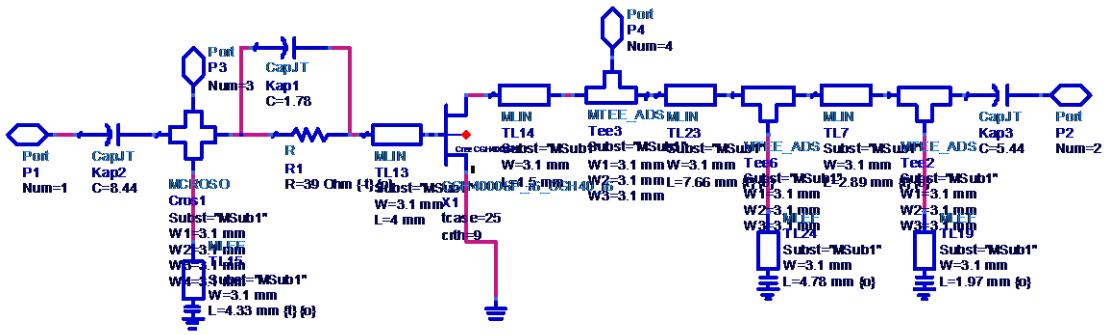

Figure 3.10 Amplifier design with matching networks

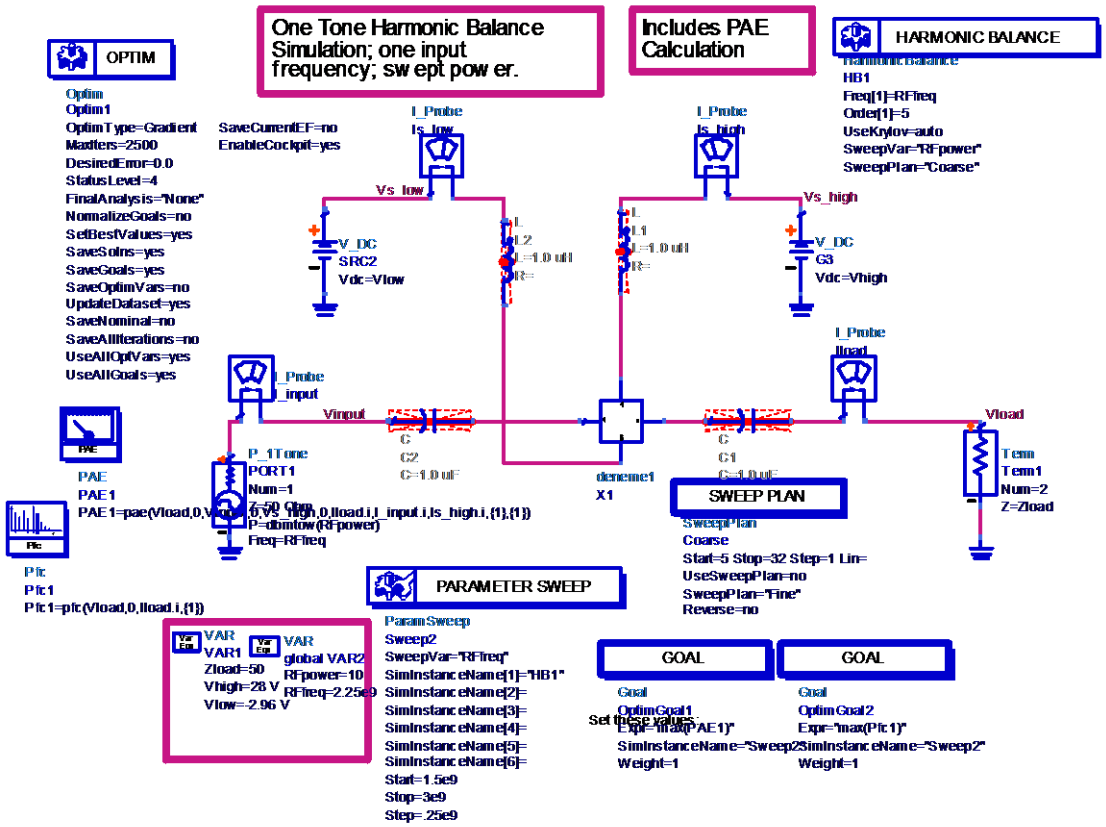

Figure 3.11: Design guide used for large-signal simulation

After simulating the amplifier with the design guide shown above, Power added efficiency of 57.3% and 24.31 dBm fundamental output power at 1dB compression point are achieved for the fundamental frequency of 2.25 GHz. However, this result is not for an ideal case amplifier design and there are some complications while manufacturing that need to be considered. First of all, after generating the layout of final design, it was clear that between the butterfly stubs of bias network and stubs of matching networks there is possibility of coupling since the angle of the butterfly stubs were set to 84 and the distance between these components was relatively short. This distance should be two times of stub line, which is an accepted reference conventionally, to get rid of coupling effect. In order to overcome this problem, angles were reduced to 55. However this reduction led to the distortion of gain ripple within the band and input return loss. For compensation of this loss, lines (TL23, TL7) and stubs (TL24, TL19) that can be seen as components of output matching network in Figure 3.10 were adjusted using optimization tool again until the specifications for small-signal are obtained. In this figure, input matching network consists of a stub, while two microstrip lines such as TL13 and TL14 were attached at both gain and drain side of the transistor for a good soldering space.

3.5 Fabrication

The layout was exported as Gerber files from ADS and it was milled on a printed circuit board known as PCB. Further, the amplifier has been subjected to following mechanical engineering:

• The length of the cooling ribs were cut to fit the card

• Holes for the transistor was milled out

• A total number of 14 screw holes were threaded into board

  • 2 for the transistor

  • 4 for the other sides of the board

  • 4 for each SMA connectors

The screws were tried to be positioned so that they would have minimal impact on scattering field from the lines. At the same time, it was necessary to place multiple screws (2 pieces) relatively close to the transistor in order to provide good signal ground at this point. The same procedure was done with two screws at each SMA connector. The components in Table 3.4 were then fitted on the finished circuit board. In this table, components which were drawn in blue color indicate the difference from their value of design in ADS.

Table 3.4: Components used in the fabrication

Place in Design	Size	Value	Tolerance	Voltage	Type
Stability network	0603	1.8pF	±0.1pF	250V	Johanson 251R14S1R8BV4S
	0603	39Ω	±1%	50V	KOA RK73H1JTTD68R0F
DC-block	0603	8.2pF	±0.25pF	250V	Johanson 251R14S8R2BV4S
	0603	3.9pF	±0.1pF	250V	Johanson 251R14S3R9BV4S

Johanson capacitors in the lab can withstand 250V, allowing them to have a good margin considering the drain voltage of 28V.

Other components that were used while taking the measurements in addition to the ones discussed in Table 3.4 are given in Table 3.5 below.

Table 3.5: Remaining parts used in fabrication in addition to Table 3.4

Description	Manufacturer	Model
Transistor	Cree	CGH40010F
SMA connector	Huber+Suhner	23 SMA-50-02/111NE
Power cable	Huber+Suhner	RADOX 125, 0.25mm^2
Heat sink	Misc	63mm(length), 65mm(width), 25mm (height)
Metal screws	Misc	M2, 5mm

The completed circuit board with components, the transistor and the SMA connectors were then screwed to the heat sink, and eventually the transistor, SMA connectors and power cables are soldered. Hence the final design is fabricated and shown in Figure 3.11 below.

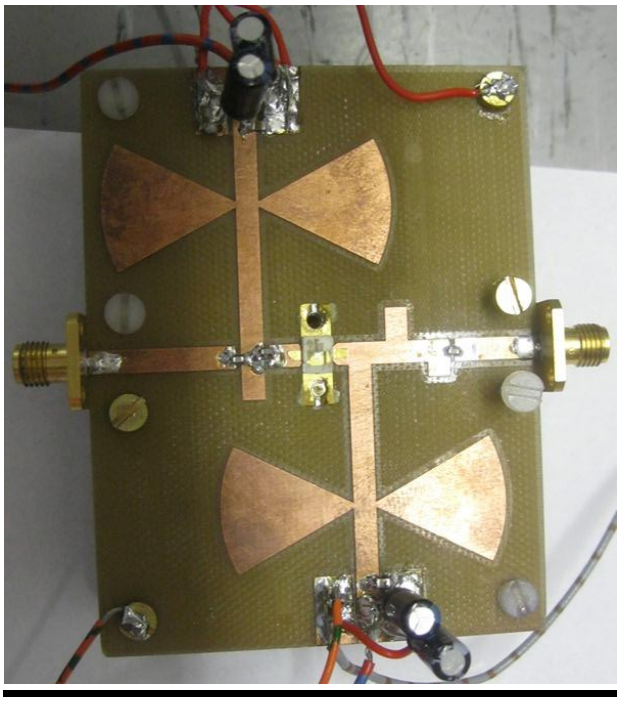

Figure 3.12: Fabricated amplifier

4. Measurements Results

In this section, results of the measurements made with the fabricated amplifier in Figure 3.11 are presented. Two PAs used in the test up as drivers are shown which resulted in decreasing gain for high-end of frequency band, hence the last amplifier designed by Einar Berge Mogstad in his thesis work was included in setup and experimented. Hence the following results are obtained. In the laboratory, a coupler and attenuator were used in the output side in order to restrain the power from exceeding too high levels which could result in destroying the signal analyzer. Results from small and large signal measurement are plotted in Matlab and shown below.

4.1 Small signal gain and bandwidth

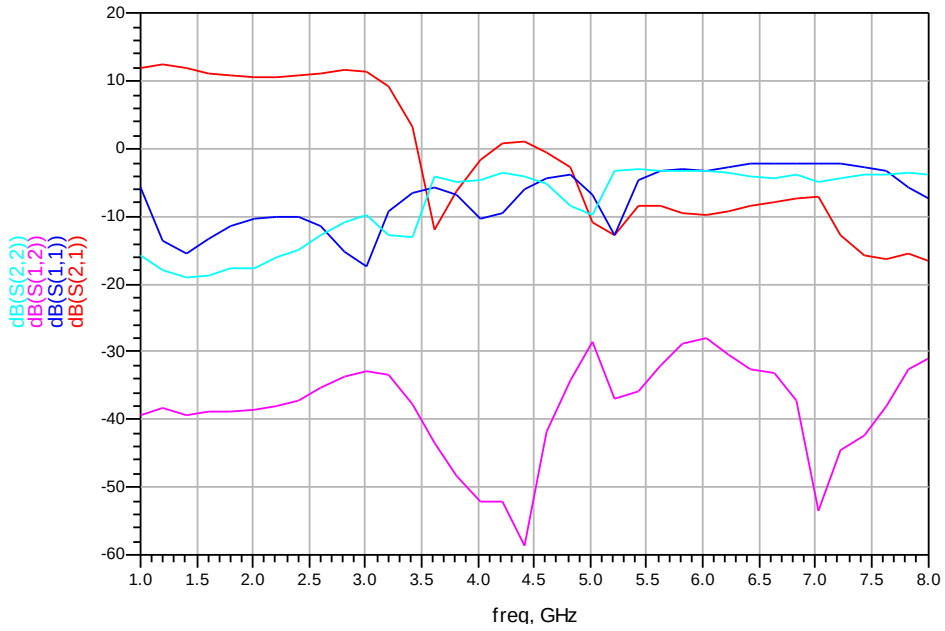

Figure 4.1: Small signal measurement results

Small signal measurement result was obtained by the aid of Matlab in laboratory and corresponding s2p file generated. The s2p file was then simulated and plotted in ADS. Looking at this figure, desired gain of 10 dB is achieved within a bandwidth of 2.2 GHz, extending the limits of the specified bandwidth in the lower end of it. In this figure, S(1,1) and S(2,2) are also plotted which indicates good matching for both input and output sides of the device.

4.2 Large signal measurement

4.2.1 Power at the output

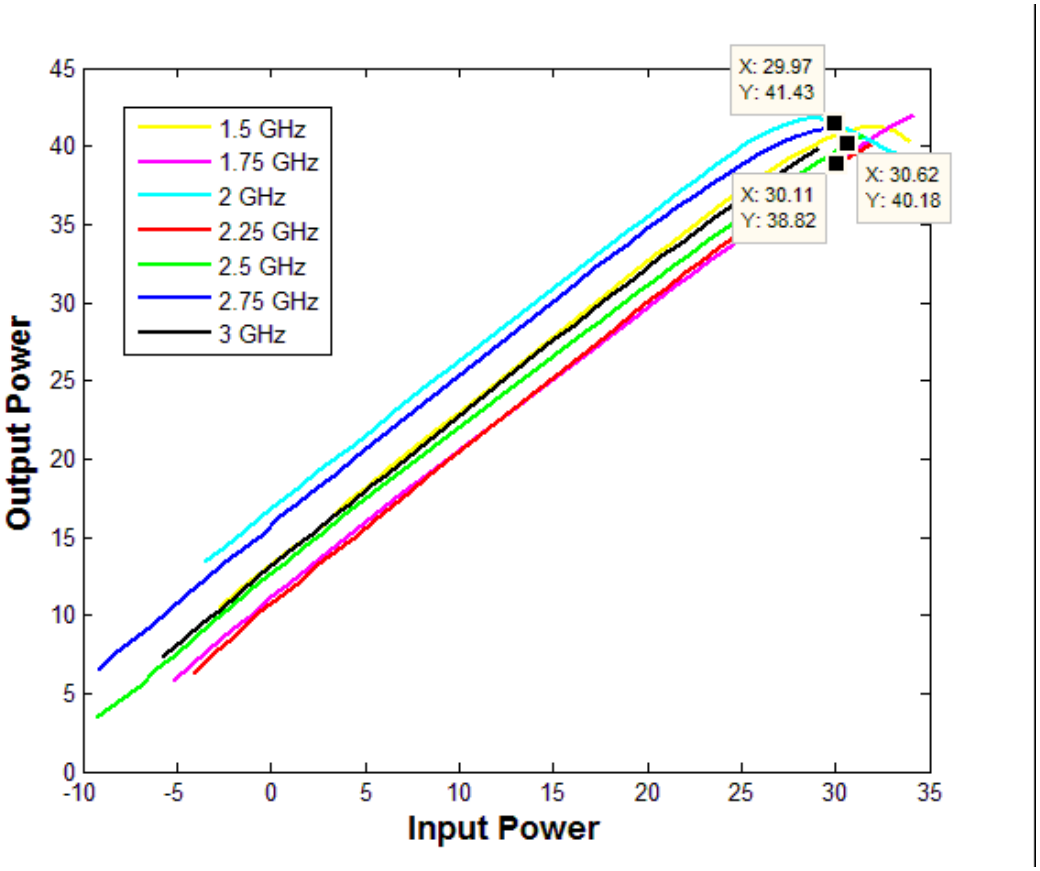

Figure 4.2: Input power versus output power in frequency band

In figure above, input power with corresponding output power as a function of some frequencies within the band is shown. At 2 GHz, an output power of 41.43 dB is achieved for 30 dB input power. For different frequency components, starting input power value is different. The reason behind this is that the driver used in setup does not provide same power level for all frequencies in the operating bandwidth.

4.2.2 Gain

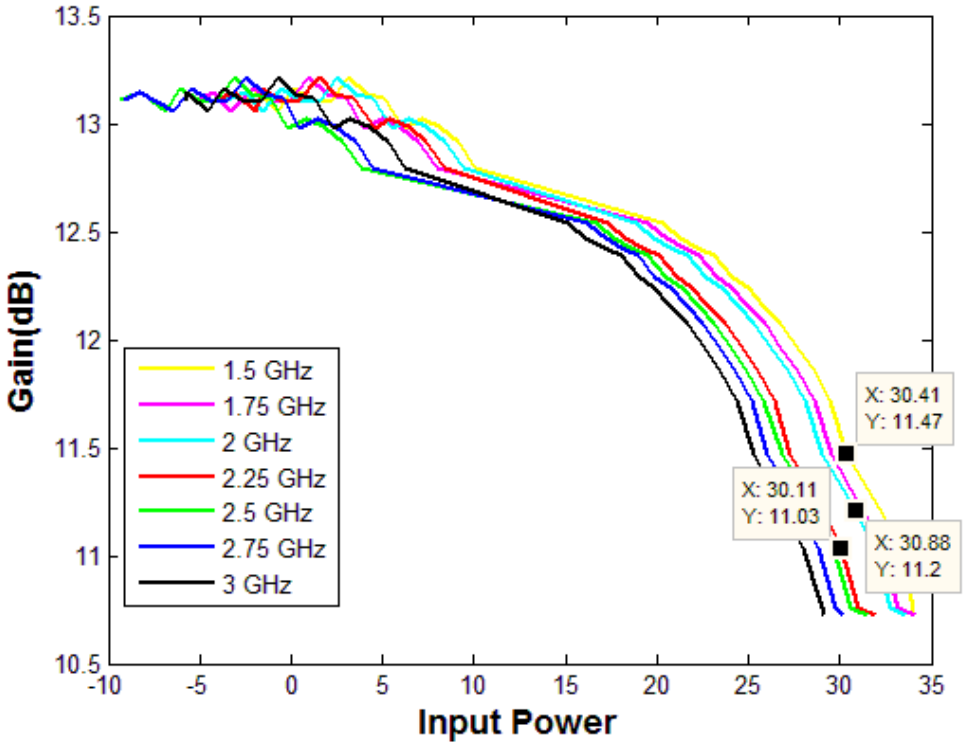

Figure 4.3: Large signal gain of the amplifier for different frequencies within band

Gain of the device is plotted in Figure 4.3 for input power levels. Plot for 2.25 GHz which is the center frequency of the band exhibits 11.03 dB gain that is equivalent of an output power above 10W. Gain ripple within band can also be calculated since all frequency components of the bandwidth are present in the figure and the ripple is around 0.5 dB.

4.2.3 Drain efficiency and PAE

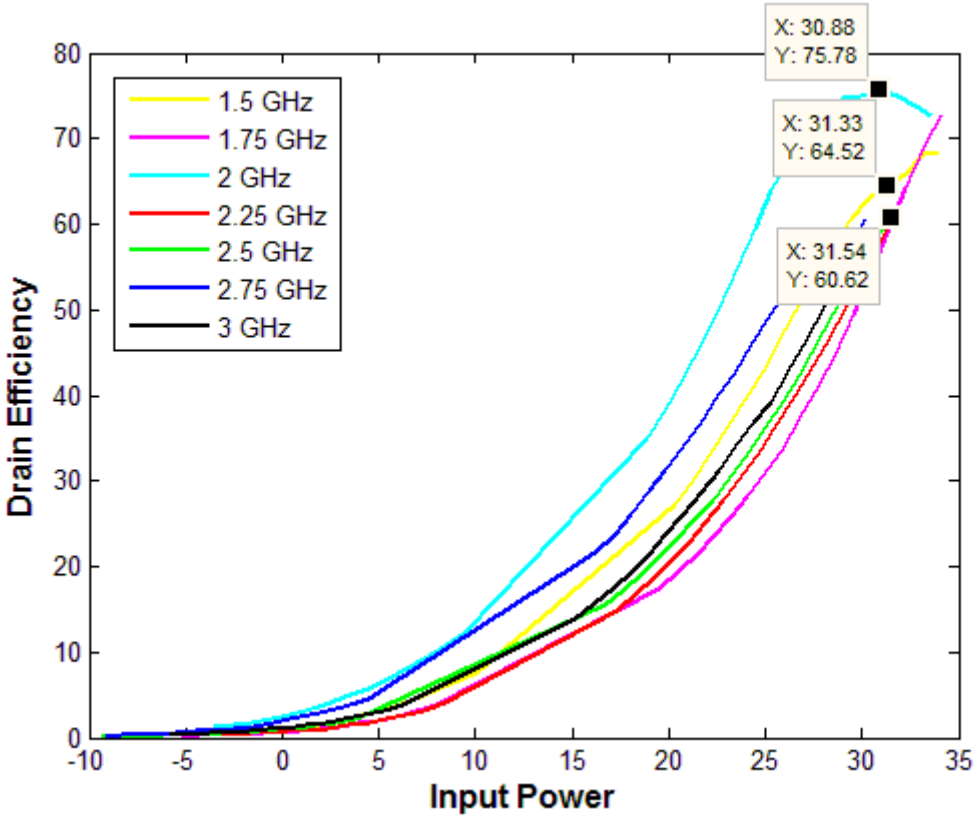

Figure 4.4: Drain efficiency versus input power

Drain efficiency, as discussed before in this thesis, does not take RF input power into account. At 2 GHz, the efficiency is 75.78% for 10W input power which is quite similar to the results of ADS simulation. Remaining two markers in the figure reveals efficiency of 64.52% and 60.62% for 1.5 GHz and 2.5 GHz respectively. For input power levels above 30 dBm, the device goes into compression, hence the output power which is function of drain efficiency, starts to drop as it was shown in Figure 4.2. This drop corresponds to the downward curve of efficiency in Figure 4.4.

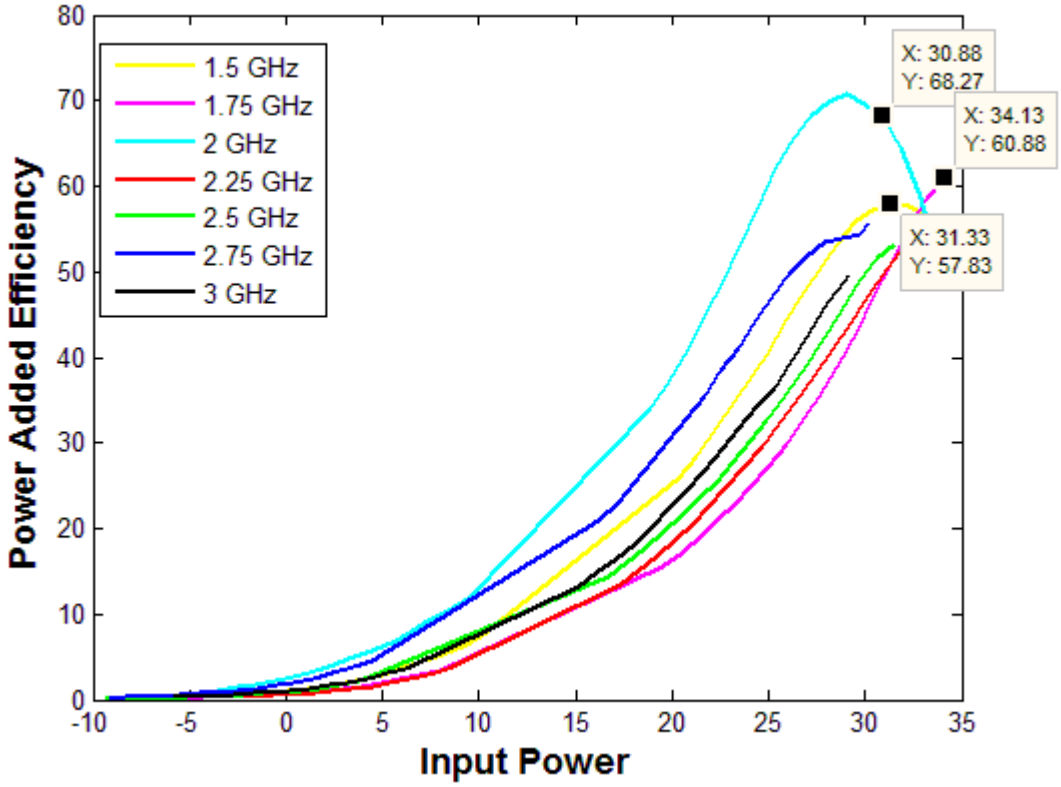

Figure 4.5: Power added efficiency versus input power

Further analysis is made on efficiency and input power is also considered in this figure. Power added efficiency is calculated as 68.27% at 2 GHz. For the same frequency, drain efficiency was at 75.78%. For frequencies above 2.75 GHz, the device does not go into compression and it is clear in the figure plotted with the black line. The driver used in the test setup hence does not provide enough power level at 3 GHz and the reason for this is discussed further down in last chapter.

5. Discussion and Conclusions

In order to drive the amplifier into compression point, 30 dBm input power is required to be fed. The available signal generator SMU 200A in laboratory provides around 25 dBm power levels, hence a driver is needed in test setup in order to achieve the wanted gain within band. First tryout has been made with first two power amplifiers designed by Einar Berge Mogstad as driver in setup, however in the generated Matlab figure of output power versus input power in the laboratory showed that above 2.5 GHz power supply do not exhibit current change, hence for high frequencies this amplifiers were not applicable.

Hence, the main problem in the setup was the measurement for the high end of the frequency band mainly above 2.5 GHz. The reason is that the amplifiers, which were utilized as driver, are designed and matched for a single frequency and cannot cope with high power levels in high frequencies. In order to overcome this problem, a number of available PAs were used until the desired gain is achieved. Finally, the use of last PA as driver that Einar Berge Mogstad designed in his thesis work made it possible to drive the amplifier into compression, thus measurements were made. Gate voltage of the amplifier in the measurement was set to 2.967 V to get 83 mA current in the laboratory setup. Because this amplifier is matched to a 50Ω system instead of a single frequency, hence differing from other amplifiers used in test setup and made it possible to make the measurement within the whole band.

Figure 4.4 show the bandwidth of a gain above 10 dB. The gain starts to drop below 10 dB at the frequency of 3.25 GHz. Corresponding input and output matches (S_11 and S_22) are also shown in this figure. According to this plot, bandwidth of 2.2 GHz in which the gain is higher than 10 dB is achieved. The results of small-signal measurement with the simulation results presented in this thesis are quite similar. Hence, the results achieved in the small-signal measurement are overall quite good since the bandwidth obtained exceeds the requirements made in the beginning of this thesis work.

The input match gained here is relatively good, since the requirement is below -10 dB for the whole band and measurement results correspond to this, even exceeding in the low-end of frequency band as it is shown in Figure 4.4. Similarly, for the output side, matching seems to be quite good according to the same figure.

In production, there are several factors such as milling of printed circuit board, quality of solder joints and the position of metal screws which might contribute. Furthermore, models of passive components used introduce some uncertainties; hence it is necessary to confirm whether these components provide a good representation. Voltage drop in the supply cable of drain to DUT should also be compensated since this will impact the measured results. In addition to this, it is clear from the plotted figures that the large signal model has slightly less gain than the available transistors.

The fabricated power amplifier provides a gain of 11.46 dB in 1 dB compression point. Output power in this compression point is measured to be 41.43 dBm which is slightly

lower than the power achieved in Load pull simulations in ADS. At 2 GHz, Power added efficiency of 68.27% is observed while for drain efficiency it is 75.78% which corresponds to a typical efficiency of class-AB mode as it is discussed in previous chapters in this thesis.

5.1 Future work

During the design, tuning for harmonic frequency components was discarded. Further study would be done by terminating harmonic components up to 2f0, since the second harmonics of fundamental falls into the operating frequency band. This extension can be done in ADS using the circuit designed before by Marius Ubostad for his PhD thesis which is based on introducing phase shift. As a result of the harmonic tuning, an increased PAE can be achieved.

The measurement made in this paper covers small-signal and 1-tone large signal measurements. A good extension of this work would be to make further investigations of amplifier such as 2-tone measurements. In addition to this, some improvement in measurement setup in laboratory would result in better measurements.

Furthermore, as it is discussed before in this thesis, amplifiers used as driver in test setup was not able to enhance the measurement because of frequency limitations. In order to make more accurate measurements for high-end components of frequency band, another power amplifier operating in this band similar to the one fabricated for this thesis could be designed and used in test setup.

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A. Amplifier design in ADS

Simulation of original Bias-test network

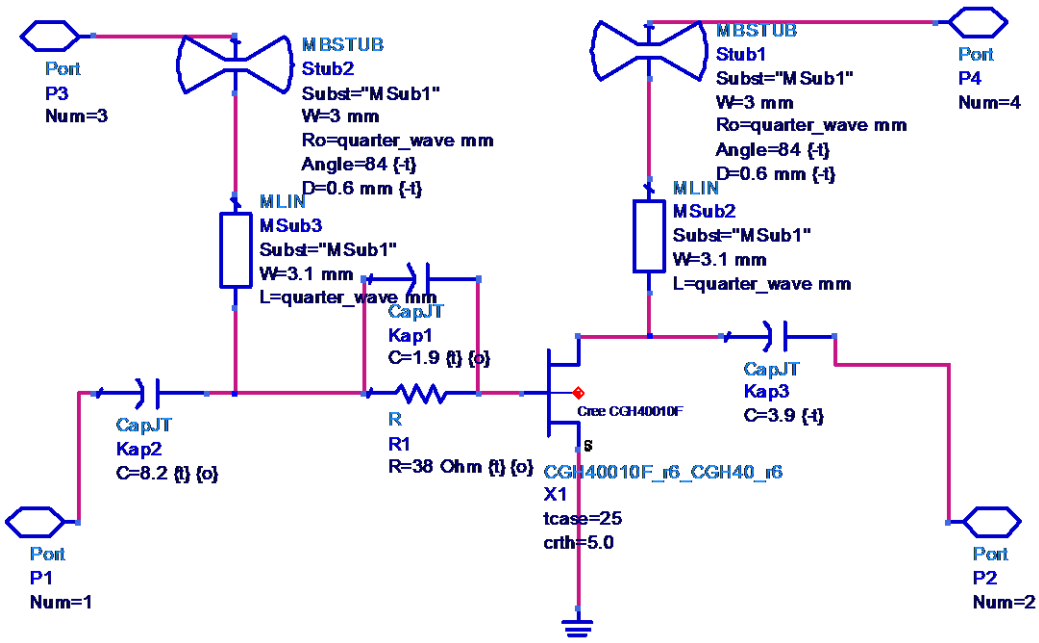

Figure A.1: Simulation with original Bias-test network

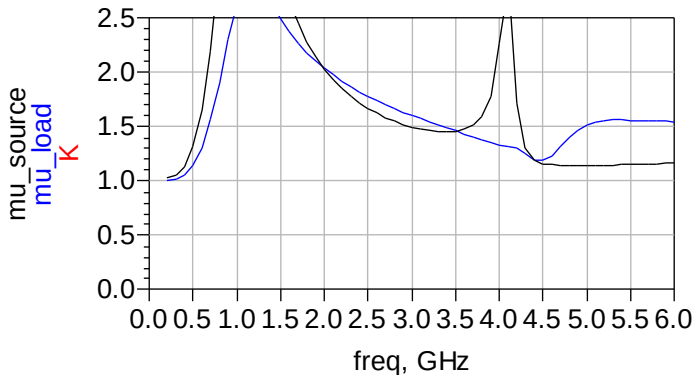

Figure A.2: Stability results from the circuit in Figure A.1

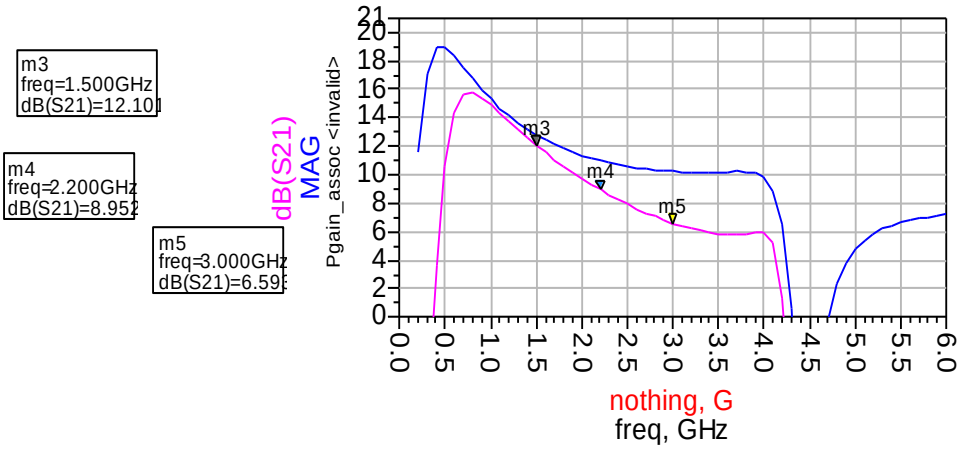

Figure A.3: Gain results of simulation the circuit in Figure A.1

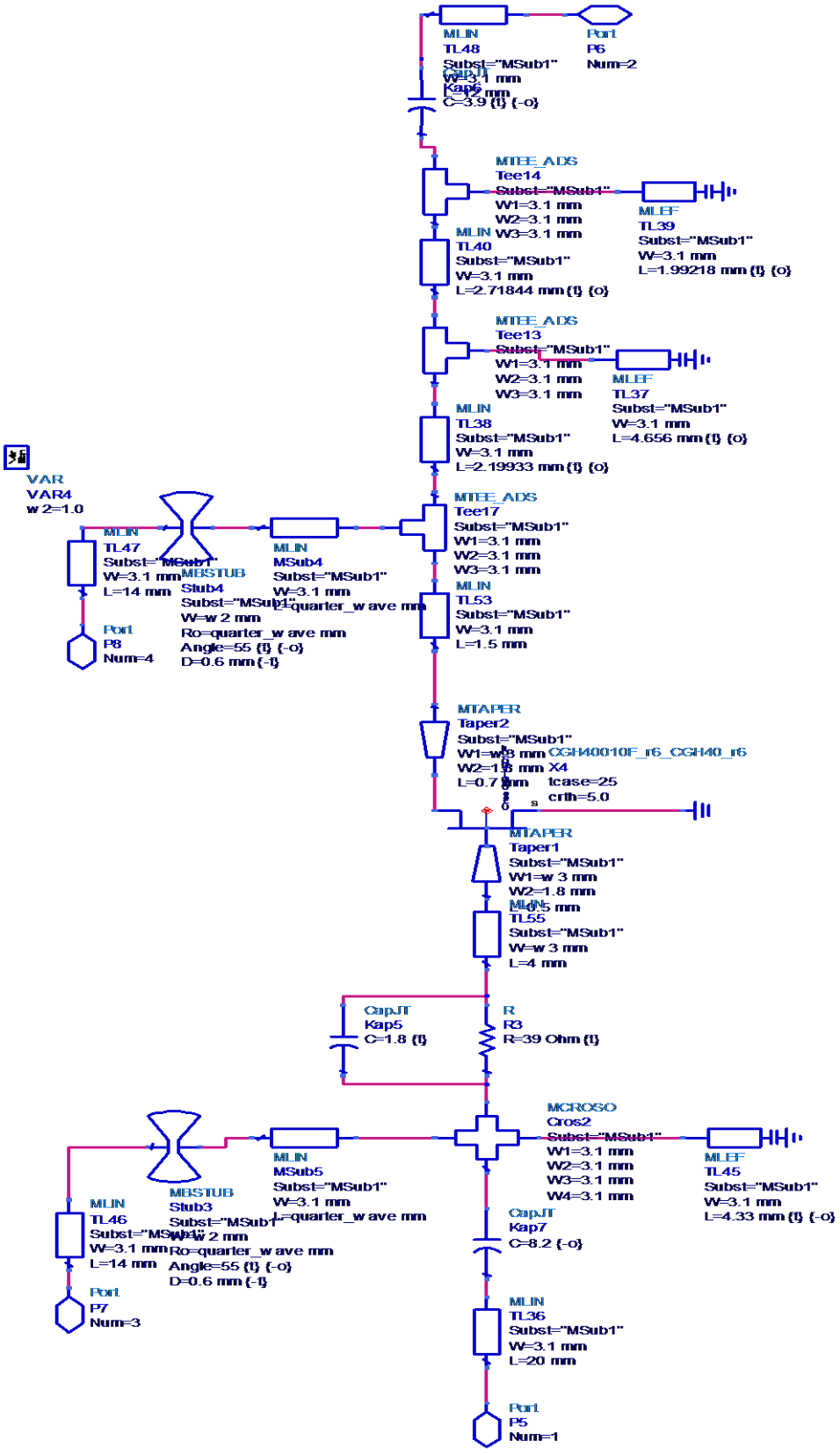

Figure A.4: Final design of the amplifier

Simulation of final design

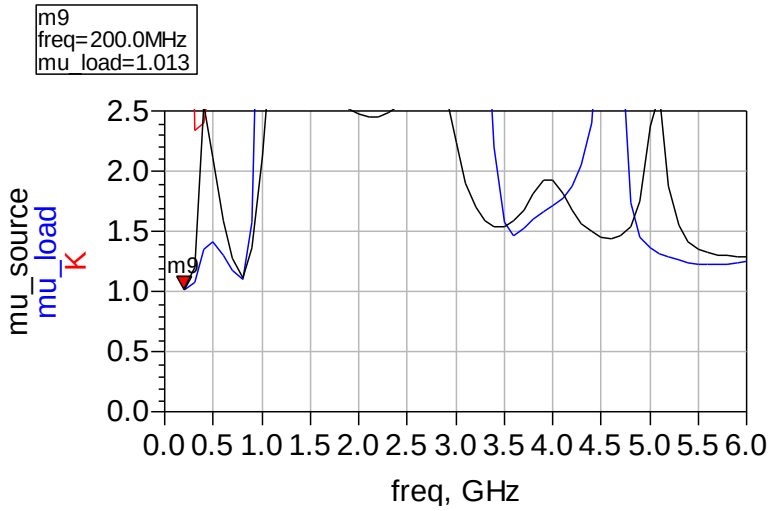

Figure A.5: Stability calculations of the device

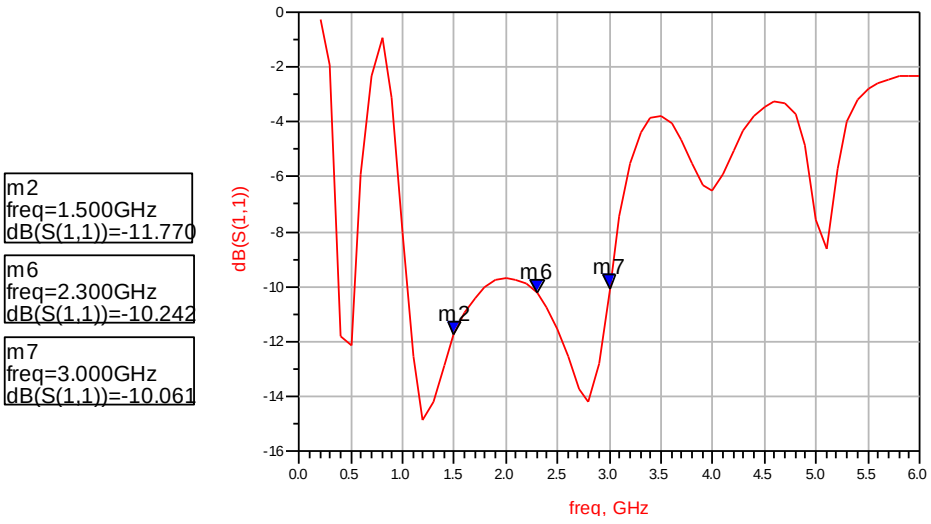

Figure A.6: S(1,1) characteristics within band

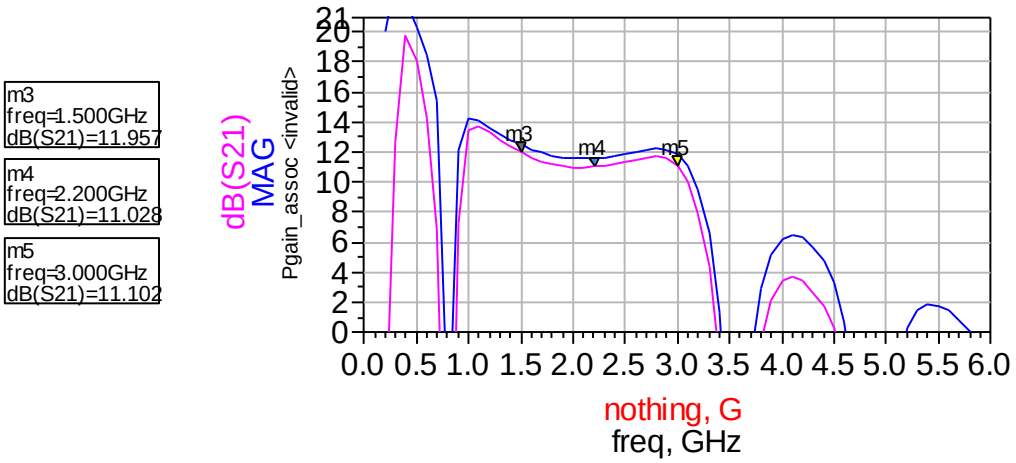

Figure A.7: Small-signal gain characteristics of final design within band

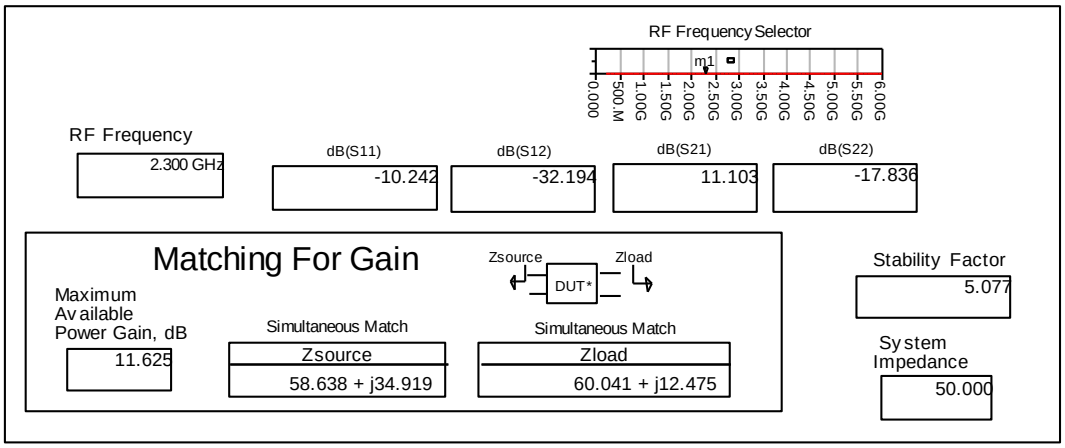

Figure A.8: Small-signal measurement results for the center frequency

Matlab code for imported measurement data displaying in Laboratory

```
function export_sparams(name,S,freq,unit,ref)
% Save 2-by-2-by-M S-parameter matrix to Touchstone S2P format
%
% Inputs:
% - name: specifies name and location of file to save data in
% - S: 2-by-2-by-M S-parameter matrix. S(i,j,:) = Sij
% - freq: frequency vector
% - unit: unit of frequencies, i.e. 'GHz' or 'kHz'
% - ref: reference impedance in ohm.

str = inputname(2);
fil = fopen(name,'w');
fprintf(fil,'! This file is written by MATLAB\r\n');
fprintf(fil,'! Date:\t%s\r\n',datestr(now));
fprintf(fil,'# %s S MA R %d\r\n',lower(unit),ref);
fprintf(fil,'! 2 Port Network Data from MATLAB variable %s\r\n',str);
fprintf(fil,'!
freq\tmagS11\tangS11\tmagS21\tangS21\tmagS12\tangS12\tmagS22\tangS22\r\n!\r\n');
fprintf(fil,'\r\n')

for n = 1:1:length(freq)
   fprintf(fil,...
      '%5.2f\t%12.5E\t%12.5E\t%12.5E\t%12.5E\t%12.5E\t%12.5E\t%12.5E\t%12.5E\r\n', ...

freq(n),abs(S(1,1,n)),angle(S(1,1,n)),abs(S(2,1,n)),angle(S(2,1,n)),abs(S(1,2,n)),angle(S(1,2,n)
),abs(S(2,2,n)),angle(S(2,2,n)))
end
fclose (fil);
end
```

Simulation for large signal measurements

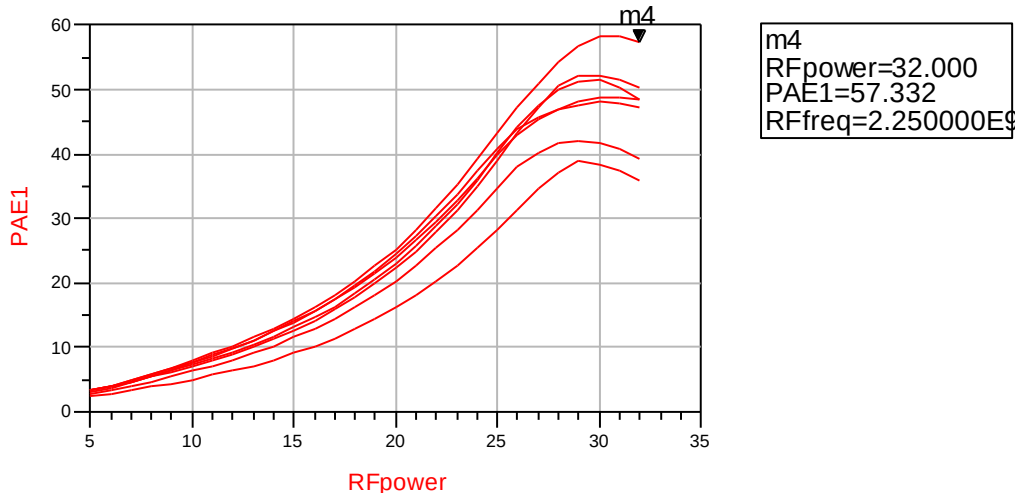

Figure A.9: Power added efficiency versus input power at center frequency

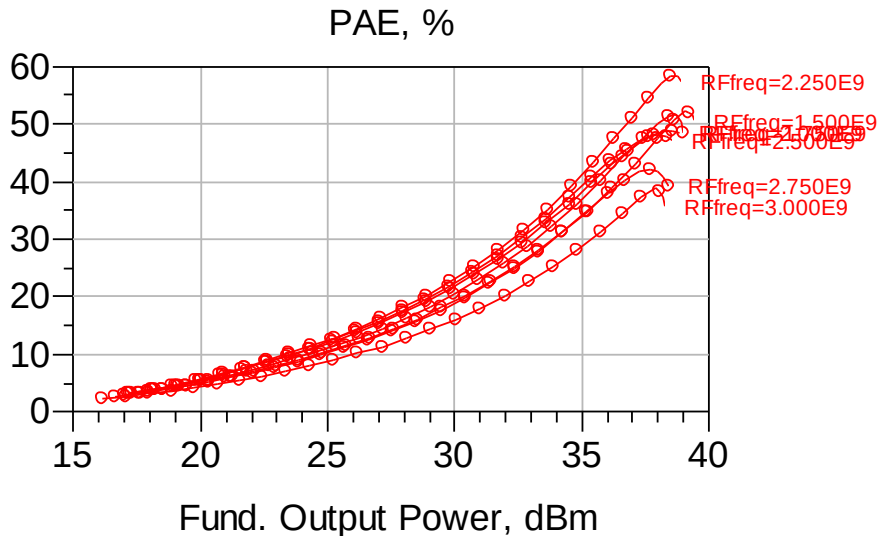

Figure A.10: PAE characteristics versus fundamental output power for different frequencies

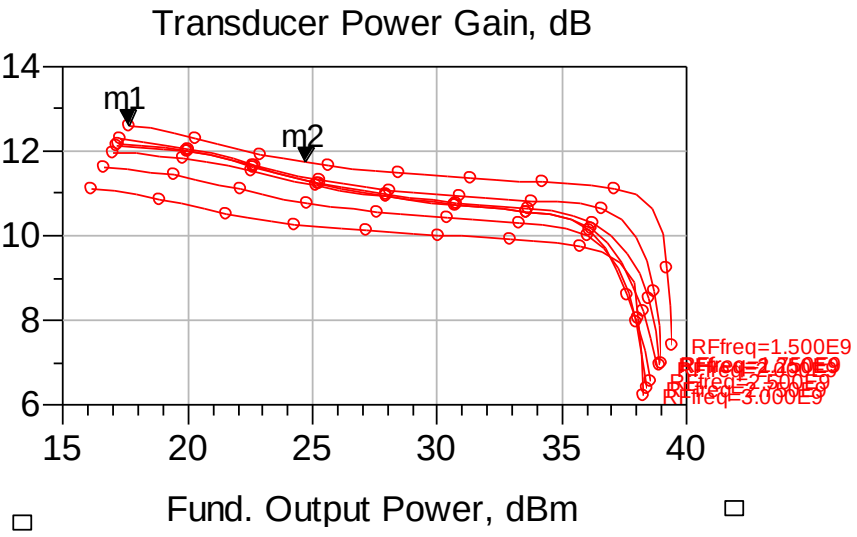

Figure A.11: Large signal gain characteristics of the device versus output power within band

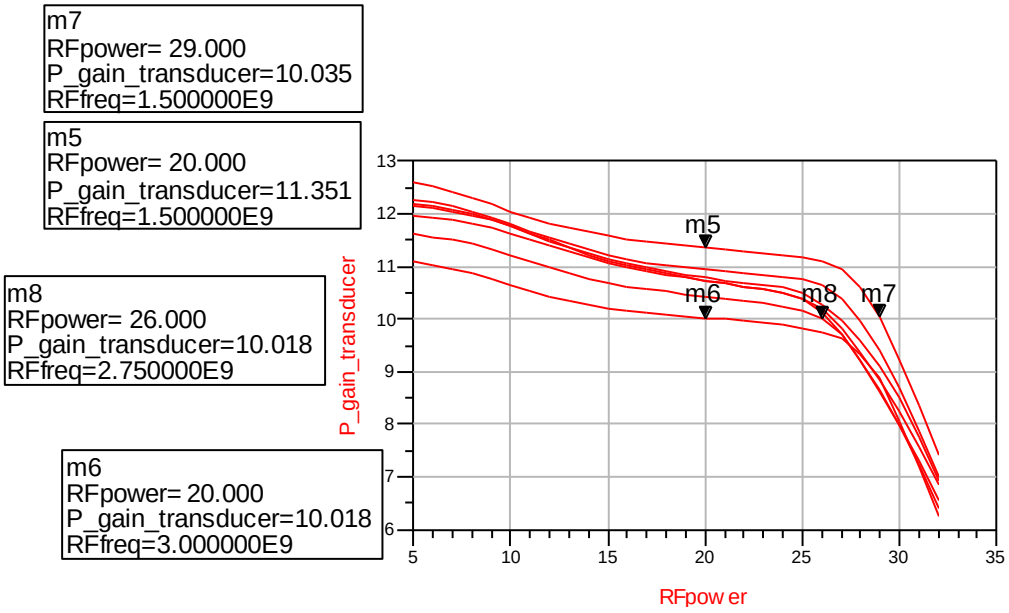

Figure A.12: Large signal gain characteristics of the device versus input power within band

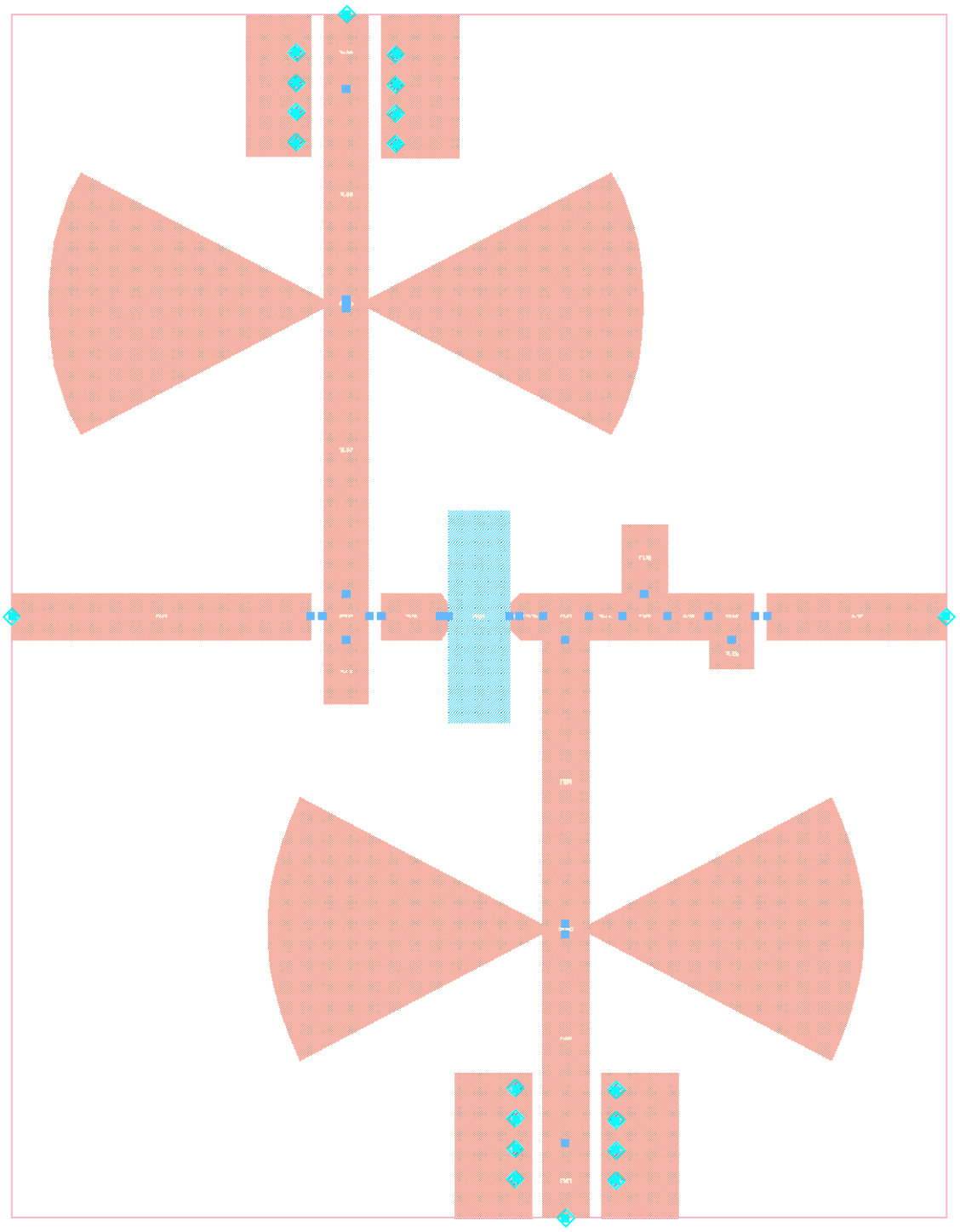

Figure A.13: Layout of the final design