

A 900 MHz 10 mW Monolithically Integrated Inverse Class E Power Amplifier

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Abstract— This work demonstrates a new integrated inverse class E amplifier circuit, employing a pHEMT switching device and fully integrated output network for pulse shaping. The circuit is particularly suitable for full integration, since it does not need any RF choke for biasing, and no DC blocking capacitor is needed between the switch and the output network parallel resonance circuit. The back plate capacitances of the additional capacitors are not connected to nodes that carry RF voltage signals. A commercial GaAs monolithic microwave integrated circuit process was used for fabricating the prototype circuit. 11.5 mW output power and 39% drain efficiency with 0.9 V supply voltage was measured at 895 MHz operating frequency. The output power remains over 10mW across 850-925 MHz, and the drain efficiency remains above 32% across this frequency range.

I. INTRODUCTION

In handheld and portable telecommunications terminals, the transmitter RF power amplifier is usually one of the most power consuming modules of the RF section. Sometimes the power consumption of the transmitter can be reduced by limiting the transmitting time. However, as many modern telecommunications systems must support continuous data transmission with high data transmission rate, the transmitter power amplifier efficiency usually plays a major role in reducing the total system power consumption and therefore the size and weight of the terminal.

Another important issue in mobile equipment power amplifier design is the possibility to integrate the RF power amplifier with the rest of the electronics. It usually turns out that the power amplifier is difficult to integrate at least for the following reasons: 1) the RF power amplifier needs different transistor characteristics from digital and low-frequency analog designs, 2) the power amplifier needs passive components that are not available in the available IC process 3) due to the limited efficiency of the power amplifier, self heating may degrade the performance of all circuits, 4) signal leaking from the power amplifier disturbs the other on-chip circuits.

To address some of these issues, switching amplifiers combined with Envelope Elimination and Restoration (EER) schemes and predistortion methods have been studied. In switching power amplifiers, the output pulse-shaping network

is usually made to generate a sinusoidal signal across the low-impedance load, while the other spectral components are made to help the amplifier in operating with good efficiency by keeping the voltage across the switching device low when it is conducting. If the voltage across the switch is zero when it is conducting current and the current is zero when the voltage across the switch is non-zero, no power is dissipated in the switching element. If the transition times between the off and on states are much shorter than the carrier period and the losses of the other output network components are negligible, the resulting DC-to-RF conversion efficiency will approach 100%. While 100% efficiency is not possible to achieve in practice, in many applications switching amplifier circuits nevertheless provide superior efficiency, compared with the classic amplifier alternatives.

Class E power amplifiers are in principle very suitable for EER and predistortion methods. One of the problems associated with integration is that the peak voltage across the switching element in the classic class E amplifier may rise up to 3.5 times the supply voltage. Since the transistors in many modern IC processes can stand only some volts of drain voltage, the classic class E designs are not easy to use with integrated designs. Class E designs also need relatively large inductor values, which are often difficult to integrate, as the spiral inductors that usually are available are rather small.

Recently, an inverse class E amplifier was proposed and investigated as an alternative to the classic class E amplifier [1-2]. This circuit (Figure 1) employs a bias choke L3 for feeding the DC supply current to the switching device. A DC blocking capacitor is necessary, in order to separate the output parallel resonance circuit (C1, L2) from the DC power supply. Since the DC block has to pass the amplifier's AC output current to the load, it has to be rather large in size. As it is located between the switching device and the output parallel resonator, it is difficult to integrate the switch together with the rest of the output network in a monolithic circuit without routing the RF signal out of the chip for DC blocking.

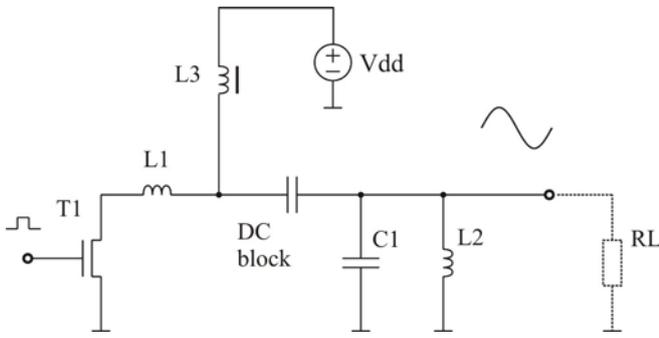


Fig. 1 A simple inverse class E amplifier, employing a DC bias choke and a DC blocking capacitor.

This paper describes a new choke-free inverse class E circuit topology, and demonstrates a simple integrated version of this circuit. The circuit is derived from the prior art inverse class E circuit ideas by rearranging the output network in the way that the circuit elements needed for biasing are either removed or moved to more favourable positions, regarding monolithic integration [3]. As the supply voltage and the RF signal input signal connections are similar to most other switching amplifiers, the circuit is compatible with many known EER and predistortion methods.

The scope of this work is to demonstrate that it is possible to integrate the output network and the switching device employing a commercial Monolithic Microwave Integrated Circuit (MMIC) process. Chapter II explains the new circuit topology, Chapter III describes the MMIC prototype implementation, Chapter IV presents the measured performance, Chapter V discusses the results, and Chapter VI presents the conclusions.

II. CHOKE-FREE INVERSE CLASS E AMPLIFIER

By removing the RF choke, adding capacitor C2, and rearranging the power supply connection of Figure 1, the circuit of Figure 2 is obtained. These modifications also move the DC blocking capacitor to the amplifier output. Since the remaining components of the pulse shaping network are rather small in size, they may be integrated on the same chip with the switching device without routing the signal outside of the chip for DC blocking. All integrated capacitors have one plate connected to the ground, which makes it easy to prevent the parasitic back plate capacitances from detuning the circuit. The DC block may be omitted, if it is acceptable to connect DC voltage to the load. Assuming an ideal and very large bypass capacitor C2, the resulting circuit has the same AC waveforms as the circuit of Figure 1, and the same equations for the component values are valid for both circuits [4].

Of course, the size of C2 is limited in practice. Due to the limited size and self-resonances, its impedance would not remain low at all harmonics of the operating frequency, which would make some RF currents to couple to the power supply. This would make the circuit sensitive to the power supply conductor dimensions and varying power supply impedance. However, since the task of C2 is only to bypass the power supply at the operating frequency and some of its harmonics,

C2 can be replaced with a set of series resonators, as is shown in Figure 3. Each resonator is tuned to one of the harmonic frequencies of the operating frequency. Since the capacitors in this resonator bank are very small, the total amount of capacitance in the resonator bank is comparable with C1. Since the resonator bank capacitors need not to be wideband, it is also easier to design a resonator bank than one single bypass capacitor that remains capacitive up to several harmonics of the operating frequency.

Yet another way to bypass the supply would be to combine a few resonators and a small bypass capacitor. As the RF currents at the harmonic frequencies are much lower than the current at the fundamental frequency, it may be sufficient to bypass the fundamental frequency employing a resonator, and the harmonic frequencies employing a small capacitor. This approach might simplify the design, yet resulting in a compact layout.

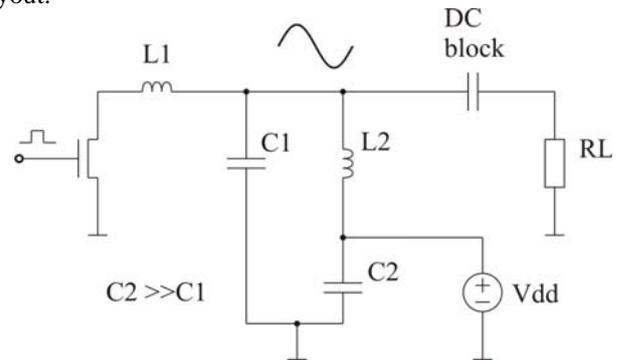


Fig. 2 An inverse class E amplifier without a bias choke. The DC blocking capacitor is not located between the switch and the pulse-shaping network.

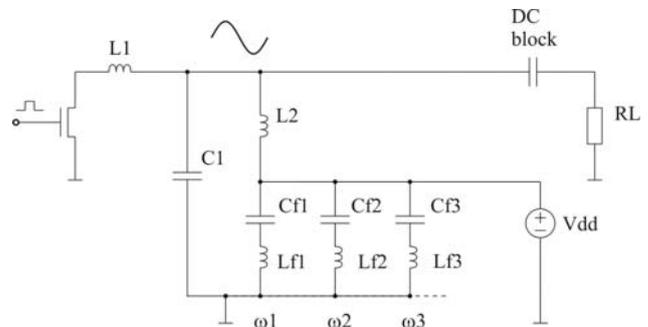


Fig. 3 The power supply bypass capacitor may be replaced with a set of series resonator circuits.

III. MMIC PROTOTYPE CIRCUIT

The schematic diagram of the MMIC prototype studied in this work is shown in Figure 4. For bypassing the power supply source, a series resonator (L3, C3) is employed at the fundamental operation frequency. The impedance at the harmonic frequencies is kept low by the MIM capacitor C2. Between the input pad and the switching transistor gate, there is an integrated L-match circuit (L5, C7) for coarsely matching the gate impedance to the signal source. In addition,

there is an RLC network (C5, R1, L4, R2, and C6) connected to the gate for improving the stability.

Minimizing the resistive losses in the output network is important, as the currents in the parallel resonator circuit (C1, L2, L3, and C3) are high. Suitable programs for generating octagonal spiral inductor geometries and high-Q MIM finger capacitors were written. All integrated passive components in the output network were EM-simulated in order to estimate their resistive losses. The D-mode pHEMT transistor size was chosen based on the channel on-state resistance. The transistor has 28 $0.5\ \mu\text{m}$ long gate fingers, and the total gate width is $1400\ \mu\text{m}$. As no large-signal model for the switching device was available, the circuit simulations were carried out using a simple switch model, with an associated serial resistor and a parallel capacitor for modelling the channel resistance and the drain capacitance, respectively. Transient simulations using the simple switch model implied that the drain efficiency in the presence of the parasitic resistances could be 30-40%.

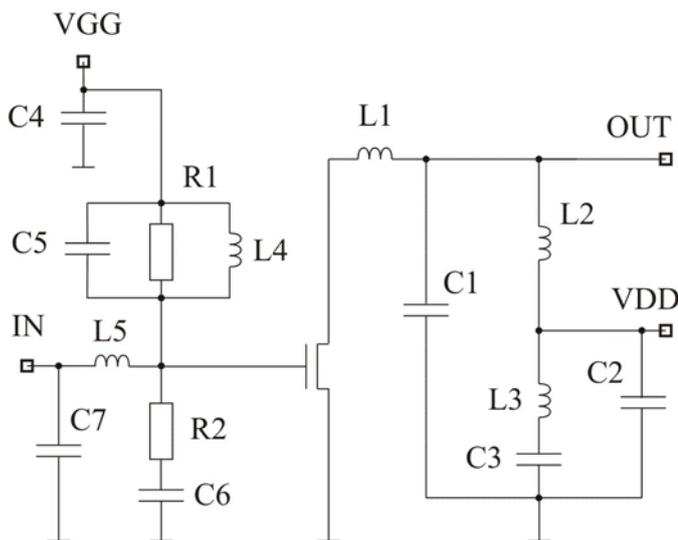


Fig. 4 The MMIC prototype circuit schematic diagram.

The circuit layout was designed both for probing the chip in an RF probe station, and for bonding the chip on a test circuit board. A photograph of the prototype chip is shown in Figure 5. The load resistance was set to 12 ohms, as this resistance is sufficiently high compared with the series resistances of the output impedance matching components. It is also sufficiently low resulting in reasonably low supply voltage. At the same time, it is high enough to keep the output L-match network capacitor and inductor sizes reasonable, if an integrated impedance matching network is employed in later designs. In this work, the 12 ohms load is converted to 50 ohms by an external tuner. The chip dimensions are $2.35\ \text{mm} \times 1.43\ \text{mm}$. The layout was designed for easy probing rather than the smallest possible size of the circuit.

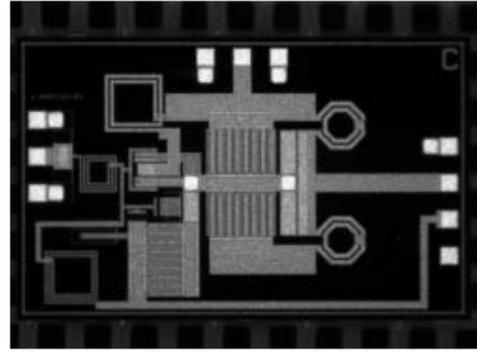


Fig. 5 A photograph of the prototype chip.

IV. MEASUREMENTS

The chip was mounted on a printed circuit board, and connected with $25\ \mu\text{m}$ bond wires to the gold-plated conductors of the FR-4 circuit board. The input and output RF signals were connected with bond wires directly to the ends of the corresponding 50 ohm microstrip lines on the circuit board. A manual stub tuner was used for matching the amplifier load impedance to 50 ohms for the measurement instruments, and an external DC block was inserted between the amplifier and the tuner. The amplifier input was driven directly from the signal generator, through an external DC block.

For the performance measurements, an unmodulated sinusoidal continuous wave signal was used. The input signal level was increased so much that the output signal did not increase significantly anymore with the drain voltage that gave 10 mW output power with the nominal operating conditions. The gate bias voltage VGG was adjusted to the level where the driving waveform duty cycle is 50%, in order to maximise the drain efficiency.

Figure 6 shows the measured output power and drain efficiency as a function of the drain supply voltage. The efficiency remains approximately constant across the supply voltage range. At 0.1 V drain voltage, the drain efficiency seems to increase as the driving signal obviously leaks through the switching transistor to the output circuit. The square root of the measured output power is comparable with VDD, showing that the voltage signals in the output network are proportional to VDD, which is the only reference voltage in the output circuit.

Figure 7 plots the output power and the drain efficiency as the operating frequency is varied. As can be seen, the operation is relatively wideband for a tuned amplifier. For example, the circuit delivers more than 10 mW in the 868 MHz ISM band with reasonable efficiency, even though the optimum operating frequency is 895 MHz.

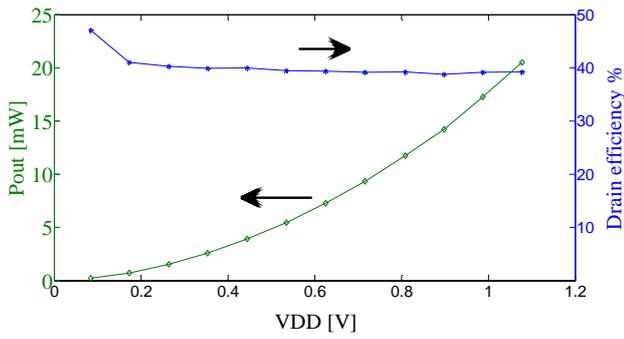


Fig. 6 Measured output power and drain efficiency vs. supply voltage.

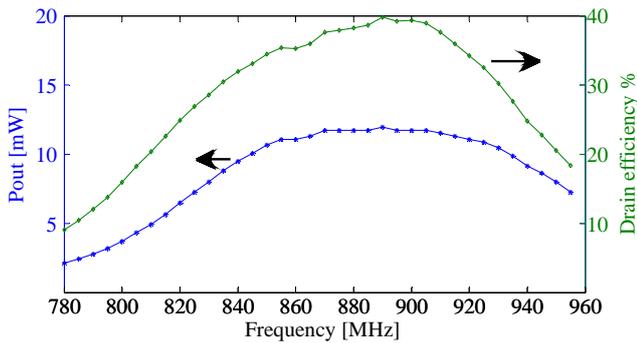


Fig. 7 Measured output power and drain efficiency vs. frequency.

V. DISCUSSION

By adjusting the load impedance by a stub tuner, the optimal load resistance of the prototype chip was found to be approximately 12 ohms. This impedance could easily be converted to 50 ohms for example by an integrated L-match network. The component values in this case would be $L=3.8$ nH and $C=6.3$ pF, which are sufficiently small to be integrated on the same chip. Alternatively, an external impedance matching circuit could be employed. In this case, the bond wire could be used as a part of the impedance matching network.

To avoid the output matching network altogether, the circuit could be designed to directly drive the 50 ohms load. However, the supply voltage would need to be higher. The necessary inductance values would also be higher, but since the resonator currents would be lower, thinner conductors could be used. In addition, the capacitances would be smaller, and the total layout size would not increase very much. As all voltages in the circuit would scale up, this approach would require an IC process that provides transistors with higher drain breakdown voltage.

The parasitic resistances of the most critical parallel resonator components (L_2 , L_3 , C_1 , and C_3) were estimated by EM simulations before the final circuit simulations, and the channel resistance of the switching device was estimated from the DC data given by the foundry.

The peak drain efficiency of 40% matches well with the simulations. The bandwidth of the prototype circuit is sufficient for compensating for less severe parameter variations in the process. Employing a commercial MMIC processes, the dominating parameter would be in practice the variation of the MIM capacitor capacitance. Fortunately, the resonance frequency of the output network is proportional to the square root of the capacitance. The optimal operation frequency is therefore inversely proportional only to the square root of the MIM dielectric thickness.

One of the problems of this (as well as any other inverse class E amplifier) circuit is that resistive losses in the output network circuit elements tend to reduce the efficiency. As the circuit operation is based on a parallel resonance circuit in the output network, the RF current circulating in the resonator is very high, if the loaded Q value of the resonator is chosen to be high. Therefore, the passive components of the output network should be designed carefully, and the Q value chosen in the way that losses do not reduce the overall efficiency too much. Scaling the output power specification up would also increase the currents and therefore the resistive losses in the output circuit, which must be taken into account.

Even though the simulation method was rather crude, the measured output power, supply voltage, and efficiency seem to fall within the expected ranges. Based on these experiments, it seems that using the simple switch model is sufficient for finding at least the starting values for the components, once the parasitic resistances of the output network inductors and capacitors are estimated correctly. For more accurate prediction of the performance by simulations, a large-signal model for the switching device should be used, in addition to EM simulations of the output network passive components.

VI. CONCLUSIONS

The circuit topology presented in this work is particularly suitable for full integration as there is no need for an RF choke, and there is no need to put a DC block between the switching device and the output pulse shaping network. The DC block is needed only if the load must be DC isolated from the amplifier output. The prototype amplifier delivers more than 10 mW of output power across the 850-925 MHz frequency range. The efficiency of the circuit is 32-39% across this frequency range. To our best knowledge, this work is the first demonstration of a monolithically integrated inverse class E power amplifier.

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