

Thomas Moe Halvorsrød

On Low Power, Analog Modules for Medical Ultrasound Imaging Systems

Thesis for the degree of Philosophiae Doctor

Trondheim, May 2010

Norwegian University of Science and Technology
Faculty of Information Technology, Mathematics
and Electrical Engineering
Department of Electronics and Telecommunications



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Abstract

This thesis describes analog, low-power modules intended used in the front-end of 3D/4D medical ultrasound imaging systems. The number of transducer elements in these systems is much higher than in conventional imaging systems because they are arranged in a matrix instead of a row. In the extreme case, the number of elements in a 3D/4D probe is squared compared to the classical 2D probe. To preserve the information generated by each single transducer element and effectively transfer it to the ultrasound console, it is believed that sub- or micro-beamforming on a small part of the aperture is necessary. Without any processing in the probe-handle the number of cables from the transducers to the ultrasound system is very high and equal to the number of elements. Such a cable is not practical to use. The classical ultrasound console is also not able to accept such a high number of signals. By its nature, beamforming reduces the number of signals by a factor equal to the number of elements processed. Micro-beamforming involves element-specific amplification, introduction of programmable delay per element and an effective summation node for all the delayed and amplified signals. Amplification is necessary to raise the signal- and noise-level before further processing. This is necessary to conserve high signal-to-noise ratio, SNR, and low noise-figure, NF, throughout the processing chain. Because the echoed signal is strongly attenuated when propagating in human tissue, time-variable gain is required in the amplifiers. This kind of gain is referred to as TGC in ultrasound-literature. Individual and programmable delay is necessary to steer the beam in the desired direction. The channel specific delay is updated from beam to beam. Typical update rate is in the kilohertz range.

Two main topics have been studied during this research. The first topic is design of low-power allpass filters. Log-domain topologies were identified as potential low power, high dynamic range modules. A log-domain allpass

filter with a power-efficient signal pre-processor is proposed and simulated. We were able to achieve $48dB$ dynamic range assuming a bandwidth of $20MHz$ when consuming $1mW$ of power. A micro-beamformer using the log-domain pre-processor and the log-domain allpass filter is also constructed and simulated. Because overall power consumption was found to be higher than what is believed to be acceptable in an application, a silicon prototype was not built. The delay line has dynamic range of $50dB$ dissipating $3.2mW$. Three delay cells were connected in series leading to four available delay steps. Three papers describing modules intended used in log-domain beamformers were written.

The second topic studied was the design of low-power, low-noise TGC amplifiers. This part of the study contains the most significant contributions. A low-power, gain compensation method compatible with all known basic amplifier architectures was proposed and implemented in silicon. The method was tested on charge sensitive trans-impedance amplifiers. Two different implementations with two different gain control schemes are demonstrated. The first implementation demonstrates $58dB$ instantaneous dynamic range and $12dB$ gain compensation when assuming a bandwidth of $20MHz$. Power consumption is $412\mu W$ and $663\mu W$ at high- and low gain-setting respectively. It is possible to adjust gain continuously from $26dB$ to $14dB$ varying an external control signal. The second design demonstrates $57dB$ instantaneous dynamic range and $15dB$ gain adjustment assuming the same bandwidth. Power consumption is $1.1mW$ and $2.2mW$ respectively. The first design is more power efficient than the second design. Though, the main goal of the second design was to demonstrate that positive feedback could be utilized in these kinds of circuits to relax the requirements on the active feedback cell. Necessary adjustment of trans-conductance was reduced from $100\mu S$ in the first design to $30\mu S$ in the second design. The results of the LNA study were published in three different papers.

Results from this thesis have found its way into several commercially available products and have therefore proven to assist making high quality cardiac imaging possible.

Preface

I submitted my Master Thesis to the Department of Physical Electronics at the Norwegian University of Science and Technology (NTNU) in Trondheim, Norway in December 1998. I immediately started working as a hardware designer at GE Vingmed Ultrasound AS (GEVU) in Horten, Norway. I found the work extremely interesting and realized quite quickly that to be able to contribute significantly in the development of future generation ultrasound systems I needed a more specialized training. I believed that a dr.ing/Phd-study would give me this. During summer 2001, I got acceptance for three years leave of absence from my job in GEVU. On September 1, 2001 I started working at NTNU in Trondheim.

During my studies, I was invited to assist in the development of three generations 3D/4D probes at GEVU. I considered this to be a golden opportunity and applied for leave of absence from the university in all three cases. This is the main reason why it has taken eight years to complete this thesis and close the research.

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List of Appended Papers

1. A Low-Power Method Adding Continuous Variable Gain to Amplifiers

Thomas Halvorsrød, Øyvind Birkenes, Christian Eichrodt

In proceedings of the
International Symposium on Circuits and Systems 2005
Kobe, Japan, 23-26 May 2005
Digital Object Identifier 10.1109/ISCAS.2005.1464907

2. A Dynamic Range Boosted, Low-Power Method Adding Continuous Variable Gain to Amplifiers

Thomas Halvorsrød

In proceedings of the
IEEE Norchip Conference 2005
Oulu, Finland, 21-22 November 2005
Digital Object Identifier 10.1109/NORCHP.2005.1597036

3. Continuous Variable Gain Amplifiers for Medical Ultrasound Applications

Thomas Halvorsrød and Giulio Ricotti

Submitted to the

IEEE Transactions on Circuits and Systems I, March 2010

4. A Low Power, Extended Dynamic Range, Fully Differential, Class AB, Log-Domain Allpass Filter

Thomas Halvorsrød, Werner Luzi

In proceedings of the
IEEE NORCHIP Conference 2003
Riga, Latvia, 10-11 November 2003

5. High Dynamic Range Preconditioning Circuit with Noise Cancellation for Fully Differential, Class AB Log-Domain Filters

Thomas Halvorsrød, Werner Luzi

Proceedings in The 46th IEEE
International Midwest Symposium on Circuits and Systems 2003
Cairo, Egypt, 27-30 December 2003
Digital Object Identifier 10.1109/MWSCAS.2003.1562221

6. A Log-Domain μ Beamformer for Medical Ultrasound Imaging Systems

Thomas Halvorsrød, Werner Luzi, Tor Sverre Lande

IEEE Transactions on Circuits and Systems I, January 2006
Digital Object Identifier 10.1109/TCSI.2005.857544

7. SCREAM - A Discrete Time micro-Beamformer for CMUT Arrays,

Thomas Halvorsrød, Linga Reddy Cenkeramaddi,
Arne Rønnekleiv, Trond Ytterdal

In proceedings of the
IEEE International Ultrasonics Symposium 2005

Rotterdam, The Netherlands, 18-21 September 2005

The following papers have also been published. Because they fall outside the theme of this thesis they are not included.

A Low Voltage Pseudo Floating-Gate All-Pass Filter

Øivind Næss, Yngvar Berg, Tor Sverre Lande, Thomas Halvorsrød

Proceedings in The 47th IEEE

International Midwest Symposium on Circuits and Systems 2004

Hiroshima, Japan, 25-28 July 2004

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B Active Floating Gate Circuits

Thomas Halvorsrd, Øivind Næss, Tor Sverre Lande,

Proceedings in the

IEEE International Workshop on BioMedical Circuits and Systems 2004

Singapore, 1-3 December 2004

Digital Object Identifier 10.1109/BIOCAS.2004.1454085

Abbreviations and Definitions

2D Two Dimensional

3D Three Dimensional

4D Four Dimensional, live 3D

AEC Analog Extension Class, A systemC class

AC Alternating Current

ADC Analog to Digital Converters

AMS Austria Microsystems

ASIC Application Specific Integrated Circuit

BF Beam-forming

BiCMOS Bipolar Complementary Metal Oxide Semi-conductor

CCCS Current Controlled Current Source

CCD Charge-Coupled Devices

CCVS Current Controlled Voltage Source

CDMA Code Division Multiple Access

CDF Common Drain FET

CMOS Complementary Metal Oxide Semiconductor

CMUT Capacitive Micro-machined Ultrasonic Transducers

DAC Digital to Analog Converter

DC Direct Current

DR Dynamic Range

HD Harmonic Distortion

IEEE Institute of Electrical and Electronics Engineers

NBW Equivalent Noise Bandwidth

ID Inter-modulation

IF Intermediate Frequency

IQ In-phase signal and Quadrature signal

I2V Current to Voltage Conversion

JSSC Journal of Solid State Circuits

FOM Figure of Merit

FPA Flat phased array

GEVU GE Vingmed Ultrasound AS

KCL Kirchhoff's Current Law

LNA Low-Noise Amplifier

LPF Low-pass Filter

MMIC Monolithic Microwave Integrated Circuit

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MESFET Metal Semiconductor Field Effect Transistor

NF Noise Figure

NMOS n-channel MOSFET

NTNU Norwegian University of Science and Technology

OLG Open Loop Gain

OTA	Operational Trans-conductance Amplifier
PDS	Power Density Spectrum
PGA	Programmable Gain Amplifier
PMOS	p-channel MOSFET
PSS	Periodic Steady State
RMS	Root Mean Square
SAP	Sup-Aperture-Processor
SNR	Signal to Noise Ratio
SOI	Silicon on Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
TGC	Time Gain Compensation
UWB	Ultra Wide Band
V2I	Voltage to Current Conversion
VCCS	Voltage Controlled Current Source
VCVS	Voltage Controlled Voltage Source
VGA	Variable Gain Amplifier
VLSI	Very Large Scale Integration

Part I

Research Summary

Chapter 1

Introduction

For several decades ultrasound has been used in medicine to examine soft tissue. The technique is based on the simple principle of analysing the echo from a transmitted sound wave. Typical frequencies used are in the low megahertz range. Resolution in radial direction is controlled by the wavelength. Higher frequency results in better resolution. On the other hand, attenuation increases with frequency. This reduces penetration. A rule of thumb is that ultrasound is attenuated $1dB/MHz/cm$. To increase performance, several transducer elements are placed next to each other. This enables beamforming. Beamforming is a technique used both during transmit and receive and is based on combining information from the individual transducers from different points in time. Electrical steering of the beams is possible if the delays can be controlled electrically. Resolution in lateral direction is controlled by the ability to place beams close to each other during beamforming.

Most commercially available ultrasound systems have a limited number of transducer elements inside the ultrasound probe. Often there is a one to one correspondence between each element and the system channel located inside the console. One cable is connected from the element to the console channel. This typically limits the maximum number of channels to a couple of hundred. A 2D plane is imaged placing the transducers in a row.

Many of us have seen the ultrasound image of an unborn baby. Without proper training or experience, it is a little bit challenging to understand what we really see. Resolution is one limitation that ultrasound manufacturers are always striving to improve. In reality, overall image quality could be improved by improving the front-end electronics. Dynamic range could be

increased and noise figure could be reduced. Though, because the processing power of computers is growing very quickly, most ultrasound image-quality improvements today come from increased signal post-processing. From cost point of view this makes perfect sense.

Now, post-processing alone would not change the fact that classical systems present a 2D slice of a 3D object. No post-processing alone could change this. To image the object under examination in 3D, significant changes to the front-end must be introduced. Mechanical tilting of the aperture is one solution that has been widely and successfully used by the industry for a long time. This is especially successful when the object under investigation doesn't move or move slowly. For cardiology, the mechanical solution has never been very successful. Contraction of the heart simply happens too fast. Instead, it is believed that the row of elements must be expanded into a matrix of elements. The imaging plane accessed by the beam from a row of element can then electronically be lifted up and down, not just back and forth. Information can then be transmitted into, and received from a three-dimensional space purely electronically. Electronics must be moved from the ultrasound console and into the probe-handle to enable this. Discrete components are too big and would enable only processing of a small number of channels. Application specific integrated circuits (ASICs) are one solution to the problem. One could imagine that by placing one or more ASICs in the probe-handle, one could do channel specific transmission, reception and delay and finally a summation of several processed channels. Each transducer could potentially get dedicated transistor and digital logic assigned to it.

Now, a great challenge when designing such a system is to get adequate performance. Dynamic range must be high at the same time as power consumption must be low. The probe containing the electronics will during normal operating mode touch the patient. The maximum temperature allowed by the regulatory authorities on devices to touch the patient is $43^{\circ}C$. Assuming that we want to turn a classical 64 channels 2D-probe into a 3D-probe. Assuming next a square aperture, 64 elements in one row translate into 4096 elements in the corresponding matrix. If we next assume each channel to consume $10mW$, total power consumption reaches about $40W$. Surface temperature of a $40W$ light bulb is definitely higher than $43^{\circ}C$. We understand that low power consumption is essential.

In addition to have high-end, high-performance systems available, consumers, including medical doctors, expect the industry to introduce portable,

handheld and battery-operated imaging systems. Based upon the development of mobile phones, it would be unrealistic to think that expectations to battery life on such devices should be any different. Design of integrated solutions like the ones discussed above could enable development and introduction of such devices. A few commercial available systems are already available.

1.1 Previous Work

To design VLSI, low-power, compact beam-formers it is necessary to understand fundamental beamforming theory, how to design delay-cells and how to design variable-gain-amplifiers (VGAs).

1.1.1 Beamforming Theory

Fundamental beamforming theory will not be discussed in this thesis. Thomenius gave a thorough introduction to the topic in [1]. Key literature is also referenced in his paper. Additional theory is presented by Angelsen in [2] and Wriath in [3].

1.1.2 Delay-cells

The delay cell studied in this thesis is based on log-domain implementation. A detailed description of log-domain theory can be found in [4]. Roberts and Leung references key work done in the field of log-domain filters. Log-domain theory is not discussed in detail in this thesis.

1.1.3 Integrated Beamformers

An introduction to fully integrated, analog beamformers can be found in the work of Stefanelli et. al in [5], in the work presented by Vermesan et. al. in [6] or in the work presented by Mo et. al. in [7].

1.1.4 Amplifiers

Amplifiers with programmable, switched or adjustable gain have been studied for several decades. A huge amount of papers are available on the topic. A few selected, published in the period 1968 to 2009, can be found in [8], [9] [10], [11], [12], [13], [14], [15] [16], [17], [18], [19], [20], [21], [22], [23], [24], [25],

[26], [27], [28], [29], [30] [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41] and [42]. Design of VGAs is the main topic of this thesis.

1.2 Primary Objective

The purpose of this research is to find efficient system- and circuit algorithms and specific circuit solutions that contribute to development of medical ultrasound imaging. Focus is kept on real time 3D/4D systems where analog signal processing is carried out inside the ultrasound probe. Low power, high dynamic range modules are necessary to enable 3D/4D imaging and to maximize image quality.

1.3 Main Contributions

The thesis is mainly concerned with the design and analysis of low power modules for future generation medical ultrasound imaging systems. The main contributions are:

- A technique extending the dynamic range of fully differential class AB log domain filters
- A fully differential, class AB log-domain allpass filter
- A log-domain micro-beamformer
- A framework for efficient simulation of large ultrasound beamforming systems using systemC.
- A low-power, continuous time, gain compensation technique compatible with all fundamental amplifier topologies. Measurements are presented.
- An extension to the demonstrated gain-compensation technique expanding the dynamic range. Measurements are presented.

It is important to mention that a dominating part of the results in this thesis would not have been possible without access to Nordholts book "Design of High-Performance Negative Feedback Amplifiers", [43]. This book has been a great source of inspiration.

1.4 Outline

This thesis is divided into two main parts. The first part gives an introduction to the challenges we face when trying to build real time 3D/4D ultrasound imaging systems. The fundamental limits are studied and previous work in the field is summarized. Fundamental, physical limits in analog design are studied and expectations to power consumption is established. Performance of the proposed circuits is compared to the fundamental limits.

The second part of this thesis contains the papers published during the research. In total, nine papers were written. All papers focus on challenges related to medical ultrasound front-end design. The topic in two out of nine papers is floating-gate-circuit design. This topic is considered to be outside the scope of the main research and is therefore not included in the thesis. A reference to the two papers is found in [44] and [45]. A complete reference to the other seven papers can also be found in the reference list.

Chapter 2

Figure of Merit for Analog Modules

Sufficient dynamic range is a very important parameter in medical ultrasound imaging systems. The echoed signal returning from human tissue during imaging suffer from heavy attenuation when propagating towards the receive electronics. Far-field signals are extremely weak and detection should be limited by the noise of the receiver. Noise in the pre-amplifier must then be as low as possible. High noise will deteriorate NF. At the same time, echoes from the near-field are very strong. It is important that the amplifier and subsequent modules can handle these strong signals at the same time as NF is low. Clipping is undesirable but often unavoidable. As far as possible, one must aim for rail-to-rail performance. High dynamic range is expensive in terms of power consumption. This section gives an introduction to the fundamental limits and compares the design presented in the research with these limits. Comparison of VGAs published in the period 1968 to 2009 is also performed.

2.1 Definition of FOM

Several studies on the fundamental lower limits of power consumption an analog circuits have been published, see eg. [46], [47], [48] and [49]. Walden proposed a figure of merit for ADCs in [50]. In this paper, dynamic range,

bandwidth and power consumption are combined in one equation, see (2.1).

$$FOM = \frac{DR \cdot BW}{P_{DIS}} \quad (2.1)$$

Here DR is the dynamic range, BW is the bandwidth and P_{DIS} is the dissipated power. Schreier and Temes argued in [51] that dynamic range should be squared. This is reasonable so that power quantities are related in the equation. Implicitly we have then defined dynamic range as the ratio between voltage-quantities and not power quantities, see (2.2).

$$DR = \frac{V_{SIG_RMS}}{V_{NOISE_RMS}} \quad (2.2)$$

We will use this definition for DR the sections below. The same approach was also used by Wulff in his Phd thesis, [52], and by Ytterdal in [53] and [54]. To have low numbers for power efficient circuits, equation (2.1) is often inverted. In the subsequent sections, the inverted FOM with dynamic range squared will be used, see (2.3).

$$FOM = \frac{P_{DIS}}{DR^2 \cdot BW} \quad (2.3)$$

2.1.1 Dynamic Range and Power Consumption

Minimum signal in an electrical circuit is limited by the noise-floor. Maximum signal in the same circuit is typically limited by the power supply¹. Dynamic range, the ratio between these to extremes, is in other words squeezed between the supply level and the noise level. What complicates the situation further is that more advanced technologies requires lower supply levels due to lower breakdown voltages. These technologies often also dictate lower power consumption per area. To achieve this, current levels must be reduced. Lower current levels leads to higher noise. This makes design of low-power, high dynamic range circuits challenging.

There is a fundamental tradeoff between dynamic range, power consumption and bandwidth. These quantities are strongly related to each other, see Fig. 2.1 to get a conceptual idea.

¹Dynamic range in current-mode circuits is not necessarily limited by the power-supply level.

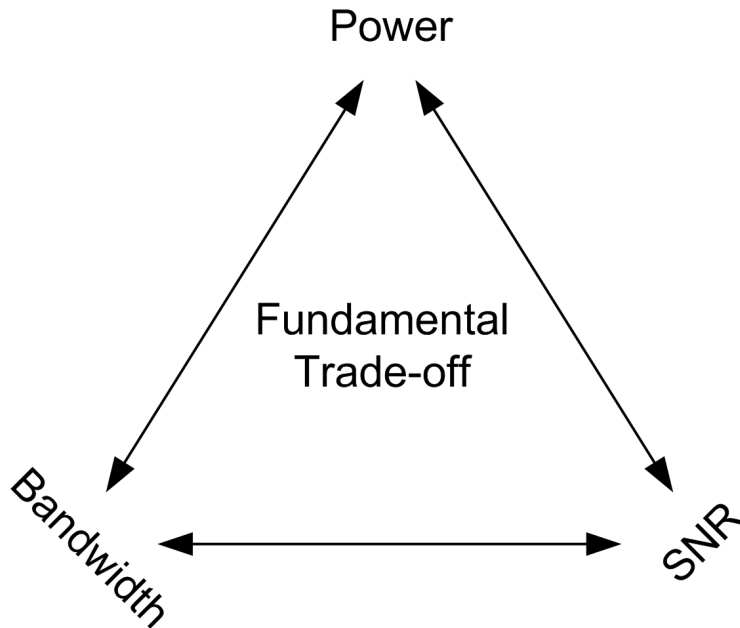


Fig. 2.1: Fundamental interactions in analog design

Minimum Power Consumption

To develop the equations relating these quantities, we start with the model shown in Fig. 2.2, [54]². Here the load capacitor, C , is driven by a class-A output-stage. In a class-A output stage, one driver module is handling the complete cycle. It is often said that the opening angle of the driver is 360 degrees. A constant current source, I_{DD} , is connected to the positive power supply, V_{DD} . During operation, I_{DD} is either steered into the load or down to ground through the controllable current source controlled by V_{IN} . For a module to be able to handle 360 degrees of a signal swing, quiescent current in the output stage must be as large as the maximum current to be delivered to the load. Because of this, efficiency in such stages can never be higher than 25% . This is well known and details can be found in [55].

In Fig. 2.2, the output voltage, V_{OUT} , is driving a capacitive load, C .

²A similar analysis was done by Vittoz in [49] and by Ytterdal and Wulff in [54]. In [54], dynamic range was expressed as the ratio between signal amplitude and rms-noise leading to a more pessimistic level for the absolute lowest energy level needed to drive the load. The author believes the analysis is more correct defining dynamic range to be the ratio between signal rms and noise rms values.

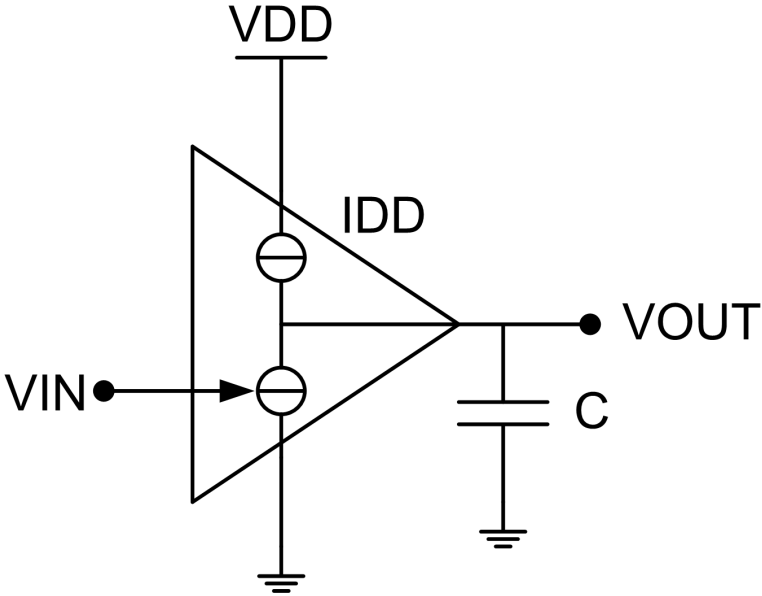


Fig. 2.2: Model for Power / Dynamic range ratio

Theoretical maximum amplitude is equal to half the supply voltage, $V_{DD}/2$. In reality it is somewhat lower due to non-zero saturation voltage in the current source. This effect is taken into account by the voltage efficiency, η_v , see (2.4).

$$V_{OUT}(t) = \frac{V_{PP}}{2} \cos(2 \cdot \pi \cdot f \cdot t) = \frac{V_{DD} \cdot \eta_v}{2} \cos(2 \cdot \pi \cdot f \cdot t) \quad (2.4)$$

In (2.4) f is the frequency and V_{PP} is the peak-to-peak value of the output signal. The current flowing into the load is given by (2.5).

$$I_{LOAD}(t) = C \cdot \frac{d}{dt} V_{OUT}(t) = -2 \cdot \pi \cdot f \cdot C \cdot \frac{V_{PP}}{2} \sin(2 \cdot \pi \cdot f \cdot t) \quad (2.5)$$

From (2.5) it is clear that the minimum bias current needed in the amplifier to drive the load throughout the complete cycle is $\pi \cdot f \cdot C \cdot V_{PP}$. In reality a slightly higher current is needed for biasing than what is delivered to the load. Steering 100% of the bias current into the load from the active circuits in the amplifier during operation would lead to unwanted distortion phenomenon. Current efficiency, I_{LOAD}/I_{DD} , is defined by η_i . Bias current

in the amplifier is $1/n_i$ higher than the maximum amplitude dictated by (2.5). The expression is shown by (2.6).

$$I_{DD} = \frac{\pi \cdot f \cdot C \cdot V_{PP}}{n_i} \quad (2.6)$$

Power consumption in the amplifier in Fig. 2.2 is equal to supply voltage multiplied by the average current, see (2.7). Average current is given by (2.6) because this current is close to constant independent if it is delivered to the load or simply flowing through the output stage to ground.

$$P = V_{DD} \cdot \overline{I_{DD}} = \frac{V_{PP}}{n_v} \cdot \frac{\pi \cdot f \cdot C \cdot V_{PP}}{n_i} \quad (2.7)$$

This result matches perfectly Ytterdal and Wulff in [54]. An ideal amplifier handling a typical ultrasound signal with $V_{PP}=3.3V_{pp}$, $f=3MHz$ and a load of $1pF$ would consume $100\mu W$ assuming $n_v = 1$ and $n_i = 1$.

Dynamic Range

Accumulated noise at the output node due to finite output resistance of the driver is given by (2.8), see [56] for details.

$$v_{noise_rms} = \sqrt{\frac{k \cdot T}{C}} \quad (2.8)$$

In (2.8), k is the Boltzmann constant and T is absolute temperature. Maximum rms output signal is given by (2.9).

$$v_{signal_rms} = \frac{V_{PP}}{2\sqrt{2}} \quad (2.9)$$

By first inserting (2.8) and (2.9) into (2.2), then inserting (2.7) into the resulting expression, we get an expression containing DR , P and BW . Then solving this expression with respect to $P/(DR^2 * BW)$, we find a solution for the figure of merit defined in (2.3). The result is shown in (2.10).

$$FOM = \frac{8 \cdot \pi \cdot k \cdot T}{n_i \cdot n_v} \quad (2.10)$$

Because of the definition of DR in (2.2), we find that the figure of merit deviates with a factor of 2 from the results presented in [54]. Assuming 100%

current- and voltage efficiency, the minimum amount of energy needed to drive a single pole is equal to $1.04e-19J$ at room temperature. This is twice as much as predicted by [54]. Note also that the expression only contains fundamental physical quantities. In the ideal case, the energy needed to drive a single pole is independent of signal amplitude and load conditions.

2.1.2 Dynamic Range in VGAs

Varying the gain of amplifiers is an effective way of increasing dynamic range. As gain is decreased, the amplifier can accept higher signals without going into saturation. At the same time, noise level is normally increased. The ratio between absolute maximum signal and absolute minimum signal is defined as dynamic range. Maximum signal can be handled at the lowest gain setting and minimum noise is present at the highest gain. Based on this, we define dynamic range for VGAs as shown in (2.11).

$$DR = \frac{\max(V_{RMS})}{\min(noise_{RMS})} \quad (2.11)$$

The instantaneous ratio of signal and noise in VGAs is labeled signal-to-noise-ratio, SNR, and is defined by (2.12).

$$SNR(gain) = \frac{V_{MAX_RMS}(gain)}{noise_{RMS}(gain)} \quad (2.12)$$

For VGAs, DR is then always higher than SNR. To have decent contrast in the ultrasonic image, a minimum SNR must be present at any depth or at any gain setting. E. Brunner indicated in [57] that instantaneous SNR should be in the $60dB$ range. Because of the differentiation of DR and SNR in VGAs, FOM as defined by (2.3) must be used cautiously when evaluating amplifier performance.

2.1.3 Previously Published VGA Concepts

Several VGA concepts have been published over the last 40 years. In most of the cases they can be put into the four categories described below and shown in Fig. 2.3, Fig. 2.4, Fig. 2.5 and Fig. 2.6.

- Circuits in category 1 vary the degeneration impedance of a differential pair and/or the bias current or bias voltage of the input stage.

- Circuits in category 2 attenuate the output by steering the information signal out of the signal path and away from the output (current-steering) or reduce the output signal by subtracting a weighted version of the inverted signal from the output (cross-coupled). The cross-coupled architecture is indicated by the dotted lines.
- Circuits in category 3 achieve gain-control by varying the trans-conductance ratio of the input stage and the diode-connected shunt circuit.
- Circuits in category 4 either controls the feedback factor or the amount of signal fed into the amplifier.

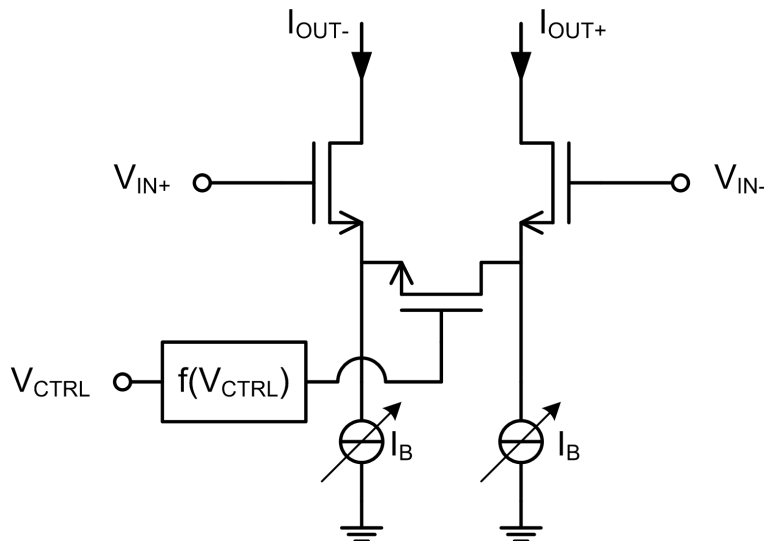


Fig. 2.3: Category 1: Trans-conductance adjustment

A thorough study of the publications available in the IEEE database was carried out. The circuits are given a comment in the sections below. Only a few circuits operating in the GHz-range are included. These circuits are typically not very interesting for medical ultrasound application mainly because they use inductors to achieve proper performance. In VLSI circuits for medical ultrasound, there is no space available for such components. From the paper-study, important performance parameters were recorded. FOM versus dynamic range was produced. Signal-to-noise-ratio at maximum and minimum gain is also plotted versus power consumption.

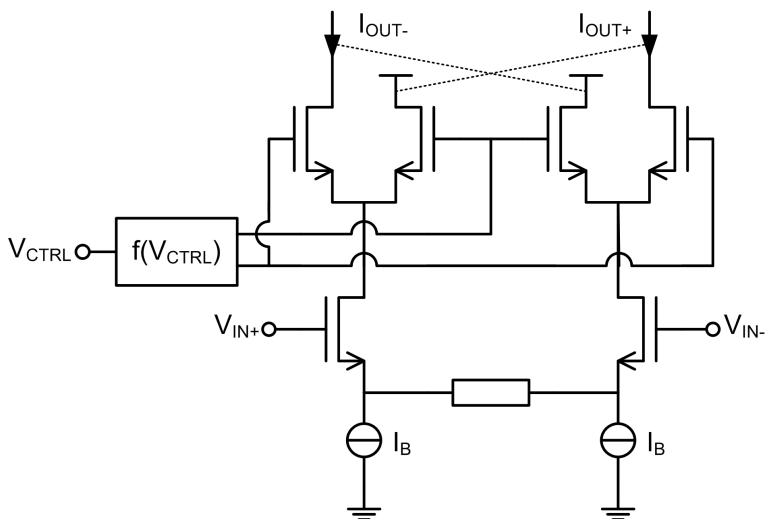


Fig. 2.4: Category 2: Current-steering / signal-summing including cross-coupled current-steering (indicated by the dotted lines)

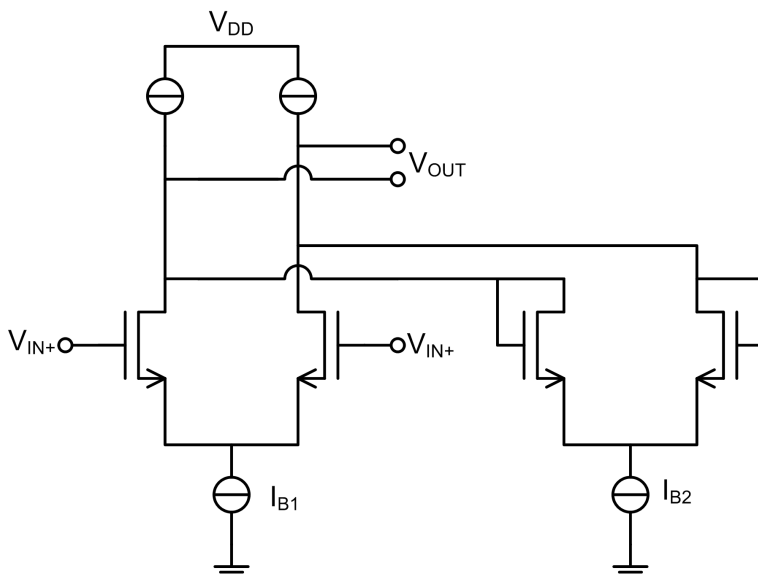


Fig. 2.5: Category 3: Trans-conductance ratio topology

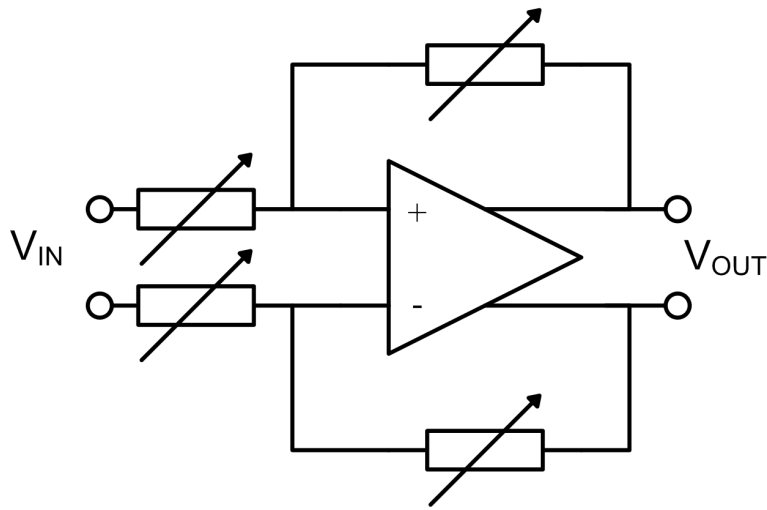


Fig. 2.6: Category 4: Feedback adjustment

Publications similar to the solutions proposed in this thesis are highlighted. An indication of the category is given.

2009

- In [8] from 2009, Elwan, Tekin and Pedrotti introduce a technique gradually changing the feedback network in a small unit element from one impedance-level, R_1 , to a second impedance level, $R_1 || R_2$ (Category 4). Several such unit elements are connected in parallel to construct a highly linear wide-range trim mechanism and a wide gain range.
- In [9] from 2009, Zheng, Yan and Xu present a VGA constructed from the cascade of three degenerated differential pairs (Category 1). Offset is cancelled using a I/Q tuning loop.

2008

- The AD600-series, [10], from Analog Devices uses the X-AMP technique, [58]. The X-AMP is based on a resistive ladder at the input of the circuit with highly linear interpolation modules connected in-between the discrete attenuation levels (Category 4). Continuous linear-in-dB gain control is achieved.

2007

- Azevedo, Fortez, Vaz and Rosario present a dual band CMOS VGA in [11] from 2007. The degeneration resistor is controlled by a 6-bit DAC (Category 1).
- The current-steering technique is implemented in a $0.18\mu\text{m}$ -CMOS-process by Fu and Luong in [12]. The intended application is UWB receivers. The differential currents from the input stage can be steered from positive to negative output and vice versa through a set of two cross-coupled cascode transistors (Category 2).
- In [13] Lee, Lee and Hong describe a VGA-circuit featuring a control voltage generator with a new method to setup the exponential function. Variable gain is achieved by controlling the gate voltage of cascade transistors. The effective trans-conductance of the input stage is varied because it is operating in the triode region (Category 1). The tail current is kept constant. The complete circuit consists of three offset-cancelled VGA-cells in cascade. A fixed gain amplifier is connected at the output.

2006

- A VGA with programmable gain and bandwidth is proposed by Tsou, Li and Huang in [14]. A R-2R ladder at the input of the amplifier is combined with a switched series-resistor to implement coarse and fine gain adjustment respectively. To achieve programmable bandwidth, the compensation network is also switched (similar to X-amp concept, category 4).
- A VGA with switched degeneration- and load-resistors is presented by D'Amico, Matteis and Baschirotto in [15] (Category 1). The circuit is intended used in multi-standard receivers covering WLAN, UMTS, GSM and Bluetooth. It has four discrete gain levels.
- A VGA with a variable source-feedback is presented by Masud, Zirath and Kelly in [16] (Category 1). The design is intended used in RF applications.

2005

- In [17], Carrara and Palmisano introduce additional, cross-coupled transistors in the differential input stage. Two extra transistors with floating and shorted emitters have their collectors connected to the opposite output. The authors claim that the parasitic path present in the classical differential pair during low gain settings, is effectively cancelled using cross-coupling. Overall gain is controlled adjusting the bias current (Category 1).
- In [18], Duong, Quan and Lee present a VGA built from a differential pair connected in parallel with a diode-connected load. Current in both the load and in the input pair can be continuously adjusted. Overall gain is given by the ratio of the trans-conductance in these two branches. Noise performance is not reported (Category 3).

2004

- A variable, resistive degenerated differential pair is used in the UMTS receiver presented by Gatta, Manstretta, Rossi and Svelto in [19] (Category 1). The VGA is used in a complete UMTS front-end system consisting of LNA, mixers, VCO and VGA. The VGA also incorporates offset cancellation.

2003

- A circuit operating the input stage in the triode region is described by Kwon, Kim, Song and Cho in [20]. Variable gain is achieved by adjusting the drain-source voltage and the bias current of the input stage (Category 1).
- Hsu and Wu presents a circuit using switched resistors in the voltage to current conversion network at the input of a current amplifier to realize gain control, [21] (Category 4). A very nice overview of VGA topologies is given in the introduction of the paper. Super-source followers are used to provide high input impedance.

2002

- In [22], Yamaji, Kanou and Itakura control the current flowing through the CMOS differential input-pair (Category 1). The input stage is di-

mentioned and biased to operate in the sub-threshold region. In this region, g_m is proportional to current. A master/slave technique is also included to have indirect feedback for stabilization over temperature.

- Koh, Youn and Yu propose a method using the cascode-transistor in an active feedback configuration to achieve switched gain, see [23] (Category 4). The proposed circuit does not contain continuous gain adjustment. Gain can only be switches between three different levels. In one of the settings, the amplifier is configured to have fixed, but active feedback. Because of this, the circuit is a subset of the method proposed by the author in [60]. Only simulation results are presented.
- Watanabe, Otaka, Ashida and Itakura propose gain compensation techniques to be used with signal-summing VGAs in [24] (Category 2). The techniques compensates for the gain-slope change in MOS-FETs when going from square-law region to exponential-law region. A control signal converter used to increase gain in the higher gain region is also proposed. The temperature dependent trans-conductance is compensated by adding a second VGA stage with a temperature dependent control signal.
- A switched capacitor VGA using positive feedback in addition to negative feedback to generate an exponential gain control is presented in the paper from 2002 by Fujimoto, Akada, Ogawa, Iizuka and Miyamoto, see [25] (Category 4). The VGA is intended used in CCD image sensor applications. The authors point out that the introduction of positive feedback reduces power consumption and increases bandwidth when comparing with Harjani's paper from 1995, [39]. The use of positive feedback effectively increases the feedback factor. A similar idea was utilized in the continuous time circuit proposed by the author in [61] and [62].

2000

- In [26], Otaka, Takemura and Tanimotot utilize the signal summing VGA first introduced by Salomon and Davis in 1968, [42] (Category 2). Otaka et. al. focus on stabilization of operation over temperature. A control signal converter referred to as a CSC, is also proposed.

- In [27], Mangelsdorf presents a circuit based on the diode-connected topology (category 3). The input stage is linearized using a second set of transistors in parallel.
- In [28], Green and Joshi present a circuit biasing the input stage in the triode region. Gain is adjusted by changing the drain-source voltage (Category 1).
- A circuit sensing the output signal in the current domain is fed back to the input through a current division network in the circuit presented by Elwan and Ismail in [29] (Category 4). Divisor size is controlled digitally with a six-bit word. Exponential gain control is realized using an implementation of the pseudo-exponential polynomial.
- The same current-steering technique proposed by Davis and Salomon is also utilized in the design presented by Sacchi, Bietti, Gatta, Svelto and Castello in [30] (Category 2). Maximum input signal is independent of gain due to the high input impedance and the lack of feedback. The circuit is able to attenuate the output down to zero.

1998

- Motamed, Hwang and Ismail describe a VGA circuit in [32] that utilizes a pseudo exponential current to voltage converter, an analog multiplier and an output stage (Category 1). The pseudo exponential converter is implemented using two back-to-back connected current mirrors. The authors claim that this circuit exhibits extremely good exponential characteristics. The multiplier is implemented using a square-law composite transistor.
- In [33] Huang, Chiou and Wang present a VGA-circuit using diode-connected loads (Category 3).
- In [34] Tadjpour, Behbahani and Abidi present a circuit built from a hybrid of a degenerated differential pair and an R-2R ladder on the input (mix of category 1 and category 4).

1997

- In [35], Sahota and Persico present an amplifier for CDMA applications using a variable degenerated differential pair succeeded by two

variable current amplifiers (Category 1).

- In [36], Lieshout and van de Plassche present a solution connecting several differential pairs in parallel, each offset by a small controllable voltage. When all offset voltages are the same, gain is at maximum. The authors report that when the offset is equidistant in the range $40mV$ to $60mV$, gain is at its minimum. The technique is referred to as differential-pair-transfer-summing (mix of category 1 and category 2).

1996

- In [37], Rijns presents a differential input, single ended output VGA for high frequency video applications. The circuit is based upon a *3-bit* programmable gain circuit using a R-2R ladder to degenerate the differential pair (Category 1). Degenerated gain is boosted using grounded gm-amplifiers in each tapping. The technique is also referred to as trans-conductance enhancement. Noise performance is poorly reported, making the FOM calculation somewhat uncertain.

1995

- In [38] Nishikawa and Tokumitsu use a circuit that is a subset of the concept presented in this thesis. A common drain FET, referred to as a CDF, is connected in the feedback circuit to control the feedback factor of a MESFET (Category 4). The common drain FET is a high input-, low output impedance module with fundamental equivalent properties compared to the trans-conductance cell used in [60], [61] and [62]. Unfortunately, power consumption is not reported making calculation of FOM as described in section 2.1 impossible.
- In [39], Harjani presents a VGA adjusting open loop gain of a differential pair by adjusting the bias current (Category 1). Harjani claim that $25dB$ of gain variation is possible with two stages in cascade. Only simulation results are presented.

1974

- Sansen and Meyer propose a circuit called the improved automatic-gain control amplifier in their paper from 1974, see [40]. The authors

recognize that to have low distortion, high dynamic range and flat transfer characteristics, different currents must flow in the differential input pair and the quads. The differential pair should have a high current while the quad should have low current. Additional current paths were added to the Davis/Solomon design to achieve this (Category 2).

1968

- In 1968, Davis and Solomon introduced the current-steering-technique (Category 2). A double differential current divider is driven by a differential input stage. Several of the above listed circuits are based on the Davis/Solomon topology or use derivations of this circuit, see eg. [42].

FOM Mapping of Published VGAs

The VGAs with enough performance parameters reported to enable calculation of FOM as defined in (2.3) is mapped below in Fig. 2.7. The following assumptions were used during evaluation of FOM.

- If the circuit contains attenuation, care is taken to evaluate if saturation happens at input or output to use correct value for maximum swing.
- Often, maximum swing is not reported. Supply level is then used to calculate maximum amplitude level. Unless rail-to-rail behavior is explicitly stated, we assume only half supply level to be useful³.
- If noise level is presented only as noise figure and source impedance is not explicitly stated, a 50Ω source is assumed.
- The equivalent noise bandwidth, NBW, used during calculation of dynamic range assumes low-pass, one dominant pole behavior. Reported 3dB-frequency is then multiplied by 1.57.

NF is defined as ratio between total noise, e_{total} , and noise from source, e_{source} , in the same node, see (2.13), [59].

$$NF = 10 \cdot \log_{10} \left(\frac{e_{total}^2}{e_{source}^2} \right) \quad (2.13)$$

³For early publications, this assumption is probably not fair due to potential high power supply level.

Equation (2.13) is most often used either at the input node or the output node of a circuit. The equation is valid in both cases. Assuming a circuit with voltage gain, G , and source impedance, R_S , total noise at the output can be calculated, see (2.14). This equation can also be used to calculate noise at the input assuming $G = 1$.

$$e_{total} = \sqrt{10^{\left(\frac{NF}{10}\right)} \cdot \left(10^{\left(\frac{G}{20}\right)} \sqrt{4 \cdot k \cdot T \cdot R_S}\right)^2} \quad (2.14)$$

When signal levels are expressed in dBm, conversion to voltage or current was done assuming 50ohm source or load. The relationship between power expressed in dBm, rms voltage and impedance is described by (2.15).

$$A(P, R) = \sqrt{\frac{10^{\left(\frac{P}{10}\right)}}{1000} \cdot R} \quad (2.15)$$

A is the rms voltage amplitude, P is the power in dBm and R is the impedance in ohm. 0dBm is equal to 224mVrms .

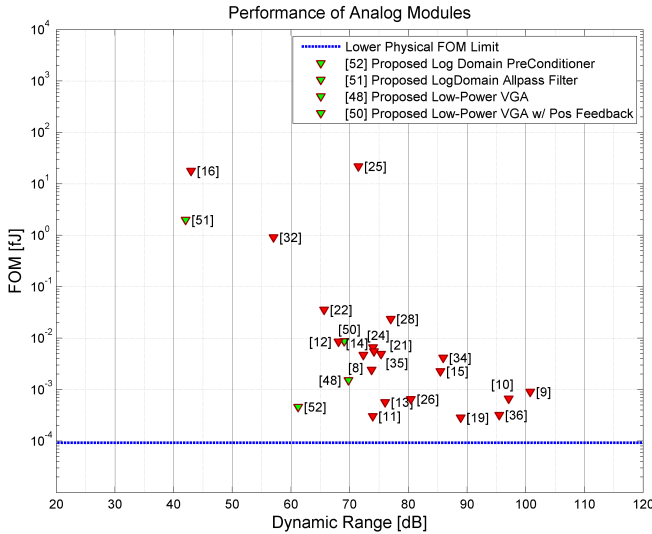


Fig. 2.7: Comparison of FOM for referenced circuits and the designs presented in this thesis

In Fig. 2.7 we see that circuits with higher dynamic range more easily achieve better FOM. Performance of the circuits presented in this is com-

comparable to several already published circuits when looking at Fig. 2.7 only. Though, in Fig. 2.7 the absolute power consumption is masked. As mentioned earlier, for a high number of transducer element, a maximum level for power consumption exists. Performance is re-plotted in Fig. 2.8 explicitly displaying SNR at maximum and minimum gain versus power consumption.

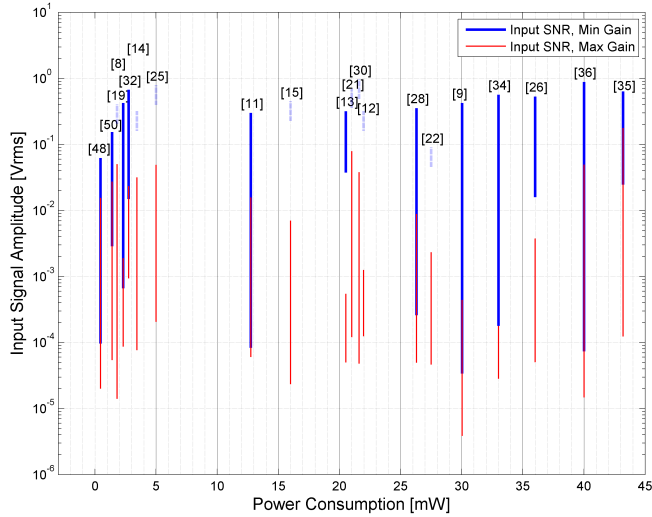


Fig. 2.8: Signal to noise ratio at maximum and minimum gain versus power consumption

Maximum and minimum signal- and noise level at both maximum and minimum gain are in many publications not reported. In publications where one or more number is missing, the bar is shaded and given a fixed length. In Fig. 2.8 the y-axis is logarithmic making it easy to get an idea of the SNR. One division is equal to $20dB$.

From Fig. 2.8 we draw the conclusion most of the referenced publications could not be used directly in medical ultrasound imaging applications. If Brunner's statement in [57] is correct, approximately $60dB$ instantaneous SNR is required at any gain setting. A few circuits report relatively good performance at both gain levels, see [9], [11], [28] and [36]. Overall power consumption is though relatively high.

Chapter 3

Research Overview

3.1 Research Background

It is believed that future generation ultrasound imaging systems will move more and more electronics into the probe handle. The reason for this is that the number of transducer elements will increase dramatically when going from traditional 2D imaging to 3D/4D imaging. This is because one or two rows of transducer elements will be extended into a full matrix of elements. To avoid losing information from the elements, it is believed that all, or part of the beamforming, must be executed inside the handle. Beamforming is a well-known signal processing technique that is used both with radio and sound waves. The purpose of beamforming is to change the direction of a sensor-array utilizing interference, [1]. Beamforming of N channels is described by

$$r_{RF}(t) = \sum_{i=1}^N A_i(t) \cdot s_i(t - \tau_i) \quad (3.1)$$

In (3.1), N channels are added together. Each channel is given a time-variant gain, $A_i(t)$. This is done both to optimize noise figure, NF , and to shape the beam-profile. Time-variant gain is necessary because of the high dynamic range of ultrasonic waves echoed from tissue. Attenuation in human tissue is known and gain can be scaled accordingly as a function of time. Time variant gain is often referred to as time-gain-compensation, TGC , in ultrasonic imaging systems. To account for the difference in travelling length to and from a specific point of interest, each signal from each

channel, $s_i(t)$ is also given an individual delay, τ_i . Constructive interference can then be created in the direction of interest.

3.2 Research Summary

The goal of the research presented in this thesis is to find power efficient solutions to the building blocks needed to implement (3.1). All findings and results are summarized in seven papers. The relationship between the papers is shown in Fig. 3.1. During the research two main paths were followed. The first one focused on design of channel-specific delay using log-domain all-pass filters. Results from this are found in paper 4, paper 5 and partly in paper 6. The second path focused on design of TGC amplifiers. Results from this are found in paper 1, paper 2 and paper 3. Two papers were written on the design of a complete micro-beamformer. These results are found in paper 6 and paper 7.

Paper 1, 2, 4, 5, 6 and 7 have been published. Paper 3 has been submitted for publication.

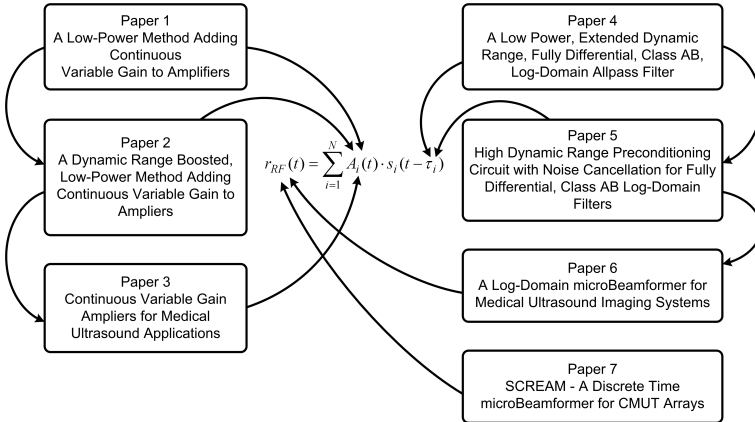


Fig. 3.1: Research overview and how the contributions relate to each other

The format of the papers are slightly changed to better fit this thesis. Apart from cosmetic changes and the fixing of minor typos, each paper is identical to their originals. A reference to the papers can be found in the reference list, see [60], [61], [62], [63], [64], [65], [66].

3.2.1 Time Gain Control Amplifiers

The concept of time gain compensation is shown in Fig. 3.2. The classical amplifier model using one forward path and one feedback path is shown in the left part. The time dependant feedback factor, $\beta(t)$, illustrates the focus of our research. In Fig. 3.2, A is open loop gain.

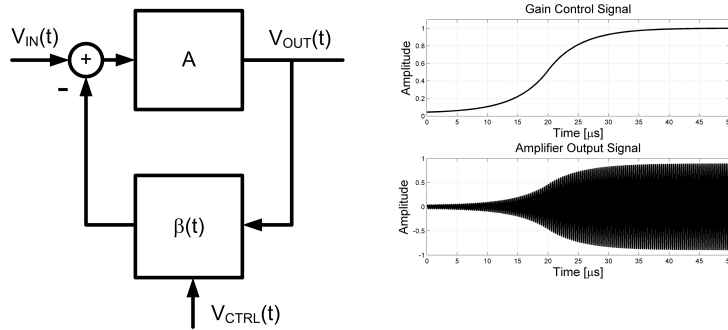


Fig. 3.2: TGC concept. Left: classical amplifier model. Right: typical signal signatures

The right part of Fig. 3.2 shows the output signal, $V_{OUT}(t)$, versus time when gain is adjusted from minimum to maximum. The input signal, $V_{IN}(t)$, is held constant while the control signal, $V_{CTRL}(t)$, is adjusted from maximum to minimum. The control signal $V_{CTRL}(t)$ is shown in the upper part and the output signal $V_{OUT}(t)$ is shown in the lower part. The main challenges when designing low-noise, low power TGC amplifiers are listed below.

- Noise.
 - Noise must be kept at an absolute minimum. The level is dictated by fundamental physics and is inverse proportional to the power consumption. Any added circuitry intended used for gain adjustment will add noise to the design deteriorating dynamic range and sensitivity.
- Power Consumption
 - Power Consumption per amplifier must be kept as low as possible because the final system will consist of thousands of amplifiers placed next to each other in a matrix. Maximum temperature

allowed in equipment to be placed on a patient is well defined and dictates the total power budget.

- Dynamic Range
 - Dynamic Range necessary in medical ultrasound applications is typically very high. Depending on available power, intended image quality, frequency range and application it is most often higher $100dB$. Dynamic range is expensive in terms of power. TBC
- Harmonic Distortion
 - Octave imaging is a technique where energy is transmitted on the fundamental frequency f_0 and the image is constructed based on the echoes from $2 * f_0$. This requires the harmonic distortion in the modules involved in the receive beamforming to have low second harmonic distortion. This is especially important in cardiology where octave imaging is more or less default.
- Area
 - The high number of transducer elements necessary to do 3D/4D imaging limits the available area to be used for each LNA.

Paper 1: A Low-Power Method Adding Continuous Variable Gain to Amplifiers

This paper presents the idea how to add gain adjustment to a fixed gain, low-power, low-noise amplifier. A physical implementation together with bench-measurements is demonstrated. The fixed gain amplifier used is a charge sensitive, common source, trans-impedance amplifier. Gain adjustment is added by connecting a trans-conductance cell to the fixed gain circuit. A dynamic range of $58dB$ over $20MHz$ bandwidth is achieved consuming $1mW$. The proposed technique adds $12dB$ of gain adjustment at the cost of $1mW$. In total, the circuit can handle $70dB$ dynamic range, over a bandwidth of $20MHz$ consuming $2mW$.

Paper 2: A Dynamic Range Boosted, Low-Power Method Adding Continuous Variable Gain to Amplifiers

Paper 2 proposes a method for minimizing the main weakness of the solution presented in paper 1. Large attenuation levels require a large control range for β . This is expensive in terms of power consumption. In paper 2, positive feedback is added to the adjustable feedback loop to make the module more efficient. A theoretical analysis is presented. The paper concludes that a linear control of gain down to $0dB$ is possible by linearly increasing power consumption.

Paper 3: Continuous Variable Gain Amplifiers for Medical Ultrasound Applications

Paper 3 analyses the fundamental theory presented in paper 2 in more detail and proposes a design solution. An implementation in a $0.35\mu m$ process is demonstrated. Measurement results are presented. A trans-conductance-cell is used as the main building block in the adjustable feedback path. The output signal from the fixed gain amplifier is converted into the current domain and added with a copy of the output of the trans-conductance-cell in a simple, one stage trans-impedance amplifier. It is the signal from the output of the trans-conductor fed back into the control circuitry that represents the positive feedback. $15dB$ gain compensation is demonstrated consuming $1.1mW$ extra power. Necessary trans-conductance in the adjustable modules is $30\mu S$. This is a reduction of $10dB$ compared to the solution in paper 1.

3.2.2 Delay Cells Using Allpass Filters

Assuming a narrow band system, delay can be constructed using allpass filters. An allpass filter is a filter with unity gain and a defined phase shift in the pass-band, see [67] and [68] for details. A first order allpass filter is

described by (3.2).¹

$$H(f) = \frac{1 - j \cdot 2 \cdot \pi \cdot f \cdot \tau}{1 + j \cdot 2 \cdot \pi \cdot f \cdot \tau} \quad (3.2)$$

In (3.2) f is frequency, τ is the time constant of the filter and j is the imaginary unit. Because the distance from the imaginary axis to the pole in the left half-plane matches perfectly the distance to the zero in the right-half plane, magnitude response is equal to one at any frequency. Any real implementation will of course have a roll-off at higher frequencies due to parasitic capacitance. By the rules of complex number multiplication, the phase response of (3.2) is found by subtracting the phase of the numerator by the phase of the denominator. The result is shown in (3.3) and expresses the phase shift in radians experienced by each sinusoidal component of the input signal.

$$\varphi(f) = -2 \cdot \arctan(2 \cdot \pi \cdot f \cdot \tau) \quad (3.3)$$

From the phase shift equation, delay in seconds for a sinusoidal can be calculated. Depending on the application, several definitions for delay exist. The most commonly used terms are phase-delay and group delay. Phase-delay, $P(f)$, is defined in (3.4).

$$P(f) = -\frac{\varphi(f)}{\omega} = -\frac{\varphi(f)}{2 \cdot \pi} \cdot T \quad (3.4)$$

Phase-delay is measured in seconds. Absolute phase-shift, $\phi(f)$, at a given frequency, f , is divided by one cycle, 2π , to get the waveform-shift in fractions of a wavelength. The result is then multiplied by the period to find the delay for that specific frequency in seconds.

When processing broadband signals containing a collection of frequencies, group delay is often used to describe the transit time through the filter. Group delay, $D(f)$, is defined as the derivative of phase, $\varphi(f)$, with respect to frequency, see (3.5).

$$D(f) = -\frac{1}{2 \cdot \pi} \frac{d\varphi(f)}{df} = \frac{2\tau}{1 + 4\pi^2 f^2 \tau^2} \quad (3.5)$$

¹Based upon the implementation, the sign of the magnitude response is easily changed. Typically an operational amplifier with the input signal connected both to the inverting and non-inverting input through passive networks, will change output polarity by using either a low-pass filter at the positive input or a high-pass filter at the positive input. Details and examples can be found in [67]. An example using a low-pass filter is shown in Fig. 3.3.

It can be shown that group delay describes the delay of the amplitude envelope of a narrow-band collection of signals, see [68]. For this to be true, the bandwidth of the signal must be limited to a range where the phase response is approximately linear.

A simple example of an allpass-filter-implementation using an op-amp is shown in Fig. 3.3. The circuit in Fig. 3.3 is described by equation (3.2) and (3.3). Delays in the tens of nano-second range, is what we are aiming for when building medical ultrasound imaging beamformers. When the phase response is linear, the group delay is equal to phase delay. This is recognized in the low- and high frequency range in Fig. 3.3.

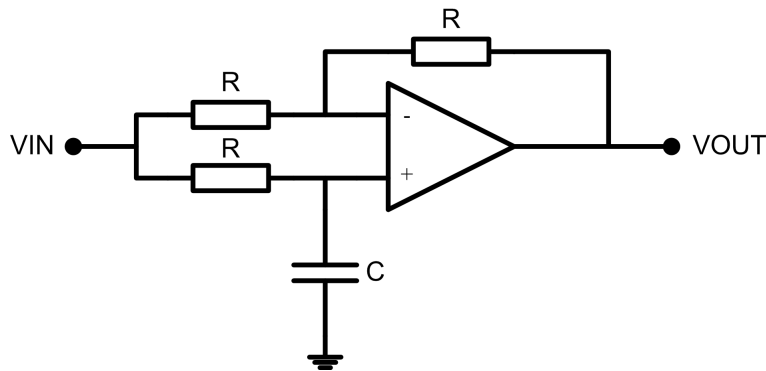


Fig. 3.3: Simple allpass filter implementation

Magnitude response, phase response and phase- and group-delay versus frequency is shown in Fig. 3.4. In the example, we assume $R=100k\Omega$ and $C=1pF$. The time-constant, τ , in this case is $10\mu s$.

Paper 4: A Low Power, Extended Dynamic Range, Fully Differential, Class AB, Log-Domain Allpass Filter

This paper presents an allpass filter intended used as a delay cell in a 3D/4D ultrasound micro-beamformer. In the paper, the allpass filter is built based upon a rewritten version of the transfer-function equation. It is shown that allpass filtering of a signal is equal to low-pass-filtering of the signal multiplied by two minus the signal itself. Because the signals are already in the current domain, the circuit implementation, and especially the subtraction, is very effective. To minimize power consumption and to avoid internal nodes from moving outside their normal operating conditions, the input

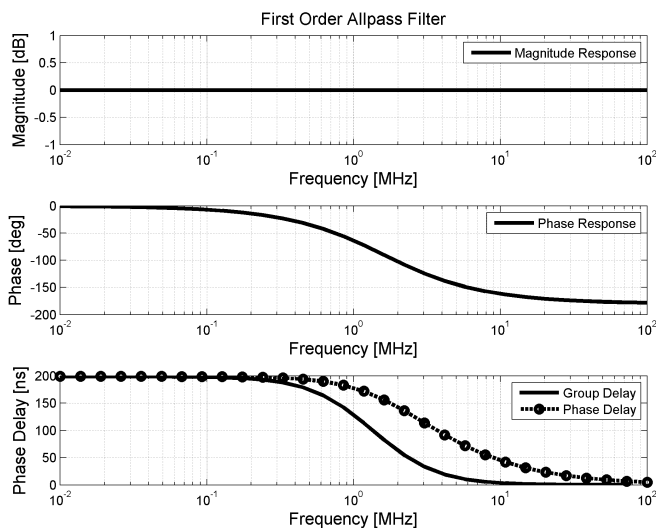


Fig. 3.4: - Generic allpass-filter response

signal must be preconditioned to be strictly positive. The trans-linear circuit presented in paper 5 is inserted in front of the allpass filter. Overall dynamic range is found to be $48dB$ at a power consumption of $1mW$.

Paper 5: High Dynamic Range Preconditioning Circuit with Noise Cancellation for Fully Differential, Class AB Log-Domain Filters

Paper 5 proposes a preconditioning circuit to be used to shape the input signal connected to differential, class AB log-domain filters. The preconditioning circuit is based on a trans-linear circuit generating the geometric mean of a signal. The Gilbert multiplier used in the circuit core is well known and presented in [69]. In the proposed architecture, two such multipliers are slightly modified and cross-connected. The dynamic range of the resulting circuit is increased both because it handles higher input swing but also because noise cancellation is carried out.

Paper 6: A Log-Domain μ Beamformer for Medical Ultrasound Imaging Systems

Paper 6 describes a micro-beamformer with four inputs and four delay levels. The micro-beamformer is constructed using the log-domain preconditioning

circuit and the log-domain allpass filter described in paper 4 and paper 5. To achieve four delay levels, three allpass filters are connected in cascade. Each input has its own preconditioning module. The presented design achieves $50dB$ dynamic range at a power consumption of $3.2mW$. The most severe limitations of the presented topology are the dynamic range reduction through the cascade of allpass filters, the narrow band operating range and the delay dependant noise levels. When using a cascade of filters as presented in the paper, lower dynamic range and higher noise figure is obtained for higher delay levels. The range of linear phase is also very limited due to the use of a single allpass filter to delay the echoed signals. Performance is expected to be very limited due to this. Because of these disadvantages, a prototype was not built. Signal dependant noise levels due to the class AB architecture is also considered a concern. The gain in power consumption due to the dynamic basing is though very interesting.

Paper 7: SCREAM - A Discrete Time μ Beamformer for CMUT Arrays

Paper 7 presents a systemC model of a discrete time micro-beamformer. An extension to systemC known as AEC is used to build the system. AEC is an abbreviation for analog extension class. This class is developed at NTNU. Models for TGC preamplifiers, the delay-cells, the delay-line and the summation nodes were constructed. The effect of gain-mismatch and jitter was studied. A micro-beamformer consisting of 16 inputs connected to a ring-buffer-shaped delay-line were demonstrated. It is shown how the beamformer delays the individual signals and add them in-phase to increase the output amplitude.

3.2.3 Clarification of Contributions

Paper 1 is co-authored by Øyvind Birkenes and Christian Eichrodt. During 2004 I had an idea how to add power efficient, low-noise gain adjustment circuits to low-noise amplifiers. Both Øyvind and Christian are experienced senior engineers and assisted in the implementation and refinement of the fundamental ideas. We worked close and intensively together during implementation. The design was a success on the first spin. On the paper, Øyvind and Christian functioned as discussion partners and reviewers.

I am the only author of paper 2. During design of the circuit presented in paper 1, a very severe limitation was discovered. An idea how to fix the

limitation was developed and elaborated in paper 2.

Paper 3 is co-authored by Giulio Ricotti. Giulio enabled the implementation of the ideas presented in paper 2. Giulio provided valuable questions and worked as a great discussion partner during the design.

Paper 4 and 5 are co-authored by Werner Luzi. Frequent discussions and brainstorming-sessions between the authors resulted in the presented topologies during summer of 2002. The circuit-solutions were worked out jointly in this period. Luzi was assigned new tasks by the end of the summer. At this point I spent the next year at the university studying and documenting theories related to our results. This resulted in the two publication of the two papers.

Paper 6 focuses on the same topic, though building a system from the single building blocks. This paper is co-authored also by Professor Tor Sverre Lande. Due to his long experience in academia, Lande acted as a very valuable discussion partner and reviewer during the writing process. We believe that the quality of the paper was increased significantly due to his role.

Paper 7 is co-authored by Trond Ytterdal, Linga Cenkeramaddi and Arne Rønnekleiv. During 2005 we had a project running at the university focusing on CMUT design and analysis. Linga wrote the jitter analysis section of the paper. Both Trond and Arne provided valuable information and background theory for the paper.

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Part II

Publications

Chapter 4

Paper A

A Low-Power Method Adding Continuous Variable Gain to Amplifiers

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Proceedings at the

IEEE International Symposium on Circuits and Systems

Kobe, Japan, 23-26 May 2005

4.1 Abstract

A method adding continuous gain control to high performance amplifiers is suggested. Any high performance, fixed gain amplifier can adopt the proposed method without deteriorating the performance of the core amplifier. The method is based on the idea of introducing an additional, adjustable feedback path in parallel with a fixed feedback path. The additional, adjustable feedback path can be an active feedback cell compatible with the amplifier architecture used. A low noise trans-impedance amplifier would for example require an additional adjustable trans-conductance cell with proper phase characteristics in parallel with the fixed feedback element used. By making the feedback factor of the adjustable feedback path proportional to the power consumption, extra power is only consumed when gain reduction is necessary. This feature is especially valuable in applications where gain reduction is necessary for a short period of time. One application having this feature is medical ultrasound imaging. The proposed method was originally developed for real-time 3D ultrasound imaging but is compatible with all systems requiring continuous gain control.

A prototype circuit was designed where the dynamic range was increased 12dB for an amplifier having 58dB SNR over a bandwidth of 20MHz with a peak penalty of 46% increase in the power consumption from $412\mu\text{W}$ to $663\mu\text{W}$. The prototype amplifier was designed to work at frequencies in the low MHz range.

Index Terms—Gain compensation, gain control, low power, variable gain amplifiers, ultrasound front-end.

4.2 Introduction

Dynamic range (DR) is expensive in terms of power consumption. A certain amount of DR will for an ideal circuit solution require a minimum amount of power as derived by [1]. Any real circuit implementations aiming for a given DR will always consume more power than what this fundamental limit dictates. The pressure of introducing handheld, portable or even wireless versions of available products is constantly increasing. The power consumption in such equipment must continuously be reduced while the performance must be kept constant or even increased. If batteries are used, better utilization is desirable and the number of recharging cycles needs to be reduced. Due to these aspects, low power, high dynamic range design is

more important than ever before.

Adding variable gain to amplifiers is one way of increasing DR of a system. Several successful implementations of variable gain amplifiers (VGAs) and the more general signal multipliers have been demonstrated throughout time, [2]-[7]. This paper demonstrates a general method adding variable gain to amplifiers keeping the power consumption low and the performance high, [8]. We define signal to noise ratio, SNR, as the ratio between the weakest and the strongest signal present simultaneously. DR is defined as the ratio between the weakest and the strongest signal a module can cope with though not necessarily at the same time. The situation is shown in Figure 4.1.

A variable gain amplifier will have a DR that is higher than the SNR. As the gain is reduced, the amplifier will be able to handle higher input swing at the penalty of high noise level.

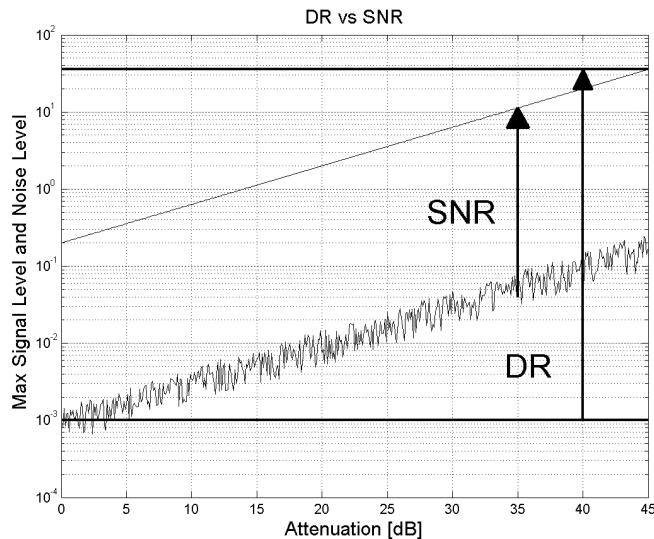


Figure 4.1: Definition of dynamic range and signal to noise ratio

4.3 Low Noise Amplifiers

Low noise amplifier design has been studied for centuries. A single transistor common source amplifier as shown in Figure 4.2a, is most often chosen as the main building block in low power, low noise systems, [9]-[10].

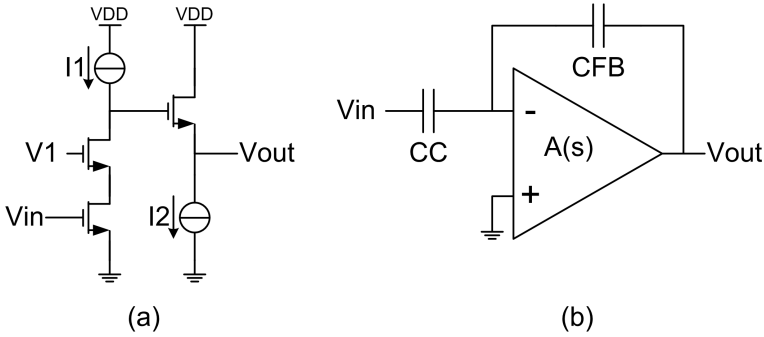


Figure 4.2: (a) Open loop configuration of a common source low noise amplifier (b) closed loop charge sensitive, trans-impedance amplifier

The three basic amplifier configurations common source, common drain and common gate (or their bipolar counterparts) have very close to equal noise properties if we look at the architectures individually. Though, a preamplifier is always connected to a second stage, e.g. a second amplifier, an analog to digital converter (ADC) or some other module. Unless the source has perfect voltage source or current source properties, noise figure will increase more than desired in the second stage if a common drain or common gate amplifier is chosen. The main reason is that these amplifiers do not have power amplification. Common source amplifier is the only configuration that has both voltage gain and current gain. Because of this, the low noise amplifier used in the design presented here is a cascode, common source amplifier having an extra output buffer. Capacitive feedback is used to eliminate the potential extra noise from the feedback components. This architecture is well known and shown in Figure 4.2b. The design is done in accordance with the guidelines given by [9] and [10]. The gain of the amplifier is given by

$$H(s) = \frac{-Z_{FB}(s)}{Z_{CC}(s) + \frac{1}{A(s)} [Z_{FB}(s) + Z_{CC}(s)]} \quad (4.1)$$

In (4.1) $Z_{FB}(s)$ is the impedance of the feedback component, $Z_{CC}(s)$ is the impedance of the input component and $A(s)$ is the open loop gain of the amplifier. Assuming the open loop gain, $A(s)$, of the amplifier to be very high, the closed loop gain of the amplifier is to a first degree independent of frequency and given by $-C_{CC}/C_{FB}$.

4.4 Adding Variable Gain

As emphasized by [10], it is important to not forget that the purpose of an amplifier is to transfer information with as high quality as possible from a source to a load. Nine main amplifier configurations are defined based on the impedance characteristics (all combinations of low, high and well defined input and output impedances). The prototype designed in this paper was constructed using a low input impedance, low output impedance amplifier, i.e. a trans-impedance amplifier. Though, the proposed gain compensation method is compatible with all possible amplifier architectures.

The proposed method is based on the idea of introducing an extra adjustable feedback loop in parallel with a fixed feedback loop. In general, the additional feedback loop must be able to sink and source current or add and subtract voltage at the input of the amplifier in-phase with the sampled output signal. In a trans-impedance configuration, the additional feedback loop must be capable of sinking and sourcing current in-phase with the current flowing into Z_{CC} . By doing this, the amount of current flowing through Z_{FB} would decrease and the output signal amplitude would decrease, effectively reducing gain. Higher gain could be implemented by changing the polarity of the additional feedback signal.

Figure 4.3 shows four possible variable-gain implementations using a trans-impedance amplifier as the core amplifier.

Corresponding architectures can be drawn for the eight other amplifier configurations. In Figure 4.3, $A(s)$ is the open-loop-gain of the amplifier, $B(s)$ is the fixed feedback factor, $V2I$ is a voltage to current converter, $I2V$ is an current to voltage converter, $VCVS$ is an adjustable voltage controlled voltage source, $VCCS$ is an adjustable voltage controlled current source, $CCVS$ is an adjustable current controlled voltage source and $CCCS$ is a current controlled current source. Of the four adjustable sources, the $VCCS$ is to the author's knowledge among the easiest to implement. An adjustable $VCCS$ is by nature a tunable gm-cell. An adjustable $CCCS$ can be implemented using a Gilbert multiplier cell.

4.5 Design of a Variable Gain Amplifier

One way of minimizing overall noise in an amplifier is to use capacitors in the feedback loop. Capacitances are by nature noise-free. High impedances consuming an acceptable amount of die-area can be implemented without

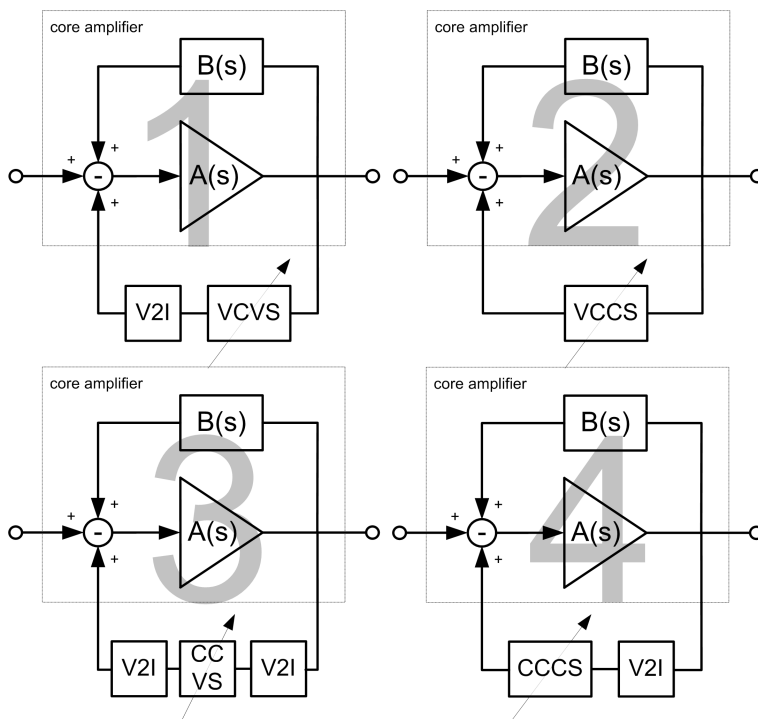


Figure 4.3: Four ways of adding variable gain to trans-impedance amplifiers

deteriorating the noise properties of the overall amplifier. Though, if using capacitors to set the fixed gain when constructing a variable gain amplifier using the above described method, a phase-correction network must be implemented in the voltage controlled current source. A pure voltage controlled current source is equivalent to a resistor and would produce an adjustable high-pass filter. To make a variable gain, charge sensitive amplifier, the *VCCS* must fulfil (4.2).

$$i_{out}(s) = j * f(ctrlsignal) * v_{out}(s) \quad (4.2)$$

In (4.2) $i_{out}(s)$ is the output current of the *VCCS*, j is equal to $\sqrt{-1}$ describing phase, $f(ctrlsignal)$ is a function controlling the transfer function of the *VCCS* and $v_{out}(s)$ is the sampled amplifier output signal. Equation (4.2) has the same format as an adjustable capacitor. This is intuitive. If we look at the signal flow in the amplifier, the output voltage resulting from the current flowing into Z_{FB} will be 90° delayed with respect to the current, i.e. the phase is negative. This voltage is sampled and the current resulting from the sampled voltage needs to be phase shifted the opposite way, given a positive phase, when injected at the amplifier input again to be in-phase with the current flowing here. A circuit diagram of the variable gain trans-impedance amplifier is shown in Figure 4.4.

In the prototype circuit the fixed gain was set to $\sim 26dB$ using $C_C = 10pF$ and $C_{FB} = 0.45pF$. The gain compensation network was constructed using $R_1 = 360k\Omega$, $C_1 = 0.5pF$, $R_2 = 100k\Omega$, $C_{AC} = 4pF$, $C_{COMP} = 0.3pF$ and $R_{COMP} = 100k\Omega$. The effective trans-conductance of the gm-cell and therefore also the overall gain of the circuit is controlled by an external signal, I_{TUNE} . A resistively terminated gm-cell as presented by [12] was used to build the trans-conductor. By changing the bias current of this gm-cell from $0\mu A$ to $100\mu A$ the resulting gm changes from $0\mu S$ to $140\mu S$. An analytical analysis of the overall gain was carried out in Mathcad using Kirchoffs current law at the input node. Due to the length of the expression, only a plot of the result is presented in section 4.6.

4.5.1 Phase Correction

As stated by (4.2), the signal flowing from the output of the amplifier through the adjustable feedback path and back to the input of the amplifiers must have positive phase shift properties. C_{COMP} and R_{COMP} as

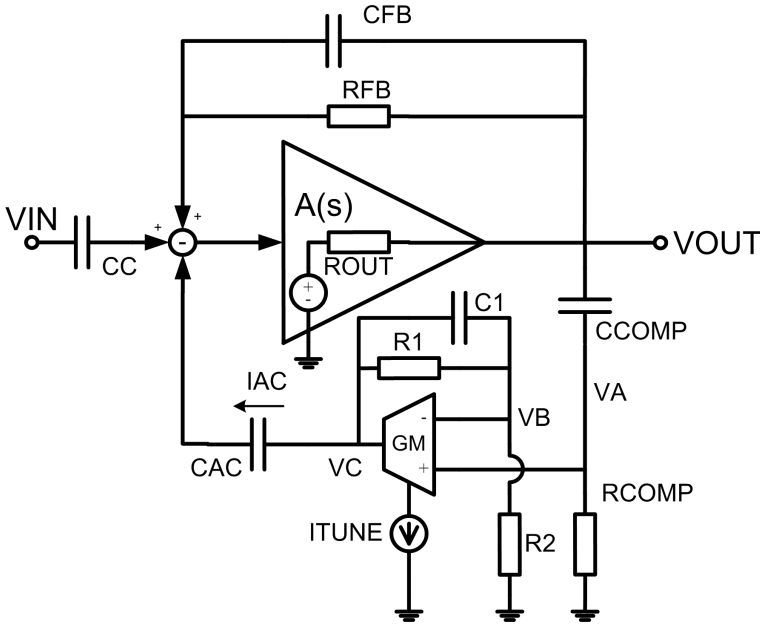


Figure 4.4: Principle sketch of the variable gain trans-impedance amplifier

shown in Figure 4.4 will advance the phase in the correct direction. Though, completely correct phase is only present in the stop-band of this first order RC-filter. Full compensation is therefore impossible using this simple network alone.

To improve the phase characteristics the feedback components R_1 , C_1 and R_2 were added to the gm-cell. The trans-impedance of the adjustable feedback path, $Z(f, GM)$, is found by and routine circuit analysis and is given by (4.3).

$$\begin{aligned}
 a &= GM \cdot R_2 \cdot Z_{AC}(f) [Z_{COMP}(f) + R_{COMP}] \\
 b &= GM \cdot R_2 \cdot Z_{AC}(f) [Z_{COMP}(f) + R_{COMP}] \\
 c &= Z_{COMP}(f) [Z_t(f) + Z_{AC}(f)] \\
 d &= R_{COMP} [Z_t(f) + Z_{AC}(f)] \\
 Z(f, GM) &= \frac{a + b + c + d}{GM \cdot R_{COMP} \cdot Z_t(f)} \quad (4.3)
 \end{aligned}$$

In (4.3) $Z_{AC}(s)$ is the impedance of C_{AC} , $Z_{COMP}(s)$ is the impedance of C_{COMP} and $Z_t(s)$ is the impedance of the parallel connection of C_1 and R_1 .

GM is controlled by an external current, I_{TUNE} . The phase characteristics and the equivalent capacitance are plotted in Figure 4.5 for three different gm-values.

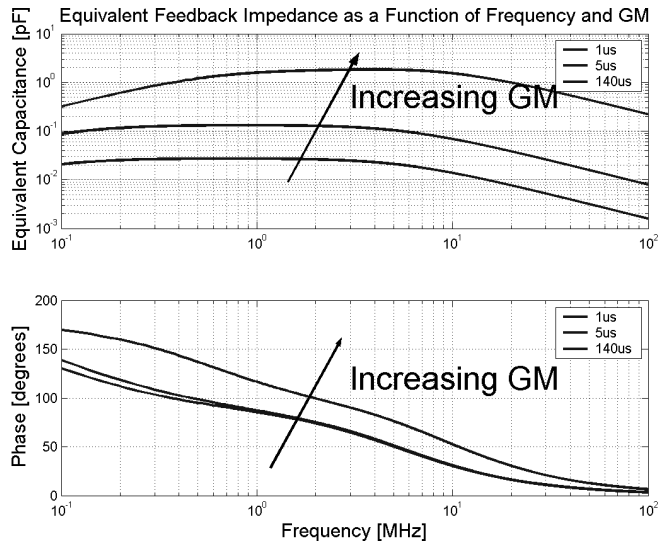


Figure 4.5: Equivalent feedback impedance

A trans-conductance of $140\mu S$ leads to an equivalent capacitance of $\sim 4pF$ which again should give us approximately $12dB$ attenuation.

4.6 Simulations & Measurements

Simulations were carried out using Mathcad for initial calculations and architecture evaluations. Silvaco-SmartSpice2.2.0.R and Cadence PSD14.2 (Capture CIS and PSpice AD) were used during design. A $0.35\mu m$ CMOS process with HRES option from AMS was used to construct the chip. Photography of the prototype-chip is shown in Figure 4.6.

A matrix of 64 variable gain amplifiers using the proposed method was laid out on the prototype chip to evaluate performance. This matrix is highlighted on the plot. The theoretical transfer function is plotted together with chip measurements in Figure 4.7. A simulated transient analysis is shown in Figure 4.8 and corresponding measurements are shown in Figure 4.9.

When the adjustable feedback cell is turned off, spare charge from the cell will be injected at the core amplifier input node disturbing the output

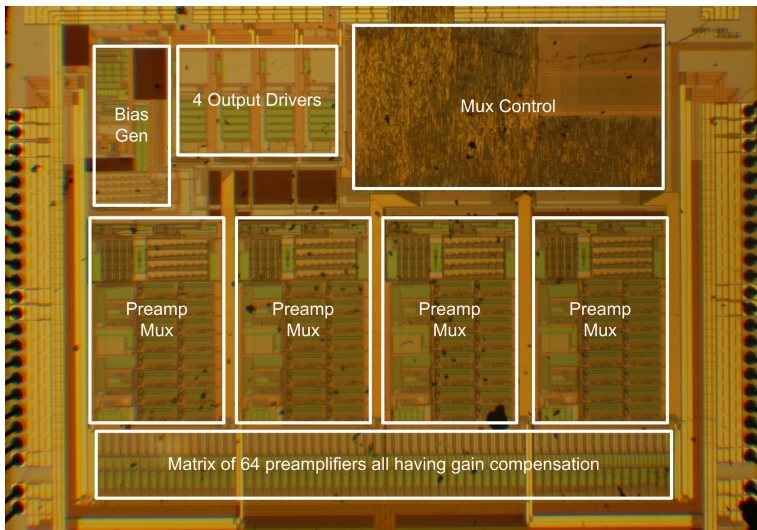


Figure 4.6: Chip photography of the prototype

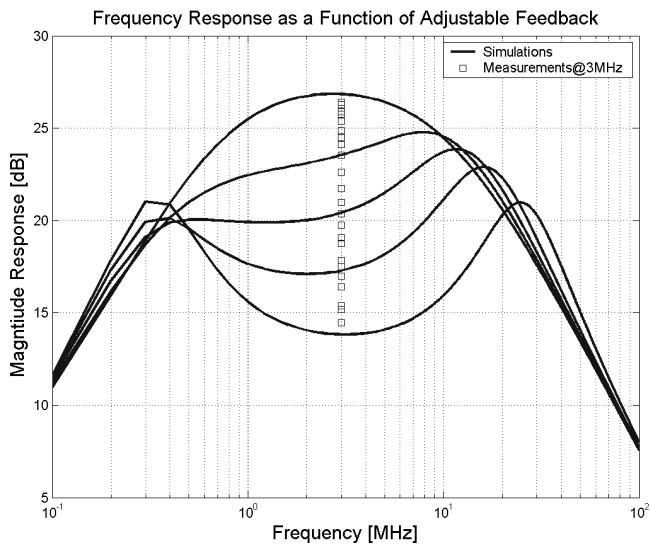


Figure 4.7: Simulated magnitude response of the variable gain amplifier. Measurement at 3MHz is shown

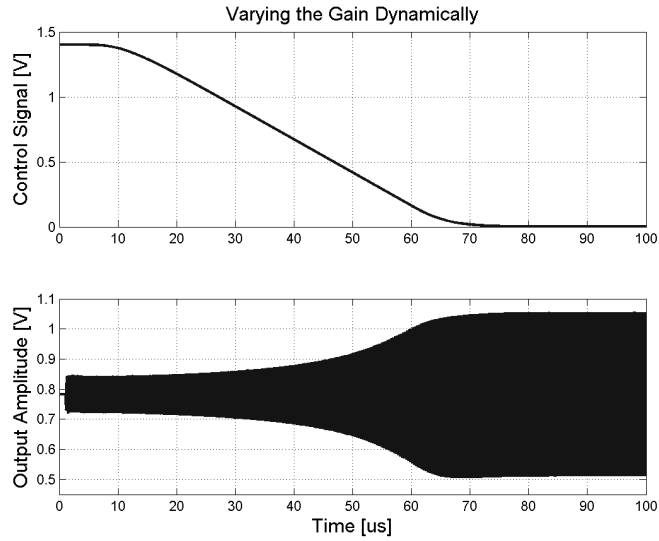


Figure 4.8: Dynamically changing the gain of the trans-impedance amplifier from ~ 13.5 dB to 26 dB over a period of $60 \mu\text{s}$. $V_{IN} = 50 \text{mV}_{PP}$, $f = 3 \text{MHz}$

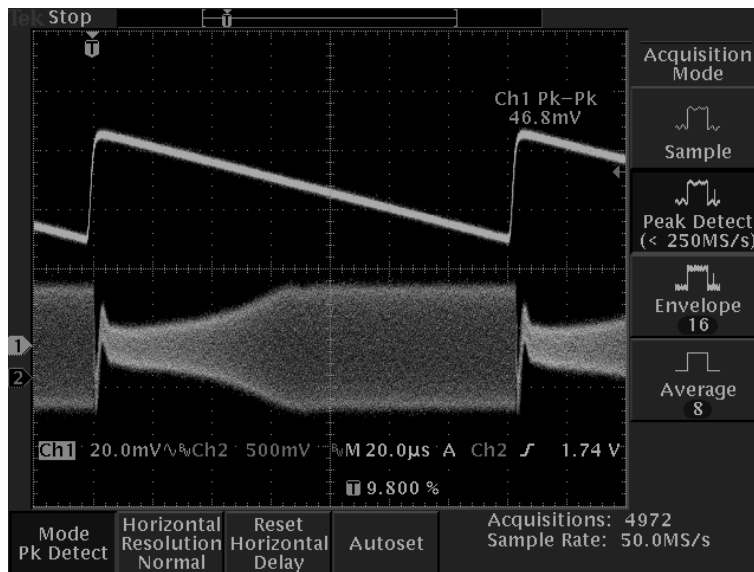


Figure 4.9: Measurement of the dynamic behavior

level. This disturbance can be seen in Figure 4.8 in the time range $60\mu s$ to $70\mu s$. The effect of the disturbance depends heavily on the nature of the control signal. A continuous control signal will minimize the effect of charge injection and move the energy out of band.

4.7 Conclusion

A low-power method adding variable gain to fixed gain amplifiers was presented. The method is compatible to all known amplifier architectures. The main advantage of the method is that no extra power is consumed when gain compensation is close to zero. The performance of the original fixed gain amplifier, here referred to as the core amplifier, is also untouched when gain compensation is zero. This feature is very attractive in applications where gain compensation is necessary for a short duty cycle. A low-noise transimpedance amplifier was designed to prove the concept. Measurements show that a gain compensation of $12dB$ was possible at $3MHz$ for an additional peak power consumption of $251\mu W$ (equivalent to a 46% increase in power consumption).

4.8 Acknowledgment

The authors acknowledge the Norwegian Research Council through the project ASICs for Microsystems (project number 133952/420) for the financial help to write this paper.

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Chapter 5

Paper B

A Dynamic Range Boosted, Low-Power Method Adding Continuous Variable Gain to Amplifiers

Thomas Halvorsrød

Proceedings in

the IEEE Norchip Conference 2005

Oulu, Finland, 21-22 November 2005

5.1 Abstract

A low-power method increasing the adjustable gain range of continuous variable gain amplifiers is presented. The method is an improvement of an architecture using continuous adjustable feedback in parallel with a fixed feedback path. This previous presented architecture suffers from the fact that high attenuation levels require dramatic increase in additional power consumption. The proposed method described in this paper avoids such a severe increase in power at higher attenuation levels. The method is based on the idea of introducing additional feedback in the gain controlling-loop of the already present additional, adjustable feedback path that continuously controls the gain. The nominal gain of $20dB$ at $3MHz$ of the core amplifier is continuously adjusted down to $0dB$. The estimated additional power consumption is $1mW$.

5.2 Introduction

As the dimensions of modern process technologies scales down, the maximum allowable power supply is dramatically reduced. The nominal supply voltage of a typical $0.35\mu m$ process is $3.3V$ while it is $1.0-1.2V$ for $90nm$. Because of this, the design of amplifiers having a certain amount of dynamic range is getting more and more difficult. Some applications, especially those having a fair chance of estimating the signal amplitude, can get around this problem by introducing variable gain. One application where this is possible is medical ultrasound imaging. The method presented here was originally developed for future generation ultrasound imaging, though the method is compatible with all basic amplifier architectures and can be adopted by any application. In medical ultrasound imaging, the signal echoes from the first few centimeters of tissue to be imaged have much higher amplitude than the echoes from deeper depths. Gain compensation as a function of time, TGC, can be implemented with great advantage. This is a well established technique in classical and commercial available ultrasound systems, see e.g. [1].

5.3 Adding Variable Gain to Amplifiers

A method introducing an adjustable active feedback loop in parallel with a passive feedback loop for gain control purposes was presented by the author

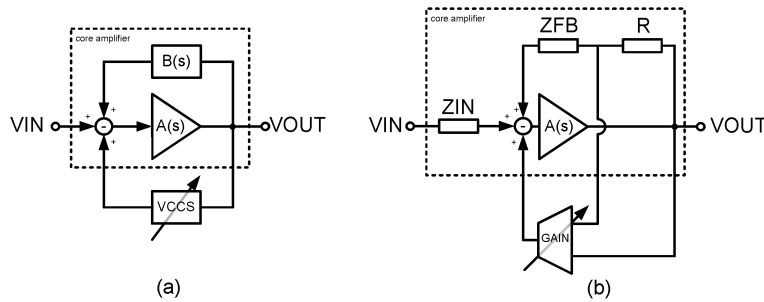


Figure 5.1: (a) Block diagram of the adjustable, additional feedback, continuous variable gain architecture, [2]-[3], (b) Implementation of the additional feedback continuous variable gain architecture

in [2] and [3]. A high level, block diagram description of this architecture is shown for reference in Figure 5.1a. V_{IN} is the input signal, V_{OUT} is the output signal, $A(s)$ is the open-loop gain, $B(s)$ is the fixed feedback factor and $VCCS$ is the adjustable voltage controlled current source. A system-level implementation is shown in Figure 5.1b. Overall gain as a function of adjustable trans-conductance is found by inspection and is given by (5.1).

$$D = \frac{R \cdot GAIN \cdot Z_{IN}(f) + R + Z_{FB}(f) + Z_{IN}(f)}{A(f)}$$

$$H(f, GAIN) = -\frac{Z_{FB}(f) + R}{(Z_{IN}(f) [1 + R \cdot GAIN] + D)} \quad (5.1)$$

In (5.1), $Z_{FB}(f)$ is the fixed feedback impedance, R is a current measuring resistor, $Z_{IN}(f)$ is the voltage to current converting impedance connected to the input node, $GAIN$ is the adjustable trans-conductance of the additional feedback loop and $A(f)$ is the open-loop gain. In Figure 5.1b the method is added to a trans-impedance amplifier to prove the concept. Though, the proposed architecture is compatible with any amplifier configuration (all combinations of high, low and controlled input and output impedance as described in [4]).

The architecture in Figure 5.1 suffers from the fact that a small increase in attenuation requires more and more current as the absolute amount of attenuation increases. The main reason for this is that the adjustable feedback loop measures the signal in the fixed feedback loop and multiplies this with a constant to control the current in the adjustable feedback loop. As

the attenuation increases, the current in the fixed path decreases requiring an even higher multiplication constant to decrease the overall gain further.

Overall gain for this architecture as a function of trans-conductance is plotted using circles in Figure 5.2.

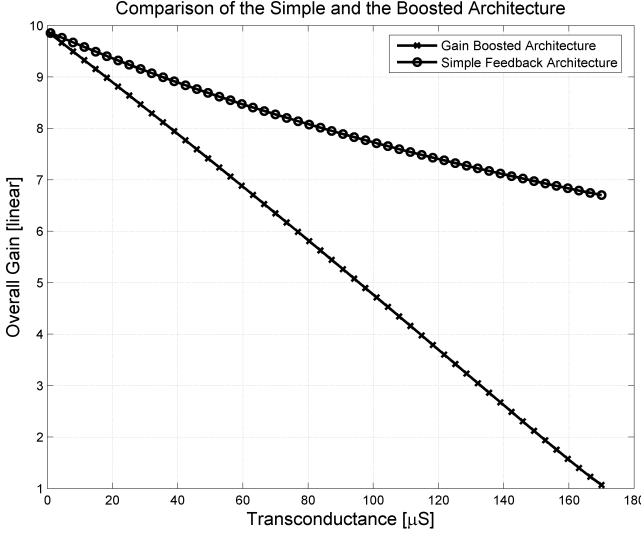


Figure 5.2: Gain comparison of the simple additional adjustable feedback architecture and the gain boosting architecture

In the following calculations, Z_{IN} is chosen equal to $5k\Omega$, Z_{FB} is chosen equal to $50k\Omega$ and R is chosen equal to $3k\Omega$. The open-loop gain was given one dominant pole at $1MHz$ and a DC gain of $46dB$. This paper proposes a way to avoid the $f(x) = 1/x$ shape of overall gain as a function of current in the additional feedback loop. The architecture is shown in Figure 5.3.

Overall gain is found by first using Kirchoffs current law at the input node, see equation (5.2) and (5.3).

$$E = \left[1 + \frac{R \cdot GM_F \cdot R_{SUM} \cdot GAIN}{(R \cdot GM_F \cdot R_{SUM} \cdot GAIN - 1)} \right] \quad (5.2)$$

$$\frac{(V_{IN} - \frac{V_{OUT}}{-A(s)})}{Z_{IN}} = \frac{(\frac{V_{OUT}}{-A(s)} - V_{OUT})}{R + Z_{FB}} \cdot E \quad (5.3)$$

From (5.2) and (5.3) we solve for V_{OUT}/V_{IN} to find the transfer-function,

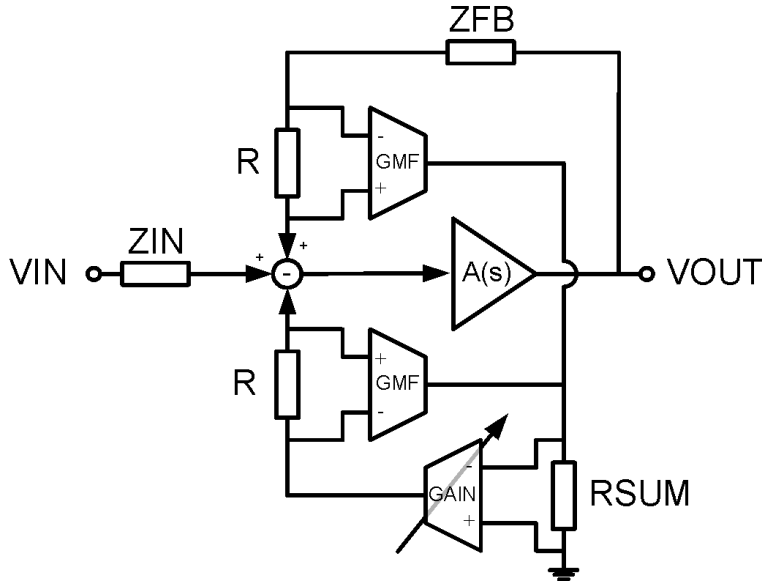


Figure 5.3: Gain Boosted, dual feedback continuous variable gain amplifier architecture

see equation (5.4).

$$D = \frac{Z_{IN} + Z_{FB} + R - GM_F \cdot R_{SUM} \cdot GAIN \cdot R [Z_{FB} + R]}{A(f)}$$

$$H(f, GAIN) = -\frac{(Z_{FB} + R - GM_F \cdot R_{SUM} \cdot GAIN \cdot R [Z_{FB} + R])}{(Z_{IN} + D)} \quad (5.4)$$

By comparing (5.1) and (5.4) we see that overall gain is proportional to $-1/GAIN$ and $-GAIN$ respectively assuming a very high open-loop gain. The circuit in Figure 5.3 is based on the idea of re-using the signal flowing in the adjustable feedback path for gain control purposes. In the original architecture as presented in [3], the signal in the adjustable feedback path increased as a function of the signal in the fixed feedback path only. In the modified architecture, the amount of signal in the adjustable feedback path increases as a function of signal in the fixed feedback path and as a function of increasing signal in the adjustable feedback path. Overall gain for this architecture as a function of trans-conductance is plotted with crosses in Figure 5.2. Components common to both architectures are assigned equal values during comparison. The fixed trans-conductance, GM_F , in the new

architecture was set to $30\mu S$ and R_{SUM} was chosen equal to $60k\Omega$.

5.4 Stability

An analytical expression for the loop-gain of the architecture shown in Figure 5.3 was developed in accordance to the guidelines given by [5]. The result is shown in (5.5).

$$\begin{aligned}
 D &= R^2 \cdot GM_F(f) \cdot R_{SUM} \cdot GAIN(f) \\
 E &= Z_{FB} \cdot R \cdot GM_F(f) \cdot R_{SUM} \cdot GAIN(f) \\
 A\beta &= \frac{Z_{IN}A(f)}{(-Z_{IN} - Z_{FB} - R + D + E)} \tag{5.5}
 \end{aligned}$$

All trans-conductors were modelled to have one dominant pole at $100MHz$ as described in [6]. A plot of the loop-gain at different gain compensations is shown in Figure 5.4.

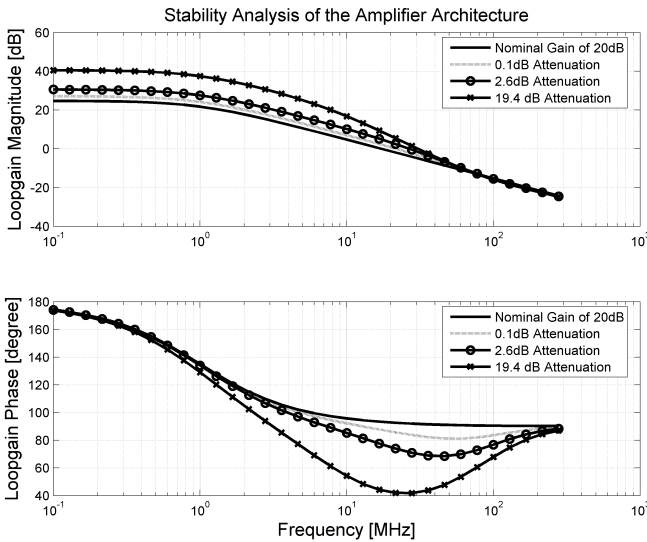


Figure 5.4: Loop-gain analysis of the proposed architecture

The phase margin decreases from 90 degrees for no gain compensation to approximately 42 degrees for $19.4dB$ attenuation. SPICE simulations were carried out to verify the analytical calculations. A close to exact match was found when using a circuit built from ideal components.

5.5 Power Consumption

The proposed architecture uses three gm-cells compared to one in the architecture proposed in 3. Two of these cells have fixed trans-conductance and therefore a fixed power consumption. Using the well known Krummenacher gm-architecture as described by [7], having W/L equal to 10, a transistor gain factor of $170\mu A/V^2$ and a power supply voltage of $3.3V$, an estimate of the additional power consumption as a function of gain was carried out. The result is plotted in Figure 5.5.

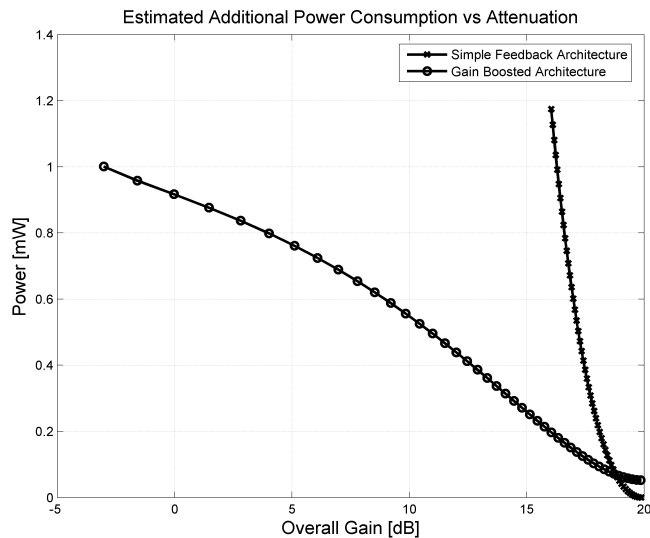


Figure 5.5: Comparison of additional power consumption due to the extra gain compensation circuits

The plot shows that the proposed architecture has additional fixed power consumption. For small gain adjustments this leads to higher overall power consumption than for the architecture presented in [3]. Though, as the gain compensation in the proposed circuit is increased, the overall power consumption for a given absolute gain is much better. If the feedback factor is increased too much, overall gain starts to increase again.

5.6 Simulations

Transient simulations were carried out to prove the concept. A 3MHz , 200mV_{pp} sine signal was connected to input of the amplifier. A trans-impedance amplifier as described above was used for the core amplifier. A voltage was used to control the trans-conductance of the variable trans-conductor. The trans-conductance was changed continuously from $180\mu\text{S}$ to $\sim 0\mu\text{S}$ over a time period of $60\mu\text{s}$. The control signal and the corresponding output signal are shown in Figure 5.6.

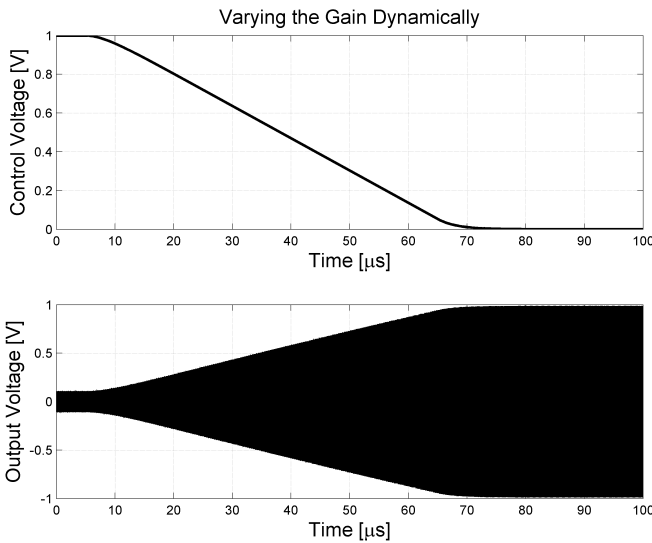


Figure 5.6: Dynamically changing the gain of the trans-impedance amplifier from 0dB to 20dB over a period of 60ms. $V_{IN} = 200\text{mV}_{pp}$, $f = 3\text{MHz}$.

The output amplitude changes from 212mV_{pp} at a stable control voltage of 1V , measured at $0.4\mu\text{s}$, to 1.96V_{pp} at stable control voltage of 0V , measured at $83\mu\text{s}$. This is equivalent to an overall gain of 0.6dB and 19.9dB respectively. The frequency response at six different gain settings is shown in Figure 5.7.

The peak in the response at higher frequencies is due to the limited bandwidth of the trans-conductors. In the intended application, i.e. medical ultrasound imaging systems, this is not expected to be a problem because the bandwidth of the information-carrying signal is relatively narrow. In applications having a more broadband signal, it might be necessary to move

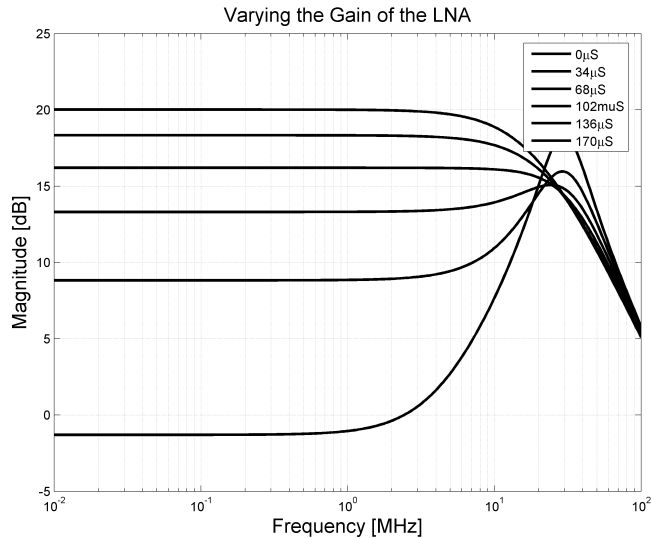


Figure 5.7: Frequency response at six different control signals. Overall gain decreases as the trans-conductance increases.

the dominant pole of the trans-conductors further up in frequency to make sure this peak does not cause a problem.

5.7 Conclusion

A very power effective method increasing the dynamic range of continuous variable gain amplifiers has been proposed. The method is compatible with all basic amplifiers configurations and can be used with great advantage in systems requiring continuous, variable gain control. The power consumption increases when the compensation level increases. This is especially beneficial in systems where gain compensation is only necessary for a fraction of the duty cycle. This is the case for medical ultrasound imaging systems.

5.8 References

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Chapter 6

Paper C

Continuous Variable Gain Amplifiers for Medical Ultrasound Applications

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* Note: Intermediate results on input- and output impedance calculations using Blackman's impedance formula can be found in Appendix A. A comment to the signal polarities at several critical nodes in the proposed circuit is also added.

6.1 Abstract

There is a strong need for gain compensation techniques in the analog front-end of medical ultrasound imaging systems. A technique adding continuous, gain adjustment to low-noise, fixed gain amplifiers is proposed. A design carried out in a $0.35\mu m$ SOI process is presented. The technique is based on the idea of adding positive feedback to an active feedback-network. The active feedback network is adjustable and controls overall gain in the LNA. The proposed technique demonstrates dynamic range adjustments of $15dB$ at the expense of $1.1mW$ additional power consumption. To cover this gain range, trans-conductance in the active feedback path must be continuously adjusted from $30\mu S$ to $0\mu S$. Due to the positive feedback, this range is reduced $10dB$ when compared to earlier publications. The presented circuit has maximum gain of $24dB$. This gain is continuously adjusted down to $9dB$. Assuming a bandwidth of $20MHz$, the dynamic range of the LNA is $57dB$ at a power consumption of $1.1mW$. During gain compensation, power consumption is proportional to the amount of attenuation. This property is especially attractive in medical ultrasound imaging systems where gain adjustment is only necessary for a fraction of the receive-period. Overall power consumption is therefore minimized. The implemented LNA occupies $220\mu m \times 220\mu m$ effective silicon area.

Index Terms-Gain compensation, gain control, low noise amplifier, variable-gain amplifiers

6.2 Introduction

Medical ultrasound imaging is slowly moving from 2D imaging to 3D/4D imaging. Several real-time systems are commercially available in the market. Two examples are described in the whitepapers [1] and [2]. Common for these systems is that the number of transducer-elements is much higher than the number typically found in classical 2D imaging systems. The main reason is that the elements are arranged in a matrix and not only in a single row. Theoretically this squares the number of elements. Figure 6.1 shows a classical ultrasound probe with one row of transducer elements. Beam-steering is only possible in a fixed plane, here indicated by the fan in front of the probe. In Figure 6.2 the row of transducer elements have been diced and transformed into an array of elements. This enables beam-steering in space as indicated by the two perpendicular scan-planes. To utilize the

number of elements to its full extent, it is desirable to dedicate one amplifier to each element before beam-forming is performed. This is necessary to avoid serious deterioration in noise figure after transporting the signal over a cable from the transducer element to the main ultrasound system. A majority of the commercially available ultrasound systems have cables longer than two meter. The amount of power available to do amplification in the probe-handle is very limited. Too high power dissipation necessitates an active cooling system like described by Fray in [1]. The system presented by Chen, Panda and Savord in [2] does not utilize active cooling. Fundamental ultrasonic theory indicates that that the signal is attenuated approximately $1dB/cm/MHz$, [3]. Medical ultrasound imaging systems typically use frequencies in the $1MHz$ to $30MHz$ range to achieve a decent resolution and penetration. Assuming a $2MHz$ signal and an imaging depth of $10cm$, the signal experience approximately $40dB$ round-trip attenuation. Assuming that $60dB$ instantaneous dynamic range is necessary to get good contrast in the image, the amplifier needs to handle $100dB$ dynamic range to do decent imaging, also see [4]. It is unrealistic to integrate one fixed-gain amplifier for each transducer element in a matrix probe with the low power budget and such a high dynamic range requirement. An amplifier with an output swing of $1V_{pp}$ would require a noise level of $3.5\mu V_{rms}$ at the output. Due to the fact that attenuation in tissue is known, it is acceptable to adjust gain as a function of time. An adjustment method like this is often referred to as time gain compensation, TGC, [5]. To avoid noise and glitches in the image, it is believed that switching of feedback element is suboptimal. This paper proposes an effective way of adding continuous-time TGC to fixed-gain, low-noise, low-power analog amplifiers.

The paper is divided into four main sections. The first section describes fundamental LNA design theory. This section also introduces the gain-control technique used in the test-chip and highlights and describes the solutions chosen for the presented circuit. Section two presents the laboratory setup and the measured performance of the design. The final section gives a discussion of the findings and draws the conclusion.

6.3 Architecture

This section gives a thorough description of the different choices made during design of the continuous, variable gain amplifier. The fundamental the-

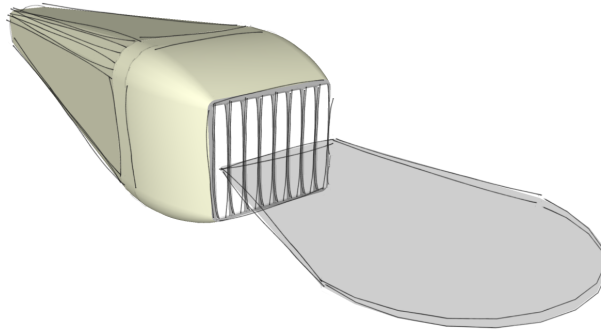


Figure 6.1: Medical ultrasound probes, [6]. Classical probe with one row of elements

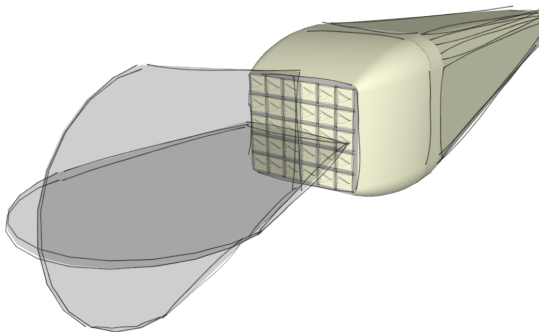


Figure 6.2: Medical ultrasound probe: Matrix probe capable of doing 4D imaging. Notice how the long rectangular elements in the upper part are divided into small squares. Because of this, beams can be to be steered in space

ory that was needed to complete the design is also presented.

6.3.1 Designing the Core Amplifier

Most literature focusing on high performance, analog circuit design recommends using the common source or common emitter circuit as the main building block for low-noise amplifiers, see [7]-[9]. This is also demonstrated thoroughly by Nordholt in [10]. Based upon a systematic study of feedback theory, Nordholt develops a very interesting approach to be used in the selection of input-stages. The conclusion is that the three commonly known single stage circuits, the common source, the common gate and the common drain have more or less the same noise properties. The main difference and performance reduction is first visible when connecting to a second stage. Because the common source stage has the largest value for all transfer parameters, the contribution from the second stage is the smallest. The transfer parameters are largest because there is no local feedback in the controlled source in the transistor. This is well known but often not elaborated as well-founded and systematic as by Nordholt in [10]. Transfer parameters is a term used collectively to describe voltage gain, trans-admittance, trans-impedance and current gain in electrical circuits. The transfer parameters, μ , γ , ζ , and α are defined as

$$\mu = \frac{1}{A} = \left(\frac{U_O}{U_I} \right)_{I_O=0}, \gamma = \frac{1}{B} = \left(\frac{I_O}{U_I} \right)_{U_O=0} \quad (6.1)$$

$$\zeta = \frac{1}{C} = \left(\frac{U_O}{I_I} \right)_{I_O=0}, \alpha = \frac{1}{D} = \left(\frac{I_O}{I_I} \right)_{U_O=0} \quad (6.2)$$

In (6.1) and (6.2) μ is voltage gain, γ is trans-admittance, ζ is trans-impedance and α is current gain. U_O and I_O are output current and output voltage respectively and U_I and I_I are input voltage and input current respectively. The inversed values, A , B , C and D are referred to as the transmission parameters. A two-port representation using transmission parameters can be used to describe the single transistor or an LNA. This is shown in Figure 6.3.

$$\begin{bmatrix} U_i \\ I_i \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} U_o \\ I_o \end{bmatrix} \rightarrow \begin{aligned} U_i &= A \cdot U_o + B \cdot I_o \\ I_i &= C \cdot U_o + D \cdot I_o \end{aligned} \quad (6.3)$$

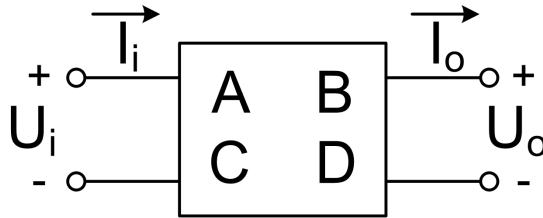


Figure 6.3: Two-port description of the transistor or an LNA using transmission-parameters

To maximize the transfer parameters when designing a low noise amplifier, it is also recommended to implement a cascode transistor together with the common source stage. Nordholt's model connected to a second stage is shown in Figure 6.4. The noise in the second stage is referred back to the input by dividing the voltage noise source in stage two by both the voltage gain and the trans-admittance and the current noise source in stage two by both the current gain and the trans-impedance.

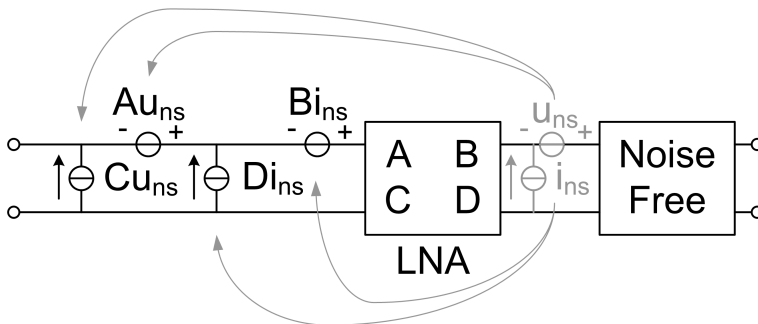


Figure 6.4: Noise contribution from second stage

Total input referred noise from the second stage assuming noise-free source impedance, Z_S , and a noise free LNA is then given by (6.4) below. From (6.4) it is clear that noise-contribution from the second stage is minimized by maximizing all transfer-parameters. The transfer-parameters of a single transistor are maximized by avoiding local feedback. In the common source and common emitter stage, there is no feedback-connection from output of internally controlled source to the input. These stages therefore potentially have the best low-noise performance. Common drain and com-

mon gate circuits have local feedback leading to a reduction of the transfer parameters.

$$u_{eq} = \sqrt{u_{n.s}^2 \left(\frac{1}{\mu^2} + \frac{Z_S^2}{\zeta^2} \right) + i_{n.s}^2 \left(\frac{1}{\gamma^2} + \frac{Z_S^2}{\alpha^2} \right)} \quad (6.4)$$

The implemented core amplifier is shown in Figure 21.

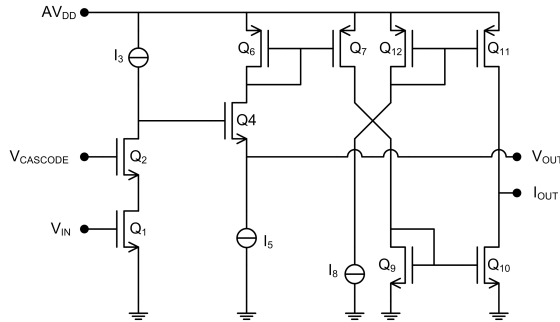


Figure 6.5: Low-noise amplifier core circuit

Bias current in the input stage was set to $100\mu A$. Bias current in the output buffer was set to $25\mu A$. The trans-conductance of the input transistor is designed to be in the range of $3\text{-}4mS$. The cascode-transistor was chosen to have same dimensions as the input stage leading to similar values in trans-conductance. The current source, I_3 , feeding the bias current into the input stage was design to have output impedance in the $M\Omega$ -range. This is achieved by using a very large and long transistor. Impedance in the node connected to both drain of the cascode and drain of the current mirror is therefore dominated by the input capacitance of the next stage, Q_4 . The second stage is included to lower the DC level of the output. Alternatively, a folded cascade could have been used. Lowering of the output DC level is necessary because the output node is, for biasing purposes, DC-connected to the input stage using a high-value resistor. This can be seen in the small-signal model in Figure 22 where also the feedback network is included. The current-copy-output shown in Figure 21 contains an inverted copy of the output signal transferred to the current domain. This signal is used during gain adjustment and will be explained in detail later. For proof of concept the current flowing in these branches were also set to $25\mu A$. With a $3.3V$ supply total power consumption in the core amplifier is $(100\mu A + 4 * 25\mu A)^*$

$3.3V=660\mu W$. A lower supply voltage could have been used at the penalty of reduced dynamic range and higher harmonic distortion.

A small-signal model of the core amplifier was developed to better understand the different contributions to the open-loop gain and also to derive equations for the noise transfer-functions from the different devices to the output node. This is essential to be able to minimize total output noise and optimize noise figure. The model used is shown in Figure 21. The noise-sources i_{n1} , i_{n2} , i_{n3} and i_{n4} represent noise in the input transistor, the cascode transistor, the current mirror and the feedback network respectively.

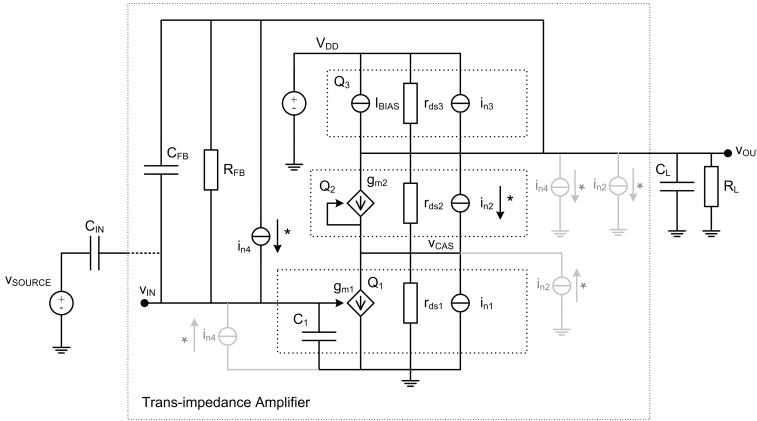


Figure 6.6: Small-signal-model for the low noise amplifier core

By using Kirchhoff's first rule at the V_{OUT} -node and the V_{CAS} -node we find an expression for the open-loop voltage gain in the telescopic cascode-amplifier. To emphasize the open-loop behaviour of the circuit, V_{SOURCE} , C_{IN} , R_{FB} and C_{FB} are not included in this analysis. Open-loop gain is given by (6.5).

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_L \cdot g_{m1} \cdot r_{ds1} (g_{m2} \cdot r_{ds2} + 1)}{Z_L + r_{ds1} + r_{ds2} + g_{m1} r_{ds1} r_{ds2}} \quad (6.5)$$

Z_L is the parallel connection of the current mirror output impedance, r_{ds3} , and the input impedance of the next stage, $R_L \parallel C_L$. The parameters g_{m1} , g_{m2} , r_{ds1} and r_{ds2} are the trans-conductance and the output impedance of the input stage, Q_1 , and the cascode-transistor, Q_2 , respectively.

Inserting $g_{m1} = g_{m2} = 4mS$, $r_{ds1} = r_{ds2} = 200k\Omega$ and $Z_L = 3M\Omega \parallel 25fF$ in (3), open-loop DC gain is calculated to be $75dB$. Simulation of the real implementation indicates open-loop DC gain in the $73dB$ range and a cut-

off frequency of $71kHz$. A simple, one-pole model of the core amplifier is then given by

$$A_{LNA}(f) = \frac{OLG}{1 + \frac{j \cdot 2 \cdot \pi \cdot f}{2 \cdot \pi \cdot f_{3dB}}} \quad (6.6)$$

In equation (6.6) OLG is the open-loop gain and f_{3dB} is the $3dB$ cut-off frequency. Design of the test-circuit has been carried out using the Cadence Virtuoso Schematic Editor, the Cadence Virtuoso Layout Editor and ELDO as the main simulator. For sake of experiment, the low-cost simulator Simetrix from Simetrix Technologies Ltd was used for verification and documentation, [11].

6.3.2 Closing the Feedback-loop

To get the desired input- and output impedance levels, correct biasing levels at input and output, accurate gain and independent performance over process, we put the module into a closed loop-configuration. This is done using the passive impedance elements R_{FB} and C_{FB} , see Figure 22. We will see later how this also enables the continuous gain adjustment methodology proposed by the author in [12], [13] and [14]. A high value resistance is used in the feedback loop to close the loop in DC and to bias the input and output node. Minimum noise contribution from this component is achieved by using as high resistance as possible. This is also demonstrated in the noise analysis section below. Fixed gain in the amplifier is controlled using the inherently noiseless capacitor. Closed-loop voltage gain assuming a voltage to current converting impedance connected between signal-source and amplifier input, is found using mesh analysis and is given by (6.7).

$$H_Z(f) = \frac{Z_{OUT}(f) - Z_{FB}(f) \cdot A_{LNA}(f)}{DN} \quad (6.7)$$

In (6.7), DN is given by

$$\begin{aligned} & Z_{FB}(f) + Z_{CIN}(f) + Z_{OUT}(f) + \frac{Z_{CIN}(f) \cdot Z_{FB}(f)}{Z_{IN}(f)} \\ & + \frac{Z_{CIN}(f) \cdot Z_{OUT}(f)}{Z_{IN}(f)} + Z_{CIN}(f) \cdot A_{LNA}(f) \end{aligned}$$

Assuming high input impedance, $Z_{IN}(f)$, and low output impedance, $Z_{OUT}(f)$, (6.7) simplifies to (6.8).

$$\tilde{H}_Z(f) = \lim_{\substack{Z_{OUT} \rightarrow 0 \\ Z_{IN} \rightarrow \infty}} H_Z(f) = \frac{-Z_{FB}(f)}{Z_{CIN}(f) + \frac{Z_{FB}(f) + Z_{CIN}(f)}{A_{LNA}(f)}} \quad (6.8)$$

In (6.7) and (6.8) $Z_{OUT}(f)$ is the output impedance of the amplifier, $Z_{FB}(f)$ is the total impedance in the feedback network, $A_{LNA}(f)$ is the open-loop-gain, $Z_{CIN}(f)$ is the impedance in the element connected from source to amplifier input and $Z_{IN}(f)$ is the impedance looking into the negative input-terminal of the amplifier. Assuming low output impedance, very high intrinsic input impedance and high open-loop-gain, voltage gain is simply given by the negative ratio $Z_{FB}(f)$ to Z_{CIN} , see (6.8).

It is important to keep in mind that even if the feedback capacitor by itself is noiseless, its presence in the feedback loop deteriorates noise performance of the core amplifier. This is seen in Figure 6.7. Before closing the loop, the amplifier (or single transistor) has two equivalent noise sources connected to the input, e_n and i_n . This is shown in (i) in the upper left part of Figure 6.7. When closing the feedback loop with impedance $Z_{FB}(f)$, the two noise-source must be moved closer to V_{IN} to represent equivalent input noise sources. The current source can be moved directly without changing the operation of the circuit. As the voltage source is moved into the node where the loop is closed, we utilize the Blakeslay transformation and split the source in two to keep correct electrical behavior of the circuit. One part is moved directly to the signal source and the other one is moved into the feedback path in the direction of the amplifier output. This is shown in (ii) in the upper right part of Figure 6.7. The voltage source is next transformed into its Norton equivalent. This is shown in (iii) the middle left part of Figure 6.7. The new current source has the value e_n/Z_{FB} . This source is next split in two as shown in (iv) in the middle, right part of Figure 6.7. One part sources current from the V_{OUT} node to ground and the other sources current from ground to the negative input node of the amplifier. These two sources are equivalent to one current sources connected between the input and output of the amplifier. Next, we need to refer all sources to the input. The current source at the output of the amplifier is referred to the input by dividing by the current gain, α , and trans-admittance, γ . The single source at the output results in two contribution on the input side. This is shown

in (v) in Figure 6.7

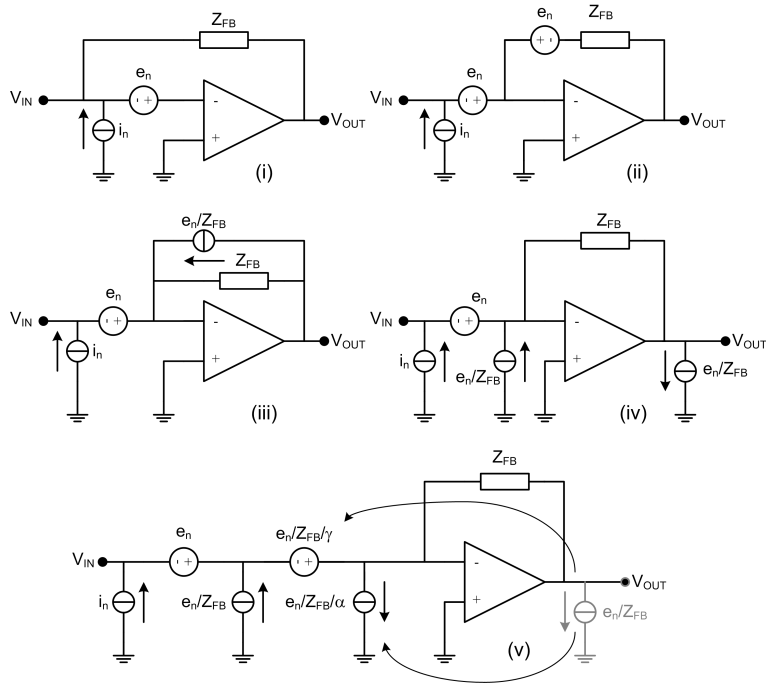


Figure 6.7: Inherent noise deterioration due to presence of feedback

We see that even the introduction of noiseless feedback to the open loop amplifier affects the input equivalent noise sources. Noise from the feedback impedance translates to the input in the exact same way. To minimize the additional noise from the resistive part of the feedback component, resistance must be maximized because it ends up at the input as one voltage noise source and one current noise source both inverse proportional to the resistor values.

Input impedance and output impedance are also easily found from fundamental mesh or nodal analysis, [15] and [16]. The expressions are derived here to better identify a way to introduce gain control to the fixed gain amplifier. The results are shown in (6.9), (6.10), (6.11) and (6.12).

$$Z_{IN} = \frac{Z_i \cdot (Z_{FB} + Z_{OUT})}{Z_i + Z_{FB} + Z_{OUT} + A(f) \cdot Z_i} \tag{6.9}$$

$$Z_{IN}|_{Z_i \rightarrow \infty} = \frac{Z_{FB} + Z_{OUT}}{1 + A(f)} \tag{6.10}$$

$$Z_{OUT} = \frac{Z_{OUT} \cdot (Z_{FB} + Z_i)}{Z_{OUT} + Z_{FB} + Z_i + A(f) \cdot Z_i} \quad (6.11)$$

$$Z_{OUT}|_{Z_i \rightarrow \infty} = \frac{Z_{OUT}}{1 + A(f)} \quad (6.12)$$

In the circuit-implementation the reduction in output impedance is somewhat limited because the assumption that Z_i goes to infinity does not hold. Z_i is the impedance of the parallel connection of the amplifier intrinsic input-impedance (the impedance seen looking into the gate of the main stage) and the source-impedance. Source impedance will in a typical application be several kilo-ohms. Because of this a separate, inherently low-output impedance common drain stage was added at the output of the core amplifier, see Q_4 and I_5 in Figure 21.

Noise Transfer

Assuming that averaging is not possible, total output- or input referred noise in an amplifier dictates the minimum useful signal-level. Any signal with amplitude below noise level is not detectable. Noise level is given by the selected circuit device, architecture and biasing condition. For minimum power consumption, a single-device solution yields the best noise-performance. The dominating part of the noise must come from the input stage. This noise source is next the one to be minimized. Noise contributors in the architecture shown in Figure 21 and Figure 22 are mainly transistor Q_1 , Q_2 , I_3/Q_3 and Z_{FB} . When representing noise in each transistor by a current source between source and drain, the trans-resistance to the output node from each source is found by mesh and nodal analysis. The noise sources can be found in Figure 22 as i_{n1} , i_{n2} , i_{n3} and i_{n4} . The analytical transfer-function of the noise sources to the output node is listed below. To simplify the expressions, r_{ds1} , r_{ds2} and r_{ds3} are all assumed very high. Gate of the input amplifier is terminated to ground through impedance $Z_{IN}(f)$. To get low noise and high gain, trans-conductance in this transistor must be high. High trans-conductance at low current results in a large device. The parasitic input impedance of the transistor becomes significant and is therefore included in the calculations below. The parasitic capacitance is connected in parallel with $Z_{IN}(f)$. Solving the set of equations resulting from using Kirchhoff's current law at the input node, the output node and the V_{CAS} node, we find a common trans-conductance for all the noise

sources to the output, Y_{NOISE} , see (6.13).

$$Y_{NOISE} \approx \frac{\frac{Z_{IN}(f)}{Z_{FB}(f)+Z_{IN}(f)} \cdot (1 - g_{m1} \cdot Z_{FB}(f)) - 1}{Z_{FB}(f)}} - \frac{1}{Z_L(f)} \quad (6.13)$$

Total output noise at the output is given by the quadratic sum of the contributions from the single elements, (6.14).

$$v_{ONoise}(f) = \frac{\sqrt{(i_{ex1})^2 + (i_{ex2})^2 + (i_{ex3})^2 + (i_{ex4})^2}}{Y_{NOISE}} \quad (6.14)$$

The contributions to the total noise at the output from each single noise source is given by (6.15), (6.16), (6.17) and (6.18).

$$i_{ex1} = \pm i_{n1} \left(\frac{1}{r_{ds2} g_{m2}} + 1 \right) \quad (6.15)$$

$$i_{ex2} = \pm i_{n2} \frac{1}{r_{ds1} g_{m2}} \quad (6.16)$$

$$i_{ex3} = \pm i_{n3} \quad (6.17)$$

$$i_{ex4} = \pm i_{n4} \left(\frac{Z_{IN}(f)}{Z_{FB}(f) + Z_{IN}(f)} (g_{m1} Z_{FB}(f) - 1) + 1 \right) \quad (6.18)$$

Noise from the input stage Q_1 and the current source represented by Q_3 propagate to the output with a trans-admittance equal to Y_{NOISE} . Noise from the cascode transistor, Q_2 , is reduced by $\sim r_{ds1} * g_{m2}$ before multiplied by the same factor. Noise from the cascode-transistor is therefore heavily attenuated when referred to the output. The contribution is insignificant. Noise from the feedback-network is minimized using a high-value resistor. Using a resistor to control gain is therefore a suboptimal solution because gain dictates the use of very low impedance. Using the inherently noise-less capacitor to control gain is therefore much better.

Total noise in a MOSFET transistor is given by the expression below, see [17].

$$i_n^2(f) = 4 \cdot k \cdot T \cdot \frac{2}{3} \cdot g_m + \frac{K \cdot g_m^2}{W \cdot L \cdot C_{OX} \cdot f} \quad (6.19)$$

In (6.19) k is the Boltzmann constant, T is absolute temperature, g_m is the trans-conductance of the transistor, K is a process dependant constant, W and L are the width and the length of the transistor, C_{OX} is the gate

capacitance per unit area and f is the frequency. The first term in (6.19) represents the shot noise from the channel and the second term represents the flicker noise. Figure 6.8, Figure 6.9 and Figure 6.10 compare simulated noise in the complete transistor-level implementation with hand-calculated output noise using equation (6.19) and (6.14). The three figures plot individual noise contributions and output noise with input shorted to ground, input left open and input terminated to ground with $10pF$ respectively.

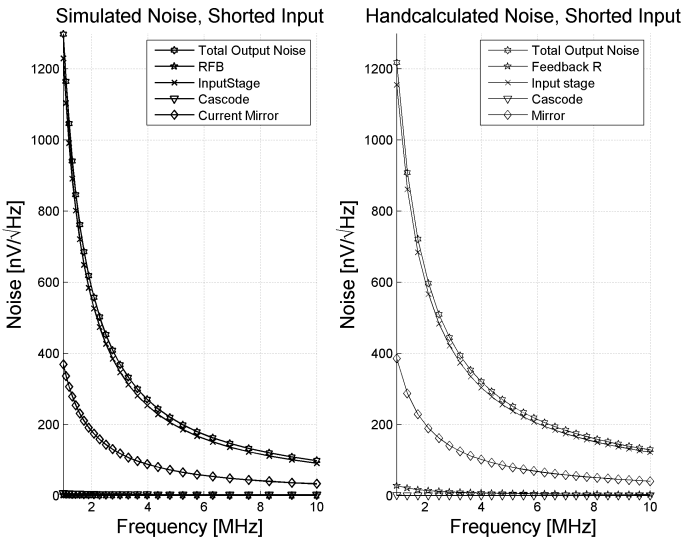


Figure 6.8: Noise contributors in LNA core. Input shorted to ground ($C_{IN}=1F$)

If we assume a bandwidth of $20MHz$ and maximum input signal of $50mV_{pp}$, the noise levels above translates to a dynamic range at the output of approximately $57dB$. This signal level results in second harmonic distortion at the output of approximately $-30dB$ relative to the fundamental component. Power consumption is $125\mu A * 3.3V = 412\mu W$ excluding the power consumption from the extra LNA outputs and from the bias circuit.

The compact, low-power, low noise amplifier described above is only useful in medical ultrasound imaging applications if continuous, adjustable gain control is added to the circuit. We want to add TGC without touching the carefully achieved performance parameters of the LNA. Equation (6.8) indicates that gain is mainly controlled by the feedback-network. Modification of the open-loop gain would not be an effective way to adjust the

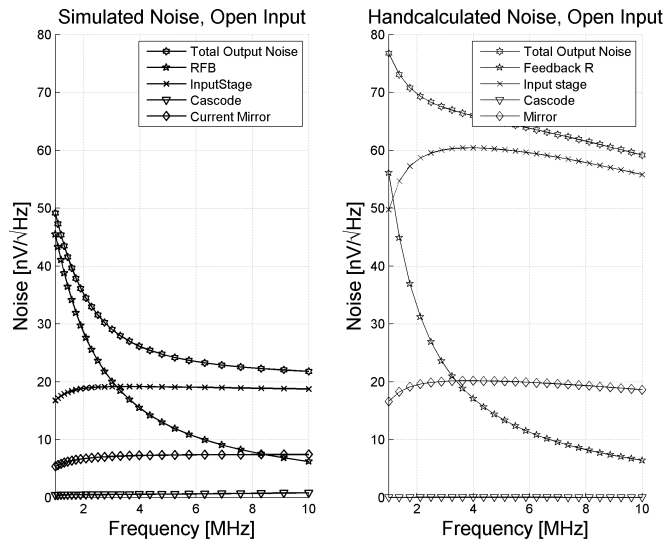


Figure 6.9: Noise contributors in LNA core. Open input terminals ($C_{IN}=1\text{fF}$)

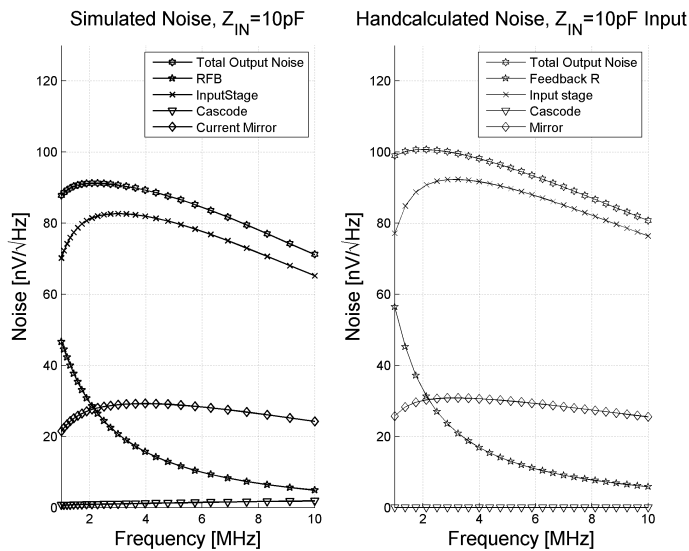


Figure 6.10: Noise contributors in LNA core. Input terminated in $C_{IN}=10\text{pF}$

transfer-function from input to output.

6.3.3 Adjusting Gain Continuously

One solution is to add an active circuit in parallel to the fixed feedback network. The active circuit must have an adjustable gain-factor that can be continuously controlled by a voltage or a current. The active circuit must also have input and output impedances compatible with the input and output levels of the core amplifier, in our case as shown in (6.10) and (6.12). Assuming a trans-impedance amplifier as shown in Figure 22, several alternative implementations are possible. The module to be added must have high output impedance and high input impedance to be compatible with the low input impedance and low output impedance of the core amplifier. If it turns out difficult to design an adjustable circuit with the correct intrinsic impedance behaviour, simple current to voltage or voltage to current converters can be used at the input and/or output. The simplest converter is a resistor. Figure 6.11 gives a summary of how to add adjustable gain to a trans-impedance amplifier assuming that either a voltage-controller-voltage source, a voltage-controlled-current source, a current-controlled-voltage-source or a current-controlled-current source is available. To the knowledge of the author, adjustable current-controlled-current sources could be built from fundamental trans-linear theory, [18]-[20]. Adjustable voltage-controlled-current-sources can be built from modified gm-cells, [17].

If gain-control is only needed for a fraction of the duty cycle it is very efficient with respect to overall power-consumption to have an adjustable gain-factor in the added active feedback circuit that is proportional to current. In Figure 6.12 the adjustable gain-factor is the current-controlled trans-conductor cell. The more current fed into the sub-circuit, the higher the signal transfer in the adjustable cell gets, the higher the overall power consumption gets and the lower the overall gain becomes. Medical ultrasound imaging typically needs gain control during the first few centimeter of the image. Normally we want to reduce gain down to a minimum for the first couple of centimeter, then, for the next four-five centimeter we want to increase gain to maximum typically in a linear-in-dB manner.

The circuit example presented in [12] is one possible implementation of the above-described methodology. The circuit is shown in Figure 6.12. In this design, a trans-conductance cell was chosen as the adjustable module

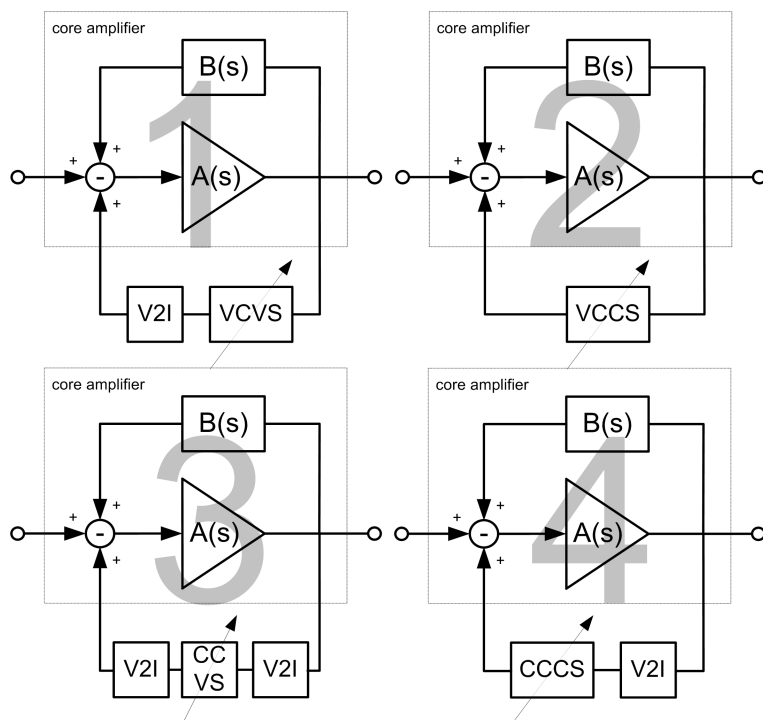


Figure 6.11: Adding gain control to low-noise amplifiers

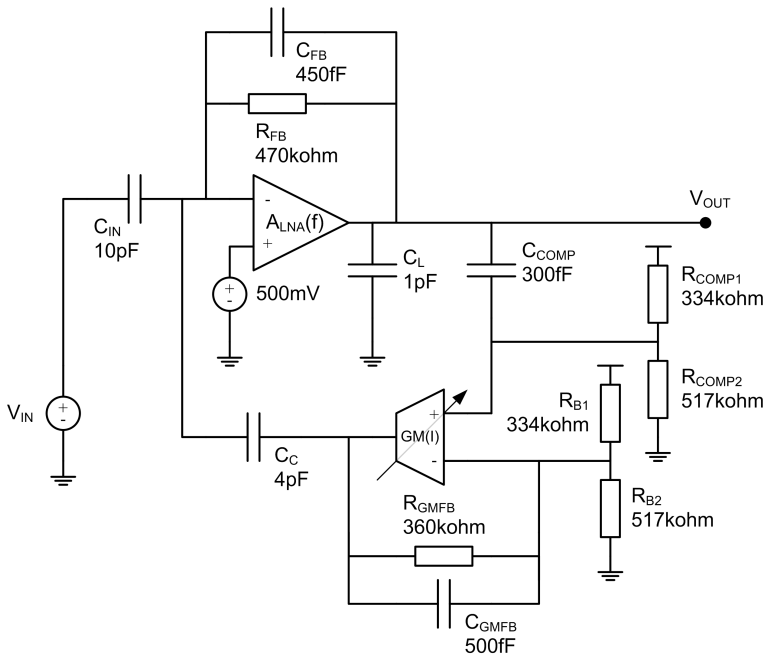


Figure 6.12: Adding gain compensation to a trans-impedance amplifier

added to the existing feedback path. By design this module has high input impedance and high output impedance. The module is therefore inherently compatible with the core trans-impedance amplifier. See section 6.3.7 for details about the adjustable gm-cell. A capacitor was used to close the fixed feedback loop and set gain in the core amplifier. When the active feedback circuit is disabled, this capacitor controls gain in the pass-band. Using a capacitor complicates the design somewhat because it introduces a phase shift of 90degrees between output voltage and feedback current. To overcome this, the sampled voltage must either be phase shifted when connected back to the input of the gm-cell or the current in the fixed feedback loop must be sampled. In the circuit shown in Figure 6.12 we decided to try to phase shift the sampled voltage by feeding it partly into the stop-band of a high-pass filter before feeding it into the trans-conductance cell. Details about the implementation can be found in [13].

6.3.4 Efficiency of the Adjustment Topology

The transfer-function of the circuit shown in Figure 6.12 is found by doing nodal analysis at the negative input node of the core amplifier, see (6.20).

$$\frac{V_{IN} + \frac{V_{OUT}}{A_{LNA}(f)}}{Z_{CIN}(f)} + \frac{V_{OUT} + \frac{V_{OUT}}{A_{LNA}(f)}}{Z_{FB}(f)} + \frac{V_C + \frac{V_{OUT}}{A_{LNA}(f)}}{Z_{CC}(f)} = 0 \quad (6.20)$$

In (6.20) V_{IN} is the input voltage, V_{OUT} is the output voltage, $A_{LNA}(f)$ is the open-loop gain of the core amplifier, $Z_{CIN}(f)$ is the impedance of the input capacitor, $Z_{FB}(f)$ is the fixed feedback impedance of the core amplifier and $Z_{CC}(f)$ is the impedance of the capacitor feeding the output of the trans-conductance cell back to the core LNA. Z_{CC} is necessary to avoid that any DC leakage current from the output of the gm-cell drives the LNA into saturation. A small current would push the amplifier output into saturation due to the high DC trans-impedance. V_C is the voltage at the output of the gm-cell and is found from similar analysis

$$A = B \quad (6.21)$$

$$B = \frac{V_C + \frac{V_{OUT}}{A_{LNA}(f)}}{Z_{CC}(f)} + \frac{V_C}{Z_{GMFB}(f) + R_2} \quad (6.22)$$

$$A = \left(\frac{V_{OUT} \cdot R_{COMP}}{R_{COMP} + Z_{CCOMP}(f)} - \frac{V_C \cdot R_2}{R_2 + Z_{GMFB}(f)} \right) \cdot GM \quad (6.23)$$

Additional components in (6.21), (6.22) and (6.23) are $Z_{CCOMP}(f)$ and R_{COMP} which are the capacitor and the resistor in the phase-shifting high-pass filter, GM which is the gain in the adjustable, active feedback cell and $Z_{GMFB}(f)$, R_{B1} and R_{B2} which are feedback components used in the gm-cell for biasing purposes and additional phase-shift purposes. Equation (6.20) and (6.21) are inserted into each other and solved for V_{OUT}/V_{IN} . The resulting transfer-function is plotted in Figure 6.13. GM is varied from $0\mu S$ to $100\mu S$. Gain at a few selected frequencies is also shown as a function of trans-conductance

In the right part of Figure 6.13 we see a hyperbolic behavior in amplifier-gain versus trans-conductance. High attenuation levels require high trans-conductance in the feedback loop. If we keep the input signal level constant, the amount of output signal available to be multiplied with g_m in is reduced for high attenuation levels. To achieve higher attenuation, even higher trans-

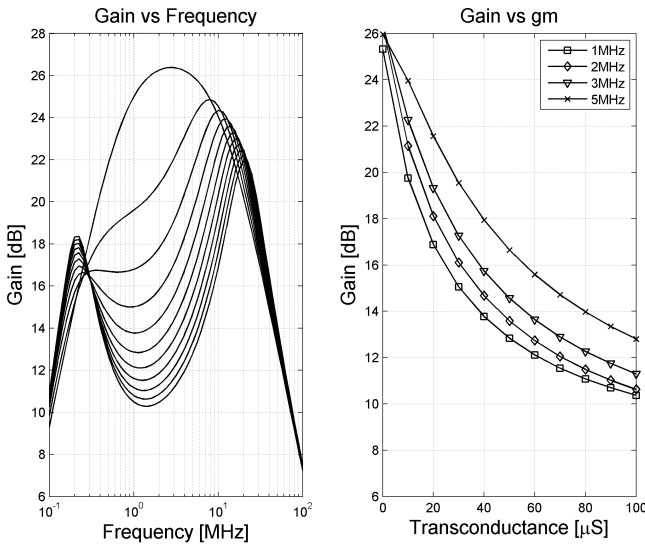


Figure 6.13: Simulated gain in the original active feedback amplifier

conductance is needed. Figure 6.13 is plotted using an ideal model for the gm-cell.

6.3.5 Adding Positive Feedback to Increase Control Efficiency

Observing the circuit in Figure 6.12, it becomes clear that as the amount of available control signal at the input of the gm-cell goes down, the amount of current flowing out of the gm-cell is increased. If we could measure the current flowing out of the gm-cell, copy it to a separate branch, if necessary multiply it by some factor and add it to the a copy of the signal used to control the overall gain, the amount of control signal at the input of the gm-cell would stay more or less constant. The available trans-conductance in the gm-cell could be utilized much more efficient. Overall gain in the LNA would then be controlled by a fraction of the current going back to the LNA input node (negative input on U_1) and a fraction of the original control signal sampled at the output of the amplifier. Intuitively, gain versus control signal should be much more linear due to the fact that the gm-cell input signal is more or less constant. The concept is shown in Figure 6.14. A summation node is constructed using U_2 in a low-input impedance con-

figuration. In an ultra-low-power circuit U_2 could be considered replaced by a diode-connected transistor. For proof of concept a separate amplifier was chosen in this design. Power consumption is higher than necessary because of this. In Figure 6.14, a copy of the output voltage signal, V_{OUT} , is translated to the current domain and connected to the input node of the summation amplifier. The concept is shown in Figure 6.14 using a current-controlled current-source, $CCCS$. The implementation is shown as Q_6 - Q_{12} in Figure 21. An inverted copy of the gm-cell output current is present on the negative output of U_3 . The information signal is already in the correct impedance domain. Next, the two signals are added in U_2 and converted to a voltage signal at the V_{GMP} -node. U_2 was design using a very simple 5-transistor differential-nMOS-input stage, single-ended output stage. Overall-gain in the complete amplifier is controlled adjusting trans-conductance in the gm-cell, U_3 . Trans-conductance is adjusted changing the bias current in the gm-cell. U_3 was realized using a modified Krummenacher/Joehl topology, [21]. See section 6.3.7 for details on the implementation. Common-mode-voltage at the output is controlled with two resistors connected to a voltage-source. The second output is implemented using the same technique incorporated in the LNA. This is shown in Figure 6.16, Q_{10} - Q_{15} . Overall gain versus frequency and current in the gm-cell is shown in Figure 6.15. Positive feedback was also utilized by Fujimoto et. al. in [22] to effectively implement an approximation to the exponential function used to control gain. The circuit presented in [22] is a switched capacitor solution.

6.3.6 Circuit Implementation

The theoretical transfer-function is developed in several steps. First, Kirchhoffs first law is utilized in the V_{SUMIN} node at the negative input of the summing amplifier:

$$I_{OUT} + I_{COMP} + \alpha \cdot I_{GM} + \frac{V_{GMP} - \left(\frac{-V_{GMP}}{A_{SUM}(f)} \right)}{R_{SUMFB}} = 0 \quad (6.24)$$

I_{OUT} is the current flowing out of the buffered output of the core amplifier, I_{COMP} is the current flowing in the compensation network, I_{GM} is the current coming from the adjustable trans-conductor, α represents the amount of positive feedback, V_{GMP} is the voltage at the output of the summing

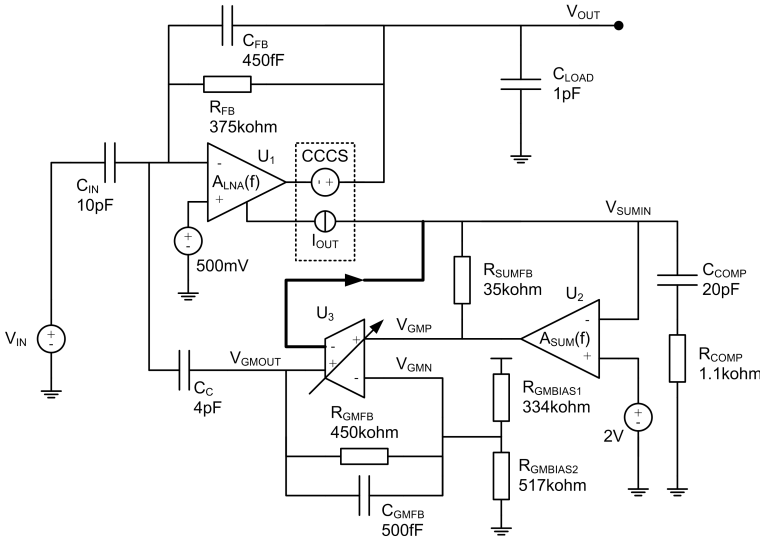


Figure 6.14: Implemented Circuit Topology

amplifier, $A_{SUM}(f)$ is the open-loop gain of the summing amplifier and R_{SUMFEB} is the feedback resistance of the summing amplifier. The equation is further developed by first inserting an expression for the impedance of the compensation network, $Z_{COMP}(f)$, then expressing output current using load impedance, $Z_{LOAD}(f)$ and output voltage, V_{OUT} , and finally solving the equation with respect to V_{GMP} . The result is shown below and will be used later..

$$V_{GMP} = \frac{\frac{V_{OUT}}{Z_{LOAD}(f)} + \alpha \cdot I_{GM}}{\frac{1}{A_{SUM}(f) \cdot Z_{COMP}(f)} + \frac{1}{R_{SUMFEB}} + 1} \quad (6.25)$$

The second major step in the development of the transfer-function is to utilize Kirchhoff's first law also on the input node of the core amplifier. Three currents flow into this node: the current from the source, the current from the adjustable feedback path and the current in the main, fixed feedback loop. The three current-expressions are added together in the equation below.

$$\frac{V_{GMOUT} - \left(\frac{-V_{OUT}}{A_{LNA}(f)}\right)}{Z_{CC}(f)} + \frac{V_{IN} - \left(\frac{-V_{OUT}}{A_{LNA}(f)}\right)}{Z_{IN}(f)} + \frac{V_{OUT} - \left(\frac{-V_{OUT}}{A_{LNA}(f)}\right)}{Z_{LNAFB}(f)} = 0 \quad (6.26)$$

In the expression V_{GMOUT} is the voltage at the output of the adjustable trans-conductor, $A_{LNA}(f)$ is the open-loop gain of the core amplifier, $Z_{CC}(f)$ is the impedance of element connecting the output of the trans-conductor to the input of the core LNA, V_{IN} is the input signal, Z_{IN} is the impedance of the element connecting the input signal to the trans-impedance amplifier and $Z_{LNAFB}(f)$ is the impedance of the fixed feedback network in the core amplifier.

An expression for V_{GMOUT} is found by replacing V_{GMN} and V_{GMP} in the simple voltage current relationship of the gm-cell shown below

$$I_{GM} = (V_{GMP} - V_{GMN}) \cdot GM \quad (6.27)$$

V_{GMN} is replaced by the voltage division-expression of V_{GMOUT} to the negative input of the gm-cell:

$$V_{GMN} = V_{GMOUT} \frac{R_{GMBIAS}}{R_{GMBIAS} + Z_{GMFB}(f)} \quad (6.28)$$

In equation (6.28) R_{GMBIAS} is the parallel connection of the two resistors, $R_{GMBIAS1}$ and $R_{GMBIAS2}$, biasing the negative input of the gm-cell. $Z_{GMFB}(f)$ is the total impedance in the feedback network connected from the output of the gm-cell to the negative input of the gm-cell. This impedance is shown as R_{GMFB} and C_{GMFB} in Figure 6.14.

V_{GMP} in (6.27) is replaced by expression (6.25). The result is plotted in Figure 6.15 setting α to 0 and 1 respectively. One can clearly see the benefit in overall gain when introducing positive feedback in the negative, active-feedback loop. Notice especially the low trans-conductance necessary to reach $15dB$ attenuation.

6.3.7 Design of the GM-cell

The gm-cell implementation is shown in Figure 6.16. A two-stage approach was used to avoid running out of output-current at low bias levels. The first stage is based on the circuit proposed by Krummenacher and Joehl in [21].

Output, short-circuit current for the single-stage, Krummenacher solution versus bias current is shown in Figure 6.17 assuming $1V_{pp}$ input signal. The straight, dotted line represents maximum available current. The curved line represents the dictated short-circuit current. Bias-currents below $300\mu A$ are not able to support $1V_{pp}$ at the input. This will result

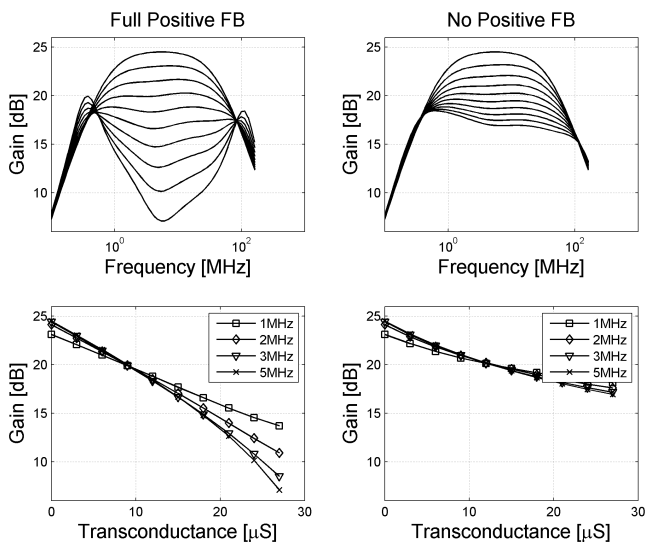


Figure 6.15: Comparison of gain adjustment with ($\alpha=1$) and without ($\alpha=0$) positive feedback

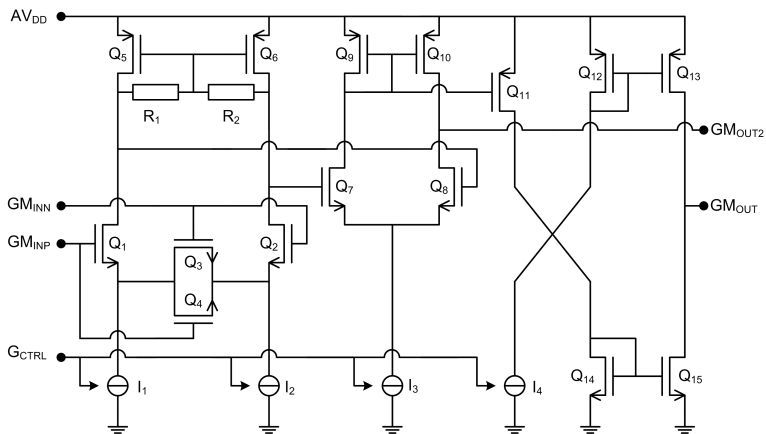


Figure 6.16: Modified Krummenacher trans-conductor

in severe distortion in the overall amplifier for high signal levels at low gain adjustment-levels. By adding the second stage, here implemented by a classical differential amplifier, the circuit is able to deliver enough current to the load for bias-levels all the way down to very low bias currents also for the high input voltage.

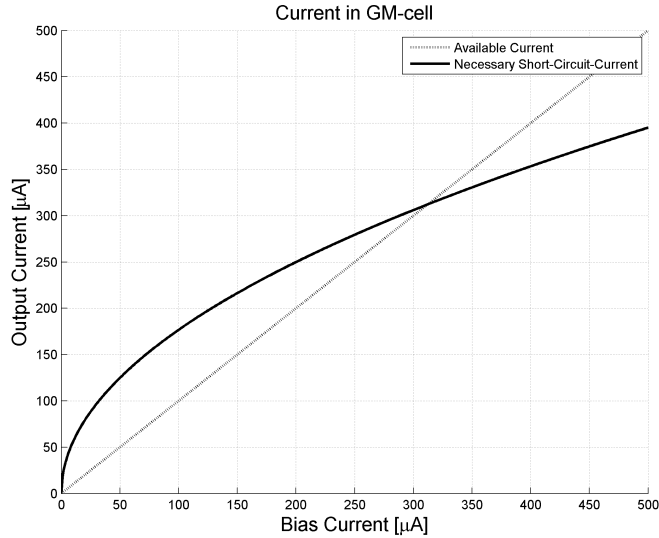


Figure 6.17: Short-circuit output current in Krummenacher trans-conductor with $1V_{PP}$ input voltage

Overall trans-conductance in the circuit in Figure 6.17 is controlled changing the bias current-sources I_1 to I_4 synchronously. An additional, inverted current-output is added to the circuit using current mirrors. This extra output, composed of Q_{11} to Q_{15} , will be used in the positive feedback loop of the gain-control circuitry. Trans-conductance in the input stage composed by Q_1 , Q_2 , Q_3 and Q_4 was discuss by Johns and Martin in [17] and is given by (6.29).

$$gm = \frac{4 \cdot k_1 \cdot k_4 \cdot \sqrt{I_1}}{(k_1 + 4k_3) \cdot \sqrt{k_1}} \quad (6.29)$$

Input transistors, Q_1 and Q_2 and degeneration transistors, Q_3 and Q_4 , have

same size respectively. In (6.29) k_i is the given by

$$k_i = \frac{\mu \cdot C_{OX}}{2} \left(\frac{W}{L} \right)_i \quad (6.30)$$

W is the width of the transistor, L is the length, μ is mobility and C_{OX} is gate capacitance per unit area.

6.3.8 Stability and Loop-Gain Analysis

Phase margin is calculated in accordance to the principle suggested by Blackman to Thomas in 1959, [23]. In short, the principle says that when trying to find the return ratio with respect to a controlled source, the dependant source must be replaced by an independent source of value equal to the gain of the source. Interconnection and polarity must be kept as is. All independent sources in the circuit must be set to zero. All other system conditions must be left unchanged. In our circuit, this means that the open-loop gain in the core-amplifier is changed into a dependant source with value $-A(s)$. Kirchhoff is then utilized on core-amplifier input node.

$$\frac{-A_{LNA}(f) - V_A}{Z_{LNAFB}(f)} + \frac{0 - V_A}{Z_{IN}(f)} + \frac{V_{GMOUT} - V_A}{Z_{GM}(f)} = 0 \quad (6.31)$$

In (6.31) V_A is the voltage at the input node representing return ratio and loop gain. An expression for V_{GMOUT} is developed and inserted into (6.31). V_{GMOUT} is dependant on V_{OUT} . In accordance to the principle described above V_{OUT} is changed into $-A(s)$. The final expression for loop gain is plotted in Figure 6.18 as a function of trans-conductance in the gm-cell.

Without compensation, the amplifier-system is unstable. A brute-force, dominant pole compensation was therefore inserted to achieve stability. This compensation technique resulted in a phase-margin of *39degrees* at minimum gain. A higher phase-margin is desirable to achieve smoother settling. Though, *39degrees* was found to be acceptable to prove the circuit-concept. This should be improved in future implementations. The compensation network, R_{COMP} and C_{COMP} can be found in Figure 6.14.

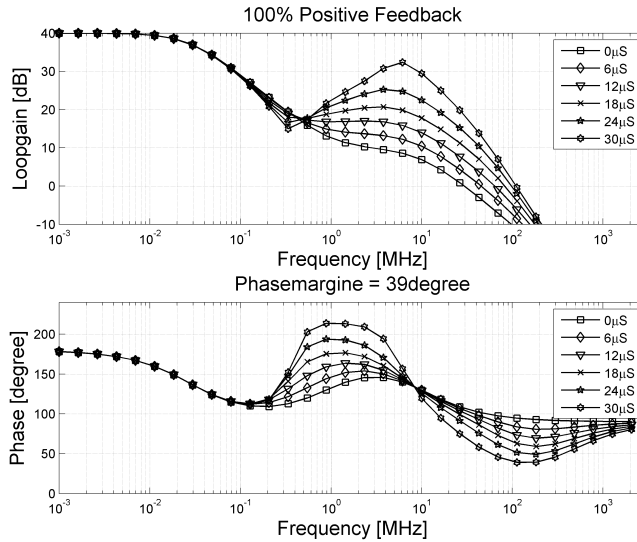


Figure 6.18: Phase-margin as a function of gain compensation

6.4 Experimental Results

The gain-booster amplifier has been realized in the $0.35\mu\text{m}$ SOI process. A microphotography is shown in Figure 6.19.

The bias circuit is shown in the upper left corner of the chip, the core amplifier is shown in the upper middle, the compensation network is shown in the upper right, the summation amplifier is shown in the lower right and the gm-squared cell is shown in the middle to the left. A simple output buffer is shown at the bottom of the chip. The area of the test-chip is $800\mu\text{m} \times 800\mu\text{m} = 0.64\text{mm}^2$. The area occupied by each sub-circuit is listed in Table 6.1. A printed circuit board connected to a National Instruments PXI test station was designed. A Tektronix AFG3102 signal generator controlled by LabView was used to connect the input signal and the control signals to the circuits. The Tektronix DPO4054 oscilloscope was used to measure the output signals and a HP3585 spectrum analyzer was used to measure harmonic distortion and noise. The test-board is shown in Figure 6.20.

6.4.1 Transfer-function

Gain was measured as a function of frequency and control current. The frequency was swept logarithmically with 24 steps per decade from 1MHz

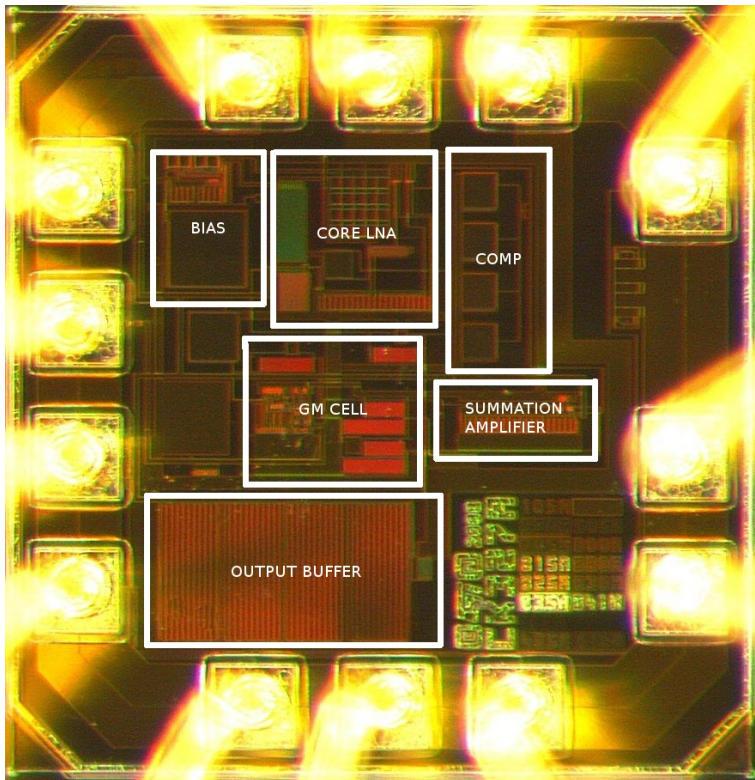


Figure 6.19: Microphotography of the amplifier

Table 6.1: Sub-circuit area consumption

#	Name	W x L	Area Core	AREA PERIPHERAL
1	Biasing	75 x 60		4500
2	Core-LNA	160 x 160	25600	
3	Σ -Amp	135 x 50	6750	
4	Gm-cell	65 x 65	4225	
5	Gm-cell output-C	60 x 60	3600	
6	Compensation	90 x 90	8100	
7	Output Driver	160 x 135		50400
-	Total Area		48275	54900
-	$\sqrt{\text{AREA}}$		$220\mu\text{m}$	$234\mu\text{m}$

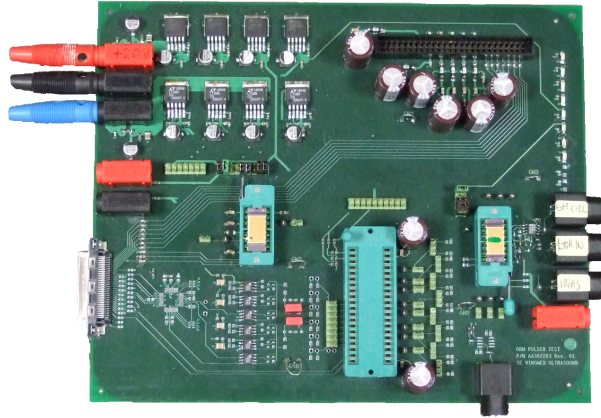


Figure 6.20: Test-board

to 10MHz . The control current was swept from $0\mu\text{A}$ to $200\mu\text{A}$ in steps of $40\mu\text{A}$. The result is shown in the left subplot in Figure 6.21. Simulation results are shown in the right subplot in the figure for comparison.

6.4.2 Power Consumption

The current flowing from the supply into the LNA was recorded during measurements. The result is shown in Table 6.2. Measured power consumption matches the expected values very well.

Table 6.2: Power consumption summary

#	Name	IGM	AVDD	Total	Bias	Core	Sum	GM	Power
1	Max gain	0	337	332	32	240	60	0	1.11
2	Interm gain	40	397	402	32	240	60	70	1.31
3	Interm gain	80	464	472	32	240	60	140	1.53
4	Interm gain	120	534	542	32	240	60	210	1.76
5	Interm gain	160	599	612	32	240	60	280	1.97
6	Minerrm gain	200	668	682	32	240	60	350	2.20

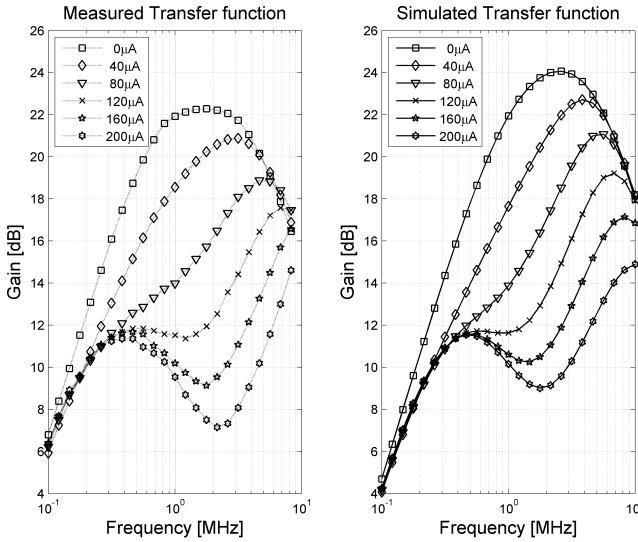


Figure 6.21: Measured transfer function of the gain boosted LNA

6.4.3 Noise Measurements

Noise at the output of the LNA was measured using a spectrum analyzer. Noise was measured in the 1MHz to 5MHz -range for six different gain settings, see Figure 6.22. At maximum- and minimum gain at 3MHz , the output noise was measured to be $125\text{nV}/\sqrt{\text{Hz}}$ and $1.180\mu\text{V}/\sqrt{\text{Hz}}$ respectively.

6.5 Discussion

Initial measurements indicated lower bandwidth and lower gain compared to the theoretical calculated and simulated values. By adding parasitic components for the external environment to the SPICE model, measurements match simulations better. This is seen in Figure 6.21. The input trace to the LNA was modeled using a 3pF capacitor. The output and the oscilloscope were modeled using a 15pF capacitor in parallel with a 10Mohm resistor.

The implementation contains a very poor solution for the current-copy outputs. To keep bandwidth high, the transistors were made close to minimum size, $2\mu\text{m}^2$. The test-circuit therefore is expected to have large spread

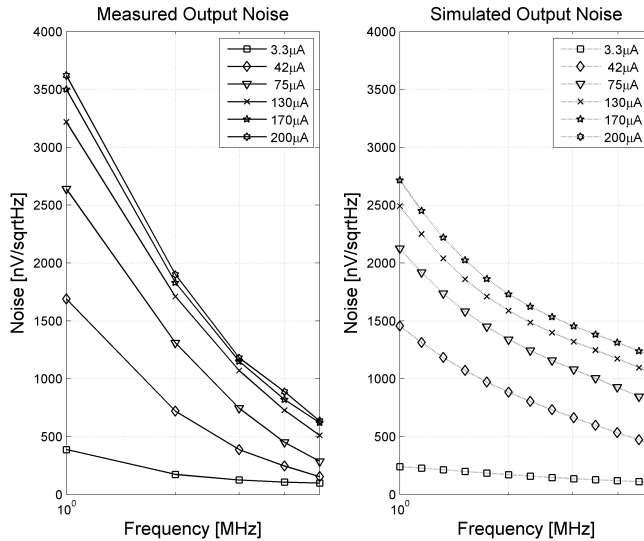


Figure 6.22: Comparison of measured and simulated LNA output noise

in gain from sample to sample. An implementation intended for mass production must use a high-speed mirror with higher accuracy.

During high gain configuration, the current in the active feedback is low. This leads to a very high noise contribution from this cell. What was not implemented in the test-circuit was a switch to gradually switch out the active circuitry when approaching high gain levels. Simulations indicate that the output noise-level suffers $\sim 2dB$ due to this. To keep complexity at an acceptable level, this was not considered important for the test-circuit and therefore not implemented.

One severe limitation of the implemented topology is that the noise level is not kept constant. Instead of increasing the dynamic range when reducing gain, the dynamic window is moved up to handle the higher swing. Simulations indicated that the window also gets smaller as soon as the gain compensation circuit is switched. A much more desirable solution would be to dynamically stretch the window, keeping the noise floor constant. This would require dynamic biasing in the core amplifier and should be a point to be studied in future work.

A bug affecting the output noise was found in the biasing network. One node was poorly decoupled and resulted in higher noise in the test-circuit than first anticipated. This probably explains the difference seen in Fig-

ure 6.22.

6.6 Conclusion

A low-power method adding variable gain to fixed gain amplifiers was presented. The method is compatible with all known amplifier architectures. The main advantage of the method is that no extra power is consumed when gain compensation is close to zero. This feature is very attractive in applications where gain compensation is necessary for a short duty cycle. The performance of the original fixed gain amplifier, here referred to as the core amplifier, is also untouched when gain compensation is zero assuming that a switch is implemented to cut out the active circuitry. A low-noise trans-impedance amplifier was designed to prove the concept. Measurements show that a gain compensation of 15dB was possible at 3MHz for an additional peak power consumption of 1.1mW . Necessary trans-conductance is only $30\mu\text{S}$. This is a reduction in trans-conductance of $\sim 10\text{dB}$ when compared to previously reported results.

6.7 Future Work

A detailed analysis of the noise contribution from the active feedback network was not carried out but is left as future work. For medical imaging applications, it is important that the instantaneous signal-to-noise ratio is kept as constant as possible during gain adjustment. If gain is reduced by 15dB , the circuit should accept at least 15dB higher input signal at the same time as noise is not increased by more than 15dB .

6.8 Acknowledgment

The author wants to thank Fabio Quaglia at STmicroelectronics for irreplaceable help to organize all practical issues related to the research. In addition, the author would like to thank Antonio Russo, Daniele Zanozzo and Marina Zambito for irreplaceable assistance during layout. The author would also like to take the opportunity to recommend the book by E. H. Nordholt, [10]. The book gave me deeper insight into LNA-design and opened up several new alternatives in the field of analog circuit design.

Ideas presented in this book enabled some of the research work presented in this paper.

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Chapter 7

Paper D

A Low Power, Extended Dynamic Range, Fully Differential, Class AB, Log-Domain Allpass Filter

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* Note: A comment to basic companding signal processing is given in Appendix B. This section explains several details found in the circuit presented in this paper.

7.1 Abstract

A fully differential, first order, class AB, log-domain allpass filter has been designed. The filter utilizes a new, low power, high dynamic range pre-processor architecture. The architecture accepts higher input swings and has lower output noise compared to a well-known, classical translinear pre-processor. The lower output noise is due to noise cancellation introduced by the architecture. The total dynamic range is increased $8.1dB$ with an increased power consumption of 22% . The described filter is the first filter using this special pre-processing technique. All published fully differential, class AB, log-domain filters are expected to benefit from the pre-processor architecture.

7.2 Introduction

Modern silicon processes with smaller and smaller element dimensions require lower and lower supply voltages. This is due to the high electrical fields introduced in each transistor and the lower breakdown voltages across the isolation barriers. The low supply voltage necessary in such processes complicates low power, high dynamic range analogue design. Low supply voltage squeezes the dynamic range between lower maximum swing and higher noise levels caused by lower supply currents. To compensate for the decrease in dynamic range, the current consumption has to be increased. Comanding techniques have been suggested as a solution to this challenge. The word comanding is a composition of the two terms *compressing* and *expanding*. A comanding filter first carries out a compression of the input signal, then performs the filtering operation and finally executes an expansion. A special case of comanding filters is the log-domain filters. Log-domain filtering was first introduced by Adams, [1], in 1979. It took several years before his ideas were picked up by other researchers and studied in detail, e.g. [2]-[4]. When compressing the input signal as is being done in log-domain filters, all internal state variables have a corresponding compressed swing. A potential high dynamic range is therefore maintained even when the power supply is drastically reduced.

In this paper, the new pre-processor architecture is used on a log-domain allpass filter for proof of concept. The maximum dynamic range is simulated in presence of an input signal using the periodic-steady-state (PSS) option in SpectreRF, [5].

7.2.1 Log-Domain Filtering

A principle sketch of a first order, single-ended, log-domain filter is shown in Figure 7.1.

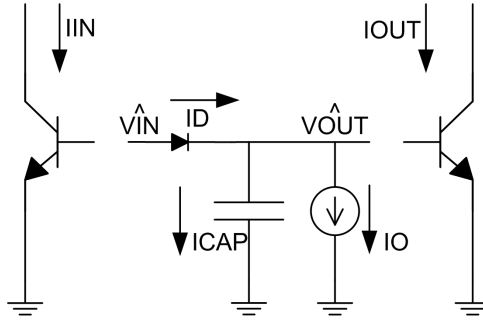


Figure 7.1: Log-domain principle sketch

Using routine KCL analysis, the following equation is developed:

$$I_D = I_{CAP} + I_0 \quad (7.1)$$

$$I_S \exp\left(\frac{\hat{V}_{IN} - \hat{V}_{OUT}}{V_T}\right) = C \frac{d}{dt} \hat{V}_{OUT} + I_0 \quad (7.2)$$

Both sides of (7.2) are multiplied by $\exp(V_{OUT}/V_T)$ and the chain rule is applied to the derivative of V_{OUT} :

$$I_S \exp\left(\frac{\hat{V}_{IN}}{V_T}\right) = CV_T \frac{d}{dt} \exp\left(\frac{\hat{V}_{OUT}}{V_T}\right) + I_0 \exp\left(\frac{\hat{V}_{OUT}}{V_T}\right) \quad (7.3)$$

V_{IN} and V_{OUT} are compressed versions of the input currents and can be replaced by

$$\hat{V}_{IN} = V_T \ln\left(\frac{I_{IN}}{I_S}\right) \quad (7.4)$$

$$\hat{V}_{OUT} = V_T \ln\left(\frac{I_{OUT}}{I_S}\right) \quad (7.5)$$

This substitution clearly shows how the output is an integrated version of the input:

$$I_{IN} = \frac{CV_T}{I_S} \frac{d}{dt} I_{OUT} + \frac{I_0}{I_S} I_{OUT} \quad (7.6)$$

A Laplace transform is carried out on equation (7.6) to highlight the low-pass filter transfer function:

$$H(s) = \frac{I_{OUT}(s)}{I_{IN}(s)} = \frac{\frac{I_S}{CV_T}}{s + \frac{I_0}{CV_T}} \quad (7.7)$$

From (7.7) we see that the corner frequency is tuneable through I_0 .

Noise analysis of log-domain filters is much more complex than noise analysis of conventional linear filters due to the fact that all internal noise sources are signal- dependent. The transfer function from each internal node to the output is also non-linear and signal dependent. This fact is not immediately seen from the filter described above due to its simplicity. The PSS analysis included in SpectreRF was used to account for these effects. A theoretical approach for analysing noise in static and dynamic translinear circuits is given by [6].

7.2.2 Fully Differential Class AB, Log-Domain Filter

In high sensitivity high dynamic range applications, a differential filter structure is chosen to suppress and remove common mode noise. This is the reason why we chose the fully differential structure for our design. The class AB structure was chosen to maximize the dynamic range/ power supply ratio. In theory, the dynamic range is only limited by transistor trans-linearity when using class AB. Maximum signal level is not limited by the bias current as is the case for class A circuits. Because of this, class AB circuits are very power efficient. When running class AB, the complete filter consists of two separate but equal modules. Each module is responsible for either the positive or the negative half cycle of the input signal. The topology is shown in Figure 7.2.

This special topology was first introduced by [7]. The input signal to each of the two filter cores must be strictly positive to keep all transistors in the active region. All fully differential, class AB filters must therefore have some sort of pre-distortion circuit in front to guarantee the swing always to be positive. The topology shown in Figure 7.2 can be used to realize all class AB filters not having complex poles. Filters with complex poles have overshoot in their response. Too large overshoot on internal nodes will move one or more of the transistors in the filter core out of the active region. This is not a problem for our allpass filter.

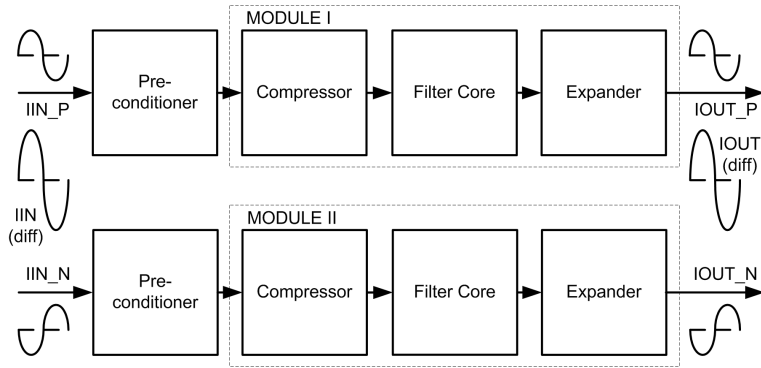


Figure 7.2: Generic differential, class AB filter based on the "two-filter" approach

7.2.3 Preprocessor Design

A circuit suitable for pre-distorting the input signal in a fully differential log-domain filter is shown in Figure 7.3.

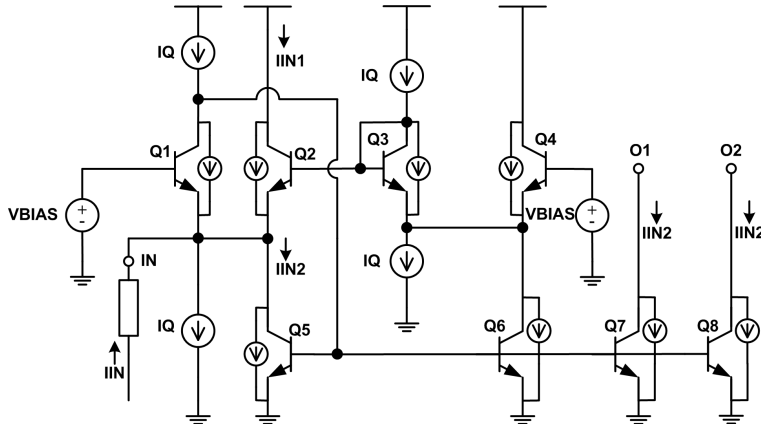


Figure 7.3: Transistor level schematic of the pre-conditioner

The circuit was suggested by [8] and implements equation (7.8) and (7.9). An input signal forced into a circuit described by (7.8) and (7.9) experience half wave rectification. The pre-processor output swing is therefore strictly positive.

$$i_{IN} = i_{IN1} - i_{IN2} \quad (7.8)$$

$$i_{IN1}i_{IN2} = I_Q^2 \quad (7.9)$$

From Figure 7.2 we see that the pre-processor circuit is connected in series with the input signal. Performance parameters like noise, linearity, accuracy and bandwidth must be better in the pre-processor than in the filter core if the performance is not to be limited by this module. This is a fact very often neglected when studying log-domain filters. For the performance of such a pre-processor to be better than the filter core, a substantial part of the power consumption might end up being dissipated here. The potential low-power consumption of log-domain filters might be compromised because of this. An architecture increasing the maximum swing by 6dB and reducing the noise level by 2.1dB while only increasing the power consumption 22% was suggested in [9]. The architecture is shown in Figure 7.4.

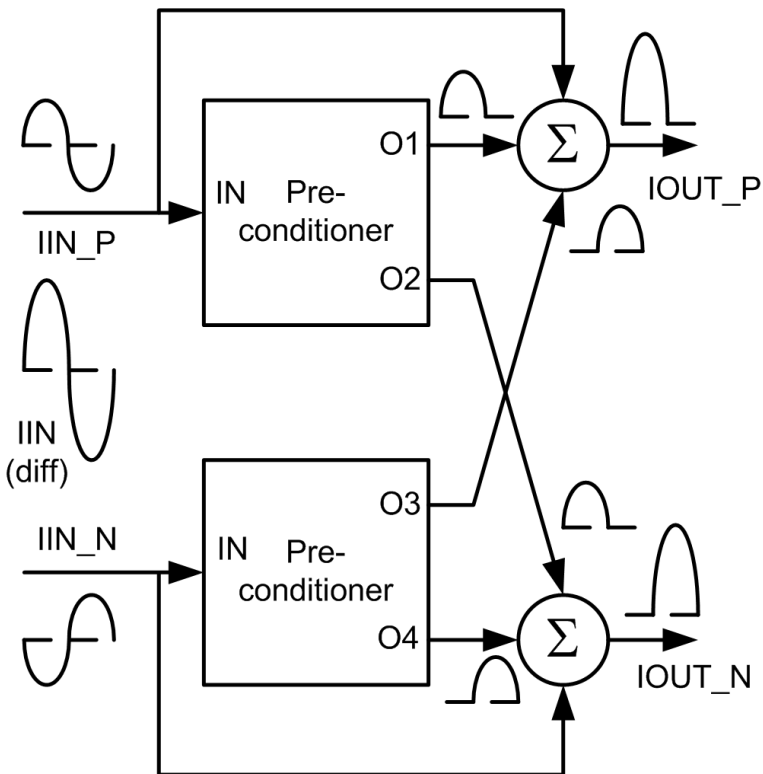


Figure 7.4: Extended dynamic range pre-processor

7.2.4 Allpass Filter

The pre-processor architecture shown in Figure 7.4 was included at the input of an allpass filter for proof of concept. An allpass filter was chosen because we wanted to design a tuneable analogue delay cell. A generic, first order allpass filter is described by equation (7.10).

$$H(j\omega) = \frac{1 - j\omega\tau}{1 + j\omega\tau} \quad (7.10)$$

The phase of this filter is given by equation (7.11).

$$\angle H(j\omega) = -2 \arctan(\omega\tau) \quad (7.11)$$

Due to the lack of log-domain differentiators, realizing zeros without dissipating too much power is a challenge. It is well known that an arbitrary transfer function can be synthesized from a state-space description of a system, [10]-[12]. However, the increase in power consumption is very often high due to the high number of transistors necessary. Equation (7.10) was rewritten as suggested by [13] to get a power efficient implementation of the allpass filter:

$$H(j\omega) = \frac{2}{1 + j\omega\tau} - 1 \quad (7.12)$$

A transistor level schematic of the allpass filter core is shown in Figure 7.5.

Q1-Q5 and C1 implements the damped integrator with a gain of two. The gain is realized using transistor scaling. This is most power efficient. The damping current, I_{DAMP} , running through Q2 is equal to the tuning current, I_{TUNE} , running in Q3. The currents are set equal by mirroring the current in Q3 to Q2 using Q5. Analysing the dynamic translinear loop composed of Q1 to Q4 and C1 using the technique described in [14] gives us the two following equations:

$$2I_{IN}I_{TUNE} = (I_{DAMP} - I_{C1})I_{OUT} \quad (7.13)$$

$$I_{C1} = -C_1 V_T \frac{d}{dt} \frac{I_{OUT}}{I_{OUT}} \quad (7.14)$$

Solving these equations for I_{OUT}/I_{IN} leads to equation (7.15). I_{TUNE} and I_{DAMP} have the same magnitude due to the mirror composed by Q5. They are nevertheless shown explicit in (7.15). The gain factor I_{TUNE}/I_{DAMP} in

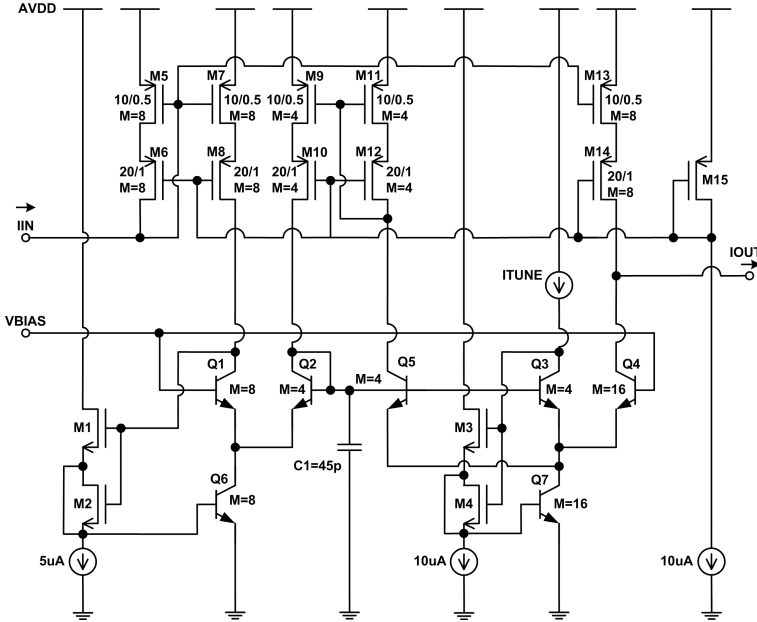


Figure 7.5: Allpass filter core. During simulations, $AV_{DD}=2.5V$, $V_{BIAS}=1.2V$ and $I_{TUNE}=40\mu A$.

(7.15) will for our circuit be equal to one. I_{DAMP} found in the denominator can also be changed to I_{TUNE} to better emphasize the tuning. The result is shown in (7.16).

$$H(s) = \frac{I_{TUNE}}{I_{DAMP}} \frac{2}{1 + s \frac{C_1 V_T}{I_{DAMP}}} \quad (7.15)$$

$$H(s) = \frac{2I_{TUNE}}{I_{TUNE} + sC_1 V_T} \quad (7.16)$$

The time constant τ is given by (7.17).

$$\tau = \frac{C_1 V_T}{I_{TUNE}} \quad (7.17)$$

In the equations above, V_T is the thermal voltage, approximately $25mV$ at room temperature. Using $C_1=45pF$ and $I_{TUNE}=40\mu A$ in (7.11) leads to a phase shift of $\sim 1rad$ at $3MHz$. This translates to a delay of $\sim 53.3ns$ at the same frequency. This delay is easily tuned through I_{TUNE} . The -1 factor in equation (7.12) is implemented using the current mirror consisting of M5, M6, M13 and M14. Because the signals are represented by currents,

the subtract operation is easily performed at the output node, i.e. at the drain of M14 and collector of Q4.

7.3 Simulations

The pre-processor and the allpass filter were implemented in a $0.35\mu\text{m}$ *BiCMOS* process. The frequency response was simulated from 1MHz to 300MHz for three different amplitudes. The result is shown in Figure 7.6.

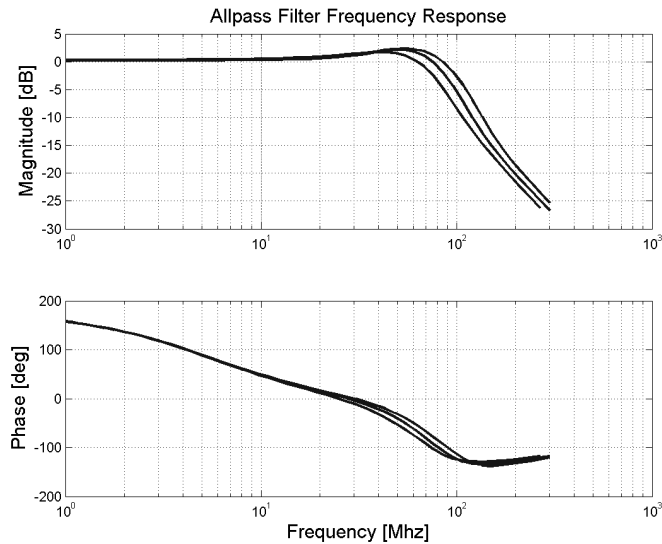


Figure 7.6: Allpass filter frequency response with the preconditioner connected to the input, $I_{IN}=4\mu\text{A}$, $10\mu\text{A}$ and $16\mu\text{A}$

The frequency response was found to be very insensitive to the signal amplitude. The gain at 3MHz changed from 0.65dB to 0.59dB as the signal amplitude increased from $4\mu\text{A}$ to $16\mu\text{A}$. Deviation from unity gain mainly exists due to non-zero base currents. To improve the accuracy of the filter, base-current cancellation must be included. The output noise was also simulated for three different amplitudes. The result is shown in Figure 7.7.

The output noise is signal dependent as expected due to the internal signal dependent noise sources and to the non-linear, signal dependent transfer functions from the internal sources to the output. The noise spectral density was found to be $8\text{pA}/\sqrt{\text{Hz}}$, $8.9\text{pA}/\sqrt{\text{Hz}}$ and $10\text{pA}/\sqrt{\text{Hz}}$ for amplitudes of $4\mu\text{A}$, $10\mu\text{A}$ and $16\mu\text{A}$ respectively.

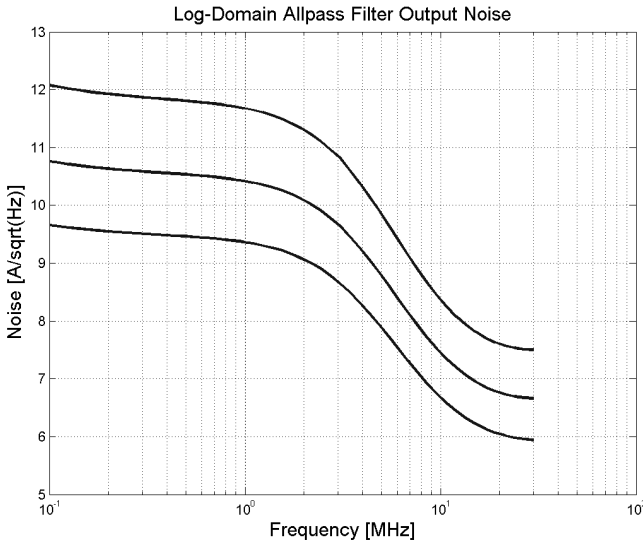


Figure 7.7: Allpass filter output noise with the pre-conditioner connected to the input, $I_{IN}=4\mu A$, $10\mu A$ and $16\mu A$ (lowest noise is produced by lowest signal amplitude)

7.4 Conclusion

A fully differential, class AB, log-domain allpass filter using a new low power, low noise, high dynamic range translinear pre-processor has been designed. The dynamic range was found to be $48.1dB$ (at $3MHz$ assuming a bandwidth of $20MHz$) with a power consumption of $1mW$. The design was carried out for proof of concept. All published fully differential, class AB log-domain filters are expected to benefit from the pre-processor architecture.

7.5 Acknowledgements

Financial support from the Norwegian Research Council through the project ASICs for Microsystems (project number 133952/420) is gratefully acknowledged.

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Chapter 8

Paper E

High Dynamic Range Preconditioning Circuit with Noise Cancellation for Fully Differential, Class AB Log-Domain Filters

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Werner Luzi

Proceedings in the

46th IEEE International Midwest Symposium on Circuits and Systems
Cairo, Egypt, 27-30 December 2003

8.1 Abstract

An architecture performing pre-distortion of the input signal fed to fully differential, class AB log-domain filters is suggested. The architecture performs noise cancellation and increases the maximum allowed input swing. All previous published fully differential, class AB log-domain filters are expected to benefit from the proposed topology. The dynamic range is increased 8.1dB from 53.1dB in the classical circuit to 61.2dB in the proposed architecture when consuming $15.7\mu\text{W}$ and $19.1\mu\text{W}$ respectively. The increase in dynamic range is obtained with the penalty of 22% increase in the quiescent power consumption.

Index Terms—Continuous time filters, log domain, log domain filter, low power, current mode, translinear circuits, companding.

8.2 Introduction

The Continuous demand for decreasing the supply voltage and the power consumption in integrated circuits while maintaining high dynamic range and high sensitivity necessitates increased focus on alternative filter architectures. Companding signal processing techniques have been suggested as a potential solution to this challenge. The term companding is composed of the two words compression and expansion. A filter based on this signal processing technique first performs a compression of the input signal, then carries out the filtering operation and finally performs an expansion of the signal at the output. A special case of companding filters is the log-domain filters. Adams introduced the concept of log-domain filtering to the Audio Engineering Society in 1979, [1]. It took several years before a thorough theory on the topic was available and straight ahead analysis and synthesis methods were developed, [2]-[4]. A great deal of research is still carried out on this group of filters (A search on the "log-domain" topic in the IEEE database revealed 25 publications since the beginning of 2002). This is necessary to give the filters commercial acceptance and to be able to fully explore all the potential advantages of such filters.

Conventional continuous time filters can operate differential to suppress common mode noise. Class AB can also be adapted to improve the dynamic range to power consumption ratio. Differential architectures and class AB operation are also possible for the external linear, internal non-linear log-domain filters. It is necessary though to pay special attention to the format

of the input signal fed to such a filter. It is very important to make sure that none of the internal state variables are moved out of their allowed signal range. All internal currents must be strictly positive for all input signals. This paper presents a new circuit architecture that shapes the input signal of a fully differential, class AB log-domain filter to guarantee correct operation. The circuit is well known in the literature and is referred to as a "pre-processor" or a "pre-conditioner". A principle sketch of a fully differential, class AB, log-domain filter is shown in Figure 8.1.

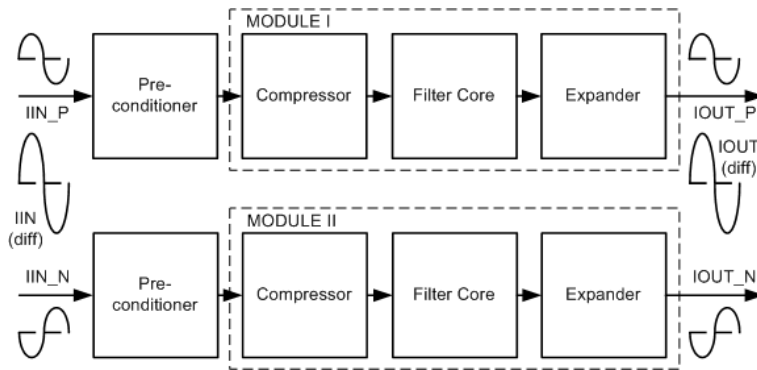


Figure 8.1: Differential filter implementation based on the "two-filter" approach

The pre-processor is shown explicitly at the input of module I and module II.

8.3 Pre-Conditioning the Input Signal

A class AB circuit contains two equal modules for handling the signal swing. Each module is responsible for processing either the positive or the negative part of an input signal. The term class AB is well known from amplifier output stage design, [5]. Here, one transistor handles the positive swing, while another transistor handles the negative swing. If there is no redundancy in the signal handling of the two transistors, the operation is referred to as class B. If there is some overlap, the mode of operation is referred to as class AB. The reason for the redundancy is to minimize distortion. The distortion is referred to as cross-over distortion and will be present in class AB filters as well as in class AB output stages. To minimize the distortion when switching from one module to the other, a controlling scheme smoothing the

transition must be implemented. A lot of different smoothing algorithms exist. Common for all of them is that the output signal can be expressed as a mathematical function of the input signal (here we assume that the signal is represented by a current):

$$i_{OUT} = f(i_{IN}) \quad (8.1)$$

Several expressions have been used successfully both in the output stage of op-amps and in the pre-conditioning of class AB companding filters, ref. [6]-[7]. One of the most popular functions is the geometric mean. This function is mathematical continuous and will therefore introduce a limited amount of cross over distortion. If a perfect half wave rectifier were to be used as a pre-processor, much more cross over distortion would have been introduced due to the discontinuity at each zero crossing. Geometric mean is described by the following equations

$$i_{IN} = i_{IN1} - i_{IN2} \quad (8.2)$$

$$i_{IN1}i_{IN2} = I_Q^2 \quad (8.3)$$

In equation (8.2) and (8.3) i_{IN} is the single ended input signal, i_{IN1} and i_{IN2} are the generated signal components and I_Q is a constant current. Solving this equation for i_{IN1} and i_{IN2} leads to

$$i_{IN1} = +\frac{i_{IN}}{2} + \sqrt{\frac{i_{IN}^2}{4} + I_Q^2} \quad (8.4)$$

$$i_{IN2} = -\frac{i_{IN}}{2} + \sqrt{\frac{i_{IN}^2}{4} + I_Q^2} \quad (8.5)$$

The ratio of the maximum signal amplitude to the constant quiescent current I_Q is referred to as the modulation index, m . The signals i_{IN} and i_{IN2} are shown in Figure 8.2 and Figure 8.3 for two different modulation indices, respectively $m = 1$ and $m = 20$. The signals can also be found in Figure 8.4.

A high modulation index is desirable to minimize the quiescent power consumption in the pre-conditioning circuit. The potential low power consumption of log-domain filters can easily be compromised if a lot of current is spent in the input module of the filter. This fact is very often neglected when discussing the advantages of log-domain filters.

As can be seen from Figure 8.1, the pre-conditioning circuit is located in

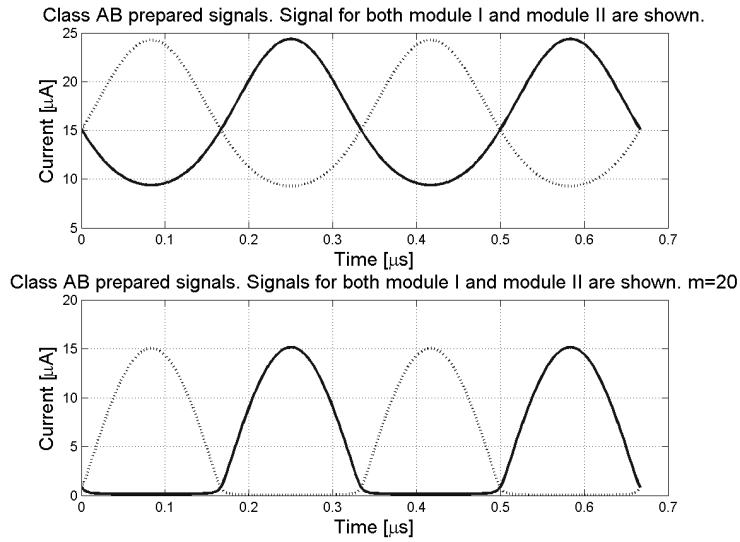


Figure 8.2: Singled-ended pre-conditioner output signals for modulation index equal to 1 (upper) and 20 (lower).

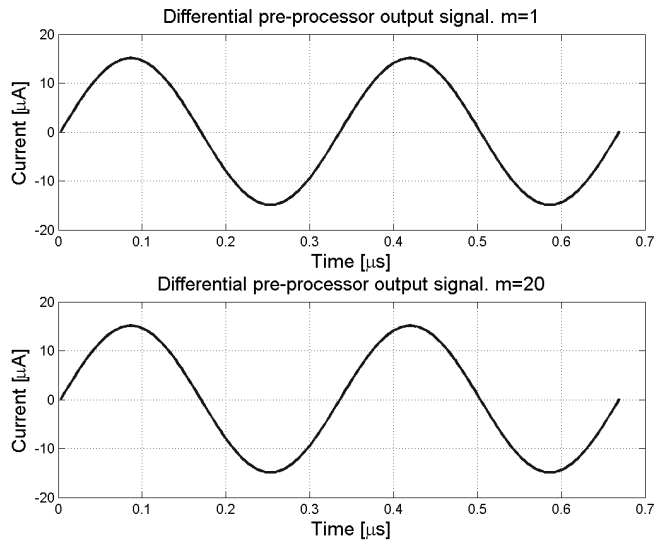


Figure 8.3: Differential pre-processor output for modulation index equal to 1 (upper) 20 (lower).

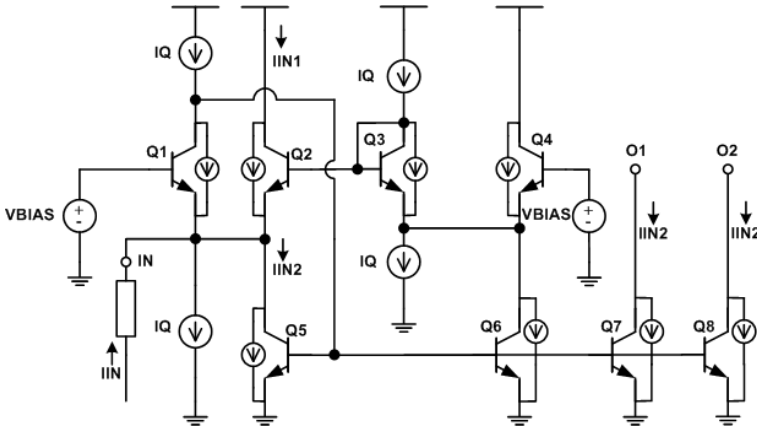


Figure 8.4: Transistor level schematic of the preconditioner core. $V_{DD}=2.5\text{V}$, $V_{BIAS}=1.2\text{V}$ and $I_Q=1\mu\text{A}$.

series with the input of the filter, making this module a potential bottleneck with respect to noise, dynamic range and distortion. To fully utilize the performance of the filter succeeding the pre-processor, this module must have better performance than the log-domain filter itself. It is not obvious that this is possible without spending a substantial amount of power.

8.4 Preprocessor Design

A circuit suitable as the core in the suggested class AB, fully differential pre-distortion circuit is shown in Figure 8.4. The circuit was suggested by [8] and implements equation (8.2) and (8.3). One additional output terminal has been added to prepare the circuit for the extended dynamic range architecture shown in Figure 8.5.

Large signal analysis of the circuit is easily performed using the translinear principle, [9]. The impedance at the input terminal of the pre-processor, IN , is low and behaves as a virtual ground due to the inherent low impedance of the emitter present and to the feedback connection from the base of Q_5 to the collector of Q_1 . As shown in Figure 8.4, voltage to current conversion can then easily be carried out using a resistor. Each transistor shown in Figure 8.4 has a shot-noise source connected between collector and emitter. This source is assumed to be the dominant noise source in the transistors. For the dynamic range analysis in the next section, we then neglect the contribution from the base resistance thermal noise, the base shot-noise and the

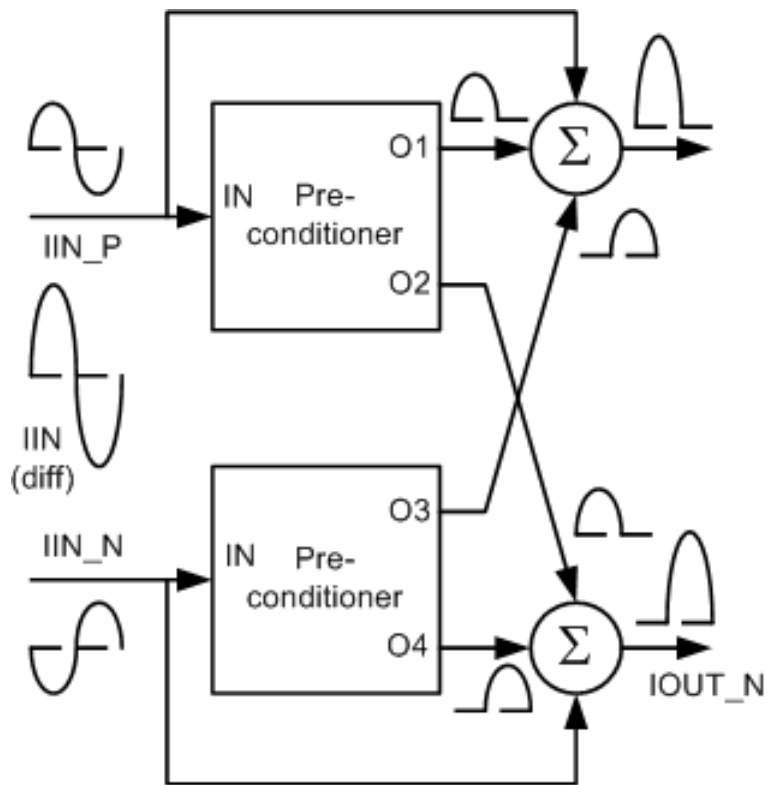


Figure 8.5: Proposed preconditioner

base 1/f-noise.

The proposed architecture is shown in Figure 8.5. The circuit has two input terminals and two output terminals. The architecture must be connected to a balanced, fully differential input signal with zero DC current. Each of the two output signals will always be strictly positive. They can be directly connected to the succeeding class AB filter. At the same time, the signals have maintained their differential nature.

The first elegant property of the circuit is that $6dB$ higher input swing is achieved due to the direct coupling of the signal from input to output. Inherently, this signal path does not add any noise or distortion.

The second elegant property of the circuit is the noise cancellation performed by the cross coupling of the outputs. In the proposed architecture, a noise reduction of $2.1dB$ is achieved. To see how this is possible, the total output noise at $O1$ and $O2$ is divided into a sum of two noise components:

$$i_{o1}^2 = i_{pre}^2 + i_{Q7out}^2 \quad (8.6)$$

$$i_{o2}^2 = i_{pre}^2 + i_{Q8out}^2 \quad (8.7)$$

The first component, i_{pre}^2 , represents the noise contribution from all internal noise sources except the output transistor $Q7$ or $Q8$. The second component i_{Q7out}^2 or i_{Q8out}^2 contains the output noise stemming from the output transistor alone. The single ended output signal of module I and module II respectively when no input signal is present is then given by

$$i_{IOUTP}^2 = i_{pre1}^2 + i_{Q7out1}^2 + i_{pre2}^2 + i_{Q7out2}^2 \quad (8.8)$$

$$i_{IOUTN}^2 = i_{pre2}^2 + i_{Q8out2}^2 + i_{pre1}^2 + i_{Q8out1}^2 \quad (8.9)$$

We see from the equations that both modules will experience common noise components, i_{pre1} and i_{pre2} . The only non-common noise signals are the ones generated in the output transistors of the pre-processors. The differential output signal is given by

$$i_{IOUT}^2 = i_{Q7out1}^2 + i_{Q8out1}^2 + i_{Q7out2}^2 + i_{Q8out2}^2 \quad (8.10)$$

We see from this equation that the common noise sources vanish. The total output noise is therefore lower than for a classic pre-conditioner circuit. A generic filter with the proposed architecture is shown in Figure 8.6.

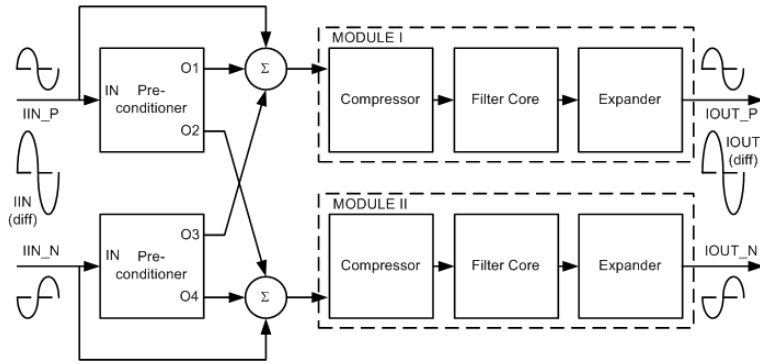


Figure 8.6: Fully differential, class AB, log-domain filter with the low-power, high dynamic range pre-processor

8.5 Noise Analysis of the Preprocessor

Analytical noise analysis of the proposed circuit is not trivial. One reason is that the dominant noise sources, i.e. the shot-noise sources, are signal dependant. The PDS of these sources is given by

$$i_n = \sqrt{2qI_C} \quad (8.11)$$

In equation (8.11) i_n is the noise density in A/\sqrt{Hz} , q is the electron charge and I_C is the collector current of the transistor. Most conventional filters have a bias current much greater than the signal current. Because of this, all internal noise sources are assumed to be stationary. The error made is negligible when using the DC value of I_C when calculating the noise. In the circuit presented in this paper, and in class AB circuits in general, the goal is to make the quiescent current m times smaller than the maximum signal amplitude where m is the modulation index as defined above. The noise sources will therefore be strongly signal dependant. During analysis they must be considered to be non-stationary. The analysis is further complicated because the transfer function from each internal noise source to the output is non-linear. This is due to the nature of the circuit. The mathematical expression to be implemented, explicit showing the non-linearity, can easily be found by applying the translinear principle.

From this discussion, the magnitude of the total output noise is expected to be proportional to the input signal. The PDS of the output noise is also expected to show modulated noise at the fundamental signal frequency and

at the harmonic frequencies.

A method for analyzing the noise analytically in both static and dynamic translinear filters is given in [10]. An analytical analysis is not carried out in this paper. The exact output noise is found from simulations only.

8.6 Simulations

Simulating non-stationary noise using traditional simulators like SPICE is not possible. It is possible to approximately predict the output noise level at different DC input levels. The modulated noise is though not possible to simulate. The main reason is that the noise analysis in SPICE is part of the AC analysis tool, which performs a linearization of the circuit around the bias points. The bias points found during initial AC analysis are then kept constant during the succeeding analysis. Frequency translation effects will not be visible. The SpectreRF simulator from Cadence has a neat tool that enables the analysis of modulation noise, [11]. The analysis is known as the Periodic-Steady-State-Analysis (PSS). This analysis requires a sinusoidal input signal with a defined frequency. Periodic varying bias points are then calculated. These bias points are then used to carry out further calculations like output noise simulations.

The total output noise of the classical pre-processor suggested in [8] was simulated using PSS. The result is shown in Figure 8.7 and Figure 8.8.

The quiescent current was $1\mu A$. The output noise was simulated for 5 different signal amplitudes. Figure 8.7 and Figure 8.8 clearly shows how the total output noise increase as a function of increasing signal amplitude. The modulation noise can be seen around the fundamental of the input signal, i.e. around $3Mhz$. As the signal amplitude increases we can also see how the modulation noise manifests itself at the second harmonic frequency. According to equation (8.9) and (8.10), the output noise of the proposed pre-processor is lower than the output noise of the classical pre-processor. The total output noise of the proposed architecture is shown Figure 8.8 using the same 5 signal amplitudes. As expected, the noise is reduced.

8.7 Conclusion

In this paper we introduced a non-linear preconditioner architecture suitable for increasing the dynamic range in any fully differential, class AB log-

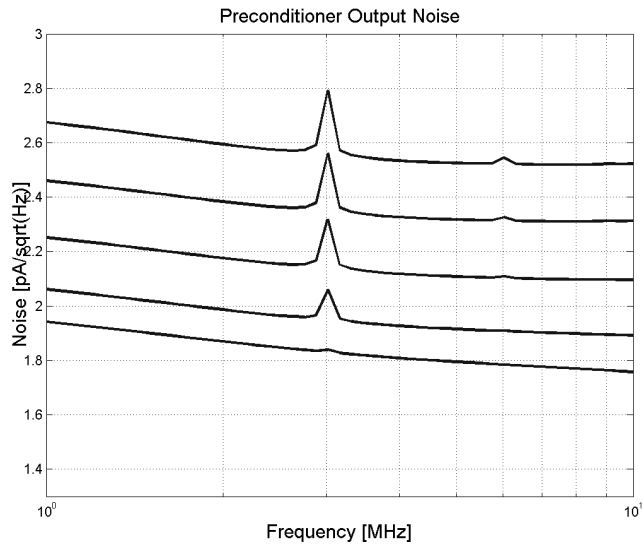


Figure 8.7: Classic pre-conditioner output noise, $I_{IN}=1\mu\text{A}$, $4.75\mu\text{A}$, $8.5\mu\text{A}$, $12.25\mu\text{A}$ and $16\mu\text{A}$ (lowest noise is produced by lowest signal amplitude). Note the presence of the inter-modulation product at the frequency of the input signal, 3MHz.

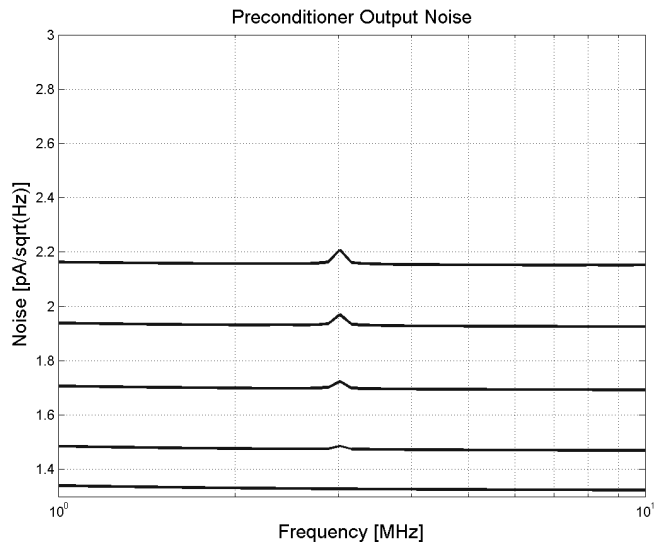


Figure 8.8: Proposed pre-conditioner output noise using the same input signal amplitudes as in Figure 8.7

domain filters. For the given pre-processor core the dynamic range was increased by $8.1dB$ with an increase in the power consumption of 22% . The suggested architecture is expected to take log-domain filtering one step closer to commercial acceptance. In this paper, the pre-processor is based on the geometric mean function. The architecture is not limited to this specific function and can easily be constructed from the harmonic mean function or other suitable core functions. Inherently, the harmonic mean has a larger DC value than the geometric mean. A higher input signal and therefore a higher dynamic range, is expected to be possible for the same distortion performance.

8.8 Acknowledgment

The authors would like to thank the Norwegian Research Council through the project ASICs for Microsystems (project number 133952/420) for the financial help.

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Chapter 9

Paper F

A Log-Domain μ Beamformer for Medical Ultrasound Imaging Systems

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9.1 Abstract

A fully differential, class AB, log domain micro-beamformer has been designed in a $60GHz$ Si-Ge BiCMOS process. The demonstrated micro-beamformer has four input channels and four delays, though the concept can easily be extended to any desirable configuration. The log domain, class AB architecture is perfect for medical ultrasound applications due to the fact that the received ultrasound signal has very low amplitude during the major part of the reception period. This leads to very low power consumption because of the class AB configuration. The delay-line in the micro-beamformer is constructed using a cascade of low input impedance allpass filter cells. A simple implementation of the zero in the allpass filter helps to keep the overall power consumption low. The delay of each allpass filter cell is programmable through the adjustment of a tuning current. Due to the class AB architecture used every source signal must be shaped by a signal preconditioning circuit before connected to the filter cells. A well known preconditioning circuit has been modified to increase the dynamic range. The modification introduces noise cancellation as well as a method to increase the maximum signal swing. The dynamic range of one preconditioning cell is shown to increase $12.6dB$ compared to the classic translinear circuit at a penalty of 15% increase in the power consumption. SNR of one allpass filter cell is typically $56.5dB$ and the global dynamic range of the same cell is typically $63.8 dB$ at an average power consumption of $3.5mW$ when connection 16 input signals to the filter. The power consumption at maximum signal amplitude for the micro-beamformer having four input channels and four delays is $3.2mW$ with a supply voltage of $2.5V$. In the intended application, the quiescent power consumption is a much better description of the average power consumption. This power consumption is $1.3mW$.

Index Terms—Beamforming, companding, log domain, low power, medical ultrasound imaging.

9.2 Introduction

To make real time, 3D medical ultrasound imaging possible, active signal processing must be integrated in the ultrasound probe handle. To keep the temperature below the maximum allowed limit, the power consumption must be low. At the same time, the performance must be kept as high

as possible. This necessitates increased focus on low power circuit design. Companding signal processing techniques have been suggested as a potential solution to low power, high dynamic range signal processing. The word companding is a combination of the two terms compression and expansion. A filter using this technique first performs a compression of the input signal, then carries out the filtering operation and finally performs an expansion of the signal at the output. A special class of companding filters is the log domain filters, [1]-[4]. These filters perform log compression on the input signal and the reciprocal operation on the output signal. One of the main advantages is that all internal nodes have a very small voltage swing which allows the supply voltage to be reduced without reducing the maximum dynamic range (DR). Several log-domain filters have been designed and fabricated for proof of concept and for performance analysis, ref [2]-[8]. The number of publications focusing on specific applications is limited, though see [9]-[11].

Next generation, real time 3D medical ultrasound imaging systems will have an increased number of transducers. This requires some of the signal processing to be performed inside the ultrasound probe, [12]. The objective of this work is to design a micro-beamformer (summation of signals, each having an individual, programmable delay) suitable for placement inside the probe handle. Because of very strict requirements regarding maximum temperature in such medical equipment, the power consumption must be very low at the same time as the performance is as high as possible.

Accurate tuning of the delay is necessary to account for process variations and for flexibility in the final system. Log-domain filters have this capability and are therefore an interesting candidate for ultrasound applications.

This paper starts with an introduction to medical ultrasound imaging. A short introduction to why and how beamforming in classical and commercially available systems is performed is given. References to more in-depth literature are listed. The challenges related to next generation, real time 3D systems are highlighted. The concept of log-domain filtering is presented and a short derivation of an overall linear, internal nonlinear system is carried out. Next, the proposed filter structure core and the preconditioning circuit are presented and analyzed. Based on this module, the log-domain micro-beamformer is designed. Simulation results are presented. A conclusion is drawn in the last section.

9.3 Overview of Medical Ultrasound Systems

Classical medical ultrasound imaging is carried out using an ultrasound probe with several passive transducer elements located in the tip of the probe. Each element is individually available for transmit and receive of ultrasound energy. Most commercial available systems have the transducer elements arranged in a row. A probe used for imaging the heart typically contains from *64 to 128* transducer elements in one row. Steering and focusing of the beam during transmission and reception is carried out by introducing a channel specific delay on each element. An example of beam-focusing and beam-steering + beam-focusing is visualized with the corresponding delay-profiles in Figure 9.1.

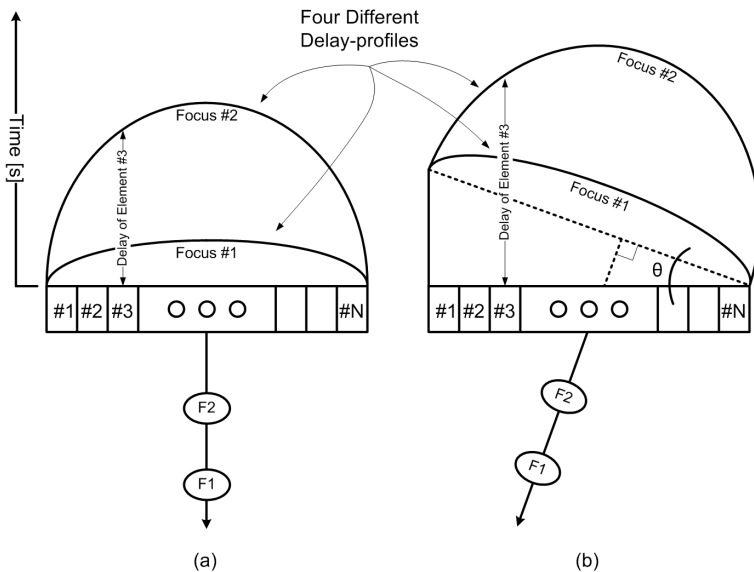


Figure 9.1: Examples of delay-profiles. The distance from the arches to the row of elements represents delay (a) Beam-focusing; two foci are shown (b) Beam-steering and beam-focusing; one angle with two foci are shown

Introducing delay-profiles during transmit and receive is referred to as beamforming. During transmission all elements are excited with an electrical pulse. The delay profile used will determine the direction of the transmitted energy due to the fundamental laws of interference. The same technique is used during reception. The image produced by a row of elements depicts a slice of the object examined (because of the way the transducer elements

are arranged). To construct an image, ultrasound pulses are transmitted from the probe and into an object. All boundaries between materials of different acoustic impedance will reflect a portion of the transmitted energy. As soon as the transmitted pulse leaves the ultrasound transducer element, this element is put into receive mode. One transmit-pulse and its echoes will image one line. To construct a 2D image, several beams must be distributed over the area to be imaged. A low noise preamplifier will be connected to each element and all echoes from the object will be amplified. The length of the amplification period depends on the depth to be depicted. The velocity of sound in water is $1540m/s$. To construct an image of depth $10cm$, each receive period must last at least $130\mu s$. Ultrasound systems based on the techniques just described have one coaxial cable connecting each transducer element to the transmit/receive electronics.

Future generation ultrasound systems will aim at carrying out real time 3D imaging. One way to make this possible is to increase the number of transducer elements and arrange them in an array. By doing this, it is possible to electronically steer the beam in two dimensions. This geometric arrangement will square the number of transducer elements. The ultrasound probe described in [12] contains $50 * 50$ transducer elements. Several algorithms have been suggested for reducing the amount of data produced by such an array, [13]-[15]. Independent of the algorithm used, a necessary building block is a delay cell. An allpass filter is one possible realization of a delay cell. An allpass filter will be used in this design. A more detailed description of ultrasound imaging theory can be found in [16]-[19].

9.4 The Concept of Log-Domain Filtering

The concept of log domain filtering was first introduced by Adams at the Audio Engineering Society in 1979, [1]. Adams recognized that the resistor in a classic RC filter could be replaced by a diode and a current source. The proposed filter is shown in Figure 9.2.

Adams discovered that the cutoff frequency of the filter was tunable over several decades of frequency through adjustment of the current source. The circuit shown in Figure 9.2 composes a low-pass filter:

$$I_D = I_{CAP} + I_0 \quad (9.1)$$

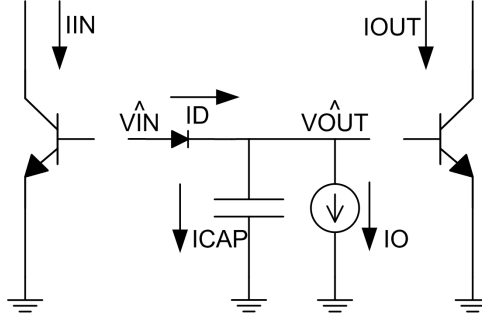


Figure 9.2: Principle sketch of a log-domain low-pass filter

$$I_S \exp\left(\frac{\hat{V}_{IN} - \hat{V}_{OUT}}{V_T}\right) = C \frac{d}{dt} \hat{V}_{OUT} + I_0 \quad (9.2)$$

Both sides of (9.2) are multiplied by $\exp(V_{OUT}/V_T)$ and the chain rule is applied to the derivative of V_{OUT} :

$$I_S \exp\left(\frac{\hat{V}_{IN}}{V_T}\right) = CV_T \frac{d}{dt} \exp\left(\frac{\hat{V}_{OUT}}{V_T}\right) + I_0 \exp\left(\frac{\hat{V}_{OUT}}{V_T}\right) \quad (9.3)$$

V_{IN} and V_{OUT} are compressed versions of the input currents and can be replaced by:

$$\hat{V}_{IN} = V_T \ln\left(\frac{I_{IN}}{I_S}\right) \quad (9.4)$$

$$\hat{V}_{OUT} = V_T \ln\left(\frac{I_{OUT}}{I_S}\right) \quad (9.5)$$

This substitution clearly shows how the output is an integrated version of the input:

$$I_{IN} = \frac{CV_T}{I_S} \frac{d}{dt} I_{OUT} + \frac{I_0}{I_S} I_{OUT} \quad (9.6)$$

A Laplace transform is carried out on equation (9.6) to highlight the low-pass filter:

$$I_{IN}(s) = \frac{CV_T}{I_S} s I_{OUT}(s) + \frac{I_0}{I_S} I_{OUT}(s) \quad (9.7)$$

$$H(s) = \frac{I_{OUT}(s)}{I_{IN}(s)} = \frac{\frac{I_S}{CV_T}}{s + \frac{I_0}{CV_T}} \quad (9.8)$$

A thorough analysis of basic log-domain building blocks, filter analysis and filter synthesis can be found in [20].

9.4.1 System Structure and Specifications

The Micro-Beamformer

All multi-channel ultrasound systems perform beam-forming, [16]. The essence of beam-forming is to add N input channels together with an individually programmable delay for each input signal:

$$x_{BF}(t) = \sum_{i=1}^N w_i x_i(t - t_i) \quad (9.9)$$

The signal $x_{BF}(t)$ is the beam-former output signal, w_i is a channel specific weight making apodization possible, $x_i(t - t_i)$ is the i^{th} input signal having a delay of t_i seconds. Apodization means that the energy at the outer edges of the transducer is decreased. This leads to lower side-lobe levels. The operation described by (9.9) will always be carried out on the signals coming from the ultrasound probe. Beam-forming is the electronic method used for steering and focusing the ultrasound beam (the technique is used both during transmission and reception of ultrasound pulses). In a system with thousands of ultrasound transducers, part of the operation or the complete operation must be carried out in the probe as described in [13]-[15]. A principle sketch of the micro-beamformer demonstrated in this paper is shown in Figure 9.3.

Our design uses $N = 4$ and $M = 4$. The preamplifier is assumed to be off-chip.

Any input signal can be connected to an arbitrary input of the delay line. The delay line is composed of M cascaded low input impedance allpass filters. Because of this, more than one input can be connected and added to the same delay-tap. To make medical ultrasound imaging possible, the dynamic range must be maximized and the power consumption minimized. Low power, high dynamic range design must due to fundamental theory compromise complexity and performance. Our design goal necessitated the consideration of designing a class A or a class AB circuit.

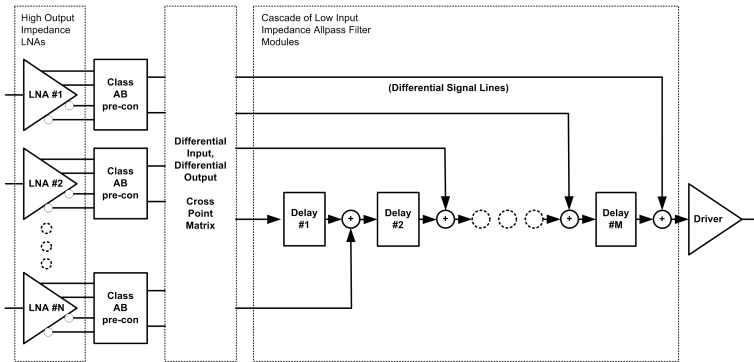


Figure 9.3: A micro-beamformer with N inputs and M cascaded allpass filters

Choosing Between Class A and Class AB

Several definitions and explanations can be found in the literature defining class A and class AB operation. In our context, a filter module operating in class A is a module that handles 360° of an input signal all by itself. It can be seen from the transistor level schematic of a class A module that all internal currents must be strictly positive. For such a module to handle a peak AC swing of I_{AC} , the bias level I_{DC} must be equal or greater than I_{AC} . This is necessary to make sure the current in the transistor never reach zero. In most practical circuits I_{DC} must be greater than I_{AC} . This puts an upper limit to the dynamic range of the circuit. The reason is that the noise floor is proportional to I_{DC} . Higher I_{DC} is necessary in a class A circuit to handle higher swings, though lower I_{DC} is necessary to achieve a lower noise floor. Though, higher SNR is achieved when the current is increased because the maximum swing increases proportional to the bias current while the noise only increases as the square root of the current.

In a class AB filter circuits, two modules will handle a little more than 180° of the swing each. The redundancy is necessary to avoid severe distortion when switching from one circuit to the other. If exactly 180° are allocated to each sub-module, the class of operation is referred to as class B. The most familiar class AB circuit is the push-pull output stage of an amplifier, [21]. To design a high dynamic range, low power filter, class AB operation must be chosen. Theoretically, the dynamic range in class AB circuits is only limited by transistor trans-linearity.

Differential Architecture

To have high immunity to common mode noise and to suppress second order distortion, a differential architecture was chosen. The suppression of second order distortion is especially important in medical ultrasound application due to the fact that the most popular imaging method relies on generated second harmonic energy in the reflected echo. Two main approaches have been reported for realizing differential log-domain circuits. The first approach is based on cross-coupled inverting trans-linear cells, [2]. The other is based on two isolated class A cells. This topology is often referred to as the “two-filter approach”, [22]. Both architectures realize differential filters. If proper preconditioning is included in the circuits, both filters can operate class AB. A block diagram of the “two-filter” approach is shown in Figure 9.4.

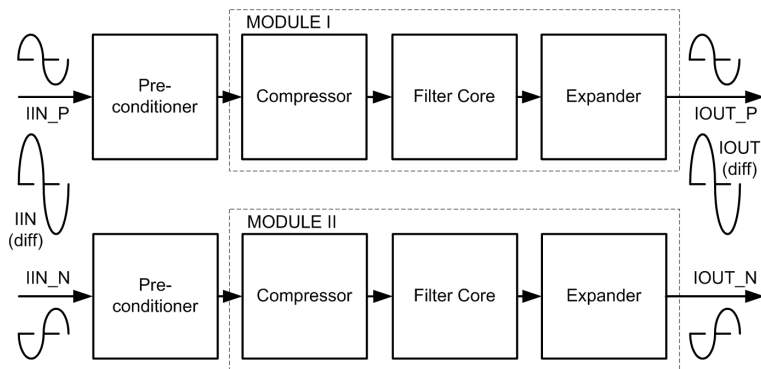


Figure 9.4: Differential filter implementation based on the “two-filter” approach

The Preconditioning Circuit

Signal preconditioning is necessary to guarantee a positive input swing to the filter core, [3]. This is necessary to make the core operate properly. We have chosen the two-filter approach for our allpass filter realization. The fundamental building block used in the preconditioning algorithm was suggested by [7]. The dynamic range of the module was extended by the authors in [23]. The circuit core is reprinted for convenience in Figure 9.5.

The preconditioning circuit is built around a trans-linear loop, [24], and

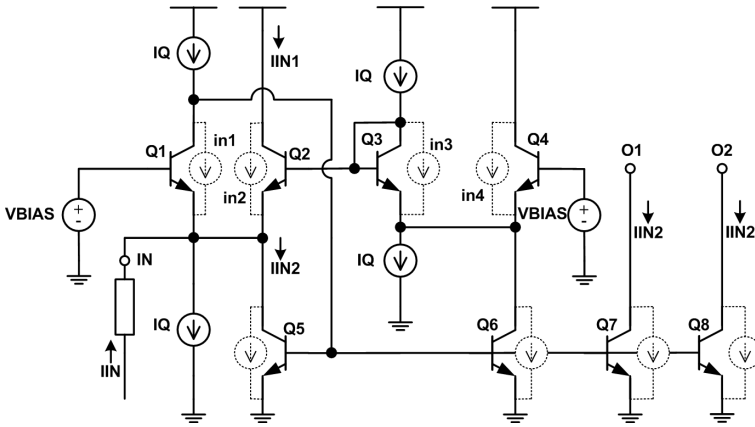


Figure 9.5: Transistor level schematic of the preconditioning circuit. Current shot noise sources, in1-in4, are included for the transistors that make up the trans-linear loop for later analysis

implements (9.10) and (9.11):

$$i_{IN} = i_{IN1} - i_{IN2} \quad (9.10)$$

$$i_{IN1}i_{IN2} = I_Q^2 \quad (9.11)$$

, where I_Q is a quiescent current implementing the constant in the equation, i_{IN} is the single ended input signal and i_{IN1} and i_{IN2} are the desired components. The above equations make sure that the output from the preconditioning circuit is always positive. Solving the equations with respect to i_{IN1} and i_{IN2} respectively leads to:

$$i_{IN1} = +\frac{i_{IN}}{2} + \sqrt{\frac{i_{IN}^2}{4} + I_Q^2} \quad (9.12)$$

$$i_{IN2} = -\frac{i_{IN}}{2} + \sqrt{\frac{i_{IN}^2}{4} + I_Q^2} \quad (9.13)$$

The ratio of i_{IN} to i_Q is referred to as the modulation index, M . The two signal components produced in a preconditioning circuit implementing (9.10) and (9.11) are shown in Figure 9.6. One signal with high modulation index and one signal with low modulation index are shown. High modulation index is necessary to achieve low-power consumption.

The preconditioning circuit is very often given too little attention when

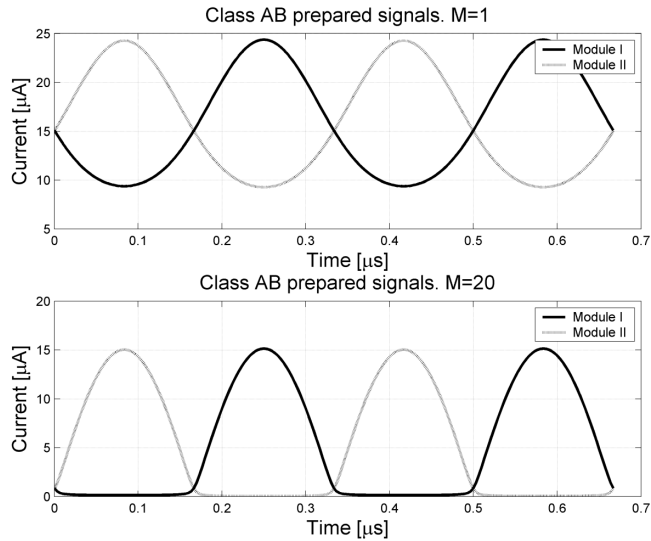


Figure 9.6: Preconditioning circuit output signal for high (lower) and low (upper) modulation indices

discussing log-domain filters. Nevertheless, this circuit module is very critical and unavoidable in every practical class AB log-domain realization. The main reason for emphasizing this is that even though a log-domain filter has the potential to consume very little power, the preconditioning circuit might contribute significantly to the total power consumption. In the end, there is a chance that the potential profit with respect to power is lost. The preconditioning circuit must also have better dynamic range properties than the filter core to make sure this module doesn't introduce a bottleneck in the signal chain. High dynamic range very often necessitates high power consumption, [25].

A way to improve the dynamic range of the preconditioning circuit is shown in Figure 9.7, [23]. No extra processing circuitry except from copies of the preconditioning output currents is needed. The increase in power consumption is therefore very small.

Noise in the Preconditioning Circuit

The output noise of a trans-linear circuit is more complicated to analyze than the noise from ordinary linear circuits, [26]. The main reason is the

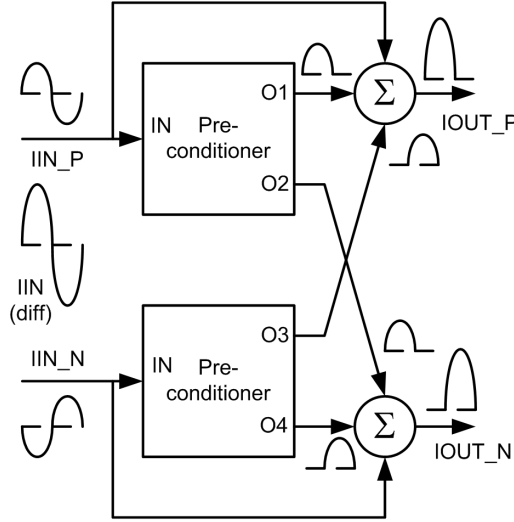


Figure 9.7: Preconditioning circuit with noise cancellation and increased dynamic range

inherent non-linear behavior of the circuit and the fact that the current flowing in the transistors changes many orders of magnitudes more than the injected bias current. The one sided shot noise density is proportional to the collector current and is given by

$$i_n = \sqrt{2qI_C} \quad (9.14)$$

, where i_n is the noise density in A/\sqrt{Hz} , q is the electron charge and I_C is the collector current of the transistor. The shot noise sources present in the translinear core is labeled $i_{n1} - i_{n4}$ in Figure 9.5. These sources are added to equation (9.11) using the translinear principle, [24]:

$$(i_{IN1} + i_{n2})(i_{IN2} + i_{n4}) = (I_Q + i_{n1})(I_Q + i_{n3}) \quad (9.15)$$

Developing this equation further and solving for i_{IN1} and i_{IN2} both shows the conformity with (9.11) as well as the additional inter-modulation products:

$$i_{IN1,IN2} = \pm \frac{i_{IN}}{2} - \frac{(i_{n4} + i_{n2})}{2} + \frac{1}{2}\sqrt{D} \quad (9.16)$$

, where D is given by

$$D = i_{IN}^2 + 4I_Q^2 - 2i_{IN}i_{n4} + 2i_{IN}i_{n2} + 4I_Qi_{n3} + 4I_Qi_{n1} + i_{n4}^2 - 2i_{n2}i_{n4} + i_{n2}^2 + 4i_{n1}i_{n3}$$

From this expression, an increased, signal dependent noise level is expected. In band, the increase in noise level will be dominated by the $2i_{IN}(i_{n2} - i_{n4})$ factor. In addition to these noise components present at the output, there will be contributions from Q5, Q6, Q7 and Q8 which are trivial to handle.

Cancellation of Noise in the Preconditioning Circuit

The architecture suggested in Figure 9.7 has one more output added compared to the classic preconditioning circuit. The second output is just a copy of the first output. The total noise found at each of the two outputs can be decomposed into two uncorrelated components:

$$i_{o1}^2 = i_{pre}^2 + i_{Q1out}^2 \tag{9.17}$$

$$i_{o2}^2 = i_{pre}^2 + i_{Q2out}^2 \tag{9.18}$$

, where i_{o1} and i_{o2} are the total noise at output o_1 and o_2 , respectively, i_{pre} is the total output referred noise from all internal components except the noise from the output mirror transistor and i_{Q1out} and i_{Q2out} are the noise from the mirror transistors itself respectively. The goal is to cancel all noise except the noise from the output transistors. Using the notation given above and assuming a noise free source, the noise at I_{OUTP} and I_{OUTN} is given by:

$$i_{I_{OUTP}}^2 = i_{pre1}^2 + i_{Q1out}^2 + i_{pre2}^2 + i_{Q3out}^2 \tag{9.19}$$

$$i_{I_{OUTN}}^2 = i_{pre2}^2 + i_{Q4out}^2 + i_{pre1}^2 + i_{Q2out}^2 \tag{9.20}$$

Because of the fully differential topology, these outputs will be subtracted at the output of the filter. The total output noise coming from the preconditioning circuit is then given by:

$$i_{I_{OUT}}^2 = i_{Q1out}^2 + i_{Q2out}^2 + i_{Q3out}^2 + i_{Q4out}^2 \tag{9.21}$$

The noise at the filter output stemming from the preconditioning circuit alone is composed of the noise from the output transistors only. Noise cancellation has been implemented. One can tell from Figure 9.7 why only

noise and not the signal is cancelled. The fully differential input signal is preconditioned in accordance with (9.10) and (9.11). The result is plotted at the output of the module as half-wave rectified waveforms. Note how only the positive half of the wave is transferred through the module. Especially note the phase of the signals at the output of the module. The upper module is swinging while the other is quite and vice versa. Bypassing the preconditioning circuit with a copy of the input signal and adding this with the result from both preconditioners leads to a fully differential, half-wave rectified signals with double amplitude.

Allpass Filter Core

A first order allpass filter has a transfer function given by:

$$H(j\omega) = \frac{1 - j\omega\tau}{1 + j\omega\tau} \quad (9.22)$$

To avoid the zero in the numerator (9.22) can be rewritten as:

$$H(j\omega) = \frac{2}{1 + j\omega\tau} - 1 \quad (9.23)$$

, i.e. a low-pass filtered version of the input signal with a gain of two minus the input signal [27]. To avoid ripple in the pass-band, all parasitic poles in the low-pass filter must lie several decades higher than the dominant pole. This is not a problem due to the high f_T in the bipolar transistors used. A block diagram of a fully differential, class AB, log-domain allpass filter is shown in Figure 9.8.

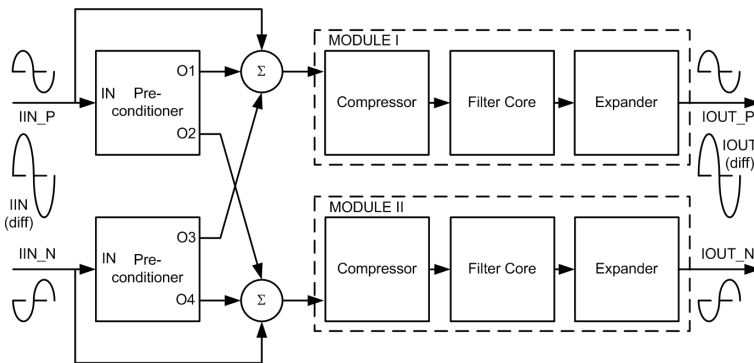


Figure 9.8: The proposed fully differential, class AB log-domain allpass filter

A transistor level schematic of the single-ended allpass filter core is shown in Figure 9.9 and was designed by the authors in [28]. The circuit is an extended damped integrator as presented in [6]. The low-pass filter core consists of C1, Q1, Q2, Q3 and Q4. The gain of two is implemented using the scaling factors indicated in Figure 9.9. A damping current is necessary to develop a low-pass filter from an integrator. This damping current is mirrored from the tune current, I_{TUNE} , using Q5 and the high swing current mirror consisting of M9-M12. A log compressor using feedback to decrease the input impedance while keeping the compressor input DC voltage at an acceptable high level is used, [6]. The high DC level is very important to keep the distortion low. It is given by V_{BE} of Q6 plus V_{GS} of M1. The input signal to the compressor flowing into the collector of Q1 is sampled by V_{BE} of Q6. If this current increases, V_{BE} of Q6 increases. When V_{BE} of Q6 increases the gate voltage of M1 increases. This is necessary to keep the current in M1 constant. The negative feedback loop is closed by connecting the gate of M1 to the collector of Q1. M2 is a double poly capacitor used to limit the bandwidth of the feedback factor and thereby reducing the risk of oscillation. The same circuit topology is used to compress and inject the tuning current, I_{TUNE} .

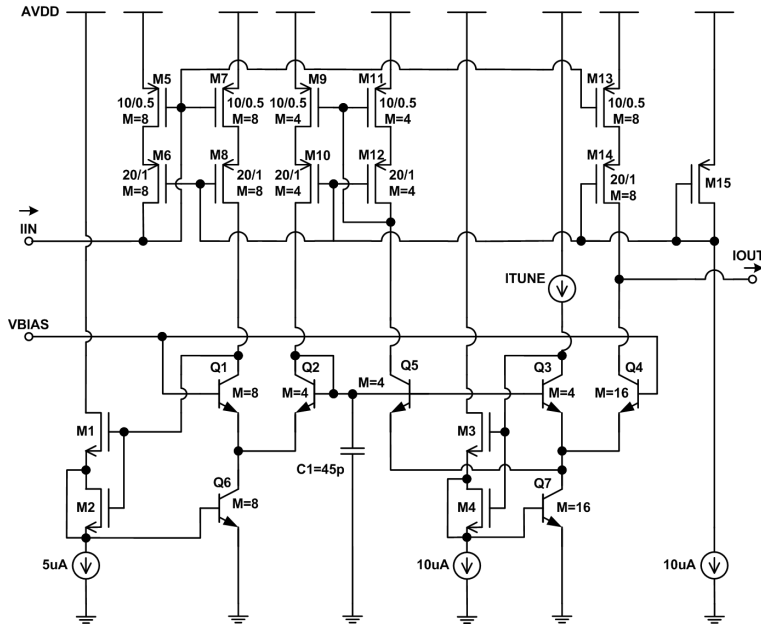


Figure 9.9: Allpass filter core

The Effect of Non-idealities on the Log-Domain Filter

Three major effects introduce non-idealities to log-domain filters. Parasitic emitter resistance leads to a lower corner frequency but keeps the passband ripple and gain intact, [20]. This effect will not cause any major problems in our architecture. Though, the error introduced is absorbed by scaling the capacitor or tuning the bias current in the integrator. This is automatically done during design. Finite base current leads to a drop in corner frequency and a change in Q-factor. Base current compensation was not implemented to compensate for these effects due to the additional power consumption added by the extra current mirrors necessary. In the application, it is of utmost importance to keep the power consumption as low as possible. The effect of Early Voltage leads to a modulation of the saturation current of the bipolar transistor. The process used has an Early Voltage higher than 100V. Variation in collector current with changing V_{CE} will occur. Luckily in log-domain filters and in translinear circuits in general, bipolar transistors are always biased in pairs leading to a good cancellation of the Early-effect. A thorough and detailed description of non-idealities in log-domain filters is given in [29]-[30].

In addition to these deterministic effects area mismatch changes the behavior of the real filter from the ideal one. Area mismatch can be translated into a shift in the saturation current, I_S , of the bipolar transistor which again can be translated into a shift in corner frequency, passband ripple and gain. A highly symmetrical layout utilizing cross-connection and common-centroid geometries will be used to minimize this effect.

Cascading Allpass Filter Cells

The architecture demonstrated in this paper and showed in Figure 9.3 cascades M equal allpass filter cells. The situation with noise sources included is shown in Figure 9.10.

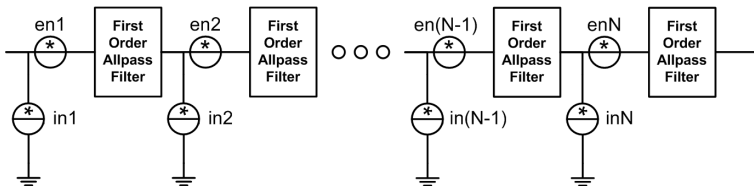


Figure 9.10: Noise analysis of a cascade of N allpass filters

To get the best overall dynamic range, all cells are designed to have the same equivalent noise power. The delay-line noise figure (NF) is given by (9.24) assuming the first cell to act as the source. This assumption is also valid when a noisy source is connected to the delay-line having noise level much lower than the level of the delay-line itself.

$$NF = 10 \log(N) \quad (9.24)$$

Provided the assumption above, equation (9.24) predicts a heavy reduction of sensitivity and dynamic range. If N is chosen equal to 10 the corresponding NF is $10dB$. Due to power consumption restrictions, this noise level from the signal source can not be increase as high above the noise level from the delay-line as desirable and as would have been the case in a classical noise scaled system. Though, a preamplifier must be included to avoid too heavy increase in NF . A preamplifier will reduce the maximum allowable input swing but increase the sensitivity. If we assume a source noise power normalized to $1W$, eight sources connected to the delay-line input and a filter cell equivalent input noise power normalized to $1W$, overall noise figure as a function of gain in the preamplifier, total dynamic range as a function of preamplifier gain and total dynamic range as a function of NF is plotted in Figure 9.11. The dynamic range of one allpass filter is assumed to be $50dB$ as indicated by the dotted line in the second plot from the left. Dynamic range is very expensive in terms of sensitivity.

An active delay-line built by cascading filters will accumulate harmonic energy. A filter module connected to a clean, single tone input will due to internal non-linearity generate an output with harmonic components as shown in Figure 9.12. Higher order harmonic components will decay very quickly and in most practical situations only second and third harmonic distortion is relevant.

In a cascade of such modules the harmonic components generated in one cell will accumulate throughout the complete delay-line. The output of the last cell will contain equal amount of harmonic energy from all cells in the delay-line taking into consideration that the magnitude response of the allpass filter is unity in the passband. To have an overall maximum amount of harmonic distortion in the delay-line, the harmonic distortion of one cell must lower than the level estimated by (9.25). We assume higher

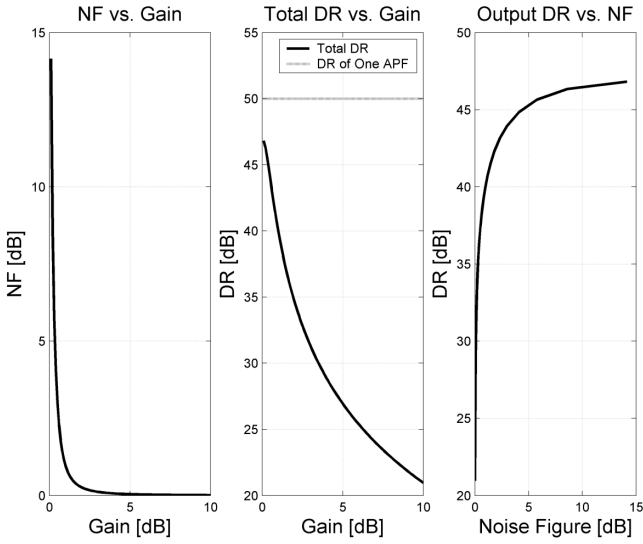


Figure 9.11: Dynamic range and noise figure considerations in the delay-line

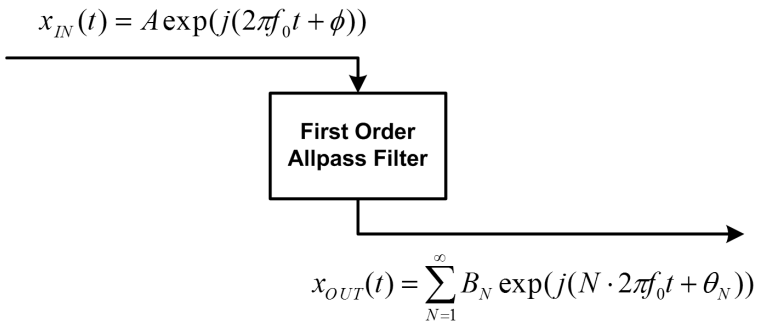


Figure 9.12: Harmonic distortion in the allpass filter

order distortion products to be negligible.

$$HDx_{MODULE} = 20 * \log 10 \left[\frac{10^{\left(\frac{HDx_{OVERALL}}{20}\right)}}{N} \right] \quad (9.25)$$

In (9.25) HDx_{MODULE} is the necessary x^{th} harmonic distortion for one module, $HDx_{OVERALL}$ is the desired total harmonic distortion for the selected component and N is the number of cells in the cascade.

9.4.2 Simulation Results

The micro-beamformer has been designed from the preconditioning modules and the allpass filter circuits. Simulations are first carried out on the preconditioning module, then on the allpass filter cells and finally on the complete micro-beamformer.

Comparison of Noise in the Preconditioning Circuits

The translinear circuit was simulated using the periodic steady state noise (PSS and PNOISE) analysis included in SpectreRF, [31]. This analysis tool takes into account any non-linear behavior. The output noise of the classical preconditioning circuit and the modified, increased dynamic range circuit was compared. The result is shown in Figure 9.13. The frequency of the input signal was $3MHz$.

Notice the noise peaks due to inter-modulation in the specter at $3MHz$ and $6MHz$ as predicted in previous sections. SNR calculations in the preconditioning circuits assuming a bandwidth of $20MHz$ are listed in Table 9.1 and Table 9.2.

Table 9.1: SNR in original preconditioning circuit

I_{IN}	I_{OUT_DIFF}	i_{nOUT}	SNR_{OUT}
$1.00\mu A_{peak}$	$0.59\mu A_{peak}$	$1.9pA/\sqrt{Hz}$	34.2dB
$4.75\mu A_{peak}$	$2.83\mu A_{peak}$	$2.1pA/\sqrt{Hz}$	46.7dB
$8.50\mu A_{peak}$	$5.07\mu A_{peak}$	$2.3pA/\sqrt{Hz}$	50.7dB
$12.25\mu A_{peak}$	$7.03\mu A_{peak}$	$2.6pA/\sqrt{Hz}$	52.7dB
$16.00\mu A_{peak}$	$9.50\mu A_{peak}$	$2.8pA/\sqrt{Hz}$	54.6dB

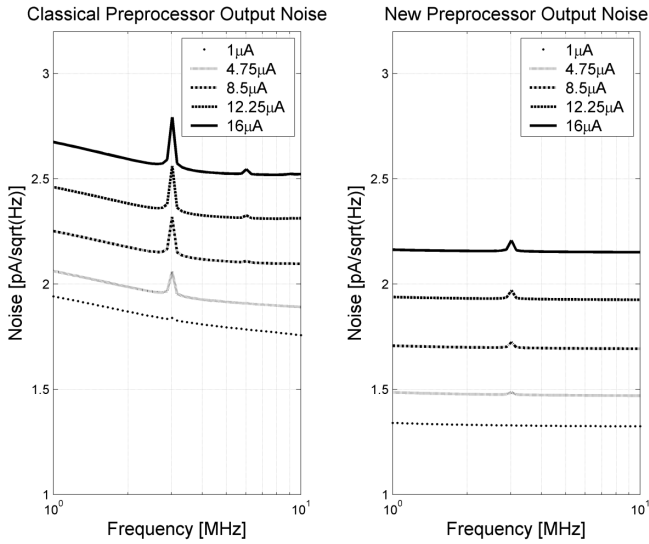


Figure 9.13: Preprocessor output noise, $I_{IN} = 1\mu A_{PEAK}$, $4.75\mu A_{PEAK}$, $8.5\mu A_{PEAK}$, $12.25\mu A_{PEAK}$ and $16\mu A_{PEAK}$

Table 9.2: SNR in new preconditioning circuit. Last column reports increase in SNR

I_{IN}	I_{OUT_DIFF}	i_{nOUT}	SNR_{OUT}	ΔSNR
$1.00\mu A_{peak}$	$2.0\mu A_{peak}$	1.3 pA/ \sqrt{Hz}	47.5dB	13.4dB
$4.75\mu A_{peak}$	$9.5\mu A_{peak}$	1.5 pA/ \sqrt{Hz}	60.1dB	13.4dB
$8.50\mu A_{peak}$	$17.0\mu A_{peak}$	1.7 pA/ \sqrt{Hz}	63.9dB	13.1dB
$12.25\mu A_{peak}$	$24.5\mu A_{peak}$	2.0 pA/ \sqrt{Hz}	65.9dB	13.1dB
$16.00\mu A_{peak}$	$32.0\mu A_{peak}$	2.2 pA/ \sqrt{Hz}	67.2dB	12.6dB

The output swing of the classical architecture is effectively divided in two because of the implemented function. Negative swings are more or less clamped to zero. Close to $6dB$ output-power is literally thrown away. The extended configuration first reinserts this loss and then again nearly doubles the output swing. In addition to this, the architecture by its nature performs noise cancellation as described in previous sections. The SNR of this architecture is therefore increased both due to higher output swing and to lower output noise. The increased in SNR comes at a penalty of 15% higher power consumption. The quiescent power consumption of one classical preconditioning circuit with no input signal is $6.6\mu A * 2.5V = 16.5\mu W$. The power consumption in the extended circuit is $7.6\mu A * 2.5V = 19\mu W$ assuming $I_Q = 1\mu A$.

Allpass Filter with the Preconditioning Circuit Connected

The core module of the delay line is the allpass filter. The micro-beamformer architecture demonstrated here dictates that anything from one up to the maximum of all transducer signals might be connected to the same allpass filter cells. The allpass filter is therefore simulated for two extremities, one and maximum preconditioning circuits connected to the input. The maximum number of input signals is in this example set to 16.

One Preconditioning Circuit at the Input

The frequency response was simulated for three different signal levels using the Periodic AC (PAC) tool in SpectreRF. The result is shown in Figure 9.14.

The gain was found to change from $0.15dB$ to $0.20dB$ (delta gain of $0.05dB$) at $3MHz$ when the amplitude of the input signal changed from $4\mu A_{PEAK}$ to $16\mu A_{PEAK}$. All results are listed in Table 9.3.

A systematic gain error of $\sim 0.2dB$ was found in the filter mainly due to base current. Base-current cancellation will remove this error. As predicted in previous sections, the output noise level is expected to vary as a function of signal amplitude. The output noise for $I_{IN} = 4\mu A_{PEAK}$, $10\mu A_{PEAK}$ and $16\mu A_{PEAK}$ is plotted in Figure 9.15.

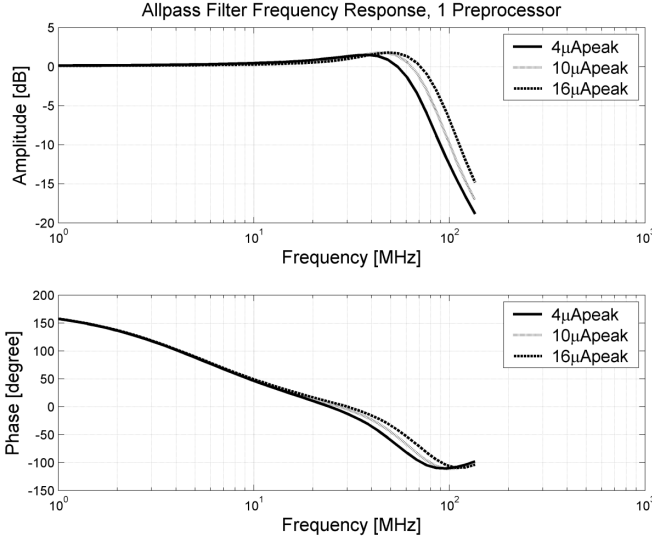


Figure 9.14: Frequency response: one pre-conditioning circuit at the input, $I_{IN}=4\mu A_{PEAK}$, $10\mu A_{PEAK}$ and $16\mu A_{PEAK}$

Table 9.3: Simulation results of the log-domain allpass filter with one pre-conditioner, $V_{DD}=2.5V$, $I_{TUNE}=40\mu A$, The fundamental frequency was 3MHz

I_{IN} [μA_{PEAK}]	4	10	16
I_{OUT} [μA_{PEAK}]	4.1	10.2	16.2
$I_{DD_QUIESCENT}$ [μA]	380	380	380
$P_{QUIESCENT}$ [mW]	~ 1	~ 1	~ 1
a_I [dB] @ $f = 3\text{MHz}$	0.15	0.17	0.20
Group delay [ns] @ $f = 3\text{MHz}$	56.4	56.4	56.4
$I_{NOISE(OUT)}$ [pA/ $\sqrt{\text{Hz}}$] @ $f = 3\text{MHz}$	8.6	9.7	11
Output dynamic range [dB]	37.5	44.4	47.3
Third harmonic distortion [dB]	-52	-43.4	-41.8

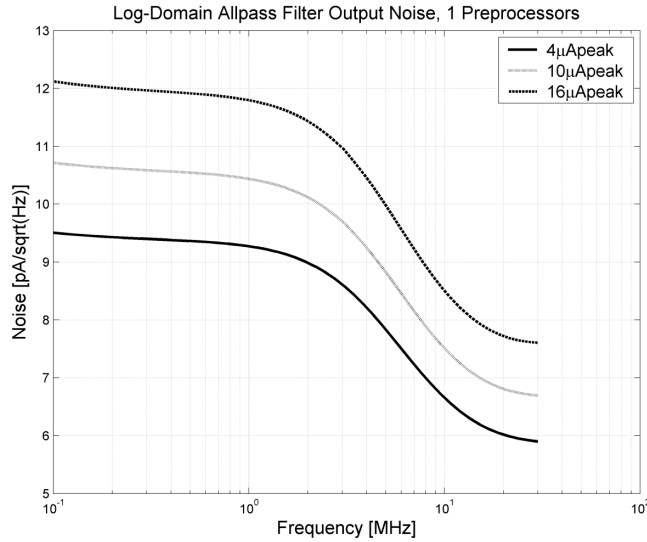


Figure 9.15: Allpass filter output noise with one preconditioning circuit connected to the input, $I_{IN}=4\mu A_{PEAK}$, $10\mu A_{PEAK}$ and $16\mu A_{PEAK}$

Sixteen Preconditioning Circuits at the Input

A simulation where 16 input channels are connected to one allpass filter was carried out. The resulting output-swing is shown in Figure 9.16 ($64\mu A_{PEAK}$, $160\mu A_{PEAK}$ and $256\mu A_{PEAK}$).

Each input channel has its own preconditioning circuit. The global dynamic range was found to be $63.8dB$. The simulated frequency response for the same three signal amplitudes is shown in Figure 9.17. The output noise is shown in Figure 9.18.

The group delay is constant and approximately $57.3ns$ at $3MHz$. The results are summarized in Table 9.4.

The Micro-Beamformer

A micro-beamformer as described in Figure 9.3 was designed. A transient analysis was carried out to prove the concept. Four input signals having an incremental delay of $60ns$ were connected to the beamformer. The input signals are plotted as dashed traces in Figure 72.

A proper cross-point matrix configuration was established to align the four input signals. The beamformed output signal is shown as the solid line

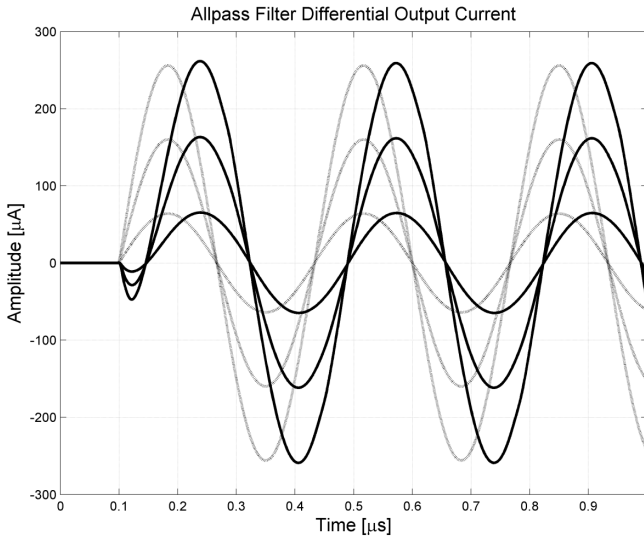


Figure 9.16: Input signal (dashed) and output signal (solid) in an allpass filter with 16 preconditioning circuits at the input. Three amplitudes are plotted to show the amplitude insensitive delay

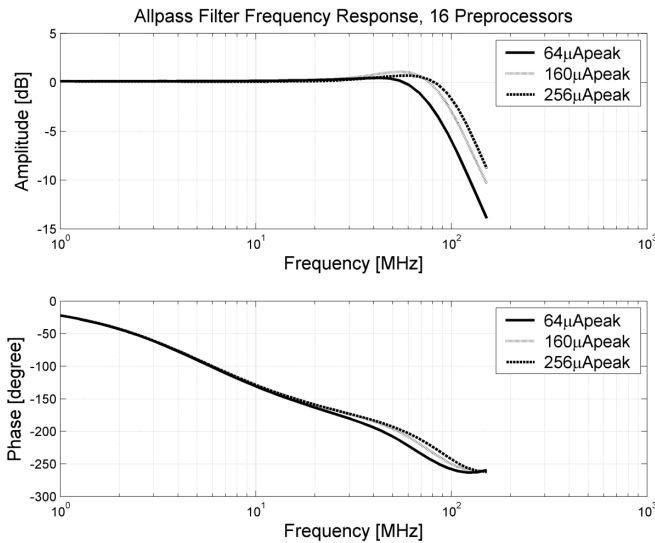


Figure 9.17: Allpass filter frequency response with 16 preconditioning circuits connected to the input, $I_{IN} = 64\mu\text{A}_{PEAK}$, $160\mu\text{A}_{PEAK}$ and $256\mu\text{A}_{PEAK}$

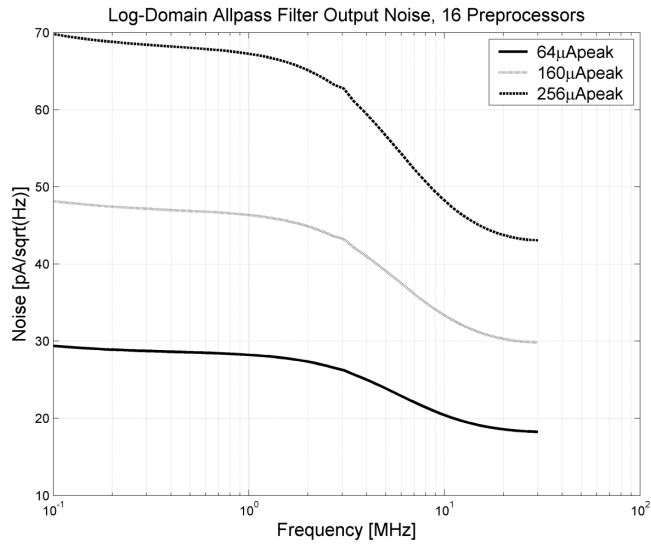


Figure 9.18: Output noise with 16 preconditioning circuits connected to the input, $I_{IN_PEAK} = 64\mu\text{A}_{PEAK}$, $160\mu\text{A}_{PEAK}$ and $256\mu\text{A}_{PEAK}$

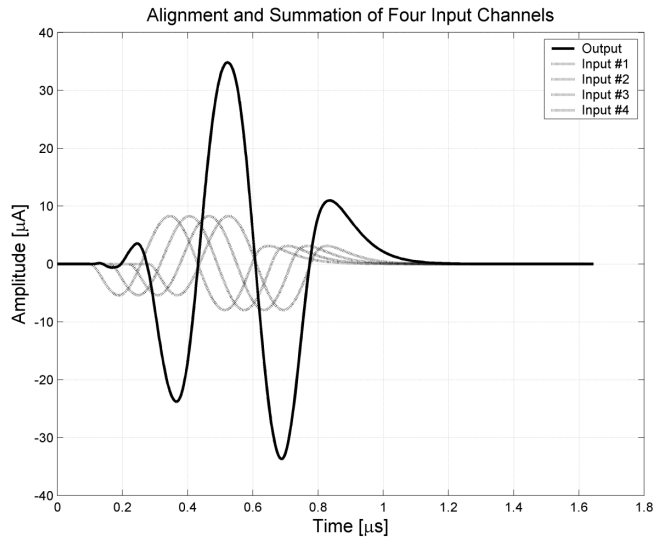


Figure 9.19: Operating the beamformer: four out-of-phase input channels are delayed and added

Table 9.4: Simulation results of the log-domain allpass filter with sixteen preconditioners, $V_{DD}=2.5V$, $I_{TUNE}=40\mu A$, The fundamental frequency was 3MHz

$I_{IN} [\mu A_{PEAK}]$	4*16 = 64	10*16 = 160	16*16 = 256
$I_{DD(QUIESCENT)} [mA]$	0.83		
$P_{D(QUIESCENT)} [mW]$	2.08		
$I_{DD(AVERAGE)} [mA]$	0.89	1.13	1.40
$P_{D(AVERAGE)} [mW]$	2.22	2.82	3.50
$A_I [dB] @ 3MHz$	0.21	0.19	0.15
GROUP DELAY [NS] @ F = 3MHz	57.3	57.3	57.3
$I_{NOISE(OUT)} [pA/\sqrt{Hz}]$ ¹⁾	26.1	42.1	60.5
SNR [dB] (BW=20MHz)	51.8	55.6	56.5
Global dynamic range [dB] (BW=20MHz)	51.8	59.7	63.8
Third harmonic distortion [dB]	-52.3	-44.9	-44.9
¹⁾ $I_{NOISE(OUT)}$ with a very small input signal was $\sim 26.0pA/\sqrt{Hz}$			

in Figure 72. A summary of the performance is listed in Table 9.5.

Table 9.5: Simulation results of the 4 channel, 4 delay-cell, log-domain μ beamformer. $V_{DD}=2.5V$, $I_{TUNE}=40\mu A$, The fundamental frequency was 3MHz

I_{IN} [μA_{PEAK}]	2	8
I_{OUT} [μA_{PEAK}]	8	32
$I_{DD(QUIESCENT)}$ [mA]	1.17	
$P_{D(QUIESCENT)}$ [mW]	2.93	
$I_{DD(AVERAGE)}$ [mA]	1.18	1.26
$P_{D(AVERAGE)}$ [mW]	2.95	3.15
$I_{NOISE(OUT)}$ [pA/ \sqrt{Hz}] ¹⁾	15.8	19.0
SNR [dB] (BW=20MHz)	38.1	48.5
Global dynamic range [dB]	38.0	50.1
¹⁾ $I_{NOISE(OUT)}$ with a very small input signal was $\sim 15pA/\sqrt{Hz}$		

Due to the strongly signal dependant noise level, a PSS/PNOISE analysis was carried out to calculate the dynamic range. The output noise level is plotted in Figure 9.20. At 3MHz, the output noise is $15.8pA/\sqrt{Hz}$ and $19.0pA/\sqrt{Hz}$ for signal amplitudes of $2\mu A_{PEAK}$ and $8\mu A_{PEAK}$ respectively. The output SNR is $38.1dB$ and $48.5dB$ respectively for a bandwidth of 20MHz.

9.5 Conclusion

A fully differential, class AB, log domain micro-beamformer has been designed. The demonstrated micro-beamformer consists of threecascaded delay cells and four input signals. All inputs can be connected to an arbitrary delay tap on the delay-line with the help of a cross-point matrix. The global dynamic range at the output of the delay-line is found to more than $50dB$ at a power consumption of $3.2mW$. Class AB, log-domain filters is found to be well suited for medical ultrasound applications due to the fact that the received signal amplitude in an ultrasound system is low during a major

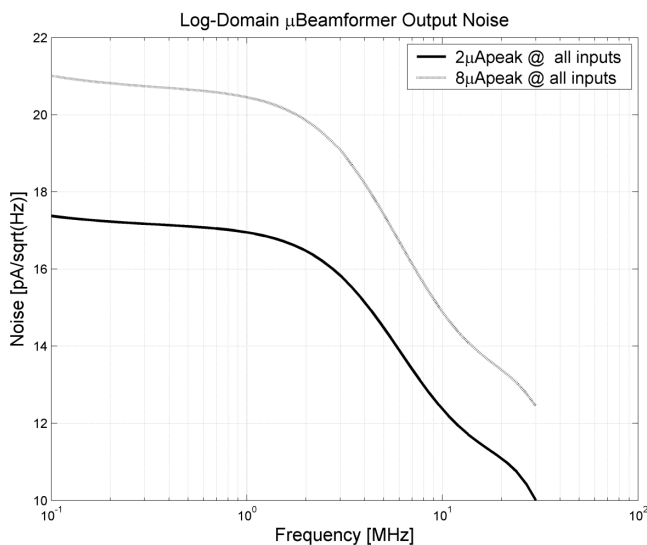


Figure 9.20: Signal dependent beamformer output noise

part of the reception period.

9.6 Acknowledgment

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Chapter 10

Paper G

SCREAM - A Discrete Time μ Beamformer for CMUT Arrays

- Behavioral Simulations Using SystemC

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The Netherlands, 18-21 September 2005

10.1 Abstract

We demonstrate an extremely efficient simulation framework to model a discrete time micro-beamformer system. Functional operation is verified and the performance limitation due to jitter and gain-mismatch is highlighted. We construct the framework using the systemC class library and simulation kernel. SystemC is an extension to C++ that enables verification of hardware designs. A unique analog extension class is added to the systemC core. This class is known as AEC and allows modeling of mixed-signal behavior. The goal of systemC is to take advantage of the high execution speed that results from compiled code and then use this to generate an executable specification.

Index Terms—Analog front-end, CMUT, low power, mixed-signal simulation, micro-beamforming, SystemC.

10.2 Introduction

It is believed that more than 80% of sudden heart attacks are caused by rupture of vulnerable plaques leading to the formation of blood clots and subsequent coronary stenosis and infarction. Techniques which could distinguish between plaques of different kind is therefore of great interest. This paper describes system level analysis of an intravascular ultrasound imaging system using SystemC. SystemC is a C++ extension library offering features like structural description, concurrency, communication and synchronization and is perfect for discrete time analysis. The imaging system described is constructed using CMUTs for signal sources, [1], and clocked mixed-signal microelectronics to realize the active modules. The sampling frequency is 120MHz and the signal center-frequency is 30MHz . To be able to construct an array imager, some signal processing must be carried out as early as possible in the signal chain. A module capable of doing this is referred to as a μ beamformer. The μ beamformer must reduce the number of signals without losing information. A direct beamformer implementation adds up a number of signal channels, each having an individual, programmable and dynamically updatable delay. This operation can be done both in the analog and in the digital domain. Digital beamforming offers much higher flexibility than the analog counterpart. Analog signal processing is far more power efficient due to the fact that one can avoid high speed, high dynamic range analog-to-digital converters. Analysis of

analog sub-systems is traditionally carried out in SPICE. When the number of transistors exceeds several thousands the simulation time increases dramatically. A system as described above will contain several tens-of-thousands discrete circuit elements. Architecture-level SPICE simulations become very time consuming. SystemC offers a much better framework to simulate such a system by using compiled code. Simulation time is strongly reduced. A discrete time μ beamformer using a ring buffer of capacitors to sample and hold the information constructs the core of the system, [2]. This is an extremely power efficient way of temporarily storing a history of the analog signals. The presented architecture assumes a source bank of 16 CMUT elements in each μ beamformer. Based upon beam-steering-angle and focus a channel dependent delay is calculated. Each pre-amplifier is connected to a capacitive ring-buffer. All ring-buffers are connected and added to a common, clocked, low-input impedance amplifier. Read out from the ring-buffers is controlled by the desired steering-angle and focus. The system level analysis demonstrates functionality and estimates chip area. We demonstrate the effects of mismatch and jitter by using the simulation framework.

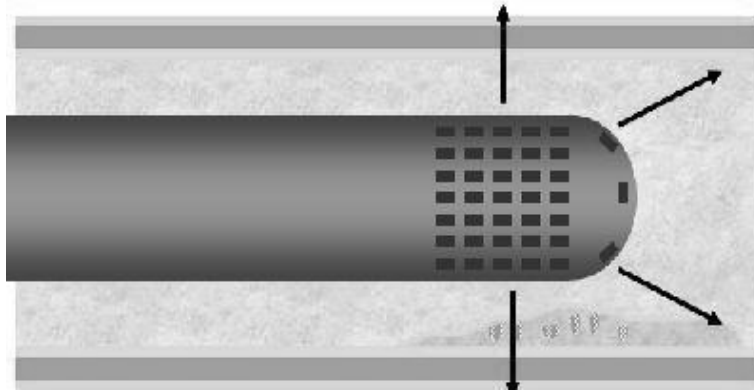


Figure 10.1: The CMUT array located in the tip of a catheter

10.3 System Overview

The imaging system described and specified by our systemC framework will be placed in the tip of a catheter as shown in Figure 10.1. The active aperture of our imaging system is rectangular with a major axis of $1.29mm$

and a minor axis of $0.89mm$. The CMUT elements have a dimension of $25\mu m \times 25\mu m$, [1]. The aperture will consist of 43×29 elements. The signal processing carried out on a sub-group of CMUT elements is described by (10.1).

$$x_{BF}(t) = \sum_{i=1}^M w_i x_i(t - t_i) \tag{10.1}$$

In this equation, i is the input channel, M is the total number of channels to be processed, w_i is a channel specific weight used for apodization, x_i is the input signal and t_i is a channel specific delay. We show a generic implementation of equation (10.1) in Figure 10.2, [2]. The channel specific weight, w_i , is controlled by the preamplifiers while the channel specific delay, t_i , is controlled by the number of capacitors and the sampling frequency.

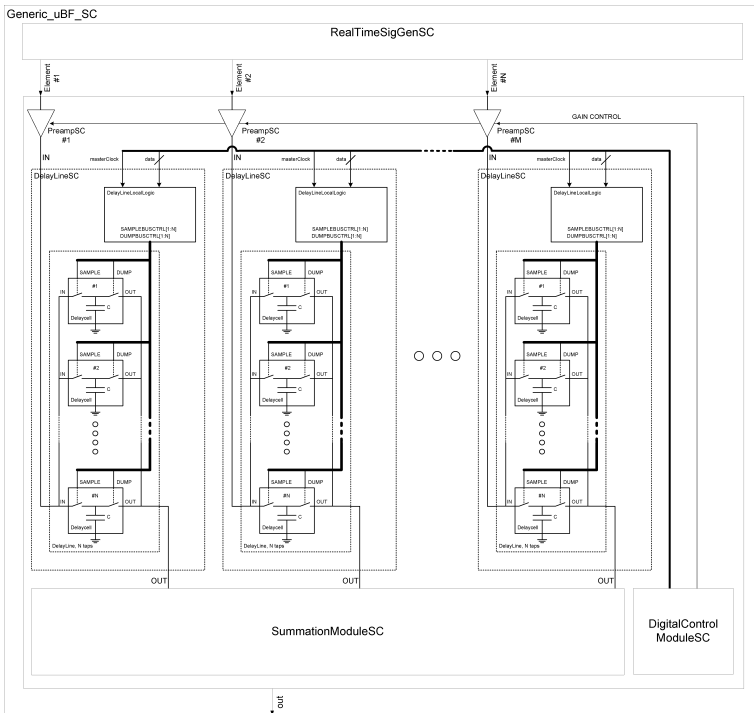


Figure 10.2: A generic discrete μ beamformer architecture

10.4 Overview of the SystemC Simulation Framework

Several approaches for mixed signal analysis is commercially available. A mixed-signal chip was simulated in [3] by adding an analog extension to the Verilog framework. A similar approach using VHDL was demonstrated in [4]. Both approaches are flexible and effective, though costly. The C programming language was used in [5] to reduce cost. Several different C compilers are freely available. The code is also very efficient with respect to execution time because of the compiled code. The goal of the systemC approach is to use the best from the approaches mentioned above. An overview of the systemC environment is drawn in Figure 10.3. Basic systemC as it is available from the <http://www.systemc.org> does not handle mixed-signal analysis, [6]. To handle this, an analog extension class known as AEC has been developed by a group at the Norwegian University of Science and Technology, [7].

AEC adds necessary analog functionality. The AEC class has been used extensively in the design of the ubeamformer framework demonstrated here.

10.5 Designing a Simple Delay-Cell Using SystemC

A very important building block in any beamformer is the delay element. In the architecture described in this paper, a capacitor is used to sample and hold the signal. The holding phase effectively implements delay. The method is shown in Figure 10.4. The amount of delay is given by the difference in number of clock cycles between the activation of the sampling pin and the dump pin. The number of capacitors connected together forming a ring buffer controls the maximum delay.

A very simple SystemC model of the delay-cell is listed Table 10.1. We tell the systemC core that we want the DelayCellSC class to behave as a systemC module by letting the class inherit properties from the `sc_module` class. Ports for communication with other modules are defined by `sc_in` and `sc_port`. Data-types from the analog-extension class have been used to define the analog input and output ports. The DelayCellSC object will be activated every time a positive transition occurs on the *sample* or *dump* input.

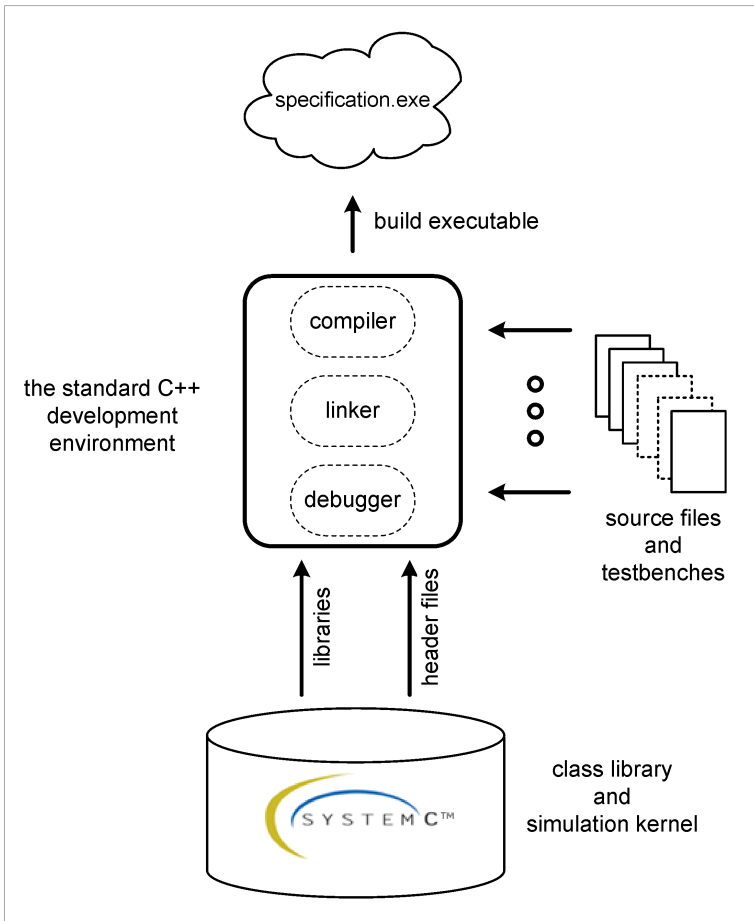


Figure 10.3: – The systemC environment

Table 10.1: Delay-cell implementation in SystemC

```
#include <stdio.h>
#include <systemc.h>
#include <aec.h>
class DelayCellSC : public sc_module
{
public:
sc_in<bool> sample;
sc_in<bool> dump;
sc_port< aec_analog_in<aec_voltage> > IN;
sc_port< aec_analog_out<aec_voltage> > OUT;
SC_CTOR(DelayCellSC)
{
SC_METHOD(SampleInput);
sensitive_pos << sample;
dont_initialize();
SC_METHOD(DumpCapValue)
sensitive_pos << dump;
dont_initialize();
}
void SampleInput() { IN->read(&_value); }
void DumpCapValue() { OUT->write(_value); }
private:
aec_voltage _value;
};
```

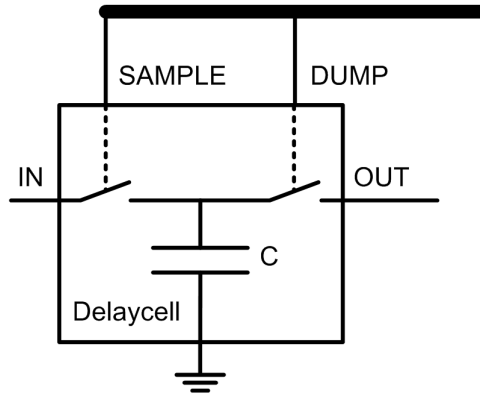


Figure 10.4: - The delay-cell used in the modeled μ beamformer

10.6 Functional Behavior

We simulated a μ beamformer having 16 inputs. Each signal from the source was given an incremental delay of $10ns$ starting at $0ns$ and ending at $150ns$. This is visualized in the upper part of Figure 10.5. We configured the μ beamformer to re-align the signals and add them together. Gain in the preamplifier is increasing from $-26dB$ to $+14dB$ over a period of $1\mu s$. The amplitude of the input signals was incremented $1mV/channel$ starting at $20mV_{PEAK}$ and ending at $35mV_{PEAK}$. The output amplitude is expected to be $(16 * 20mV_{PEAK} + 8 * 15mV_{PEAK}) = 2.2V_{PEAK}$. We assumed perfect channel match and clock-jitter equal to zero for this simulation. Result from the simulation is plotted in the lower part of Figure 10.5.

10.7 Analysis of Non-idealities

One of the main reasons for using SystemC in the analysis of large systems is to in a very effective way, predict the effect of non-idealities and to check that the system specification is possible to design.

10.7.1 Jitter and Gain Mismatch Analysis

Clock jitter is an uncertainty in the instants of clock edges. Jitter in clocks arises mainly due to the non-idealities such as phase noise in the case of

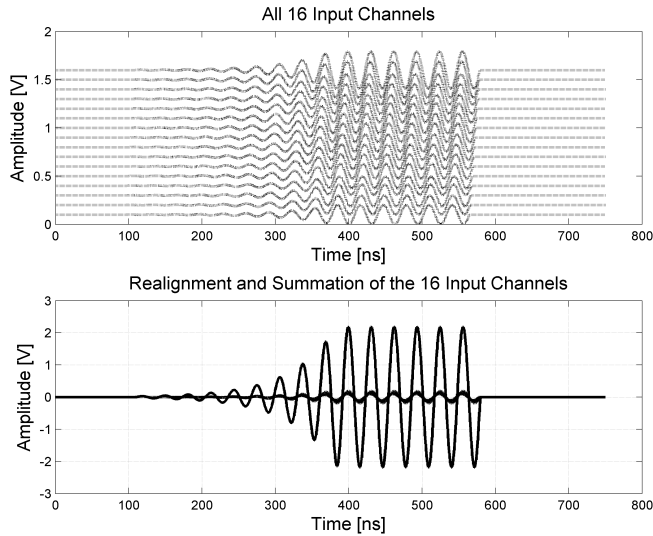


Figure 10.5: - Beamforming of 16 input channels. Upper plot: all input signals. A small offset has been added to better visualize the delay. Lower plot: Each individual delay-line output signal and the output of the beamformer

on-chip oscillators and device noise [8]. Clock jitter is one of the limiting factors for accuracy and speed in the applications that require clock [8]. Applications that use the clock such as sampling circuits and A/D converters demand a clock with perfect rising and falling edges without any jitter. Jitter in the clocks is an undesirable quantity and it causes errors in the sampled signals. For example, in the case of voltage sampling, error due to the jitter, δt_0 , for the instantaneous voltage of the sine wave $A_v \sin(2\pi ft)$ is given by [9]:

$$\sqrt{2} \cdot \pi \cdot f \cdot A_V \cdot \delta t_0 \quad (10.2)$$

The corresponding SNR is given by:

$$SNR = -20 \log(2 \cdot \pi \cdot f \cdot \delta t_0) \quad (10.3)$$

One way to reduce the impact of jitter is to use crystal-based clocks. Such clocks possess the lowest jitter. The impact of clock jitter on system level performance of the discrete time micro-beamformer is studied. To better visualize the effect, a clock jitter of $1ns$ was turned on at $t=150ns$. The output from the simulator is plotted in Figure 10.6. A very useful feature

that comes with the designed simulation model is the ability to turn on and off the different non-idealities during simulation.

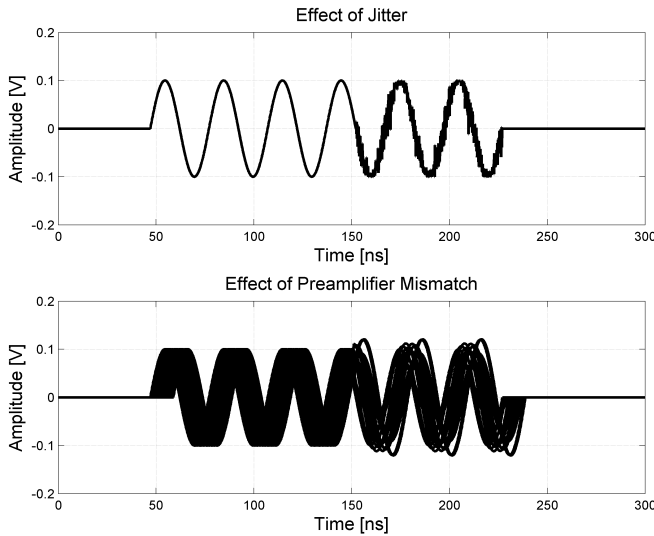


Figure 10.6: Analysis of non-idealities. Upper plot: the effect of jitter. Lower Plot: the effect of gain mismatch in the preamplifier

To save power, each preamplifier must draw as low current as possible. This will lead to limited open-loop gain. Limited open-loop-gain leads to a variation in the absolute gain. The channel-to-channel variation was analyzed using the designed framework. Gain mismatch was turned on at $t=150ns$. The output is shown in the lower part of Figure 10.6.

10.8 Conclusion

We have constructed a very effective simulation framework to be used in the evaluation of different μ beamformer architectures. The framework is very fast and flexible and generates an executable requirement specification. This increases the probability that the specified system is possible to construct.

10.9 Acknowledgment

The authors would like to thank the Norwegian Research Council through the project ASICs for Microsystems (project number 133952/420) Smart

Microsystems for Diagnostic Imaging in Medicine (159559/130) for the financial help.

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Chapter 11

Conclusion

We have focused on design of analog, low-power modules for medical ultrasound imaging in the research presented in this thesis. First we looked at delay-cells realized from log-domain allpass filters. Then we focused on low-noise, variable-gain amplifiers.

11.1 Log-Domain Allpass Filters

When we started to design log-domain delay cells as described in paper A, B and C, our hope was that this could lead to very power efficient, high dynamic range implementations of a delay line. The main limitation in the way we use the log-domain allpass filter in this thesis is the severe deterioration of noise figure when several cells are connected in series. This topology is not well suited for high performance imaging systems. Because of the inefficient use of the delay-cell, a prototype was never built. Another concern is the effect of signal-dependant noise on image quality.

Future work should focus on

- finding alternative ways of using allpass-filters to construct delay-lines
- analyzing the effect of signal-dependent noise on image quality
- increase dynamic range of the pre-processors

11.2 Low-Noise, Time-Gain Compensated Amplifiers

When designing amplifiers intended used in next generation medical ultrasound systems, the major challenge is to keep very low power-consumption at the same time as sensitivity and dynamic range is maximized. A single stage cascade-amplifier connected in a charge sensitive, negative-feedback configuration results in a very low-power, high performance solution. The problem is to add continuous, variable gain to the high performance circuit without compromising performance.

In this thesis, we've proposed a systematic method that enables continuous gain control of any fixed-gain amplifier. The method is based on adding active feedback to the fixed feedback network. The active feedback must be compatible with the amplifier impedance levels. For a trans-impedance amplifier, this means adding an adjustable trans-conductance stage in the feedback loop.

The first circuit implementation presented in this thesis adds $12dB$ gain adjustment to a $26dB$ fixed gain amplifier at the cost of $250\mu W$. Performance of the fixed gain amplifier is close to unaffected by the added circuitry. Dynamic range is also constant when moving from minimum to maximum gain. The amplifier has the lowest reported power consumption of the amplifiers studied in the literature review.

The biggest challenge with the design is gain variation due to process. A similar design utilizing the proposed method has been in full production for years. Out of over eight million amplifiers produces, minimum gain is reported to vary between $14dB$ and $18dB$. A way to tune the trans-conductance cell must be implemented to better predict absolute gain. Tuning by adjustment of bias-current should be avoided to affect overall power consumption.

Another weakness of the circuit is the relatively low gain-adjustment range of $12dB$. This is somewhat low for medical ultrasound applications. Instantaneous dynamic range of $58dB$ at the cost of $450\mu W$ is also not very impressive and should be increased in future design.

In short, future work should focus on

- Stabilization of gain versus process variation
- Increasing the absolute gain control range

- Increasing instantaneous dynamic range while keeping power consumption
- Keeping noise floor constant utilizing dynamic biasing

When we designed the second LNA presented in this thesis, the goal was to increase gain range by introducing positive feedback to the active feedback network. The goal was to have a more linear relationship between added power consumption and gain compensation. We were relatively successful on this. We were able to reach a compensation range of $15dB$ at the expense of $1.1mW$. Every $100mW$ of added power consumption resulted in approximately $1.5dB$ gain compensation. Overall power-consumption is much higher than in the first design. Though, our main goal was to prove the concept of positive feedback in the active feedback network.

Sensitivity to process variation is the same for the second design.

Future work should focus on

- Stabilization of gain versus process variation
- Reduce power consumption
- Design gm-cell with higher input range
- Design low-power, more efficient summation stage

Chapter 12

Appendix A – Comments to Paper C

12.1 Calculation of Input and Output Impedances

Input impedance and output impedance are also easily found from fundamental mesh or nodal analysis. The expressions are derived here to better identify a way to introduce gain control to the fixed gain amplifier. For sake of experiment we have utilized Blackman's impedance formula as described by Rosenstark in [15] and originally proposed by Blackman in [16]:

$$Z_{AB} = Z_{AB}^0 \frac{(1 + T_{SC_AB})}{(1 + T_{OC_AB})} \quad (12.1)$$

In (12.1) Z_{AB} is the impedance between the nodes A and B in a negative feedback-circuit, Z_{AB}^0 is the impedance between the same two nodes with the controlled source set to zero (here this means setting $A(s)$ to zero), T_{SC_AB} is the return ratio referred to the controlled source with A node short circuited to B node. Finally T_{OC_AB} is the return ratio referred to the controlled source with an open circuit between A and B node. The different intermediate expressions together with the final expression for input impedance and output impedance are listed below. The source impedance, including the coupling capacitor C_{IN} , is not included in the equations to emphasize the fact that we're designing a trans-impedance amplifier.

$$Z_{IN}^0 = Z_i || (Z_{FB} + Z_{OUT}) \quad (12.2)$$

$$T_{SC_IN} = 0 \quad (12.3)$$

$$T_{OC_IN} = A(s) \frac{Z_i}{Z_i + Z_{FB} + Z_{OUT}} \quad (12.4)$$

$$Z_{IN} = \frac{Z_i \cdot (Z_{FB} + Z_{OUT})}{Z_i + Z_{FB} + Z_{OUT} + A(s) \cdot Z_i} \quad (12.5)$$

$$Z_{IN}|_{Z_i \rightarrow \infty} = \frac{Z_{FB} + Z_{OUT}}{1 + A(s)} \quad (12.6)$$

$$Z_{OUT}^0 = Z_{OUT} || (Z_{FB} + Z_{IN}) \quad (12.7)$$

$$T_{SC_IN} = 0 \quad (12.8)$$

$$T_{OC_IN} = A(s) \frac{Z_i}{Z_i + Z_{FB} + Z_{OUT}} \quad (12.9)$$

$$Z_{OUT} = \frac{Z_{OUT} \cdot (Z_{FB} + Z_i)}{Z_{OUT} + Z_{FB} + Z_i + A(s) \cdot Z_i} \quad (12.10)$$

$$Z_{OUT}|_{Z_i \rightarrow \infty} = \frac{Z_{OUT}}{1 + A(s)} \quad (12.11)$$

In the real implementation the reduction in output impedance is somewhat limited because the assumption that Z_i goes to infinity does not hold. Keep in mind that this impedance is the parallel connection of the amplifier intrinsic input impedance (the impedance seen looking into the gate of the main stage) and the source impedance. Source impedance will in a typical application be several kilo-ohms. Because of this a separate, inherently low-output impedance common drain stage was added at the output of the core amplifier, see Q_4 and Q_5 in Figure 21.

12.1.1 Signal Polarity of Voltages and Currents

Getting the polarities in the different sub-circuits right is a challenge. A comment is required to better understand the interconnection between the modules and the usage of positive / negative input nodes. This is given in the section below.

Original Design

The first continuous gain controlled LNA was based upon the idea of trying to steal the current flowing into the impedance element connected between signal source and the virtual ground node of the LNA. The current flow-

ing in the gain control circuit must therefore have the same phase as the current in the fixed feedback loop. When the current flowing into the coupling capacitor on the input is increasing, the current flowing into CC in Figure 6.12 from the virtual ground node must be increasing. If so, signal is effectively stolen and less current is flowing to the output node to produce voltage swing. Electrically this means that the equivalent feedback capacitor is larger. In the original design in Figure 6.12, the output goes negative when a current is pushed into the fixed feedback network from the virtual ground node. To be able to do gain compensation, a negative voltage swing must therefore sink, not source, current in the gm-cell. This is achieved by connecting the LNA output node to the positive control node of the trans-conductor.

Design with Positive Feedback

In the new design, the same rule applies: when the LNA output node goes negative, the gm-cell must sink current. To sink current, the positive input of the gm-cell must go negative. For the gm-cell positive input node to go negative, current must be pushed from the virtual ground node of the summation amplifier into the resistive feedback. This current is the sum of the current flowing from the extra output of the core LNA and the extra output of the gm-cell. Both sub-circuits should source current to the summation amplifier. Sourcing current in a time period when the core-LNA goes negative actually means that the current in the original output and copied output have opposite phase. This is also the case for the output of the gm-cell. Current inverter circuits must be incorporated at the extra current outputs in both the core-LNA and the gm-cell. The current-inverter circuits can be seen as Q₇-Q₁₂ in Figure 21. Signal polarities are inverted using current mirrors. To avoid AC coupling, the bias current is removed by subtraction.

Chapter 13

Appendix B – On Fundamental Log-Domain Theory

This section contains comments to the log-domain circuits used in paper D, E and F. The fundamental theory necessary to construct a log-domain integrator is presented. The details explained below makes it easier to understand the circuits and concepts presented in paper D, E and F.

13.1 Basic Principle of Log-Domain Filters

Log-domain signal processing is based on the idea of doing internal non-linear but external linear filtering utilizing non-linear building blocks. The concept is shown in Figure 13.1.

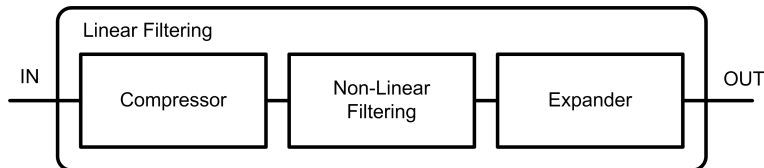


Figure 13.1: Principle of log-domain filtering

It is believed that overall power consumption is reduced because energy is not dissipated on linearizing non-linear devices. The main building block in most published log-domain filters is the bipolar transistor or MOSFETs

operating in weak inversion. This is because of their exponential relationship between current and voltage. For more details about log-domain integrators and filters, see [1], [2] and [3].

13.1.1 Building the Log-Domain Integrator

A current mode integrator is described by (13.1) and (13.2).

$$i_{out} = \frac{1}{\tau} \int i_{in} \cdot dt \quad (13.1)$$

$$\frac{di_{out}}{dt} = \frac{1}{\tau} i_{in} \quad (13.2)$$

In (13.1) and (13.2) i_{out} is the output current, i_{in} is the input current and τ is the time-constant of the integrator. We assume the expander to be a continuous, strictly monotonic function. Output current from the expander is given by (13.3).

$$i_{out} = f(v) \quad (13.3)$$

The two quantities i_{out} and $f(v)$ can be found in the right part of Figure 13.2. Here, the trans-conductor represents the expander. An internal, compressed voltage, v , is expanded according to a function $f(v)$ into the output signal, i_{out} . The derivative of (13.3) with respect to time is shown in (13.4).

$$\frac{di_{out}}{dt} = f'(v) \cdot \frac{dv}{dt} \quad (13.4)$$

Using a capacitor, C , to do integration, the current flowing into the device is given by (13.5).

$$i_C = C \frac{dv}{dt} \quad (13.5)$$

To express the integration-current, i_C , as a function of the output-current, (13.4) is inserted in (13.5). The result is shown in (13.6).

$$i_C = C \frac{di_{out}}{dt} \cdot \frac{1}{f'(v)} \quad (13.6)$$

Equation (13.2) is next inserted into (13.6) leading to (13.7).

$$i_C = \frac{C}{\tau} \cdot i_{in} \cdot \frac{1}{f'(v)} \quad (13.7)$$

An implementation of the integrator described above is shown in Figure 13.2. This figure does not assume any specific compression / expansion function-pair.

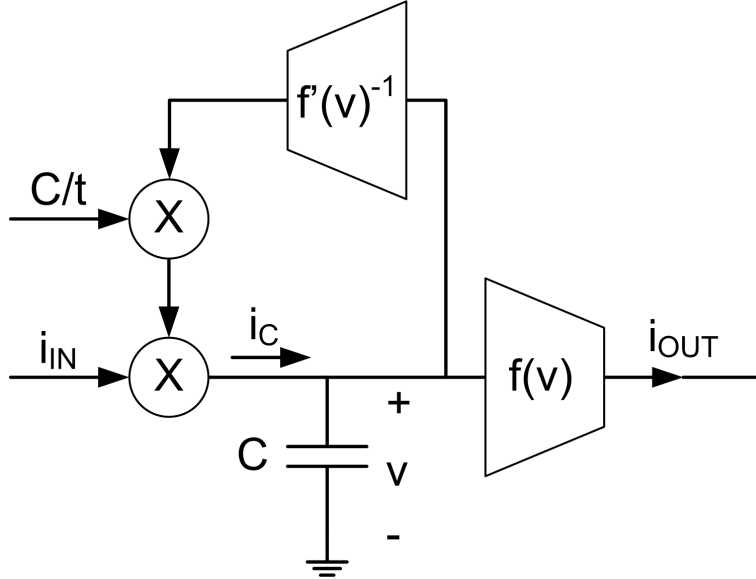


Figure 13.2: Block-diagram of the log-domain integrator

Next, we assume compression and expansion to be realized using bipolar transistors. Collector-current, i_{out} , versus base-emitter voltage, v , in the bipolar transistor is given by (13.8).

$$i_{out} = I_S \cdot \left[\exp\left(\frac{v}{V_T}\right) - 1 \right] \cong I_S \cdot \exp\left(\frac{v}{V_T}\right) \quad (13.8)$$

In (13.8), I_S is the saturation current and V_T is the thermal voltage. The derivate of current with respect to voltage is shown in (13.9). This expression is equal to $f'(v)$.

$$f'(v) = \frac{di_{out}}{dv} = \frac{I_S}{V_T} \cdot \exp\left(\frac{v}{V_T}\right) = \frac{i_{out}}{V_T} \quad (13.9)$$

If we insert (13.9) into (13.7) we get an expression connecting the input- and the output signal.

$$i_C = \frac{C}{\tau} \cdot i_{in} \cdot \frac{V_T}{i_{out}} = I_0 \frac{i_{in}}{i_{out}} \quad (13.10)$$

In equation (13.10), I_0 is a constant equal to $C * V_T / \tau$.

Expression (13.10) is easily implemented using a trans-linear loop. A damped integrator is realized by adding a fixed current, I_{DAMP} to the (13.10).

$$(i_C + I_{DAMP}) = I_0 \frac{i_{in}}{i_{out}} \quad (13.11)$$

Implementation of (13.10) is relatively straight-forward utilizing trans-linear circuit theory. Circuit implementation is found in paper D, E and F.

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Chapter 14

Appendix C – Facsimile from Aftenposten

Visste du at ...
... Norge vil mangle mellom 5000 og 15000 ingeniører i 2010, ifølge SSB og Kunnskapsdepartementet?

Visste du at ...
... fagbokhandelen på Kongsberg er datterselskap av Akademika-bokhandelen ved Universitetet i Oslo, og garanterer at de har laveste pris?

ultralyd



Thomas Halvorsrød tar doktorgrad på 3D-ultralyd. Når den er levert fortsetter han i jobb hos GE Vingmed Ultrasound i Horten, som er blant verdens største leverandører innen ultralydutstyr.

Doktorgrad ga drømmejobb

Tekst: Jorunn Nilssen ✳ Foto: T. Busch-Christensen

Thomas Halvorsrøds doktorgrad er med på å gjøre ULTRA-LYD-BILDER STADIG TYDELIGERE. Selv mener han at studiene har ledet ham til drømmejobben.

– Å forske på noe som kan redde liv er utrolig givende, sier doktorgradsstipendiat Thomas Halvorsrød fornøyd.

Til våren leverer han doktorgraden som tar for seg en del av elektronikken som må til for å se 3D-bilder ved ultralydundersøkelser. 3D-ultralyd gir helsepersonell bedre mulighet til å se hva som foregår inni kroppen til en pasient.

Sikkert jobb

I begynnelsen av 90-tallet startet Halvorsrød utdanningsløpet ved Høgskolen i Vestfold (HVE).

Allerede er han på plass hos sin fremtidige arbeidsgiver GE Vingmed Ultrasound i Horten, som han også var ansatt hos før doktorgraden. Selskapet er blant verdens største leverandører av ultralydutstyr til brukere innefor de fleste medisinske fagområder. Selskapet ligger helt i front når det gjelder utviklingen innenfor tre- og

firedimensjonal ultralyd. Arbeidet Halvorsrød har lagt ned i forbindelse med sin doktorgrad, er en del av denne utviklingen.

Interessert i ultralyd

– Allerede som ingeniørstudent bestemte jeg meg for å jobbe ett år før jeg eventuelt gikk i gang med sivilingeniørstudiet, forteller Halvorsrød. Han mener at det var med på å motivere ham til å gå i gang med sivilingeniørgraden ved NTNU i Trondheim. Den gang var det ikke muligheter for å ta hele graden ved HVE – det er det imidlertid i dag.

I studietiden fikk Halvorsrød høre om GE Vingmed Ultrasound. Han syntes ultralyd virket spennende, og gjorde iverdige forsøk på å få sommerjobb i bedriften.

– Det ordnet seg, og jeg ble fort hektet på elektronikk i forbindelse med ultralyd. Bedriften var interessert i at jeg brukte dem som case i forbindelse med den av-

sluttende diplomoppgaven. Dermed kom vi fram til et samarbeid som begge var fornøyd med, forteller han.

Etter et par år i jobb hos GE Vingmed Ultrasound ville Thomas Halvorsrød lære mer.

– Jeg hadde lyst til å fordype meg i elektronikken som gjør det mulig å få tredimensjonale bilder. Derfor undersøkte jeg muligheten for å ta en doktorgrad, forteller han. Snart bar det tilbake til NTNU som doktorgradsstipendiat.

Doktorgraden bygger videre på utviklingen av produkter hos GE Vingmed Ultrasound.

Halvorsrød mener en doktorgrad er en glimrende mulighet for å studere noe nytt. Som igjen gir muligheter for en spennende jobb.

– Gode karakterer må til, samtidig som det er veldig viktig å være motivert for å løse oppgaven, slår han fast. ■

Spansk kjemi-prisvinner valgte Porsgrunn

●● For spanske Marta Dueñas Díez (30) ga halvåret som utvekslingsstudent ved Høgskolen i Telemark mersmak. To år senere var hun tilbake som doktorgradsstipendiat. For doktorgraden som Marta Dueñas Díez tok ved Høgskolen i Telemark (HIT) mottok hun en forskerpris av organisasjonen European Federation of Chemical Engineering.

– Det var utrolig gøy å få en pris for arbeidet jeg la ned, smiler spanske Dueñas Díez, som nå jobber som forsker ved Hydro olje og energi i Porsgrunn.

Valgte Porsgrunn

Dueñas Díez studerte kjemiteknikk ved universitetet i hjembyen Valladolid i Spania. Høsten 1998 bod muligheten for et utvekslingssemester seg, og hun valgte å dra til HIT.



Spanske Marta Dueñas Díez kunne velge mellom fem jobber etter endt utdanning ved HIT.

– Semesteret var helt topp. Jeg ble tatt veldig godt i mot i Porsgrunn og trives fra første stund – selv om det var få andre utvekslingsstudenter der samtidig med meg, sier hun. Kontakten mellom lærere og studenter, og samarbeidet mellom høgskolen og industrien var noe hun satte særlig pris på.

– I Spania er undervisningen i større grad preget av oneiokommunikasjon, sier Dueñas Díez, som er overrasket over at ikke flere jenter velger ingeniørutdanning i Norge.

– Utdanningen passer like godt for jenter som gutter, påpeker hun.

Fristet å ta doktorgrad

Etter å ha fullført mastergraden i Valladolid, som resulterte i at hun ble kåret til årets beste kjemiteknikk-student i Spania, reiste hun til Porsgrunn igjen for å ta doktorgraden.

– Jeg ble spurt om jeg var interessert i å ta doktorgrad da jeg var utvekslingsstudent, og syntes umiddelbart det høstes ut som en spennende mulighet. Det har vist seg å være en veldig riktig beslutning for meg, sier Dueñas Díez.

Doktorgraden om hvordan partikler oppfører seg, avsluttet hun i 2004, og like etterpå sto jobbtilbudene i kø. Valget falt på produksjonsteknologiarbeid i Hydro.

– Foreløpig har jeg ingen planer om å flytte tilbake til Spania. Nå føler jeg meg nesten halvt norsk, ler hun.

Fleksibel ingeniørutdanning

●● Som ingeniørstudent ved Høgskolen i Telemark (HIT), Høgskolen i Buskerud (HiBu) eller Høgskolen i Vestfold (HVE) går det an å ta en pause etter bachelorgraden for en gyver løp på det toårige mastergraden som utgjør sivilingeniørstudiet. Muligheten for å avslutte studentlivsværelsen etter tre år finnes imidlertid ikke ved uni-

versitetene. Hvis man starter for eksempel en femårig sivilingeniørutdanning ved universitet og hopper av etter tre år, har man ingen grad eller tittel.

– Et opphold i arbeidslivet passer spesielt godt for dem som er usikre på hva de vil gjøre etter ingeniørstudiet. I starten av en utdanning er det ikke alltid like lett å se

for seg hele utdanningsløpet, sier dekan for teknologiske fag ved HIT, Ole Ringdal. Høgskolen opplever ofte at studentene som velger å ta seg en pause, kommer tilbake.

– Studentene synes faget er spennende, og velger å ta mastergraden. Det viser seg å være lønnsomt når studentene søker

jobber etter endt utdanning, sier Ringdal.

