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Compact Modeling of the Current through Nanoscale Double-Gate MOSFETs.

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Problem Description

The goal of this master thesis is to find a compact current model for nanoscale double-gate MOSFETs. The model should be analytical and must contain solutions for the sub-threshold, near threshold and strong inversion regimes.

Assignment given: 22. January 2009
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Preface

This thesis will describe in detail my Master project, which is part of the "Master of technology" education program at the Norwegian University of Technology and Science (NTNU) in Trondheim. The work was carried out at the University Graduate Center at Kjeller (UNIK).

An abstract including the same work has been accepted by the 2009 IEEE Regional Symposium on Micro and Nano Electronics.

I would like to thank my supervisor Tor A. Fjeldly for his guidance. Also, I would like to thank Udit Monga for guidance and help throughout the work and Dag-Martin Nilsen for many helpful discussions.

Summary

In this thesis a compact drain current model for nanoscale double-gate MOSFETs is presented. The model covers all operation regimes and bias voltages up to 0.4V.

The modeling is done using conformal mapping techniques to solve the 2D Laplace equation in sub-threshold, and using a long channel model in strong-inversion. In near threshold, a quasi-Fermi level model which uses empirical constants is used to find the current. A continuous model is found by expressing asymptotes in the sub-threshold and strong inversion regimes, and combining them using a interpolation function. The interpolation function uses a parameter that is decided analytically from the near threshold calculations.

The model shows good agreement with numerical simulations for bias voltages below 0.4V and channel lengths bellow 50nm.

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Notation and symbols

t_{ox}	Oxide (insulator) thickness
t'_{ox}	Effective oxide (insulator) thickness
ϵ_{ox}	Relative dielectric permittivity of oxide
ϵ_{si}	Relative dielectric permittivity of silicon
t_{si}	Silicon (body) thickness
L	Gate length
W	Device width
N_A	Acceptor doping density
N_C	Effective density of states in conduction band
N_V	Effective density of states in valence band
n_i	Intrinsic electron density
n	Mobile charge sheet density
ϕ_b	Fermi-intrinsic band bending
V_{bi}	Built in potential, band bending
V_{FB}	Flat band voltage
k_B	Boltzmanns constant
T	Temperature
q	Electron charge
V_{th}	Thermal voltage
χ_s	Electron affinity silicon
φ	Electrostatic potential in the body
φ_1	Mobile charge potential contribution
φ_2	Laplace potential contribution
φ_m	Potential at the top of the barrier
φ_c	Potential at the source drain symmetry line
x_m	Position of the top of the barrier
Φ_m	Gate contact work function
Φ_s	Silicon work function

V_F	Quasi-Fermi potential
V_{F0}	Quasi-Fermi potential at the center of the device.
I_{ds}	Drain to source current
V_{gs}	Gate to source voltage
V_{ds}	Drain to source voltage
I_{DD}	Drift diffusion current
m_n	Effective mass of electrons in silicon
m_p	Effective mass of holes in silicon
$\hbar$	Reduced Planc's constant
μ_n	Electron mobility

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Chapter 1

Introduction

1.1 Background

In the early 60s John Atalla and Dawon Kahng fabricated the first metal-oxide semiconductor field-effect transistors (MOSFETs), and demonstrated the first successful MOS field-effect amplifier. Since then the MOSFET has become the favorite of the electronics industry. The development of the MOSFET the last 40 years has been dramatic, and the performance of integrated circuits has had an exponential growth. The main driving force for this improvement has been the downscaling of the MOSFET. Smaller transistors means faster transistors and more logic on a chip, which will lead to cheaper circuits, faster processing speeds and better memory capacity. In 2009 Intel expects to deliver 32nm microprocessors[1].

The single-gate MOSFET (SG-MOSFET) has been scalable down to the sub 100nm range with the help of high doping and steep doping gradients, which reduce the mobility of the carriers. However, the favorite of the industry is now reaching it's scaling limits and new devices will be needed if the transistor is to be scaled further. Such a device will have to be fabricated with comparable cost and yield to that of the SG-MOSFET. The double-gate MOSFET (DG-MOSFET) is one of the most promising candidates. One advantage of the DG-MOSFET is that it makes it possible to achieve high gate control by using a fully depleted body with low doping. This will lead to a higher mobility for the carriers. The electrostatics of the DG will however lead to a two dimensional problem, which means that new device models will be needed as it's not possible to continue the patchwork of the SG models. The double-gate case will also be different because the threshold voltage will not be defined in the same manner for the DG-MOSFET as for the SG-MOSFET.

1.2 Integrated Circuit Design

Integrated circuits, also called "chips", are electronic circuits where all the components have been manufactured on a thin slice of semiconductor material, called a wafer. With very large scale integration (VLSI) 200 million transistors can be placed on one cm^2. An integrated circuit can contain both digital and analog functions on the same chip. Since Complementary metal-oxicide semiconductor (CMOS) technology can provide high density and low power dissipation for the digital part, and a good mix of components for the analog part it has become the most common technology used in integrated circuits.

1.3 Device Simulation

In this work the numerical device simulator Atlas from Silvaco has been used to verify the accuracy of the proposed models. Atlas has been used since experimental data haven't been available. Numerical device simulators are technology computer aided design (TCAD) tools, which usually simulate devices by iterations over Poisson's equation with a transport model for a given set of boundary conditions. This is usually done by discretizing the 2D surface or 3D volume with a grid and iterate over this with a partial differential equation (PDE) solver. The convergence time and accuracy of the solution depend strongly on the grid distribution and size, as more points will give better accuracy and require more time. The convergence time will also depend on the carriers statistics, solver type and current continuity. Numerical solvers are usually not used to simulate circuits, as the models are too complex and will require too much computer power.

1.4 Circuit Simulation

Because of the high cost of Integrated circuit fabrication, it is very important that the circuits can be simulated accurately before fabrication. Mistakes in the integrated circuit would be very costly. The circuit must therefore be verified with a circuit simulation tool. The industry standard simulation tool is called SPICE (Simulation Program with Integrated Circuit Emphasis). The key element in SPICE is the device models, and a large variety of models and modeling approaches are developed at different research groups. This ensures the development and quality of SPICE. The BSIM MOSFET model, developed at Berkley, was the industry standard for many years, but in 2005 the Compact Model Council decided to make PSP, developed by Phillips semiconductors and Pennsylvania State University, the new industry standard. SPICE has a lot of different models with different complexity. This means that the designer has to choose what kind of model to use, whether

he wants to use a time-consuming but precise model or a faster and less accurate model.

1.5 Objective of Thesis

The objective of this work is to develop a compact short-channel DG-MOSFET model based on the framework described by Kolberg[2] and Børli[3]. The model should be analytical, not based on fitting parameters and cover short gate lengths where there are few existing models. At gate lengths above 100nm there are other models available. The main focus in the work will be on low bias voltages as these will be needed in important low power applications, and are important in devices where battery life time is an important factor.

1.6 Outline of Thesis

In this thesis a compact drain current model for nanoscale double-gate devices is presented. The model uses conformal mapping techniques to solve the Laplace equation, in order to find the 2D potential in sub-threshold. In strong inversion a long channel approximation is used in order to evaluate the current. In near threshold the quasi-Fermi level is modeled with the use of empirical constants. A continuous model, covering all regimes will be presented.

In chapter 2 existing double-gate MOSFET models are reviewed. This chapter includes short-channel models and long channel-models.

In chapter 3 basic conformal mapping theory is presented. The sub-threshold solution used in the presented model is based on this theory.

In chapter 4 the compact model is presented. This chapter is divided into 5 sections. Section 4.1 presents the device that will be considered in the work. The sub-threshold modeling, strong-inversion modeling and near threshold calculations will be presented in section 4.2, 4.3 and 4.4 respectively and in the final section, 4.5, the continuous model, which uses the modeling and calculations from section 4.2, 4.3 and 4.4, will be shown.

In chapter 5 the compact model is compared to numerical simulations.

Chapter 6 and 7 contains the discussion and conclusion respectively. Future work is discussed in the conclusion.

Chapter 2

Review of DG-MOSFET Models

This chapter gives an introduction to different DG-MOSFET models, and their strengths and weaknesses.

The potential in all DG-MOSFETs dominated by 2D electrical potential is described by Poisson's equation;

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = \frac{q}{\varepsilon_{si}}(N_a + n) \tag{2.1}$$

where q is the electron charge, ε_{si} is the permittivity of the silicon, N_a is the acceptor doping, n is the mobile charge density and $\varphi(x, y)$ is the potential referred to the Fermi potential at the source contact. Equation (2.1) is valid for a n-type device with the x-axis being the lateral direction along the gates. Using classical Boltzmann statistics the density of carriers, n, can be expressed as:

$$n = \frac{n_i^2}{N_a} exp\left[\frac{\varphi(x,y) - V_F}{V_{th}}\right] \tag{2.2}$$

where n_i is the intrinsic carrier density for undoped silicon, V_{th} is the thermal voltage and V_F is the quasi-Fermi level.

There are two main transport mechanisms used as a basis for compact modeling of drain current, drift-diffusion[4] and ballistic[5]. With drift diffusion the velocity of the carriers is limited because there will be lots of collisions between the carriers in the channel. These collisions occur because the mean free path, which is the length an electron travels on average between collisions, is much smaller than the channel length. With ballistic transport however the mean free path will be longer than the channel and no collisions will occur. In addition to these two transport mechanisms we have quasi-ballistic[6] transport which is a combination where the mean free

path is comparable to the channel length, and some electrons will suffer collisions while others will pass through without colliding. In compact modeling quasi-ballistic behavior is described as a ballistic transport with a statistical ballistic carrier scattering quotient included as a model parameter.

2.1 Long-channel Models

Long channel modeling describes approaches where the effects of the 2D field are regarded as inferior to the effect of the gates. The carriers in the channel are mostly located close to the gates and the effects from the source and drain electrodes are insignificant. This means that the 2D problem is viewed as a 1D problem and can be solved by solving the 1D Poisson's equation transversal to the channel. A transport model can be used between source and drain to calculate the current.

2.1.1 Modeling of undoped devices

Long channel models for undoped DG-MOSFETs have been presented by Taur[7] and Ortiz-Conde[8]. Both of these models are based on solving the 1D Poisson's equation in the direction transverse to the channel. All though they used different approaches it was proved that the two methods were equivalent[9]. Taur solves the problem by introducing a new parameter β and gets a model that gives total agreement with the numerical simulations for channel lengths of $L = 1\mu m$ and a thin silicon film, $t_{si} \leq 25nm$.

2.1.2 Modeling of doped devices

A 1D modeling procedure which included doping was proposed by Francis et al.[10]. This model is based on the difference between the potential at the interface between the oxide and the silicon, and the potential at the center of the device, being taken as a constant. This means that Poisson's equation can be reduced to its depletion form, taking only into account the fixed charges with:

$$\varphi_S - \varphi_0 = \frac{qN_a t_{Si}^2}{8\varepsilon_{Si}} \tag{2.3}$$

where φ_S is the potential at the interface between the oxide and the silicon and φ_0 is the potential at the center of the device ($y = t_{si}/2 + t_{ox}$). Using Gauss' law the charge can be integrated over the surface to find an expression for the current. In moderate inversion, accurate modeling of the surface potential using Taylor expansion of Poisson's equation will give:

$$\frac{d^2\varphi(y)}{dy^2} = \frac{q}{\varepsilon_{si}}(N_a + \frac{n_i^2}{N_a}exp[\varphi_S - (t_{si}/2 + y)E_S/V_{th}]) \tag{2.4}$$

Integrating equation (2.4) twice will lead to the following expression:

$$\varphi_S = C_2(\varphi_S, E_S) + V_{th}^2 \frac{q}{\varepsilon_{si}} \frac{n_s}{E_S^2} \tag{2.5}$$

where C_2 is an integration constant, n_s is the surface electron concentration, E_S is the surface fields and φ_s is the surface potential.

The current is given by:

$$I_{DD} = 2\frac{V_{ds}}{L} \int_{-t_{si}/2}^{0} q\mu n(x)dx \tag{2.6}$$

which can be solved, using iterations over equation (2.5). The mobility is considered as a constant. This model is valid for small drain-source voltages, but does not include short channel effects, such as DIBL (drain induced barrier lowering).

Another approach for finding the current through a doped DG device was presented by Baccaranis et al.[11]. This model is based on the DG device being thought of as two SG devices placed back-to-back with two inversion channels close to the gates. It is assumed that the current close to the gates far exceeds the current at the center of the device. Using the gradual channel approximation, the following equation is found:

$$I_{DD} = 2\frac{\mu}{L} \frac{C_0}{1 + \alpha_n V_{ds}} \int_0^{V_{ds}} [V_G' - \varphi_c(V)]dV \tag{2.7}$$

Here C_0 is the gate capacitance, α_n is given as $\alpha_n = \mu/v_{sat}L$ where v_{sat} is the saturation velocity, V_G' is the effective gate voltage given as $V_G' = V_{gs} - (\phi_m - \chi_s + qN_a/2C_g)$, ϕ_m is the work function of the gate metal, χ_s is the electron affinity in the silicon and $\varphi_c(V)$ is the center potential found implicitly by:

$$2C_g(V_G' - \varphi_c) = -Q_c(\varphi_c, V_F) \tag{2.8}$$

where $Q_c = -qN_C exp[(\varphi_c - V_F)/V_{th}]$, assuming boltzmann statistics.

Equation (2.8) is only correct below the drain saturation voltage, which is given by $V_{DSS} = \frac{1}{\alpha_n(\sqrt{1+2\alpha_n(V_{gs}-V_T)}-1)}$. The threshold voltage is given by:

$$V_T = \phi_m - X_s + qN_a/2C_g + V_{th} log(\frac{2C_g V_{th}}{qN_c}) \tag{2.9}$$

In weak and moderate inversion the center potential will be be pinned to the threshold voltage. This will lead to the following expression for the drain current:

$$I_{DD} = 2\frac{\mu}{L} \frac{C_0}{1 + \alpha_n V_{ds}} [(V_{GS} - V_T)V_{ds} - \frac{1}{2}V_{ds}^2] \tag{2.10}$$

and when the drain voltage exceeds the saturation voltage the following equation will give the current:

$$I_{DD} = 2\frac{\mu}{L}\frac{C_0}{1+\alpha_n V_{DSS}}[(V_{GS}-V_T)V_{DSS}-\frac{1}{2}V_{ds}^2] \tag{2.11}$$

Both of these equations are similar to the equations used for single-gate devices and in sub-threshold the current will take the same form as the standard MOSFET equations:

$$I_{DD} = 2\frac{C_0\mu}{L}V_{th}^2 exp[(V_{GS}-V_T)/V_{th}][1-exp(-V_{ds}/V_{th})] \tag{2.12}$$

2.2 Short-channel Models

Short channel devices are devices where the length/height ratio is so small that the effect of the source and drain electrodes can not be ignored. This means that the 2D electrostatics, including both the electrostatic effects of the electrodes and the space charge must be considered. In short channel devices there are short channel effects such as DIBL present.

Attempting to parameterize the 2D effects will lead to a lot of empirical adjustable parameters. In order to avoid this the problem must be solved in a more physical way.

2.2.1 Modeling of undoped/lightly doped devices

Chen et al[12] has proposed a threshold based short channel model. This model is found by solving Poisson's equation with only the mobile charge term:

$$\frac{\partial^2\varphi}{\partial x^2}+\frac{\partial^2\varphi}{\partial y^2}=\frac{q}{\varepsilon_{si}}n \tag{2.13}$$

where $n = n_i exp[(\varphi - V_F)/V_{th}]$ is the mobile charge term adjusted for the quasi-Fermi level. The mobile charge can be expressed as $n = n_i exp[\varphi/V_{th}]$, if the drop in the quasi-Fermi level is assumed to be close to the drain. This leads to the solution being independent of V_{ds} and therefore ignoring DIBL. This can be compensated for by using superposition the 1D part in the lateral direction can be found:

$$\frac{\partial^2\varphi}{\partial x^2}=\frac{q}{\varepsilon_{si}}n_i exp[\varphi_0/V_t h] \tag{2.14}$$

Using the boundary conditions $\varphi_0(-L/2) = \varphi_0(L/2) = V_{bi}$ with equation (2.14) and (2.13) the following equation is found:

$$\frac{\partial^2\varphi}{\partial x^2}+\frac{\partial^2\varphi}{\partial y^2}=\frac{q}{\varepsilon_{si}}n_i exp[\varphi_0/V_t h][exp(\varphi_1/V_{th})-1] \tag{2.15}$$

Using an assumption that the change in the x direction is given in $\varphi_0(x)$ the 2D equation can be solved using Taylor expansions.

The threshold voltage can be found as:

$$V_T = V_{FB} + \eta V_{th} \frac{cosh(\theta)}{cosh(\theta/2)} ln(Q_T/n_i t_{si}) - \varphi_{0m} \left[\frac{cosh(\theta)}{cosh(\theta/2)} \eta - 1 \right] \quad (2.16)$$

where θ and η are geometrical constants and Q_T is the inverse carrier density found from the long-channel approximation:

$$V_{T,long} = V_{FB} + V_{th} ln(Q_T/n_i t_{si}) \quad (2.17)$$

Numerical simulations or measured data are needed to find Q_T. The authors do not suggest any transport mechanism for use in the lateral direction.

2.2.2 Modeling of strongly doped devices

A strongly doped device will be more difficult to model as the carriers in the channel will lead to a second conducting channel, even in sub-threshold. Munteanu et al[13] have suggested a model which uses empirical parameters. The approach is based on a superposition of lateral and transversal parts of the electrostatic potential. This is given by:

$$\varphi(x, y) = \varphi_S(x) \times A(x, y) \quad (2.18)$$

where $\varphi_S(x)$ is the surface potential and $A(x, y)$ is an envelope function , which modulates the surface potential. The following function for the quasi-Fermi potential is used by Munteanu et al.:

$$\begin{aligned} V_F(x) =& 2V_{th} \frac{m}{n} \\ & \times ln[(exp[-V_{ds} n/V_{th} m] - 1)(x/L^{)} c/(V_{gs} - V_{FB}) + 1]^{-1} \\ & \times (a t_{si})^{V_{ds}/3c} \end{aligned} \quad (2.19)$$

Here m and n are structural parameters while a,b and c are empirical parameters. The surface potential is found by:

$$\frac{d^2 \varphi_S}{dx^2} - \frac{2C_{ox}}{\varepsilon_{si} t_{si}} \varphi_S = \frac{1}{\varepsilon_{si} t_{si}} [q N_S t_{si} - 2C_{ox}(V_{gs} - V_{FB} - \varphi_F) + q_i] \quad (2.20)$$

where q_i is the inversion charge. Evaluation of q_i leads to the following solution of equation (2.20):

$$\varphi_S(x) = C_1 exp(m_1 x) + C_2 exp(-m_1 x) - \frac{R(x)}{m_1^2} \quad (2.21)$$

C_1, C_2 and m_1 are found from geometrical and electrical properties while R(x) also consists of the inversion charge density.

Using drift-diffusion with a constant mobility the following expression for the current is found:

$$I_{DD} = \mu V_{th}[1 - exp(-V_{ds}/V_{th})] / \int_0^L \frac{dy}{\int_0^{t_{si}} qn_i exp(\varphi(x,y)/V_{th})} \tag{2.22}$$

This expression gives good results compared to numerical and experimental results at aspect ratios(length/height) above 3. when it is solved numerically.

Chapter 3

Conformal Mapping

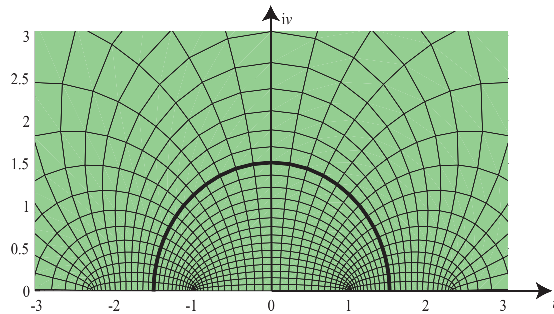

Figure 3.1: Mapping between the Z-plane and the W-plane.

Conformal mapping is a set of transformations $z = x+jy = f(w = u+jv)$ that preserve angles and directions of curves through a point in the z-plane unless $f'(z)$ is zero in this point. Conformal mapping is an important tool in engineering mathematics since problems can be solved in a simpler region than the original one.

Any polygon in the Z-plane can be transformed to the upper half of the W-plane with the Schwarz-Christoffel transformation. This is a transformation that will map the periphery of the polygon to the real axis of the W-plane and the body to the upper half of the W-plane, as shown in figure 3.1.

3.1 Conformal Mapping of DG-MOSFET

The potential in the DG-MOSFET is described by Poisson's equation;

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = \frac{q}{\varepsilon_{si}}(N_a + n) \tag{3.1}$$

where N_a is the acceptor doping, n is the mobile charge density and $\varphi(x, y)$ is the potential referred to the Fermi potential at the source contact. N_a can often be ignored for lightly doped devices, i.e. $N_a < 10^{16} cm^{-3}$.

The potential can be divided into the mobile charge contribution, φ_1, and the inter-electrone coupling contribution, φ_2. The total potential will be given by the sum of these two contributions $\varphi = \varphi_1 + \varphi_2$, and by doing this Poisson's equation, (3.1), can be separated into a laplace equation and a simplified Poisson's equation giving the inter-electrode coupling contribution and the mobile charge contribution respectively:

$$\frac{\partial^2 \varphi_2(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_2(x,y)}{\partial y^2} = 0 \tag{3.2}$$

$$\frac{\partial^2 \varphi_1(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_1(x,y)}{\partial y^2} = \frac{nq}{\varepsilon_{si}} \tag{3.3}$$

In the sub-threshold regime of the DG-MOSFET the electrostatics is dominated by the inter-electrode coupling and the potential is described by the laplace equation. This means that it will be possible to use conformal mapping to find the potential.

Using Schwarz-Christoffel transformation the rectangular body of the DG-MOSFET can be mapped into the W-plane. This transformation of the device will be done by;:

$$\frac{\partial z}{\partial w} = \frac{kC}{\sqrt{(1-w^2)(1-k^2w^2)}} \tag{3.4}$$

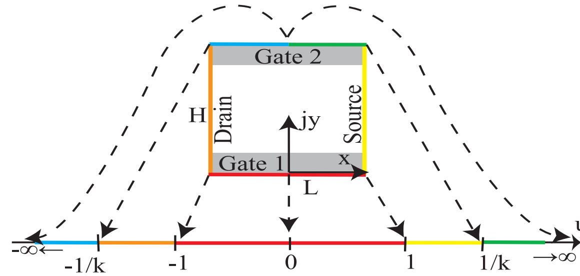

Figure 3.2: The DG device body periphery mapped to the real axis of the W-plane.

where C and k are geometry dependent constants. When the body is transformed to the W-plane, the periphery of the body will lie along the real axis and the corners will be at $u = -1/k, -1/\sqrt{k}, 1/k$ and $1/\sqrt{k}$. The rest of the body will be mapped into the semi-infinate upper half of the complex W-plane, as shown in figure 3.1.

Integration of equation (3.4) will lead to the following form;

$$z = kC \int_0^w \frac{\partial w'}{\sqrt{(1 - w'^2)(1 - k^2 w'^2))}} + C_1 = kCF(k, w) + C_1 \tag{3.5}$$

where C_1 is an integration constant that will be zero if the center of gate 1 is defined by z=0, and F(k,w) is defined by the general Legendre elliptic integral of the first kind:

$$F(k, w) = \int_0^w \frac{dw'}{\sqrt{(1 - w'^2)(1 - k^2 w'^2))}} \tag{3.6}$$

F(k,w) can be found by using look-up tables, simple iteration algorithms or regular power expansions.

Integrating equation (3.5) from the center of gate 1, u=0 and v=0, to the corner between gate 1 and the source, u=1 v=0, gives half of the length, L, of the device and leads to the following equation;

$$L = 2kC \int_0^1 \frac{du'}{\sqrt{(1 - u'^2)(1 - k^2 u'^2))}} = 2kCK(k) \tag{3.7}$$

Here K(k)=F(k,1) is the complete elliptic integral of the first kind. Integrating equation (3.5) from the corner between source and gate 1 (u=1, v=0) to the corner between source and gate 2 (u=1/k, v=0) can be done by solving the integral from u=0 to u=1/k and then subtract the integral from u=0 to u=1. This integration gives the following equation;

$$jH = kC(F(k, \frac{1}{k}) - F(k, 1)) \tag{3.8}$$

Since F(k,1/k)=K(k)-K(k'), where k' is defined by $k' = \sqrt{1 - k^2}$, equation (3.8) becomes:

$$jH = jkCK(k')) \tag{3.9}$$

Rearranging (3.7) leads to:

$$C = \frac{L}{2kK(k)} \tag{3.10}$$

and combining equation (3.10) and (3.9) results in:

$$\frac{L}{2H} = \frac{K(k)}{K(k')} \tag{3.11}$$

The k-value can be extracted from equation (3.11).

Using equation (3.10) and (3.11) the transformation (3.5) can be simplified to:

$$z = x + jy = \frac{LF(k, u + jv)}{2K(k)} \tag{3.12}$$

The transformation of the DG body to the W-plane can be simplified by using an extended device body. This is done by replacing the oxide layer with a dielectrically equivalent layer of undoped silicon. The device body will now have an effective thickness of $H = t_{si} + 2t'_{ox}$ where $t'_{ox} = \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}$. Figure 3.3 shows the body of the extended device.

More detailed information on conformal mapping and the extended body can be found in work by Kolberg and others[14–18].

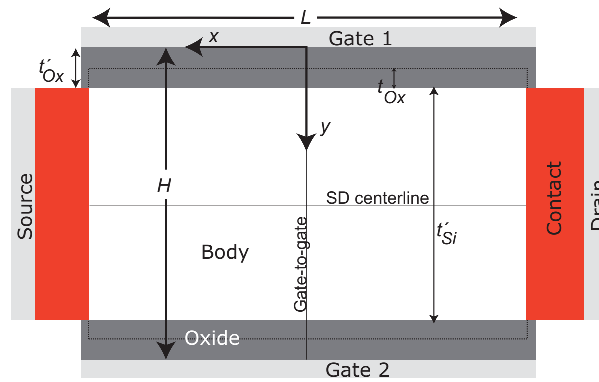

Figure 3.3: Schematic diagram of the extended DG device body.

Chapter 4

Compact Current Modeling

4.1 The Device

The device that will be considered in this thesis is a nanoscale double-gate MOSFET transistor with a big range of geometries. The double-gate MOSFET transistor is a transistor with two gates, one on each side of the channel, as can be seen in figure 3.3. The width of the device is W=1μm, the length varies between 15- and 50nm, the oxide thickness is t_{ox}=1.6nm and the thickness of the silicon varies between 8- and 12nm . The channel consists of p-doped silicon with an acceptor doping of $N_A = 10^{15} cm^{-3}$ and the drain and source terminals consist of n-doped silicon with donor doping concentration of $N_D = 10^{20} cm^{-3}$. The oxide used is a nitrided oxide and a metal with a work function of $\Phi_m = 4.53eV$, which is close to that of molybdenum, is used as the gate metal. The permittivity of the silicon and oxide is $\varepsilon_{si} = 11.8$ and $\varepsilon_{ox} = 7$ respectively and the n+ silicon work function is $\Phi_s = 4.17eV$.

The built in voltage is given as

$$V_{bi} = \frac{E_g}{2} + \phi_b + \frac{k_b T}{2q} ln\left(\frac{N_C}{N_V}\right) \tag{4.1}$$

Where ϕ_b is the potential difference between the Fermi level of the intrinsic silicon and the p-type silicon and is given by $\phi_b = V_{th} ln\left(\frac{N_A}{n_i}\right)$. N_C and N_V are given by $N_C = 2\left(\frac{m_n k_b T}{2\pi\hbar^2}\right)^{\frac{3}{2}}$ and $N_V = 2\left(\frac{m_p k_b T}{2\pi\hbar^2}\right)^{\frac{3}{2}}$. N_C and N_V are dependent on the effective mass of electrons(m_n) and holes(m_p) respectively and will in the simulations in this report be taken as constants found in Atlas. The value of the constants will be $N_C = 2.8 \cdot 10^{25}$ and $N_V = 1.04 \cdot 10^{25}$ The reason why this is done is that the model will be compared with Atlas and should therefore be using the same values to prevent errors that follow the use of different constants. The effective masses are anisotropic quantities, and they're not defined as exact constants.

The flat band voltage is given by

$$V_{FB} = \frac{\left(\Phi_m - \left(\chi + \frac{E_g}{2} + q\phi_b\right)\right)}{q} - \frac{k_b T}{2q} ln\left(\frac{N_C}{N_V}\right) \tag{4.2}$$

where χ is the electron affinity and Φ_m is the work function of the metal. The electron affinity of silicon is 4.17eV and the work function of the metal is assumed to be 4.53eV.

The device body will be fully depleted and this will lead to better gate control[2, page 1].

4.2 Sub-threshold

In sub-threshold the electrostatics of the device is dominated by the inter-electrode capacitive coupling between the electrodes. This means that the 2-D Laplace equation (3.2) can be used to find the potential in the device. The 2-D Laplace equation can be solved using conformal mapping. The carriers will be situated close to the source and drain terminals and along the source-drain symmetry line. The potential can be calculated from equation (4.10) and is shown in figure 4.1.

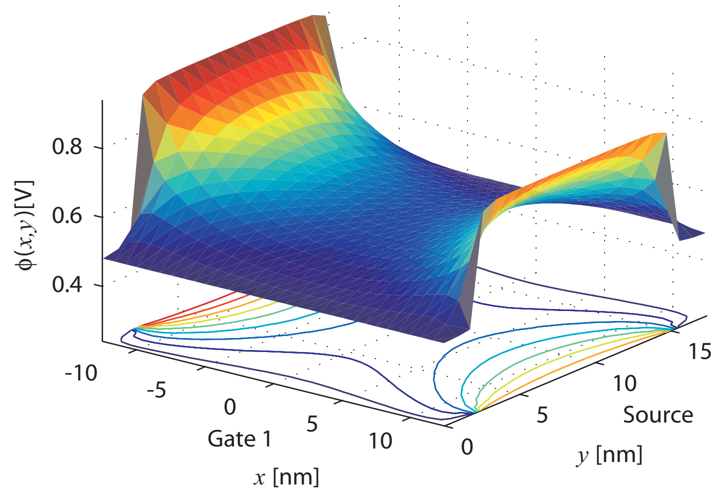

Figure 4.1: The electrostatic potential of the DG device in sub-threshold

The drain current based on drift-diffusion theory can be expressed as;

$$I_d = -q\mu_n W \iint n(x,y) \frac{dV_F(x)}{dx} dxdy \tag{4.3}$$

where V_F is the quasi-Fermi potential, μ_n is the electron mobility, n is the electron distribution, W is the width of the device and q is the electron

charge. Th quasi-Fermi level is assumed to be constant in the x-direction and the integral of equation (4.3) runs over the entire hight and width of the device. Invoking current continuity along the channel and seperating equation (4.3) into a V_F-dependent and a coordinate-dependent part the following equation will be found[19]:

$$I_d = \frac{Wq\mu_n V_{th}[1 - exp(-\frac{V_{ds}}{V_{th}})]}{\int_{-L/2}^{L/2} \frac{dx}{\int_{t'_{ox}}^{t_{si}+t'_{ox}} \frac{n_i^2}{N_a} exp[\frac{\varphi(x,y)}{V_{th}}]dy}} \tag{4.4}$$

Here n_i is the carrier concentration in intrinsic silicon, V_{ds} is the drain-source voltage and $\varphi(x, y)$ is the potential. The current given by equation (4.4) is dependent on the inverse of the charge sheet density given by Boltsmann statistics:

$$n_s = \int_{t'_{ox}}^{t_{si}+t'_{ox}} \frac{n_i^2}{N_a} exp\left[\frac{\varphi(x,y)}{V_{th}}\right] dy \tag{4.5}$$

It is evident, when looking at numerical simulations, that the inverse charge sheet density can be approximated by a normal distribution with the mean value at the top of the barrier. The mean value will be at the top of the barrier because this point carries the least charge, which leads to the maximum of the inverse charge sheet density. The normal distribution will be given by:

$$\frac{1}{n_s(x)} = \frac{1}{n_{sm}} exp\left(- \frac{(x - x_m)^2}{\sigma^2} \right) \tag{4.6}$$

where x_m is the position of the top of the barrier, n_{sm} is the charge sheet density at the top of the barrier and σ defines the position where the charge has increased by a factor of e compared to that of the top of the barrier.

The charge sheet density at the top of the barrier, n_{sm}, can be found through Boltzmann statistics, given in equation (4.5). To find n_{sm} a potential distribution along the y-axis will be needed. It has been shown that a parabolic function is a good approximation in sub-threshold.[20]. The parabolic equation is given as:

$$\varphi(x, y) = \varphi_c(x) \left[1 - \left(1 - \frac{2y}{H}\right)^2\right] + V_{gs} - V_{FB} \tag{4.7}$$

Here φ_c is the potential along the source to drain symmetry line compared to the gate silicon interface of the extended body, and is given by $\varphi_c = \varphi(x, H/2) + V_{FB} - V_{gs}$. Using equation (4.5) together with equaton (4.7) the following expression for the charge sheet density at the top of the barrier can be found:

$$n_{sm} = \frac{n_i^2}{N_a} exp\left(\frac{\varphi_m}{V_{th}}\right) \int_{t'_{ox}}^{t_{si}+t'_{ox}} exp\left[-\frac{\varphi_c(x)}{V_{th}}\left(1-\frac{2y}{H}\right)^2\right] dy \qquad (4.8)$$

where $\varphi_m = \varphi(x_m, H/2)$ is the potential minimum (barrier maximum) along the drain-source symmetry line. Solving the integral of equation (4.8) will lead to the following expression:

$$n_{sm} = \frac{n_i^2}{N_a} exp\left(\frac{\varphi_m}{V_{th}}\right) \frac{H\sqrt{\pi V_{th}} Erf\left(\frac{\sqrt{\varphi_c(x_m)}t_{si}}{H\sqrt{V_{th}}}\right)}{2\sqrt{\varphi_c(x_m)}} \qquad (4.9)$$

The potential will have to be found in order to find n_{sm} and the current. By mapping the device to the W-plane and solving the 2-D Poisson's equation the following expression can be found:[2]:

$$\begin{aligned}\varphi(u,v) =& \frac{1}{\pi}\{\pi(V_{gs}-V_{FB}) + (V_{bi}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1-ku}{kv}\right) \\ &+ (V_{bi}+V_{ds}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1+ku}{kv}\right) \\ &- (V_{bi}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1-u}{v}\right) \\ &- (V_{bi}+V_{ds}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1+u}{v}\right)\end{aligned} \qquad (4.10)$$

In the W-plane, the source-drain symmetry line is mapped into a semicircle with radius $\sqrt{\frac{1}{k}}$. Using equation (4.10) with $v = \sqrt{\frac{1}{k} - u^2}$ will give us the potential along the source-drain symmetry line. Differentiating equation (4.10) with respect to u will lead to an expression for the barrier maximum:

$$u_m = \frac{(1+k)V_{ds}}{2k(2V_{bi} + v_{ds} - 2V_{gs} + 2V_{FB})} \qquad (4.11)$$

$$v_m = \sqrt{\frac{1}{k} - u_m^2} \qquad (4.12)$$

The barrier maximum in the Z-plane can be found through mapping along the source-grain symmetry line with equation (4.11):

$$x_m = \frac{L}{2}\frac{F(\frac{2\sqrt{k}}{1+k}, \sqrt{k}u_m)}{K(\frac{2\sqrt{k}}{1+k})} \qquad (4.13)$$

Finally, combining equation (4.4) with equation (4.9) and (4.8) will lead to the following expression for the drain current:

$$I_d = \frac{Wq\mu_n kT[1 - exp(-\frac{V_{ds}}{V_{th}})]n_{sm}}{\sqrt{\frac{\pi}{2}}\sigma[Erf(\frac{L-2x_m}{2\sqrt{2}\sigma}) + Erf(\frac{L+2x_m}{2\sqrt{2}\sigma})]} \tag{4.14}$$

As mentioned earlier, σ is the distance from the top of the barrier where the charge has increased by a factor of e. By using a parabolic approximation similar to equation (4.7) to describe the potential along the source symmetry line the following expression for σ can be found:

$$\sigma = \sqrt{\frac{\varphi(x_m + \sigma, t'_{ox} + t_{si}) - \varphi_m}{(V_{bi} - \varphi_m)}}(L/2 - x_m) \tag{4.15}$$

where $\varphi(x_m + \sigma, t_{ox} + t_{si}/2)$is given in:

$$\frac{n_i^2}{N_a} e^{\frac{\varphi(x_m+\sigma,t_{ox}+t_{si}/2)}{V_{th}}} \frac{H\sqrt{\pi V_{th}\left[\frac{\sqrt{\varphi(x_m+\sigma,t_{ox}+t_{si}/2)}t_{si}}{H\sqrt{V_{th}}}\right]}}{2\sqrt{\varphi(x_m + \sigma, t_{ox} + t_{si}/2)}} = en_{sm} \tag{4.16}$$

4.2.1 Sub-threshold Asymptote

An asymptote in the logarithmic plane is needed for implementation in a continuous function later in this thesis. The asymptote can easily be extracted by using equation (4.14) at two different V_{gs}-values. With I_{dd1} corresponding to V_{gs1} and I_{dd2} corresponding to V_{gs2} the following function can be used to give the slope:

$$S = \frac{Log[\frac{I_{dd2}}{I_{dd1}}]}{V_{gs1} - V_{gs2}} \tag{4.17}$$

The slope could also be found without extracting the current at a second V_{gs}-value by solving the following slope function:

$$S = \frac{ln[10]I_{dd}}{I_{dd}/V_{gs}} \tag{4.18}$$

When the slope has been found the asymptote is given by:

$$I_{dd} = I_{dd1}10^{(V_{gs}-V_{gs1})S} \tag{4.19}$$

Figure 4.2 shows the asymptotes compared to the numerical simulations of the current. The asymptotes follow the current until it enters the near threshold regime.

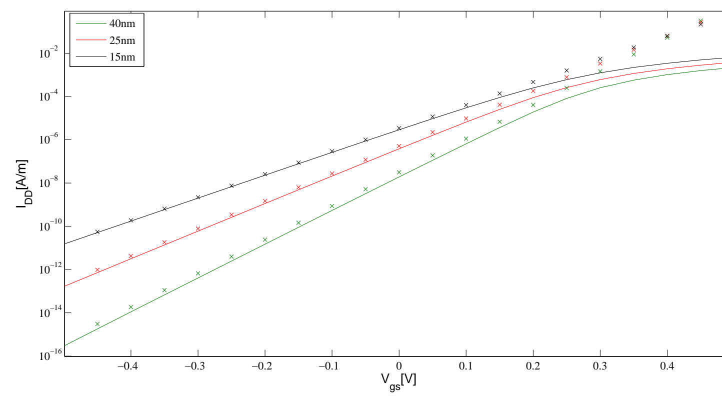

Figure 4.2: Graph showing the asymptotes from the model compared to the numerical simulations. The solid line indicates the numerical simulations

4.3 Strong Inversion

In the strong-inversion the electrostatics is dominated by the mobile charge contribution. The carriers in the channel will mostly be situated at the silicon-oxcide border right under the gates and create two conducting channels (figure 4.3). Because of this it is possible to use long channel models as the source and drain terminals won't have a significant effect on the electrostatics. The field between the gate and body will be much larger than the field between drain and source through the entire channel.

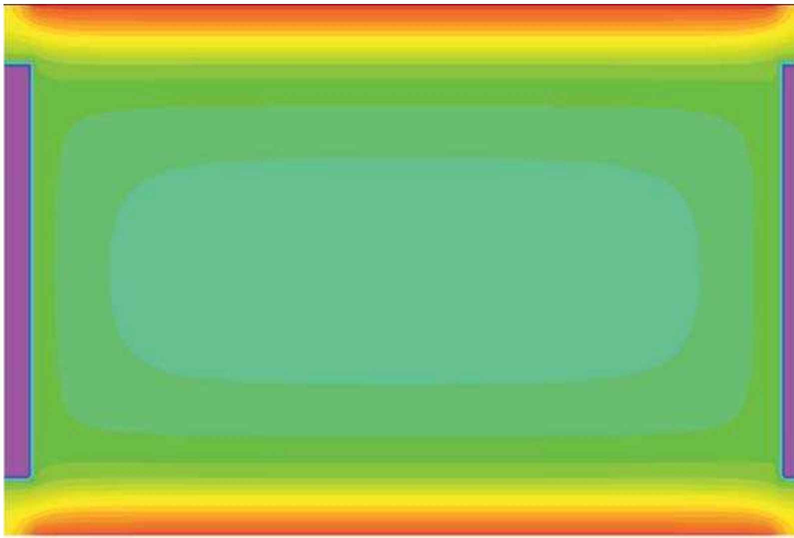

Figure 4.3: Potential contour plot for the strong-inversion region.

The gradual channel approximation (CGA) is the basis for the long channel model. The GCA states that the electrostatic problem can be solved as two coupled equations, the one dimensional poison equation between the gates and a charge transport equation between source and drain. This approximation is dependent on the vertical field (gate) being much larger than the horizontal (drain/source). Therefore the GCA will usually not work if the transistor reaches saturation. With transistors with small gate lengths, as considered in this report (<50nm), there will be no saturation as the transport mechanisms will change to quasi-ballistic transport, before the current saturates completely. Using the GCA, an equation that's very similar to the long channel equation for a single gate transistor multiplied by a factor of two can be found. The big difference will be the threshold voltage that will not be as simple in the double gate case as in the single gate case. The V_t value in the long channel equation will only represent the threshold value for the strong-inversion region and not the threshold-value for the transistor or

continuous model.[7]

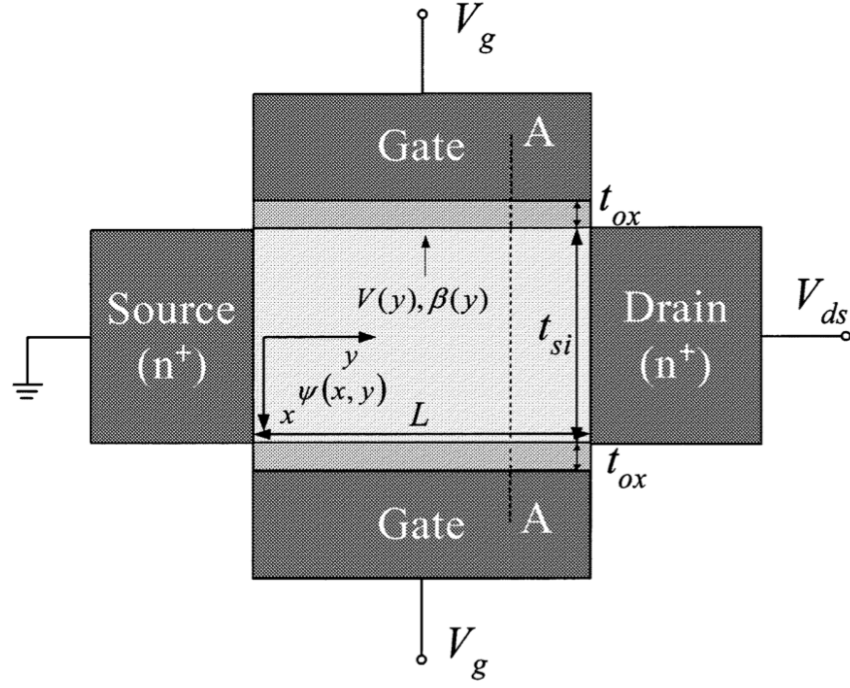

Figure 4.4: Schematic diagram of a double-gate MOSFET.

V_t will be found by starting with the 1-D Poisson's equation and then follow the approach suggested by Taur[7]. The DG-MOSFET structure is shown, with y- and x-directions defined, in figure 4.4. Because the mobile charge (electrons) will be much larger than the static charge, the starting point will be Poisson's equation along the vertical direction (gate to gate) with only the mobile charge term.

$$\frac{d^2\varphi}{dx^2} = \frac{qn_i^2}{\varepsilon_{si}N_a}exp\left(\frac{\varphi - V_F}{V_{th}}\right) \tag{4.20}$$

Where φ is the electrostatic potential, ϵ_{si} is the permittivity of the silicon, V_F is the electron quasi-Fermi potential and n_i is the intrinsic electron density. By integrating equation (4.20) twice the following solution will be reached[7]

$$\varphi(x) = V_F - \frac{2kT}{q}ln\left[\frac{t_{si}}{2\beta}\sqrt{\frac{q^2n_i^2}{2\epsilon_{si}kTN_a}}cos(\frac{2\beta x}{t_{si}})\right] \tag{4.21}$$

where β is a constant in the x-direction, not in the y-direction. β can be found by using the boundary conditions

$$\epsilon_{ox}\frac{V_{gs} - V_{FB} - \varphi(x = \pm\frac{t_{si}}{2})}{t_{ox}} = \pm\epsilon_{si}\frac{d\varphi}{dx} \mid x = \pm\frac{t_{si}}{2} \tag{4.22}$$

where V_{FB} is the work function of the gates with respect to the intrinsic silicon. By inserting equation (4.21) into (4.22) the following equation will be found

$$\frac{q(V_{gs} - V_{FB} - V_F)}{2kT} - ln\left[\frac{2}{t_{si}}\sqrt{\frac{2\epsilon_{si}kTN_a}{q^2n_i^2}}\right] = ln\beta - ln[cos\beta] + \frac{2\epsilon_{si}t_{ox}}{\epsilon_{ox}t_{si}}\beta tan\beta \tag{4.23}$$

By using equation (4.23) β can be found as a function of V_F for a given V_{gs}. V_F will change between the drain and source, and since V_F is y dependent β will be the same.

The fact that the current must be the same through the channel, that means the same for any y value, can be used to find the y dependence of V_F and β. The current continuity condition can be expressed as

$$I_{ds} = \mu WQ_i\frac{dV_F}{dy} = constant \tag{4.24}$$

where μ is the effective mobility, Q_i is the charge per unit gate area and W is the channel width. Integrating formula (4.24) and using $\frac{dV}{dy} = \frac{dV}{d\beta}\frac{d\beta}{dy}$ the following equation will be found

$$I_{ds} = \mu\frac{W}{L}\int_0^{V_{ds}} Q_i(V_F)dV = \mu\frac{W}{L}\int_{\beta_s}^{\beta_d} Q_i(\beta)\frac{dV}{d\beta}d\beta \tag{4.25}$$

where β_s is the β value at source and β_d is the β value at drain. The charge per unit gate area Q_i can be expressed as a function of β by inserting formula (4.21) into gauss law[21], $Q_i = 2\epsilon_{si}\frac{d\varphi}{dx}\Big|_{x=\frac{t_{si}}{2}}$

$$Q_i = 2\epsilon_{si}\frac{2kT}{q}\frac{2\beta}{t_{si}}tan\beta \tag{4.26}$$

By substituting equation (4.26) into (4.25) and then integrate the expression analytically a solution can be found

$$\begin{aligned} I_{ds} &= \mu\frac{W}{L}\frac{4\epsilon_{si}}{t_{si}}\left(\frac{2kT}{q}\right)^2\int_{\beta_d}^{\beta_s}[tan\beta + \beta tan^2\beta + \frac{2\epsilon_{si}t_{ox}}{\epsilon_{ox}t_{si}}\beta tan\beta\frac{d}{d\beta}(\beta tan\beta)]d\beta \\ &= \mu\frac{W}{L}\frac{4\epsilon si}{t_{si}}\left(\frac{2kT}{q}\right)^2\left[\beta tan\beta - \frac{\beta^2}{2} + \frac{\epsilon_{si}t_{ox}}{\epsilon_{ox}t_{si}}\beta^2tan^2\beta\right]\Bigg|_{\beta_d}^{\beta_s} \end{aligned} \tag{4.27}$$

The right hand side of equation (4.23) and the β dependent part of equation (4.27) can be expressed as

$$f_r(\beta) = ln\beta - ln[cos\beta] + 2r\beta tan\beta \tag{4.28}$$

$$g_r(\beta) = \beta tan\beta - \frac{\beta^2}{2} + r\beta^2 tan^2\beta \tag{4.29}$$

were $r = \frac{\epsilon_{si} t_{ox}}{\epsilon_{ox} t_{si}}$ is a structural parameter. If boundary conditions are used with equation (4.23), f_r can be used to find expressions for the β values at drain and source. By using these values in g_r it will be possible to find an expression for I_{ds} that is not β dependent. To simplify equation (4.23), the constant V_0 is used.

$$V_0 = V_{FB} + \frac{2kT}{q} ln\left[\frac{2}{t_{si}}\sqrt{\frac{2\epsilon_{si} kTN_a}{q^2 n_i^2}}\right] \tag{4.30}$$

At the drain the voltage, V_F, will be equal to V_{ds} and at source it will be equal to 0. This leads to the following equations at source and drain respectively: $f_r(\beta_s) = \frac{q}{2kT}(V_{gs} - V_0)$ and $f_r(\beta_d) = \frac{q}{2kT}(V_{gs} - V_0 - V_{ds})$. By using these equations β_s and β_d can be found. β_s and β_d can then be inserted into equation (4.27) to yield an expression for I_{ds} that is only dependent on the variables V_{gs} and V_{ds}

$$I_{ds} = \mu C_{ox}\frac{W}{L}[(V_{gs} - V_t)^2 - (V_{gs} - V_t - V_{ds})^2] = 2\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} \tag{4.31}$$

where $V_t = V_0 + \delta$ and $\delta = \frac{2kT}{q} ln\left[\frac{V_{gs} - V_0}{4rkT}\right]$ is a second order term that comes from the $ln(cos\beta)$ part of f_r(equation (4.28))[7].

4.3.1 Strong inversion asymptote

It is necessary to find the asymptote of the current to implement it in the continuous model. One way to do this is by expressing a linear equation in the logarithmic scale

$$log(I_{ds}) = log(I_{const}) + \frac{V_{gs}}{S} => I_{ds} = I_{const} \cdot 10^{\frac{V_{gs}}{S}} \tag{4.32}$$

where S is the slope factor in the logarithmic scale and I_{const} is the current at $V_{gs} = 0$ found through a chosen V_{gs} value. The I_{const} value will adjust the current by a constant and be found at the V_{gs} that gives the best results.

$$I_{const} = 2\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} \cdot 10^{-\frac{V_{g1}}{S}} \tag{4.33}$$

By calculating the derivative of the logarithm of I_{ds} an expression for the slope factor can be found[22].

$$\frac{dln(I_{ds})}{dV_{gs}} = \frac{1}{I_{ds}} \frac{dI_{ds}}{dV_{gs}} = \frac{d}{dV_{gs}} \left(ln(I_{const}) + \frac{V_{gs}}{S} \cdot ln(10) \right) \quad (4.34)$$

$$S = \frac{ln(10) I_{ds}}{dI_{ds}/dV_{gs}} \quad (4.35)$$

S is found by inserting equation (4.31) and its derivative into equation(4.35). This is done in appendix A.

$$S = ln(10)(V_{gs} - V_0 - \frac{V_{ds}}{2}) \quad (4.36)$$

The slope is dependent on V_{gs}. Since a linear equation is desired in the logarithmic scale, a constant slope factor must be found. This is done by deciding the slope factor at a certain V_{gs} value. The V_{gs} value is decided graphically through simulations to see which value gives the best resemblance to results from Atlas. In this thesis both I_{const} and the slope S are found at $V_{gs} = 1V$

Figure 4.5 shows the asymptote compared to numerical simulations of the current.

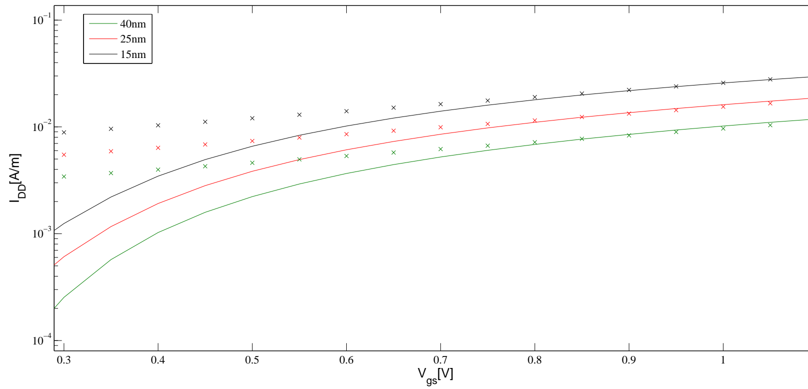

Figure 4.5: Graph showing the asymptotes from the model compared to the numerical simulations. The solid line indicates the numerical simulations

4.4 Near Threshold

In the threshold region the potential due to the charge in the channel will be comparable to the inter-electrode potential. This means that an approximation where only one of these terms is considered can not be used. In other words, both the inter-electrode potential and the mobile charge term must be considered in the potential. For low-frequency signals, current can be assumed to be same at every point along the channel, it is therefore sufficient to find the current through the device at a single point. The current through the center of the device can be found using the following equation:

$$I_d = q\mu W n_{s0} e^{-\frac{V_{F0}}{V_{th}}} \frac{dV_{F0}}{dx}\bigg|_{x=0} \tag{4.37}$$

Here V_{F0} is the quasi-Fermi level at the center of the device, $(\frac{dV_{F0}}{dx})$ is the effective field and n_{s0} is the charge sheet density at the center, referred to the quasi-Fermi level.

In this thesis the current will be found through the middle of the device at $V_{gs} = 0.3V$. $V_{gs} = 0.3V$ is selected because it is close to the threshold value, and a current at a V_{gs} near threshold is needed to find the m-parameter in the continuous equation (4.49). The current will be found by modeling the quasi-Fermi level, the effective electric field and the potential. The potential will be used to find the charge sheet density at the center of the device.

4.4.1 Quasi-Fermi potential

The drift diffusion current density is given as[3]:

$$J_{ds} = q\mu_n n_s(x)\frac{dV_F(x)}{dx} \tag{4.38}$$

By assuming that the quasi-Fermi level is constant over any cross-section perpendicular to the x-axis, and using Boltzmann statistics for the charge sheet density, integration of equation (4.38) will lead to the following equation[3]:

$$I_{DD} = q\mu_n V_{th}\frac{\int_0^{V_{ds}} exp(\frac{-V_F}{V_{th}dV_F})}{\int_{-L/2}^{L/2}\frac{dx'}{n_{s0}(x)}} = q\mu_n\frac{1-exp(\frac{-V_{ds}}{V_{th}})}{\int_{-L/2}^{L/2}\frac{dx'}{n_{s0}(x)}} \tag{4.39}$$

An expression for the quasi-Fermi level can be derived from (4.39)[3]:

$$V_F(x) = -V_{th} ln\left[1 - \frac{I_{DD}}{q\mu_n}\int_{-L/2}^{x}\frac{1}{n_{s0}(x')}dx'\right] \tag{4.40}$$

By combining equation (4.40) and (4.39) an equation describing the quasi-Fermi level in the center of the device can be found:

$$V_{F0} = -V_{th} ln\left[1 - \frac{1 - e^{-\frac{V_{ds}}{V_{th}}}}{\int_{-L/2}^{L/2} \frac{dx}{n_{so}(x)}} \int_{-L/2}^{0} \frac{dx}{n_{so}(x)}\right] \tag{4.41}$$

The quasi-Fermi level at the center, given as V_{F0}, is dependent on the ratio, R, of the inverse charge sheet density between the center of the device and the source, compared to the complete channel. At very low V_{ds}-values the charge distribution will be close to symmetrical around the center of the device and R will be close to 0.5. In this case the quasi-Fermi level can be approximated quite easily[23], at higher V_{ds}-values it will however be more difficult, and a model for the ratio is required.

Numerical simulations of the ratio show an exponential shape that can be approximated by:

$$R = 1 - 0.5e^{aV_{ds}} \tag{4.42}$$

Where the factor a has been found empirically by numerical simulations of the ratio at $V_{ds} = 0.2V$ with different silicon thicknesses, t_{si}, and lengths, L. With this the final expression for the ratio becomes:

$$R = 1 - 0.5[0.27446 - 1.873 \cdot 10^7 t_{si} + (0.0134914 - 3.41 \cdot 10^5 t_{si})L]^{\frac{V_{ds}}{0.2V}} \tag{4.43}$$

This approximation is based on empirical data from the numerical simulations of the ratios. It it is only valid at $V_{gs} = 0.3V$ but that is the only value needed in this model. Figure 4.6 shows the ratio from equation (4.43) compared with the ratio from the numerical simulations.

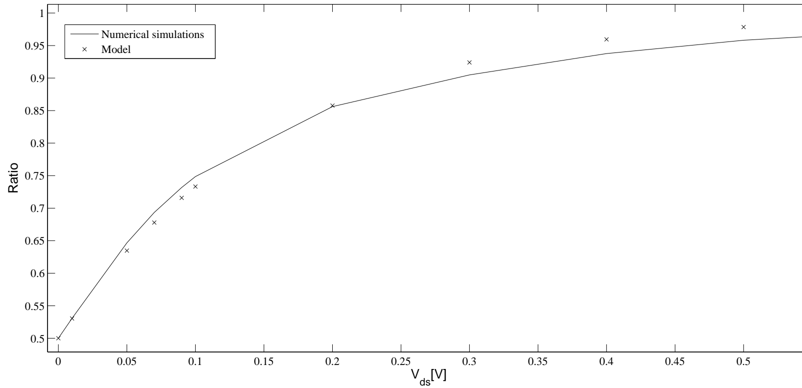

Figure 4.6: Graph showing the ratio from the model compared to the numerical simulations. The solid line indicates the numerical simulations

Using equation (4.41) together with (4.43), the quasi-Fermi level at the center of the device at $V_{gs} = 0.3V$ can be found. At high V_{ds}-voltages the

term inside the natural logarithm in equation (4.41) will get close to zero as the ratio and $1 - e^{-\frac{V_{ds}}{V_{th}}}$ both become closer to 1. This means that the model will be very sensitive and amplify the errors from the ratio at high V_{ds}. Figure 4.7 shows the quasi-Fermi level from the model compared with the numerical simulations with gate lengths 15nm, 25nm and 40nm. Several other quasi-Fermi level models were tested and found inadequate during the work.

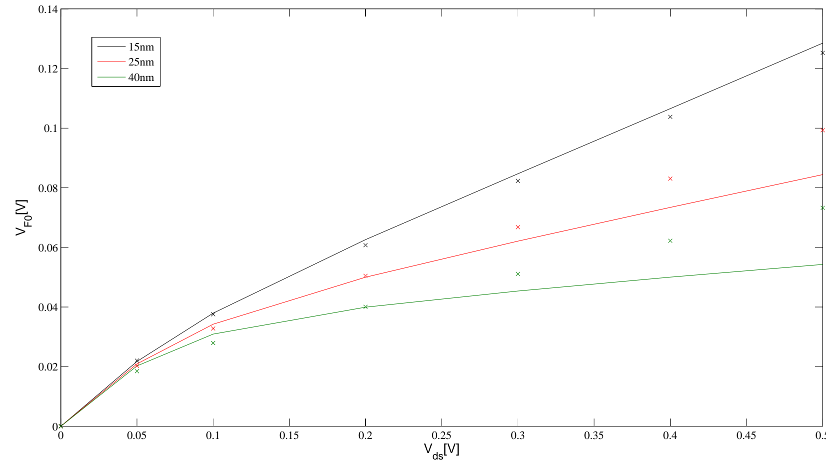

Figure 4.7: Graph showing the quasi fermi level from the model compared to the numerical simulations. The solid line indicates the numerical simulations

4.4.2 Effective Electric Field

Next, the effective electric field ($\frac{dV_{F0}}{dx}$) will have to be found, differentiating the expressions for the quasi-Fermi level will be inaccurate and a new approximation is needed. The following compact model is purposed:

$$\frac{dV_{F0}}{dx} = \frac{V_{ds}}{L} \tag{4.44}$$

A more exact model was also found empirically:

$$\frac{dV_{F0}}{dx} = \frac{(90 \cdot 10^{-9}m - L)}{50 \cdot 10^{-9}m} \frac{V_{ds}}{L} - \frac{V_{ds}^2}{L \cdot 1V} \tag{4.45}$$

The model of equation (4.45) is more accurate, but is also much more complex. New empirical parameters will be introduced if equation (4.45) is used. This will make the model less physical and more empirical. The model of equation (4.44) is therefore preferred even though it gives less accuracy

than the other proposed model. Figure 4.8 shows the differentiated quasi-Fermi level from numerical simulations together with the two proposed approximations. The approximation of equation (4.44) is marked with crosses and that of equation(4.45) is marked with triangles.

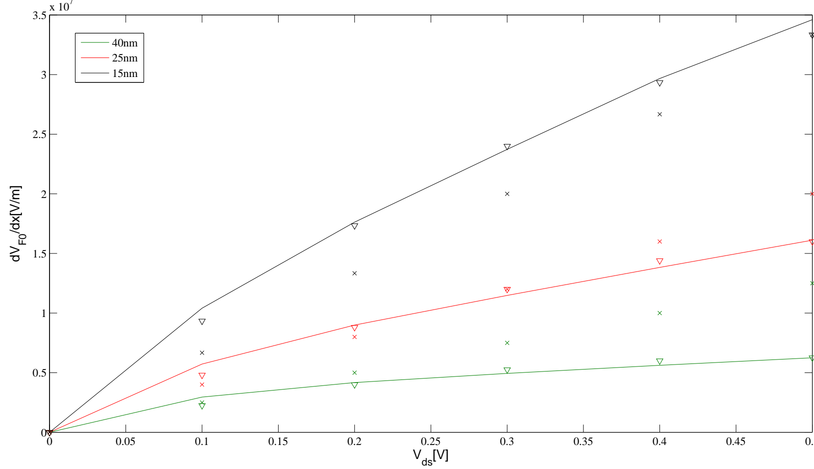

Figure 4.8: Graph showing the differentiated quasi-Fermi level from the models compared to the numerical simulations. The solid line indicates the numerical simulations

4.4.3 Electrostatic Potential

As mentioned in section 3.1, the potential can be divided into the mobile charge and inter-electrode contributions. The inter-electrode contribution is given by equation (4.10). The mobile charge contribution to the potential can be found by solving Poisson's equation, (3.3). Near threshold, the potential due to the charge (φ_1) will have an almost linear slope at the center of the source drain symmetry line, and the approximation $\frac{d^2\varphi_1}{dx^2}|_{x=0} = 0$ can be used. This means that the 1D Poisson's equation is sufficient to find the potential at the center of the device.

A parabolic shape was assumed for the gate to gate symmetry line:

$$\varphi_1(0, y) = \varphi_{1m}(1 - (1 - 2\frac{y}{H})^2) \tag{4.46}$$

where φ_{1m} is the potential at the center of the device and H is the height of the device. Differentiating equation (4.46) twice with respect to y will lead to the following equation:

$$\frac{d\varphi_1(0, y)}{dy} = -\frac{8\varphi_{1m}}{H^2} \tag{4.47}$$

Combining equation (4.47) and (3.3) and setting $\frac{d^2\varphi_1}{dx^2}$ at the center equal to zero will lead to the following equation:

$$-\frac{8\varphi_{1m}}{H^2} = \frac{q}{\varepsilon_{si}}\frac{n_i^2}{N_s}exp(\frac{\varphi_{1m} + \varphi_2(0, H/2) - V_{F0}}{V_{th}}) \tag{4.48}$$

φ_{1m} can easily be found by combining equation (4.48) with equation (4.10) and (4.41).

The charge sheet density at the center can now easily be found using the Boltzmann statistics from equation (4.5) with the potential from equation (4.48) and (4.10).

Using the models described in this section the current at $V_{gs} = 0.3V$ can now easily be found with equation (4.37).

4.5 Continuous Model

In strong inversion and sub-threshold it is possible to simplify the potentials and find expressions based on simple approximations. These expressions can be used to find compact models that describe the current in these regimes. In this thesis asymptotes describing the current in sub-threshold and strong inversion have been found in section 4.2 and 4.3 respectively. Both these asymptotes will overestimate the current in the threshold region, and a continuous model that combines these compact models is desired. Such a model must meet the requirements of circuit simulators, and not be too complex or give too much error. The following interpolation function is purposed:

$$I_{DD} = 10\hat{}\left(\frac{log(I_{sub})}{\left[1 + \left(\frac{log(I_{sub})}{log(I_{inv})}\right)^m\right]^{\frac{1}{m}}}\right) \tag{4.49}$$

where I_{sub} and I_{inv} are the asymptotes in sub-threshold and strong inversion respectively and m is a parameter found by matching the current to the near threshold calculations of section 4.4. The continuous model will follow the sub-threshold and strong inversion asymptote in the sub-threshold region and strong inversion region respectively.

Figure 4.9 shows the interpolation function of equation (4.49) together with the numerical simulations from Atlas and the modeled asymptotes in strong inversion and sub-threshold. The crosses indicate the continuous model and the solid line indicates the numerical simulations while the dotted lines show the asymptotes.

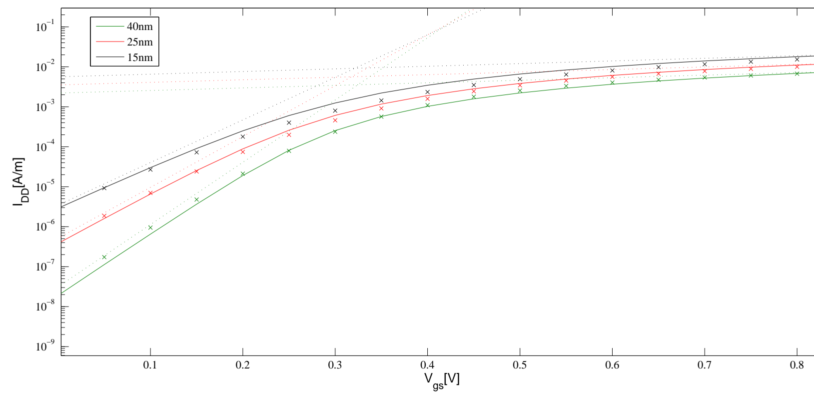

Figure 4.9: The continuous model compared with numerical simulations and the asymptotes. The solid line indicates the numerical simulations, the crosses indicate the continuous model and the dashed lines show the asymptotes from sub-threshold and strong inversion.

Chapter 5

Simulations

In this chapter the performance of the model will be investigated. At short channel lengths ($L \leq 20nm$) the scaling factor(Length/hight) of the device becomes too large, and Poisson's equation from equation (4.48) starts giving large errors. Because of this, all simulations of the device at 15nm will be performed with a silicon thickness of $t_{si} = 8nm$. All gate lengths from 20nm and above are simulated using a silicon thickness of $t_{si} = 12nm$. Figure 5.1, 5.2 and 5.3 show the $I - V_{gs}$ curves of the 15nm, 25nm and 40nm devices for V_{ds}=0.1V, 0.3V and 0.4V respectively.

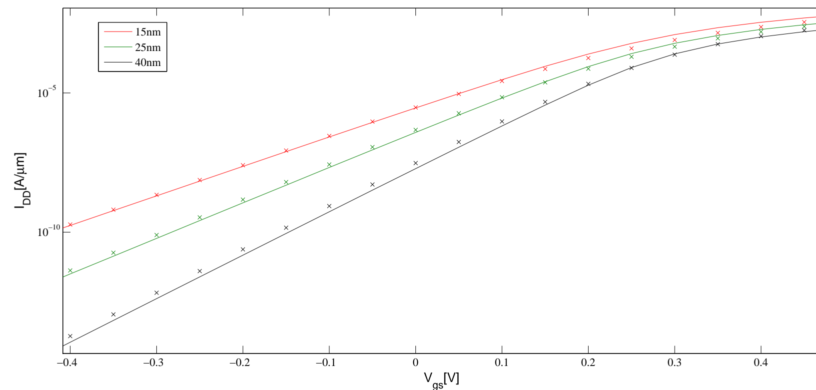

Figure 5.1: Graph showing how the current varies with V_{gs} at V_{ds} set to 0.1V. The crosses show the performance of the compact model.

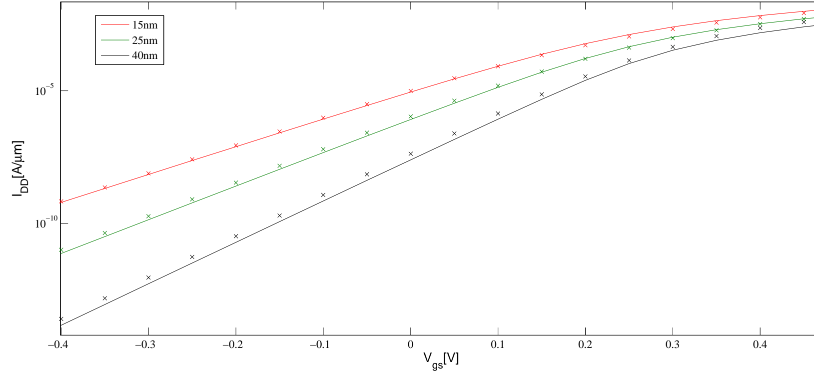

Figure 5.2: Graph showing how the current varies with V_{gs} at V_{ds} set to 0.3V. The crosses show the performance of the compact model.

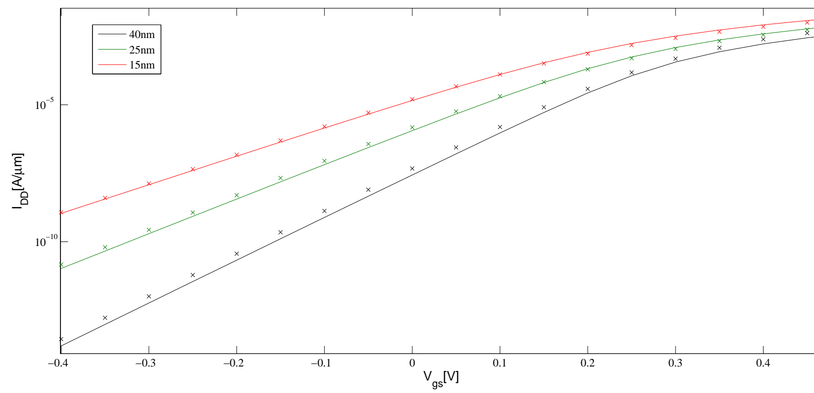

Figure 5.3: Graph showing how the current varies with V_{gs} at V_{ds} set to 0.4V. The crosses show the performance of the compact model.

It can be seen that the model yields good results for the 15nm device and the 25nm device, however, the 40nm device overestimates the current at high V_{gs} and V_{ds} values. At $V_{ds} = 0.1V$ the model performs well even for the 40nm device, but at higher V_{ds} values it only returns good results below $V_{gs} = 0.4V$.

The results for the 25nm and 15nm device can be viewed closer in the $I - V_{ds}$ curves in figure 5.4 and 5.5. The model underestimates the current for the 15nm device and figure 5.6 shows how this could be improved by using the more exact model for the differentiated quasi-Fermi level of equation (4.45).

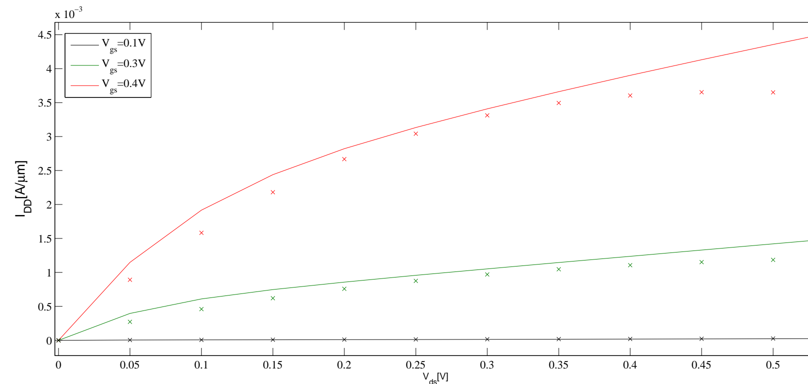

Figure 5.4: The $I - V_{ds}$ curve of the 25nm device with t_{si}=12nm. The crosses show the performance of the model.

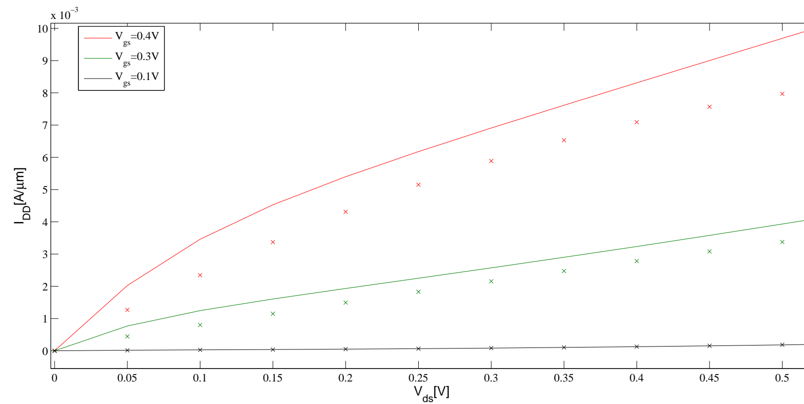

Figure 5.5: The $I - V_{ds}$ curve of the 15nm device with t_{si}=8nm. The crosses show the performance of the model.

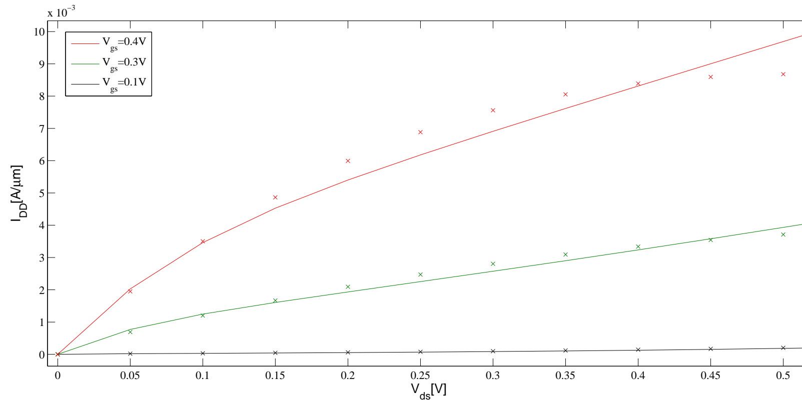

Figure 5.6: The $I-V_{ds}$ curve of the 15nm device with t_{si}=8nm and the differentiated quasi-Fermi model of equation (4.45). The crosses show the performance of the model.

At low V_{gs} values the model gives an excellent agreement with the numerical simulations for all lengths between 15nm and 40nm. The $I - V_{ds}$ curve at V_{gs}=0.1V for devices with gate lengths of 15nm, 25nm and 40nm can be seen in figure 5.7.

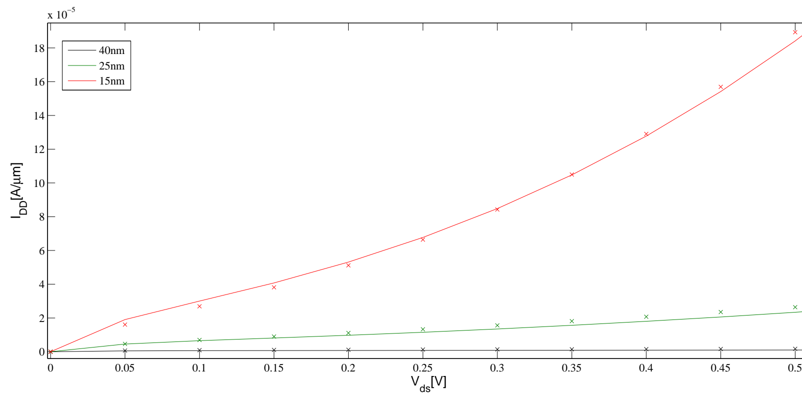

Figure 5.7: Graph showing the models compared to numerical results at $V_{gs} = 0.1V$. The crosses indicate the compact model.

Chapter 6

Discussion

A compact drain current model for a nanoscale double-gate transistor has been presented. The model has been tested with different voltages and gate lengths.

The model presented in this work yields good results until it reaches V_{gs}-values above 0.4V. It is therefore natural to call this model a low power model. Such a model could be very useful as low power circuits are much needed, especially in battery dependent applications.

At gate lengths of 40nm and above the model will give substantial errors also at V_{gs}=0.4V, where the model returns good results for devices with shorter gate lengths. The main focus in the work was however on the smaller gate lengths as other models that work on longer gate lengths exist. Models describing the drain currents of transistors with gate lengths below 50nm are scarce.

The model has some empirical parameters in the quasi-Fermi level model, but can still be thought of as analytical.

A look-up-table or a completely empirical function for the m-values of equation (4.49) could be an alternative to the solution in the near threshold regime. This would give better accuracy in the near threshold region and also reduce the V_{gs} limitations of the model. However, a solution like that would not allow any adjustments to the model. Using an analytical model means that the inversion and sub-threshold models can be changed without the near-threshold model becoming useless. Another benefit of using an analytical model is the possibility of using parts of this model for other uses. A model describing the quasi-Fermi level could for instance be very useful for other modeling tasks. However, the quasi-Fermi potential presented in this work is only valid at one specific gate voltage, $V_{gs} = 0.3V$ and will because of this probably not be very useful in other models. This is also the case for the modeling of the potential at near threshold, since this model uses the quasi-Fermi level model.

Chapter 7

Conclusion

A compact model describing the current through a nanoscale double-gate MOSFET has been presented. At low V_{gs}-values the currents generated by the model correspond well to numerical simulations done with Atlas from Silvaco. However, the model will generate large errors for V_{gs}-values above 0.4V and is therefore regarded as a low power model.

In sub-threshold, the model is based on conformal mapping techniques used to solve the inter-electrode potential contribution, and a long channel approximation is used in the strong inversion regime. The two regimes are combined using an interpolation function that involves an m-parameter that is found analytically through calculations of the current in near threshold.

7.1 Future Work

A complete compact model for inclusion in circuit simulators must include models describing the current, capacitances and noise in the device. Since this work only concentrates on the modeling of the current, models describing the noise and capacitances are needed in the future. When these models are developed SPICE-type models can be created.

The model presented in this work can also be used to find an expression for the threshold voltage. This can be done by differentiating the current with regard to the gate voltage in order to find the transconductance. The maximum transconductance will be at the threshold voltage.

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Appendix A

Derivation of the slope factor

This appendix will show how S was derived through the differentiation of I_{ds}.

The current I_{ds} is given by

$$I_{ds} = 2\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} \tag{A.1}$$

where V_t is given by

$$V_t = V_0 + \frac{2kT}{q}ln\left[\frac{V_{gs} - V_0}{4rkT}\right]$$

The derivative of I_{ds} will be

$$\frac{dI_{ds}}{dV_{gs}} = 2\mu C_{ox}\frac{W}{L}\left(1 - \frac{dV_t}{dV_{gs}}\right)V_{ds}$$

where the derivative of V_t can be expressed as

$$\frac{dV_t}{dV_{gs}} = \frac{2kT}{q}\frac{1}{V_{gs} - V_0}$$

The derivative of I_{ds} with respect to V_{gs} will be

$$\frac{dI_{ds}}{dV_{gs}} = 2\mu C_{ox}\frac{W}{L}\left(1 - \frac{2kT}{q}\frac{1}{V_{gs} - V_0}\right)V_{ds} \tag{A.2}$$

The next step will be to find the slope, S.

$$S = \frac{ln(10)I_{ds}}{dI_{ds}/dV_{gs}} \tag{A.3}$$

By inserting equation (A.1) and equation (A.2) into equation (A.3) the following expression will be found

$$
\begin{aligned}
S =& ln(10)\frac{2\mu C_{ox}\frac{W}{L}\left(V_{gs}-V_0+\frac{2kT}{q}ln\left[\frac{V_{gs}-V_0}{4rkT}\right]-\frac{V_{ds}}{2}\right)V_{ds}}{2\mu C_{ox}\frac{W}{L}\left(1-\frac{2kT}{q}\frac{1}{V_{gs}-V_0}\right)V_{ds}} \\
S =& ln(10)\frac{\left(V_{gs}-V_0+\frac{2kT}{q}ln\left[\frac{V_{gs}-V_0}{4rkT}\right]-\frac{V_{ds}}{2}\right)}{\left(1-\frac{2kT}{q}\frac{1}{V_{gs}-V_0}\right)}
\end{aligned}
\tag{A.4}
$$

According to Taur[7] $\frac{2kT}{q}ln\left[\frac{V_{gs}-V_0}{4rkT}\right]$ is a small second-order effect with values close to 0.05V. By using series expansion, $\frac{1}{1+\alpha} = 1-\alpha+\alpha^2...$, and only considering factors of the first degree, since α is small, the following equation will be found from equation (A.4)

$$
S = ln(10)(V_{gs}-V_0-\frac{V_{ds}}{2}) \tag{A.5}
$$