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Design of a low-cost CC-VFC for one-celled Li-Ion batteries

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Problem Description

The assignment is to design a low-cost Coulomb Counter (VFC) that fulfills the requirements of the 1-cell Li-Ion Battery Management IC. This VFC will be supplied at 2.2 V in a 0.25 µm process. The project work previous done concluded that the operation amplifiers in the VFC are very critical for reaching high performance.

The first design task will be to identify a suitable opamp architecture, suppress nonidealities like gain-error and offset by using feedback or other cancellation techniques. Then the opamp’s will be integrated into the VFC and data as achievable resolution and current consumption should be extracted. The design should be fully analyzed if it is suitable for the given IC.

Assignment given: 18. January 2007
Supervisor: Trond Sæther, IET

Prosjektoppgave

Kandidatens navn: Fredrik Hafslund

Oppgavens navn: Design a low-cost CC-VFC for one-celled Li-Ion batteries

Oppgave 1:
"In the new smart battery microcontrollers from Atmel, high accuracy continuous current measurements are becoming very important. This is due to the chemically advanced Lithium-ion battery, which requires intense control of the charging process for 100% utilization. Atmel is therefore looking to design a low-cost, low-voltage, high-performance coulomb counter."

Oppgave 2:
The assignment is to design a low-cost Coulomb Counter (VFC) that fulfills the requirements of the 1-cell Li-Ion Battery Management IC.
This VFC will be supplied at 2.2 V in a 0.25 µm process. The project work previous done concluded that the operation amplifiers in the VFC are very critical for reaching high performance.
The first design task will be to identify a suitable op-amp architecture, suppress non-idealities like gain-error and offset by using feedback or other cancellation techniques. Then the op-amp will be integrated into the VFC and data as achievable resolution and current consumption should be extracted. The design should be fully analyzed if it is suitable for the given IC.

Dette arbeidet er basert på prosjektoppgave høst 2006 og masteroppgave 2007 med henholdsvis oppgave 1 og oppgave 2 som oppgavetekst.

I tillegg til den gitte oppgaveteksten ble det spesifisert av veileder at forskjellige typer ladningstellere skulle sees på for å identifisere fordeler og ulemper ved lav spenning og effekt. Det skulle samles informasjon om løsninger på markedet, og ut i fra det skulle spesifikasjoner for oppløsning og hastighet estimeres. Det ble spesifisert at det skulle designes en VFC for en-cellede applikasjoner og denne skulle simuleres i VHDL-AMS ved hjelp av ADVance-MS[1].

Veileder: Fredrik Jonsson, Atmel Norway AS

Faglærer: Trond Sæther, NTNU

Summary

The Lithium-ion battery is today used by close to every portable battery powered device, and this marked is constantly increasing because not only are the products the consumer have had for years getting more and more sophisticated, so he or she often “has” to replace yesterdays model with tomorrows. But as many products are furnished with new functions they use more power, hence their battery life is shortened. Because the Lithium-ion battery is so chemically advanced, it requires a sophisticated management system if it is to be fully utilized by the product.

In this report, the parameters of the Lithium-ion battery which are the reason for this strict management are explained. The explanation does not look into the underlying chemistry for them because that is beyond the scope of this report. But sources for further reading on the subject are included.

Different solutions for battery management are discussed and a Voltage-to-Frequency (VFC) converter is implemented in VHDL-AMS and simulated in ADVance-MS from Mentor[2]. The sources of error in the design are identified but dealt with in this report. This is not necessary before implementation in a CMOS-process has been shown possible. Simulations without component deviations are good, but once they are introduced, the converter shows that it is too sensitive for them. This can be solved utilizing digital error correction and calibration.

After the ideal simulations are performed, transistor level simulations for the circuit are performed. Different solutions and requirements for the various components in the Voltage-to-Frequency converter are looked into with respect to the results found while simulating the ideal circuit. It was found that the comparator should have hysteresis to avoid unwanted chattering in its output signal. The architecture was chosen and the comparator was simulated. It was found that this architecture provided some offset-voltage, but this can easily be compensated by subtracting the offset from its reference voltage. Digital calibration can also here be utilized, but this is not looked into.

Two high-gain op-amp architectures are looked into and simulated in this report, it was found that the two-stage used slightly more power than the two-stage op-amp with cascode-output, but they both provided approximately the same gain, even though the two-stage op-amp with cascode-output theoretically should provide about 100 times more gain. From this it is concluded that this architecture has a gain-limit independent of architecture used around 56dB.

It is concluded that the Voltage-to-Frequency-architecture looked into is not suitable for implementation in this CMOS-process and that another architecture must be found if a Voltage-to-Frequency converter shall be made for the architecture.

Abbreviations

C – Coulomb
COV – Cut-Off voltage
SD – Self-discharge
LIB – Lithium-ion Battery
CC – Constant Current
CV – Constant Voltage
SoC – State of Charge
C-C Coulomb-Counter
OEM – Original Equipment Manufacturer
ADC – Analog-to-Digital Converter
VFC – Voltage-to-Frequency Converter
CMRR – Common-mode rejection ratio
PSRR – Power Supply Rejection Ratio

Definitions

C-Rate(C):	The C-rate is defined as a charge or discharge current equal to the rated capacity of the specific battery in Ah. For example for a 500mAh battery, a current of 1 C equals 500mAh and a current of 0.5 C 250mAh. [1]
Cut-off voltage:	The cell voltage when the discharge is terminated. [1]
Self-Dischcarge:	Recoverable loss of capacity. Expressed as a loss of capacity in percent over a given time period at a given temperature, often one month. This is a major contributor to the batteries temperature dependency. [1]
SoC:	The State of Charge of a battery is its available capacity measured as a percentage of its rated capacity.

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1. Introduction

The Lithium-ion battery is today used by close to every portable battery powered device, and this marked is constantly increasing because not only are the products the consumer have had for years getting more and more sophisticated, so he or she often “has” to replace yesterdays model with tomorrows. But as many products are furnished with new functions they use more power, hence their battery life is shortened. Because the Lithium-ion battery is so chemically advanced, it requires a sophisticated management system if it is to be fully utilized by the product.

For the user of a battery powered device, he or she wants to be able to read out how much capacity is left in the battery. The device needs accurate battery measurement if it shall be able to provide the user with an accurate remaining battery life estimate.

In a Coulomb-Counter this is done by measuring the charge charged to or discharged from the battery. And storing these measurements in a register where so that the battery management always know how much the battery is charged or discharged and can compare this with the battery’s capacity stored in the system. From this ratio between capacity and the charge- and discharge registers, the device can accurately predict the remaining battery life.

The scope of the work performed is to look into why it is so important for maximum utilization of a Lithium-ion battery to have this accurate measurement, and how they can be obtained. Then an ideal simulation of a Voltage-to-Frequency analog front end for battery management is implemented in VHDL-AMS and simulated in ADVance-MS from Mentor[2]. Then this Voltage-to-Frequency converter shall be simulated in an Atmel® CMOS-process called 35K9 with intentions of use in a battery monitoring circuit. Here various solutions for the various components of the Voltage-to-Frequency converter must be looked into and simulated with respect to the requirements found for these components during the ideal circuit simulations.

If the requirements found during the ideal simulations for the various Voltage-to-Frequency-converter components can be met with this CMOS-process, non-idealities for every component in the circuit must be looked into and eliminated.

2. Battery capacity monitoring

Battery capacity monitoring is measuring the current State of Charge (SoC) of the battery and predicting the remaining battery life. Measuring the battery's SoC not only gives the user an indication on how long he or she can expect his mp3 player or portable computer to continue running before the battery is empty, it is also necessary to keep the use of the battery in the safe region. The following sections describe how sensitive the LiB is to its operating conditions thus implicating the necessity of an accurate for measuring the SoC for a battery.

2.1.1. Lithium-ion batteries

The Lithium-ion battery (LIB) is today the fastest growing and most promising battery for use in portable applications. Compared with other battery types used in portable devices, the LIB differs in man ways. The battery has a much higher cell-voltage (3.6V) compared with Ni-based batteries (usually 1.2V). The specific energy of the LIB is also relatively high compared with Ni-based batteries. These two factors make it possible to largely reduce the weight and size of the battery pack used in many applications[3]. One cell is often enough to provide sufficient voltage and capacity, and if a higher voltage is required, the amount of cells required is always smaller than if a Ni-based battery where used. The LIB has more or less totally replaced NiMH batteries in several applications. In the cellular phone marked already in year 2000 almost every cell-phone in Japan based on the PDC system was powered with a single Li-ion cell while GSM based phones where still mostly powered with NiMH-batteries[4]. Today Japanese cellular phones still run on Li-ion batteries and finding a new GSM-phone powered by a NiMH battery is close to impossible.
Portable computers, digital cameras mp3 players and almost every other type of consumer-electronics use LIB because of the high voltage and low weight. Common for all of these is that they use little power and have a relatively controlled environment. But the LIB is also gaining marked in power-demanding products as well. Battery-powered tools have traditionally used Ni-based batteries because of their robustness and ability to deliver large amounts of power fast. But the LiB's ability to deliver a higher voltage than Ni-based batteries makes it possible for the manufacturer to use a lower current, thus not exceeding the absolute limits for the battery and again producing lighter and stronger tools[5].

2.1.2. Pros and cons with Lithium-ion batteries

As mentioned in the previous chapter, the LiB voltage is higher than Ni-based batteries and has a better charge/weight ratio. In addition to these, the LiB has a third advantage, charging. With a LiB, there is no need for fully discharge of the battery in each cycle. Fully discharging the battery actually reduces the capacity and amount of cycles for the battery. There is also no need for a special first charge. When the battery is fully charged, it is ready for use. Partially recharging of the LiB is neither a problem. But the LiB also has disadvantages compared with other battery-types. The advantages and disadvantages will be discussed in the following chapters.

2.2. Charging of Li-ion batteries

The LiB has to be charged with a CC/CV regime. The battery is first charged with a constant current (CC) and then with a constant voltage (CV). This is illustrated in Figure 1.

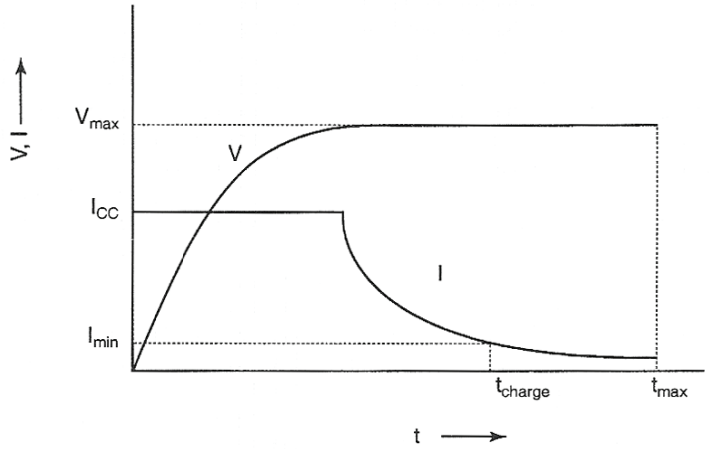

Figure 1: Constant Current, Constant Voltage charging regime[6].

Charging parameters V_{max} and I_{cc}

The maximum current and voltage is specified by the manufacturer of the battery. In CC mode the charge current (I_{cc}) can typically be in a range between 0.7C to 1.0C. The maximum voltage V_{max} depends on the battery type, also specified by the manufacturer of the cell. This voltage must be measured very accurate because exceeding it drastically reduces the batteries cycle life. Figure 2 illustrates how steep the reduction in cycle life is for a small change in maximum charge voltage V_{max} (the "Charging voltage").

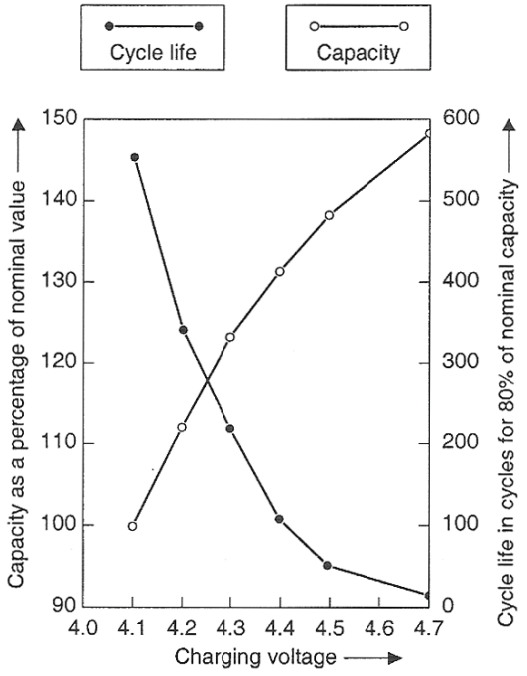

Figure 2: Maximum battery capacity as a function of charge voltage[7].

Figure 2 also illustrates the increase in the battery's capacity for a small change in V_{max}. The maximum charge voltage is thus a trade-off between requirements for cycle life and capacity. If V_{max} is increased from 4.1V to 4.2V, the increase in battery-capacity is from the rated 100% to approximately 113%, but it also decreases the number of charge/discharge-cycles from 550 to 350 which is almost a 40% reduction[8].

It must here be mentioned that an increase of I_{cc} above 1.0C hardly decreases the charge time. If the charge current is above 1.0C this only prolongs the time the battery experiences maximum charge voltage thus reducing battery cycle-life.

Charge cut-off parameters t_{max} and I_{min}

The charge cycle can be terminated depending on two parameters, either a maximum charge time (t_{max}) or a minimum charge-current (I_{min}). It is not indifferent which is chosen. A charge cut-off based on a maximum charge current results in a battery that is always charged to the same SoC if the temperature and internal impedance are the same. This current is usually chosen between 0.05C to 0.1C. If a maximum time is used to stop the charging, the battery will have a different SoC from charge-cycle to charge-cycle. If the battery is charged from 10% SoC with a given maximum charge time, the end SoC will differ from a battery charged from 40% SoC[8].

2.3. Discharging the Lithium-ion battery

Compared to other batteries, the LiB has strict requirements on how it must be discharged. The available capacity is also largely affected by the discharge current and the temperature, but this will be discussed more thoroughly in the "Degrading parameters that can be compensated for in the C-C" chapter. The LiB has an absolute minimum voltage, that if dropped below, the battery is not to be recharged. If compared to Ni-based batteries where the electronics shuts down below a preset voltage because it cannot operate below that voltage, the reason for the shutdown in a LiB-based system is much more important. If the battery drops below a voltage given by its manufacturer, it might be dangerous to recharge it due to the sophisticated chemistry it is based on. Frequently deep-discharging the LiB also speeds up the degradation of its capacity, which of course is not desired, but it is not dangerous. This is discussed further in the "Safety precautions" chapter.

Discharge rates

Because the LiB has an absolute minimum voltage, the experienced capacity decreases with an increasing discharge rate. Looking at an example with a temperature of 20°C and a discharge cut-off voltage of 3.3V the remaining capacity as seen in Table 1 is 265mAh with a discharge rate of 0.1C compared to the remaining capacity of 392mAh with a discharge rate of 0.7C. The result is that the same battery is experienced to have a capacity that is 130mAh (10%) less with the higher discharge rate. The battery is has a rated capacity of 1250mAh.

Table 1: Remaining Li-ion capacity in mAh vs. voltage and temperature with a 0.1C discharge rate[9]

Voltage (V)	Temperature (°C)								
	60	50	40	30	20	10	0	-10	-20
4.1	1240.17	1216.83	1195.83	1177.16	1157.33	1152.66	1100.17	1004.50	953.17
4.0	1053.50	1032.49	1016.16	1007.99	1009.17	1041.83	1069.83	1003.33	951.25
3.9	824.83	801.49	786.33	780.49	789.93	842.33	952.00	994.00	949.33
3.8	670.83	646.33	626.49	610.16	607.83	627.66	756.00	932.17	947.33
3.7	581.00	556.49	535.49	519.16	513.33	513.33	565.83	802.67	924.00
3.6	505.17	480.66	460.83	444.49	436.33	432.83	466.67	632.33	866.83
3.5	438.67	416.49	396.66	380.33	372.17	367.49	394.33	488.83	753.67
3.4	380.33	359.33	340.66	324.33	315.00	311.49	333.67	397.83	583.33
3.3	326.67	306.83	289.33	274.16	264.83	261.33	281.17	329.00	432.83
3.2	277.67	258.99	242.66	227.49	218.17	216.99	234.50	271.83	330.17
3.1	228.67	212.33	197.16	184.33	175.00	176.16	192.50	220.50	256.67
3.0	179.67	165.66	152.83	141.16	133.00	136.49	154.00	175.00	198.33
2.9	129.50	118.99	110.83	100.33	93.33	99.16	117.83	154.00	148.17

Table 2: Remaining Li-ion capacity in mAh vs. voltage and temperature with a 0.7C dicharge rate[9]

Voltage (V)	Temperature (°C)								
	60	50	40	30	20	10	0	10	20
4.1									
4.0									
3.9	1157.34	1148.00	1129.34	1082.67	1036.00				
3.8	980.00	989.33	1026.67	1045.34	1008.00	924.00	672.00		
3.7	756.00	774.67	830.67	933.34	961.33	914.67	668.83	214.67	
3.6	588.00	588.00	616.00	746.67	868.00	896.00	665.75	212.80	
3.5	494.67	485.33	494.67	560.00	700.00	877.33	662.67	210.94	37.33
3.4	420.00	410.67	410.67	438.67	513.33	830.67	648.67	209.07	35.46
3.3	354.67	345.33	345.33	354.67	392.00	653.33	634.67	207.21	33.60
3.2	298.67	289.33	289.33	298.67	317.33	457.33	611.34	205.34	31.73
3.1	242.67	242.67	242.67	242.67	252.00	317.33	588.00	186.67	29.87
3.0	196.00	196.00	196.00	186.67	196.00	233.33	420.00	177.34	28.00
2.9	158.67	149.33	149.33	149.34	149.33	168.00	289.33	163.34	18.66

Safety precautions

When a LiB is designed, there are a few tests regarding its safety the manufacturer can use for guaranteeing its stability. These tests are simulating different scenarios the battery might be exposed to during normal and extreme use. One of the tests is the UL 1642 which covers many of the potential risks a battery might be exposed for. But not all OEM use this test as it is not a mandatory test[10]. The UL 1642 test is continuously updated. Most tests available have been developed for scenarios such as dropping a cell, crushing it, short circuiting it and overcharging. The result if a test fails is overheating in the cell and thus the cell might immerse into fire or as a worst case scenario, explode[11]. A Lithium cell must therefore designed so that it can withstand both internal and external overheating.

But batteries passing these tests are still not safe if the manufacturer's safety requirements are not met. There are two boundary voltages which are never to be exceeded due to safety reasons and a maximum temperature if exceeded the battery shall be disconnected from the load or the charger.

3. Measuring the State of Charge

Until now this report gives a short explanation for some parameters with the LiB which results must be kept within a certain range. But it doesn't say anything about how it is done; only that it is necessary. There are basically two methods for measuring the SoC, either the battery voltage can be measured and SoC estimated from that or the current flowing in and out of the battery can be measured. The latter method is the only method providing the accuracy required by modern Lithium-ion batteries close to 100% utilization is required. Thus the first method is primarily used when a rough estimate for SoC is sufficient. The method for measuring the current is called Coulomb-Counting because one coulomb is defined as the amount of electric charge carried by a current of one ampere flowing for one second. In principle, current measuring or Coulomb-Counting (C-C) is method for counting the number of elementary charges (electrons) flowing in and out of the battery. There are two main approaches to the C-C method which are to be described in the following sections along with a short explanation of the voltage measurement method.

3.1. Battery voltage measurement

Only measuring the battery voltage has one advantage compared to C-C approaches. It is cheaper. But the disadvantages with this approach are so severe that it is practically never used where battery life is important. Table 1 shows the remaining capacity of a LiB for different temperatures and cut-off voltages. If looking at a typical example, with a temperature of 20°C and a cut-off voltage of 3.3V, the remaining capacity is here as much as 265mAh (21%). It is possible to add a temperature sensor and knowledge about the battery's discharge rate, but the added parameters actually makes the final solution more complex than a C-C based battery management system[12].

3.2. The fundamentals of Coulomb-counting

Coulomb-Counting measures and integrates the voltage over a series sensing resistor. Constant integration of the voltage across the sensing resistor, if any present, will finally reach a preset value. When this happens, a constant value representing the charge flow either added to or drained from the battery, either a Charge Counting Register (CCR) or a Discharge Counting Register (DCR) is modified respectively[13]. This is illustrated in Figure 3

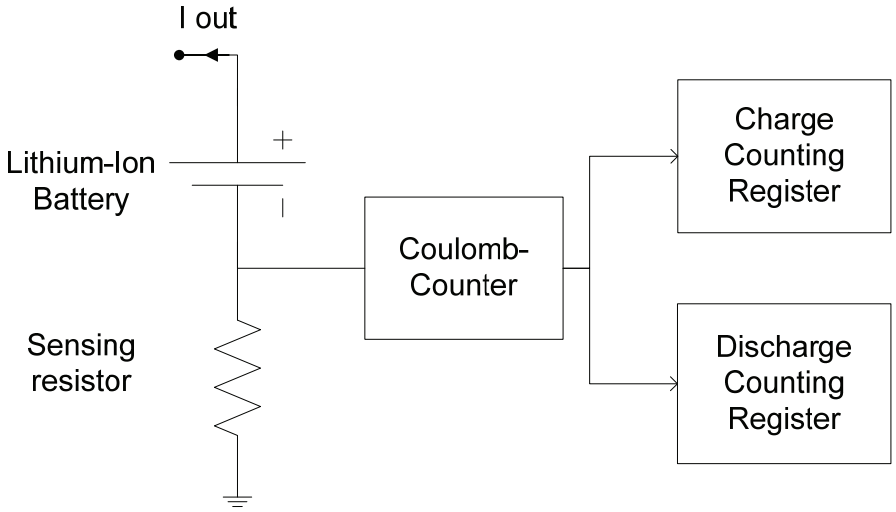

Figure 3: Block Diagram of a Coulomb-Counter

This is a book-keeping method where, in theory the remaining charge in the battery is always known. But because several parameters degrade the accuracy, temperature of and voltage across the battery is also measured and used for determining the present SoC. The temperature and the voltage are measured, and thus the battery's behaviour depending on these can be compensated. Compensating for other degrading parameters is also possible, but not always. It is neither always possible to fully compensate for them. The most important degrading parameters for LiB are listed below[14].

Degrading parameters that can be compensated for in the C-C

Available charge: Even if the battery's SoC is 100%, it might not be possible to fully utilize the available charge in the battery. This is depending on the discharge current and the battery's temperature. If a cold battery is discharged with a relatively large current (i.e. above 0.5C), the battery might drop below its minimum voltage before the DCR equals the CCR (the drained charge equals the added charge). It would still be possible to drain the remaining charge if the current is lowered or the battery's temperature is increased. But if the discharge current and the temperature remain constant, the measured SoC can be compensated for them, if known [14, 15].

Capacity loss: An old battery is never as good as a new one. This is due to the capacity loss experienced when a battery is ageing. This can be compensated with a full charge-discharge cycle. In such a cycle, the battery is first charged to 100% SoC. The DCR is then reset, and the battery is fully discharged. The value for DCR now equals the maximum available charge for a full battery and is thus its new capacity [14, 15].

Degrading parameters that cannot be compensated in the C-C

Self-discharge: Every battery is gradually discharging itself. Because this discharge is internal, there is no current flowing through the sensing resistor and the C-C cannot measure it. Although this is not a big problem because the battery can be recharged to a 100% SoC and thus the C-C will perform as expected again if the battery shortly after is used. The self discharge is strongly dependent on the SoC when the battery is left for storage and the storage temperature. A Li-ion battery should ideally be stored at 40% SoC in a cold environment [14, 15].

3.3. Coulomb-Counting techniques

There are two main categories of coulomb-counters; either an Analog-to-Digital Converter (ADC) approach, or a Voltage-to-Frequency Converter (VFC) approach. The ADC is a sampling system and the VFC is in integrating system. For a given bandwidth they can provide equivalent performance. If a large bandwidth is needed the integrating system (VFC) normally is more power-efficient[16]. The resistor can be placed on the positive side of the battery, called high-side current measuring, or placed on the negative side of the battery, called low-side current measuring. Both high-side and low-side current measuring has its disadvantages, and trade-offs must be made. Low-side current measuring result in additional resistance between the battery and ground, and for a high-side measuring system, the ADC must cope with a common mode voltage close to the battery voltage. For further reading on high- or low-side current measuring, [17] is recommended.

3.3.1. C-C-ADC

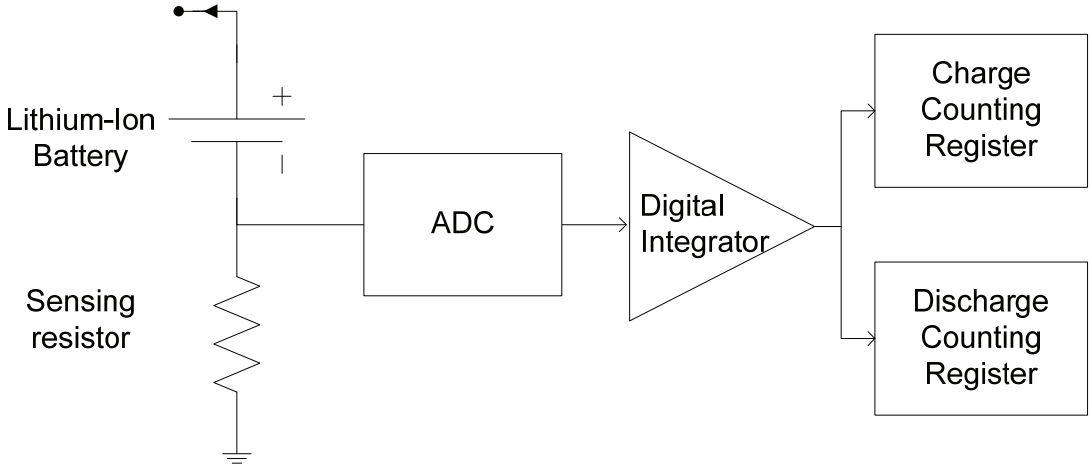

Figure 4: ADC C-C approach

For an ADC C-C, the voltage across the sensing resistor is sampled in an ADC. The ADC then outputs a digital value which is integrated digitally. When the integrated charge equals the minimum quantum of charge in the CCR or DCR, their value is updated.

Parameters degrading the ADC measurement accuracy

The performance of a CC-ADC is mainly affected by three factors; minimum voltage-resolution, offset voltage and gain error. The minimum voltage resolution can in the case of an ADC be stated as the least significant bit (LSB). The size of LSB only depends on the number of bits and the ADC's reference voltage. The formula for LSB is;

$$LSB = q = \frac{V_{ref}}{2^N - 1} \quad 1.$$

Where N is the number of bits and q is the minimum quantum of charge for the system. The problem with this error is that if the current drained from the battery is less then ½ LSB, the

system would register that as 0V, and thus no current drain. This is of course an extreme example, because a system where the smallest current is not registered would never be designed[13, 16].

Offset voltage, on the other hand is a major contributor to measurement error. But the offset voltage can be corrected to the nearest LSB. This requires calibration of the ADC where the output of the ADC, for an absolute zero input is measured. This deviation is then digitally subtracted from the ADC output. The worst case offset voltage error is;

$$V_{offset,max} = \pm\frac{V_{ref}}{2^{N+1}} \qquad 2.$$

and equal to the maximum quantization error. This correction of offset can be done by periodically adding or subtracting an appropriate number of LSB counts from CCR and DCR when an offset calibration command is issued. This eliminates the need for logic subtracting the error from ADC output signal, thus simplifying the design. The offset voltage error can in cases of long discharge times be significant unless q is very small[13, 16].

Gain error can be stated as a percentage deviation of the reported output from an ideal best fit straight-line output. The gain error can be constant when the error is descending from manufacturing deviations, but the error can also come from variations in the supply-voltage, temperature and nonlinearities in the output over the range of input voltages. The constant error can be digitally compensated, but the remaining gain error. It is therefore very important to have a very stable supply-voltage if high accuracy is required[13, 16].

3.3.2. C-C-VFC

An integrating VFC outputs a series of pulses where a certain number of pulses define 0V. The output pulse series can be linearly proportional with the input voltage, but not necessarily. If a small dynamic range, the output can be squared resulting in better accuracy[18]. As with the ADC, the pulses are converted to either charge or discharge counts in the CCR or DCR registers. The VFC has no theoretical minimum voltage resolution, but one register pulse still represent a quantum of charge. The minimum resolution is thus discussed more in terms of granularity[13].

Parameters degrading the VFC measurement accuracy

For the VFC, gain error due to variations in power supply, temperature and input signal amplitude contribute with most of the error. Because the VFC always integrates the input signal no information is lost, it merely takes longer time before one charge (q) is accumulated and either CCR or DCR is modified[13, 16].

4. Estimating the required resolution

It is possible to extract the needed resolution and speed and bandwidth from already available products and battery-life of modern cellular phones. The bandwidth is not a very important issue, because a low-pass filter can be utilized on the input reducing the bandwidth while not loosing any information.

4.1. A comparison of different currently available products

A random selection of battery management chips suitable for low-cost, low power applications with one Li-ion cell has been made, and their specifications are listed in Table 3.

Table 3: C-C specifications

Model	**V_{max}**	**Error/resolution**	**Type**
LTC4150[19]	±50mV	±150µV	High-side VFC
DS2745[20]	±51.2mV	±512µV (±1%)	ADC
Bq27000[21]	±100mV	±15µ	ADC

The three selected products have an error in the μV range. The bq27000 is the most accurate chip, but also the most expensive of the three so the comparison is rather unfair. All the errors are for maximum input swing so the error is not representative for a typical input signal. So based on this data, it seems sensible to estimate that a C-C for one lithium-cell must have an input-swing somewhere around ±50mV and an error below 250µV.

4.2. Estimating the needed signal swing V_{max} based on cell-phones

To estimate the needed signal swing it is necessary to look at the battery-life and capacity where the ratio between capacity and standby-time is the largest. A random selection of cell-phones has been made based on low prize and, low battery capacity and long standby time.

Table 4: Cell-phone battery life and capacity

Model	Battery	Talk-time	Standby time	Charge time
Nokia 6030	900mAh	3h	300h	
Nokia 1112	700mAh	3h 10 min	245h	
Samsung X650	800mAh	6h	250h	2.5h
Nokia 7360	760mAh	4h	450h	

The numbers are collected in Table 4, and it is the Nokia 7360 that has the standby-time compared with battery-capacity. With that is the smallest current is calculated to;

$$I_{min} = \frac{0{,}760Ah}{450h} = 1{,}69mA \quad (3.)$$

The largest current has to be calculated from the Samsung X650 because this is the only one with a stated charge time. The current is calculated to;

$$I_{max} = \frac{0{,}800Ah}{2{,}5h} = 320mA \quad (4.)$$

Current ratio

$$CR = \frac{320mA}{1{,}69mA} = 190 \quad (5.)$$

The reason for calculating the smallest current is that contrary to what stated in the "C-C-VFC" chapter, that the VFC can measure an infinitely small voltage, this is only valid for an ideal VFC. A real VFC will always have a lower limit for how small voltage it can integrate. The I_{min} and I_{max} values will be used when estimating the components in the VFC in chapter 6,

estimating the components in the VFC and in chapter 7, simulations on the ideal circuit, respectively.

5. Choosing the best VFC

There are many different VFC architectures which all have their advantages and disadvantages for this use. One architecture might have very good accuracy but use too much power. A different architecture might have the needed low-power properties but not the needed accuracy. The design used in [18] has an accuracy of about 0.02% of full scale and an 8kHz bandwidth, but the article doesn't mention the power consumption of the circuit. However it utilizes a 1024MHz clock, which uses much power and renders the design useless for a battery-powered application.

The design of a VFC can roughly be divided into two different categories, with or without feedback [22]. Usually a design with feedback is chosen, because such is known for having better accuracy and stability. It is also able to process a signal with lower amplitude. But feedback circuitry requires area, it dissipates power and increases the complexity of the circuit.

In 2006 an article with an "An All-MOS High-Linearity Voltage-to-Frequency Converter Chip With 520-kHz/V Sensitivity[23]" was presented. The design in this article has no feedback and no clock, still the linearity error is less than one percent at an input voltage range from 0.1 to 0.8V. The reason for this good result is of course a good design, but also the fact that a modern 0.25µm process is used manufacturing the chip. This result, and the knowledge that many old ADC designs are revitalized with modern manufacturing processes the chosen design has a low level of complexity.

The chosen design is a charge reset VFC with time-interleaved operation. With an ordinary charge reset VFC, shown in Figure 5, the charge drained from, or added to the battery when the switch S_1 is closed is lost.

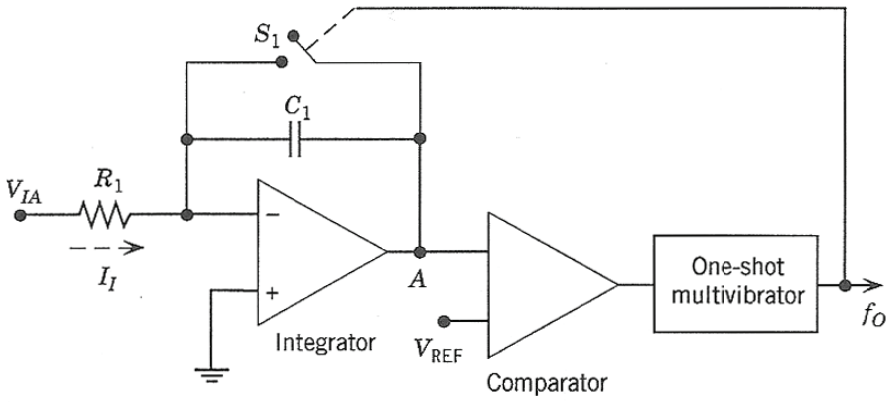

Figure 5: Charge reset VFC[24]

To avoid this problem, a time interleaved VFC, shown in Figure 6 is used. Using two alternating branches have several benefits. When the capacitor is reset, input is processed in the alternately working branch, thus the VFC is always processing the input signal. Time interleaved operation also increases the time available for the switches to reset the

accumulated charge. This relaxes the demand for low resistance when the switch is on, and a higher resistance switch uses less area, less power and has smaller parasitic capacitances. Op-amp bandwidth can also be narrowed. Narrow band (slow op-amps) op-amps are desired because they can have a large gain, and still use little area and power, compared with op-amps with the same gain and a wider bandwidth.

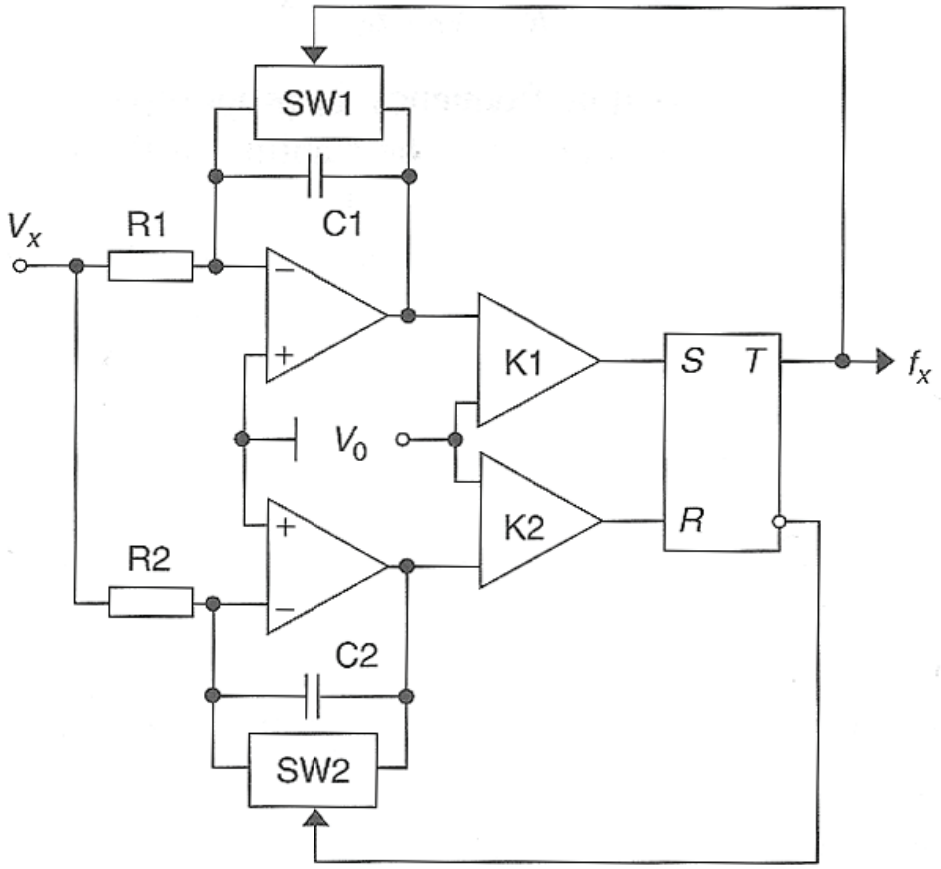

Figure 6: Time interleaved charge reset VFC[22]

6. Estimating the components in the VFC

Before simulating the VFC it is desirable to have good estimations for the component values, except for the S-R trigger and the comparators which operate digitally. It is also desired to have the threshold voltage V_0 as large as possible to minimize the possible influence of noise. But the op-amps must be able to provide this voltage with the lowest input voltage $V_{\_IN,MIN}$, and because the op-amp gain preferably should be as low as possible to minimize power use, this speaks for the threshold voltage to be as low as possible. The resistors R1 and R2 isolate the VFC from the battery and should have a large value, but they must also let enough current through to charge the capacitor fast enough. They are chosen to 2kΩ. The capacitors must be small to control the time it takes to charge them to V_0. Their value is chosen to 1.0μF.

From the "A comparison of different currently available products" chapter, the smallest current is calculated to 1.69μA. This value is calculated for a specific application, therefore some margin is needed. A current of 1.0μA is used. Assuming a threshold voltage V_0 of 0.5V and setting the sensing resistor (see Figure 4) to 100mΩ results in a needed op-amp gain of

$$G = \frac{0.5}{1.0mA * 100m\Omega} = 200000000 \quad (6)$$

which equals 166dB. Therefore the threshold voltage V_0 is set to a much lower value of 200mV. The closed switch resistance is chosen at 200Ω and the open switch resistance is chosen high.

7. Simulations on the ideal circuit

The simulations have been performed with component models with non-idealities included. This minimizes the difference between the VHDL-AMS high level simulations and later transistor level simulations. First all the components for the model were written, and then the system was build by adding one component at a time to the VFC. During this build-up, a test bench was written for every component added to ensure that the desired functionality is achieved. When the entire system was build and tested for basic functionality began the testing optimization of the system. Basically all of the estimated values had to be changed to achieve the wanted performance.

7.1. Test bench

The test bench for the entire system had to test its ability to cope both large and small input signals and its robustness to deviations in the VFC's components. The test bench is included in appendix one. First the test bench creates all the static parameters in the VFC. Here the test bench has a parameter called deviation, which is used if a percentage deviation from the ideal value shall be simulated. Then the different parts of the VFC is created and connected together. Then it provides the stimulus for the VFC. Here the current going through the battery is stepped from 1.0μA to 600mA. 600mA is used for the same reason as 1.0μA, the values are calculated for a specific product and margin is therefore needed. The VFC is simulated with many different component deviations, but mainly it is those where both components deviate and those for the op-amp which are really interesting. The cases where both component deviate are interesting because in CMOS it is easy to match two components with each other, but the deviation from the desired value (for both components) can be as much as 20%. These results are presented in Table 5 for op amp gain deviations and in Table 6 for randomly selected deviations. All the results are not presented here because of the large amount of simulation results. An example of the simulation results are presented as Appendix B.

Table 5: Deviations in op-amp gain

	Output frequency (Hz) and the deviation from ideal behaviour in percent								
Battery current	**Ideal gain**	**-5dB one op-amp**	**In percent**	**-5dB both op-amps**	**In percent**	**-10dB one op-amp**	**In percent**	**-10dB both op-amps**	**In percent**
$20\mu A$	0.33	0	N/A	0	N/A	0	N/A	0	N/A
$40\mu A$	1.0	1	0.0%	0.9	-12.5%	0	N/A	0	N/A
$60\mu A$	1.8	1.5	-14.0%	1.5	-14.0	1.25	28.9%	1.0	-42.9%
$80\mu A$	2.5	2	-20.0%	2.0	-20.0	2.5	0.0%	2.0	-20.0%
$100\mu A$	3.0	3	0.0%	3.0	0.0%	2.0	-33.3%	2.0	-33.3%
$500\mu A$	16	17	6.3%	16	0.0%	16	0.0%	16	0.0%
$1{,}0mA$	34	33	-2.9%	33	-2.9%	33	-2.9%	33	-2.9%
$10mA$	332	332	0.0%	332.	0.0%	332	0.0%	332.5	0.0%
$100mA$	3377	3377	0.0%	3377	0.0%	3377	0.0%	4477	0.0%
$200mA$	6847	6847	0.0%	6847	0.0%	6847	0.0%	6845	0.0%
$400mA$	14075	14080	0.0%	14075	0.0%	14080	0.0%	14080	0.0%
$600mA$	21730	21720	0.0%	21730	0.0%	21730	0.0%	21720	0.0%

Table 6: Deviations in component values

	Output Frequency (Hz) and the deviation from ideal behaviour in percent				
Battery Current	**Ideal gain**	**-10% deviation all components**	**Deviation in percent**	**+10% deviance one capacitor**	**Deviance in percent**
$20\mu A$	0.33	0.53	60%	0.27	-18%
$40\mu A$	1.0	1.5	50%	1.1	27%
$60\mu A$	1.8	2.3	28%	1.5	-17%
$80\mu A$	2.5	3.5	40%	2.5	0.0%
$100\mu A$	3.0	4.0	33%	3	0.0%
$500\mu A$	16	23	44%	15	-6.0%
$1{,}0mA$	34	45	32%	32	-6.0%
$10mA$	332	458	38%	318	-4.0%
$100mA$	3377	4643	38%	3215	-5.0%
$200mA$	6847	9462	38%	6523	-5%
$400mA$	14075	19555	39%	13410	-5.0%
$600mA$	21730	30490	40%	20700	-5.0%

7.1.1. Simulated component values

After simulation, the following component values were found

Table 7: Simulated component values (ideal simulations)

Op-amp gain	100dB
Input resistors	1000Ω
Sensing resistor	100m Ω
Closed switch resistance	200 Ω
Integrating capacitor	10.0ηF
Threshold voltage comparator	-150.0mV

7.1.2. Comments on the results and the simulation

The results show that the selected design is very sensitive for component deviations and in particular for deviations in op amp gain. Other error sources are discussed in chapter 8. This design can also apparently only be used for either charging or discharging of the battery because a negative input voltage in this circuit, as charging of the battery would result in, would cause the VFC not to work. This can easily be corrected by creating a common mode voltage or by using some digital logic in the input sensing negative input and thus adding a positive, known voltage.

8. Discussion to the ideal simulations

The simulation results presented in Table 5 and 6 show that the selected design is very sensitive for deviations in component values. Compensating for the large sensitivity for deviations in op amp gain can be done by utilizing an op amp with feedback controlling the op amp's gain. This introduces more circuitry and area, but it is necessary if a useable VFC is to be designed.

Other sources for error is deviation in the sensing resistor's value, variations in power supply and the threshold voltages used by the comparators. Deviations in these parameters will generate an error that is proportional with the deviation.

9. Analog devices theory

The following segments contain basic theory and properties on the devices utilized in this design. They are followed by a discussion on which properties to be emphasised while choosing designs suitable for the analog devices used in this VFC and suggestions for architectures to be simulated. Where the theory for the component differs between analog and digital use, the theory for analog use is used as this is an all-analog device.

9.1. Comparator

The comparator is probably the second most widely used analog component in electronic circuits, after operational amplifiers. It is widely used as an analog building block in a variety of applications from detecting the level of an input signal (denoted $v_{in}(t)$) compared to a preset reference voltage (denoted V_{REF}) to the design of analog-to-digital converters. What the comparator essentially does is comparing two analog voltages and providing a logical level output depending on whether the input level is larger or smaller than the reference voltage. In its simplest form the comparator can be considered as a one-bit analog-to-digital converter. The input-output transfer characteristics of a typical comparator are shown in Figure 7: **Ideal comparator transfer characteristics**.

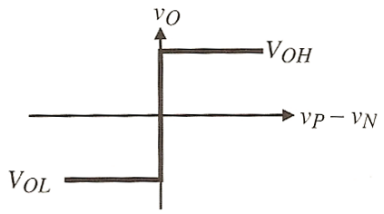

Figure 7: Ideal comparator transfer characteristics[25]

9.2. Comparator characteristics

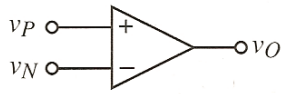

Figure 8: Comparator circuit symbol[25]

The comparator symbol in the figure above is the same as for an op-amp mainly because the comparator has many of the same characteristics of a high gain amplifier. If a positive voltage is applied to the $v_P$terminal, the output would reach its maximum positive output voltage, and if a positive voltage is applied to the v_N terminal, the output would reach maximum negative output-voltage. The maximum and minimum voltages output are defined as v_{OH} and v_{OL}respectively. But the transfer characteristics shown in Figure 7 are not feasible in CMOS circuitry as it requires a gain of infinity. The requirement for infinite gain is shown for a transition from $v_{OH}$to $v_{OL}$where ΔV approaches zero below.

$$A_{V.ideal} = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \qquad 7.$$

The transfer characteristics for a real comparator thus differ from an ideal comparator, and the gain for a real comparator can be found from looking at Figure 9.

$$A_{V,real} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \quad 8.$$

where V_{IH} and V_{IL} represent the input-voltage difference $v_P - v_N$ needed to saturate the output at its upper and lower limit, respectively. This input change is called the resolution of the comparator. This resolution is defined by the comparators gain because it defines the voltage-change required by the comparator to change from one output-level to the other. It is also important that the upper and lower output-voltage satisfy the requirements set by the digital logic the comparator is connected to. Common levels are 70 % and 30 % respectively.

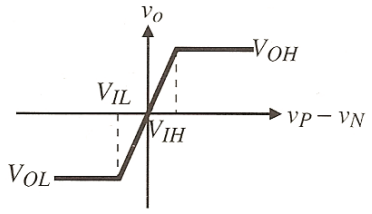

Figure 9: Transfer characteristics real comparator[25]

A second non-ideal comparator-effect is offset voltage, V_{OS}.

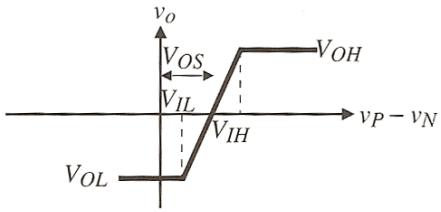

Figure 10: Comparator with offset[25]

If the output doesn't change when $v_P - v_N$ crosses zero until a value V_{OS}, the comparator is said to have an input-output offset. This offset is called V_{OS} and is illustrated in Figure 10. If this offset was constant from circuit to circuit this effect would not be a problem, because then it would be possible to compensate for it through digital correction logic. But because this is not the case, the input-output offset voltage makes the performance different even between neighboring comparators. The result of the offset voltage acts as noise because of its random nature and the fact that its polarity is not known. The result is illustrated in Figure 11 below. This figure also illustrates that V_{OS} is not known in polarity because the noise is evenly distributed around the y-axis.

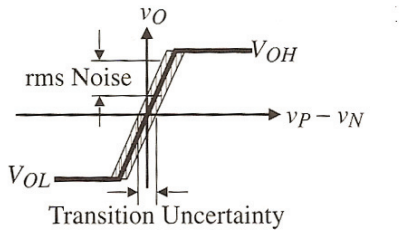

Figure 11: Comparator affected by noise[25]

A third effect that must be considered while designing a comparator for use in an analog environment is the effect of a slowly varying input-signal. If the response-time of the

comparator is much quicker than the variations in the input-signal and the input signal is around the threshold level; $v_P - v_N = 0$, the output of the comparator might enter a state where the output oscillates from v_{OH} to v_{OL}. Input-noise could also cause this effect with an input level around the threshold level. The result of this effect is illustrated in Figure 14(a) below.

9.3. Hysteresis

To eliminate this effect, positive feedback can be added to the comparator. The comparator will then experience an effect called *hystersis*, which will eliminate the oscillation behaviour. Comparators utilizing this technique are called Schmitt triggers. In this chapter the trigger points for the hysteresis for a simple positive feedback solution are found and the effects of hysteresis are illustrated.

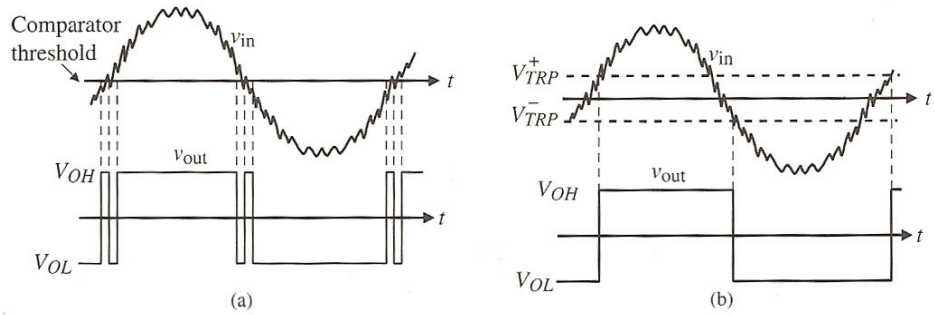

Figure 12: Output from a comparator with hysteresis[26]

The Schmitt trigger can be implemented using positive feedback in a differential comparator (see Figure 8 for the symbol of a differential comparator). The effect of hysteresis on the comparators response is illustrated in Figure 14 and new transfer characteristics can be seen in Figure 12(b).

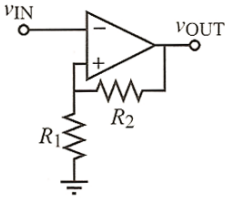

Figure 13: Comparator with positive feedback[27]

If the input voltage v_{IN} is assumed to be lower than the positive comparator input it the output state at V_{OH} can be defined. The upper trip point can be found by input equal to the voltage at the positive input of the comparator.

$$V_{TRP}^{+} = v_{IN} = \left(\frac{R_1}{R_1 + R_2}\right) V_{OH} \qquad 9.$$

And assuming that the input is greater than the voltage at the positive input of the comparator defines the output voltage as $V_{OL}$and therefore the lower trip point can be found by setting the input equal to the voltage at the at the positive input of the comparator. Thus

$$V_{TRP}^{-} = v_{IN} = \left(\frac{R_1}{R_1 + R_2}\right) V_{OL} \qquad 10.$$

And then the width of the bistable characteristics of the hysteresis-comparator can be found as

$$\Delta V_{IN} = V_{TRP}^{+} - V_{TRP}^{-} = \left(\frac{R_1}{R_1 + R_2}\right)(V_{OH} - V_{OL}) \qquad 11.$$

Adding hysteresis changes the comparators behaviour from having one detection-level to an upper (V_{TH}) and a lower (V_{TL}) detection level symmetrically placed about the reference voltage V_{REF}. The result of adding hysteresis is that a small change in the input signal doesn't cause any change in the output-level and the chattering effect is thus eliminated. This is illustrated in Figure 12**: Output from a comparator with hysteresis**(b).

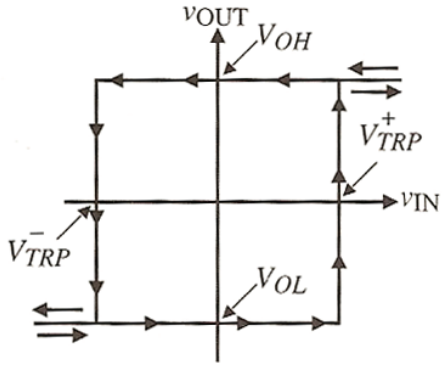

Figure 14: Comparator transfer characteristics with hysteresis[26]

9.4. Operational amplifiers

The CMOS operational amplifier is probably the most intricate, important and versatile building blocks in modern analog circuitry. The operational amplifier usually limits the high-frequency properties and the dynamic range of the circuit. It also consumes most of the power and must be thoroughly understood while estimating the behaviour of the entire circuit. It is also important to know which parameter is the most important when deciding the op-amp type most suitable for the selected task.

9.4.1. Non-ideal op-amps

The ideal op-amp has infinite gain, infinite input resistance, zero output resistance and is not affected by noise of any kind. But in reality, the gain is limited, the resistances only approach the desired values and the op-amp is affected by noise. These non-ideal effects are listed below under Non-ideal effects and then they are discussed as to which are important for this application. The symbol for an op-amp is shown in Figure 15 a, and the output voltage can be expressed as

$$v_{OUT} = A\_v(v_1 - v_2) \quad 12.$$

where A_v is the open-loop differential-voltage gain. v_1 and v_2 are the input voltages applied to the non-inverting an inverting terminals, respectively.

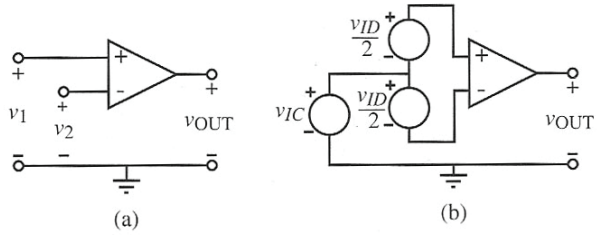

Figure 15: Differential amplifiers[28]

Non-ideal effects

1. *Finite gain.* For a real op-amp the gain is limited. Values for low frequencies gain, A, are typically between 60 to 100dB.
2. *Finite linear range*. The linear relation $v_{OUT} = Av_{ID}$, where v_{OUT} is the output voltage, A is the gain and v_{ID} is the input differential voltage.

   $$v_{ID} = v_1 - v_2 \quad 13.$$

   This relation is only valid for a limited range. The maximum output voltage is usually limited somewhat below the positive supply voltage and the minimum output voltage is limited to just above the negative supply voltage.

3. *Offset voltage.* For an ideal op-amp, a zero input voltage i.e. $v_{id} = 0V$, the output voltage should be exactly zero also. But for a real device, this is not exactly true resulting in an output voltage $v_{OUT,OFF} \neq 0V$ with zero input voltage. Zero input voltage can easily be obtained by shorting the two input terminals. The output offset voltage is usually directly proportional to the op-amp gain. For convenience, a voltage $v_{IN,OFF}$

can be defined. This is the voltage required on the input terminals to restore an output voltage; $v_{OUT} = 0V$ in a real device.

4. *Common-Mode Rejection Ratio (CMRR)*. The *CMRR* is an important measurement as it measures the ability to suppress noise in differential op-amps. The common-mode input voltage v_{IC}, is defined as the average value of v_1 and v_2 given by the following equation where v_1 and v_2 are defined in Figure 15.

$$v_{IC} = \frac{v_1 + v_2}{2} \tag{14.}$$

The output voltage from a differential amplifier can be expressed in terms of its differential-mode- and common-mode input voltages as

$$v_{OUT} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 - v_2}{2}\right) \tag{15.}$$

where A_{VD} is the differential-mode gain and A_{VC} is the common mode gain. The ± sign implies that the polarity of this voltage gain is not known beforehand. And as the only objective of a differential op-amp is to amplify v_{ID} and not v_{IC} it is possible to characterize the op-amp by its ability to reject the common-mode voltage, thus the term *Common-Mode Rejection Ratio*. The *CMRR* is defined as the ratio of the magnitude of the differential gain to the common-mode gain. The *CMRR* is typically denoted in dB and the equation is as follows;

$$CMRR = 20\log\left(\frac{A_{VD}}{A_{VC}}\right) \tag{16.}$$

5. *Frequency response*. The gain of an op-amp is not only limited to an upper level in terms of magnitude, but also in frequency. Because of stray capacitances, finite carrier mobility and other effects op-amps gain diminishes as the frequency increases. The frequency response can be described in terms of unity-gain bandwidth and a 3-dB bandwidth. The unity gain bandwidth is a frequency where the output-voltage of the op-amp has the same magnitude as the input-voltage, thus the term unity. The 3-dB bandwidth is the point where the frequency response is 3dB below the DC gain. These effects are illustrated in Figure 16 below. The unity-gain bandwidth is at the intersection between the plot and the *x-axis*.

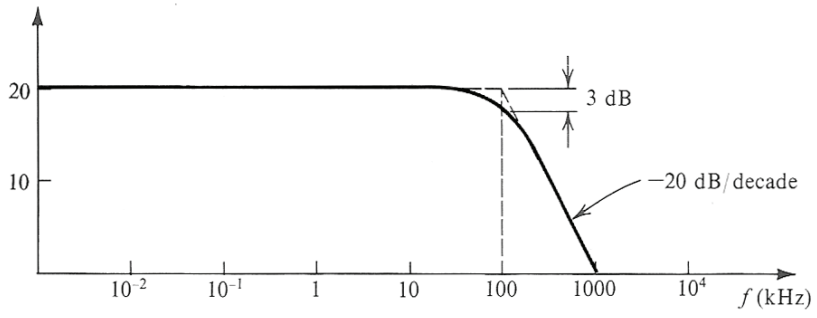

Figure 16: Op-amp gain bandwidth[29]

6. *Slew Rate*. The slew rate is defined as the maximum allowable rate that the output voltage can change. The slew rate is defined by

$$SR \triangleq^{\text{def}} \frac{dv_{OUT}}{dt}|_{max} \quad 17.$$

The reason for this limitation is that if the op-amp is imprinted by a large DC input step voltage, some transistors in the op-amp might be driven out of saturation or cut off completely. The result of such action would be that the output follows the input at a slower finite rate than the input pulse. The slew rate is thus defined with respect to the output voltage, and limits the change-rate the op-amp can be imprinted.

7. *Nonzero Output resistance*. For an ideal op-amp the output resistance would be zero ohms. But for a real amplifier this is not the case. This limits the maximum output current and thus the speed and frequency an op-amp can deliver with a capacitive load.
8. *Noise.* The MOS-transistor generates noise. It is normally described as if the transistor were noise-free with a noise source connected in parallel with the transistor gate. A MOS-transistor generates two different types of noise, white- and flicker-noise. White noise has a constant spectral density over a given frequency i.e. a white noise signal would have a flat signal spectrum. This is shown in the following figure.

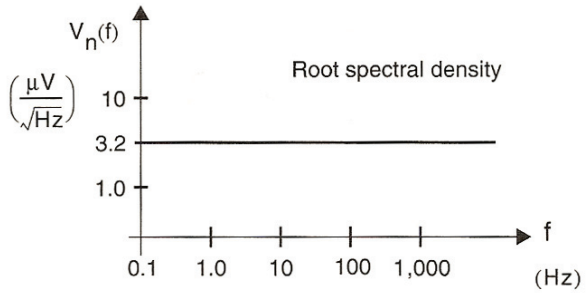

Figure 17: White noise[30]

Where $V_n(f)$ is given by

$$V_{n(f)} = V_{nw} \quad 18.$$

V_{nw} is the white noise voltage.

1/f noise or flicker-noise has a spectral density approximated by

$$V_f^2 = \frac{k^{2v}}{f} \quad 19.$$

where k_v is a constant. Thus the spectral density is inversely proportional to the frequency and hence the term 1/f noise. The effect of both 1/f- and white noise is shown in Figure 18. It can be noted that the 1/f noise drops 10 dB/decade since it is inversely proportional with the frequency. The intersection between the flicker noise and the white noise is called the 1/f noise corner. [30]

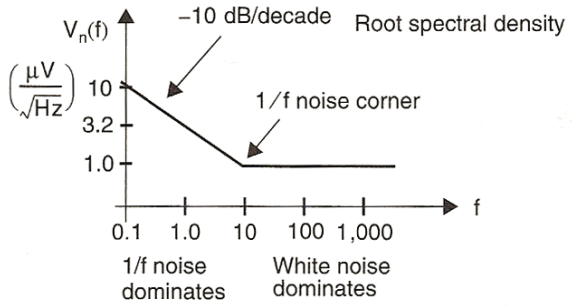

Figure 18:Flicker and white noise[30]

9. *Dynamic Range*. The op-amp input range is restricted between a minimum and a maximum voltage. The maximum voltage $v_{IN,MAX}$ an op-amp can handle without generating an excessive amount of nonlinear distortion can roughly be estimated to

$$v_{IN,MAX} \approx \frac{V_{CC}}{A} \tag{20.}$$

where $\pm V_{CC}$ is the supply voltage and A is the open loop gain. This is an optimistic estimate because it doesn't consider threshold voltages and other non-ideal effects. The minimum input voltage $v_{IN,MIN}$ is result of spurious signals (noise and clock-feedthrough) and low level distortion such as crossover distortion. If the op-amp is imprinted with a signal below the minimum input voltage, the signal drowns in noise and distortion. The minimum voltage is usually in the same order of magnitude as the equivalent input noise $\sqrt{V_n}$ (18). The dynamic range is defined as

$$Dynamic\ Range = 20\log\left(\frac{v_{IN,MAX}}{v_{IN,MIN}}\right) \tag{21.}$$

and it is measured in decibels. It is possible to increase the op-amps dynamic range by operating it in a closed loop with negative feedback. Typical values for an open-loop op-amp is 30 to 40 dB, and for a closed loop up to 90 dB is obtainable. If an even greater dynamic range is required, this is possible through cancellation of low frequency 1/f noise. This can be seen in Figure 18, where 1/f noise is dominant on the left side of the noise corner. Cancellation of this noise lowers $v_{IN,MIN}$ and thus increases the dynamic range.

10. *Power Supply Rejection Ratio (PSRR)*. The PSRR is as the product of the ratio of the change in supply voltage to the output voltage due to the change in power supply voltage and open-loop gain of the op-amp. The PSRR is commonly expressed in decibels.

$$PSRR = 20\log\left\{\frac{\Delta V_{dd}}{\Delta V_{OUT}} A_v(s)\right\} \tag{22.}$$

11. *DC Power Dissipation*. Contrary to ideal op-amps real op-amps dissipate power from the power supply.

[31], [32]

10. General op-amp design

In general, an operational amplifier can be said to consist of three stages; the input stage, a high-gain stage and an output stage. The output stage is mainly used if a resistive load is to be driven and thus often not necessary if the amplifier is used on-chip. If the last buffer stage is excluded, the op-amp is usually called an operational transconductance amplifier (OTA). This chapter will discuss the two first op-amp stages. Different design-approaches and properties mainly relevant for designing the op-amp for this VFC are also discussed. The third stage is not discussed because this design will not be connected to a resistive load and thus this stage is not included in the design. The three stages are illustrated in Figure 19 below.

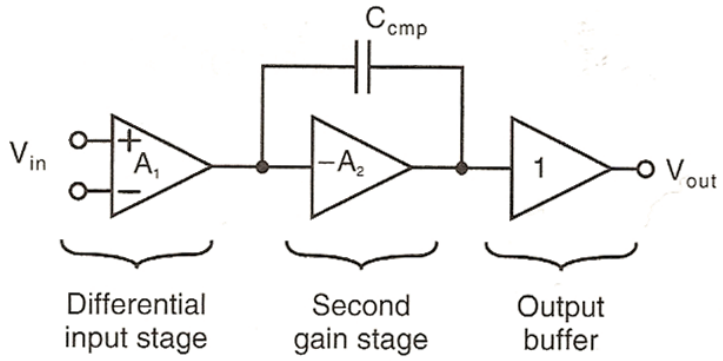

Figure 19: Two stage op-amp block diagram[33]

10.1. Considerations regarding this design

As summarized in Table 7, this design requires a closed loop op-amp gain of 100 dB to obtain the required accuracy and input swing. The primary object selecting op-amp architecture is therefore finding the architecture with the most gain possible. It is also important that the chosen architecture is power efficient and simple. Therefore op-amp architectures known for having large gain are looked into. The other effects listed under chapter 9.4.1 must also be considered, but the primary objective of maximizing the gain is the first parameter to be simulated. Because this circuit is going to operate with very low frequencies, op-amp compensation has not been emphasized.

10.2. The two-stage op-amp

For this VFC it was found through ideal simulations that the op-amp's closed-loop-gain would have to be approximately 100dB to manage the required resolution. Thus several op-amp architectures were looked into and simulated. It was found that the two-stage op-amp and the two-stage op-amp with cascode output gave the best gain and thus they are presented in this report. This chapter looks into the two-stage op-amp.

10.2.1. Input stage

The differential input stage is the most widely used input stage due to its versatility in analog circuit design. The differential input stage is often realized using a differential transistor pair as the differential input combined with a current mirror used as a load and a differential to single ended converter. In Figure 19, these functions are included in the differential input stage, but this is not necessarily always the case.

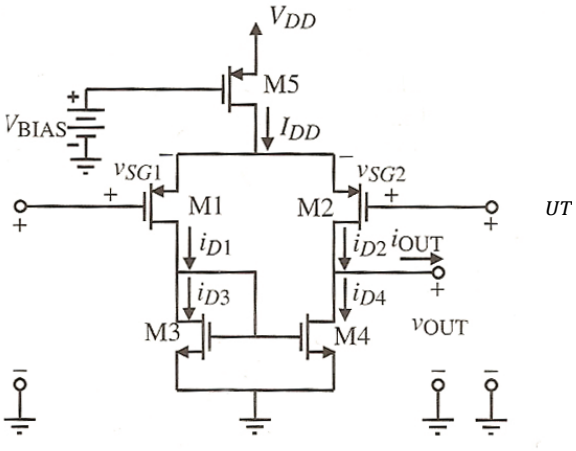

Figure 20: Differential input stage[34]

The low frequency gain A_1 of the first stage is given by [35]

$$A_1 = g_{m1}(r_{ds2}||r_{ds4}) \tag{23.}$$

and from this relationship one of the difficulties designing the input stage is evident. Because both the transconductance g_{m1} and the drain-source resistance of a transistor are dependent on the same parameter I_D as shown in equation (24) and (25), simulations are required to find the ideal transistor-sizes and bias current.

$$g_{m1} = \sqrt{2\mu_1 C_{OX}\left(\frac{W}{L}\right) I_D} \tag{24.}$$

$$r_{DS} = \frac{1}{\lambda I_D} \tag{25.}$$

I_{DD} from Figure 20 can be expressed with respect to I_D using the following relation

$$I_{DD} = I_D + I_D \tag{26.}$$

where $i_{D1,}$ i_{D2}, i_{D3} and i_{D4} from Figure 20 equals I_D from equation (26).

n-channel or p-channel input stage

It is possible to realize an op-amp with either an n-channel input stage or a p-channel input stage. This choice depends on the op-amps intended use and several trade-offs. The gain of the entire op-amp is largely unaffected because an n-channel input stage would be followed by a p-channel gain stage and vice versa.

For a given power dissipation, using a p-channel input stage maximizes the slew rate, a result that can be seen from

$$SR = \frac{2I_{D1}}{\sqrt{2\mu_p C_{OX}\left(\frac{W}{L}\right)_1 I_{D1}}}\omega_{ta} = V_{eff1}\omega_{ta} \tag{27.}$$

which is derived from equation (17) for an op-amp with p-channel input stage, hence the $\mu_p$notation. But the result; $SR = V_{eff1}\omega_{ta}$ is equal for an op-amp with an n-channel input stage. Since the p-channel input transistor has a larger V_{eff}than the equivalent n-channel the slew rate is improved using the p-channel input solution. The term equivalent here means that both transistors have been optimized for maximum gain. This difference is probably the main reason why the p-channel input stage often is preferred.
Although this design will not require operation at high frequencies, the different frequency characteristics between p- and n-channel input stages, it is such an important property in general op-amp design that it must be mentioned here. The result of using a p-channel input stage combined with a second stage that has n-channel drive transistors is that the transconductance of the second stage is maximized. This is an important feature because the second stage equivalent pole and thus also the unity-gain frequency is proportional to the second stage transconductance. The higher transconductance also reduces the effect of a capacitive load on the op-amps frequency response.
Because choosing between p- or n-channel input-stage transistors directly affect the type of output source follower used, this is another feature that must be considered. Choosing a p-channel input stage requires an n-channel output stage, and this is often preferable because it has a lower voltage drop. There is one disadvantage with having an n-channel output stage drive transistor. That is for an n-well process, it is not possible to connect the source to the substrate, and thus the output voltage-drop cannon be minimized.
The choice of input stage also affects the op-amps noise characteristics. Using a p-channel input stage minimizes the 1/f noise because their majority of charges are holes. But for thermal noise it is important to have a large transconductance input stage because all noise is referred to the input of the device. This means that if minimizing thermal noise is important, using a modern architecture such as folded-cascode must be considered. [36],[37]

10.2.2. The gain stage

The second stage or the gain stage of a two-stage amplifier consists of Q_7which is a common source amplifier actively loaded with Q_6. A capacitor C_C is normally included in the negative feedback path of the second stage to enhance the miller effect already present in Q_6. The capacitor thus provides the amplifier with a dominant pole which if placed correctly can make the op-amp gain decrease with 6 dB/octave down to the unity gain frequency. The benefit of such behaviour is that this amplifier is guaranteed to operate in a stable fashion with nearly all possible feedback connections.

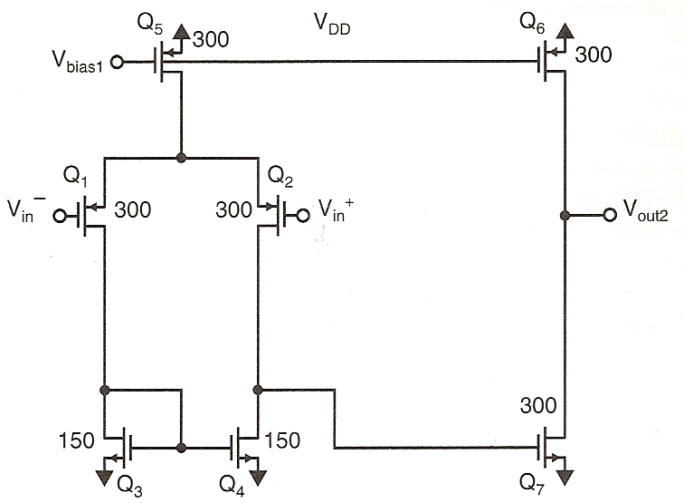

Figure 21: Two stage op-amp input and gain stage

The output resistance of this stage is equal to $r_{ds1}||r_{ds2}$ i.e. the output resistance is quite high. This is the reason why this stage is followed by a buffer stage if a resistive load is to be driven. But it is also why this rather simple design can manage such good results in a very small chip area. The voltage gain for the first stage was shown in (23) and the gain in the second stage is similarly

$$A_2 = g_{m6}(r_{ds6}||r_{ds7}) \tag{28.}$$

The overall DC open-loop gain of the op-amp is the product of A_1 and A_2.

[38]

Systematic offset voltage

In this section all transistor references are related to Figure 21. When designing a two-stage CMOS op-amp it is important to avoid a systematic input-offset voltage. To avoid a systematic input-output offset voltage, the output of the first stage with $V_{ID} = 0$ must equal the voltage required to make I_{D7} equal its bias-current I_{D6}. This implies that the voltage V_{GS7}must be given by

$$V_{GS7} = \sqrt{\frac{2I_{D6}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_7}} + V_{tn} \tag{29.}$$

When $V_{ID} = 0$, the output voltage of the first stage is given by

$$V_{GS7} = V_{DS3} = V_{DS4} \tag{30.}$$

This is the voltage required to satisfy (29) and if this value is not satisfied, the output of the second stage would reach either negative or positive rail due to the high gain in the circuit. The gate-source voltage of $Q_4$is given by

$$V_{GS4} = \sqrt{\frac{2I_{D4}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_4}} + V_{tn} \qquad 31.$$

From (29) and (30) it can be found that the condition required for zero input-offset voltage is

$$\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5} \qquad 32.$$

It must be noted that this analysis ignores the voltage drop of a possible level-shifter output stage and any mismatch between the output impedances of the p- and n-channel transistors. Fortunately, these effects cause only minor offset voltages and an offset voltage below 5mV can be obtained if (32) is satisfied.[39]

10.3. Two-stage op-amp with cascode output

There are three ways to increase the gain of an op-amp.

1. Add additional gain stages
2. Increase the transconductance of the first or second stage
3. Increase the output resistance seen by the first or second stage

The first approach is not attractive as it increases the possibility of unstable operation. Of the two latter, the last one is the most desirable as an increase of the transconductance would create a squared increase of the bias current whereas an increase of the output resistance proportionally decreases the bias current. Thus it is generally more efficient to increase the output resistance rather than the transconductance. This increase can be made by using circuit techniques like cascode structures.

The cascode amplifier has two distinct advantages over the two stage op-amp. First it provides a higher output resistance and second it reduces the effect of the Miller capacitance on the input of the amplifier. The second benefit is very important when designing the frequency characteristics of the amplifier. The cascode architecture is also seldom used in combination with an output buffer rather than as an OTA.

To further increase the gain of the cascode op-amp, a second stage can be added similarly to the one used for in two-stage op-amp discussed under 10.2.2. But one of the disadvantages with this solution is that the compensation is more complicated than for the single-stage folded cascode op-amp.

It is therefore advantageous to move the cascode to the second stage, resulting in an op-amp like the one shown below in Figure 22.

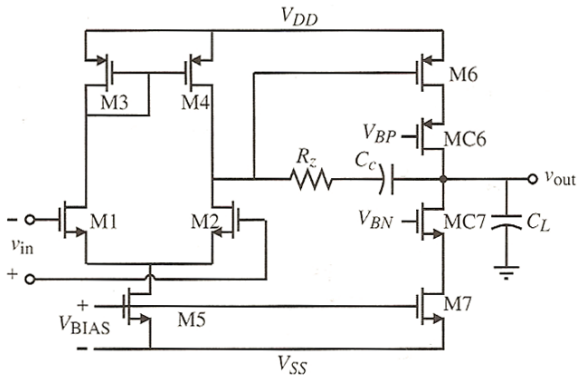

Figure 22: Two stage op-amp with cascode output stage[40]

The overall gain of this circuit is

$$A = g_{mI} g_{mII} R_I R_{II} \tag{33.}$$

Where

$$g_{mI} = g_{m1} = g_{m2} \tag{34.}$$

$$g_{mII} = g_{m6} \tag{35.}$$

$$R_I = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4) I_{D5}} \tag{36.}$$

and

$$R_{II} = (g_{mC6} r_{dsC6} r_{ds6}) || (g_{mC7} r_{dsC7} r_{ds7}) \tag{37.}$$

Compared with the gain of an ordinary two-stage op-amp this architecture should obtain an increase of gain of approximately 100(magnitude). Although this might lead to decreased stability, the ability to increase the gain with such a factor makes it an interesting architecture for simulation. [41],[42]

11. Analyses performed prior to simulating the circuits

This circuit was designed for a CMOS called 35K9 which is developed by Atmel® primary for use with digital logics. It is a 25μm process. This process is very new and no parameters for use in hand calculations were available, thus calculations were performed before simulating the circuits.

11.1. Comparator

The chosen comparator consists of a source-coupled differential pair with positive feedback and a differential-to-single-ended converter. For this circuit the hysteresis is given by

$$\Delta V_{IN} = V_{TRP}^{+} - V_{TRP}^{-} = 2 \times \sqrt{\frac{I_O}{k'\left(\frac{W}{L}\right)_1}} \left(\frac{\sqrt{\alpha} - 1}{\sqrt{1+\alpha}}\right) \quad 38.$$

Where α is given by

$$\alpha = \left[\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_3}\right] = \left[\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4}\right] \quad 39.$$

α is called "the positive feedback factor". For $\alpha < 1$ the input stage behaves as a gain stage, for $\alpha = 1$, the circuit becomes a positive feedback latch and for $\alpha > 1$ the input stage becomes a Schmitt-trigger where the hysteresis is given by (38). Thus should the ratio $(W/L)_5$ be bigger than $(W/L)_3$ and $(W/L)_6$ be bigger than $(W/L)_4$ for this circuit to operate with hysteresis. The circuit is shown below in Figure 23 where Q_1 to Q_6 represent the input stage, Q_8 and Q_9 the differential to single-ended converter and Q_0, Q_9 and Q_{10} the bias circuitry. All transistors were minimum-sized prior to the simulations, except Q_5 and Q_6 which were chosen to have twice the width of the minimum-size transistor.

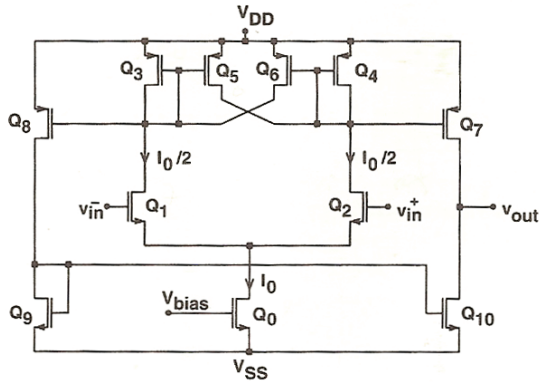

Figure 23: Complete schematic of comparator with hystersis[43]

11.2. Op-amp

No analyzes were made prior to simulating the op-amps except it was ensured that equation (27) was satisfied, because no parameters for hand-calculations were available for this process.

12. Analog simulations and simulation-results

The circuit from Figure 6 was built in Cadence using Virtuso Schematic and Analog Artist. The circuit was drawn in Virtuso Schematic and a spice netlist were created using Analog Artist. This is illustrated in Figure 24**: VFC-circuit created with Virtuso Schematic** below. Simulation-results were extracted using Mentor's EZ-wave's built in graph calculator.

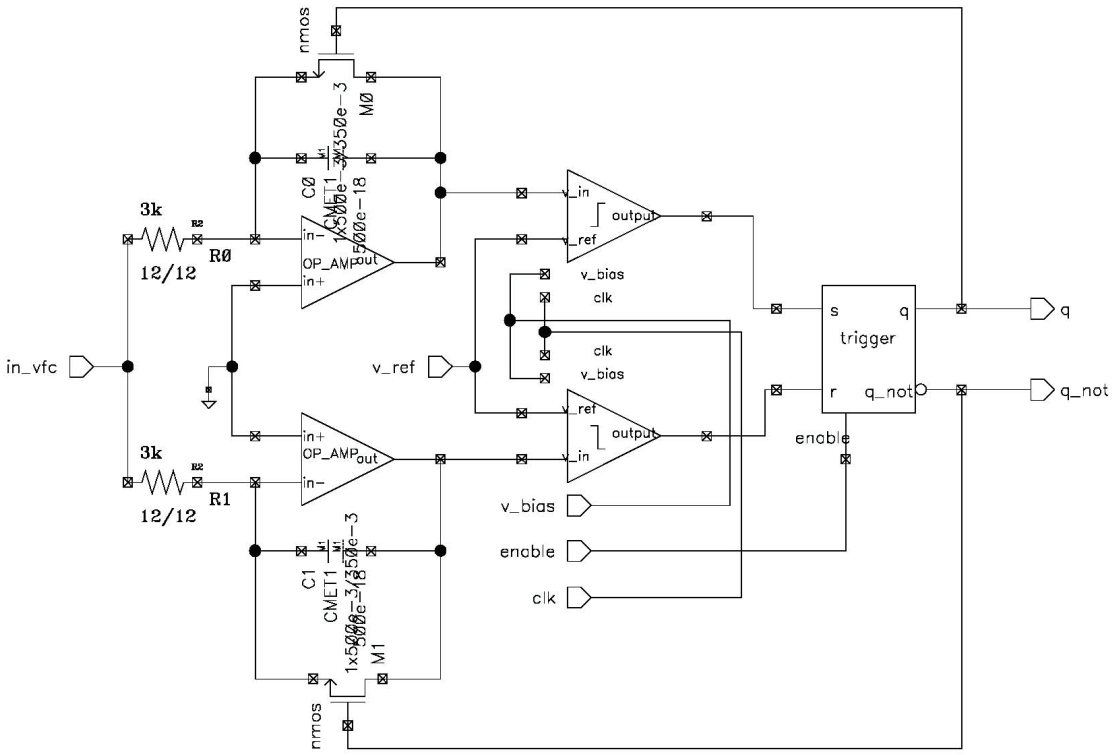

Figure 24: VFC-circuit created with Virtuso Schematic

12.1. Simulations and results

12.1.1. Triggers and switches

The trigger is based on components from the integrated library in Cadence and they are thus not discussed further here. For the switches, minimum size transistors where used. It is assumed that these components work until otherwise proven.

12.1.2. Comparator

The comparator was simulated according to the conditions presented in chapter 11.1. After some fine-tuning of the parameters it was found that deviating from the condition for α (presented in 11.1) and using the component parameters presented in Table 8 gave a suitable ΔV (equation (38)) for this application. The D-latch is added to synchronize the signals from the comparator with the clock used on the Smart-battery-chip. This is also an included device from Cadence and its function is thus not looked further into. The simulated circuit is presented below in Figure 25 where the D-latch is presented as the box on the right hand side.

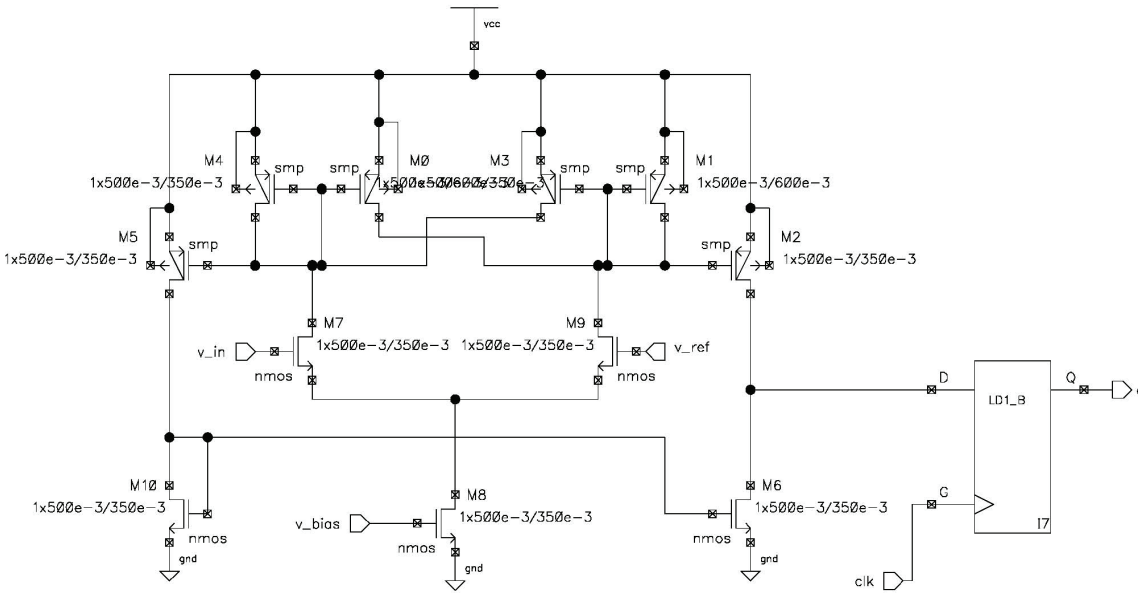

Figure 25: Comparator hysteresis

Table 8: Simulation results for the hysteresis comparator component parameters

Parameter	Dimension
$W_{0,1,2.3.4,5,6,7,8,9,10}$	$\mathbf{500e-3}$
$L_{0,1,2,3,4,5,6,7,8,9,10}$	$\mathbf{350e-3}$

This comparator was simulated with a threshold voltage of 0,5V. Its trip-voltages and ΔV are presented in Table 9 below. One of the plots used for finding the results is included for illustrative purposes as Appendix 0-b).

Table 9: Simulation results for the hysteresis comparator voltages

Trip voltage	Value
V_{TRP}^{+}	$\mathbf{0,588V}$
V_{TRP}^{-}	$\mathbf{0,445V}$
ΔV	$\mathbf{0,143V}$

The results show that ΔV is not entirely symmetrical around the threshold voltage so there is a slight offset-voltage, $\frac{(0{,}588+0{,}445)V}{2} - 0{,}5V = 0{,}0165V$. This can be compensating when converting the output-frequency to current utilizing digital error correction or it can be compensated by changing the threshold voltage equivalently to the offset-voltage.

12.1.3. Two-stage-op-amp

The two-stage op-amp simulated was first simulated with transistor-dimensions satisfying (32) but after simulating the op-amp, it was found that the transistor-sizes in Table 10 gave more gain. The increased input-output offset was compensated by increasing the threshold level above the offset voltage. The maximum gain was found to be $55{,}8dB$ and the power-consumption $2{,}18e-8W$. The results are presented in Table 11. The output from EZ-wave is included as Appendix C - c).

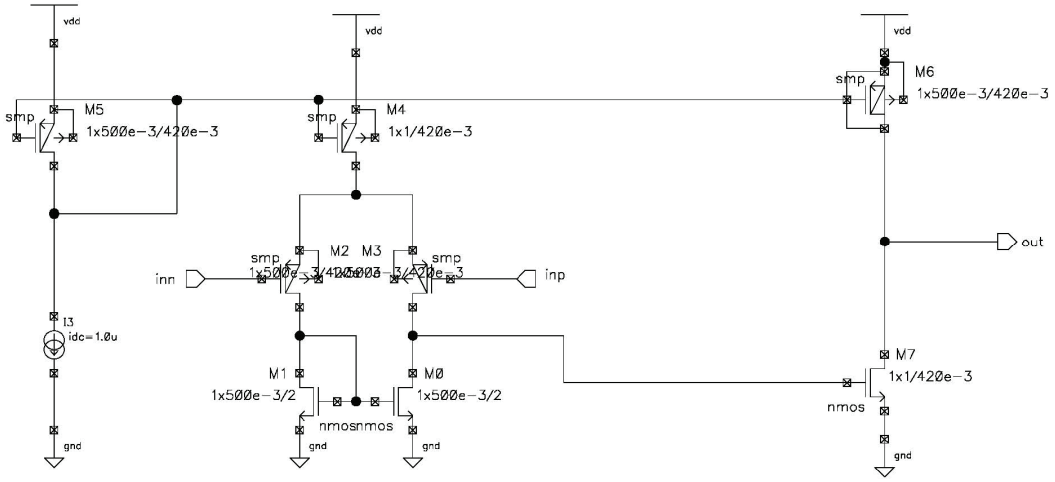

Figure 26: Two-stage op-amp created with Virtuso Schematic

Table 10: Simulation results for two-stage-op-amp parameters

Parameter	Dimension
$bias\ current$	$\mathbf{1e-9}$
$W_{0,1}$	$\mathbf{500e-3}$
$L_{0,1}$	$\mathbf{2000e-3}$
$W_{2,3}$	$\mathbf{500e-3}$
$L_{2,3}$	$\mathbf{420e-3}$
W_4	$\mathbf{1000e-3}$
L_4	$\mathbf{420e-3}$
w_5	$\mathbf{500e-3}$
L_5	$\mathbf{420e-3}$
W_6	$\mathbf{500e-3}$
L_6	$\mathbf{420e-3}$
W_7	$\mathbf{1000e-3}$
L_7	$\mathbf{420e-3}$

Table 11**:** Results for the two-stage op-amp

Parameter	Value
$Maximum\ gain$	$\mathbf{55,8dB}$
$Power\ consumtion$	$\mathbf{2,18e-8W}$

12.1.4. Two-stage-op-amp with cascode output

The two-stage op-amp with cascode output from Figure 22 was converted to p-channel input transistors according to the discussion in 10.2.1 - n-channel or p-channel input stage. The input stage and bias current from the two-stage op-amp in 12.1.3 was used as basic for the simulations on this op-amp. Then the op-amp was optimized for maximum gain. The result was a gain of $56{,}8dB$ and a power consumption of $9{,}01e-10W$. These results are presented in Table 13 and the EZ-wave plot is included as Appendix C - d).

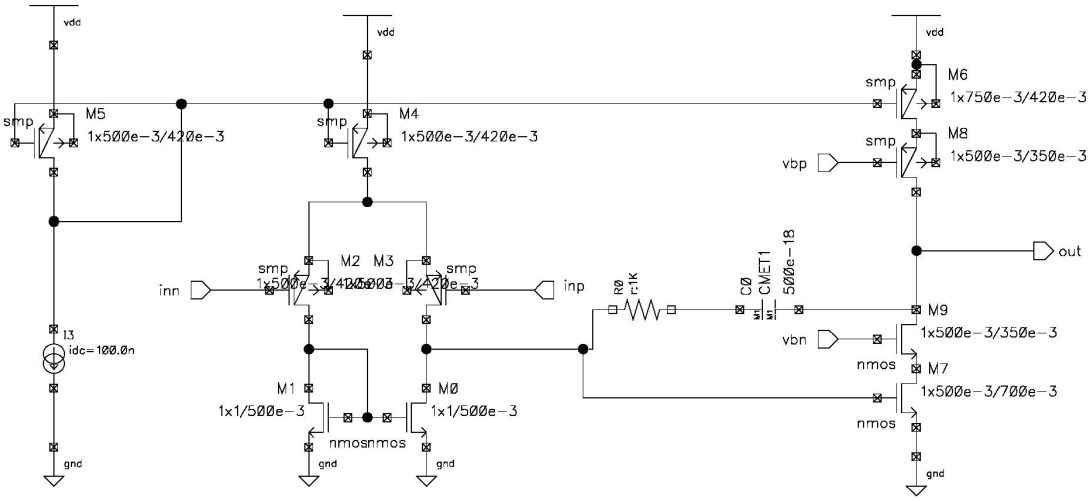

Figure 27: Two stage op-amp with cascode output

Table 12: Simulation results for two-stage op-amp with cascode output stage parameters

Parameter	Dimension
$bias\ current$	$\mathbf{0.1e-9}$
$W_{0,1}$	$\mathbf{500e-3}$
$L_{0,1}$	$\mathbf{1000e-3}$
$W_{2,3}$	$\mathbf{500e-3}$
$L_{2,3}$	$\mathbf{420e-3}$
W_4	$\mathbf{500e-3}$
L_4	$\mathbf{420e-3}$
w_5	$\mathbf{500e-3}$
L_5	$\mathbf{420e-3}$
W_6	$\mathbf{750e-3}$
L_6	$\mathbf{420e-3}$
W_7	$\mathbf{500e-3}$
L_7	$\mathbf{700e-3}$
W_8	$\mathbf{500e-3}$
L_8	$\mathbf{350e-3}$
W_9	$\mathbf{350e-3}$

Table 13: Results for two-stage op-amp with cascode output

Parameter	Value
$Maximum\ gain$	$\mathbf{56,8dB}$
$Power\ consumtion$	$\mathbf{9,01e-10W}$

12.2. VFC

Even though the required op-amp gain was not obtained, the entire VFC was simulated to confirm the results found during the ideal simulations.

Table 14: VFC Simulation results

Input voltage	Output frequency
$0{,}0mV$	$\mathbf{0,0Hz}$
$0{,}02mV$	$\mathbf{0,0Hz}$
$0{,}03mV$	$\mathbf{32Hz}$
$0{,}05mV$	$\mathbf{44Hz}$
$0{,}1mV$	$\mathbf{62Hz}$
$0{,}2mV$	$\mathbf{87Hz}$
$0{,}5mV$	$\mathbf{140Hz}$
$1{,}0mV$	$\mathbf{208Hz}$
$2.0mV$	$\mathbf{301Hz}$
$5{,}0mV$	$\mathbf{426Hz}$
$7{,}0mV$	$\mathbf{430Hz}$

Table 15: Comparing ideal and real simulations

Ideal simulations		**Real simulations**	
Input voltage	**Output frequency**	**Input voltage**	**Output frequency**
$0{,}0mV$	$0Hz$	$\mathbf{0,0mV}$	$\mathbf{0,0Hz}$
$2{,}0\mu V$	$0{,}33Hz$		
$4{,}0\mu V$	$1Hz$		
$6{,}0\mu V$	$1{,}8Hz$		
$8{,}0\mu V$	$2{,}5Hz$		
$10\mu V$	$3{,}0Hz$		
$20\mu V$	$6{,}4Hz$	$\mathbf{20\mu V}$	$\mathbf{0,0Hz}$
$30\mu V$	$9{,}6Hz$	$\mathbf{30\mu V}$	$\mathbf{32Hz}$
$50\mu V$	$16Hz$	$\mathbf{50\mu V}$	$\mathbf{44Hz}$
$100\mu V$	$34Hz$	$\mathbf{100\mu V}$	$\mathbf{62Hz}$
		$\mathbf{200\mu V}$	$\mathbf{87Hz}$
		$\mathbf{500\mu V}$	$\mathbf{140Hz}$
$1{,}0mV$	$332Hz$	$\mathbf{1,0mV}$	$\mathbf{208Hz}$
		$\mathbf{2.0mV}$	$\mathbf{301Hz}$
$5{,}0mV$	$1688Hz$	$\mathbf{5,0mV}$	$\mathbf{426Hz}$
		$\mathbf{7,0mV}$	$\mathbf{430Hz}$
$10mV$	$3377Hz$		
$20mV$	$6847Hz$		
$40mV$	$14080Hz$		
60mV	$21720Hz$		

The results from Table 5 are here converted to input voltages for direct comparability with the ideal simulation results. The values present in this table for ideal simulations not found in Table 5 are found utilizing the input-output relation for an ideal VFC

$$f_O = kv_{IN} \tag{40.}$$

where k is the VFC sensitivity in hertz per volt.[44] The results from the ideal simulations on op-amp gain are thus confirmed.

13. Discussion analog components

The lack of op-amp gain results, as shown in Table 15, in no output signal from the VFC for input voltages below $20\mu V$ and that the output frequency increases slower for the real simulations compared to the ideal. The slower increase in frequency is basically just an advantage as it would result in less power consumed by the circuit. The reason for this deviation is that the output transistors in the op-amp don't manage to charge the integrating capacitor as fast as the ideal transistors can. It is also because of the lack of frequency-compensation in the op-amps. Compensation of the op-amps where not prioritized because they didn't manage the required gain.

14. Conclusion

It has been shown in this report that there are several parameters connected with the Lithium-ion battery that requires very precise control by voltage and current measuring. This even though the manufacturer has strict guidelines

Three approaches for measuring the state of charge in a Lithium-ion battery have been looked into, and their advantages and disadvantages have been discussed. No conclusion has been drawn regarding which approach is the best other than that the voltage measurement method isn't suitable for a Lithium-ion battery because of its large error.

A Voltage-to-Frequency converter has been implemented in VHDL-AMS and simulated in ADVance-MS[2]. During the simulation values for its components have been found, but the design is still not good enough for commercial use and requires high-gain operational amplifiers.

Simulation several high-gain operational amplifiers where simulated in the 35K9 process and this reviewed that this process appears to have a gain limit somewhat around 56dB. This because the two-stage op-amp and the two-stage op-amp with cascode output managed both about the same gain, but the two-stage op-amp amplifier with cascode output should theoretically have managed around 100 times the gain of the ordinary two-stage architecture.

The conclusion on this VFC-design is therefore that it is not suitable for its intended CMOS-process.

15. Further work

As shown with the simulations, it is not possible to obtain enough gain for this VFC-design using this CMOS-process. If a VFC is to be developed for this process it is necessary to look into other VFC-architectures to find a solution which doesn't require this much closed-loop gain.

16. Sources

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[2] Mentor-Graphics, "ADVance MS," 4.4_1.1 ed.

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Appendix A

a) The test bench for the ideal simulations

```
library IEEE;
library IEEE_proposed;
use IEEE_proposed.electrical_systems.all;
use IEEE.math_real.all;
use IEEE.std_logic_1164.all;

entity vfc is
port (
  placement : out integer := 0;
  q     : out std_ulogic;
  q_not : out std_ulogic);
end entity vfc;

architecture vfc of vfc is

--------------------------------------------------------------------------------
-- Constants for the ideal components values
--------------------------------------------------------------------------------

  constant gain_db : real := 100.0;            -- Opamp gain in dB
  constant v_out : real := 1.0;               -- Output from comparator
  constant res_ideal : real := 1000.0;         -- The input resistors
  constant cap_ideal : real := 10.0e-9;        -- Capacitance one
  constant r_leak_c : real := 10.0e9;          -- Leakage resistance in capacitor one
  constant threshold_comparator : real := -150.0e-3;  -- Threshold voltage comparator
  constant threshold_trigger : real := 0.5;     -- Threshold voltage trigger
  constant r_open : real := 10.0e9;            -- Resistance when the switch is open
  constant r_closed : real := 200.0;           -- Resistance when the switch is closed
  constant trans_time : real := 1.0e-6;        -- Transition time switch
  constant r_sensing : real := 100.0e-3;       -- Sensing resistor

--------------------------------------------------------------------------------
-- The deviations from ideal values
--------------------------------------------------------------------------------

  constant gain_deviation_1 : real := 0.0;      -- Deviation from ideal gain in opamp one(dB)
  constant gain_deviation_2 : real := 0.0;      -- Deviation from ideal gain in opamp two(dB)
-- The following deviations are measured in percent
  constant resistance_deviation_1 : real := 0.0; -- Deviation from ideal resistance in input
resistor one
  constant resistance_deviation_2 : real := 0.0; -- Deviation from ideal resistance in input
resistor two
  constant capacitance_deviation_1 : real := 0.0; -- The same as for resistors and opamps
  constant capacitance_deviation_2 : real := 0.0;
  constant threshold_deviaton_comp_1 : real := 10.0;
```

```
  constant threshold_deviaton_comp_2 : real := 10.0;
--------------------------------------------------------------------------------
-- The used component values
--------------------------------------------------------------------------------

  constant gain_1 : real := 10**((gain_db + gain_deviation_1) / 20.0);
  constant gain_2 : real := 10**((gain_db + gain_deviation_2) / 20.0);
  constant resistance_1 : real := (res_ideal + res_ideal * (resistance_deviation_1 / 100.0));
  constant resistance_2 : real := (res_ideal + res_ideal * (resistance_deviation_2 / 100.0));
  constant capacitance_1 : real := (cap_ideal + cap_ideal * (capacitance_deviation_1 / 100.0));
  constant capacitance_2 : real := (cap_ideal + cap_ideal * (capacitance_deviation_2 / 100.0));
  constant threshold_comparator_1 : real := (threshold_comparator + threshold_comparator *
(threshold_deviaton_comp_1 /100.0));
  constant threshold_comparator_2 : real := (threshold_comparator + threshold_comparator *
(threshold_deviaton_comp_2 / 100.0));

--------------------------------------------------------------------------------
-- Constants for the stimulus
--------------------------------------------------------------------------------

  constant batt_current_1 : real := 20.0e-6;    -- The battery current
  constant td_1 : time := 7.5sec;               -- The time the converter is imprinted with current
one
  constant batt_current_2 : real := 40.0e-6;    -- Same as for current_1
  constant td_2 : time := 4sec;                 -- Current_1
  constant batt_current_3 : real := 60.0e-6;
  constant td_3 : time := 2sec;
  constant batt_current_4 : real := 80.0e-6;
  constant td_4 : time := 1000ms;
  constant batt_current_5 : real := 100.0e-6;
  constant td_5 : time := 500ms;
  constant batt_current_6 : real := 500.0e-6;
  constant td_6 : time := 500ms;
  constant batt_current_7 : real := 1.0e-3;
  constant td_7 : time := 500ms;
  constant batt_current_8 : real := 10.0e-3;
  constant td_8 : time := 200ms;
  constant batt_current_9 : real := 100.0e-3;
  constant td_9 : time := 200ms;
  constant batt_current_10 : real := 200.0e-3;
  constant td_10 : time := 200ms;
  constant batt_current_11 : real := 400.0e-3;
  constant td_11 : time := 100ms;
  constant batt_current_12 : real := 600.0e-3;
  constant td_12 : time := 50ms;

--------------------------------------------------------------------------------
-- Various terminals, quantities and signals
--------------------------------------------------------------------------------
```

```
  terminal batt_pos : electrical;
  terminal batt_neg : electrical;
  terminal out_res_1 : electrical;
  terminal out_res_2 : electrical;
  terminal out_opamp_1 : electrical;
  terminal out_opamp_2 : electrical;
  terminal threshold_cmp_1 : electrical;
  terminal threshold_cmp_2 : electrical;
  terminal out_cmp_1 : electrical;
  terminal out_cmp_2 : electrical;
  alias vss is ELECTRICAL_REF;          -- ground
  quantity v_batt across i_batt through batt_pos to batt_neg;
  quantity v_threshold_cmp_1 across i_threshold_1 through threshold_cmp_1;
  quantity v_threshold_cmp_2 across i_threshold_2 through threshold_cmp_2;
  signal s_batt : current := 0.0;      -- The battery current signal
  signal s_threshold_cmp_1 : voltage := 0.0;  -- The threshold voltage signal
  signal s_threshold_cmp_2 : voltage := 0.0;  -- The threshold voltage signal
  signal sw_state_1 : std_ulogic;     -- Control signal switch_1
  signal sw_state_2 : std_ulogic;  -- Control signal switch_2

-------------------------------------------------------------------------------
-- Begin
-------------------------------------------------------------------------------

begin
  s_threshold_cmp_1 <= threshold_comparator_1;
  v_threshold_cmp_1 == s_threshold_cmp_1'ramp;
  s_threshold_cmp_2 <= threshold_comparator_2;
  v_threshold_cmp_2 == s_threshold_cmp_2'ramp;

-------------------------------------------------------------------------------
-- Creating the different parts in the VFC
-------------------------------------------------------------------------------

  opamp_1 : entity work.opamp(slew_limited)
    generic map (
      gain => gain_1)
    port map (
      minus_in  => out_res_1,
      plus_in => vss,
      output   => out_opamp_1);
  opamp_2 : entity work.opamp(slew_limited)
    generic map (
      gain => gain_2)
    port map (
      minus_in => out_res_2,
      plus_in  => vss,
      output   => out_opamp_2);
  res_1 : entity work.resistor(ideal)
    generic map (
```

```
    resistance => resistance_1)
  port map (
    p1 => batt_neg,
    p2 => out_res_1);
res_2 : entity work.resistor(ideal)
  generic map (
    resistance => resistance_2)
  port map (
    p1 => batt_neg,
    p2 => out_res_2);
res_sense : entity work.resistor(ideal)
  generic map (
    resistance => r_sensing)
  port map (
    p1 => batt_neg,
    p2 => vss);
cap_1 : entity work.capacitor(leakage)
  generic map (
    c      => capacitance_1,
    r_leak => r_leak_c)
  port map (
    p1 => out_res_1,
    p2 => out_opamp_1);
cap_2 : entity work.capacitor(leakage)
  generic map (
    c      => capacitance_2,
    r_leak => r_leak_c)
  port map (
    p1 => out_res_2,
    p2 => out_opamp_2);
comp_1 : entity work.comparator(comparator)
  generic map (
    v_out => v_out)
  port map (
    input  => out_opamp_1,
    output => out_cmp_1,
    v_ref  => threshold_cmp_1);
comp_2 : entity work.comparator(comparator)
  generic map (
    v_out => v_out)
  port map (
    input  => out_opamp_2,
    output => out_cmp_2,
    v_ref  => threshold_cmp_2);
switch_1 : entity work.switch(ideal)
  generic map (
    r_open     => r_open,
    r_closed   => r_closed,
    trans_time => trans_time)
  port map (
```

```
    sw_state => sw_state_1,
    p1       => out_res_1,
    p2       => out_opamp_1);
switch_2 : entity work.switch(ideal)
  generic map (
    r_open     => r_open,
    r_closed   => r_closed,
    trans_time => trans_time)
  port map (
    sw_state => sw_state_2,
    p1       => out_res_2,
    p2       => out_opamp_2);
trigger: entity work.trigger(hysteresis)
  generic map (
    threshold => threshold_trigger)
  port map (
    s     => out_cmp_1,
    r     => out_cmp_2,
    q     => sw_state_1,
    q_not => sw_state_2);

-- purpose: Provide the stimulus
stimulus: process
begin  -- process stimulus
  wait for 10 ns;                   -- Required for convergence
  placement <= 1;
  s_batt <= batt_current_1;
  wait for td_1;
  placement <= 2;
  s_batt <= batt_current_2;
  wait for td_2;
  placement <= 3;
  s_batt <= batt_current_3;
  wait for td_3;
  placement <= 4;
  s_batt <= batt_current_4;
  wait for td_4;
  placement <= 5;
  s_batt <= batt_current_5;
  wait for td_5;
  placement <= 6;
  s_batt <= batt_current_6;
  wait for td_6;
  placement <= 7;
  s_batt <= batt_current_7;
  wait for td_7;
  placement <= 8;
  s_batt <= batt_current_8;
  wait for td_8;
  placement <= 9;
```

```
    s_batt <= batt_current_9;
    wait for td_9;
    placement <= 10;
    s_batt <= batt_current_10;
    wait for td_10;
    placement <= 11;
    s_batt <= batt_current_11;
    wait for td_11;
    placement <= 12;
    s_batt <= batt_current_12;
    wait for td_12;
    s_batt <= 0.0;
    placement <= 13;
    wait;
  end process stimulus;

  i_batt == s_batt'ramp;
  q <= sw_state_1;
  q_not <= sw_state_2;
end vfc;
```

Appendix B

```
signal:
discharge_register = {{5} {8} {7} {5} {3} {16} {34} {133} {1351} {2739}
{2815} {2173}}
pw_vector = {{7499999999745000 fs} {3999999999864000 fs}
{1999999999932000 fs} {999999999966000 fs} {499999999983000 fs}
{499999999983000 fs} {499999999983000 fs} {199999999993200 fs}
{199999999993200 fs} {199999999993200 fs} {99999999996600 fs}
{49999999998300 fs}}
frq_vector = {{0.333333} {1} {1.75} {2.5} {3} {16} {34} {332.5}
{3377.5} {6847.5} {14075} {21730}}
clk = 0
f_in = 1
f_in_inv = 0
placement = 13
t_temp_1 = {{3816793893 fs} {7500003816538893 fs} {11500003816402893
fs} {13500003816334893 fs} {14500003816300893 fs} {15000003816283893
fs} {15500003816266893 fs} {16000003816249893 fs} {16200003816243093
fs} {16400003816236293 fs} {16600003816229493 fs} {16700003816226093
fs}}
t_temp_2 = {{7500003816538893 fs} {11500003816402893 fs}
{13500003816334893 fs} {14500003816300893 fs} {15000003816283893 fs}
{15500003816266893 fs} {16000003816249893 fs} {16200003816243093 fs}
{16400003816236293 fs} {16600003816229493 fs} {16700003816226093 fs}
{16750003816224393 fs}}
finished_1 = true
finished_2 = true
```

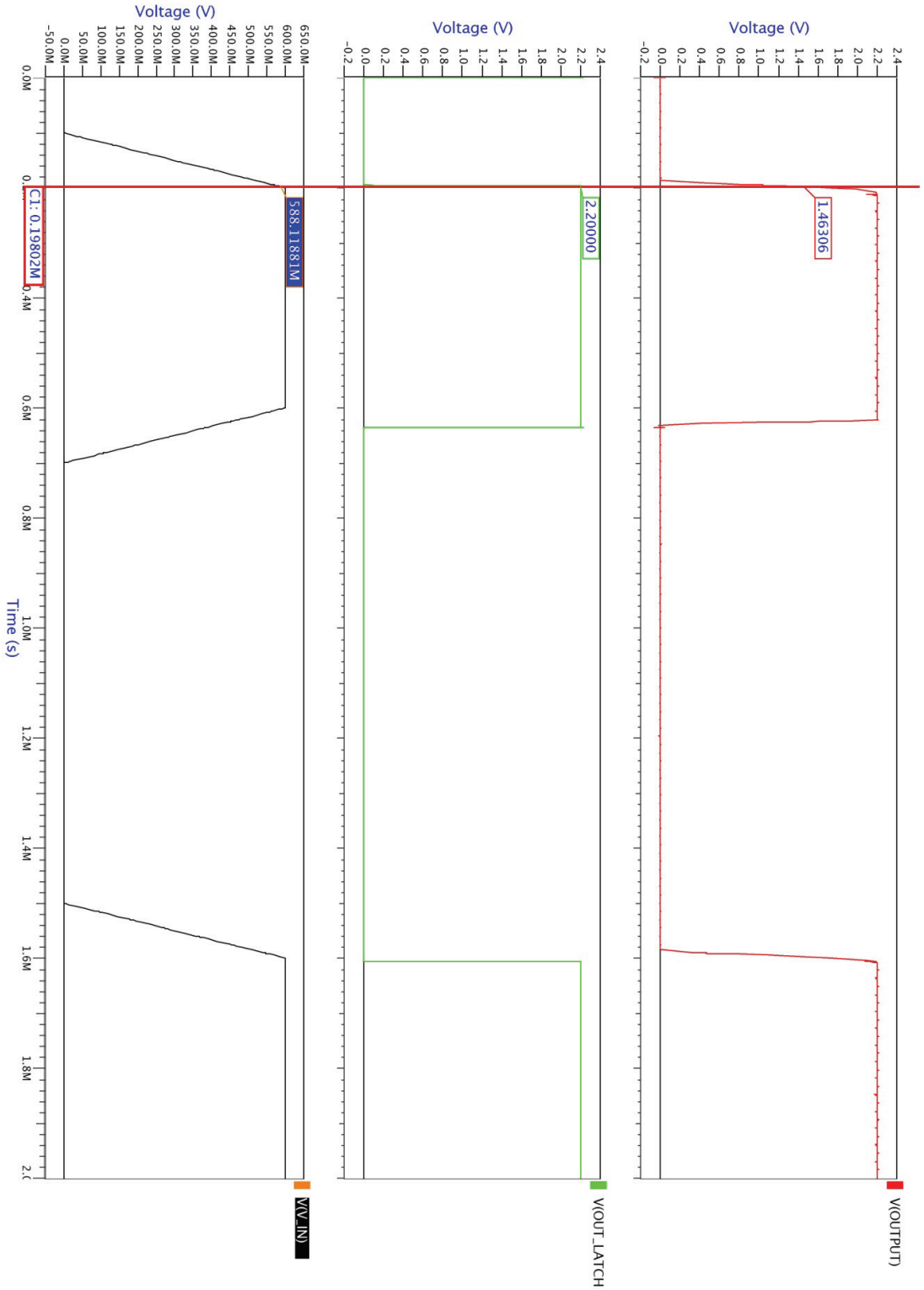
Appendix C

```
** Generated for: hspiceD
** Generated on: Mar  5 16:26:13 2007
** Design library name: fhafslund_kladd
** Design cell name: vfc
** Design view name: schematic

.GLOBAL vdd! 0 vcc!
.connect vcc! vdd!

.TRAN 1e-8 20m START=0.0

vdd vdd! 0 dc 2.2
vthreshold v_threshold 0 dc 0.55

**Input voltage
*vinput vfc_input 0 pulse(0.0 0.005 0.1m 2m 1m 1m 4m)
vinput vfc_input 0 dc 0.00m  ac 0.0m
* vinput vfc_input 0
* + pulse(2m 20m 0.1m 0 0 0.5m 1m)
* + sin(10m 10m 1000 0 0)
* .sinus vfc_input 0.005 0.005 1000 0.01m

**Enable signal for the state machine (modified S_R latch)
venable enable 0 pulse(0 2.2 50u 1u 1u 1s 1.0005s)

**Bias voltage and clock signal used by the comparator
vclk clk 0 pulse(0 2.2 0 0 0 15.1515e-6 30.303e-6)
vbias v_bias 0 dc 250m

.plot v(vfc_input)
*.plot v(in_op_1)
*.plot v(in_op_2)
.plot v(out_op_1)
*.plot v(out_op_2)
*.plot v(out_cmp_1)
*.plot v(out_cmp_2)
*.plot v(enable)
.plot v(q)
*.plot v(q_not)
*.plot v(clk)

.TEMP 25
.OPTION
+    BRIEF
+    INGOLD=2
+    MEASOUT=1
+    NOMOD
+    NOPAGE
+    PARHIER=LOCAL
```

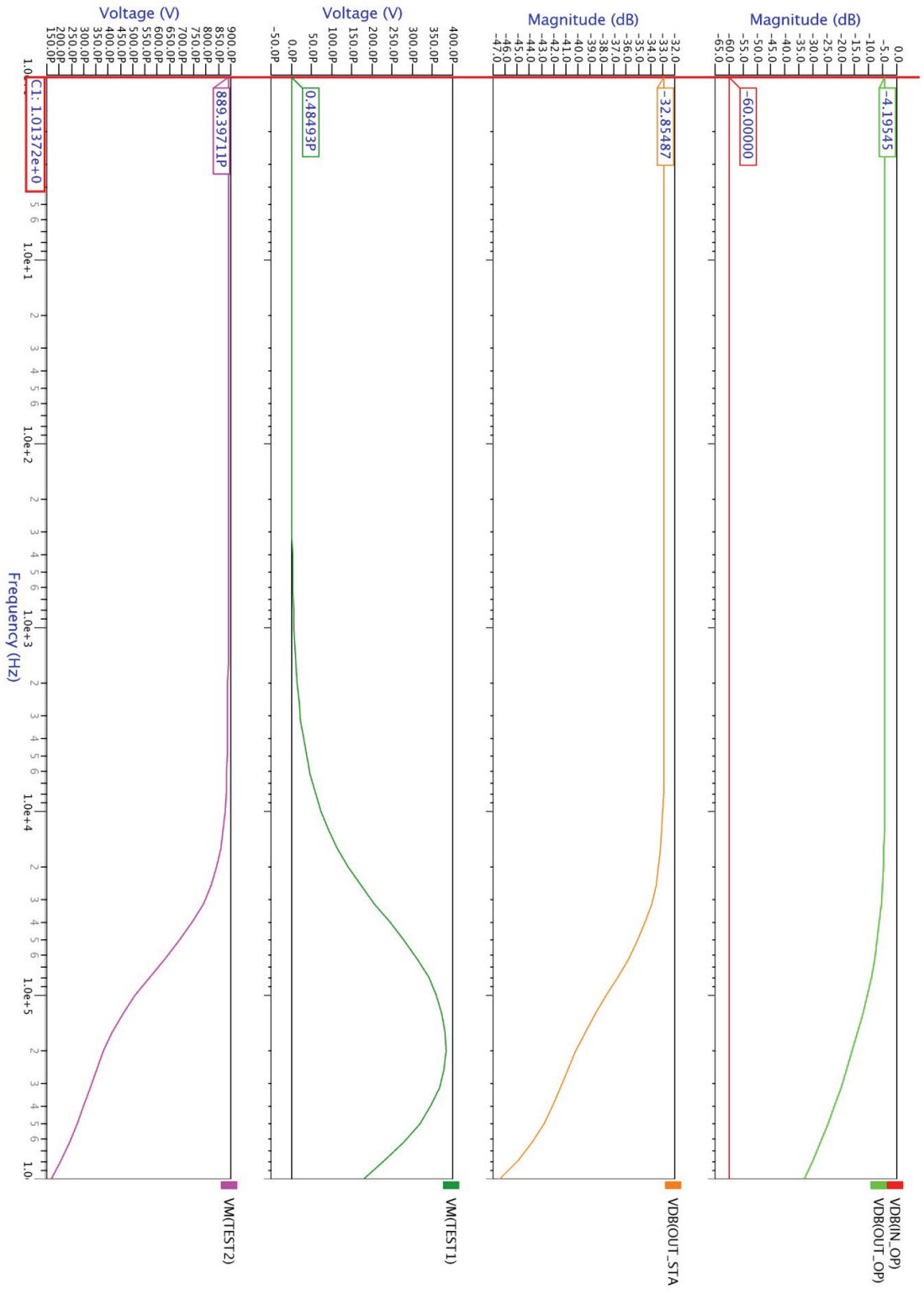
```
+   PSF=2
+   SCALE=1e-6
+   MSGNODE=0

.include /ic/backend/lib/atmel/ee35900/eldo/typ.s
.include /ic/backend/lib/atmel/ee35900/eldo/rcD.s
.include /home/fhafslund/eldo/fhafslund_kladd/vfc/subckt/opamp_twostage.cir
.include /home/fhafslund/eldo/fhafslund_kladd/vfc/subckt/comparator_hysteresis.cir
.include /home/fhafslund/eldo/fhafslund_kladd/vfc/subckt/SRL.cir
.include /home/fhafslund/eldo/fhafslund_kladd/vfc/subckt/latch.cir
.include /home/fhafslund/eldo/fhafslund_kladd/vfc/subckt/inverter.cir

** Library name: fhafslund_kladd
** Cell name: vfc
** View name: schematic
xSR q q_not out_latch_2 out_latch_1 enable gnd! vdd! SRL_A
m00 out_op_1 q in_op_1 0 nmos L=5000e-3 W=500e-3 AD=280e-3 AS=280e-3 PD=2.12
PS=2.12 NRD=420e-3 NRS=420e-3 M=1
m01 out_op_2 q_not in_op_2 0 nmos L=5000e-3 W=500e-3 AD=280e-3 AS=280e-3
PD=2.12 PS=2.12 NRD=420e-3 NRS=420e-3 M=1
r1 vfc_input in_op_1 5k
r2 vfc_input in_op_2 5k
c1 in_op_1 out_op_1 '100e-13' M='1'
c2 in_op_2 out_op_2 '100e-13' M='1'
xOP1 0 in_op_1 out_op_1 0 opamp_twostage
xOP2 0 in_op_2 out_op_2 0 opamp_twostage
xCMP1 clk out_cmp_1 v_bias out_op_1 v_threshold 0 comparator_hysteresis
xCMP2 clk out_cmp_2 v_bias out_op_2 v_threshold 0 comparator_hysteresis
xlatch1  out_cmp_1 clk out_latch_1 0 vdd! LD1_B
xlatch2 out_cmp_2 clk out_latch_2 0 vdd! LD1_B
.end
```

Appendix D

b) Simulation-graph comparator

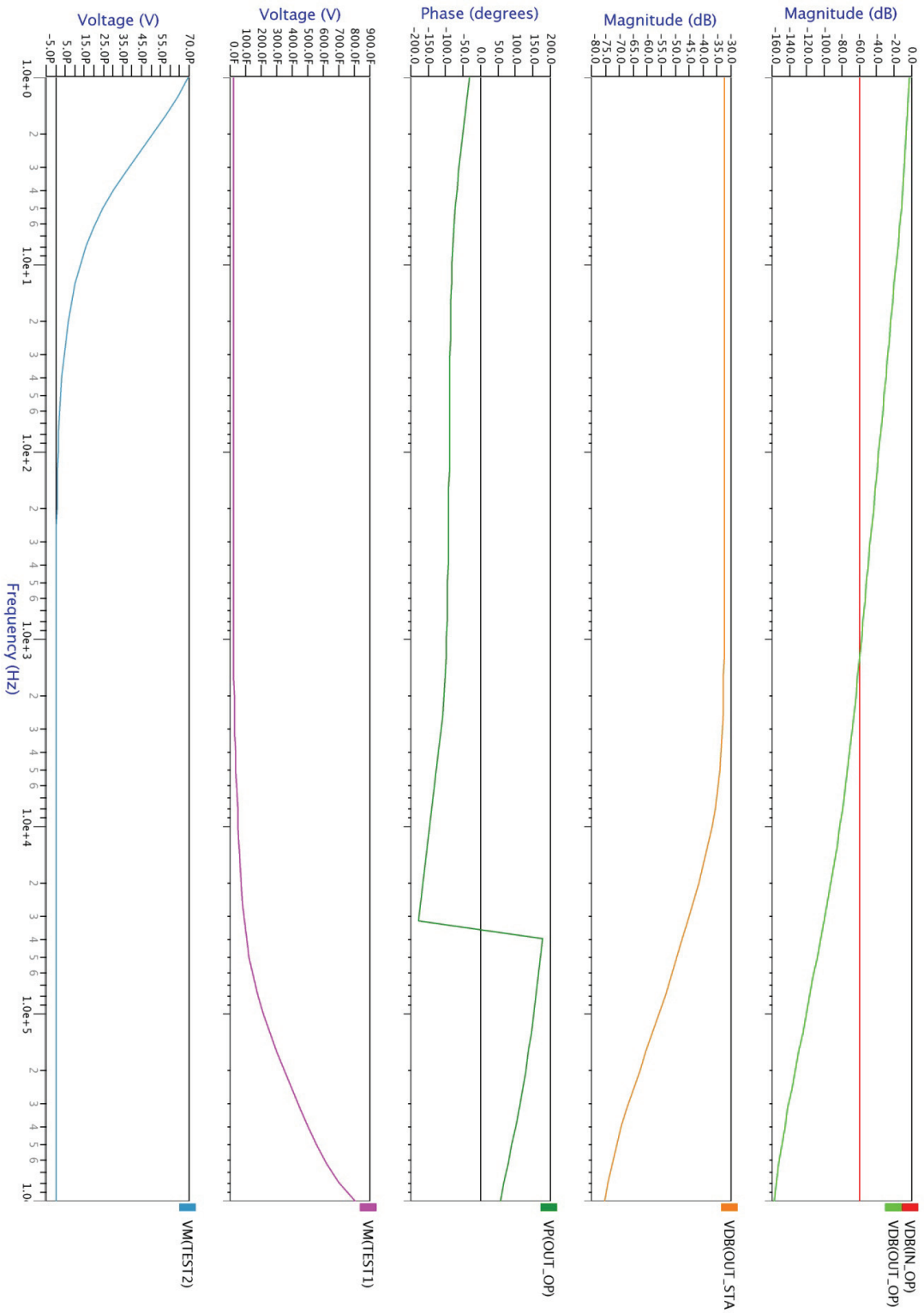


c) Output op-amp two-stage

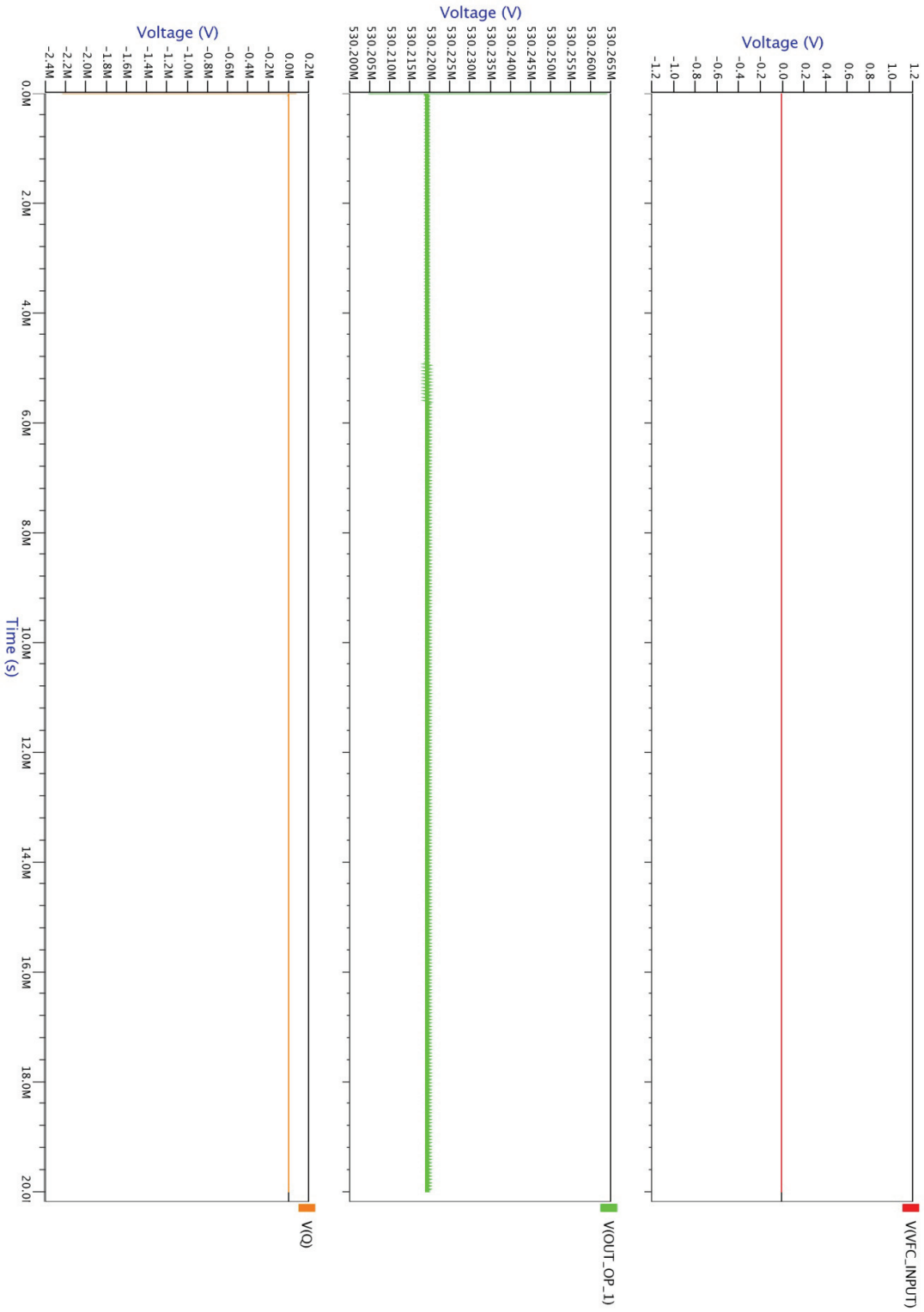


Simulation results op-amp two-stage

d) Output op-amp two-stage with cascode output



e) *Output VFC 0,0V input*



f) Output VFC 5,0mV input