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A digital audio playback system with USB interface

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Problem Description

The audio and music industry as a whole is going through a change towards more computerized playback systems. Today it is not uncommon to have a private music library organized on a personal computer or a media device instead of a large collection of CDs. High quality audio tracks can be downloaded directly from the internet. It is therefore desireable to be able to play back these tracks on a hifi-system with a minimal loss of quality.

The main purpose of the project is to create a high performance audio digital to analog converter (DAC) system, which can retrieve data via a USB connection. The DAC should be followed by an appropriate filter and preamplifier to directly connect to a power amplifier. Also, a digital control of source selection and analog volume circuitry should be implemented. The system should support high quality audio formats, up to 192 kHz sampling frequency with 24 bit resolution.

A modular design allows for a separate decoder for various audio formats retrieved over USB, either as a sound card or as a standalone audio player.

Assignment given: 23. January 2009
Supervisor: Trond Ytterdal, IET

Abstract

A high performance sound card is designed and implemented using a USB enabled microcontroller and an external dataconverter. Data is retrieved either via USB or S/PDIF. The sampling clock is generated by a precision clock synthesizer. This is programmable and can be adapted to different sampling rates of USB data. The system supports 24 bit, 192 kHz audio.

Signal attenuation is performed through a relay based stepped voltage divider with constant output impedance. 64 dB attenuation in steps of 1 dB is available.

An extensive power supply is made to support the range of required voltages. The signal to noise ratio of the power supply was measured to be 93 dB in the audio frequency band.

The microcontroller has been programmed to handle the USB communication and provision of control signals for the system.

The whole system is assembled on PCBS and tested. The audio performance measurements show a dynamic range of 105 dB, measured at the system output in a noisy environment. The total harmonic distortion plus noise was 0.0011 %.

Contents

Acronyms and abbreviations

This section describes various acronyms and abbreviations used throughout the text.

AC	Alternating Current
ADC	Analog to Digital Converter
AES	Audio Engineering Society
AES/EBU	A digital audio interface
AKM	Asahi Kasei Microdevices Corporation
AUX	Auxiliary
BPM	Bi-Phase Mark
BGA	Ball Grid Array
CAD	Computer Aided Design
CD	Compact Disc
CFI	Common Flash Interface
DAC	Digital to Analog Converter
DC	Direct Current
DR	Dynamic Range
EBU	European Broadcast Union
EIAJ	Electronic Industries Associations of Japan
EP	Endpoint (USB terminology)
ENOB	Effective Number Of Bits
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FIFO	First In, First Out (Buffer topology)
FS	Full Scale
FSK	Frequency Shift Keying
HID	Human Interface Device
HW	Hardware
I^2C	Inter-Integrated Circuit bus
IO	Input/Output

ICOB	Inverted Complementary Offset Binary code
IRQ	Interrupt Request
JEIDA	Japan Electronic Industry Development Association
JEITA	Japan Electronics and Information Technology Industries Association (Merger of former EIAJ and JEIDA)
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPCM	Linear Pulse Code Modulation
LSB	Least Significant Bit
MAC	Media Access Controller
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MSOF	Micro Start Of Frame (USB terminology)
NAND	Negating Boolean AND
OE	Output Enable
PC	Personal Computer
PCM	Pulse Code Modulation
PCB	Printed Circuit Board
PDF	Probability Density Function
PIO	Programmable Input/Output
PLL	Phase Locked Loop
P–P	Peak to Peak
PSRR	Power Supply Rejection Ratio
PSU	Power Supply Unit
RMS	Root Mean Square
RTC	Real Time Clock
SCL	SMBUS clock line
SCMS	Serial Copy Management System
SDA	SMBUS data line
SMBUS	System Management Bus
SNR	Signal to Noise Ratio
SOF	Start Of Frame (USB terminology)
SFDR	Spurious Free Dynamic Range
SPI	Serial Peripheral Interface
SRC	Source
SSC	Synchronous Serial Communication
S/PDIF	Sony/Philips digital interface
THD+N	Total Harmonic Distortion plus Noise
TWI	Two Wire Interface (Atmel's implementation of I^2C)
USB	Universal Serial Bus

Chapter 1

Introduction

This thesis is written in fulfillment of the degree of master of science in electrical engineering at the Norwegian university of science and technology. The work has been done in the spring of 2009, in the last semester of a five-year master program.

1.1 Motivation

The area of home audio systems is in a state of change. The time of the large physical record collections is on the wane, and music libraries contained in computer storage is taking over. One of the main benefits with a computerized playback system is ease of use. Consider a scenario where one wishes to compile a playlist consisting of tracks distributed over several records. Using compact discs (CDs), it becomes necessary to change discs between tracks, or use a player capable of handling several discs. Both methods introduce a pause in the playback, and are rather cumbersome in their execution.

Now, enter the era of the computer based music playback system, where advanced playlist creation on nearly any criteria can be done through a personal computer (PC) or a more specialized device. Some systems offer audio distribution to any room in the house, some are completely self contained and have internal audio storage, while others rely on networking or short range busses for data retrieval. Others again are only docks for portable units.

People are getting used to the instant availability of music through these playback systems, but many of the devices leave a lot to be desired audio quality wise.

1.2 Objective

The paramount objective of this thesis is to design an audio playback system which receives audio data over an universal serial bus (USB) connection. These data shall be converted to analog signals and amplified suitably for driving an audio power amplifier. In the same way the system should be able to decode the digital S/PDIF signal provided by CD players.

It is preferable that the system supports 24 bit linear pulse code modulated audio data with a sampling rate as high as 192 kHz, which is today's state of the art in the audio market. In addition it should support lower sampling frequencies, among them 44.1 kHz used on CDs.

A second goal is to design a passive attenuator circuit to adjust the output volume with minimal distortion, and an input source selection functionality. This should be controlled digitally, allowing for remote control.

The work will include the selection of proper components and the interconnection of these. A microcontroller must be programmed to control the system and handle the USB data reception. Finally the system should be realized and tested for both performance and functionality.

1.3 System overview

A block schematic of the system, based on the problem description, is shown in figure 1.1. The schematic is a mixture of both logical and physical building blocks.

Audio data is collected either via S/PDIF or USB, and then fed to the digital to analog converter (DAC). S/PDIF data is delivered nearly directly to the DAC from a dedicated decoder with an onchip clock generator. The microcontroller contains a USB controller module, and audio data from a host computer travels through this to the DAC, controlled from the external precision clock generator.

When the audio signals are back in the analog domain, they are at first converted from current to voltage in through the I/V-converter. Then a lowpass filter follows, and finally source selection and attenuation for volume control.

A large number of different supply voltages are needed in the system, and these are generated in a low noise power supply.

Interaction with the device is done through a human interface device (HID), consisting of a control panel with pushbuttons and status lights. The USB connection also provides the possibility of controlling the system.

The finalized system is shown in figure 1.2. Three different printed circuit boards (PCBS) plus a mains transformer make up the device. The power supply dominates the lower half of the figure, while the digital control board is the smallest module of the system.

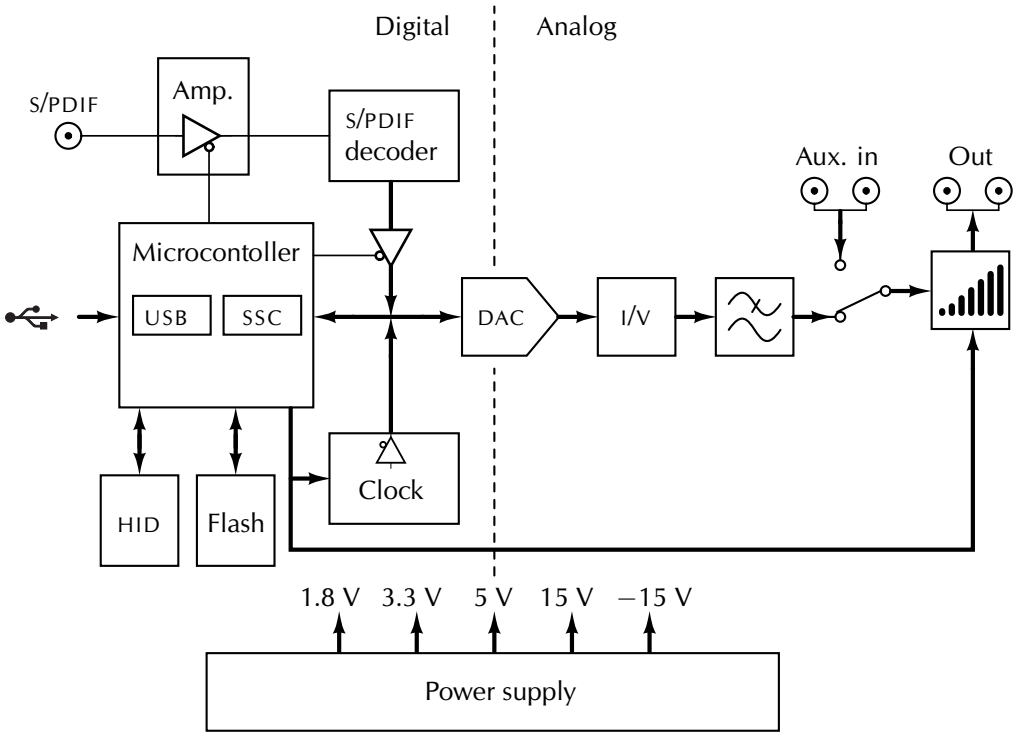


Figure 1.1: System overview. The microcontroller receives audio data via USB and serves the DAC. This is multiplexed with the S/PDIF decoder data. The human interface device (HID) provides a user interface for source selection and volume control. The DAC current outputs are converted to voltages and low pass filtered prior to the attenuator at the output. An extensive power supply generates the required voltages for both the analog and digital domains.

1.4 Report outline

Chapter 2 will cover the theory that is necessary to support the practical implementation. A brief introduction to dataconverters with focus on sampling time uncertainty and signal to noise ratio is given. Performance parameters for power supplies and distribution will be discussed next. The chapter ends with a short description of USB.

Chapter 3 covers the system implementation with component selection and circuit design. Prototypes of parts of the system are presented along with each module and finally the whole system.

Testing methodology for performance tests is discussed is **chapter 4.**

Measured results are presented in **chapter 5.**

Discussion of the implemented system and achieved results is done in **chapter 6.**

Chapter 7 concludes the thesis and proposes further work.

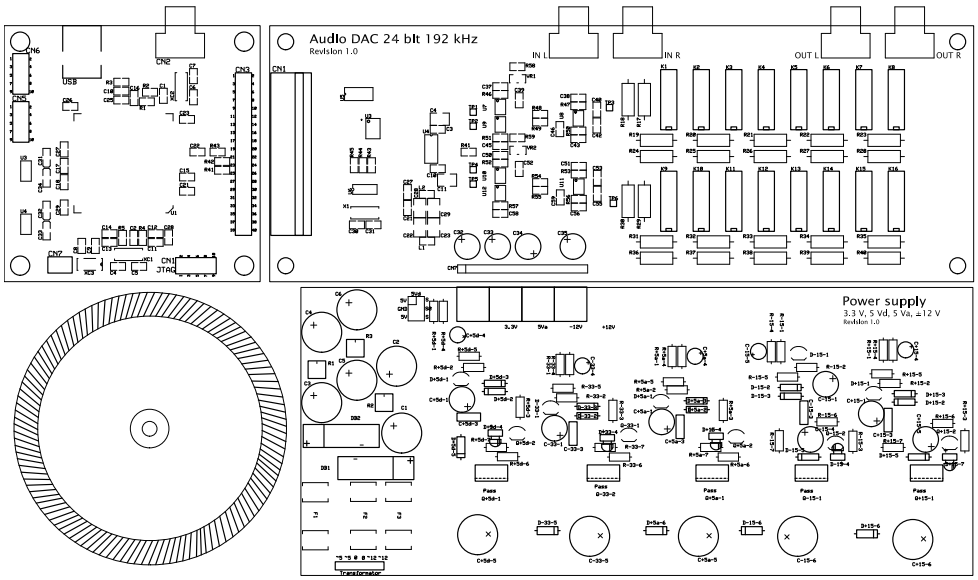


Figure 1.2: Overview of the complete system. The system consist of three printed circuit boards. The upper leftmost board is the digital control unit, the upper rightmost board is the analog board with DAC and volume control and the lower board is the power supply. The mains transformer is located in the lower left corner. Scale approximately 0.45:1.

In the appendices additional material is presented. This includes complete circuit diagrams in **appendix B** and PCB layouts in **appendix C.** Components used in the system are listed in **appendix D.**

An electronic file archive is available with complete source code for the microcontroller firmware.

Chapter 2

Theory

Much of the work done for this thesis is based on theoretical considerations. To fully understand the text, a thorough knowledge of the underlying theory is recommended. Some of the most important theoretical aspects are therefore presented here.

2.1 Dataconverters

When music is recorded it is converted from analog signals into digital signals and stored digitally, e.g. on a CD or a computer. A much better control of accuracy is acheived when entering the digital domain. In analog systems it is hard to control the signal processing accuracy, which depends on compoent tolerances. Advanecd signal processing in analog circuitry is also difficult and requires dedicated hardware. On the other hand, digital signals can be processed by a software program on a computer. Advanced operations can be done easily, where quality reduction is a matter of software programming. The digital data is also more suited for transportation and storage. Audio data converters operate normally on frequencies from 20 Hz to 20 kHz, providing high accuracy.

At the core of the system is the DAC. Its performance is governed by several fundamental relationships and ultimate limits. Additional limitations stem from the actual implementation.

Mixed signal systems are often easier to understand when going from analog to digital and then back. The theory on dataconverters therefore begins with analog to digital conversion and then briefly follows up with digital to analog conversion. Much of the theory and concepts applies for both conversions, and will therefore only be discussed once.

2.1.1 Analog to digital conversion

Although electrical charge only exist as discrete quantized packets in the form of elementary charges (Popović & Popović, 2000), analog signals can safely be considered continuous in both time and amplitude for the vast majority of practical purposes. The occupied signal bandwidth can theoretically be infinite. As some topics are considered best illustrated by analog to digital conversion, this approach will be used to here even though the target application is based on a DAC.

Digital signals, on the other hand, have discrete amplitudes and are sampled at discrete time intervals. The typical steps performed in an analog to digital converter (ADC) to convert analog to digital signals are shown in figure 2.1.

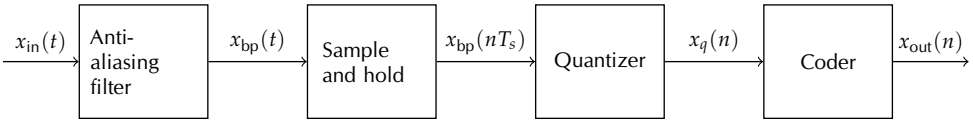


Figure 2.1: Basic structure of an ADC.

Bandpass filtering

Before the analog signal can be sampled, its bandwidth has to be bandlimited to less than half the sampling frequency according to the Nyquist criterion (Nyquist, 1928; Shannon, 1984). Higher frequencies will be folded into the frequency band of interest and cause distortion in form of false frequency components so the signal cannot be fully reconstructed. This effect, called aliasing, is prevented by the anti-aliasing filter prior to the sample and hold device in figure 2.1. In practical implementations the sampling frequency must be significantly higher than twice the signal bandwidth, since real filters have a finite transition band and finite attenuation in the stop band.

Sampling

The *sample and hold* circuit converts the signal from a continuous time signal to a discrete time signal. In the general case the sampled signal will be equal to $x_{bp}(nT_s)$, where the integer n denotes the sample number and T_s is the sampling interval, reciprocal to the sampling frequency F_s.

Assume the input signal is sinusoidal, as expressed by equation (2.1):

$$x_{bp}(t) = A\sin(2\pi Ft)\,, \tag{2.1}$$

where A is the amplitude, F is the frequency and t is time. The output from

the sample and hold circuit can then be expressed as

$$x_{\mathrm{bp}}(nT_s) = A\sin(2\pi FnT_s)\,. \tag{2.2}$$

If the relative sampling moments of the analog to digital conversion differ from the sampling moments of the digital to analog conversion when the analog signal is reconstructed, distortion is introduced. Jitter around the ideal sampling time instant arises from unwanted effects such as clock instability and power supply ripple (Hawksford, 2006).

Consider the sinusoidal signal of equation (2.1). Differentiating with respect to time gives

$$\frac{\mathrm{d}x_{\mathrm{bp}}(t)}{\mathrm{d}t} = A2\pi F\cos(2\pi Ft)\,. \tag{2.3}$$

When $x_{\mathrm{bp}}(t)$ crosses zero this rate of change reaches its maximum and is thus the moment the signal is most sensitive to sampling time jitter.

To be able to disregard sampling time uncertainty as performance reducing the introduced error must at maximum be equal to the quantization step (Plassche, 1994). Rearranging equation (2.3) gives the maximum allowed sampling time uncertainty:

$$\Delta t(\Delta A, F, t) = \frac{\Delta A}{A2\pi F\cos(2\pi Ft)}\,, \tag{2.4}$$

where ΔA is the introduced amplitude error. If the converter is binary weighted with n bit the maximum allowable sampling time uncertainty is given by (Plassche, 1994):

$$\Delta t(n, F, t) = \frac{2^{-n}}{\pi F\cos(2\pi Ft)}\,. \tag{2.5}$$

According to equation (2.4) the maximum allowable sampling time uncertainty depends on the frequency and is most significant at high frequency signals. The tolerance is smallest when $\cos(2\pi Ft) = 1$, leading to the worst-case sampling time requirement:

$$\max\left(\Delta t(n, F)\right) = \frac{2^{-n}}{\pi F}\,. \tag{2.6}$$

In table 2.1 the maximum time uncertainties for converters of different resolutions are listed for an input frequency of 20 kHz. As an example, a 24 bit converter needs a clock signal with less than a pico second variation, which is an unreasonable requirement for most applications.

Quantization

The *quantizer* converts the discrete time input signal, $x_{\mathrm{bp}}(nT)$, from continuous to discrete amplitude. The amplitude value of each input signal sample

Table 2.1: Maximum allowable sampling time uncertainty versus ADC resolution for a single 20 kHz sinusoid.

Resolution n/bit	Max. jitter $\max(\Delta t/\mathrm{s})$
16	243×10^{-12}
18	61×10^{-12}
20	15×10^{-12}
24	949×10^{-15}

is mapped to a finite set of possible values, where an n bit quantizer can represent 2^n different values. This is an irreversible operation which results in loss of information and signal distortion. As long as the converter is not overloaded, that is, the signal is contained within the converters input range, the quantization error will be equal to or less than $\pm V_{\mathrm{LSB}}/2$. V_{LSB} is the voltage level corresponding to one quantization step, or a change the size of the least significant bit (LSB).

Assuming that the probability density function (PDF) of the quantization noise is uniform and limited to the interval $\pm V_{\mathrm{LSB}}/2$, the total quantization noise power can be shown to be only dependent on quantizer resolution (Johns & Martin, 1997):

$$P_q = \frac{V_{\mathrm{LSB}}^2}{12}\,. \tag{2.7}$$

This assumption generally holds true for high resolution quantizers where the signal is large compared to an LSB (Wannamaker, Lipshitz, Vanderkooy, & Wright, 2000). The condition can also be enforced to the nth statistical moment by dithering, i.e. adding uncorrelated noise with a PDF of the same order before quantization (Wannamaker, 1997). If subtractive dither is used, i.e. the same dither signal is subtracted from the analog signal during reconstruction, a simple rectangular PDF is sufficient for proper dithering (Schuchman, 1964). Even though subtractive dithering has this major advantage, it is seldom used since the dither signal has to be stored alongside the quantized signal and it must undergo the same processing as the signal.

The quantization noise power is a fundamental performance limit in dataconverter systems as it affects the maximum achievable signal to noise ratio (SNR):

$$\max(\mathrm{SNR}) = 10 \log \frac{P_x}{P_q}\,. \tag{2.8}$$

It can be shown that for a full scale (FS) sinusoidal input signal the best

Table 2.2: Maximum dynamic range versus resolution at 0 dB_{FS} input.

Resolution/bit	Dynamic range/dB
16	98
18	110
20	122
22	134
24	146

possible SNR for an n bit dataconverter is (Johns & Martin, 1997):

$$\text{SNR} \approx 6.02n + 1.76 \text{ dB}. \tag{2.9}$$

Table 2.2 lists the maximum SNR for several values of n. However, oversampling techniques can be used to improve the SNR by keeping the input bandwidth significantly lower than the Nyquist rate.

Oversampling

The quantization noise within the baseband is uniformly distributed from $-F_s/2$ to $F_s/2$, with a power spectral density of $V_{\text{LSB}}^2/12F_s$ if the prerequisites for equation (2.7) are valid. If the sampling rate is increased, the quantization noise power is spread over a larger frequency range which decreases its power spectral density. If the signal bandwidth on the other hand is unchanged, the signal to noise ratio within the baseband will be increased by 3 dB for each doubling of the sampling frequency (Candy, 1986).

By modulation of the quantization noise its spectral distribution can be shifted out of the baseband and a further increase in SNR obtained. The maximum obtainable SNR for an Lth order noise shaping modulator with oversampling equals:

$$\text{SNR}_{\Delta\Sigma} = \text{SNR} + (6L + 3 \text{ dB})/6 \text{ dB}_{\text{Hz}}, \tag{2.10}$$

where SNR is the value obtained in equation 2.8 (Johns & Martin, 1997).

The effects of oversampling and noise shaping are illustrated in figure 2.2. The signal is band limited to $f_0 = 0.1f_s$, while the noise is spread over the whole frequency range up to $0.5f_s$. In addition, noise shaping moves the quantization noise out of the signal frequency band, improving the SNR. When the modulator order increases, the noise curve gets steeper and less noise appear at the signal frequencies.

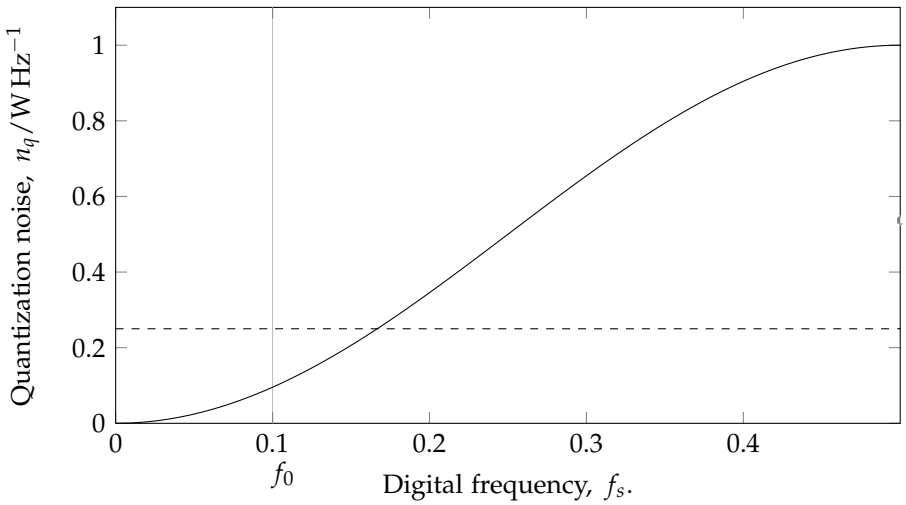


Figure 2.2: Shifted noise spectrum due to noise shaping. The baseband is marked with f_0. Linear oversampling, i.e. no noise shaping, will give a noise spectral density equal to the dashed line. The solid line is modulated, and has a shape of $0.5(1 - \cos f)$.

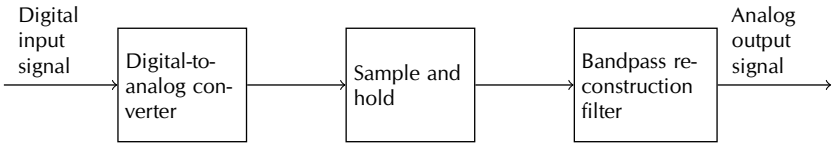


Figure 2.3: Basic structure of a DAC.

Coding of the sample

In the *coder*, each discrete signal value is represented by a b bit digital word. This block is often considered as a part of the quantizer. The most common coding scheme is *offset binary* (Plassche, 1994), where the most negative level is assigned code zero and the succeeding levels are assigned codes by counting upwards.

The Red Book CD standard uses 16 bit two's complement coded samples.

2.1.2 Digital to analog conversion

The purpose of the digital to analog converter is to convert the digital words into analog values and interpolate between these samples to reconstruct the original signal. A typical DAC system is depicted in figure 2.3.

The filtering and sampling requirements discussed for ADCs are of equal importance here. In contrast to the ADC this operation can theoretically be lossless, as no quantization is performed.

2.1.3 Performance of dataconverters

This section gives a definition of the performance parameters that is considered to be of major importance in high performance audio converters. These parameters are usually given in the converters datasheets and is useful when choosing a specific converter. Only reproduction of digital audio from CDs has a standard specification defined by EIAJ/JEITA, while test methods for other audio applications are somewhat ambiguous (Gaddy & Kawai, 1997).

These performance parameters are usually specified to use an A-weighted filter, taking the human hearing response into account.

Resolution

Resolution is the number of different digital words the DAC can output. Usually this is stated as the number of bit in the converter, where an n bit DAC can resolve 2^n different analog levels. This does not necessarily say anything about the converter's performance or accuracy.

Accuracy

Accuracy can be divided into relative accuracy and absolute accuracy. The absolute accuracy includes offset, gain and linearity errors, while the relative accuracy defines the accuracy after gain and offset errors have been removed.

Signal to noise ratio (SNR)

The SNR of a DAC is measured with all input data set to zero. From the total noise voltage the SNR becomes

$$\text{SNR} = 20 \log V_n \,. \tag{2.11}$$

Effective number of bits (ENOB)

The effective number of bits (ENOB) can be found by rearranging equation (2.9) (Johns & Martin, 1997):

$$\text{ENOB} \approx \frac{\text{SNR} - 1.76}{6.02} \,. \tag{2.12}$$

Dynamic range

Following the Japan Electronics and Information Technology Industries Association (JEITA) standard measurement for dynamic range of CD players, a -60 dB input signal should be applied and THD+N measured. The dynamic range is then found by inverting the THD+N value and adding 60 dB.

The dynamic range is limited by the quantization noise by the expression in equation (2.9).

Spurious free dynamic range (SFDR)

This is the ratio between the maximum signal component and the largest non-signal component. This distortion free dynamic range is usually less than the SNR of high performance converters.

Total harmonic distortion plus noise (THD+N)

Total Harmonic Distortion plus Noise (THD+N) indicates the system linearity in addition to the level of in band system noise. It is defined as the ratio of the total power of the second and higher harmonic components plus noise to the power of the fundamental signal component:

$$\text{THD+N} = \frac{\sqrt{V_n^2 + V_{h2}^2 + V_{h3}^2 + \cdots + V_{hi}^2}}{V_f^2} \times 100. \tag{2.13}$$

The ratio between the sampling frequency and the input frequency should be irrational.

2.1.4 Transimpedance amplifier

Many modern audio DACs have a current mode output. For a typical audio application, the signal must be converted to the voltage domain. This can be done with a transimpedance amplifier. A simple, yet common transimpedance amplifier is depicted in figure 2.4.

Assuming that the amplifier is ideal, the transfer function becomes:

$$H(s) = \frac{1}{\left(\frac{R_s}{R_f} + sC_fR_f\right)}. \tag{2.14}$$

The implied source resistance R_s in equation (2.14) is not shown in the schematic.

This circuit forms a low pass filter with a corner frequency of $\omega_0 = 1/(C_fR_f)$ and a DC gain of $-R_f/R_s$. However, these characteristics are only valid if the opamp is ideal. If the time derivative of the input current, $\mathrm{d}I_{\text{in}}/\mathrm{d}t$, is too high, a real opamp will reach its slewrate limit. Instead of a proper first order settling response, the output voltage will change linearly until it settles at the target voltage. This causes gross audible distortion, with higher order harmonic content. Hawksford (1994) shows that the distortion introduced by a slewrate limited transimpedance amplifier can be equated to that of sampling clock jitter. Both types arises from the loss of pulse area.

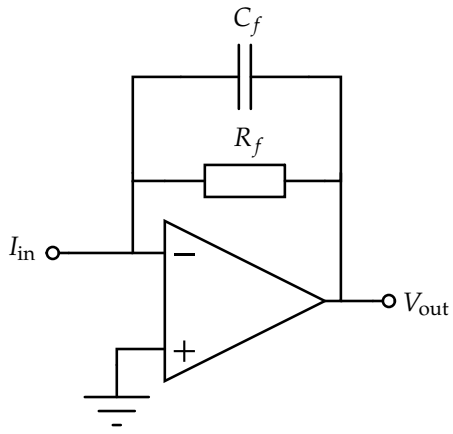


Figure 2.4: Basic inverting transimpedance amplifier with shunt–shunt feedback. First order lowpass filter with DC gain given by $V_{\text{out}}(\omega = 0) = -I_{\text{in}}R_f$. Cutoff frequency $\omega_0 = 1/R_fC_f$.

2.2 Power supply

As all devices have a finite resilience against power supply noise, deviations from the nominal voltage of the supply rails will find its way to the output signal. A stable power supply with both good line and load regulation is therefore necessary to achieve the desired performance from both the analog and mixed signal parts of the system.

In low and medium cost systems the ubiquitous LM78 and -79 series of positive and negative tree terminal voltage regulators, or some equivalent thereof, are frequently used. They offer decent performance for a price tag that fits nicely into a commercial product intended for mass production. Near DC they typically offer line regulation in excess of 70 dB, but they quickly deteriorate at higher frequencies. At 50 kHz the ripple rejection of an LM7815 regulator has dropped to 40 dB (*LM78xx Series Voltage Regulators*, 2000). Operational amplifiers usually have an excellent power supply rejection ratio (PSRR) at very low frequencies, but not so for higher frequencies. The positive PSRR of the LT1028 high performance opamp is 140 dB at 1 Hz, but only 70 dB at 10 kHz (*LT1028/LT1128 Ultralow Noise Precision High Speed Op Amps*, 1992). Therefore, for high performance audio applications a power supply that is quiet far above the audible spectrum is necessary.

Two major topologies of regulators exist, linear and switched. Only linear regulators will be considered for this application as they do not contribute with any unwanted signals other than the noise of the components used. Switched regulators, on the other hand, introduces major signal components at the switching frequency and harmonics thereof. They therefore require heavy filtering to be usable in analog audio applications, and even then they

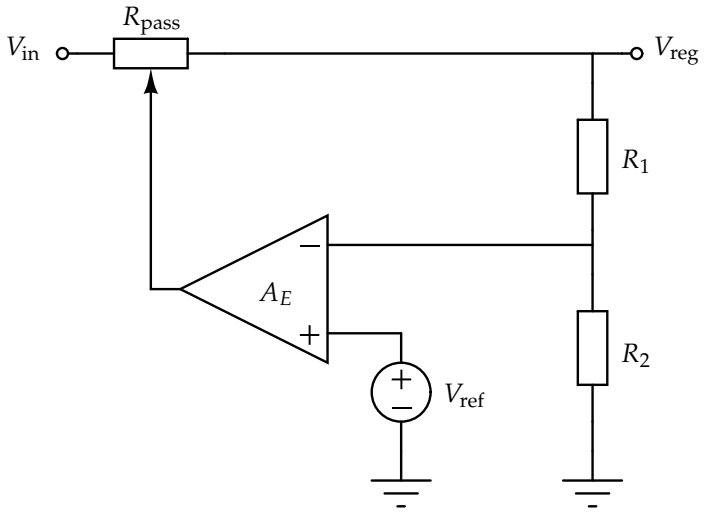


Figure 2.5: Basic series voltage regulator. The reference voltage is scaled to allow the reference to be powered from the regulated output.

are inferior to their linear counterpart in this regard. Their virtue lies in being far more power efficient, thus requiring less cooling and space for components.

2.2.1 Linear series voltage regulator

Consider the schematic of the basic series regulator shown in figure 2.5. To obtain the desired output voltage, the pass element, here modeled as a controlled resistance, must vary its resistance so that the voltage drop over R_{pass} due to the output current equals the difference between V_{in} and V_{reg}:

$$R_{\text{pass}} = \frac{V_{\text{in}} - V_{\text{reg}}}{I_{\text{out}}}\,. \tag{2.15}$$

This resistance is controlled by the an error amplifier, denoted A_E. Assuming that A_E is an ideal opamp, and that the pass impedance R_{pass} is perfectly controlled by the amplifier, the output voltage V_{reg} is given by

$$V_{\text{reg}} = V_{\text{ref}}\left(1 + \frac{R_1}{R_2}\right). \tag{2.16}$$

From equation (2.16) it is evident that the reference voltage must be as stable as possible for a noise free output, as V_{reg} is directly proportional to V_{ref}. Usage of an intrinsically low noise reference and heavy filtering of this node is therefore applied.

For the common case of less than ideal components, the gain and bandwidth of the control loop determines the overall performance of the regulator.

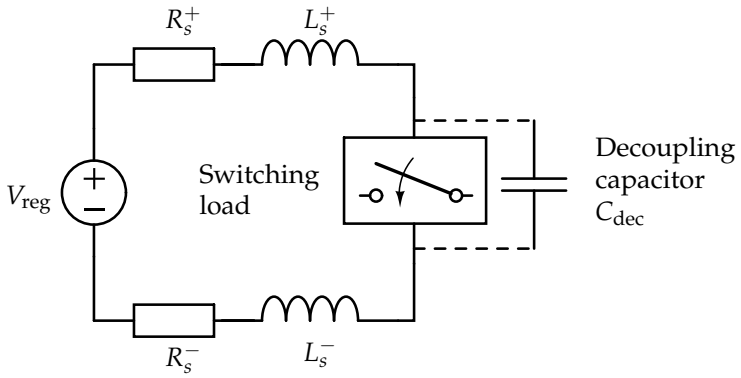


Figure 2.6: Switched load connected to a voltage regulator, with dominant parasitics included. The decoupling capacitor will reduce the effect of the parasitics R_s and L_s and the slow response of the voltage regulator when the load is changing.

This includes both the pass element, usually an NPN-transistor for a positive regulator, and the error amplifier.

2.2.2 Power distribution and decoupling

In practical implementations the power supply may be located distant to the target circuit. Even though a good regulator can respond very quickly to load variations, the connection from the power supply to the target circuit may introduce considerable series inductance and slow down its response at high frequencies. The goal is to achieve a power distribution system that has negligible impedance at all relevant frequencies seen from the loads.

The use of decoupling capacitors can mitigate the effect of this inductance while placed close to the target. Figure 2.6 shows a switching load connected between the power supply rails, and can represent a typical module in a digital circuit. When the output level changes, current has to flow through at least one of the parasitic inductors, L_s. The parasitic inductors may be a printed circuit board trace or a bonding wire, for example. With short switching times, an excessive voltage will arise across the inductor as the induced voltage over an inductor is proportional to the time derivative of the current passing through it:

$$V_L = L\frac{\mathrm{d}I}{\mathrm{d}t}\,. \tag{2.17}$$

Assuming that the load switches from high to low, the discharge current will flow through the lower inductor, L_s^-. This causes a voltage rise at the negative supply rail of the load, changing its ground potential for a short time. This effect is called ground bouncing (Brooks, 2003).

A decoupling capacitor connected close to the power supply terminals of

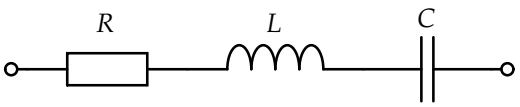


Figure 2.7: Equivalent *RLC*-circuit of a non-ideal capacitor.

the circuit will serve as a small charge storage. It will be able to both supply and absorb current. This will reduce transient currents through the stray inductors, thereby stabilizing the supply voltage at the load.

Unfortunately, real capacitors have both a series inductance and resistance. They can be modeled as shown in figure 2.7 (Brooks, 2003). Here R represents the equivalent series resistance (ESR) and L represents the equivalent series inductance (ESL). The total impedance of the capacitor will then be given as:

$$Z_C(\omega) = R + j\omega L + \frac{1}{j\omega C}, \tag{2.18}$$

whereas the magnitude is expressed as:

$$|Z_C| = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}. \tag{2.19}$$

The magnitudes of the impedances of two different capacitors are plotted in figure 2.8. The short dashed line is a 100 nF capacitor with 0.1 Ω ESR and the long dashed line is a 1 nF capacitor with 0.2 Ω ESR. Both capacitors have 5 nH inductance. Self resonance occur when the imaginary part is zero as can be seen as the minima on the curves. Above this frequency the capacitor starts to become inductive and its decoupling effect is reduced. To obtain a low impedance over a large frequency range, several capacitors can be connected in parallel, where the typical configuration is to have small capacitors with high resonance frequencies close to the load and larger capacitors with slower response closer to the power supply (Prymak, Reed, Randall, Blais, & Long, 2008).

The solid curve in figure 2.8 shows the result of connecting the two capacitors in parallel. As can be seen the impedance is lowered over a larger frequency range. Yet an improved decoupling scheme is not guaranteed if the capacitors are not chosen carefully. It is clearly seen that in between the two resonance frequencies, the total impedance is getting quite high. The total impedance is found to be:

$$Z = \frac{(R_1 + jX_1)(R_2 + jX_2)}{R_1 + R_2 + j(X_1 + X_2)}. \tag{2.20}$$

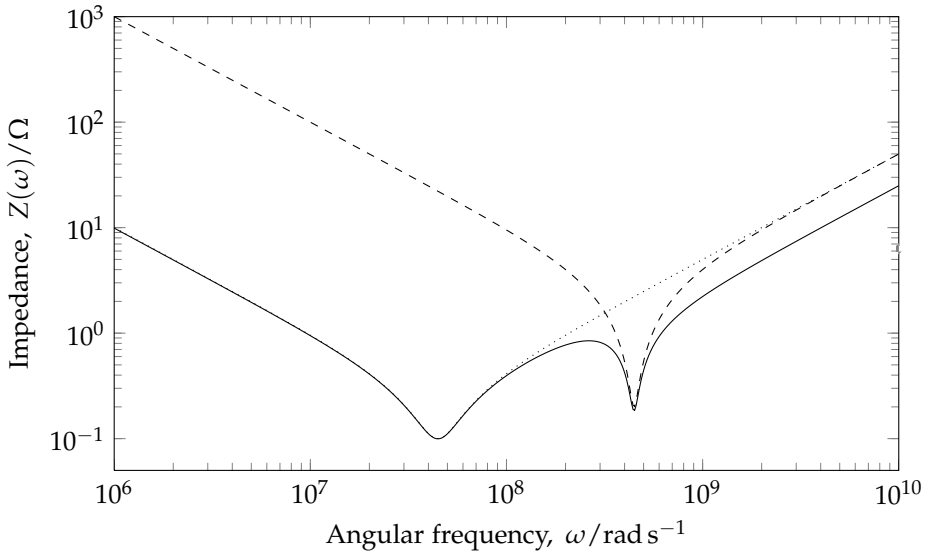


Figure 2.8: Impedance of realistic capacitors versus frequency. Short dotted line shows a 100 nF capacitor with 0.1 Ω ESR and 5 nH ESL while the long dashed line shows a 1 nF capacitor with 0.2 Ω ESR and 5 nH ESL. The solid line shows the total impedance of a parallel connection of the two capacitors.

2.2.3 Frequency content of signals

The common understanding of the frequency of signals is the number of times the signals current changes direction during some time. This consideration does not say anything about the frequency content of the signals above the fundamental frequency. When working with digital signals the common signal shape is square waves with fast rising and falling edges. These signals contains frequency components far above the fundamental frequency. As will be shown, the required bandwidth depends on the rise and fall times of the signals.

Every real periodic signal can be described as a sum of cosine and sine functions called Fourier series, named after Jean-Baptiste-Joseph Fourier for his work on the subject (1888). A function represented by a Fourier series takes the form (Kreyszig, 1999):

$$f(x) = a_0 + \sum_{n=1}^{\infty} \left(a_n \cos \frac{n\pi}{L} x + b_n \sin \frac{n\pi}{L} x \right), \tag{2.21}$$

where a_0 is a DC level while a_n and b_n are the amplitudes of the cosine and sine terms, which are the Fourier coefficients of the signal. While a pure sinusoidal signal will only have one frequency component at the fundamental frequency, all other varying signals will consist of several frequency components.

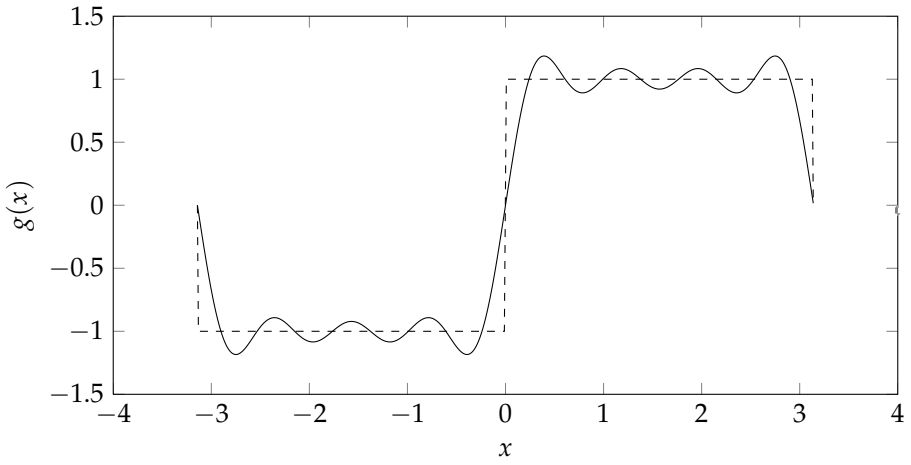


Figure 2.9: The dashed line shows a perfect square wave, while the solid line represents the sum of the seven first Fourier components of the square wave.

Figure 2.9 shows a square wave in its original shape (dashed line) and its reconstruction (solid line) when only the first seven harmonic components are used. The amplitudes of the coefficients are shown in figure 2.10.

The same plot of a trapezoidal waveform is shown in figure 2.11. Its corresponding Fourier coefficients are presented in figure 2.12.

As can be seen when comparing these figures, the trapezoidal wave can be much better approximated with only seven frequency components than the square wave. This is due to the higher rise and fall times of the trapezoid. From this it can be concluded that if the relative time spent in edge transitions is increased, the higher frequency components of the signal are reduced. Less bandwidth is therefore required for the signal to retain its original shape. Additionally, less high frequency noise and radiation is generated, and the demands on the decoupling circuitry can be lessened.

Brooks (2003) proposes that the required bandwidth is estimated by taking one third of the inverse of the shortest rise time in the system:

$$B = \frac{0.3}{t_r}. \tag{2.22}$$

2.3 Noise

Noise is a fundamental effect present in all electronic circuits. Thermal noise will always exist at temperatures above absolute zero. Generation and recombination noise exists in semiconductor devices. Shot noise, caused by charge carriers passing potential barriers appear in junction devices, such as diodes and bipolar transistors. Flicker noise dominates at low frequencies, while thermal noise dominates at high frequencies.

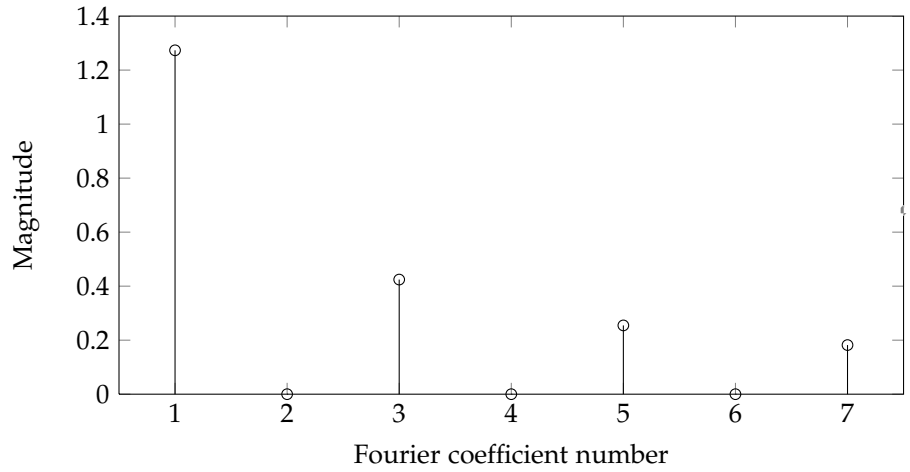


Figure 2.10: The seven first Fourier coefficients of the square wave shown with dashed line in figure 2.9.

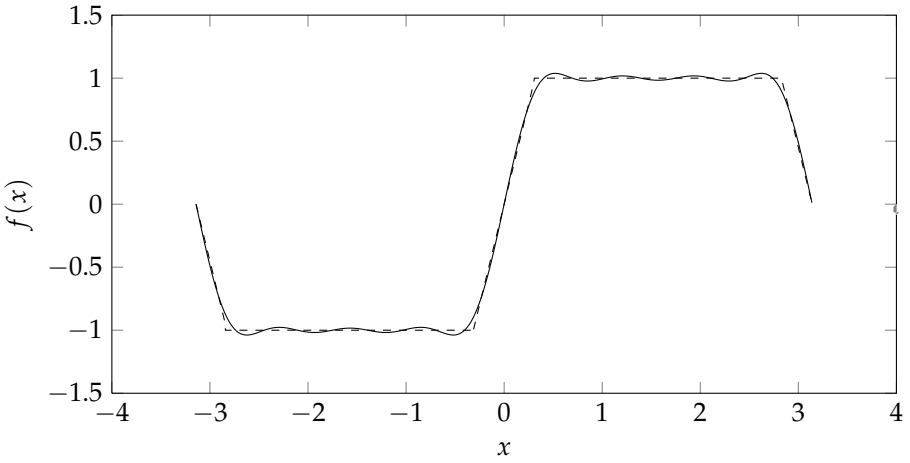


Figure 2.11: The dashed line shows a trapezoidal wave where the rise time from 0 % to 100 % equals 10 % of the period. The solid line represents the sum of the seven first Fourier coefficients of the trapezoidal wave.

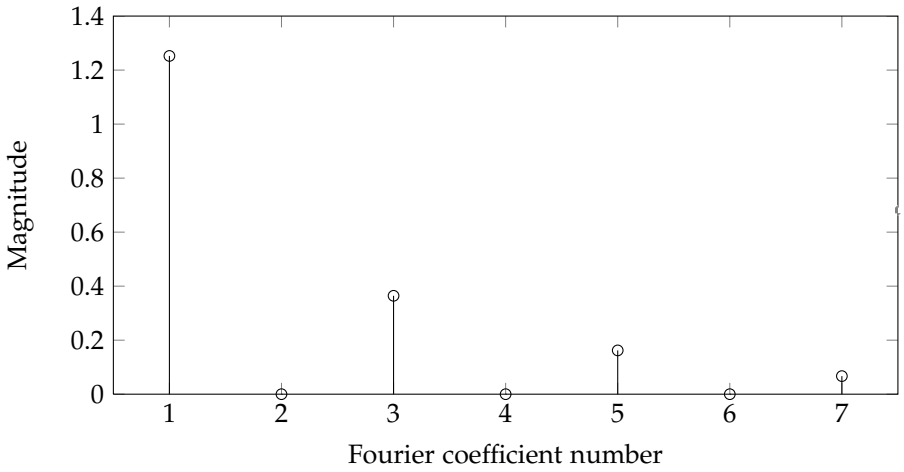


Figure 2.12: The seven first Fourier coefficients of the trapezoidal wave shown with dashed line in figure 2.11.

Noise can be divided into two categories, inherent and interference noise (Johns & Martin, 1997). Interference noise exists due to external factors like power supply hum and interaction between devices, while inherent noise is a part of the fundamental properties of the device.

Although both noise types are affected by the design, inherent noise cannot be completely removed, and may even be amplified by the circuit itself.

The signal to noise ratio (SNR) defines the dynamic area of the circuit, and can easily be improved by increased power consumption, but this is not always a desirable option. Power spent in bias circuits is usually wasted, but inadequate bias schemes may increase the noise which result in a proportional increase in power to maintain the SNR.

2.3.1 Noise in resistors

Resistors are prone to thermal noise inherent in all conductors arising from thermal agitation of atoms. This noise is approximately white for the frequencies relevant here, with a noise power spectral density equal to (J. B. Johnson, 1928):

$$V_R^2 = 4kTR\,. \tag{2.23}$$

The symbol k is Boltzmann's constant, R is the resistance value and T is the absolute temperature.

Thermal noise is independent of the size, shape and material of the resistor. The only ways to reduce the thermal noise in resistors are to lower the temperature or the resistance.

In addition to thermal noise, excess noise occurs when the resistor conducts current. Unlike the thermal noise, current noise vary widely with geometry, materials and the way the resistors are constructed. To unify the way resistor noise is measured the noise index was introduced.

The noise index is defined as the number of microvolts of open circuit RMS current-noise voltage per DC-voltage drop across the resistor per decade of frequency (Conrad, Newman, & Stansbury, 1960):

$$\text{Noise index} = 20 \log \left(\frac{v_{\text{RMS}}}{V_{\text{DC}}} \right) . \tag{2.24}$$

Table 2.3 lists the common noise index in the resistor types produced by Vishay Intertechnology. As can be found from this table, the noise voltage generated by the carbon composite resistors can be 200 times worse than the best bulk metal foil resistors aimed at audio applications. The current noise depends on how the end termination is made, where soldered or welded terminations are better than molded terminations. Also improper handling of the resistor during assembly may degrade the terminations, leading to increased current noise. As an extreme case, Knott (1965) found that an ordinary carbon resistor produced 10^8 times its thermal noise at 3 Hz when passing 4 A.

Table 2.3: Noise index of different resistor types produced by Vishay Intertechnology (*Audio noise reduction through the use of bulk metal foil resistors*, 2005).

Technology	Noise index /dB
Bulk metal foil	-40
Wirewound	-38
Metal film	-32 to -16
Thick film	-18 to -10
Carbon composite	-12 to $+6$

2.3.2 Noise bandwidth

The usual definition of bandwidth in e.g. amplifier circuits is the frequency span between the points on the frequency range where the signal transmission has been reduced to -3 dB. The noise bandwidth Δf, on the other hand, is the frequency span of a rectangularly shaped power gain curve equal in area to the area of the actual power gain versus frequency curve and where the peak gain is equal for both curves (Motchenbacker & Connelly, 1993). This

can be expressed as:

$$\Delta f = \frac{1}{A_{v0}^2} \int_0^\infty |A_v(f)|^2 \, \mathrm{d}f \,, \tag{2.25}$$

where A_{v0} is the peak magnitude of the voltage gain and $|A_v|$ is the magnitude of the frequency dependent voltage gain.

From the thermal expression given in equation (2.23) the noise voltage depends on the frequency bandwidth indicating an infinite noise voltage due to an unlimited frequency bandwidth. In practice there will always be some shunt capacitances that limit this voltage. A capacitor in parallel with a resistor forms a low pass filter which reduces the noise bandwidth, without adding any additional noise as ideal capacitors are noiseless.

It can be shown that a resistor in parallel with a capacitor have an output root mean square (RMS) voltage equal to (Motchenbacker & Connelly, 1993):

$$E_{\text{no}} = \sqrt{\frac{kT}{C}} \,, \tag{2.26}$$

and is thus independent of the resistor value.

2.3.3 Noise summation

When adding two sinusoidal signals with a specified amplitude and phase, the resultant voltage can be found by using phasor algebra. Noise sources, on the other hand, may contain a large amount of different frequencies with random amplitudes and phases, where the noise sources are completely uncorrelated. In such cases the total output power will be the sum of the power from each individual noise source. Thus adding i number of uncorrelated noise sources must be performed by adding their mean square values, giving the mean square value of the sum:

$$E_n^2 = E_1^2 + E_2^2 + \ldots + E_i^2 \,. \tag{2.27}$$

If the noise sources are correlated an extra term will be added to the expression in equation 2.27 (Motchenbacker & Connelly, 1993).

2.4 Printed circuit boards

2.4.1 Parasites

Once a circuit is implemented physically it is prone to parasites caused by copper layout and component placement. Inductance and capacitance in PCBs can be decisive for the system performance, wheter they are desired or not.

Inductance

The inductance per meter in a microstrip trace can be approximated to

$$L \approx Z_0 T_p, \tag{2.28}$$

where Z_0 is the characteristic trace impedance and T_p is the propagation delay (H. W. Johnson & Graham, 1993). The impedance (Ω) and propagation delay (ps/mm) is given as:

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \tag{2.29}$$

and

$$T_p = 3.35\sqrt{0.475\varepsilon_r + 0.67}\,. \tag{2.30}$$

Here w is the tracewidth, t is the line thickness and h is the trace's height above ground. Standard FR4 laminate used for PCBs have a relative permittivity of $\varepsilon_r = 4.7$. The inductance is mainly affected by the microstrip's height above the ground plane. This equations are valid for narrow microstrips where $0.1 < w/h < 2.0$ and $1 < \varepsilon_r < 15$.

2.5 The Universal Serial Bus

Since its first incarnation in 1994, the universal serial bus (USB) has become one of the most successful peripheral buses for personal computers to date. Its ease of use made it a welcome replacement for the cumbersome parallel and serial buses it replaced.

Revision 2.0, released in 2000, brought a number of improvements to the standard. Most notable was a 40-fold increase in bandwidth, from 12 Mbit/s to 480 Mbit/s, allowing for USB devices with higher bandwidth requirements, like storage solutions and networking.

The USB specification also defines a number of device classes that will behave in a standardized way. This eliminates the need for special driver software for simple devices, and reduces development time and cost. For the end user, things are also greatly simplified by this architecture because it permits plug-and-play usage patterns. The device will also be compatible with other or newer operating systems, even though abandoned or unsupported by the original vendor.

2.5.1 USB communication flow

The universal serial bus (USB) is a one host bus, where a single host controller coordinates the bus. Differential signaling over a single twisted pair is used in a point to point connection. The data transfer is asynchronous as no clock

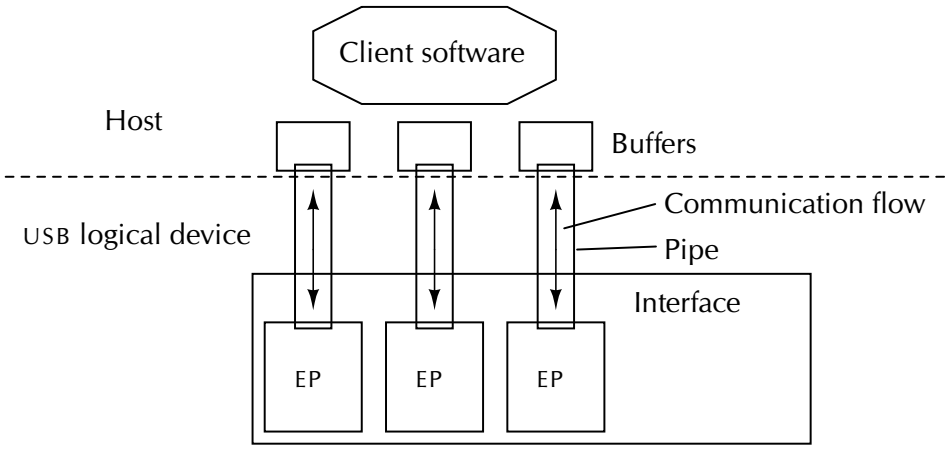


Figure 2.13: USB communication flow (*Universal Serial Bus Specification*, 2000). Communication between the USB host and the USB device is performed through *pipes*.

signal is present. Data is only transmitted by one device at a time.

Figure 2.13 shows the USB communication flow (*Universal Serial Bus Specification*, 2000). This flow can be divided into a host side and a device side. Client software on the host side communicates with the device functionalities through USB software programming interfaces.

Each USB logical device is composed of a collection of independent endpoints where a group of endpoints implement an interface. The term endpoint is used to describe the point where data leaves or enters the system. The endpoints are uniquely referenced by an endpoint number and data direction together with the logical device address. Each endpoint can have only one data direction which is defined relative to the host, where an outward endpoint receives data from the host and an inward endpoint transmits data to the host. An association between an endpoint on a device and software on the host is called a pipe. There are two types of pipes, *message pipes* and *stream pipes*.

2.5.2 USB devices

Descriptors

Almost every type of peripheral computer component can be purchased with a USB interface, for example mice, printers and desktop speakers. Common for all devices is that they support a standard method of reporting device functionality. Information about data transmission types, data handling capacity and functionality is stored in the devices in *descriptors*. These

are tables of data formatted in a specific way describing both endpoints, interfaces and configurations.

Every USB device must have an endpoint with endpoint number zero to handle control signals in both directions, which constitute the default control pipe. This control endpoint handles standard device requests in addition to device and vendor specific device requests. Before the device is properly configured, this is the only accessible endpoint.

Enumeration

When an USB device is attached to the bus, *enumeration* is performed. In a successful enumeration the device is moving from the *attached* to the *configured* state and is assigned an unique seven bit address. When a device is configured the host has read its descriptors, and knowing its capabilities a configuration is chosen. A device may have several configurations, but only one can be used at a time.

2.5.3 Transfer types

Four different transfer types exist in the USB specification. These are *control*, *interrupt*, *bulk* and *isochronous* transfer types. Only control and isochronous transfer types are of interest for the application, and are therefore briefly described here.

Control transfer

A control transfer is intended to support configuration and status type communication between client software and its function. A control transfer is composed of a setup stage, a data stage and a status stage. As these transfers adhere to a specific format they are only carried out through message pipes.

Isochronous transfer

The isochronous transfer is suitable when one requires a continuous data flow where the order and the timing of the data arrival is of importance. An isochronous pipe is guaranteed the granted bandwidth and a bounded latency, ensuring a continuous data flow as long as data is provided. There is no retrying if delivery fails, as data is considered useless if it does not arrive on time. No handshaking is performed. An isochronous pipe operates in simplex mode and is bound to a single endpoint number in the appropriate direction.

2.5.4 Feedback

As data is transferred asynchronously over the USB bus some means of synchronization may be necessary. For example when receiving audio data over an isochronous out pipe, some synchronization is necessary to adapt the data rate to the sampling frequency. Three different synchronization types exist:

Asynchronous Sample clock locked to external clock or free running internal clock.

Synchronous Sample clock locked to start of frame (SOF) or micro start of frame (MSOF) for high speed devices.

Adaptive Sample clock locked to data flow.

If the USB device contains its own clock which determines the data rate, asynchronous feedback can be used to alter the amount of data sent from the host in each transmission. In a high speed USB environment, a MSOF package arrives every 125 µs as a system heart beat, independently of whether data is transmitted or not. Using an internal phase locked loop (PLL), the USB device can use this signal to perform synchronization. Finally adaptive synchronization can be used, where synchronization is performed by adjusting the device's sample rate to the data stream.

2.5.5 USB audio device

In addition to the standard USB class, several device specific sub classes are specified to generalize their functionality making them compatible with standardized drivers on the host side. One such predefined device-class is the *USB Device Class Definition for Audio Devices* (Knapen, 2006). When a device conforming to this specification is plugged into a USB-host, its capabilities will be reported to the host during *device enumeration*. If the host has drivers for this device class available, the user will now be able to select the device as an input or output device for audio, without installing any additional software. The audio class supports a comprehensive collection of features including clock control and sound processing. Sampling frequency synchronization between the host and the device can be adjusted to less than a hertz inaccuracy when using asynchronous feedback.

Commercial solutions commonly available today offer only limited fidelity in terms of sample rate and bit depth. A maximum sample rate of 48 kHz and 16 bit sample size is not uncommon. The systems are often targeted as low-cost solutions, and they perform accordingly with poor sample rate synchronization. High-performance solutions do exist, but these usually consist of expensive studio-grade equipment with proprietary software for the host PC. For ease of use the USB audio class is preferred.

Chapter 3

Implementation

The system is based on a modular design, where the different components operate more or less independent of one another. The implementation process of each module is described in this chapter. This covers considerations of part selection, topologies and system solutions.

At the end of the chapter, the final system is presented.

3.1 Microcontroller

The main criteria when choosing a microcontroller was that it had built in high speed USB capabilities. An attempt was made to find a microcontroller as small as possible to ease the implementation, but at the same time powerful enough to support the data rate of 24 bit, 192 kHz audio.

The 32 bit multimedia application processor AVR32AP7001 from Atmel fulfilled these criteria. Together with the AP7000 and AP7002 versions it makes up the AP7 family. As the authors both had experience with this microcontroller prior to this work, it was chosen to minimize the development time. Also, development tools such as programmers and starter kits were already available.

The controller has a great amount of peripheral connectivity options, making it suitable for a single chip multimedia system. Among these are synchronous serial communication (SSC), two wire interface (TWI), and serial peripheral interface (SPI) modules which will be used to communicate with the DAC, clock and volume controls, respectively. In addition, a lot of general purpose IO lines are available for control signals.

To reduce the power consumption, the controller is equipped with an extensive power management module which makes it possible to scale or

turn off the clock to every module. Additionally, the bus is divided into a high speed bus plus two peripheral bus bridges to allow for both high and low speed modules. Reducing the power consumption through clock management can lead to less noise on the supply rails and reduced power supply requirements.

The AP7001 is the smallest controller in the AP7 family and the only one available in a non ball grid array (BGA) package, a 208 pin quad flat pack, which makes it more suitable for hand soldering. Choosing the AP7000 adds two Ethernet media access controllers (MACS) and an LCD controller. If the system was to be extended to support network audio streaming, and a graphical interface, these would be desirable features.

The Linux kernel also runs on the AVR32 architecture, thereby opening for the use of a vast collection of multimedia software.

As the controller does not have any internal program memory, this has to be added as an external device. The 16 Mbit NAND flash AT49BV160D is used for this purpose. Configuration of the memory is done automatically at power on through the common flash interface (CFI).

3.2 DAC

The best audio dataconverters have now for quite some time been transparent to human senses when used properly.

Table 3.1 lists some of the highest performance audio DACS found in the market today, their dynamic range (DR) and total harmonic distortion plus noise (THD+N). Both the dynamic range and THD+N are measured with a 0 dB_{FS} signal applied at 44.1 kHz sampling frequency unless otherwise noted. The dynamic range is measured using A-weighted filtering. All the DACS support 24 bit linear pulse code modulation (LPCM) at up to 192 kHz sampling frequency.

Table 3.1: Key parameters for several high performance DACS. The data for the AKM AK4399 is measured at $f_s = 48$ kHz, the others at $f_s = 44.1$ kHz.

Vendor	Part	Dynamic range/dB	THD+N/dB
Texas Instruments	PCM1794A	127	−108
Wolfson Microelectronics	WM8741	125	−100
Analog Devices	AD1955	122	−110
AKM	AK4399	123	−105
Cirrus Logic	CD4398	120	−107

The PCM1794A Burr-Brown DAC from Texas Instruments has been chosen due to its slightly better dynamic range. It uses a mixed architecture of inverted complementary offset binary code (ICOB) and a 3rd order, 5 level delta sigma modulator. The outputs are differential current sinks, which can take 66 different levels. When the input is zero the DAC sinks -6.2 mA from both outputs, while a full scale input gives a current swing of 7.8 mAP–P at each output. It requires a 3.3 V supply for the digital part and a 5 V supply for the analog outputs.

3.3 DAC clock

The DAC clock must be able to generate three different clock signals simultaneously, which all have to be synchronous. These are used as bit clock, word clock and system clock, which frequencies depends on the audio sampling frequency. Table 3.2 list the needed frequencies. To fulfill these requirements the clock must be programmable in some way.

Table 3.2: Required clock frequencies for various sample rates.

Sampling frequency F_s/kHz	Word clock F_s/kHz	Bit clock $64F_s$/MHz	System clock $384F_s$/MHz
32	32	2.048	12.288
44.1	44.1	2.8224	16.9344
48	48	3.072	18.432
96	96	6.144	36.864
192	192	12.288	73.728

The CDCE706 clock generator circuit from Texas Instruments has been chosen to generate the required clock for the USB audio data. The circuit can generate six different clocks with a wide range of frequencies from a single crystal, utilizing three internal PLLS and several multiplexers and dividers. The clock signals are reported to have a jitter as low as 60 ps RMS at 50 MHz output frequency with one PLL and one output active. Rise and fall times are typically on the order of 0.6 ns (*CDCE706 Programmable 3 PLL clock synthesizer/multiplier/divider*, 2008). As shown in section 2.2.3, transition times this short implies a considerable amount of high frequency components. To mitigate this the clock circuit is equipped with a slewrate limitation which can be programmed to increase the rise time to a typical value of 3.3 ns.

3.3.1 Clock decoupling

A parallel connection of five capacitors of different values have been used for decoupling at the clock supply rails according to the discussion in section 2.2.2. The simulated resulting equivalent impedance to ground is shown in figure 3.1.

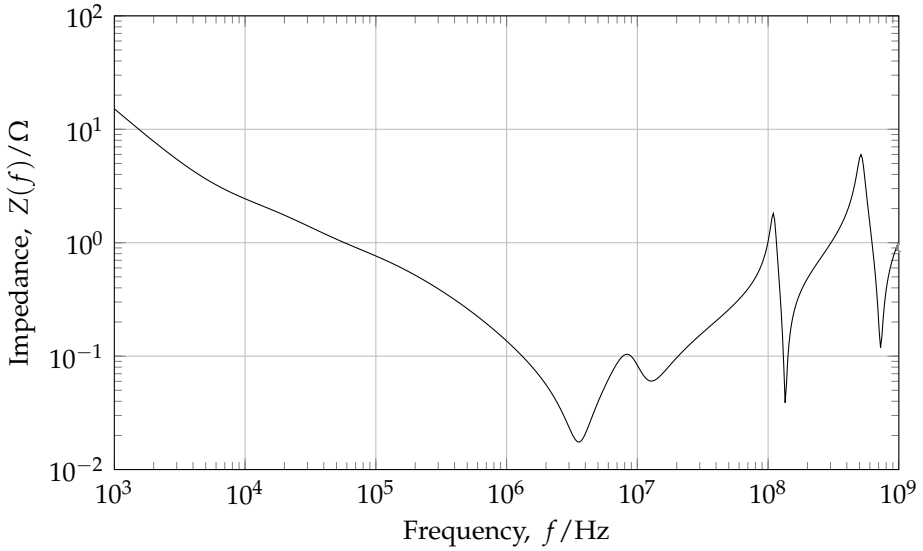


Figure 3.1: Simulated equivalent impedance to ground of five parallel decoupling capacitors.

3.3.2 Crystal selection

Although the CDCE706 accepts crystals with fundamental resonance frequencies ranging from 8 MHz to 54 MHz, only some crystals are suitable for generating the desired frequencies. By choosing a crystal with 28.224 MHz resonance frequency, the required frequencies can be generated without violating the locking range of the internal PLL in the circuit.

3.3.3 SMBUS programming interface

The clock is programmed via the two wire interface system management bus (SMBUS) which is based on the principles of operation of the inter-integrated circuit bus (I^2C), developed by Philips Semiconductors. The bus consist of a data line (SDA) and a clock line (SCL) with open drain configuration which requires a pull-up resistor to the supply voltage to function.

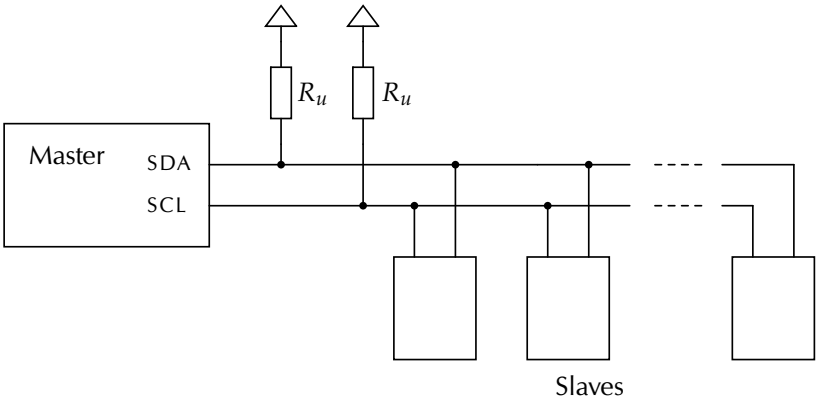


Figure 3.2: Bus topology of the SMBUS. 7 bit addressing allows for 127 slaves.

Several bus masters and slaves can be connected. But only one master at the time can drive the bus. A master can address up to 127 slaves.

Figure 3.2 shows the simplified hardware configuration of the bus. For details about the data protocol, refer to the SMBUS specification (*System Management Bus Specification*, 2000).

3.4 DAC reconstruction filter

The PCM1794A DAC has differential current mode outputs. For this application the signal has to be converted to the single ended voltage domain before it leaves the device.

The filter presented in figure 3.3, sourced from the PCM1794A datasheet (2006), is considered adequate for filtering of the dataconverter output.

Low noise is important in this circuit. The differential to single ended conversion is done by the LT1028 operational amplifier from Linear Technology. This is an ultra low noise operational amplifier with only 0.85 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ input noise at 1 kHz (*LT1028/LT1128 Ultralow Noise Precision High Speed Op Amps*, 1992). To obtain such a low input noise voltage the input transistors are biased with a large collector current. This in turn requires a low source resistance to maintain the low noise. With $R_{31} = R_{33} = 560\ \Omega$ and $R_{32} = R_{34} = 270\ \Omega$, the equivalent input resistance becomes approximately 364 Ω. This falls within the range where the LT1028 has lower noise than other operational amplifiers from Linear, which has an upper limit of 400 Ω.

In the I/V conversion prior to this stage the NE5534 operational amplifiers from Texas Instruments have been employed. They have a slewrate of 13 V/µs (*NE5534, NE5534A, SA5534, SA5534A low noise operational amplifiers*, 2004), which is high enough to minimize the nonideal effects discussed in section 2.1.4.

To some extent the common mode distortion from these amplifiers will

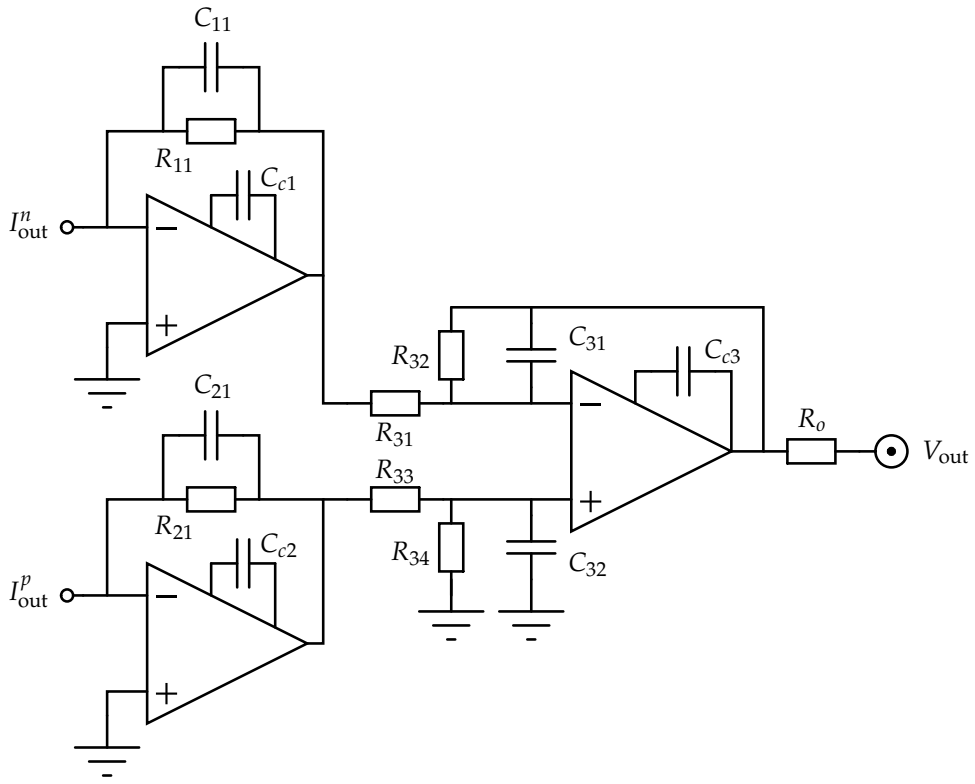


Figure 3.3: Combined reconstruction filter and I/V converter as per the PCM1794A datasheet (2006). The rightmost stage converts from differential to single ended, while the two stages on the left hand side converts the current mode signal to voltage mode.

be suppressed by the differential to single ended conversion in the following stage.

With poles at $F_1 \approx 96$ kHz in the I/V converter and $F_2 \approx 217$ kHz in the differential to single ended stage, the filter has an attenuation of a quarter of a decibel and a phase shift of -17° at 20 kHz.

Human ears are sensitive to phase shifts, but they mostly go unnoticed under normal listening conditions. Lipshitz, Pocock, and Vanderkooy (1982) argues that phase linearity is not a necessity for audio reproduction.

3.5 Attenuator

To avoid distortion from active circuits, a stepped attenuator with passive elements is used. Using relays as switches, it is possible to create an attenuator that behaves very linearly even for large signal swings. A constant output impedance is obtained by using a topology similar to the R–$2R$-configuration

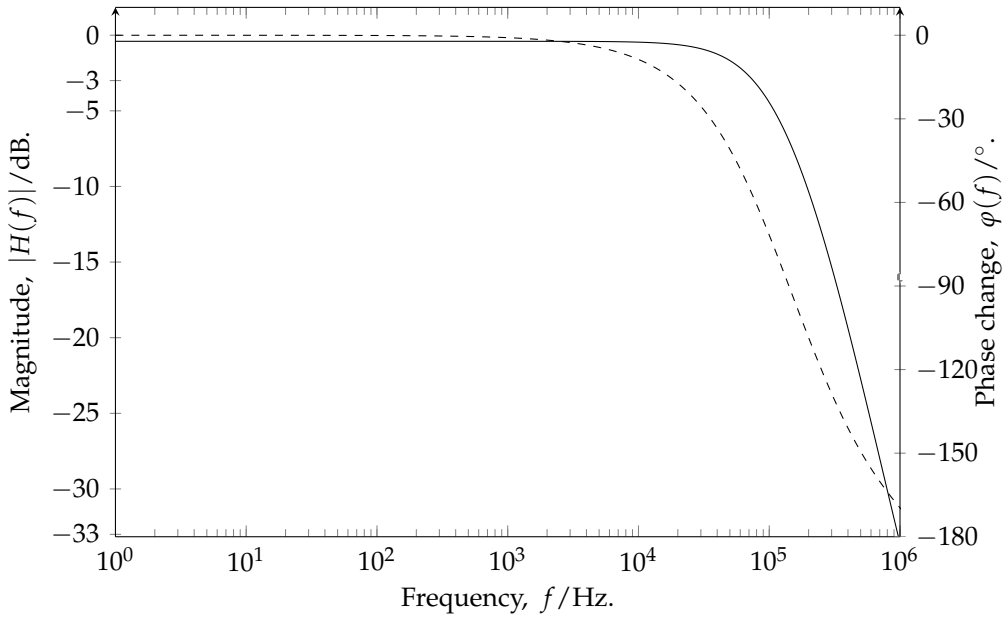


Figure 3.4: Simulated response of the I/V filter. Magnitude is drawn with a solid line, phase is dashed.

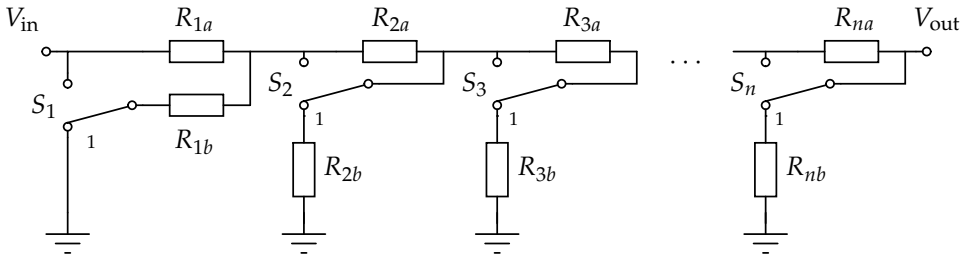


Figure 3.5: Schematic diagram of the stepped attenuator. Each element is scaled in proportion to the previous to provide binary weighted attenuation.

commonly used in DACs.

The circuit diagram of such an attenuator is shown in figure 3.5. When a damping element is disabled, its resistors are either disconnected from the circuit or bypassed altogether.

Each step is dimensioned to give an attenuation so that the ith element in the row will, when connected, attenuate the signal by a factor of $2^{-i/20}$, where $i \in \mathbb{Z} \in [0, n-1]$. This converts to -2^i dB. For a six-element attenuator this translates to a maximum of 64 dB attenuation in steps of 1 dB.

Equations (3.1) and (3.2) describes the resistor values necessary to obtain the desired output impedance. R'_{ia} is the equivalent resistance seen from the output towards the input node with only the ith element enabled. The

input-to-output voltage ratio $V_{\text{in}}/V_{\text{out}}$ is derived directly from the attenuation of the element.

$$R_{ib} = \frac{R'_{ia}}{V_{\text{in}}/V_{\text{out}} - 1}. \tag{3.1}$$

$$R'_{ia} = R_{\text{out}} \frac{V_{\text{in}}}{V_{\text{out}}}. \tag{3.2}$$

Beginning from the input side of the attenuator, all of the resistor values can be calculated recursively, with the proper R_{ia} calculated by subtracting the equivalent resistance of the previous elements:

$$R_{ia} = R'_{ia} - R_{(i-1)\,a}. \tag{3.3}$$

An Octave/Matlab program has been written to perform these calculations, and is included in appendix A.1 for completeness.

The output impedance from the attenuator is the equivalent noise resistance contribution as seen from the following device. It is desirable to make this noise power density less than the noise floor from the preceding stages to not degrade signal quality. Referring to section 2.3.1, metal film resistors have been used in this circuit as they offer low noise at an affordable price.

As long term reliability is wanted from the switches, hermetically sealed reed relays are favorable. Coto's 8L41 reed relays are used. They have a maximum contact resistance of 200 mΩ when applied a 10 mA control current, and can switch up to 250 mA (*8L Series/Spartan DIP Reed Relays*, 2004).

SPI interface

The relays in the attenuator are controlled via serial to parallel shift registers over an SPI link. This interface consists of a clock line and a data line which performs synchronous data transmission.

The shift registers used are the common SN74HC595, which includes an separate latch clock line, used to shift the register content to the outputs. This ensures that all the outputs remains stable during shifting and are set simultaneously.

3.6 Sony/Philips digital interface (S/PDIF)

With the increasing use of digital recording and playback equipment in the 1980s, especially after the introduction of the CD in 1982, there was also a demand for digital transfer of audio data between devices. One of the interfaces that emerged was the Sony/Philips digital interface (S/PDIF). The protocol is very similar to the AES/EBU interface, differing only in the

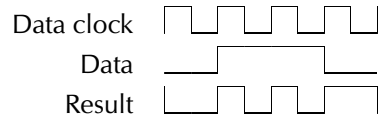


Figure 3.6: Bi-phase mark encoding scheme. The data sequence '0110' is encoded.

interpretation of a status bit. Electrically there are more differences, however.

S/PDIF is intended for use in non-professional home systems, and normally uses an unbalanced 75 Ω coaxial cable or plastic optical fibre for transmission. When using coaxial cable, unmatched connectors are often employed together with low grade video cable. This provides sufficient performance for shorter runs with a very affordable interconnect. An optical interface developed by Toshiba, TOSLINK, supports cable runs of up to 10 m, and gives the additional benefit of galvanic separation of the devices, thus eliminating electrical noise (Sakura, Onobuchi, Ito, & Katagiri, 1988).

S/PDIF is a serial interface, utilizing bi-phase mark (BPM) encoding to embed the clock into the signal. Between two consecutive bits, there will always be a phase change in the encoded stream. A one-bit will have an additional phase change in the middle of its period, whereas a zero-bit will not. This is in effect a variation of the modulation scheme frequency shift keying (FSK), where a different carrier frequency is used to transmit each state of a symbol (Haykin, 2001). In this case square waves are used as carriers, opposed to the pure sine waves of basic FSK. Figure 3.6 depicts the encoding of the data stream '0110'.

With the clock embedded in the data stream in this fashion, the system gains robustness against transmission errors, as the information is defined using phase changes, and not by the amplitude at a given sampling instant.

3.6.1 Data format

Important metadata is added to the audio stream, and the result is divided into blocks, frames, subframes and time slots, listed in descending order of abstraction. A complete subframe is shown in figure 3.7.

A subframe consists of 32 time slots, each containing a BPM encoded bit. The exception is the first four time slots of each subframe, which form a preamble used for synchronization. This preamble consists of an eight bit pattern that can take six different values depending on subframe type, subframe position and the parity of the preceding subframe. The pattern is crafted such as to minimize the DC offset of the line.

The next four time slots contains auxiliary audio data. This can be used for an additional low rate audio channel or extending the sample length to a total of 24 bit.

Time slots eight through twenty-seven carry the audio sample data in

big endian format, i.e. the rightmost time slot contains the most significant bit (MSB). There is always one whole sample per subframe if the link is transferring linear PCM audio.

If an error is detected at the sending end, the validity bit in time slot 28 will be set to indicate that the data is not necessarily a perfect copy of the source. This can be the case if a read error occurs during CD playback.

The user bit of time slot 29 contains subcode data, forming a 192 bit word during a block of 192 frames.

A channel status bit is stored in time slot 30. The bits regarding copy control through the serial copy management system (SCMS) lies here.

Simple error detection is provided by the parity bit of time slot 31. This bit is set so that the sum of the values in time slots four to thirty-one is even.

Two subframes form a frame containing a sample for both channels. A block consists of 192 frames in which the user and channel status time slots carry 384 bit of metadata. The standards specify the usage of this data to detail, but it is far beyond the scope of this thesis to discuss them any further. The interested reader is referred to the AES-3 standard.

3.6.2 Receiving end

At the receiving end of the cable, the signal amplitude will typically be on the order of 0.5 V. Before it can be processed by digital circuits for decoding, it needs to be amplified to a full scale rail-to-rail signal. There are numerous ways to accomplish this, some of which include high speed comparators or opamps. For this task it was decided upon a simple two-stage amplifier design based on tri-statable inverters for power management.

Amplifier

A schematic of the amplifier is shown in figure 3.8. The first stage supplies most of the large signal gain. It is comprised of the closed feedback loop around the leftmost inverter, A_1. The feedback resistor R_f also biases the

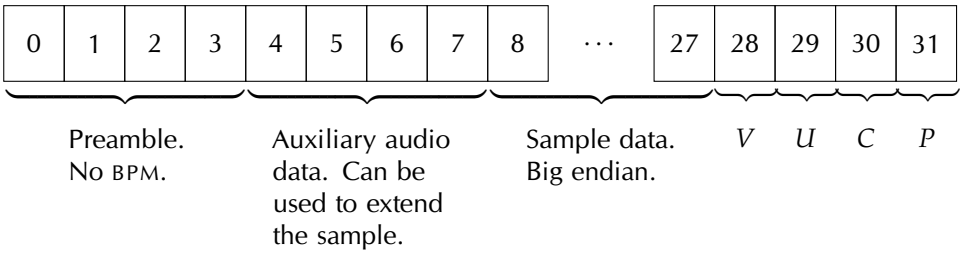


Figure 3.7: Subframe of S/PDIF stream consisting of 32 time slots. V – Validity of audio data. U – User bit. C – Channel status. P – Parity, calculated from time slots four through thirty-one.

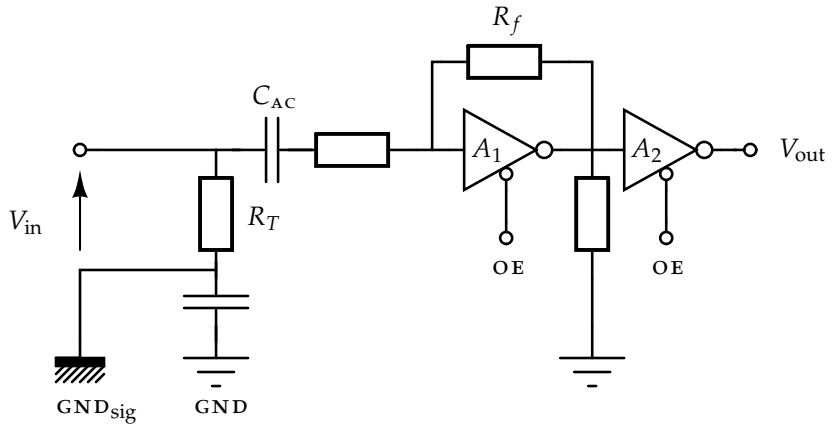


Figure 3.8: S/PDIF amplifier. $R_T = 75\ \Omega$ provides termination. R_f both biases A_1 and provides negative feedback. The output enable (OE) terminals makes it possible to turn off the amplifier.

inverter to its bistable operating point. Such a biasing scheme is called feedback biasing, as bias voltage is supplied via the feedback loop.

The use of a complementary MOS-pair also brings some interesting benefits of power and gain efficiency, although they are not of any significance for this application. Vittoz (1994) shows that for a given bias current, this topology gives the highest transconductance obtainable, and thus gain if the stage is biased in weak inversion. Its equivalent noise resistance is also the lowest one can obtain for a given bias current. For a low power/low voltage system, these factors would be a significant benefit.

Sufficient gain is provided by the first stage for any signal within the S/PDIF specifications, but to provide sharper edge transitions, an additional open loop inverter is employed before the output node.

The capacitor C_{AC} decouples the DC-component of the first gain stage from the cable. The DC offset of a properly dimensioned inverter will be around $V_{dd}/2$ when biased to its bistable operating point, and this voltage must be isolated from the input. As a design guideline, the European Broadcast Union (EBU) recommends a receiver bandwidth from 100 kHz to 6 MHz (Emmett, 1995).

Decoder

The decoding process requires estimation of the signal rate and periodic sampling at this interval. For CD-quality playback this means an incoming data rate of ~2.8 Mbit/s, with a bandwidth of over 5.6 MHz. If the microcontroller core is clocked at 150 MHz, less than 27 cycles are available for each sample of the S/PDIF stream. Over the course of these limited cycles, the microcontroller must decide the value of the current time slot and arrange a

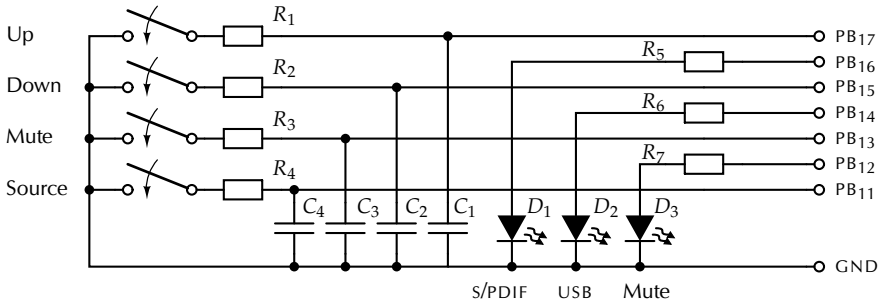


Figure 3.9: User interface to control the volume and input source selection.

complete S/PDIF subframe in memory when enough data has been received.

To overcome this resource limitation, a dedicated receiver circuit is used. Several vendors offer such monolithic decoders, among them AKM, Cirrus Logic, Texas Instruments and Wolfson Microelectronics. The DIR9001 receiver from Texas Instruments was chosen due to availability and its wide support of standards. It can decode a continuous range of sample rates from 28 kHz to 108 kHz. The vast majority of S/PDIF and AES/EBU siblings is supported. Further details are found in the datasheet (*DIR9001 96 kHz, 24 bit Digital Audio Interface Receiver*, 2006).

Audio data and clock signals from the decoder is multiplexed with the microcontroller and clock generator and then fed into the DAC.

3.7 User interface hardware

To control the volume and input source a small user interface was made as shown in figure 3.9. The circuit was soldered on a stripboard and connected with a ribbon cable to the spare connector CN_5 on the digital control unit.

The buttons are equipped with a low pass filter. A 100 Ω resistor and a 100 nF capacitor form a debouncing filter. Normally the line is held high by an internal pull-up resistor in the microcontroller. It will be pulled low when a button is pushed. The *Up*, *Down* and *Mute* buttons control the volume. Selection between the USB, S/PDIF and auxiliary input sources is performed through the *Source* button. When S/PDIF is chosen, D_1 is lit, while D_2 is lit when USB is the selected source. D_3 lights when muting is activated.

3.8 Power supply

All the different components in the system needs a total of five different supply voltages. Because of the separation between the analog and digital domains, this is split into four primary supplies for the analog section,

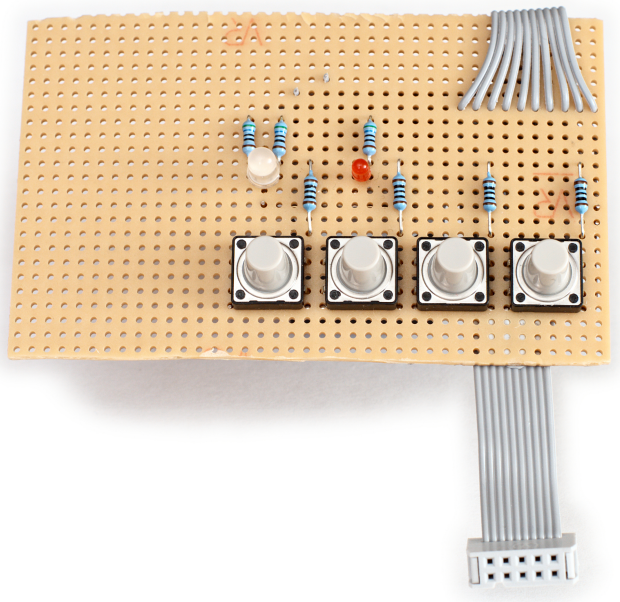


Figure 3.10: Implementation of the user interface.

and a digital supply that is further divided into two rails on the digital control board. The raw voltages are supplied by a mains transformer with tree secondary windings, intended for regulation to 5 V and ±12 V by the manufacturer.

Each of the five primary regulators are variants of the linear series regulator shown in section 2.2.1. They are of the Jung type, named after the works of Walt Jung (2000, 1997, 1995).

Two monolithic linear regulators are placed on the digital control board to deliver 1.8 V and 3.3 V to the microcontroller and the S/PDIF signal conditioner. To lower the power dissipation in these regulators, and to avoid supply contamination from the digital system, a dedicated 5 V regulator is provided for the digital board.

The regulators for the symmetrical ±15 V supplies are completely self contained, i.e. the error amplifiers are driven by the regulated voltage. This improves the regulation performance by a substantial amount, over 30 dB has been obtained (Jung, 1997). But a bootstrapping mechanism is required to ensure proper startup in this configuration. The error amplifiers for the lower voltages, however, are powered from the positive 15 V supply, and therefore does not need any additional startup circuitry.

The schematic of the positive 15 V regulator is shown in figure 3.11. Complete connection diagrams of the power supply are included in appendix B.3.

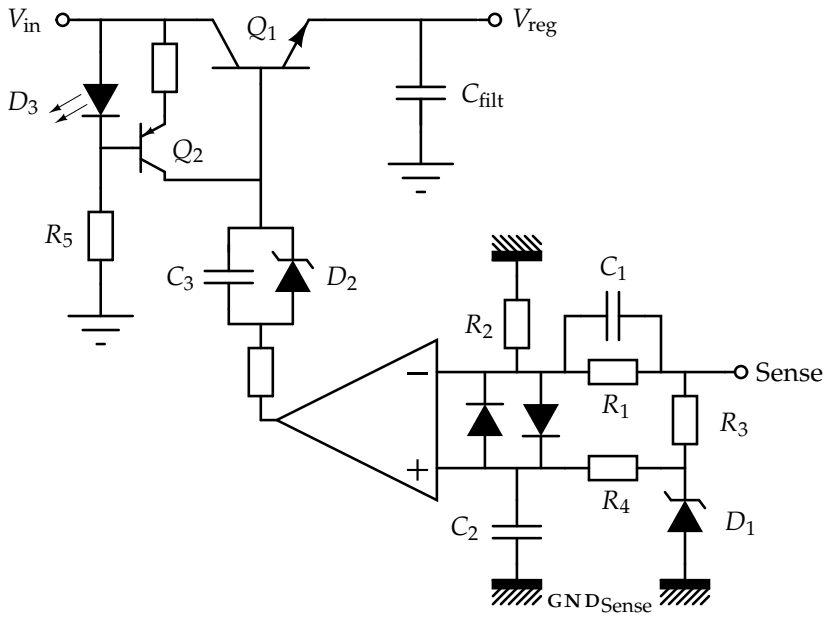


Figure 3.11: Jung positive voltage regulator (2000). The sense and sense ground terminals will be connected to the rails near the load to eliminate parasitic effects in the supply leads.

3.8.1 Startup

The diode D_3 together with the transistor Q_2 will provide a base current to the pass transistor Q_1 as V_{in} rises at power on. At this point the error amplifier is non-functional, and its output lies at zero. Without D_2 this would normally inhibit the current flow to Q_1. But if the Zener breakdown voltage of D_2 is properly dimensioned, current will not be diverted into the amplifier before the regulated voltage V_{reg} is high enough to power the opamp and the voltage reference D_1. The circuit is thus bootstrapped into operation.

3.8.2 Remote voltage sensing feedback

Remote sensing is employed to give better voltage regulation near the load where it is needed. Due to the inevitable series resistance and inductance of the supply leads, good regulation at the regulator terminals does not necessarily imply good regulation at the load. With a dedicated sense line that carries a negligible current, the problem is heavily reduced.

A high-pass filter with a finite stop band is formed by R_1, R_2 and C_1. At DC the sensing voltage is scaled down to match the reference D_1, but at higher frequencies C_1 passes the perturbations to the amplifier.

The reference voltage from D_1 is low-pass filtered by R_4 and C_2. The filter limits the noise bandwidth from the reference and reduces any effects

of insufficient regulation on the reference.

3.8.3 Error amplifier and pass device

Fast regulation of line and load changes requires a high bandwidth in the error amplifier and the pass transistor. But as the bandwidth increases, stability issues become more prominent. Especially with remote sensing the phase margin quickly becomes critical.

Low noise is also a major performance factor. In Jung's original design, the AD825 opamp was used. It has a voltage noise of 12 nV/$\sqrt{\text{Hz}}$. Instead we elected on the NE5534 opamps, the same as used in the I/V-filter (See section 3.4). They have a lower voltage noise of 3.5 nV/$\sqrt{\text{Hz}}$ at a tenth of the cost. Their limited bandwidth makes them less prone to oscillate when the digital circuitry introduces high frequency noise by switching.

As a pass transistor, just about any medium to high power device will do. The complementary bipolar pair 2SA2037/2SC5694 from Sanyo was used at first. They are capable of delivering ample current for the application, and the allowable power dissipation also suits the task. Noteworthy properties are a high gain–bandwidth product ($f_t = 330$ MHz) and a high DC current amplification ($150 < h_{\text{FE}} < 300$) (*2SA2037/2SC5694 PNP/NPN Epitaxial Planar Silicon Transistors*, 2003).

3.8.4 Rectification and prefiltering

The schematics for the rectifier is shown in appendix B.3. Immediately following the rectifier bridge is a *CRC*-filter for ripple reduction. The series resistor R adds a second pole at $\omega_1 = 1/RC_2$. This pole will smooth the unregulated waveform substantially and effectively remove higher order harmonics.

3.8.5 Simulation

Simulations of the regulator shows excellent results. The models however, are limited in accuracy. It was not attempted to accurately model all the parasitic effects in the power supply.

However, it was noted that when introducing estimated parasitic inductance and capatitance in the remote sensing loop, the regulator tended to oscillate.

3.9 Prototyping

To test the function of some key components, prototypes were made. The hand crafted PCBs are presented here. High performance was not a purpose

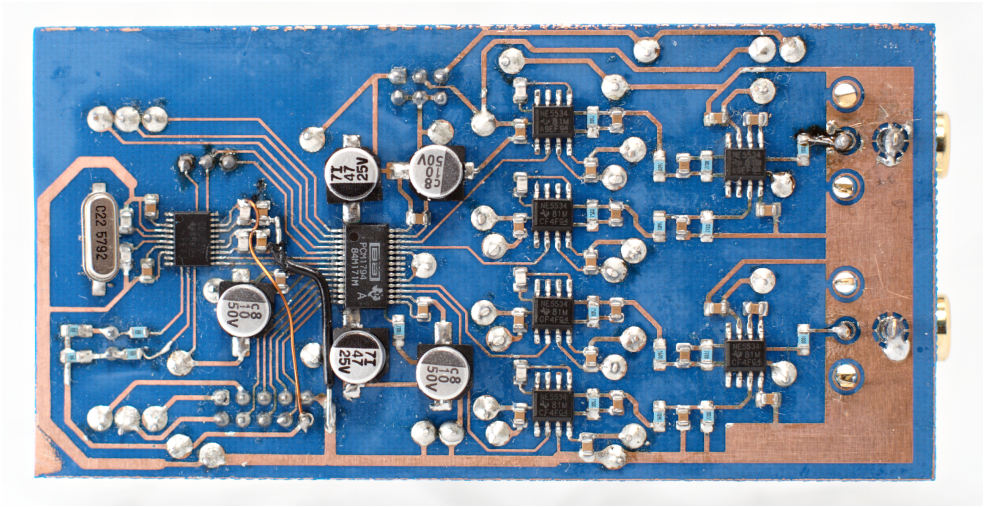


Figure 3.12: Prototype PCB with clock generator, DAC and reconstruction filter.

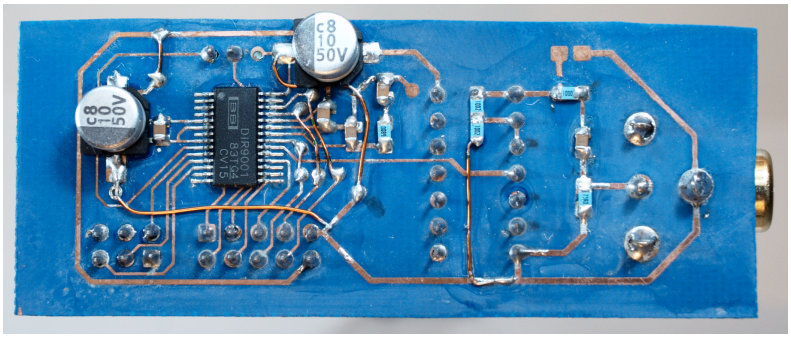


Figure 3.13: Prototype PCB with S/PDIF signal conditioner and decoder. Backside shown. Topside contains headers and the inverter circuit used as an amplifier.

of these boards, only system functionality. For program developement, the starter kit STK1000 from Atmel was used, which contains an AP7000 microcontroller. This was connected to the prototype boards with ribbon cable, providing control and data signals.

Figure 3.12 shows the board for testing the clock generator and the dataconverter with reconstruction filter. As mentioned in section 3.3 the clock must be programmed over a serial interface. In addition the DAC needs proper control signal to work as intended. This board gave a possibility to test the clock programming and playback of USB audio data.

The S/PDIF decoder with signal conditioner is depicted in figure 3.13. While provided the correct control signals, S/PDIF reception was tested. The audio data was passed on to the DAC and played back in a desktop speaker.

3.10 Printed circuit boards

Three separate PCBs have been made for the digital control unit, the analog DAC unit and the power supply respectively, to allow for separate testing. As the price of PCBs increases with the number of copper layers, processing tolerance and area, both the analog DAC card and the power supply was implemented using double sided PCBs. Because of the large number of power and ground pins on the microcontroller, two additional copper layers were added dedicated to a ground and a power plane.

The PCBs were designed in the CAD program CADint. This program allows for mapping between the schematics and PCB layout, simplifying the layout process. PCBs were ordered from PCBCart in China. It was used a standard process with minimum trace width of 203 µm and a copper thickness of 35 µm. The printed circuit board layers are shown in appendix C.

3.11 Firmware

Firmware has been programmed in C to obtain the desired functionality of the system. This includes drivers for the external circuits and usb device functionality. A short introduction to the code are given here. For further documentation refer to the comments included in the program files.

3.11.1 Main program flow

The main functionality of the program is illustrated briefly in figure 3.14.

System initialization

Once the system is powered the hardware is given its initial setup. To generate a 120 MHz main clock, the 20 MHz crystal frequency on the main oscillator has to be multiplied by an internal PLL. This is done when setting up the power manager. For the system to be able to handle interrupts, the interrupt controller has to be configured and every interrupt routine must be registered. This is done when initializing the internal modules. Control signals for the DAC and S/PDIF receiver are issued and the external clock is programmed to generate 44.1 kHz sampling frequency as default.

Main program execution

As the system is mainly interrupt driven, the main loop only consists of a function which reads audio data from the USB FIFO buffer when the USB device is configured and data is present. Every time a new audio frame has been received, the audio data is written to a FIFO buffer, where the DAC

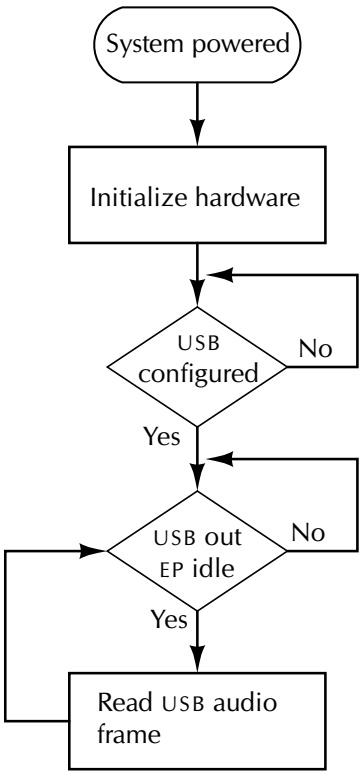


Figure 3.14: Flow chart of main file.

retrieves data.

Audio data buffering

Some means of buffering has to be performed when retrieving data over USB as discussed in section 2.5. A simple FIFO buffer is programmed for this purpose as illustrated in figure 3.15. The buffer consists of n number of banks, each with a size determined by the number of bytes received in a transmission. When a bank is full, the write pointer USB buffer index is incremented, pointing to the subsequent bank. If all banks are filled up, the pointer is reset to the base address, starting at the bottommost buffer. The audio data is read by the SSC_1 module feeding the DAC. The DAC buffer index pointer function similar to the write pointer. The write speed is determined by how fast data arrives on the isochronous USB endpoint, while the readout is controlled by the external clock. This emphasizes the need for rate feedback on the USB streaming endpoint. If the write and read speed are different, the pointers will collide, causing corrupt data to be sent to the DAC.

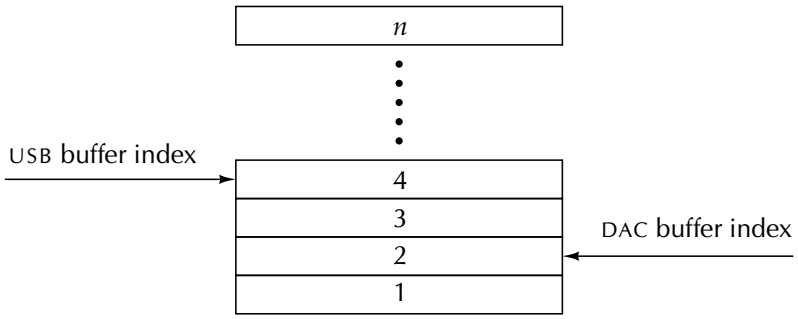


Figure 3.15: Audio FIFO buffer organization. n buffers exist.

3.11.2 User interface firmware

Buttons and LEDS have been used to make a simple user interface as discussed in section 3.7. The buttons which are connected to PIO pins trigger a pin-change interrupt every time the input level changes. When a button is pressed, further interrupts are disabled and a counter is started. The interrupts are not enabled again before this counter has reached a certain value, this to mitigate contact bouncing in the switch. A push on a volume button alters the volume level by one single step. When the source selection button is pressed, the audio input source are changed in a circular manner through USB, S/PDIF and AUX. When USB is selected, the S/PDIF receiver is disconnected from the data and clock lines feeding the dac. Simultaneously, the S/PDIF signal conditioner is disabled and the external clock is enabled. The opposite is true when S/PDIF is the input source. When selecting AUX the DAC output is disconnected from the attenuator and a separate analog input is selected. Figure 3.16 shows the main functionality of the buttons.

Two 8 bit shift registers control the relays in the volume and source selection circuitry. Each audio channel is controlled separately allowing for volume balance control, an unimplemented feature. The bit arrangement for each shift register is shown in figure 3.17. When a button is pressed, the corresponding bits in this byte are altered. When all the buttons have been checked for interrupt and the two bytes are updated, the new settings are shifted out on the SPI lines.

3.11.3 Universal Serial Bus (USB) firmware

The firmware that handles the USB functionality is quite comprehensive so only a brief description will be given. It is based on a software framework provided by Atmel intended for the AT91SAM9RL64, an ARM-9 based microcontroller, which is quite similar the AVR32AP7001 used here. Thus all the hardware specific code had to be adapted to this controller.

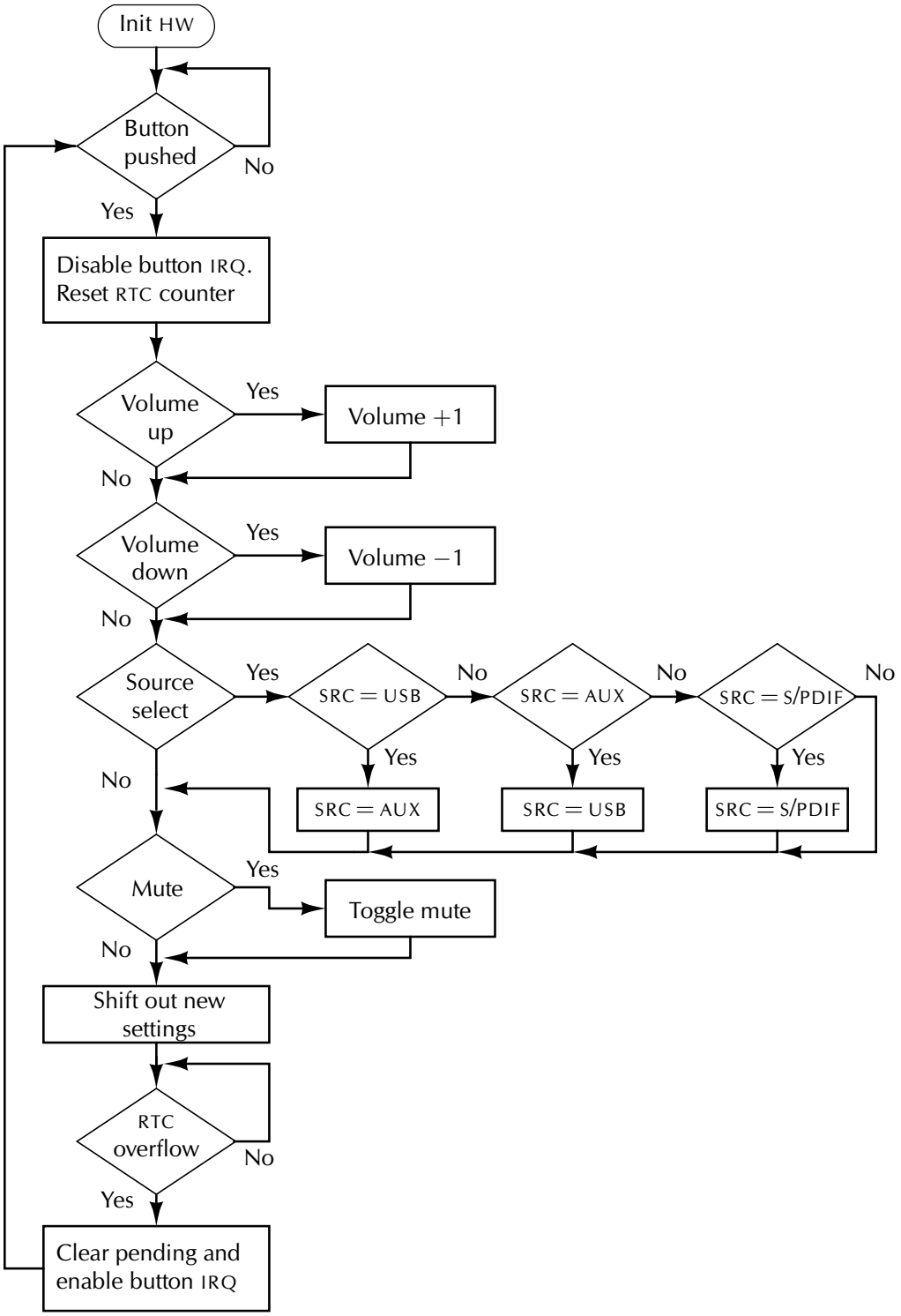


Figure 3.16: Flow chart of user interface firmware.

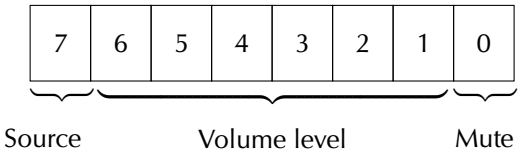


Figure 3.17: Attenuator control byte for one channel. Six bit represent the volume level, while the remaining two bit control the source selection and mute.

When the device is connected to an USB host, enumeration is performed. Only two endpoints are configured, the control endpoint zero and an isochronous out endpoint for audio streaming. All the control are performed over the control endpoint. As the out endpoint is isochronous, no control signals are required. Data just arrives when transmitted by the host.

Several interrupts may appear in the USB module. During enumeration the *end of reset* interrupt occurs, and if the device is detached a *suspend* interrupt is triggered. The most frequent interrupt is the *endpoint* interrupt. Figure 3.18 shows the main features of this interrupt.

The endpoint interrupt can be divided into control interrupts directed to endpoint zero and interrupts directed to the remaining endpoints. Presently, this is only the out endpoint, which simply receives data when called by an interrupt. When data is read, the endpoint status is set to idle, ready to read the next incoming data. The control interrupts are a bit more complex. The control endpoint receives requests which can be device specific or more general. These message streams have a predefined structure. Device specific requests supported are the SET_CUR and GET_CUR which is used to control for example the volume and mute status. This functionality is supported and makes it possible to control the attenuator over the USB connection. However, as the system includes separate buttons, changing the volume by pressing these should be reported to the USB host. This can be implemented as a separate USB HID device or as an integral part of the audio control.

The standard requests are used to control the device functionality. Among other these are SET_ADDRESS, SET_INTERFACE and SET_CONFIGURATION, used in the enumeration process. Unsupported requests are handled by returning a stall handshake.

3.12 Final system

The various modules discussed in the preceding sections have been assembled to a complete system. A photograph of the system is shown in figure 3.19.

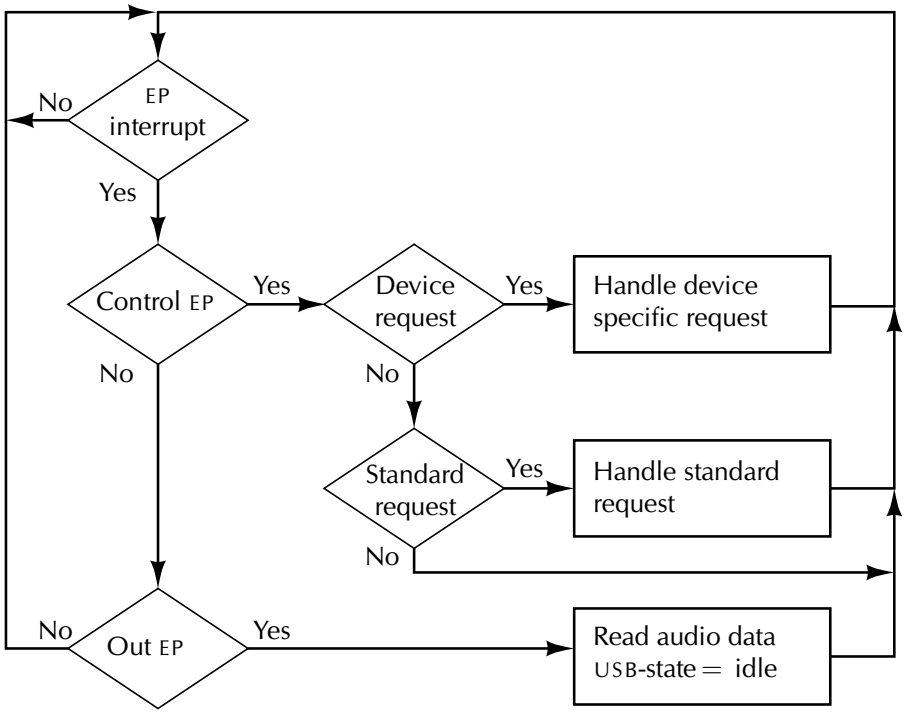


Figure 3.18: Flow chart of USB endpoint (EP) interrupt.

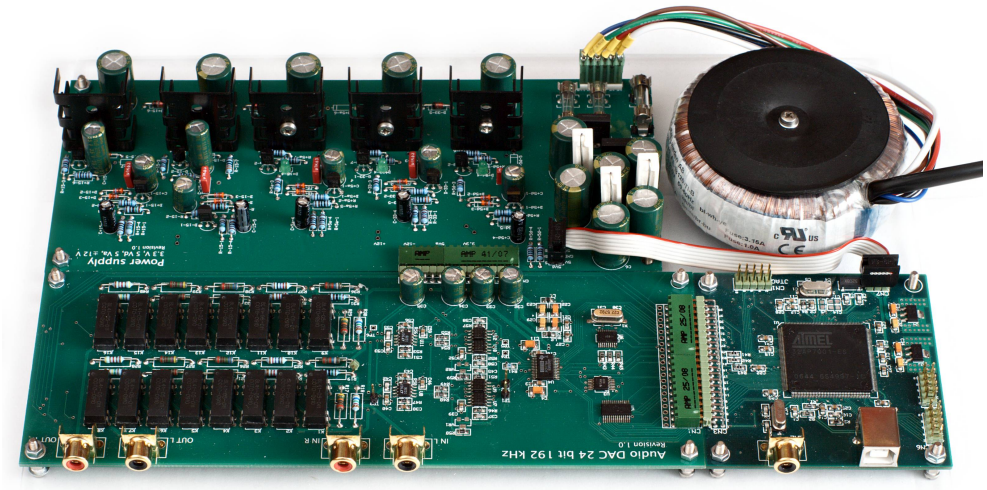


Figure 3.19: Final assembled system.

Chapter 4

Test methodology

Testing and measuring the performance of the product is an important aspect of this thesis. As mentioned in the introduction, high performance is a major goal. A rigorous testing methodology is required to measure the extreme performance the components used are able of producing.

Important tests include dynamic dataconverter performance and power supply regulation. This will be elaborated in the appropriate sections.

4.1 Test equipment

A range of instruments were used when measuring the system. Manufacturer and model names are listed in table 4.1. Equipment will later only be referred by their functional name, e.g. *the oscilloscope*.

4.2 Dataconverter

Dataconverters in general have a set of fundamental performance parameters to measure. Converters intended for use in audio applications are typically only characterized by a subset of these parameters, as not all are applicable to human hearing. The dynamic parameters signal to noise ratio (SNR), total harmonic distortion plus noise (THD+N) and dynamic range (DR) will be tested.

As this is an audio system, it becomes meaningless to test for performance parameters that cannot be sensed by human beings. The Japan Electronics and Information Technology Industries Association (JEITA) have published specifications regarding testing methodology for CD players. JEITA CP-2402A

Table 4.1: Test equipment used.

Instrument	Vendor	Model	Description
Oscilloscope	Hewlett Packard	Infinium 54845A	8 GSa/s
Oscilloscope probes	Hewlett Packard	1600	10:1, 10 pF, 500 MHz
Signal generator	Hewlett Packard	33120A	15 MHz
Audio analyzer	Audio Precision	SYS-2722	Analog and digital.
Electronic load			Own design. See §4.5.2

(2002) specifies that a -60 dB_{FS} sinusoid test tone is to be used when measuring the total harmonic distortion plus noise (THD+N) performance of the converter.

Additionally, the signal bandwidth should be limited to ± 0.1 dB between 4 Hz and 20 kHz, and be attenuated with 60 dB at 24.1 kHz. A-weighting of the spectrum is needed to compensate for the frequency dependency of the human hearing, and is specified by CP-2402A.

This test standard is not in common use for high performance audio DACs. It is therefore not used in this system. The bandwidth from 20 Hz to 20 kHz is considered in the measurements. A-weighting is often used as it improves the measurement results, but to get more realistic results, it is not employed here.

All of the dynamic parameters of the audio system can be derived from frequency spectra when applying proper test signals.

The audio benchmarking instruments from Audio Precision are widely regarded as the *de facto* standard for audio equipment measurements.

4.3 Clock jitter

The two clock signals important to the DAC performance, F_s and F_{sys}, were tested for timing errors. Period jitter on the clock signals was measured using the oscilloscope set up for jitter measurement. Both P–P and RMS measurements were taken. As there are two sources of these clock signals, both the CDCE706 and the clock signals from the S/PDIF receiver were measured. The effect of changing the CDCE706 output slewrate from the nominal rise time of 0.6 ns to 3.3 ns was examined. The oscilloscope probes was connected close to the DAC.

4.4 Reconstruction filter

The filter was tested alone, without the PCM1794A DAC mounted. This was done to avoid test signal distortion by the DACS outputs.

The signal generator was used to insert a test signal into the filter. This was done through a series resistor connected to the TP_1 test point, shown in figure B.7. The test point TP_2 was left unconnected as it is virtually grounded by the following operational amplifier. Using the oscilloscope, both the input and output signals were measured. The output signal was collected before the attenuator at testpoint TP_3.

4.5 Power supply

There are three main performance parameters of power supplies: Line regulation, load regulation and noise. The first specifies how good the power supply is at rejecting variations in the raw supply. The second tells how good the regulated voltage is maintained when the load changes. The noise stems from the regulator itself, and is ideally unaffected by both line and load.

4.5.1 Line regulation

The only major disturbance on the line that needs to be regulated is the ripple from the rectifier. This can be measured both in the time domain and in the frequency domain by observing the regulated voltage. The line regulation is defined as the ratio between the ripple before and after the regulator. Expressed in decibels, this becomes

$$20 \log \frac{V_{r,\mathrm{reg}}}{V_{r,\mathrm{raw}}} . \tag{4.1}$$

The oscilloscope was used to measure the line regulation.

4.5.2 Load regulation

For testing the load regulation of the power supply unit (PSU), an electronically controlled load was developed. The resulting test setup is shown in figure 4.1.

The load element is the NPN transistor Q_L, a generic medium power device. To be able to measure the actual current load, a 1 Ω resistor, $R_{I\text{-}S}$, was connected in series with the load transistor.

As electric isolation between the controlling circuitry and the load is wanted, an optocoupler is used. A variable resistor, R_b, is inserted after the CNY17 optoisolator. The resistor controls the base current of Q_L, and thus the load.

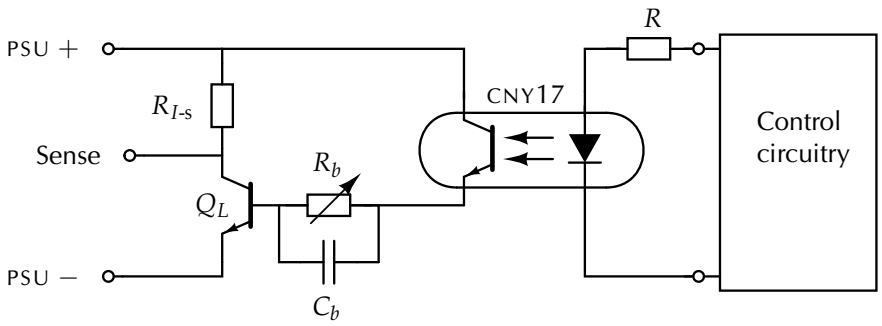


Figure 4.1: Test setup used when testing the load regulation of the power supply.

To decrease the switching time of Q_L, C_b was used to bypass R_b during switching transitions.

The switching signals were generated with a microcontroller programmed to switch with appropriate rates. A separate double insulated PSU was used to power the controller. This setup eliminates ground loops arising from the use of a grounded signal generator and oscilloscope.

A drawback of this configuration is the long switching time of the load. It is dominated by the time it takes to charge the base capacitance of Q_L. An attempt to vary the load by switching a relay instead of a transistor was made at first. But because of severe contact bouncing in the relay, the results were not reliable. Driving the load transistor directly from a signal generator without the optocoupler was troublesome due to the introduced ground loop.

In addition to the electronic load, each rail was preloaded with a dummy load resistor. The 3.3 V and 5 V lines were loaded with 330 Ω, while the ±15 V rails received a 680 Ω load.

4.5.3 Noise

The Audio Precision test bench was used to measure the noise spectrum of the PSU in the audio band. The power supply was operative in the system when measured so noise generated by the system should be observable.

Chapter 5

Results

Results from the tests described in chapter 4 are presented here. The order of presentation is the same as for the test chapter.

5.1 Dataconverter

5.1.1 Total harmonic distortion plus noise (THD+N)

The THD+N was calculated from the measurement shown in figure 5.1 using equation (2.13). From this, the THD+N was found to be

$$\text{THD+N} = 0.0011\ \%.$$

5.1.2 Signal to noise ratio (SNR)

The SNR was calculated from the measurement shown in figure 5.1 excluding the 1 kHz signal, resulting in

$$\text{SNR} = 102\ \text{dB}.$$

5.1.3 Spurious free dynamic range (SFDR)

The spurious free dynamic range (SFDR) is found from the measurements in figure 5.1 as the distance from 0 dB to the highest spur, which occurs at 2 kHz.

$$\text{SFDR} = 103\ \text{dB}.$$

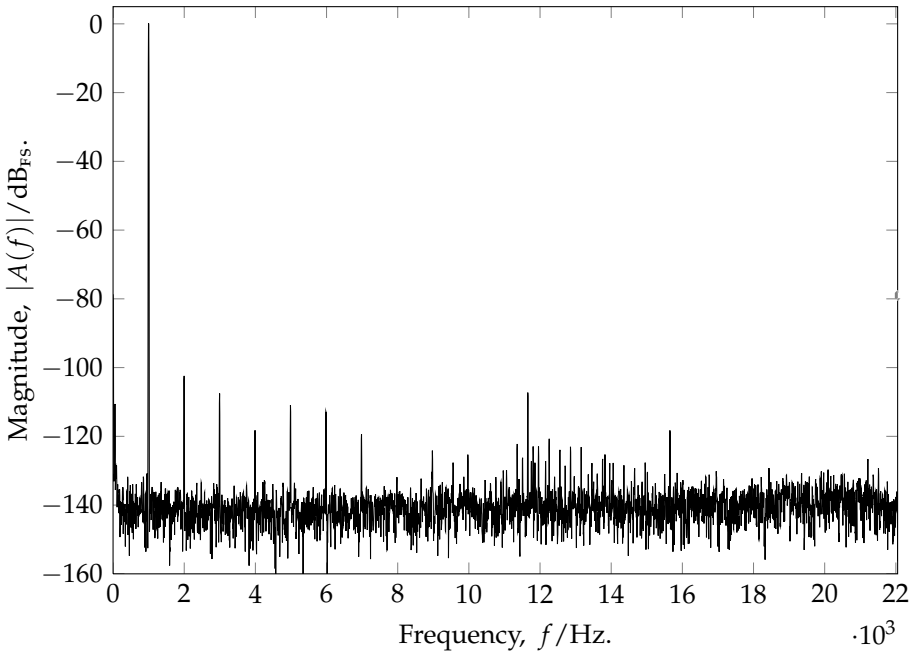


Figure 5.1: Frequency spectrum of output with a 1 kHz 0 dB$_{FS}$ sinusoid applied.

5.1.4 Dynamic range

The dynamic range was calculated from the data shown in figure 5.1 and 5.2.

$$\text{DR} = 105 \text{ dB}.$$

5.1.5 Frequency spectra

Frequency spectra from the left channel output with 0 dB$_{FS}$ and -60 dB$_{FS}$ sinusoidal input are given in figure 5.1 and 5.2 respectively. Figure 5.4 shows the noise on a unterminated input channel of the audio analyzer with 128 times averaging.

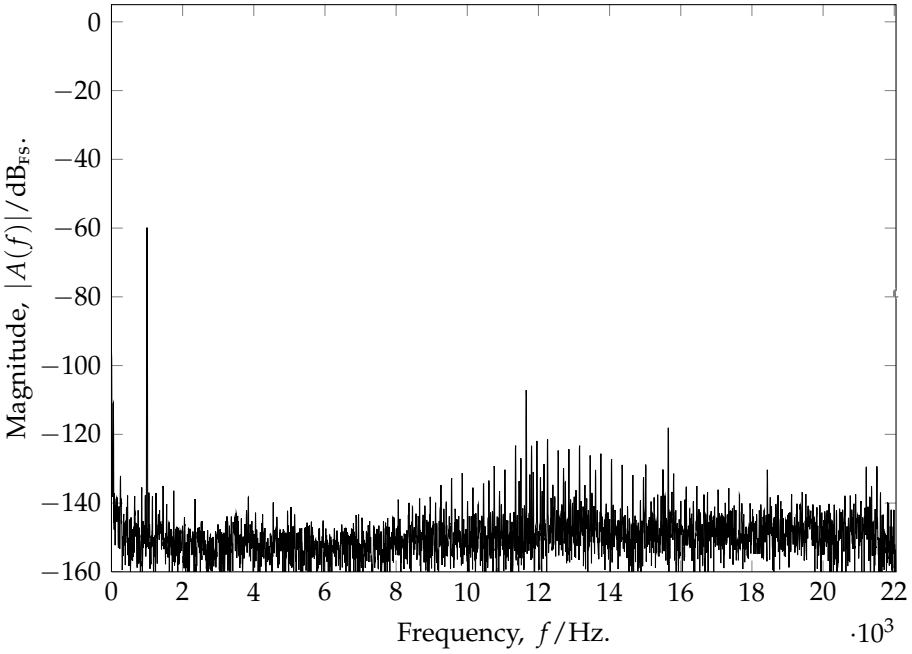


Figure 5.2: Frequency spectrum of output with a 1 kHz -60 $\mathrm{dB_{FS}}$ sinusoid applied.

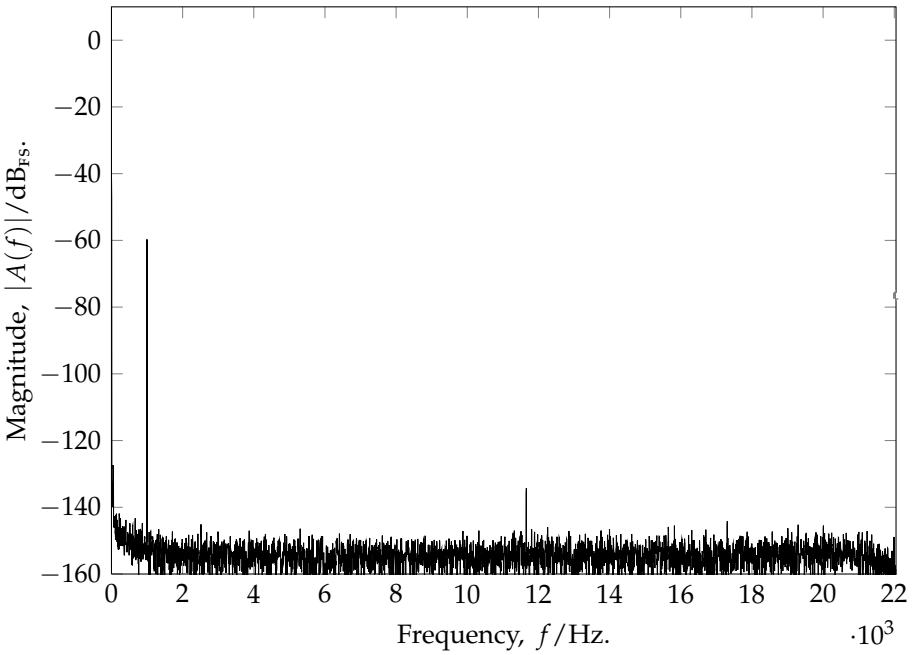


Figure 5.3: Frequency spectrum of output with a 1 kHz -60 $\mathrm{dB_{FS}}$ sinusoid applied. Battery based power supply.

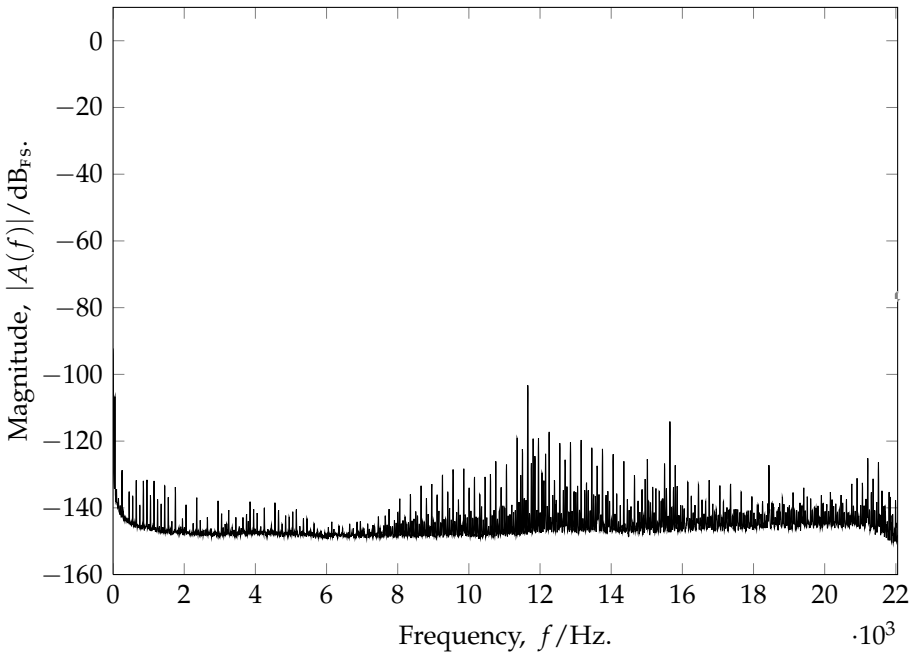


Figure 5.4: Noise spectrum with nothing connected to the analyzer, average of 128 spectra. Normalized with respect to audio full scale.

5.2 Clock generator

Clock jitter measurements were taken from the CDCE706 with $F_s = 44.1$ kHz and $F_{\text{sys}} = 384F_s = 16.9344$ MHz.

Table 5.1: Measured clock jitter from CDCE706 clock generator.

Clock line	Rise time, t_r/ns	Measurement	Clock jitter, Δt/ps	Standard deviation, σ/ps
F_s	0.6	RMS	77.4	1.7
	0.6	P–P	463.3	7.6
	3.3	RMS	323.1	5.2
	3.3	P–P	1940.7	46.1
F_{sys}	0.6	RMS	57.3	13.8
	0.6	P–P	366.7	100.3
	3.3	RMS	192.5	1.9
	3.3	P–P	1609	31.7

Clock signals from the S/PDIF receiver were obtained when playing a test CD. In accordance with the Red Book standard, this means $F_s = 44.1$ kHz. The system frequency was set to $F_{\text{sys}} = 256F_s = 11.2896$ MHz.

Table 5.2: Measured clock jitter from DIR9001 S/PDIF receiver.

Clock line	Measurement	Clock jitter, Δt/ps	Standard deviation, σ/ps
F_s	RMS	129	2.3
F_{sys}	RMS	96.88	1.13

5.2.1 Rise time

Results from adjustment of the clock generator rise and fall times are shown in this section. Figure 5.5 shows the system clock with maximum slew rate, while figure 5.6 shows the system clock configured to have 3 ns additional rise time. The same conditions are shown for the bit clock in figure 5.7 and figure 5.8 respectively.

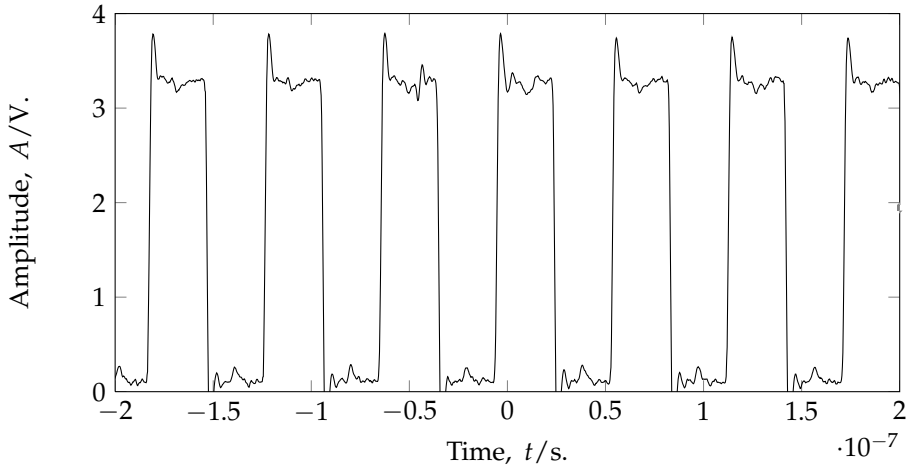


Figure 5.5: System clock with rise time $t_r \approx 0.6$ ns.

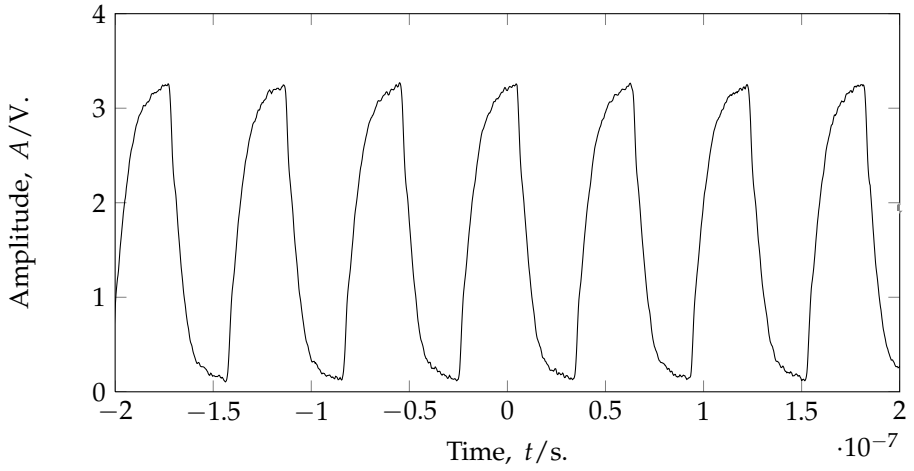


Figure 5.6: System clock with rise time $t_r \approx 3.3$ ns.

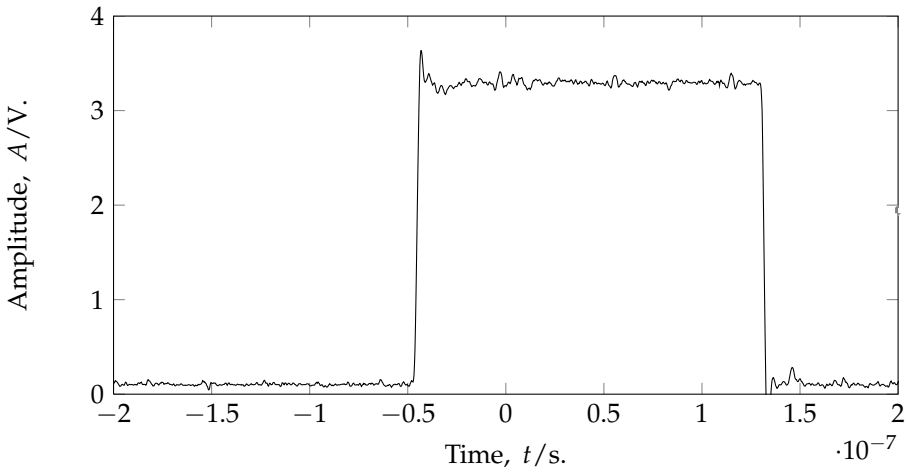


Figure 5.7: Bit clock with rise time $t_r \approx 0.6$ ns.

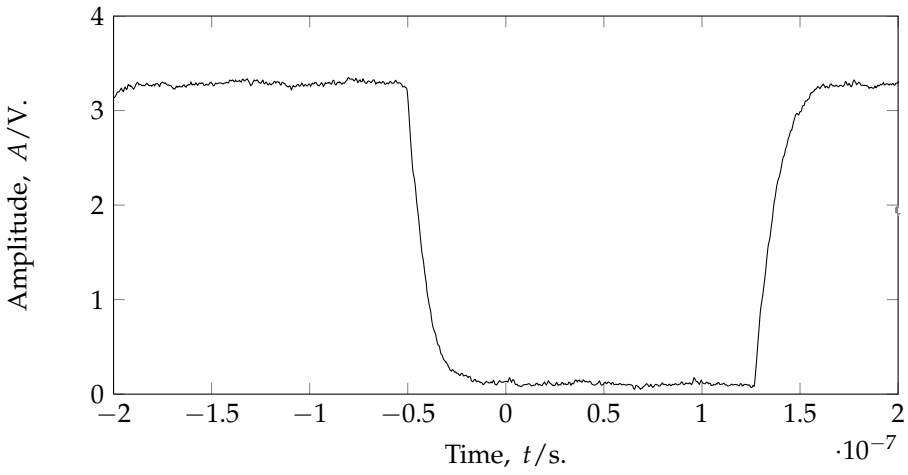


Figure 5.8: Bit clock with rise time $t_r \approx 3.3$ ns.

5.3 Reconstruction filter

Measurements of the frequency response of the reconstruction filter are presented in figure 5.9.

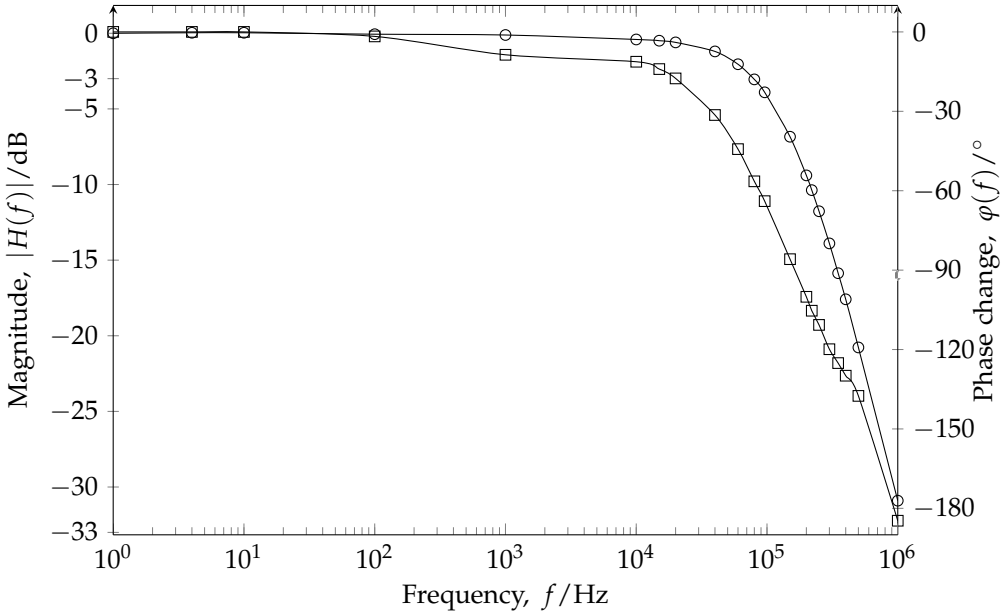


Figure 5.9: Measured frequency response of reconstruction filter. Magnitude drawn with circles, phase with squares.

5.4 Power supply

Figures 5.10 and 5.11 shows the impact of the series resistor in the rectifier filter of the PSU. The peak to peak ripple voltage was reduced by 62 % from 0.514 V to 0.195 V.

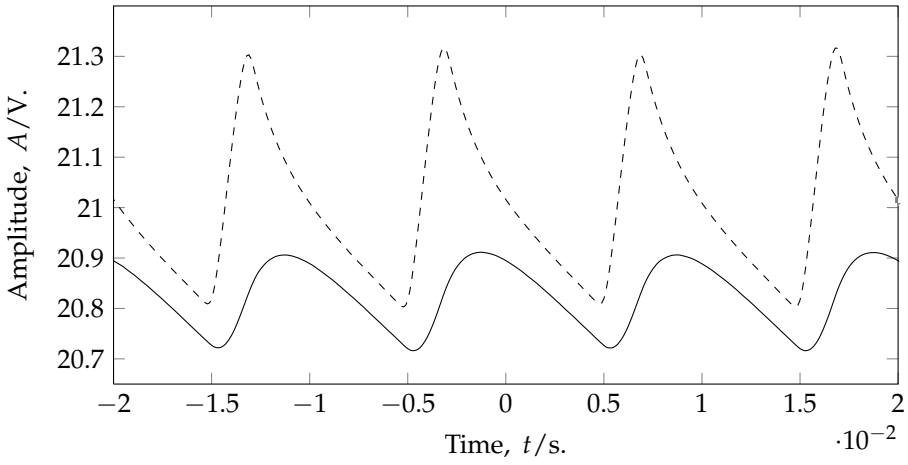


Figure 5.10: Effect of series resistor in rectifier filter for the 15 V rail. Time domain. Dashed line from rectifier. Solid line after resistor.

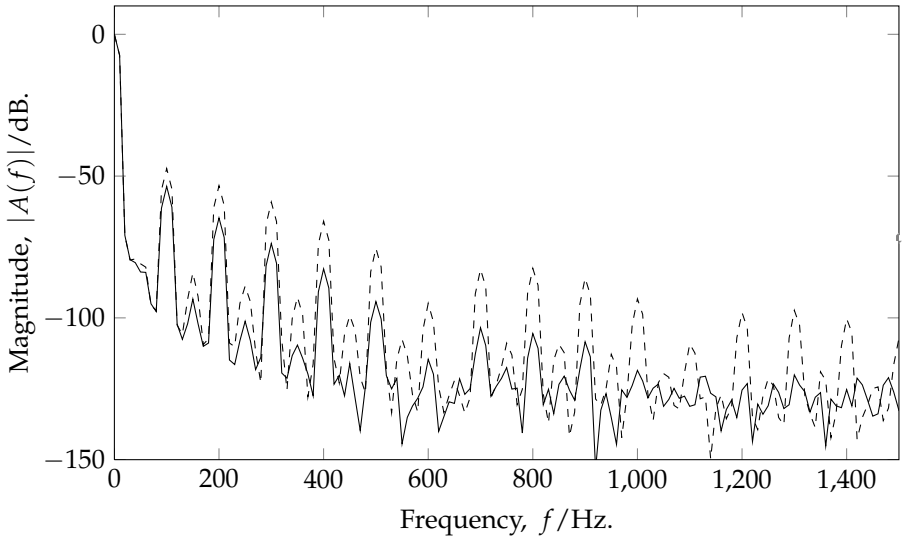
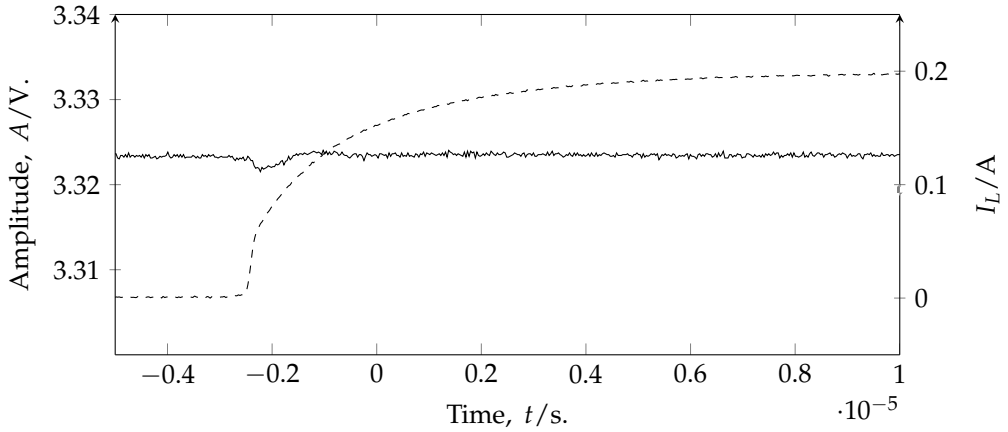


Figure 5.11: Effect of series resistor in rectifier filter for the 15 V rail. Frequency domain. Magnitude normalized with respect to DC. Dashed line from rectifier. Solid line after resistor.

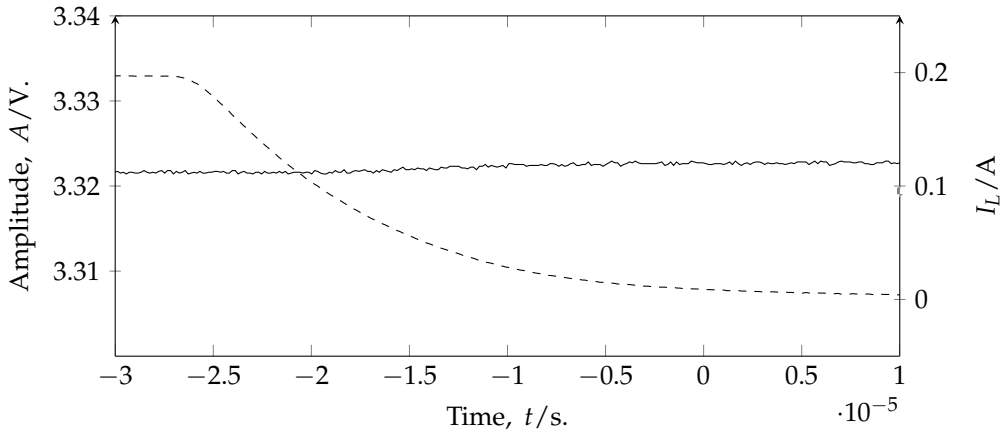
5.4.1 Signal to noise ratio (SNR)

The SNR was calculated from the measurement shown in figure 5.14, excluding the DC level, resulting in

$$\text{SNR} = 93 \text{ dB}.$$

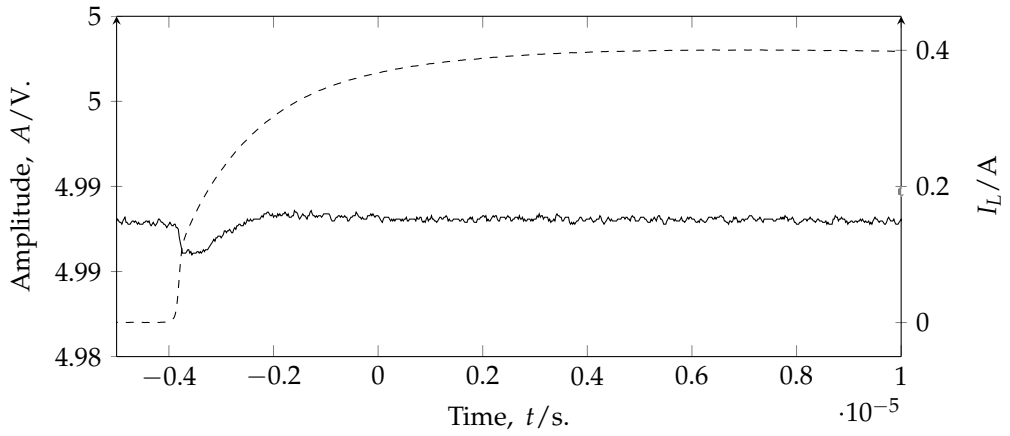


(a) Load on.

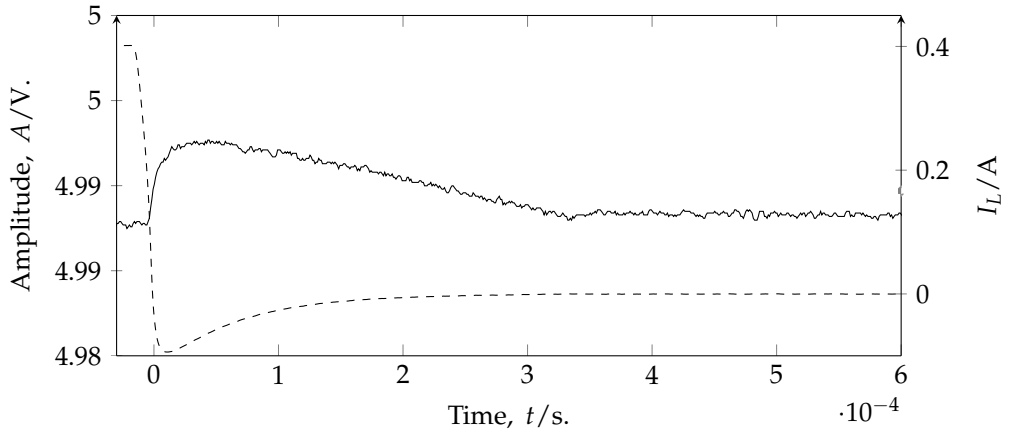


(b) Load off.

Figure 5.12: Load regulation on 3.3 V line. 200 mA load. Solid line regulated voltage. Dashed line load.



(a) Load on.



(b) Load off.

Figure 5.13: Load regulation on 5 V analog line. 400 mA load. Solid line regulated voltage. Dashed line load.

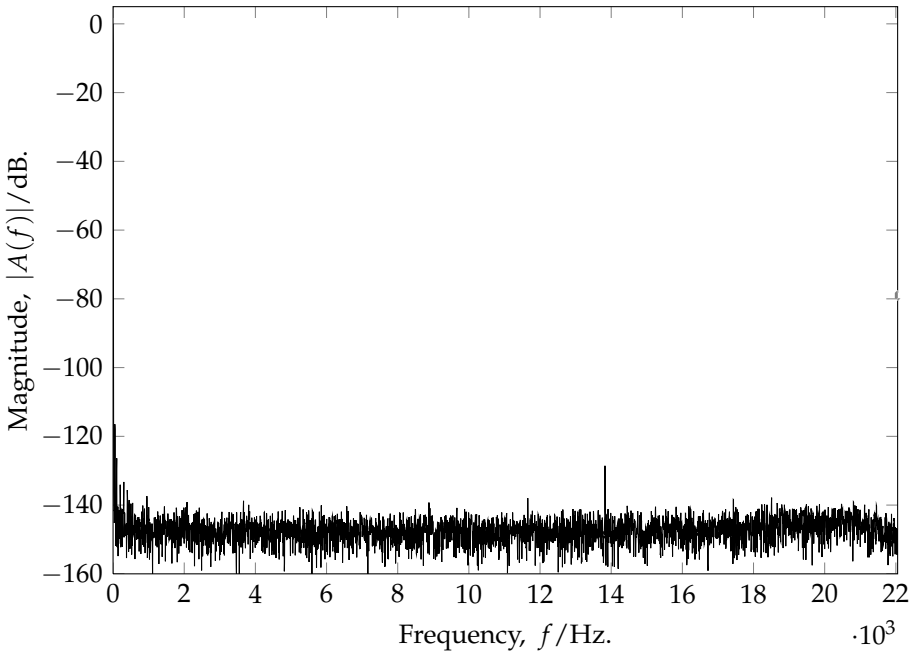


Figure 5.14: Frequency spectrum of 5 V analog PSU. Normalized with respect to DC.

Chapter 6

Discussion

6.1 System solution

A lot of different topics must be handled to make a complete audio system. Even though the design of a small piece of a system may seem trivial, the situation changes considerably when designing a whole system. The challenge does not necessarily lie in circuit calculations but more to find a suitable solution when considering architecture and components. In addition the performance requirements have to be fulfilled.

The implemented system supports all the required functionality. The measured performance is also good, surpassing the theoretical dynamic range achievable with CDs. The system is designed with the intention of becoming a commercialized product. Anyway, some improvements can be made, as discussed in the following sections.

6.1.1 USB functionality

The microcontroller was programmed to handle incoming audio data on the USB link, using the USB audio device class. When connected to a computer, the system is registered as a sound card, ready to receive audio data. A lot of additional functionality can be supported by the USB connection, but has not been implemented due to limited time.

The feedback functionality discussed in section 2.5.4 has not been implemented, although most of the firmware needed to support this are written. It is considered a necessity for proper audio playback, and the first thing that should be added.

Another issue is the support of different audio sampling rates. When

the system is connected to the host computer, it reports the supported sampling frequencies during enumeration. Presently only 44.1 kHz sampling frequency is supported in firmware. To support other frequencies, the system should reprogram the CDCE706 clock whenever another sampling frequency is requested. This is supported by the USB audio class, and can be implemented.

As the system contains a volume control, this should be synchronized with the host computer to allow for volume adjustments through the USB connection. This can be implemented as a USB HID, which is another device class supported by USB. In such way, the volume buttons in the system will be linked to the volume settings on the host computer. This implementation was considered to be outside the main objectives and not treated any further.

6.1.2 Button user interface

The system needed a user interface to control source selection and volume. For this purpose the circuit in figure 3.9 was made as a prototype. For further implementation, this interface is expected to contain remote control support and possibly a display. Several IO pins from the microcontroller are made available for this purpose at the connectors CN_5 and CN_6 shown in figure C.1.

6.2 Dataconverter and filter performance

The measured dataconverter performance presented in section 5.1. These results should be considered as absolutely worst case values. Comparing the frequency spectra in figures 5.1, 5.2 and 5.4 clearly shows that the measurements are contaminated by surrounding noise. This noise has not been removed when doing the calculations and no averaging has been used. Neither was the system shielded during the measurements.

Harmonic distortion

The harmonic distortion when applied a 0 dB_{FS} input signal is clearly seen in figure 5.1, giving an SFDR of 103 dB. Only the six first harmonics are prominent. This distortion occurs only for large input signals and was not observable when input a -20 dB_{FS} signal.

THD+N was calculated to equal 0.0011 % when no measurement noise was removed. This corresponds to -99 dB, which is beyond CD quality. No significant improvement is expected without changing the postfilter, but some system specific subjects may affect it to some degree. The ± 15 V power supplies feeding the opamps were not perfectly symmetrical, and differed by several hundred millivolts from the target voltages. Decoupling of the opamps was done by a single 100 nF capacitor close to each power pin, which

is considered appropriate.

A small DC offset can be observed on the frequency spectra, as no offset compensation has been performed. However, this can be adjusted by mounting the potentiometers VR_1 and VR_2, shown on the schematic in figures B.7 and B.8. These are connected to the offset compensating terminals of the I/V converter opamps.

6.2.1 Signal to noise ratio

The SNR was calculated from the case with a -60 dB_{FS}, 1 kHz input signal, while removing the fundamental in figure 5.2. Including the measurement noise, the SNR becomes 102 dB. Using equation (2.12) this gives an ENOB of 16.7 bit, which is 0.7 bit beyond the number achievable with CD. The typical SNR stated in the PCM1794A DAC datasheet yields an ENOB of 20.8 bit. It should be emphasised that this value is measured under more ideal circumstances and on an evaluation board targeted against maximum performance only.

Noise

The output noise level is centered around -140 dB when applied a 0 dB_{FS} input signal and around -150 dB when applied a -60 dB_{FS} input signal, referring to figures 5.1 and 5.2. From this, the noise level depends on the input signal. A large amount of noise is present from 8 kHz to 16 kHz, in addition to some noise around DC, most pronounced in figure 5.2. However, this is found to be noise from the surroundings and not from the system. This is confirmed by the results in figure 5.4, showing the noise from an unterminated input on the audio analyzer, when the system was disconnected from the mains supply. Ideally this measurement should have been performed with test leads connected to the system, unpowered, to serve as a calibration measurement. With unterminated input, this figure serves only as a evidence for surrounding noise at these frequencies.

The power supply was replaced by a battery power pack to see how this affected the output noise as shown in figure 5.3. Only a small spur at 11.6 kHz remained as noise from the surroundings. The surroundings noise is picked up by signal loop area in the system. When replacing the PSU with a battery, this area is significantly decreased, and less noise is picked up.

6.3 Clock

Table 5.1 lists the period jitter measurements from the CDCE706 clock generator. The output rise and fall time of the clock can be programmed to increase the slew rate with 3 ns from the nominal value that is 0.6 ns. According to

the discussion in section 2.2.3 a short risetime means higher frequency components, which can couple through to other parts of the system. The clock jitter for both fast and slow rise time was measured. The system clock RMS jitter increased from 57.3 ps to 192.5 ps when increasing the rise time. Due to extensive decoupling no clock noise was observed on the power supply. As the fast rise time gave best jitter performance without contaminanting the power supply, this would be the preferred setting.

Table 5.2 lists the periodic jitter measurements of the clocks recovered from the S/PDIF signal by the DIR9001 decoder. The system clock had a RMS jitter of 96.88 ps measured at the DAC input. From its datasheet, the DIR9001 S/PDIF decoder has a typical system clock jitter of 50 ps when the system clock frequency is 256 times the sampling clock. Maximum jitter is 100 ps (*DIR9001 96 kHz, 24 bit Digital Audio Interface Receiver*, 2006). The tri-state buffer in between this receiver and the DAC is expected to introduce extra jitter. As can be seen in figure B.9 this buffer has only one decoupling capacitor on the power supply. Its ground pin is connected directly to the ground plane. This in addition to that the circuit is placed close to the DIR9001 with digital circuitry may cause dirsturbance on the buffer power supply, giving rise to additional jitter. The DIR9001 circuit itself has a better power supply decoupling with two capacitors as shown in figure B.12. Overall, this clock jitter agrees well with the expectations.

All jitter measurements were taken with around 5 min averaging. Since the system was unscreened, it is probable that noise contaminated the peak to peak measurements.

6.4 Power supply

6.4.1 Prefilter resistor

From the plots in figures 5.10 and 5.11 in section 5.4 the benefit of the series resistor in the *CRC*-filter following the rectifier is visualized. The effect is very visible in the spectral plot, where the reduction in harmonic content is prominent.

The resistor will introduce an extra voltage drop, in addition to its dissipated power. But because this is a linear regulator, the total dissipated power is independent of this resistor for a given load. The voltage drop, however, means that the raw voltage necessary for the regulator to function properly increases. This will in turn increase the lowest obtainable power loss through the regulator.

For this system the raw voltage is determined by the mains transformer, and is not easily controlled. The use of the resistor will have no ill effects here, and the prefilter gain is beneficial for the power supply as a whole.

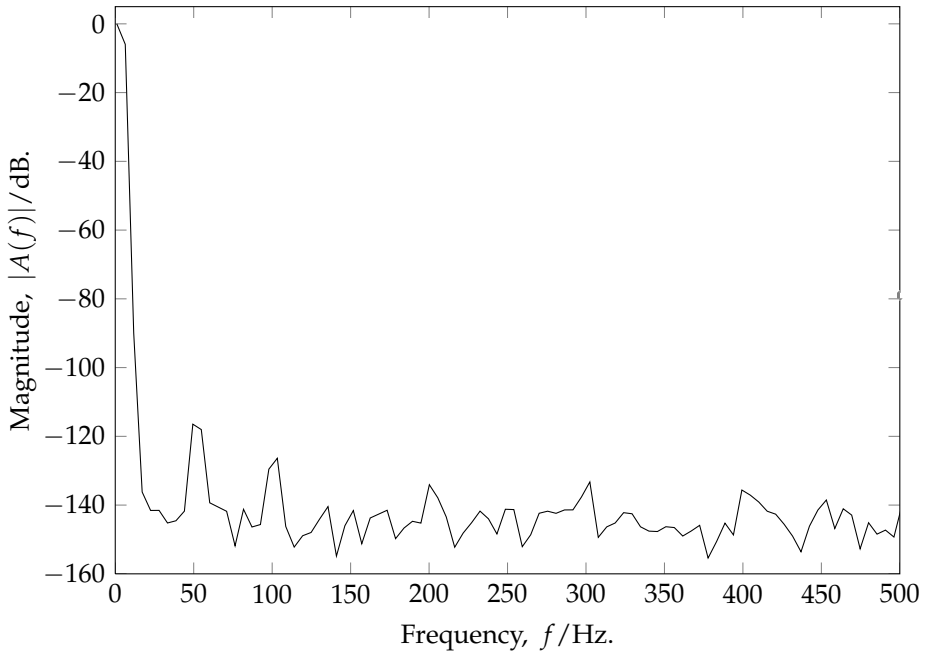


Figure 6.1: Zoomed frequency spectrum of 5 V analog PSU. Original plot in figure 5.14. Normalized with respect to DC.

6.4.2 Line regulation

A magnified portion of figure 5.14 is shown in figure 6.1. From this spectral plot of the 5 V analog regulator it is seen that the fundamental frequency of the rectified mains voltage, 100 Hz, is damped to more than 125 dB below the DC level.

In contrast, the 50 Hz line frequency lies at -115 dB. This indicates that the regulator itself is better at ripple rejection than the system's immunity against mains hum induction.

6.4.3 Load regulation

In figure 5.12 the load change response of the 3.3 V regulator is plotted. When the 200 mA load is turned on, the output voltage is regulated back to the starting voltage in 0.5 µs. This is a very decent performance compared to that of comparable regulators. The REG1117, used on the digital control board, needs ∼25 µs to settle when subjected to a 0.75 A load (*REG1117(A) 800 mA and 1 A Low Dropout Positive Regulator*, 2004).

At voltages as low as 3.3 V, the electronic load cannot turn off quickly enough to give any meaningful measurements.

The load responses of the 5 V analog regulator are shown in figure 5.13.

Regulation is excellent when the load turns on, stabilizing within 2 µs. When the load turns off, however, the regulator requires 300 µs to settle. The settling slope appears very linear, and could be mistaken for a slewrate related problem. But if the curve is extended down to zero volts, it will correlate nicely with the time constant of the regulated node. This time constant is formed by the filter capacitor C_{filt} of figure 3.11 and the dummy load resistor parallelled with the sense resistors:

$$\begin{aligned} \tau \approx & C_{\text{filt}} \left(R_{L\text{-d}} || (R_4 + R_5) \right) \\ \approx & 283 \text{ ms} . \end{aligned} \tag{6.1}$$

The linear portion of the settling response has a slope of ~ -16.7 V/s, which corresponds to a time constant of 300 ms. This is well within the ± 20 % tolerance limits of C_{filt}.

The dummy load is the only significant drainage path for C_{filt} when the electronic load disconnects, and is thus the only way to lower the output voltage of the regulator. A smaller filter capacitor will reduce the time constant and the settling time.

It should be mentioned that this test is not very realistic in terms of the current loading scenarios the power supply will undergo. The minimum load will be higher than the 15 mA drawn by the 330 Ω dummy load resistor. Only during certain volume adjustments in the attenuator, current changes will begin to near the orders in this test. During such changes, there will be audible effects on the sound, so that any distortion introduced by the power supply is masked and thus insignificant.

6.5 Printed circuit board layout

As shown in figure 3.19, three printed circuit boards have been made allowing for a modular design. The boards are interconnected through headers so that they can easily be put together. An advantage of this is that each board can be tested separately, and a system upgrade does not necessarily mean that the whole system has to be replaced. Unfortunately this makes the system more distributed, resulting in longer PCB traces. The headers also contribute considerably to the overall system cost. A final revision should therefore be designed onto a single PCB. This would also ease the assembly.

6.5.1 Power supply

As discussed in section 3.8 the feedback topology used in the power supply is prone to oscillations if insufficient phase margin is present. As seen in figure C.14 especially the supply and sense traces from the 15 V regulator are quite long. Both exceed 10 cm and have a parasitic inductance larger than

60 nH. When inserting these values into the simulation, some oscillation occurs. Placing the power supplies closer to the target circuits, preferably on the same PCB, could have mitigated this effect. Also using dedicated power planes would have reduced the parasitic inductance.

All the components in the power supply, except for the operational amplifiers, are hole mounted. A lot of area could have been saved if surface mounted devices had been used. Also, using the PCB as heatsink for the pass transistors would have saved both assembly time and money. Performance is expected to increase by using surface mounted decoupling capacitors, eliminating the large lead inductance in hole mounted capacitors.

6.5.2 DAC module

In mute mode, a large amount of noise was picked up from the surroundings, although the output was grounded by a relay located close to the output. Examining the PCB layout showed the cause. Figure 6.2 displays a section of the analog module PCB. The right channel analog output is encircled in the upper right corner, where its ground pin is directly tied to the ground plane. The upper most circle down to the right encircles the point where the positive output terminal is grounded during mute. Due to the eight traces from the shift registers controlling the relays, a large slot is made in the ground plane. This makes a large ground loop around this area which is more than 20 cm long. Despite the fact that this effect is most prominent during mute, it also concerns the normal operation. The lowermost circle shows a point where some of the signal is shunted to ground by the attenuator. Similarly, this is quite distant to the output. In the left channel these distances are a bit shorter, making it less prone to surrounding noise.

As only two copper layers were used for carrying both signal and power, this effect would to some extent be unavoidable. A simple solution would be to use hole mounted wires which could serve as an additional copper layer, to keep the ground plane more intact. Preferably, separate copper layers for power and ground should be used.

The use of separate ground planes for the digital and analog part of this board as shown in figure C.10 seemed to be a success. No digital noise was observed on the analog signals.

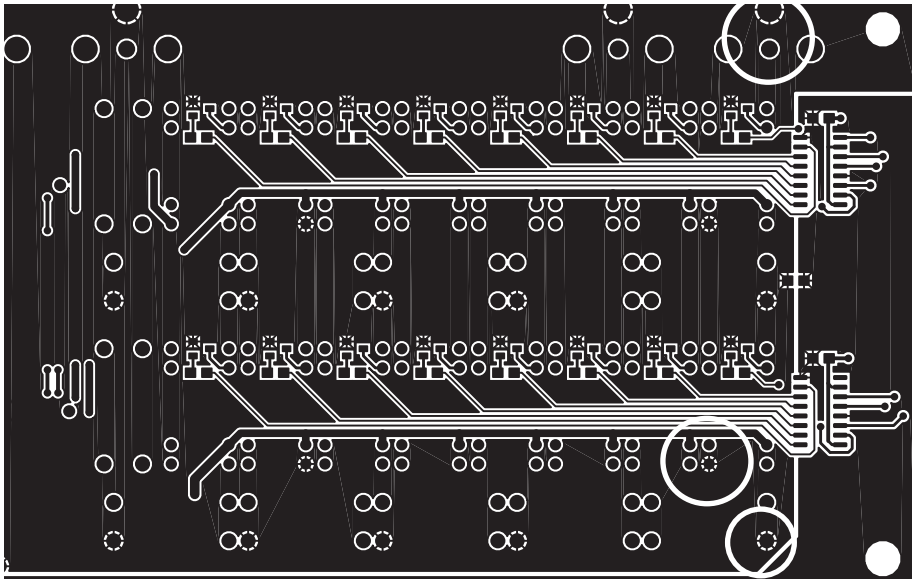


Figure 6.2: Section of the analog PCB, copper bottom.

Chapter 7

Conclusions

A high performance audio soundcard has been developed and assembled. The focus has been to develop a system with hardware that fulfilled the requirements stated in the problem description. Subjects regarding the program code has been given lower priority as this can easily be added later on. There was not enough time to handle all topics in detail. The system that is made offers a complete hardware solution with the neccesary firmware to demonstrate its capabilities.

Measurements showed that the system had a dynamic range of 105 dB. As this was calculated from measurements without removing the measurement noise, the actual value is expected to be even better. This high performance is a result of proper circuit design as a whole. It is not sufficient to buy an excellent DAC if the surrounding circuitry does not perform accordingly. A separate power supply for each voltage resulted in an excellent division between the analog and digital circuitries. The 5 V analog PSU delivered an SNR performance of 93 dB. Inductance in PCB trances due to the large extension could have been avoided by using more densely placed surface mounted components.

Even though this system has high performance, it will only be a single part of the complete audio system. To acheive high quality sound, the power amplifier, speakers and interconnections have to be of equal capabilities.

Further work

Small changes can be made to complete the system and possibly improve the performance further.

First of all the firmware should be updated to provide USB sampling rate feedback. In addition, synchronizing the volume control over USB would be

desireable.

The button user interface should be designed properly, not only as a prototype. Support for an infrared remote control or a similar device should be added.

To reduce the overall system cost, an attempt to reduce the component cost should be performed. Components may be of unnessesarily high specifications. The system should be tested further to see if some components are superfluous and could be left out.

The three PCBs should be merged into a single board to ease assembly and reduce total system cost. The problem with long traces in the power supply and the large loop area at the volume control should be fixed as discussed in section 6.5.

Appendices

Appendix A

Source code

Program code developed during the work on the thesis is presented here.

A.1 Resistor value calculation

Listing A.1: Octave program for calculation of resistor values.

```
function [r zout] = r2r_val (Rout, nstep)

  %% usage:  r = r2r_val (Rout, nstep)
  %%
  %%
  r = zeros(3, nstep); % Initialize resistor matrix.
  req = zeros(1, nstep); % Vector with (temporary) equivalent resistors.

  for i=2:nstep
    steps(i) = 2^(i-1);
  end
  steps(1)=1;

  % The first attenutaion step have a different topology.
  % We want -1 dB.

  r(1, 1) = Rout*10^(steps(1)/20);
  r(2, 1) = r(1, 1) / (10^(steps(1)/20) - 1);

  % The eq. res. from the first step is r1||r2.
  req(1) = r(1, 1)*r(2, 1) / (r(1, 1) + r(2, 1));
  r(3, 1) = req(1);

  for i=2:1:nstep
    % Required equivalent resistance for this step.
    req(i) = Rout*10^(steps(i)/20);
  % Value of shunt resistor.
    r(2, i) = req(i) / (10^(steps(i)/20) - 1);
```

```
29    % Value of series resistor. This steps req. res. minus previous steps eq.
          res.
30      r(1, i) = req(i) - r(3, 1);
31    end
32
33    % Now calculate the output impedance for each code.
34    codes = 0:(2^nstep - 1);
35
36    vout = ones(1,2^nstep);
37    for i=codes
38      znet = zeros(2, 6);
39
40      for j=1:nstep
41        if (bitget(i, j) == 1)
42        % Resistor pair j connected.
43          znet(1, j) = r(1, j);
44          znet(2, j) = r(2, j);
45        else
46          % Resistor pair j not connected.
47          znet(1, j) = 0;
48          znet(2, j) = 1e30;
49        end
50      end
51
52    % Calculate temp. eq. impedances.
53      zeq(1) = r(2,1)*r(1,1) / (r(2,1) + r(1,1));
54      for k=2:1:nstep
55        zeq(k) = znet(2,k)*(znet(1,k) + zeq(k-1)) / (znet(2,k) + (znet(1,k) +
              zeq(k-1)));
56      end
57      zout(i+1) = zeq(nstep);
58    end
59  end
```

Listing A.1: Octave program for calculation of resistor values.

A.2 Fourier coefficient calculation

Listing A.2: Octave program for calculation of Fourier coefficients of trapezoidal and square waves.

```
% Fourier plots
clear all;

% Number of fourier coefficients
N = 7;

% Risetime 0 < tr <0.5
% tr = 0.5 gives triangular wave
tr = 0.1;

%Range, do not change
x = -pi:0.01:pi;

% Initialize variables
trapeze = zeros(1, length(x));
trapeze_ser = zeros(1,length(x));
square = zeros(1, length(x));
square_ser = zeros(1, length(x));
coeff_tr = zeros(1,N);
coeff_sq = zeros(1,N);

% Generate sine wave
sine = sin(x);

% Generate trapeze wave
pts = length(x);
t = tr*2*pi;
trapeze(1, 1:0.5*tr*pts) = -1 + (2/t) * ((t/2)-pi-x(1:0.5*tr*pts));
trapeze(1, 0.5*tr*pts:pts*(0.5-0.5*tr)) = -1;
trapeze(1, pts*(0.5-0.5*tr):pts*(0.5+0.5*tr)) = (2/t)*x(1, pts*(0.5-0.5*tr):
    pts*(0.5+0.5*tr));
trapeze(1, pts*(0.5+0.5*tr):pts*(1-0.5*tr)) = 1;
trapeze(1, pts*(1-0.5*tr):pts) = 1 + (2/t)*(pi-(t/2)-x(pts*(1-0.5*tr):pts));

% Generate square wave
square(1, 2:length(x)/2) = -1;
square(1,length(x)/2+1:length(x)-1) = 1;

%Find fourier coefficients and superimpose the harmonics into the fourier
%series
for n = 1:N
    % Fourier coefficients of trapezoidal waveform
    coeff_tr(1,n) = (2*(-2*sin(n*pi)+2*sin(n*pi)*cos((1/2)*t*n)-2*cos(n*pi)*
        sin((1/2)*t*n)+t*n*cos(n*pi)*cos((1/2)*t*n)+t*n*sin(n*pi)*sin((1/2)*
        t*n)))/(pi*n^2*t)-(2*(-2*sin((1/2)*t*n)+cos((1/2)*t*n)*n*t))/(pi*n
        ^2*t)+(2*(-cos((1/2)*n*(2*pi-t))+cos((1/2)*t*n)))/(pi*n);
    % Trapezoidal waveform series
    trapeze_ser(1,:) = trapeze_ser(1,:) + coeff_tr(1,n)*sin(n.*x);
    % Fourier coefficients of square waveform
    coeff_sq(1,n) = (2/(n*pi))*(1-cos(n*pi));
    % Square waveform series
    square_ser(1,:) = square_ser(1,:) + coeff_sq(1,n)*sin(n.*x);
end

% Plot figures
figure();
```

```
53 box on;
54 hold on;
55 plot(x,trapeze(1,:), 'Linestyle', ':','Color',[0 0 0]);
56 plot(x,trapeze_ser(1,:),'Color',[0 0 0]);
57 title(['Trapezoidal waveform with ' num2str(N) ' harmonics, risetime = '
       num2str(tr) ' period.']);
58 ylabel('f(x)');
59 xlabel('x');
60
61 figure();
62 box on;
63 hold on;
64 plot(x,square(1,:), 'Linestyle', ':', 'Color',[0 0 0]);
65 plot(x,square_ser(1,:),'Color',[0 0 0]);
66 title(['Square waveform with ' num2str(N) ' harmonics.']);
67 ylabel('g(x)');
68 xlabel('x');
69
70 figure();
71 box on;
72 stem(coeff_tr(1:N),'Color',[0 0 0]);
73 xlim([0.5 N]);
74 ylim([0 1.41]);
75 title([num2str(N) ' first Fourier coefficients of the trapezoidal waveform'
       ]);
76 ylabel('Magnitude');
77 xlabel('Fourier coefficient number');
78
79 figure();
80 box on;
81 stem(coeff_sq(1:N),'Color',[0 0 0]);
82 xlim([0.5 N]);
83 title([num2str(N) ' first Fourier coefficients of the square waveform']);
84 ylabel('Magnitude');
85 xlabel('Fourier coefficient number');
```

Listing A.2: Octave program for calculation of Fourier coefficients of trapezoidal and square waves.

Appendix B

Schematics

B.1 Digital control unit

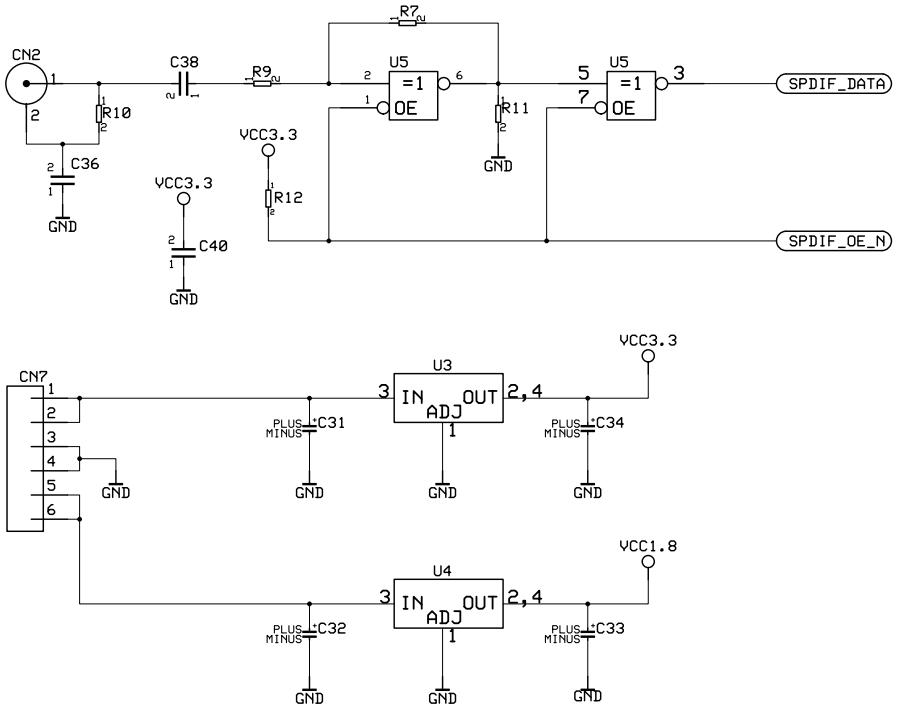


Figure B.1: S/PDIF buffer circuitry (top) and digital power supply linear regulators (bottom).

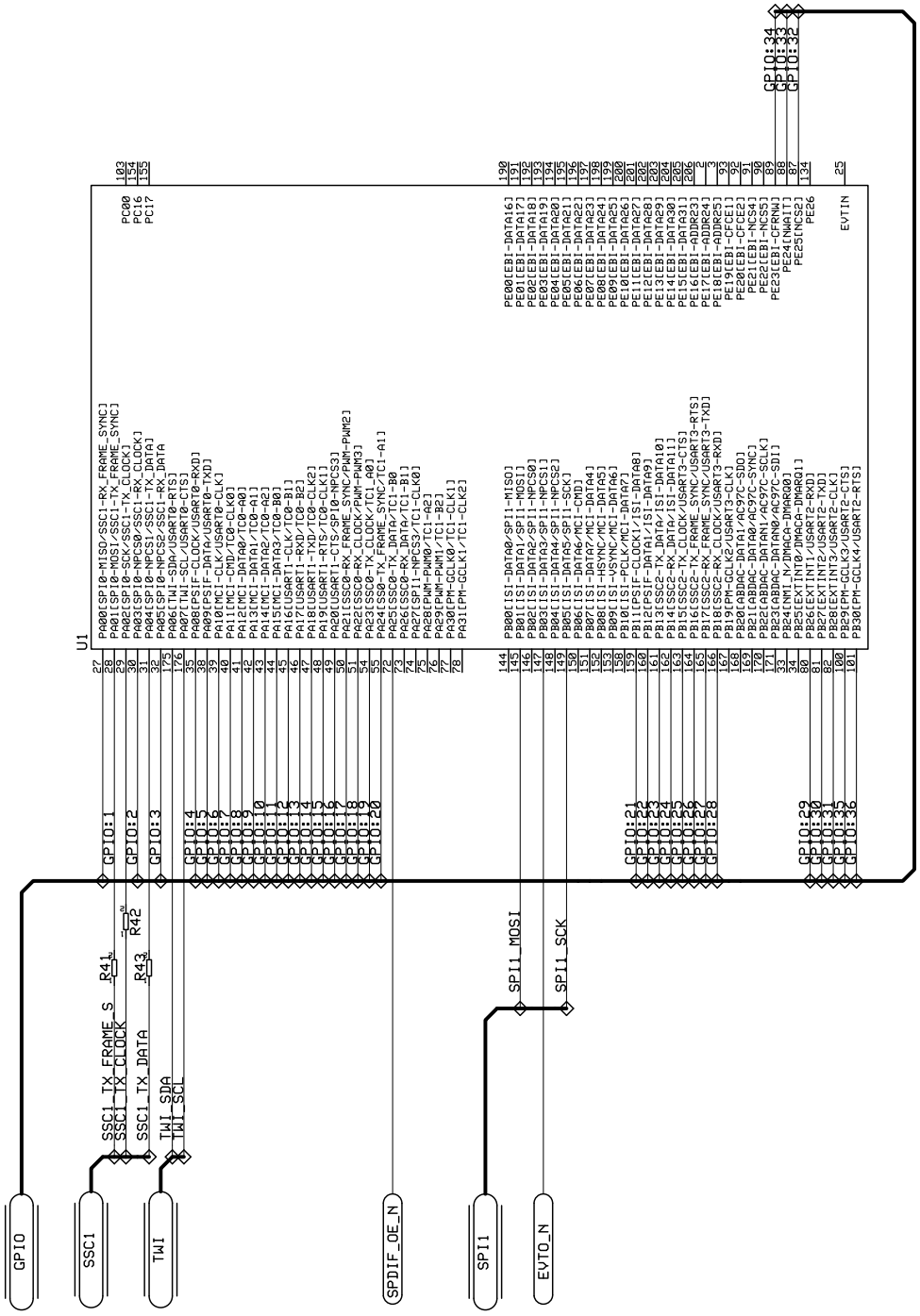


Figure B.2: Microcontroller part 1.

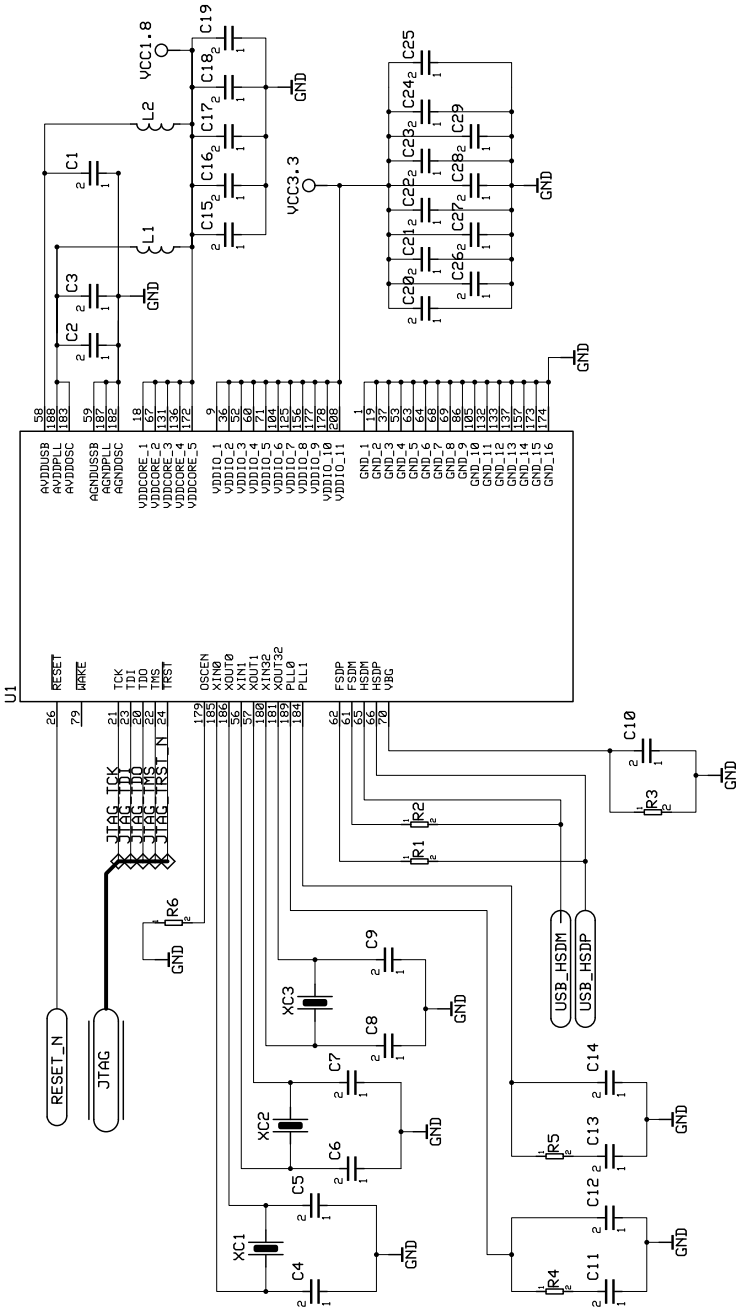


Figure B.3: Microcontroller part 2.

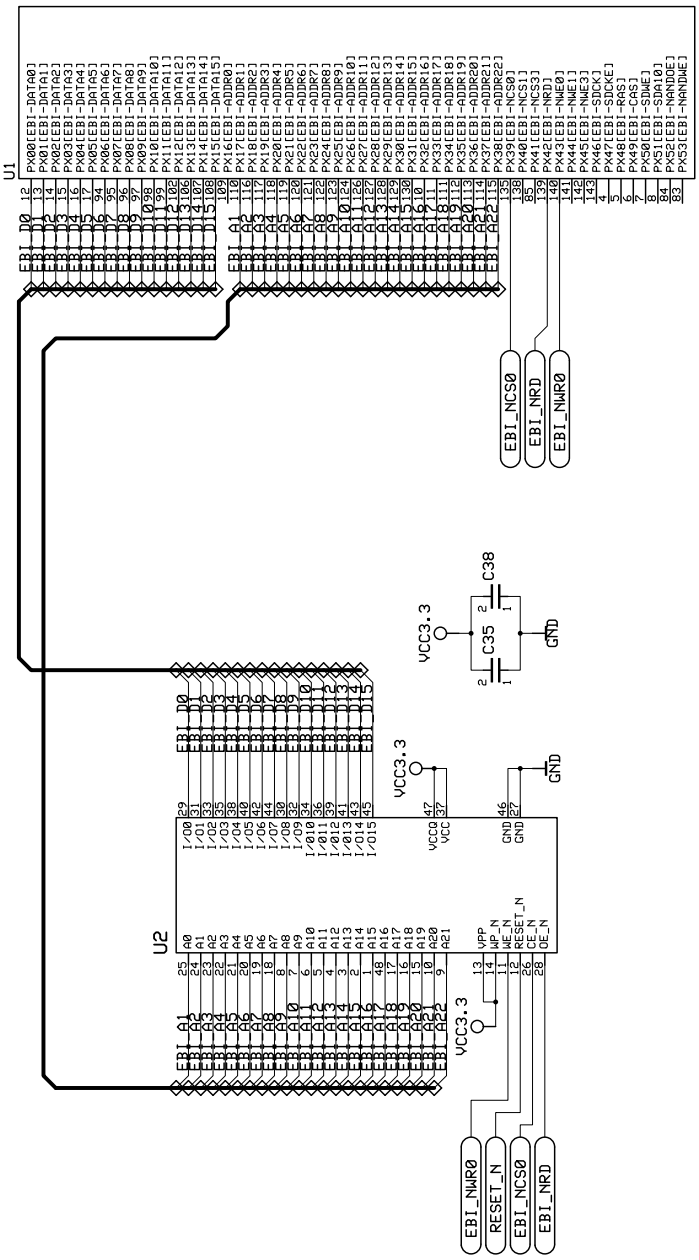


Figure B.4: Flash memory for microcontroller.

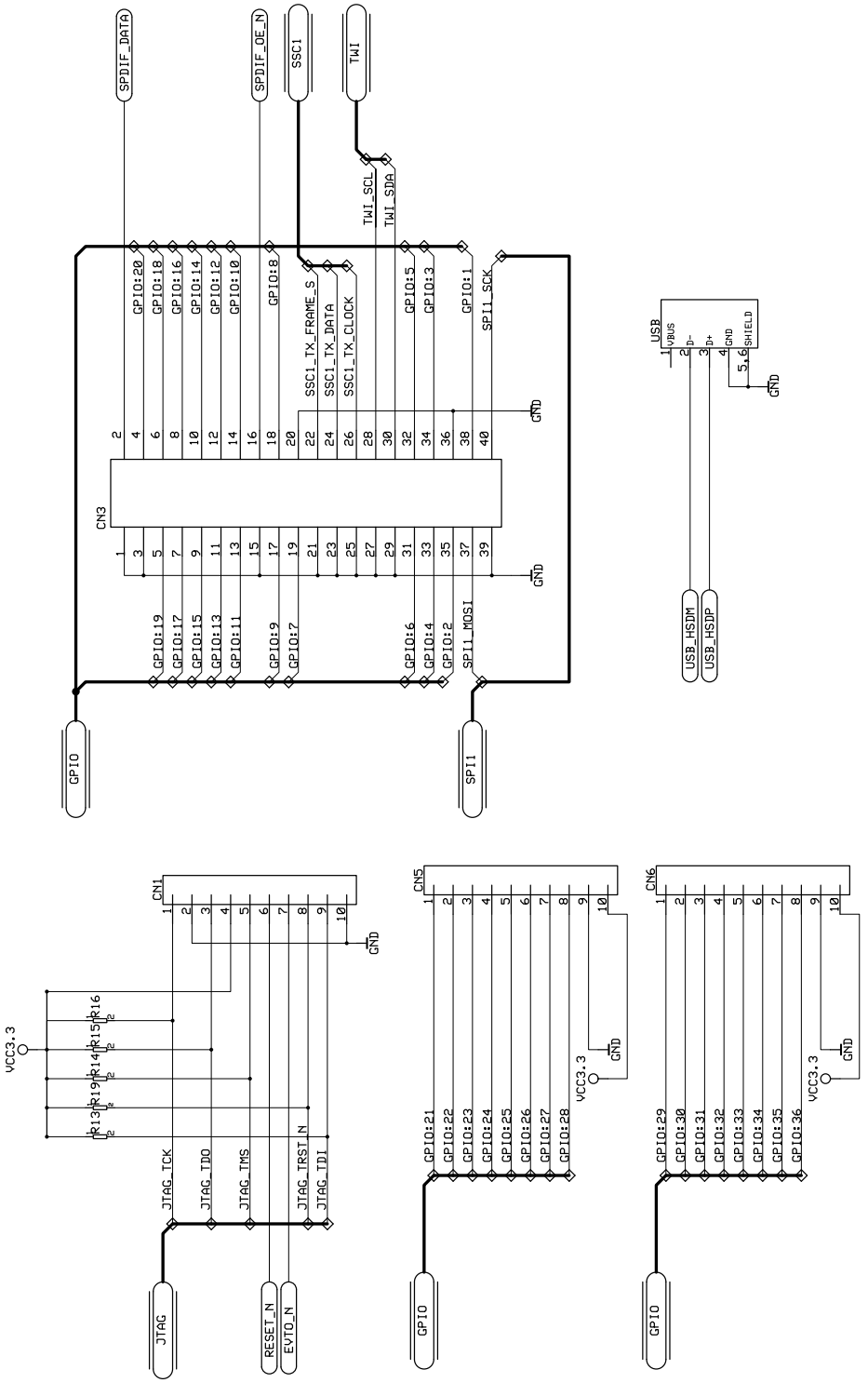


Figure B.5: Interconnects.

B.2 DAC unit

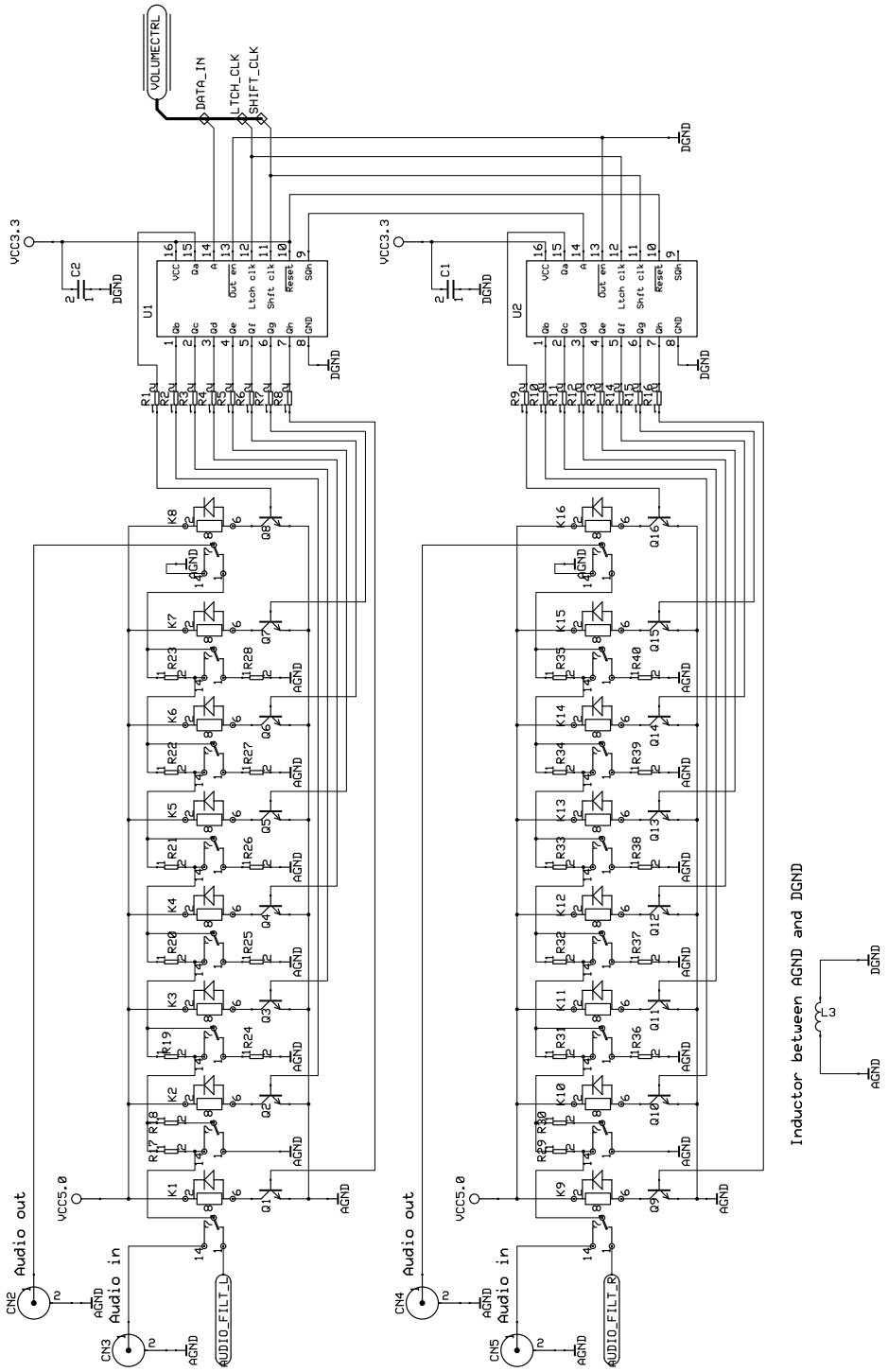


Figure B.6: Stepped attenuator.

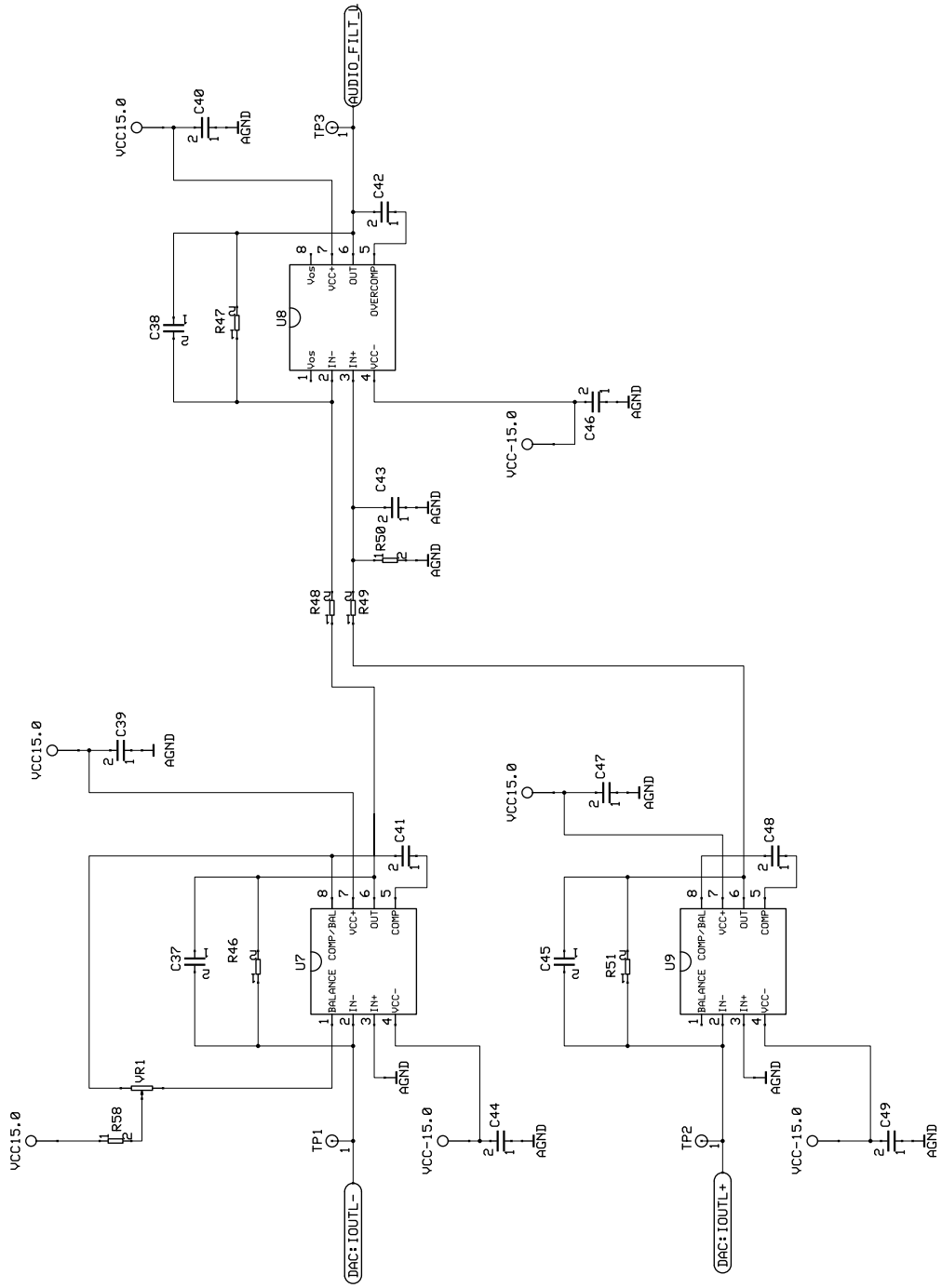


Figure B.7: Reconstruction filter, left channel.

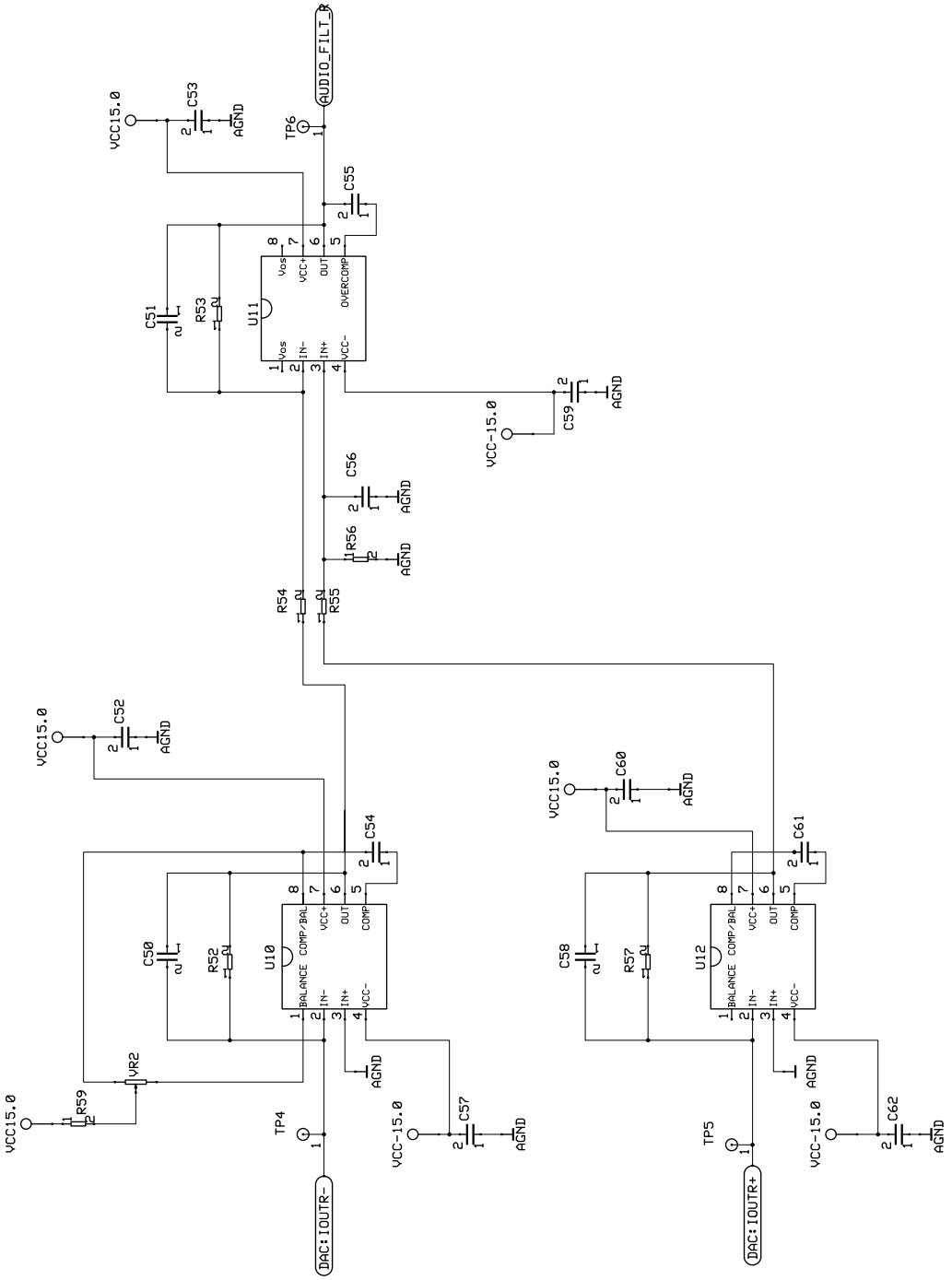


Figure B.8: Reconstruction filter, right channel.

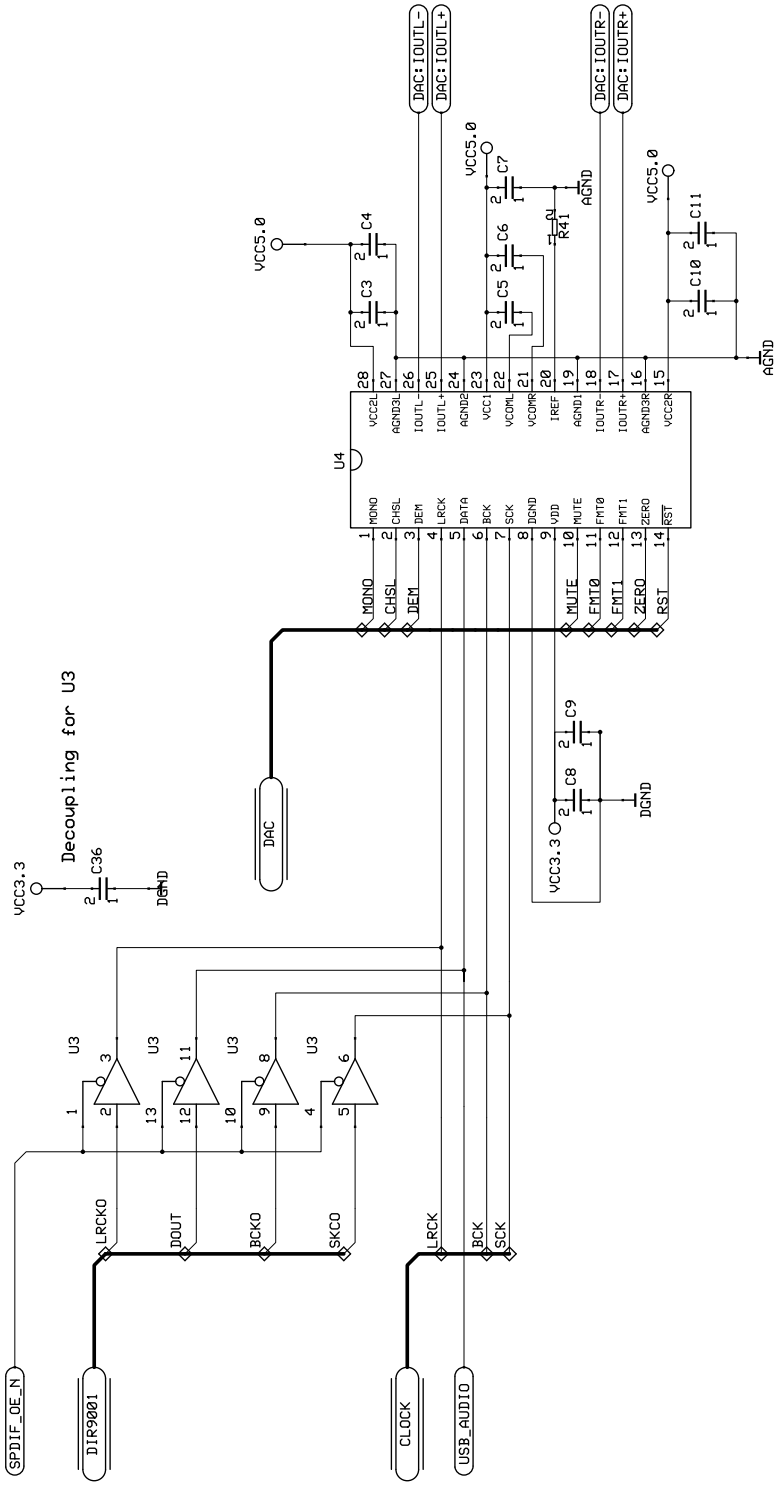


Figure B.9: DAC.

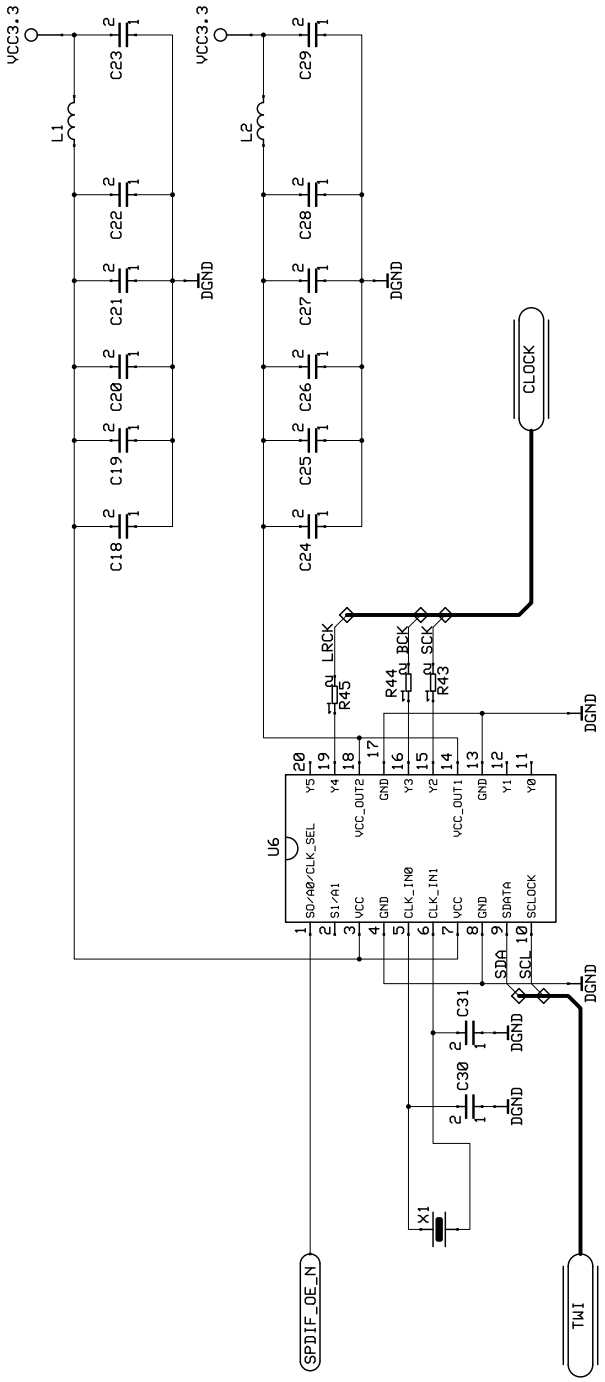


Figure B.10: Clock generator.

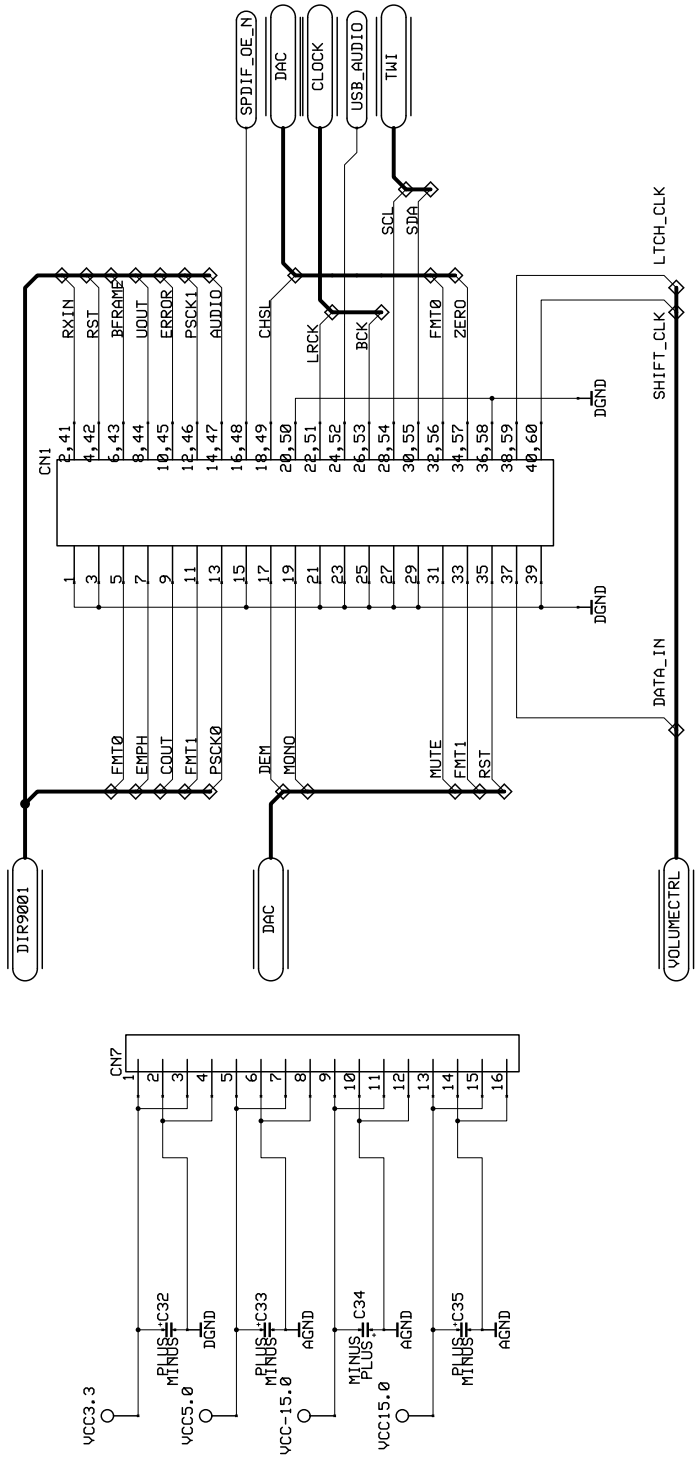


Figure B.11: Interconnect.

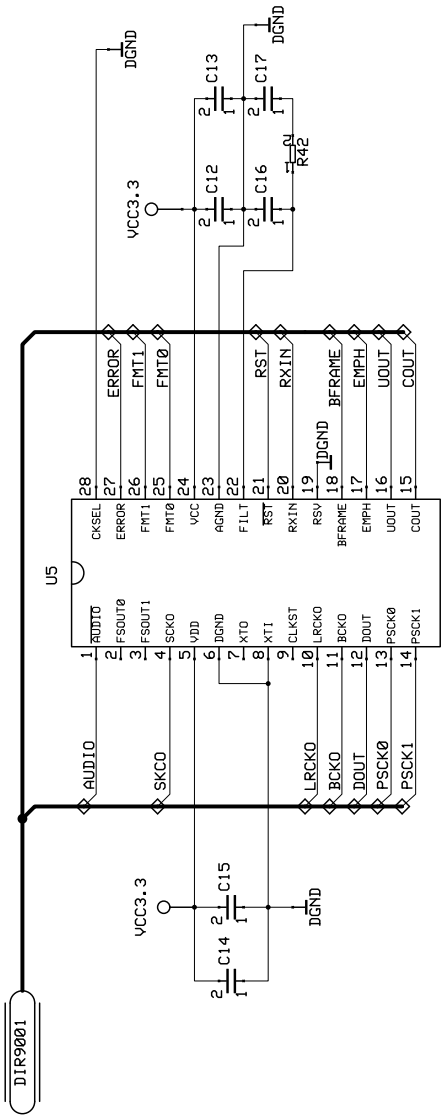


Figure B.12: S/PDIF receiver.

B.3 Power supply unit

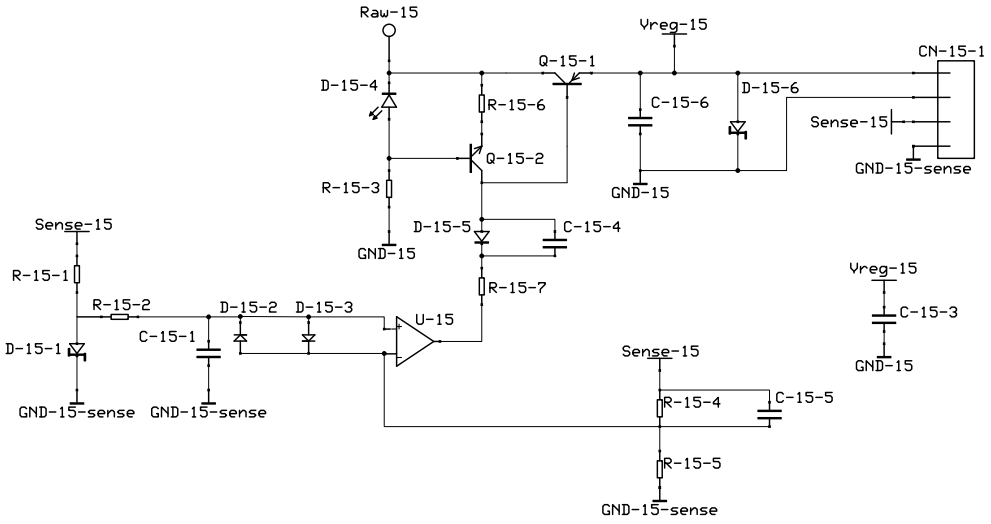


Figure B.13: Negative 15 V power supply.

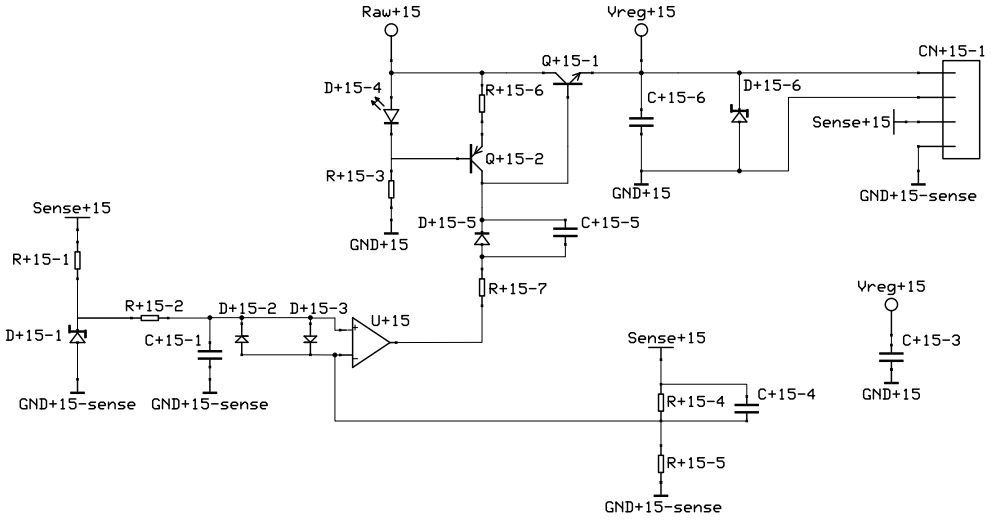


Figure B.14: Positive 15 V power supply.

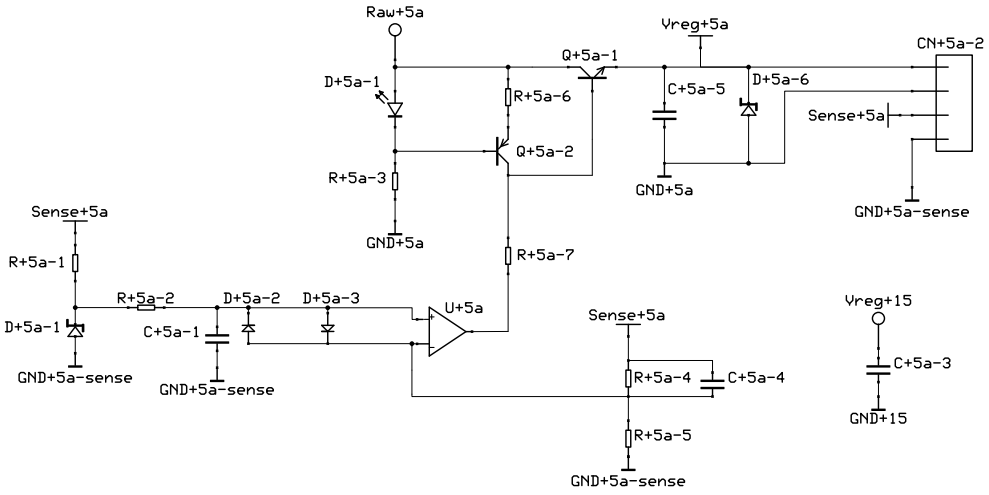


Figure B.15: 5 V analog power supply.

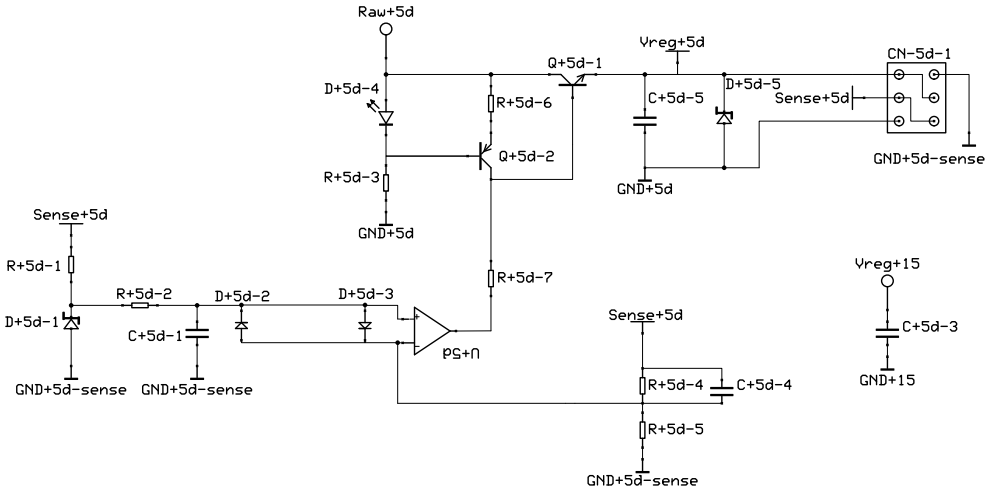


Figure B.16: 5 V digital power supply.

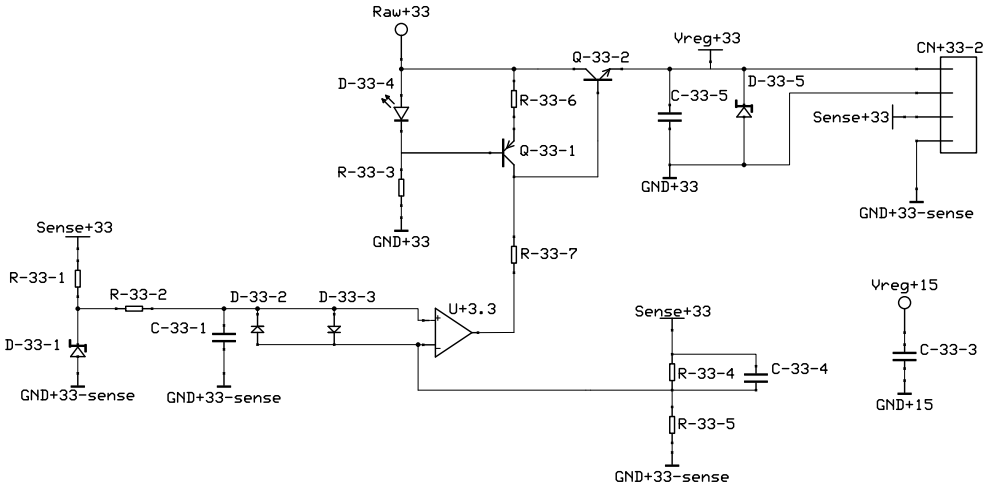


Figure B.17: 3.3 V power supply.

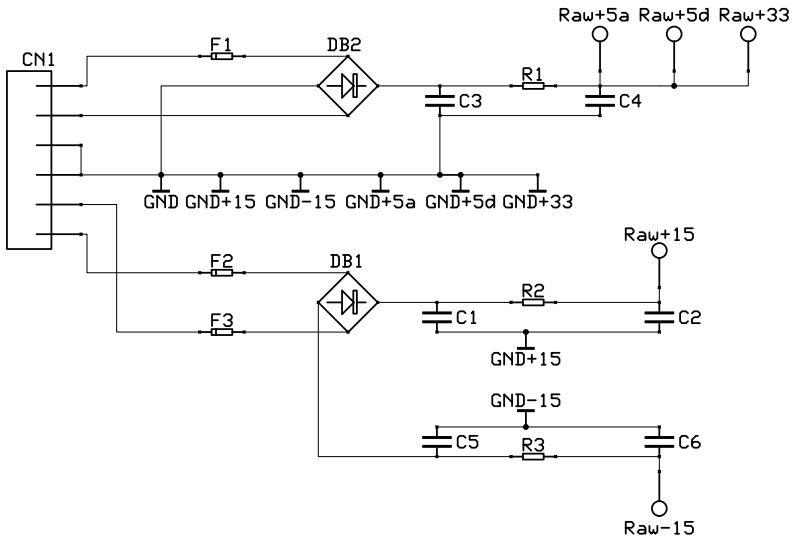


Figure B.18: Rectifier and prefilter.

Appendix C

PCB layout

C.1 Digital control unit

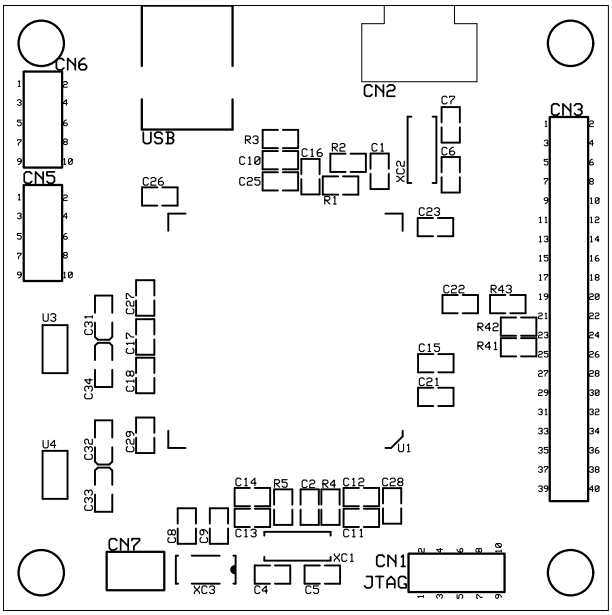


Figure C.1: Digital card, silkscreen top.

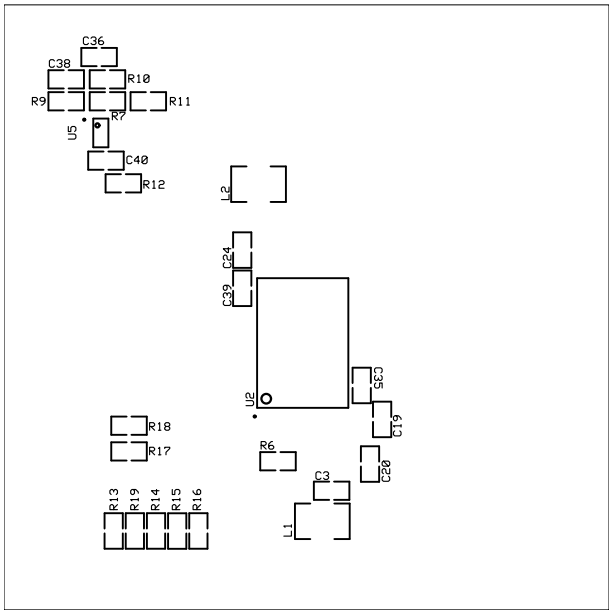


Figure C.2: Digital card, silkscreen bottom.

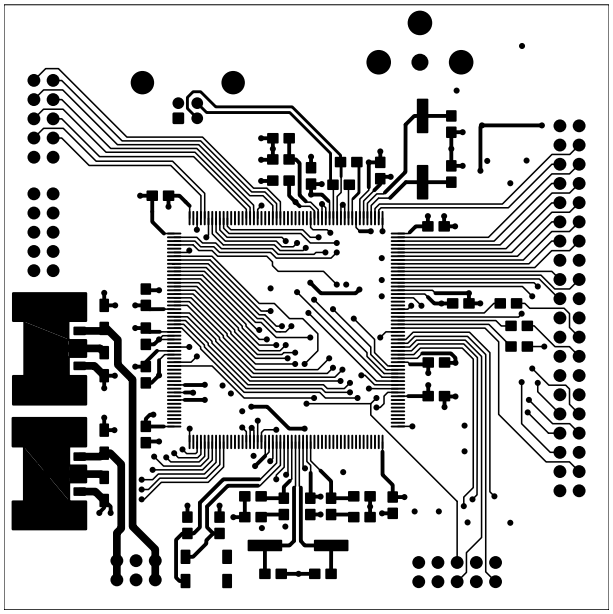


Figure C.3: Digital card, copper top.

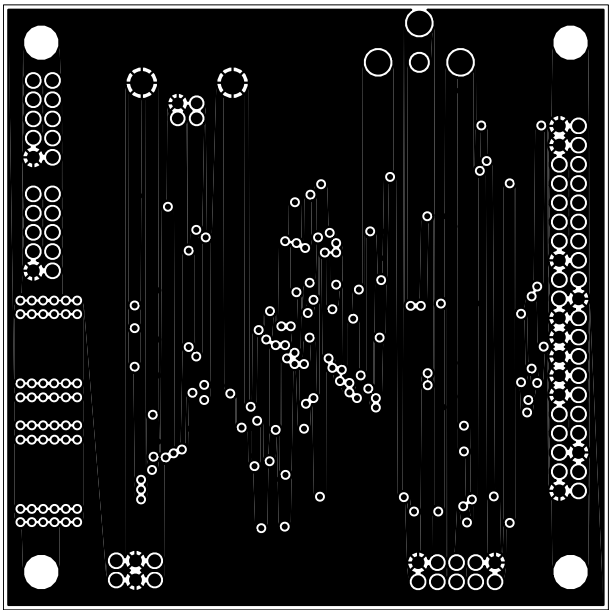


Figure C.4: Digital card, ground plane.

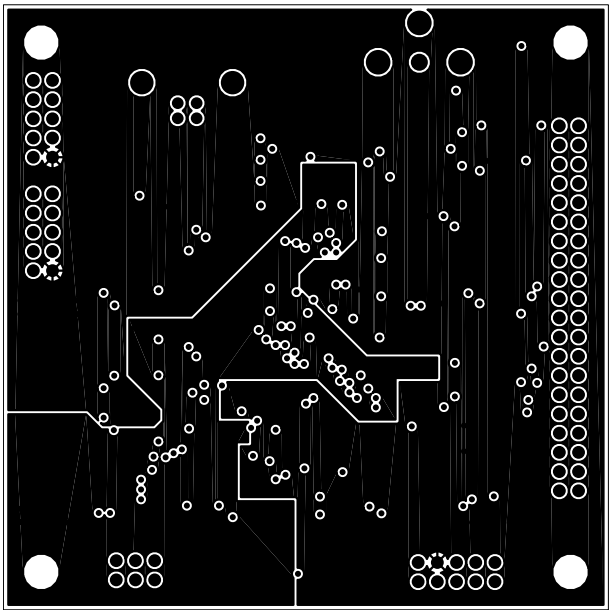


Figure C.5: Digital card, power plane.

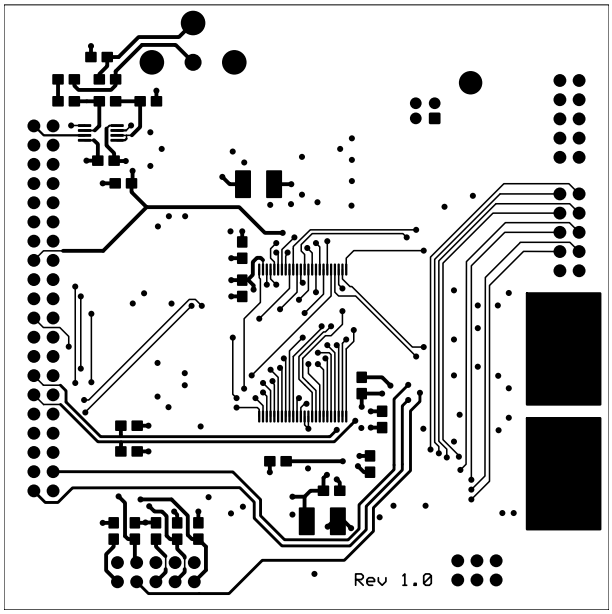


Figure C.6: Digital card, copper bottom.

C.2 DAC unit

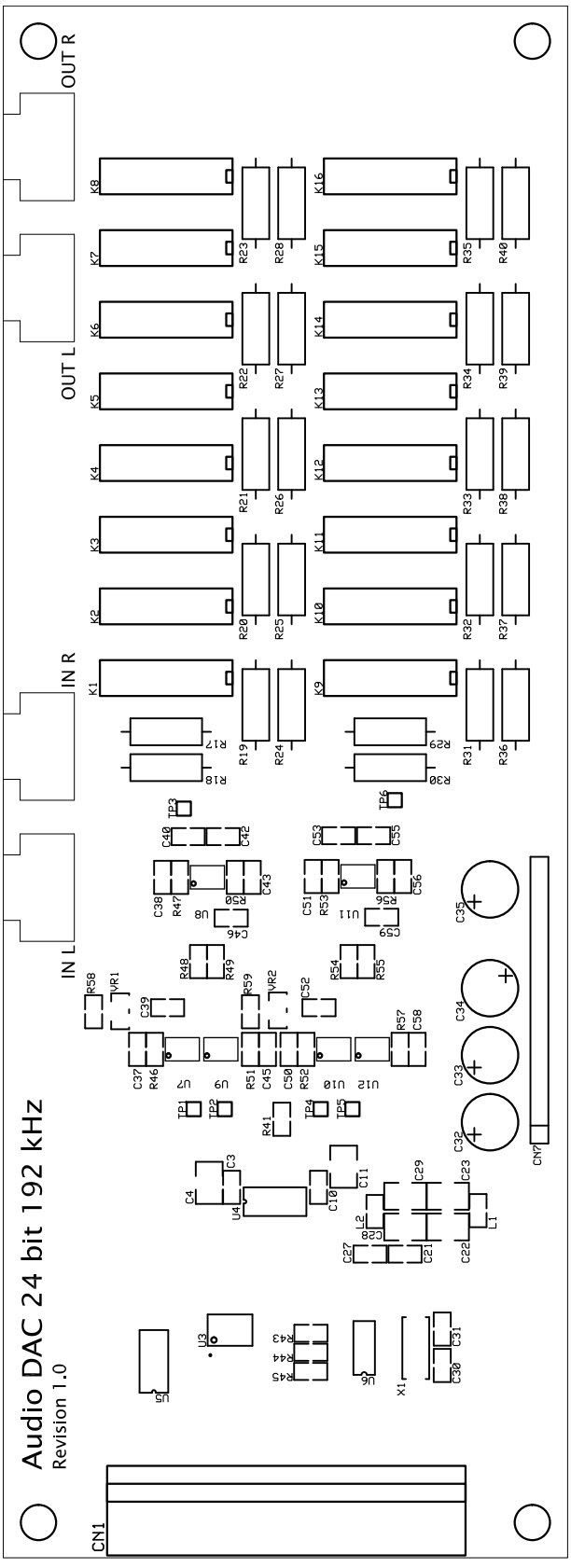


Figure C.7: Analog card, silkscreen top.

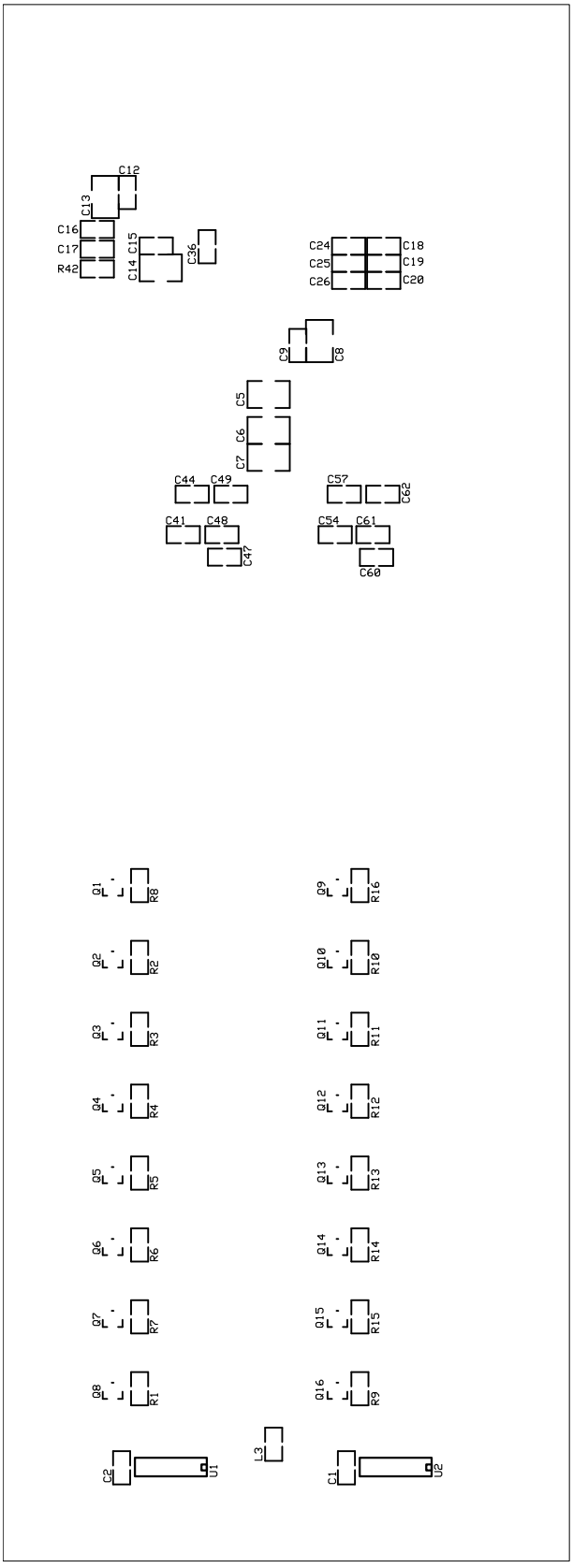


Figure C.8: Analog card, silkscreen bottom.

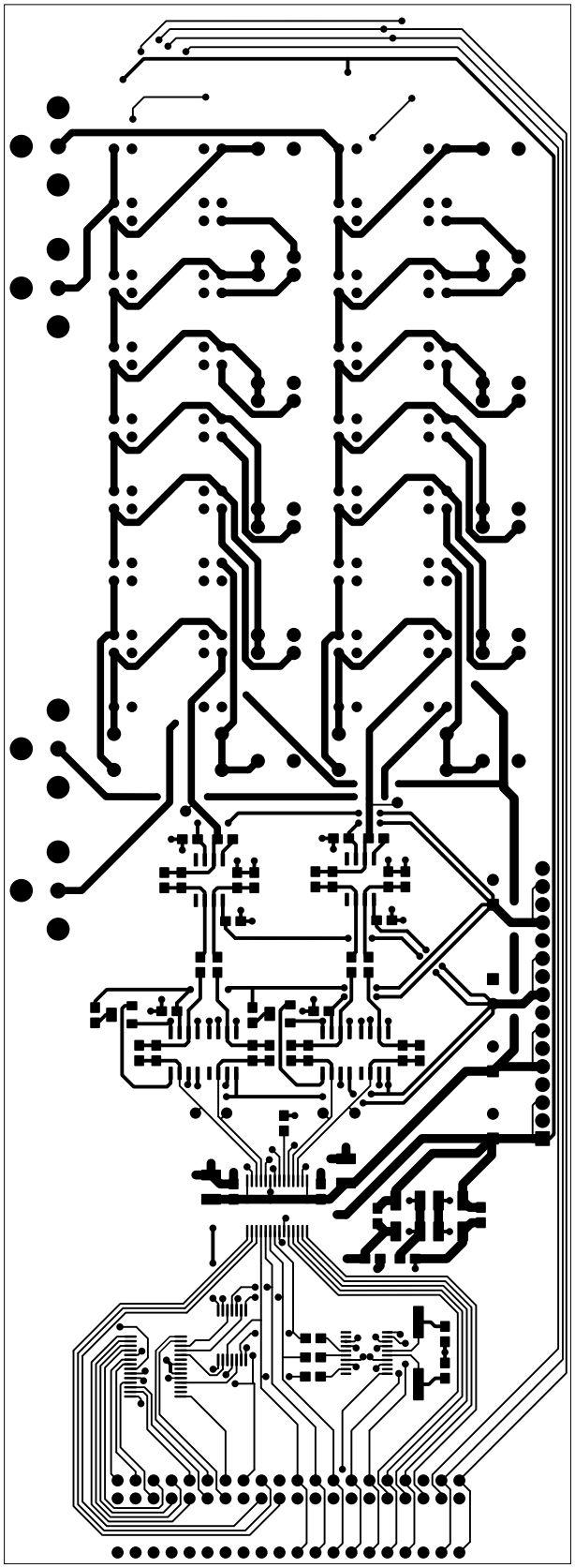


Figure C.9: Analog card, copper top.

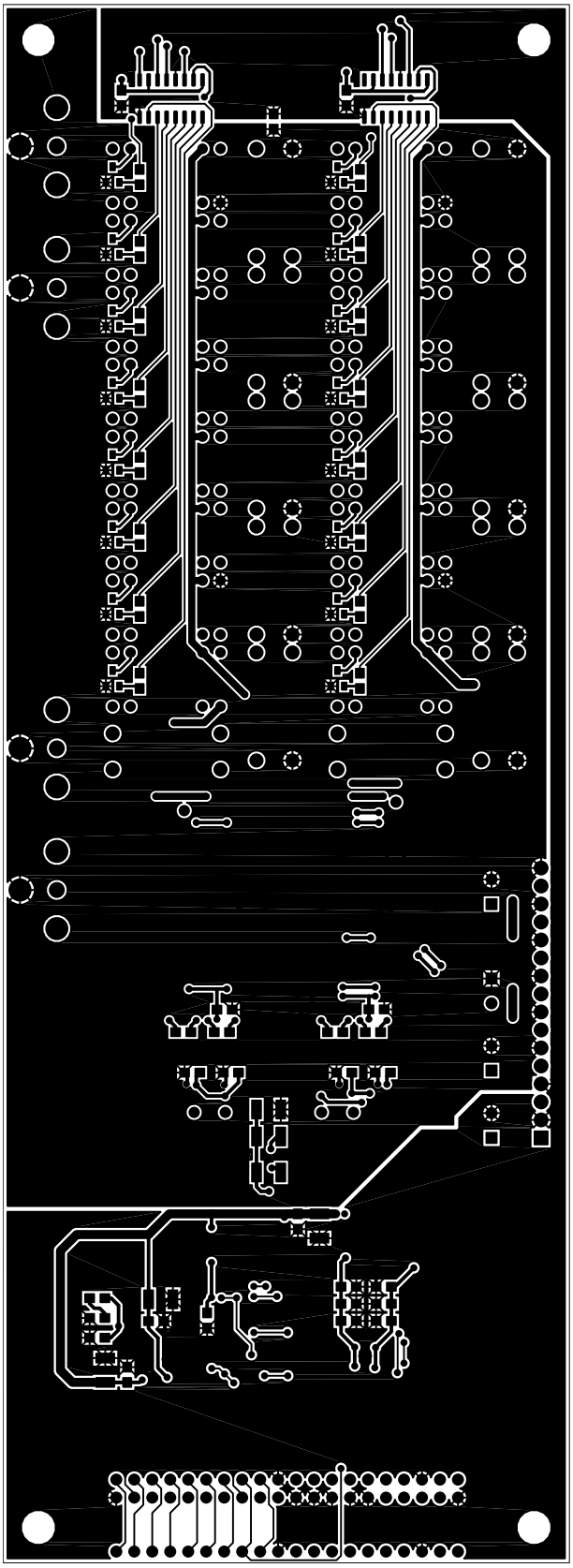


Figure C.10: Analog card, copper bottom.

C.3 Power supply unit

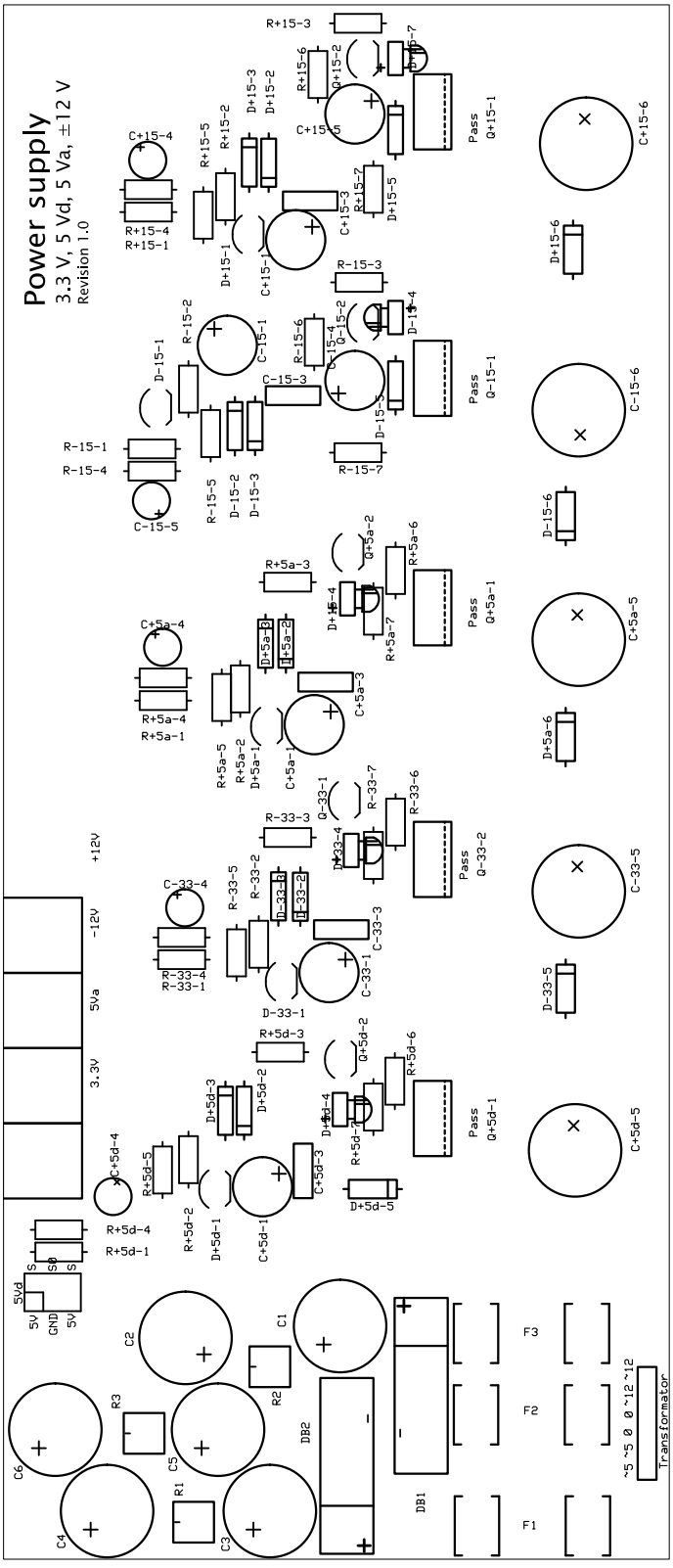


Figure C.11: Power supply, silkscreen top.

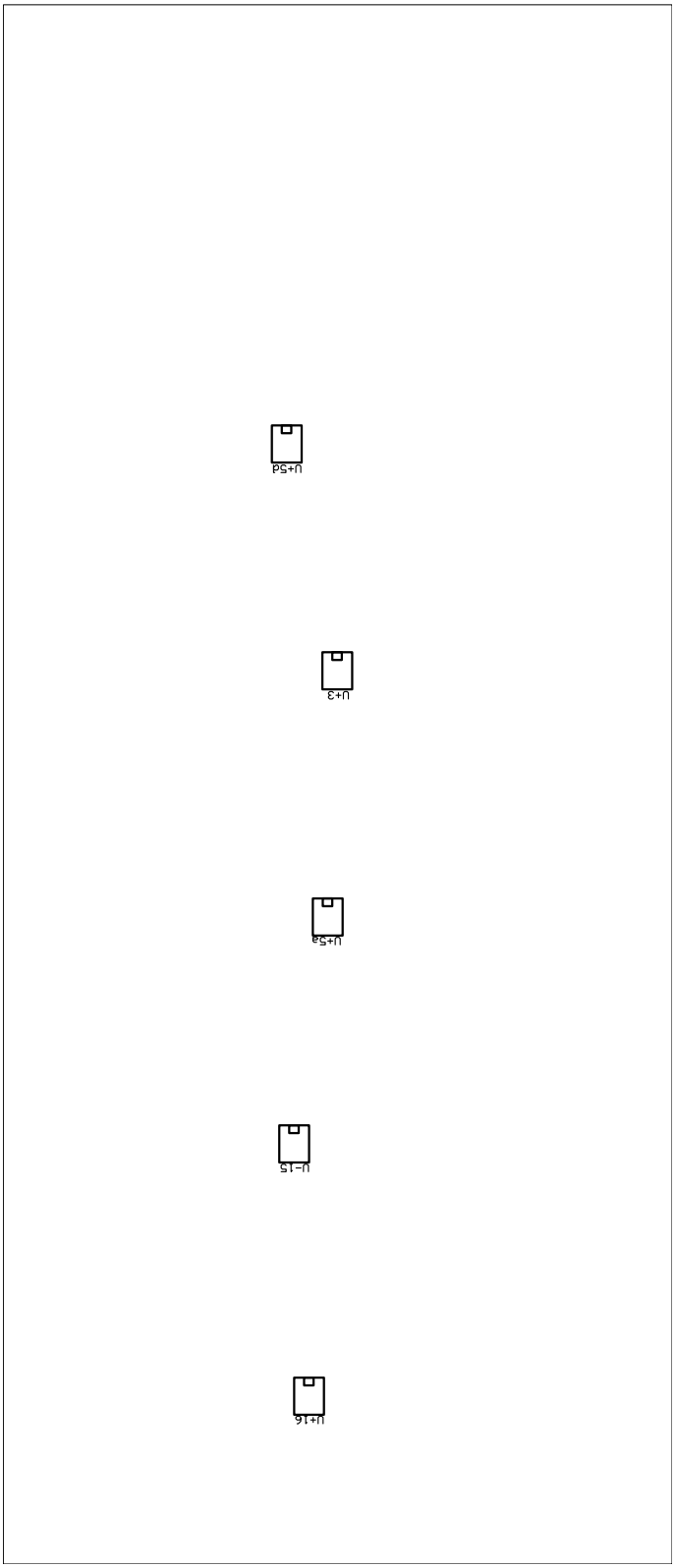


Figure C.12: Power supply, silkscreen bottom.

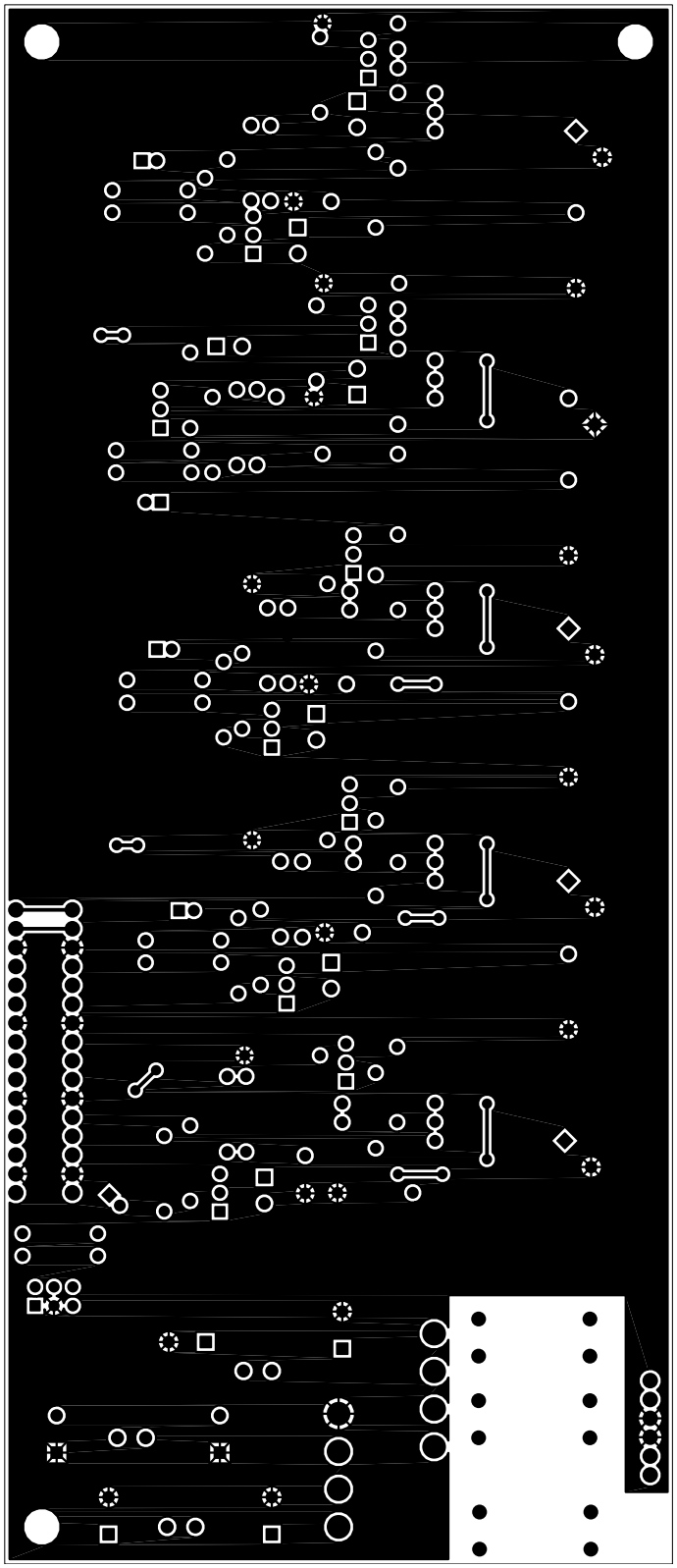


Figure C.13: Power supply, copper top.

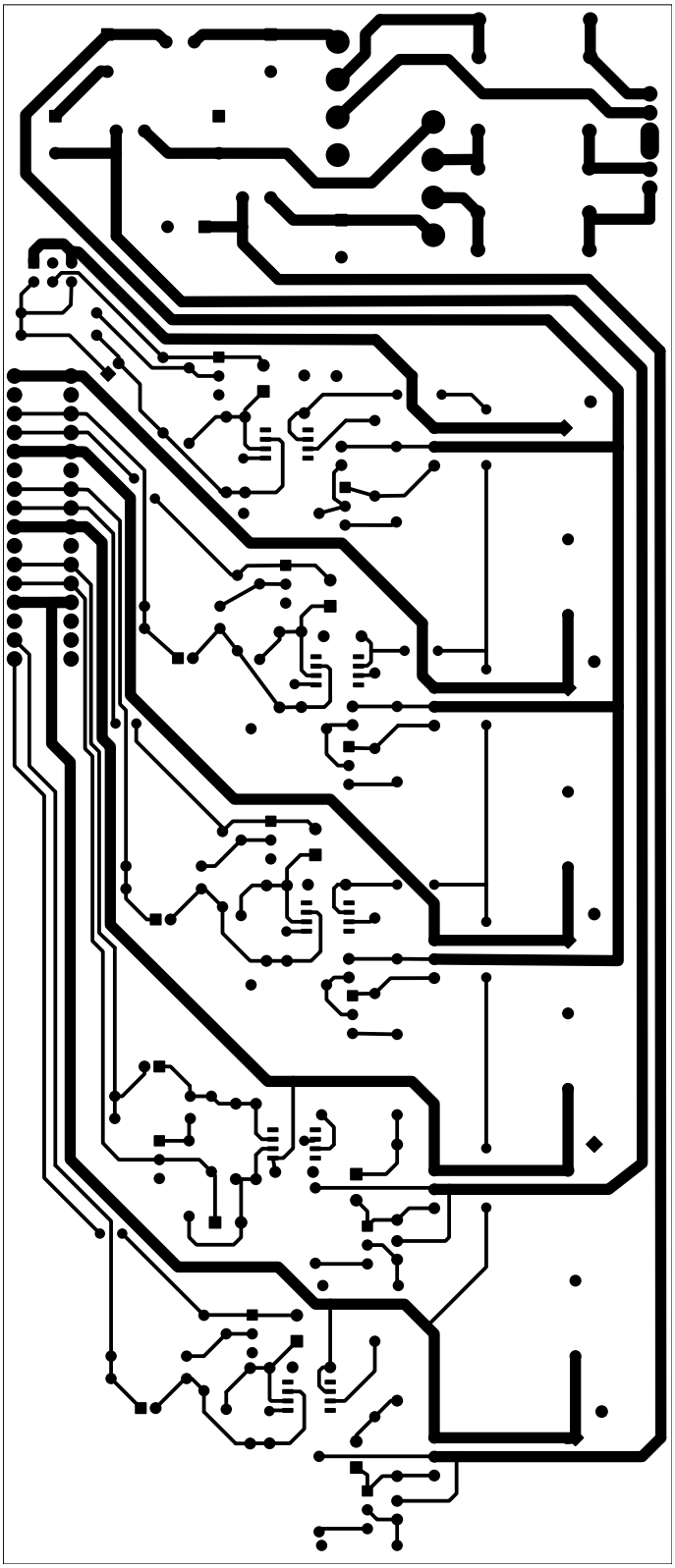


Figure C.14: Power supply, copper bottom.

Appendix D

Bill of materials

D.1 Digital control unit

Table D.1: Component list for digital control unit.

Quantity	Reference	Value	Part number
22	C_1, C_2, C_3, C_{15}, C_{16}, C_{17}, C_{18}, C_{19}, C_{20}, C_{21}, C_{22}, C_{23}, C_{24}, C_{25}, C_{26}, C_{27}, C_{28}, C_{29}, C_{35}, C_{36}, C_{39}, C_{40}	100 nF	Kemet C0805C104J5RAC
8	R_{12}, R_{13}, R_{14}, R_{15}, R_{16}, R_{17}, R_{18}, R_{19}	10 kΩ	KOA RK73H2ATTD1002F
1	C_{38}	10 nF	Kemet C0805C103K5RAC C-7025
1	C_{10}	10 pF	Kemet C0805C100J5GAC-TU
1	R_6	1 kΩ	Susumu RR1220P-102-D
2	R_1, R_2	39 Ω	Multicomp MCHP05W4F390JT5E
1	CN_3		AMP 2-0826634-0
4	C_4, C_5, C_6, C_7	33 pF	Kemet C0805C330J5GAC C-7025
2	C_8, C_9	22 pF	Kemet C0805C220J5GAC C-7025
1	C_{12}	3300 pF	Kemet C0805C332K5RAC
1	C_{11}	33 nF	Kemet C0805C333K5RAC

1	R_4	294 Ω	Multicomp MCTC0525B2940T5E
3	R_{41}, R_{42}, R_{43}	0 Ω	Phycomp (Yageo) RC11 0805 0R
2	C_{31}, C_{32}	15 µF, 10 V	AVX TRJA156K010R1000
2	C_{33}, C_{34}	22 µF, 6.3 V	AVX NOJA226M006RWJ
2	L_1, L_2	3.3 µH	Tyco Electronics 3613C3R3K
1	R_9	100 Ω	KOA RK73H2ATTD1000F
2	R_7, R_{11}	10 kΩ	KOA RK73H2ATTD1002F
1	R_3	6.81 kΩ	Vishay Dale CRCW08056K81FKEA
1	R_{10}	75 Ω	KOA RK73H2ATTD75R0F
1	U_4	1.8 V	LM1117MP-1.8 NOPB
1	U_3	3.3 V	LM1117MP-3.3 NOPB
1	XC_3	12.768 kHz	Citizen America CM200S32.768KDZF-UT
1	XC_2	12 MHz	Citizen America HCM49 12.000MABJ-UT
1	XC_1	20 MHz	Citizen America HCM49 20.000MABJ-UT
1	U_5,		Texas Instruments SN74LVC2G240DCTR
1	U_2	16 Mbit	Atmel AT49BV160DT-70TU
1	CN_7	2 × 3 header	Multicomp 2213S-06G
3	CN_1, CN_5, CN_6	2 × 5 header	Multicomp 2213S-10G
1	U_1		Atmel AVR32AP7001
1	CN_2	RCA jack	172-1-6
1	USB	USBB plug	

D.2 DAC unit

Table D.2: Component list for analog card.

Quantity	Reference	Value	Part number
1	U_4		Texas Instruments PCM1794ADB
2	U_1, U_2	74HC595D	
1	U_5		Texas Instruments DIR9001PW
1	C_{16}	4.7 nF	Murata GRM216R71H472JA01D
1	C_{17}	68 nF	Phycomp (Yageo) 644225RL
2	C_{18}, C_{24}	100 pF	Kemet C0805C101K5GAC-TU
2	C_{19}, C_{25}	1 nF	Kemet C0805C102J5GAC-TU
2	C_{21}, C_{27}	1 µF	Kemet C0805C105K4RAC
2	C_{23}, C_{29}	22 µF	Kemet T491A226K010AT
2	C_5, C_6	47 µF	AVX TPSB476K010R0350
4	C_{37}, C_{45}, C_{50}, C_{58}	2200 pF	Murata GRM2165C1H222JA01D
4	C_{41}, C_{48}, C_{54}, C_{61}	22 pF	Kemet C0805C220J5GAC C-7025
4	C_{38}, C_{43}, C_{51}, C_{56}	2700 pF	Kemet C0805C272K5RAC C-7025
4	C_{30}, C_{31}, C_{42}, C_{55}	33 pF	Kemet C0805C330J5GAC C-7025
8	C_4, C_7, C_8, C_{11}, C_{13}, C_{14}, C_{22}, C_{28}	10 µF	AVX NOJA106M006RWJ
22	C_1, C_2, C_3, C_9, C_{10}, C_{12}, C_{15}, C_{20}, C_{26}, C_{36}, C_{39}, C_{40}, C_{44}, C_{46}, C_{47}, C_{49}, C_{52}, C_{53}, C_{57}, C_{59}, C_{60}, C_{62}	100 nF	Kemet C0805C104K5RAC
3	L_1, L_2, L_3	?	Murata BLM21BB750SN1D
2	R_{58}, R_{59}	22 kΩ	Vishay Dale CRCW080522K0FKEA
1	R_{42}	680 Ω	Multicomp MC 0.1W 0805 1%
1	R_{41}	10 kΩ	KOA RK73H2ATTD1002F
3	R_{43}, R_{44}, R_{45}	0 Ω	Phycomp (Yageo) RC11 0805 0R
4	R_{47}, R_{50}, R_{53}, R_{56}	270 Ω	Multicomp MC 0.1W 0805 1% 270R

4	R_{48}, R_{49}, R_{54}, R_{55}	560 Ω	Multicomp MC 0.1W 0805 1% 560R
4	R_{46}, R_{51}, R_{52}, R_{57}	750 Ω	Multicomp MC 0.1W 0805 1% 750R
16	R_1, R_2, R_3, R_4, R_5, R_6, R_7, R_8, R_9, R_{10}, R_{11}, R_{12}, R_{13}, R_{14}, R_{15}, R_{16}	40.2 kΩ	Vishay Dale CRCW080540K2FKTA
1	U_6		Texas Instruments CDCE706PWG4
1	CN_7		AMP 3-0826631-6
1	CN_1		AMP 1-0216604-0
4	C_{32}, C_{33}, C_{34}, C_{35}	220 µF	Sanyo MV-WX
2	U_8, U_{11}		Linear Technologies LT1028CS8#PBF
4	U_7, U_9, U_{10}, U_{12}		Texas Instruments NE5534D
1	U_3		Texas Instruments SN74BTLV3125PW
2	CN_2, CN_3	Black	172-1-6
2	CN_4, CN_5	Red	172-1-5
16	K_1, K_2, K_3, K_4, K_5, K_6, K_7, K_8, K_9, K_{10}, K_{11}, K_{12}, K_{13}, K_{14}, K_{15}, K_{16}		Coto 8L41-05-011
2	R_{19}, R_{31}	1.05 kΩ	Vishay Sfernice MRS25 1K05 1%
2	R_{25}, R_{37}	10.7 kΩ	Vishay Sfernice MRS25 10K7 1%
2	R_{23}, R_{35}	154 kΩ	Vishay Sfernice MRS25 154K0 1%
2	R_{24}, R_{36}	19.6 kΩ	Vishay Sfernice MRS25 19K6 1%
2	R_{20}, R_{32}	2.32 kΩ	Vishay Sfernice MRS25 2K32 1%
2	R_{22}, R_{34}	21 kΩ	Vishay Sfernice MRS25 K 1%
2	R_{18}, R_{30}	36.5 kΩ	Vishay Sfernice MRS25 36K5 1%
2	R_{28}, R_{40}	4.2 kΩ	Vishay Sfernice MRS25 4K2 1%
2	R_{17}, R_{29}	4.42 kΩ	Vishay Sfernice MRS25 4K42 1%
2	R_{27}, R_{39}	4.75 kΩ	Vishay Sfernice MRS25 4K75 1%

2	R_{21}, R_{33}	6.04 kΩ	Vishay Sfernice MRS25 6K04 1%
2	R_{26}, R_{38}	6.65 kΩ	Vishay Sfernice MRS25 6K65 1%
16	Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, Q_7, Q_8, Q_9, Q_{10}, Q_{11}, Q_{12}, Q_{13}, Q_{14}, Q_{15}, Q_{16}		On Semiconductor BC847CLT1G
2	VR_1, VR_2	1 kΩ	BITechnologies 44WR1KLFTB
1	X_1	28.224 MHz	Citizen America HCM49 28.224MABJ-UT

D.3 Power supply unit

Table D.3: Component list for power supply.

Quantity	Reference	Value	Part number
2	R_{+15-4}, R_{-15-4}	1.1 kΩ	
1	R_{-33-1}	1.2 kΩ	
2	R_{+15-5}, R_{-15-5}	1.5 kΩ	
2	R_{+5a-1}, R_{+5d-1}	1.8 kΩ	
5	R_{+5a-7}, R_{+5d-7}, R_{+15-7}, R_{-15-7}, R_{-33-7}	10 Ω	
5	R_{+5a-6}, R_{+5d-6}, R_{+15-6}, R_{-15-6}, R_{-33-6}	100 Ω	
2	R_{+15-3}, R_{-15-3}	10 kΩ	
5	C_{+5a-3}, C_{+5d-3}, C_{+15-3}, C_{-15-3}, C_{-33-3}	100 nF	
2	C_{+15-5}, C_{-15-4}	120 µF	
1	D_{-33-5}	1N5335B	
2	D_{+5a-6}, D_{+5d-5}	1N5341B	
2	D_{+15-6}, D_{-15-6}	1N5353B	
4	R_{+5a-4}, R_{+5a-5}, R_{+5d-4}, R_{+5d-5}	1 kΩ	
11	C_1, C_2, C_3, C_4, C_5, C_6, C_{+5a-5}, C_{+5d-5}, C_{+15-6}, C_{-15-6}, C_{-33-5}	1 mF	
2	D_{+15-5}, D_{-15-5}	1N5235B	
4	C_{+5a-4}, C_{+5d-4}, C_{+15-4}, C_{-15-5}	1 µF	
3	R_1, R_2, R_3	2.7 Ω	
5	C_{+5a-1}, C_{+5d-1}, C_{+15-1}, C_{-15-1}, C_{-33-1}	220 µF	
1	C_{-33-4}	3.7 µF	
1	R_{-33-5}	330 Ω	
2	R_{+15-1}, R_{-15-1}	5.6 kΩ	
1	R_{-33-4}	560 Ω	

3	R_{+5a-3}, R_{+5d-3}, R_{-33-3}	6.8 kΩ	
5	R_{+5a-2}, R_{+5d-2}, R_{+15-2}, R_{-15-2}, R_{-33-2}	680 Ω	
4	U_{+3}, U_{+5a}, $U-_{+5d}$, U_{+15}, U_{-15}		Texas Instruments NE5534D
2	DB_1, DB_2	Rect. bridge	
1	$CN_{5\,Vd}$	2 × 3 header	
3	F_1, F_2, F_3	5 mm × 20 mm	Glass fuse holder
1	D_{-33-1}	LT1034-1.2	
2	D_{+5a-1}, D_{+5d-1}	LT1034-2.5	
1	Q_{-15-1}	2SA2037	
5	D_{+5d-4}, D_{+15-4}, D_{+15-7}, D_{-15-4}, D_{-33-4}	LED	
4	Q_{+5a-1}, Q_{+5d-1}, Q_{+15-1}, Q_{-33-2}	2SC5694	
4	CN_1	Socket	
2	D_{+15-1}, D_{-15-1}	Ref	
1	Q_{-15-2}	2N5089	
4	Q_{+5a-2}, Q_{+5d-2}, Q_{+15-2}, Q_{-33-1}	2N5087	
1	6-Polig	Transformator	
10	D_{+5a-2}, D_{+5a-3}, D_{+5d-2}, D_{+5d-3}, D_{+15-2}, D_{+15-3}, D_{-15-2}, D_{-15-3}, D_{-33-2}, D_{-33-3}	1N4148	

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