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Capacitive Sensor Interface Circuits

Thesis for the degree of Philosophiae Doctor

Trondheim, July 2009

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Abstract

This thesis focuses on simple capacitive measurement techniques suitable for integration in CMOS technologies. The main motivation being: to realize simple frontends for capacitive sensors and microsystems for integration in high-density sensing applications, for example, in arrays of sensors for high-resolution ultrasound imaging. In addition, there are many applications where a high accuracy in sensing is not essential; in such cases, a simple interface circuit can not only save the design time, but may also offer area and power advantages over the more complex circuits. Therefore, one of the main aims in this research has been to realize simple circuit topologies that may benefit such applications.

Two different kinds of sensing circuits form the highlight of this thesis. The first interface circuit is the realization of a current-mode approach that has the main advantage of being able to produce a fully-differential output also from a single-ended sensor by using just a fixed reference capacitor. The circuit, prototyped in a commercial 0.8-μm CMOS process, was estimated capable of achieving an accuracy of around 0.2% relative to full-scale which may be sufficient in many applications. In the second prototype, the feedback biasing technique is rediscovered for nanoscale CMOS technologies. It is shown that some of the classic limitations imposed by the use of feedback biasing in CMOS circuits are removed in nanoscale technologies, and when using MOSFET as feedback resistor; it is possible to realize extremely compact amplifiers. Such feedback-biased cascaded CS amplifiers, designed in a commercially available CMOS technology, achieved a voltage gain of 28 dB, an output noise power spectral density of 0.11 $(\mu V)^2$/Hz at center-frequency, and a total harmonic distortion of -30 dB at full-scale output. These specifications are acceptable for application of such amplifiers as CMUT frontends. By using subthreshold MOSFETs as feedback resistors, extremely compact amplifiers (measuring just 20 μm $\times$ 10 μm) were obtained. However, by using the MOSFET feedback resistor, the linearity of the amplifier is affected by the non-linearity in the resistance of the MOSFET. A simple remedy is

proposed that recovers a large part of the linearity degradation by sacrificing slightly on the input resistance. The linearity improvement was observed to be more than 100% in the best case. The area overhead due to the additional device is very small.

Preface

This thesis is the result of my doctoral research on capacitive sensor interface circuits carried out at Norwegian University of Science and Technology (NTNU) Trondheim at the Department of Electronics and Telecommunications from 2002 to 2008. The domain of my research was CMOS interface circuits for capacitive detection for application in microsensors and MEMS.

Overview of the Presented Work

Three tapeouts were made during this research, the first (Tapeout 1) in 0.8-μm CMOS technology, the second (named *Alabama*) and the third (named *Bombay*), both in 90-nm CMOS technology. This thesis constitutes six research papers published/submitted by me as the first author, during my work at NTNU. The first prototype based on the measurement concept presented in Paper [1] was produced in Tapeout 1. An alternative version of the measurement concept was presented in Paper [2]. Paper [3] presents the amplifier design taped-out in *Alabama*. Tapeout *Alabama* was the first in 90-nm technology, for us at the department. Therefore, the *Alabama* chips were used for characterizing the devices in 90-nm technology and for testing the DC performance of the first batch of CS amplifiers using feedback biasing. The measurement results of Tapeout 1 prototypes are discussed in Paper [4]. The prototypes for full characterization of CS amplifiers using feedback biasing were produced in *Bombay*. The measurement results of this chip are discussed in Papers [5] and [6].

This thesis begins with an introductory chapter on sensor systems (Chapter 1) to provide a motivation behind this work. The chapter also explains the importance and reasons for capacitive sensing being popular in integrated sensors, and an application of capacitive sensing in CMUTs is also covered. Chapter 2 provides an overview of the individual papers that are part of this thesis, and their respective errata. Chapter 3 contains the chip photographs of the characterized prototypes included in this thesis. Indi-

vidual research papers are appended in Chapters 4 – 9. The conclusion to this research work is presented in Chapter 10.

Comments on Style

This thesis contains two bibliographies. The first bibliography, immediately following this chapter is composed of the research papers that are presented as a part of this thesis. The references to these papers in this thesis appear as plain-numbered citations (for example, [1]). The second bibliography, in the very end, lists the external literature cited in this thesis. The citations in the second bibliography appear in an alpha-numeric format (for example, [Whi87]).

List of appended papers

[1] T. Singh and T. Ytterdal, "A single-ended to differential capacitive sensor interface circuit designed in CMOS technology," in *Proc. IEEE International Symposium on Circuits and Systems(ISCAS'04)*, Vancouver, Canada, May 2004, pp. I – 948–51 Vol.1.

[2] T. Singh, T. Sæther, and T. Ytterdal, "A linear capacitive sensor interface circuit with single-ended to differential output capability," in *Proc. NORCHIP'04)*, Oslo, Norway, Nov. 2004, pp. 32–35.

[3] ——, "Common source amplifier with feedback biasing in 90nm CMOS," in *Proc. IEEE Research in Microelectronics and Electronics 2006, Ph.D. (PRIME'06)*, Otranto (Lecce), Italy, Jun. 2006, pp. 161–164.

[4] ——, "Current mode capacitive sensor interface circuit with single-ended to differential output capability," *IEEE Transactions on Instrumentation and Measurement*, 2009, Accepted for publication.

[5] ——, "Feedback biasing in nanoscale CMOS technologies," *IEEE Transactions on Circuits and Systems—Part II: Express Briefs - Special Issue on Circuits and Systems Solutions for Nanoscale CMOS Design Challenges*, vol. 56, no. 5, pp. 349–353, May 2009.

[6] ——, "Compensating for non-linearity in feedback biased common-source amplifiers using MOS feedback resistors," *IET Electronics Letters*, 2009, Submitted.

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Within the professional circle, I sincerely thank my main supervisor Prof. Trond Ytterdal and my co-supervisor Prof. Trond Sæther for making this work possible. I am very grateful for their advice, ideas and guidance, which have been of crucial importance to this work. I express my special gratitude to Prof. Ytterdal, for offering me absolute freedom in choosing my research domain and his support all the way through. I would like to thank him also for providing me ample opportunities, altogether around 2 years, for teaching masters' level courses in analog design.

Due to my long association with the Department of Electronics and Telecommunications, there is a long list of people who, although not directly associated with my research work, but deserve my heartfelt thanks. In no particular sequence, they are: Associate Prof. Ragnar Hergum for entrusting me with the responsibility to teach his courses, Tore Barlindhaug for his immense help and support during the lab work, PCB design and other related matters, my colleagues Carsten Wulff, Thomas Halvorsrød and Linga Reddy Cenkeramaddi for valuable professional discussions, our secretaries at the department Randi Hostad, Hagel M. Øyan and Signe J. Talukder for their help (with a smile) in administrative and official matters. Last but not the least, Prof. Einar J. Ås for forwarding my application and résumé to Prof. Sæther and Prof. Ytterdal – which is where this all started. I extend my gratitude also to those many other people at the department who have not been named here, but with whom I had the pleasure of working with. My thanks also go to the students to whom I had the opportunities of teaching analog design and with whom I had all those interesting discussions that helped me broaden my horizon in this field.

On the personal side, my thanks again go first to Trond Ytterdal for

being there also as a guardian, with his advice and help also in non-work related issues. This period at NTNU forms an exciting (and long) chapter of my life. This was perhaps the greatest challenge that I could have taken at that time. Having a background in Instrumentation and Control Engineering (Bachelor degree) and Sensor Systems Technology (Master degree), to be working with analog IC design was a long sought dream for me, but with very little experience. I thank Trond Ytterdal and Trond Sæther for recognizing my zeal to work in this field and entrusting me with this valuable opportunity. Due to little prior experience in analog design before starting my research, this period at NTNU was not short of frustration, silly mistakes, and petty failures at times, but fortunately, in equal proportions also not short of a sense of accomplishment. Summing it all up by twisting Neil Armstrong's famous words, "*one small step for mankind, but a giant leap for myself*".

When talking on the personal side, my family deserves a very special thanks. My father, for dreaming for me always one step ahead of me, for his guidance in all phases of my life, from most of the application forms that I have filled, to proof-reading most of the professional letters that I wrote, and looking out for future professional opportunities for me in his spare time. Thank you for cultivating the passion for electronics in me by buying for me my first multi-meter and many soldering irons and tools. My mother, for being a buffer between me and the real-life problems, for not letting any kind of pressure to be passed on to me and letting me do whatever I love to do. Thanks to my sister for her love and prayers. Thanks to my loving wife for entering my life during this period, after which, things somehow always seemed easier. Thanks to God Almighty for always showing the right path, and blessing us with everything, especially our loving daughter Sukrit.

This period at NTNU has also given me many good friends to be proud of: Chang Chuan You, Tron Arne Nilsen, Lucero Alvarez, Marta Laguna, Lars G. Evje, Øystein Dahl, Silje Marie Nedland, Thomas Halvorsrød, Ekaterina Ponomareva and Øystein Gjermundnes.

I am obliged to my present employer Atmel Norway AS, especially my current supervisor Terje Sæther, for their understanding and for giving me the time to complete this thesis.

Trondheim, May 2009

Tajeshwar Singh

Contents

List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
CMUT	Capacitive Micromachined Ultrasound Transducer
CS amplifier	Common-source amplifier
DC	Direct Current
DSP	Digital Signal Processing
EDA	Electronic Design Automation
GBW	Gain Bandwidth (product)
FoM	Figure of Merit
HD	Harmonic Distortion
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IM3	Third Order Intermodulation (distortion)
IMD	Intermodulation Distortion
IT	Information Technology
MEMS	Micro-Electro-Mechanical Systems
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-channel MOSFET
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PMOS	p-channel MOSFET
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
RMS	Root Mean Square
SMiDA	Smart Microsystems for Diagnostic Imaging in Medicine
SNR	Signal to Noise Ratio
TIA	Transimpedance Amplifier
THD	Total Harmonic Distortion

Chapter 1

Sensor Systems

1.1 Motivation

Sensors have come a long way, from being applied in specialized applications, to being a part of our everyday life. From a simple thermostat in the ovens, to fingerprint identification systems now commonly seen in many portable computers, sensors are already such an important part of our everyday lifestyle that sometimes we may not even realize. For example, a modern car may easily contain more than 100 sensors [MI02], that are used for several functions. To name a few with examples: basic operation (*engine temperature, oil pressure*), information and driving help (*parking aid, tire pressure measurement*), comfort (*air conditioning*), safety (*airbag deployment, yaw rate sensing*) and optimization (*exhaust gas monitoring*) etc.

Besides the automobile segment, which is one of the largest sectors in the sensors market [Int99], there are several other areas where sensors improve our lifestyle, for example, medical diagnosis, security systems, and several other automation applications at home and in the industry. As we strive for more and more information and better automation, there is a steady push to the increasing applications of sensors.

1.2 The Role of CMOS Technology

There is a little doubt that CMOS technology has been the engine driving the IT revolution. It is the CMOS technology that has made it possible to fabricate cheap integrated circuits (ICs) that are now an integral part of the world around us. The systems designed and developed using the chips produced by the CMOS technology also, in turn, help improve this technology, thereby creating a snowball effect due to which we have seen,

and continue to see, new innovations come out almost everyday. This is perhaps a unique example of such a fast-paced development within any given technology. Like many other fields, sensor systems technology owes a fair amount of its progress to the developments in the CMOS technology.

One of the most important features of the CMOS technology, that has made all this possible, is its suitability to create digital logic which can be used to produce cheap and flexible digital signal processing (DSP) that gets faster and denser by each succeeding technology generation. On the contrary, analog signal processing capabilities typically become poorer as device dimensions are scaled down i.e., in each new technology generation [ANvLT05]. Due to flexibility and ease of implementing signal processing functions in the digital domain, the use of analog signal processing has diminished a lot over all these years. There are, however, certain blocks in a sensor system that are not possible to implement in the digital domain and where analog circuits are required. We will discuss more about this in the subsequent sections.

1.3 Classification of Sensors

The definition of a *sensor* in open literature can be found sometimes as a generalized one i.e., *a device that receives and responds to a signal or stimulus* [Fra03], and at other times, a more specific one; *a device that converts a physical phenomenon into an electrical signal* [Wil04, PAW00]. There is, however, one thing which is common, that is, a sensor serves as a *translator* converting the physical quantity that it measures, to the output that it produces (electrical, in most modern day sensors). This electrical output can then be processed and used for eventual automation purposes. From this point forward in this thesis, we will refer to the term *sensor* for a device that produces an electrical output.

Due to different varieties and applications of sensors, there are many ways to classify them. These classification schemes range from the very simple to the complex [Whi87]. Some most commonly used classification categories for the sensors are shown in Fig. 1.1.

Sensors can be classified based on the physical quantity that they measure (measurand), for example, *temperature*, *pressure*, etc. Some sensors generate their own current/voltage signal (*active* sensors), for example, thermocouples and piezoelectric sensors, while the others require an external power supply (*passive* sensors). This difference can be used to categorize the sensors by what kind of output signal they produce. But, the property that is perhaps most important to a sensor system designer is the kind of

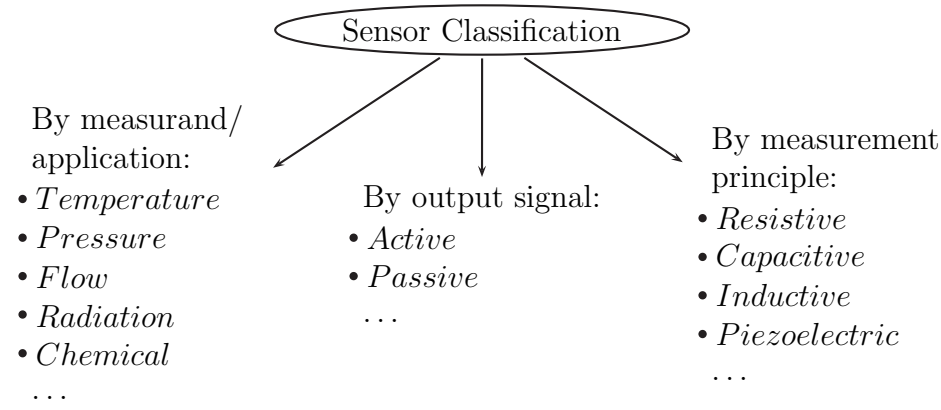

Figure 1.1: Sensor Classification.

measurement principle a given sensor uses. Some of the candidates in this category are *resistive*, *capacitive*, *inductive* sensors, etc. This property of the sensor mostly decides what kind of signal conditioning it will require.

1.4 Sensor Signal Conditioning

The output signal produced by a sensor is usually not suitable to be processed directly in the digital domain, therefore, the sensor output needs to be *conditioned* before it can be input to the DSP. This signal conditioning usually involves *amplification*, but it may also involve *filtering*, *compensation* or other types of analog processing. Therefore, the circuit block that directly handles the sensor output is usually analog. As a matter of fact, the use of analog signal processing is almost always required in the situations when it comes to interacting with the "real" world. This is because most of the physical phenomenon and information in the world around us consists of "continuous", and not discrete, quantities unlike the digital domain.

Fig. 1.2 shows the block diagram of such a typical electronic sensor system. The sensor operation can be broadly divided into two main parts *detection* and *output generation*. As the sensor converts the physical quantity to an electrical signal, it has an interface that interacts with this physical quantity. Depending upon the kind of physical quantity (*temperature*, *pressure*, *gas composition*, etc.), this detection interface may, for example, consist of a mechanical element, a chemical film, or a magnetic component, etc. The detection interface changes its properties as a function of the physical quantity to generate an output which is also a function of the physical quantity

interacting with the sensor. The sensor output is fed to a *signal conditioning* block which is mostly composed of analog frontends. The *conditioned* output may then either be an input to the DSP, or may be subject to further analog processing, depending upon the sensor system.

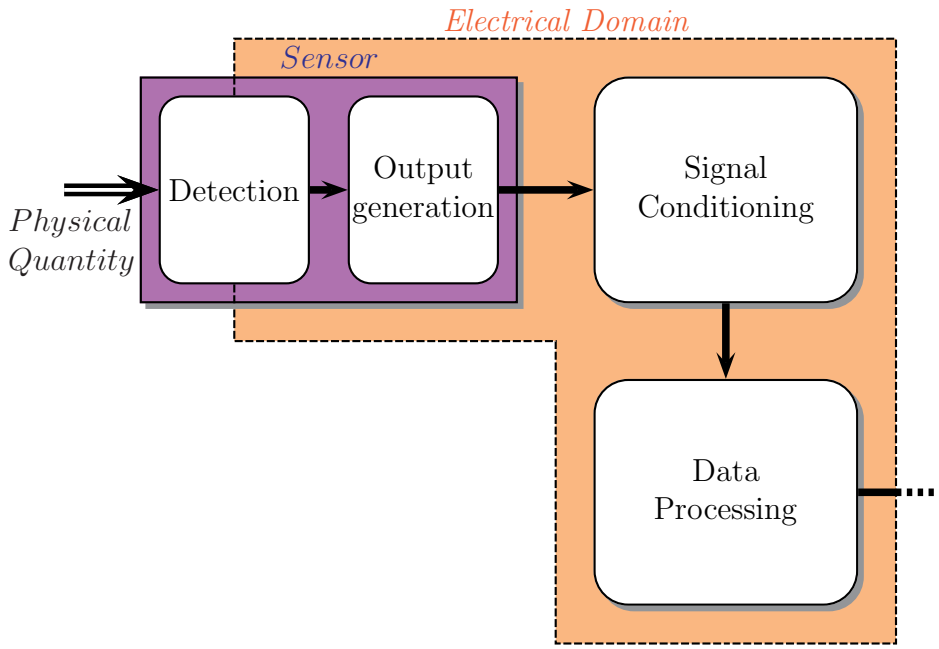

Figure 1.2: A typical sensor system.

In *smart* sensors, all of the blocks shown in Fig. 1.2 are usually integrated with the sensor.

1.5 Capacitive Sensors

Based on the classification discussed in the previous sections, capacitive sensors are categorized based on their operating principle (variable capacitance). They also fall under the category of *passive* sensors. Capacitive measurement principle based sensors are extensively used for several applications due to numerous advantages [Bax96] that they offer, some of which are listed as follows:

1. Possibility of non-contact measurements.
2. Simple principle (only two surfaces required to make a capacitor).
3. Compatible with CMOS technology (may not require exotic processing steps or materials).
4. Can be easy to fabricate as compared to the other sensor types.
5. MEMS realization options (several micromachining techniques available).
6. Can be applied for measurements of several types of physical quantities.
7. Do not require continuous bias current.
8. Can be unaffected by temperature, mechanical misalignment, etc.
9. Among the electronic devices fabricated in microtechnology, the capacitors have their characteristics closest to the ideal behavior.

Capacitive sensing is, almost exclusively, the sensing principle of choice for application in numerous micro-devices such as accelerometers, pressure sensors, RF MEMS resonators, etc. An important advantage of choosing capacitive sensing in such cases is that there is no physical contact between the measuring surfaces, which means that the sensor does not physically *load* the mechanical movement, for example, of the cantilever/resonator. Since ideal capacitors are perfect insulators at DC, they do not consume any DC current which makes them ideally suited for low-power applications. Several micromachining schemes have been developed to integrate the MEMS in CMOS technology [BBF$^+$05], and capacitive sensing scheme is an ideal candidate for use in devices developed with such schemes because it does not require any additional special materials (for example piezoelectric films, etc.) for realization.

The well known capacitance formula for a parallel plate capacitor

$$C = \epsilon \frac{A}{d} \tag{1.1}$$

can be referred to show the possibilities for designing a capacitive sensor. The quantities on the right hand side (RHS) of equation (1.1) are, the dielectric constant (ϵ) of the medium sandwiched between the two plates that are placed at a distance (d) apart from each other and share an overlapping

area (A). The capacitance (C) of a capacitor is dependent on each of these quantities. For example, the variation in the dielectric constant can be used to sense the changes in the liquid level inside a tank with the parallel capacitor plates placed vertically such that the variations in the liquid level changes the medium between the plates and hence the capacitor's (ϵ).

But, in the most widely used applications of the capacitive sensing principle in microsensors (pressure sensors, accelerometers, microphones, etc.), the detection schemes based on distance (d) or area (A) variations are used more commonly. Fig. 1.3 (a)-(b) shows an example of the plate *distance* based measurement. The left plate is fixed and the right plate movement is a function of the physical quantity to be measured. Therefore, the capacitance of the sensor deviates from its nominal value C based on the value of the physical quantity. Such a two terminal sensor can also be called a *single-ended* sensor, as its capacitance value changes in only one direction at a time, corresponding to the direction of change in the physical quantity.

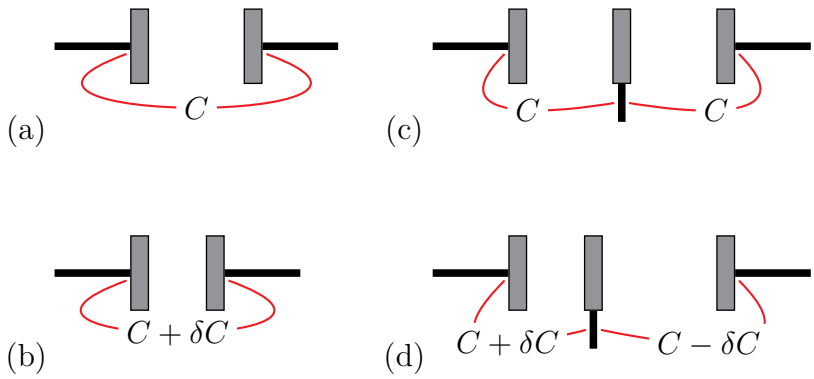

Figure 1.3: (a)-(b) Single ended and, (c)-(d) differential capacitive sensors.

Another configuration that is possible to realize with capacitive sensors, and with other sensors as well, is the *differential* configuration as shown in Fig. 1.3 (c)-(d). In such differential capacitive sensors, the movable plate is placed at equal distances from the two fixed plates. Due to this, whenever the moving plate moves laterally in either direction, capacitance value of this plate in relation to the two fixed plates changes by an equal amount, but with opposite signs. These sensor types can offer well-known advantages of a differential system, such as rejection of common-mode noise and interference. However, due to higher mechanical complexity, differential capacitive sensors can be difficult and expensive to manufacture as compared to their single-

ended counterparts.

1.6 CMUT: An application of capacitive sensing

1.6.1 Introduction

Capacitive Micromachined Ultrasound Transducers[1] (CMUTs) are currently a topic of widespread research. Among the potential applications of CMUTs are, medical ultrasound imaging [WZY+08, CCC+08] and non-destructive material testing [WFT+07]. It is possible to fabricate CMUTs with a performance that can compete with that of piezoelectric transducers. It is the development in silicon micromachining technology that has brought the capability to manufacture these devices and which gives them such a competitive edge [KYCD+00]. There is a plenty of literature available on the design and fabrication of CMUTs, see for example [LJS+98, NJR+01].

As the term *transducer* in the name "CMUT" might indicate, the device can not only act as a *sensor*, but also as an *actuator* i.e., a CMUT can be used both for generating and sensing the ultrasound signals. This capability of CMUTs is similar to their conventionally used counterparts in ultrasound applications: piezoelectric transducers. Some of the main differences, however, that make CMUTs such an attractive alternative to piezoelectric transducers are:

1. Compatibility with CMOS technology.
2. Inherent impedance match between the transducer and the surrounding medium [EYKY03].
3. Ease in fabricating dense transducer arrays for advanced imaging capabilities [OEC+03].

Above three advantages open a whole new area of applications for ultrasound systems based on CMUTs. In conventional medical ultrasound systems, the cable connecting the ultrasound transducer to the processing console is one of the most expensive items in the whole system [Bru02]. This hardwiring approach of connecting each transducer element individually to the processing console not only sets a limit to the resolution of the system due to the cost factor, but also due to practical reasons, for example, impracticality during use due to increased thickness of such a cable. Compatibility

[1] A *transducer* is defined as a device that converts one form of energy into another. This term encompasses both sensors and actuators [Kov98].

of CMUTs with the CMOS technology means that the devices can have local signal conditioning option and possibility of making *smart* transducers. The output of such a smart system can be a digital data stream, that contains outputs of several transducer elements and, transmitted over a simple cable or even wirelessly. Reduced problems with impedance matching means that CMUT devices can be easily used in immersed media. Silicon micromachining technology also allows large arrays of CMUTs to be fabricated, which not only means higher resolution of the imaging system, but also by using beam forming techniques in such arrays; the possibility to generate 3-dimensional images.

1.6.2 Developments in Ultrasound Imaging

As discussed in the previous section, CMUTs possess several advantages that can help achieve many new possibilities with ultrasound imaging. Besides other areas, medical diagnostic imaging will benefit a lot from the CMUT technology. The ability to use CMUTs also in immersed media means that CMUT based systems can also be incorporated in catheter based intravenous medical diagnostic systems. Due to the possibility of fabricating dense arrays of CMUT elements, one could actually have many such elements on the catheter to be able to image a multi-dimensional intravenous view. Such a system can be instrumental in an early diagnosis of certain heart diseases.

The operating concept behind such a system is depicted in Fig. 1.4, from the SMiDA (Smart Microsystems for Diagnostic Imaging in Medicine) project [SMi] at NTNU.

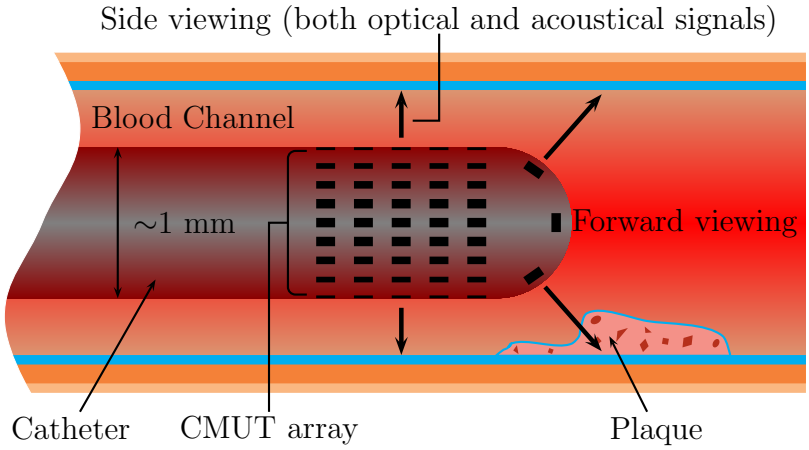

Figure 1.4: A CMUT based intravenous ultrasound imaging [SMi].

SMiDA project has a goal to design and build a catheter based ultrasound imaging system that helps to identify early symptoms of sudden heart attacks. It is estimated that more than 80% of sudden heart attacks are caused by the rupture of vulnerable plaques leading to the formation of blood clots and subsequent coronary stenosis and infarction. Such a system would not only allow imaging inside the blood channels to trace the plaque buildup, but also help in differentiating the stable plaque from the unstable (malignant) plaque that is one of the main causes of sudden heart attacks.

1.6.3 CMUT Operation

Fig. 1.5 shows the cross-section of a typical CMUT connected in *actuation* configuration. The CMUT structure consists of a highly doped silicon substrate that forms the bottom electrode, and an aluminum film on top of a micromachined silicon nitride membrane forming the top electrode of the CMUT capacitor.

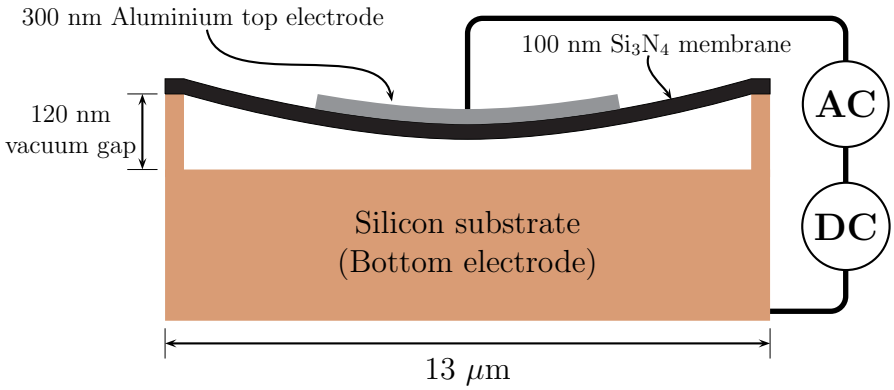

Figure 1.5: A typical CMUT cross-section [MAER07]. The disproportional scale for different shapes in the figure is intentional.

When a DC potential is applied between the two electrodes, the membrane *bows* towards the bottom electrode due to the electrostatic force. The membrane can be made to oscillate by superimposing a suitable AC signal over this DC bias, as shown in Fig. 1.5. The CMUT in this condition is said to be in the *transmit* mode, i.e., sending out acoustic signals. The second mode of operation of a CMUT is the *receive* mode. In this mode the AC signal source is replaced[2] by a capacitive sense circuit. When the reflected

[2]Using switches: not shown in Fig. 1.5

acoustic waves hit the biased CMUT membrane, they generate variations in the capacitance of the CMUT that are detected by the sensing circuit. This capacitance sensing circuit, or an *interface* circuit is usually *analog*. The output of this interface circuit, if suitable, may directly become an input to a digital signal processing circuit.

1.6.4 Interface Circuits for CMUTs

A CMUT interface circuit has to detect the variations in capacitance generated by the acoustic waves impeding on the membrane. For a large array of CMUTs, each element might require its own interface circuit. Although, after the processed signals are digitized, many or all of the outputs may be combined and transmitted together. To be able to achieve a high density of CMUT elements, especially in catheter based systems, the interface circuits should be really compact. For example, the system shown in Fig. 1.4 has a catheter diameter of the order of 1 mm. This means that all the signal processing functions discussed before must be implemented in such a limited space. Another aspect which is important for medical imaging systems is the *power dissipation*. The system must not dissipate more power than a specific limit – this is dictated by the safety requirements for medical imaging systems. Depending on the density of components, this power budget may divide down to a small number when it comes to the power dissipation per unit. Hence, the circuits used in such an application should not only be very compact, but also low-power, or power *efficient*. Power efficiency for such systems might be another way of describing the importance of achieving a certain desired degree of performance per unit die area and power consumed by the circuit.

There are fundamentally three ways to implement the interface circuit for capacitive sensors. Since most common signal processing function performed by the interface circuit is amplification, we list three kind of amplification approaches that are possible to implement for a capacitive sensor [Bax96]:

1. High input impedance (High-Z) sensing.
2. Low input impedance (Low-Z) sensing.
3. Feedback assisted sensing.

Fig. 1.6 shows the equivalent circuits suitable for explaining the sensing as performed by the high-Z and low-Z amplifiers. The high-Z sensing (or *voltage* sensing) can be best explained by the *Norton* equivalent of the system, as shown in Fig. 1.6 (a). The output signal is a voltage (v_{sig}) that is

generated across the sensor. This type of sensing is typically sensitive to the parasitic impedance between the output node and ground. The low-Z (or *current* sensing in continuous domain) can be best explained with the help of a *Thévenin* equivalent of the system, as shown in Fig. 1.6 (b). The output signal is a short circuit current (i_{sig}) that flows into the low-Z amplifier. This type of sensing is ideally insensitive to the parallel parasitic impedance at the sensor output.

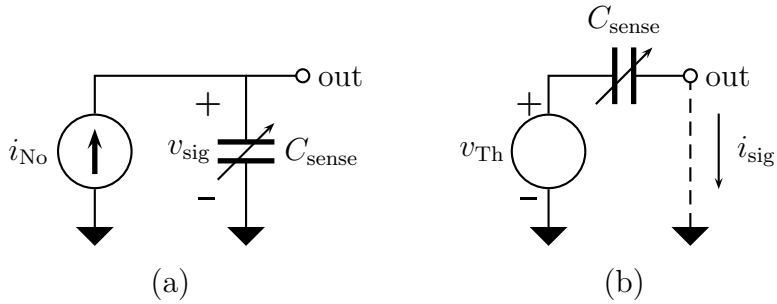

Figure 1.6: Equivalent circuits for (a) High-Z sensing, and (b) Low-Z sensing.

Feedback assisted sensing consists of a feedback amplifier that controls the excitation to the sensor element. Such an approach may help in reducing the sensitivity to stray capacitance and improving the output linearity. Such a system, besides typically requiring a very high gain amplification in the feedback loop, may be more complex than the simple high-Z or low-Z sensing schemes.

Majority of literature on CMUT interface circuits reports the use of low-Z amplifiers as signal conditioning elements. The most used topology is TIA based [NDK$^+$02, GB06, WYZ$^+$05], but charge based sensing is also reported [PQB$^+$06, CY07]. As a comparison, the voltage amplifier based sensing schemes are relatively few. In [CCS$^+$04], a simple comparison has been made between a voltage amplifier based sensing and a TIA based sensing. The authors of [CCS$^+$04] foresee that the voltage amplifier based sensing can be a better option than the TIA at higher frequencies. Both the voltage amplifier and the TIA considered in the article are opamp based, which is just one of the many topologies possible to realize the respective sensing types. Therefore, such a comparison is hard to use as a rule of thumb in all situations. In any case, the voltage sensing approach can be worth exploring and comparing with the other topologies due to a relatively small amount of literature available in this context. This can be especially interesting

because CMUTs, unlike other ultrasound transducers, can be optimized for a specific application. Voltage amplification approach in CMOS does have advantages of its own, such as:

- It is simple to implement because,
  - a MOSFET already has a high input impedance and,
  - CMOS voltage amplifiers are vastly covered in literature.
- It is possible to achieve high efficiency.

For example, the common-source (CS) amplifier is not only very simple to realize, but it is also one of the most efficient stages in CMOS technology [Nor00]. It is possible to realize a CS amplifier within very small area, and *cascading* can always be used to get a higher system gain even if conventional *cascoding* might not be feasible due to headroom issues.

1.7 Conclusion to the Chapter

Sensor systems technology is growing steadily due to an ever increasing use of sensors in our day-to-day life. Among the measurement principles for sensing, capacitive sensing has found widespread application in modern sensors and devices due to its inherent advantages. One such application is in the CMUT based ultrasound imaging field that promises to replace the conventionally used piezoelectric transducers. Many improvements and innovations in medical diagnostic imaging are in sight as the CMUT technology matures at a fast pace. One of these applications is intravenous imaging for early diagnosis of specific heart conditions. Due to very limited area and power budgets, compact and efficient analog interface circuits are required for such applications. Voltage amplifier based sensing may be a promising candidate for achieving this, however, very little relevant literature can be found in this context. Hence, it can be interesting to design and implement a CMUT imaging system based on voltage sensing and compare it with the widely covered low-Z interfacing options.

Chapter 2

Research Overview

This chapter presents an overview of the contributions in the included research articles and their respective errata. Although the content of the attached articles is the same as the published/submitted versions, they have been reformatted according to this thesis. The bibliography of each article is merged in the main bibliography in the end of this thesis. The section numbers are also changed to match the style of the thesis.

2.1 Summary of Contributions

Paper [1]: *A Single-Ended to Differential Capacitive Sensor Interface Circuit Designed in CMOS Technology*

This paper presented the first simulated version of the interface concept of Prototype 1 that is characterized in Paper [4]. A simple circuit realization and its simulation results using Austria Microsystems' 0.8-μm CMOS process were presented.

Comments and errata: Equation 4.7 is not an accurate expression, it actually shows a very simple expression for the output referred noise power spectral density. A number of assumptions have been made to reach this expression such as, OTA with an ideal transfer function (although not noise-free), simplifications in node impedances – only dominating impedance is considered.

There is an error in the realization of the first-stage of the fully-differential OTA as shown in Fig. 4.5. The active-load transistor M3 is diode-coupled. In normal case this could cause large distortion because the gain of the two output paths could be appreciably different

especially at large-signals. But, no noticeable affect was observed during the measurements (Paper [4]) probably due to small output swing of the circuit.

Paper [2]: *A Linear Capacitive Sensor Interface Circuit with Single-Ended to Differential Output Capability*

An alternative approach of obtaining a linear output from a capacitive sensor was presented. This circuit can also generate a differential signal from a single-ended sensor although, the differential conversion in this case is somewhat pseudo-differential, unlike the differential signal generation in Papers [1, 4]. But, this approach is also parasitic insensitive as compared to that in Papers [1, 4]. The fundamental difference between the two approaches is that in this case a voltage ramp generator is used instead of a DC current source, due to which the signal current generated in the measuring and reference capacitors is independent of the parasitic capacitance at the common node. The currents generated in the measuring and the reference capacitors are compared with a fully-differential TIA to generate a differential output. The output transfer function is also simple and linear in this case. The circuit was simulated with Eldo® macromodels [Men07].

Comments and errata: Equation 5.20 is a simplified expression for the power spectral density that may be used to calculate the RMS output noise of the circuit. The expression, as such, is not an expression for the RMS output noise – as mistakenly implied in the introductory sentence. The simplifications used to reach this expression are similar to those used in Paper [1].

Paper [3]: *Common Source Amplifier with Feedback Biasing in 90nm CMOS*

It was shown in this paper that the circuits in nanoscale technologies can benefit from the simplicity of feedback biasing. Non-proportional scaling of MOSFET threshold voltage in CMOS technologies (see, for instance, Fig. 9. in [CC02]) is the main factor that actually creates a benefit in this case. Due to non-proportional scaling of the threshold voltage with respect to the power supply voltage in CMOS technology generations, the gate overdrive voltage at V_{GS} close to mid-supply voltage eventually ends up low enough such that it is no longer a limitation to use feedback biasing. In earlier technology generations, this high gate overdrive voltage value was reflected as a severe limitation to the output swing of such circuits. A 100-MHz CMUT device was taken as a test case for this amplifier. Amplifier specifications were decided

based on the requirements of the SMiDA project. Headroom limitations in 90-nm technology meant that stacking of devices (cascoding) was not feasible. Hence, a cascaded CS topology was selected. The prototypes of this amplifier were fabricated in ST Microelectronic's 90-nm CMOS process. The chip was called *Alabama* and it was used as a trial IC for testing the new process.

Comments and errata: In Figs. 6.4 and 6.5, the transistors M2, M2a and M2b are mistakenly drawn as NMOS devices. They should be read as PMOS devices as the device M2 shown in Fig. 6.3 (a). The correct devices were used in the EDA tools and in all the simulations.

Paper [4]: *Current Mode Capacitive Sensor Interface Circuit with Single-Ended to Differential Output Capability*

This paper presented the measurement results of Prototype 1. The original concept was first presented by the authors in Paper [1]. The main highlight of the circuit, differential output generation even from a single-ended capacitive sensor, can be a significant advantage when using this in applications where a more expensive differential sensor element is not available. The circuit does require a fixed reference capacitor, which ideally should be similar to the sensor element. However, since capacitors are relatively stable with respect to varying operating conditions such as temperature, an on-chip reference capacitor should also be fine. Prototypes were fabricated in Austria Microsystems' 0.8-μm CMOS process. There are minor changes that were made in the prototype design as compared to the circuit presented in Paper [1], for example removal of the common-mode current subtraction at the inputs of the differential OTA. On-chip capacitor bank was used to generate capacitance changes. The measurement concept may be realized as different circuit realizations. Only one simple transimpedance amplifier (TIA) based realization was presented with the measurement results as a proof-of-concept for this method. The circuit demonstrated better accuracy performance than that presented in [Pen05]. The presented method can, therefore, be a cheap and straightforward way to implement an interface circuit with differential output in applications where very high accuracy is not required.

Paper [5]: *Feedback Biasing in Nanoscale CMOS Technologies*

Measurement results of the feedback-biased CS-amplifiers were presented in this paper. The measurements did not show any detrimental effect of placing the coupling capacitor above the circuit. Therefore,

the *oncap* design did benefit from this because the capacitor sat perfectly on top of the amplifier layout without consuming any additional area. The whole *oncap* amplifier measured just 20 μm $\times$ 10 μm including the current mirror transistors for biasing. The *farcap* amplifier measured 20 μm $\times$ 18 μm due to additional area taken by the coupling capacitor. Due to an extremely compact form factor of these amplifiers, they are potential contenders for applications requiring small and efficient interface circuits, for example, catheter based CMUT imaging systems.

Paper [6]: *Compensating for Non-linearity in Feedback biased Common-Source Amplifiers Using MOS feedback resistors*

This paper features a possible solution to compensate for the non-linearity due to sub-threshold MOSFETs as feedback resistors in feedback biased CS amplifiers. Sub-threshold MOSFETs demonstrate a very high incremental resistance value. Therefore, by using these devices as feedback resistors, appreciable silicon area can be saved. However, this resistance value is very non-linear with respect to voltage. Even though the passband gain of a feedback biased CS amplifier may not be directly dependent on the feedback resistance value (see Paper [5] for analysis), the behavior of the sub-threshold MOSFET resistor can still have a severe affect on the linearity performance of the amplifier. This has been identified to be the asymmetric charging/discharging of the input capacitance of the amplifier, which shifts the DC operating point of the amplifier. This paper shows that most of the linearity performance of the amplifier can be recovered by simply adding another MOSFET to the circuit that facilitates the recovery of input node of the amplifier. All this is achieved with a minimal area overhead, while still preserving the compactness of the amplifier.

2.2 Clarification to Contributions

All papers included in this thesis are co-authored by my main supervisor Prof. Trond Ytterdal who helped me with his valuable guidance, support and resources used to perform the design and experiments. My second supervisor Prof. Trond Sæther is also the co-author of the included papers, except Paper [1]. The discussions with him were instrumental in planning the design strategy and as a quality check of the results and the articles.

Chapter 3

Chip Photographs

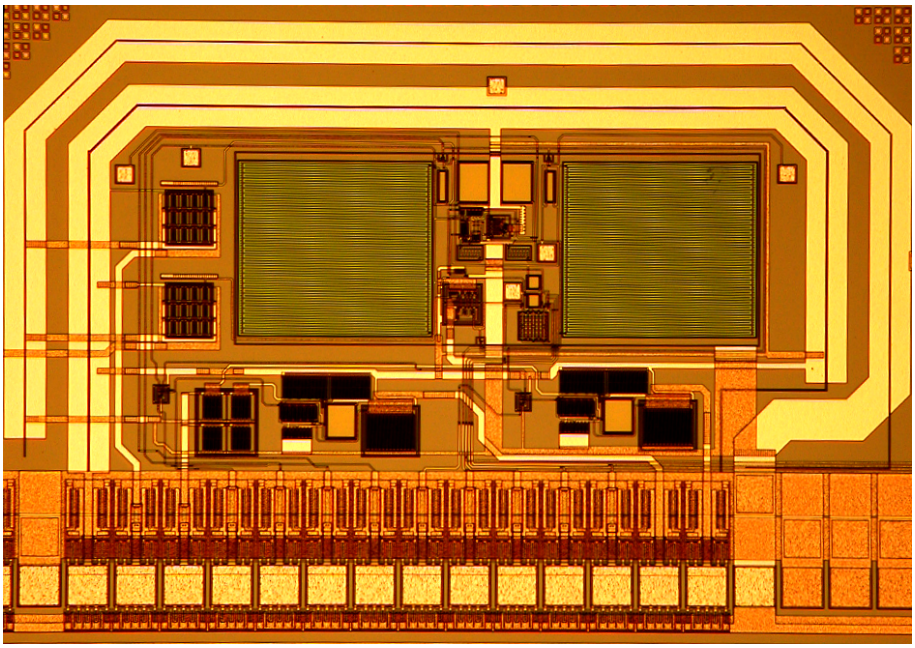

Figure 3.1: *Prototype 1*: Current-mode capacitive sensor interface with single-ended to differential output capability. The chip is fabricated in Austria Microsystems' 0.8-μm CMOS technology.

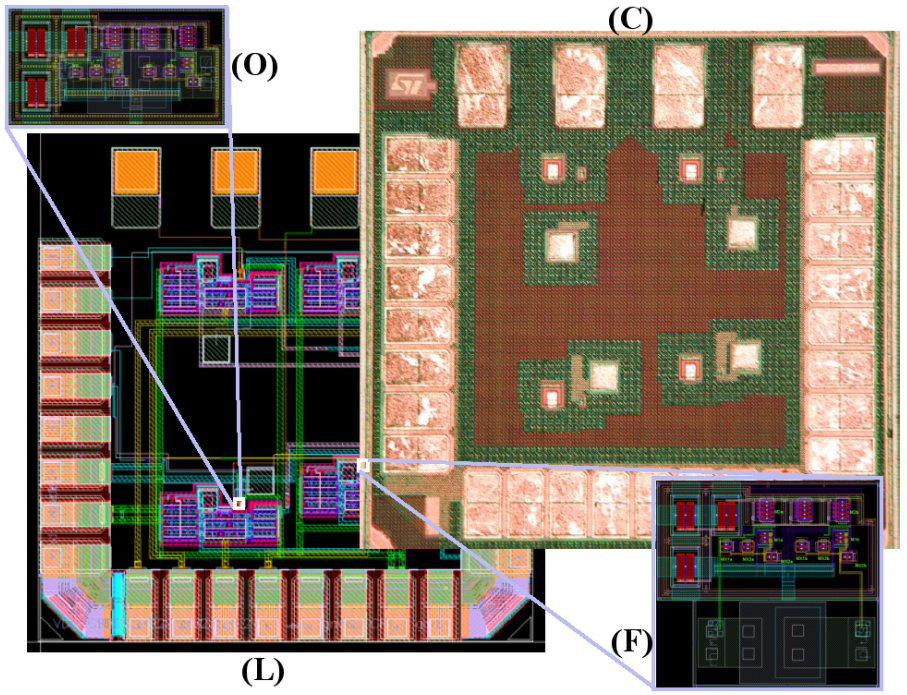

Figure 3.2: *Bombay*: Prototype chip **(C)** and layout plot **(L)** containing 4 two-stage CS amplifiers in 2 versions, **(F)** *farcap* with a coupling capacitor placed *away* from the circuit (20 μm $\times$ 18 μm), **(O)** *oncap* with the coupling capacitor placed *above* the circuit (20 μm $\times$ 10 μm). The chip is fabricated in ST Microelectronic's 90-nm CMOS technology and measures less than 1 mm $\times$ 1 mm.

Chapter 4

Paper 1

A single-ended to differential capacitive sensor interface circuit designed in CMOS technology

Tajeshwar Singh and Trond Ytterdal
In proceedings of:
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Abstract

In this paper, we present a single-ended to differential capacitive sensor interface circuit suitable for implementation in CMOS. The interface circuit converts the capacitance change of a single sensor capacitor into a differential output voltage. The circuit has been designed in a 0.8 μm CMOS technology.

4.1 Introduction

Most of the sensor interface circuits used for capacitance detection exploit the symmetry of complementary capacitances, wherein two capacitors of equal nominal value are used (see, for example [TS03][YNS03][MMW98]). The change in the measured physical parameter results in positive change in the capacitance of one capacitor and negative change in capacitance of the other capacitor. Such capacitance detection circuits offer a variety of advantages, which can be attributed to the differential scheme. However, in

many sensor systems, such a sensor with complementary capacitances might not be available.

An alternative is to use a single measuring capacitance which changes with the variation in the detected parameter. The sensed signal is compared with a reference capacitance, which is normally equal to the nominal value of the measuring capacitance. Such schemes are primarily based on comparison methods (see, for example [ALB01][IMN02]). Besides, these techniques may require many digital blocks such as microcontroller, high-speed counter, and multiplexer for achieving the final measurement. Although compensation is provided by alternatively measuring each capacitance, the real 'fully-differential' concept is missing.

We were hence looking for a circuit that, in addition to being suitable for integration, could convert from a single-ended to differential signal representation. In this paper, we present such a circuit. To our knowledge the circuit presented here has not been previously published in the open literature. This new technique overcomes the limitations mentioned above, and provides an alternative approach to achieve a fully-differential output from a single-ended sensor. The main objective of this paper is to illustrate the principle of operation of the new circuit.

4.2 The Interface Circuit

The concept of our single-ended to differential interface circuit is based on the simple equation for the current in a capacitor.

$$I = C\frac{\mathrm{d}V}{\mathrm{d}t} \tag{4.1}$$

Consider the circuit in Fig. 4.1. Here C_m and C_r represent the sensing and reference capacitors, respectively. The current source I_b is the bias current for charging the capacitors. Throughout this work the bias currents are DC currents.

Nominally, $C_m = C_r$ and $I_1 = I_2$. However, if C_m increases with respect to C_r, I_1 will increase and I_2 will decrease. The difference of the two currents is the signal current, which we will denote as i throughout this work.

We can write the following equations for the currents through the two capacitors in this circuit:

$$I_1 = C_m\frac{\mathrm{d}V_1}{\mathrm{d}t} = \frac{I_b}{2} + \frac{i}{2} \tag{4.2}$$

and

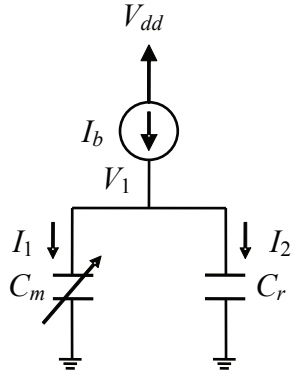

Figure 4.1: Schematic of the proposed interface circuit.

$$I_2 = C_r \frac{\mathrm{d}V_1}{\mathrm{d}t} = \frac{I_b}{2} - \frac{i}{2} \tag{4.3}$$

Since I_b is a DC current, we have:

$$\frac{\mathrm{d}V_1}{\mathrm{d}t} = \frac{I_b}{C_m + C_r} \tag{4.4}$$

If we assume that the two capacitors can be matched, and choose a unit capacitance equal to C, we can write $C_m = (C + \Delta C)$ and $C_r = C$, where ΔC is the capacitance change of the sensing capacitor around its nominal value of C.

By combining equations (4.2)–(4.4) and using the assumptions above, we get the following expression for the difference $I_1 - I_2$, which is the signal current i:

$$i = \frac{I_b \Delta C}{2C + \Delta C} \tag{4.5}$$

The differential nature of the signal current is clearly apparent in equations (4.2) and (4.3). We can see from (4.5) that the signal current is independent of time as long as we assume that I_b and ΔC are time invariant. Also note that in addition to the linear term in ΔC we have a non-linear term caused by ΔC also appearing in the denominator. Such non-linearity is not very uncommon in sensor systems. It is quite usual to remove it by simple digital calibration circuitry [vdHH97].

To measure the differential signal current i, we replace the ground terminal in Fig. 4.1 with two virtual ground terminals implemented by a fully

differential transimpedance amplifier that converts the differential input current to a differential output voltage. The complete circuit is shown in Fig. 4.2.

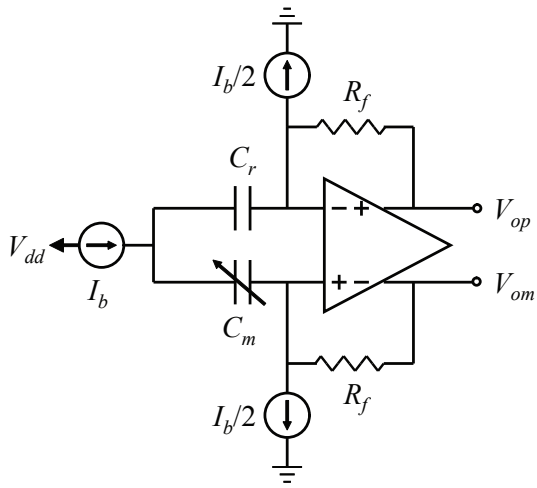

Figure 4.2: The complete interface circuit using a transimpedance amplifier.

The advantage of this circuit is that the main topology is maintained and the signal current is measured differentially to create a differential output voltage. The voltage at the bottom plates of the measurement capacitance and the reference capacitance is maintained at the common-mode voltage by the feedback loop.

The purpose of the current sources connected to the input terminals of the amplifier is to subtract the bias current from the total current such that only the signal current i is fed to the transimpedance stage. Hence, the differential output voltage is given as

$$V_{out} = V_{op} - V_{om} = iR_f = R_f I_b \frac{\Delta C}{2C + \Delta C} \tag{4.6}$$

where R_f is the feedback resistor of the transimpedance amplifier.

Here, we should mention that the capacitors are discharged during a reset phase (switches not shown) to prepare for the next measurement cycle.

In Fig. 4.3, we have plotted the ideal output voltage V_{out} versus the change in the sensor capacitance ΔC according to (4.6).

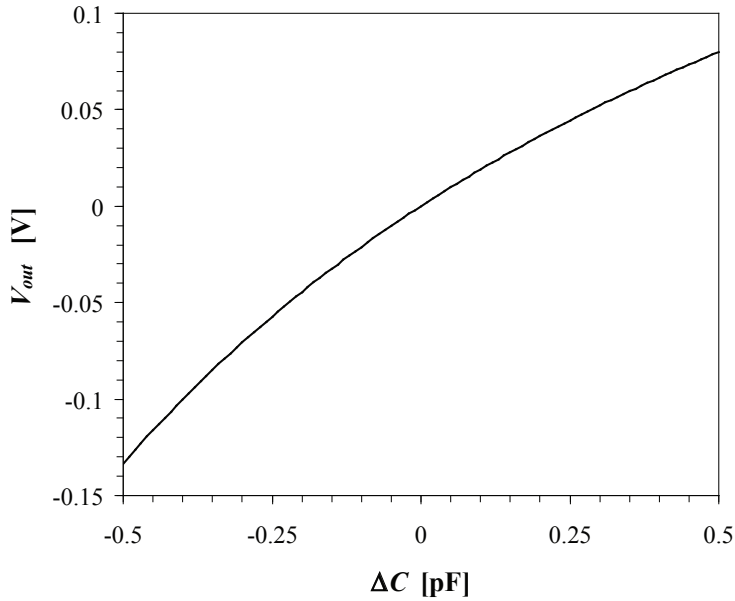

Figure 4.3: Plot of the transfer function in equation (4.6). Parameter values were $R_f = 200$ kΩ, $I_b = 2$ μA, and $C = 1$ pF.

4.3 CMOS Design

The interface circuit has been designed in a 0.8-μm CMOS process. The schematics of the interface circuit and the amplifier are shown in Figs. 4.4 and 4.5, respectively.

The transimpedance amplifier was realized using a fully differential Miller OTA. The current mirrors on the top (M21-M29), supplying the charging current to the capacitors are realized using enhanced output impedance wide-swing current mirrors to achieve the high output impedance needed in order to ensure that the charging current remains relatively constant irrespective of rising drain voltage of the current mirror transistors as the voltage across the capacitors increases. Since the voltage at the inputs of the transimpedance amplifier does not change, simple current mirrors (M34-M35) are sufficient here.

The capacitors are discharged every 2 μs. This ensures that the current mirror transistors remain in saturation. Four NMOS switches were used, one across each capacitor (not shown). The output voltage can be sampled at the end of each 2 μs cycle.

Since we target the interface circuit for low-power applications, a low

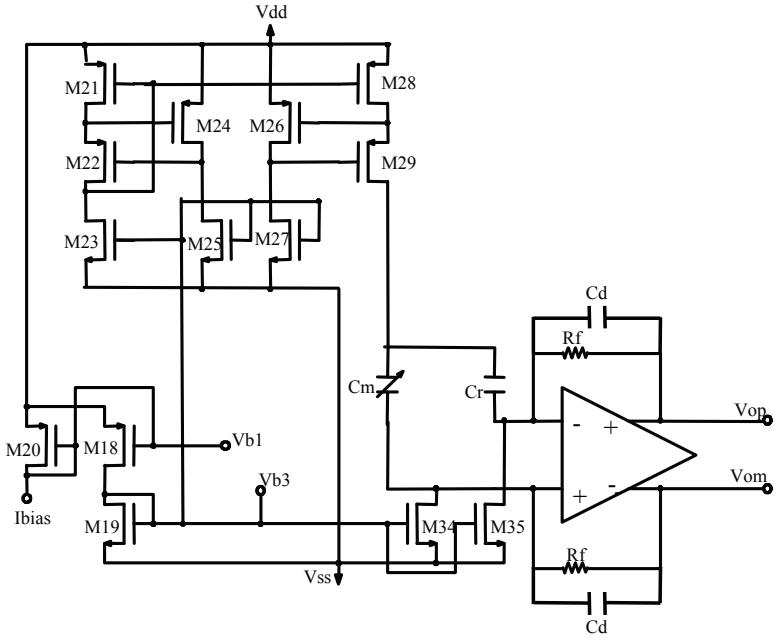

Figure 4.4: Schematic of the CMOS interface circuit (switches not shown). Notice the inclusion of the feedback capacitors C_d to damp the response of the system [HP98]. High frequency noise is also effectively bypassed directly to the output.

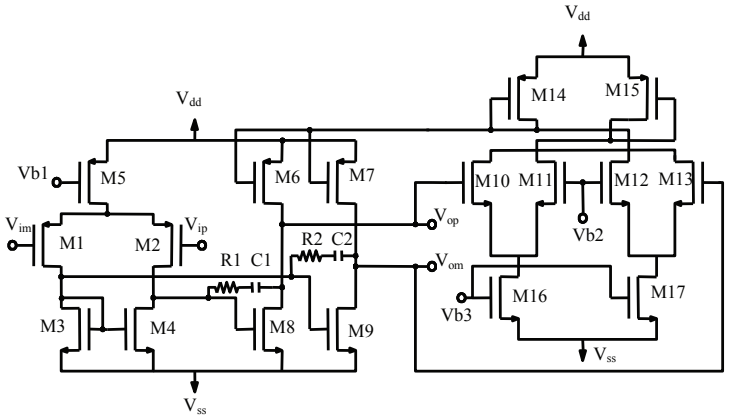

Figure 4.5: Schematic showing the fully differential Miller OTA used for in the interface circuit of Fig. 4.4. Common mode feedback circuit is also shown. The common mode voltage is set by Vb2, which was set to 1.26 V.

value of charging currents was chosen, only a few microamperes. This is an advantage when the supply voltage is scaled down. However, the tradeoff is increased noise. To study the noise properties of the interface circuit, a noise model was constructed as shown in Fig. 4.6. Based on this model the expression for the total output referred noise voltage squared at low frequencies is derived as:

$$V_{no}^2 = R_f^2(I_{n1}^2 + I_{n2}^2 + A^2 I_{n3}^2 + I_{n4}^2 + I_{n5}^2) + E_{n1}^2 + E_{n2}^2 + E_{n6}^2 + E_{n7}^2$$
$$A = \frac{C_m - C_r}{C_m + C_r} \tag{4.7}$$

In our design, we use the following values: $C_r = C_m = 1$ pF and $R_f = 200$ kΩ. We note from (4.7) that the noise currents are multiplied with the feedback resistor R_f, which indicates that these sources could dominate the total noise.

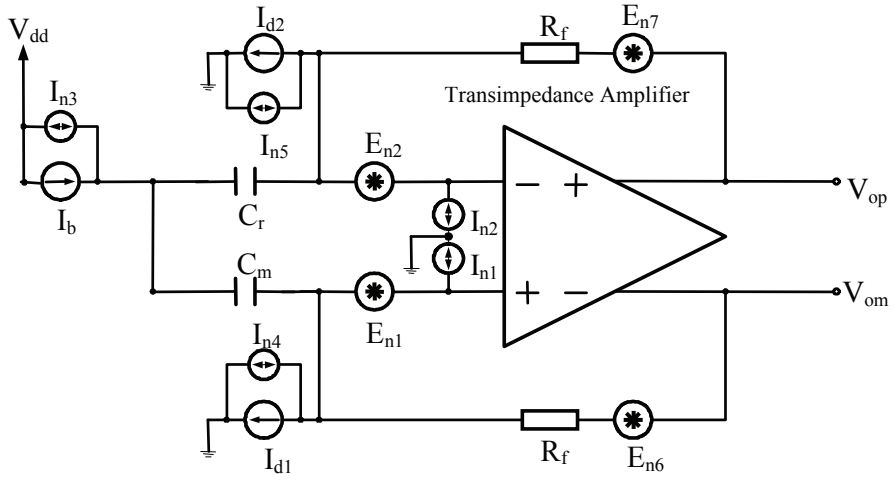

Figure 4.6: Schematic showing the noise sources.

4.4 Simulation Results and Discussions

All simulations were performed with Eldo from Mentor Graphics using AMS 0.8-μm CMOS device models. Supply voltages V_{dd} and V_{ss} were 5 V and

0 V, respectively. Furthermore, the nominal charging current was around 2.5 μA. Note that it is not important to set the charging current to a specific value as long as it is stable over time because the system can be calibrated easily. However care should be taken that the reset time is appropriate for not letting the current-mirror transistors to enter the linear region.

As discussed in the previous section the noise current sources get multiplied with a large factor which indicate that they could dominate. Noise simulations in Eldo confirmed this observation. The command .OPTNOISE in Eldo was used which sorts the noise sources based on their rank in contribution to the total noise. The simulation results indicate that current mirrors M34 & M35 have the highest contribution to the total noise, followed by the output stage transistors of the transimpedance amplifier (M6-M9).

Several simulation iterations were performed with different values of charging currents. The results are summarized in Table 4.1.

Table 4.1: Summary of results

Maximum output swing	118.5 mV
RMS output noise voltage relative to full scale	0.28%
Maximum static error in the output voltage (caused by mismatch and finite output resistance of the current mirrors)	0.026%
Total current consumption	125 μA

As we observe from the table, noise dominates the error in the output voltage and has to be reduced by optimizing the circuit for low noise. However, as stated in the introduction, the main objective of this paper is to illustrate the principle of operation of the interface circuit. Optimizing the noise performance will be addressed in future work. Other areas for further work include: Studying the effects of charge injection for resetting the capacitances, parasitics, increasing the output swing and researching schemes for increasing SNR by clever biasing and over-sampling techniques.

Also, it should be mentioned that a very basic transimpedance amplifier was designed and one can also see the peak in the frequency response plot due to input capacitance and resistance [HP98], which results in ringing in the transient response. The inclusion of feedback capacitors Cd (see Fig. 4.4) improves the transient response and lowers the noise by shunting R_f at high frequencies.

The optimized circuit will be fabricated in an AMS 0.8-μm CMOS technology and characterized.

4.5 Conclusions

We have presented a single-ended to differential capacitive sensor interface circuit which has been designed in a 0.8-μm CMOS technology. The interface circuit converts the capacitance change of a single sensor capacitor into a differential output voltage. The circuit was analyzed mathematically and the expressions validated by simulations. Non-linearity is a drawback of this approach, however it can be calibrated and the output can be linearized, as commonly done in sensor systems [vdHH97]. The noise currently limits the accuracy of the designed CMOS circuit and further work is needed to optimize the noise properties.

4.6 Acknowledgements

This work has been funded by the Norwegian Research Council through the project ASICs for Microsystems (project number 133952/420).

Chapter 5

Paper 2

A linear capacitive sensor interface circuit with single-ended to differential output capability

Tajeshwar Singh, Trond Sæther and Trond Ytterdal
In proceedings of:
The NORCHIP Conference *2004*.
8-9 Nov. 2004, Page(s):32–35
Digital Object Identifier 10.1109/NORCHP.2004.1423815

Abstract

In this paper, we present a concept for single-ended to differential capacitive sensor interface circuit suitable for implementation in CMOS. The interface circuit converts the capacitance change of a single sensor capacitor into a differential output voltage. The main advantages of the proposed circuit are high linearity, immunity from parasitic capacitances of the sensor capacitor, and sensitivity to the capacitance change rather than the absolute capacitance.

5.1 Introduction

Capacitance based techniques for sensors offer numerous advantages especially for low-power operation. Capacitive sensor elements do not require DC biasing currents. Hence, reduced power consumption is usually achieved compared to piezo-resistive sensors. As the miniaturization in sensors and electronics continues and the size of the sensing and parasitic capacitances

becomes comparable, the issue of parasitics becomes more and more important. The concept we present here shows one way of reducing the influence of sensor parasitics while measuring small capacitances.

The core concept was presented in [1]. The circuit presented here tries to minimize the influence of parasitics by using a modified technique compared to the circuit presented in [1].

High linearity is a desired feature for a measurement system, as it simplifies the signal conditioning and calibration requirements. The proposed circuit achieves this feature. Another advantage of the proposed circuit is its sensitivity to the capacitance change rather than the absolute value of the sensing capacitor by just using a single reference capacitor matching the nominal value of the sensing capacitor. This also takes care of the common mode effects in the two capacitors.

This paper is divided in 9 sections with introduction to the interface concept in Section 5.2, followed by the modified method in Section 5.3. Section 5.4 discusses an approach of realizing the interface. Section 5.5 analyses important error sources followed by simulations and results in Section 5.6. We conclude the paper with a short summary in Section 5.7.

5.2 The Interface Concept

The concept presented in [1] is based on (5.1) and the circuit shown in Fig. 5.1 (a), where the signal current is defined as the difference between I_1 and I_2.

$$I = C \cdot \frac{\mathrm{d}(V_1 - V_2)}{\mathrm{d}t} \tag{5.1}$$

As shown in [1], using a current source I_b to charge the capacitors, the expression for the signal current i becomes

$$i = \frac{I_b \cdot \Delta C}{2 \cdot C + \Delta C} \tag{5.2}$$

This signal current can be used to generate a differential output voltage by a fully-differential transimpedance amplifier [1].

However this circuit poses two important challenges. The first one is due to parasitics and the second is due to the inherent non-linearity in (5.2).

From Fig. 5.2 we notice that the parasitic capacitance C_p at node V_1 appears in parallel with the sensing and the reference capacitances. Hence, it will also draw some charging current from the current source I_b. As seen from (5.2), it introduces an error in the signal current. Further, as these

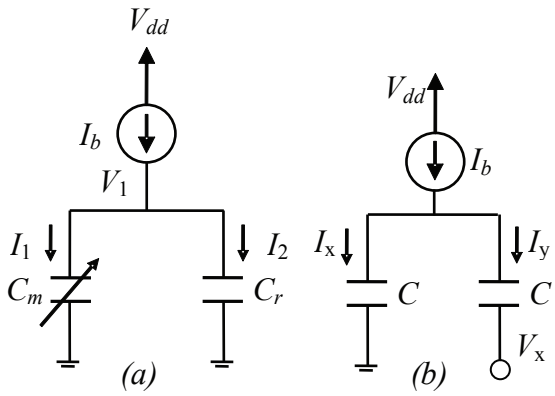

Figure 5.1: (a) The Concept. (b) $I_x = I_y$ for V_x being a constant DC voltage.

parasitics are voltage dependent, the induced error is dependent on the node voltage V_1, hence dependent of C_m, which makes it difficult to predict and calibrate.

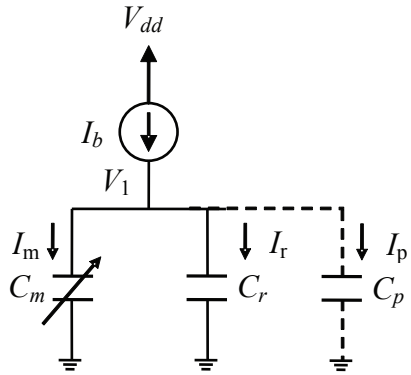

Figure 5.2: Influence of a parasitic capacitance at the V_1 node.

5.3 The Ramp Based Approach

To remove the sensitivity to parasitics in the transfer function, we replace the current source in Fig. 5.2 by a voltage ramp generator V. Similar circuit operation is achieved, at the same time taking care of the parasitics at the node V_1, see Fig. 5.3.

The voltage at node V_1 is generated according to:

$$V_1 = a \cdot t \tag{5.3}$$

where, a is the slope of the ramp and t is time.

By having a constant linear slope at the node V_1, the charging current in the respective capacitors can be written as:

$$I_m = C_m \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} = C_m \cdot a \tag{5.4}$$

$$I_r = C_r \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} = C_r \cdot a \tag{5.5}$$

$$I_p = C_p \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} = C_p \cdot a \tag{5.6}$$

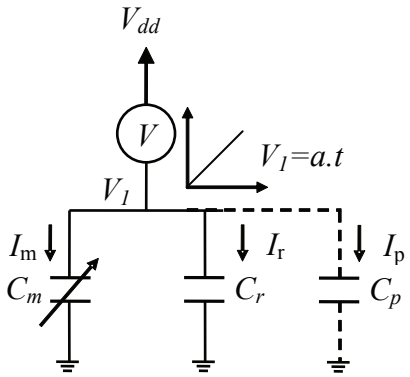

Figure 5.3: Voltage based approach.

Note that as long as the ramp generator can satisfy the simple requirement of supplying charging currents to C_m, C_r and C_p without affecting the linearity of the ramp, the respective charging currents in C_m and C_r remain independent of C_p.

Considering (5.4) and (5.5) and $C_m = (C + \Delta C)$ and $C_r = C$, where ΔC is the change in the sensing capacitor, we can write:

$$I_m = I + i = (C + \Delta C) \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} \tag{5.7}$$

$$I_r = I = C \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} \tag{5.8}$$

Subtracting (5.8) from (5.7), we get:

$$i = \Delta C \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} = a \cdot \Delta C \tag{5.9}$$

Note that the expression for the signal current i generated by the ramp based approach, given by (5.9), is linear in contrast to the expression for the signal current in the current based approach given by (5.2). However this is achieved at the cost of increasing the circuit complexity, and the requirement of having a linear ramp generator.

5.4 Realization

Fig. 5.4 presents one method of realizing the measurement setup based on the concept described in the previous section.

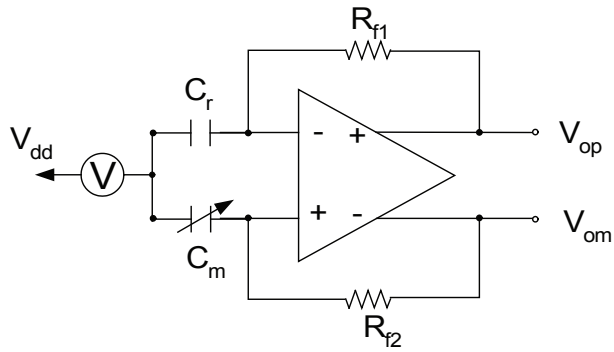

Figure 5.4: Circuit realization using a Transimpedance Amplifier. Note that the Voltage source 'V' is a linear ramp generator. $R_{f1} = R_{f2} = R_f$.

C_m and C_r are connected to the non-inverting and inverting input terminals respectively of the transimpedance amplifier. C_m draws its charging current from node V_1 as described in (5.4) and C_r draws its charging current from node V_1 as described by (5.5). The same currents flows in the respective feedback resistors of the transimpedance amplifier. The output voltage is given by:

$$V_o = V_{op} - V_{om} = (I_+ - I_-) \cdot R_f \tag{5.10}$$

where, $I_+ = I_m$ and $I_- = I_r$, as described in (5.4) and (5.5). Therefore:

$$I_+ - I_- = I_m - I_r = i \tag{5.11}$$

Applying (5.9) and (5.11) to (5.10), we get:

$$V_o = \Delta C \cdot R_f \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} = \Delta C \cdot R_f \cdot a \tag{5.12}$$

As seen from (5.12), the output voltage expression is linear with respect to the change in the sensing capacitance. The requirement on the linearity for the slope $\frac{\mathrm{d}V_1}{\mathrm{d}t}$ is directly set by the linearity requirement of the output signal.

The ramp generator has a direct impact on the accuracy of the proposed circuit. A capacitor charged by a DC current source is the simplest ramp generator. However desired requirements are high linearity. For this, the charged node must be immune to voltage dependant parasitics and the charging current should be constant with respect to rising node voltage. Repeatability and adaptability are additional desirable features which can effectively reduce the calibration requirements. A simple concept for a positive ramp generator is shown in Fig. 5.5

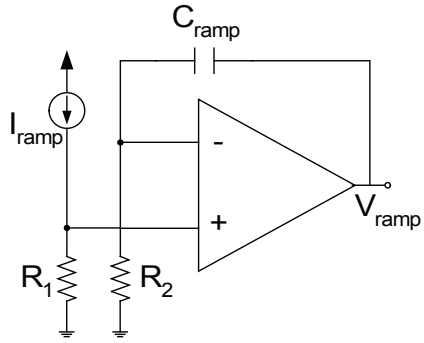

Figure 5.5: A Simple Ramp Generator.

It can be easily shown, assuming a zero offset voltage and high gain that:

$$\frac{\mathrm{d}V_{ramp}}{\mathrm{d}t} = \frac{R_1}{R_2} \cdot \frac{I_{ramp}}{C_{ramp}} \tag{5.13}$$

The attractive feature of this circuit is that the slope is determined by resistance ratio and can be altered by linearly adjusting I_{ramp}.

This ramp generator was used for the simulations of the proposed circuit, using Eldo macro-models for a single pole Opamp.

Another approach planned for the future work is the adaptive ramp generation scheme demonstrated in [BABR02], with some modifications for

high output impedance for the current mirrors (to improve the linearity).

5.5 Error Sources

In this section we discuss some of the most important error sources of the proposed circuit:

Mismatch between feedback resistors:

Refer to Fig. 5.4, if $R_{f1} \neq R_{f2}$ we can write following equations:

$$V_{im} - V_{op} = I_r \cdot R_{f1} \tag{5.14}$$

$$V_{ip} - V_{om} = I_m \cdot R_{f2} \tag{5.15}$$

Assuming zero input offset voltage (due to finite gain of the Opamp), we can subtract (5.14) from (5.15) to get:

$$V_o = V_{op} - V_{om} = I_m \cdot R_{f2} - I_r \cdot R_{f1} \tag{5.16}$$

Since $I_m - I_r = i$, and assuming $R_{f1} = Rf$, $R_{f2} = R_f \pm \Delta R$, such that the mismatch is $R_{f2} - R_{f1} = \pm\Delta R$, we get:

$$V_o = i \cdot (R_f + \Delta R) + I_r \cdot \Delta R \text{ ; for } + \Delta R \tag{5.17}$$

$$V_o = i \cdot R_f - I_r \cdot \Delta R \text{ ; for } - \Delta R \tag{5.18}$$

From (5.17) and (5.18) we note that the mismatch between the feedback resistors adds as a signal independent offset in the output voltage since it is proportional to the current in the reference capacitor. Also, it changes the slope or sensitivity of the output voltage. However, if the slope is stable, this error can easily be removed by a two-point calibration. See for example [vdHH97].

Mismatch between the nominal value of C_m and C_r:

Let us denote the mismatch between the nominal value of C_m and C_r by δC. At zero condition, i.e., when no signal is applied to the sensor and C_m is supposed to be equal C_r, there will be a difference, $|C_{m0} - C_{r0}| = \delta C$. This means that the differential output voltage will not be zero in initial condition. The output voltage can be written as:

$$V_{o0} = \delta C \cdot R_f \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} \tag{5.19}$$

Thus the output voltage will always contain this constant offset. However this error can also easily be removed by calibration of the zero point.

Finite gain of the amplifier:

Finite gain of the amplifier will result in an input offset voltage which can be written as $V_{off} = \frac{1}{A}$, where A is the open loop voltage gain of the Opamp. This expression is true assuming that the offset exists only due to the finite gain and ignoring other factors such as device mismatch. This voltage will be constant and will have an implication that the two capacitors will be connected to slightly different DC potentials. However due to the inherent nature of the capacitor to act as a differentiator for the applied voltage, it does not matter in our case because $\frac{\mathrm{d}V}{\mathrm{d}t}$ is zero as long as V is a constant DC voltage, see Fig. 5.1 (b). In other words, the charging current drawn by the capacitor will be the same whether one of its plates is connected to ground or to any constant DC voltage.

Noise:

Fig. 5.6 shows the noise sources present in the circuit. E_{n1}, E_{n2} and I_{n1}, I_{n2} represent the noise voltages and noise currents respectively associated with the fully differential Opamp. E_{n3} and E_{n4} represent the noise voltages of the respective feedback resistors. E_{n5} represents the noise voltage associated with the ramp generator.

Within the signal bandwidth of interest, the expression for the equivalent RMS output noise voltage can be easily derived as:

$$E_{no}^2 = R_f^2 \cdot \left(\Phi \cdot (E_{n1}^2 + E_{n2}^2) + I_{n1}^2 + I_{n2}^2 + \frac{E_{n3}^2}{R_f^2} + \frac{E_{n4}^2}{R_f^2} + \Psi \cdot E_{n5}^2 \right)$$
$$\Phi = \left(\frac{2 \cdot C_m \cdot C_r}{C_m + C_r} \right)^2 \; ; \; \Psi = (C_m - C_r)^2 \tag{5.20}$$

As seen from (5.20), the amplifier noise currents are dominating the total system output noise since they get multiplied directly by the gain of the transimpedance amplifier.

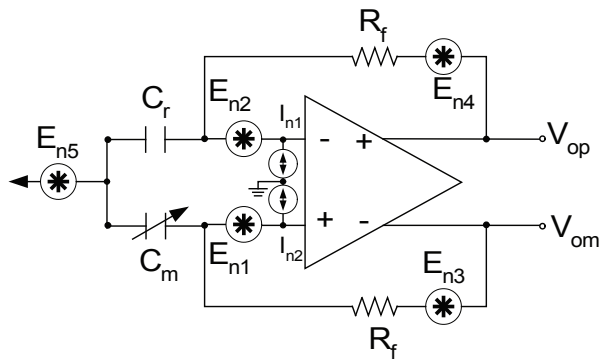

Figure 5.6: Noise model of the proposed circuit.

Output ringing:

Input capacitance of a transimpedance amplifier can result in a lightly damped response [HP98]. This overshoot can be reduced by adding a compensating capacitance in parallel to each R_f. The reduction in bandwidth due to compensating capacitors is not an important issue.

5.6 Simulations & Results

The circuit was simulated using Eldo macro-models of a single pole Opamp with finite gain. The amplifier model was closely matched to the real Opamp used by the authors in [1]. The plots are shown in Fig. 5.7. As seen, the output needs some time to settle. This is due to charging of the capacitors at the input nodes of the amplifier. The output is ready to be read as soon as the input nodes stabilize. The output is sampled 2 μs after the commencement of each ramp.

Following simulations were made with Eldo macro-models and with $C_m + \Delta C_{max}$ = 1 p +0.5 p, C_r = 1 p, R_f = 150 kΩ, compensating capacitors across the feedback resistors R_f, C_c = 0.2 p each:

1. Ideal ramp of slope 1.5 $\frac{\text{V}}{\mu\text{s}}$ applied to the capacitors leads to a maximum error of 0.047% (mainly due to overshoot and ringing in the output). Resulting output swing was 112.5 mV.

2. Ramp generated with the circuit shown in Fig. 5.5 with Opamp open loop gain of 80 dB and a unity gain frequency of 5 MHz confirm maximum non-linearity of 0.74% due to finite gain and bandwidth of the Opamp. Constant gain error with respect to the ideal ramp was nearly

25%. Although this gain error can be easily calibrated because it appears as an offset in the output.

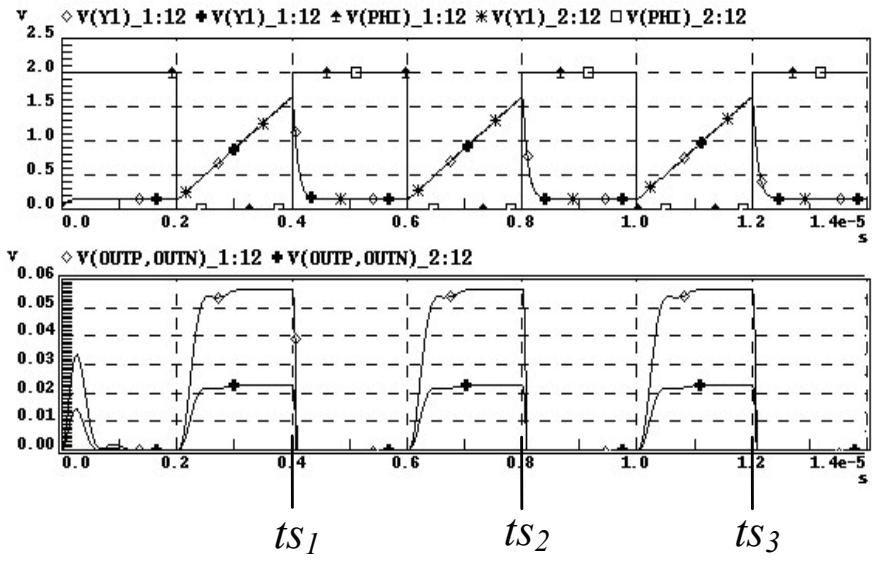

Figure 5.7: Simulated waveforms of the circuit shows: applied ramp V(Y1) (generated by the ramp generator in Fig. 5.5), reset pulse V(PHI), and the differential output V(OUTP,OUTN) for C_m = 1.5 pF and 1.2 pF respectively. The time stamps $ts1$–$ts3$ are sampling points. The output is only shown for positive values; the interface is reset after the sampling point to discharge the compensating capacitors.

5.7 Conclusion

We have presented a parasitic insensitive approach to measure differentially the capacitance change of a single ended sensor. One way of realizing the basic concept (by using a transimpedance amplifier) was also presented. The advantage of this approach is high linearity with respect to the change in capacitance. The circuit will be designed and fabricated in a 0.35 μm CMOS technology. An error analysis for the circuit was also presented. Future work will focus on design of the ramp generator, methods to increase the output swing and minimizing the output overshoot and ringing by design modification.

5.8 Acknowledgement

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Chapter 6

Paper 3

Common source amplifier with feedback biasing in 90nm CMOS

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Abstract

Design of a high-frequency Common Source (CS) amplifier in 90nm CMOS suitable for use with high impedance sources is presented. High impedance sources pose challenges on the biasing of voltage amplifiers where maintaining high input impedance is necessary. To remedy this, a feedback biasing scheme is proposed. The amplifier is developed for a Capacitive Micromachined Ultrasonic Transducer (CMUT) based ultrasound system for intravenous medical imaging with a center-frequency of 100 MHz and 100% bandwidth (passband: 50 MHz–150 MHz). The proposed amplifier achieves a voltage gain of 31.4 dB, and when interfaced with the CMUT: a noise figure of 0.32 dB, an SNR of 35.2 dB, and THD of −35dB, while drawing 460 μA from a 1 V power supply.

6.1 Introduction

Nanoscale CMOS technologies are ideal for applications demanding smaller and faster transistors, or in other words, where very-high frequency operation is required with very small parasitic capacitances. However, scaled down technologies introduce limitations such as low voltage headroom, low output resistance of transistors and low accuracy in terms of matching and noise [ANvLT05]. Thus it becomes difficult to design amplifiers having high enough gain. Also, when using minimum device dimensions various short and narrow-channel effects influence the device characteristics.

In some cases, low accuracy can be tolerated if the source itself is less accurate (noisy). It can thus be advantageous to use simple signal conditioning – to preserve compactness and to obtain low power operation. The issues due to short-channels can actually be exploited as will be discussed later in the paper.

The amplifier presented in this paper interfaces with a CMUT as the signal source. The system considered here is a high-resolution short distance intravenous medical imaging system that is specified in the research project SMiDA [SMi].

CMUTs have recently gained a lot of interest due to numerous advantages as compared to their conventional counterparts: piezo-electric ultrasound transducers. CMUTs can be integrated with electronics on Silicon, and they are compact. A lot of literature is available on CMUT operation and applications (see, for example, [OHB$^+$04][WYZ$^+$05]).

Two common techniques for CMUT read-out are voltage- and current sensing. The advantage of voltage sensing is that simple amplifier circuits can be used, for example the well-known common source amplifier which is one of the most efficient single transistor amplifiers that can be implemented in standard CMOS technology (see, for example,[Nor00]). A drawback with voltage sensing surfaces when the signal source is non-linear. Large voltage swings will excite the nonlinearities and degrade the accuracy of the read-out function. In such cases current sensing may be used to alleviate the problem. The work presented here is based on CMUTs optimized for voltage sensing and the task was to optimize the read-out function using a voltage amplifier.

Our imaging system requires high resolution, on the order of 10 μm. To achieve this, frequencies on the order of 100 MHz are needed. As a consequence, the CMUT elements have to be scaled down to about 10 μm in diameter which causes the magnitude of the impedance to be on the order of 30 kΩ at 100 MHz. When using voltage sensing, the input impedance of the amplifier must be sufficiently higher to cause minimum attenuation of

the CMUT voltage signal at the input of the amplifier. This imposes a great challenge on the amplifier biasing circuitry.

In this paper, we start with discussions on the CMUT parameters and desired amplifier specifications in Section 6.2, amplifier design is covered in Section 6.3, simulation results are presented in Section 6.4, and we conclude this paper in Section 6.5.

6.2 CMUT Parameters and Amplifier Specification

Fig. 6.1 shows the block diagram of the CMUT ultrasound detection system. In this system, different elements are used for transmit and receive. The enclosed area represents the electrical equivalent of the receiver CMUT element linearized around its operating point. Details of the model can be found in [WYZ+05].

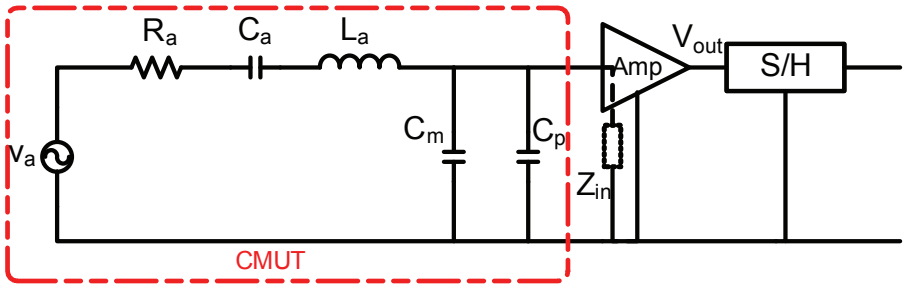

Figure 6.1: Block diagram of a typical CMUT ultrasound detector. Enclosed area represents electrical equivalent of the CMUT element. Signal conditioning amplifier and Sample and Hold block (S/H) is also shown.

Based on the CMUT optimization done for the voltage sensing based system, TABLE 6.1. lists various parameters for the CMUT equivalent circuit shown in Fig. 6.1.

As it can be seen from TABLE 6.1, the CMUT capacitance C_m is half the estimated interconnect parasitic capacitance C_p – this warrants the use of local signal conditioning. Various specifications laid out for the amplifier based on the requirements set by the other signal conditioning blocks are:

1. The amplifier should be designed in a 90-nm CMOS technology with 1.0 V nominal supply voltage.

2. The voltage gain should be around 34 (30.6 dB)) to provide a voltage swing at the output of 0.5 V V_{pp} with a DC level of around 0.5 V -

Table 6.1: CMUT Parameters Optimized for Voltage Sensing

Parameter	Description	Value
f_m	CMUT mechanical resonance frequency	110 MHz
R_a	Acoustic resistance of the resonant circuit	38.58 kΩ
C_a	Acoustic capacitance of the resonant circuit	35 fF
L_a	Acoustic inductance of the resonant circuit	59.81 μH
C_m	CMUT capacitance	15 fF
C_p	Interconnect Capacitance (Parasitic)	30 fF
v_a	Acoustic input Signal (max. amplitude)	20 mV

(i.e., with v_a ranging from −20 mV to +20 mV, Vout should range from 0.25 V to 0.75 V).

3. The load capacitance should be 100 fF.
4. The amplifier should have a bandwidth of 500 MHz.
5. The input capacitance should be as small as possible.
6. The input resistance should be greater than 1 MΩ because above this value the overall transfer function (CMUT+voltage amplifier) has minimal sensitivity to the input resistance variations (refer Fig. 6.2).

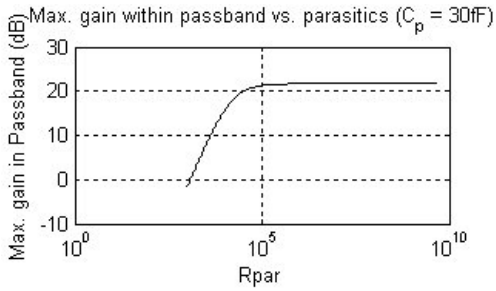

Figure 6.2: Effect of input resistance (real part of Z_{in}) on the circuit performance.

6.3 Amplifier Design

For the sake of compactness, a CS-amplifier was chosen. The main challenge in this case is to provide gate bias to the input transistor, especially when

voltage head-room is limited, and at the same time maintaining high input resistance which is required due to the high source impedance of the CMUT (refer condition 6. above). A simple CS amplifier with a bias network using MOSFETs is shown in Fig. 6.3 (a) (see for example [GT86]). Although simple, the main problem in using such an approach is that the diode connected transistor Mb2 results in the input impedance at the gate of transistor M1 to be approximately the inverse of its transconductance i.e., $\frac{1}{g_{m\_\mathrm{Mb2}}}$. Since we require an input resistance of more than 1 MΩ, this approach is not feasible.

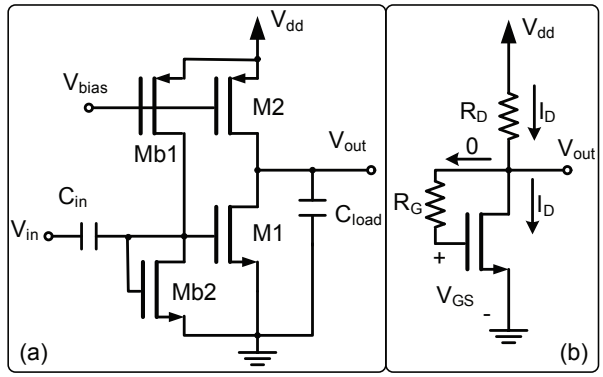

Figure 6.3: (a) A simple CS amplifier with supply independent bias network. Note that C_{in} might not be required for a high impedance input device (like CMUT). (b) Biasing using a Drain-to-Gate feedback resistor [SS04].

Another known approach for providing a gate bias is using a drain-to-gate feedback resistor as shown in Fig. 6.3 (b) [SS04]. Besides requiring a high resistance value to get a high input impedance (notice that the effective resistance as seen at the gate of the MOSFET will be much lower than R_G due to Miller effect), this circuit suffers from limited output swing, which can be understood by (6.1):

$$v_{OUT\_min} \equiv v_{DS\_min} = v_{GS\_max} - V_t \tag{6.1}$$

In technologies where supply voltage is much greater than the threshold voltage of the MOSFETs, this equation states that the usable output swing is very low relative to the supply voltage. However, in newer technologies like the 90nm technology used in our case, the power supply is only 1 V and the relative reduction in usable swing is reduced since the threshold voltage is not scaled proportionally to the power supply voltage. Hence, this feedback biasing scheme is more attractive in nanoscale technologies.

The feedback resistor is implemented using a high resistance device. In [HC03] it was suggested to use pseudo-resistors i.e., diode connected MOSFETs in sub-threshold region to get very high resistance. Therefore we can replace the feedback resistor by a diode connected PMOS as shown in Fig. 6.4 (device MX1).

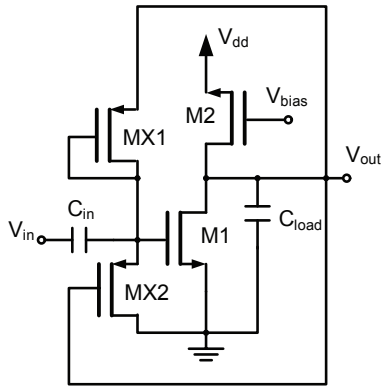

Figure 6.4: Designed CS amplifier with the new biasing scheme.

If we assume that MX2 is absent, then we can see that MX1 serves the same purpose as R_G. Assuming that there is no gate leakage in M1 then using the ideal case MOSFET square law, the output voltage V_{OUT} and hence the gate voltage of M1 will adjust according to (6.2) (refer for example [SS04]).

$$V_{OUT} = V_{GS\_M1} = V_{tn} + \left(\frac{I_{BIAS}}{K}\right)^{\frac{1}{2}} \tag{6.2}$$

Here, V_{GS_M1} is the gate-source voltage of M1, V_{tn} is the threshold voltage of M1, I_{BIAS} is the bias current injected in M1 (by M2), and K is the product of half the 'transconductance parameter' and the aspect ratio $\left(\frac{W}{L}\right)$ of M1 $\left(K = \frac{k'_n}{2} \cdot \frac{W}{L}\right)$ [SS04]. Since V_{tn} of M1 is around 0.36 V in the CMOS technology used, depending on the second term in RHS of (6.2), the output DC level is already close to 0.5 V i.e., what we require. If we can reduce the gate voltage slightly then the output level will shift upwards. For this reason PMOS MX2 is added. Another reason for using a transistor is to create a resistive path from the gate of M1 to ground, i.e., the gate of M1 can discharge through MX2 rather than both charging and discharging through MX1. MX2 actually 'adapts' its resistance according to the gate voltage of M1, or according to the output voltage. To ensure that MX2 remains in

sub-threshold at all times, it should have a high threshold voltage. Although devices with different threshold voltages are available in this technology, but to use them employs additional processing steps during manufacture i.e., extra cost. To avoid this, and to achieve a high threshold voltage, MX2 is dimensioned with the minimum dimensions possible. This is because smaller devices tend to have higher effective channel doping due to diffusion from highly doped source and drain junctions. Higher channel doping means higher threshold voltage for a given MOSFET. This results in the short device having V_t that can be 0.1 V more than the V_t of the long device for same MOSFET type. This phenomenon is exploited here for not only alleviating the need of a high-V_t device, but also preserving the compactness of the circuit.

Input capacitance consists not only of the gate-source capacitance of M1 but also the Miller capacitance of M1 i.e., roughly $C_{gd}(1+A_v)$; where C_{gd} is the gate-drain capacitance of M1 and A_v is the voltage gain of the amplifier. Due to small size of MX1 & MX2, their contribution to input capacitance is very small.

Figure of Merit (FoM) based approach was used for the amplifier design. FoM based design process is already covered in open literature, see for example [AIM05].

The FoM maximized for this design is given in (6.3):

$$FoM = \left(\frac{g_m}{I_{DS}}\right) \cdot \left(\frac{g_m}{2\pi C_{GS}}\right) \tag{6.3}$$

Various circuit parameters were extracted by mathematical expressions calculated in the same simulation run, using the technology models. This avoids the need to compensate for errors to meet the specifications due to difference between results of hand calculations and simulations.

During the first phase of the simulations, various MOSFET parameters were simulated and extracted to characterize the performance of 90nm technology. It was concluded that the design of a single-stage CS amplifier with requirements 2., 4., and 5. is not possible. For example, to fulfill the gain requirement, the input MOSFET would need an intrinsic gain of nearly 60 (assuming that drain-source resistances of M1 & M2, r_{ds_M1} and r_{ds_M2} respectively are equal). This intrinsic gain was not achievable for standard threshold voltage NMOS for lengths less than 0.4 μm. Even at higher lengths, this value of intrinsic gain required very wide devices carrying small current which resulted in very high C_{GS}. Thus, a cascaded two stage CS amplifier was selected. Schematic of the cascaded amplifier is shown in Fig. 6.5.

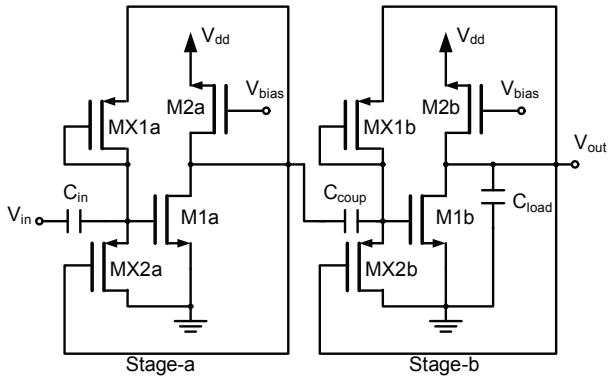

Figure 6.5: Designed CS amplifier with the new biasing scheme.

The design was started by choosing a target DC gain A_{v0} of around 17 dB (or 7.08 V/V) for each stage with typical-typical (TT) models. As a starting point, an analytical estimate for the required circuit parameters was made. The following equations give a quick overview of the device parameters required [SS04]:

$$R_{out} = \frac{1}{2\pi f_{-3db} C_{load}} \tag{6.4}$$

$$g_{mn} = \frac{A_{v0}}{R_{out}} \tag{6.5}$$

Equation (6.4) assumes that the dominant pole is set by the output node, R_{out} is the resistance as seen in the output node (i.e., $(r_{ds\_M1}||r_{ds\_M2})$, f_{-3db} is the desired amplifier bandwidth (500 MHz), and g_{mn} is the transconductance of M1. Width of M1 was considered the first design parameter because most of the other parameters such as input capacitance, gain depend on it. The width of M1 was swept during simulations while keeping the minimum length (to minimize input capacitance). such that the FoM (6.3) at a given bias current was maximized, provided that all other conditions, such as bandwidth, gain, V_{DS_SAT} were satisfied and the output DC level was close to 0.5 V. The PMOS M2 supplying I_{BIAS} to M1 was dimensioned such that its V_{DS_SAT} was acceptable (for required output swing). Each stage was designed for a load capacitance of 100 fF.

Biasing transistor MX1 was dimensioned as a long device such that its resistance is greater than 1 MΩ during the maximum positive swing at the output (refer condition 6. in the previous section). It can be shown analytically that the loop gain (LG) of the feedback loops can be written:

$$LG(s) = g_{mn} \cdot \left(R_{out} || \frac{1}{sC_{load}} \right) \cdot \frac{R_{MX2} || \frac{1}{sC_{inp}}}{R_{MX1} || \frac{1}{sC_{gt}} + R_{MX2} || \frac{1}{sC_{inp}}} \tag{6.6}$$

R_{MX1} & R_{MX2} represent the effective DC device resistances of MX1 and MX2 respectively, C_{inp} is input capacitance at the gate of M1, and, C_{gt} is the total capacitance between the gate and drain of M1. It can further be seen that the loop gain has a dominant pole decided by $R_{MX1}||R_{MX2}$ and $C_{in} + C_{gt}$. Since $R_{MX1}||R_{MX2} \gg R_{out}$, the bandwidth of LG is much lower than the lower 3dB frequency of the amplifier. In fact in our case, the unity-gain frequency of the loop gain is much lower than the lowest operating frequency of interest. This ensures that the biasing scheme does not influence signals within the passband. Thus, if the lower 3dB frequency of the amplifier is required to be moved to still lower frequencies then C_{in} should be designed (increased) accordingly to move the loop-gain dominant pole at a sufficiently low frequency such that it has lowest influence on the passband signals. In addition, the loop gain has a left-hand plane zero decided by R_{MX1} and C_{gt}. Fig. 6.6 shows the signal transfer function and loop gain response respectively of the individual stage of the amplifier. The input AC source was coupled with a capacitance of 1 pF: such high capacitance was used just for testing amplifier gain with minimum attenuation of the AC signals at the input of the amplifier. The loop gain response has very high attenuation at the frequencies of interest. The final transistor dimensions and bias currents are shown in TABLE 6.2.

6.4 Simulation Results

The simulation results are summarized in TABLE 6.2.

Note these modifications done to improve the final design:

- Length of M1 is slightly increased. This stabilized the gain over process corners at the cost of slightly more input capacitance.
- To stabilize the DC level over process corners, the width of MX1 was increased slightly. The length was chosen accordingly such that its resistance requirement was satisfied.

Coupling capacitor C_{coup} used to couple the two amplifier stages was chosen (50 fF) such that it is much larger than the input capacitance of the second stage to minimize the voltage attenuation. Since the proposed

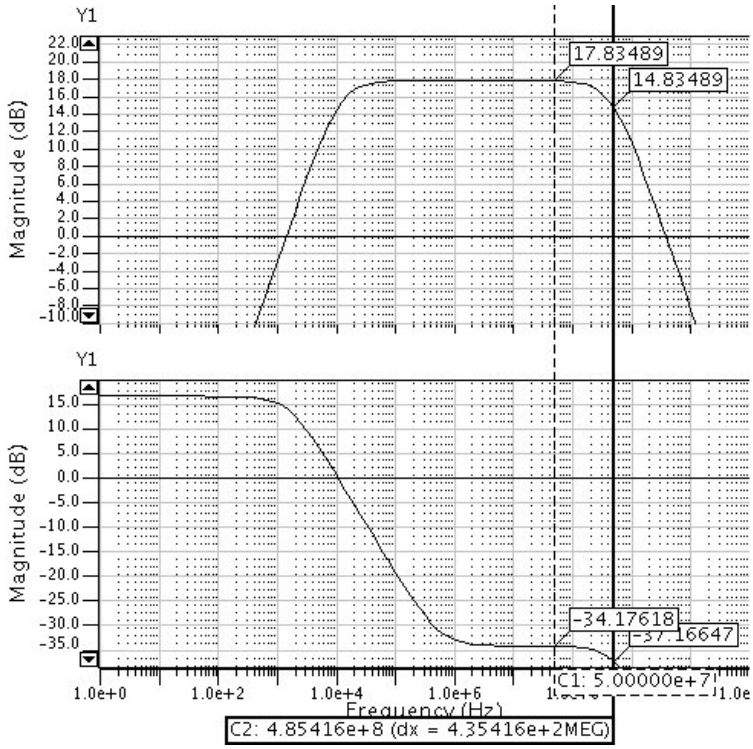

Figure 6.6: (Top) Midband response of a single stage (TT models) with feedback biasing. Midband gain of 17.8 dB and a bandwidth of 485 MHz is achieved with a capacitive load of 100 fF. C_{in} used was 1 pF. (Bottom) Loop-gain response of the feedback.

amplifier is to operate inside the human body, a nominal temperature of 37 °C was used in all simulations. The amplifier has been designed in 90nm CMOS technology and has been submitted for fabrication. Fig. 6.7 shows the layout of the single CS stage. Double guard rings were added for ESD protection during testing around each transistor. The circuit measures just 15 μm × 15 μm.

Table 6.2: Summary of Results and Key Parameters

Parameter	**Value**	
$\left(\frac{W}{L}\right)_{M1a/b}$	$\frac{6.5\mu}{0.11\mu}$	
$\left(\frac{W}{L}\right)_{MX1a/b}$	$\frac{0.3\mu}{2.6\mu}$	
$\left(\frac{W}{L}\right)_{MX2a/b}$	$\frac{0.2\mu}{0.1\mu}$	
Parameter	**Maximum**	**Minimum**
Voltage gain	31.4 dB	28.4 dB
Bandwidth (−3-dB frequency)	751 MHz	523 MHz
Output DC level	0.556 V	0.471 V
Input Capacitance	28.9 fF	25.13 fF
Total Input Resistance (at DC)	31.68 MΩ	3.762 MΩ
RMS output noise (Source+Amplifier)	4.89 mV	3.77 mV
Noise Figure (passband)/ SNR (100 MHz signal frequency)	0.32 dB / 35.2 dB	
Total Harmonic Distortion (THD) at center frequency (100 MHz)	1.79% or −35 dB (Typical)	
Power Consumption (Amplifier only)	460 μW	

The Maximum and Minimum values are the respective extreme values at process corners.

6.5 Conclusions

We have presented a biasing scheme for the CS amplifier that offers a high amplifier input impedance. A two stage cascaded CS amplifier was designed with the specifications mentioned in Table 6.2. The suggested approach takes advantage of some of the limitations posed by newer CMOS technologies. A summary of the results are given in Table 6.2. Although the presented amplifier was designed for CMUT interfaces, the approach presented

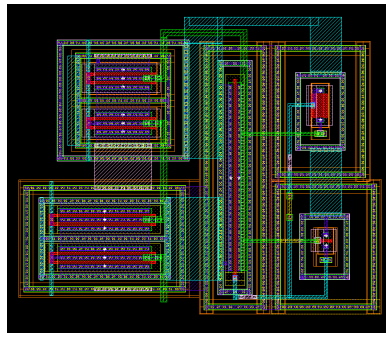

Figure 6.7: Layout of a single CS stage. The biasing transistors can be seen on the right side. The circuit measures 15 μm $\times$ 15 μm.

in this paper can nevertheless be applied where high-resistance biasing might be required. A design procedure for such an amplifier was also presented.

Chapter 7

Paper 4

Current Mode Capacitive Sensor Interface Circuit with Single-Ended to Differential Output Capability

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Abstract

This paper presents a current mode interface circuit for capacitive sensors with the main features being its ability to produce a differential output from a single-ended sensor (using a fixed reference capacitor), and its simplicity in realization. These advantages make it a potential candidate for applications where differential sensors are not available and where a simple design is required. The principle is, however, easily applicable to differential sensors as well. The interface concept can be realized in different ways; however, to present a proof of concept on silicon, a prototype has been fabricated and tested in a commercially available 0.8-μm CMOS process. The circuit has been designed using common analog building blocks such as a fully differential Operational Transconductance Amplifier (OTA), a high output resistance wide-swing current source, and a single clock phase. The estimated linearity error was 0.2% relative to full-scale with a simple 2-point calibration. The circuit consumes 145 μA from a 5 V power supply.

7.1 Introduction

The advantages of capacitive sensing are exploited in many sensor applications [Bax96][BBF+04], for example, in the areas of position sensing, pressure sensing, and MEMS-based systems such as resonators, filters, and micro-sensors. Developments in the field of micro-sensors and MEMS have placed increased demands on interface circuits for these applications. As miniaturization of such devices continues, interface circuits need to match up with an equal reduction in form factor. There are a number of published techniques for capacitive sensor signal conditioning [BBF+04] [GK07] [GPGPA07] [FGMT06] [GLM05] [JMLG05] [DS06] [BMPH07] [DKPS06] [WKST98] [LZG05] [1] [Pen05], having features (i.e., accuracy, power or complexity) similar to the proposed circuit.

These published interface circuits are either designed for a stand-alone sensor, or for integrated sensors and electronics. For example, in [GK07] [GPGPA07] [FGMT06] [GLM05] [JMLG05], the work is focused on systems having a large capacitance and using commercially available discrete components. However, it can be difficult to use such approaches directly in integrated sensor systems because of the difficulty in realizing all discrete components on-chip without adding a large overhead in area (for example, 100 MΩ resistors in [FGMT06]), power and complexity.

Among recently published interface circuits designed for integrated sensor systems, circuits mostly either require some sort of oscillator for excitation [DS06] or highly complex circuitry [BMPH07] [DKPS06] [WKST98] [LZG05]. There are also other limitations associated with each of these approaches – for example, although [BMPH07] and [DKPS06] are suitable for low-power applications, [BMPH07] offered a sample frequency of 10 Hz, [DKPS06] reported a linearity error of 0.8%, and [WKST98] [LZG05] required several internal clock phases for operation.

This paper presents the design and measured results of a proof-of-concept prototype implementation of a new interface circuit first proposed in [1]. The prototype was fabricated in a 0.8-μm commercially available CMOS process. Besides being simple to design and implement, the circuit produces output at 285 kHz, achieves a non-linearity error on the order of 0.2%, and requires only one clock phase for operation. The complexity of the circuit is limited to a fully differential amplifier and a high output-resistance current source, both of which are basic analog building blocks and are covered extensively in the available literature. In applications where the best accuracy is not important, a simple concept realized with generic circuit building blocks has the potential of not only saving design time, but also power consumption

and silicon area.

A similar concept has also been independently proposed in [Pen05], although its realization is different. The differential output of the circuit presented in this paper produces a much better accuracy as compared to that in [Pen05] with single-ended output that resulted in a an error of 2% (simulations only).

This paper is arranged in the following main sections: Section 7.2 presents possible circuit configurations with this interface circuit, with a possible CMOS realization of the interface circuit discussed in Section 7.3. The measurement results and discussions are presented in Section 7.4. This section also discusses the strengths and weaknesses of the prototype, such that the reader can easily evaluate the suitability of the proposed approach for the application at hand.

7.2 Circuit Configurations

Differential configurations are commonly used in signal conditioning because of their ability to reject common mode effects such as substrate noise, interference, and supply and bias variations. This is achieved by injecting the signal (and also reading out the output, in the case of fully differential circuits) along two balanced paths. Since the signals are defined relative to each other, errors common to both paths are canceled out. This, of course, comes typically at the cost of higher power consumption and larger chip area as compared to the equivalent single-ended realization. Differential circuits and their other advantages are covered vastly in detail in the literature, see for example [JM96] [LS94].

Fig. 7.1 (a) shows a simple schematic of how a differential signal is obtained from a single-ended sensor capacitance.

The capacitor C_m represents the sensor capacitance, and C_r is a fixed reference capacitor, both with a nominal capacitance value C. At zero ($C_m = C_r = C$) the charging current I_b splits equally between C_m and C_r. Assuming that C_m deviates from its nominal value by a time-invariant change (during measurement) ΔC, the expressions for I_1 and I_2 become:

$$I_1 = C_m \frac{\mathrm{d}V_1}{\mathrm{d}t} = \frac{I_b}{2} + \frac{i}{2} \tag{7.1}$$

and

$$I_2 = C_r \frac{\mathrm{d}V_1}{\mathrm{d}t} = \frac{I_b}{2} - \frac{i}{2} \tag{7.2}$$

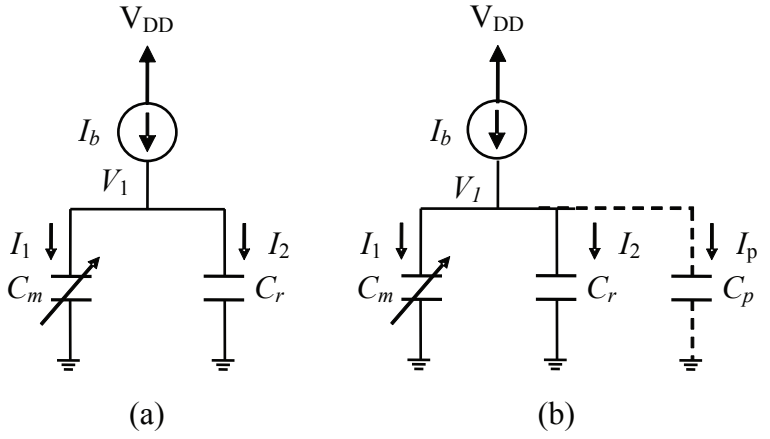

Figure 7.1: Schematic explaining the current mode approach, (a) without stray capacitance, (b) considering stray capacitance C_p, C_m and C_r represent the sensor capacitance and a reference capacitance respectively

where $\frac{dV_1}{dt} = \frac{I_b}{C_m+C_r} = \frac{I_b}{2C+\Delta C}$.

As seen in the rightmost terms of (7.1) and (7.2), the signal current 'i' is differential, despite the sensor being single-ended.

Notice that this single-ended to differential signal conversion occurs in the sensor/reference capacitors itself, and it is not a pseudo-conversion as is done in many cases (see for example [PDMD$^+$06]). In [PDMD$^+$06], infinite g_m is assumed to prove that the DC voltage of the amplifier is maintained. The proposed circuit does not pose such requirement. This advantage comes by virtue of the use of the current source (I_b), i.e., if a voltage source were used instead of I_b, the current signal would not have been a true differential. This may be a significant advantage in terms of relaxed common mode performance requirements for the signal conditioning amplifier.

The signal current is defined as $I_1 - I_2$ and can be expressed, by combining the above equations:

$$i = \frac{I_b \Delta C}{2C + \Delta C} \tag{7.3}$$

It is apparent from (7.3) that the differential signal current 'i' is independent of time as long as I_b and ΔC are time invariant. The non-linearity due to the ΔC term appearing in the denominator of (7.3) is due to the single-ended capacitance. Since this non-linearity is deterministic, it can easily be removed, as is done in many applications. Notice that all parameters on the

right hand side of (7.3) except ΔC are known and constant; therefore, by measuring the signal current 'i', the value of ΔC can be easily calculated.

Stray capacitance at node V_1 modifies the transfer function. Fig. 7.1 (b) shows the stray capacitance C_p at node V_1. This capacitance is the sum of plate stray capacitances of C_m and C_r, routing capacitance and the output capacitance of the current generator I_b. It can be shown that the expression for the signal current is modified due to C_p as:

$$i = \frac{I_b \Delta C}{2C + \Delta C + C_p} \tag{7.4}$$

Fig. 7.2 shows the concept applied to a differential sensor system.

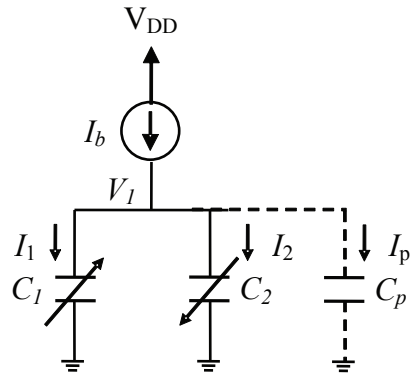

Figure 7.2: Schematic showing the application of the interface concept in a differential sensor. C_1 and C_2 represent the sensor capacitances that vary in an opposite direction.

Capacitors C_1 and C_2 have the same nominal value C. It can be easily shown that the differential signal current is now given by:

$$i = \frac{2I_b \Delta C}{2C + C_p} \tag{7.5}$$

Here ΔC is the deviation in each C_1 and C_2 from their nominal value such that $C_1 = C + \Delta C$ and $C_2 = C - \Delta C$. Notice from (7.5) that not only is the differential signal current doubled as compared to that in (7.4), but also the non-linearity due to the ΔC term in the denominator is absent. We will,

however, focus only on the single-ended sensor application in the rest of this paper.

7.2.1 Circuit Realization

Notice that there are a number of ways by which the signal current can be measured (see for example [Pen05]). The signal current can be amplified, for example, using a transimpedance amplifier (TIA), a current amplifier followed by an *I-V* converter to obtain a voltage output, depending upon the application.

Simulation results of a possible circuit realization of the concept using a fully differential TIA were presented in [1]. A fully differential realization was selected due to its advantages discussed earlier. The block diagram for such a realization is shown in Fig. 7.3.

The differential transimpedance amplifier was realized with a fully differential Operational Transconductance Amplifier (OTA) and feedback resistors $R_{f1} = R_{f2}$ (with a nominal value R_f). The dotted portion of the block diagram is the circuitry added in the prototype for driving the signals off-chip. Hence, the experimentally measured output of the prototype was the output voltage V_{out_b}. Three switches, realized by MOS transistors and driven by the clock phase ϕ, were used to reset the circuit after each measurement period. The circuit was powered by V_{DD} and V_{SS} of 5 V and 0 V, respectively. The common mode voltage (analog ground) of the amplifier was set to 1.2 V (band-gap reference level). The switch at node V_1 resets the node to V_{SS} after each measurement period.

The circuit operates as follows: During the reset period 't_r', node V_1 is reset to V_{SS}. The measurement period 't_m' follows the reset period during which all switches are opened. The charging current I_b splits between C_m and C_r depending on ΔC, and hence creates a differential signal current according to (7.3). This signal current, along with the common mode current, passes through the feedback resistors, creating an output voltage. Since the output is read differentially, the common mode effects are canceled out. The output is read right before the measurement period ends (or when the amplifier output has settled). The circuit is reset once again to prepare it for the next measurement period.

Assuming an ideal amplifier, the differential output voltage created by the signal current can be expressed as:

$$V_{out} = V_{op} - V_{om} = R_f \cdot i = R_f I_b \frac{\Delta C}{2C + \Delta C} \tag{7.6}$$

This transfer function is plotted in Fig. 7.4.

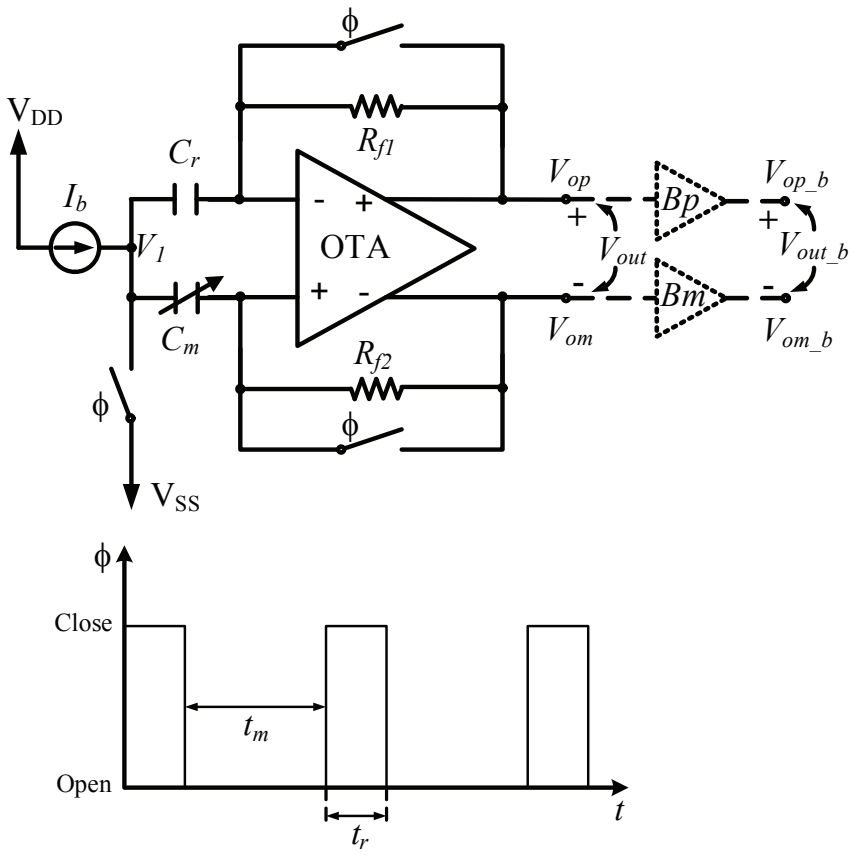

Figure 7.3: Block diagram representation of the prototype interface circuit. Node V_1 is reset during time t_r of a clock phase ϕ to prepare it for the next measurement. The dotted portion of the diagram represents the output buffers (Bp and Bm) added for driving signals off-chip. The output signal V_{out} (V_{out_b} for the prototype) is differential and is read out right before the end of the measurement time t_m.

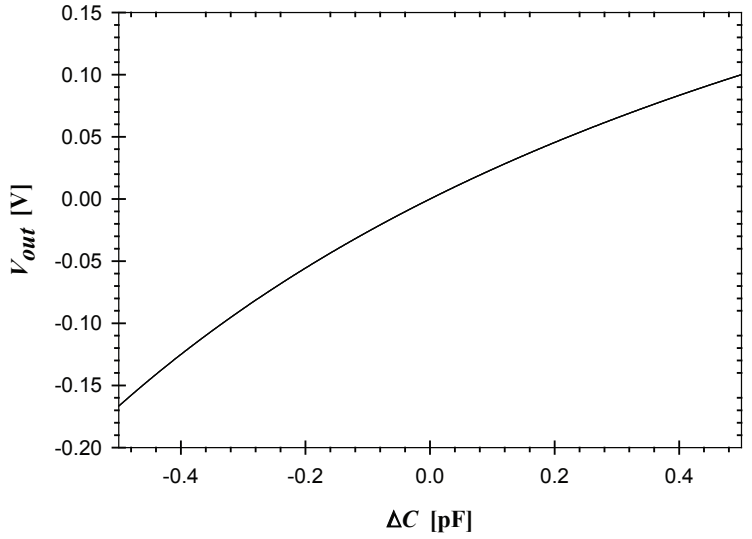

Figure 7.4: Equation (7.6) plotted for $\Delta C \pm 0.5$ pF. Other parameter values are: $R_f = 200$ kΩ, $I_b = 2.5$ μA, and $C = 1$ pF.

By solving (7.6) with respect to ΔC, we get

$$\Delta C = \frac{2C \cdot V_{out}}{R_f I_b - V_{out}} \tag{7.7}$$

This expression is used to calculate ΔC based on the measured output voltage.

The capacitors C_m and C_r are reset after each measurement to limit the voltage at node V_1 such that the transistors of the current source are at all times operating in the desired region.

7.2.2 Impact of Mismatch on the transfer function

The effect on the transfer function due to mismatch between the key circuit elements is analyzed. Equation (7.4) is the expression of the signal current including the influence of parasitics. We will use this expression and expand it to add the effect of mismatch.

Mismatch between the feedback resistors

Let us say that the feedback resistor (R_{f2}) connected to V_{om} has a nominal value R_f, and the resistor connected to V_{op} has a mismatch δR_f with respect

to R_f such that $R_{f1} = R_f + \delta R_f$. Then it can be shown that, in this case, the output voltage can be expressed as:

$$V_{out} = \frac{I \cdot \Delta C \cdot (2R_f + \delta R_f)}{2(2C + \Delta C + C_p)} \tag{7.8}$$

Here, I is the nominal value of the current source I_b.

Mismatch between C_m and C_r

It was considered earlier that C_m and C_r have a same nominal value C. Let us assume that C_m deviates from the nominal value C by δC. We can add the influence of this mismatch to (7.8) as:

$$V_{out} = \frac{I \cdot (\Delta C + \delta C) \cdot (2R_f + \delta R_f)}{2(2C + \Delta C + \delta C + C_p)} \tag{7.9}$$

Deviation in I_b

If the value of the current source I_b deviates from its nominal value I by δI then, the circuit transfer function of (7.9) can be modified as:

$$V_{out} = \frac{(I + \delta I) \cdot (\Delta C + \delta C) \cdot (2R_f + \delta R_f)}{2(2C + \Delta C + \delta C + C_p)} \tag{7.10}$$

If all deviations in (7.10) are constant, then the variations in the values of R_f and I_b cause gain errors in the output voltage. The mismatch between the nominal value of the measuring and reference capacitors causes an offset error at zero and also affects the 'shape' of the transfer function plotted in Fig. 7.4. All these errors, however, can be removed by a simple calibration [vdHH97].

7.3 CMOS Realization

The final realization of the prototype in a 0.8-μm CMOS technology is shown in Fig. 7.5 (reset switches not shown).

Transistors M21-M29 form an enhanced output resistance current mirror [JM96] supplying charging current to the capacitors C_m and C_r. We used a generic 2-stage Miller OTA [LS94] with 90 dB open-loop gain, 490 kHz gain bandwidth product (GBW), and 80 degrees phase margin. The resulting -3-dB frequency of the TIA was around 400 kHz. The capacitors C_d across resistors R_{f1} and R_{f2} are for lag compensation to improve the transient response of the transimpedance amplifier (see for example [HP98]).

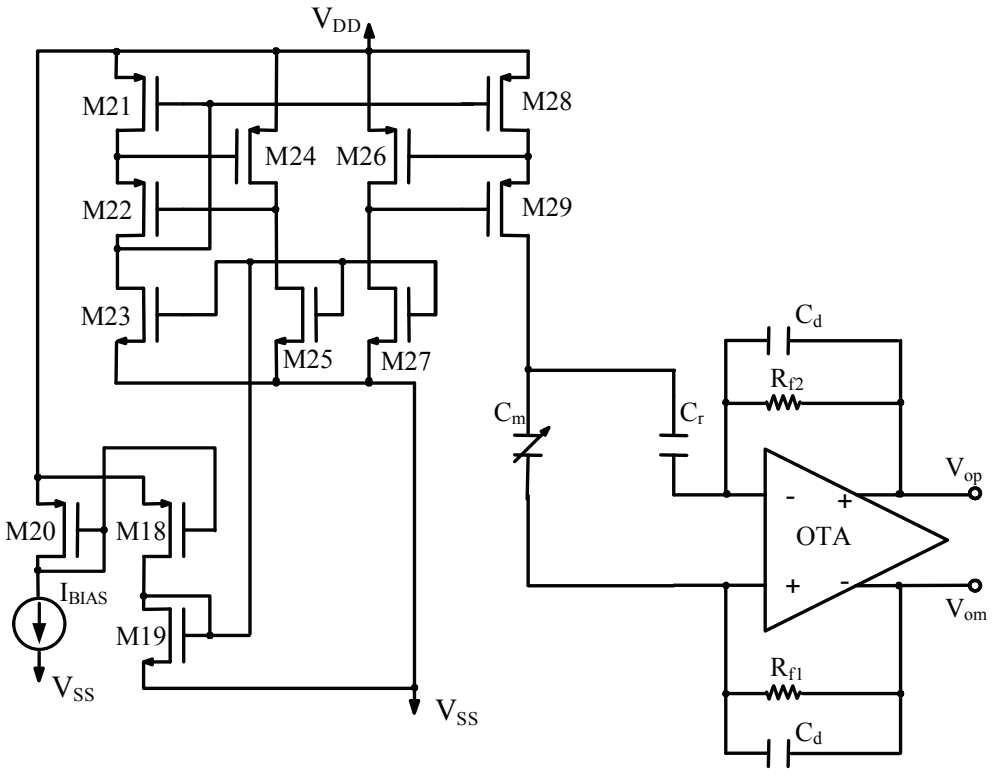

Figure 7.5: CMOS realization of the interface circuit (switches are not shown).

The most important OTA parameters for this application are the open-loop gain, GBW, settling time and slew rate, which are dictated by the accuracy requirements [LS94]. A nominal value of 1 pF was chosen for C_m and C_r. The feedback resistors set the transimpedance gain (see (7.6)). We used 200 kΩ resistors for our prototype. The prime trade-offs involved in choosing the resistor value are between high gain and output swing on one hand, and input resistance, noise, and chip area on the other hand. The choice of charging current primarily depends on: the voltage headroom at V_1, the size of capacitors C_m and C_r, and the measurement time. Based on this, a charging current of 2.5 μA was selected.

It is more important for the charging current to be stable over time rather than being exact to a certain value because a constant offset in the current value will result in only a gain error, which can easily be removed by calibration. Also, notice that the current source should supply current that has sufficiently low dependence on the voltage V_1 such that the δI term in (7.10) does not introduce more non-linearity at the output than tolerable. As seen above, the circuit complexity of the proposed circuit is limited to the design of the enhanced output resistance current mirror and fully differential OTA, both of which are discussed extensively in the literature.

Fig. 7.6 shows the transient response of the prototype circuit. Clock timings controlling the reset switches were optimized during simulations such that the reset time was enough to discharge the capacitors, and the measurement time was enough for the system output to settle A clock frequency of 285 kHz with a 28.57% duty cycle was used for the reset switches, tm being 2.5 μs and t_r being 1 μs. The output is read out at the end of the measurement period tm. Note that the only requirement for the clock is to allow enough time for discharging the capacitors in the reset phase and to let the amplifier settle in the measurement phase. The output can be read out at any time, after the amplifier has settled.

Following recipe can be used to decide the circuit parameters: For a given sensor (and reference) capacitance C, and a given capacitance change ΔC, (7.3) provides the value of differential signal current 'i' produced. The value of R_f is decided by the output voltage swing desired within a feasible area budget. The minimum value of the measurement time t_m is decided by the settling time of the system, i.e., if the output can settle faster, measurement time can be shorter. The maximum value of the measurement time t_m is decided by the node voltage V_1. Within the measurement time t_m, the node voltage V_1 is a steadily rising ramp that needs to be reset before the voltage V_1 reaches a point where it starts producing more error than maximum allowed δI in (7.10).

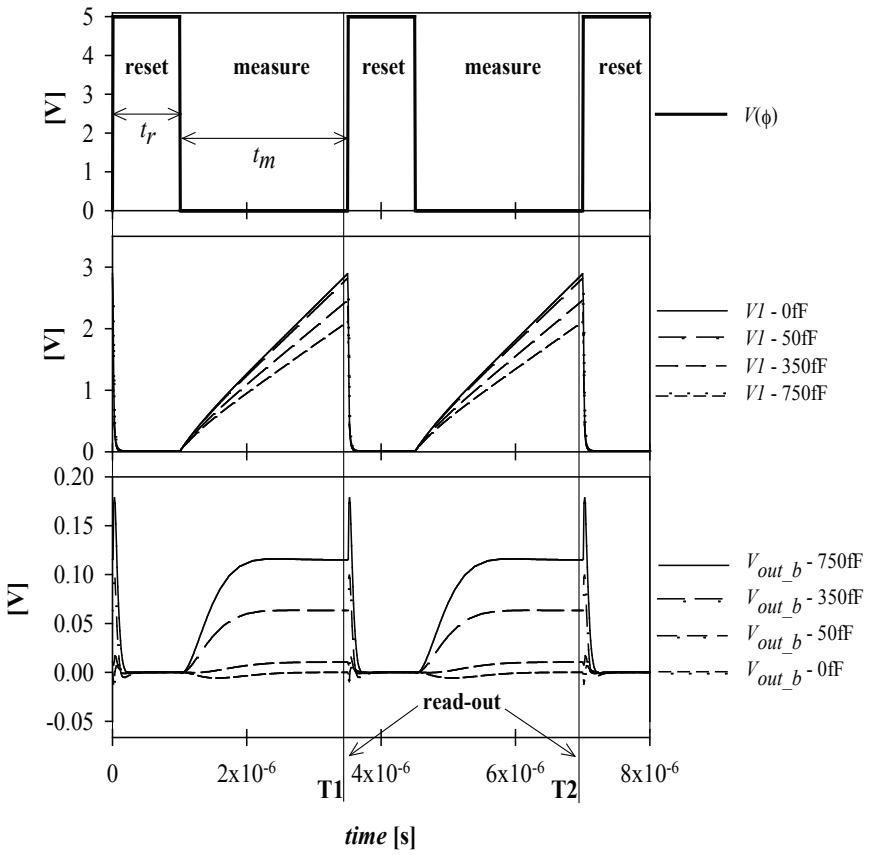

Figure 7.6: Simulated transient response illustrating a snapshot of the operating sequence of the prototype for different ΔC values. V(ϕ) denotes the reset clock, node voltage V_1, and the differential output voltage V_{out_b} ($= V_{op\_b} - V_{om\_b}$) are as shown in Fig. 7.3. The output is read out just before the reset phase starts, as marked by timing instances **T1** and **T2** in the figure.

The advantage with the circuit realization shown in Fig. 7.3 is that the node V_1 is isolated from the OTA inputs therefore, it can be reset to a voltage lower than the common-mode voltage of the OTA, as shown in the figure where it is reset to V_{SS}. Using (7.1)–(7.3), we can express the maximum measurement time as:

$$t_{m\_max} = \frac{2C \cdot (V_{1\_max} - V_{1\_min})}{I_b} \tag{7.11}$$

Here, V_{1_max} is the maximum voltage at V_1 such that the non-linearity in I_b remains below acceptable, and V_{1_min} is the voltage at which V_1 is reset to. The reset time t_r is simply decided by the time it takes to reset the V_1 node to V_{1_min}.

7.4 Measurement Results and Discussion

A chip photograph of the fabricated circuit is shown in Fig. 7.7. Various circuit components are marked. The circuit measures 2.12 mm × 1.04 mm with output buffers (without pads). Without buffers and associated wide power supply routing, the circuit measures 1.24 mm × 0.52 mm.

A simple weighted capacitance bank was integrated with the circuit to create on-chip capacitance variations (Inset 'X' in Fig. 7.7). The capacitor bank consisted of capacitors of nominal values 50 fF, 100 fF, 200 fF and 400 fF respectively, switched by control switches. Each of these capacitors corresponded to a ΔC change in the C_m capacitor, which therefore resulted in a nominal resolution of 50 fF for the bank.

The curves in Fig. 7.8 show the measured output voltage and ideal output voltage (equation (7.6)) respectively, versus ΔC with offset and gain errors removed.

The non-linearity error between the ideal and the measured curves includes the non-ideal effects of the capacitor bank, such as switch impedances, mismatch, and internal stray capacitances. The horizontal bars in Fig. 7.8 represent this total error between the ideal and measured curve at measurement points (50 fF apart). The total error was measured as a maximum of 1% relative to full-scale swing (FS) (simulated 0.8%). Since this error includes the non-idealities of the capacitor bank, it does not justify attributing this accuracy value to the interface circuit. Therefore, the non-linearity performance of the interface circuit was characterized by post layout simulations (PLS). In the first run, the measured results were compared with the PLS results of the whole system (including the capacitor bank) to verify that the measurements agree with the simulated response. In the next run,

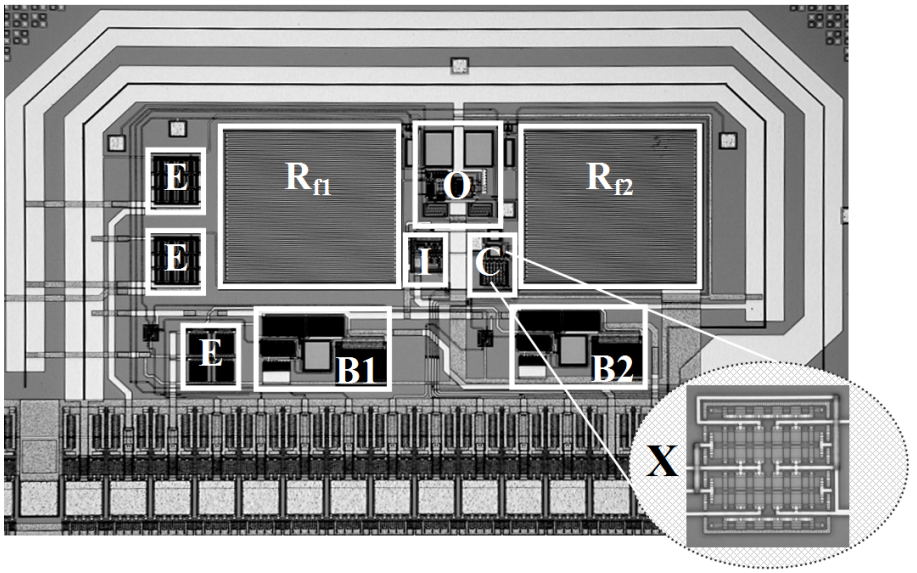

Figure 7.7: Picture of the complete interface circuit with output buffers and capacitor bank. Areas 'R_{f1}' and 'R_{f2}' are the feedback resistors, 'O' is the OTA, 'I' is the high output-resistance current source, 'C' is C_m and C_r, 'B1' and 'B2' are the output buffers, and the 'E' areas consist of current mirrors for supplying external biasing current to the chip. Inset 'X' shows the on-chip capacitor bank used to create ΔC steps.

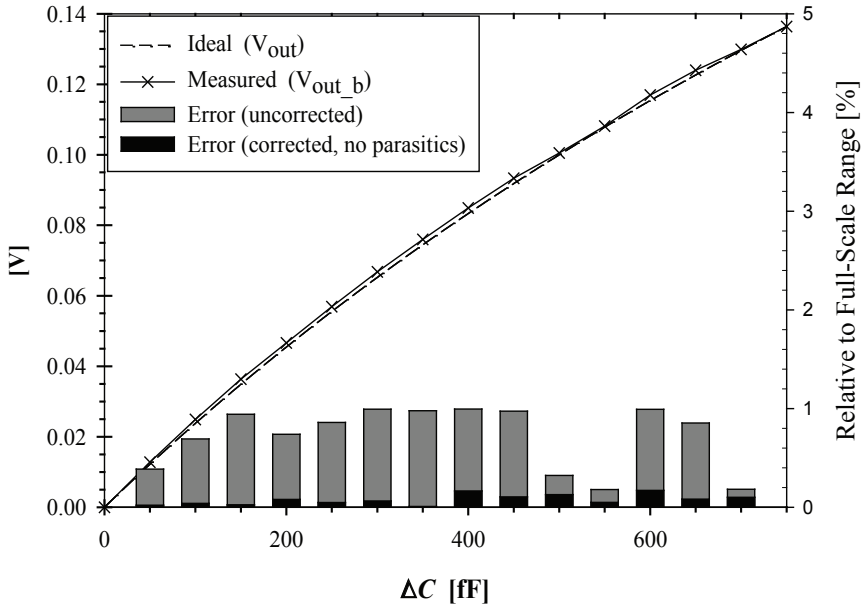

Figure 7.8: Prototype output voltage plotted versus capacitance change from 0–750 fF with an output swing of 136.4 mV. The dotted line shows the ideal output (equation (7.6)). The prominent non-linearity between the two curves is due to the non-ideal capacitor bank used in the prototype to generate capacitance changes. The horizontal bars represent the relative uncorrected (gray) and, corrected (black) errors between the ideal and measured outputs at respective measurement points.

an ideal capacitor bank was used in the PLS netlist such that the errors in the capacitor bank were excluded (corrected). This led to an estimated accuracy of better than 0.2%, represented by the black bars. The errors due to the parasitics on node V_1 were also removed.

If the effect of stray capacitance on node V_1 is included with a capacitance of 0.25 pF (as extracted for the capacitor bank and the circuit by the PLS tool), an accuracy of better than 0.7% was estimated, which is slightly better than that in [DKPS06]. Key parameters and results obtained from the prototype are summarized in Table 7.1.

Table 7.1: Summary of Results and Key Parameters

Parameter	**Value**
Nominal value of C_m and C_r	1 pF
Capacitance range (ΔC)	0.75 pF
Value of feedback resistors R_f	200 kΩ
Charging current I_b	2.5 μA
Measurement uncertainty due to noise (simulated)	1.13 fF
Maximum non-linearity error relative to full-scale swing	0.17% (no stray capacitance) 0.67% (with 0.25 pF stray cap.)
Current consumption	145 μA (without buffers)

With the selected bias currents and component values, the circuit gives a full-scale output swing of 136.4 mV and consumes 145 μA from a 5 V power supply. The output noise determines the measurement uncertainty (or resolution) in the capacitance change detection; this is calculated as 1.13 fF.

To provide the reader with an overview of the features of the proposed technique, and to aid in choosing an approach for a specific application, the authors provide, a list of strengths and weaknesses based on their best knowledge.

7.4.1 Strengths

- Able to produce differential output from single-ended sensors. This differential signal is generated at the input of the amplifier itself.

- The approach can even be extended for resistive sensors, without requiring discharging switches.
- The concept proposed is simple to realize and to apply. No complex signal sources, special amplifiers or switched capacitor circuits are required.
- Does not require accurate clock phases. Provided the amplifier has settled to the required accuracy within the measurement period, the output is independent of clock jitter.
- Since the output is not integrated (instead, the instantaneous value of the output voltage, or signal current, is measured at the end of t_m), the circuit is immune to clock feedthrough. The TIA output should settle after this glitch within the period t_m, but this is not a difficult requirement.
- Can be realized using a standard fully differential amplifier and a high output resistance current source.
- Features a linear transfer function for differential sensors.
- Realization in CMOS technology is feasible, making it a promising candidate for on-chip signal conditioning for sensors based on silicon technology.

7.4.2 Weaknesses

- Non-linearity (although deterministic) as seen in (7.3), for single-ended sensors. The interface is linear for differential sensors (7.5).
- Sensitivity to stray capacitance at node V_1. The designer should try to minimize this stray capacitance to reduce its influence on the circuit. Possible solutions might include reduction in routing to the sensor, and design of the sensor such that plate stray capacitances are minimal.
- Relationship between output swing, charging current, clock frequency and headroom. For a given nominal capacitance, in order to get higher swing, the designer might want to increase the charging current. However, this also means that the capacitors charge faster, hence either the measurement time must be decreased or the voltage headroom must be increased in order to prevent non-ideal effects in the current source. Therefore, the designer must settle for an optimum compromise that satisfies design requirements.

- Large feedback resistors for high output swing. This paper focuses this approach, but an alternative signal conditioning topology, such as a differential current amplifier in feedback and subsequent I-V conversion, may alleviate the need for large resistors.
- The proposed circuit realization can only be applied to capacitive sensors where both capacitor plates can be connected to any potential. It does not work with sensors that have one plate connected to bulk.

7.5 Conclusions

We have presented the proof of concept for a simple current mode interface circuit with the ability to produce differential output from a single-ended sensor. The approach is also applicable to differential sensors. The application of the approach is not limited to capacitive sensors alone, but can also be used with resistive sensors. Design and measurement results of a prototype, based on the proposed concept and designed and tested in a 0.8-μm CMOS technology, have been presented. The measured accuracy of the prototype with a non-ideal capacitor bank signal source was around 1%. By removing the non-ideal effects of the signal source, a circuit accuracy of better than 0.2% was estimated. With an improved OTA and current source, the accuracy can be increased further. The purpose of the designed prototype was to prove the concept and to demonstrate the advantages of the proposed approach. The concept has also been recognized and proposed independently [Pen05], and can be implemented in different ways. Future work can focus on finding suitable topologies to alleviate all or some of the weaknesses (the effect of stray capacitance, output swing, etc.) that were found in the prototype presented in this paper. Therefore, there is great potential for this approach to be applied and improved to realize simple sensor interfaces.

Acknowledgment

The authors wish to thank Tore Barlindhaug for designing the PCBs used for prototype testing.

Chapter 8

Paper 5

Feedback Biasing in Nanoscale CMOS Technologies

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Abstract

This work rediscovers the attractiveness of feedback biasing when applied to circuits designed in nanoscale CMOS technologies. It is shown that very compact amplifiers can be obtained by utilizing a type of biasing that imposes minimal area overhead. We discuss how the undesired features of the nanoscale CMOS technologies actually help in the revival of this simple biasing method in newer technology generations. The measurement results of prototyped common-source (CS) amplifiers utilizing feedback biasing for application in medical ultrasound imaging systems are presented in this brief. The proposed feedback biasing is also suitable for amplifying signals from high-impedance sources that pose challenges on maintaining high input impedance for the voltage amplifiers while maintaining a very low input capacitance value. Measurements show that the proposed amplifier achieves a voltage gain of 28 dB, an output noise power spectral density of 0.11 $(\mu\text{V})^2/\text{Hz}$ at center-frequency, and a total harmonic distortion of -30 dB, with the full-scale output at 30 MHz, while drawing 120 μA from

a 1-V power supply. The amplifiers were fabricated in 90-nm CMOS technology and measured to be just 20 μm $\times$ 10 μm.

8.1 Introduction

CMOS integrated-circuit technology growth is encouraged by the demand for decrease in cost per performance of digital processing [ANvLT05]. Each technology generation comes with its set of advantages and limitations. Nanoscale CMOS technologies are suitable for applications that demand smaller and faster transistors or, in other words, where very high frequency operation is required with very small parasitic capacitances. However, scaled-down technologies introduce limitations, such as low voltage headroom, low output resistance of transistors, and low accuracy in terms of matching and noise. Another characteristic of CMOS technologies is that the MOSFET threshold voltage does not scale proportionally to the power supply voltage as the technology generation (minimum gate length) changes. As a matter of fact, the threshold voltage reduces at a lower rate, compared with the power supply voltage, as one moves to newer technology generations (see, e.g., [CC02]). This is usually not good news for an analog designer, as it becomes difficult to design amplifiers having high-enough gain, particularly because performance enhancement techniques such as cascoding cannot be used without sacrificing most of the headroom.

There are, however, some applications where compactness in the analog footprint is also essential. In such cases, the nanoscale technologies can be a viable option for the analog circuitry as well. Some of the features of nanoscale technologies that are otherwise not desirable to an analog designer may actually be useful in some circuit techniques, as we will show in this brief for the case of feedback biasing. Even though a feedback-biasing scheme is simple and ensures that the input MOSFET remains in saturation, irrespective of the process and temperature variations, its biggest disadvantage has been the limited voltage swing [SS04]. We, however, show that this disadvantage vanishes as one moves to nanoscale technologies.

We present measurement results of common-source (CS) amplifiers using feedback biasing designed for application in a capacitive-micromachined-ultrasonic-transducer (CMUT)-based intravenous imaging system based on the SMiDA project [SMi] specifications. CMUTs have recently gained much interest due to their numerous advantages as ultrasound transducers. CMUTs can be integrated with electronics on silicon and are compact. A number of works on CMUT operation and applications are available (see, e.g., [OHB$^+$04] and [WYZ$^+$05]).

Due to the requirement of having an array of several transducers with local signal conditioning on a catheter tip for performing imaging inside the human arteries, the compactness of the circuitry is of utmost importance, followed by the constraint on the power consumption of the system. It is for this reason that a CS amplifier topology is being investigated for this application, as the CS amplifier is one of the most efficient amplifier stages that can be realized in CMOS technology [Nor00].

To realize the biasing within a very small area, we use subthreshold MOSFETs as high-value resistors to bias our amplifiers. Such techniques have been used before in low-frequency systems (see, e.g., [HC03]) but not with CS amplifiers operating at such frequencies, as proposed by the authors.

The simulation results and advantages of feedback biasing in nanoscale technologies were first reported in [3] for a 100-MHz CMUT. In this brief, we present the analysis, design, and measurement results of the first batch of amplifiers that are fabricated for interfacing with 30-MHz CMUTs. The fabricated amplifiers achieve a very small form factor.

This brief is arranged as follows: We will start with the theoretical background and analysis of the feedback-biased amplifiers in Section 8.2. The circuit design is discussed in Section 8.3. We present the simulation and measurement results in Section 8.4 before we conclude this brief.

8.2 Theoretical Background

8.2.1 Negative Feedback and Closed-Loop Gain

The closed-loop gain of a system in negative feedback, with input $x(s)$ and output $y(s)$, can be written as the well-known expression given by [SS04]

$$A_{CL}(s) = \frac{y(s)}{x(s)} = \frac{A(s)}{1 + A(s) \cdot \beta}. \tag{8.1}$$

Assuming feedback factor β to be frequency independent and loop gain $A(s) \cdot \beta \gg 1$, the result is a desensitized closed-loop gain $A_{CL}(s) \approx 1/\beta$.

The resulting closed-loop gain is usually smaller, compared with the open-loop gain, such that $A_{CL}(s) < A(s)$. Let us now consider a case where the feedback factor is also frequency dependent such that loop gain $A(s) \cdot \beta(s) \ll 1$ within the frequency range of interest; the closed-loop gain (8.1) can be expressed as

$$A_{CL}(s) \approx A(s). \tag{8.2}$$

Although the advantage of a desensitized closed-loop gain is lost in this case, it does result in a closed-loop gain that is as high as the open-loop gain. We will use such feedback in our amplifier such that the influence of the feedback loop is limited to controlling the bias point of the amplifier such that, within the frequency band of interest, the amplifier operates effectively as an open-loop amplifier.

8.2.2 Suitability of Feedback Biasing for CMOS Technologies

Fig. 8.1 (a) shows an NMOS input transistor using feedback biasing [SS04].

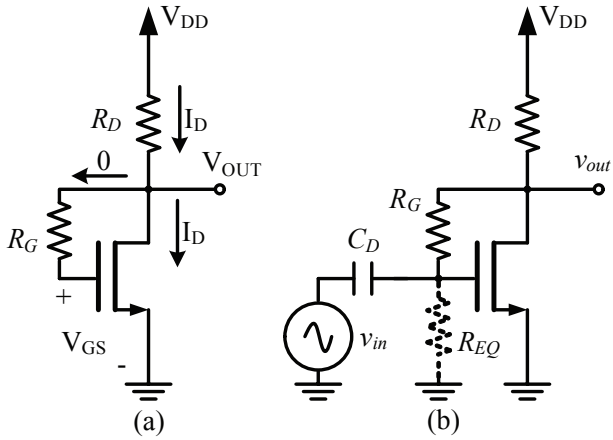

Figure 8.1: (a) An NMOS with feedback biasing [SS04]. (b) When used as a voltage amplifier with a low impedance source.

Since the gate of a MOSFET is a high-impedance node (at low frequencies), almost no dc current flows through feedback resistor R_G (neglecting any gate leakage). Therefore, at dc, the MOSFET can be thought of as a diode-connected transistor that is "self" biased in the active region as long as threshold voltage V_T is larger than zero.

Although simple, this biasing method poses a restriction on the output swing toward the lower power rail. If we assume strong inversion operation, then the minimum output voltage that is achievable without driving the transistor in the linear region is

$$v_{OUT\_MIN} \equiv v_{DS\_MIN} \approx v_{GS\_MAX} - V_T. \tag{8.3}$$

For maximum possible swing around the bias point, the amplifier would normally be biased such that the output dc level (V_{OUT}) is exactly at the

middle of the power rails i.e., $(V_{DD} - V_{SS})/2$. In this case, the output swing would be limited by the saturation voltage of the MOSFET. Assuming that the amplifier has a high gain such that the magnitude of the ac signal required at the input (gate) to drive the amplifier output to full swing is much smaller than the dc value at the input (i.e., $v_{gs} \ll V_{GS}$), from (8.3), we can see that the minimum output voltage possible would be

$$v_{OUT\_MIN} \approx \frac{V_{DD} - V_{SS}}{2} - V_T. \tag{8.4}$$

This is a serious limitation when using feedback biasing, as shown in Fig. 8.1, in older technologies, where the supply voltage is much larger than the MOSFET's threshold voltage. It means that getting a high output swing with this type of biasing in such technologies is difficult, because, when the MOSFET is biased at the middle of the power rails, its high saturation voltage would restrict the minimum output voltage that is achievable (8.4) to a very high value, and if it is biased to a lower saturation voltage, then the asymmetric bias point would limit the maximum possible output swing.

This, however, changes as one moves to newer technologies, where it is a well-known fact that the threshold voltage scales much slower than the power supply voltage as the technology generation changes. This means that the minimum output voltage that is achievable, as shown in (8.3), reduces to more favorable numbers in nanoscale technologies.

8.2.3 Basic analysis of feedback biasing

The circuit shown in Fig. 8.1 (a) can be recognized as a simple transimpedance configuration with feedback resistor R_G. If the feedback resistor is very large, then the loop gain response of this amplifier can be designed to decay at low-enough frequencies such that the amplifier operates effectively in open loop at high frequencies, as mentioned in (8.2).

For analysis, the circuit can be redrawn to include other important impedances, as shown in Fig. 8.2.

Additional devices shown in Fig. 8.2 (a) are C_L, which is the capacitive load at the output of the amplifier; C_G, which consists primarily of the gate–drain capacitance of the MOSFET; and C_{IN}, which comprises dc block capacitance C_D, as shown in Fig. 8.1(b), and the gate–source capacitance of the MOSFET.

Fig. 8.2 (b) is used to calculate the loop gain response of the feedback, as expressed in

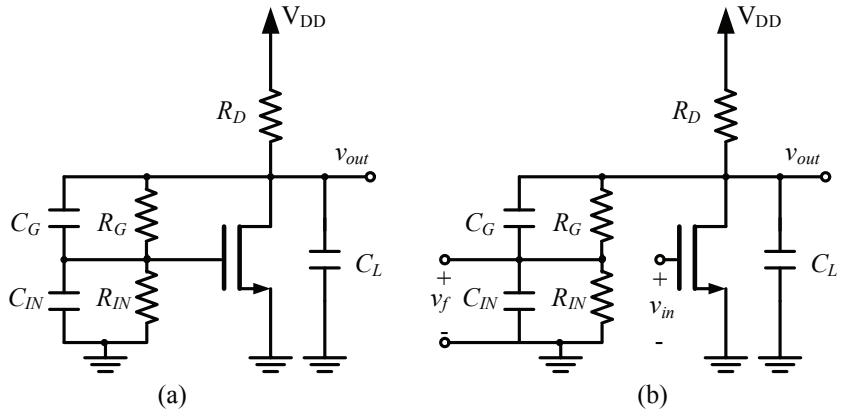

Figure 8.2: (a) Schematic showing feedback-biased amplifier with important impedances shown. (b) The feedback loop is broken to calculate the loop gain.

$$\begin{aligned} LG(s) &= -\frac{v_f(s)}{v_t(s)} \\ &= g_m \cdot (R_{out} \| 1/sC_L) \cdot \frac{1/sC_{IN}}{R_G \| 1/sC_G + 1/sC_{IN}} \\ &= g_m \cdot \frac{R_{out}}{1 + sR_{out}C_L} \cdot \frac{1 + sR_GC_G}{1 + sR_G(C_G + C_{IN})} \end{aligned}$$

.

(8.5)

Here, R_{out} is the output resistance of the amplifier given by $R_D \| r_{ds}$, and g_m is the transconductance of the MOSFET. The loop gain response has a dc gain of $(g_m R_{out})$. In the case when $R_G \gg R_{out}$ (the output resistance is poor in nanoscale technologies for small devices [ANvLT05]) and load capacitance C_L and C_{IN} are of the same order, the dominant pole of the loop gain response is set by the RC product at the input node (i.e., the product of R_G and $C_G + C_{IN}$).

There is also a zero set by the product of R_G and C_G, but, assuming that $C_{IN} \gg C_G$, it lies at much higher frequencies than the dominant pole.

Assuming that the second pole of the loop gain response lies far beyond its unity gain frequency ω_t, one can estimate ω_t as the product of the dc gain and the frequency of the dominant pole, i.e.,

$$\omega_t = \frac{g_m R_{out}}{R_G(C_G + C_{IN})} \approx \frac{g_m R_{out}}{R_G C_{IN}}. \tag{8.6}$$

Since the input signal v_{in} to the amplifier shown in Fig. 8.1 (b) is capacitively coupled (by C_D) to the gate of the MOSFET, capacitor C_D forms a high-pass filter, in combination with the equivalent resistance R_{EQ} at the gate of the MOSFET. Resistance R_{EQ} appears due to the Miller effect at the gate of the MOSFET, i.e.,

$$R_{EQ} = \frac{R_G}{1 + g_m(R_{out} \| 1/sC_L)} \approx \frac{R_G}{1 + g_m R_{out}} \text{at low freq.} \tag{8.7}$$

The 3-dB frequency of this high pass filter is given by

$$\omega_{3dB} = \frac{1}{R_{EQ} C_{IN}} \approx \frac{1 + g_m R_{out}}{R_G C_{IN}}. \tag{8.8}$$

As shown in (8.6) and (8.8), the unity gain frequency of the loop gain almost coincides with the 3-dB frequency of the high-pass filter at the amplifier input. This means that the loop gain is less than unity beyond this frequency; hence, the feedback loop is disabled beyond this frequency, and the amplifier operates effectively in open loop, as outlined in (8.2). Therefore, the feedback loop, while biasing the MOSFET, does not interfere with the signals beyond ω_{3dB}.

8.3 Circuit Design

Since CMUT is a capacitive device, dc block capacitor C_D, as shown in Fig. 8.1 (b), is not required. The CMUT itself provides the dc isolation.

Amplifier specifications were partly defined as a part of the SMiDA project and partly calculated by simulations and optimization done with the CMUT model. More details on the CMUT model used and optimization done can be found in [3].

In order to achieve a target gain of 30 dB (about 30 V/V) from a single CS stage, the input MOSFET needs to have an intrinsic gain of about 60 V/V (assuming that the input device and active load have similar output resistances). This is very hard to achieve in 90-nm CMOS while keeping a small device length. In fact, such intrinsic gain was not achievable for standard threshold voltage devices with lengths of less than 0.4 μm. Even at higher lengths, this value of intrinsic gain required very wide devices carrying small current and resulted in a very high gate–source capacitance C_{GS}, thus making it unsuitable for this application. Therefore, a cascaded topology was chosen. Fig. 8.3 shows the schematic of a feedback-biased cascaded CS amplifier with two identical stages “a” and “b”.

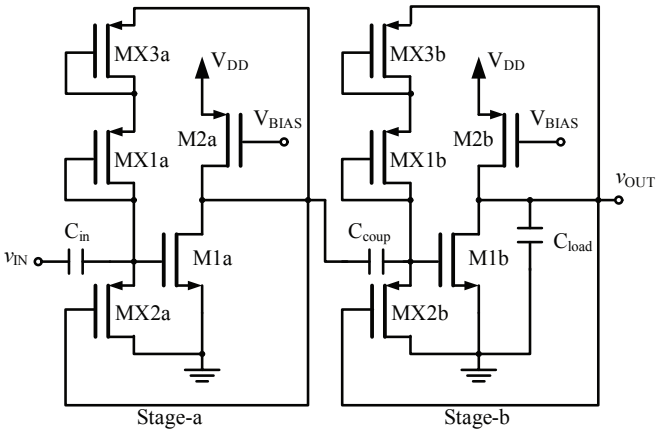

Figure 8.3: Schematic of a feedback-biased cascaded common source amplifier.

Coupling capacitor C_{coup} (50 fF) isolates the input dc level of "stage b" from the output of "stage a." A power supply voltage V_{DD} of 1 V was used in the circuit. Since stages "a" and "b" are identical, we will refer to their devices without the stage's suffix while explaining the circuit operation. For example, when talking about device M2a (or M2b), we will refer to it as M2, and so on.

The use of MOS-bipolar devices and MOSFETs in subthreshold as pseudoresistors and voltage-dependent resistors, respectively, has been shown and implemented already [HC03], [CNW99]. Not only do such devices exhibit a very high incremental resistance, but it is also possible to implement them in minimum feature size, thereby introducing very little area overhead. There is another advantage of using minimum feature-size devices for such applications in nanoscale technologies. Devices with minimum features tend to have a higher threshold voltage due to higher effective channel doping resulting from diffusion from highly doped source and drain junctions.We observed a difference of as high as 0.1 V between the threshold voltages of a minimum-feature-sized device and a larger device in the same category. The higher-than-nominal threshold voltage of a small device, in this case, helps in guaranteeing that the device remains in the subthreshold region, thereby minimizing distortion at large voltage swings.

Diode-connected devices MX1 and MX3, which are connected in series across input device M1, form the feedback biasing resistance. Using two devices in series ensures that the voltage across them is not sufficient to turn them both "on" during large voltage swings. Hence, a high-resistance

path is guaranteed at all voltage levels. If we assume that there is no gate leakage in M1 and that MX2 is absent, then, using the square law model, the output dc level of each stage will be

$$V_{OUT} = V_{GS\_M1} = V_T + (I_{DS}/K)^{1/2}. \tag{8.9}$$

Here, V_{GS_M1} is the total gate–source voltage of M1, V_T is the threshold voltage of M1, I_{DS} is the bias current injected into M1 by active load M2, and K is the product of half the "transconductance parameter" and the aspect ratio W/L of M1 ($K = (k'_n/2) \cdot W/L$).

Device MX2 is optional in the design for the feedback biasing to work. It typically exhibits a much higher resistance, compared to the feedback-resistive path (series combination of MX1 and MX3), and forms a direct high-resistance path to ground for the gate node of M1. It also acts as a voltage dependent resistance that forms a weak feedback loop that keeps M1 from entering deep into the linear region during higher-than-rated input voltages. It was also observed that MX2 helped improve the linearity performance of the amplifier by compensating for the nonlinear behavior of the main feedback path. Under normal operation of the amplifier, the input resistance (at the gate of M1) is dominated by the equivalent resistance decided by devices MX1 and MX3.

The circuit shown in Fig. 8.3 was optimized, during simulations, for efficiency in terms of gain while, at the same time, having as small input capacitance as possible.We used the well known g_m/I_D-based design optimization (see, e.g.,[SFJ96]). To optimize the transconductance per current consumed and the transconductance per area, the figure of merit (FoM) was used as follows:

$$FoM = (g_m/I_{DS}) \cdot (g_m/2\pi C_{gs}). \tag{8.10}$$

Optimization was done with typical-typical models, and the gain of each stage was selected such that the amplifier's maximum output swing did not exceed 0.5 V peak to peak at the maximum CMUT signal (SMiDA project requirement).

Fig. 8.4 shows the layout plan (L) and the chip photograph (C). The circuits were fabricated in a commercially available 90-nm CMOS process with seven metal layers. Four amplifiers were placed on each chip with two different types of layout, as shown in Fig. 8.4. In one type, the coupling metal–insulator–metal capacitor C_{coup} was placed on top of circuit (O), which measures 20 μm $\times$ 10 μm, such that the capacitor does not occupy more space than the circuit itself, and in the other type (F), which measures

20 μm $\times$ 18 μm, the capacitor was placed away from the circuit, thereby taking an area larger than that in (O).

In the case of (O), two metal layers between the capacitor's bottom plate and the circuit below were left unused to reduce the stray capacitance between the capacitor and the circuit beneath. Therefore, by placing the coupling capacitor above the circuit, appreciable area was saved. A possible disadvantage of doing this can be poor control of the absolute value of the capacitor, but it is not important in this case. Since the amplifiers are so small, gain calibration would be used for the CMUT amplifier arrays to compensate for the mismatch effects. Insets (O) and (F) shown in Fig. 8.4 are the zoomed-out views of the tiny windows on (L) representing the actual area taken by amplifiers on the die. The rest of the circuitry surrounding the amplifiers in (L) is composed of the buffers used to drive the output signals off chip. The four input pads, one for each amplifier, which can be distinctly seen on the north side of the die (C), are expected to be used for both wire and flip-chip bonding with the CMUT die.

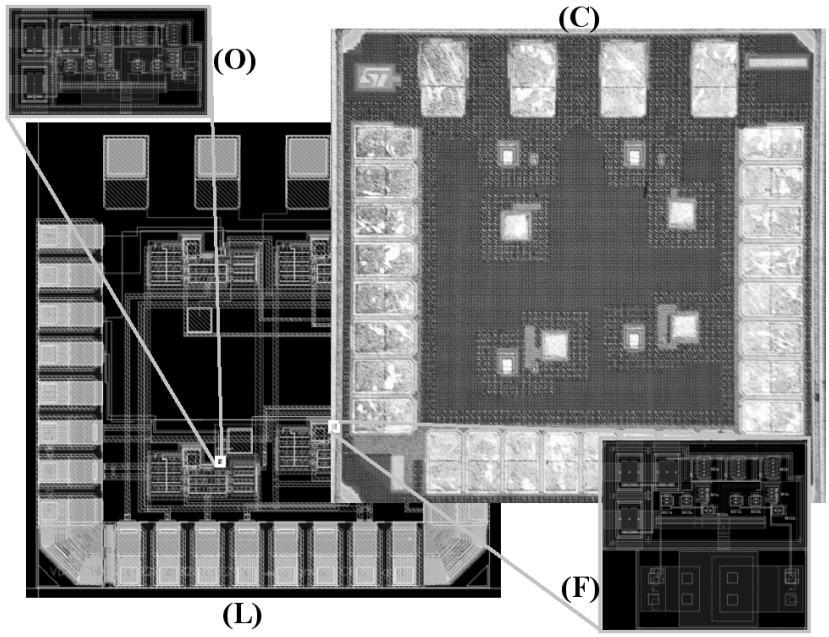

Figure 8.4: Layout (L) and chip photograph (C) of the fabricated circuits. The die (C) measures about 1 mm $\times$ 1 mm. Amplifier type (O) measures 20 μm $\times$ 10 μm and has a coupling capacitor on top of the circuit. Amplifier type (F) measures 20 μm $\times$ 18 μm and has the coupling capacitor away from the circuit.

8.4 Simulation and Measurement Results

Although the circuit is mainly intended for intravenous applications (i.e., a constant operating temperature of about 37 °C), the measurements were done at room temperature due to practical reasons. In this section, we present the measurement results and the simulations at 27 °C, even though the amplifiers were designed for operation at 37 °C.

Simulated results are reported for the slow-slow (SS) corner, because the chip batch we received performed closest to the foundry's SS models.

Fig. 8.5 shows the typical gain frequency plot of the amplifier. The maximum gain variation within the desired amplifier passband (20–50 MHz) for any tested amplifier was not higher than 0.6 dB.

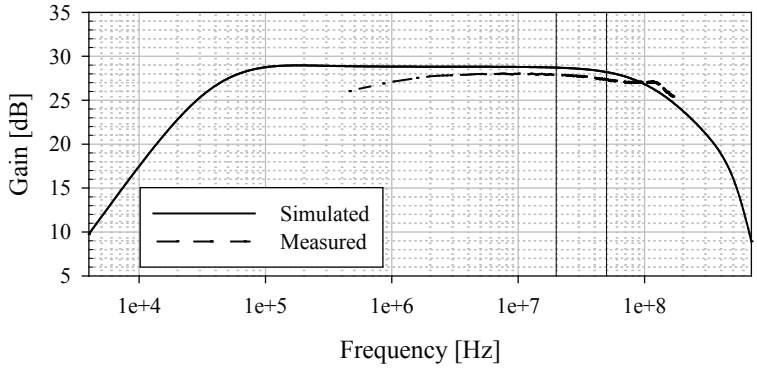

Figure 8.5: Simulated and measurement gain plots for the amplifiers. CMUT passband (20–50 MHz) is marked with solid vertical lines in the graph.

Fig. 8.6 shows the plots of output noise power measurements and simulations done on the amplifiers within the CMUT passband (20–50 MHz) for different bias currents. In Fig. 8.7, the output noise power spectral density (PSD) of the amplifier at 30 MHz (the CMUT central frequency) is plotted versus the amplifier bias current.

The output noise of the cascaded amplifier was dominated by the noise of input device M1a and active load M2a. The contribution of the subthreshold biasing devices to the total output noise voltage was just a small fraction of the noise contribution of the active devices of the first stage. The main features of the amplifier are summarized in Table 8.1.

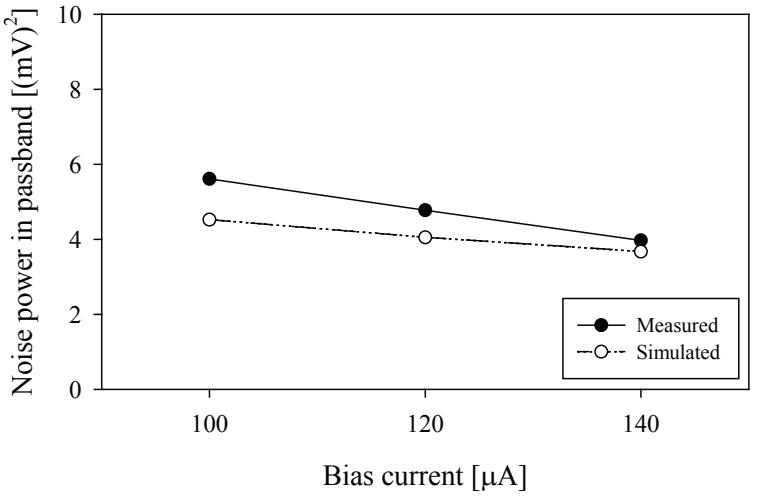

Figure 8.6: Measured and simulated output noise power within 20–50 MHz (CMUT passband) at different bias currents.

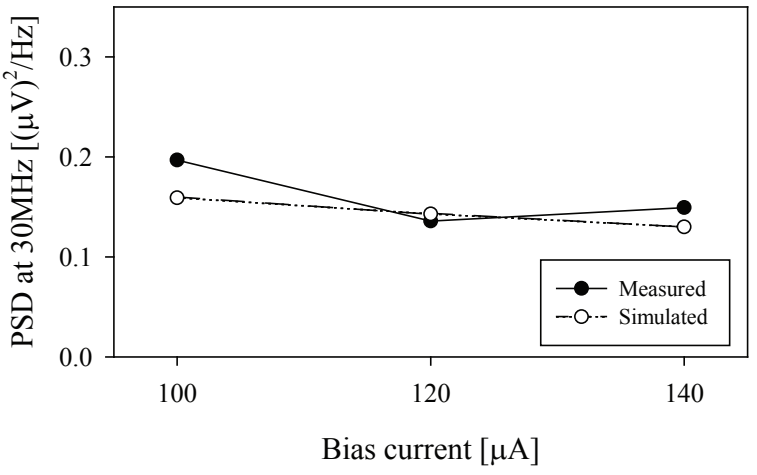

Figure 8.7: Measured and simulated output noise PSD at 30 MHz (the CMUT center frequency) at different bias currents.

Table 8.1: Summary of Main Results

Parameter	**Type / Value**	
	Simulated	*Measured*
Voltage gain at 30 MHz	28.5 dB	27.5 dB
Gain variation within passband (20 MHz–50 MHz)	0.4 dB	0.6 dB
Output DC level	0.577 V	0.537 V
Output noise PSD at 30 MHz	0.14 $(\mu V)^2$/Hz	0.11 $(\mu V)^2$/Hz
THD at FS output at 30 MHz	−26.33 dB	−30 dB
Input impedance (RC)	R = 6 MΩ C = 7 fF	
Current consumption (1 V power supply)	120 μA (without biasing current mirror)	
Area	20 μm × 10 μm	

Values measured / simulated at room temperature (27 °C) with a nominal bias current of 120 μA.

8.5 Conclusion

We have presented the application of feedback biasing to CS amplifiers realized by nanoscale CMOS technology. It has been shown that the classic disadvantage of feedback biasing, i.e., limited output swing, vanishes as one moves to nanoscale technologies. The simulation and measurement results of the CS amplifiers with feedback biasing in 90-nm CMOS have been presented. By using minimum-feature-size subthreshold MOSFETs as feedback resistors, we were able to produce amplifiers with a very small form factor. Additional area was further saved by placing the coupling capacitor over the amplifier, without having any detrimental affect on the amplifier performance.

Acknowledgment

The authors would like to thank T. Barlindhaug for designing the PCBs used for prototype testing.

Chapter 9

Paper 6

Compensating for non-linearity in feedback biased common-source amplifiers using MOS feedback resistors

Tajeshwar Singh, Trond Sæther and Trond Ytterdal
Submitted to:
IET Electronics Letters, 2009.

Abstract

A simple method for compensating the non-linearity introduced due to the use of sub-threshold MOSFETs in feedback biasing of common source (CS) amplifiers is presented. The compensation can be achieved with a single additional MOS transistor and it can improve the distortion performance by more than 100% in the best case. The simulated results are compared with measured data and a good agreement is found.

9.1 Introduction

Feedback biasing is one of the simplest methods for biasing CS amplifiers [SS04]. Non-proportional scaling of the MOSFET threshold voltage versus the power supply voltage with technology generation (gate length) makes feedback biasing a viable biasing method in nanoscale CMOS technologies [5]. The high value biasing resistor can be easily realized using MOSFETs operating in the sub-threshold region, where they exhibit a very high incremental resistance [HC03]. One problem, however, when using MOSFETs

instead of conventional resistors is that their resistance is non-linear. Although the feedback-biased CS amplifiers can be designed in such a way that this non-linear resistance does not affect the small-signal gain, this non-linear property can still affect the large signal behavior of the amplifier and introduce significant non-linearity. This Letter proposes a simple modification to such an amplifier that, for our application, improved the linearity performance by 100% in the best case.

9.2 Feedback biasing in nanoscale technologies

A feedback-biased CS amplifier is shown in Fig. 9.1 (a). Such biasing ensures that the input device is biased in the active region irrespective of the process and temperature variations. Besides requiring a large enough feedback resistor (R_G) (that can be realized as sub-threshold MOSFETs, see Fig. 9.1 (b)) to ensure wide enough bandwidth, one of the classic disadvantages of feedback biasing has been the restricted output voltage swing – that can be a serious limitation. Fortunately, this restriction is removed in nanoscale CMOS technologies, thanks to the non-proportional threshold voltage scaling of the MOSFETs [5]. Ignoring MX2 for now, the two diode connected devices MX1 and MX3 shown in Fig. 9.1 (b) are used in series to ensure that they are always in sub-threshold, hence guaranteeing a large enough resistance. The circuit can easily be designed such that the feedback effect is limited to controlling the bias point (low frequencies) and that feedback resistance value does not influence the voltage gain of the amplifier – by ensuring that the loop-gain response of the feedback loop is less than unity within the amplifier passband.

9.3 Non-linearity with MOSFETs as feedback devices

Resistors realized using sub-threshold MOSFETs can achieve very high, but non-linear, resistance values. This non-linear influence cannot be seen while observing the small-signal operation. But, it can affect the amplifier linearity. In out case, by leading to a significant shift in the bias point especially while handling large voltage swings. This can be explained as follows. The role of the biasing network in such a capacitively coupled amplifier is to keep the amplifier input (and output) at a desired operating point. When a conventional resistor is used as shown in Fig. 9.1 (a), the bias point will be maintained for symmetrical positive and negative input voltage swings.

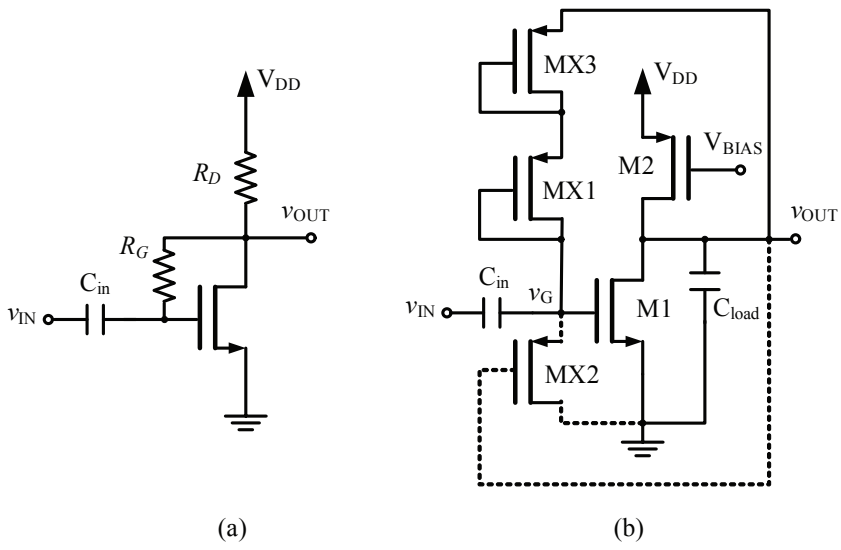

Figure 9.1: A feedback biased common-source (CS) amplifier with R_G and R_D as feedback and load resistors respectively and, (b) a typical full-CMOS realization using sub-threshold devices as feedback resistance.

This is not the case when sub-threshold devices MX1 and MX3 are used. The effective resistance of the MX1-MX3 path (say denoted by $\mathrm{R_{up}}$) is dependent on the voltage drop across them (say, $V_{up} = V_{out} - V_g$), i.e., $\mathrm{R_{up}}$ reduces as V_{up} increases and vice versa. The difference between the maximum and minimum value of R_{up} is typically very large (several orders of magnitude). Since the input bias is set by the output voltage, the problem arising with such a behavior is that during the positive excursion of V_{out}, there is a larger current flowing from the output to the input into charging the input capacitance, than the current flowing out while V_{out} goes in the opposite direction. In other words, due to asymmetric resistance R_{up} of the feedback path, there is a net positive charging of the input capacitance that results in shifting of the output bias level towards the negative power rail. This not only causes shift in the DC level, but also increases distortion in the amplifier stage. In order to compensate this shift, the excessive charge needs to be drained from the input capacitance. This can be achieved by placing MX2 in the circuit as shown in Fig. 9.1 (b). PMOS transistor MX2 results in an effective resistance (say R_{dn}) that has inverse dependence on the output swing as compared to R_{up}. The effect of R_{up} and $\mathrm{R_{dn}}$ on the circuit operation is depicted in Fig. 9.2. During the positive excursion of V_{out}, R_{up} decreases while R_{dn} increases and vice versa. Therefore, at low

V_{out}, the low resistance of MX2 helps the charge on the input capacitance to escape, hence restoring the bias point. Hence, inclusion of MX2 in the circuit compensates for the non-linearity introduced into the amplifier by non-linear resistance of MX1-MX3.

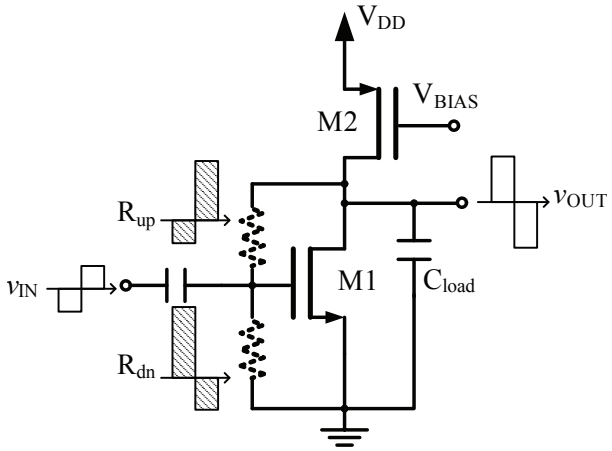

Figure 9.2: Dependence of the effective resistances R_{up} and R_{dn} on the voltage swing. The levels shown are indicative only.

9.4 Results

The amplifier stage shown in Fig. 9.1 (b) is designed in 90-nm CMOS technology and is intended to be used as an interface in a capacitive micromachined ultrasound transducer (CMUT) based intravenous imaging system. The CMUT passband in our case is 20–50 MHz. To get sufficient gain (around 30 dB total), two such stages were used in cascade with a coupling capacitor of 50 fF to isolate the DC levels. The amplifiers were designed with a 1 V power supply and output DC level of around 0.5 V, an output swing of 0.5 $V_{\text{p-p}}$ and 150 MHz −3-dB frequency. Fig. 9.3 shows the Monte Carlo simulations for the total harmonic distortion (THD), at maximum output swing (0.5 $V_{\text{p-p}}$) at 50 MHz, including random mismatch of all transistors of both stages. The benefit of using MX2 is clearly evident. In our case, MX2 was designed at minimum device size to keep its resistance much higher as compared to the resistance of MX1-MX3 feedback path, to have minimum affect on the system gain and input resistance of the amplifier. Hence, in the results shown in Fig. 9.3, the benefit in linearity is observed even though the resistance of MX2 and the MX1-MX3 path are not exactly matched.

In in Fig. 9.4 (a)-(d), the simulated and measured plots for the second order harmonic (HD2), third order harmonic (HD3), total harmonic distortion (THD), and third order intermodulation product (IM3) are plotted versus frequency for different output swings. In each case, FS refers to full-scale output swing i.e., when the output swing is 0.5 $V_{p\text{-}p}$. The plots show that the measurement results are in close agreement with the simulations.

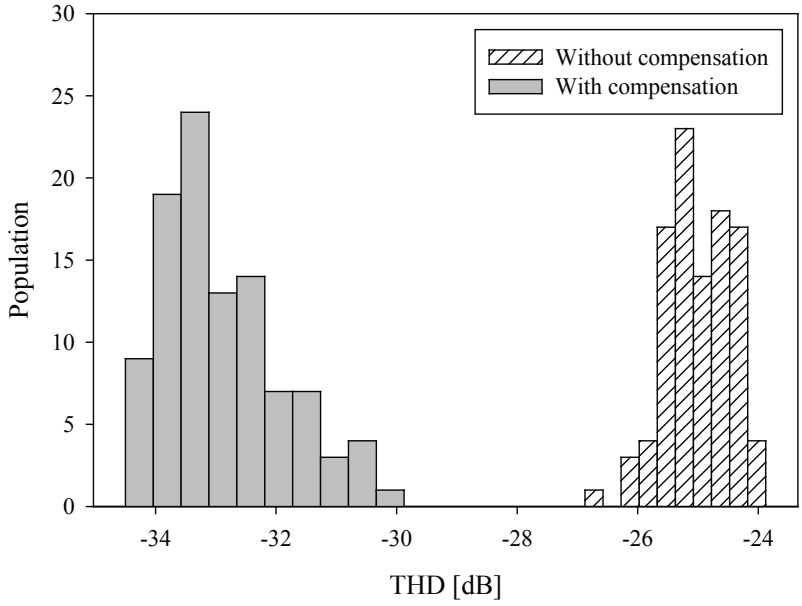

Figure 9.3: Monte Carlo simulation results for circuits showing linearity performance at 50 MHz, with and without compensation. The circuits were simulated with the same input signal amplitude that resulted around 0.5 $V_{p\text{-}p}$ output swing.

9.5 Conclusion

The impact on the linearity of the CS amplifier when using sub-threshold MOSFETs as feedback resistors is discussed and a possible compensation method shown that results in noticeable improvements in the linearity performance.

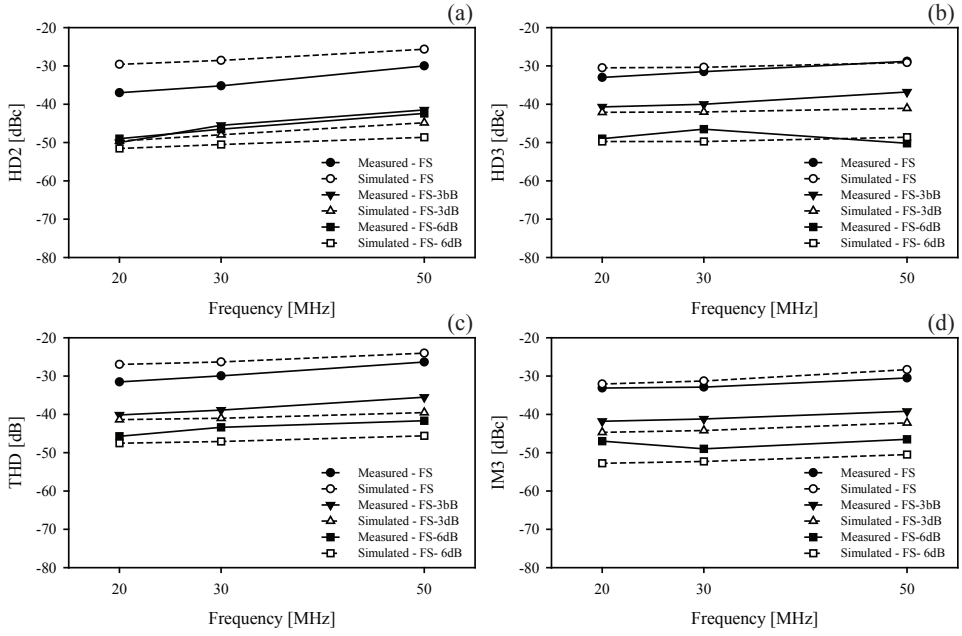

Figure 9.4: (a) Second order harmonic (HD2), (b) third order harmonic (HD3), (c) total harmonic distortion (THD), and (d) third order intermodulation product (IM3) plotted versus frequency and at different output swings. Full-scale swing (FS) refers to 0.5 $V_{p\text{-}p}$ output swing.

9.6 Acknowledgments

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Chapter 10

Conclusion

Capacitive sensing has found an extensive application in the field of microsystems such as integrated sensor applications, MEMS etc. Due to steadily increasing use of microsensors and MEMS based devices, capacitive sensing is going to be an important approach, also for upcoming large-scale market applications such as touch screens. *Low-power* and *low-voltage* are the other two key phrases that perhaps have never been more important before, and it is easy to say that they will continue to be heard more and more, as battery based applications increase and as voltage headrooms shrink in nanoscale technologies. As the arsenal of usable high performance circuit topologies (for example, cascoding) reduces for an analog designer, there are design challenges in store for capacitive sensing as well.

Due to ongoing quest to achieve high density of sensors in certain applications such as CMUTs for intravenous imaging, compact and efficient sensor interfaces are an important requirement due to tight area and power budgets. Since most classical performance enhancing techniques in analog circuit design become hard to apply in nanoscale CMOS, the only option is to use the basic analog building blocks such as a common-source amplifier. It is well known that the nanoscale CMOS technologies have made the analog design more challenging, not only by reducing the set of useful circuit topologies, but also due to poorer device parameters (such as intrinsic gain). However, it is sometimes also possible to use some of these, otherwise limiting properties to one's benefit. For example, as demonstrated in this thesis that the non-proportional scaling of the threshold voltage actually helps in the application of feedback biasing. The end result is a very simple and area effective amplifier. An amplifier based on such a design, targeted towards CMUT applications has been demonstrated in a commercially available 90-nm CMOS technology.

Another motivation behind using a voltage amplifier has been to investigate the voltage sensing approach to detect the CMUT signals. TIA based interfaces have been widely used in CMUT based designs so far, but there is not enough justification to reject the voltage sensing approach altogether. An advantage with CMUTs is that they can be optimized for voltage sensing as well. Therefore, more work is needed to say for sure that which approach is the best for sensing application in CMUT based systems.

Two other approaches for application in capacitive sensing were also presented. Both of these are able to produce differential outputs also from single-ended sensors.

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