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Efficient ADCs for nano-scale CMOS Technology

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Abstract

The topic of this thesis is efficiency of analog-to-digital converters (ADC) in nano-scale CMOS technology. With downscaling of CMOS technology it is harder to design ADCs. The power supply is reduced due to reliability concerns and the output resistance of transistors is reduced because of shorter channel lengths. Such challenges makes it harder to design ADCs with conventional circuit techniques and ADC architectures.

We investigate two separate paths towards higher efficiency in nano-scale CMOS technologies: circuit implementation, and ADC architectures.

The research into ADC architectures assumes that circuit implementation challenges will be solved. It looks at how a sigma-delta modulator can be used as a front-end to pipelined ADCs. A new class of sigma-delta modulators, the switched-capacitor (SC) open-loop sigma-delta modulator (OLSDM) is introduced. We introduce the SC modulo integrator and the SC modulo resonator that facilitates implementation of sigma-delta modulators that do not have feedback of the quantized signal. Thus, high-latency converters such as pipelined ADCs can be used as quantizers. Limitations of OLSDM, like operational amplifier (opamp) DC gain, quantizer linearity, and input signal amplitude are discussed in detail. Behavioral simulations of OLSDMs confirm the theory.

The research into circuit implementations investigate how the opamp can be removed from SC circuits. Two techniques are investigated: open-loop residue amplification and comparator-based switched-capacitor circuits (CBSC).

We present the design of a 7-bit 200MS/s 2mW pipelined ADC based on switched open-loop residue amplifiers. By turning off the open-loop

amplifiers when they are not needed the power dissipation is reduced by 23%.

Comparator-based switched-capacitor circuits (CBSC) are an alternative to opamp based SC circuits. By replacing the opamp with a comparator and current sources the same charge transfer is achieved.

We discuss design equations for CBSC, and how one can model CBSC in MATLAB and SPICE.

We present an 8-bit 60MS/s 8.5mW pipelined ADC with 7.05-bit effective number of bits (ENOB). At the time of writing it was the first silicon proven differential CBSC pipelined ADC.

Preface

This thesis was submitted to the Norwegian University of Science and Technology (NTNU) in partial fulfilment of the requirements for the degree of philosophiae doctor (PhD). The work presented herein was conducted at the Department Electronics and Telecommunication, NTNU, under the supervision of Professor Trond Ytterdal, with Professor Trond Sæther as co-advisor. Financial support from the Norwegian Research Council through the project Smart Microsystems for Diagnostic Imaging in Medicine (project number 159559/130) and the project ASICs for Microsystems (project number 133952/420) is gratefully acknowledged.

Research Path

This is a document that has been four years in the making. I began by my work in January 2004. The intent was to investigate calibration algorithms for micro-systems, with focus on genetic algorithms. But I strayed from this path and found analog-to-digital converters. The project Smart Microsystems for Diagnostic Imaging in Medicine (SMIDA) needed a low resolution high speed ADC, and I was asked to build it. This led to some initial work on dynamic comparators, opamps in 90nm CMOS and bootstrapped switches.

Wislands doctoral thesis (2003) on *Non-feedback Delta-Sigma modulators for digital-to-analog conversion* peaked my interest. We[1] wanted to see if we could apply the open-loop sigma-delta technique to analog-to-digital

[1] Trond Ytterdal and I

converters. We believed they could be used as front-ends to pipelined ADCs. In that respect, we developed techniques for switched-capacitor circuits.

At ISSCC 2006 the first comparator-based switched-capacitor circuit was published, and we immediately jumped on it. From the summer of 2006 to the summer of 2007 my time was dedicated to tape-out the first differential comparator-based switched-capacitor ADC. That year I was fortunate to spend my time at the University of Toronto as a visiting researcher. The time in Toronto inspired much of my work, like the open-loop residue amplifiers for pipelined ADC, and the continuous time bootstrapped switches.

My chip came back in January 2008, and most of the spring was spent on making the chip work. On the first day I got 4.2-bit ENOB, and it took me four months to get to 7.05-bit.

As these four and a half years draw to a close, I find that I am satisfied. In a sense I have come full circle with the genetic algorithm used to calibrate my ADC.

Acknowledgements

- To my wife, Anita, without her this thesis would not have seen the light of day. She was willing to move half way around the world with me, for which I am forever grateful.
- To my son, Villem, born during my years as a PhD student you have shown me that it's possible to get up at 05:30 A.M and still survive the day. This has been immensely helpful. Your smiles and hugs brighten my mood after a long day at work.
- To my late mother, my dad, my sisters and my extended family for your love and support.
- To my supervisor, Trond Ytterdal, he has always been available for questions and his guidance is valued. He has provided the resources necessary to do this work.
- To my co-advisor, Trond Sæther, for his support and convincing me that analog integrated circuits was the way to go.

- To my colleagues at Department of Electronics and Telecommunication, Circuits and Systems Group for lunch discussions, coffee sessions and support.

- To my fellow PhD students for many fun discussions: Øystein Gjermundnes, Ashgar Havashki, Are Hellandsvik, Tajeshwar Singh, Ivar Løkken, Anders Vinje, Saeeid Tahmasbi Oskuii, Linga Reddy Chenkeramaddi and Bertil Nistad.

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- A special thanks to Professors Ken Martin and David Johns for many useful questions and suggestions.

Comments on style

In a break from conventional page numbering this thesis start with page number 1 on the title page. In this digital age it is likely that this thesis will be read on a computer. As the title page is page one, the page numbers of the thesis will match the page numbers of the electronic document. I believe this will make the thesis easier to navigate.

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List of abbreviations

ADC	Analog-to-digital converter
ADSL	Asymmetric digital subscriber line
ASIC	Application specific integrated circuit
CBSC	Comparator-based switched-capacitor
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analog converter
DC	Direct current
DITS	Drain-induced threshold shift
DIBL	Drain-induced barrier lowering
DNL	Differential non-linearity
DRAM	Dynamic random access memory
ENOB	Effective number of bits
ERBW	Effective resolution bandwidth
FFT	Fast Fourier transform
FOM	Figure of merit
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral non-linearity
IO	Input - Output
ISSN	International Standard Serial Number
ITRS	International Technology Road-map for Semiconductors
JSSC	Journal of solid state circuits
GPRS	General Packet Radio Service
LDI	Lossless discrete integrator
LSB	Least significant bit

LC-SDM	Low-pass Conventional Sigma-Delta Modulator
L-SDM	Low-pass Sigma-Delta Modulator
MASH	Multi-stAge noise SHaping
MDAC	Multiplying digital-to-analog converter
MOSFET	Metal oxide semiconductor field effect transistor
MSB	Most significant bit
NMOS	n-channel MOSFET
NTF	Noise transfer function
NTNU	Norwegian university of science and technology
NUD	Number of unit devices in parallel
OLSDM	Open-loop sigma-delta modulator or open-loop sigma-delta modulation
opamp	Operational amplifier
OSR	Oversampling ratio
PMOS	p-channel MOSFET
PSD	Power spectral density
RMS	Root mean square
SADC	Sub analog-to-digital converter
SAR	Successive approximation register
SC	Switched-capacitor
SDM	Sigma-delta modulation
SFDR	Spurious free dynamic range
SMIDA	Smart Microsystems for Diagnostic Imaging in Medicine
SNDR	Signal to noise and distortion ratio
SNR	Signal to noise ratio
SoC	System-on-Chip
SPICE	Simulation Program With Integrated Circuit Emphasis

List of appended papers

1. Analog Modulo Integrator For Use In Open-Loop Sigma-Delta Modulators

Carsten Wulff, Øystein Knauserud, Trond Ytterdal

In proceedings of the 24th NORCHIP Conference, 2006.

Nov. 2006 Pages 125 - 128

Digital Object Identifier 10.1109/NORCHP.2006.329259

2. Switched capacitor analog modulo integrator for application in open loop sigma-delta modulators

Carsten Wulff, Øystein Knauserud, Trond Ytterdal

Analog Integrated Circuits and Signal Processing

Springer Netherlands, ISSN 0925-1030

Volume 54, Number 2, Pages 121-131 February 2008

DOI 10.1007/s10470-007-9084-2

3. Resonators in open-loop sigma-delta modulators

Carsten Wulff and Trond Ytterdal

Submitted to IEEE Transactions on Circuits and Systems I: Regular Papers

4. 0.8V 1GHz Dynamic Comparator in Digital 90nm CMOS Technology

Carsten Wulff and Trond Ytterdal
In proceedings of the 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005 Pages 237 - 240
Digital Object Identifier: 10.1109/NORCHP.2005.1597033

5. Design of a 7-bit 200MS/s, 2mW Pipelined ADC With Switched Open-Loop Amplifiers In a 65nm CMOS Technology

Carsten Wulff and Trond Ytterdal
In proceedings of the 25th NORCHIP Conference, 2007.
Digital Object Identifier 10.1109/NORCHP.2007.4481042

6. Design and Behavioral Simulation of Comparator-Based Switched Capacitor Circuits

Carsten Wulff and Trond Ytterdal
Accepted at NORCHIP 2008

7. An 8-bit 60-MS/s 8.5mW Differential Comparator-Based Switched-Capacitor Pipelined ADC in 90nm CMOS Technology

Carsten Wulff and Trond Ytterdal
Submitted to IEEE Journal of Solid State Circuits

The following papers have also been published. Because they fall outside the theme of this thesis they are not included in the thesis.

A Next Generation Lab - A Solution for remote characterization of analog integrated circuits

Carsten Wulff, Trond Ytterdal, Thomas Aas Saethre, Arne Skjevlan, Tor A. Fjeldly and Michael S. Shur

Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, April 17-19, 2002.

B Programmable Analog Integrated Circuit for use in remotely operated laboratories

Carsten Wulff and Trond Ytterdal
International Conference on Engineering Education, ICEE-2002
August 18-21, 2002, Manchester, U.K.

C Programmable Analog Integrated Circuit

Carsten Wulff, Roger Erstad and Trond Ytterdal
In Proceedings of the 22nd NORCHIP Conference, 2004.
Nov. 2002, Pages 99 - 102

D High Speed, High Gain OTA in a Digital 90nm CMOS Technology

Øyvind Berntsen, Carsten Wulff, Trond Ytterdal
In proceedings of 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005

E Bootstrapped Switch In Low-Voltage Digital 90nm CMOS Technology

Christian Lillebrekke, Carsten Wulff and Trond Ytterdal
In proceedings of 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005

F New Approach for Continuous Time Sigma Delta Modulators

Francisco Colodro, Marta Laguna, Carsten Wulff, Trond Ytterdal and Antonio Torralba
In proceedings of 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005

Chapter 1

Introduction

How can we make efficient analog-to-digital converters (ADCs) in nano-scale CMOS? Challenges like reduced headroom and reduced output resistance has made it hard to design efficient ADCs in the new nano-scale CMOS technologies. Why do we want more efficient ADCs? The simple answer is: longer battery life. The ADC is a key component in any signal chain that interface with the real world. The receive chain of GPRS networks, Wi-Fi networks, indeed any current mobile wireless communication technology has an ADC. Most of the processing today is done in the digital domain. The pure analog signal chains have been banished to obscurity. But the real world is analog, and information from the real world must be converted to digital before it can be digitally processed.

Consumers demand high speed mobile networking on the bus to work, at the local cafe, and in their homes. They want their portable devices to have infinite battery lives, and they should cost nothing. To reduce the cost and increase efficiency there has been a push for integration of features on a single chip (System-on-Chip). In SoCs with high integration most of the functions are digital, thus technologies that allow cheap integration of digital features are used. These are the nano-scale technologies (less than 100nm transistor gate length).

Reliability concerns of downscaled CMOS transistors has lead to a decrease in power supply. At high electrical fields the transistor gate oxide

breaks down. In downscaled transistors the thickness of the gate oxide is reduced, hence the maximum power supply must be reduced. Fig. 1.1 shows the historic power supply and future trends (from ITRS 2007 [1]). At the 250nm gate length the power supply is 2.5V, but in 90nm the power supply is reduced to 1.2V.

A challenge with reduced power supply is the reduced signal swing, in most cases the signal swing cannot be larger than the power supply. The accuracy of an ADC is proportional to sampling capacitance[1], and sampling capacitance is inversely proportional to the square of the signal swing. Hence, the capacitor size quadruples when we go from 250nm to 90nm CMOS technology for the same accuracy. An increased capacitor size result in higher area consumption and increased cost.

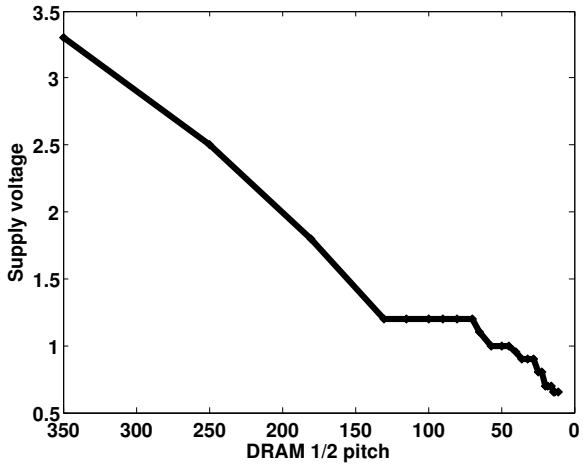


Fig. 1.1: Historic and future scaling of power supply (based on ITRS 2007 [1]). DRAM 1/2 pitch is smallest half-pitch of contacted metal lines in a DRAM cell.

Another challenge is the reduced output resistance of nano-scale CMOS transistors. As devices are scaled down the transistor channel lengths

[1]This is easily seen from the equation

$$S/R = \frac{Signal\ Power}{Noise\ Power} = \frac{A^2/2}{kT/C} = \frac{A^2C}{2kT} \tag{1.1}$$

shorten. At shorter channel lengths channel length modulation and drain induced barrier lowering [2] reduce the output resistance of the transistor. Longer channels can be used to increase the output resistance, but the effectiveness of using a longer channel is reduced by the pocket implants [3]. Pocket implants are used to reduce V_T roll-off and punch-through in nano-scale technologies. Due to the pocket implants the output resistance of a 1μm long transistor in a 90nm technology is lower than a 1μm long transistor in a 350nm technology.

For high accuracy circuits we need high gain in our transistors. The gain in a transistor is proportional to the output resistance of the transistor. The gain of the single transistor is called the intrinsic gain. It is defined as $A_i = g_m/g_{ds}$, where g_m is the transconductance and g_{ds} is the output conductance (inverse of output resistance). When the output resistance is reduced the intrinsic gain goes down, and in 65nm technology the intrinsic gain of a minimum device is 6[2] (15-dB). In 350nm technology a minimum device has a gain of 43[3] (32-dB). As a result, one must use multiple stages, cascoding, or gain boosting to achieve high gain amplifiers in 65nm technology. But techniques like cascoding (stacking transistors) is hard in 65nm technology due to the low supply voltage.

Downscaling of analog circuits is not all bad. The speed can be increased due to shorter channel lengths, and the parasitic capacitances are smaller. But these two advantages are overshadowed by the reduction in gain and power supply.

We believe that efficiency in nano-scale technology is best attacked from both ends: the circuit implementation, and the ADC architecture.

One approach to efficiency is to investigate the architectural level. If we assume that the circuit challenges can be solved, can we do anything about the ADC architectures? High accuracy (14-bit) high-speed ($>$ 10MS/s) ADCs are challenging to implement in nano-scale technologies because of the large sampling capacitors. With a 1V input signal swing the sampling capacitors will be 53pF for a 14-bit converter, which is a large capacitor.

[2] $L = 0.06$, $W = 10L$, $V_{DS} = V_{DD}/2$, $V_{EFF} = V_{DD}/8$, typical corner
[3] $L = 0.35$, $W = 10L$, $V_{DS} = V_{DD}/2$, $V_{EFF} = V_{DD}/8$, typical corner

To reduce the sampling capacitor we can use oversampling. In sigma-delta modulators oversampling is used in addition to quantization noise shaping to achieve high accuracy. We wanted to investigate a class of sigma-delta modulators called *Open-Loop Sigma-Delta Modulators* (OLSDM), and their use as a front-end to pipelined ADCs. The part of this thesis that focus on OLSDM is of a theoretical nature.

The other approach to increased efficiency is to investigate the circuit implementation. Switched-capacitor (SC) circuits are ubiquitous in ADCs. They are a tried and tested accurate method of implementing high speed ADCs. The sigma-delta modulators and pipelined ADCs predominate in the use of SC circuits. The traditional approach to SC circuits use opamps, which consume most of the power in an ADC. In nano-scale technology opamps have become increasingly hard to design due to the reduced headroom and decreased output resistance. Techniques that replace opamps have received interest from the research community. Part of this thesis investigate how one can replace opamps in pipelined ADCs, and through this improve efficiency. This part of the thesis is a combination of theoretical work and measurements on a nano-scale CMOS ADC.

1.1 Main contributions

The main contributions of this thesis are:

- We introduce the switched-capacitor modulo integrator. It facilitates implementation of switched-capacitor open-loop sigma-delta modulators.

- We introduce the switched-capacitor open-loop sigma-delta modulator. A versatile type of sigma-delta modulator suited as front-end to pipelined ADCs

- We introduce the modulo resonator. It enables implementation of high resolution open-loop sigma-delta modulators with low oversampling ratio.

- We prove that open-loop sigma-delta modulation is equivalent to sigma-delta modulation if

$$|x_n| < R\left(\frac{1}{2} - \frac{2^{N-1}}{2^B}\right) \tag{1.2}$$

  where x_n is the input signal at time n, R is the full scale range, N is the order of the modulator and B is the number of bits in the quantizer.

- We introduce the switched open-loop residue amplifiers. Using these the power dissipation is reduced by 23% for a 7-bit pipelined ADC.

- We introduce the first fully differential silicon proven comparator-based switched-capacitor pipelined ADC. Differential implementation allow higher signal swing, which is essential in nano-scale technologies.

Other significant contributions are:

- We present a comprehensive figure of merit survey of ADCs in Journal of Solid State Circuits (1975-2008) and International Solid State Circuits conference (2000-2008).

- We present the limits of figure of merit for ADCs

- We present design equations for comparator-based switched-capacitor circuits.

- We introduce a simple calibration scheme for comparator threshold calibration. This technique cancels the overshoot in comparator-based switched-capacitor pipelined ADCs

1.2 Thesis outline

This thesis is a collection of papers, hence the results are in the papers. The research presented in this thesis is on analog-to-digital converters, with focus on pipelined ADCs and sigma-delta modulators. If this subject is unfamiliar we suggest reading Chapters 9, 10, 11, 13 and 14 in [4].

This thesis is organized as follows: Chapter 2 discuss the fundamental limits of ADC figure of merit, and how parasitic capacitance make it hard to implement a low resolution converter with high efficiency.

In Chapter 3 the papers are introduced and we detail how the papers are related. The papers are presented in Chapter 4 to Chapter 10. Comments to papers, a conclusion and further work is presented in Chapter 11

Chapter 2

Limits of ADC figure of merit

Efficiency is one of the key measures of analog-to-digital converters. A more efficient ADC can translate into longer battery life of our hand-held devices. For ADCs the power dissipation (P), sampling frequency (f_s) and effective number of bits (B) are combined to give a single measure of the efficiency, the figure of merit (FOM). For the figures of merit discussed here a smaller value is better.

The historic figure of merit proposed by Walden [5] was (2.1)[1]

$$FOM = \frac{P}{2^B f_s} \tag{2.1}$$

This FOM, however, is incorrect if we assume the ADCs should be limited by thermal noise. A more correct figure of merit is

$$FOM = \frac{P}{2^{2B} f_s} \tag{2.2}$$

This figure of merit, the Thermal FOM, is based on the fact that in an ADC limited by thermal noise we must use 4 times the power if we add one bit of resolution, since the required sampling capacitance increases 4 times.

[1] It was actually presented as $FOM = 2^B f_s/P$, but the inverse is the most used.

A more in-depth argument is given in [6] on page 360.

If we have the ADC parameters (accuracy, power dissipation, speed) we can calculate the FOM from (2.2). But what is the limit of the FOM? How low FOM can we expect to get with future ADCs?

We will in this chapter derive expressions for the FOM limit and compare the limit to results of published ADCs. But first we have to derive the required sampling capacitance for a certain resolution.

2.1 Required sampling capacitance

We assume a switched-capacitor based ADC. The input signal is sampled across a sampling capacitor (C). And C is the only capacitor in the ADC. In such a system the thermal noise power can be represented as

$$\overline{V_{thermal}^2} = a_1 \times kT/C \tag{2.3}$$

where a_1 is a constant greater than one, k is Boltzmann's constant, T is the temperature in Kelvin and C is the sampling capacitance.

The thermal noise power should be less than the quantization noise power, but not too small, because a small thermal noise power will cost in terms of power dissipation. We assume that the quantization noise power is four times the thermal noise power.

$$\overline{V_{LSB}^2} = 4 \times \overline{V_{thermal}^2} \tag{2.4}$$

where $\overline{V_{LSB}^2}$ is the quantization noise power, which can be calculated as

$$\overline{V_{LSB}^2} = V_{LSB}^2/12 = V_{PP}^2/(2^{2B} \times 12) \tag{2.5}$$

where V_{LSB} is the voltage step of the least significant bit (LSB) and V_{PP} is the peak-to-peak input signal voltage.

If we combine (2.3), (2.4) and (2.5) we get

$$\frac{V_{PP}^2}{2^{2B} \times 12} = 4 \times a_1 \times kT/C \tag{2.6}$$

Solved for sampling capacitance (C) (2.6) becomes

$$C = a_1 \times \frac{48kT2^{2B}}{V_{PP}^2} \tag{2.7}$$

Using equation (2.7) we can calculate how large C must be for a certain resolution. For example for $V_{PP} = 1\,V, T = 300\,K$ we get $C_{[B=6]} = 0.8fF$, $C_{[B=12]} = 3.3pF$, and $C_{[B=14]} = 53pF$.

Assume the capacitor is used in a switched capacitor circuit, and that an amplifier is used to charge the capacitor to its final value. We will consider two methods for this capacitance to reach its final value: a constant ramp, and linear settling. Constant ramp is equivalent to what is used in comparator-based switched-capacitor circuits. Linear settling is equivalent to what is used in opamp based switch-capacitor circuits and open-loop residue amplifiers.

2.2 Constant ramp FOM limit

For a constant ramp the voltage across C is given by

$$V_o(t) = \frac{I}{C} \times t \tag{2.8}$$

where $t = 1/2f_s$, I is the current used to charge the capacitor, and f_s is the sampling frequency.

The maximum $V_o(t)$ is equal to V_{PP}, and will require the most time. Accordingly, we set $V_o(t) = V_{PP}$, insert for (2.7) in (2.8), and multiply each side with V_{DD}

$$V_{PP}V_{DD} = \frac{IV_{DD}V_{PP}^2}{96a_1kT2^{2B}f_s} \tag{2.9}$$

Solved for FOM (2.9) becomes

$$FOM_{ramp} = \frac{P}{2^{2B}f_s} = \frac{96a_1kT}{\frac{V_{PP}}{V_{DD}}} \tag{2.10}$$

This FOM does not depend on the number of bits (B) or the sampling

frequency (f_s).

2.3 Linear settling FOM limit

We assume the voltage across C must reach a final value within a certain accuracy, given by the LSB, and reach this accuracy within half the sampling period ($1/2f_s$).

Assume a transconductance amplifier (an ideal transistor with resistive load $R_o = 1/g_m$) is used to drive the capacitance C. The amplifier has the transfer function

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + sC/g_m} \tag{2.11}$$

where V_o is the voltage across the capacitance, V_i is the input signal voltage, and g_m is the transconductance.

Assume the input is a unit step function $V_i(t) = V_{PP}u(t)$. The output will then be

$$V_o(t) = V_{PP} - V_{PP}e^{-g_m t/C}, t > 0 \tag{2.12}$$

Written in terms of the settling error ($\epsilon = V_{PP} - V_o(t)$) we get

$$\epsilon = V_{PP}e^{-g_m t/C} \tag{2.13}$$

The settling error (ϵ) should be smaller than one LSB, $\epsilon < V_{PP}/2^B$, but to simplify we set $\epsilon = LSB$. The transconductance in (2.13) can be written as $g_m = \eta_1 2I_D/V_{EFF}$ where η_1 is a technology dependent constant (it depends on high field effects and short channel effects, η_1 is larger than zero, but less than one. For a 90nm process it's around 0.5-0.6), I_D is the drain current and V_{EFF} is the effective gate overdrive. Inserted into (2.13) together with (2.7) results in

$$\frac{V_{PP}}{2^B} = V_{PP}\, e^{\left(-\frac{\eta_1 2 I_D \frac{V_{PP}^2}{V_{DD}^2} V_{DD}^2}{2 f_s \frac{V_{EFF}}{V_{DD}} V_{DD} a_1 48 k T 2^{2B}} \right)} \tag{2.14}$$

Solved for FOM we get

$$FOM = \frac{I_D V_{DD}}{2^{2B} f_s} = \frac{B \ln(2) \frac{V_{EFF}}{V_{DD}}}{\eta_1 \frac{V_{PP}^2}{V_{DD}^2}} a_1 48kT \tag{2.15}$$

According to this equation, it will be more difficult to get a good figure of merit with additional bits, but this ignores the influence of parasitic capacitances.

2.4 FOM limit including parasitic capacitance

Assume that an ADC has as many stages as bits (B), define M_0 as the number of circuit nodes per stage and C_0 as the parasitic capacitance per node. The total parasitic capacitance in the ADC will then be

$$C_p = C_0 M_0 B \tag{2.16}$$

The parasitic capacitance (2.16) will add to the load of our transconductance amplifier, accordingly the load will be

$$C = a_1 \times \frac{48kT 2^{2B}}{V_{PP}^2} + C_0 M_0 B \tag{2.17}$$

Inserted into (2.13)

$$\frac{V_{PP}}{2^B} = V_{PP}\, e^{\left(-\frac{\eta_1 2 I_D}{2 f_s \frac{V_{EFF}}{V_{DD}} V_{DD}} \frac{1}{\frac{a_1 48kT 2^{2B}}{V_{PP}^2} + C_0 M_0 B} \right)} \tag{2.18}$$

And with some manipulation

$$FOM = \frac{B \ln(2) \frac{V_{EFF}}{V_{DD}}}{\eta_1 \frac{V_{PP}^2}{V_{DD}^2}} \left(a_1 48kT + \frac{C_0 M_0 B V_{PP}^2}{2^{2B}} \right) \tag{2.19}$$

For $C_0 = 0$ (2.19) reduces to (2.15).

These three equations: (2.10), (2.15), and (2.19), are based on numerous assumptions, and it is interesting to see how well the equations predict published results for ADCs.

2.5 Comparison with published results

The FOM limits have been compared to selected ADCs published in Journal of Solid State Circuits (JSSC) in the years 1975-2008.[2] And selected ADCs published at the International Solid State Circuits Conference (ISSCC) in the years 2000-2008.

The comparison is shown in Fig. 2.1. We have used $V_{EFF}/V_{DD} = 1/8, V_{PP}/V_{DD} = 0.5, \eta_1 = 0.5, a_1 = 1, T = 300\ K$. Choosing the value for M_0 and C_0 is guesswork since they depend on ADC architecture and technology, but it is unlikely that $M_0 < 10$ and $C_0 < 1fF$. A more realistic model would arguably be $M_0 = 200$ and $C_0 = 10fF$.

None of the published ADCs go below the FOM limit given by (2.15) or (2.10), but for high number of bits ($>$ 14-bits) they begin to approach the limit. At high number of bits it is more straightforward to achieve a good FOM because the required sampling capacitor becomes large and the parasitic capacitances become less important. But for low to medium number of bits ($<$ 12-bits) the required sampling capacitance is so low ($<$ 4 pF) that the parasitic capacitances dominate.

At 7-bit the best ADC is more than 100 times worse than the FOM limit.

The parasitic FOM limit given by (2.19) match the shape of the data points. The realistic model ($M_0 = 200, C_0 = 10fF$) enclose most of the data points, and the likely limit ($M_0 = 10, C_0 = 1fF$) enclose all.

For ENOB larger than six bits constant ramp has an advantage over linear settling.

[2] The data for this study can be downloaded from `http://www.wulff.no/carsten` *Electronics, ADC FOM*

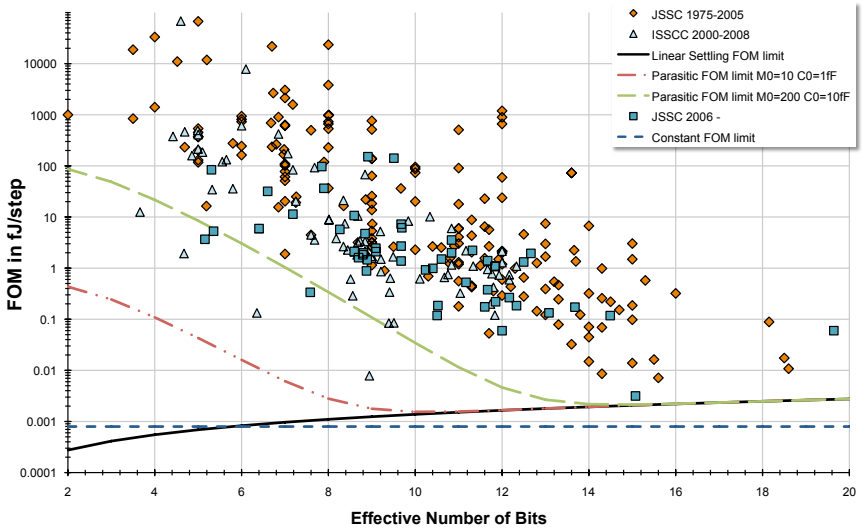


Fig. 2.1: FOM versus bits for selected ADCs published in JSSC in the years 1975-2008 and ADCs published at ISSCC 2000-2008 compared to: the FOM limit for constant ramp, FOM limit for linear settling, and the parasitic FOM model

Chapter 3

Research Overview

The research in this thesis is presented in seven papers. Fig. 3.1 shows how the papers are related. Papers 1, 2, 4, 5 and 6 are published works, while 3 and 7 are submitted for publication. The format of all papers have been modified to suit this thesis. The references for each paper has been included into the complete reference list at the end of the thesis. The content of papers 1, 2, 4, 5 and 6 have not been modified in any way from the published version.

The topic of the research is efficient ADCs in nano-scale CMOS technology. We focus on two separate paths:

1. Assume switched-capacitor implementation challenges will be solved and investigate ADCs with sigma-delta modulator front-end and pipelined back-end.

2. Investigate efficient circuit solutions for pipelined ADCs

The first path include papers 1, 2 and 3 while the second path include papers 4, 5, 6 and 7. We will describe the two paths separately.

3.1 Open-loop sigma-delta modulators (OLSDM)

The open-loop sigma-delta modulators in this thesis brings the OLSDM architecture to switched-capacitor architectures. Our motivation for creating

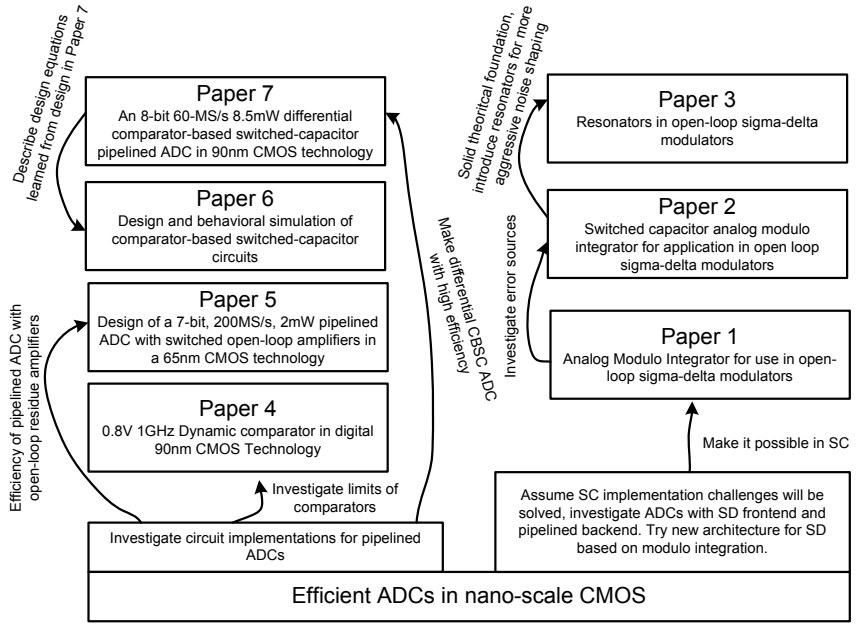


Fig. 3.1: How papers relate to each other and the central theme

an OLSDM is the use in hybrid converters. The idea is to use an OLSDM front-end and pipelined ADC back-end. Such hybrid converters can achieve good performance [7]. Previous OLSDM architectures have been digital-to-analog modulators [8], or frequency sigma-delta modulators [9].

Fig. 3.2 shows an example of why we believe an OLSDM-Pipelined hybrid might have an efficiency advantage. The figure shows a comparison between a 14-bit pipelined ADC and a 14-bit hybrid ADC. A 14-bit pipelined ADC need a sample and hold and seven 1.5-bit stages[1] if we use a 7-bit back-end ADC. The hybrid converter has 5 stages before the back-end (no sample an hold), a saving of three stages. The hybrid has two modulo resonators and a modulo integrator that result in a fifth order noise transfer function.

[1]The number of stages can be reduced if more bits are converted in each stage. This requires more comparators in each stage, a 1.5-bit pipelined stage has two comparators. The accuracy of a comparator in a B-bit stage must be $\pm V_{REF}/2^B$. Mismatch determine the accuracy of the comparators, which usually limit the number of bits per stage to 3-bits.

To clarify why we believe that OLSDM can have an advantage, we will describe some of the challenges in high-speed, high-accuracy converters. These are:

Clock skew In pipelined ADCs clock skew between the sub-ADCs and the sampling network (input switches and sampling capacitors) is a challenge. This skew (difference in delay) cause a signal dependent offset. The problem can be alleviated by placing a sample and hold before the first stage.

In the hybrid only the sampling capacitors are connected to the input. Thus, clock skew is not a problem and the hybrid does not need a separate sample and hold.

Capacitor size In a 14-bit pipelined converter with low signal swing the capacitor size can be large. For 1V peak-to-peak input swing the input capacitance has to be 53pF (from (2.7)). In 90nm CMOS this capacitance will measure 163μm by 163μm, which is a large area.

The capacitor size can be reduced by oversampling. In the hybrid example in Paper 3 the oversampling ratio is four, accordingly the sampling capacitors can be reduced by a factor of four (13pF).

Opamp DC gain is a significant challenge, and it is equivalent in the hybrid and pipelined ADC. The error introduced by finite opamp gain cause static non-linearities in a pipelined ADC—this limits the accuracy of the converter to below the gain of the first opamp.

In the hybrid the finite opamp gain cause leakage of quantization error from each modulo integrator. The error is shaped by the preceding signal transfer function. As a result, the opamp gain can be scaled differently than in a pipelined ADC.

ADC speed translate into opamp branch current. The hybrid runs four times faster than the pipelined ADC, but has four times less capacitance, which cancel with respect to current consumption. But the hybrid has a switched-capacitor circuit with at least three clock phases,

compared to two clock phases for pipelined ADC. Assuming the settling requirements are the same for the pipelined ADC and the hybrid, the hybrid opamps must be 1.5 times faster than in the pipelined ADC. Preliminary simulations suggest that the hybrid will require opamps even faster than this, but a thorough study is left for future work.

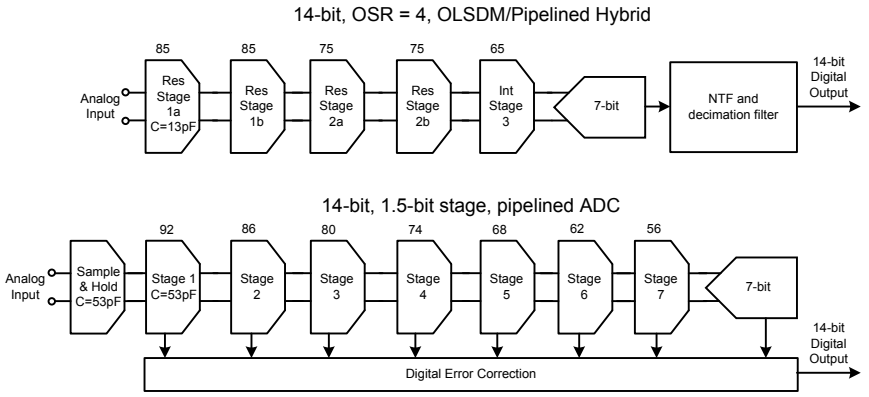


Fig. 3.2: Comparison between a 14-bit high-speed OLSDM and a 14-bit pipelined converter. The numbers above the stages denote the required operational amplifier DC gain in dB.

Paper 1: Analog Modulo Integrator For Use In Open-Loop Sigma-Delta Modulators

In this paper we introduce the switched-capacitor modulo integrator. The modulo integrator makes it possible to design an open-loop sigma-delta modulator. The theory of OLSDM and analog modulo integration is explained and verified through simulation.

Paper 2: Switched Capacitor Analog Modulo Integrator For Application In Open Loop Sigma-Delta Modulators

Paper 2 is an invited paper based on Paper 1, hence there is some overlap in the areas covered. Paper 2 discuss one of the error effects in OLSDM (false modulo) and investigate effects of a non-linear quantizer. Behavioral level

simulations in SPICE of the analog modulo integrator verify the function, and prove the concept of amplitude modulated OLSDM.

Paper 3: Resonators In Open-Loop Sigma-Delta Modulators

In Paper 3 we introduce the modulo resonator for use in open-loop sigma-delta modulators. The OLSDM presented in this work is intended for use in high accuracy (14- bit), high-speed ADCs. The modulo resonator is used with a modulo notch filter to insert a zero in the noise transfer function at a non-zero frequency. The effect of finite gain in modulo integrators and modulo resonators are described and verified through simulation. The modulo resonator and previously published modulo integrator are used in a behavioral model of a switched-capacitor fifth-order OLSDM with more than 13-bit effective number of bits for an oversampling ratio of four.

We prove for the N-order OLSDM that the number of bits in the quantizer (B) must be larger than N to ensure equivalence between OLSDM and sigma-delta modulation.

3.2 Efficient circuit solutions for pipelined ADCs

Circuit solutions that remove the opamp from switched-capacitor circuits have received interest from the research community. The idea is to replace the hard to make opamps with something more amenable to nano-scale CMOS integration. In the papers we have focused on two techniques; open-loop amplifiers, and comparator-based switched capacitor circuits. Not only are these techniques more amenable to nano-scale integration, but CBSC has been shown to have a fundamental efficiency advantage over opamp based integration [10].

We have also investigated the comparators used in the sub-ADC in the pipelined ADCs.

Paper 4: 0.8V 1GHz Dynamic Comparator In Digital 90nm CMOS Technology

This paper present simulations of a dynamic comparator in 90nm CMOS technology. It shows how 90nm CMOS technology can achieve high speed at low supply voltages.

One of the challenges in dynamic comparators is controlling the offset over process corners. As the signal swing scales down (due to supply voltage scaling) the demands on comparators in pipelined ADC become harder to fulfill, but as the paper shows, at 90nm CMOS it is quite possible to have high-speed and low supply voltage.

Paper 5: Design of a 7-bit 200MS/s, 2mW Pipelined ADC With Switched Open-Loop Amplifiers In a 65nm CMOS Technology

In this paper we present the design of a 7-bit 200MS/s pipelined ADC with switched open-loop amplifiers in a 65nm CMOS technology. As a result of turning off the open-loop amplifiers during sampling we reduce the power dissipation by 23%. The ADC achieves a SNDR of 40dB close to the Nyquist frequency, with a power dissipation of 2mW, which results in a Walden FOM of 0.13pJ/step and a Thermal FOM of 1.6fJ/step.

Paper 6: Design and Behavioral Simulation of Comparator-Based Switched Capacitor Circuits

This paper summarize some of the design equations derived in designing and debugging the chip in Paper 7. It presents a method for calculating the required parameters for comparator-based switched capacitor circuits. The parameters are capacitance (C), current (I_0), comparator delay (T_D), current source output resistance (R_o) and comparator threshold (V_{ct}). The design equations are verified with behavioral simulations in SPICE and MATLAB.

Paper 7: An 8-bit 60-MS/s 8.5mW Differential Comparator-Based Switched-Capacitor Pipelined ADC in 90nm CMOS Technology

In this paper we present the first differential comparator-based switched-capacitor (CBSC) pipelined ADC. The switched-capacitor multiplying digital-to-analog converter (MDAC) use current sources and a comparator to do charge transfer. Continuous time bootstrapped switches are used in the first stage to reduce signal dependent switch resistance. A simple calibration algorithm correct for comparator delay variation caused by the manufacturing process. Calibration reduces ramp overshoot, which dominate the non-linearity in CBSC ADCs. The ADC is produced in a 90nm low-power CMOS technology. The ADC core is 0.85mm x 0.35mm, with a 1.2V supply for the core and 1.8V for input switches. The ADC has an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.5mW at 60MS/s. The ADC achieves an Waldon FOM of 1.07pJ/step and Thermal FOM of 8.09fJ/step.

3.3 Clarification of contributions

All papers have been co-authored with my supervisor Trond Ytterdal. He has provided valuable questions, guidance and resources.

Two papers have been co-authored with Øystein Knauserud. During spring of 2006 he did his master thesis on OLSDM and I was his supervisor. He worked out that to do switched-capacitor OLSDM we needed a switched-capacitor modulo integrator. As such I worked on the problem found a viable implementation of a switched-capacitor modulo integrator. He provided questions and valuable insight.

Chapter 4
Paper 1
Analog Modulo Integrator For Use In Open-Loop Sigma-Delta Modulators

Carsten Wul_, _ystein Knauserud, Trond Ytterdal
In proceedings of the 24th NORCHIP Conference, 2006.
Nov. 2006 Pages 125 - 128
Digital Object Identi_er 10.1109/NORCHP.2006.329259

Chapter 5

Paper 2

Switched Capacitor Analog Modulo Integrator For Application In Open Loop Sigma-Delta Modulators

Carsten Wulff, Øystein Knauserud, Trond Ytterdal
Analog Integrated Circuits and Signal Processing
Springer Netherlands
ISSN 0925-1030
Volume 54, Number 2, Pages 121-131 Febuary 2008
DOI 10.1007/s10470-007-9084-2

Errata

- Section 5.3.3, 5'th line: an → a

- Section 5.3.3, second to last paragraph: We say that quantization noise can have codes that span the range of the quantizer, but this is incorrect. Quantization noise is limited to 1LSB, so the maximum difference between two output codes with the same analog input is 1LSB. This assumes that thermal noise is less than 1LSB. Thus, the statment in the second to last paragraph is not valid for quantizers with more than on bit.

Abstract

We introduce the switched capacitor analog modulo integrator, which to our knowledge is a new circuit. We introduce the amplitude modulated open loop Sigma-Delta modulator (OLSDM), which is an analog modulo integrator followed by a quantizer and a modulo differentiator. The mathematical equivalence between low pass Sigma-Delta modulators and OLSDM is explained. Behavioral simulations confirm the equivalence. The necessary circuit, a switched capacitor analog modulo integrator, is explained in detail. Behavioral level simulations in SPICE of the analog modulo integrator verify the function, and prove the concept of amplitude modulated OLSDM.

Keywords Sigma-Delta Modulators, Switched Capacitor Circuits, Analog Modulo Integrator

5.1 Introduction

Sigma-Delta modulators have become a natural choice for analog-to-digital conversion in applications with low to medium bandwidth and high resolution. The Sigma-Delta modulator shapes the spectral density of the quantization error of data converters. The quantization error, or as it is often called, quantization noise, is the error introduced by converting a continuous value signal into a discrete value signal. This error is often considered to have uniform spectral density, or in other words, be a white noise source. The conditions for considering quantization error as a white noise source was covered in [15].

The conventional low-pass Sigma-Delta modulator (L-SDM) in its simplest form consists of an integrator followed by a quantizer. The quantized signal is fed back to the input through a digital-to-analog converter (DAC) and subtracted from the input. The transfer function of the modulator is different for the input signal and the quantization noise. [1] The input signal

[1] This assumes a linear model of the quantizer, since the transfer function is only defined for a linear system

will undergo an integration followed by a differentiation and have a transfer function of one. The quantization noise will be differentiated and thus high pass filtered.

In an ideal world, with no voltage swing limitations, an L-SDM system could be implemented by an integrator followed by a quantizer and a differentiator, but since supply voltage is limited in electronic circuits, and an integrator has infinite dc gain, it is difficult to implement. Somehow the output swing of the integrator has to be limited. Feedback is normally used to limit the output swing of the integrator.

There are many different types of Sigma-Delta modulators. In this paper we discuss a small sub group that we denote Open Loop Sigma-Delta Modulators (OLSDM). We define an OLSDM as: Any Sigma-Delta modulator that does not have feedback of the quantized modulator output signal.

One of the first suggestion of an OLSDM can be found in [11]. Although there is no system implementation they explain a method that avoids the feedback DAC. More recently there have been others like the Frequency Sigma-Delta Modulator (FSDM) in [9] and [16].

In the FSDM a voltage to frequency converter, a voltage controlled oscillator (VCO), was used in place of the integrator, and it was shown in [9] that the pre-processing in FSDM is equivalent to modulo integration. The FSDM could be identified as a frequency modulated OLSDM.

In [12] they introduced the non-feedback Sigma-Delta digital-to-analog modulator where the integrator was implemented as a digital modulo integrator.

In the past the noise shaping of Sigma-Delta modulators has been combined with the high speed of pipelined ADCs. In [7] a second order five bit Sigma-Delta Modulator was cascaded with a 12 bit pipelined ADC. The output of the Sigma-Delta Modulator was combined with the output of the pipelined ADC to generate the digital output word. We wanted to investigate whether one could avoid any interaction, with the exception of the input and output signals, between the Sigma-Delta Modulator and the pipelined ADC in such a system. The question was; could one pre-process the input signal to implement the sigma, quantize and do post-processing

to perform the delta, without interaction between the sigma and the delta. The block diagram of such a system is shown in Figure 5.1

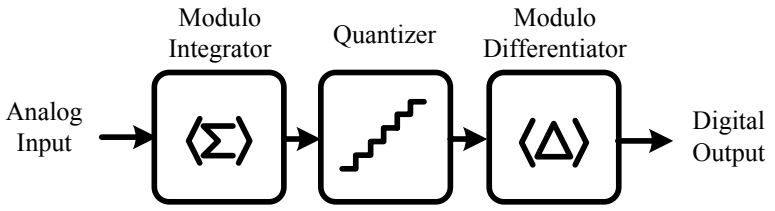


Figure 5.1: First order OLSDM block diagram

We knew from [12] that the open loop Sigma-Delta modulator was possible when all blocks were digital, by using modulo integration, quantization and modulo differentiation. However, in an analog-to-digital OLSDM the modulo integration would have to occur in the analog domain. We were unable to find any published circuit that matched our requirements for an analog modulo integrator. Accordingly, the switched capacitor analog modulo integrator was developed, which we present here. To our knowledge, this switched capacitor analog modulo integrator is a new circuit.

In Section 5.2 we elaborate on the mathematical equivalence between OLSDM and L-SDM, which is supported by behavioral simulations in Matlab in Section 5.3. Quantizer non-linearity and common errors are also discussed in Section 5.3. In Section 5.4 we introduce the analog switched capacitor modulo integrator. Behavioral level simulations with a SPICE macro model of the analog modulo integrator and the OLSDM are presented in Section 5.5.

5.2 Open Loop Sigma-Delta Modulator

The most basic low pass OLSDM is an integrator, followed by a quantizer and a differentiator as illustrated by Figure 5.1. The input signal is integrated and afterwards differentiated, hence the output is equal to the input, assuming a linear system. The quantization error added by the quantizer is differentiated thus high pass filtered. To limit the swing in the analog domain we use a modulo operation at the output of the integrator. The

inverse operation, which is also a modulo operation, is performed in the digital domain after the differentiator. A modulo operation is trivial to implement in the digital domain. The analog modulo operation is not trivial, and it has previously been implemented as a voltage to frequency converter in [9] and [16].

The equivalence of L-SDM and OLSDM was shown in [12]. Here we endeavor to explain the equivalence more intuitively.

The OLSDM has been modeled as a piecewise linear system. The modulo operation is a non-linear operation, but it can be seen as a piecewise linear system if we ignore the discontinuities when the modulo operation occurs. The quantizer has been modeled as a linear addition of noise. Figure 5.2 shows the complete modulator.

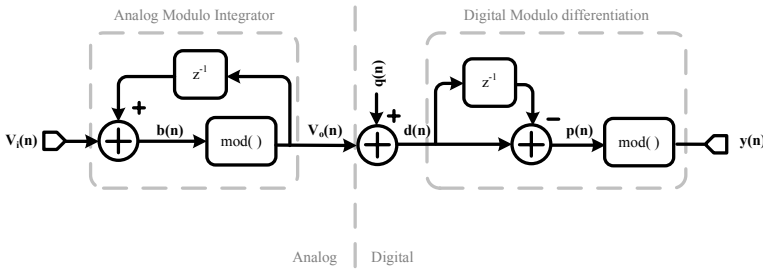


Figure 5.2: Piecewise linear model of the OLSDM

The input signal to the modulator is $V_i(n)$, where n is the sample index. A signal with sample index n is the current sample while $n-1$ is the previous sample. The input is added to the previous output of the integrator, $V_o(n-1)$, resulting in $b(n)$. The signal $b(n)$ is subjected to modulo operation with $V_o(n)$ as a result. $d(n)$ is the sum of $V_o(n)$ and the quantization noise, $q(n)$. The differentiator output $p(n)$ is $d(n)$ minus the previous quantizer output $d(n-1)$. To get the output, $y(n)$, $p(n)$ is subjected to a modulo operation. In this system the second modulo operation cancels the first modulo operation and we have a system that is equivalent to an L-SDM. The equations in more detail follow.

We define the previous output from the integrator as

$$V_o(n-1) \in \langle -V_{ref}, V_{ref} \rangle \tag{5.1}$$

and the input signal as

$$V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \tag{5.2}$$

where V_{ref} is the reference voltage.

We know that after integration, but before the modulo operation, we get

$$b(n) = V_i(n) + V_o(n-1) \tag{5.3}$$

where $b(n)$ will be bounded by

$$b(n) \in \langle -V_r, V_r \rangle \tag{5.4}$$

where $V_r = 2V_{ref}$. The modulo operation is used to reduce the output swing to $V_o(n) \in \langle -V_{ref}, V_{ref} \rangle$. The modulo operation subtracts or adds V_r, depending on the value of the summation in (5.3). The next output from the integrator can be written as

$$V_o(n) = \begin{cases} b(n) + V_r & b(n) \in \langle -V_r, -V_{ref}] \\ b(n) & b(n) \in \langle -V_{ref}, V_{ref} \rangle \\ b(n) - V_r & b(n) \in [V_{ref}, V_r \rangle \end{cases} \tag{5.5}$$

Accordingly (5.5) is the equation for a modulo integrator. After quantization the input to differentiation will be

$$\begin{aligned} d(n) &= V_o(n) + q(n) \\ d(n-1) &= V_o(n-1) + q(n-1) \end{aligned} \tag{5.6}$$

where $q(n), q(n-1)$ are the quantization errors. The the output of the differentiator is

$$p(n) = d(n) - d(n-1) \tag{5.7}$$

If we in (5.7) insert for $d(n)$, $d(n-1)$, $V_o(n)$ and set $e(n) = q(n) - q(n-1)$ the expression becomes

$$p(n) = \begin{cases} V_i(n) + V_r + e(n) & V_i(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + e(n) & V_i(n) \in \langle 0, V_{ref} \rangle \end{cases} \tag{5.8}$$

The bounds of $V_i(n)$ in (5.8) are derived from the possible input signal values for the modulator to reach the states in (5.8). Consider the first case where

$$p(n) = V_i(n) + V_r + e(n), V_i(n) \in \langle -V_{ref}, 0 \rangle \tag{5.9}$$

Here V_r has been added, thus

$$b(n) \in \langle -V_r, -V_{ref}] \tag{5.10}$$

from (5.5). For b(n) to have these bounds

$$V_i(n) \in \langle -V_{ref}, 0 \rangle \tag{5.11}$$

and

$$V_o(n-1) \in \langle -V_{ref}, 0 \rangle \tag{5.12}$$

This is sufficient to ensure the bounds of $p(n)$ in case 1 in (5.8) are

$$p(n) \in [V_{ref}, V_r \rangle$$

Thus when we apply another modulo operation we get

$$y(n) = \begin{cases} V_i(n) + V_r - V_r + e(n) & V_i(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + V_r + e(n) & V_i(n) \in \langle 0, V_{ref} \rangle \end{cases} \tag{5.13}$$

and for all cases in (5.13), $y(n) \in \langle -V_{ref}, V_{ref} \rangle$. Equation (5.13) can be expanded into

$$y(n) = V_i(n) + q(n) - q(n-1)$$

Which result in the well known equations

$$\frac{y(z)}{V_i(z)} = 1\,,\ \frac{y(z)}{q(z)} = 1 - z^{-1} \tag{5.14}$$

The transfer function from the input signal to the output is one, which is the same as for an L-SDM, although often the transfer function of an L-SDM from input to output contains a time delay, $y(z)/V_i(z) = z^{-1}$. The quantization error is differentiated, thus first order high pass filtered. This proof can be extended to higher order modulators.

5.3 Behavioral Simulations In Matlab

The behavioral simulations presented here are an implementation of the equations explained in the previous section. [2]

5.3.1 First And Second Order OLSDM

A first and second order OLSDM and an oversampled quantizer without noise shaping were modeled and simulated in Matlab. The oversampled quantizer without noise shaping was included to compare ideal results with the simulated results. All quantizers were implemented as 7 bit quantizers. An oversampling ratio (OSR) of 8 was chosen. An overview of the system can be seen in Figure 5.3.

The ideal signal to noise and distortion ratio (SNDR) for the different cases are shown in Table 5.1. The ideal SNDR are based on equations from [4].

Table 5.1: Ideal SNDR for 7 bit quantizer, OSR=8

Noise Shaping	Improvement (dB)	Total (dB)
None	$10 \times \log(OSR)$	52.9
First order	$30 \times \log(OSR) - 5.17$	65.8
Second order	$50 \times \log(OSR) - 12.9$	76.1

[2] The Matlab code for the first and second order OLSDM can be downloaded from http://www.nextgenlab.net/olsdm

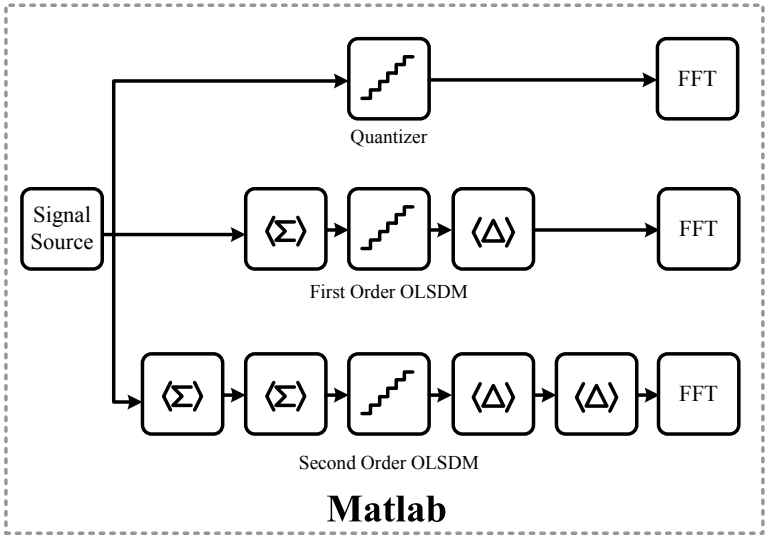


Figure 5.3: Overview of behavioral level simulation system

The equations for the OLSDM were implemented as specified in the previous section with one exception. We chose to implement the quantizer using unsigned integer outputs, the output ranging from 0-127. With this implementation $d(n)$ has a dc offset. The differentiator is a high pass filter and removes this dc offset. For the modulo operation to work, a dc offset was added after the differentiator to restore the correct common mode. In the second order OLSDM a dc offset was added after both differentiators.

The sampling frequency was chosen arbitrarily at 1MHz and the input signal was chosen according to the rules of coherent sampling [17]. In Matlab the sampling frequency is of no importance, we could just as well have used normalized frequencies. However, these simulations will be compared to SPICE simulations, and in SPICE the sampling frequency is of importance. The input frequency was $f_{in} = 6164.6Hz$ and 2^{15} samples of the output, $y(n)$, were calculated.

The input signal to the OLSDM must be limited, as specified in equation (5.2). It turns out that (5.2) is incorrect when we deal with a finite resolution quantizer, which we will discuss in the next section. For the remainder of this paper the input signal amplitude has been fixed at 0.9FSR, unless

otherwise specified. As a consequence SNDR will be 0.91dB lower than ideal cases in Table 5.1.

The outcome of simulations are summarized in Table 5.2. Both the second order OLSDM and the first order OLSDM have approximately the same SNDR as the ideal modulators. When we remove the effects of reduced input amplitude we are left with an error of $+0.2dB$ for no noise shaping, $+0.01dB$ for first order OLSDM, and $-0.19dB$ for second order OLSDM, which is within the errors of the SNDR extraction.

The Fast Fourier Transform was used to extract the SNDR, the FFTs can be seen in Figure 5.4 and Figure 5.5. The light gray spectrum in the figures are the FFTs of the ideal 7 bit quantizer, which is the same for the two figures.

Table 5.2: SNDR of OLSDM modulators with 2^{15} point FFT

Noise Shaping	Total (dB)	Difference from Ideal (dB)
None	52.2	-0.7
First order	64.9	-0.9
Second order	74.9	-1.1

5.3.2 Input Signal Amplitude Limitations

In the derivation of (5.2) we ignored quantization noise. But when we deal with a finite resolution quantizer, quantization noise cannot be ignored. With quantization noise (5.8) becomes

$$p(n) = \begin{cases} V_i(n) + V_r + e(n) & V_i(n) + e(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) + e(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + e(n) & V_i(n) + e(n) \in \langle 0, V_{ref} \rangle \end{cases} \tag{5.15}$$

The boundaries of (5.15) now include the quantization noise. For example for case two, where

$$p(n) = V_i(n) + e(n)$$

no digital modulo should be performed. To make certain no digital modulo

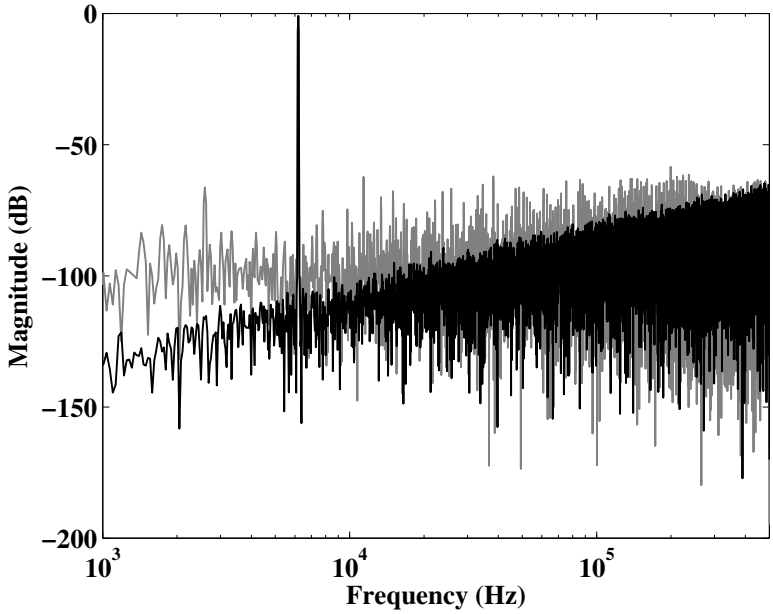


Figure 5.4: 2^{15} point FFT of the first order OLSDM output

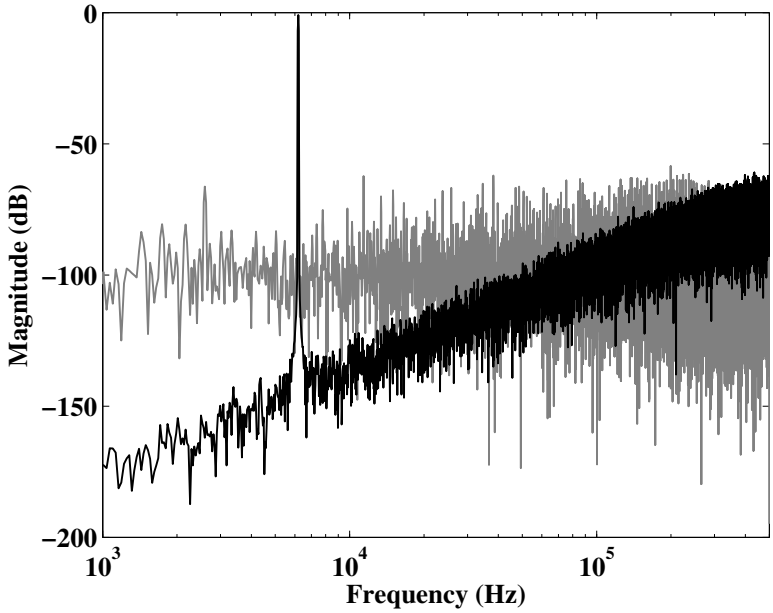


Figure 5.5: 2^{15} point FFT of the second order OLSDM output

is performed

$$V_i(n) + e(n) \in \langle -V_{ref}, V_{ref} \rangle$$

accordingly

$$V_i(n) \in \langle -V_{ref} + |e(n)|, V_{ref} - |e(n)| \rangle \tag{5.16}$$

If the input amplitude is not limited as specified by (5.16), we get a condition we denote as *false modulo* errors. For example, assume that for case two in (5.15) we get

$$p(n) = V_i(n) + e(n) <= -V_{ref} \tag{5.17}$$

as a consequence

$$y(n) = V_i(n) + V_r + e(n) \tag{5.18}$$

here a modulo operation was carried out on $p(n)$ when it should not have been.

The limit in (5.16) indicate that low resolution quantizers may not be suited for this type of OLSDM.

These errors are easy to spot in the output of the OLSDM, shown in Figure 5.6. They cause large glitches which span the range of the output codes. To avoid these errors it is sufficient to limit the input signal. It should be noted that the presence of these errors completely removes the noise shaping of the OLSDM.

In the circuit implementation of the analog modulo integrator, described by equation (5.5), we use comparators to detect $b(n) \in \langle -V_r, -V_{ref}]$ and $b(n) \in [V_{ref}, V_r \rangle$. If we use the outputs from these comparators we can prevent the *false modulo* errors from occuring. In the first order OLSDM we know that a modulo should only be performed after differentiation when a modulo was performed in the analog modulo integrator. Consequently we can use the outputs of the comparators in the modulo integrator to control the modulo operation in the differentiator. This ensures that *false modulo* errors never occur. The solution comes at the cost of delay lines that must be added to synchronize the comparator outputs from the modulo integrators

with the modulo differentiator. For the remainder of the paper we do not use this solution. In Section 5.3.3 we describe an error correction technique that corrects *false modulo* errors without using the comparator outputs.

Unrelated to these errors it was shown in [18] that for digital-to-analog OLSDM $N+1$ quantizer bits are normally needed, where N is the OLSDM order. Thus for a second order OLSDM we would need a 3 bit quantizer. We expect the same to be true for analog-to-digital OLSDM.

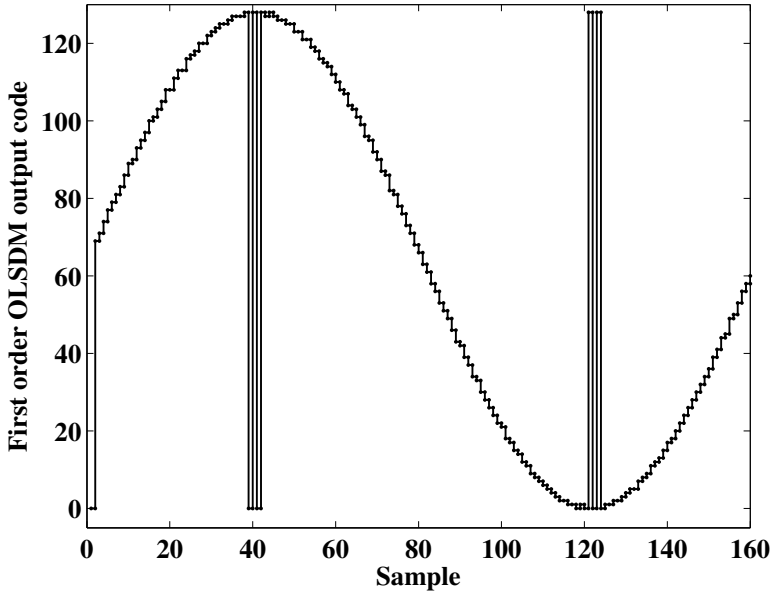


Figure 5.6: The output of the first order OLSDM in the presence of *false modulo* errors

5.3.3 Quantizer Linearity And Correction Of False Modulo Errors

An important issue of the amplitude modulated OLSDM is how the linearity of the quantizer affects the system. The step sizes in the quantizer were made dependent on the input signal, thus introducing a non-linearity. By changing the dependence on the input signal we control the linearity of the quantizer. In this example an 7 bit quantizer with a maximum of 6.8 bit linearity was used as the quantizer in the second order OLSDM. The results are

presented for two different input amplitudes, $0.8FSR$ and $0.9FSR$. Figure 5.7 shows the linearity of the OLSDM as a function of quantizer linearity. As expected, the linearity of the OLSDM does depend on the linearity of the quantizer. For each bit of reduction in the linearity of the quantizer the second order OLSDM looses half a bit of linearity. The slope is constant until a threshold is reached, the threshold marks the onset of *false modulo* errors. Below this threshold the SNDR of the OLSDM degrades rapidly. The threshold is highly dependent on the input amplitude and is on the order of (5.16). Such a sharp decrease in SNDR at a particular input signal amplitude is undesirable, and it would be advantageous to correct for the cause of the sharp degradation, the *false modulo* errors. As mentioned we can use the comparator output from the analog modulo integrators to control modulo differentiation, which will remove the *false modulo* errors. However, there is an alternate solution.

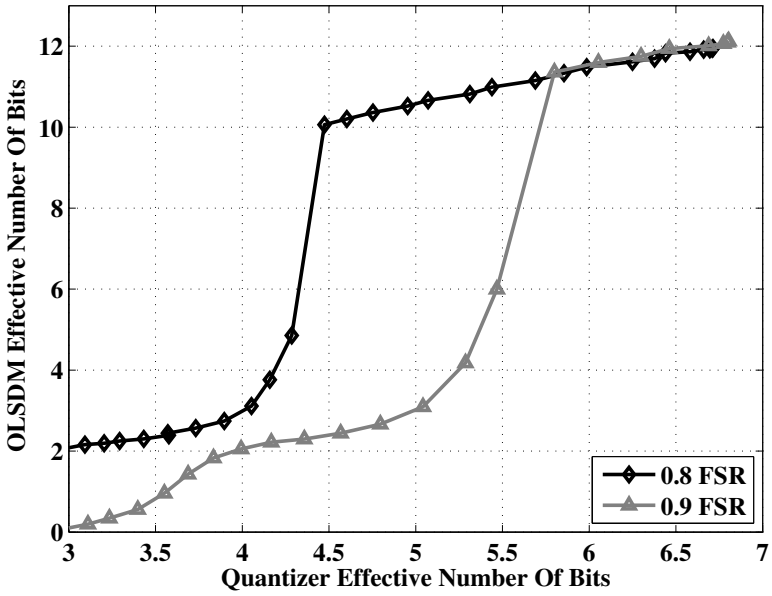


Figure 5.7: Linearity of second order OLSDM as a function of quantizer linearity

The *false modulo* errors have a large amplitude and high frequency, as seen in Figure 5.6. They span the range of the output codes in two samples,

and thus have a frequency close to the Nyquist frequency. If we take advantage of the fact that the input signal is, by choice, at least eight times lower than the Nyquist frequency, since we chose an OSR of eight, we can reduce the errors. There is a maximum difference between two adjacent output codes, which depend on the input signal. We assume a sinusoidal input at one-eight of the Nyquist frequency. A sinusoid has a maximum slope at the zero crossing which is approximately given by

$$Slope \approx A\pi/OSR \tag{5.19}$$

, where A is the amplitude. In (5.19) we have used the well known assumption that $\sin x \approx x$ if x is small and that $OSR = f_s/2f_{in}$. With an OSR of eight $Slope \approx 0.39$ at zero crossing, which is approximately one fifth of the FSR.

We assume that any change in the output of more than $0.6FSR$ between two consecutive samples is due to a *false modulo* error. If two consecutive samples of the OLSDM output has a difference of more than 0.6FSR we undo the modulo operation. The result of this simple correction can be seen in Figure 5.8. The error correction compensates for the dependence on input signal amplitude and the onset of *false modulo* errors. It should be noted that this error correction technique now allows the input signal amplitude to be FSR.

In this error correction technique we have made an assumption on the properties of the output signal of the modulator. In this assumption we must be cautious of the quantization noise. If we use a low resolution quantizer the quantization noise power at higher frequencies can be significant, and output codes which span the range of output codes in two samples are certainly possible. Having said that, with higher resolution quantizer and low order noise shaping the quantizer noise power is not significant enough to influence the error correction.

The circuit implementation of an amplitude modulated OLSDM requires an analog modulo integrator. The next section explains how such a function can be implemented by a switched-capacitor circuit.

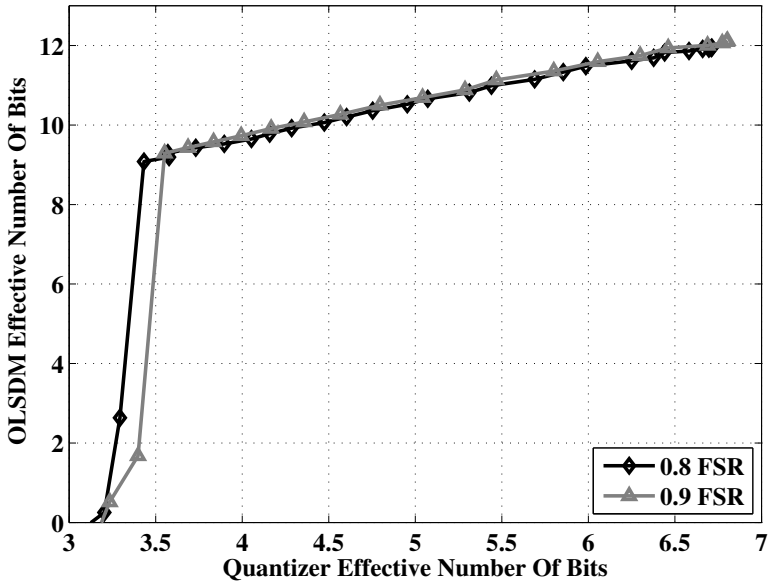


Figure 5.8: Linearity of second order OLSDM as a function of quantizer linearity with error correction enabled

5.4 The Analog Modulo Integrator

A requirement set on the analog modulo integrator was that it should use maximum swing available, for example 0.8V peak-to-peak with 1.2V supply. It should also be a discrete time system and it should be amplitude modulated and not frequency modulated as was used in [9] and [16]. The discrete time equation for a analog modulo integrator was shown in (5.5).

Using pseudo code the modulo integrator can be described as

1. Add the previous output to the current input
2. If the new output is equal to or exceeds the reference voltages
3. Subtract/Add the range of the integrator, V_r
4. Set the current output to the remainder

A modulo operation is trivial to implement in the digital domain, but it may not be obvious how it should be implemented in the analog domain.

Adding two voltages in the analog domain is conceptually trivial. Whether a voltage exceeds a reference can be detected using a comparator. Subtraction in the analog domain is also trivial, but keeping the remainder presents a challenge.

Assume that the reference voltages are symmetric around the common mode, such that $|V_{ref}| = |-V_{ref}|$ and $|V_{ref}|+|-V_{ref}| = V_r$. The maximum internal voltage in the modulo integrator would be less than $V_{ref}+V_{ref} = V_r$ or more than $-V_{ref} + -V_{ref} = -V_r$. So the output after summation, but before modulo operation, will be bounded by

$$-V_r < b(n) < V_r \tag{5.20}$$

In a circuit where the analog value is represented by voltages the swing would have to be $2V_r$ to accurately represent all analog values. Since our input signal has a range of V_r we would waste an extra range of V_r just to represent intermittent values in the integrator. It would be better if we could set the voltage swing of the circuit to V_r, which is equal to the maximum input swing. But in a circuit where the analog values are represented with voltages this is difficult.

5.4.1 A Solution Based On Switched Capacitors

Switched-Capacitor (SC) circuits are prevalent in many analog integrated circuits. In discrete time Sigma-Delta modulators it is common to implement the integrator with a switched-capacitor circuit. It turns out that with small modifications a switched-capacitor integrator can be converted to an analog modulo integrator.

In switched-capacitor circuits the analog values are represented by voltages across charged capacitors. A conventional switched-capacitor integrator, shown in Figure 5.9, adds the previous output and current input.

This simple integrator has two phases, sample ($\phi 1$) and charge transfer ($\phi 2$). Assume the charge stored on C_2 is zero ($Q_2 = 0$). In the sample phase we charge C_1 to the input voltage, thereby placing a charge of $Q_1 = V_i C_1$ on the capacitor. During charge transfer the charge of C_1 is transferred to

C_2 by forcing the voltage V_g to be equal to ground using an operational amplifier. The voltage across C_1 is then zero and there is no charge stored across it, all charge is across C_2. This causes the output voltage to be $V_o(n) = Q_1/C_2$. If the input value is kept constant, the next output value, after a clock cycle, will be $V_o(n+1) = 2Q_1/C_2$.

In the charge transfer phase V_g is a high impedance node, thus the total charge, Q_{tot}, given by $Q_{tot} = Q_1 + Q_2$, does not change. Q_{tot} is independent of the voltages at V_g and V_o. Thus we can argue that the ideal output value, $V_{o-ideal} = Q_{tot}/C_2$ is only dependent on the total charge across the capacitors. By ideal output voltage $V_{o-ideal}$ we mean the output voltage V_o if V_g was forced to ground.

A real world operational amplifier will normally have a maximum output signal swing. For example, if we exceed this signal swing the gain in the operational amplifier goes down, and it is unable to force virtual ground. In this case V_o saturates, it cannot go any higher, hence $V_o < V_{o-ideal}$. This saturation voltage we define as $V_{sat} > V_{ref}$.

Assume that the operational amplifier saturates in $\phi 2$, hence $V_o = V_{sat} > V_{ref}$. If we can detect this condition, $V_o > V_{ref}$, we can subtract a charge from V_g that represents V_r ($V_r = 2V_{ref}$ as defined in Section 5.2), thus perform a modulo operation. We would now have

$$V_{o-ideal} = (Q_{tot} - Q_{V_r})/C_2 < V_{ref} < V_{sat}$$

as a consequence the operational amplifier will be able to force virtual ground.

One of the differences between the switched capacitor analog modulo integrator and the conventional integrator is that the latter has three clock phases. The first two have the same function as in the conventional integrator, sample and charge transfer. The third clock phase is added to detect if $V_o > V_{ref}$ (and the opposite, $V_o < -V_{ref}$) in phase two. If it does exceed, a charged capacitor is connected to the charge transfer node of the integrator, node V_g in Figure 5.9. This subtracts or adds the charge which represent V_r. This will change the charge transfer equation, and as we shall see, implement a modulo operation.

Provided that the input signal limited as specified by (5.16), the subtracted/added charge will ensure that

$$-V_{ref} < V_o < V_{ref} \tag{5.21}$$

The circuit needed to implement a modulo integrator is shown in Figure 5.10. It is connected to the integrator in node V_g and V_o. The complete circuit has, as mentioned, three clock phases; $\phi 1$, $\phi 2$ and $\phi 3$. The timing diagram is shown in Figure 5.11, where T denotes the period and $1/3, 2/3$ denotes the fractional time steps.

Consider the integrator in Figure 5.9. During clock phase $\phi 1$ the input signal is sampled across capacitor C1. In clock phase $\phi 2$, before $\phi 3$, the charge from C1 is transferred to C2. The charge transfer equation will be

$$C_2 V_o(n - T/3) = C_2 V_o(n - T) + C_1 V_i(n - 2T/3) \tag{5.22}$$

In this equation, $V_o(n - T/3)$, is equivalent to $b(n)$ from equation (5.3) and will have the same bounds, assuming $C_1 = C_2$. For the output, $V_o(n)$, to stay within the reference voltages, V_r has to be added or subtracted as in equation (5.5).

Figure 5.12 shows the states of Figure 5.10 in more detail. During $\phi 1$, Figure 5.12 a) , the capacitor C_3 is charged to $V_r = V_{ref} - -V_{ref}$. At the start of $\phi 3$ the latched comparators ($X2$ and $X3$ in Figure 5.10) determine whether the output voltage exceeds the reference. Figure 5.12 b) shows the

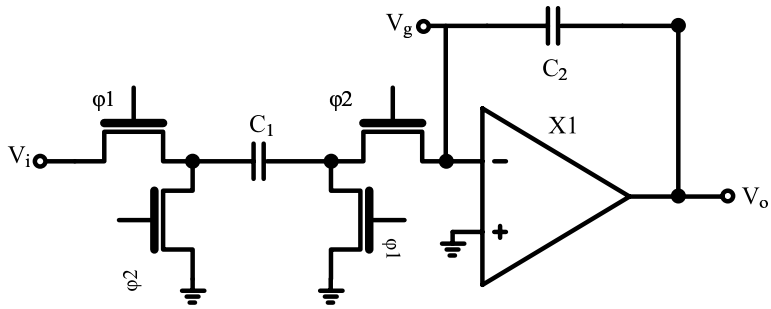


Figure 5.9: Conventional switched capacitor integrator

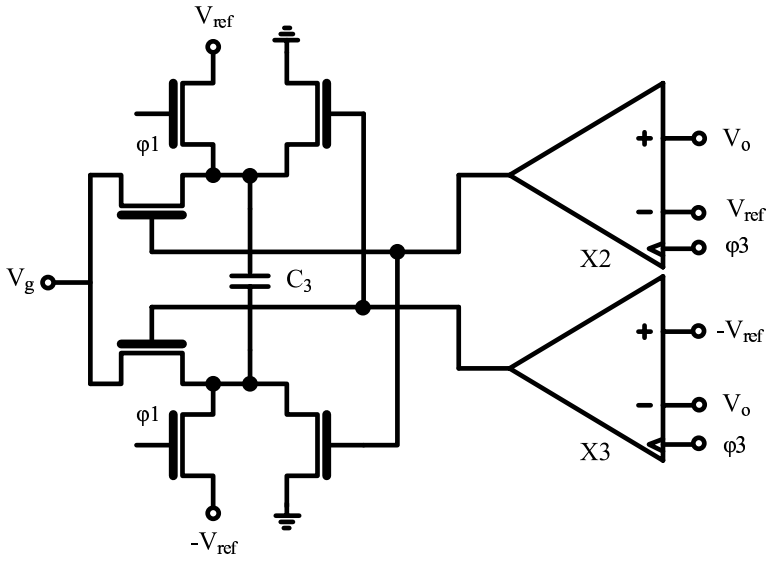


Figure 5.10: Modulo circuit

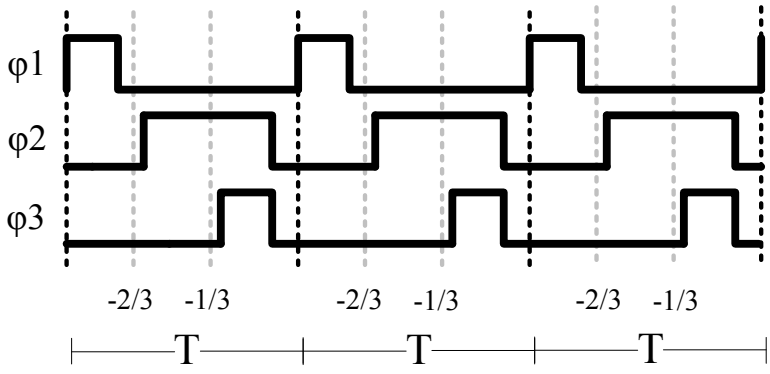
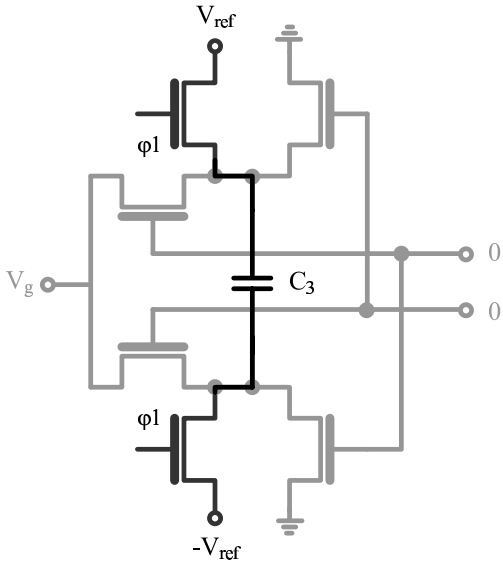
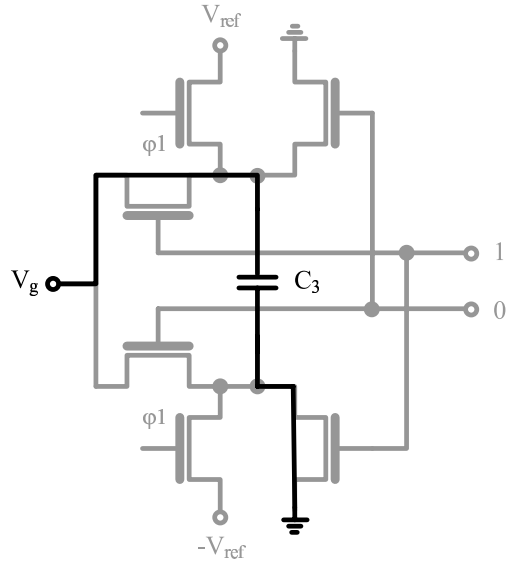


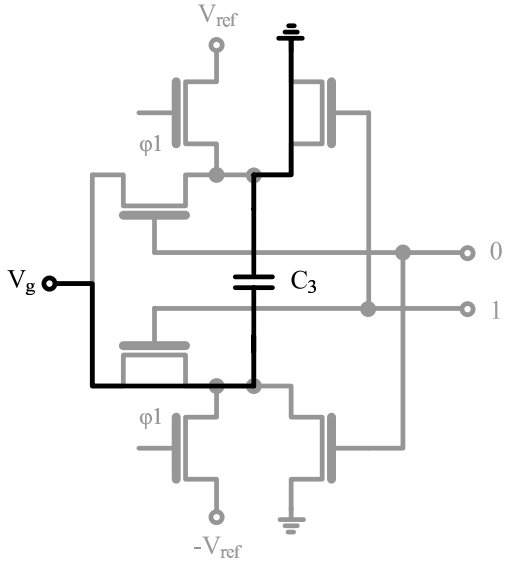
Figure 5.11: Timing diagram for the modulo integrator



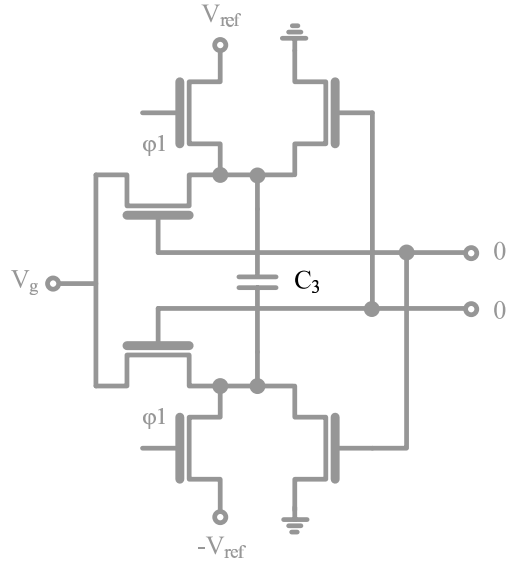
a) In φ1 the capacitor is charged.



b) In φ3, if $V_o \geq V_{ref}$ the charge transfered to V_g will be $Q_3 = C_3V_r$



c) In φ3, if $V_o \leq -V_{ref}$ the charge transfered to V_g will be $Q_3 = -C_3V_r$



d) In φ3, if $-V_{ref} < V_o < V_{ref}$ no charge is transfered to C_3

Figure 5.12: The states of the modulo circuit in Figure 5.10

connections if the output voltage, $V_o(n - T/3)$, is higher than V_{ref}. Here a charge of $Q_3 = C_3V_r$ is transferred to the node V_g in the integrator. This will change the charge transfer equation into

$$C_2V_o(n) = C_2V_o(n - T) + C_1V_i(n - 2T/3) - C_3V_r \tag{5.23}$$

For $V_o(n-T/3)$ lower than $-V_{ref}$, Figure 5.12 c) , the polarity of the charge is reversed and the charge transfer function is

$$C_2V_o(n) = C_2V_o(n - T) + C_1V_i(n - 2T/3) + C_3V_r \tag{5.24}$$

And if $-V_{ref} < V_o(n - T/3) < V_{ref}$ the capacitor C_3 is not connected to V_g and the charge transfer function (5.22) remains unchanged as shown in Figure 5.12 d). Notice that the outputs from the comparators can never be high at the same time.

Combining the three equations, (5.22), (5.23) and (5.24) with $C_1 = C_2 = C_3$ and ignoring the fractional time-steps ($n-T/3$ and $n-2T/3$) the result is (5.5).

The analog modulo integrator presented here resemble a first-order low pass 1.5 bit Sigma-Delta Modulator. If one plots the spectrum of the combined comparator outputs it is a quantized first order noise shaped version of the input. What makes an analog modulo integrator different from a first order low pass Sigma-Delta Modulator is

- The quantizer levels are set at $\pm V_{ref}$, and not evenly distributed between $\pm V_{ref}$.

- The three phase clock implements a form of zero time quantizer feedback, if V_o is higher than V_{ref} V_r is immediately subtracted before the next output of the integrator.

- The comparator outputs are not necessary to reverse the effect of the modulo operation in the digital domain.

5.5 Behavioral Level Verification Of The SC OLSDM

We implemented a macro model description of the SC analog modulo integrator described in the previous section.[3] A single pole operational amplifier macro model with a dc gain of 74dB and a voltage limiter was used to model the operational amplifier. The comparators were modeled as latched comparators. Ideal switches with an on resistance of 200 Ohms were used and the capacitors C1-C3 were 5pF. The reference voltages were $V_{ref} = 1V$ and $-V_{ref} = -1V$. The switch resistance, capacitance and references were chosen arbitrarily. The output of the operational amplifier was limited to $\pm 1.4V$. This ensures that for some values of the input the integrator will saturate during $\phi 2$. The input frequency, sampling frequency and the number of samples was the same as for the Matlab simulation. An overview of the system can be seen in Figure 5.13.

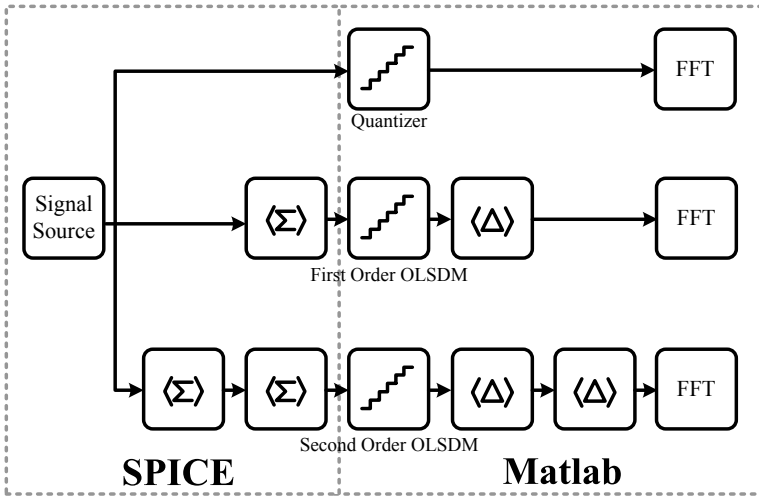


Figure 5.13: Overview of circuit simulation with macro models

Only the analog modulo integrator was implemented in SPICE. Its output was extracted and post-processed in Matlab. The code for the differentiator and the quantizer were the same as in the behavioral simulations.

[3]The SPICE macro model of the switched capacitor analog modulo integrator can be downloaded from http://www.nextgenlab.net/olsdm

In Figure 5.14 the input signal (dark gray) and the output signal (light gray) of the first order SC modulo integrator is shown for the first 150 samples. The sinusoidal input had an amplitude of $0.9V$. The output, V_o, has been sampled at the end of $\phi 3$ and it can be seen how it never exceeds the references at V_{ref} and $-V_{ref}$.

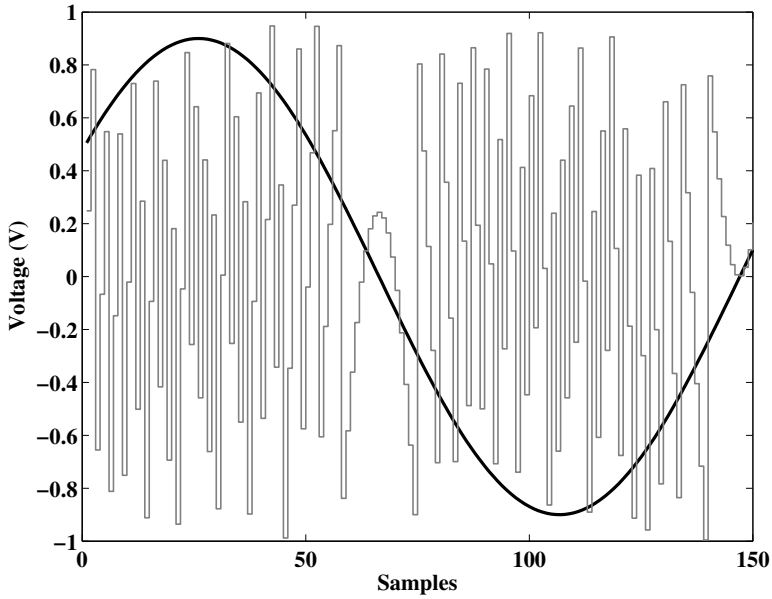


Figure 5.14: Input vs output for the modulo integrator. Input is a sine with an amplitude of 0.9 V

A transient simulation was performed. The results are summarized in Table 5.3. If we remove the effect of reduced input signal amplitude the errors are $-0.2dB$ for first order OLSDM and $-2.1dB$ for second order OLSDM. The error for first order OLSDM is within the error of the SNDR extraction. The error for the second order OLSDM it is to large to be caused by deviations due to SNDR extraction. This extra loss of $-2.1dB$ was mainly due to non-linearity of the voltage limiter used in the simulation. When the voltage limiter is removed the error for second order OLSDM is reduced to $-0.79dB$. The remaining difference is mostly due to finite gain in the operational amplifier. The FFTs of the first and second order OLSDM are shown in Figure 5.15 and Figure 5.16, the ideal quantizer in light gray

and the OLSDM output in dark gray.

Table 5.3: SNDR of OLSDM modulators in SPICE

Noise Shaping	Total (dB)	Difference from Ideal (dB)
First order	64.7	-1.1
Second order	73.1	-3

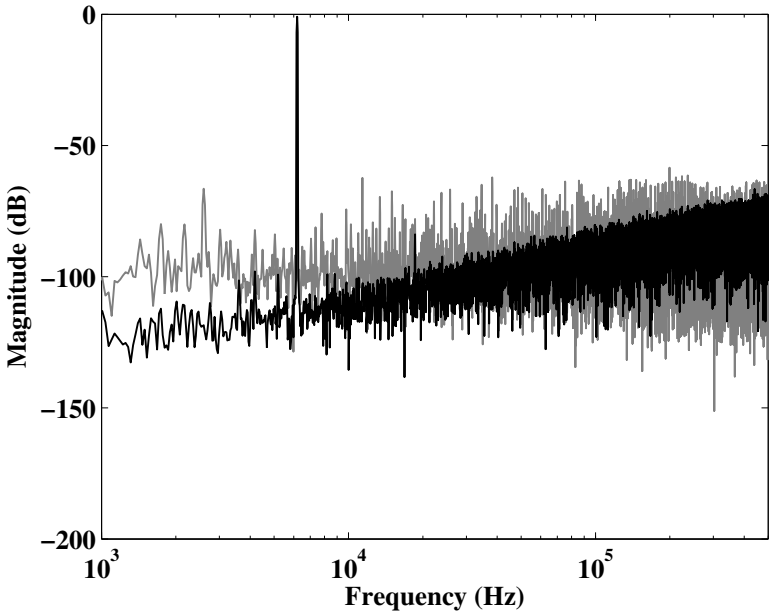


Figure 5.15: FFT of output from first order OLSDM simulation in SPICE.

5.6 Future Work

There are no integrated circuit implementations of an amplitude modulated OLSDM as of yet. An integrated circuit implementation would be the next step. It is needed to check whether the amplitude modulated OLSDM has a place in the family of analog-to-digital converters, or whether it is just of academic interest. There are many questions to be answered and some questions that have not yet been asked. The switched capacitor analog modulo integrator is, to our knowledge, new circuit, and it may find applications

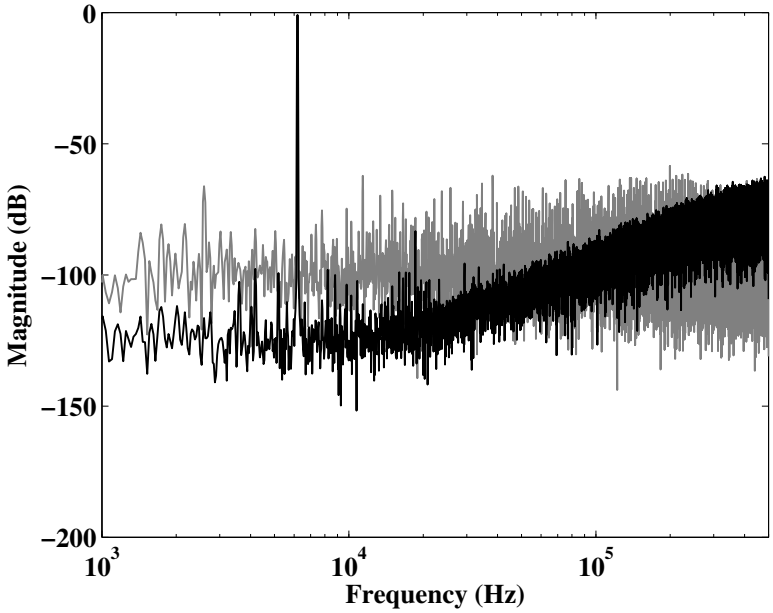


Figure 5.16: FFT of output from second order OLSDM simulation in SPICE.

outside the realm of OLSDM.

5.7 Conclusion

We introduced the switched capacitor analog modulo integrator, which to our knowledge is a new circuit. We introduced the amplitude modulated open loop Sigma-Delta modulator (OLSDM), which is an analog modulo integrator followed by a quantizer and a modulo differentiator. The mathematical equivalence between low pass Sigma-Delta modulators and OLSDM was explained. Behavioral simulations confirmed the equivalence. The necessary circuit, a switched capacitor analog modulo integrator, was explained in detail. Behavioral level simulations in SPICE of the analog modulo integrator verified the function, and proved the concept of amplitude modulated OLSDM.

Acknowledgments

Financial support from the Norwegian Research Council through the project Smart Microsystems for Diagnostic Imaging in Medicine (project number 159559/130) and the project ASICs for Microsystems (project number 133952/420) is gratefully acknowledged.

Chapter 6
Paper 3
Resonators In Open-Loop Sigma-Delta Modulators

Carsten Wul_ and Trond Ytterdal

Submitted to IEEE Transactions on Circuits and Systems I: Regular papers

Chapter 7
Paper 4
0.8V 1GHz Dynamic Comparator In Digital 90nm CMOS Technology

Carsten Wul_ and Trond Ytterdal
In proceedings of the 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005 Pages 237 - 240
Digital Object Identi_er: 10.1109/NORCHP.2005.1597033

Chapter 8
Paper 5
Design of a 7-bit 200MS/s, 2mW Pipelined ADC With Switched Open-Loop Ampli_ers In a 65nm CMOS Technology

Carsten Wul_ and Trond Ytterdal
In proceedings of the 25th NORCHIP Conference, 2007.
Digital Object Identi_er 10.1109/NORCHP.2007.4481042

Chapter 9
Paper 6
Design and Behavioral Simulation of Comparator-Based Switched Capacitor Circuits

Carsten Wul_ and Trond Ytterdal
Accepted at 26th NORCHIP Conference 2008

Chapter 10
Paper 7
An 8-bit 60-MS/s 8.5mW Di_erential Comparator-Based Switched-Capacitor Pipelined ADC in 90nm CMOS Technology

Carsten Wul_ and Trond Ytterdal

Submitted to Journal of Solid State Circuits

Chapter 11

Comments to papers, conclusion and further work

11.1 Comments to papers

11.1.1 Paper 2

In the suggested future work of this paper we mention that an integrated circuit implementation would be the next step. We did investigate some implementations on the simulation level, but we discovered that low-pass noise shaping was insufficient to create an efficient high-speed, high-resolution ADC. With a high oversampling ratio in a high-speed modulator the requirements for the unity gain of the opamps was to high. Thus, we decided to concentrate on more aggressive noise shaping using zeros at non-zero frequency to lower the OSR of the modulator.

11.1.2 Paper 4

The comparator developed in this paper was intended for the pipelined ADCs in this thesis (Paper 5 and Paper 7), but a problem was discovered after publication. The comparator in Paper 4 has significant kick-back through the input transistors M1 and M4. In the reset phase the drain of these transistors are reset to ground. When the comparator turns on, both

the sources go to VDD. This results in a kick-back through the gate-source capacitor. The kick-back can become large if input capacitance of the comparator is significant compared to the sampling capacitors in the pipelined stage. As a consequence, this comparator was not used in Papers 5 and Paper 7.

11.1.3 Paper 7

Fig. 11.1 shows a comparison of this ADC to other 8-bit converters. At 8-bits and above 1MS/s there are three converters that have better FOM. The first is a zero-based crossing switched-capacitor (similar to CBSC) by Brooks et al with 4.5fJ/step at 200MS/s [50], this was a single ended architecture implemented in 0.18μm CMOS. The second is by Kim et al [62] in a 0.18μm CMOS technology with a FOM of 3.56fJ/step at 200MS/s. They used switched-opamps to reduce power dissipation. The third is by Mulder et al [63] with 4.5fJ/step at 125MS/s, this was a sub-ranging ADC in 0.13μm CMOS technology. At 8-bit and above 1MS/s there is only one other ADC in 90nm CMOS by Shen et al [64], which has a FOM of 11.37fJ/step at 10MS/s.

The ADC in Paper 7 was designed to be a 10-bit converter, but we underestimated the noise from digital IO, which limited the performance. Thus, the ADC was not optimized for 8-bit operation, and in that light the achieved performance is satisfactory.

11.2 Conclusion

In this thesis we have focused on two of the challenges facing an ADC designer in nano-scale CMOS technology, reduced power supply and reduced output resistance.

For high-resolution ($\geq$ 12-bit) ADCs one of the challenges is the increased capacitance due to reduced signal swing. As seen in Fig. 1.1 the power supply is expected to reach 0.65V at the 14nm node (year 2020). If we assume the signal swing is 80% of the power supply a 12-bit ADC will require a minimum of 12pF sampling capacitance, while a 14-bit ADC will

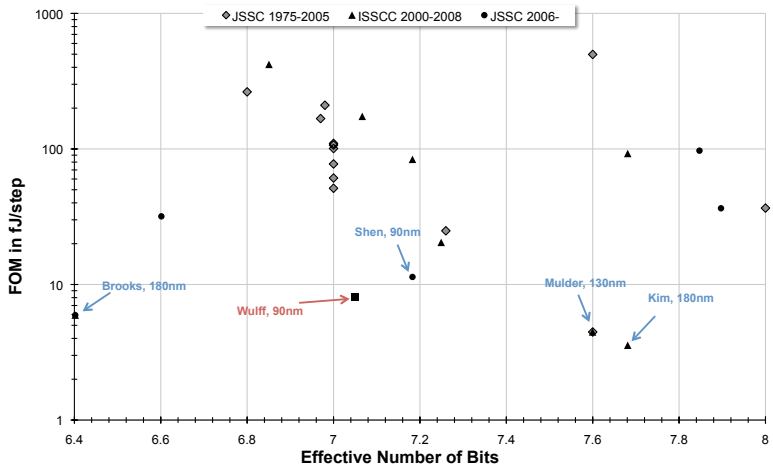


Fig. 11.1: Figure of merit comparison of the ADC in Paper 7 and other eight bit converters with sampling frequency above 1MS/s. A lower value is better.

require 192pF sampling capacitance. Hence, high-resolution converters in nano-scale CMOS must use oversampling to reduce the capacitance.

The switched-capacitor open-loop sigma-delta modulator introduced in this work is a new architecture. In this thesis we have described how one can build such an ADC and explained most of the theory behind OLSDM. We believe that OLSDM is an interesting alternative to the MASH[1] sigma-delta as a front-end to pipelined ADCs.

Another challenge for pipelined ADCs and sigma-delta ADCs is reduced headroom and reduced output resistance. The reduced headroom makes it harder to stack transistors (cascoding) to achieve high gain. This combined with the reduced output resistance of nano-scale CMOS transistors make it difficult to design high gain circuits. Unless something is done at the device level it will be challenging to design high gain ($>$ 40dB) operational amplifiers in the future nano-scale CMOS technologies.

For high-resolution ($\geq$ 12-bit) high-speed ADCs techniques like correlated-level shifting [46] or gain-calibration [53] could be alternatives to conventional opamps.

[1]MASH: Multi-stAge noise SHaping

For low- to medium-resolution (6-bit to 10-bit) high-speed ADCs techniques like open-loop residue amplifiers and comparator-based switched-capacitor circuits are an alternative to opamp-based SC.

For pipelined ADCs up to 7-bit the open-loop residue amplifier is a good option, as was demonstrated in Paper 5. But the use of open-loop residue amplifiers above 7-bit requires calibration due to the non-linearity of open-loop amplifiers.

Comparator-based switched-capacitor ADCs can bridge the gap from 7-bit to 10-bit resolution. We have shown that it is possible to create a differential CBSC ADC. And we have shown that the efficiency of such a converter is good. The ADC in Paper 7 is only two times less efficient than the best 8-bit ADCs above 1MS/s. To par the best ADCs it would have to increase its resolution by 0.5-bit (from 7.05-bit to 7.5-bit). As the pipelined ADC in Paper 7 was designed for 10-bit operation and achieved 9-bit ENOB in simulation we believe that differential CBSC pipelined ADCs can be made more efficient than our prototype. The limiting factor in our ADC was noise from digital IO, which is an problem that can be solved.

11.3 Further work

For open-loop sigma-delta modulation the next question is: What is the expression for the effect of incomplete settling in the modulo resonator and the modulo integrator? The effects of incomplete settling are well known for conventional integrators, but it must be verified that the modulo operation does not introduce any new phenomena. An analytical expression that can be translated into a MATLAB model is needed, and it should be verified with SPICE simulations. A place to start is with the papers by Temes [26] and Martin [27], which detail the effects of incomplete settling for switched-capacitor integrators.

For comparator-based switched capacitor ADCs there are two challenges we would like to mention. Our ADC has digitally controlled current sources and comparators and a digital calibration algorithm is used to calibrate the ADC. But the search space is too large, $2^{154} - 1$ is simply too many possible

solutions. In future versions we would recommend limiting the search space. One way to do this is to reduce the number of CBSC stages. We believe that a combination of MSB CBSC stages and LSB opamp-based stages, LSB open-loop residue amplifier stages, or a multi-bit flash-ADC is the way to go. For example a 10-bit pipelined ADC with four CBSC stages and a 6-bit back-end. The search space for calibration of CBSC stages is then reduced. With our calibration method there would be $2^{88}-1$ possible solution, which still is too many. But with the help of the design equations in Paper 6 the search space can be further reduced. The necessary comparator threshold (V_{ct}) can be calculated from the comparator delay (T_d), the current source current (I_0), the output capacitance (C_o) and the output resistance (R_o). With SPICE simulations the standard deviation of these variables can be found. Accordingly, the standard deviation of V_{ct} could be found, which would limit the number of bits required to calibrate it after production.

Another challenge is the noise from digital IO. For future prototypes we would recommend synchronizing all bits. Knowing when the digital outputs switch is essential. Reducing the number of bits would also be a good idea. For a pipelined ADC with four CBSC stages and a 6-bit back-end we would need $2 \times 4 + 6 = 14$ digital outputs, compared to 18 digital outputs for eight CBSC stages and a two bit flash-ADC. In addition, in an ADC prototype is a good idea to include a down-sampler, so the digital outputs can be run at a lower speed than the ADC core. We did not do this for the ADC in Paper 7, but we wish we had.

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