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Modeling of Electrostatics and Drain Current in Nanoscale Double-Gate MOSFETs

Thesis for the degree philosophiae doctor

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NTNU

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Preface

This thesis is submitted in fulfillment of the requirements for the degree Philosophiae Doctor at the Norwegian University of Science and Technology (NTNU). The work has mainly been carried out at UniK - University Graduate Center and partly at Universitat Rovira i Virgili in Spain. The project (SINANO) has been funded jointly by the European Union and UniK.

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Summary

This work comprises a new technique for 2D compact modeling of short-channel, nanoscale, double-gate MOSFETs. In low-doped devices working in the subthreshold regime, the potential distribution is dominated by the capacitive coupling between the body contacts. This 2D potential is determined by an analytical solution of the Laplace equation for the body using the technique of conformal mapping. Near threshold, where the spatial inversion charge becomes important, a self-consistent solution is applied. In sufficiently strong inversion, the electronic charge will dominate the potential profile in central parts of the channel. For this case, an analytical solution of the 1D Poisson's equation is used. Based on the modeled barrier topography, the drain current is calculated for the drift-diffusion transport mechanism. The results compare favorably with numerical simulations.

A parametrized model for drain current, with all parameters extracted from the modeling framework, is presented as an example of a compact model suitable for inclusion in circuit simulators.

Table of Contents

1	Background/introduction	1
1.1	Background	1
1.1.1	MOSFET/CMOS historical overview	2
1.1.2	Importance of CMOS	3
1.1.3	Technology-development scaling Moore's law	3
1.1.4	Integrated circuit design - tools	4
1.1.5	Device simulation (TCAD) - applications	4
1.1.6	Circuit simulation - SPICE	4
1.1.7	Device modeling - compact/analytical models	5
1.2	Objectives of thesis	6
1.3	Challenges/Scope	6
1.4	Outline of thesis	7
2	Review of DG MOSFET models	9
2.1	Long-channel modeling	10
2.1.1	Modeling of undoped devices	11
2.1.2	Methods for including effects of doping	12
2.2	Short-channel models	17
2.2.1	Approximate models, quasi-2D	18
2.2.2	Quasi-2D approaches for an undoped/lightly doped body	18
2.2.3	Quasi-2D approaches for a strongly doped body	20
2.2.4	Hydrodynamic/energy balance model	22
2.2.5	Conformal mapping - outline	23
3	Conformal mapping	25
3.1	Schwarz-Christoffel transformation of the double-gate MOSFET	25
3.1.1	Geometric constants C and k	27
3.1.2	Expressions along boundaries and symmetry lines	28
3.1.3	Orthonormal grid in the Z-plane	30

4	DG MOSFET electrostatics	31
4.1	Device structure	32
4.2	Sub-threshold	33
4.2.1	Extended device body	33
4.2.2	Boundary conditions	34
4.2.3	Oxide gaps	34
4.2.4	Body potential distribution	35
4.2.5	Self-consistency at contacts	36
4.2.6	Model simulations	38
4.2.7	Modeling of DIBL	39
4.2.8	Asymmetric gate biasing	45
4.3	Near threshold	47
4.3.1	Superposition	48
4.3.2	Approximations used	48
4.3.3	Self-consistency	48
4.4	Strong inversion	60
4.4.1	Long channel approximation	60
4.5	Quantum mechanical aspects	63
4.6	Discussion	66
5	DG MOSFET drain current	67
5.1	Self-consistent modeling of drain current	69
5.2	Drain current calculations	69
5.3	Compact drain current model	72
5.4	Discussion	76
6	Conclusion	77
7	Future work	79
7.1	Strong inversion modeling	79
7.2	Development of SPICE-type model	79
7.3	Capacitances	80
7.4	Noise	80
7.5	Application to other FET devices	80
7.5.1	GAA MOSFET	80
7.5.2	FinFET	80
A	The Schwartz-Christoffel transformation	81
1.1	Definition of the Schwartz-Christoffel Mapping	81
1.2	Schwarz-Christoffel rectangle transformation	82
1.3	Elliptic integrals and evaluation	82
1.3.1	Elliptic functions	84

Table of Contents

B SINANO template	87
2.1 Template description	87
Reference list	89

Notation and symbols

$F(k, \phi)$	Elliptic integral of first kind
$K(k)$	Complete elliptic integral of first kind
k	Elliptic modulus
k_1	Complementary elliptic modulus
t_{ox}	Oxide (insulator) thickness
t'_{ox}	Effective thickness of oxide (insulator) for silicon permittivity
ϵ_{ox}	Relative dielectric permittivity of oxide
ϵ_{Si}	Relative dielectric permittivity of silicon
t_{Si}	Silicon (body) thickness
H	Effective transformed device height
L	Gate length
W	Device width
N_S	Substrate doping
N_C	Effective density of states in conduction band
N_V	Effective density of states in valence band
n_i	Intrinsic electron density
ϕ_b	Fermi-intrinsic band bending
V_{bi}	Built-in potential, band bending
V_{FB}	Flat band voltage
k_B	Boltzmanns constant
T	Temperature
q	Electron charge
V_{th}	Thermal voltage
h	Plancks constant
\hbar	Reduced Plancks constant
E_g	Silicon band gap
X_s	Electron affinity silicon
φ_m	Gate contact work function
Φ_s	Silicon work function
E_F	Fermi level

E_i	Intrinsic fermi level
V_F	Quasi-fermi potential
V_T	Threshold voltage
μ_{eff}	Effective electron mobility
I_{DD}	Drift diffusion current
V_{gs}	Gate to source potential
V_{ds}	Drain to source potential
ϕ_m	Gate contact/center body potential difference

List of Figures

1.1	Circuit illustration of CMOS configuration to the left, with N- and P-channel (circle) discrete devices. To the right, a NAND logic circuit is shown utilizing the same components.	2
2.1	Schematic symmetrical DG MOSFET structure and its electrical and geometrical parameters considered in this work.	9
3.1	Mapping between corners and the real axis in W -space.	26
3.2	The body of the DG MOSFET mapped into the upper half of the (u, jv) -plane. The insets show the mapping functions for the u -axis (lower), the jv -axis (upper left) and the circle with radius $1/\sqrt{k}$. These represent the boundary, the gate-to-gate symmetry line, and the source-to-drain symmetry line, respectively. In this plot $k = 0.4278$	29
3.3	The orthonormal grid in Z -space transformed into W -space. Note the semi-circle at $u^2 + v^2 = 1/k$, which represents the line for $y = H/2$. In this plot $k = 0.4278$	30
4.1	The double-gate MOSFET extended body, illustrating the increased effective thickness of the silicon body, including the transformed oxide thickness t_{ox} to an equivalent silicon field displacement thickness t'_{ox}	33
4.2	Device potential distribution in the transformed W -plane for a rectangular grid in Z -plane. The drain contact is biased at $V_{ds} = 0.1$, and molybdenum gates at $V_{gs} = 0V$	38
4.3	The potential distribution in the Z -plane for drain biasing of $V_{ds} = 0.1V$ and symmetrical gates at $V_{gs} = 0V$	39
4.4	The potential distribution in the Z -plane for zero drain bias and symmetrical gates at $V_{gs} = 0V$	40

4.5	Potential distributions along the source-to-drain (SD) and gate-to-gate (GG) symmetry lines for zero drain and gate bias in subthreshold conditions. The modeling is shown with solid lines and the crosses indicates a corresponding numerical simulation of the device.	41
4.6	Drain-source barrier for $V_{ds} = \{0.05, 0.25, 0.5\}V$, indicating DIBL-effect in subthreshold. Solid lines indicate the modeling and crosses indicate corresponding numerical simulations.	42
4.7	Gate-gate potential at the source-drain minimum for $V_{ds} = \{0.05, 0.25, 0.5\}V$, and $V_{gs} = 0V$ in subthreshold. The modeling is shown with solid lines and the crosses indicates the numerical simulations.	42
4.8	Shift of source-drain barrier location versus V_{ds} for device lengths $L = \{50, 25, 20, 15, 12.5\}$ nm. The silicon and oxide thicknesses are held constant. The gates are biased at $V_{gs} = 0$ which corresponds to subthreshold conditions. The modeling results are shown as solid lines, while numerical simulations are indicated with crosses.	43
4.9	The drain influence on the minimum potential along the source-drain symmetry line for device lengths $L = \{50, 25, 20, 15, 12.5\}$ nm. The silicon and oxide thicknesses are held constant. The gates are biased at $V_{gs} = 0V$ which corresponds to subthreshold conditions. The modeling results are shown as solid lines, while numerical simulations are indicated with crosses.	44
4.10	Asymmetric operation of device with molybdenum and p^+ polysilicon gate materials at gate 1 and gate 2 respectively. Inversion carriers are shifted to the gate 1 interface. Shown for $V_{ds} = V_{gs} = 0V$	45
4.11	Numerical simulation of asymmetric operation of device with molybdenum and p^+ polysilicon gate materials at gate 1 and gate 2 respectively. Inversion carriers are shifted to the gate 1 interface. Shown for $V_{ds} = V_{gs} = 0V$. The potential reference is the source contact Fermi level.	46
4.12	Center potential calculated from the Laplace subthreshold model shown with solid lines and the numerical simulations of Poisson's equation are indicated with crosses, versus V_{gs} for $V_{ds} = 0V$	47
4.13	Threshold voltage dependence on gate length when holding silicon thickness constant. The modeling is for zero drain voltage, and numerical simulations are shown with crosses. This plot does not include the corrections associated with the oxide gaps discussed in Section 4.2.3.	51

LIST OF FIGURES

4.14 The parameter ϕ_m as a function of gate bias, compared with numerical calculations marked with crosses. At $\phi_m = 0$, the gate-to-gate distribution is flat. (Corrections for oxide gaps are included.) 52

4.15 The potential along the drain-source symmetry line for threshold, $V_{ds} = 0V$ and $V_{gs} = 0.25V$. The proposed model expression is shown as a solid line, the dashed lines are the two terms of the model expression in (4.35). Numerical simulations are indicated with crosses. The boundary conditions are indicated with circles. 55

4.16 The charge potential contributions along the drain-source symmetry line for threshold $V_{gs} = 0.25V$, and $V_{ds} = \{0.1, 0.25, 0.5\}V$. The modeled potentials $\phi_1(x)$ are shown as solid lines and numerical simulations are indicated with crosses. The boundary conditions are indicated with circles. 56

4.17 The potential contribution at the gate-to-gate symmetry line resulting from the body inversion charge for $V_{ds} = 0V$. Modeling is shown in solid and numerical simulations with crosses. 57

4.18 The total potential at the gate-to-gate symmetry line for $V_{ds} = 0V$. Modeling is shown in solid and numerical simulations with crosses. 57

4.19 The total potential for threshold, $V_{gs} = 0.25V$ and $V_{ds} = \{0.1, 0.25, 0.5\}V$, on the drain-source symmetry line. Modeling is shown in solid and numerical simulations with crosses. 58

4.20 The potential and quasi-fermi potential at the drain-source symmetry line for the near threshold region $V_{gs} = \{0.2, 0.25, 0.3\}V$ and $V_{ds} = \{0.1, 0.25, 0.5\}V$. Modeling is shown in solid (potential) and dashed (quasi-Fermi potential), numerical simulations with crosses. 59

4.21 Potential contour plot showing strong inversion conditions for the double-gate device. The flat region close to the gates (red) indicates that long-channel modeling can be applied. (The source and drain contacts in purple.) $V_{ds} = 0V$ 60

4.22 Strong inversion gate-to-gate potential distributions for $V_{gs} = \{0.3, 0.35, 0.4, 0.45, 0.5, 0.55, 0.6\}$, and with zero drain-source voltage. Modeling is shown in solids and numerical simulations are indicated with crosses. 61

4.23 Modeled (solid) and simulated (crosses) potentials versus gate voltage for the device center and the mid-gate silicon/oxide interface. $V_{ds} = 0V$ 62

4.24	Electron concentration for subthreshold conditions ($V_{gs} = 0V$) in the transverse direction, modeled with classical Boltzmann (dashed blue) and Fermi (solid blue) statistics compared with corresponding numerical simulations indicated with red line/crosses.	64
4.25	Electron concentration at threshold ($V_{gs} = V_T$) in the transverse direction, modeled with classical Boltzmann (dashed blue) and Fermi (solid blue) statistics compared with corresponding numerical simulations indicated with red line/crosses.	65
5.1	The potential distribution for threshold $V_{gs} = 0.25V$, and $V_{ds} = 0.1V$. The upper surface shows how the parabolic function is applied from gate to gate. The surface below is the absolute error between the numerical simulations and the parabolic approximation.	68
5.2	The subthreshold and near threshold drain current versus V_{gs} for $V_{ds} = \{0.1, 0.25, 0.5\}V$. Numerical simulations are marked with crosses.	70
5.3	I_{DD} - V_{ds} plot for a range of gate voltages. Solid lines indicate modeling and numerical simulations are marked with crosses. . . .	71
5.4	Illustration of the asymptotes which for each V_{ds} are from subthreshold and strong inversion calculations, and then adjusted for one threshold current calculation indicated with the crosses. . .	73
5.5	The m -parameter versus drain bias. Dashed line indicates a second degree polynomial least square curve fit.	73
5.6	$I_{DD} - V_{gs}$ interpolated plot for $V_{ds} = \{0.1, 0.25, 0.5\} V$, compared with numerical simulations indicated with crosses.	74
5.7	$I_{DD} - V_{ds}$ interpolated plot compared with numerical simulations indicated with crosses.	74
5.8	$I_{DD} - V_{ds}$ interpolated plot approximating the m -parameter from a polynomial curve fit. The modeling in solid is compared with numerical simulations indicated with crosses.	75
A.1	The elliptic integral as function of u , $k = [0, 1]$	83
A.2	The elliptic integral as function of ϕ , $k = [0, 1]$	83
B.1	Source to drain cuts of doping profile at the silicon/oxide boundary(blue) and at the center symmetry line.	88
B.2	Source contact potential profile for template and ideal device. . . .	89
B.3	Source to drain potential profile at the center symmetry line for template and ideal device.	90

Chapter 1

Background/introduction

1.1 Background

Over the last 40 years, semiconductor device technology has been developing with an amazing speed. With an exponential growth in integrated circuit performance, the scaling of MOSFET^a dimensions has been the primary driver. From the vantage point of today, in the 65 nm process era, we look 5 years into the future and find that the double-gate MOSFET (DG-MOSFET) is widely expected to take over for the long-lasting industrial favorite, the single-gate MOSFET. As scaling is expected to reach the 25 nm era in a few years¹, the DG-MOSFET becomes necessary in terms of its superior properties in this scaling region. The studies of this kind of device are mainly performed on numerical device simulators, with a few exceptions of laboratory experimental devices², creating a good foundation for further research into analytical compact models which are needed for circuit design. Current drive, potential distributions and short-channel effects are all important properties on which we base the comparisons with our proposal for a new compact analytical modeling framework.

Scaling of single-gate MOSFETs into the sub-100nm range, has been possible by for example using a high doping and steep doping gradients, which is detrimental for the charge carrier mobility. In a double-gate transistor, it is possible to achieve a high level of gate control by using a fully-depleted device body with low doping. This poses a new challenge in device modeling because of the two-dimensionality of the field pattern, which requires a new modeling strategy for short channel devices. This is in contrast to the continual patchwork on the classical single-gate MOSFET models, which are basically one-dimensional by nature.

^aMetal-Oxide-Semiconductor Field Effect Transistor

Another difference is the single-gate all-important threshold voltage parameter which marks the onset of the device for most models. In the context of the double-gate MOSFET, the earlier definition loses most of its foundation and meaning due to a different set of physical mechanisms controlling the on and off switching of the transistor.^{3 4 5}

A new model paradigm based on the specific central physical mechanisms in this kind of device is therefore desirable and creates a foundation for the work presented in this thesis.

1.1.1 MOSFET/CMOS historical overview

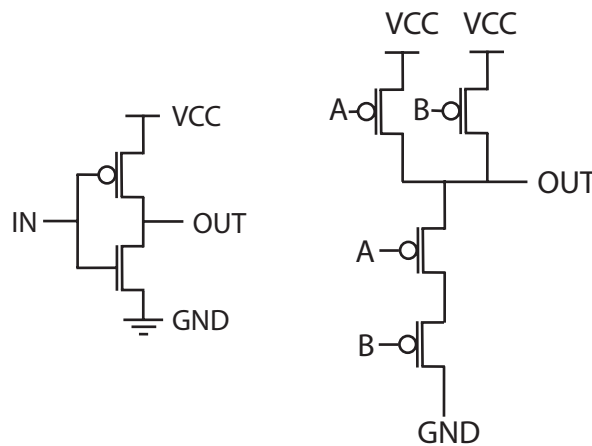


Figure 1.1: Circuit illustration of CMOS configuration to the left, with N- and P-channel (circle) discrete devices. To the right, a NAND logic circuit is shown utilizing the same components.

In 1963, Fairchild Semiconductor invented CMOS^b circuits⁶. Five years later, RCA created CMOS-based integrated circuits illustrated in Figure 1.1. The new invention had a long switching time, but had less standby power than the BJT^c based TTL^d circuits at that time. CMOS technology was used in battery-critical applications, such as watches, where less power was more important

^bShort for complementary MOSFETs, consisting of one N- and one P-channel MOSFETs in series.

^cBipolar Junction Transistor

^dTransistor transistor logic

than speed. Early generations of CMOS logic were based on aluminum gates, which could operate and interface with the old TTL logic. The advancements in device processing permitted a continual down-scaling of the device feature size, which allowed reduction of the power supply voltages and better performance. These advances became more important than backward compatibility with TTL. A switch to poly-silicon gates, which had better resistance to annealing, introduced the concept of self-aligned gates, resulting in lower overlap and stray capacitances. Later, the focus on increased speed, smaller dimensions and less power consumption has resulted in a thriving development where integration density and power dissipation are the main challenges.

1.1.2 Importance of CMOS

CMOS based technology is, and has been, the main contributor to steadily decreasing switching time in digital circuits and high speed performance of analog electronics. Important aspects, such as established production technology, low power dissipation, and integratability have made the popular technology the greatest driver of new computation intensive hardware and software. Compared to the single transistor gate logic which consisted of an NMOS transistor only with a resistor pull-up and the BJT-based TTL, the CMOS established a completely new paradigm for circuit power consumption and speed. After this transition, CMOS technology has had no major challengers from other technologies. This state of affairs is expected to continue for at least one more decade with the new advances in MOSFET technologies, including double-gate, gate-all-around, and FinFET as the most promising configurations.

1.1.3 Technology-development scaling Moore's law

In 1965, Gordon Moore, the co-founder of Intel, one of today's greatest manufacturers of integrated circuits, made the statement that: *"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer."* This soon turned into an addiction for the semiconductor industry and the famous statement was adopted as Moore's law. The doubling of performance every second year has created a market driven demand of expectations that the future will give the same increase in performance.

1.1.4 Integrated circuit design - tools

With the demand for evermore complex circuits, the design of such circuits requires efficient simulation tools. Designing new integrated circuits involves the use of several electronic design automation (EDA) tools for high-level digital design, mask level synthesis, and simulation and modeling of discrete devices. In this work, we are primarily interested in device modeling as it relates to circuit simulation and the device simulation for model verification.

1.1.5 Device simulation (TCAD) - applications

Numerical device simulation mostly involves iteration over Poisson's equation in combination with a transport model for a given set of boundary conditions. A common way to solve this problem is to discretize the 2D surface or 3D volume with a grid and iterate over this with a PDE^e solver. Convergence and accuracy of the solutions depends strongly on the grid distribution and size. In addition, convergence time depends strongly on the solver type, models for carrier statistics, and current continuity. Typically, numerical solvers are not applicable for simulating integrated circuits due to the high computational overhead. In the present work, we have used the device simulator Atlas from Silvaco. Central in this tool is a range of models for physical phenomena behavior such as charge carrier transport models, classical and quantum carrier statistics, material properties, etc. These can be combined in the simulation of specific transistor configurations.

1.1.6 Circuit simulation - SPICE

Tools for simulating the behavior of simple circuits, began emerging in parallel with the development of integrated circuits. The tool CANCER (Computer Analysis of Non-Linear Circuits Excluding Radiation) was developed by Ronald Rohrer of U.C. Berkeley along with some of his students in the late 1960's⁷. In the seventies CANCER was re-written and called SPICE (Simulation Program with Integrated Circuits Emphasis), released as version 1 to the public domain in May of 1972. The program has gone through several important evolution steps later on. Central elements in circuit simulators are the device models. Different research groups have steadily provided models and modeling approaches to SPICE, adding a wide range of functionality to the simulator engine. The MOSFET model BSIM by the Berkeley group has been highly successful and was an industry standard for many years. In 2005, for the first time since the seventies, the Compact Model Council, which works for a standardization of compact

^ePartial Differential Equation

models and model interfaces, has decided to make the PSP⁸ model developed by Philips semiconductors and Pennsylvania State University the industry standard, succeeding the Berkeley groups BSIM3 and BSIM4. ^f

SPICE simulators come with a selection of models for different semiconductors. Choosing the most effective and exact model for the circuit simulation is a difficult task and often leaves the circuit designer with a dilemma, whether to choose a time-consuming precise model or a more simplified and quick model for simulation and parameter extraction. Precise models are often characterized by many parameters that have to be identified empirically by analyzing measurements or TCAD simulations. This may be a quite difficult task considering that some models use several hundred parameters. These parameters cannot always be associated directly with physical mechanisms. However, for a specified technology, this task only has to be performed once by the transistor manufacturer. The numerical tools sometimes come with additional parameter extractors which aid the designer in the process.

1.1.7 Device modeling - compact/analytical models

In the present context, a physics based device model is understood to be a description of device behavior in terms of analytical, algebraic expressions. This is contrary to device simulations, which are numerical derivations behavior based on complex equations, such as partial differential equations.

Furthermore, device models may be characterized as being compact if they are described in terms of analytical, explicit expressions. Compact models can also cover models which involves preprocessing of model expressions by iterative routines that result in parameter lookup-tables for fast retrieval for use in simplified parameterized models. Compact models have the characteristic of being computational efficient in the context of circuit simulations.

^fWeb site: <http://www-device.eecs.berkeley.edu/bsim/>

1.2 Objectives of thesis

The objective of the present work is to establish a detailed, physically based framework for precise modeling of short-channel double-gate MOSFETs. This framework may serve as an excellent starting point for the development of more compact modeling expressions suitable for use in circuit simulators. One possibility is to use a set of generic, semi-empirical expressions for the I-V characteristics with parameters that can be extracted to any desired accuracy from the framework. Typically, such a model may be based on explicit sub-threshold and strong-inversion limits that are readily available from the modeling framework, and on the bias dependences of I_d near threshold expressed in terms of extractable parameters.

The modeling framework will be based on a two-dimensional analysis, taking into account short-channel effects with a set of clearly defined simplifications, and be largely based on analytical expressions for central parts of the model calculations.

1.3 Challenges/Scope

Some of the main challenges for developing a nanoscale short-channel DG MOSFET model are the modeling of:

- 2D electrostatics
- Self-consistency
- Charge transport
- Quantum-mechanical effects
- Gate tunneling
- Noise

In the present work, we are considering (as an example) a double-gate MOSFET with a gate length of 25nm and a silicon film thickness of 12nm.[§] This means that source/drain contact will have a significant influence on the conducting channel. This 2D capacitive effect is dominant in subthreshold due to the small concentration of mobile and fixed charges. Near threshold the electrostatic influence from the inversion charge become significant and has to be taken into consideration in a self-consistent manner. In strong inversion the

[§]The complete description of the device properties is provided in Section 4.1

electrons dominate the device electrostatics, although the capacitive effects will still be important.

In nanoscale MOSFETs, with channel lengths less than about 50 nm, the relaxation times of the carriers indicate that the drain current will have the character of both drift-diffusion and ballistic/quasi-ballistic transport. In this work, to make the transport modeling manageable, we have used the drift-diffusion transport model to validate the electrostatic modeling techniques and simplifications which have been applied to the modeling process. Ballistic and quasi-ballistic transport are briefly discussed in the review of models in Chapter 2.

When device dimensions are larger than 10nm, classical theory is still applicable.⁹ For smaller dimensions, quantum confinement has to be considered. In this work, the modeling is based on classical theory, but some examples of quantum-mechanical confinement in one direction are also shown.

The modeling of gate tunneling is considered to be beyond the scope of this work. We have considered high- κ dielectric with a permittivity of 7 and a thickness of 1.6 nm, in which case the tunneling current is relatively small.¹⁰ Noise modeling is also beyond the scope of the present work.

1.4 Outline of thesis

In this thesis, we present a new technique for 2D modeling of short-channel, nanoscale DG MOSFETs. In low-doped devices working in the subthreshold regime, the potential distribution is dominated by the capacitive coupling between the body contacts. This 2D potential is determined by an analytical solution of the Laplace equation for the body using the technique of conformal mapping. Near and above threshold, the influence of the electronic charge on the electrostatics is taken into account in a precise, self-consistent manner by combining suitable model expressions with Poisson's equation. For finite drain voltages, the self-consistency also extends to a calculation of the quasi-Fermi potential and the drain current using the drift-diffusion transport mechanism. In strong inversion, where the electronic charge dominates the device electrostatics, the device behavior approaches that of a long-channel device.

Throughout the thesis, intermediate results such as electrostatics and drain current modeling are verified against the numerical simulator Atlas developed by Silvaco.

In chapter 2, we review existing models for DG MOSFET devices related to the type considered in this work. The theory introduced in this chapter represents much of the foundation for the modeling work in the subsequent chapters.

In Chapter 3, the method of conformal mapping is introduced. The solution of the 2D Laplace equation is more easily derived in a complex transformed plane into which the device body is mapped, yielding analytical results. This solution is then mapped back to the normal plane using a mapping function for the coordinates between the two planes.

In Chapter 4, the specification for the considered device technology is presented, followed by a discussion of the electrostatic modeling, covering all plausible ranges of DC-voltages.

Applying the superposition principle to Poisson's equation, the contribution to the 2D electrostatics from the capacitive coupling can always be separated out and determined from Laplace's equation. In order to make this part manageable, we assume that each of the contacts, source, drain, and the gates, is equipotential. This is achieved by using metal gates and source/drain Schottky contacts. The source and drain contacts are chosen to have the same work function as that of n^+ silicon. The gate metals are chosen to have a near midgap work function, which is needed to obtain a suitable threshold voltage of 0.25 V.

In the sub-threshold regime, the device electrostatics is dominated by capacitive coupling between the electrodes resulting in an explicit, analytical expression for the potential distribution.

Close to threshold, the mobile charge carriers become significant and influence the device electrostatics to a such degree that the electrostatic potential must be evaluated self-consistently based on Poisson's equation. Moreover, the quasi-Fermi potential arising from the channel current will also be taken into account.

In strong inversion, where the electronic charge dominates the device electrostatics, the device behavior approaches that of long-channel devices. Long-channel models of the double-gate device exists, and are used in this operating regime.

In Chapter 5, the drain current modeling is shown using the drift-diffusion transport mechanism. In this modeling, we show that the barrier minimum and its proximity are all-important in the drain current calculations.

Finally, an example of a parametrized, compact current-voltage model is presented, where the parameters are extracted from the full modeling framework.

Chapter 6 contains conclusions and Chapter 7 discusses possible future work.

Chapter 2

Review of DG MOSFET models

This chapter gives an introduction to the evolution of DG MOSFET modeling, with a review⁹ on advantages and weaknesses. In particular, modeling which is central to the later improved models, will be discussed rigorously. For all DG

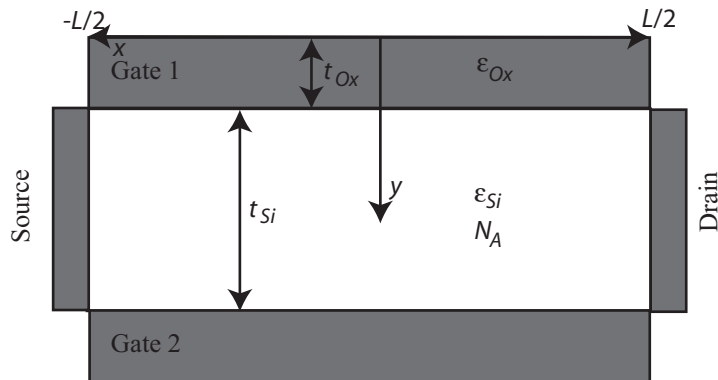


Figure 2.1: Schematic symmetrical DG MOSFET structure and its electrical and geometrical parameters considered in this work.

MOSFETs which are dominated by 2D electrical fields, the electrostatic potential ϕ can be found by Poisson's equation:

$$\nabla^2 \phi(x, y) = \frac{q}{\epsilon_{Si}} (N_S + n) \quad (2.1)$$

Considering an n-channel device, the x -axis is the lateral direction along the gate, q the electron charge, ϵ_{Si} the permittivity of silicon, N_S and n are the acceptor doping and mobile charge density respectively. The classical Boltzmann 3D density of mobile charge carriers is found as:

$$n = \frac{n_i^2}{N_S} \exp((\phi - V_F)/V_{th}) \quad (2.2)$$

where n_i is the intrinsic carrier density for undoped silicon, V_F and V_{th} the quasi-Fermi and thermal voltage respectively. To find the quantum confinement effects related to ultra-thin device bodies, the following expression for quantum-mechanical inversion carrier concentration per unit area is valid for a 1D confinement:¹¹

$$n_s = \frac{m_n}{\pi \hbar^2} k_B T \sum_{j=1}^l \ln \left[1 + \exp \left(\frac{E_F - E_j}{k_B T} \right) \right] \quad (2.3)$$

where m_n is the density of states effective mass, and E_j is the lowest energy of sub-band j measured relative to the conduction band.

For compact modeling of drain current, there are two main strategies. Firstly, drift-diffusion¹², where carriers experience a considerable amount of collisions in the conducting channel. Secondly, ballistic¹³ current in very short devices, which is dominated by a mechanism where the carriers have enough energy to cross the barrier before being subjected to significant scattering. Between these two distinct models, we have quasi-ballistic¹⁴ behavior which is described as ballistic transport with a statistical ballistic carrier scattering quotient included as a model parameter.

2.1 Long-channel modeling

Long-channel modeling is the procedure where the 2D field contribution can be regarded as an inferior mechanism to the main channel control mechanism by the gate. This means that when the electrical fields associated with the body charge carriers terminate mainly on the gate electrodes, we postulate that the device exhibits a long-channel behavior. This implies that it is sufficient to solve the Poisson equation in one dimension transversal to the channel to capture the main body effects. Nonetheless, charges close to the source and drain contacts will terminate their fields completely or partially on these contacts (charge sharing).

2.1.1 Modeling of undoped devices

For DG devices which exhibit long-channel behavior, it is possible to take advantage of this and tackle the relatively small short-channel effects by suitable approximations. This is done in several models, which all are mostly concerned with the solution of Poisson's equation in 1D (transversal direction).

Taur-model for undoped body

A long-channel double-gate device with an undoped silicon body can be described by an implicit analytical solution of the 1D Poisson's equation¹⁵. Integrating once, we obtain

$$\frac{d\phi}{dy} = \sqrt{\frac{2qV_{th}n_i}{\epsilon_{Si}} (\exp(\phi/V_{th}) - \exp(\phi_0/V_{th}))} \quad (2.4)$$

where ϕ_0 is the potential on the symmetry plane midway through the silicon body $y = t_{ox} + t_{Si}/2$. Integration of 2.4 gives

$$\frac{\phi - \phi_0}{2V_{th}} = -\ln \left[\cos \left(\sqrt{\frac{qn_i}{2\epsilon_{Si}V_{th}}} \exp(\phi_0/V_{th})(y - (t_{Si} + 2t_{ox})/2) \right) \right] \quad (2.5)$$

The oxide/silicon surface potential $\phi_s = \phi(y = t_{ox})$ is found by invoking continuity in the displacement fields at this interface, i.e.

$$\epsilon_{ox} \frac{V_{gs} - V_{FB} - \phi_s}{t_{ox}} = \epsilon_{Si} \left. \frac{d\phi}{dy} \right|_{y=t_{ox}} \quad (2.6)$$

The result is an implicit dependence of ϕ_0 on the gate-source potential V_{gs} .

The current modeling, is found by combining (2.5) and (2.6) with the drift-diffusion equation, resulting in¹⁶

$$I_{DD} = \frac{16V_{th}^2 \epsilon_{Si} \mu_{eff}}{Lt_{Si}} [g_r(\beta_s) - g_r(\beta_d)] \quad (2.7)$$

where β is an integration variable, and

$$g_r(\beta) = \beta \tan(\beta) - \beta^2/2 + \rho\beta^2 \tan(\beta^2) \quad (2.8)$$

,

$$f_r = \ln(\beta_{s/d}) - \ln(\cos(\beta_{s/d})) + 2\rho\beta_{s/d} \tan(\beta_{s/d}) \quad (2.9)$$

have to satisfy the boundary conditions at source (β_s) and drain (β_d) in the following two implicit expressions

$$f_r(\beta_s) = \frac{1}{2V_{th}} [V_{GS} - V_0] \quad (2.10)$$

and

$$f_r(\beta_d) = \frac{1}{2V_{th}} \left[V_{GS} - V_0 - V_{DS} \right] \quad (2.11)$$

where $V_0 \equiv V_{FB} + 2V_{th} \ln \left[\frac{2}{t_{Si}} \sqrt{\frac{2\epsilon_{Si}V_{th}}{qn_i}} \right]$ and $V_t = V_0 + \delta$ is the threshold voltage. Here, $\delta = 2V_{th} \ln [(V_{gs} - V_0)/4rV_{th}]$ and $r = \epsilon_{Si}t_{ox}/\epsilon_{ox}t_{Si}$.

For long channels ($L = 1\mu m$) and a thin silicon film ($t_{Si} \leq 25nm$), the modeling gives results in total agreement with numerical simulations.

2.1.2 Methods for including effects of doping

For n-channel devices, a light acceptor doping will shift the body quasi-Fermi potential towards the valence band by $\phi_b = V_{th} \ln \frac{N_s}{n_i}$, creating a larger potential difference between contacts and body (V_{bi}). Assuming that the light doping represents relatively few carriers in a thin device, the electrostatic effect from the dopants can be regarded as negligible in strong inversion. Hence, it is possible to use the solution from Taur (2.7) or Ortiz-Conde¹⁷ by including the potential shift for the body.¹⁸ In sub-threshold, the dopant electrostatic effect will eventually dominate over the mobile carriers. Approximations have to be made to solve Poisson's equation in this case.

Francis modeling of weak and moderate inversion

A 1D modeling procedure which includes body doping has been proposed by Francis et al.¹⁹. In sub-threshold when the mobile charge density is much less than the body doping concentration, it is found that $\phi_S - \phi_0$ is constant. Poisson's equation can be reduced to its depletion form, taking only into account the fixed charges with

$$\phi_S - \phi_{0,appr} = \frac{qN_s t_{Si}^2}{8\epsilon_{Si}} \quad (2.12)$$

Applying Gauss' law at the surface, the charge can be integrated along the channel and express the current.

For moderate inversion, an accurate modeling of the surface potential from a Taylor expansion of Poisson's equation, gives

$$\frac{d^2\phi(y)}{dy^2} = \frac{q}{\epsilon_{Si}} \left(N_s + \frac{n_i^2}{N_s} \exp[(\phi_S - (t_{Si}/2 + y)E_S)/V_{th}] \right) \quad (2.13)$$

and a double integration of this gives the implicit integral equation

$$\phi_S = C_2(\phi_S, E_s) + V_{th}^2 \frac{q}{\epsilon_{Si}} \frac{n_s}{E_s^2} \quad (2.14)$$

where

$$C_2 = V_{gs} - V_{FB} + V_{th} \frac{q}{\epsilon_{Si}} \frac{n_s}{E_s} \quad (2.15)$$

$$\times \left(\frac{\epsilon_{Si}}{C_{ox}} \left[\exp\left(-\frac{E_s t_{Si}}{2V_{th}}\right) - 1 \right] - V_{th} \frac{1}{E_s} \right) - \frac{qN_S t_{Si}}{C_{ox} 2}$$

is an integration constant, E_s and ϕ_s are the surface field and potential, n_s is the surface electron concentration, C_{ox} is the gate oxide capacitance, and N_S is the body acceptor dopant.

(2.14) and (2.15) can be solved iteratively, and through Gauss' law, to give a direct relation between the gate voltage and the surface potential. The current can be modeled as follows

$$I_{DD} = 2 \frac{V_{ds}}{L} \int_{-t_{Si}/2}^0 q\mu n(x) dx \quad (2.16)$$

where the mobility μ is considered constant. The model is valid for small drain-source voltages, and does not include short-channel effects such as DIBL. A threshold voltage model is also derived from a transconductance analysis, which gives the maximum transconductance change I_{DD} vs V_{gs} , independent of series resistances.

Baccaranis modeling of weak to moderate inversion

Modeling of doped devices can be thought of by having two back-to-back SGDs with two inversion channels close to the gates. This implicitly assumes that the current flowing through the device center at $y = t_{Si}/2$ is negligible compared to the inversion carrier current found at the body/insulator interfaces. Based on the gradual channel approximation²⁰

$$I_{DD} = 2 \frac{\mu}{L} \frac{C_o}{1 + \alpha_n V_{ds}} \int_0^{V_{ds}} [V'_G - \phi_c(V)] dV \quad (2.17)$$

where C_o is the gate capacitance, $\alpha_n = \mu/v_{sat}L$, where v_{sat} is the saturation velocity, and $V'_G = V_{gs} - (\varphi_m - X_s + qN_S/2C_g)$ the effective gate voltage. $\phi_c(V)$ is the center potential found implicitly by

$$2C_g (V'_G - \phi_c) = -Q_c(\phi_c, \phi_{Fn}) \quad (2.18)$$

where $Q_c = -qN_C \exp[(\phi_c - \phi_{Fn})/V_{th}]$, assuming Boltzmann statistics, though an expression for Fermi statistics and quantum mechanical effects may be used.

This equation holds for drain voltages not exceeding the drain saturation voltage $V_{DSS} = \frac{1}{\alpha_n} \left(\sqrt{1 + 2\alpha_n(V_{gs} - V_T)} - 1 \right)$. The threshold voltage can be found as

$$V_T = \varphi_m - X_s + qN_S/2C_g + V_{th} \log \left(\frac{2C_g V_{th}}{qN_C} \right) \quad (2.19)$$

For gate voltages leading to strong inversion, the center potential ϕ_c is pinned to the threshold voltage, resulting in the following expression for drain current

$$I_{DD} = 2 \frac{\mu}{L} \frac{C_o}{1 + \alpha_n V_{DS}} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (2.20)$$

and for drain voltages above saturation $V_{ds} \geq V_{DSS}$,

$$I_{DD} = 2 \frac{\mu}{L} \frac{C_o}{1 + \alpha_n V_{DSS}} \left[(V_{GS} - V_T) V_{DSS} - \frac{1}{2} V_{DSS}^2 \right] \quad (2.21)$$

which both are close to the standard SGD form except for some effects related to the partial depletion body effects. In sub-threshold, the current takes on the same form as the standard MOSFET equations,

$$I_{DD} = 2 \frac{C_o \mu}{L} V_{th}^2 \exp [(V_{GS} - V_T)/V_{th}] [1 - \exp(-V_{ds}/V_{th})] \quad (2.22)$$

NanoMOS

A group at Purdue University²¹ has developed a complete simulator founded on the assumption on a double-gate ultra-thin body and can be regarded as a long-channel modeling, despite that short gate channels below 100nm may be simulated. Assuming further on that the transistor is scaled to a such degree that the carrier mean free path distance becomes comparable to the effective gate length, a ballistic or at least quasi-ballistic transport behavior can be expected. The fact that the ultra-thin body can be no more than $t_{Si} < 5nm$ of thickness in this modeling, implies that the transversal quantum phenomena is an important factor to be accounted for. Thus, both a real and a quasi-2D Schrödinger solver have been implemented to provide a benchmark, and give better simulation time performance, respectively. For a fully ballistic transistor, a full 2D Schrödinger solution can be calculated. Since this is not compatible with expressions for compact models, approaches which remedy the complexity are commonly applied. A quasi-2D approach, which is easier to solve, decouples the transport and the always quantified transverse direction. By using this technique, quantization of the transport channel is voluntary and a classical or quantization method can be chosen for the current calculation. For ultra-short devices which approaches the ballistic limit (no scattering), the channel quantization is necessary, but for longer

semi-ballistic configurations, a slow varying classical potential method should be chosen due to computational effort. The boundary conditions of the solvers are based on a non-equilibrium Green's function formulation.

The quasi-2D model calculates the transversal quantum confinement, and the longitudinal confinement before the results is fed into a Poisson solver and checked for convergence. Because of this, the simulator enters an iteration scheme, which is hardly compact. Despite of this, the simulator has properties which renders it very interesting for further compact modeling. Among these are the transport model.

For short device gate lengths, the mechanisms involved in charge transport become different. The charge transport gradually changes from a drift-diffusion type to a ballistic current which is determined by quantum calculations. If carriers experience only a few scattering events along the channel, the carrier injection at the source will, rather than the channel, be the limiting factor. It has been shown that for sub-30nm devices it is experienced a high degree of ballistic transport with little or no scattering of charge carriers.²²

Looking at weak inversion and depletion in SG devices, Ferrier²³ has developed analytical expressions based on Airy-based quantization. It differs from standard Airy quantization by taking into account the insulator tunneling effect. In addition, the model considers a multi-band transport, which is more applicable to thicker devices than the ultra-thin assumption which assumes single-band transport.

In the Natori formalism^{13 24}, a ballistic current is calculated from two electron emitters which both generates a flux of charge. These are located at the source (F^+) and drain (F^-) with opposite directions of the current.

$$I_B = q(F^+ - F^-) \quad (2.23)$$

The carriers from these emitters are filtered through the quantum states at the barrier maximum, it is only the electrons with the high enough energy which are filtered through the available barrier quantum states which are transported across the barrier. The flux is given by

$$F^\pm = \frac{(2k_B T)^{3/2}}{\pi^2 \hbar^2} \left[\sum_i \sqrt{m_{cL}} F_{1/2} \left(\frac{E_{F_s} - E_i^L - qV^\pm}{k_B T} \right) + \sum_i \sqrt{m_{cT}} F_{1/2} \left(\frac{E_{F_s} - E_i^T - qV^\pm}{k_B T} \right) \right] \quad (2.24)$$

where

$$F_{1/2}(u) = \int_0^\infty \frac{\sqrt{y}}{1 + \exp(y - u)} dy \quad (2.25)$$

is the Fermi-Dirac integral of order 1/2, which corresponds to a 1D transverse quantum mechanical quantization to the channel. E_{F_s} is the Fermi level at the source, E_i are the quantum levels at the barrier maximum, and $V^+ = 0$ and $V^- = V_{ds}$ are the source and drain potentials respectively. The conduction masses are m_{cL} and m_{cT} for the primed (L)ongitudinal and unprimed (T)ransverse ladder respectively. These are given as the conduction longitudinal mass $m_{cL} = m_t$ and the combined conduction transverse mass $m_{cT} = (\sqrt{m_l} + \sqrt{m_t})^2$ from the quantization masses m_l (longitudinal) and m_t (transverse).

By using a Fermi-Dirac integral of order 1/2, we assume that the quantum effects on carriers are negligible in the transport and transistor width direction.

We can obtain the inversion sheet charge density by using the two-dimensional density of states function along with the Fermi distribution function.

$$|Q| = \frac{qk_B T}{2\pi\hbar^2} \sum_{valleys} \sum_{n_x} \sqrt{m_x m_y} \times \ln \left[1 + \exp \left(\frac{E_{F_s} - E_{ij} - qV^\pm}{k_B T} \right) \right] \quad (2.26)$$

Compact and exact expressions for general 1D quantum wells are not possible to find. Such problems can be solved by Schrödinger/Poisson solvers. These numerical solvers use iterative routines, which are too computationally intensive for compact modeling. However, there are ways to compute quantum effects which gives very good agreement between the exact solution and the so-called quasi-approaches.

For example, sub-band engineering can be used to create a device in the electric quantum limit, where only one state is occupied.

$$I_B = W I_0 [F_{1/2}(u) - F_{1/2}(u - v_d)],$$

$$I_0 = \frac{\sqrt{2}q(k_B T)^{3/2}}{\pi^2 \hbar^2} M_v \sqrt{m_i}, \quad (2.27)$$

$$u = \ln[\sqrt{(1 + e^{v_d})^2 + 4e^{v_d}(e^p - 1)} - (1 + e^{v_d})] - \ln 2,$$

$$v_d = \frac{qV_{ds}}{k_B T} \quad (2.28)$$

$$\rho = \frac{2\pi\hbar^2 C_{eff}(V_{gs} - V_T)}{qk_B T m_t M_v}$$

where $Q_{eff} = C_{eff}(V_{gs} - V_T)$ is the effective electron concentration at the maximum channel barrier.

As an ideal ballistic transport hardly will take place in any physical device, a formalism for quasi-ballistic transport which includes scattering has been developed by Lundstrom.¹⁴

Quasi ballistic transport includes correction terms for the expression in (2.23) resulting in

$$I_B = q(F^{+} - (rF^{+} + (1 - r)F^{-})) \quad (2.29)$$

where r is defined as the reflection coefficient. Different conditions apply for a low and high lateral field. For high fields, a critical distance l_{kT} defines where the potential drops $k_B T/q$ from the source. If the backscattering of a carrier happens inside this critical distance, the carrier will not be able to pass the barrier because of insufficient energy in the channel direction. It is, in addition, likely that the carrier will not go back into the source, but will be reflected by the channel potential and undergo a drift transport toward the drain contact.¹⁴ From this it follows that the high-field coefficient is

$$r_{HF} = \frac{l_{kT}}{l_{kT} + \lambda} \quad (2.30)$$

where λ is the mean free path and l_{kT} is the distance over which the channel potential drops by V_{th} . The high field coefficient has been developed from the low field scattering coefficient which can be obtained from the Mc Kelvey's flux method^{25, 26}.

$$r_{LF} = \frac{L_{eff}}{L_{eff} + \lambda}, \lambda = \frac{2\mu k_B T}{v_t q}, v_t = \sqrt{\frac{2k_B T}{\pi m}} \quad (2.31)$$

where L_{eff} is the effective channel length, λ the low field mean free path, μ the low field mobility and v_t the injection velocity. In addition a unified expression between the two regimes have been presented in²⁵.

2.2 Short-channel models

In so-called short-channel devices, the length/height aspect ratio is so small that the 2D effects contribute so much to the device behavior that they become non-negligible when modeling. This manifests itself through various short-channel effects (SCEs), such, for example drain-induced barrier lowering (DIBL).²⁷ To deal with this in a precise manner, a 2D device model is needed, where both the capacitive coupling between the electrodes (source, drain and gates) and the electrostatic effects of the space charge are self-consistently included. For

nanoscale devices (less than 50nm in length), we also have to be concerned with ballistic and quasi-ballistic current modes involving non-stationary charge transport mechanisms.

2.2.1 Approximate models, quasi-2D

Parameterizing 2D effects does not come for free. Usually this approach generates a lot of empirically adjustable parameters that have to be determined in order to perform satisfying simulations. To avoid excessive use of parametrization, short channel effects have to be treated in more physical way. This has resulted in an effort to further development of the 2D analysis.

One of the main developments paths relies on the superposition principle²⁸, utilized in a range of modeling strategies.^{29 30} The method suggests that it is possible for undoped/lightly doped to separate Poisson's equation into a 2D capacitive part represented by Laplace equation

$$\nabla^2\phi(x, y) = 0 \tag{2.32}$$

and a 1D Poisson part which arises from mobile charges in the body. The total potential may then be expressed as

$$\phi(x, y) = \phi_1(y) + \phi_2(x, y) \tag{2.33}$$

where ϕ_1 and ϕ_2 is the 1D and 2D parts respectively. The 1D part can be thought of as the long-channel solution, while the 2D part will represent all short-channel effects. Separation allows a more flexible way of solving Poisson's equation.

2.2.2 Quasi-2D approaches for an undoped/lightly doped body

In an undoped body, the potential will in principle follow the effective gate potential $V_{gs} - V_{FB}$. Adding short-channel effects, these will be the only which disturbs the electrostatic potential in the body. In lightly doped bodies, it is common to make the following assumptions about the effects related to the dopants. The electrostatic fields emerging from these can be neglected, and will only affect the built-in potentials.

Adding the assumption of subthreshold conditions, Liang and Taur's modeling procedure completely disregards dopants and free carriers^{31 10}. The 2D electrostatics is modeled with an infinite series of sinh and sin functions. For an aspect ratio (length/height) larger than 2, the modeling yields good results retaining only a couple of terms of the series.

Expanding the area of interest into a regime where free carrier fields cannot be neglected, self-consistency between 1D and 2D solutions become important.

The mutual interdependence can be found either with empirical trial functions or through iteration procedures.

Chen and Meindl's approach

Chen et al has proposed that a threshold based short-channel model can be found by solving Poisson's equation with only the mobile charge term⁵

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = \frac{q}{\epsilon_{Si}} n \quad (2.34)$$

where ϕ is the electrostatic potential referenced to the source Fermi potential and $n = n_i \exp[(\phi - \phi_F)/V_{th}]$ is the mobile charge term adjusted for the quasi-Fermi level ϕ_F . Since the quasi-Fermi level is assumed to incur most of the voltage drop near drain, the electrostatic potential is not influenced by the change. Then $n = n_i \exp[\phi/V_{th}]$, leaving the solution independent on V_{ds} , and thus incapable of finding the DIBL effect. To compensate for this approximation, a superposition different from (2.33) which solves the 1D equation in the transversal direction is applied. The 1D part is solved in the lateral direction

$$\frac{\partial^2 \phi}{\partial x^2} = \frac{q}{\epsilon_{Si}} n_i \exp[\phi_0/V_{th}] \quad (2.35)$$

subject to the boundary conditions $\phi_0(-L/2) = \phi_0(L/2) = V_{bi}$. The 2D remainder

$$\frac{\partial^2 \phi_1}{\partial x^2} + \frac{\partial^2 \phi_1}{\partial y^2} = \frac{q}{\epsilon_{Si}} n_i \exp(\phi_0/V_{th}) [\exp(\phi_1/V_{th}) - 1] \quad (2.36)$$

with $\phi_1 = 0$ at source and drain and continuous derivative with respect to permittivity at body/insulator interface. Arguing that the most significant change in the x -direction has been captured by $\phi_0(x)$, the 2D equation is solved with a Taylor expansion of the separation of variables truncated to the first term.

The threshold voltage is then found to be

$$V_T = V_{FB} + \eta V_{th} \frac{\cosh(\theta)}{\cosh(\theta/2)} \ln(Q_T/n_i t_{Si}) - \phi_{0m} \left[\frac{\cosh(\theta)}{\cosh(\theta/2)} \eta - 1 \right] \quad (2.37)$$

where θ and η are some geometrical constants from the 1D solution, related to the Debye length. Q_T is the inverse carrier density found by the long-channel approximation

$$V_{T,long} = V_{FB} + V_{th} \ln(Q_T/n_i t_{Si}) \quad (2.38)$$

and identified with numerical I-V simulations or measured data. A transport mechanism for this model has not been suggested by the authors.

2.2.3 Quasi-2D approaches for a strongly doped body

Including the effects of dopants invalidates a lot of the previously discussed modeling procedures. Depending on how high the body doping is, a single-gate behavior can be expected for high doping densities, and a combination of single-gate and volume inversion can be expected for lower doping concentrations.

Munteanu's approach

Empirical functions for modeling the electrostatic potential can be used as a solution to (2.1). Having found a suitable candidate with a few adjustable parameters to account for some intricate modeling details, may leave a compact, non-iterative expression. The advanced mathematical development of a series expansion can thus be avoided.

A simplified superposition of (2.1) can be found in Munteanu et al¹¹, where the electrostatic potential is divided into separate transversal and lateral solutions, giving

$$\phi(x, y) = \phi_S(x) \times A(x, y) \quad (2.39)$$

where ϕ_S is the surface potential on the body/insulator interface, and $A(x, y) = \frac{B(x, y)}{B(x, y=0)}$ is an envelope function, modulating the surface potential. In short-channel undoped devices, it is common to assume some kind of parabolicity in sub-threshold.^{30 32 33 34} However, for a relatively highly doped body, in the order of 10^{17}cm^{-3} or above, the volume inversion changes to two conducting channels even for sub-threshold conditions. The envelope function is developed from (2.5)¹⁵ and¹⁷ including the quasi-Fermi potential $V_F(x)$ along the conducting surface channel.

Utilizing the quasi-Fermi potential as proposed in³⁵ for bulk MOSFETs (and originally for sub-threshold conditions), which postulates a diffusion drain current, and expanding with a gate dependency in the last term, we get a trial function for the quasi-fermi potential

$$\begin{aligned} V_F(x) = & 2V_{\text{th}} \frac{m}{n} \quad (2.40) \\ & \times \ln \left[(\exp[-V_{ds}n/V_{\text{th}}m] - 1) (x/L)^{c/(V_{gs} - V_{\text{FB}})} + 1 \right]^{-1} \\ & \times (at_{Si})^{V_{ds}/3c} \end{aligned}$$

where m and n are structural parameters, and a, b, c are empirical adjustable

parameters. The surface potential differential equation is found with

$$\frac{d^2\phi_S}{dx^2} - \frac{2C_{ox}}{\epsilon_{Si}t_{Si}}\phi_S = \frac{1}{\epsilon_{Si}t_{Si}} [qN_S t_{Si} - 2C_{ox}(V_{gs} - V_{FB} - \phi_F) + q_i] \quad (2.41)$$

where q_i is the inversion charge evaluated either in a quantum-mechanical or the classical integral as a function of $\phi_S(x)$, creating an implicit expression for the approximate solution of (2.41):

$$\phi_S(x) = C_1 \exp(m_1 x) + C_2 \exp(-m_1 x) - \frac{R(x)}{m_1^2} \quad (2.42)$$

To fill the boundary conditions, C_1, C_2, m_1 are derived from geometrical and electrical properties, and $R(x)$ in addition consists of the inversion charge density.

Drain current is calculated with a classical drift-diffusion¹² approach with constant mobility

$$I_{DD} = \mu V_{th} [1 - \exp(-V_{ds}/V_{th})] / \int_0^L \frac{dy}{\int_0^{t_{Si}} q n_i \exp(\phi(x, y)/V_{th})} \quad (2.43)$$

which can be evaluated numerically and gives good results compared to both numerical and experimental data down to an aspect ratio (length/height) of 3.

UFDG

A modeling procedure dealing with short-channel effects have been developed at University of Florida, Gainesville.³⁶ The modeling accounts for carrier-energy quantization in the body, quasi-ballistic or ballistic carrier transport, capacitances, and parasitics.

$$\nabla^2 \phi(x, y) = \frac{q}{\epsilon_{Si}} (N_S) \quad (2.44)$$

The modeling is divided into two distinct areas, weak inversion and lower, and strong inversion. For weak inversion, the electrostatics is modeled with a superposition (2.33), solving for the transversal direction in 1D, neglecting the free carriers, assuming that the uniform body doping N_S is dominant in the electrostatics, by a second-order polynomial.³⁴

Finding an average channel length for the diffusion-dominated current is based on the encroachments of the depletion regions associated with the source and drain contacts, giving

$$L_e = L - L_s - L_d + 2L_D \quad (2.45)$$

where L_D is the Debye length defined by N_S and

$$L_s \cong \frac{2[\phi_b - \phi_{s(min)}]}{\left| \frac{\partial \phi(x,y)}{\partial y} \right|_{x=-L/2}} \quad (2.46)$$

and

$$L_d \cong \frac{2[\phi_b - \phi_{s(min)}] + V_{ds}}{\left| \frac{\partial \phi(x,y)}{\partial y} \right|_{x=L/2}} \quad (2.47)$$

The modeling of inversion carrier density is based on summation of sub-bands for an infinite square well at the virtual cathode near source, resulting in a compact quasi-Poisson and Schrödinger solver. Current is found by utilizing the ballistic or quasi-ballistic behavior, described in the NanoMOS section above.

Fourier expansions and Green's function

A popular approach to find the solution of the Laplace equation (2.32) has been to apply Fourier analysis on the 2D rectangular body. Even for doped bodies, where the mobile charge is considered negligible compared to the dopants, Poisson's equation

$$\nabla^2 \phi(x,y) = K \quad (2.48)$$

where $K = qN_S/\epsilon_{Si}$ is constant for a uniform doping, can be reduced to the Laplace equation by use of a proper trial function³⁷. Oh et al²⁹ proposed to use a Fourier expansion of modes, each with a characteristic length, for the Laplace part of the superposition (2.33). By truncating the series first found by Woo³⁸, to the lowest-order mode a more physical model can be obtained. Instead of assuming the transversal parabolic potential profile, a half-period cosine function is used, enforcing a continuous displacement field across the body/insulator interface.

Recently a Green's function approach has been used to solve Laplace parts of the Poisson's equation in a long-channel single-gate device, resulting in good agreement for the electrostatics in sub-threshold conditions³⁹.

2.2.4 Hydrodynamic/energy balance model

Current calculation with the drift-diffusion model neglects non-stationary transport effects such as velocity overshoot, carrier temperature associated diffusion, and the dependence on impact ionization rates. Derived from the Boltzmann transport equation, the energy balance model is built to capture these mechanisms and decomposes to the hydrodynamic model when the equations are

made independent on carrier mobility variations. One energy balance model⁴⁰, which is implemented in Silvaco Atlas, is used for verification of ballistic transport models.

2.2.5 Conformal mapping - outline

Compact models which deals with the two-dimensional nature of double-gate devices have been investigated intensively. Conformal mapping was introduced as a technique to cope analytically with the 2D effects of scaled device and the first example on inclusion of this technique was shown in⁴¹ where conformal mapping was used to map the fields of a semi-infinite slab of silicon onto a complex plane with analytical solutions. Taking into account the electrostatic fields from dopants into the boundary conditions for the 2D solution, gave rise to a very powerful method where most of the parameters dealing with short-channel effects in long-channel models could be eliminated due to the physical modeling. This modeling was later refined by Østhaug et al⁴², by simplifying the integrals associated with the conformal mapping procedure. The modeling was also verified against published experimental results from sub-100nm single-gate devices with good agreement.

Based on the good results, we have applied a conformal mapping procedure to a double-gate device, see Refs^{43, 44, 18, 45, 46, 47} where a device with aspect ratio (length/height) of 2 was considered. Here, significant 2D effects can be expected and a short-channel modeling procedure is necessary. The procedure has even been shown to work well in a quasi-3D analysis of gate-all-around (GAA) devices^{48, 49, 50}.

Chapter 3

Conformal mapping

Conformal mapping is a collection of transformations $z = x + jy = f(w = u + jv)$ which mathematically preserves angles and directions of curves through a point z_0 except at points where $f'(z)$ is zero. Conformal mapping is important in engineering mathematics, because boundary value problems in two-dimensional potential distributions may be solved in a simpler region than the original. For harmonic functions, which satisfy Laplace's equation $\nabla^2 h = 0$, the transformation f is also harmonic, and may be solved in the mapped space. A mapping that allows a complex multi-angled area in the $x, y \in Z$ -plane to be transformed into the upper half of the $u, v \in W$ complex plane, is the Schwarz-Christoffel transformation. In this transformation, f maps the real axis of W to the edges of the polygon in Z . If we postulate that the area in Z is solid and thus simply connected^a, the transformation is bijective, which means that f maps the two open sets into one another, in a one-to-one transformation.

This transformation allows us to find a solution of the electrostatic problem in the W -plane, and then map it back to the Z -plane. In Weber,⁵¹(pp.303) the electrostatic solution to the Laplace equation is further shown to be invariant to conformal mappings of the geometry at all regular points.

3.1 Schwarz-Christoffel transformation of the double-gate MOSFET

We are interested in finding the mapping of the device body from the Laplace equation. For $x, y, u, v \in \Re$, the independent complex variable $z = x + jy$ and

^aA part of the Riemann mapping theorem

3.1 Schwarz-Christoffel transformation of the double-gate MOSFET

the mapping function $f(z) = u(x + y) + jv(x, y)$, complex analysis implies that $\nabla^2 u = 0$ and $\nabla^2 v = 0$.

Considering the double-gate MOSFET, we find that the Schwarz-Christoffel transformation is a good candidate to map the rectangular structure onto a complex half-plane. The double-gate device, consisting of four right-angled corners, has the following Schwarz-Christoffel transformation with the four sides mapped onto the real axis in W

$$\frac{\partial z}{\partial w} = \frac{kC}{\sqrt{(1-w^2)(1-k^2w^2)}} \quad (3.1)$$

This is derived from the general transformation rules discussed in Appendix 1.1. This way the entire device boundary is mapped into the real axis of the W -plane. The corners of the body, which are identified as the inverse square root singularities in (3.1), are located at the following positions

$$\left\{ u_1 = 1, u_2 = \frac{1}{k}, u_3 = -\frac{1}{k}, u_4 = -1 \right\} \quad (3.2)$$

when moving along the positive real u -axis to infinity and back from negative infinity toward zero, illustrated in figure 3.1.

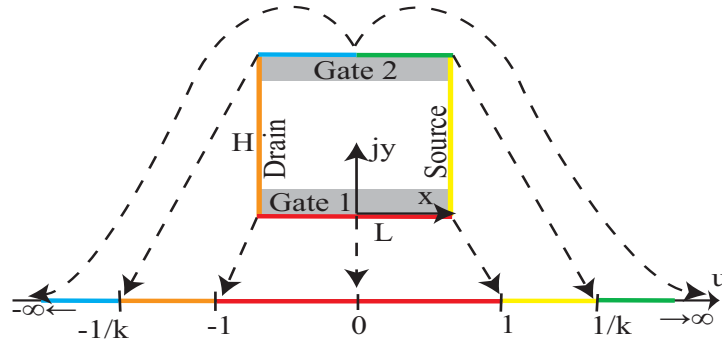


Figure 3.1: Mapping between corners and the real axis in W -space.

The integral form of (3.1) becomes

$$z = kC \int_0^w \frac{\partial w'}{\sqrt{(1-w'^2)(1-k^2w'^2)}} + C_1 = kC F(k, w) + C_1 \quad (3.3)$$

where C_1 is an integration constant which is zero if $z = 0$ defines the center of gate 1 (see 3.1) and maps into $w = 0$. Both C and the elliptic modulus k are

constants to be determined from the device geometry. F is defined by the general Legendre elliptic integral of the first kind:

$$F(k, w) = \int_0^w \frac{dw'}{\sqrt{(1-w'^2)(1-k^2w'^2)}} \quad (3.4)$$

Calculation of this integral is well defined and can be performed with simple iteration algorithms, look-up tables, or regular power expansions, see Appendix (1.1).

3.1.1 Geometric constants C and k

To complete the mapping between Z and W , the constants C and k have to be identified.

The *standard* elliptic integral of the first kind for F is defined for real values of $0 \leq w \leq 1$. Using (3.1) with $C_1 = 0$, the first corner along the x -axis at $L/2$ corresponding to $u_1 = 1, v = 0$ gives the following relationship between k and C

$$L = 2kC \int_0^1 \frac{du'}{\sqrt{(1-u'^2)(1-k^2u'^2)}} = 2kC K(k) \quad (3.5)$$

Here, $K(k) = F(k, 1)$ is the *complete* elliptic integral of the first kind. Each of the 4 intervals along the boundary is defined as a quarter-period⁵². The quarter-period $K(k)$ and $K(k')$ is defined in terms of the parameter k^2 and k'^2 where $k' = \sqrt{1-k^2}$. Then, because $F(k, 1/k) = K(k) - K(k')$

$$jH = kC [F(k, 1/k) - F(k, 1)] = jkC K(k') \quad (3.6)$$

where H is the height of the rectangle. From (3.5) we have

$$C = \frac{L}{2k K(k)} \quad (3.7)$$

and combining (3.6) and (3.7) gives

$$\frac{L}{2H} = \frac{K(k)}{K(k')} = \frac{K(k)}{K(\sqrt{1-k^2})} \quad (3.8)$$

from which k is determined. Hence the transformation in (3.3) simplifies to

$$z = x + jy = \frac{L F(k, u + jv)}{2K(k)} \quad (3.9)$$

3.1.2 Expressions along boundaries and symmetry lines

Along the boundary, $F(k, u)$ may be expressed in terms of the standard elliptic integral of the first kind as follows⁴⁵:

For $0 \leq u < 1$,

$$F(k, u) = \int_0^u \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}} \quad (3.10)$$

For $1 < u \leq 1/k$,

$$\begin{aligned} F(k, u) &= K(k) + j \int_1^u \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}} \\ &= K(k) + j \left[K(\sqrt{1-k^2}) - F\left(\sqrt{1-k^2}, \sqrt{\frac{1-k^2u^2}{1-k^2}}\right) \right] \end{aligned} \quad (3.11)$$

For $1/k < u < \infty$,

$$\begin{aligned} F(k, u) &= K(k) + jK(\sqrt{1-k^2}) - \int_{1/k}^u \frac{dt}{\sqrt{(t^2-1)(k^2t^2-1)}} \\ &= F\left(\sqrt{1-k^2}, \sqrt{\frac{1-k^2u^2}{1-k^2}}\right) - jK(\sqrt{1-k^2}) \end{aligned} \quad (3.12)$$

In addition, we have the symmetry property

$$F(k, -u) = -F(k, u) \quad (3.13)$$

The mapping expressions along the boundary thus become

$$x = \frac{L}{2} \begin{cases} F(k, u)/K(k), & \langle -1, 1 \rangle \text{ gate 1} \\ 1, & \langle 1, \frac{1}{k} \rangle \text{ source} \\ F(k, \frac{1}{ku})/K(k), & \langle \frac{1}{k}, -\frac{1}{k} \rangle \text{ gate 2} \\ -1, & \langle -\frac{1}{k}, -1 \rangle \text{ drain} \end{cases} \quad (3.14)$$

$$y = H \begin{cases} 0, & \langle -1, 1 \rangle \text{ gate 1} \\ 1 - F(k', \sqrt{1-k^2u^2}/k')/K(k'), & \langle 1, \frac{1}{k} \rangle \text{ source} \\ 1, & \langle \frac{1}{k}, -\frac{1}{k} \rangle \text{ gate 2} \\ 1 - F(k', \sqrt{1-k^2u^2}/k')/K(k'), & \langle -\frac{1}{k}, -1 \rangle \text{ drain} \end{cases} \quad (3.15)$$

This mapping is illustrated in the lower part of figure 3.2.

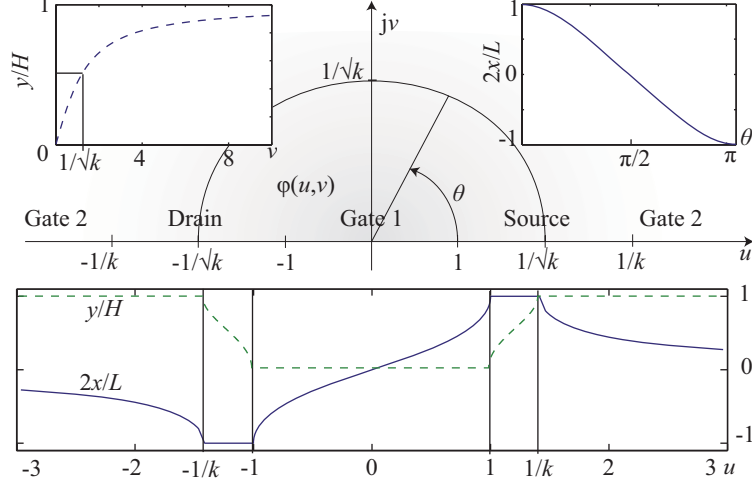


Figure 3.2: The body of the DG MOSFET mapped into the upper half of the (u, jv) -plane. The insets show the mapping functions for the u -axis (lower), the jv -axis (upper left) and the circle with radius $1/\sqrt{k}$. These represent the boundary, the gate-to-gate symmetry line, and the source-to-drain symmetry line, respectively. In this plot $k = 0.4278$.

Similarly, holding $u = 0$, the transformation of the jv -axis for the interval $v \in [0, \infty)$ to $y \in [0, H)$ can be done with

$$y = H F\left(\sqrt{1-k^2}, \frac{v}{1+v^2}\right) / K\left(\sqrt{1-k^2}\right) \quad (3.16)$$

From (3.16) we get the upper left plot in figure 3.2. A transformation which is also important is that of the source-drain symmetry line. In transformed W -space the line is a semicircle going through $v = 1/\sqrt{k}$. We prove this by postulating that $y = H/2$ corresponds to the imaginary part of the general transformation rule in (3.9) and that this remains constant as we move along the semi-circle $v = \sqrt{1/k - u^2}$. This implies that the point $(L/2, H/2) \in Z$ corresponds to the point $(1/\sqrt{k}, 0) \in W$. Solving for the source-drain symmetry line at $y = H/2$ we find

$$x = \frac{L}{2} F\left(\frac{2\sqrt{k}}{1+k}, \sqrt{ku}\right) / K\left(\frac{2\sqrt{k}}{1+k}\right) \quad (3.17)$$

shown in the upper right of figure 3.2. Here, $\theta = \cos^{-1}(\sqrt{ku})$.

3.1.3 Orthonormal grid in the Z-plane

Because of the complexity in the transformation function, it is hard to create a grid in W -space and then transform it to Z -space and end up with an orthonormal spacing. It is useful to create an orthonormal grid in real space in (x, y) -coordinates and then transform it through the elliptic *functions*, which can express the inverse of F . The elliptic functions are $\text{sn}, \text{cn}, \text{dn}$, leading to the inverse of equation (3.9)

$$w = u + jv = \frac{\text{sn}(x|k^2) \text{dn}(y|k'^2) + j \text{cn}(x|k^2) \text{dn}(x|k^2) \text{sn}(y|k'^2) \text{cn}(y|k'^2)}{\text{cn}(y|k'^2)^2 + k^2 \text{sn}(x|k^2) \text{sn}(y|k'^2)} \quad (3.18)$$

where the elliptic functions in this expression are reviewed in Appendix 1.1. The orthonormal grid in the Z -plane when transformed to the W -plane is shown in figure 3.3.

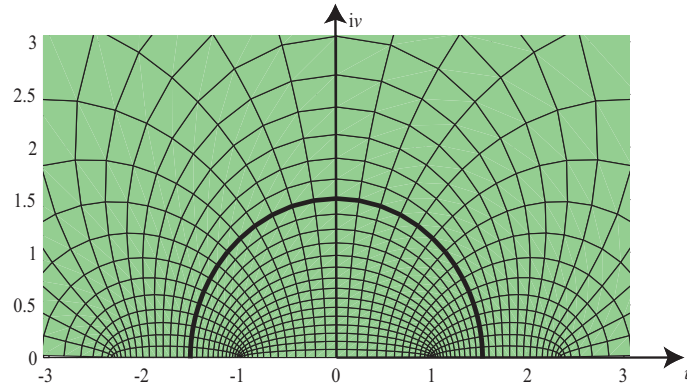


Figure 3.3: The orthonormal grid in Z -space transformed into W -space. Note the semi-circle at $u^2 + v^2 = 1/k$, which represents the line for $y = H/2$. In this plot $k = 0.4278$.

Chapter 4

DG MOSFET electrostatics

In order to calculate currents and capacitances in the double-gate MOSFET, we have to model the device electrostatics. Fields and potentials have to satisfy Poisson's equation (2.1) to a certain precision.

Solutions of Poisson's equation may be separated into several regimes, where it is possible to isolate certain dominating phenomena and disregard unnecessary complexity in finding possible solutions. Here, these regimes are chosen to be called:

- Sub-threshold
- Near threshold
- Strong inversion

The regime definitions clearly depend on the threshold value, and in this report, the threshold voltage is defined to be the gate-source voltage bias where the vertical field at the gate changes sign at the gate-to-gate symmetry axis (for zero drain bias). There have been several attempts to define a universal threshold voltage for this type of device. Among these are the traditional gate bias for where the body band bending equals $2\phi_b$, a gate bias where the drain current versus V_{gs} has maximum curvature, and the present definition.⁵³

In undoped/lightly doped devices, the mobile carrier density that is required to turn on the transistor far exceeds the channel doping concentration, and the $2\phi_b$ surface potential definition no longer serves as an indicator of the turn-on condition.

A problem with the proposed threshold voltage is that the value increases as the drain voltage increases, thereby losing its conventional meaning as a method to capture short-channel (DIBL) effects. However, in the modeling proposed later

in this thesis, the short-channel effects are captured by other modeled relations, related to the 2D effects.

For the threshold voltage, the sign change discussed above indicates that the electrostatics in the body is becoming dominated by charge carriers rather than by capacitive effects described by Laplace's equation(2.32).

4.1 Device structure

In this work, a simplified model device template has been developed based on a more physical device template described in Appendix B.

We consider a double-gate MOSFET which has a channel length of $L = 25$ nm, a nitrated oxide that is $t_{ox} = 1.6$ nm thick, and a body of lightly doped silicon that is $t_{Si} = 12$ nm high. Nitrated oxide and silicon have permittivities of $\epsilon_{ox} = 7$ and $\epsilon_{Si} = 11.8$, respectively. The source/drain contact surfaces are defined to be sharp boundaries where on the body side we have an acceptor concentration of $N_S = 10^{15}cm^{-3}$ and, on the contact side a Schottky metal with work function 4.17 eV, corresponding to that of n^+ silicon. We choose metal contacts to obtain an equipotential surface, no depletion region and negligible series resistance in the contacts. The built-in voltage is found with

$$V_{bi} = E_g/2q + \phi_b + \frac{k_B T}{2q} \ln \frac{N_C}{N_V} \quad (4.1)$$

where $\phi_b = V_{th} \ln(N_S/n_i)$ is the potential difference between the Fermi level of the intrinsic silicon and the doped p-type silicon, and E_g is the silicon band gap. The last term is a small shift of approximately $V_{th}/2$, which emerges from the difference in electron density states between the conduction and the valence band. N_C and N_V are the effective densities of states defined as

$$N_C = 2 \left(\frac{m_n k_B T}{2\pi \hbar^2} \right)^{3/2}, \quad N_V = 2 \left(\frac{m_p k_B T}{2\pi \hbar^2} \right)^{3/2} \quad (4.2)$$

The work function difference between gate metal and the silicon body gives rise to the flat-band voltage

$$V_{FB} = (\varphi_m - (\chi + E_g/2 + q\phi_b)) / q \quad (4.3)$$

where φ_m is the gate metal work function, and χ is the electronic affinity for silicon.

In this thesis, we have assumed a midgap gate metal with work function $\varphi_m = 4.53V$ (which corresponds to that of molybdenum).

4.2 Sub-threshold

For sub-threshold conditions, we assume that the body is dominated by the solution of the 2D Laplace electrostatics. The assumption is based on the fact that the field strength at the gates emerging from the mobile charge carriers are much weaker than the fields related to the capacitive coupling between the contacts and the gates. Therefore, we neglect the body charge term in Poisson's equation, converting it to a Laplace equation. This assumption has been verified by numerical simulations for the device considered.

4.2.1 Extended device body

Another assumption is that the oxide thickness is relatively small (compared to the body thickness and length). In that case, we may replace the oxide layers by dielectrically equivalent layers of undoped silicon for the purpose of modeling the device electrostatics. This is possible since the electrical field is perpendicular to the gates and therefore also predominantly so in the oxide. Hence, the extended

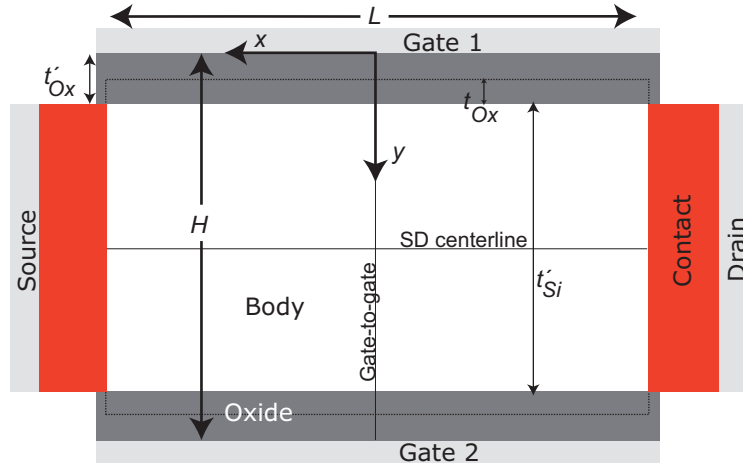


Figure 4.1: The double-gate MOSFET extended body, illustrating the increased effective thickness of the silicon body, including the transformed oxide thickness t_{ox} to an equivalent silicon field displacement thickness t'_{ox} .

silicon body will have an effective thickness of $H = t_{Si} + 2t'_{ox}$ where $t'_{ox} = t_{ox}\epsilon_{Si}/\epsilon_{ox}$ as indicated in Figure 4.1.

The rectangular extended body may now be mapped onto the complex plane using conformal mapping described in chapter 3, with the transformation in (3.9).

We are then ready to solve Laplace's equation in the transformed W -plane.

4.2.2 Boundary conditions

To obtain the potential distribution in W -space, we consider the contact boundaries to be equipotential at

$$\begin{aligned}\phi_{gs1} &= V_{gs1} - V_{\text{FB}} \\ \phi_{gs2} &= V_{gs2} - V_{\text{FB}}\end{aligned}\tag{4.4}$$

for the two gates, and

$$V_{bi}, V_{bi} + V_{ds}\tag{4.5}$$

for the source and drain, respectively. These values are mapped to the boundary in the W -plane as illustrated in Figure 3.1.

4.2.3 Oxide gaps

Considering the extended body, we find that the boundary is piecewise equipotential except at the oxide gaps, where we have a near-linear potential variation between the gates and the source and drain as shown by numerical simulations^a. For simplicity, the transitions can be modeled by creating a number of different equipotential pieces across the gaps. If we choose to use only two pieces, we may select a point inside the gap to which we extend the adjoining contact potentials. Alternatively, the whole gap can be set to the middle potential between these electrodes. The potential distribution in the body depends slightly on the approach used. However, the oxide gaps are small and relatively insignificant compared to the size of the contacts, and good agreement with numerical simulations is found when choosing any of these approaches.

For simplicity, in deriving expressions for the body potential, the contributions from the oxide gaps are assumed to be negligible. However, in all the model calculations, we have implemented a correction to account for the oxide gaps. This is done by extending adjoining the electrodes to a position located on the boundary $7/8t_{ox}$ from the gates. This is found to give an accuracy in the mV range for the potential at the body center.

^aThe precise potential variation can be obtained by using another, suitable conformal mapping procedure, involving only one isolated source or drain corner and the neighboring gate electrode.⁵¹

4.2.4 Body potential distribution

A solution of the Laplacian in the W -plane that describes the body potential, is given by the following integral along the u -axis:⁵¹

$$\phi(u, v) = \frac{v}{\pi} \int_{-\infty}^{+\infty} \frac{\phi(u')}{(u - u')^2 + v^2} du' \quad (4.6)$$

where $\phi(u)$ is the boundary conditions from (4.4)-(4.5) mapped to the u -axis. It may be solved for

$$u \in \langle -\infty, \infty \rangle, v \in [0, \infty)$$

resulting for general asymmetric biasing in¹⁸

$$\begin{aligned} \phi(u, v) = \frac{1}{\pi} \left\{ (V_{gs2} - V_{FB}) \left[\pi - \tan^{-1} \left(\frac{1 - ku}{kv} \right) - \tan^{-1} \left(\frac{1 + ku}{kv} \right) \right] \right. \\ + (V_{gs1} - V_{FB}) \left[\tan^{-1} \left(\frac{1 - u}{v} \right) + \tan^{-1} \left(\frac{1 + u}{v} \right) \right] \\ + V_{bi} \left[\tan^{-1} \left(\frac{1 - ku}{kv} \right) - \tan^{-1} \left(\frac{1 - u}{v} \right) \right] \\ \left. + (V_{bi} + V_{ds}) \left[\tan^{-1} \left(\frac{1 + ku}{kv} \right) - \tan^{-1} \left(\frac{1 + u}{v} \right) \right] \right\} \quad (4.7) \end{aligned}$$

The various terms in (4.7) may be reorganized to reflect the effects of the potential drops across the four oxide gaps, giving for the case of symmetric gate biasing ($V_{gs1} = V_{gs2}$)

$$\begin{aligned} \phi(u, v) = \frac{1}{\pi} \left\{ \pi (V_{gs} - V_{FB}) + (V_{bi} + V_{FB} - V_{gs}) \tan^{-1} \left(\frac{1 - ku}{kv} \right) \right. \\ + (V_{bi} + V_{ds} + V_{FB} - V_{gs}) \tan^{-1} \left(\frac{1 + ku}{kv} \right) \\ - (V_{bi} + V_{FB} - V_{gs}) \tan^{-1} \left(\frac{1 - u}{v} \right) \\ \left. - (V_{bi} + V_{ds} + V_{FB} - V_{gs}) \tan^{-1} \left(\frac{1 + u}{v} \right) \right\} \quad (4.8) \end{aligned}$$

It is also possible to find solutions for the symmetry-lines of the Z -plane (see Figure 4.1), in terms of the standard form of the elliptic integral (3.10), and the transformations (3.16)-(3.17).

Solving for $u = 0$ gives the potential distribution along the v -axis, corresponding to the gate-to-gate symmetry line in the Z -plane.⁴³

$$\begin{aligned}
 \phi_{GG}(v) = \frac{v}{\pi} \int_{-\infty}^{\infty} \frac{\phi(u')}{u'^2 + v^2} du' = \frac{1}{\pi} \left\{ 2(V_{gs} - V_{FB}) \tan^{-1} \left(\frac{1}{v} \right) \right. \\
 + (V_{gs} - V_{FB}) \left[\pi - 2 \tan^{-1} \left(\frac{1}{kv} \right) \right] \\
 \left. - (2V_{bi} + V_{ds}) \left[\tan^{-1} \left(\frac{1}{kv} \right) - \tan^{-1} \left(\frac{1}{v} \right) \right] \right\} \quad (4.9)
 \end{aligned}$$

For zero drain bias, (4.9) simplifies to

$$\phi_{GG} = V_{gs} - V_{FB} + \frac{2}{\pi} \left[\tan^{-1} \left(\frac{1}{kv} \right) - \tan^{-1} \left(\frac{1}{v} \right) \right] (V_{bi} - V_{gs} + V_{FB}) \quad (4.10)$$

In this case, the electrical field is zero at the device center ($x = 0, y = H/2$). Taking $d\phi_{GG}/dv = 0$, the center point is found to correspond to $v = 1/\sqrt{k}$ in accordance with (3.17). In chapter 3 we found that the source-to-drain center line corresponds to a circle of radius $1/\sqrt{k}$ in W -space. Hence, the relationship is $v = \sqrt{1/k - u^2}$ for this symmetry line in the W -plane. Substituting this into (4.8) results in the following expression for the potential distribution along the source-to-drain symmetry line

$$\begin{aligned}
 \phi(u)|_{v=1/\sqrt{k}} = \frac{1}{\pi} \left\{ \pi (V_{gs} - V_{FB}) - (V_{gs} - V_{FB} - V_{bi}) \tan^{-1} \left((1 - ku) / \left(k \sqrt{\frac{1}{k} - u^2} \right) \right) \right. \\
 - (V_{gs} - V_{FB} - V_{bi} - V_{ds}) \tan^{-1} \left((1 + ku) / \left(k \sqrt{\frac{1}{k} - u^2} \right) \right) \\
 + (V_{gs} - V_{FB} - V_{bi}) \tan^{-1} \left((1 - u) / \left(\sqrt{\frac{1}{k} - u^2} \right) \right) \\
 \left. + (V_{gs} - V_{FB} - V_{bi} - V_{ds}) \tan^{-1} \left((1 + u) / \left(\sqrt{\frac{1}{k} - u^2} \right) \right) \right\} \quad (4.11)
 \end{aligned}$$

4.2.5 Self-consistency at contacts

Near the source and drain contacts, the potential is relatively large, allowing a significant amount of electrons to accumulate, depending on the bias condition.⁵ It is necessary, to consider this electrostatic effect even under subthreshold conditions. In subthreshold this effect is included simply by adjusting the

boundary conditions at source and drain. Near and above threshold, the full body charge has to be considered.

Applying a 1D Poisson's equation to the regions and considering a linear approximation for the potentials, the surface field E_S near the source can be written as

$$E_S = E_{S1} + E_{S2} \approx \frac{qN_C}{\epsilon_{Si}} \int_0^\infty \exp\left(-\frac{E_S}{V_{th}}x\right) dx + E_{S2} = \frac{qN_C V_{th}}{\epsilon_{Si} E_S} + E_{S2} \quad (4.12)$$

where E_{S1} and E_{S2} are the electrical fields associated with the electrons and the capacitive coupling, respectively, and N_C is the electron concentration at the contact interface. Note that the above linearization is permitted only when E_S is sufficiently large, i.e. near-linear within a drop of a thermal potential (V_{th}) of $\phi(x)$ away from the source.

From 4.12, we obtain

$$E_S = \frac{E_{S2}}{2} \left[1 + \sqrt{1 + 2 \left(\frac{E_0}{E_{S2}} \right)} \right] \quad (4.13)$$

where $E_0 = \sqrt{2qN_C V_{th}/\epsilon_{Si}}$ is the approximate 1D electron charge contribution to the total field at one contact. This charge gives rise to a contribution to the interface potential, which can be obtained by integrating over the total electrical field (4.13). To lowest order, this contribution becomes

$$\Delta\phi_S \approx \frac{V_{th}}{2} \left(\frac{E_0}{E_S} \right)^2 \quad (4.14)$$

We obtain the electrical field at the contacts by differentiating (4.11) and applying the transformation in (3.17)

$$E_{S2} = -2\sqrt{1 - \frac{4k}{(k+1)^2}} \text{K}\left(\frac{4k}{(k+1)^2}\right) / ((k-1)L\pi) \times \left\{ V_{ds} + \sqrt{k} \left[-4V_C + (\sqrt{k} - 2) V_{ds} + 4(V_{gs} - V_{FB}) \right] \right\} \quad (4.15)$$

where $V_C = V_{bi} - \Delta\phi_S$ is the new modified contact potential for the capacitive solution.

In the case of the drain contact, we replace E_{S2} by E_{D2} , E_S by E_D , $\Delta\phi_S$ by $\Delta\phi_D$ and set the new 2D drain boundary condition to $V_C = V_{bi} + V_{ds} - \Delta\phi_D$.

4.2.6 Model simulations

The equations derived above have been applied to the physical structure described in Section 4.1, and some results are shown in this section.

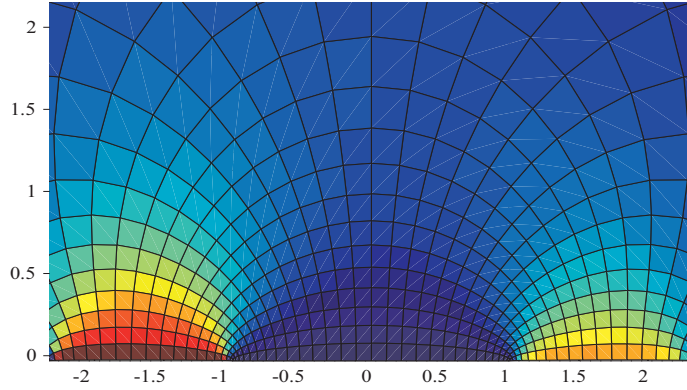


Figure 4.2: Device potential distribution in the transformed W -plane for a rectangular grid in Z -plane. The drain contact is biased at $V_{ds} = 0.1$, and molybdenum gates at $V_{gs} = 0V$.

The body potential topography, calculated from (4.6)-(4.8) for $V_{ds} = 0.1$, is shown in Figure 4.2. The calculation is performed for a rectangular grid in Z -space transformed to W -plane as shown in Figure 3.3. Then this potential distribution in the W -plane is mapped back to the Z -plane resulting in Figure 4.3.

The corresponding Z -plane distribution for $V_{ds} = 0$ is shown in Figure 4.4. The potential distribution in the present device always retains a non-negligible curvature in the x -direction, as opposed to the long-channel case. This curvature can be expressed as follows for the device center (symmetric gate bias)

$$\frac{d^2\phi}{dx^2} = \frac{8(1-k)}{\sqrt{1/k}(1+k)^2 L^2\pi} (2V_{bi} + V_{ds} - 2V_{gs} + 2V_{FB}) \left[\text{K} \left(\frac{4k}{(1+k)^2} \right) \right]^2 \quad (4.16)$$

Adjusting the drain bias affects the entire potential profile. Thus, the energy barrier over which an electron at the source has to climb decreases with increasing V_{ds} . This is known as the drain-induced barrier lowering (DIBL), an important short-channel effect.

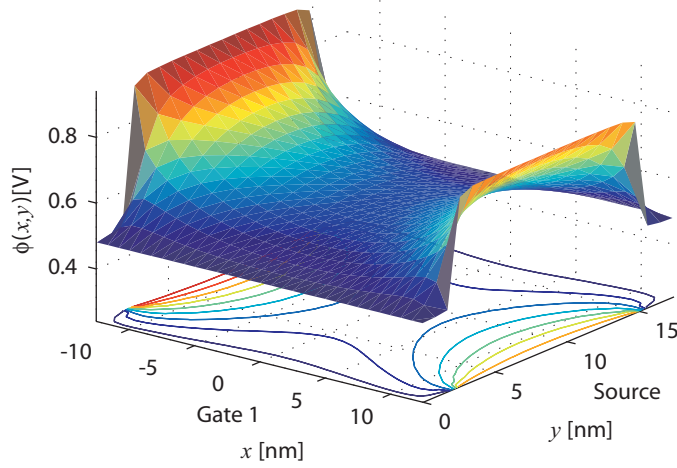


Figure 4.3: The potential distribution in the Z -plane for drain biasing of $V_{ds} = 0.1V$ and symmetrical gates at $V_{gs} = 0V$.

An illustration of the potential distribution along the two symmetry axes is shown in Figure 4.5. The modeling is compared with numerical simulations, revealing an excellent agreement. For the lower line, illustrating the gate-to-gate potential, we note that the highest potential is located in the device center. This means that for subthreshold, symmetric conditions, the main current path will be along the source-to-drain symmetry axis. Knowing that the electron concentration changes exponentially with the potential, the modeling of the potential distribution in the lateral (x) direction is of crucial importance for calculating the drain current.

Comparing Figures 4.3 and 4.4, we notice that the minimum potential position shifts toward the source with increasing V_{ds} . For conditions where all the assumptions above hold, the important short-channel effects in sub-threshold are found from the potential distribution in (4.11). We note that no adjustable parameters are needed in the present model to accurately estimate the DIBL effect in the DG MOSFET.

4.2.7 Modeling of DIBL

The analytical source-to-drain expression enables us to investigate the DIBL-effect more carefully. Differentiating (4.11) with respect to u , we obtain the

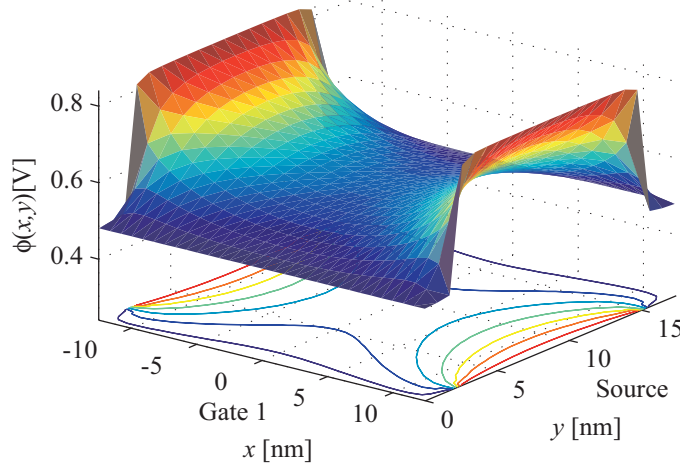


Figure 4.4: The potential distribution in the Z -plane for zero drain bias and symmetrical gates at $V_{gs} = 0V$.

V_{ds} -dependent position u_m of the potential minimum along the SD-symmetry line from

$$\frac{d\phi}{du} = \frac{(1-k)(V_{ds} - k[2u(2V_{bi} + V_{ds} - 2V_{gs} + 2V_{FB}) - V_{ds}])}{\pi\sqrt{\frac{1}{k} - u^2(4k^2u^2 - (1+k)^2)}} = 0 \quad (4.17)$$

resulting in

$$u_m = \frac{(1+k)V_{ds}}{2k(2V_{bi} + V_{ds} - 2V_{gs} + 2V_{FB})} \quad (4.18)$$

Evaluating (4.11) at $u = u_m$ gives the minimum source-to-drain potential (the maximum source-to-drain barrier). The corresponding x -value is found with the mapping equation (3.17).

Figure 4.6 illustrates the barrier shift in both potential minimum and its location along the source-drain symmetry line. Correspondingly, gate-to-gate potential distributions at the minima are shown in Figure 4.7. The model calculations are compared and verified against numerical simulations.

Figures 4.8 and 4.9 show the DIBL-effect in terms of location of the potential minimum and its shift along the source-to-drain symmetry line versus V_{ds} . For

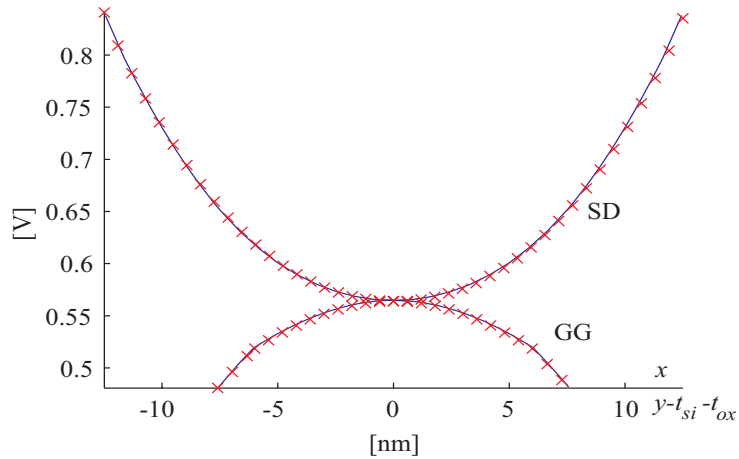


Figure 4.5: Potential distributions along the source-to-drain (SD) and gate-to-gate (GG) symmetry lines for zero drain and gate bias in subthreshold conditions. The modeling is shown with solid lines and the crosses indicates a corresponding numerical simulation of the device.

the device specified in Section 4.1, we have calculated the potential minimum and its location as a function of the device length $12.5nm \leq L \leq 50nm$.

For the shortest device length, the barrier lowering is so large that the effects of the charge carriers on the electrostatics becomes important throughout the body. This effect is not included in the modeling in Figures 4.8 and 4.9 giving rise to a deviation from the numerical simulations. The full effect of body charge is discussed in Section 4.3.

For larger device lengths, the model shows good agreement with numerical simulations.

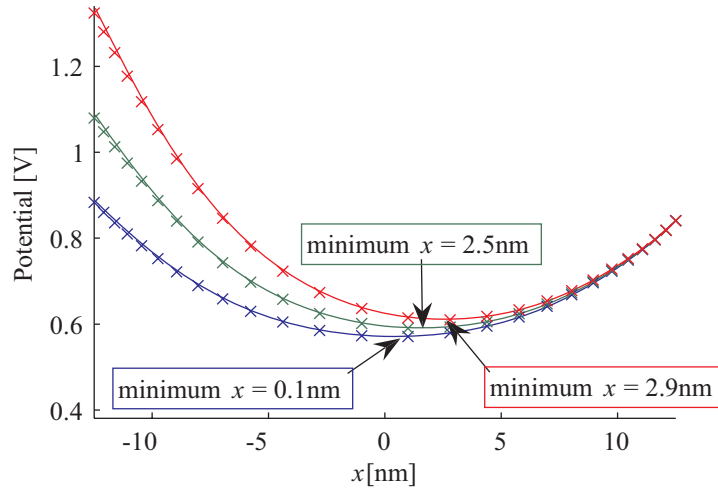


Figure 4.6: Drain-source barrier for $V_{ds} = \{0.05, 0.25, 0.5\}V$, indicating DIBL-effect in subthreshold. Solid lines indicate the modeling and crosses indicate corresponding numerical simulations.

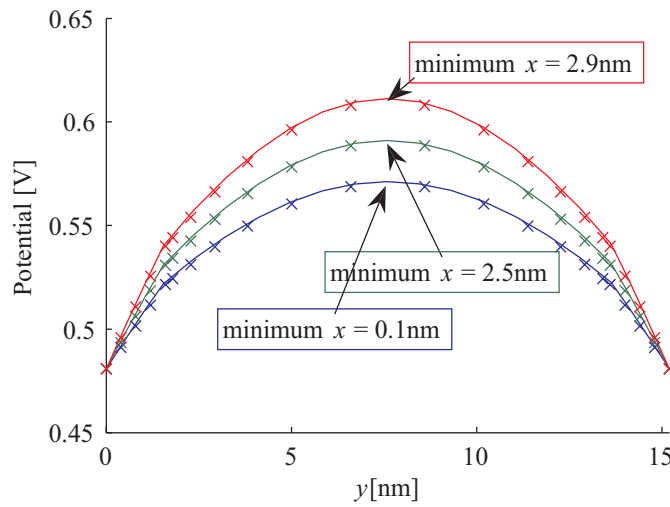


Figure 4.7: Gate-gate potential at the source-drain minimum for $V_{ds} = \{0.05, 0.25, 0.5\}V$, and $V_{gs} = 0V$ in subthreshold. The modeling is shown with solid lines and the crosses indicates the numerical simulations.

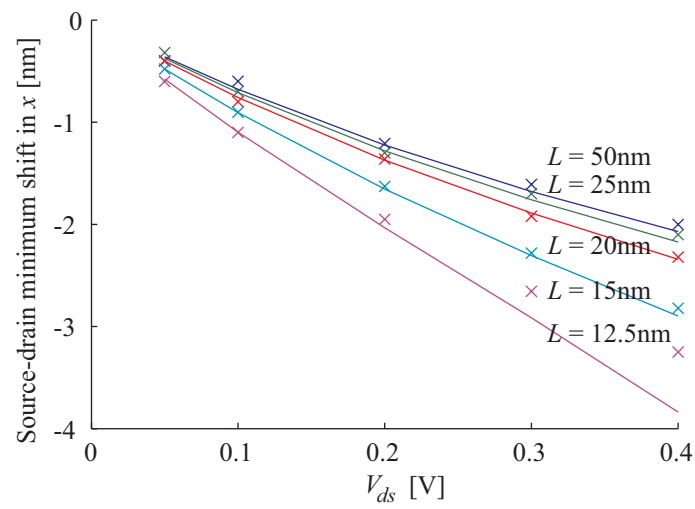


Figure 4.8: Shift of source-drain barrier location versus V_{ds} for device lengths $L = \{50, 25, 20, 15, 12.5\}$ nm. The silicon and oxide thicknesses are held constant. The gates are biased at $V_{gs} = 0$ which corresponds to subthreshold conditions. The modeling results are shown as solid lines, while numerical simulations are indicated with crosses.

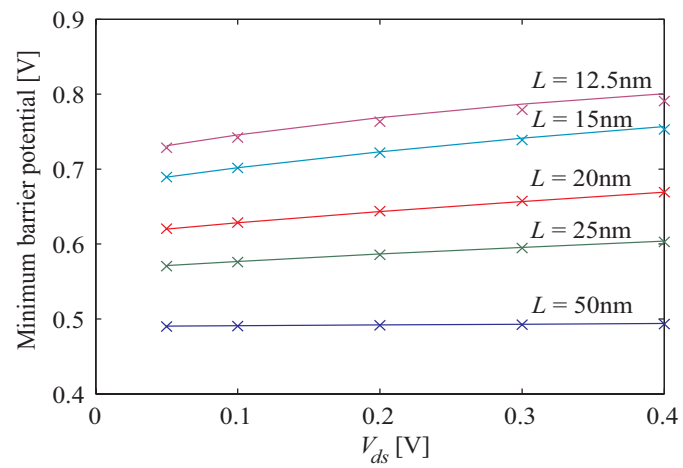


Figure 4.9: The drain influence on the minimum potential along the source-drain symmetry line for device lengths $L = \{50, 25, 20, 15, 12.5\}$ nm. The silicon and oxide thicknesses are held constant. The gates are biased at $V_{gs} = 0V$ which corresponds to subthreshold conditions. The modeling results are shown as solid lines, while numerical simulations are indicated with crosses.

4.2.8 Asymmetric gate biasing

Applying a different bias on the two gates, or equivalently, using different gate materials at the two gates, strongly affects the potential distribution in the body.⁵⁴ When utilizing the properties of the gate material specified in Section 4.1 at gate 1 and p^+ polysilicon at gate 2, we find that the barrier is shifted from the source-to-drain symmetry line towards gate 1, establishing an inversion channel at that silicon/oxide interface for $V_{gs} = 0$. The modeling of the sub-threshold electrostatics is shown in Figure 4.10. A numerical simulation of the potential distribution, shown in Figure 4.11, also indicates the inversion channel close to gate 1.

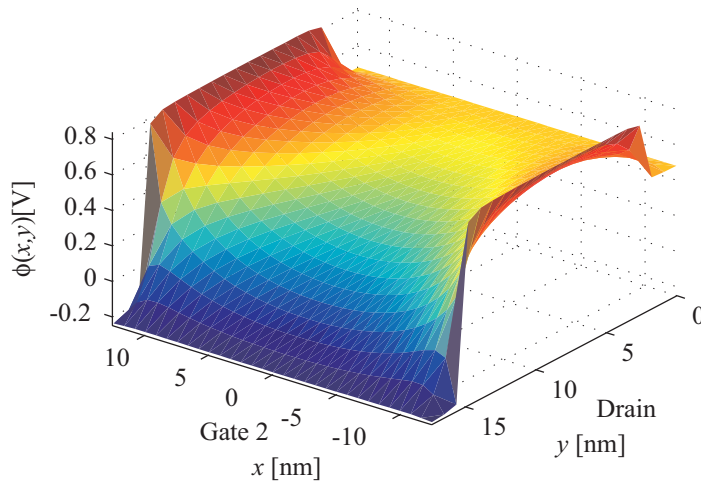


Figure 4.10: Asymmetric operation of device with molybdenum and p^+ polysilicon gate materials at gate 1 and gate 2 respectively. Inversion carriers are shifted to the gate 1 interface. Shown for $V_{ds} = V_{gs} = 0V$.

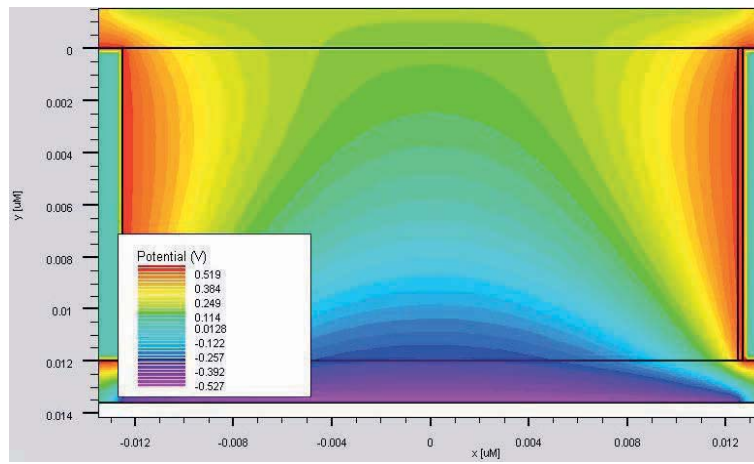


Figure 4.11: Numerical simulation of asymmetric operation of device with molybdenum and p^+ polysilicon gate materials at gate 1 and gate 2 respectively. Inversion carriers are shifted to the gate 1 interface. Shown for $V_{ds} = V_{gs} = 0V$. The potential reference is the source contact Fermi level.

4.3 Near threshold

When higher gate biases are applied, the device moves into the *near threshold* regime. This is the regime where the electronic and capacitive electrostatic contributions are comparable. Increasing the gate-source bias, the body charge will eventually dominate the body electrostatics. The subthreshold to near threshold transition is illustrated in Figure 4.12. Here, subthreshold modeling is compared with numerical simulations for the potential at the device center versus V_{gs} for zero drain bias. We note that the subthreshold Laplace solution becomes

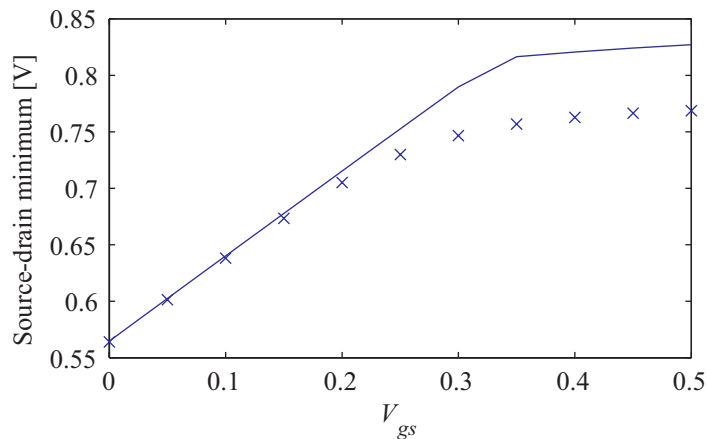


Figure 4.12: Center potential calculated from the Laplace subthreshold model shown with solid lines and the numerical simulations of Poisson's equation are indicated with crosses, versus V_{gs} for $V_{ds} = 0V$.

increasingly erroneous as the gate bias approaches threshold. According to the subthreshold equation (4.10), for $V_{ds} = 0$, the threshold condition (flat gate-to-gate potential distribution) is met when $V_{gs} = V_{bi} + V_{FB} \approx 0.36V$ (symmetric gates). However, the numerical simulation indicates that threshold occurs at $V_{gs} \approx 0.25$, indicating the strong influence of the inversion charge. Therefore, a self-consistent treatment that takes into account both the mobile charge and the capacitive coupling has to be introduced for this regime. To this end, we consider the self-consistent potential distributions along the two symmetry axis. Suitable modeling expressions are applied, whose parameters are determined from the boundary conditions and by enforcing consistency using Poisson's equation.

4.3.1 Superposition

To solve Poisson's equation with both mobile carriers and the 2D capacitive coupling, we propose a superposition modeling approach when

$$\phi(x, y) = \phi_1(x, y) + \phi_2(x, y) \quad (4.19)$$

where $\phi_1(x, y)$ is the potential contribution related to the inversion charge, and $\phi_2(x, y)$ is the contribution related to the capacitive coupling.

4.3.2 Approximations used

In order to solve Poisson's equation with the proposed superposition, we assume that the lateral term $d^2\phi/dx^2$ is relatively small near the device center. This assumption is based on the characteristic parameter for electrostatic influence of source and drain into the device body.³³

$$\lambda = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} \left(1 + \frac{\epsilon_{ox}t_{Si}}{4\epsilon_{Si}t_{ox}} \right) t_{Si}t_{ox}} \quad (4.20)$$

If $\lambda < L/2$, the assumption above will be reasonable in the interval $-L/2 + \lambda < x < L/2 - \lambda$. We notice that this condition also holds for a wider range when sufficiently close to the gates. For the device considered here, we have $\lambda \approx L/4$.

Near source and drain, $d^2\phi/dy^2 \approx 0$, a condition that was already exploited in Section 4.2.5.

In order to find the transversal y -dependent potential contribution related to the mobile carriers at the gate-to-gate symmetry line, we use a 1D application of Gauss' law.

4.3.3 Self-consistency

A range of self-consistent procedures are developed to take care of the inter-dependent super-positioned solutions. From (4.12)-(4.14), we obtain the lateral solution $\phi_1(x, H/2)$ related to the charge carriers near source and drain as well as modified boundary conditions for the capacitive coupling. Note that in the following self-consistent analysis, the proper boundary conditions of the source and drain are used, without the correction of (4.14).

Threshold voltage

Assuming zero drain-source bias, we know that the source-drain potential minimum is in the middle of the device. We then consider the electron density

and its distribution at the gate-to-gate symmetry line by classical Boltzmann statistics

$$n_s(y) = \frac{n_i^2}{N_S} \exp\left(\frac{\phi(y)}{V_{th}}\right) \quad (4.21)$$

A special case is the threshold condition ($V_{gs} = V_T$), which we define as the V_{gs} where the total potential $\phi(y)$ is approximately constant and close to $V_T - V_{FB}$ on the gate-to-gate symmetry axis. In this case the electrostatic effects of the capacitive coupling and the free electrons are equal and opposite at this axis. Some minor fluctuations in $\phi(y)$ is observed, owing to the small difference in the potential distributions between that related to the capacitive coupling and that of the inversion charge part, but this effect can be ignored.

Hence we can use the following condition,

$$\phi(y) \approx \phi(H/2) = V_T - V_{FB} \quad (4.22)$$

together with (4.21) in Poisson's equation. Further, imposing the the condition $d^2\phi/dx^2 = 0$, the resulting one dimensional Poisson's equation becomes:

$$\frac{d^2\phi_1}{dy^2} = \frac{qn_i^2}{\epsilon_{Si}N_S} \exp\left(\frac{V_T - V_{FB}}{V_{th}}\right) \quad (4.23)$$

Using this uniform electron concentration distribution, we can easily integrate (4.23) to obtain

$$\begin{aligned} E_1(y) &= \frac{q}{\epsilon_s} \times \begin{cases} \int_{t'_{ox}}^{H/2} n_s dy & , y < t'_{ox} \\ \int_{t'_{ox}}^{H/2} n_s dy & , t'_{ox} \leq y \leq H/2 \end{cases} \quad (4.24) \\ &= \frac{qn_i^2}{\epsilon_{Si}N_S} \exp\left(\frac{V_{gs} - V_{FB}}{V_{th}}\right) \begin{cases} (H/2 - t'_{ox}) & , y < t'_{ox} \\ (H/2 - t'_{ox}) & , t'_{ox} \leq y \leq H/2 \end{cases} \\ &= \frac{qn_i^2}{\epsilon_{Si}N_S} \exp\left(\frac{V_{gs} - V_{FB}}{V_{th}}\right) \times \begin{cases} (t_{Si}/2) & , y < t'_{ox} \\ (H/2 - y) & , t'_{ox} \leq y \leq H/2 \end{cases} \end{aligned}$$

and

$$\begin{aligned}\phi_1(y) &= - \int_0^y E_1(y) dy \\ &= \frac{qn_i^2}{\epsilon_{Si}N_S} \exp\left(\frac{V_{gs} - V_{FB}}{V_{th}}\right) \times \begin{cases} yt_{Si}/2 & , y < t'_{ox} \\ \frac{1}{2} (Hy - y^2 - t'_{ox}{}^2) & , t'_{ox} \leq y \leq H/2 \end{cases}\end{aligned}\quad (4.25)$$

We are now able to combine the solutions related to the inversion charge (4.25) and the capacitive coupling (4.10) in (4.19). In Figure 3.2 we found that the device middle $x = 0, y = H/2$ corresponds to $u = 0, v = 1/\sqrt{k}$ in the transformed space, which gives

$$\phi(0, H/2) = \phi_1(0, H/2) + \phi_{2GG}\left(1/\sqrt{k}\right) = V_T - V_{FB} \quad (4.26)$$

Substituting $\phi(0, H/2)$ from (4.25) and $\phi_{2GG}(y)$ from (4.10) into (4.26) results in the following self-consistent expression for the threshold voltage.

$$\begin{aligned}\frac{qn_i^2}{\epsilon_{Si}N_S} \frac{H^2}{8} \exp\left(\frac{V_T - V_{FB}}{V_{th}}\right) \left[1 - \left(\frac{2t'_{ox}}{H}\right)^2\right] &= \\ \left[\frac{4}{\pi} \tan^{-1}\left(\frac{1}{\sqrt{k}}\right) - 1\right] (V_{bi} - V_T + V_{FB}) &\end{aligned}\quad (4.27)$$

This can be rewritten in the form of the Lambert function ($we^w = c$) as

$$\begin{aligned}\frac{V_{bi} - V_T + V_{FB}}{V_{th}} \exp\left(\frac{V_{bi} - V_T + V_{FB}}{V_{th}}\right) &= \\ \frac{qn_i^2}{\epsilon_{Si}N_S} \frac{H^2}{8V_{th}} \frac{1 - \left(\frac{2t'_{ox}}{H}\right)^2}{\frac{4}{\pi} \tan^{-1}\left(\frac{1}{\sqrt{k}}\right) - 1} \exp\left(\frac{V_{bi}}{V_{th}}\right) &\end{aligned}\quad (4.28)$$

The threshold voltage obtained from this expression for the device described in Section 4.1 versus gate length is presented in Figure 4.13. We note that when holding the silicon thicknesses constant, the modeling gives excellent agreement with numerical simulations for gate lengths down to less than 15 nm. For shorter gate lengths, the assumption of $d^2\phi/dx^2 \ll d^2\phi/dy^2$ at the device center breaks down since the penetration depths from (4.20) gives $\lambda \geq L/2$. For the present device with $L = 25nm$, we find $V_T \approx 0.25$.

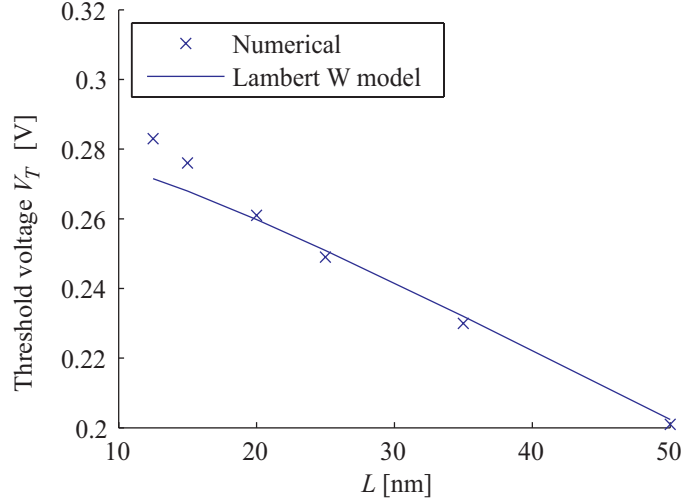


Figure 4.13: Threshold voltage dependence on gate length when holding silicon thickness constant. The modeling is for zero drain voltage, and numerical simulations are shown with crosses. This plot does not include the corrections associated with the oxide gaps discussed in Section 4.2.3.

Gate-to-gate profile

Near threshold, we make the assumption that the center gate-to-gate potential distribution $\phi(y)$ has a symmetric parabolic form, as verified by numerical simulations. With a potential $V_{gs} - V_{FB}$ at the gate and $\phi_m + V_{gs} - V_{FB}$ at the device center, we have

$$\phi(y) = V_{gs} - V_{FB} + \phi_m \left[1 - \left(1 - \frac{2y}{H} \right)^2 \right] \quad (4.29)$$

In this case, the 1D-Poisson's equation for the contribution of the electronic charge to the potential has the form

$$\frac{d^2 \phi_1}{dy^2} = \frac{qn_i^2}{\epsilon_{Si} N_S} \exp \left(\frac{\phi_1(y) + \phi_2(y)}{V_{th}} \right) \quad (4.30)$$

Integration of this expression leads to a self-consistent expression for $\phi_1(y)$. Applying the condition $\phi_1(H/2) + \phi_2(H/2) = \phi(H/2)$, we obtain the following

implicit algebraic equation for ϕ_m versus V_{gs} ,

$$\begin{aligned} \phi_m = & \left[\frac{4}{\pi} \tan^{-1} \left(\frac{1}{\sqrt{k}} \right) - 1 \right] (V_{bi} - V_{gs} + V_{FB}) \\ & - \frac{qn_i^2 H^2}{8\epsilon_{Si} N_S} \exp \left(\frac{V_{gs} - V_{FB} + \phi_m}{V_{th}} \right) \times \\ & \left\{ \text{sgn}(\phi_m) \sqrt{\frac{\pi V_{th}}{\phi_m}} \text{erf} \left[\sqrt{\frac{\phi_m}{V_{th}}} \left(1 - \frac{2t'_{ox}}{H} \right) \right] + \right. \\ & \left. \frac{V_{th}}{\phi_m} \left[\exp \left(-\frac{\phi_m}{V_{th}} \left(1 - \frac{2t'_{ox}}{H} \right)^2 \right) - 1 \right] \right\} \end{aligned} \quad (4.31)$$

Here, 'erf' is the error function and 'sgn' returns the sign of its argument.

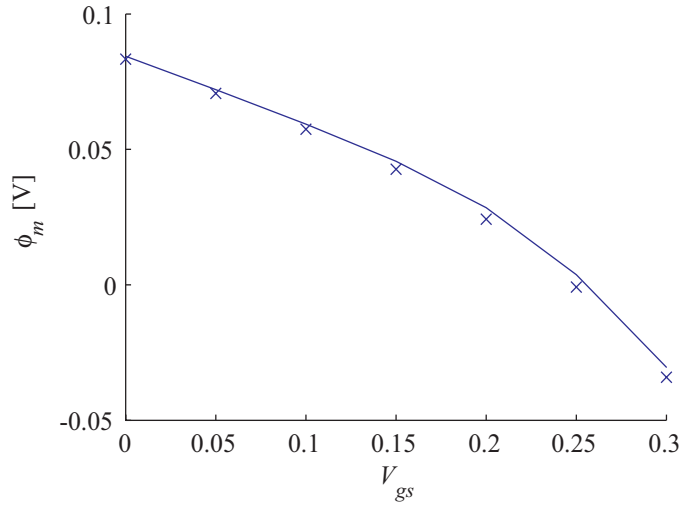


Figure 4.14: The parameter ϕ_m as a function of gate bias, compared with numerical calculations marked with crosses. At $\phi_m = 0$, the gate-to-gate distribution is flat. (Corrections for oxide gaps are included.)

Figure 4.14 shows a comparison of the potential ϕ_m versus applied V_{gs} for zero drain bias as calculated from (4.31), corrected for oxide gap effects. We observe an excellent agreement between the model and the numerical simulation within the range of V_{gs} considered. Note that slightly above threshold ($V_T \approx 0.25$ V for the 25 nm device), the assumption of a parabolic form of $\phi(y)$ tends to break down.

In the above discussion, we have only considered zero drain voltage. The effects of an applied drain voltage will be considered in the following sections.

Source-to-drain potential profile

Here we consider the potential distribution along the source-to-drain symmetry axis, where also the effects of drain bias are included. A drain bias causes a longitudinal variation in the quasi-Fermi potential, which affects the charge distribution. In subthreshold, the body charge concentration is relatively small and the potential distribution is mainly determined by the capacitive coupling (see (4.7)). However, near and above threshold where the influence of the charges is significant, we have to account for the drain-induced change in the charge distribution. This, in turn affects the potential distribution. To describe these inter-relationships, we have to consider the drain current and the quasi-Fermi potential distribution in the channel.

In this section, the quasi-Fermi potential in the device center point is assumed to be known, although its final value will be determined of an appropriate transport model.

Solving a self-consistent system consisting of Poisson's equation and a transport model implies an iterative solution scheme. To achieve the initial solution before calculating the current, we need to make a few qualified assumptions.

To find the initial central gate-to-gate solution from the 1D Poisson's equation, we assumed that the curvature in the x -direction was small, see previous sections. This was justified by the observation that the region between the penetration depths of the source and drain contacts is almost flat and thus the charges in this area have their main portion of mirror charge in the gate direction. We can then expect a relatively flat distribution of electrons in the x -direction, resulting in that $d^2\phi/dx^2 \ll d^2\phi/dy^2$.

In the previous section, we assumed a parabolic form of the total potential at the gate-to-gate symmetry line, which lead to an analytic, implicit expression for the center potential ϕ_m . However, here we instead make the parabolic assumption for the potential contribution $\phi_1(0, y)$, related to the charge, in order to facilitate the generalization of our analysis.

To find a boundary condition for the center point $\phi_1(0, H/2)$ in (4.19), we assume a parabolic shape of the gate-to-gate potential contribution related to the charge. Near threshold, this approximation has the same order of precision as that of (4.29).

$$\phi_1(0, y) = \phi_{1m} \left(1 - \left(1 - 2\frac{y}{H} \right)^2 \right) \quad (4.32)$$

The center potential ϕ_1 is referenced to the potential at the gate metal interface ($V_{gs} - V_{FB}$) of the extended body, with $\phi_1(0, 0) = 0$ and $\phi_1(0, H/2) = \phi_{1m}$, where we can find ϕ_{1m} from Poisson's equation. From (4.32), we find that

$$\frac{d^2\phi_1}{dy^2} = -\frac{8\phi_{1m}}{H^2} \quad (4.33)$$

Hence, for the device center, Poisson's equation can be written as

$$-\frac{8\phi_{1m}}{H^2} = \frac{q}{\epsilon_{Si}} \frac{n_i^2}{N_S} \exp((\phi_{1m} + \phi_2(0, H/2) - V_F)/V_{th}) - \frac{d^2\phi_1}{dx^2} \quad (4.34)$$

To obtain an initial approximation for ϕ_{1m} , we set $d^2\phi/dx^2$ equal to zero in the initial solution.

On the other hand, to find potential distributions arising from the electron populations near the source and drain contacts, we can use a 1D Poisson's equation. Integrating twice over these charges, we find solutions for $\phi_{1S}(x)$ and $\phi_{1D}(x)$ close to the contacts, which are improved compared to that of (4.12). We may also assume that the quasi-Fermi potential is constant close to the contacts.

Next, we locate the two points along source-to-drain symmetry axis where the charge-associated field lines change direction from mainly in the y -direction to mainly in the x -direction, $x = \{x_S, x_D\}$, on the source and drain side, respectively.

To obtain the full potential distribution along the source-to-drain symmetry line, we introduce a parametrized modeling expression $\hat{\phi}_1(x, H/2)$, where the parameters are determined by the five locations discussed above, i.e.,

- The contacts, $\hat{\phi}_1(\pm L/2, H/2) = 0$
- Change in field direction, $\hat{\phi}_1(x_{\{S/D\}}, H/2) = \{\phi_{1S}, \phi_{1D}\}$
- The center point, $\phi_1(0, H/2)$

The test function parameters are determined iteratively by initially guessing values of x_S and x_D . This initial solution gives first estimates for the potentials $\{\phi_{1S}, \phi_{1D}\}$. The iteration, which involves Poisson's equation, leads to an optimized set of values for x_S , x_D , $\hat{\phi}_1(x_{\{S/D\}}, H/2)$, and of the test function parameters.

The proposed modeling expression $\hat{\phi}_1(x, H/2)$ is as follows:

$$\hat{\phi}_1(x, H/2) = \quad (4.35)$$

$$P_p \left\{ \left(1 - \exp \left[\alpha \left(x - \frac{L}{2} \right) \right] \right) \left(1 + \left[x - \frac{L}{2} \right] / a \right)^{-n} \left(\frac{3}{4} + \frac{x}{L} - \frac{x^2}{L^2} \right) + \right.$$

$$\left. \left(1 - \exp \left[\beta \left(x + \frac{L}{2} \right) \right] \right) \left(1 + \left[x + \frac{L}{2} \right] / b \right)^{-n} \left(\frac{3}{4} - \frac{x}{L} - \frac{x^2}{L^2} \right) \right\}$$

The parameter P_p is directly given by the solution of Poisson's equation in the device middle. All of the parameters are obtained from the procedure indicated above.

After a few iterations, the source-to-drain potential distribution can be fed into the transport model expression (see chapter 5) to obtain an estimate for the current and the quasi-Fermi potential distribution. This, in turn, can be used to obtain a global self-consistent solution for drain current and the body electrostatics.

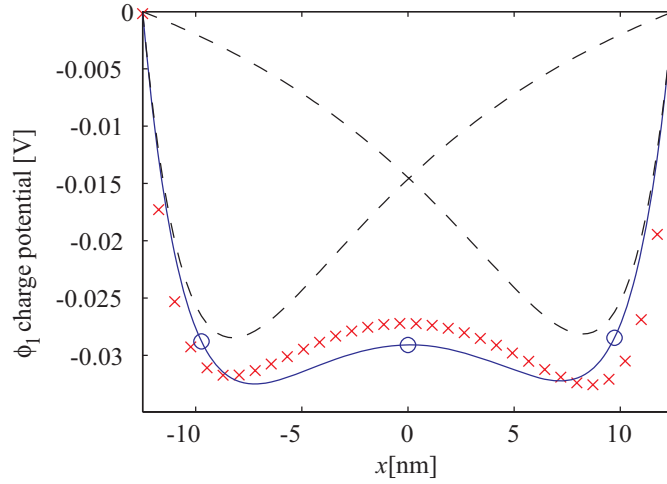


Figure 4.15: The potential along the drain-source symmetry line for threshold, $V_{ds} = 0V$ and $V_{gs} = 0.25V$. The proposed model expression is shown as a solid line, the dashed lines are the two terms of the model expression in (4.35). Numerical simulations are indicated with crosses. The boundary conditions are indicated with circles.

The modeling expression is shown for the symmetric case ($V_{ds} = 0$) in Figure 4.15. A good agreement with the numerical simulation is obtained, to within a

few millivolts.

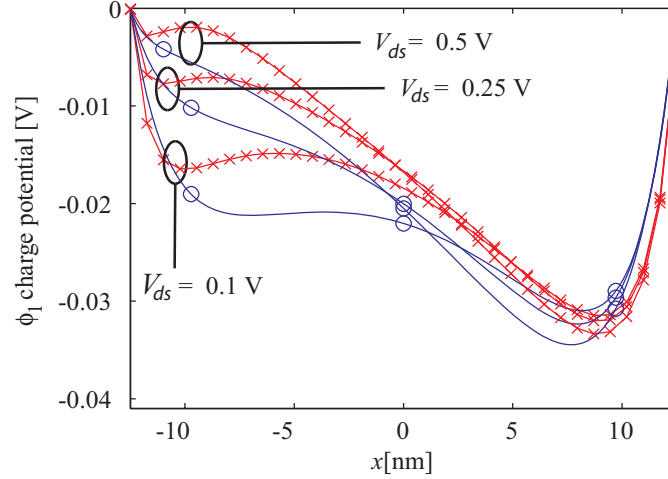


Figure 4.16: The charge potential contributions along the drain-source symmetry line for threshold $V_{gs} = 0.25V$, and $V_{ds} = \{0.1, 0.25, 0.5\}V$. The modeled potentials $\phi_1(x)$ are shown as solid lines and numerical simulations are indicated with crosses. The boundary conditions are indicated with circles.

Correspondingly, results for applied drain voltages are shown in 4.16. We again find a good agreement with the numerical simulation, especially in the important region close to the potential minimum near the source contact.

The gate-to-gate distribution of the inversion charge contribution to the potential is shown in Figure 4.17 for $V_{ds} = 0V$ and different gate voltages. The small deviation from the numerical simulations at the device center can be attributed to the following:

- The assumed, parabolic gate-to-gate model potential distribution $\phi_1(0, y)$.
- The approximate shape of the source-to-drain modeling expression $\phi_1(x, H/2)$ used, which affects our estimates $d^2\phi_1/dx^2$ and the quasi-Fermi potential at the device center.

The total potential $\phi(0, y) = \phi_1(0, y) + \phi_2(0, y)$ along the gate-to-gate symmetry line is shown in Figure 4.18 for the same biasing voltages as in Figure 4.17.

In Figure 4.19, the total potential distribution $\phi(x, H/2)$ along the source-to-drain symmetry axis is shown for $V_{gs} = 0.25V$ and different drain voltages. This figure illustrates the DIBL-effect associated with the drain bias.

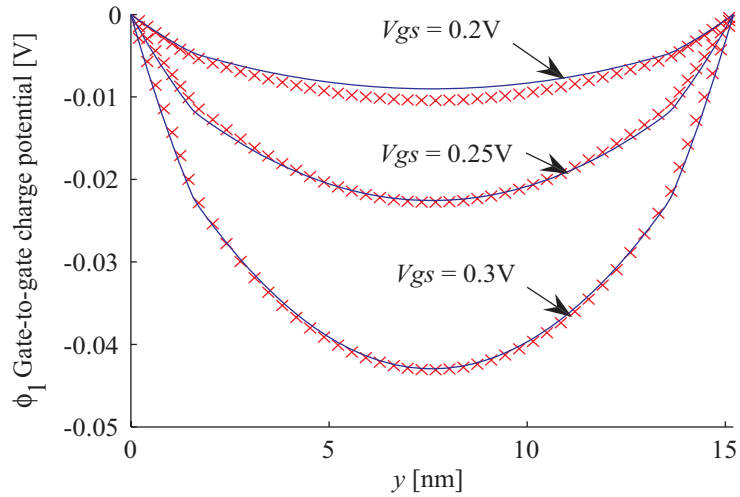


Figure 4.17: The potential contribution at the gate-to-gate symmetry line resulting from the body inversion charge for $V_{ds} = 0V$. Modeling is shown in solid and numerical simulations with crosses.

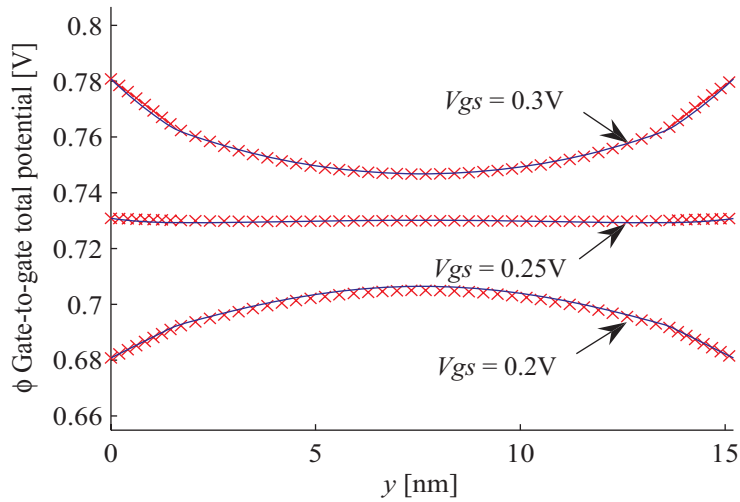


Figure 4.18: The total potential at the gate-to-gate symmetry line for $V_{ds} = 0V$. Modeling is shown in solid and numerical simulations with crosses.

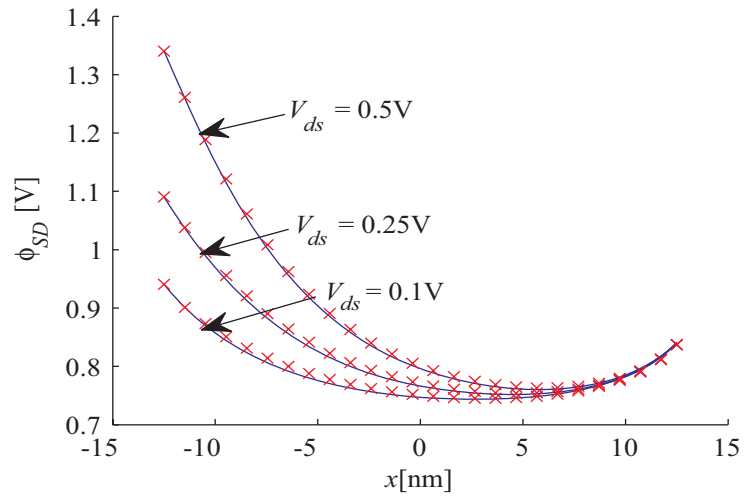


Figure 4.19: The total potential for threshold, $V_{gs} = 0.25V$ and $V_{ds} = \{0.1, 0.25, 0.5\}V$, on the drain-source symmetry line. Modeling is shown in solid and numerical simulations with crosses.

Figure 4.20 shows examples of the total source-to-drain potential distributions and quasi-Fermi potential distributions for different combinations of V_{gs} and V_{ds} .

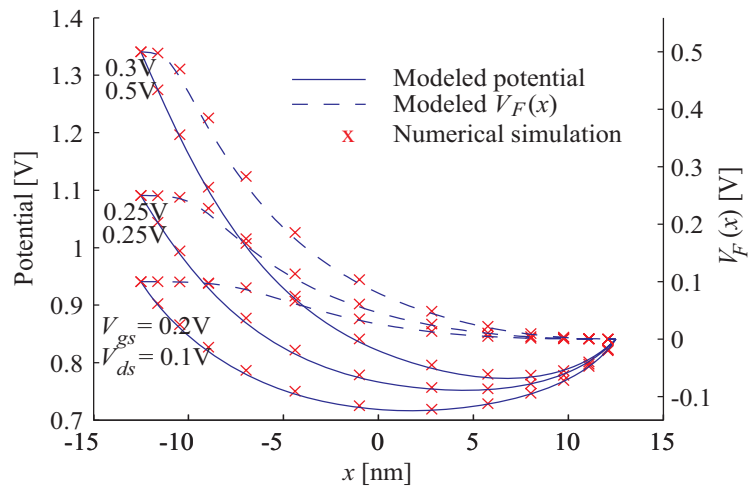


Figure 4.20: The potential and quasi-fermi potential at the drain-source symmetry line for the near threshold region $V_{gs} = \{0.2, 0.25, 0.3\}V$ and $V_{ds} = \{0.1, 0.25, 0.5\}V$. Modeling is shown in solid (potential) and dashed (quasi-Fermi potential), numerical simulations with crosses.

4.4 Strong inversion

4.4.1 Long channel approximation

Well into the strong inversion regime, the accumulation of electrons close to the gates has associated fields which are dominating the device electrostatics. Moreover, the inversion charge concentration will be so high that it effectively screens out the electrostatic influence from source and drain along most of the channel. This means that the device attains more of a long-channel behavior with increasing gate bias. Hence, well-defined channels develop along the silicon-insulator interfaces in strong inversion, where the flat section defines an effective channel length, which is close to the physical gate length. This is indicated in in the simulated potential contour plot in Figure 4.21.

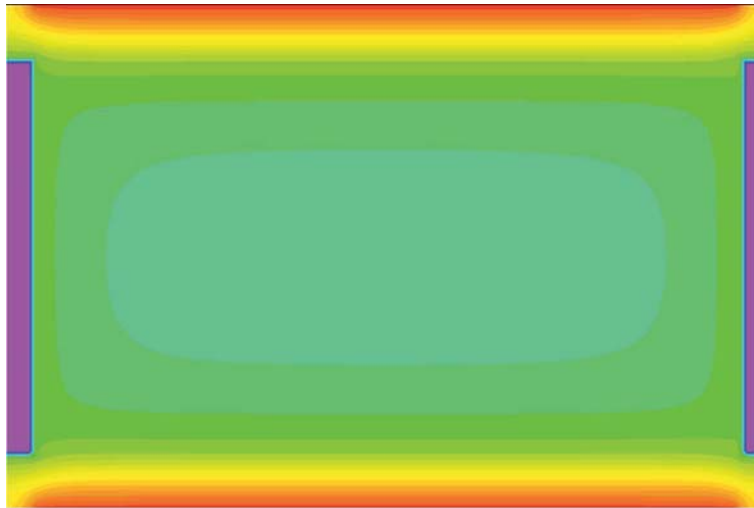


Figure 4.21: Potential contour plot showing strong inversion conditions for the double-gate device. The flat region close to the gates (red) indicates that long-channel modeling can be applied. (The source and drain contacts in purple.) $V_{ds} = 0V$

A long channel model of the device electrostatics for undoped double-gate MOSFETs was developed by Taur (see Section 2.1.1). The model consists of analytical solutions for the potential distribution and the current transport. This model is adopted for the strong inversion regime of the present device, by including the effects of doping on the the body Fermi potential. Hence, (2.5)

can simply be modified by including $\phi_b = V_{th} \log\left(\frac{N_s}{n_i}\right)$ as follows

$$\frac{\phi - \phi_0}{2V_{th}} = -\ln \left[\cos \left(\sqrt{\frac{qn_i}{2\epsilon_{Si}V_{th}}} \exp((\phi_0 - \phi_b)/V_{th})(y - (t_{Si} + 2t_{ox})/2) \right) \right] \quad (4.36)$$

combining this with (2.6) gives the gate-to-gate potential profiles shown in Figure 4.22 for $V_{ds} = 0V$. We observe from these results that the model accuracy improves with increasing gate bias. This is illustrated in Figure 4.23 by the decreasing difference between the modeled and simulated potentials on the gate-to-gate symmetry axis for the oxide/silicon interface and at the center.

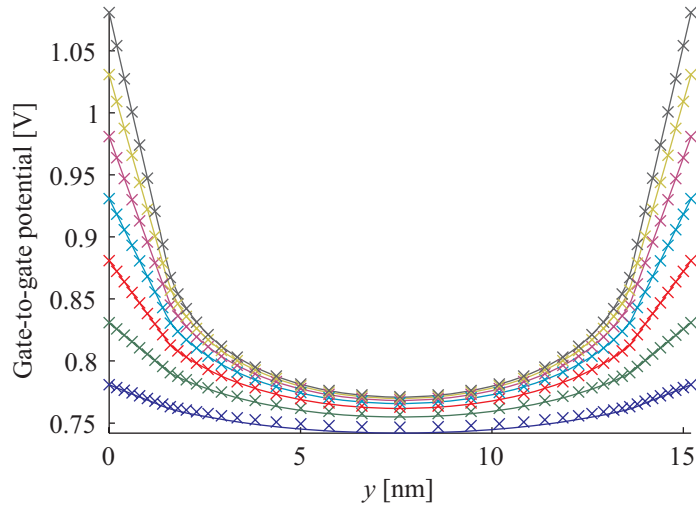


Figure 4.22: Strong inversion gate-to-gate potential distributions for $V_{gs} = \{0.3, 0.35, 0.4, 0.45, 0.5, 0.55, 0.6\}$, and with zero drain-source voltage. Modeling is shown in solids and numerical simulations are indicated with crosses.

In the presence of drain current, the self-consistent calculations of the device must involve the calculation of the current. See Chapter 5.

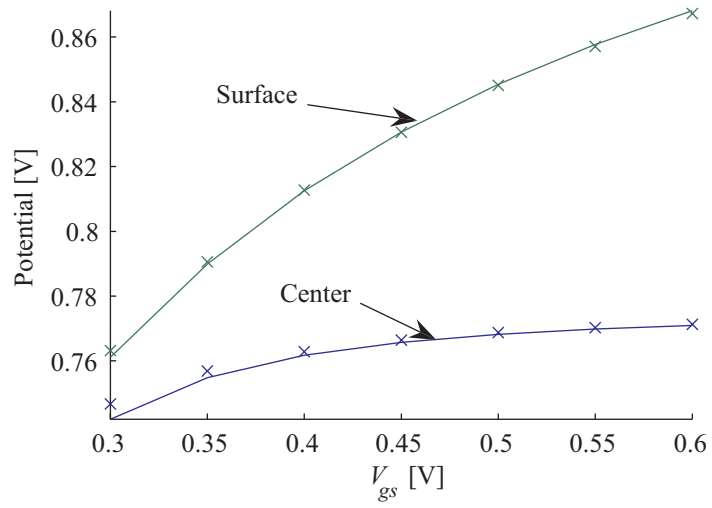


Figure 4.23: Modeled (solid) and simulated (crosses) potentials versus gate voltage for the device center and the mid-gate silicon/oxide interface. $V_{ds} = 0V$

4.5 Quantum mechanical aspects

Above we have used the classical theory for calculating the device electrostatics. A rigorous approach would be to account for the quantization of energy levels primarily in the gate-to-gate direction and apply Fermi statistics. As an example of such an analysis, we consider the special case of a flat potential well where $\phi(y) = V_{gs} - V_{FB}$. As discussed previously, this situation takes place at threshold. We observe a flat gate-to-gate electron concentration except at the silicon-insulator interface where quantum mechanics requires that $n(y)$ drops to zero. This is situation which typically occurs for body thicknesses large than 10 nm. In this case we have the well known square well solution to the Schrödinger equation.

An ultra-thin body (UTB) will exhibit significant quantum effects due to its small silicon body thickness. The concentration of carriers close to the steep oxide walls will be very small, and the loss of charge-induced fields in the self-consistent equation will not be compensated by a increased concentration further into the device. For thicker devices this effect will be less important.

When the charge carrier concentration starts increasing to such levels that the fields emerging from this becomes significant, the quantum effects from confinements have to be considered.

In general, for a 1D quantum confinement, (2.3) gives the electron density per unit area becomes the sum over all states and all sub-bands in a 2D gas of an infinitely deep potential well.

To find the electron distribution along the gate-to-gate center line, we have to consider the wave functions ψ_j of the different sub-bands. For an infinitely deep square well, the Schrödinger equation yields

$$E_{Sq,j} = \frac{(\pi\hbar j)^2}{2m_n t_{Si}^2}, j > 0 \quad (4.37)$$

for the energy levels j and

$$\psi_{Sq,j}(y) = \sqrt{\frac{2}{t_{Si}}} \sin\left(\frac{\pi j(y - t_{ox})}{t_{Si}}\right), t_{ox} < y < t_{ox} + t_{Si} \quad (4.38)$$

for the wave functions. From this we obtain the following probability density functions (PDFs)

$$|\psi_{Sq,j}(y)|^2 = \frac{2}{t_{Si}} \sin^2\left(\frac{\pi j(y - t_{ox})}{t_{Si}}\right), t_{ox} < y < t_{ox} + t_{Si} \quad (4.39)$$

For parabolic wells, the solution of the Schrödinger equation gives harmonic

oscillator solutions. The two first normalized wave functions are

$$\psi_{P,0}(\xi) = \left(\frac{\alpha}{\pi}\right)^{1/4} \exp\left(-\frac{\xi^2}{2}\right) \quad (4.40)$$

and

$$\psi_{P,1}(\xi) = \left(\frac{\alpha}{\pi}\right)^{1/4} \sqrt{2}\xi \exp\left(-\frac{\xi^2}{2}\right) \quad (4.41)$$

where $\xi = \sqrt{\alpha}y$ and $\alpha = m_n\omega/\hbar$, where

$$\hbar\omega = \hbar\sqrt{-\frac{2}{m_n} \frac{d^2\phi}{dy^2}} \quad (4.42)$$

is twice the zero point energy level (lowest). The energy levels are given with the equation

$$E_{P,j} = \hbar\omega(j + 1/2), j \geq 0 \quad (4.43)$$

Multiplying each term in (2.3) with the corresponding probability density functions gives the following total electron distribution over the quantized well.

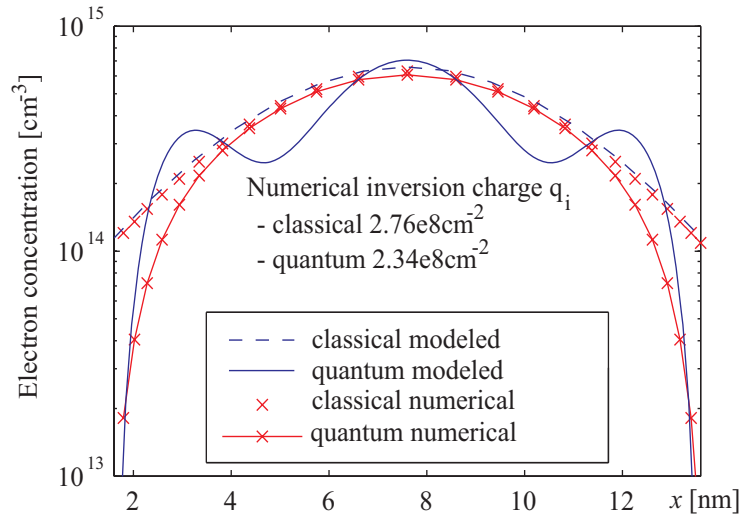


Figure 4.24: Electron concentration for subthreshold conditions ($V_{gs} = 0V$) in the transverse direction, modeled with classical Boltzmann (dashed blue) and Fermi (solid blue) statistics compared with corresponding numerical simulations indicated with red line/crosses.

A comparison of the classical and quantum corrected electron density distribution at the center gate-to-gate axis is depicted in Figure 4.24. We note that the undulations for the modeled quantum distribution comes from the approximated wavefunction solutions for the quantum well. The modeled quantum distribution is composed of 10 approximate waveforms, two Hermite functions for the parabolic energy shape at the lower energy levels, and 8 sine functions which correspond to the higher energies of an infinite square well. The approximation seems to hold for a reasonable error with the present device. We note that the quantum inversion charge is calculated to 84% of the classical concentration.

The numerical quantum simulations are done with the "Density gradient" method, equivalent to the "Quantum Moments Model"⁵⁵.

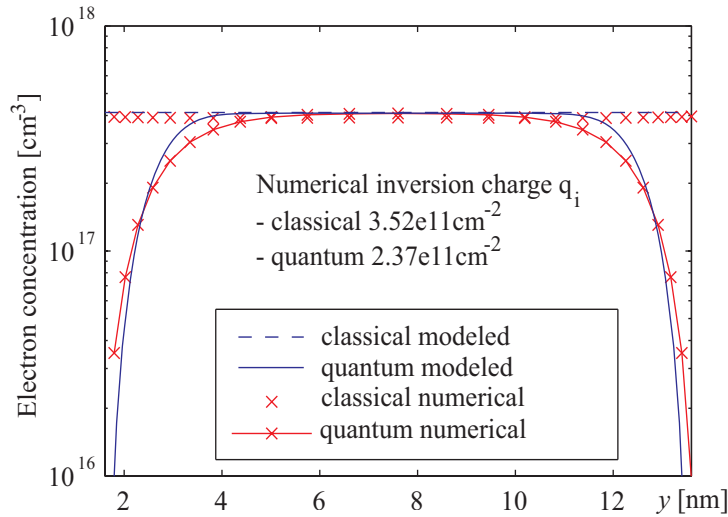


Figure 4.25: Electron concentration at threshold ($V_{gs} = V_T$) in the transverse direction, modeled with classical Boltzmann (dashed blue) and Fermi (solid blue) statistics compared with corresponding numerical simulations indicated with red line/crosses.

For the 'flat' condition, Figure 4.25 illustrates the electron distribution across the transversal direction. We note that the quantum effects on the inversion charge concentration is becoming increasingly important with the quantum inversion charge being 67% of the classical density.

4.6 Discussion

In this chapter we have confronted the problem of 2D modeling of the double-gate MOSFET electrostatics. This modeling is complicated by the self-consistency requirement between the inter-electrode capacitive coupling, the inversion charge, and the drain current.

In sub-threshold, the device electrostatics is dominated by the inter-electrode capacitive coupling, where an explicit, analytical expression for the potential distribution has been obtained from the 2D Laplace equation. Because of the superposition principle, this Laplace solution can always be separated out from the total Poisson's equation, to give an additive contribution to the total potential together with that from the electronic charge.

Near threshold, where the effects of the inversion charge becomes significant, the above mentioned self-consistency is invoked. This is done by using suitable modeling expressions in combination with Poisson's equation, resulting in a description of the total electrostatics that closely agrees with numerical simulations.

For the type of devices discussed here it is found that the classical definition of the threshold voltage, which is based on the band bending $2\phi_b$ is not appropriate. We have therefore proposed as our new definition the gate bias where the electrostatic effects of the capacitive coupling and the electronic charge are equal and opposite at the gate-to-gate symmetry axis for zero drain bias.

In strong inversion, where the electronic charge dominates the device electrostatics, the device behavior approaches that of long-channel devices. Existing long-channel models of the double-gate device are adapted and used in this operating regime.

Chapter 5

DG MOSFET drain current

Different transport models may be applied to calculate drain current, as reviewed in chapter 2.

When modeling charge transport, the channel length is an important modeling parameter. Considering the device presented in Section 4.1, several physical transport mechanisms characterize the charge transport. In this thesis, we assume that the carriers will experience several scattering processes from the source to the drain contact. Although the current will have the character of both ballistic and drift-diffusion transport for short devices, we choose to apply the latter mechanism here assuming a constant mobility to compensate for non-stationary effects. The main advantages of drift-diffusion theory are its simplicity and clear identification of the key processes governing device operation. This choice is made in order to make the transport modeling manageable for validating the electrostatic modeling techniques and simplifications used.

In this chapter, for current calculation, the numerical simulations are performed based on the same assumptions as in the drain current modeling i.e., assuming drift-diffusion transport mechanism with a constant mobility.

However, in our modeling any transverse variation in the quasi-Fermi potential is neglected.

The current strength in this chapter is calculated per unit width of $W = 1\mu m$ and then compared. The drain current per unit width can then be expressed as

$$I_{DD} = -q\mu_n n_s(x) \frac{dV_F}{dx} = q\mu_n n_{s0}(x) e^{(-V_F(x)/V_{th})} \frac{dV_F}{dx} \quad (5.1)$$

where $n_s(x)$ is the surface carrier concentration and $n_{s0}(x)$ is independent of the x -variation in the quasi-Fermi potential. We find the surface carrier concentration by integrating over the spacial electron distribution resulting from the gate-to-gate potential profiles.

Equation (5.1) is separable in the dependencies on x and V_F , which results in the following drain current expression

$$I_{DD} = \mu_n k_b T \frac{(1 - e^{-V_{ds}/V_{th}})}{\int_{-L/2}^{L/2} 1/n_{s0}(x) dx} \quad (5.2)$$

where the term $(1 - e^{-V_{ds}/V_{th}})$ results from the integration over the quasi-Fermi potential from source to drain.

The gate-to-gate potential profiles used for calculating n_{s0} are approximated by parabolas identified by the source-to-drain center line potentials $\phi(x, H/2)$ from (4.19) and the gate potential $V_{gs} - V_{FB}$, as illustrated in the upper part of Figure 5.1.

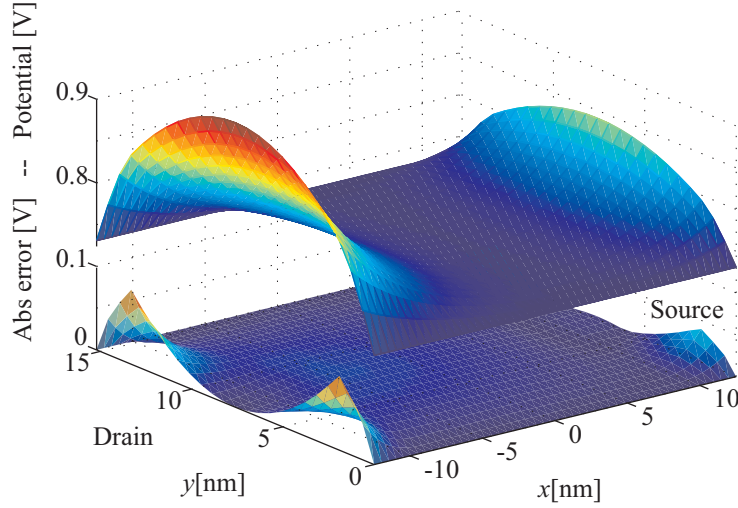


Figure 5.1: The potential distribution for threshold $V_{gs} = 0.25V$, and $V_{ds} = 0.1V$. The upper surface shows how the parabolic function is applied from gate to gate. The surface below is the absolute error between the numerical simulations and the parabolic approximation.

In the lower part, we find, as expected that the error is largest at the corners, and very small throughout the interior. Also the use of parabolic gate-to-gate potential profiles near source and drain is contrary to the earlier assumption of equipotential contacts. However, from (5.2) we observe that the current is determined by the inverse of the electron sheet density, which has its minimum away from the contacts. In that region we observe that the accuracy of the potential is within the desired limits, while the errors at the boundary close to

the source and drain become insignificant in the calculation of the current.

5.1 Self-consistent modeling of drain current

In the electrostatic modeling in Chapter 4, the drain current calculation was divided into three regimes: Subthreshold, near threshold, and strong inversion.

In subthreshold, we observe a rigid source-drain capacitive barrier where the electrostatic influence related to the inversion charge is negligible (See Figure 4.12). Therefore, the potential distribution as calculated from the capacitive coupling is quite unaffected by the relative small amount of inversion charge and the correspondingly small drain current flowing through the device.

While the rigid barrier approximation may be plausible for subthreshold currents, the effects of the drain current and accordingly of the quasi-Fermi potential variation, become increasingly important under near-threshold conditions, see Section 4.3.3. The quasi-Fermi potential can be found by first calculating the current from (5.2), and redo the integration from source up to a position x in the channel. Solving for the quasi-Fermi potential we obtain

$$V_F(x) = -qV_{th} \ln \left[1 - \frac{I_{DD}}{\mu_n q V_{th}} \int_0^x \frac{dx}{n_s(x)} \right] \quad (5.3)$$

This value can then be fed back into Poisson's equation (4.34). Iterating over the equation set improves the accuracy of the electrostatic potential to a high precision of V_F .

In strong inversion, the long-channel model based on the gradual channel approximation is used to find the drain current¹⁶, as discussed in Section 4.4.1. For this regime, we use an effective threshold voltage of $V_T = V_0 + 2\phi_b$ where V_0 is given with the implicit expression¹⁸

$$V_0 = V_{FB} + 2V_{th} \log \left(\frac{\epsilon_{ox} t_{Si} (V_{gs} - V_0)}{2t_{ox} q n_i} \right) \quad (5.4)$$

In the expressions (2.7) - (2.11), constant mobility is assumed. We note that, current saturation is implicitly included through the pinch-off mechanism. Below saturation, the current can be approximated as

$$I_{DD} = \frac{2\mu_n t_{ox}}{\epsilon_{ox} L} \left((V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad (5.5)$$

5.2 Drain current calculations

The 2D modeling presented here is valid from deep subthreshold to slightly above threshold $V_{gs} \leq 0.3V$. Figures 5.2 and 5.3 show a comparison of the modeled

and simulated drain current for a full range of drain-source and gate-source bias conditions. Throughout, we observe deviations between the two of less than ten percent.

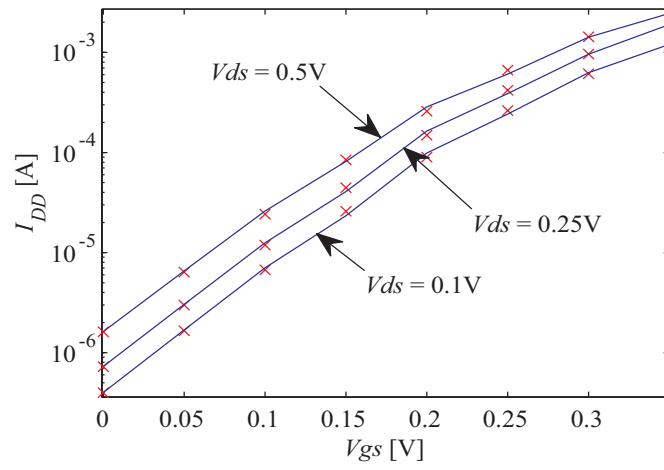


Figure 5.2: The subthreshold and near threshold drain current versus V_{gs} for $V_{ds} = \{0.1, 0.25, 0.5\}V$. Numerical simulations are marked with crosses.

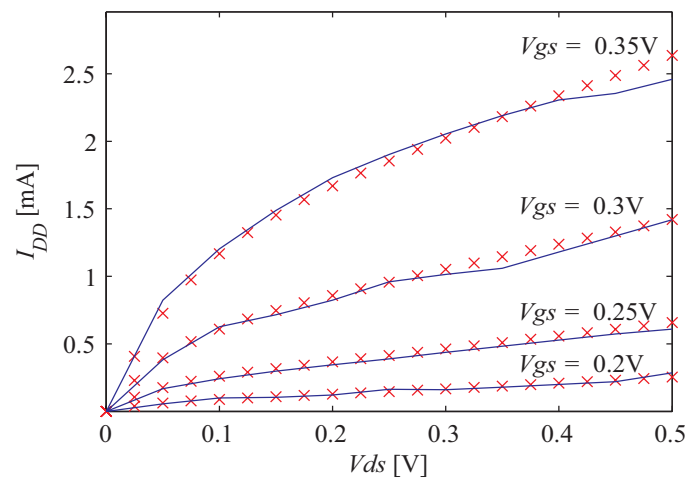


Figure 5.3: I_{DD} - V_{ds} plot for a range of gate voltages. Solid lines indicate modeling and numerical simulations are marked with crosses.

5.3 Compact drain current model

In compact modeling of the drain current, the main concern compared to the previous sections is to find analytical expressions for the current voltage characteristics, which are compatible with the efficiency requirements of circuit simulators. The modeling framework discussed in the earlier chapters enables us to extract parameters for such models. As noted in Sections 2.1.1, 4.4.1, and 5.1, the long-channel strong inversion model is only valid well above threshold.

An example of a compact drain current model can be found by writing a suitable interpolation function that matches the limiting behavior in subthreshold and in strong inversion, and which matches the framework modeling results near threshold.

The proposed interpolation function has the following form

$$I_{DD} = 10^{\wedge} \left[\frac{\log(I_{sub})}{\left[1 + \left(\frac{\log(I_{sub})}{\log(I_{inv})} \right)^m \right]^{1/m}} \right] \quad (5.6)$$

where I_{sub} and I_{inv} are the subthreshold and strong inversion asymptotes, respectively.

Figure 5.4 shows schematically the interpolation function together with the asymptotes. The parameter m is found by matching the interpolated curve to the near threshold calculation, which is marked with symbols. m will be dependent on the applied drain voltage, see Figure 5.5 (solid line).

Figures 5.6 and 5.7 show the interpolated $I - V$ characteristics compared to numerical simulations, using the extracted values for m .

The undulations observed in the characteristics of Figure 5.7 reflect a slight lack of precision in the extraction of m , which is also seen in Figure 5.5. Nonetheless, we observe a very good agreement between the compact modeling and the numerical simulations. We note in particular that this good agreement includes the range between threshold and strong inversion not covered by the modeling framework of Section 5.2.

For the compact model it is suitable to express the dependence of the parameter m on V_{ds} by a smooth function. As an example, Figure 5.5 shows this relationship approximated by a second degree polynomial least-square fit to the extracted values of m . The corresponding $I_{DD} - V_{ds}$ characteristics are shown in Figure 5.8.

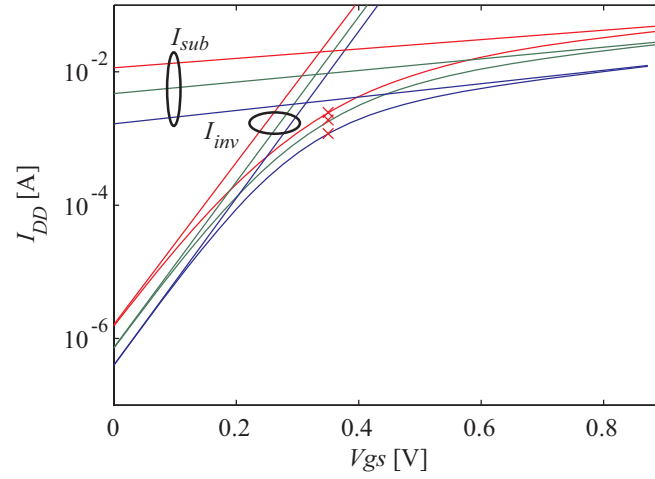


Figure 5.4: Illustration of the asymptotes which for each V_{ds} are from subthreshold and strong inversion calculations, and then adjusted for one threshold current calculation indicated with the crosses.

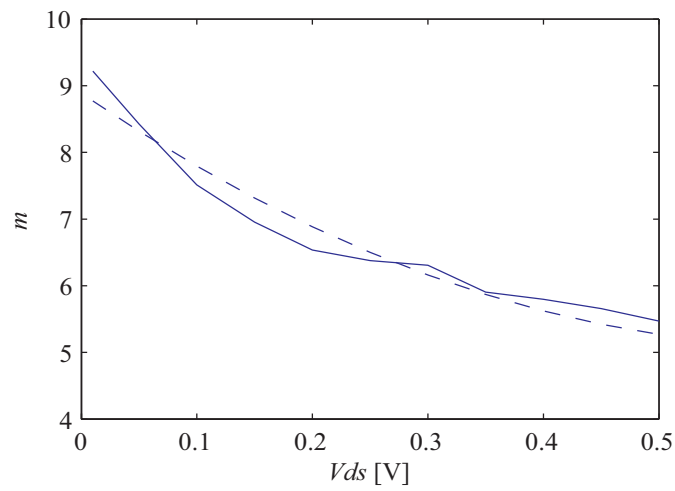


Figure 5.5: The m -parameter versus drain bias. Dashed line indicates a second degree polynomial least square curve fit.

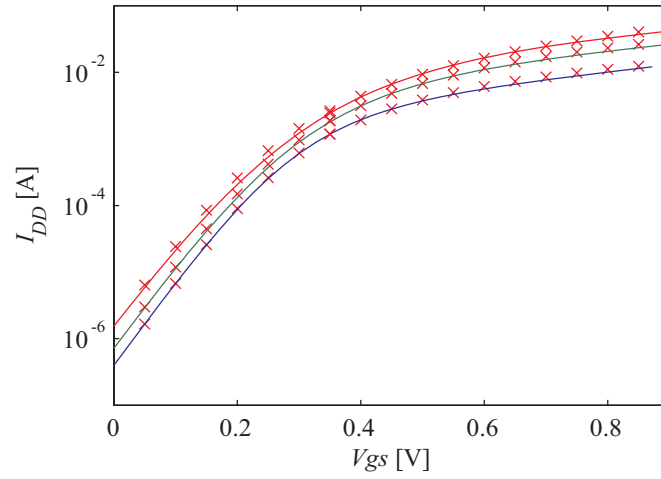


Figure 5.6: $I_{DD} - V_{gs}$ interpolated plot for $V_{ds} = \{0.1, 0.25, 0.5\}$ V, compared with numerical simulations indicated with crosses.

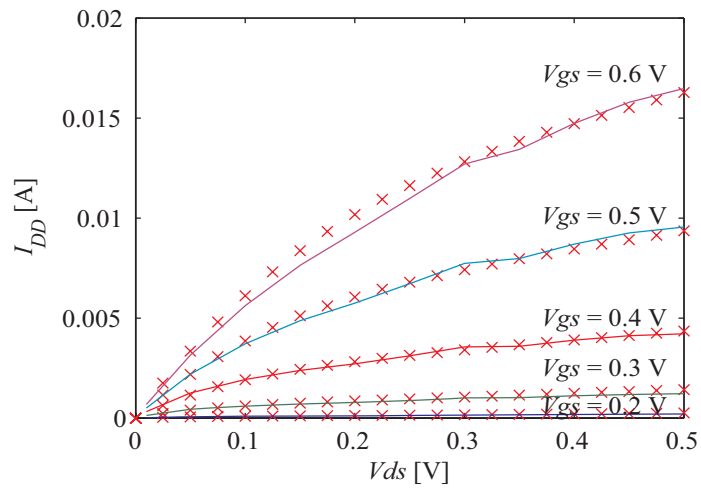


Figure 5.7: $I_{DD} - V_{ds}$ interpolated plot compared with numerical simulations indicated with crosses.

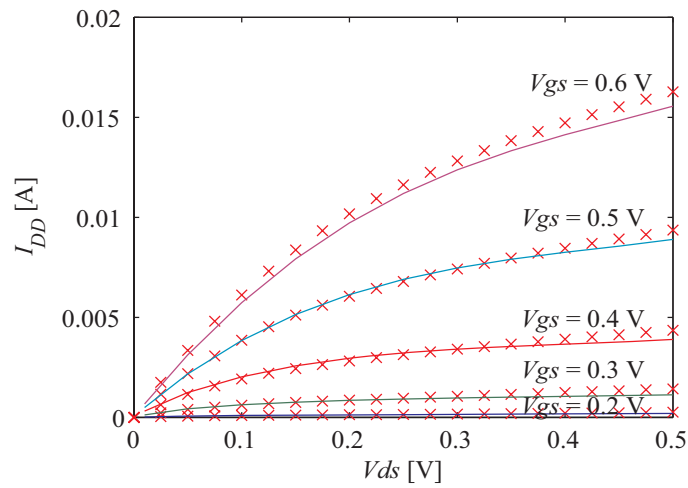


Figure 5.8: $I_{DD} - V_{ds}$ interpolated plot approximating the m -parameter from a polynomial curve fit. The modeling in solid is compared with numerical simulations indicated with crosses.

5.4 Discussion

In nanoscale MOSFETs, with channel lengths less than about 50 nm, the relaxation times of the carriers indicate that the drain current will have the character of both drift-diffusion and ballistic/quasi-ballistic transport. In this work, to make the transport modeling manageable, we have used the drift-diffusion transport model in order to validate the electrostatic modeling techniques and simplifications which have been applied in the modeling process. Furthermore, we have assumed a constant mobility, thereby neglecting velocity saturation. Instead, the drain current is described by the pinch-off mechanism. This tends to overestimate the drain current especially in saturation. On the other hand, neglecting the ballistic component, would lead to an underestimation of the current. Some work on the modeling of transport in the transition region between drift-diffusion and ballistic has recently been reported⁵⁶. These issues clearly require further studies.

Numerical simulations performed with energy-balance and hydrodynamic models⁵⁷ show that the present modeling using drift-diffusion with constant mobility falls between the two with a maximum deviation of 20 % to either.

Compared to this, drift-diffusion simulations assuming default velocity saturation, underestimate the drain current by typically an order of magnitude for the present device. Similar behavior is observed for a range of different gate lengths. Hence, we conclude that the present modeling gives a satisfactory representation of the drain current.

We have also presented an analytical and explicit $I - V$ model. The parameters of this model are fully extractable from the modeling framework. This compact model is predictive in the sense that it also covers bias conditions for which the modeling framework, as presented here, still does not apply. Moreover, the model is continuous in all derivatives, which is highly advantageous in the context of circuit simulators. Likewise, the scaling properties of the compact model parameters can also be obtained from the modeling framework. This will be subject of future investigations.

Chapter 6

Conclusion

In this work, an electrostatics and drain current modeling framework for double-gate MOSFETs has been established. The modeling covers the subthreshold and near threshold regimes of operation. In addition, the limiting behavior in very strong inversion is described.

The sub-threshold modeling is analytical and explicit, whereas the near-threshold region is calculated in an iterative scheme mostly due to the self-consistent analysis of the electrostatic effects arising from the mobile charge, the capacitive coupling and the drain current. The strong inversion modeling is based on a long-channel approximation, which is applicable at high gate bias.

An example of a parametrized compact model for drain current calculation has been presented. This model covers the full range of bias conditions and is suitable for implementation in circuit simulators, such as SPICE. The model parameters are all extracted from the modeling framework, which provides a precise physical basis for the computed results.

Both electrostatics and current calculations have been compared to numerical simulations performed with the Atlas device simulator from Silvaco. The electrostatics has been verified for potential profiles along the device symmetry lines and the current has been verified for $I_d - V_{gs}$ and $I_d - V_{ds}$ characteristics for a wide range of applied bias voltages. They all show excellent agreement with the results from the numerical device simulator.

Chapter 7

Future work

A complete compact model for inclusion in circuit simulators must have procedures for calculating currents, capacitances, and noise. Here, we have exclusively considered electrostatics and drain current of a DG MOSFET. Thus, there are several issues within this work that is in need of additional analysis, including the ones discussed below.

7.1 Strong inversion modeling

Strong inversion current modeling in this thesis is based on a long channel model, which applies to the device considered here only for high gate bias. The present modeling therefore does not cover the gate bias range between the threshold region and the upper part of the strong inversion regime. Work is already well under way to bridge this gap, and preliminary results are already scheduled for publication.⁴⁷

7.2 Development of SPICE-type model

The modeling framework developed in this thesis is based on analytical expressions. However, because of the complexity of the analysis, it has been necessary to apply iterative schemes. To make the modeling applicable for circuit simulation, we therefore used the modeling framework as a preprocessing routine, where parameters are extracted from the framework for use in parametrized compact models. These compact models are suitable for implementation in SPICE-type circuit simulators. A high computational speed is necessary if the model is to be implemented in a SPICE simulator. Additionally, the compact

model will be continuous in the derivatives with respect to applied biasing.

7.3 Capacitances

To ensure accuracy, a capacitance model should be derived from the charge distribution in the device body, or equivalently of the vertical electric field distribution on the four electrodes. The bias dependence of this distribution is contained implicitly in our analysis. It requires in principle numerical analysis to obtain the capacitive values. Compact, analytical modeling expressions need to be developed for use in circuit simulators.

7.4 Noise

Noise modeling is also an important part of a compact model. Cooperating groups are working with this subject and results have been posted in publications.⁵⁸

7.5 Application to other FET devices

Next generation candidates for device technology include not only double-gate MOSFETs, but also FinFETs and Gate-All-Around (GAA) MOSFETs. The modeling presented here is a good foundation on which modeling procedures for these device configurations can be developed.

7.5.1 GAA MOSFET

The cylindrical GAA MOSFET is inherently a 3D device, which means that conformal mapping procedure is inapplicable. However, the topography of the GAA MOSFET is particularly interesting, because the inter-electrode effects of this configuration can be shown to have a good similarity to that of the DG MOSFET. This allows us to map the DG MOSFET results into the GAA MOSFET with good precision. Preliminary analysis along this line is presently being published^{48, 50, 47} and a coming doctoral thesis will discuss this device in detail.

7.5.2 FinFET

The FinFET configuration is another next generation device type which could have the potential to fit into the modeling framework presented here in this thesis. The FinFET is also a 3D device, for which the 2D conformal mapping cannot be directly applied. Work on this is already in progress.

Appendix A

The Schwartz-Christoffel transformation

1.1 Definition of the Schwartz-Christoffel Mapping

The following are collected from Abramovitz & Stegun,⁵² and The Mathematica help.⁵⁹

A conformal mapping, also called a conformal map, conformal transformation, angle-preserving transformation, or biholomorphic map, is a transformation $w = f(z)$ that preserves local angles. An analytic function is conformal at any point where it has a nonzero derivative. Conversely, any conformal mapping of a complex variable which has continuous partial derivatives is analytic.

Consider a polygon in the complex plane. The Riemann mapping theorem implies that there is a bijective holomorphic mapping f from the upper half-plane

$$\{\zeta \in \mathbb{C} : \text{Im } \zeta > 0\} \tag{A.1}$$

to the interior of the polygon. The function f maps the real axis to the edges of the polygon. If the polygon has interior angles $\alpha, \beta, \zeta, \dots$ then this mapping is given by

$$f(\zeta) = \int^{\zeta} \frac{K}{(w-a)^{1-(\alpha/\pi)}(w-b)^{1-(\beta/\pi)}(w-c)^{1-(\gamma/\pi)} \dots} dw \tag{A.2}$$

where K is a constant, and $a < b < c < \dots$ are the values, along the real axis of

the ζ plane, of points corresponding to the vertices of the polygon in the z plane. A transformation of this form is called a Schwarz-Christoffel mapping.

1.2 Schwarz-Christoffel rectangle transformation

Application of the Schwartz-Christoffel transformation to a rectangle-shaped structure is done by recognizing the corner angles which all are at $\alpha = \beta = \phi = \gamma = \pi/2$. Hence all singularities will be square roots. The corners position is located at the transformed boundary at the points $u = \{-1/k, -1, 1, 1/k\}$.

$$f(\zeta) = \int^{\zeta} \frac{K}{(w-1)^{1/2}(w-(-1))^{1/2}(w-1/k)^{1/2}(w-(-1/k))^{1/2}} dw \quad (\text{A.3})$$

which gives the following simplified integral

$$f(\zeta) = \int^{\zeta} \frac{K}{\sqrt{w^2-1}\sqrt{w^2-1/k^2}} dw \quad (\text{A.4})$$

This integral is defined as an elliptic integral of the first kind and can be computed in terms of power series or iteration algorithms.

1.3 Elliptic integrals and evaluation

Implementations for elliptic integrals are well documented in a range of books, for example⁶⁰ and⁵².

$$F(k, u) = \phi + m \frac{\phi^3}{6} + m \frac{(-4+9m)\phi^5}{120} + m \frac{(16-180m+220m^2)\phi^7}{5040} + m \frac{(-64+3024m-12600m^2+11025m^3)\phi^9}{362880} + O(z^{11}) \quad (\text{A.5})$$

F as argument of u and ϕ is illustrated in figure A.1 and A.2 correspondingly.

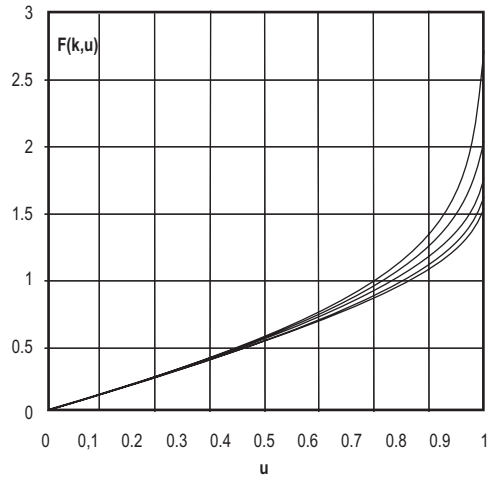


Figure A.1: The elliptic integral as function of u , $k = [0, 1]$.

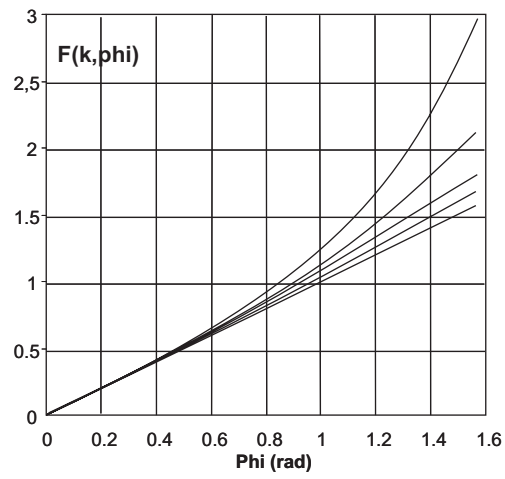


Figure A.2: The elliptic integral as function of ϕ , $k = [0, 1]$.

1.3.1 Elliptic functions

- k is the elliptic modulus
- $m = k^2$
- α the modular angle, $k = \sin \alpha$
- ϕ the amplitude
- x where $x = \sin \phi = \operatorname{sn} u$
- u , where $x = \operatorname{sn} u$ and sn is one of the Jacobian elliptic functions
- $\operatorname{sn} u = \sin \phi$
- $\operatorname{cn} u = \cos \phi$
- $\operatorname{dn} u = \sqrt{1 - m \sin^2 \phi}$

$$F(x; k) = \int_0^x \frac{1}{\sqrt{(1-t^2)(1-k^2t^2)}} dt \quad (\text{A.6})$$

$$x = \sin \phi, \quad t = \sin \theta, \quad \alpha = \sin(\alpha), \quad m = k^2$$

$$F(x; k) = F(\phi|m) = F(\phi \setminus \alpha) = \int_0^\phi \frac{1}{\sqrt{1 - \sin^2 \alpha \sin^2 \theta}} d\theta \quad (\text{A.7})$$

$$K(k) = \int_0^1 \frac{1}{\sqrt{(1-t^2)(1-k^2t^2)}} dt \quad (\text{A.8})$$

$$K(k) = \int_0^{\frac{\pi}{2}} \frac{d\theta}{\sqrt{1 - k^2 \sin^2 \theta}} \quad (\text{A.9})$$

$$K(m) = K = \int_0^{\pi/2} \frac{d\theta}{\sqrt{1 - m \sin^2 \theta}},$$

$$iK'(m) = iK' = i \int_0^{\pi/2} \frac{d\theta}{\sqrt{1 - m' \sin^2 \theta}} \quad (\text{A.10})$$

K and K' are called the real and imaginary quarter-period respectively. They also represent the complete elliptic integral for $K(k)$ and $K(k' = \sqrt{1 - k^2})$. Per definition $K'(k) \equiv K(k')$ We get that $K(m) = K'(m') = K'(1 - m)$.

It is possible to get the Jacobi elliptic functions from a numerical procedure which uses the boundary normed to the quarter-period and the elliptic modulus $m = k^2$.

In terms of elliptic functions, an inverse of the incomplete elliptic integral is found to be the Jacobi amplitude which can be defined by⁵⁹

$$\phi = \text{am}(u, k) = \int_0^u \text{dn}(u', k) du' \quad (\text{A.11})$$

$$\phi = \text{am}(k, z) = F^{-1}(k, z) \quad (\text{A.12})$$

$$\sin^{-1} \phi = \text{Arcsn}(x, k) = \int_0^x \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}} \quad (\text{A.13})$$

substituting for $w = \sin \phi$

$$w = F(x, k) = \int_0^\phi \frac{d\theta}{\sqrt{(1-k^2 \sin^2 \theta)}} \quad (\text{A.14})$$

$$\phi = \sin^{-1} w = F^{-1} \left(k^2, \frac{2K}{L} z \right) \quad (\text{A.15})$$

and together with

$$w = \sin(\text{am}(k, z)) = \text{sn}(k, z) \quad (\text{A.16})$$

where

$$z = \sin \phi = \text{sn}(k, w) \quad (\text{A.17})$$

The inverse of the elliptic integral can be expressed in terms of the above elliptic functions as follows

$$\text{sn}(x + iy) = \frac{\text{sn}(x|m) \text{dn}(y|m') + i \text{cn}(x|m) \text{dn}(x|m) \text{sn}(y|m') \text{cn}(y|m')}{\text{cn}(y|m')^2 + m \text{sn}(x|m) \text{sn}(y|m')} \quad (\text{A.18})$$

Appendix B

SINANO template

The European union research project Silicon Nano-devices (SINANO) has defined a template for a double-gate device.

2.1 Template description

The device is based on a symmetrical doping profile for both source and drain with the same Gaussian characteristic. Doping of the bulk case is a mirroring of the top process.

P-type uniform substrate doping:

Body acceptor concentration: $N_S = 1 \cdot 10^{15} \text{cm}^{-3}$

$$N(x, y) = G(y) \cdot L(x) \quad (\text{B.1})$$

All injections have a gaussian profile with an implant of $N_{PEAK} = 1 \cdot 10^{20} \text{cm}^{-3}$ in $y = 0$.

N-type source extension profile:

Standard deviation: $\sigma_y = 5.64 \cdot 10^{-3} \mu\text{m}$

$$G(y) = N_{PEAK} e^{-\frac{1}{2}[(y)/(\sigma_y)]^2}; y > 0 \quad (\text{B.2})$$

$$L(x) = 1; \quad x < x_0 \quad (\text{B.3})$$

$$L(x) = N_{PEAK} e^{-\frac{1}{2}[(x-x_0)/0.28\sigma_y]^2}; \quad x > x_0 \quad (\text{B.4})$$

N-type source contact profile:Standard deviation: $\sigma_y = 1.12 \cdot 10^{-2} \mu m$

$$G(y) = N_{PEAK} e^{-\frac{1}{2}[y/\sigma_y]^2}; y > 0 \quad (\text{B.5})$$

$$L(x) = 1; \quad x < x_1 \quad (\text{B.6})$$

$$L(x) = N_{PEAK} e^{-\frac{1}{2}[(x-x_1)/(0.35\sigma_y)]^2}; \quad x > x_1 \quad (\text{B.7})$$

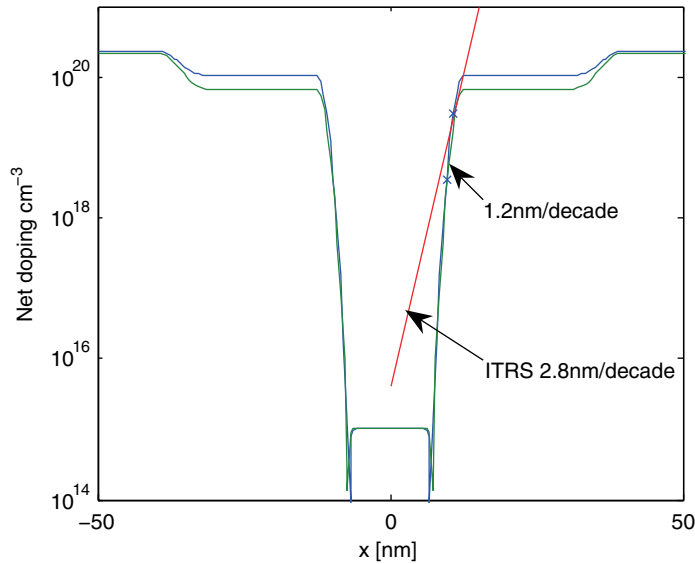


Figure B.1: Source to drain cuts of doping profile at the silicon/oxide boundary (blue) and at the center symmetry line.

As can be seen in the doping profile in figure B.1, the lateral profile drops very fast towards the center. While the target profile for the 65nm node is 2.8nm/decade according to the ITRS roadmap, the source extension first drop close to this target, but it approaches 0.7nm/decade into the body.

Compact modeling of physical mechanisms in doping profiles is difficult. To simplify, a piecewise equipotential boundary around the device is desirable.

An ideal device has been created, based on the template device. The doping profiles at the contacts of the template device is replaced with ideal n^+ polysilicon contacts resulting in negligible depletion regions. This creates equipotential

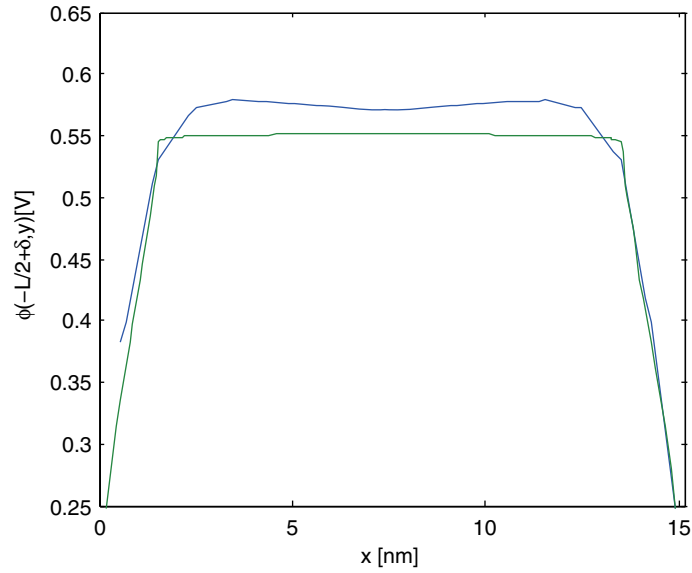


Figure B.2: Source contact potential profile for template and ideal device.

surfaces along the contact boundary, which is more suitable to model. Figure B.2 illustrates the difference between the two at the contact/body border.

Changing the contacts also changes the intrinsic device potential illustrated in figure B.3.

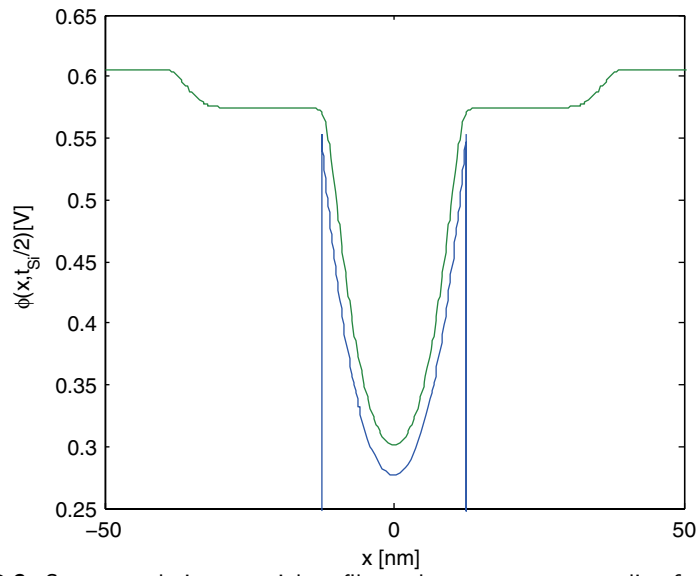


Figure B.3: Source to drain potential profile at the center symmetry line for template and ideal device.

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