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Fabrication and Electronic Investigation of GaAs nanowire/Graphene Hybrid Devices

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Master's thesis

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Abstract

In the present study, a process for fabricating GaAs nanowire/graphene hybrid devices using electron beam lithography processing techniques is presented and demonstrated. Fabricated devices were investigated electronically by measuring I-V characteristics under a variable gate voltage.

Fabrication processes for both exfoliated and CVD-grown graphene were developed. For exfoliated graphene the outlined process is unsuccessful, as the graphene flakes were found to crumble and fall off during the first processing step following transfer. It is thus concluded that exfoliated graphene flakes are too delicate to perform any significant processing after graphene transfer.

The fabrication process was successfully demonstrated in fabrication of devices with CVD-grown graphene. However, nanowires in these devices were seen to undergo significant corrosion during the process, which is credited to the water exposure associated with graphene transfer. This was found to be an especially prominent issue for contacted nanowires, where the metal contact is believed to facilitate galvanic corrosion.

I-V characteristics and gate voltage dependence were measured for GaAs nanowire/graphene hybrid devices made with CVD-grown graphene. Large variations in the I-V behavior and gate voltage dependence was observed. This is credited to corrosion in the nanowires, which is thought to result in uncharacteristic behavior for metal-GaAs contacts. There are also indications that several devices are shortened by graphene. The electronic investigations are therefore found to be inconclusive in respect to the electronic properties of the graphene/GaAs nanowire junction. It is concluded that further developments in the fabrication process are needed to achieve GaAs nanowire/graphene hybrid devices suitable for detailed analysis.

Sammendrag

I den foreliggende studien blir en prosess for fremstilling av GaAs nanotråd/grafén-prøver ved hjelp av elektronstrålelitografi presentert og demonstrert. Fabrikkerte prøver ble undersøkt elektronisk ved å måle I-V karakteristikker med variabel styrespenning.

Fabrikasjonsprosesser for både eksfoliert og CVD-grodd grafén ble testet. For eksfoliert grafén var fabrikasjonsprossesen mislykket, da det viste seg at grafénflakene smuldret opp og falt av substratet i det første prosesseringstrinnet etter grafénoverføringen. Det konkluderes dermed at eksfolierte grafénflak er for sensitive til å gjøre noen signifikant prosessering etter grafénoverføringen.

Fabrikasjonsprosessen ble demonstrert til å fungere for prøver med CVD-grodd grafén. Imidlertid ble en signifikant korrosjon for nanotrådene i disse prøvene observert, noe som blir kreditert til vanneksponeringen under grafenoverføringstrinnet. Dette var et spesielt fremtredende problem for kontaktete nanotråder. I dette tilfellet mistenkes det at metallkontaktene forårsaker galvanisk korrosjon i nanotrådene.

Målinger av IV-karakteristikk og styrespenningsavhengighet ble utført på GaAs nanotråd/grafén-kontakter med CVD-grodd grafén. Store variasjoner i I-V oppførsel og styrespenningsavhengigheten ble observert, noe som blir kreditert til korrosjonen av nanotrådene, ettersom det antas at dette fører til ukarakteristisk oppførsel i GaAs-metall kontaktene. Det er også indikasjoner på at enkelte prøver er kortsluttet av grafén. De elektroniske undersøkelsene antas derfor å være for mangelfulle til å kunne trekke noen konklusjon i forhold til egenskapene ved GaAs nanotråd/grafén-kontakter. Det konkluderes derfor at videre utvikling av fabrikasjonsprosessen er nødvendig for å oppnå GaAs nanotråd/grafén-prøver egnet for mer detaljert analyse.

Acknowledgements

This project has been conducted at the Norwegian University of Science of Technology (NTNU), with the Department of Electronics and Telecommunications (IET). The work were done in Prof. Helge Weman and Prof. Bjørn Ove Fimland's group at IET, a research group working with growth and characterization of GaAs nanowires for optoelectronic applications, such as solar cells. The practical work was conducted in NTNUs cleanroom facilities, NTNU Nanolab, with the exception of the electrical characterization, which was done in the IET probing station lab.

First, I would like to thank my supervisor Helge Weman for giving me the opportunity to participate and contribute to their exciting research. By working on this project I feel that I have gained valuable insight and knowledge on the scientific research on nanowires, both in theory and practical experiments. This has been a very exciting project, and I am very motivated to continue on similar topics in the future.

I would also thank my co-supervisor Dr. Dong Chul Kim. He has been very helpful to me throughout this project, devoting countless hours to both guiding me through the practical procedures in Nanolab, and helping me understand the theory behind the processes.

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Acronyms

IPA Isopropyl Alcohol

EBL Electron Beam Lithography

rpm Rounds per minute

PMMA Polymethyl Methacrylate

CVD Chemical Vapor Deposition

RIE Reactive Ion Etching

SEM Scanning Electron Microscope

CVDG-device CVD-grown Graphene device

ExG-device Exfoliated Graphene device

DI water Deionized water

MGM-contact Metal-Graphene-Metal contact

VB Valence Band

CB Conduction Band

MNWM-contact Metal-Nanowire-Metal contact

GP/NW-device Graphene-Nanowire device

MSC-junction Metal-Semiconductor junction

GPSC-junction Graphene-Semiconductor junction

Chapter 1

Introduction

Semiconductors are today an indispensable part of modern technology. Forming the basis for the transistor, they are the fundamental building blocks of today's electronics [1]. The development in the semiconductor industry has traditionally been driven by miniaturization, following the trend of doubling the amount of transistors that can be fitted into a given area every second year, a trend commonly known as Moore's law. Ten years ago, the transistor dimensions were pushed to 100 nm, putting transistors in the nano regime [2]. In the nano scale, devices behave differently as surface effects start dominating over bulk effects, and quantum effects come into play [3]. Although the nano regime poses a great challenge to the conventional scaling of the semiconductor industry, the new regime also offers many exciting new possibilities.

A perfect example of these possibilities is graphene, a rising star within the field of nanotechnology. Graphene is a material consisting of one single layer of carbon atoms organized in a honey-comb lattice. Since its first successful isolation in 2004 [4], graphene has been subject to an explosive increase in research, which can be credited to its extraordinary properties like mechanical strength and flexibility [5], thermal conductivity [6] and impermeability to gases [7]. In terms of semiconductors, graphene is especially interesting due to its electronic properties [8]. Graphene exhibits excellent transport properties, including an exceptional electron mobility [9]. Although graphene has been suggested as a replacement of silicon in transistors [10], a complete replacement is considered unlikely [11]. Graphene is however expected to play a major role in future electronics in combination with other semiconductors.

One particular interesting combination for graphene is semiconductor nanowires,

which is also one of the most active research areas within the nano science community [12]. Nanowires are one-dimensional, crystalline structures with a diameter in the nano regime, and a typical length of a few micrometers. Due to their unique physical properties, semiconductor nanowires are considered as an ideal candidate for various future nanoscale devices [13, 14, 15]. Semiconductor nanowires have been demonstrated in light-emitting diodes [16], lasers [17], transistors [18] and solar cells [19].

Recently, it has been demonstrated that graphene can in fact also act as a substrate for epitaxial growth of nanowires [20]. This is an especially tantalizing concept. Not only would this represent potential substantial cost-savings in terms of replacing the costly single-crystalline semiconductor substrates normally required for epitaxial growth, but it also opens up the possibility for a wide array of unconventional electronic and optoelectronic devices, where graphene acts as a flexible, transparent electrode [21]. To realize such devices, it is however paramount to establish a good understanding of the interface formed between graphene and semiconductors, and the electronic properties of such a junction.

In terms of optoelectronic devices, a natural partner for graphene is the III-V semiconductor GaAs, which is regarded as a ideal candidate due to its direct-band gap and high electron mobility. Graphene-GaAs is however a relatively unexplored system, both in terms of GaAs acting as substrate for graphene [22] and the electronic properties of the GaAs-graphene junction [23]. Furthermore, to the author of this thesis's knowledge, there exists no studies that explore the electronic properties of a graphene-GaAs nanowire junction.

In the present study, an investigation of the graphene-GaAs nanowire system is conducted. A fabrication process for graphene/GaAs nanowire hybrid devices is developed and presented. Fabricated devices are investigated electronically by measuring I-V characteristics in the presence of a variable gate voltage, and the results are discussed in light of the present theory on graphene-semiconductor junctions.

Chapter 2

Theory

2.1 Semiconductor physics

To discuss the Graphene-Semiconductor junction (GPSC-junction), a brief introduction to some important concepts from semiconductor physics is needed.

2.1.1 Band Theory

In order to analyse the behavior of an electrical current in semiconductors, a model for describing electrons propagating through a solid is needed. An electron is a quantum particle, and should therefore be described in terms of the Schrödinger equation, which treats electrons like waves. Solving this equation for electrons affected by the coulomb potential of a positive atom core gives rise to a discrete set of allowed energy states, commonly referred to as orbitals. One of the postulates of quantum mechanics, the Pauli exclusion principle, states that two quantum particles can not occupy the same quantum state. For the case of electrons, this implies that each energy state can be occupied by two electrons, as electrons have two quantum states due to their internal spin [1, p. 49].

In the *nearly free electron* model, one assumes that the electrons occupying the outermost orbitals around an atom can be treated as free electrons in a periodic coulomb potential arising from the atom cores, and electron-electron interactions are ignored. Solving Schrödinger equation for this case gives rise to bands centered on the energy states from the single-atom case. These bands consist of N discrete energy states, where N is the number of positive ion cores

making up the periodic potential. The gap between each discrete state in a band is narrow enough to let the bands be treated as continuous.

In a nearly free electron model at 0 K, the electrons fill the lowest available energy states. The energy of the highest occupied energy state is defined as the *Fermi energy*. When we allow the temperature to rise, there will be thermal energy available to the system, which can excite electrons to higher energy states. This will however only affect the electrons with an energy close to the Fermi energy, as only these have empty states separated by an energy comparable to the thermal energy available. The probability of an orbital being filled is described by the *Fermi-Dirac distribution*, which is given as:

$$f(E) = \frac{1}{exp[\frac{E-\mu}{kT}] + 1} \tag{2.1}$$

where T is temperature, k is Boltzmann's constant, and the chemical potential μ is the quantity at which the Fermi-Dirac distribution equals 1/2. This quantity is paramount in the analysis of electron transport, as the nearly free electron model predicts that only electrons with energy close to μ are important in determining electrical properties of solids. The quantity μ is a function of temperature, and is often referred to as the *Fermi level* in semiconductor physics. The Fermi level should not be confused with the Fermi energy, which is only defined for 0 K.

Based on band theory, one can classify solids based on their electrical properties. In a simplified view, an electrical current can be viewed as electrons moving between states, as empty states within short interval energy interval are needed for electrons to propagate through a solid. For metals the Fermi level is situated in the middle of a band, implying that electrons near the Fermi level have empty available states nearby for all temperatures. Metals are thus good conductors at all temperatures. In the case where the Fermi level is situated between two bands, the completely filled band below the Fermi energy is normally referred to as the Valence Band (VB) and the empty band above as the Conduction Band (CB). At low temperatures, these materials are isolating, as there are no electrons in the CB and the electrons in the VB have no states to move to. However, if the energy gap is comparable to the available thermal energy, electrons can be thermally excited into the CB and contribute to a current. Such materials are either called semiconductors or isolators, based on the size of their energy gap. There is no exact definition of the value of the energy gap to differ a semiconductor from an isolator, but materials are typical called semiconductors up until ~ 6 eV.

While all current is composed of the movement of electrons, it is necessary to distinguish between electron transport in the CB and VB for semiconductors. Electrons excited to the conduction band will experience a large amount of available states at the same energy, and can thus more or less move freely in the crystal. This excitation will however leave an empty state in the valance band, and this electron vacancy can contribute to a current in the form of an electron moving into this vacancy, leaving an empty state somewhere else. A convenient method for modelling this current mechanism is to treat this "hole" as a positive particle, which accordingly behaves opposite to an electron for an applied electric field.

2.1.2 Crystal structure and k-space

In a crystalline solid, the atoms are arranged in a periodic manner. An ideal crystal can be described in terms of a mathematical lattice with a basis, the smallest repetitive element in the crystal, at each lattice point [24, p. 4]. A three dimensional crystal may be defined by three translation vectors a_1, a_2, a_3, such that the crystal will look identical from any point reached from doing translation by an integer number of a's,

$$r' = r + u_1 a_1 + u_2 a_2 + u_3 a_3 \tag{2.2}$$

. This defines the *primitive translational vectors* of the lattice. Based on the internal relations of angles and lengths of these vectors, one can define 14 mathematical lattices, which can be used to present real crystals by introducing a basis of atoms at the lattice points.

The periodic nature of a crystal make them ideal for use of Fourier analysis[1]. By Fourier transforming the *primitive lattice vectors* one obtains the *reciprocal lattice vectors*, which defines the reciprocal space of the lattice. The reciprocal space is the representation of a crystal in terms of its periodicity in k-space. Instead of spatial coordinates, the reciprocal space coordinates are given terms of wave numbers, and is therefore often called k-space. A function viewed in reciprocal space at a specific k - value, for example $k = \pi$ would convey information on how said function varies on a π periodicity.

[1]Fourier analysis - the study of the way general functions may be represented or approximated by sums of simpler trigonometric functions. In practice Fourier analysis implies presenting a function in terms of their periodicity instead of spatial values.

2.1.3 Band structure

While a simple assessment of the *nearly electron model* can justify the formation of energy bands in a solid, a more accurate model that includes the crystal structure and electron-electron interactions is needed to portray the accurate band structure in a solid. Developing such models and mapping the electronic structures is a complex task, and normally involves extensive simulations and numerical methods. These models plot the allowed energy values in terms of the wave-vectors k of the electrons, and these relations are thus often called E-k relations. As the crystal periodicity is different for various crystal directions, these relations constitute complex surfaces that should be visualized in three dimensions. It is however common to choose specific axes of interest, and plot these in a 2-dimensional manner, as seen in Figure 2.1a.

For the analysis of devices, it is however common to adopt a "simplified" band diagram. In these diagrams, one plots the bottom of the conduction band and the top of the valence band as a function of position in the device, along with the Fermi level (Figure 2.1b). Such diagrams are plotted in terms of potential energy for the negative electrons, implying that holes, being positive, gain potential energy by moving downwards in these diagrams.

2.1.4 Metal-semiconductor junctions

When a contact between a metal and a semiconductor is made, the ideal nature of the contact can be estimated from a band diagram assessment, and by examining the difference between the work function of metal,Φ_M, and the workfunction of the semiconductor,Φ_S [1, p. 227]. The work function is defined as the difference between the Fermi level and the energy level at vacuum, i.e. the energy required to remove an electron from the Fermi level and put it in vacuum. To assess the nature of the contact, one can make the thought experiment of having two separate blocks of metal and semiconductor and bringing them into contact. It can be shown that for a junction at thermal equilibrium it is necessary to have Fermi levels in both materials at the same level, as a gradient in the Fermi level would implicate a current [**?** , p. 109]. Bringing the metal and semiconductor together will thus result in an alignment of Fermi levels, which happens by charge transfer between the two materials. If the charge required to align the Fermi level is supplied by the minority carriers in the semiconductor, as is the case for p-type semiconductors and metals where $\Phi_m - \Phi_s < 0$, a depletion region[2] will form, creating a potential barrier for

[2]Depletion region: A region depleted of mobile carriers, and dominated by space charge.

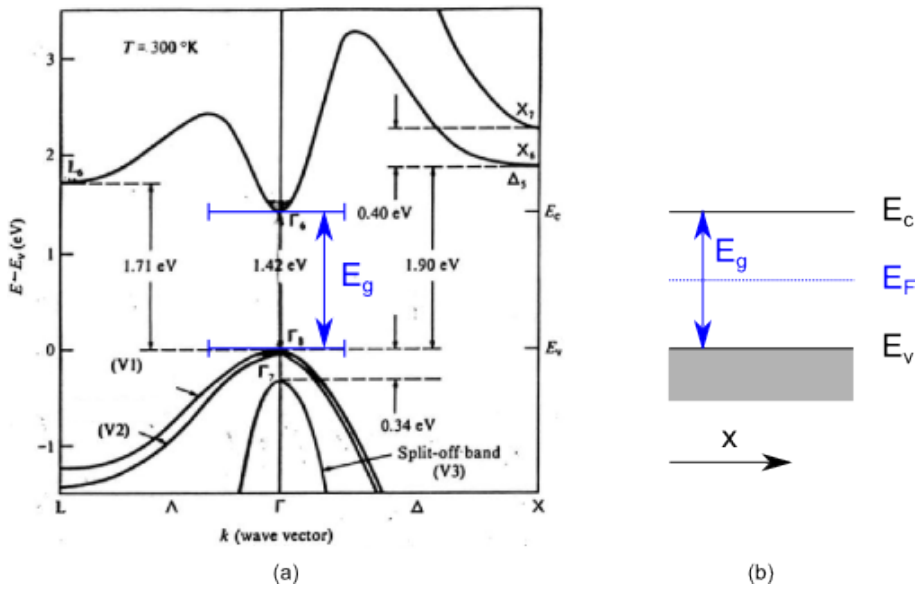


Figure 2.1: *(a)* Important axes of 3-dimensional band structure of GaAs in k-space [25]. *(b)* Simple band diagram as a function position, where the value of the energy gap is taken as the smallest energy gap from *(a)*

hole transport to the metal, as illustrated in Figures 2.2a and 2.2b. This will create a rectifying contact, implying the current is more easily conducted in one direction. Such potential barriers are referred to as *Schottky barriers*.

If the Fermi levels are aligned by accumulation of majority carriers, no depletion region is formed. There will still be a small energy difference as illustrated in Figures 2.2c and 2.2d.,but this barrier easily overcome by charge carriers by a small voltage. The current will thus flow easily in both directions. Such non-rectifying contacts is referred to as *ohmic contacts*.

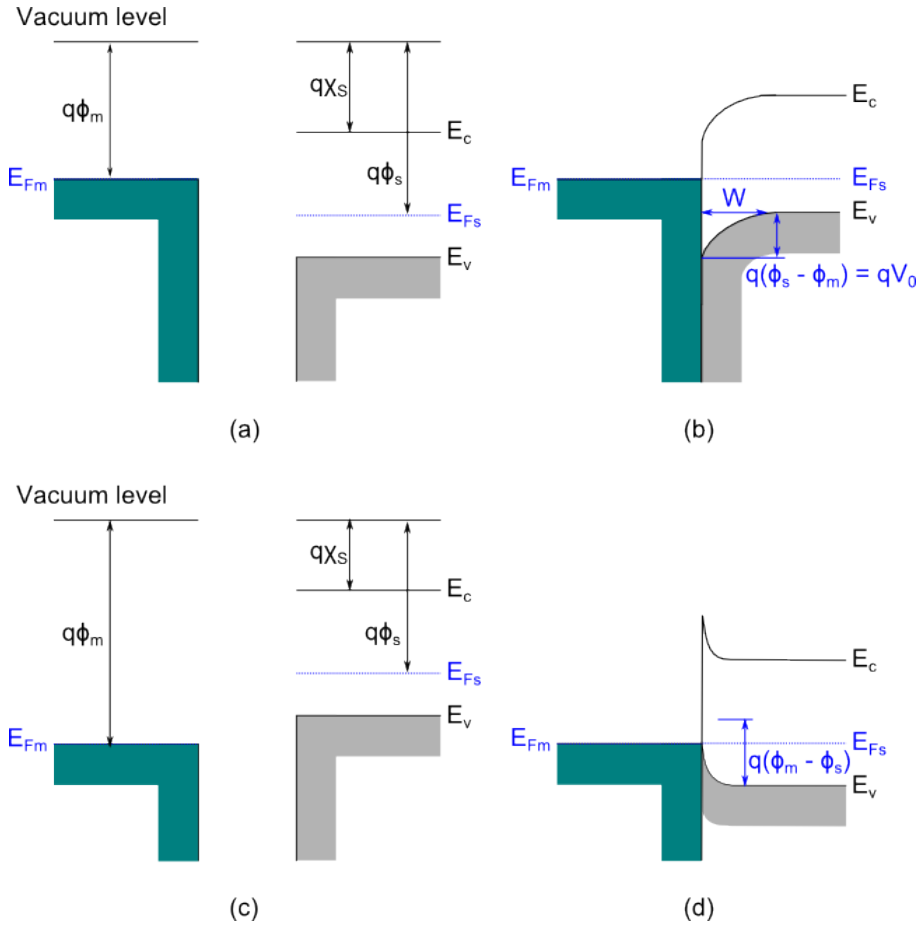


Figure 2.2: Band diagrams of a metal- p-type semiconductor junction demonstrating the formation of: *(a)* and *(b)* a Schottky barrier.*(c)* and *(d)* an ohmic contact.

This ideal metal-semiconductor junction nature is based on the *Schottky-Mott* model, and makes several important assumptions. First it assumes perfect contact between the metal and semiconductor, and secondly that are no effects arising from surface states [26, p13]. At the surface of a semiconductor the covalent bonding is broken, meaning that the boundary atoms will have

unpaired electrons, so called dangling bonds. To minimize the free energy of the surface, the surface will undergo *relaxation* and *reconstruction*, In terms of band theory, this has the effect of introducing new surface and interface states in the middle of the bandgap [1].

In the *Bardeen* model the metal-semiconductor junction is modelled with a thin isolating layer between the metal and the semiconductor. By also including the charge arising from interface states and requiring electrical neutrality for zero bias, the barrier height can be described in the simplest form as [26, p. 20]

$$\Phi_B^0 = \gamma(\Phi_M - \chi_S) + (1 - \gamma)(E_g - \Phi_0) \tag{2.3}$$

where Φ_B is the barrier height, χ_S is the electron, E_G is energy gap in the semiconductor, Φ_B^0 is the barrier height attained for the case of flat bands, and

$$\gamma = \frac{\epsilon_i}{\epsilon_i + q\delta D_s} \tag{2.4}$$

where ϵ_i is the electrical permittivity of the isolating layer, δ is the length if the isolating layer, D_S is the density of surface states in the semiconductor. From this expression we see that if we let $D_S \to 0$ we get $\Phi_B^0 \to \Phi_M - \chi_S$, which is the same result has predicted from the Schottky-Mott model. This scenario is therefore referred to as the *Schottky-Mott Limit*. If we let $D_S \to \infty$ we get $\Phi_B^0 \to E_g - \Phi_0$, which is referred to as the *Bardeen limit*. In this limit the barrier height is independent of the difference in work functions between the metal and semiconductor, as illustrated in Figure 2.3. This scenario also referred to as *Fermi level pinning*, as the Fermi level is the semiconductor is said to be "pinned" by the high density of surface states.

The Bardeen model makes the assumption that the surface states of the semiconductor is not affected by being put into contact with a metal. Tung et al. argues that such an assumption is too simple to capture the true nature of the contact, as this intimate contact is bound to affect the orbitals around surface atoms, thus creating new surface states dependent on the interface chemistry[27]. They therefore argue that a more realistic model should include a quantum mechanical treatment of the surface.

2.1.5 Ideal rectifying behavior

The effect of applying a voltage over a metal-semiconductor junction can initially be found by assessing the simple band diagrams. By applying a negative voltage to the semiconductor relative to the metal, the electron energies in the

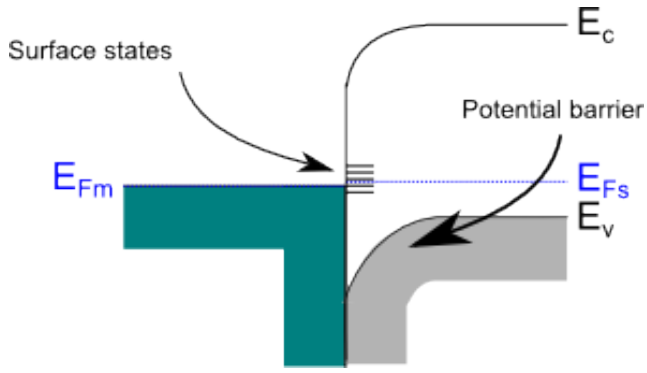


Figure 2.3: Band diagram illustrating Fermi level pinning in the Bardeen limit. The surface states in the middle of the band gap cause band bending at the surface, creating a potential barrier regardless of position of metal Fermi level.

semiconductor is raised as the electrostatic potential gets larger. This has the effect of raising semiconductor Fermi level relative the metal. For a p-type semiconductor this raises the potential barrier at the junction by an amount equal to the applied voltage, as illustrated in Figure 2.4a. For this case the junction is said to be in reverse bias. If the voltage is applied with the opposite sign, the potential barrier is lowered as seen in Figure 2.4b. In this case the junction is said to be forward biased.

There are various ways for a charge carrier to be transported across the potential barrier at the metal-semiconductor. The most important mechanisms are the emission over the top of the barrier and the quantum mechanical tunneling through the barrier. Recombination inside and outside the depletion regions will also contribute to the current, but these mechanisms are often neglected. Several models exist to explain these mechanisms. In the diffusion theory of Wagner, Schottky and Spenke [26, p. 92], the current is explained in terms of concentration gradients arising from the carrier accumulation at the junction. In this model the rate of transport is limited by the carrier transport from the bulk to the interface, rather than the actual transport across the junction. Another model is the thermionic-emission model proposed by Bethe [26, p. 94]. In this model the current is explained in terms of carriers gaining enough thermal energy to surpass the barrier. For this model the current is limited by the actual transport across the barrier.

Both these models in their simpler forms lead to *ideal rectifying behaviour*,

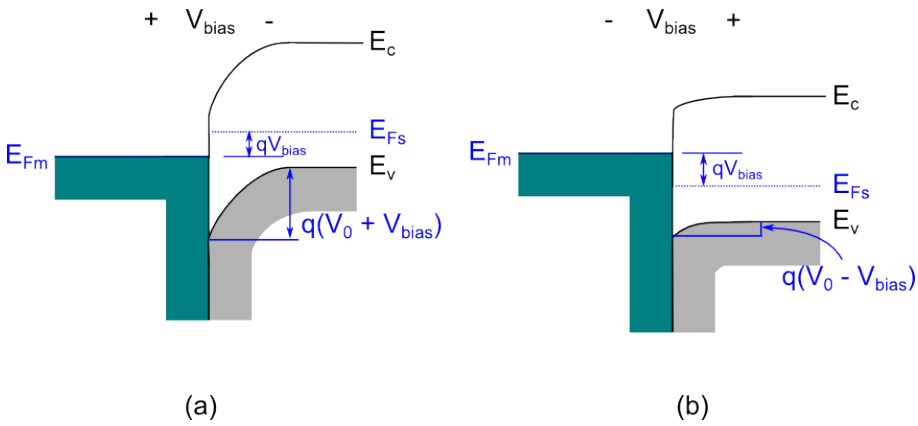


Figure 2.4: Band diagrams illustrating the effect of an applied voltage to a metal-semiconductor junction in the: *(a)* Reverse biased regime. *(b)* Forward biased regime.

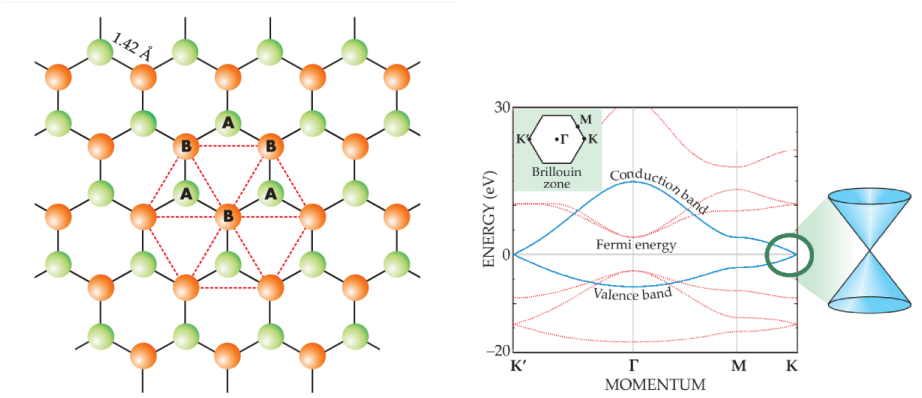
which is the current-voltage relations on the form

$$I = I_0 \left(\exp\left(\frac{qV}{kT}\right) - 1 \right) \tag{2.5}$$

, where Φ_B is the barrier height, V is applied voltage, and I_0 is the saturation current. For this characteristic behavior the current increases exponentially in the forward bias, while saturating at a relatively low value for reverse bias.

2.2 Graphene

Graphene is an allotrope of carbon, consisting of a single layer of carbon atoms arranged in a honeycomb lattice, as seen in Figure 2.5a. Being only one atom thick, graphene is effectively a 2D-material, and electronic transport is thus constrained to two dimensions. Although the first theoretical models of graphene go as far back as 1947 [28], it was along with other 2D-crystals thought to be thermodynamically unstable and thus impossible to create physically. This was disproved when Novoselov and Geim et al. successfully isolated graphene simply by separating graphite sheets using tape [4]. The stability of graphene was initially credited to a gentle rippling of the graphene in a third



(a) (b)

Figure 2.5: *(a)* Illustration of the honeycomb lattice in a graphene layer [29]. *(b)* Band structure of graphene. CB and VB intersect at the **K** points in reciprocal space, where the bands can be seen as two cones intersecting at one point [29].

dimension, as well as the small size of flakes. Later studies have however concluded that graphene owes its existence to the strong carbon-carbon bonds and π orbitals [7].

While graphene has a host of interesting properties like record stiffness and heat conductivity at room temperature [7], it is mainly the electrical properties that is of interest for this thesis. As seen in Figure 2.5a, the honeycomb lattice can be reduced to two triangular sub lattices, which give rise to the band structure depicted in Figure 2.5b. Put in simple terms, due to each carbon atom having an unpaired electron in this structure, these electrons gather in so called π and $\pi*$ orbitals which constitute the VB and CB. These orbitals are forbidden to overlap, but touch at six points in the $E - K$ relation of graphene [29]. These points are referred to as *Dirac points* or *Neutrality points*. This implies that graphene is a zero-overlap semimetal, but it is also often referred to as zero-gap semiconductor.

An unique property of the π orbital is the approximate linearity as it approaches the Dirac points[8],

$$E(k) = \hbar v_F |k| \tag{2.6}$$

, where $\hbar$ is the reduced Planck's constant, v_F is Fermi velocity[3], and $|k|$ is wave vector close to the Dirac point. Recalling that the energy of relativistic particle is given by

$$E = \sqrt{m^2c^4 + p^2c^2} \tag{2.7}$$

, where m is the rest mass of the particle, p its momentum, and c its velocity, we see that the linear energy dispersion in graphene actually implies that electrons behave as zero rest mass, relativistic particles described by the Dirac equation. They are therefore often referred to as Dirac fermions.

Graphene also exhibits excellent electron transport properties, in the forms of a very high electron mobility[4] attainable at room temperature. This is thought to be the result of Dirac fermions being more unlocalized than conventional electrons, thus behaving more like waves than particles. This allows the current to remain in the ballistic regime[5]. In suspended, free-hanging graphene, electron mobility can be as high as 200 000 $\frac{\text{cm}^2}{\text{Vs}}$ [9]. Being a 2D-dimensional material, graphene is however strongly influenced by its substrate, which typically limits the mobility significantly. On amorphous SiO_2 the mobility is reduced to around 10 000 $\frac{\text{cm}^2}{\text{Vs}}$ [8].

Another fascinating property of graphene is its pronounced ambipolar field effect. By applying a gate voltage to the graphene, induced concentrations of both holes and electrons have been demonstrated up to 10^{13}cm^{-3}, while still retaining a mobillity in excess of 10000 $\frac{\text{cm}^2}{\text{Vs}}$ [4]. This implies that graphene in effect has a tunable Fermi level, and the conductivity (resistivity) of graphene is seen to vary significantly as a function of gate voltage, as seen in Figure 2.6. When the Fermi level is at the Dirac point, which is ideally the case for a gate voltage of zero, graphene is said to be intrinsic, and conductivity (resistivity) is very low (high) due to a very low density of states. If the Fermi level is raised via application of a gate voltage to the CB, an excess of electrons are induced, and graphene becomes capable of conducting a current characterized by electrons in the conduction band, similarly to a n-doped semiconductor. Reducing the Fermi level to the VB through applying a gate voltage of opposite sign will similar induce a concentration of holes, and the current will behave like in a

[3]Fermi velocity - the velocity of an electron at Fermi energy.

[4]Electron mobility: Average particle drift velocity per unit electric field, $\mu_n = -\frac{<v>}{E}$.

[5] Ballistic transport - Current transport regime where the carriers only experience scattering by the confining walls. In this regime electron transport is dictated by wave physics, and unlike ohm's law, the resistance is independent of length of the sample.

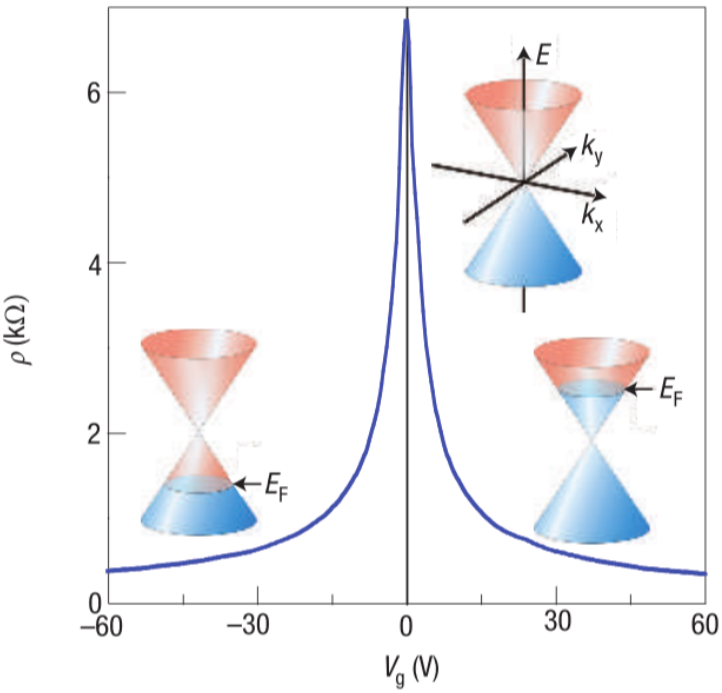


Figure 2.6: Demonstration of the ambipolar field effect in graphene. The graph plots the resistivity of a graphene field effect device with a 300 nm SiO_2 layer as dielectric, as a function of applied gate voltage. The insets indicate how the position of the Fermi level is changed with the gate voltage, making graphene behave as a p-doped (n-doped) semiconductor at negative(positive) gate voltages. [30]

p-doped semiconductor. Graphene can thus be thought of as a semiconductor with a doping concentration[6] tunable by a gate voltage.

2.2.1 Graphene visibility

One of the reasons that graphene was not discovered until recent times is its poor visibility [30]. Although graphene is probably created every time someone uses a pencil, it is extremely difficult to identify single layer flakes amidst the substantially larger amount of thicker graphite flakes. Although graphene is visible to electron, atomic force, scanning tunneling microscopes, all of these are inefficient at finding graphene flakes due to the low throughput at the required resolution, or an absence of a clear signature of a single-layer graphene [31]. One of the key factors in graphene discovery was the usage of a 300 nm SiO_2. At this thickness SiO_2 exhibits a combination of blue and purple contrast, where single-layer graphene becomes visible in optical microscope due to a feeble contrast difference, as seen in Figure 2.7. Only a 5 % difference in thickness of the SiO_2 can make single-layer graphene flakes completely invisible [30], though studies have shown that graphene can be made more visible on SiO_2 thicknesses by utilizing filters [31].

Another technique found to be usable in identifying graphene is the usage of Raman microscopy[7], as it has been showed that the Raman spectrum of graphene clearly evolves with the number of layers [32].

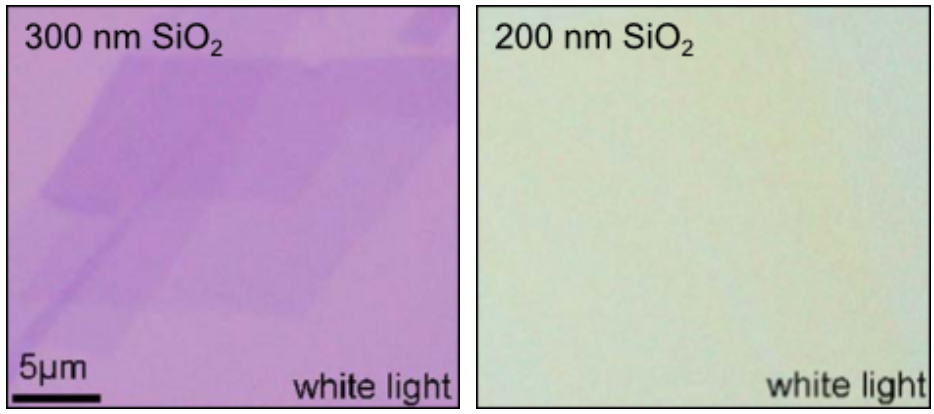
2.2.2 Graphene fabrication

Due to its host of interesting properties and possibilities for different applications, there are numerous methods used and developed for fabrication of graphene. For graphene intended for optoelectronic applications, the two most common fabrication methods are exfoliation and Chemical Vapor Deposition (CVD) (Section 2.4).

Exfoliated graphene refers to graphene created by mechanical exfoliation or cleaving of flakes from graphite. This was the original method used in the first isolation of graphene [4], and is generally regarded as the method

[6] It should be kept in mind that doping by definition refers to tuning the carrier concentration of a semiconductor through introduction of foreign atoms, and that these foreign atoms give rise to other important effects not present in graphene.

[7] Raman spectroscopy - Study of the inelastic scattering from illumination of a sample using a monochromatic laser with wavelengths in near infrared, visible, or near ultraviolet spectrum. This gives information on the low-frequency rotational and vibrational modes of the sample.



(a) (b)

Figure 2.7: Comparison of optical microscope images of single-layer graphene on *(a)* 300 nm SiO_2. *(b)* 200 nm SiO_2 [31].

that produces the best quality graphene. The highest reported mobility in graphene was reported on suspended exfoliated graphene [9]. An exfoliation normally involves the repeated peeling of small mesas of graphite, which is then transferred to a substrate, for example by rubbing a bit of tape on the surface. Single-layer or Few-layer graphene is then located by optical microscope and/or Raman spectroscopy.

The CVD fabrication of graphene has in the recent years emerged has an important method for preparation and production of graphene, which can partly be credited to its potential for industrial scale-up [33]. In a CVD process graphene is grown by surface-catalyzed reaction on a metal surface. While a variety of metals can be used, the most common include Ni and Cu, where Cu is often regarded as the most efficient catalyst. This is credited to the low carbon solubility in Cu, which allows for a greater portion of single-layer graphene. To utilize CVD-grown graphene for electronic applications, the metal must be removed and the graphene transferred to wanted surface. This is normally done by etching away the metal, and transfer the graphene using Polymethyl Methacrylate (PMMA) as a scaffold. The introduction of PMMA is however a disadvantage in terms of quality, as PMMA is known to adhere to the graphene surface and affect its electrical properties [34].

2.3 GaAs

GaAs is a compound semiconductor consisting of Ga from the periodic system group III and As from group IV. GaAs is therefore referred to as a III-IV semiconductor. It was originally assessed as a candidate for electronic devices with the discovery of the transistor in 1947 [35], but was surpassed by Si, because of the easier fabrication and native oxide of Si. Compared to Si, GaAs has some distinct advantages. Firstly it has higher electron mobility and electron saturated velocity, making it more efficient for switching operations, as internal charge can respond quicker to external potentials. This makes GaAs a better suited candidate for high frequency applications.

Moreover, GaAs is a direct band gap semiconductor, opposed to Si, which has an indirect band gap. A direct gap semiconductor has its conduction band minimum (CBM) located directly over the valence band maximum (VBM) in k-space, or in other words the CBM and VBM have the same k-vector, while the opposite is true for indirect gap materials [1]. Examples of the energy bands plotted for direct and indirect gap materials are shown in Figure 2.8. In practice, this means that electron excitation from valence band to conduction band in indirect gap materials is dependent on interaction with the lattice, as a change in electron k-vector, i.e. momentum is required in the transition. This is not the case for direct gap materials, making GaAs a better candidate for optoelectronic applications like solar cells and lasers.

2.3.1 GaAs contacting

Fermi level pinning is an especially prominent issue for GaAs, because of its high density of surface states [35]. Making ohmic contacts to GaAs is therefore notoriously difficult, as the barrier height in junction is relatively insensitive to the metal used.

To obtain good quality contacts to GaAs, a contact material also needs to have good adherence to the GaAs surface, and be stable and resistant to oxidation and corrosion. In practice, all these criteria can not be met for a single metal. It is therefore common to utilize a stack of metal layers. A typical ohmic contact scheme for p-type GaAs is Pt/Ti/Au [35, p. 200], where Pt ensures good electrical behaviour, Au optimizes the outside contact performance, and Ti acts as an adhesion and diffusion stop-layer to hinder Au atoms diffusing into the the Pt layer.

Fabrication of GaAs contacts should also include a surface treatment step, as presence of oxides on the GaAs surface will deteriorate the quality of the

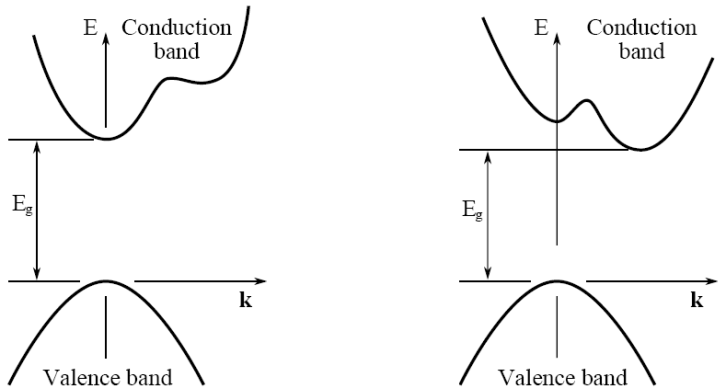


Figure 2.8: Illustration of band diagram in k-space for a : *(a)* direct gap and *(b)* indirect gap semiconductor [1].

contact. Because of its high surface density, the GaAs surface is very reactive, and will form a native oxide in contact with air in the manner of minutes. To obtain ohmic contact, it is therefore paramount to minimize the time between surface treatment and metal deposition in contact fabrication process.

Metal-nanowire junctions

One of the prominent features of ideal rectifying behavior, is the prediction of a bias independent saturation current in the reverse bias regime. In the scenario where a piece of semiconductor nanowire is contacted with a metal in both ends forming two Schottky barriers with opposite orientation, this implicates that only the low saturation current would be conductible, as one Schottky barrier will always be reverse biased. This is generally not observed in semiconductor nanowires, which typically display a non-saturating currents [36]. There are several theories proposed to deal with this in literature.

Zhang et al argues that thermionic emission model fails to explain the *I-V* behavior of semiconductor nanowires because of the absence of tunneling, which they claim to be the dominant component in the reverse bias current for low-dimension systems [37]. They suggest that for a reverse bias and intermediate temperature, the current can be explained in terms of the *thermionic field emission theory*. This model allows for both tunneling (field emission) and

thermionic emission, and predicts a current-voltage relation[26, p. 113] as

$$I\left(V,\Phi_B\right) = -I_{sr}\left(V,\Phi_B\right)\ \exp\left(V\left(\frac{q}{kT}-\frac{1}{E_0}\right)\right) \tag{2.8}$$

, where I_{sr} is a slowly varying function of applied bias, and E_0 is a parameter from tunneling theory.

On the other hand, Chiquito et al. argue that a semiconductor nanowire can be explained in terms of a modified Thermionic emission mode [38] They claim that the thermionic field emission model proposed by Zhang et al. is only applicable in heavily doped semiconductors where the tunneling probability is greatly increased.

A quantitative analysis of 2-probe devices of the same type of nanowire utilized in this thesis was attempted by another master's thesis [39]. In this thesis the I-V behavior is found to be in accordance with the behavior predicted from the thermionic field emission model.

2.3.2 Graphene contacting

2.3.3 Graphene - semiconductor junctions

The GPSC-junction has been studied for many types of semiconductors, and the formation of a Schottky barrier at the interface is well established [23, 40, 41]. This is generally explained by graphene acting as a metal at the junction, so that the GPSC-junction can be approximated by a Metal-Semiconductor junction (MSC-junction). However, an important difference is that while the Fermi level in a metal will remain unchanged upon contacting, the Fermi level of graphene is expected to shift upon contacting due to the charge induced at the interface. This is due to the relatively low density of states for graphene around the Fermi level, as opposed to metals [23].

Zhong et al. proposes a Schottky-model modified with a floating Fermi level to describe this behavior [42], and predicts that this causes the barrier height to be lower for a GPSC-junction than for a MSC-junction. This is illustrated in Figure 2.9.

The current transport across the GPSC-junction is in most studies explained in terms of a thermionic emission model,

$$J(T,V) = A^*T^2\exp\left(-\frac{q\Phi_B}{kT}\right)\exp\left(\frac{qV}{\eta kT}-1\right) \tag{2.9}$$

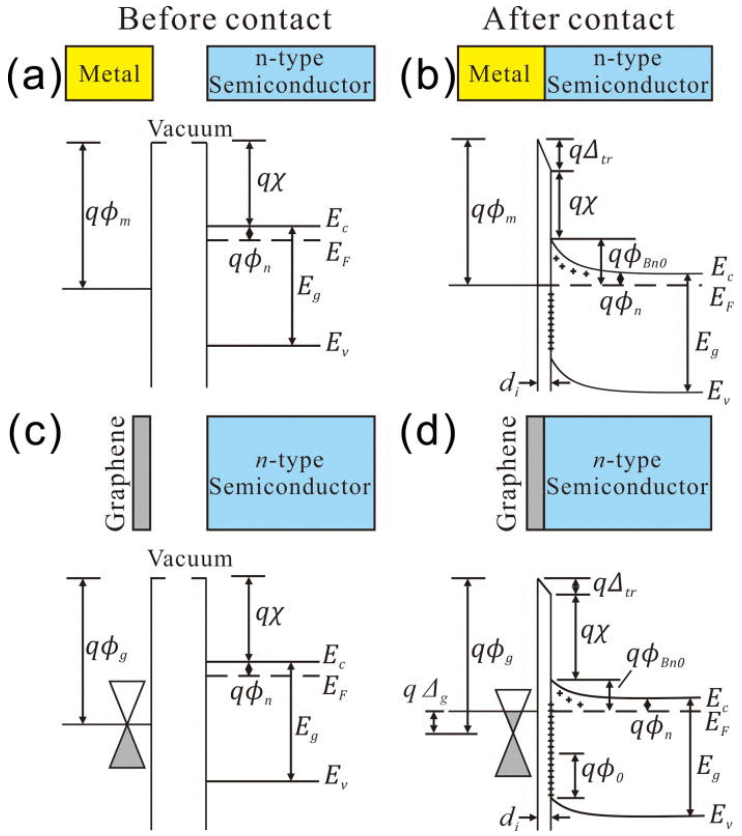


Figure 2.9: Simplified band diagrams illustrating the difference between the graphene-semiconductor *(a)* and metal-semiconductor junction *(c)* before and after being brought into contact *(b)*-*(d)* in the presence of surface charge and a thin isolating layer. For the graphene-semiconductor junction the resulting barrier height is lower due an induced change in the graphene Fermi level [42].

, where A^* is the Richardson constant, T is temperature, Φ_B is the zero bias barrier height. Deviation from ideal rectifying behavior is captured in the parameter, η, and is generally attributed to thermally assisted tunneling, generation-recombination current and bias dependent barrier height. This model is justified by the appearance of linear behavior for a logarithmic plot for the forward bias regime, which is in accordance with the prediction from thermionic emission. Using the slope in the logarithmic plot, the barrier height can be extracted. If one further assumes the Schottky-Mott limit to be valid, $\Phi_B^0 = \Phi_M - \chi_S$, the barrier height can be used to calculate the work function of graphene using the electron affinity of the semiconductor [41].

A trend observed for the GPSC-junction is the higher current in reverse bias than predicted from the thermionic emission model. Tongay et al. have demonstrated that while a significant reverse bias current is present in a GPSC-junction, this is not the case for a graphite junction [41]. They propose that this can be credited to the graphene Fermi level being shifted by the applied bias voltage, unlike in graphite where the Fermi level will be fixed. In response to a large reverse bias, the graphene Fermi level will therefore increase, decreasing the barrier height and thus increasing the current. This effect should also be visible for higher voltages in the forward regime in the form of a slightly decreased current, but here the effect will be difficult to distinguish from other resistance effects coming into play at a high current.

Graphene - Silicon

Graphene - silicon is probably the most studied graphene-semiconductor junction [40, 43, 44]. Silicon has the advantage of having a surface that is easily saturated, thus reducing interface states and Fermi-level pinning. Studies have shown while a silicon surface with dangling bonds will modify the orbitals of graphene, this is not case for a silicon surface passivated with hydrogen, where the electrical properties remain unperturbed [45]. The system is therefore well described by the Schottky-Mott limit, where the barrier height is only dependent on the difference in work function between graphene and the semiconductor. This makes the graphene-silicon junction ideal for investigating the effect of shifting the Fermi level of graphene on the GPSC-junction.

Yang et al. have demonstrated a three-terminal device they call a "barristor" [46], which is essentially a GPSC-junction with a top gate over the graphene. By modulating the gate voltage, they found that a positive gate voltage increases the current for p-type silicon and reduces the current for n-type, which they credit to the Fermi level of graphene approaching or di-

verging from the Fermi level of Silicon. Chen et al. demonstrated a similar device, where an electrolyte gate was utilized [47]. Due to the large dielectric constant of an electrolyte gate, they were able to induce large shifts in the graphene Fermi level with relatively low gate voltages. As seen in Figure 2.10, they were able to observe a transition from almost ideal rectifying behaviour to almost ohmic behaviour, which they credit to the Fermi level of graphene being shifted almost past the Fermi level of silicon, where an ohmic contact is predicted from the Schottky-Mott model (Section 2.1.4).

Graphene - GaAs junctions

The graphene-GaAs junction is not well-studied, and to the author of this thesis's knowledge, there only exists four published studies on the electrical transport across this junction [23, 41, 48, 49].

Tongay et al. have demonstrated Schottky barriers for n-type GaAs on highly oriented pyrolytic graphite (HOGP) [41] and graphene [23]. The work function for HOGP and graphene found from the extracted barrier height using Schottky-mott theory is found to be in accordance with experimental results. But as Tongay et al. points out, the extracted barrier height is on par with the expected barrier height as a result of Fermi level pinning. It is therefore more likely that the graphene-GaAs junction is better approximated by the Bardeen limit.

2.4 Chemical Vapor Deposition - CVD

The CVD process is a method for a deposition of a solid film on a substrate through a chemical reaction of a gas mixture CVD has traditionally been used for depositing thin films by the semiconductor industry due to the low costs and high purity attainable [50, Ch.11], but in recent years the CVD process has been utilized in the fabrication of more exotic materials like nanowires (Section 2.5) and graphene (Section 2.2.2). The essential aspect of the CVD process is that the reactants are introduced in gas form, and these undergo chemical reactions to become film precursor. The chemically reactions should happen as close to the substrate surface as possible, and should ideally be surface catalyzed, as this produces the highest film quality [50, p. 266]. A schematic stepwise overview of the CVD process is shown in Figure 2.11.

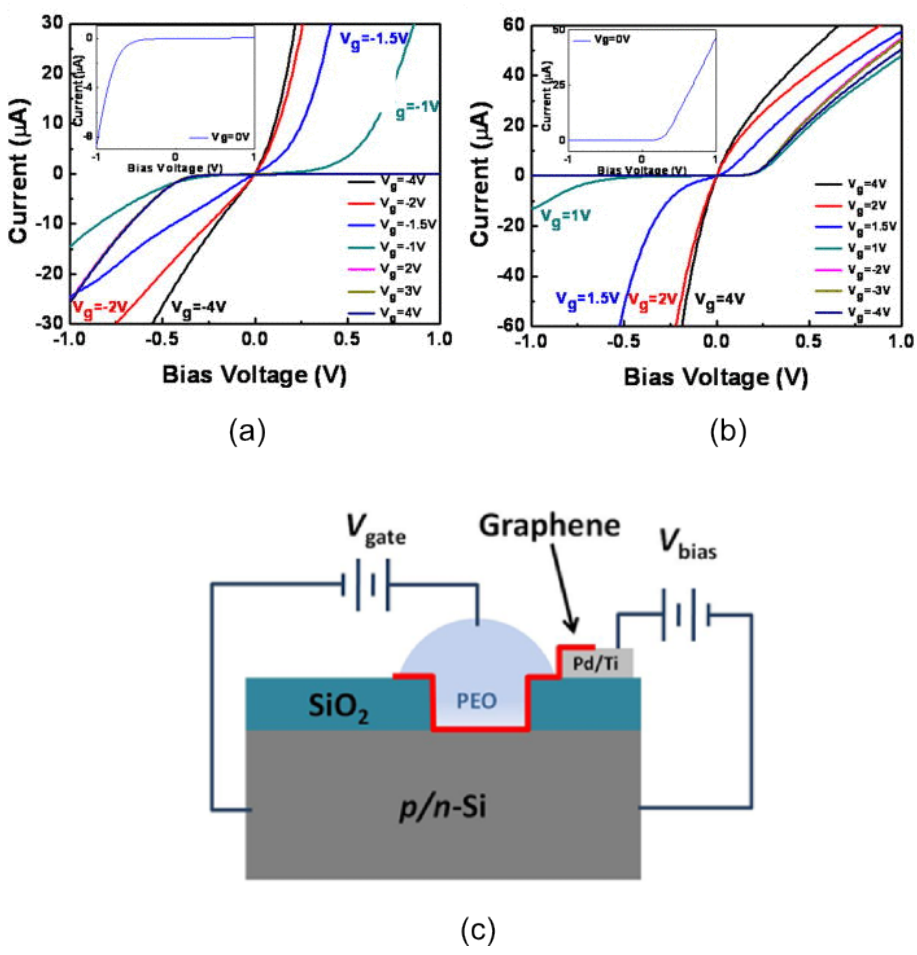


Figure 2.10: $I-V$ curves obtained from a graphene - silicon junction as different gate voltages induced in an electrolyte gate for *(a)* p-type silicon. *(b)* n-type silicon. *(c)* Schematic overview of the device structure [47].

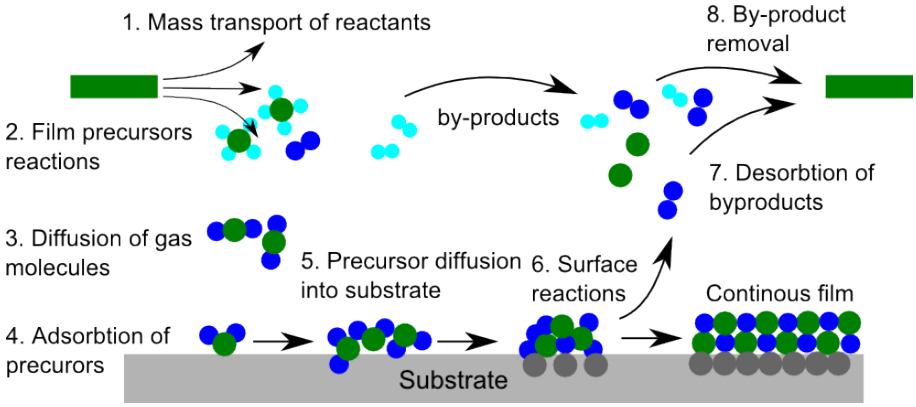


Figure 2.11: Schematic overview of the reaction steps taking place within a typical CVD-reactor.

2.5 Vapor-liquid-solid growth mechanism - VLS

The *vapor-liquid-solid mechanism* is a well-established growth mechanism for fabricating nanowires by a form of CVD [51, 52]. Unlike conventional CVD, where the gas reactants adsorb to the substrate surface to form a continuous film, the VLS method makes use of catalytic droplets to control growth. The droplets act as a preferred site for gas reactants, absorbing atoms both directly and via surface diffusion. This continues until the droplet becomes supersaturated, at which point epitaxial growth[8] commences at the boundary between the catalytic droplet and the substrate. Growth continues as more reactants absorb in the droplet, where they move to the boundary and deposit on the nanowire. The site of growth is thus confined by the area covered by the catalytic droplet, which in effect is the hole size. The nanowire will be uniform in diameter until the length becomes comparable with the surface diffusion length of the reactants, at which point tapering occurs. At this point the nanowire will become broader at the base than at the top near catalyst droplet, as most of the reactant atoms deposit before reaching top through a direct vapor solid - VS-growth. This process is illustrated in Figure 2.12.

GaAs nanowires have traditionally been grown using Au as catalyst droplet [53],

[8] Epitaxial growth or epitaxy: crystal growth on a crystalline substrate where the new crystal maintains the structure and orientation of the substrate [1, p. 18].

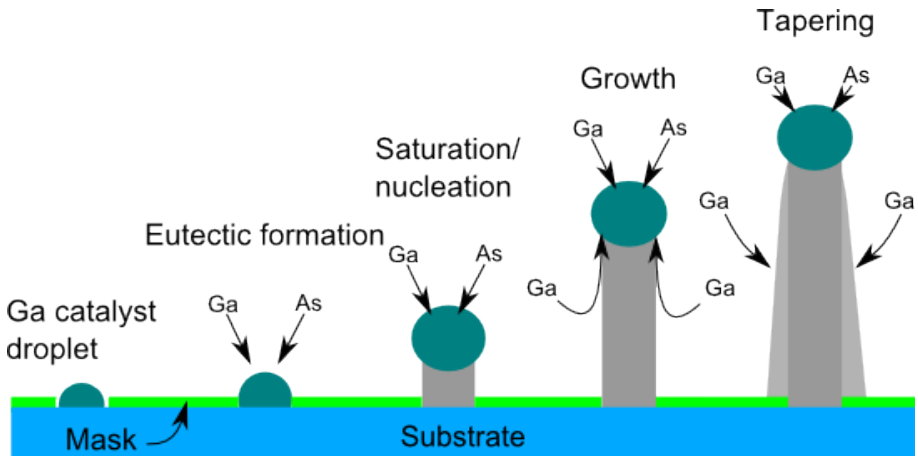


Figure 2.12: Schematic overview of a Ga-assisted vapor-liquid-solid GaAs growth mechanism. Ga catalyst droplets form in the holes of the prepatterned mask, and absorb Ga and As atoms. When the droplet becomes supersaturated, Ga and As atoms go to the boundary between the droplet and the substrate and deposit as epitaxial GaAs. The growing nanowire is uniform in diameter until its length surpasses the surface diffusion length, at which point tapering is observed.

often referred to as Au-assisted VLS. In 2008 it was shown that GaAs nanowires can be grown Ga- or self-assisted, by forming Ga droplets at predefined spots using a mask [54]. This has since been the most popular method for fabricating GaAs nanowires, as extrinsic metal particles are generally not desired in nanowire devices. The presence of Au in GaAs nanowires is thought to introduce efficient non-radiative recombination centers[9], making Au-assisted GaAs nanowires less desirable for optoelectronic applications [55].

Doping is conducted by introducing a gas flux of doping specimens during the growth process. The incorporation of doping atoms is currently not well understood, as the exact dopant concentrations in nanowires are generally unknown and difficult to measure. Growth parameters are therefore based on data from the growth of planar semiconductors. The system for VLS-growth utilized in this thesis, self-catalyzed GaAs doped with Be to achieve p-type,

[9]Non-radiative recombination center: An energy level in the band gap, allowing excited carriers to relax their energy without emitting a photon.

have been studied by Casadei et al. [56]. The study concludes that the incorporation of Be atoms happens mainly through VS-growth at the nanowire sidewalls, followed by diffusion toward the core. Due to the high diffusion mobility of Be atoms in a GaAs structure, they argue that homogeneous dispersion of dopant atoms can achieved for high dopant concentrations. It will therefore be assumed the nanowires in this thesis have a uniform doping concentration.

2.6 Molecular beam epitaxy - MBE

Molecular beam epitaxy is a technique for epitaxial growth by introducing the source material as molecular beams on a heated substrate in ultra-high vacuum, $10^{-10} - 10^{-11}$ Torr [50, p. 291]. A schematic of a MBE system is shown in Figure 2.13. The source materials are separated from the main chamber in *effusion cells*, where they are heated until evaporation. The flux of each source material can then be accurately adjusted through controlling the cell temperature, and a mechanical shutter. This provides an excellent control of the ratio between the source materials, making MBE a well-suited method for deposition of compound semiconductors such as GaAs.

The vacuum level of the main chamber ensures that the mean free path of the source atoms is long enough for the atoms to reach the substrate without undergoing any chemical reactions. Upon reaching the surface, epitaxial growth occurs by atoms diffusing around until they find an empty lattice point, or attach to the side of a two-dimensional sheet. The key for achieving efficient and defect-free growth is thus to maintain a substrate temperature where the surface mobility is high, but not high enough to cause too much desorption from the surface. The reaction temperature is usually 500 to 900 °C. For compound semiconductors it is important to consider the difference in atom properties on the substrate surface. For GaAs growth, As atoms will generally experience more desorption, meaning a relatively higher As flux is required to obtain the desired ratio [35, p. 40].

To ensure epitaxial growth, a very slow growth rate must be utilized, and MBE growth rates are often given as monolayers per second, ML/s.

2.7 Scanning electron microscopy - SEM

A Scanning Electron Microscope (SEM) is a type of electron microscope, an instrument that uses a focused high energy electron beam to scan the surface of a sample and produce images on the nanometer scale. SEM is a very versatile

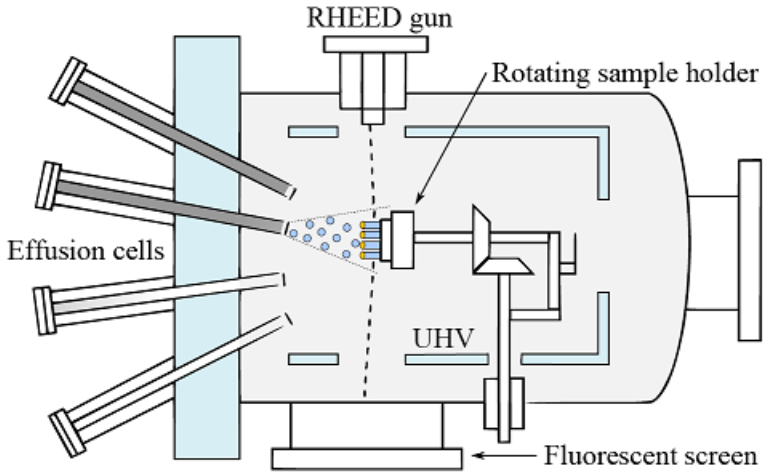


Figure 2.13: Schematic of a typical MBE system, showing effusion cells, main chamber, and RHEED system for in-situ characterization during growth [57].

and popular instrument in material sciences, as electrons are well suited for characterization of structure and chemical characterization of surfaces due to their limited escape depth [58, p. 243]. According to the de Broglie theory electrons can be given wavelength according to

$$\lambda = \frac{h}{\sqrt{2mE}} \tag{2.10}$$

, where h denotes Planck constant, m electron mass, and E is the kinetic energy of an electron. At 50 keV this equals less than 0.1 Å, a value substantially lower than the wavelength of visible light at around 400 - 750 nm. Electrons can therefore be scattered by and provide information on smaller features than visible light, which is the main motivation for utilizing electrons in microscopy.

The interaction of an electron beam with matter gives rise to a multitude of different signals, which can analysed for both structural and chemical information about samples. The most important signals for a SEM is secondary electrons (SE), back-scattered electrons (BSE), and characteristic X-rays. Secondary electrons originate from the sample, and not from the electron beam itself [59, p. 60]. These are electrons that are knocked out from the valence

and conduction bands of the atoms in the sample, and then emitted from the surface. They will typically have energies less than 50 eV, and as a consequence they are only able to escape the sample if they are close to the surface. The SE-signal can thus give structural information about the surface, as the intensity will be a function of surface topography. Back-scattered electrons are electrons from the beam that scatters elastically[10] with atomic cores in the material. The amount of BSE will depend on the atomic number, as heavier atomic cores cause more back-scattering. The BSE is thus often called Z-contrast[11]. Characteristic X-rays arise from primary electrons knocking out electrons from the inner shell of sample atoms, causing the atom to transfer an electron from an outer shell to fill the hole and send out surplus energy in form of an X-ray. These X-rays will have energies corresponding to differences in the electron energy levels, and can therefore be used to identify the elements present in the sample. The interaction volume of a SEM is shown in Figure 2.14.

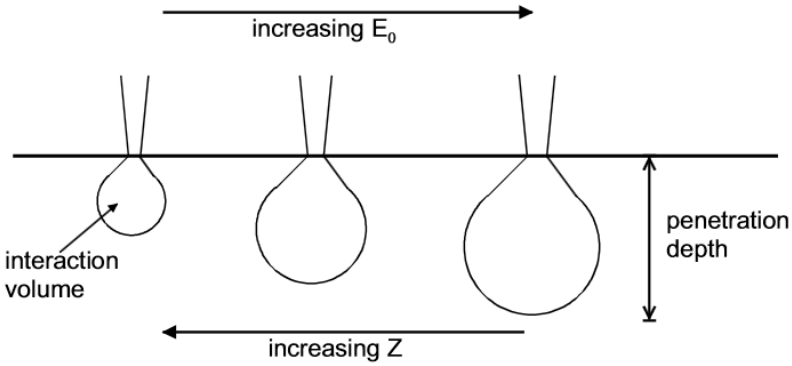


Figure 2.14: Interaction volume in a SEM as a function of increasing electron energy or decreasing atomic number of sample [60, p. 130].

The image in a SEM is obtained by moving the beam across the surface in a raster manner, and detecting the intensity arising from each position in the raster scan. These intensities are then visualized in an image using the SEM

[10] In practice they do lose a little energy, thereby not justifying the term elastic, which by definition implies a scattering without energy loss. They are called elastic by convention to distinguish them from SE, where the energy loss is more substantial.

[11] Z is normally used as a symbol for atomic number, i.e. number of protons in the core.

software. The images obtained from a SEM is purely digital, and one is dependent on software to get images, unlike in optical microscopes. The electron beam is created by thermal emission or field emission, and the most common electron sources are tungsten filaments or field emission guns. After emission, the electrons are accelerated towards the sample in vacuum. Typical acceleration voltages for the SEM range from 1 kV to 20 kV. The electron beam is then focused through several electromagnetic lenses. These electromagnetic lenses have tunable focal lengths by changing the currents controlling the magnets. The beam is usually focused to a size from 1 - 10 nm, and swept across the surface by a deflecting coil. This is illustrated in Figure 2.15.

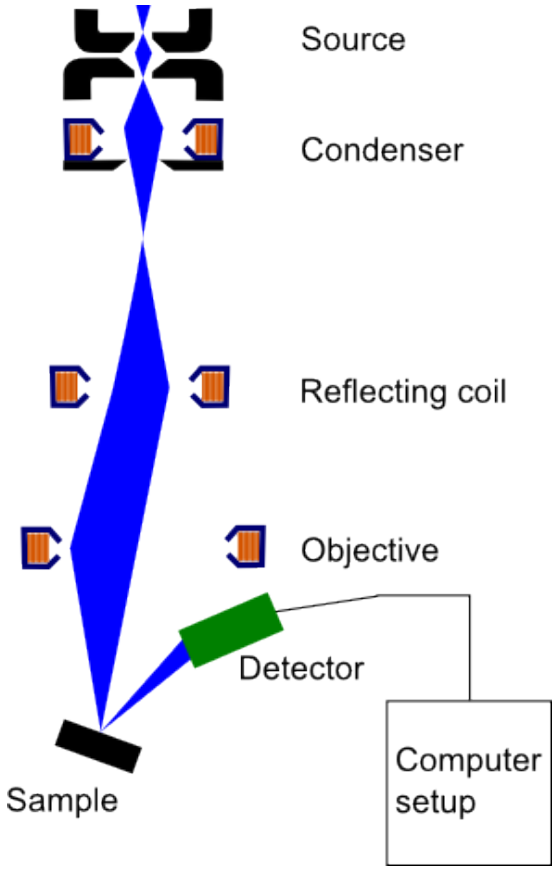


Figure 2.15: Schematic of a beam path in a typical SEM .

A larger magnification in a SEM is obtained by reducing the scan distances in the raster scan, and the obtainable resolution is therefore limited by the spot size achievable. This is in practice limited by aberrations in the lense system and electron source, such as chromical aberrations arising from energy differences in electrons emitted from the source, or astigmatism arising from non-symmetrical electromagnetic lenses.

2.8 Electron beam lithography - EBL

Electron Beam Lithography (EBL) is a technique where an electron beam is used to write patterns with sub-100 nm resolution in a sacrificial layer commonly known as resist. An EBL system is essentially a SEM with added systems for an accurate sample stage and electron beam movement, and most EBL systems can be operated like a SEM. The high resolution in the SEM is then used in the EBL system to create patterns on the nanometer scale. EBL is a direct write method, with the beam moving across the pattern in a sequential manner, unlike photolithography where simultaneous illumination of an entire wafer is possible. This means that lithography can be conducted without the use of prefabricated masks, a great advantage when making unique patterns. However, the same aspect means making large patterns with EBL a very time-consuming process, and EBL is thus considered unsuitable for large-scale industry productions. It is nevertheless very popular in scientific communities due to the high resolution attainable [58, p. 212].

When exposed, the resist will either soften (positive resist) or harden (negative resist), so that we in both cases can selectively remove areas of resist. The resist can then shield underlying structures from subsequent etching or deposition processes. The resist used in this project, PMMA (polymethyl methacrylate), consists of approximately 10 nm long polymer chains that will break upon exposure from the electron beam, leaving shorter chains that are soluble to IPA.

EBL patterns are made by designing digital masks in .gds or CAD format. These patterns are then organized in *write fields*, areas defined for writing by the EBL software. Smaller write fields generally result in greater accuracy but longer process time. One of the most important factors in achieving good EBL accuracy is to align these write fields correctly according to sample coordinates. The EBL software typically controls the sample stage using an accurate laser interferometer system. The sample has a predefined three-dimensional coordinate system *(x, y, z)*, and a sample specific coordinate system *(u, v, w)* that can be modified with different origin, rotation and scale relative to the predefined coordinate system. This is illustrated in Figure2.16.

The most common techniques for achieving optimal alignment are *stage movement alignment* and *write field alignment*. Stage movement alignment is conducted by moving the beam and sample inversely relative to each other, so that one ends up on the same spot on the sample, but with the offset between beam and stage movement visible. This offset is then be corrected by scaling the u- and v-axes of the sample specific coordinate system. Write field

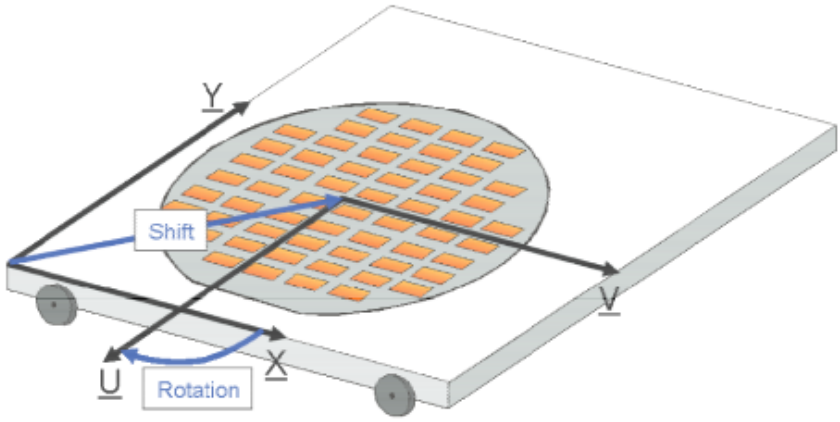
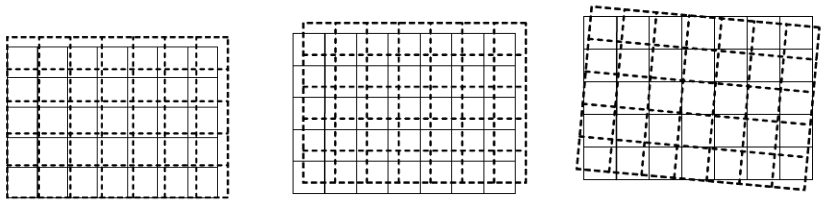


Figure 2.16: Illustration of a stage-sample coordination transformation[61, p. 149].

alignment involves choosing three points in the digital mask. The beam moves to these three alignment marks, and any offset between beam position and the intended sample area can be corrected by scaling the axis of the sample specific coordinate system. This gives a good fit between the pattern and existing sample features used for alignment. However, if the features used for alignment marks have different coordinates than the intended coordinates relative to the pattern, write field alignment will end up distorting the pattern. The consequences of incorrectly aligned write fields are illustrated in Figure 2.17.



(a) (b) (c)

Figure 2.17: Figure demonstrating how incorrectly aligned write fields affect patterning. *(a)* Incorrect size. *(b)* Incorrect position. *(c)* Incorrect rotation angle [57].

Chapter 3

Experimental

In the following chapter the fabrication process and the method for electrical characterization will be presented. A substantial part of this thesis has been devoted to developing a a successful fabrication route for graphene/GaAs nanowire hybrid devices. The starting point for this development was the process for making single nanowire devices developed in earlier theses [57, 62, 63]. Numerous parameters in several processing steps have been tested, but for the convenience of the reader, the following section will only cover the variations deemed most important. All results that impacted the fabrication route have been included in the Results (Chapter 4).

3.1 Overview

For the purpose of obtaining measurable GaAs nanowire/graphene hybrid devices, graphene of two different origins were tested. Due to the different processes associated with transferring each kind of graphene, a slightly different device structure for each device was necessary.

The first of device was made using CVD-grown graphene, and will hereby be referred to as CVD-grown Graphene device (CVDG-device).

For the second kind device, substrates were prepared at NTNU, and then sent to Konkuk University, Korea, where a PMMA-mediated transfer of exfoliated graphene was conducted. Due to the smaller size of graphene flakes transferred in this manner, and an extra process step for contacting the graphene was necessary. These devices will be referred to as Exfoliated Graphene de-

vice (ExG-device). Figure 3.1 shows a schematic diagram of the device structure envisioned for the two devices.

The fabrication process can be summarized in the following general steps that will be elaborated in this section:

1. Sample preparation - Section 3.2
2. Graphene transfer - Section 3.3 and 3.4
3. Contact design - Section 3.5
4. Graphene contacting - Section 3.6 (Only ExG-device)
5. Graphene trimming - Section 3.7
6. Nanowire contacting - Section 3.8

3.2 Sample preparation

3.2.1 Substrate fabrication

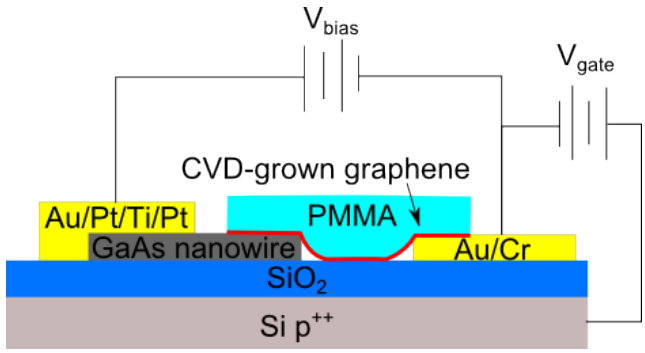
Two kinds of substrates were utilized in this thesis. Both types were prefabricated by Professor Gyu-Tae Kim's group at the Korea University. p++[1] doped Si substrates had either 300 nm SiO_2 or 150 nm Si_3N_4 deposited as an isolating layer via CVD. The doped Si substrate and isolating layer has the purpose of allowing the substrate to be used as a back gate during electrical measurements.

Probe pad and lead pattern were then deposited using two photolithography processes. The contact pads had 50 nm layer of Cr followed by 300 nm of Au deposited. For the lead pattern 10 nm Cr followed by 50 nm of Au was utilized. Cr is used as an adhesive layer, while Au is intended as the conductor.

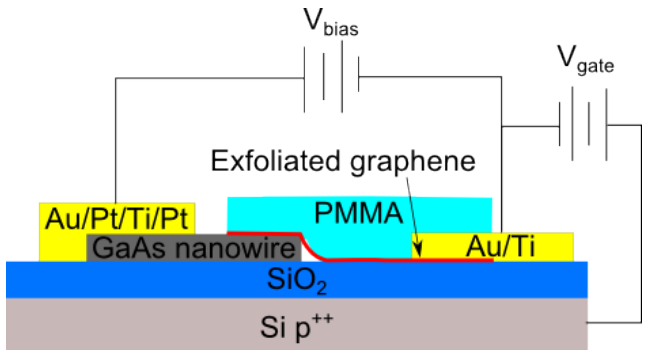
3.2.2 Substrate details

Initially 7.5 x 7.5 mm^2 Si substrates with 150 nm of Si_3N_4 as isolating layer were utilized. These substrates have eight 400 x 400 μm^2 contact pads with lead arms leading into a 100 x 100 μm^2 area. This area is intended for further further contacting by EBL in a 100 x 100 μm^2 write field. These areas will

[1] p++ indicates a high concentration of p-type doping.



(a)



(b)

Figure 3.1: Figure showing the schematic diagram of the envisioned device structure for: *(a)* CVDG-device. For this device the graphene will be resting on top of a Cr/Au contact. *(b)* ExG-device. For this device, the graphene will be contacted with Au/Ti contacts due to the smaller size of the graphene flakes.

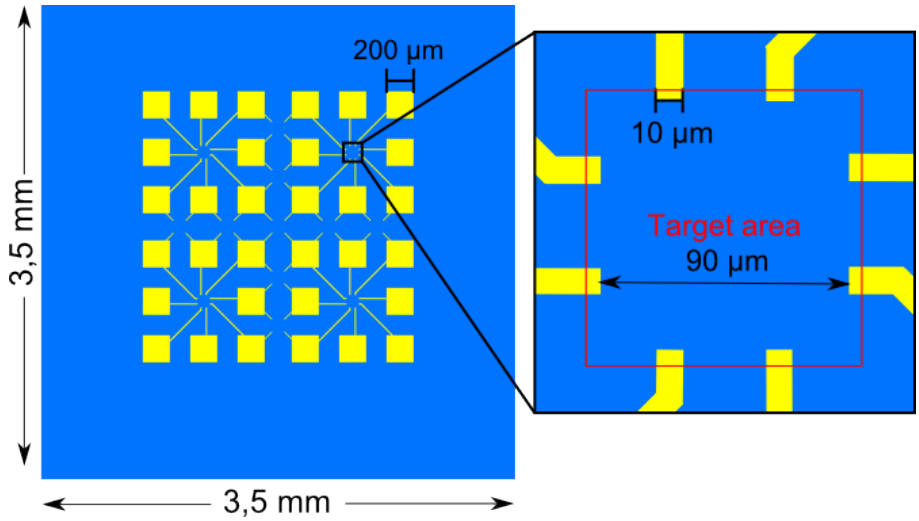


Figure 3.2: Figure showing the dimensions for the SiO_2 substrates. The target area indicated in red is the 100 x 100 μm^2 area intended as write field for the subsequent EBL processing.

from hereby be referred to as the target areas. The size of the substrate and contact pads are designed to be compatible with the photonics lab at NTNU.

Later 3.5 x 3.5 mm^2 substrates with a 300 nm of SiO_2 was adopted. These consists of 32 connect pads measuring 200 x 200 μm^2 leading to 13 100 x 100 μm^2 target areas. Four connected by eight pad arms and nine by four pad arms. This is shown in Figure 3.2. Further dimension details can be found in Appendix A.

3.2.3 Substrate cleaning

The samples were thoroughly cleaned to ensure a clean and even surface for the subsequent lithography process. They were first given a sonication treatment, first for 5 minutes immersed in a beaker with acetone, and then 5 minutes in Isopropyl Alcohol (IPA). The samples were then withdrawn from the beaker, sprayed gently with IPA for 10 seconds, and blow-dried with N_2.

Plasma cleaning was then conducted for 5 minutes, at 90 % power and 50 mbar O_2. This treatment removes carbon and oxide contamination, as

Table 3.1: Cleaning procedure parameters.

Procedure			**Time**
Sonication in acetone			5 min
Sonication in IPA			5 min
IPA spray			10 sec
N_2 blow-dry			-
Plasma cleaning	Power	90 %	5 min
	Gas	O_2	
	Pressure	50 mbar	

well as any potential residuals from the acetone/IPA treatment. The cleaning parameters are summarized in table 3.1.

3.2.4 Nanowire synthesis

The nanowires utilized in this thesis were grown by PhD-student Abdul Mazid Munshi in Helge Weman's group at IET. Ga-assisted (self-catalysed) GaAs nanowires were grown via the VLS mechanism (Section 2.5) in a *Varian Gen II Modular* MBE system equipped with a Ga dual filament cell and an As_4 valved cracker cell.

All devices were made using p-type GaAs nanowires from the same growth batch, with the internal sample number SC369. This was to minimize potential variations in electrical properties arising from slight differences between growth sessions.

Growth was carried out on a p-type Si(111) substrate, which was dipped in HF (5 %) for 5 seconds, rinsed in Deionized water (DI water) and blow-dried with N_2, before being brought to the MBE chamber. First a growth step according the parameters listed in table 3.2 was conducted, which is equivalent to achieving a Be concentration (p-type) of $\sim 3 \cdot 10^{18}\text{cm}^{-3}$ in growth of GaAs thin films. The temperature is then lowered to make the Ga droplet solidify, thus stopping further axial growth. A second growth step is then conducted according to the parameters listed in Table 3.2, which results in only radial growth, effectively growing a shell on the nanowire. The nanowires are then annealed at a temperature of 630 °Cfor 10 minutes, to assist in the diffusion of Be atoms, producing a uniform p-doping.

Table 3.2: SC369 p-type GaAs nanowire growth parameters. *(a)* Parameters used for the core growth process. *(b)* Parameters used for the shell growth process.

(a)

First growth step (core)

Parameter	**Value**
Temperature	640 °C
Ga growth rate	0.6 ML/s
As_2 flux	$5 \cdot 10^{-6}$ Torr
Doping specimen	Be
Be-cell temperature	1010 °C
Growth time	35 min

(b)

Second growth step (shell)

Parameter	**Value**
Temperature	460 °C
Ga growth rate	0.6 ML/s
As_2 flux	$9 \cdot 10^{-6}$ Torr
Doping specimen	Be
Be-cell temperature	1040 °C
Growth time	30 min

3.2.5 Nanowire dispersion

Following nanowire growth in the MBE, substrates were put in a solution of IPA and sonicated. This tears off the nanowires at the base and suspends them in IPA. First the solution containing nanowires was given a light sonication for 10 seconds to ensure a good nanowire dispersion in the solution. The substrates were put on a hot plate at 85 °C. 2 µl of solution was extracted using a micropipette with an adjustable pipetting volume. The solution was partially extracted in a manner such that the droplet is clinging to the tip of the pipette. The tip was then brought almost into contact with the substrate surface at the approximate position of the target areas, making sure the droplet was in contact with both the pipette and the substrate, as shown in Figure 3.3. This ensures

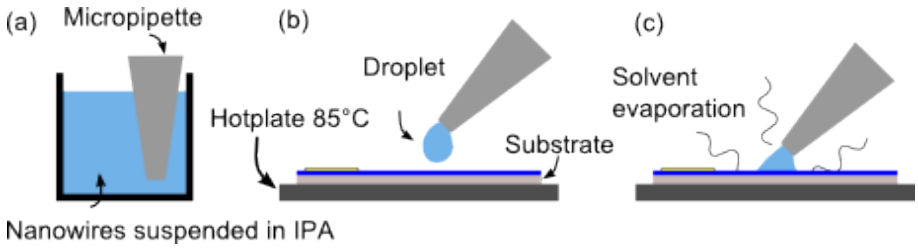


Figure 3.3: Figure illustrating the process used to disperse nanowires. *(a)* Micropipette is used to extract 2 μL of IPA solution containing nanowires. *(b)* Droplet is partially extracted, and brought into contact with intended deposition area. *(c)* The micropipette is held at this position while the droplet is quickly evaporated due to the elevated temperature.

the droplet is fixed at the location of the tip while quickly evaporating due to the elevated temperature. This was repeated until optical inspection showed an acceptable nanowire concentration in the target area, which was usually the case after one to six droplets.

3.3 Graphene transfer - exfoliated graphene

After sample preparation, the substrates were sent to Konkuk University, Korea, where the following process step was conducted by Professor Sang-wook Lee's group.

3.3.1 Graphene dispersion

Small pieces of kish graphite was placed between two bits of scotch tape, and repeatedly pressed together and drawn apart, until only a fine power covered both tape surfaces. This tape was then rubbed against the surface of Si wafer with a 300 nm SiO_2 top layer to transfer exfoliated graphene flakes. Using optical and Raman microscopy, single-layer graphene flakes were identified. Such flakes will generally be roughly 20 μm^2 in size. C4 PMMA[2] was applied by spin coating to act as scaffold for subsequent processing. The Si and SiO_2 layers were then selectively etched away.

[2] 4 % PMMA in chlorobenzene.

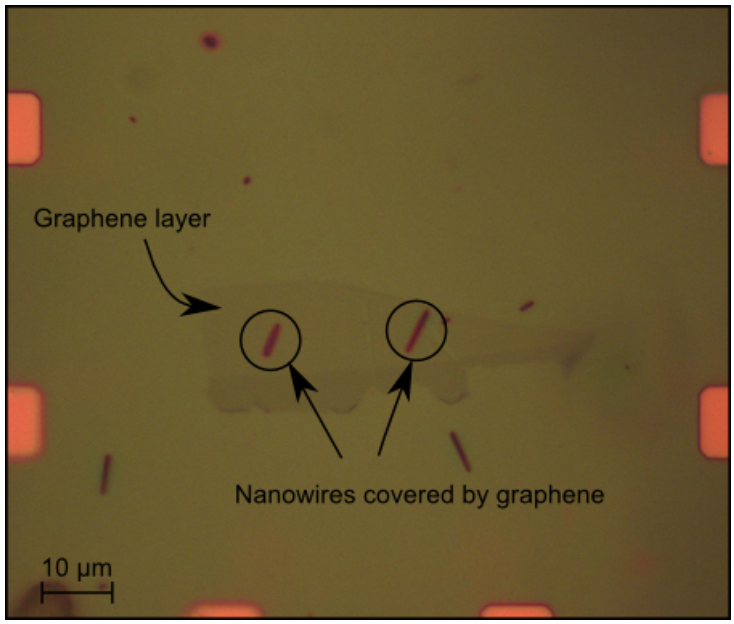


Figure 3.4: Optical microscope image showing one of the substrates received from Konkuk Unversity, Korea after completing an exfoliated graphene transfer. The surface is covered in C4 PMMA.

3.3.2 Surface treatment

The substrates sent from NTNU was then subjected to a surface treatment to remove the native GaAs oxide layer. from the nanowires. This was done by Reactive Ion Etching (RIE) treatment, followed by an exposure to 10 % HCl for 10 seconds. Finally they were rinsed in running DI-water for 30 seconds.

3.3.3 Transfer

The substrates were first placed in a solution of IPA. Using custom built probe operated by vacuum, the exfoliated graphene/PMMA layer was placed on top of suitable nanowires within target areas. The substrates were then dried in room temperature, before finally being sent back to NTNU. Figure 3.4 shows a substrate after undergoing transfer.

3.4 Graphene transfer - CVD-grown graphene

3.4.1 Graphene fabrication and preparation

Two kinds of CVD-grown graphene were tested.

First graphene supplied by Graphene Supermarket in 2011 was tested. This graphene is supplied as a Cu-foil with graphene on both sides. To remove graphene on one side, the Cu-foil was attached to a large Si wafer by caption tape, and treated by plasma ashing at 50 % power in a O_2 gas of 35 mbar pressure for 1 minute. A 200 nm layer of A2 PMMA [3] was then applied by spin coating on the graphene side to act as a scaffold for the subsequent transfer.

Secondly graphene supplied by Professor Keun-Soo Kim's group, Sejong University, Korea was utilized. The graphene was initially grown on a Cu-foil by CVD. C4 PMMA was applied by spin coating on the graphene surface on one side of the Cu-foil right after growth to minimize air exposure. The graphene on the other side was removed by conducting plasma ashing.

3.4.2 Cu etching

To etch away the Cu foil covering one side of the graphene, an etching solution of 3 % $(NH_4)_2S_2O_8$ in DI water was prepared. This was done by weighing up 1.8 g of $(NH_4)_2S_2O_8$ in powder form , which was then diluted with 60 ml of DI water in a beaker. The beaker was then put on a magnetic stirrer in a fume hood.

A small flake of was clipped from the Cu foil using a scissor, while taking care not to bend and twist the Cu foil. For this purpose a plastic tweezer with broad tip was used. In the cases where the flake was slightly bent, it was straightened by putting in between two glass slides.

The graphene flake was then transferred to the etching solution using a plastic tweezer, making sure the side containing graphene and PMMA was pointing up. The beaker was covered in aluminium foil to avoid solution evaporation, and the magnetic stirrer set to 100 Rounds per minute (rpm) to ensure a steady flow in the etching solution, effectively lowering the time needed to fully etch away the Cu. The graphene flake was left in the solution until all visible traces of Cu were gone, which was usually the case after approximately one hour.

Following the etching of the Cu foil, the graphene flakes were transparent, and only faintly visible though refraction from the PMMA. To dilute the etching solution, two large water baths were prepared. This was done by filling

[3] 2 % PMMA in anisole.

two 1.8 l beakers to the brink with DI water, and placing these next to the etching solution. The graphene flake was then transferred to the first water bath by gently scooping it up with a small oval glass slide. After waiting a few seconds, the graphene flake was transferred to the second water bath by the same method. This was to ensure that the final water bath contained a minimal amount of the etching solution. This process is illustrated in Figure 3.5

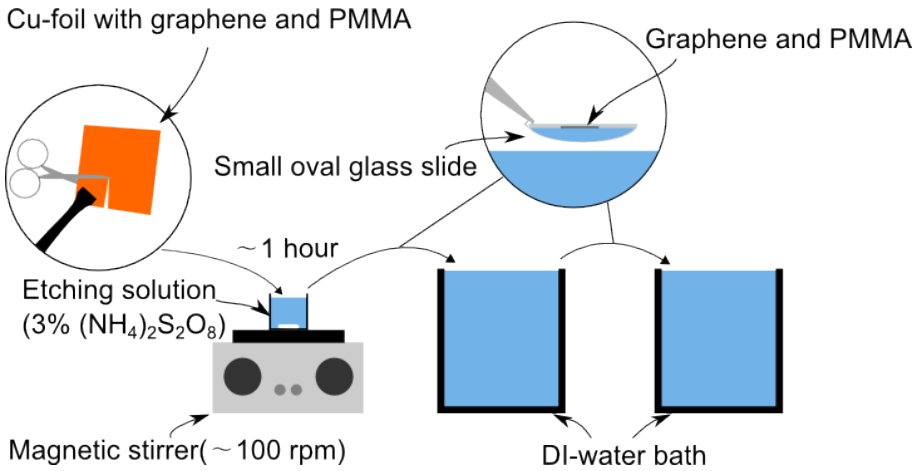


Figure 3.5: Figure illustrating the Cu etching process. A small flake is clipped from a Cu foil with PMMA and graphene on one side using a pair of scissors and a plastic tweezer. This flake put in an etching solution of 3 % $(NH_4)_2S_2O_8$ in DI water on a magnetic stirrer for approximately one hour until all Cu is gone. The flake is then transferred by a small oval glass slide to two large water baths to remove remaining etching solution.

3.4.3 Surface treatment

The samples were surface treated to remove any oxide layer on the GaAs nanowire surface that could affect the electric behavior of the contact. This was done by first conducting a plasma cleaning at 50 % power and 35 mbar O_2 pressure for 12 seconds. This followed by an immersion in 2.5 % HCl for 5 seconds, before being rinsed in running water for 1 minute. These parameters are summarized in Table 3.3. As GaAs forms an oxide layer in contact with air

Table 3.3: Surface treatment parameters.

Procedure			**Time**
Plasma cleaning	Power	50 %	12 sec
	Gas	O_2	
	Pressure	35 mbar	
Immersion 2.5 % HCl			5 sec
Running water rinse			1 min

after a relatively short time, care was taken immediately to transfer graphene following the surface treatment.

3.4.4 Transfer

The substrates intended for transfer were first fastened to a glass slide with double sided caption tape. To ease the transfer process, the substrates should be placed together on the edge of the glass slide.

Transfer was conducted by first immersing the glass slide just under the water surface. A plastic tweezer was then used to push the graphene flake towards the samples. This was done without actually touching the graphene flake, as the flake will be pushed away once the it gets close to the tweezer. The glass slide was then raised slowly, gently scooping up the graphene flake on top of the substrates. They were intermediately inspected using optical microscope to evaluate the quality of the transfer.

In the event that of an unsuccessful transfer, either due to unsatisfactory coverage of contact areas or extensive wrinkling, it was attempted to transfer the graphene flake back to the water bath by immersing the substrates slowly. If this was successful, a new transfer could be conducted.

3.4.5 Drying

Following the transfer, the samples were left to dry, so that the remaining water from the transfer process could evaporate. Two different drying processes were tested.

In the first process graphene quality was prioritized. The samples were left in room temperature for minimum 1 hour, before being placed on a 80 °C hot plate for 30 minutes.

Table 3.4: Drying process parameters.

Procedure		**Time**
Normal drying process	Room temperature	1 hour
	80 °C hotplate	30 min
Fast drying process	80 °C hotplate	10 min
	Room temperature	10 min

The second process was tested to minimize nanowire water exposure. In this case the samples were placed on a 80 °C hot plate for ten minutes, and then left in room temperature for 10 minutes. The parameters for these processes are summarized in Table 3.4

3.4.6 PMMA removal

To ensure a complete dissolving of the scaffold PMMA, the samples were left in a beaker filled with acetone for an extended period of time, usually overnight. They were then immersed in an IPA beaker for 10 minutes, before finally being blow-dried with N_2.

3.4.7 Preliminary SEM investigation

During the development of the graphene transfer step, samples were investigated in a *Hitachi S-5500 S(T)EM* after PMMA removal to verify graphene quality. Several different acceleration voltages and beam current values were tested. Only samples intended to test transfer process was investigated, as imaging by SEM leads to deposition of carbon on sample surface, which can potentially affect electrical properties.

3.5 Contact design

3.5.1 Optical microscope imaging for alignment

To design a digital mask for the later EBL procedure, an accurate determination of location of nanowires relative to the prepatterened contacts was needed. For this purpose, the samples were investigated using an optical microscope. Images intended for alignment was captured at maximum magnification, 1000x.

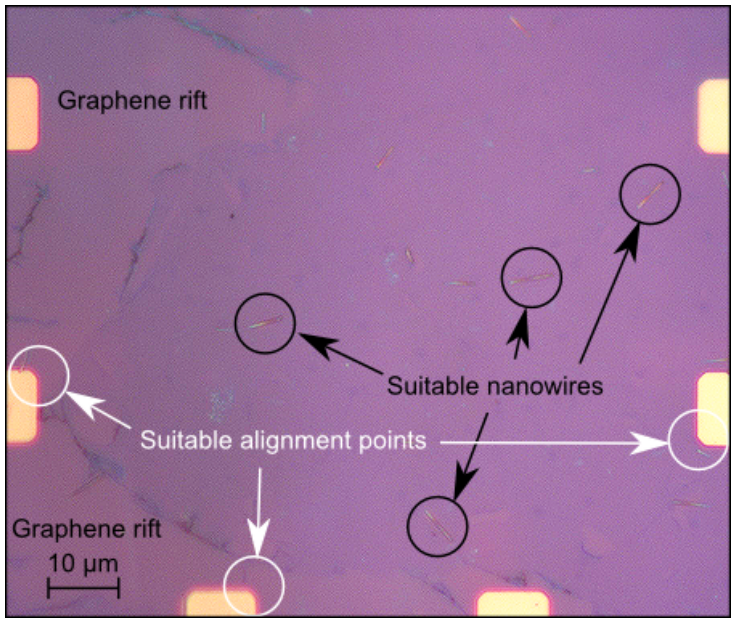


Figure 3.6: Example of an alignment image used to determine location of nanowires relative to prepatterned contact arms, including examples of suitable nanowires and alignment points. Graphene rifts are visible through contrast differences, as rifts will generally appear lighter and will often have a defined border due to curled up graphene.

The image should contain six of the prepatterned lead arms and minimum three nanowires suitable for contacting. Suitable nanowires are not surrounded by other nanowires or too close to graphene rifts. An example of an alignment image with suitable nanowires are shown in Figure 3.6.

3.5.2 Digital mask design

The alignment images were imported into the program Engauge Digitizer 2.15, where the nanowires were given coordinates relative to corners on the prepatterned contact arms. These coordinates were then transferred to CleWin, a digital mask editor, where they were visualized as rods. These processes have been covered in an earlier thesis [57, Appendix B, Appendix C].

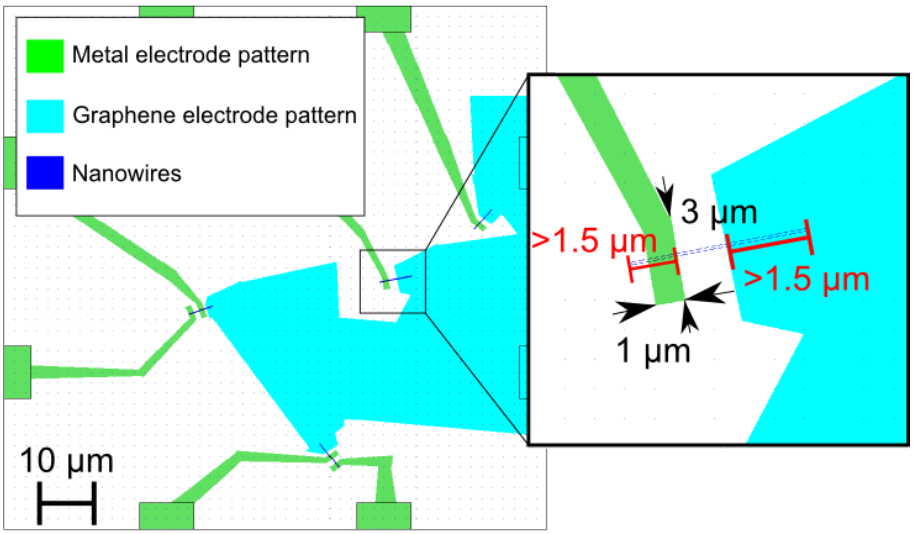


Figure 3.7: Example of an EBL pattern made using CleWin. Close-up image shows contact dimensions in black, while red markers demonstrate the design dimensions used to account for potential pattern off-set.

Using Clewin, a 100 x 100 µm^2 digital mask with two layers was designed. The first layer was intended to contact one end of the nanowires to the prepatterned contact arms. The second layer was designed to act as a shielding layer for the graphene electrode.

The patterns were saved saved in *.gds* files, and transferred to the computer controlling the EBL instrument.

3.6 Graphene contacting

This step was only conducted for ExG-devices, as the the graphene flakes transferred by this method was not large enough to cover any of the prepatterned contact arms. As the samples that arrived from Sangwook Lee's group at Kunkuk University was already covered in PMMA, no spin coating step was necessary.

Table 3.5: EBL exposure parameters.

Parameter	**Value**
Acceleration voltage	20 kV
Beam current	40 pA
Step size	4 nm
Area dwell time	0.72 µs
Area dose	180 µAs/cm^2

3.6.1 Electron beam lithography

EBL was conducted using a *Hitachi S-4300SE*. This is a converted SEM instrument, where the *Hitachi S-4300SE* software controls the SEM function, while the *Raith ELPHY Plus* program controls the lithography function. The exposed was exposed in a 100 x 100 µm write field, with an acceleration voltage of 20 kV and a beam current of 40 pA. These and other EBL parametres are listed in Table 3.7.

The EBL process can be summarized in the following steps:

1. Sample mounting and insertion
2. Beam current adjustment
3. Beam alignment
4. Rotation and angle correction
5. Locating target area
6. Position correction
7. Stage movement alignment
8. Write field alignment
9. Exposure
10. Sample unloading

A detailed description of the EBL procedure can be found in Appendix B.

3.6.2 Development

A developer solution was made by mixing IPA 9:1 deionized water (DI water). The samples were immersed in this solution of 15 seconds, before quickly bringing them under running DI water to avoid overdeveloping. Finally they were kept under running water for approximately 30 seconds and blow-dried with N_2.

3.6.3 Metallization and lift-off

The samples underwent metallization in *Custom ATC-2200V AJA sputter and e-beam evaporator*. First a 5 nm layer of Ti was deposited, followed by a 35 nm Au layer. Both layers were deposited at a rate of 5 Å/s, the recommended deposition rate for this instrument. Following metallization, the samples were immersed in an acetone bath to perform lift-off. The length of lift-off step was not measured, but was rather done at time deemed reasonable to let all resist dissolve. This usually meant leaving the samples in acetone overnight.

3.7 Graphene trimming

Following graphene transfer, a removal of the graphene not intended for any electrodes is necessary. This is to ensure that no lead contact arms are shortened by graphene, and that the nanowires are only partially covered by graphene. To perform this, a shielding layer for the graphene electrode was deposited via EBL, which allowed the rest of the graphene to be removed via plasma ashing. A schematic of the graphene trimming process is shown in Figure 3.8.

For the purpose of applying a shielding layer, three different approaches were tested. This section will only cover the successful approach, while the results from the other two approaches are elaborated in the Results chapter.

3.7.1 Spin coating

In preparation for the EBL processs, the samples were applied a layer of PMMA A3.57 950k positive resist[4] from Micro Chem Corp. This was done by placing the samples one at a time in a spin coater, and applying the resist by pipette. They were then spun at 3000 rpm for 2 minutes, with a 5 second acceleration and deacceleration step before and after, giving a final thickness of 200 nm[5].

[4] 3.57% PMMA in anisole.

[5] Measured using a Filmetrics F20 reflectometer.

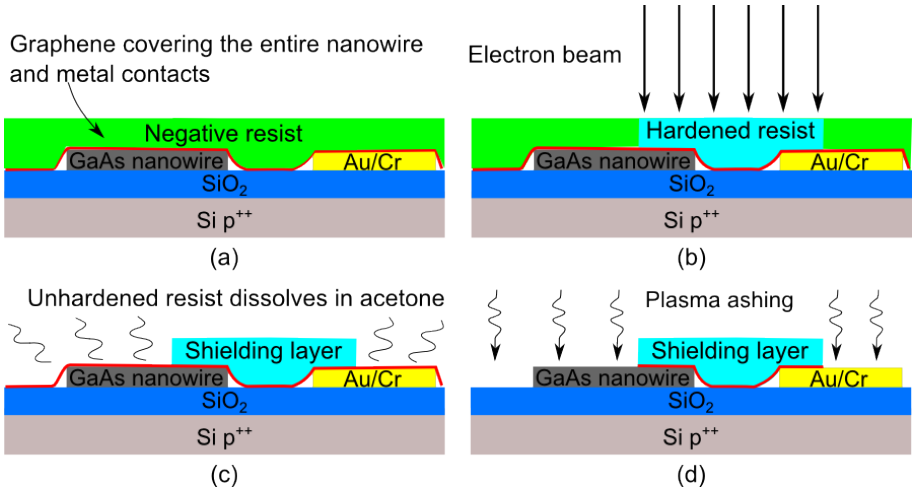


Figure 3.8: Schematic overview of the graphene trimming process. *(a)* A negative resist is applied to the sample via spin coating. *(b)* Resist laying on top the grapehene electrode is exposed via EBL, causing it to harden. *(c)* Immersion in acetone causes the unhardened resist to dissolve, exposing all but the graphene electrode. *(c)* Plasma ashing removes all graphene not shielded by hardened resist.

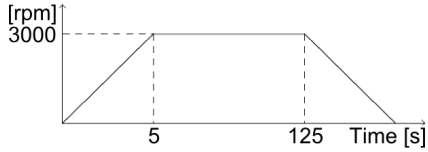


Figure 3.9: Graph illustrating the spin profile used when spin coating.

The samples were then soft baked at 160 °C for 2 minutes. Spin coating parameters are shown in Table 3.6 and the spin profile is shown in Figure 3.9.

3.7.2 Electron beam lithography

The EBL procedure utlized for graphene trimming was the same as the one listed in section 3.6.1, but with other exposure parameters were used. PMMA

Table 3.6: Table listing parameters used in the spin coating procedure.

Parameter	**Value**
Spin speed	3000 rpm
Spin acceleration	1000 rpm/s
Spin time	120 sec
Baking time	120 sec
Baking temperature	160 °C

Table 3.7: EBL exposure parameters.

Parameter	**Value**
Acceleration voltage	20 kV
Beam current	400 pA
Step size	8 nm
Area dwell time	0.016µs
Area dose	10000 µAs/cm^2

is originally intended to be used as a positive resist. To be able to use it as a negative resist, a relatively large area dose was needed. Several different step sizes and doses were tested, and the optimal EBL parameters found is listed in Table 3.7.

3.7.3 Development

For development the samples were immersed in acetone for approximately 1 minute, before being sprayed with IPA for 10 seconds and blow-dried with N_2.

3.7.4 Plasma ashing

To remove all graphene not shielded by hardened resist, the samples were treated with a plasma ashing. This was done by conducting a plasma cleaning at 50 % power and 35 mbar O_2 pressure for 30 seconds.

3.8 Nanowire contacting

3.8.1 Spin coating

Prior to electron beam lithography, samples were spin coated with a two-layer PMMA resist. First a layer of PMMA 200k A12 was applied with pipette, before spinning the sample at 5000 rpm, with a 5 second acceleration and deacceleration step at 1000 rpm/s. The samples were then soft baked at 2 min. The same process was then used to apply a layer of PMMA 950k A3.57, giving an total thickness of approximate 1 µm [6]. The spin coating parametres and spin profile are the same as illustrated in Figure 3.9 except that 5000 rpm instead of 3000 rpm was utilized. This two-layer resist was chosen to provide a resist approximate three times thicker than the thickness intended for the deposited metal[7], while the first layer with a higher PMMA concentration is expected to solve easier during the development stage, providing a good undercut.

3.8.2 Electron beam lithography, Development and Metallization

The remaining processing steps consisting EBL exposure, development, and metallization was conducted in the same manner as previously explained in sections 3.6.1, 3.6.2, and 3.6.3.

For the metallization step, a different metal stack consisting of Pt/Ti/Pt/Au with a total thickness of 250 nm was deposited (Table 3.8). This metal stack is known to achieve good contact properties with GaAs (Section 2.3.1). The thickness of the Au layer was chosen to ensure total overlap between metal and nanowire.

3.9 Electrical Measurements

3.9.1 Setup

In preparation for the measurements, the SiO_2 substrates were glued on to a PCB plate using conductive *Dotite D-500* silver paste. This allows the SiO_2 substrate to act as a back gate by applying a voltage to the PCB plate.

[6] Estimated from supplier spin curves.

[7] For lift-off purposes, one generally recommends a resist layer three to four times thicker than the metal layer.

Table 3.8: Metal stack used for nanowire contacts.

Metal	**Thickness** $[nm]$
Pt	5
TI	10
Pt	10
Au	225

The electrical measurements were conducted at *Summit* RF-shielded probingstation from *Cascade Microtech* with *DCM 208 Series Precision Positioners*. The cables from the probes were connected through triax connectors to a *Keithley 2636A Dual-channel System SourceMeter*, with two source measuring units (SMUs). This source meter was again connected to computer through *Nattional Instruments GPIB-USB-HS connector*, where the program LabVIEW was used to conduct and record the measurements. This setup is illustrated in figure 3.10a The measurement script utilized was written and developed by Dr. Dong Chul Kim at CrayoNano.

To conduct the measurements, the PCB plate containing the SiO_2 substrate was placed inside the probing station, and SMU A source and ground probes were placed on the appropriate connect pads. The probe connected to SMU B source was placed on the PCB plate to provide a gate voltage. This setup is illustrated in Figure 3.10b.

3.9.2 *I-V* measurements

IV-curves were constructed by conducting voltage sweeps over the SMU A setup while measuring resistance and current. Open and short circuit current was first measured to verify the probe function. For *I-V* measurements under gate voltage, a constant voltage was applied to PCB plate via SMU B during the voltage sweep. Voltage sweeps were conducted by increasing voltage at preset intervals while measuring current. This was normally done by sweeping the voltage from zero to +3 V, down to -3 V, and then back to zero at 0.2 V intervals. To avoid the unintentionally destroy contacts by conducting too much current through them, a compliance current in the source meter was utilized, meaning the sourcemeter will limit the current to a preset value. 50 - 100 µA was used as compliance current for contacts involving nanowires, while 500 µA were used for graphene contacts.

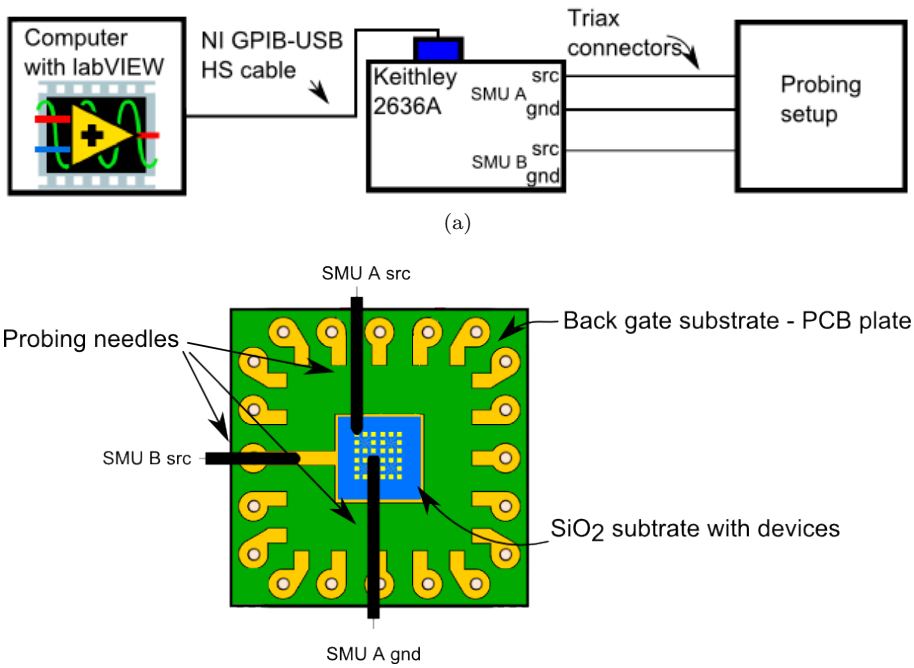


Figure 3.10: Schematic overview of measurement and probing setup. *(a)* The probing setup is connected by triax connectors to a source measuring units (SMU) of Keithly 2636a sourcemeter, which is controlled by the LabVIEW software on a computer. *(b)* The SiO_2 containing devices are glued to a PCB plate using conductive silver paste. The SMU A probes are then placed on the appropriate connect pads on the SiO_2, while the SMU B probe is placed on the PCB plate to provide a gate voltage.

3.9.3 Gate voltage measurements

For the gate voltage measurements, the probes were placed in a similar manner as explained above. Measurement was then conducted by sweeping the gate voltage while applying a constant bias voltage. Gate voltage sweeps were conducted by increasing the voltage from zero to +80 voltage, down to -80 and then back to zero at either 1 or 0.25 V intervals.

3.10 SEM imaging

Finalized samples were investigated using either *Hitachi S-5500 S(T)EM* or *Hitachi S-4300SE*. SEM investigation was always performed after all electrical characterization was finished, as SEM imaging inevitably leads to carbon contamination which can potentially affect electrical properties.

Chapter 4

Results

4.1 Preliminary EBL procedure testing

A development of the EBL procedure was made, and tested by making a batch of GaAs nanowire devices. The accuracy of the pattern was verified by optical inspection, and found to yield satisfactory results. The new EBL procedure was thus adopted for all subsequent EBL processing. The results from these tests can be found in Appendix C, while the EBL procedure is elaborated in Appendix B.

4.2 Graphene transfer

4.2.1 CVD-grown graphene - Graphene Supermarket

Initially the graphene transfer was tested by transferring graphene supplied by Graphene Supermarket to both Si_3N_4 and SiO_2 substrates. The transfer process was found to yield unsatisfactory results, as extensive wrinkling of the graphene layer was observed in all cases. This is thought to be the result of a non uniform application of scaffold PMMA. These results are shown in detail in Appendix D

Si_3N_4 substrates were found to be unsuitable compared to SiO_2 substrates, as graphene layers were found to be much easier to spot on SiO_2. The poor visibility of graphene on Si_3N_4 made assessing graphene quality difficult, and these substrates were therefore deemed unsuitable.

4.2.2 CVD-grown graphene - Sejong University

The transfer process was tested on graphene supplied by Sejong University and found to yield better results. As seen in Figure 4.1a, a nearly continuous graphene layer is covering on the surface, with rifts and holes easily visible through contrast differences.

Following the successful transfer, the samples were studied using SEM. The surface of the transferred graphene was found to appear dirty, with small creaks and particles covering the surface, as seen in Figures 4.1 and 4.2. The layer also appears thicker than one would expect from a pure graphene sample. Figure 4.2a shows a close-up SEM image captured at 30 kV, where the layer covering the GaAs nanowire is still visible. As graphene is only one atom thick, it should only be visible only at low acceleration voltages, making this a strong indication that a layer of PMMA remnants is still present after PMMA removal.

Initial conductivity test by simple multimeter

By using a simple hand held multimeter, samples were found to be conductive regardless of where the probes where placed on the surface after graphene transfer. The multimeter was operated in resistance detection mode, and resistance values were found to be in the range of 4 - 8 kΩ. This was found to be a convenient method for checking for good graphene quality after doing a transfer. While the resistance values measured is thought to be an inaccurate estimate of the real graphene resistance, it is nonetheless a clear indication that a layer with good conductance is covering the surface.

Effect of water exposure

Close-up study of surface of nanowires not covered by graphene revealed a rough, rugged surface (Figure 4.3). Prior to transfer, the surface of GaAs nanowire consists of smooth well-defined facets, as seen in figure 4.4a. The degree of corrosion was found to depend on the duration of the drying step (Section 3.4.5), where longer drying time resulted in more corrosion. This is thought to be the result of the various forms of Gallium- and Arsenide oxides present in the native GaAs oxide layer dissolving in water. This exposes a pure GaAs surface to water, which is then able to oxidize due to oxygen presence in water, and yet again dissolve in water.

This hypothesis was tested by immersing a substrate containing nanowires in water for 1 hour. As seen in Figure 4.4, this resulted in similar corrosion as observed after transferring graphene.

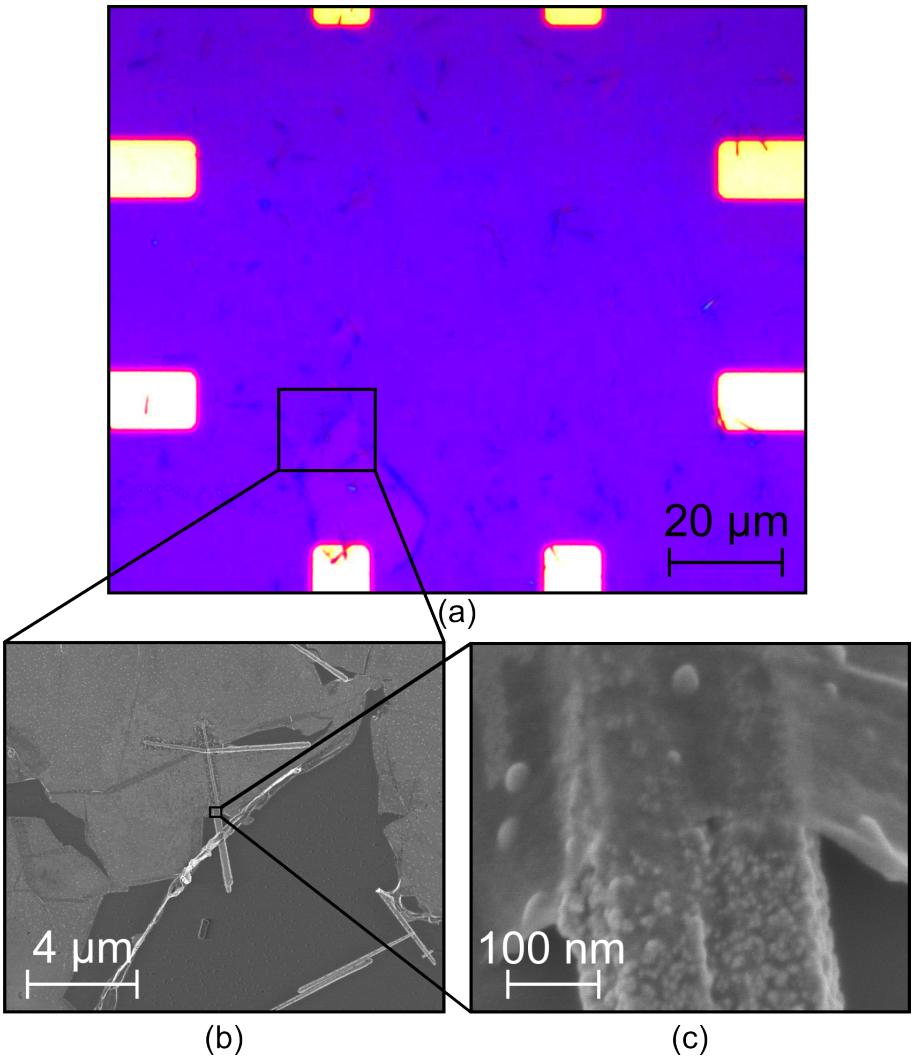
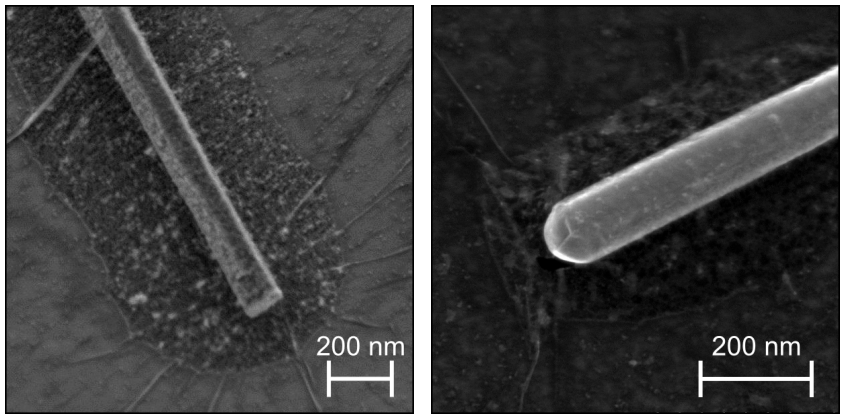
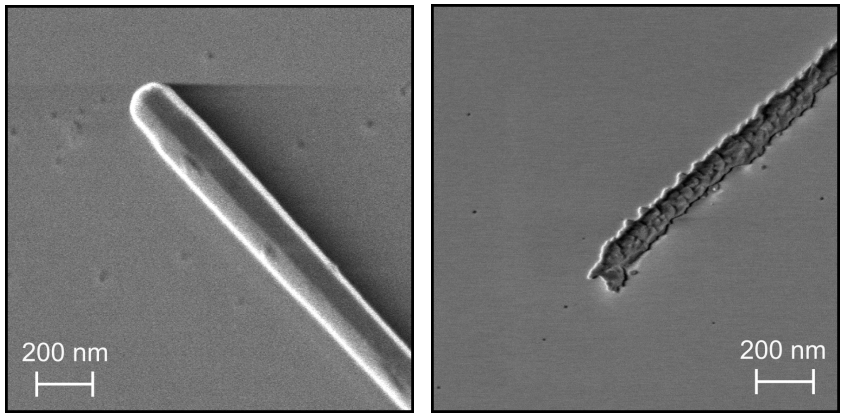


Figure 4.1: Optical micropscope *(a)* and SEM images *(b)*, and *(c)* of a sample after finishing graphene transfer.



(a) (b)

Figure 4.2: SEM images of GaAs nanowires after graphene transfer captured at: *(a)* 5 kV *(b)* 30 kV.



(a) (b)

Figure 4.4: SEM images of nanowires before *(a)* and after *(b)* being exposed to DI water for 1 hour.

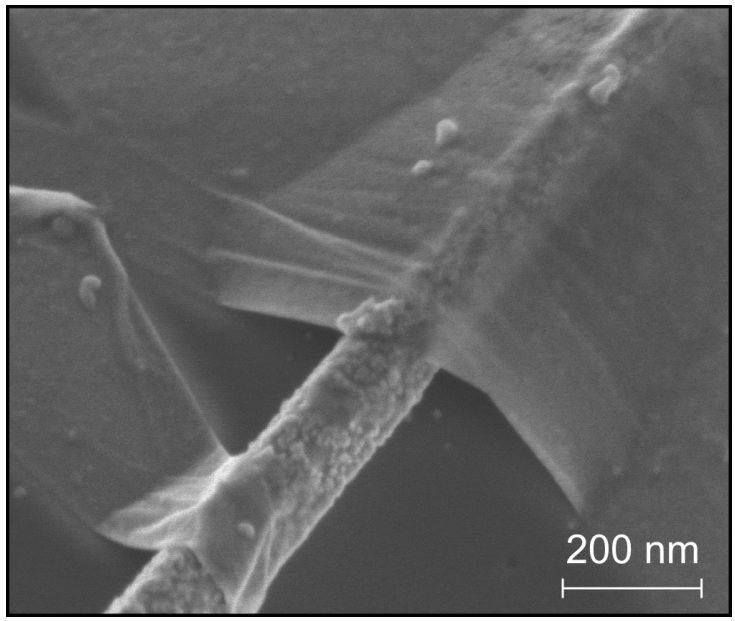


Figure 4.3: SEM image showing a nanowire partially covered by graphene. The nanowire surface is seen to be rugged, indicating corrosion the graphene transfer process.

Measures to reduce water exposure

Several measures were tested to reduce the water exposure during the transfer process without succeeding.

First the usage IPA instead of DI water for the transferring solution was tested. This involved moving the graphene flake to a solution of IPA, after etching away the Cu-foil. This method was found to be unsuccessful. As the etching of the Cu-foil is carried out in solution of water, there will inevitably be water clinging to the graphene and scaffold PMMA when moving this to the transfer solution. When moving the graphene and PMMA it was found that this water made the graphene flake sink and twirl up in the IPA, as water is denser and has a higher surface tension. This means that immediately after moving the graphene flake to IPA, the water clinging to the graphene flake will sink and drag the graphene down in the solution.

A faster drying procedure was tested with the intent of minimizing the water exposure. This resulted in extensive amount of rifts and holes and in the graphene layer, as seen in Figure 4.5. This is thought to be the result of graphene having insufficient time to achieve good contact with the underlying substrate. Immediately after transferring the graphene and scaffold PMMA to the substrate, small volumes of water will be trapped in between them. Given insufficient time to dry, these water pockets will result in holes when the PMMA is removed.

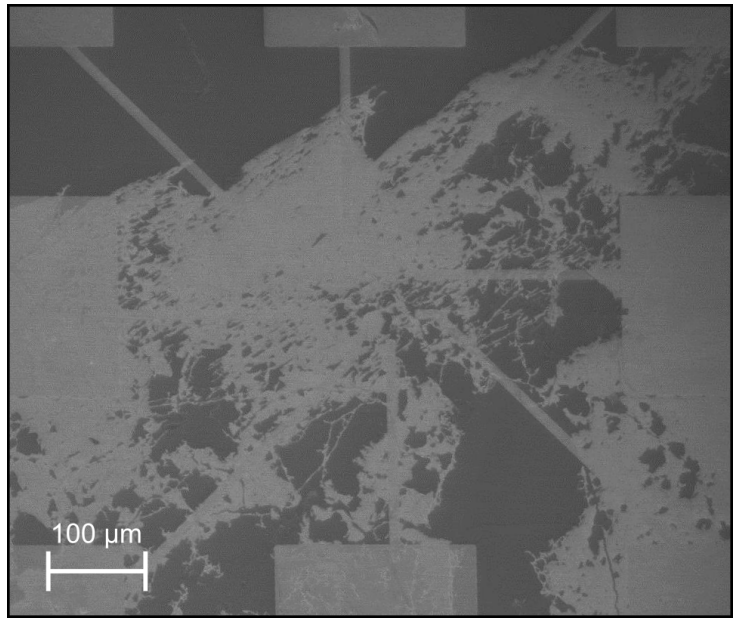


Figure 4.5: SEM image showing a sample after graphene transfer where a faster drying procedure was utilized.

4.2.3 Exfoliated graphene

Initially a batch of three Si_3N4 substrates with a total of 11 contacted nanowires were fabricated and sent to Professor Sang-wook Lee's group, Konkuk University, for exfoliated graphene transfer. Transfers to all three substrates were attempted, but found to be unsuccessful. It was concluded that the combination of the limited visibility of graphene on Si_3N4 along with close proximity

of the relative thick nanowire metal contacts of 225 nm made these samples unsuitable for transfer.

A new batch of SiO_2 substrates with non-contacted nanowires were prepared. These had exfoliated graphene successfully transferred, and a total of three substrates, each containing a target area with an identified single-layer graphene flake, were received from Konkuk University.

4.3 Device fabrication

4.3.1 Choice of resist for graphene shielding layer

For the purpose of shielding the graphene electrode during the graphene trimming (Section 3.7), three approaches were tested. As evident from Figure 4.3, graphene resting on top of nanowires is in a strained condition, with an air gap between the nanowire and graphene layer. This condition is thought to be very delicate , and it was therefore deemed important to choose a thin shielding layer to induce as little stress on the strained graphene as possible.

Negative Ma-N 4201

First the negative Ma-N 4201 resist was tested, but found to be unsuitable due to insufficient adhesion to the graphene/PMMA surface. Initially a recipe for obtaining a 100 nm layer was followed, but later numerous variations of the spin coating parameters were tested, without achieving a complete coverage. The resist would only stick to the substrate in small puddles, and later investigation by SEM showed these puddles to have a thickness of over 2 µm. It was therefore concluded that the Ma-N 4201 is incompatible with the graphene/PMMA surface.

PMMA A3.57

PMMA is primarily used as a positive resist, and the PMMA supplied by Microchem is intended for this usage. PMMA is however also known to be able to serve the role of negative resist, given a high enough dosage [64, 65].

The thinnest PMMA layer found to be depositable in reliable and reproducible manner, was the A3.57 PMMA applied in a 200 nm layer[1].

[1] Estimated from supplier spin curves.

Several EBL procedures were conducted to test the usage of PMMA in a negative manner. Doses in excess of 6000 $\mu As/cm^2$were found to give reproducible patterns when using acetone as a developer. Initially a beam current of 40 pA was utilized, as it was believed that a low current was necessary for achieving the necessary pattern accuracy. The low beam current was however found to give too long exposure times for EBL patterning, which resulted in a low accuracy in the final pattern due to beam drifting during the exposure. Increasing the beam current to 400 pA was found to solve this problem, as this decreased the exposure times sufficiently to minimize the effect of the electron beam drifting during exposure. It was thus found that utilizing PMMA as negative resist in this manner was a viable choice, with patterning accuracy on par with PMMA being used in a positive manner.

Scaffold PMMA - CVD-grown graphene device

For the CVDG-devices, using the scaffold PMMA also as a shielding layer was tested. This involved skipping the PMMA removal step in the transfer process (section 3.4.6), and instead go directly the EBL exposure step 3.7. This was first believed to better preserve graphene quality, as the PMMA applied right after growth would never be removed, thus shielding graphene from all subsequent air exposure. This approach turned out to be unsuitable, as not removing the scaffold PMMA also implicate that the nanowires laying under the scaffold PMMA will endure longer durations of water exposure. After development in the graphene trimming process, all nanowires were found to be completely destroyed by corrosion.

4.3.2 Choice of fabrication order

For the fabrication route, two different orders where tested.

Nanowire contacting prior to graphene transfer and trimming

Initially the nanowire contacting was carried out before graphene transfer and graphene trimming. Several devices were finalized in this fabrication order, but SEM investigation revealed that all contacted nanowires were destroyed. Closer inspection revealed that only contacted nanowires where completely destroyed, while non-contacted nanowires were found in a much better condition, as demonstrated in figure 4.6. This is believed to be the result of galvanic corrosion. In the presence of a metal with higher electronegativity like Au,

GaAs is known to be able to act as a anode and undergo galvanic corrosion with the metal acting as the cathode [66]. This corrosion process is believed to occur at much higher rate than the corrosion in non-contacted nanowires, thus explaining the observed difference between contacted and non-contacted nanowires in Figure 4.6.

Graphene transfer and trimming prior to nanowire contacting

In response to the observed destruction of nanowires, conducting graphene transfer and trimming prior to nanowire contacting was tested. This approach turned out to solve the problem, thus strengthening the proposed theory of contacted nanowires undergoing galvanic corrosion. Figure **??** shows some of the finalized devices obtained.

4.3.3 ExG-device - failure during graphene trimming

The three SiO_2 substrates obtained from Professor Sang-wook Lee's group, Konkuk University where first subjected to graphene contacting (Section 3.6). Optical inspection following the development showed the graphene to be slightly damaged, with some new rifts showing up. After application of PMMA for graphene trimming (Section 3.7), the graphene flakes were found to have been damaged to the extent that the samples were unusable. Optical inspection showed that the graphene flakes had curled up and wrinkled in the three target areas, as seen in Figure 4.8.

It was thus concluded that the outlined fabrication process is unsuitable for ExG-devices due to single-layer graphene flakes being too delicate to sustain three EBL processing steps after transfer.

4.4 Electrical measurements

A total of 16 CVDG-devices were fabricated and measured in the course of this thesis. No measurable ExG-devices were obtained due to graphene breakdown during fabrication (Section 4.3.3).

In the following section the electrical measurements will be presented.

4.4.1 Nanowire measurements

Several Graphene-Nanowire devices (GP/NW-devices) were made with two probes on the nanowire, so Metal-Nanowire-Metal contact (MNWM-contact)

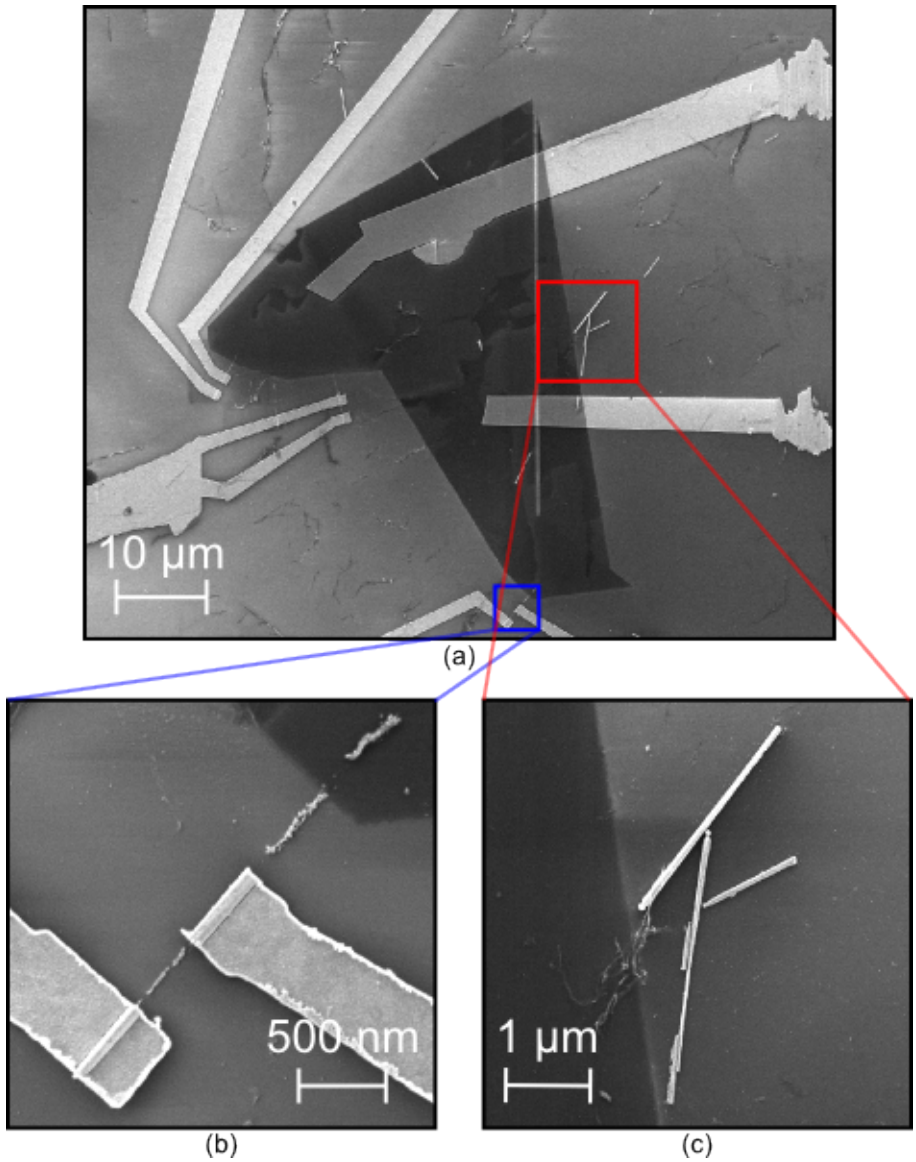


Figure 4.6: SEM images showing a finalized device where the nanowires were contacted prior to graphene transfer and trimming *(a)*. Close-up images demonstrate how contacted nanowires were found to be completely destroyed (*b*), while the non-contacted nanowires were found in a much better condition *(c)*.

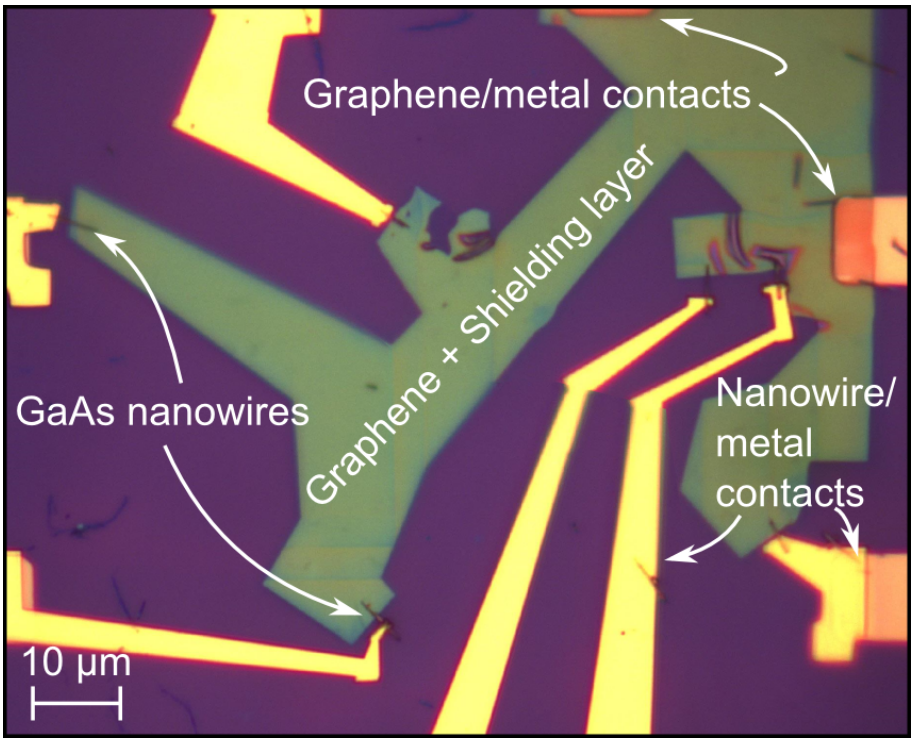


Figure 4.7: Optical microscope image demonstrating six finalized graphene/GaAs nanowire hybrid devices.

I-V measurements were possible. These were measured and compared *I-V* measurements conducted on nanowires contacted prior to graphene transfer to determine if the observed corrosion would affect the electrical behavior.

Figure 4.9a shows *I-V* behavior of five MNWM-contacts fabricated without doing graphene transfer, i.e. without being exposed to water. These were initially compared to five MNWM-contacts contacted after doing graphene transfer, as seen in Figure 4.9b. Devices exposed to water were consistently seen to yield lower current values, which is credited to the reduced diameter from corrosion.

Further measurements on other substrates have however shown large variations in *I-V* behavior, as seen in Figure 4.9c and Figure 4.9d. Measurements

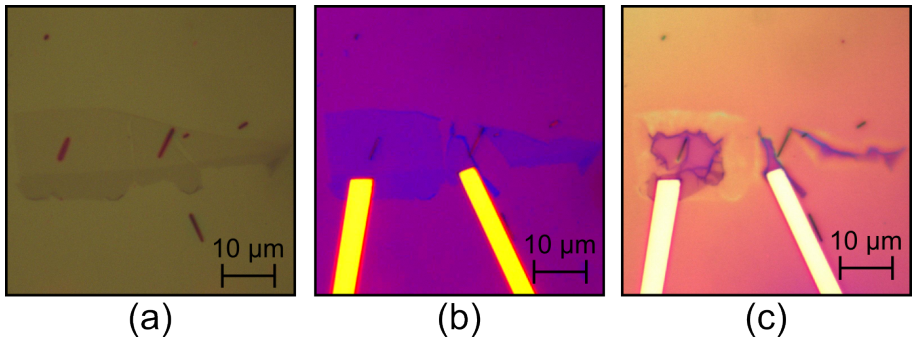


Figure 4.8: Optical microscope images showing ExG-devices during processing: *(a)* After receiving the samples from Sangwook Lee's group at Konkuk University *(b)* After finalizing graphene contacting. *(c)* After applying PMMA for graphene trimming.

were generally seen to yield different degrees of symmetry between negative and positive bias, and the current values and curve slopes were seen differ between measurement sessions. Hysteresis was generally observed in all measurements.

The *I-V* curves like the one seen in Figure 4.9d is thought to be the result of extensive corrosion. Figure 4.9c shows one of the *I-V* curves obtained from MNWM-contacts in the last batch of GP/NW-devices, where the current values were seen to greatly exceed earlier measurements. At this point there were indications that a software error in the machine used for the metallization (Section 3.8.2) had prevented the first 5 nm layer of Pt from being deposited on earlier samples. The first Pt layer serves the role of creating a good electrical contact, while the following Ti layer acts as a adhesion and diffusion stop layer. If the first Pt layer is absent, it is believed that this would result in a larger potential barrier at the contact, due to the lower work function of Ti. This would explain why the later samples showed higher current values.

4.4.2 Graphene measurements

A series of measurements to verify the graphene quality were made. The graphene electrodes were fabricated with two metal contacts for this purpose. The following measurements were conducted on Metal-Graphene-Metal contacts (MGM-contacts).

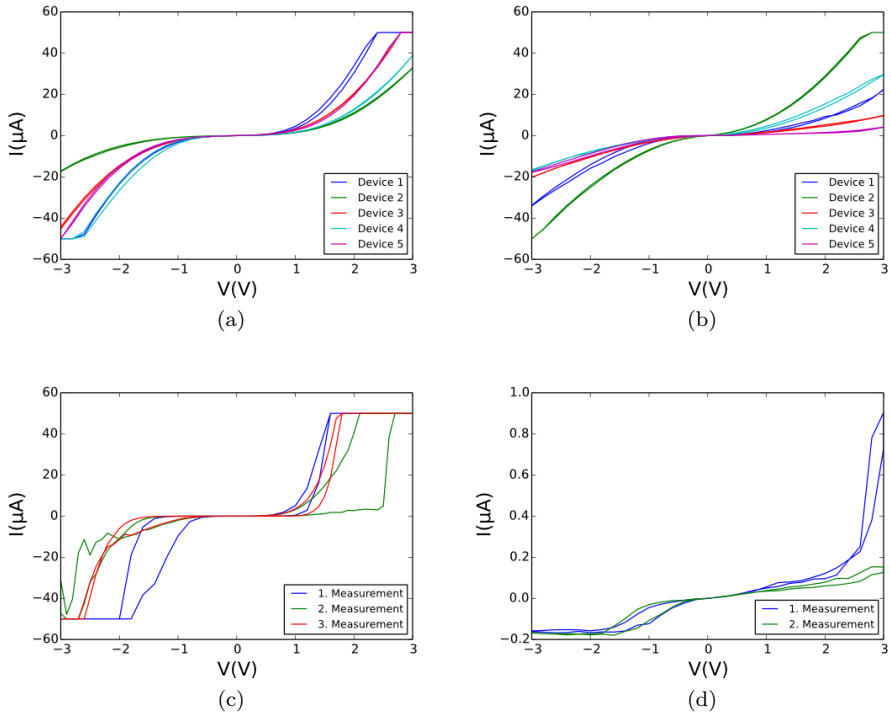


Figure 4.9: I-V curves from different MNWM-contacts. *(a)* Five MNWM-contacts measured before graphene transfer. *(b)* Five MNWM-contacts measured after graphene transfer. *(c)* Three different measurements from the same MNWM-contact. Three measurements are included to illustrate how I-V curves would vary from different measurements. *(d)* Two measurements on a MNWM-contact displaying low current. The two measurements illustrate how the maximum current was seen to vary significantly between measurements.

Table 4.1: Resistance values obtained from five MGM-contacts, presented as standard ± one standard deviation

Sample	Resistance
#1_1	9221.11 ± 13.59 Ω
#2_1	4461.74 ± 117.92 Ω
#2_2	3726.55 ± 339.72 Ω
#2_3	2734.20 ± 20.24 Ω
#3_1	8466.67 ± 542.19 Ω

I-V measurements

I-V measurements of nine MGM-contacts across four different substrates were conducted. Initially one displayed ohmic behavior, while eight displayed rectifying behavior indicating the formation of a Schottky barrier at one or both contacts. Both the symmetry and current values were seen to vary on same contacts from different measurement sessions.

For MGM-contacts subjected to bias voltage over longer durations, a sudden shift to ohmic behavior was observed, as seen in Figure 4.10. The duration and magnitude of the applied voltage before observing a shift to ohmic behavior vary significantly between the three samples, with one becoming ohmic after the second measurement, while others shifted after prolonged exposure to a constant bias voltage during gate-voltage measures.

After shifting to ohmic behavior, MGM-contacts were generally found to be stable. *I-V* measurements were found to consistently reproduce.

Table 4.1 lists some of the resistance values obtained from the linear MGM-contacts.

Gate voltage measurements

Several gate voltage sweeps were conducted on MGM-contacts on two different substrates, and the results were found to vary significantly from substrate to substrate.

Figure 4.11 shows the resistance plotted toward the applied gate voltage for MGM-contacts two different substrates. Figure 4.11a displays the characteristic Dirac behavior expected from MGM-contacts. The applied gate voltage induces charge carriers in graphene electrode, effectively shifting the Fermi level, and thus the doping concentration (Section 2.2). The curve in Figure 4.11a was reproduced for all MGM-contacts on this substrate, at several differ-

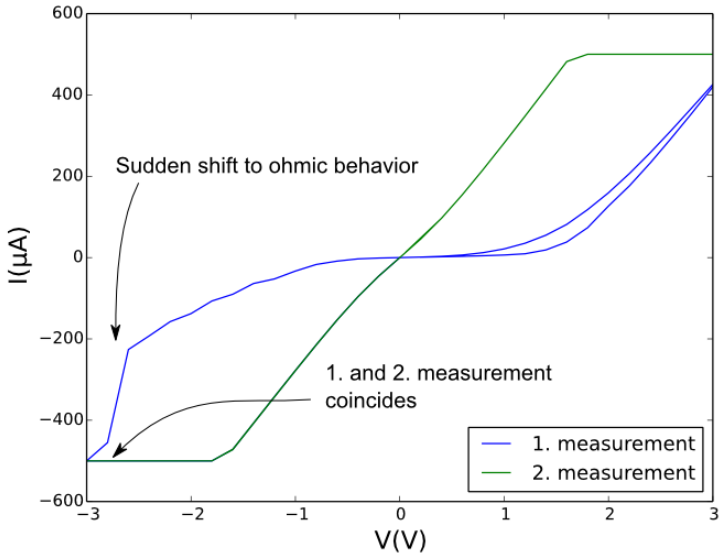
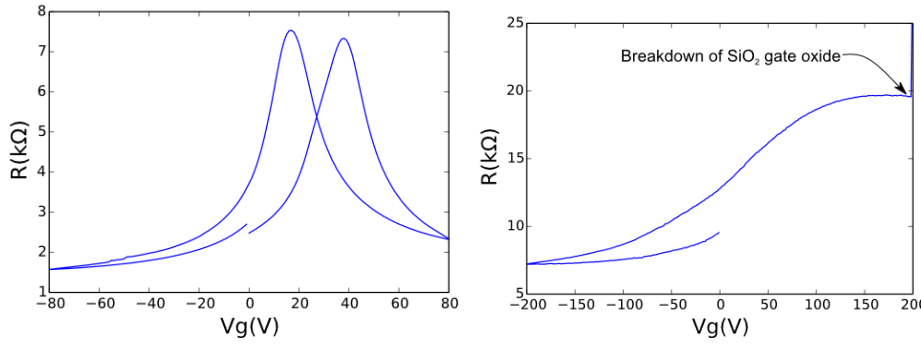


Figure 4.10: *I-V* curve from a MNWM-contact demonstrating a shift from rectifying to ohmic behavior. The linear 2. Measurement curve reproduced at all subsequent measurement, indicating the ohmic behavior to be relevant stable. A compliance current of 500 μA was utilized, which is why the linear curve is seen to flatten at roughly ± 2 V.

ent bias voltages, with the resistance maximum always occurring at 18 V when approach from a lower voltage, and a 38 V when approached from a higher voltage.

Figure 4.11b shows another substrate where the Dirac behavior was not observed. A gradual increase in resistance is seen, but due to the broadness of the peak and large amount of applied gate voltage, this not thought to be the result of Dirac behavior. A possible explanation for the lack of Dirac behavior for this sample is contamination by air. On this sample the graphene was transferred one month in advance of the measurements, with the graphene being exposed to air without any shielding layer in a clean room environment in the mean time.



(a) (b)

Figure 4.11: Typical $R - V_{gate}$ characteristics for MGM-contacts on two different substrates. *(a)* Displays Dirac behavior, with the Dirac point being slightly shifted dependent on the direction it is approached from. For *(b)* an increase in resistance is seen, but no maximum was found until the SiO_2 gate oxide broke down at 200 V. The peak is also thought to be too broad to be credited to Dirac behavior.

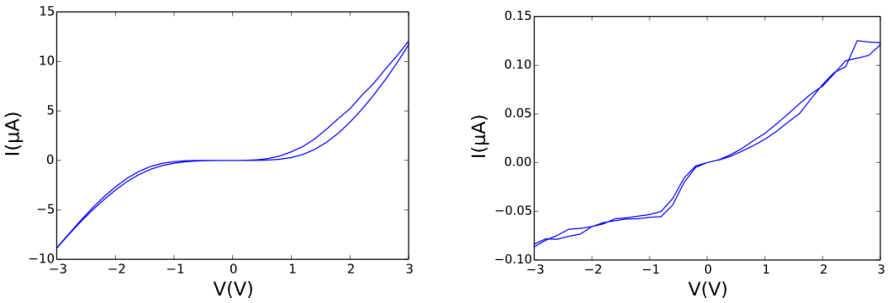
4.4.3 GP/NW-device measurements

I-V measurements

16 GP/NW-devices were measured, and while current value, symmetry and hysteresis to were seen to vary significantly between devices and measurement sessions, two notable trends were observed.

The *I-V* behavior seen in Figure 4.12a were observed in five devices. Several voltage sweeps on the same device would generally reproduce the same *I-V* curve, though small variations of 1 - 3 μA for the maximum values were observed.

The behavior seen in Figure 4.12b was observed in six devices. Devices displaying this behavior were generally less consistent between different measurements. Larger relative changes in the current were observed, and the measurements would often produce spikes, i.e. a sudden increase and decrease arising from one measurement point. Often these devices displayed a large degree of asymmetry, with typically one bias polarity resulting in less than 0.1 μA, while applying the same voltage with opposite polarity would result in several μA. This asymmetry was however not seen to be consistent with the



(a) (b)

Figure 4.12: *I-V* curves obtained from GP/NW-devices, displaying the two noteable trends observed. *(a)* Typical *I-V* behavior in a high current GP/NW-device. *(b)*Typical behavior in a low current GP/NW-devices.

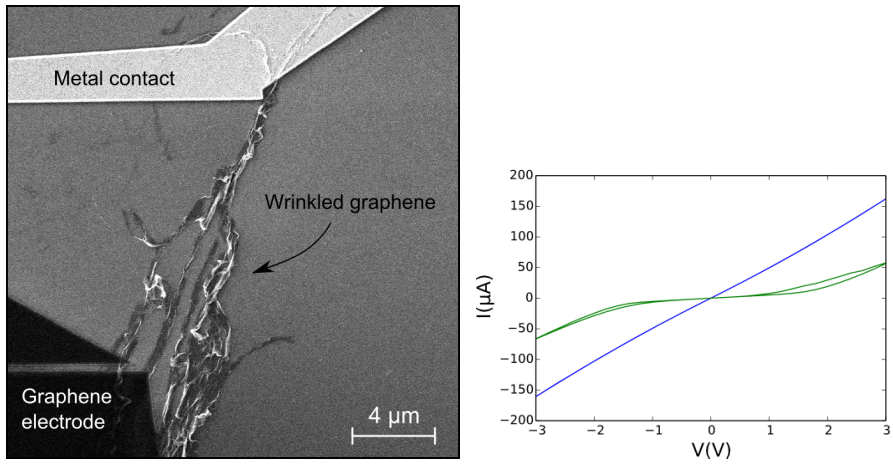
polarity of the voltage.

Shortening by graphene

As mentioned in Section 4.2.2, the transfer process would generally leave rifts and holes with a border of curled up/wrinkled graphene. These wrinkled were observed to remain after plasma ashing, and it is believed that they are not removable with plasma ashing parameters compatible with preserving the nanowire quality.

In some cases, these wrinkles were seen to overlap the graphene electrode and the metal arm contacting the nanowire, as seen in Figure 4.13a. This is believed to cause a shortening in the GP/NW-device, as MGM-contacts are believed to be significantly less resistive than GP/NW-devices. The *I-V* curves of these contacts were seen to initially display rectifying behavior, before shifting to ohmic behavior after several *I-V* measurements (Figure 4.13b), thus displaying similar behavior as MGM-contacts.

Three devices were also seen to shift to ohmic behavior, but without any visible trace of graphene wrinkles overlapping the electrodes. One of these devices is shown in Figure 4.14. Due to the layout of the contact arms on the substrate, it is believed that a shortening by graphene should be visible in the area shown in Figure 4.14. However, no visible traces of graphene wrinkles overlapping the electrodes were found at any point in the substrate.



(a) (b)

Figure 4.13: *(a)* SEM image showing wrinkled graphene overlapping a metal contact and the graphene electrode, shortening a GP/NW-device. *(b) I-V* curve before and after the contact shifted to ohmic behavior.

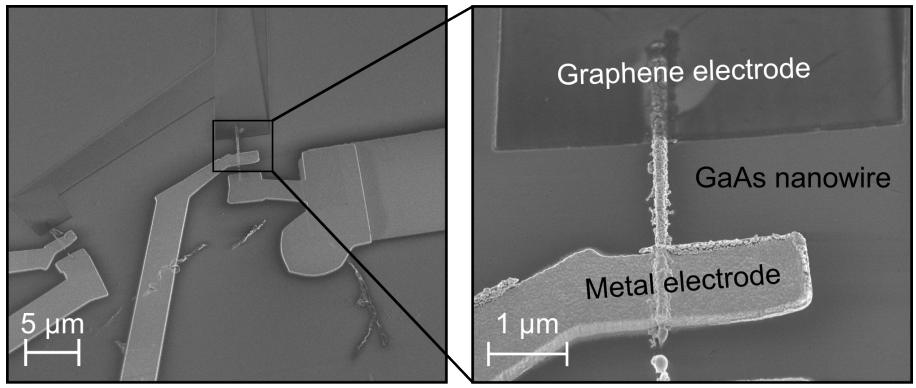


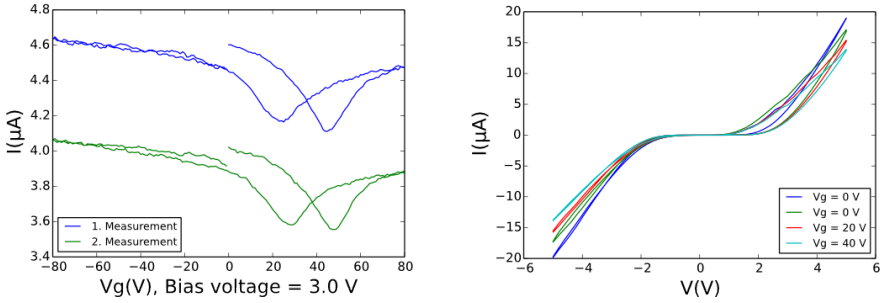
Figure 4.14: SEM images showing a GP/NW-device displaying linear behavior. Due to the layout of the contact lead arms, a shortening by graphene should be visible within the area showed in *(a)*. However, no visual trace of graphene shortening is seen in *(a)*, or in the close-up image *(b)*.

4.4.4 Gate voltage measurements

Two devices displaying high current (Figure 4.12a) and four devices displaying low current (Figure 4.12b were subjected to gate voltage measurements.

For the devices displaying high current, gate voltage sweeps in the linear area of the *I-V* curve would produce measurements as seen in Figure 4.15a. Though the current values were seen to seen to vary between measurements, the gate voltage values at the minimum current values were seen to consistently coincide with the Dirac points found in the graphene measurements. The resistance increase is however seen to exceed 50 kΩ, a value significantly larger than the resistance increase seen around the Dirac point for pure graphene measurements ($\sim$ 8 kΩ).

Figure 4.15b shows the *I-V* behavior found under different constant gate voltages. The effect of gate voltage is seen in the slope in the linear regime, while the shape and symmetry is seen to be unchanged.

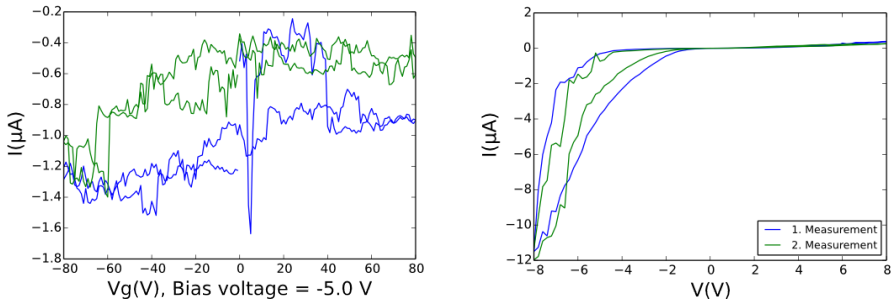


(a) (b)

Figure 4.15: *(a)* Current in a high current GP/NW-device plotted as a function of gate voltage, under constant bias voltage. The current minima coincide with the Dirac points found from pure graphene measurements. *(b) I-V* curves obtained under different constant gate voltage values. A smaller maximum current is observed for gate voltage values at the Dirac points. Two measurements at zero gate voltage is included to illustrate the variations associated with different measurements at the same gate voltage.

For devices displaying low current, gate voltage sweeps were always associated with a high degree of noise. Measurements were also dependent on

previous measurements, and often several voltage sweeps had to be conducted to obtain relatively reproducible results. For gate voltage sweeps at bias voltages in excess of 5 V in linear regime (less than -5V in Figure 4.16b), a trend of slightly decreasing current was observed, as seen Figure 4.16b. For gate voltage sweeps at bias voltages outside the linear region in the *I-V* curve, no consistent changes in current or resistance was observed.



(a) (b)

Figure 4.16: Current in a low current GP/NW-device plotted as a function of gate voltage, under constant bias voltage.*(b) I-V* curves from the same GP/NW-device.

Breakdown

In an effort to try to determine whether current was conducting through a GP/NW-device, breakdown tests were conducted on several GP/NW-devices.

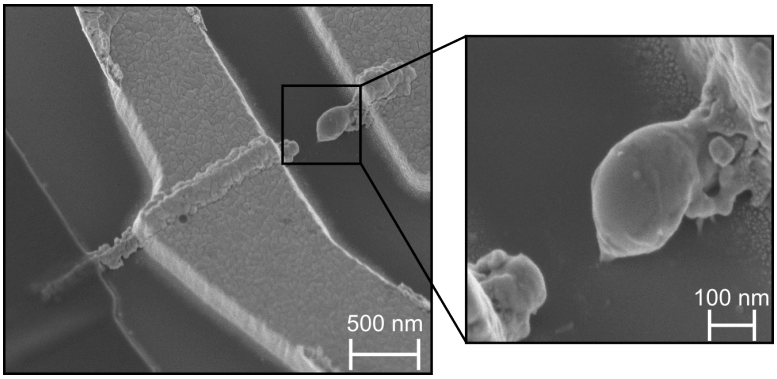
Initially, three MNWM-contacts were tested for breakdown by conducting *I-V* measurements without compliance current, increasing the range for the bias voltage sweep until breakdown was observed. All MNWM-contacts experienced breakdown when exposed to current values in excess 100 μA. Figure 4.17a shows one of these MNWM-contacts after breakdown. The breakdown seems to be caused by the nanowire melting, which is believed to be the result of Joule heating due to the nanowire resistance.

For GP/NW-devices displaying a low current, no breakdown test was conducted, as all the GP/NW-devices were found to break down during the gate voltage measurements. Figure 4.17b shows one of these GP/NW-device after breakdown, where the nanowire is seen to be extensively damaged. However

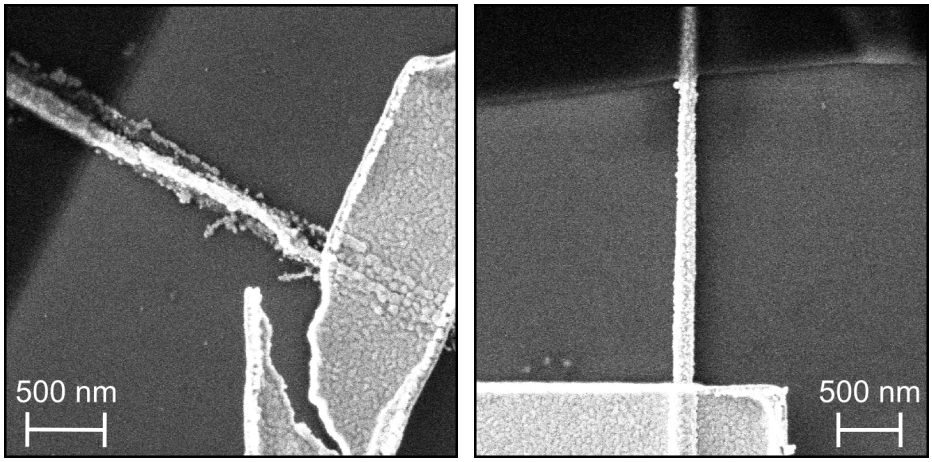
since no SEM investigation was conducted prior to the electrical measurements, it is difficult to determine whether the damage is primarily caused by electrical breakdown or corrosion from water exposure.

Two GP/NW-devices displaying high current were tested, and both found to break down at approximately 80 μA. As seen in Figure 4.17c, there was however to visual trace of the breakdown in the nanowire.

Finally the GP/NW-devices displaying linear behavior without any visual trace of graphene shortening were tested, and found to be able to sustain current values in excess of 700 μA without breaking down.



(a)



(b) (c)

Figure 4.17: SEM images showing devices after breakdown: *(a)* MNWM-contact. *(b)* GP/NW-device displaying low current. *(c)* GP/NW-device displaying high current.

Chapter 5

Discussion

5.1 Development of EBL procedure

The starting point for device fabrication for this thesis was the procedure developed in an earlier project [62]. This method can briefly be explained as first depositing an array with accurate positions, which can then be used as alignment points in 25 x 25 μm^2 , greatly increasing the accuracy of EBL patterning. The method was developed under the assumption that nanowire contacting was the most delicate step in the fabrication process, and that obtaining optimal accuracy was most important.

The initial graphene transfer results obtained were however found to give an indication that the nanowire contacts were not as stable as first believed. This required extensive testing with contacted nanowires, and it thus became evident that the substantial extra time length associated with the array method was impractical, and that a faster approach was necessary.

The two most critical factors for obtaining good EBL accuracy is the determination of nanowire coordinates relative to the substrate corners, and the choice of sample points for the write field alignment. Due to inaccuracies in the photolithography process used for fabricating the substrates, there will generally be offsets in the positions of contact arms leading into target areas. It was therefore found that utilizing the same points for write field alignment and giving coordinates to nanowires is paramount to obtain good accuracy. In addition, points should be chosen as close to the nanowire as possible. This is however not always an available option. Due to the unintentional exposure of the alignment points during write field alignment, points should not be placed

too close to devices. This exposure also implies that new alignment points must be chosen for each EBL process, as previous points will be hidden under metal or hardened resist.

During the course of this thesis it was found that the offset associated with placing alignment points far away from the nanowire was somewhat consistent in length and direction. This made it possible to make an estimate of the potential offset based on previous experiences. In addition it was also observed that as long as one alignment point was close to a nanowire, pattern offsets were never seen to exceed 0.5 µm. Based on these observations it was possible to design larger nanowire contacts that would account for offset. This meant the alignment process could be conducted in a shorter time, as the nanowire contacts were not dependent on perfect alignment to be successfully contacted. By introducing the step of *Origin correction* it was also found that the time needed to attain sufficient alignment by sample stage movement was significantly reduced.

The success of the new development for the EBL procedure is also credited to two sample specific factors. SiO_2-substrates were found to have much more defined corners than observed in Si_3N_4, where the corners were generally found to be smeared out, making the it difficult to determine an exact corner coordinate. Also the nanowires utilized in this thesis (SC369) were generally long enough to allow for the bigger contact design.

5.2 Nanowire measurements

Based on the discussion in section 2.3.1, we expect the MNWM-contacts to form a back-to-back diode system, i.e. two Schottky barriers with opposite orientation. The contacting scheme utilized for nanowires contacts are known to be capable of forming ohmic contacts to GaAs, but this requires thermal annealing after contacting [67]. This was not attempted for any devices in this thesis, as it is suspected that the rapid thermal process would destroy the graphene. While graphene have been shown to have thermal stability up to 2300 °C[6], the PMMA remnant layer lying on top are thought to only be able to sustain temperatures up to 300 °C before cracking.

As seen in Section 4.4.1, a variety of different *I-V* characteristics were observed. Based on previous studies on the *I-V* behavior in GaAs nanowires [39, 62, 67], the observed IV-results are generally less stable and consistent than expected. Variations in slope and current magnitudes and the presence of hysteresis are expected behavior for this kind of system, and can be explained in

terms of local variations of for example doping, nanowire diameter, and charge trapping at the contact interface. The inconsistency of the devices measured in this thesis indicates that the effect of these effects is increased for devices exposed to water. The unstable *I-V* behavior is therefore thought to be the result of corrosion.

In the presence of water, GaAs is thermodynamically inclined to produce Ga and As oxides, which can dissolve in water [66]. Huang et al. have found that a corrosion process is dependent of the hole concentration at the surface, which implicate that the nanowires studied in this thesis would be especially vulnerable to etching, as these are highly p-doped. As the corrosion appears to make the nanowire rugged and uneven, there is a possibility that the different oxides dissolve at different rates, which would impact the doping concentration at the surface.

5.3 Graphene measurements

The graphene-metal contacting scheme utilized in this thesis have been demonstrated in several other studies [40] [47]. Although graphene strain could potentially affect the device transport characteristics, Chen et al. have shown that no effect of straining is seen with Raman spectroscopy. It is thus expected that the graphene-metal contacts will display ohmic behavior. For all but one MGM-contact measured in this thesis, rectifying behavior was observed initially, before a sudden shift to linear behavior seen under prolonged application of bias voltage. This is seen as a sign of graphene not achieving intimate contact with the metal at first. The shift to ohmic behavior is thought to be the result of a Joule heating induced annealing, where the power dissipation associated with the contact resistance heats the interface to the point where an intimate contact occurs.

Gate voltage measurements on graphene show the resistance increase associated with the Dirac point to be dependent on direction it is approached from, i.e. the resistance peak is produced at different gate voltage when the gate voltage is increasing, than when the gate voltage is decreasing. This hysteresis is thought to be the result of charge trapping in the SiO_2. When first increasing the gate voltage, charges can be trapped at the graphene/SiO_2 interface. This implies that the surface charge is different when the gate voltage is decreased to zero again, which is why the resistance peak is observed for another value.

5.4 Graphene-nanowire device measurements

As GP/NW-devices were only obtained at a late stage for this thesis, only preliminary investigations could be conducted. Because of the observed uncertainties in MNWM-contacts, the results in this thesis are thought to be unsuitable for quantitative analysis. The following discussion will therefore be centered around the observed results seen in light of the expected behavior from Section 2.3.3.

5.4.1 Field effect in GaAs nanowire

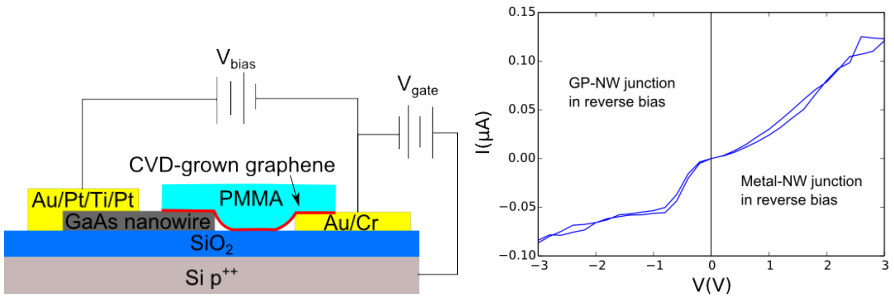
Due to the device design, the GaAs nanowire is also subjected to the same gate voltage as the graphene during electrical measurement. We therefore consider whether the gate voltage is capable of inducing a depletion region in the nanowire large enough to affect the conductivity of the nanowire. In order to determine the effect of a gate voltage on the GaAs nanowire, the *Debye screening length* can be calculated. The *Debye screening length* is the length at which charge imbalances in a material are smeared out or screened due to the accumulation of mobile charge carriers [1, p. 275], and is defined as

$$L_D = \sqrt{\frac{\epsilon_0 \epsilon_r kT}{q^2 p_0}} \tag{5.1}$$

, where ϵ_0 is the electrical permittivity in vacuum, ϵ_r is the relative permittivity, k is the Boltzmann constant, T is the temperature, q is the elementary charge, and p_0 is the hole concentration (For an n-type semiconductor, the electron concentration should be utilized). The hole concentration of the GaAs nanowires is not readily available, due to the difficulty in knowing the exact doping concentration (Section 2.5). The doping concentration is therefore set as $N_A = 10^{18}\text{cm}^{-3}$, which is believed to be a lower bound of what can be expected. As the intrinsic carrier concentration of GaAs at room temperature is $n_i = 2 \cdot 10^6\text{cm}^{-3}$ [1, p. 95], we set $p_0 \approx N_a = 10^{18}$. The permittivity of GaAs is set as $\epsilon_r = 13.1$ [35, p. 277], and the expression is then calculated as

$$L_D = 4.33 \cdot 10^{-9}\ \text{m} = 4.33\ \text{nm} \tag{5.2}$$

It is thus assumed that the effect of an applied gate voltage is screened within ~ 5 nm. Since this is a small number compared to the diameter of the nanowires (~ 200 nm), it is therefore assumed that the application of a gate voltage will have negligible impact on the conductivity of the GaAs nanowire.



(a) (b)

Figure 5.1: *(a)* Schematic overview of the GP/NW-device. The graphene electrode is connected to ground. *(b)* IV-curve illustrating how GP-NW device systems can be divided into one part dominated by a GPSC-junction in reverse bias, while the other part is dominated by a MSC-junction in reverse bias.

5.4.2 Expectations from theory

From the discussion in Section 2.3.3, we expect that a Schottky barrier will form both at the metal-nanowire interface and at the graphene-nanowire interface. This means that the GP/NW-devices will form a back-to-back diode system, where one junction will always be reverse biased. As the resistance of a reverse junction is generally much larger than the resistance of a forward biased junction, we make the assumption that the voltage drop over the forward biased junction is negligible. The system can be divided into one part dominated by a MSC-junction in reverse bias, and one part dominated by a GPSC-junction in reverse bias, as illustrated in Figure 5.1. This implies that the effect of the GPSC-junction will only be visible in the reverse bias regime, as the forward bias regime will effectively be masked by the GPSC-junction operating in reverse bias.

Because of the high density of surface states in GaAs (Section 2.3.1) we expect the system to be approximated by the Bardeen limit, implying that the barrier height will be mostly independent from the work function of the contacting material. We therefore expect the barrier height to only show a small dependence of the graphene Fermi level, which should be much smaller than the dependence observed for the graphene-silicon systems. For gate-voltage

measurements we expect that the measured current will be reduced as the graphene Fermi level is shifted from p-type to n-type.

5.4.3 *I-V* measurements - linear behavior

The appearance of linear behavior for regarded as unrealistic result for GP/NW-devices, as this would imply an ohmic contact for both the GPSC-junction and the MSC-junction. This is ruled out be the MNWM-contacts measurements, which clearly indicate rectifying behavior. Due to the high magnitude of current in these *I-V* curves ($\sim$ 150 µA at 3 V), it is also believed that the possibility of some unknown high resistance effect "masking" the effect of the Schottky barrier can be ruled out. While two devices were visually confirmed to be shortened by graphene, the linear behavior was also observed for three devices showing no visual sign of graphene shortening. No indication of shortening was found even after extensive investigation by SEM along the entire length of the contact arms up to connect pads. How these devices can be shortened by graphene without showing any visual sign is not understood, as both optical inspection and electrical investigation indicate that all but the wrinkled up graphene is removed by plasma ashing during the graphene trimming (Section 3.7).

5.4.4 *I-V* measurements - high current behavior

For the GP/NW-devices displaying high currents, the gate voltage measurements are seen to produce current minimums at the gate voltages that coincide with the Dirac point found from the pure graphene measurements. While the resistance increase associated with the Dirac point should be present also for the GP/NW-device, the effect is not expected to be as pronounced as observed in these devices. While the resistance increase in the graphene measurements were found to be ~ 8 kΩ, the resistance increase for GP/NW-devices were found to exceed 50 kΩ for all measurements. These resistance values are thought to be too large to be credited to the graphene electrode in the GP/NW-device, and it is there suspected that these device are also shortened by graphene. However, this can not be confirmed without investigation the gate voltage dependent resistivity for graphene, so an accurate estimate of the resistance increase based on the size of the graphene electrode can be made. Furthermore, these devices were never seen to shift to ohmic behavior, and breakdown tests also found the devices to break down at approximately 80 µA, which is much lower than the current the graphene contacts were observed to be able to sustain without

breaking down. This breakdown was however not visible in the device after the breakdown, unlike breakdowns for MNWM-contact, where the nanowire is seen to be severed by melting. The breakdown test can therefore not be used to determine whether a current has been passed through the GP/NW-device. It is therefore believed that more tests are necessary to determine the true nature of this behavior.

5.4.5 *I-V* measurements - low current behavior

For the GP/NW-devices displaying low current, the *I-V* curves were often seen to saturate in one direction. This saturation was however not consistent with the applied bias, implying that the current was sometimes seen to saturate for GPSC-junctions in reverse bias, and sometimes for MSC-junctions in reverse bias. This is unexpected behavior from both junctions considering the high doping concentration of the nanowires, and thus a strong indication that these devices were not functioning as intended. Although the low current behavior can be explained in terms of the graphene and GaAs nanowire not achieving intimate contact, it is first and foremost believed be the result of extensive water corrosion, because of the similar behavior observed for corrodedMNWM-contacts. This is backed up by the images from the subsequent SEM investigation, where the low current devices were seen to appear extensively damaged by corrosion.

The gate voltage measurements show a decreasing bias current for increasing gate voltage, which is in line with the expectations. It is however believed that this system will be dominated by a very high resistance and unstable behavior arising from the severely corroded nanowire, making it hard to determine which effects arise from the GPSC-junctions.

Chapter 6

Conclusion

In this thesis, a fabrication process for GP/NW-devices using EBL processing techniques is presented and demonstrated. Fabricated devices were characterized by measuring gate depdendent I-V characteristics. The procedure used for EBL was developed with an emphasis on speed and simplicity, and successfully demonstrated by fabricating GaAs nanowire 2-probe and 4-probe devices. It was found that inaccuracies in the EBL pattern could be estimated and accounted for in the contact design, thus allowing for successful contacting without perfect alignment.

For ExG-devices, samples were sent to Konkuk University, Korea, where a PMMA-mediated transfer of exfoliated graphene was conducted. Transfer was first attempted on contacted nanowires, but this was unsuccessful due to the difficulty of placing graphene flakes near the relatively thick nanowire contacts. Exfoliated graphene was however successfully transferred to substrates containing uncontacted nanowires. The graphene flakes were destroyed during the subsequent processing at NTNU, and no measurable ExG-devices were thus obtained. It is concluded that the outlined fabrication process is unsuitable for exfoliated graphene.

To transfer CVD-grown graphene, a PMMA-mediated transfer process was tested and optimized. While the graphene transfer was found to be successful, the water exposure associated with the transfer process was seen to cause significant corrosion in GaAs nanowires. This was an especially prominent issue for contacted nanowires, and is credited to the metal contact acting as a cathode causing galvanic corrosion in the nanowire [66]. This is also thought to be the reason for the observed disappearance of nanowires following graphene transfer

observed in an earlier project [62]. Due to the galvanic corrosion, nanowires had to be contacted after the graphene transfer. This excluded the possibility of annealing the nanowire-metal contacts, as the rapid thermal process used for annealing is thought to be incompatible with conserving graphene quality.

I-V measurements of MNWM-contacts exposed to water displayed a much more inconsistent and unstable behavior than expected from earlier results. This behavior is credited to the observed corrosion. In addition to reducing the nanowire diameter in an unpredictable manner, the corrosion is thought to create unpredictable conditions at the contact interfaces, due to the possibility that dopant atoms oxidizing and dissolving at different rates than gallium and arsenide.

A total of 16 CVDG-devices were obtained and measured, and found to display a variety of different *I-V* behaviors. Some devices were found to display linear behavior, and it is believed that this can only be the result of shortening by graphene. This shortening was however not visible during investigation by SEM. How a shortening by graphene can occur without being visible in the SEM is currently not understood. In addition to linear behavior, there were two notable trends in the *I-V* measurements. The first trend was a relatively stable and high current observed in *I-V* curves. In gate voltage measurements, these devices showed large increases in resistance around the Dirac point of graphene, which is unexpected from GPSC-junction theory. It is therefore suspected that these devices are in fact also shortened by graphene, but without knowing gate voltage dependence on resistivity for graphene, no conclusion can be made. The second trend is an unstable and relatively low current observed in *I-V* curves. These devices display a decreasing current for positive gate voltages, which is in line with what is expected from theory and published studies. The highly resistive and unstable nature of these devices is however believed to first and foremost be the result of corrosion, and it is therefore difficult to interpret the data from these devices.

Based on the uncertainties thought to be introduced by the corrosion in nanowires, the *I-V* measurements are found to be inconclusive. It is thus concluded that further developments in the fabrication process is needed to obtain samples suitable to properly characterize the graphene-GaAs nanowire contact.

Chapter 7

Further work

Following the conclusions reached in the present study, a further development of the fabrication process is suggested.

In order to obtain ExG-device, no spin coating should be conducted after the first removal of PMMA. As the nanowires have to be uncontacted to conduct the exfoliated graphene transfer, this implies that graphene and nanowire would have to be contacted with the same EBL step. This could prove to be a feasible method, as all the metals used in for the nanowire contacts have been shown to make good contacts to graphene [68].

To improve the fabrication process for CVDG-device it is considered paramount to develop a transfer process without exposing nanowires to water. This can be done by investigating methods for dry transfer [69], or by developing a reliable method for transferring the graphene/PMMA layer to a solution of IPA after the Cu etching. This transfer process should also be performed after contacting the nanowire, so that a thermal annealing of the nanowire contacts is possible. Obtaining an ohmic contact between the metal electrode and the GaAs nanowire would greatly benefit the analysis of graphene-GaAs nanowire junction, because this would allow the junction to be investigated in forward bias. An investigation of graphene resistivity as a function of gate voltage is also suggested, as this would enable a more accurate estimate of the resistance increase in the graphene electrode associated with the Dirac point.

Bibliography

[1] Ben G. Streetman and Sanjay Banerjee. *Solid state electronic devices.* Number 6th ed. Pearson/Prentice-Hall, Upper Saddle River, N.J., 2006.

[2] Mark Lundstrom. Moore's Law Forever? *Science*, 299(5604):210–211, 2003.

[3] Gabor L. Hornyak. *Introduction to nanoscience & nanotechnology.* CRC Press, Boca Raton, Fla., 2009.

[4] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov. Electric Field Effect in Atomically Thin Carbon Films. *Science*, 306(5696):666–669, 2004.

[5] Changgu Lee, Xiaoding Wei, Jeffrey W. Kysar, and James Hone. Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene. *Science*, 321(5887):385–388, 2008.

[6] Alexander A. Balandin, Suchismita Ghosh, Wenzhong Bao, Irene Calizo, Desalegne Teweldebrhan, Feng Miao, and Chun Ning Lau. Superior Thermal Conductivity of Single-Layer Graphene. *Nano Lett.*, 8(3):902–907, 2008.

[7] A. K. Geim. Graphene: Status and Prospects. *Science*, 324(5934):1530–1534, 2009.

[8] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim. The electronic properties of graphene. *Rev. Mod. Phys.*, 81(1):109–162, 2009.

[9] K.I. Bolotin, K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H.L. Stormer. Ultrahigh electron mobility in suspended graphene. *Solid State Communications*, 146:351–355, 2008.

[10] Dharmendar Reddy, Leonard F Register, Gary D Carpenter, and Sanjay K Banerjee. Graphene field-effect transistors. *Journal of Physics D: Applied Physics*, 44(31):313001, 2011.

[11] Kinam Kim, Jae-Young Choi, Taek Kim, Seong-Ho Cho, and Hyun-Jong Chung. A role for graphene in silicon-based semiconductor devices. *Nature*, 479(7373):338–344, 2011.

[12] Peidong Yang, Ruoxue Yan, and Melissa Fardy. Semiconductor Nanowire: What's Next? *Nano Lett.*, 10(5):1529–1536, 2010.

[13] Thomas J. Kempa, Robert W. Day, Sun-Kyung Kim, Hong-Gyu Park, and Charles M. Lieber. Semiconductor nanowires: a platform for exploring limits and concepts for nano-enabled solar cells. *Energy Environ. Sci.*, 6(3):719–733, 2013.

[14] R. Agarwal and C.M. Lieber. Semiconductor nanowires: optics and optoelectronics. 85(3):209–215–, 2006.

[15] Erik C. Garnett, Mark L. Brongersma, Yi Cui, and Michael D. McGehee. Nanowire Solar Cells. *Annual Review of Materials Research*, 41(1):269–295, 2011.

[16] Ethan D. Minot, Freek Kelkensberg, Maarten van Kouwen, Jorden A. van Dam, Leo P. Kouwenhoven, Valery Zwiller, Magnus T. Borgström, Olaf Wunnicke, Marcel A. Verheijen, and Erik P. A. M. Bakkers. Single Quantum Dot Nanowire LEDs. *Nano Lett.*, 7(2):367–371, 2007.

[17] Xiangfeng Duan, Yu Huang, Ritesh Agarwal, and Charles M. Lieber. Single-nanowire electrically driven lasers. *Nature*, 421(6920):241–245, 2003.

[18] Yi Cui, Xiangfeng Duan, Jiangtao Hu, and Charles M. Lieber. Doping and Electrical Transport in Silicon Nanowires. *J. Phys. Chem. B*, 104(22):5213–5216, 2000.

[19] Peter Krogstrup, Henrik Ingerslev Jorgensen, Martin Heiss, Olivier Demichel, Jeppe V. Holm, Martin Aagesen, Jesper Nygard, and Anna Fontcuberta i Morral. Single-nanowire solar cells beyond the Shockley-Queisser limit. *Nat Photon*, 7(4):306–310, 2013.

[20] A. Mazid Munshi, Dasa L. Dheeraj, Vidar T. Fauske, Dong-Chul Kim, Antonius T. J. van Helvoort, Bjørn-Ove Fimland, and Helge Weman. Vertically Aligned GaAs Nanowires on Graphite and Few-Layer Graphene: Generic Model and Epitaxial Growth. *Nano Lett.*, 12(9):4570–4576, 2012.

[21] A. Mazid Munshi and Helge Weman. Advances in semiconductor nanowire growth on graphene. *Phys. Status Solidi RRL*, 7(10):713–726, 2013.

[22] A V Babichev, V E Gasumyants, A Yu Egorov, S Vitusevich, and M Tchernycheva. Contact properties to CVD-graphene on GaAs substrates for optoelectronic applications. *Nanotechnology*, 25(33):335707, 2014.

[23] S. Tongay, M. Lemaitre, X. Miao, B. Gila, B. R. Appleton, and A. F. Hebard. Rectification at Graphene-Semiconductor Interfaces: Zero-Gap Semiconductor-Based Diodes. *Phys. Rev. X*, 2(1):011002–, 2012.

[24] Charles Kittel and Paul McEuen. *Introduction to solid state physics*. Number 8th ed. Wiley, Hoboken, N.J., 2005.

[25] I. Vurgaftman, J. R. Meyer, and Ram-Mohan. Band parameters for III-V compound semiconductors and their alloys. *Journal of Applied Physics*, 89(11):5815–5875, 2001.

[26] E.H. Rhoderick and R.H. Williams. *Metal-semiconductor contacts*. Number 2nd ed. Clarendon Press, Oxford, 1988.

[27] Raymond T. Tung. The physics and chemistry of the Schottky barrier height. *Applied Physics Reviews*, 1(1):–, 2014.

[28] P. R. Wallace. The Band Theory of Graphite. *Phys. Rev.*, 71:622–634, 1947.

[29] A. K. Geim and A. H. MacDonald. Graphene: Exploring Carbon Flatland. *Physics Today*, 60(8):080000, 2007.

[30] A. K. Geim and K. S. Novoselov. The rise of graphene. *Nat Mater*, 6(3):183–191, 2007.

[31] P. Blake, E. W. Hill, A. H. Castro Neto, K. S. Novoselov, D. Jiang, R. Yang, T. J. Booth, and A. K. Geim. Making graphene visible. *Applied Physics Letters*, 91(6):–, 2007.

[32] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, and A. K. Geim. Raman Spectrum of Graphene and Graphene Layers. *Phys. Rev. Lett.*, 97:187401, 2006.

[33] Yi Zhang, Luyao Zhang, and Chongwu Zhou. Review of Chemical Vapor Deposition of Graphene and Related Applications. *Acc. Chem. Res.*, 46(10):2329–2339, 2013.

[34] Yung-Chang Lin, Chun-Chieh Lu, Chao-Huei Yeh, Chuanhong Jin, Kazu Suenaga, and Po-Wen Chiu. Graphene Annealing: How Clean Can It Be? *Nano Lett.*, 12(1):414–419, 2011.

[35] A. G Baca and Carol Iris Hill Ashby. Fabrication of GaAs devices, 2009.

[36] Z. Y. Zhang, C. H. Jin, X. L. Liang, Q. Chen, and L.-M. Peng. Current-voltage characteristics and parameter retrieval of semiconducting nanowires. *Applied Physics Letters*, 88(7):–, 2006.

[37] Z. Zhang, K. Yao, Y. Liu, C. Jin, X. Liang, Q. Chen, and L.-M. Peng. Quantitative Analysis of Current-Voltage Characteristics of Semiconducting Nanowires: Decoupling of Contact Effects. *Adv. Funct. Mater.*, 17(14):2478–2489, 2007.

[38] Adenilson J Chiquito, Cleber A Amorim, Olivia M Berengue, Luana S Araujo, Eric P Bernardo, and Edson R Leite. Back-to-back Schottky diodes: the generalization of the diode theory in analysis and extraction of electrical parameters of nanodevices. *Journal of Physics: Condensed Matter*, 24(22):225303–, 2012.

[39] Maximilian Erlbeck. Probing the Electronic Properties of P-Doped Gallium Arsenide Nanowires. Master's thesis, Department of Physics, Faculty of Natural Sciences and Technology, NTNU, 2014.

[40] Chun-Chung Chen, Mehmet Aykol, Chia-Chi Chang, A. F. J. Levi, and Stephen B. Cronin. Graphene-Silicon Schottky Diodes. *Nano Lett.*, 11(5):1863–1867, 2011.

[41] S. Tongay, T. Schumann, and A. F. Hebard. Graphite based Schottky diodes formed on Si, GaAs, and 4H-SiC substrates. *Applied Physics Letters*, 95(22):–, 2009.

[42] Haijian Zhong, Ke Xu, Zhenghui Liu, Gengzhao Xu, Lin Shi, Yingmin Fan, Jianfeng Wang, Guoqiang Ren, and Hui Yang. Charge transport mechanisms of graphene/semiconductor Schottky barriers: A theoretical and experimental study. *Journal of Applied Physics*, 115(1):–, 2014.

[43] Xinming Li, Hongwei Zhu, Kunlin Wang, Anyuan Cao, Jinquan Wei, Chunyan Li, Yi Jia, Zhen Li, Xiao Li, and Dehai Wu. Graphene-On-Silicon Schottky Junction Solar Cells. *Adv. Mater.*, 22(25):2743–2748, 2010.

[44] Chanyoung Yim, Niall McEvoy, and Georg S. Duesberg. Characterization of graphene-silicon Schottky barrier diodes using impedance spectroscopy. *Applied Physics Letters*, 103(19):–, 2013.

[45] Y. Xu, K. T. He, S. W. Schmucker, Z. Guo, J. C. Koepke, J. D. Wood, J. W. Lyding, and N. R. Aluru. Inducing Electronic Changes in Graphene through Silicon (100) Substrate Modification. *Nano Letters*, 11(7):2735–2742, 2011.

[46] Heejun Yang, Jinseong Heo, Seongjun Park, Hyun Jae Song, David H. Seo, Kyung-Eun Byun, Philip Kim, InKyeong Yoo, Hyun-Jong Chung, and Kinam Kim. Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier. *Science*, 336(6085):1140–1143, 2012.

[47] Chun-Chung Chen, Chia-Chi Chang, Zhen Li, A. F. J. Levi, and Stephen B. Cronin. Gate tunable graphene-silicon Ohmic/Schottky contacts. *Applied Physics Letters*, 101(22):–, 2012.

[48] Jung Min Lee, Jae Woong Choung, Jaeseok Yi, Dong Hyun Lee, Monica Samal, Dong Kee Yi, Chul-Ho Lee, Gyu-Chul Yi, Ungyu Paik, John A. Rogers, and Won Il Park. Vertical Pillar-Superlattice Array and Graphene Hybrid Light Emitting Diodes. *Nano Lett.*, 10(8):2783–2788, 2010.

[49] Wenjing Jie, Fengang Zheng, and Jianhua Hao. Graphene/gallium arsenide-based Schottky junction solar cells. *Applied Physics Letters*, 103(23):–, 2013.

[50] Michael Quirk and Julian Serda. *Semiconductor manufacturing technology*. Prentice Hall, Upper Saddle River, N.J., 2001.

[51] R. S. Wagner and W. C. Ellis. VAPOR-LIQUID-SOLID MECHANISM OF SINGLE CRYSTAL GROWTH. *Applied Physics Letters*, 4(5):89–90, 1964.

[52] Y. Xia, P. Yang, Y. Sun, Y. Wu, B. Mayers, B. Gates, Y. Yin, F. Kim, and H. Yan. One-Dimensional Nanostructures: Synthesis, Characterization, and Applications. *Adv. Mater.*, 15(5):353–389, 2003.

[53] Z.H. Wu, X.Y. Mei, D. Kim, M. Blumin, and H.E. Ruda. Growth of Au-catalyzed ordered GaAs nanowire arrays by molecular-beam epitaxy. *Applied Physics Letters*, 81(27):5177–5179, 2002.

[54] C Colombo, D Spirkoska, M Frimmer, G Abstreiter, and A Fontcuberta i Morral. Ga-assisted catalyst-free growth mechanism of GaAs nanowires by molecular beam epitaxy. *Physical Review B*, 77(15):155326, 2008.

[55] Steffen Breuer, Carsten Pfuller, Timur Flissikowski, Oliver Brandt, Holger T. Grahn, Lutz Geelhaar, and Henning Riechert. Suitability of Au- and Self-Assisted GaAs Nanowires for Optoelectronic Applications. *Nano Letters*, 11(3):1276–1279, 2011.

[56] Alberto Casadei, Peter Krogstrup, Martin Heiss, Jason A. Röhr, Carlo Colombo, Thibaud Ruelle, Shivendra Upadhyay, Claus B. Sörensen, Jesper Nygård, and Anna Fontcuberta i Morral. Doping incorporation paths in catalyst-free Be-doped GaAs nanowires. *Applied Physics Letters*, 102(1):–, 2013.

[57] Åsmund Bakke Bø. Fabrication and Characterization of Single GaAs Nanowire Devices. Master's thesis, NTNU, 2010.

[58] Rainer Waser. *Nanoelectronics and information technology: advanced electronic materials and novel devices.* Number 3rd ed., completely rev. and enl. ed. Wiley-VCH, Weinheim, 2012.

[59] David B. Williams and C. Barry Carter. *Transmission electron microscopy: a textbook for materials science.* Number 2nd ed. Springer, New York, 2009.

[60] R.F. Egerton. *Physical principles of electron microscopy: an introduction to TEM, SEM, and AEM.* Springer, New York, 2007.

[61] Raith Gmbh. *Raith software reference manual.* Raith GmbH, Hauert 18, 44227 Dortmund, Germany, v.5 edition, 2007.

[62] Ambjørn Dahle Bang. Development of Electron Beam Lithography Processes for Fabrication of GaAs Nanowire/Graphene Hybrid Devices. Master's thesis, NTNU, 2013.

[63] Ole Morten Christoffersen. Contacts to P-doped GaAs Nanowires by Fabrication of Electrodes using Metals and Graphene. Master's thesis, NTNU, 2012.

[64] A C F Hoole, M E Welland, and A N Broers. Negative PMMA as a high-resolution resist - the limits and possibilities. *Semiconductor Science and Technology*, 12(9):1166, 1997.

[65] Huigao Duan, Donald Winston, Joel K W Yang, Bryan M. Cord, Vitor R. Manfrinato, and K.K. Berggren. Sub-10-nm half-pitch electron-beam lithography by using poly(methyl methacrylate) as a negative resist. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 28(6):C6C58–C6C62, 2010.

[66] Yin Huang, Jingli Luo, and Douglas G. Ivey. Comparative study of GaAs corrosion in H2SO4 and NH3 · H2O solutions by electrochemical methods and surface analysis. *Materials Chemistry and Physics*, 93(3):429–442, 2005.

[67] D.L. Dheeraj, A.M. Munshi, O.M. Christoffersen, D.C. Kim, G. Signorello, H. Riel, A.T.J. van Helvoort, H. Weman, and B.O. Fimland. Comparison of Be-doped GaAs nanowires grown by Au- and Ga-assisted molecular beam epitaxy. *Journal of Crystal Growth*, 378(0):532–536, 2013.

[68] Joshua A. Robinson, Michael LaBella, Mike Zhu, Matt Hollander, Richard Kasarda, Zachary Hughes, Kathleen Trumbull, Randal Cavalero, and David Snyder. Contacting graphene. *Applied Physics Letters*, 98(5):–, 2011.

[69] Ji Won Suk, Alexander Kitt, Carl W. Magnuson, Yufeng Hao, Samir Ahmed, Jinho An, Anna K. Swan, Bennett B. Goldberg, and Rodney S. Ruoff. Transfer of CVD-Grown Monolayer Graphene onto Arbitrary Substrates. *ACS Nano*, 5(9):6916–6924, 2011.

Appendices

Appendix **A**

Substrate Dimensions

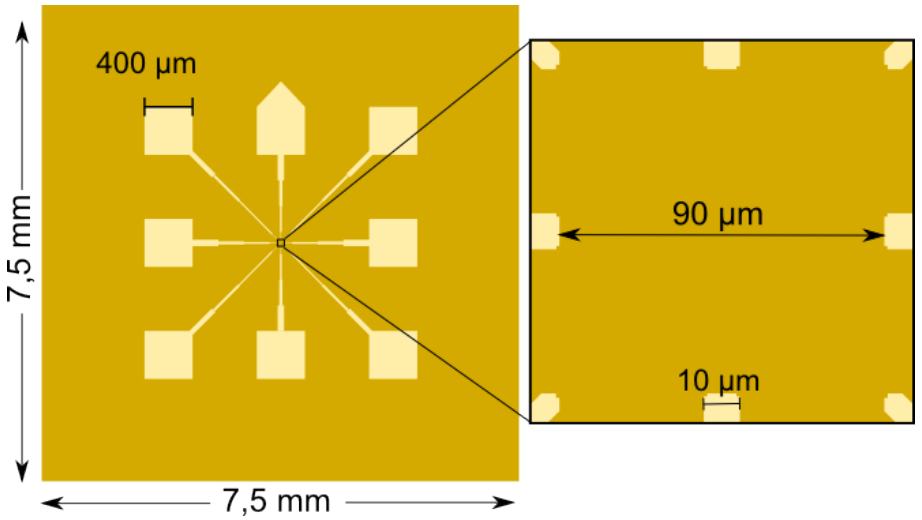
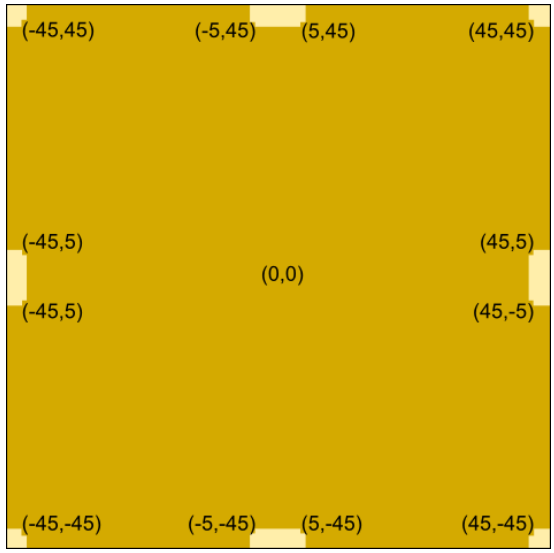
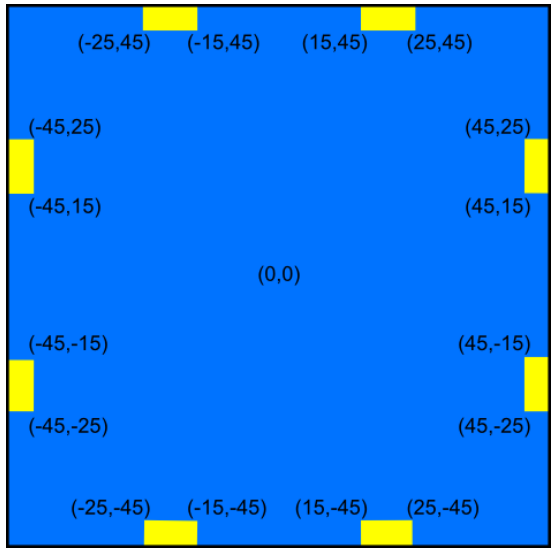


Figure A.1: Illustration demonstrating the dimensions of Si_3N_4-substrates. Close-up image shows the area intended for further processing by EBL, referred to as a target area.



(a)



(b)

Figure A.2: Figure showing the coordinates given to the corners in the target areas of: *(a)* Si_3N_4-substrates. *(b)* SiO_2-substrates.

Appendix **B**

EBL procedure

B.1 Overview

In this chapter an accurate description of the EBL procedure developed and utilized in this thesis is given. The EBL procedure can be summarized in the following steps:

1. Sample mounting and insertion - Section B.2
2. Beam current adjustment - Section B.4
3. Beam alignment - Section B.4
4. Rotation and angle correction - Section B.5
5. Locating target area- Section B.6
6. Position correction - Section B.7
7. Stage movement alignment - Section B.8
8. Write field alignment - Section B.9
9. Exposure - Section B.10
10. Sample unloading - Section B.11

B.2 Sample mounting and insertion

First the stage is retrieved by evacuating the loading chamber, and unscrewing it. The substrates are then inserted into the sample holder using the clamp. Care should be taken to line the sample approximately parallel to stage walls, as demonstrated in Figure B.1, to ease later alignment. Make sure that the samples are lying horizontally with respect to the sample holder, i.e. there is no gap between the sample and stage. Any gap will cause height differences across the sample, which can have significant impact on patterning accuracy. If any gap is present, the sample should be placed upside down on a wipe and carefully scraped with a scalpel to remove any unevenness from the sample back side. After this treatment, it should be possible to place the samples in the stage with no visible gap. The stage is then screwed on the sample stage holder, and loading chamber vacuum is turned on. The chamber door can then be opened, and the stage is carefully inserted into the larger stage in the sample chamber. After the holder had been pulled back, one closes the chamber door and opens the door to the electron column. The beam can then be turned on after choosing the appropriate acceleration voltage.

B.3 Beam current adjustment

The sample stage can then be moved to the correct height and centered above the faraday cup, the area of the sample stage used to measure beam current. This is done by using the predefined positions in the Raith software. The *Faraday cup_21052010* position is chosen, followed by clicking go. Next the beam current and alignment is adjusted, which is done from the Hitachi software. The control between Raith and Hitachi can be switched by clicking external and internal in the Raith control. There is also an option for beam deflection, which stops the beam without changing position. After turning off beam deflection, the faraday cup should become visible as a dark circle in the Hitachi computer screen. One can then proceed to measure the beam current by by centering the beam on the faraday cup, go to 400-500kx magnification to make sure the entire beam goes into this spot, and turn on the external current measurement apparatus. The beam current can then be adjusted via the column setup menu, shown in Figure B.2a, and adjusting the condenser lenses.

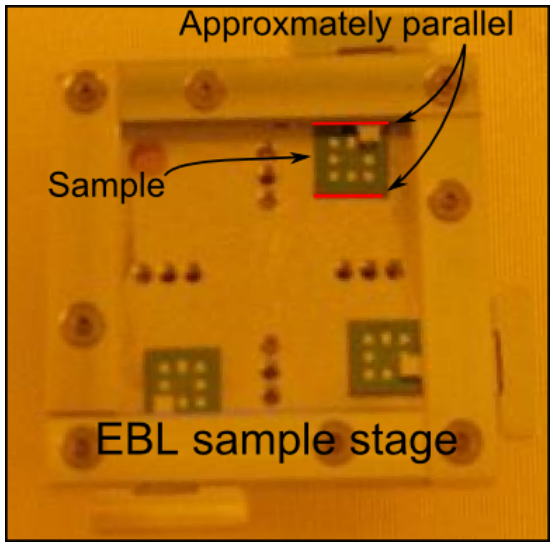
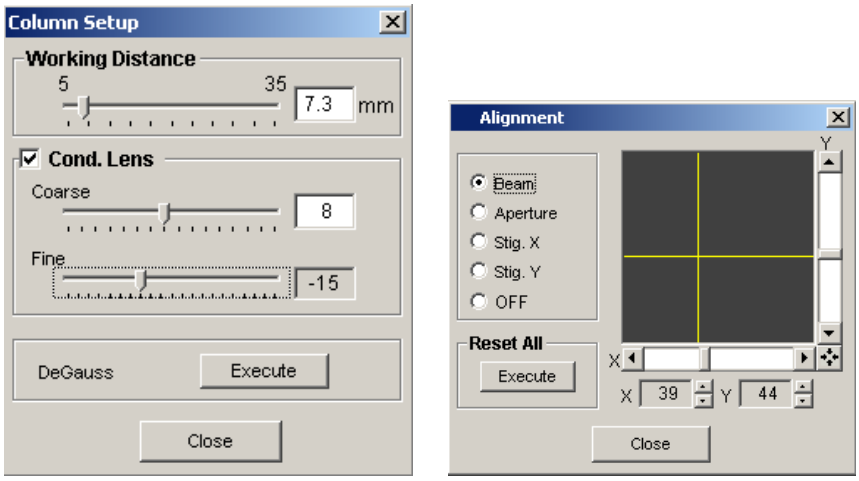


Figure B.1: Demonstration of correct sample placement relative to the sample stage.

B.4 Beam alignment

After the desired beam current has been found, the beam has to be aligned for this current, i.e. one has to account for astigmatism[1] in the lense system. This can be done via four settings; beam, aperture, x stig., and y stig.; as shown in Figure B.2b. First a feature easily distinguishable from its surroundings should be found.Zoom on to this feature and focus the image as sharp as possible. Such features can for example be found on the edge of the faraday cup. The beam alignment menu should then be entered, and one can start by adjusting to the wanted beam size, and correcting x- and y settings so that the beam is centered on the cross. This corrects actual beam position to the beam position used by the software. Then the values for aperture, x stig., y-stig. settings should be corrected. These settings lets one view the features while software shifts the focus to slightly defocus and then back to

[1] Astigmatism is uneven focus in x- and y-directions, making the image distorted from its real dimensions, i.e. a square can appear to have rectangular shape with incorrect alignment settings.



(a) (b)

Figure B.2: *(a)* Menu for adjusting beam current. *(b)* Menu for correcting astigmatism.

focus in an oscillatory manner. This makes astigmatism easily recognizable, and it can then be corrected. Astigmatism should be corrected incrementally for aperture, x-stig, and y-stig settings, as these all dependent on each other, and changes to one setting will thus affect all. Astigmatism correction should be conducted until the image under all settings appear to be dragged out evenly in all directions during the defocusing. Optimal alignments settings should be found at a magnification value larger than the magnification required for patterning by a great margin. Finding optimal alignment settings at 100-200 kx magnification was sufficient in this work.

B.5 Rotation and angle correction

The sample should first be located by moving the beam towards the the approximate location until one sees the metal pads, which are easily distinguished from their surroundings. Once the electron beam is over the substrate, prolonged viewing of the same location can cause unintentionally exposure of resist. A rule of thumb is to never move the beam over target areas intended for exposure.

A corner of the metal pad can be used to adjust the rotation tilt of the raster scan until the sample is approximately horizontal with respect to the screen.

Angle correction should then be conducted by choosing the two upper corners of a pad leading into the target area intended for exposure. This is to ensure the angle correction is done close to the target area, but not close enough to expose it. An illustration of suitable positions are seen in Figure B.3. The angle correction menu can be seen in Figure B.4a

B.6 Locating target area

The contact arm leading from the pad used for angle correction to the target area should then be located, and followed until the metal pad is not visible. Zoom in to approximately 5-6kx while doing focusing and contrast adjustments on the contact. The arm is then carefully followed while zooming, until the end is found without exposing any of the center. The beam should be placed exactly at one of the corners, as shown in Figure B.4b, before finding the best focus settings for approximately 8kx magnification. It is often not possible to obtain a sharp image due to the resist laying over it, and in these cases the best compromise should be used.

B.7 Position correction

Due software incompatibles between the *Hitachi S-4300SE* and *Raith ELPHY Plus* software, there exists a offset between the beam positions in the two programs. In other words, when the beam position in accurately placed on a corner in the *Hitachi S-4300SE* software, checking the beam position in the *Raith ELPHY Plus* software will reveal an offset in excess of 1 µm . As the stage movement alignment is done from the *Raith ELPHY Plus* software, this offset should be somewhat corrected beforehand, as this eases time required for stage movement alignment.

This can be done by using a combination of*fine three point adjustment* and *origin correction*. The menu for this, and the other menus used in this step are shown in Figure B.5. If this scan is set up for only one mark, it can be utilized to view points with a selected scan size. A scan size of 6 µm was found to be suitable. The position of the scan is configured in properties, under *Mark Procedure*.

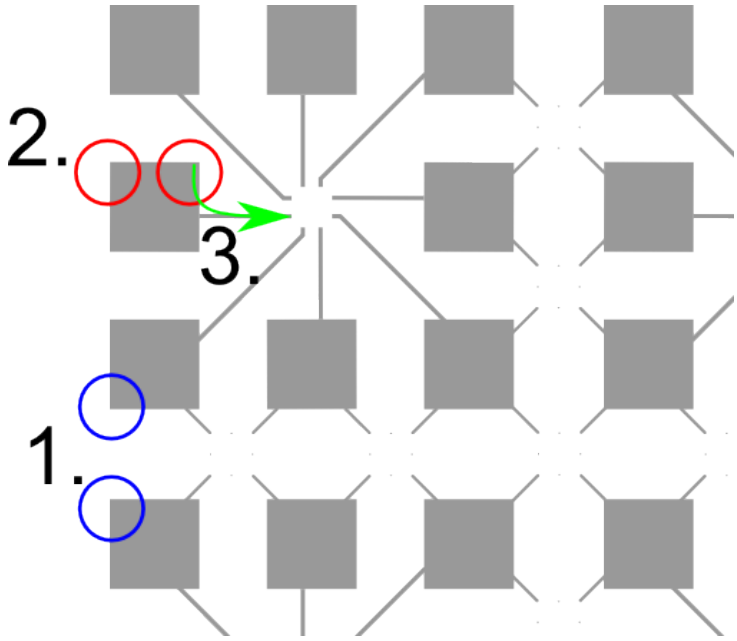
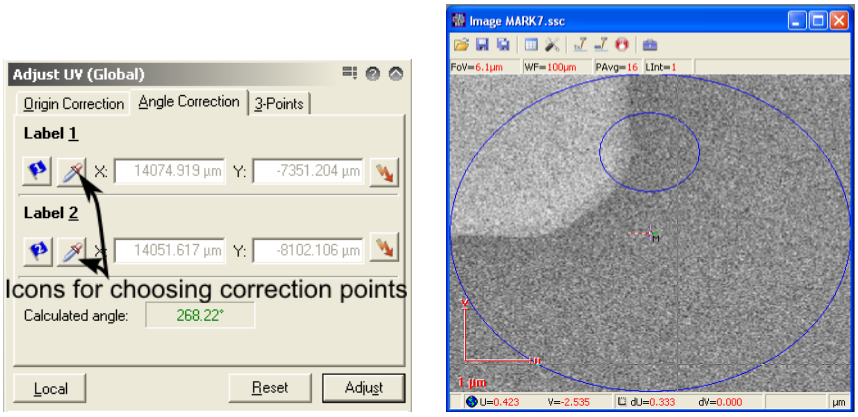


Figure B.3: Illustration demonstrating suitable positions for steps outlined in sections B.5 and B.6. 1. Suitable positions for correcting the rotation tilt of the raster scan. 2. Suitable locations for angle correction. 3. Suitable approach to locate target area.

After centering the beam position on a corner in the *Hitachi S-4300SE* software, do an origin correction so that the coordinate system in the *Raith ELPHY Plus* software is centered at this position. Doing a fine 3 point adjustment-scan at (0,0) will now reveal the offset. Measure the offset between the beam position in the scan and the corner of the contact arm. The measured distances is then input in the stage control, and one can then move the stage by relative movement to this position. A new origin correction is then made, and the position is checked by a *fine three point adjustment*- scan. As this is done prior to stage movement alignment, this stage movement is somewhat inaccurate, and generally two to three repetitions is required to center the *Raith ELPHY Plus* software beam position on the corner.



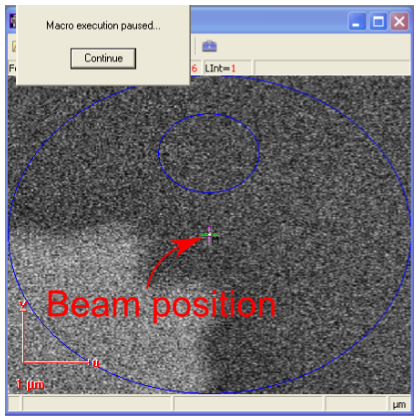
(a) (b)

Figure B.4: *(a)* Menu for doing angle correction. By clicking the pen icon under *label* the current position is chosen for angle correction.*(b)* Zoomed in view on a corner of a contact arm.

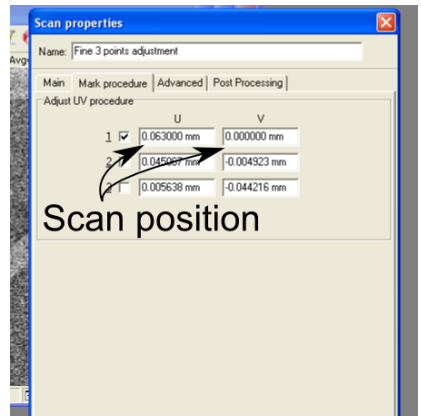
B.8 Stage movement alignment

Stage movement alignment (Manual field alignment) should then be commenced by entering the *000_field scan for any field* menu shown in Figure B.6a. This alignment works by moving the stage a distance corresponding to the edge of the chosen write field size, and then moving the beam inversely, meaning one should ideally end up in the same spot. For a 100 x 100 µm write field, this corresponds to moving 45 µm in both x - and y - directions. Any offset can then be corrected by dragging the cross indicating the beam position from its current position, to the desired position, as shown in figure B.6b. Alignment needs to be based on placing the markers at the same amount of gray contrast in the image, as the corner will generally appear somewhat unfocused due to the presence of resist. After doing this for all four corners in the write field, the software will calculate new zoom values for the sample coordinate system. These calculations are based on the off-sets from all the corners, and several repetitions are needed to attain optimal correction.

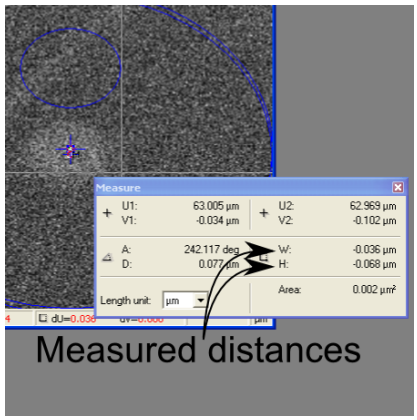
The correction is deemed to be optimal when the finished field scan suggests a correction scaling value of less than 10^{-4} for both U and V under the ZOOM settings in the *Align Writefield* menu shown in Figure B.6c. For this thesis the



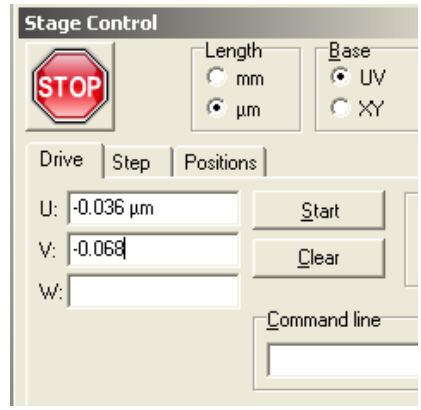
(a)



(b)



(c)



(d)

Figure B.5: Menus associated with postion correction(B.7. *(a)* Scan window for *fine three point adjustment*. *(b)* Menu for inputting position for *fine three point adjustment*. *(c)* Menu for beam position measurements. *(d)* Stage control drive menu.

optimal scan size for stage movement alignment was found to be 4 μm^2 .

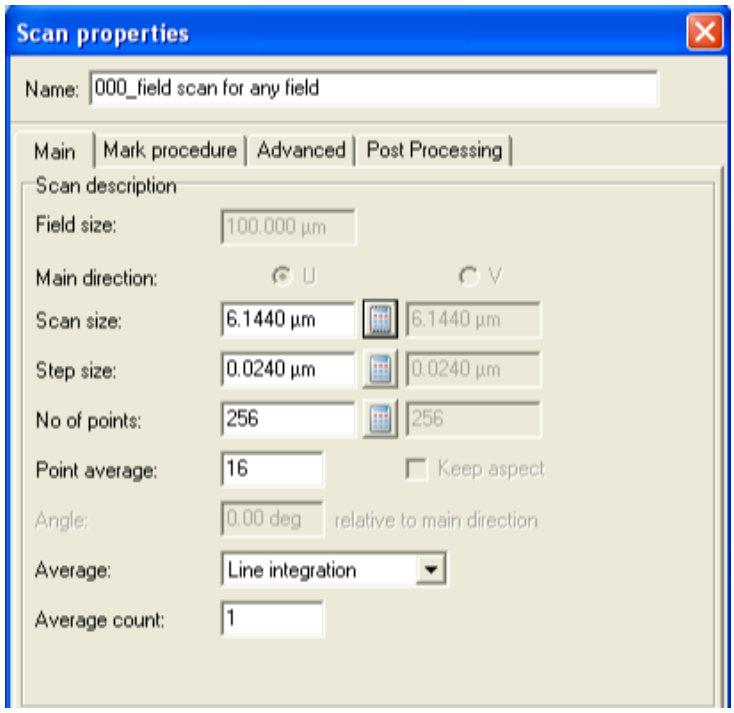
B.9 Write field alignment

Prior to write field alignment, the *Raith ELPHY Plus* coordinate system needs to be centered in target area. This is done be by moving the beam from the corner used from for stage movement alignment to the center via the same relative stage movement as utilized in sectionB.7, and do an origin correction.

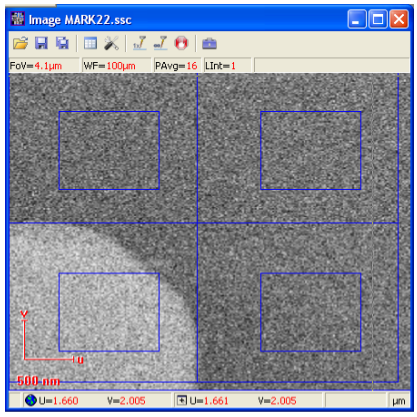
The digital mask should then be opened in the Raith ELPHY Plus software- By pressing edit, a schematic of the pattern is brought up. To conduct write field alignment, one needs to place three marks called *manual marks* in the software, as shown in Figure B.7a. This is done by making three squares, and then double-clicking them to edit their sizes and positions. For a 100 x 100 μm^2 write field size, a manual mark size of 4 x 4 μm^2 was found to be sufficient. Care should be taken to place the manual marks over the same corners as where used to give nanowire coordinates to minimize pattern offset. Once all marks for one write field has been made, the schematic is closed and saved.. The file is then dragged down on to the position list window. Properties is clicked to bring up the scan menu. To start write field alignment, *manual marks* is chosen from the roll down menu, and write field coordinates should be checked. These menus are shown in Figures B.7b and B.7c. Write field alignment can then be conducted by starting the scan. The procedure for correcting offset is identical as for stage movement alignment. The marker should be placed at the same amount of gray contrast, and the process repeated until the suggested correction scale value is less than 10^{-4}.

B.10 Exposure

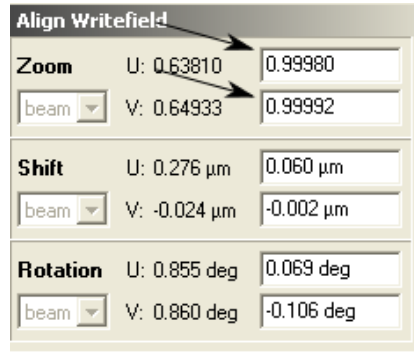
Exposure is initiated by opening the position list, and dragging the gds. file unto this window as shown in Figure B.8a. One then checks the properties by right clicking the pattern in the position list window. Correct exposure parameters should then be entered, and checked to give correct values as shown in Figure B.8b. Before starting exposure, one should also check the calculated exposure time. Unreasonable exposure time values will be an indication of a problem with the digital mask.



(a)

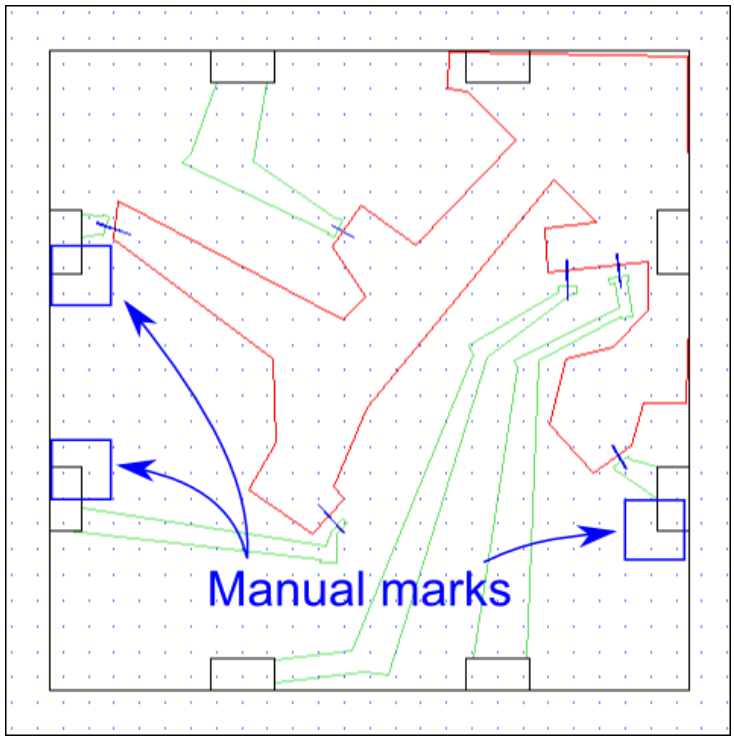


(b)

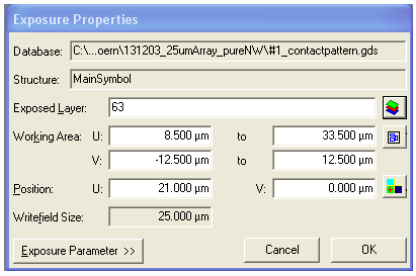


(c)

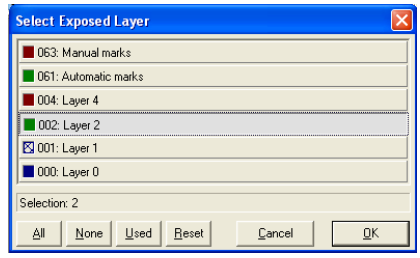
Figure B.6: *(a)* Menu for doing a manual field alignment. Scan size and step size both needs to be changed when changing scan field size. *(b)* The menu for seeing the calculated zoom values. Arrows indicate the zoom correction scaling values. *(c)* Demonstration of optimal beam placement relative corner.



(a)



(b)

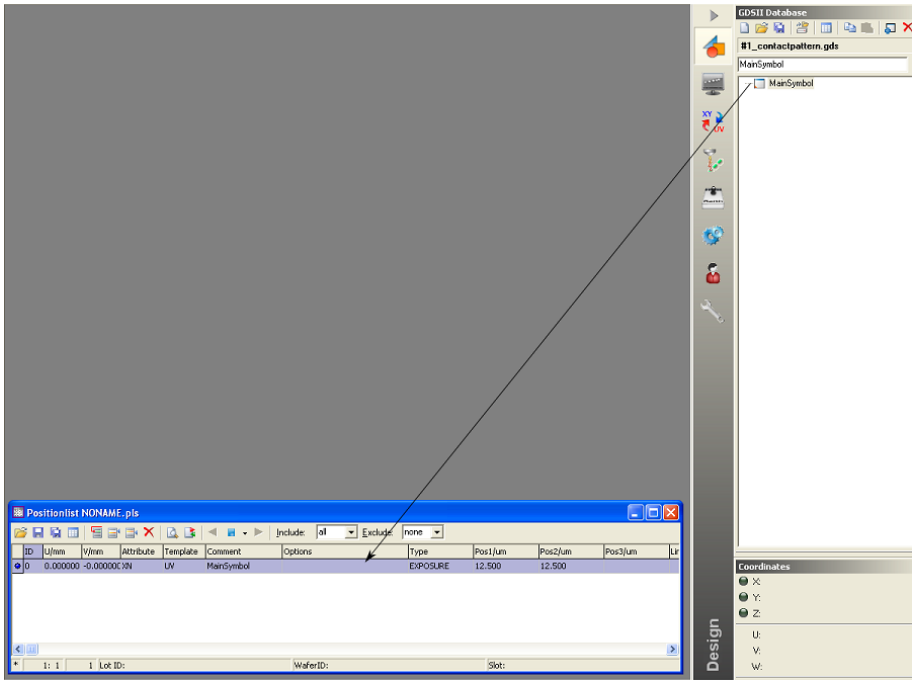


(c)

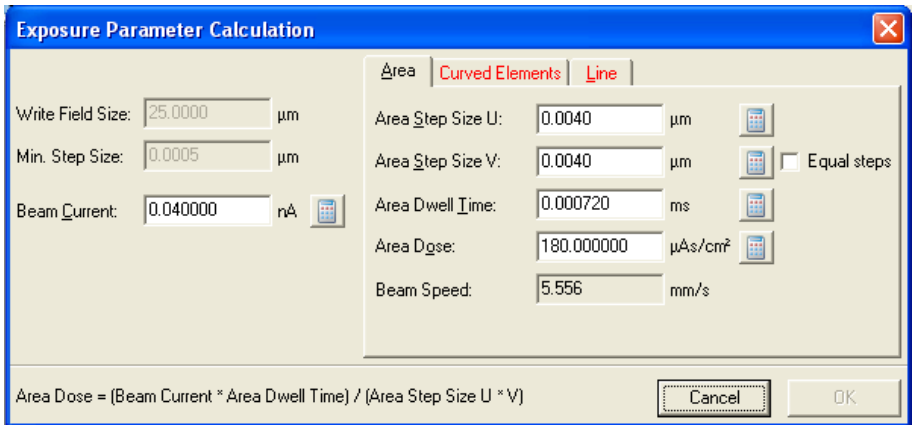
Figure B.7: *(a)* Schematic of the digital mask and manual marks in *Raith ELPHY Plus* software. *(b)* Exposure properties menu. *(c)* Select exposure layer menu.

B.11 Sample unloading

Once all exposure is finished, the beam should be moved back to the faraday cup, by using the predefined *Faraday cup_21052010* position. The acceleration voltage is turned off, the stage is moved to *Exchange position for load lock*, and the sample is unloaded.



(a)



(b)

Figure B.8: *(a)* Position list window. The arrow indicates the icon that should be dragged on to this window to commence write field alignment. *(b)* Menu for exposure parameters.

Appendix **C**

EBL procedure test

To test the new EBL procedure, an initial batch of nanowire devices were made. A total of 10 nanowires were contacted. Of these, six were contacted in two places, while the four others where contacted in four places to make 4-probe devices. Alignment points were chosen as close as possible to the 4-probe devices to attain maximum pattern accuracy for these, while the 2-probe devices were placed slightly further away to observe the effect of longer distance from alignment points on accuracy. One of the finalized samples are shown in figure C.1.

Inspection by optical microscope shows that all 10 nanowires were successfully contacted. For the four 4-probe devices with all alignment marks as close as possible, which in practice means within 50 μm of the device, no off-set was visible from the optical inspection. For 2-probe devices further away, off-sets of up to 0.5 μm could be observed. This trend is illustrated in figure C.2, which shows a comparison between the finished the devices and the digital mask used during EBL exposure.

The optical inspection was deemed sufficient to verify the accuracy of the deposited contacts, and this method was thus adopted for all subsequent EBL processes.

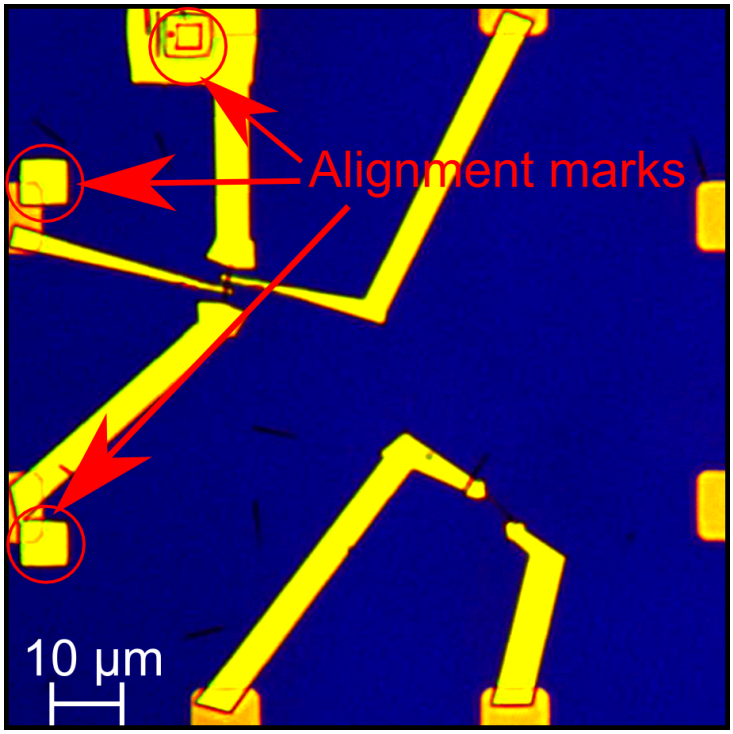
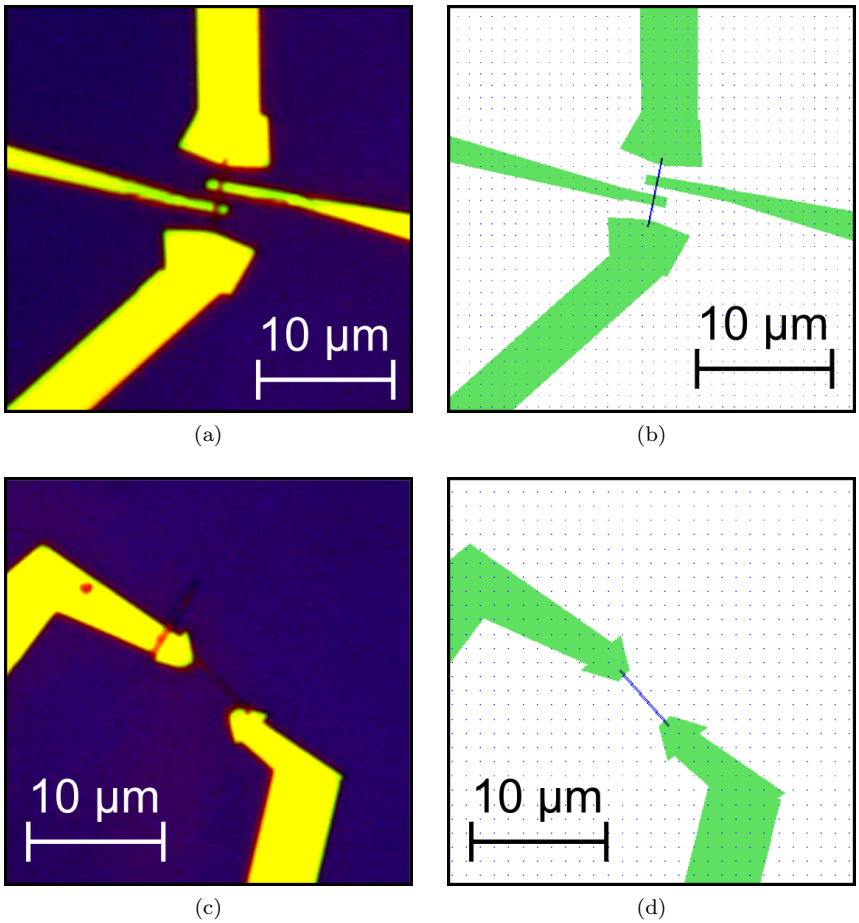


Figure C.1: Optical microscope image showing a finished 2- and 4-probe device. The alignment marks used for both determining nanowire coordinates and for write field alignment are indicated by red circles.



(a) (b)

(c) (d)

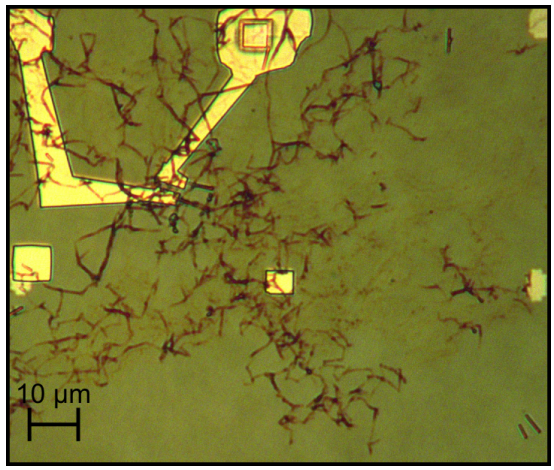
Figure C.2: Comparison between finished contacts and digital mask used for EBL exposure. *(a)* and *(b)* are optical microscope images, while *(c)* and *(d)* show the corresponding areas in the digital mask.

Appendix **D**

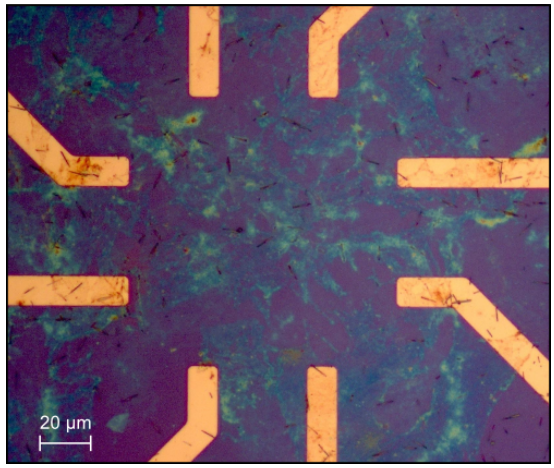
Graphene transfer results - Graphene Supermarket

Initially the graphene transfer process was tested on Si_3N_4 substrates with contacted nanowires. Optical inspection after removing scaffold PMMA showed the graphene to have poor quality. As seen in Figure D.1a, the graphene was found to be extensively wrinkled and curled up. Besides the wrinkles, there were no abrupt changes in contrast on the substrate. This indicates a poor visibility of single-layer graphene on Si_3N_4, as it is thought to be highly unlikely that the transfer should leave no single-layer graphene areas on the sample.

The transfer process was then tested on SiO_2 substrates with non-contacted nanowires, which were then observed in optical microscope. Figure D.1b shows one of the substrates following the transfer, and again the observed quality was very poor. The images indicate a large amount of PMMA remnants on the surface, even after extended periods of aceton immersion. A possible explanation is that the PMMA has been caught within wrinkles of graphene, effectively shielding the PMMA from dissolving in the aceton. The poor results from the graphene supplied from graphene supermarket is thought to be the result of inadequate application of scaffold PMMA. The PMMA was applied by spin coating on a 5 x 5 cm^2 Cu-foil. This rather large size inevitablly leads to some curling of the Cu-foil during handling, which is thought to lead to a non-uniform application of scaffold PMMA.



(a)



(b)

Figure D.1: Optical microscope images captured after transferring Graphene Supermarket graphene to a: *(a)* Si_3N_4-substrate. The graphene is seen to be extensively wrinkled, and lack of contrast change makes it hard to determine whether single-layer graphene is present. *(b)* SiO_2 substrate. The lighter areas indicate remnants of PMMA caught in curled up graphene.